S905Y4

Datasheet

Revision: 0.7

Release Date: 2022-09-08

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Revision History

Issue 0.7 (2022-09-08)

This is the 0.7 release.

Compared to last version, the following topics are changed.

Section	Change Description
3	Updated the spec version of DS/HS modes for SDSDSC/ SDHC/SDXC card and SDIO interface.

Issue 0.6 (2022-05-23)

This is the 0.6 release.

Compared to last version, the following topics are changed.

Section	Change Description
3	Updated the size of One-Time-Programming memory.

Issue 0.5 (2021-12-17)

This is the 0.5 release.

Compared to last version, the following topics are changed.

Section	Change Description
7.8.2	Updated the description of GPIOD_x Multi-Function Pin.

Issue 0.4 (2021-11-23)

This is the 0.4 release.

Compared to last version, the following topics are changed.

Section	Change Description
Remove unsupported interfaces	Deleted PCIe and USB3.0.
14.3	Added the net length of S905Y4.
3	The size of One-Time-Programming memory has been increased from 4k bits to 32k bits.
4.1 and 4.2	Updated C7, A14, B13, B14, C14, E12, E13, F13, E17, E18, N9 and P20 balls' net name.

Issue 0.3 (2021-09-10)

This is the 0.3 release.

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Compared to last version, the following topics are changed.

Section	Change Description
13.2	Deleted RGMII.

Issue 0.2 (2021-06-22)

This is the 0.2 release.

Compared to last version, the following topics are changed.

Section	Change Description
5.5.1	Updated GPIO specifications.
6	Updated mechanical dimensions.
3	Updated DVB-C demodulators description.
5.10	Updated recommended power on sequence.

Issue 0.1 (2021-04-08)

This is the preliminary 0.1 release.

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1 About This Document

This document is applicable to S905Y4 SoC series, please contact your Amlogic sales representative for more detail.

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2 General Description

S905Y4 is an advanced application processor designed for hybrid OTT/ IP Set Top Box(STB) and high-end media box applications. It integrates a powerful CPU/GPU subsystem, a secured 4K video CODEC engine and a best-in-class HDR image processing pipeline with all major peripherals to form the ultimate low power multimedia AP.

The main system CPU is a quad-core ARM Cortex-A35 CPU with unified L2 cache to improve system performance. In addition, the Cortex-A35 CPU includes the NEON SIMD co-processor to improve software media processing capability.

The graphic subsystem consists of two graphic engines and a flexible video/graphic output pipeline. The ARM G31 MP2 GPU handles all OpenGL ES 3.2 Vulkan 1.1 and OpenCL 2.0 graphic programs, while the 2.5D graphics processor handles additional scaling, alpha, rotation and color space conversion operations. Together, the CPU and GPU handle all operating system, networking, user-interface and gaming related tasks. The video output pipeline includes Dolby Vision^{Optional}, HDR10+, HDR10 and HLG processing, BT.709/BT.2020/BT.2100 processing, motion adaptive edge enhancing de-interlacing, flexible pro- grammable scaler, and many picture enhancement filters before passing the enhanced image to the video output ports.

Amlogic Video Engine (AVE-10) offloads the Cortex-A35 CPUs from all video CODEC processing. It includes dedicated hardware video decoder and SW H.264/VP8 encoders. AVE-10 is capable of decoding 4Kx2K resolution video at 60fps with complete Trusted Video Path (TVP) for se- cure applications and supports full formats including MPEG-1/2/4, VC-1/WMV, AVS, AVS+, MJPEG streams, AV1, H.264, H265-10 and also JPEG pictures with no size limitation.

The processor integrates all standard audio/video input/output interfaces including a HDMI 2.1a transmitter with 3D, Dynamic HDR(w/EMP), CEC and HDCP 2.2/2.3, ALLM (Auto Low Latency Mode) support, multiple TDM, PCM, I2S and SPDIF digital audio input/output interfaces, and 2 channel far-field PDM digital microphone (DMIC) inputs. It also has build-in Voice Activity Detection(VAD)module for ultra-low power operations during system standby.

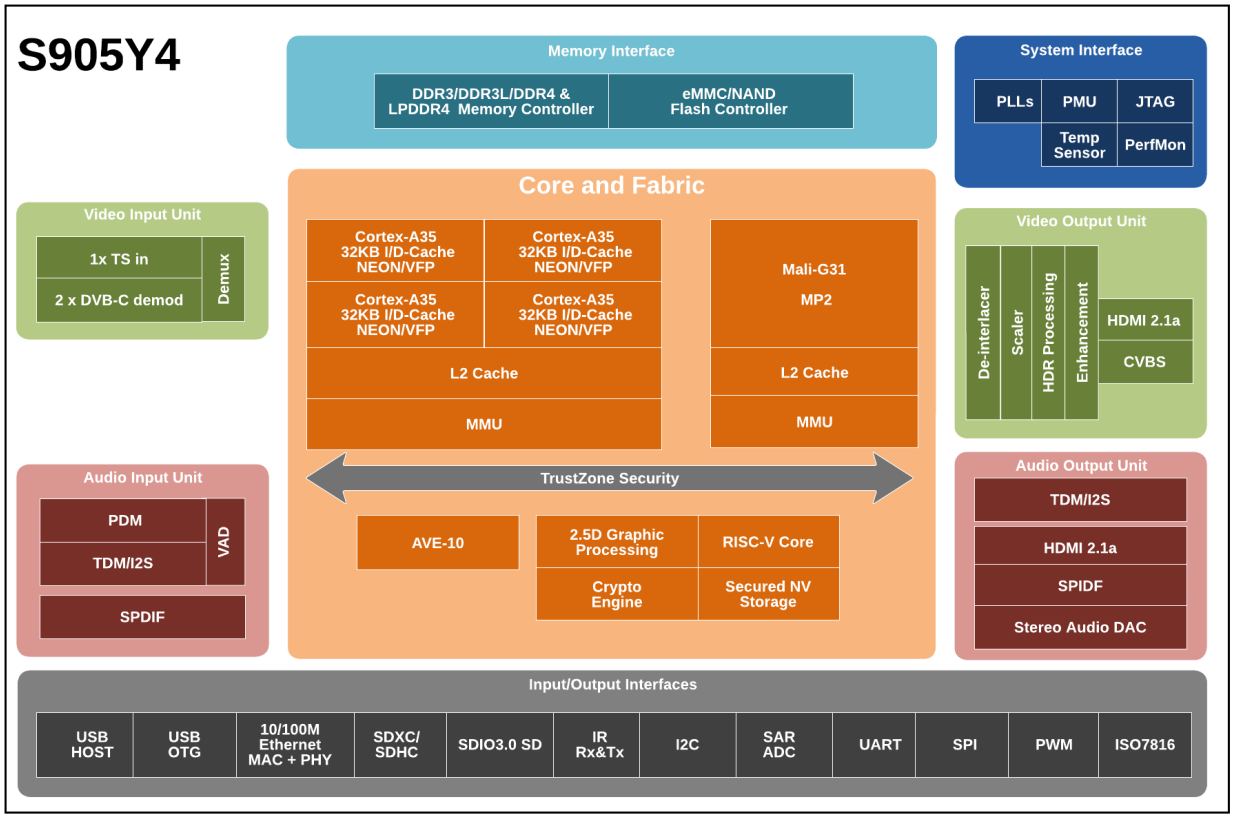
It also integrates a set of functional blocks for digital TV broadcasting streams. The built-in demultiplexer can process the TV streams from the serial transport stream input interface, which can connect to external tuner/demodulator.

The processor has rich advanced network and peripheral interfaces, including a 10/100M Ethernet MAC with and PHY interface, a set of multi- PHY for USB2, and multiple SDIO/SD card controllers, UART, I2C, high speed SPI and PWMs.

Standard development environment utilizing GNU/GCC Android tool chain is supported. Please contact your AMLOGIC sales representative for more information.

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3 Features Summary



CPU Sub-system

- Quad core ARM Cortex-A35 CPU
- ARMv8-A architecture with Neon and Crypto extensions
- 8-stage in-order full dual issue pipeline
- Unified system L2 cache
- Build-in RISC-V core for system control processing
- Advanced TrustZone security system
- Application based traffic optimization using internal QoS-based switching fabrics

3D Graphics Processing Unit

- ARM G31 MP2 GPU
- 4-wide warps, dual texture pipe, 2 x 4 wide execution engines (EE)
- Concurrent multi-core processing
- OpenGL ES 3.2, Vulkan 1.1 and OpenCL 2.0 support

2.5D Graphics Processor

- Fast bitblt engine with dual inputs and single output
- Programmable raster operations (ROP)
- Programmable polyphase scaling filter
- Supports multiple video formats 4:2:0, 4:2:2 and 4:4:4 and multiple pixel formats (8/16/24/32 bits graphics layer)

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- Fast color space conversion
- Advanced anti-flickering filter

Crypto Engine

- AES/ block cipher with 128/256 bits keys, standard 16 bytes block size and streaming ECB, CBC and CTR modes
- TDES block cipher with ECB and CBC modes supporting 64 bits key for DES and 192 bits key for 3DES
- RSA block cipher with 4K bits keys
- Hardware crypto key-ladder operation and DVB-CSA for transport stream encryption
- Built-in hardware True Random Number Generator (TRNG), CRC and SHA-1/ SHA-2/HMAC SHA engine

Video/Picture CODEC

- Amlogic Video Engine (AVE) with dedicated hardware decoders and SW H.264/ VP8 encoders
- Support multi-video decoder up to 4x1080P@60fps
- Supports multiple “secured” video decoding sessions and simultaneous decoding and encoding
- Video/Picture Decoding
  - AV1 MP-10@L5.1 up to 4Kx2K@60fps
  - VP9 Profile-2 up to 4Kx2K@60fps
  - H.265 HEVC MP-10@L5.1 up to 4Kx2K@60fps
  - AVS2-P2 Profile up to 4Kx2K@60fps
  - H.264 AVC HP@L5.1 up to 4Kx2K@30fps
  - MPEG-4 ASP@L5 up to 1080P@60fps (ISO-14496)
  - WMV/VC-1 SP/MP/AP up to 1080P@60fps
  - AVS-P16(AVS+) /AVS-P2 JiZhun Profile up to 1080P@60fps
  - MPEG-2 MP/HL up to 1080P@60fps (ISO-13818)
  - MPEG-1 MP/HL up to 1080P@60fps (ISO-11172)
  - Multiple language and multiple format sub-title video support
  - MJPEG and JPEG unlimited pixel resolution decoding (ISO/IEC-10918)
  - Supports JPEG thumbnail, scaling, rotation and transition effects
  - Supports *.mkv,*.wmv,*.mpg, *.mpeg, *.dat, *.avi, *.mov, *.iso, *.mp4 and *.jpg file formats

8th Generation Advanced Amlogic TruLife Image Engine

- Supports Dolby Vision[optional], HDR10+, HDR10, HLG HDR processing
- Motion compensated noise reduction and 3D digital noise reduction for random noise
- Block noise, mosquito noise, spatial noise, contour noise reduction
- Motion compensated and motion adaptive de-interlacer
- Edge interpolation with low angle protection and processing
- 3:2/2:2 pulldown and Video on Film (VOF) detection and processing
- Smart sharpness with SuperScaler technology including de-contouring, de-ring, LTI, CTI, de-jaggy, peaking
- Dynamic non-Linear contrast enhancement
- All dimension multiple regions smart color management including blue/green extension, flesh-tone correction, wider gamut for video

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- 2 video planes and 3 graphics planes hardware composer
- Independent HDR re-mapping of video and graphic layer

Video Input/Output Interface

- Built-in HDMI 2.1a transmitter including both controller and PHY supporting CEC, Dynamic HDR and HDCP 2.2/2.3, 4Kx2K@60 max resolution output
- CVBS 480i/576i standard definition output
- Supports all standard SD/HD/FHD video output formats: 480i/p, 576i/p, 720p, 1080i/p and 4Kx2K

Audio Decoder and Input/Output

- Supports MP3, AAC, WMA, RM, FLAC, Dolby Audio[Optional], DTS[Optional] and programmable with 7.1/5.1 down-mixing
- Low-power VAD
- Built-in serial digital audio IEC958 input/output, SPDIF input/output and PCM input/output, SPDIF supports 192KHz 16/24/32bit stereo
- TDM/PCM/I2S audio interface supporting 2-channel input and 8-channel (7.1) output
- Digital microphone PDM input with programmable CIC, LPF, HPF, support up to 4 DMICs
- Built-in stereo audio DAC
- Supports concurrent dual audio stereo channel output with combination of analog+PCM or I2S +PCM

Memory and Storage Interface

- 32-bit DRAM memory interface with dual ranks and max 4GB total address space
- Compatible with JEDEC standard DDR3-2133 / DDR3L-2133 / DDR4-2666 / LPDDR4-2666 SDRAM
- Supports SLC NAND Flash with 60-bit ECC, compatible to Toshiba toggle mode in addition to ONFI 2.2
- SDSC/SDHC/SDXC card and SDIO interface with 1-bit and 4-bit data bus width supporting spec version 2.x/3.x DS/HS modes up to UHS-I SDR104
- eMMC and MMC card interface with 1/4/8-bit data bus width fully supporting spec version 5.0 HS400
- Built-in 8k bits One-Time-Programming memory for key storage

Network

- Integrated IEEE 802.3 10/100 Ethernet MAC controller and 10/100M PHY interface
- WiFi/IEEE802.11, Bluetooth supporting via SDIO/USB/UART/PCM
- Network interface optimized for mixed WIFI and BT traffic

Digital Television Interface

- 2 x DVB-C demodulators[Optional], compatible with DVB-C EN300429 and ITU-T J.83 annex A/C
- 1 serial transport stream (TS) input interface with built-in demux processor for connecting to external digital TV tuner/demodulator
- Built-in PWM, I2C and SPI interfaces to control tuner and demodulator
- Integrated ISO 7816 smart card controller

Integrated I/O Controllers and Interfaces

- Dual USB 2.0 high-speed USB I/O, one USB Host and one USB OTG
- Multiple PWM, UART, I2C and SPI interface with slave select

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- Programmable IR remote input/output controllers
- Built-in 10bit SAR ADC with 4 input channels
- A set of General Purpose IOs with built-in pull up and pull down

System, Peripherals and Misc. Interfaces

- Integrated general purpose timers, counters, DMA controllers
- 24 MHz crystal input
- Embedded debug interface using ICE/JTAG
- Integrated Power On Reset(POR) module

Power Management

- Multiple internal power domains controlled by software
- Multiple sleep modes for CPU, system, DRAM, etc.
- Multiple internal PLLs for DVFS operation
- Multi-voltage I/O design for 1.8V and 3.3V
- Power management auxiliary processor can communicate with an external PMIC

Security

- Trustzone based Trusted Execution Environment (TEE)
- Secured boot, encrypted OTP, encrypted DRAM with memory integrity checker, hardware key ladder and internal control buses and storage
- Separated secure/non-secure Entropy true RNG
- Pre-region/ID memory security control and electric fence
- Hardware based Trusted Video Path (TVP) , video watermarking and secured contents (needs SecureOS software)
- Secured IO and secured clock

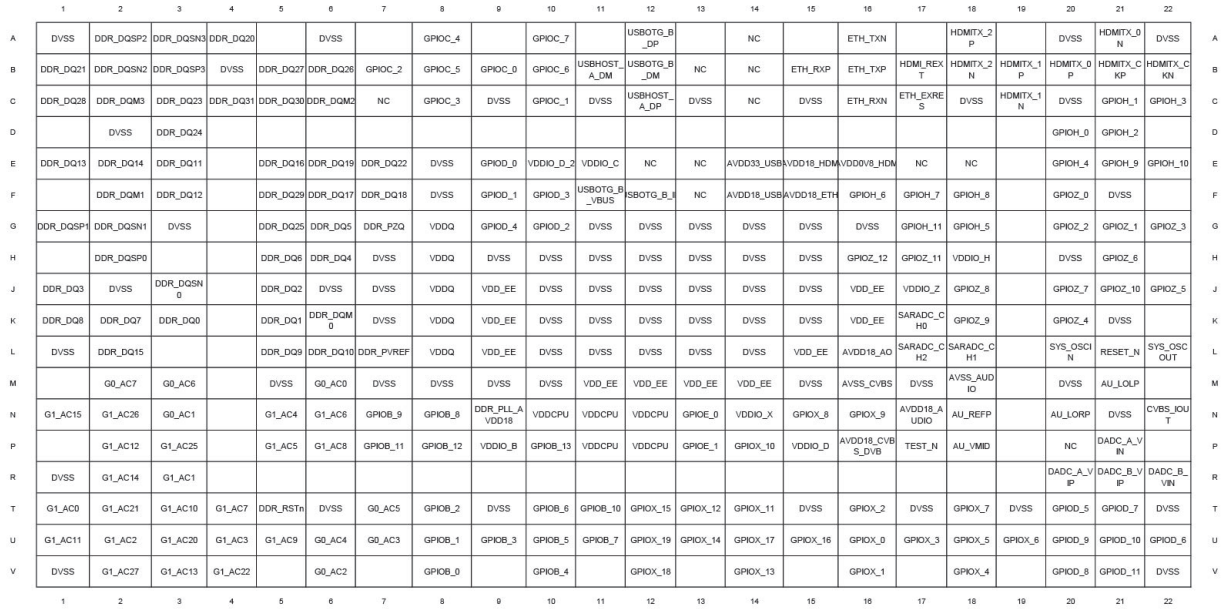
Package

- WBBGA, 11mm x 13.3mm, 0.6mm ball pitch, RoHS compliant

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4 Pinout Specification

4.1 Pin-Out Diagram (top view)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	DVSS	DDR_DQSP2	DDR_DQSN3	DDR_DQ20		DVSS		GPIOC_4		GPIOC_7		USBOTG_B_DP		NC		ETH_TXN		HDMITX_2P		DVSS	HDMITX_0N	DVSS	A
B	DDR_DQ21	DDR_DQSN2	DDR_DQSP3	DVSS	DDR_DQ27	DDR_DQ26	GPIOC_2	GPIOC_5	GPIOC_0	GPIOC_6	USBHOST_A_DM	USBOTG_B_DM	NC	NC	ETH_RXP	ETH_TXP	HDMI_REXT	HDMITX_2N	HDMITX_1P	HDMITX_0P	HDMITX_CKP	HDMITX_CKN	B
C	DDR_DQ28	DDR_DQM3	DDR_DQ23	DDR_DQ31	DDR_DQ30	DDR_DQM2	NC	GPIOC_3	DVSS	GPIOC_1	DVSS	USBHOST_A_DP	DVSS	NC	DVSS	ETH_RXN	ETH_EXRES	DVSS	HDMITX_1N	DVSS	GPIOH_1	GPIOH_3	C
D		DVSS	DDR_DQ24																	GPIOH_0	GPIOH_2		D
E	DDR_DQ13	DDR_DQ14	DDR_DQ11		DDR_DQ16	DDR_DQ19	DDR_DQ22	DVSS	GPIOD_0	VDDIO_D_2	VDDIO_C	NC	NC	AVDD33_USB	AVDD18_HDM	AVDD0V8_HDM	NC	NC		GPIOH_4	GPIOH_9	GPIOH_10	E
F		DDR_DQM1	DDR_DQ12		DDR_DQ29	DDR_DQ17	DDR_DQ18	DVSS	GPIOD_1	GPIOD_3	USBOTG_B_VBUS	USBOTG_B_I	NC	AVDD18_USB	AVDD18_ETH	GPIOH_6	GPIOH_7	GPIOH_8		GPIOZ_0	DVSS		F
G	DDR_DQSP1	DDR_DQSN1	DVSS		DDR_DQ25	DDR_DQ5	DDR_PZQ	VDDQ	GPIOD_4	GPIOD_2	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	GPIOH_11	GPIOH_5		GPIOZ_2	GPIOZ_1	GPIOZ_3	G
H		DDR_DQSP0			DDR_DQ6	DDR_DQ4	DVSS	VDDQ	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	GPIOZ_12	GPIOZ_11	VDDIO_H		DVSS	GPIOZ_6		H
J	DDR_DQ3	DVSS	DDR_DQSN0		DDR_DQ2	DVSS	DVSS	VDDQ	VDD_EE	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	VDD_EE	VDDIO_Z	GPIOZ_8		GPIOZ_7	GPIOZ_10	GPIOZ_5	J
K	DDR_DQ8	DDR_DQ7	DDR_DQ0		DDR_DQ1	DDR_DQM0	DVSS	VDDQ	VDD_EE	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	VDD_EE	SARADC_CH0	GPIOZ_9		GPIOZ_4	DVSS		K
L	DVSS	DDR_DQ15			DDR_DQ9	DDR_DQ10	DDR_PVREF	VDDQ	VDD_EE	DVSS	DVSS	DVSS	DVSS	DVSS	VDD_EE	AVDD18_AO	SARADC_CH2	SARADC_CH1		SYS_OSCIN	RESET_N	SYS_OSCOUT	L
M		G0_AC7	G0_AC6		DVSS	G0_AC0	DVSS	DVSS	DVSS	DVSS	VDD_EE	VDD_EE	VDD_EE	VDD_EE	DVSS	AVSS_CVBS	DVSS	AVSS_AUDIO		DVSS	AU_LOLP		M
N	G1_AC15	G1_AC26	G0_AC1		G1_AC4	G1_AC6	GPIOB_9	GPIOB_8	DDR_PLL_AVDD18	VDDCPU	VDDCPU	VDDCPU	GPIOE_0	VDDIO_X	GPIOX_8	GPIOX_9	AVDD18_AUDIO	AU_REFP		AU_LORP	DVSS	CVBS_IOUT	N
P		G1_AC12	G1_AC25		G1_AC5	G1_AC8	GPIOB_11	GPIOB_12	VDDIO_B	GPIOB_13	VDDCPU	VDDCPU	GPIOE_1	GPIOX_10	VDDIO_D	AVDD18_CVBS_DVB	TEST_N	AU_VMID		NC	DADC_A_VIN		P
R	DVSS	G1_AC14	G1_AC1																	DADC_A_VIP	DADC_B_VIP	DADC_B_VIN	R
T	G1_AC0	G1_AC21	G1_AC10	G1_AC7	DDR_RSTn	DVSS	G0_AC5	GPIOB_2	DVSS	GPIOB_6	GPIOB_10	GPIOX_15	GPIOX_12	GPIOX_11	DVSS	GPIOX_2	DVSS	GPIOX_7	DVSS	GPIOD_5	GPIOD_7	DVSS	T
U	G1_AC11	G1_AC2	G1_AC20	G1_AC3	G1_AC9	G0_AC4	G0_AC3	GPIOB_1	GPIOB_3	GPIOB_5	GPIOB_7	GPIOX_19	GPIOX_14	GPIOX_17	GPIOX_16	GPIOX_0	GPIOX_3	GPIOX_5	GPIOX_6	GPIOD_9	GPIOD_10	GPIOD_6	U
V	DVSS	G1_AC27	G1_AC13	G1_AC22		G0_AC2		GPIOB_0		GPIOB_4		GPIOX_18		GPIOX_13		GPIOX_1		GPIOX_4		GPIOD_8	GPIOD_11	DVSS	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

4.2 Pin Order

BALL #	NET NAME
A1	DVSS
A2	DDR_DQSP2
A3	DDR_DQSN3
A4	DDR_DQ20
A6	DVSS
A8	GPIOC_4
A10	GPIOC_7
A12	USBOTG_B_DP
A14	NC
A16	ETH_TXN
A18	HDMITX_2P
A20	DVSS
A21	HDMITX_0N
A22	DVSS
B1	DDR_DQ21
B2	DDR_DQSN2
B3	DDR_DQSP3
B4	DVSS

BALL #	NET NAME
B5	DDR_DQ27
B6	DDR_DQ26
B7	GPIOC_2
B8	GPIOC_5
B9	GPIOC_0
B10	GPIOC_6
B11	USBHOST_A_DM
B12	USBOTG_B_DM
B13	NC
B14	NC
B15	ETH_RXP
B16	ETH_TXP
B17	HDMI_REXT
B18	HDMITX_2N
B19	HDMITX_1P
B20	HDMITX_0P
B21	HDMITX_CKP

BALL #	NET NAME
B22	HDMITX_CKN
C1	DDR_DQ28
C2	DDR_DQM3
C3	DDR_DQ23
C4	DDR_DQ31
C5	DDR_DQ30
C6	DDR_DQM2
C7	NC
C8	GPIOC_3
C9	DVSS
C10	GPIOC_1
C11	DVSS
C12	USBHOST_A_DP
C13	DVSS
C14	NC
C15	DVSS
C16	ETH_RXN
C17	ETH_EXRES

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BALL #	NET NAME
C18	DVSS
C19	HDMITX_1N
C20	DVSS
C21	GPIOH_1
C22	GPIOH_3
D2	DVSS
D3	DDR_DQ24
D20	GPIOH_0
D21	GPIOH_2
E1	DDR_DQ13
E2	DDR_DQ14
E3	DDR_DQ11
E5	DDR_DQ16
E6	DDR_DQ19
E7	DDR_DQ22
E8	DVSS
E9	GPIOD_0
E10	VDDIO_D_2
E11	VDDIO_C
E12	NC
E13	NC
E14	AVDD33_USB
E15	AVDD18_HDMI
E16	AVDD0V8_ HDMI
E17	NC
E18	NC
E20	GPIOH_4
E21	GPIOH_9
E22	GPIOH_10
F2	DDR_DQM1
F3	DDR_DQ12
F5	DDR_DQ29
F6	DDR_DQ17
F7	DDR_DQ18
F8	DVSS
F9	GPIOD_1

BALL #	NET NAME
F10	GPIOD_3
F11	USBOTG_B_ VBUS
F12	USBOTG_B_ID
F13	NC
F14	AVDD18_USB
F15	AVDD18_ETH
F16	GPIOH_6
F17	GPIOH_7
F18	GPIOH_8
F20	GPIOZ_0
F21	DVSS
G1	DDR_DQSP1
G2	DDR_DQSN1
G3	DVSS
G5	DDR_DQ25
G6	DDR_DQ5
G7	DDR_PZQ
G8	VDDQ
G9	GPIOD_4
G10	GPIOD_2
G11	DVSS
G12	DVSS
G13	DVSS
G14	DVSS
G15	DVSS
G16	DVSS
G17	GPIOH_11
G18	GPIOH_5
G20	GPIOZ_2
G21	GPIOZ_1
G22	GPIOZ_3
H2	DDR_DQSP0
H5	DDR_DQ6
H6	DDR_DQ4
H7	DVSS
H8	VDDQ

BALL #	NET NAME
H9	DVSS
H10	DVSS
H11	DVSS
H12	DVSS
H13	DVSS
H14	DVSS
H15	DVSS
H16	GPIOZ_12
H17	GPIOZ_11
H18	VDDIO_H
H20	DVSS
H21	GPIOZ_6
J1	DDR_DQ3
J2	DVSS
J3	DDR_DQSN0
J5	DDR_DQ2
J6	DVSS
J7	DVSS
J8	VDDQ
J9	VDD_EE
J10	DVSS
J11	DVSS
J12	DVSS
J13	DVSS
J14	DVSS
J15	DVSS
J16	VDD_EE
J17	VDDIO_Z
J18	GPIOZ_8
J20	GPIOZ_7
J21	GPIOZ_10
J22	GPIOZ_5
K1	DDR_DQ8
K2	DDR_DQ7
K3	DDR_DQ0
K5	DDR_DQ1
K6	DDR_DQM0

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BALL #	NET NAME
K7	DVSS
K8	VDDQ
K9	VDD_EE
K10	DVSS
K11	DVSS
K12	DVSS
K13	DVSS
K14	DVSS
K15	DVSS
K16	VDD_EE
K17	SARADC_CH0
K18	GPIOZ_9
K20	GPIOZ_4
K21	DVSS
L1	DVSS
L2	DDR_DQ15
L5	DDR_DQ9
L6	DDR_DQ10
L7	DDR_PVREF
L8	VDDQ
L9	VDD_EE
L10	DVSS
L11	DVSS
L12	DVSS
L13	DVSS
L14	DVSS
L15	VDD_EE
L16	AVDD18_AO
L17	SARADC_CH2
L18	SARADC_CH1
L20	SYS_OSCIN
L21	RESET_N
L22	SYS_OSCOUT
M2	G0_AC7
M3	G0_AC6
M5	DVSS
M6	G0_AC0

BALL #	NET NAME
M7	DVSS
M8	DVSS
M9	DVSS
M10	DVSS
M11	VDD_EE
M12	VDD_EE
M13	VDD_EE
M14	VDD_EE
M15	DVSS
M16	AVSS_CVBS
M17	DVSS
M18	AVSS_AUDIO
M20	DVSS
M21	AU_LOLP
N1	G1_AC15
N2	G1_AC26
N3	G0_AC1
N5	G1_AC4
N6	G1_AC6
N7	GPIOB_9
N8	GPIOB_8
N9	DDR_PLL_ AVDD18
N10	VDDCPU
N11	VDDCPU
N12	VDDCPU
N13	GPIOE_0
N14	VDDIO_X
N15	GPIOX_8
N16	GPIOX_9
N17	AVDD18_ AUDIO
N18	AU_REFP
N20	AU_LORP
N21	DVSS
N22	CVBS_IOUT
P2	G1_AC12

BALL #	NET NAME
P3	G1_AC25
P5	G1_AC5
P6	G1_AC8
P7	GPIOB_11
P8	GPIOB_12
P9	VDDIO_B
P10	GPIOB_13
P11	VDDCPU
P12	VDDCPU
P13	GPIOE_1
P14	GPIOX_10
P15	VDDIO_D
P16	AVDD18_ CVBS_DVB
P17	TEST_N
P18	AU_VMID
P20	NC
P21	DADC_A_VIN
R1	DVSS
R2	G1_AC14
R3	G1_AC1
R20	DADC_A_VIP
R21	DADC_B_VIP
R22	DADC_B_VIN
T1	G1_AC0
T2	G1_AC21
T3	G1_AC10
T4	G1_AC7
T5	DDR_RSTn
T6	DVSS
T7	G0_AC5
T8	GPIOB_2
T9	DVSS
T10	GPIOB_6
T11	GPIOB_10
T12	GPIOX_15

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BALL #	NET NAME
T13	GPIOX_12
T14	GPIOX_11
T15	DVSS
T16	GPIOX_2
T17	DVSS
T18	GPIOX_7
T19	DVSS
T20	GPIOD_5
T21	GPIOD_7
T22	DVSS
U1	G1_AC11
U2	G1_AC2
U3	G1_AC20
U4	G1_AC3
U5	G1_AC9
U6	G0_AC4
U7	G0_AC3

BALL #	NET NAME
U8	GPIOB_1
U9	GPIOB_3
U10	GPIOB_5
U11	GPIOB_7
U12	GPIOX_19
U13	GPIOX_14
U14	GPIOX_17
U15	GPIOX_16
U16	GPIOX_0
U17	GPIOX_3
U18	GPIOX_5
U19	GPIOX_6
U20	GPIOD_9
U21	GPIOD_10
U22	GPIOD_6
V1	DVSS

BALL #	NET NAME
V2	G1_AC27
V3	G1_AC13
V4	G1_AC22
V6	G0_AC2
V8	GPIOB_0
V10	GPIOB_4
V12	GPIOX_18
V14	GPIOX_13
V16	GPIOX_1
V18	GPIOX_4
V20	GPIOD_8
V21	GPIOD_11
V22	DVSS

4.3 Pin Description

The SoC application processor pin assignment is described in the following table.

Net Name	Type	Default Pull UP/ DN	Description	Power Domain	If Unused
GPIOZ-Refer to Table 4-1 for functional multiplex information.					
GPIOZ_0	DIO	Up	General purpose input/output bank Z signal 0	VDDIO_Z	NC
GPIOZ_1	DIO	Up	General purpose input/output bank Z signal 1	VDDIO_Z	NC
GPIOZ_2	DIO	DWN	General purpose input/output bank Z signal 2	VDDIO_Z	NC
GPIOZ_3	DIO	Up	General purpose input/output bank Z signal 3	VDDIO_Z	NC
GPIOZ_4	DIO	DWN	General purpose input/output bank Z signal 4	VDDIO_Z	NC
GPIOZ_5	DIO	Up	General purpose input/output bank Z signal 5	VDDIO_Z	NC
GPIOZ_6	DIO	DWN	General purpose input/output bank Z signal 6	VDDIO_Z	NC
GPIOZ_7	DIO	DWN	General purpose input/output bank Z signal 7	VDDIO_Z	NC
GPIOZ_8	DIO	Up	General purpose input/output bank Z signal 8	VDDIO_Z	NC
GPIOZ_9	DIO	Up	General purpose input/output bank Z signal 9	VDDIO_Z	NC
GPIOZ_10	DIO	Up	General purpose input/output bank Z signal 10	VDDIO_Z	NC
GPIOZ_11	DIO	DWN	General purpose input/output bank Z signal 11	VDDIO_Z	NC

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Net Name	Type	Default Pull UP/ DN	Description	Power Domain	If Unused
GPIOZ_12	DIO	DWN	General purpose input/output bank Z signal 12	VDDIO_Z	NC
GPIOB-Refer to Table 4-2 for functional multiplex information.					
GPIOB_0	DIO	Up	General purpose input/output bank GPIOB signal 0	VDDIO_B	NC
GPIOB_1	DIO	Up	General purpose input/output bank GPIOB signal 1	VDDIO_B	NC
GPIOB_2	DIO	Up	General purpose input/output bank GPIOB signal 2	VDDIO_B	NC
GPIOB_3	DIO	Up	General purpose input/output bank GPIOB signal 3	VDDIO_B	NC
GPIOB_4	DIO	Up	General purpose input/output bank GPIOB signal 4	VDDIO_B	NC
GPIOB_5	DIO	Up	General purpose input/output bank GPIOB signal 5	VDDIO_B	NC
GPIOB_6	DIO	Up	General purpose input/output bank GPIOB signal 6	VDDIO_B	NC
GPIOB_7	DIO	Up	General purpose input/output bank GPIOB signal 7	VDDIO_B	NC
GPIOB_8	DIO	Up	General purpose input/output bank GPIOB signal 8	VDDIO_B	NC
GPIOB_9	DIO	Up	General purpose input/output bank GPIOB signal 9	VDDIO_B	NC
GPIOB_10	DIO	Up	General purpose input/output bank GPIOB signal 10	VDDIO_B	NC
GPIOB_11	DIO	DWN	General purpose input/output bank GPIOB signal 11	VDDIO_B	NC
GPIOB_12	DIO	DWN	General purpose input/output bank GPIOB signal 12	VDDIO_B	NC
GPIOB_13	DIO	DWN	General purpose input/output bank GPIOB signal 13	VDDIO_B	NC
GPIOC - Refer to Table 4-3 for functional multiplex information.					
GPIOC_0	DIO	Up	General purpose input/output bank C signal 0	VDDIO_C	NC
GPIOC_1	DIO	Up	General purpose input/output bank C signal 1	VDDIO_C	NC
GPIOC_2	DIO	Up	General purpose input/output bank C signal 2	VDDIO_C	NC
GPIOC_3	DIO	Up	General purpose input/output bank C signal 3	VDDIO_C	NC
GPIOC_4	DIO	Up	General purpose input/output bank C signal 4	VDDIO_C	NC
GPIOC_5	DIO	Up	General purpose input/output bank C signal 5	VDDIO_C	NC
GPIOC_6	DIO	Up	General purpose input/output bank C signal 6	VDDIO_C	NC
GPIOC_7	OD 5V	Hi-Z	General purpose input/output bank C signal 7	VDDIO_C	NC
GPIOX - Refer to Table 4-4 for functional multiplex information.					
GPIOX_0	DIO	Up	General purpose input/output bank X signal 0	VDDIO_X	NC

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Net Name	Type	Default Pull UP/ DN	Description	Power Domain	If Unused
GPIOX_1	DIO	Up	General purpose input/output bank X signal 1	VDDIO_X	NC
GPIOX_2	DIO	Up	General purpose input/output bank X signal 2	VDDIO_X	NC
GPIOX_3	DIO	Up	General purpose input/output bank X signal 3	VDDIO_X	NC
GPIOX_4	DIO	Up	General purpose input/output bank X signal 4	VDDIO_X	NC
GPIOX_5	DIO	Up	General purpose input/output bank X signal 5	VDDIO_X	NC
GPIOX_6	DIO	DWN	General purpose input/output bank X signal 6	VDDIO_X	NC
GPIOX_7	DIO	Up	General purpose input/output bank X signal 7	VDDIO_X	NC
GPIOX_8	DIO	Up	General purpose input/output bank X signal 8	VDDIO_X	NC
GPIOX_9	DIO	Up	General purpose input/output bank X signal 9	VDDIO_X	NC
GPIOX_10	DIO	Up	General purpose input/output bank X signal 10	VDDIO_X	NC
GPIOX_11	DIO	Up	General purpose input/output bank X signal 11	VDDIO_X	NC
GPIOX_12	DIO	Up	General purpose input/output bank X signal 12	VDDIO_X	NC
GPIOX_13	DIO	Up	General purpose input/output bank X signal 13	VDDIO_X	NC
GPIOX_14	DIO	Up	General purpose input/output bank X signal 14	VDDIO_X	NC
GPIOX_15	DIO	Up	General purpose input/output bank X signal 15	VDDIO_X	NC
GPIOX_16	DIO	Up	General purpose input/output bank X signal 16	VDDIO_X	NC
GPIOX_17	DIO	DWN	General purpose input/output bank X signal 17	VDDIO_X	NC
GPIOX_18	DIO	Up	General purpose input/output bank X signal 18	VDDIO_X	NC
GPIOX_19	DIO	Hi-Z	General purpose input/output bank X signal 19	VDDIO_X	NC
GPIOH - Refer to Table 4-5 for functional multiplex information.					
GPIOH_0	OD 5V	Hi-Z	General purpose input/output bank H signal 0	VDDIO_H	NC
GPIOH_1	OD 5V	Hi-Z	General purpose input/output bank H signal 1	VDDIO_H	NC
GPIOH_2	OD 5V	Hi-Z	General purpose input/output bank H signal 2	VDDIO_H	NC
GPIOH_3	OD 5V	Hi-Z	General purpose input/output bank H signal 3	VDDIO_H	NC
GPIOH_4	DIO	DWN	General purpose input/output bank H signal 4	VDDIO_H	NC
GPIOH_5	DIO	DWN	General purpose input/output bank H signal 5	VDDIO_H	NC
GPIOH_6	DIO	Up	General purpose input/output bank H signal 6	VDDIO_H	NC
GPIOH_7	DIO	DWN	General purpose input/output bank H signal 7	VDDIO_H	NC
GPIOH_8	DIO	DWN	General purpose input/output bank H signal 8	VDDIO_H	NC
GPIOH_9	DIO	Up	General purpose input/output bank H signal 9	VDDIO_H	NC

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Net Name	Type	Default Pull UP/ DN	Description	Power Domain	If Unused
GPIOH_10	DIO	DWN	General purpose input/output bank H signal 10	VDDIO_H	NC
GPIOH_11	DIO	DWN	General purpose input/output bank H signal 11	VDDIO_H	NC
GPIOD-Refer to Table 4-6 for functional multiplex information.					
GPIOD_0	DIO	Up	General purpose input/output bank D signal 0	VDDIO_D	NC
GPIOD_1	DIO	Up	General purpose input/output bank D signal 1	VDDIO_D	NC
GPIOD_2	DIO	DWN	General purpose input/output bank D signal 2	VDDIO_D	NC
GPIOD_3	DIO	Up	General purpose input/output bank D signal 3	VDDIO_D	NC
GPIOD_4	DIO	DWN	General purpose input/output bank D signal 4	VDDIO_D	NC
GPIOD_5	DIO	Up	General purpose input/output bank D signal 5	VDDIO_D	NC
GPIOD_6	DIO	DWN	General purpose input/output bank D signal 6	VDDIO_D	NC
GPIOD_7	DIO	DWN	General purpose input/output bank D signal 7	VDDIO_D	NC
GPIOD_8	DIO	Up	General purpose input/output bank D signal 8	VDDIO_D	NC
GPIOD_9	DIO	DWN	General purpose input/output bank D signal 9	VDDIO_D	NC
GPIOD_10	DIO	Up	General purpose input/output bank D signal 10	VDDIO_D	NC
GPIOD_11	DIO	DWN	General purpose input/output bank D signal 11	VDDIO_D	NC
GPIOE- Refer to Table 4-7 for functional multiplex information.					
GPIOE_0	DIO	Hi-Z	General purpose input/output bank E signal 0	VDDIO_E	NC
GPIOE_1	DIO	Hi-Z	General purpose input/output bank E signal 1	VDDIO_E	NC

Abbreviations:

- DI = Digital input pin
- DO = Digital output pin
- DIO = Digital input/output pin
- OD 5V = 5V input tolerant open drain (OD) output pin, need external pull up
- A = Analog setting or filtering pin
- AI = Analog input pin
- AO = Analog output pin
- AIO = Analog input/output pin
- P = Power pin
- AP = Analog power pin
- NC = No connection
- UP = Pull-Up
- DOWN = Pull-down
- Z = High-Z

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4.4 Pin Multiplexing Tables

Multiple usage pins are used to conserve pin consumption for different features. The processor devices can be used in many different applications but each application will not utilize all the on chip features. As a result, some of the features share the same pin. Most of the multiple usage pins can be used as a GPIO pin as well.

Table 4-1 GPIOZ_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4	Func5	Func6	Func7
GPIOZ_0	TDM_FS2	TSin_A_CLK	SDCARD_D0	SPI_A_MISO	UART_D_TX		
GPIOZ_1	TDM_SCLK2	TSin_A_SOP	SDCARD_D1	SPI_A_MOSI	UART_D_RX		
GPIOZ_2	TDM_D4	TSin_A_VALID	SDCARD_D2	SPI_A_CLK	UART_D_CTS		
GPIOZ_3	TDM_D5	TSin_A_D0	SDCARD_D3	SPI_A_SS0	UART_D_RTS		
GPIOZ_4	TDM_D6		SDCARD_CLK	SPI_A_SS1	PWM_G		
GPIOZ_5	TDM_D7		SDCARD_CMD	SPI_A_SS2	PWM_F		
GPIOZ_6	MCLK_2	DTV_A_IF_AGC			PWM_E		
GPIOZ_7		DTV_B_IF_AGC				DISEQC_OUT	
GPIOZ_8		I2CM_D_SDA	UART_E_TX				
GPIOZ_9	SPDIF_OUT	I2CM_D_SCL	UART_E_RX				GEN_CLK
GPIOZ_10	DTV_A_IF_AGC	DTV_A_RF_AGC	PDM_DIN1				
GPIOZ_11	UART_E_TX	DTV_B_RF_AGC	PDM_DIN0	I2CM_E_SCL			
GPIOZ_12	UART_E_RX(in)		PDM_DCLK	I2CM_E_SDA			GEN_CLK

Table 4-2 GPIOB_x Multi-Function Pin

Pin Name	Func1	Func2	Func3
GPIOB_0	EMMC_D0		
GPIOB_1	EMMC_D1		
GPIOB_2	EMMC_D2		
GPIOB_3	EMMC_D3		SPIF_HOLD
GPIOB_4	EMMC_D4		SPIF_MO
GPIOB_5	EMMC_D5		SPIF_MI
GPIOB_6	EMMC_D6		SPIF_CLK
GPIOB_7	EMMC_D7		SPIF_WP

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Pin Name	Func1	Func2	Func3
GPIOB_8	EMMC_CLK	NAND_WEN_CLK	
GPIOB_9		NAND_ALE	
GPIOB_10	EMMC_CMD	NAND_REN_WR	
GPIOB_11	EMMC_DS	NAND_CLE	
GPIOB_12		NAND_CE0	
GPIOB_13			SPIF_CS

Table 4-3 GPIOC_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4
GPIOC_0	SDCARD_D0	JTAG2_TDO	PDM_DIN1	TDM_D2
GPIOC_1	SDCARD_D1	JTAG2_TDI	PDM_DIN0	TDM_D3
GPIOC_2	SDCARD_D2	UART_B_RX	I2CM_E_SCL	TDM_FS1
GPIOC_3	SDCARD_D3	UART_B_TX	I2CM_E_SDA	TDM_SCLK1
GPIOC_4	SDCARD_CLK	JTAG2_CLK	PDM_DCLK	MCLK_1
GPIOC_5	SDCARD_CMD	JTAG2_TMS	ISO7816_CLK	TDM_D4
GPIOC_6		I2CM_B_SDA	ISO7816_DATA	TDM_D5
GPIOC_7		I2CM_B_SCL		

Table 4-4 GPIOX_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4	Func5
GPIOX_0	SDIO_D0				
GPIOX_1	SDIO_D1				
GPIOX_2	SDIO_D2				
GPIOX_3	SDIO_D3				
GPIOX_4	SDIO_CLK				
GPIOX_5	SDIO_CMD				
GPIOX_6	PWM_A				
GPIOX_7	PWM_F				
GPIOX_8	TDM_D1	PDM_DIN0	SPI_A_MOSI	PWM_C	
GPIOX_9	TDM_D0	PDM_DIN1	SPI_A_MISO		
GPIOX_10	TDM_FS0		SPI_A_SS0	I2CS_A_SDA	I2CM_D_SDA
GPIOX_11	TDM_SCLK0	PDM_DCLK	SPI_A_CLK	I2CS_A_SCL	I2CM_D_SCL
GPIOX_12	UART_A_TX				
GPIOX_13	UART_A_RX				
GPIOX_14	UART_A_CTS				

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Pin Name	Func1	Func2	Func3	Func4	Func5
GPIOX_15	UART_A_RTS				
GPIOX_16	PWM_E				
GPIOX_17	I2CM_B_SDA				
GPIOX_18	I2CM_B_SCL				
GPIOX_19	PWM_B				

Table 4-5 GPIOH_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4	Func5	Func6
GPIOH_0	HDMITX_ SDA	I2CM_C_SDA				
GPIOH_1	HDMITX_SCL	I2CM_C_SCL				
GPIOH_2	HDMITX_ HPD_IN					
GPIOH_3	AO_CEC_A	AO_CEC_B				
GPIOH_4	SPDIF_OUT	UART_D_TX		MCLK_1	SPI_A_MISO	
GPIOH_5	SPDIF_IN	UART_D_RX		TDM_SCLK1	SPI_A_MOSI	
GPIOH_6	I2CM_B_SDA	UART_D_ CTS	PWM_D	TDM_FS1	SPI_A_CLK	
GPIOH_7	I2CM_B_SCL	UART_D_ RTS	PWM_I	TDM_D2	SPI_A_SS0	
GPIOH_8	I2CM_C_SDA	ISO7816_ CLK	PDM_DCLK	TDM_D3		
GPIOH_9	I2CM_C_SCL	ISO7816_ DATA	PDM_DIN0	TDM_D4		
GPIOH_10	ETH_LINK_ LED	UART_E_TX	PDM_DIN1			
GPIOH_11	ETH_ACT_ LED	UART_E_RX				GEN_CLK

Table 4-6 GPIOD_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4	Func5	Func6
GPIOD_0	UART_B_TX					
GPIOD_1	UART_B_RX					
GPIOD_2	UART_B_ CTS	I2CM_E_SCL	UART_C_TX	CLK_32K_IN	MIC_MUTE_ EN	
GPIOD_3	UART_B_ RTS	I2CM_E_SDA	UART_C_RX		MIC_MUTE_ KEY	
GPIOD_4	IR_RE- MOTE_OUT	MCLK_1	PWM_B	PWM_B_HIZ		
GPIOD_5	IR_RE- MOTE_ INPUT					

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Pin Name	Func1	Func2	Func3	Func4	Func5	Func6
GPIOD_6	JTAG_CLK	TDM_SCLK1	PWM_A	PWM_A_HIZ	I2CM_B_SDA	
GPIOD_7	JTAG_TMS	TDM_FS1	PWM_C	PWM_C_HIZ	I2CM_B_SCL	
GPIOD_8	JTAG_TDI	TDM_D4	PWM_D	PDM_DCLK		
GPIOD_9	JTAG_TDO	TDM_D3	PWM_I	PDM_DIN0		
GPIOD_10	CLK12M_ 24M	TDM_D2		PDM_DIN1	I2CM_C_SDA	GEN_CLK
GPIOD_11	PWM_G_HIZ	PWM_G			I2CM_C_SCL	HDMITX_ TEST_O

Table 4-7 GPIOE_x Multi-Function Pin

Pin Name	Func1	Func2	Func3
GPIOE_0	I2CM_A_SDA	UART_B_TX	PWM_H
GPIOE_1	I2CM_A_SCL	UART_B_RX	PWM_J

4.5 Signal Description

Table 4-8 SD Card Interface Signal Description

Signal Name	Type	Description
SDCARD_D0	DIO	SD Card data bus bit 0 signal
SDCARD_D1	DIO	SD Card data bus bit 1 signal
SDCARD_D2	DIO	SD Card data bus bit 2 signal
SDCARD_D3	DIO	SD Card data bus bit 3 signal
SDCARD_CLK	DO	SD Card clock signal
SDCARD_CMD	DIO	SD Card command signal

Table 4-9 SDIO Interface Signal Description

Signal Name	Type	Description
SDIO_D0	DIO	SDIO data bus bit 0 signal
SDIO_D1	DIO	SDIO data bus bit 1 signal
SDIO_D2	DIO	SDIO data bus bit 2 signal
SDIO_D3	DIO	SDIO data bus bit 3 signal
SDIO_CLK	DO	SDIO clock signal
SDIO_CMD	DIO	SDIO command signal

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Table 4-10 Clock Interface Signal Description

Signal Name	Type	Description
CLK_32K_IN	DI	32KHz clock input
CLK12_24	DO	12MHz/24MHZ clock output

Table 4-11 UART Interface Signal Description

Signal Name	Type	Description
UART_D_ TX	DO	UART Port D data output
UART_D_RX	DI	UART Port D data input
UART_D_ CTS	DI	UART Port D Clear To Send Signal
UART_D _ RTS	DO	UART Port D Ready To Send Signal
UART_E_ TX	DO	UART Port E data output
UART_E_ RX	DI	UART Port E data input
UART_A _TX	DO	UART Port A data output
UART_A_RX	DI	UART Port A data input
UART_A_CTS	DI	UART Port A Clear To Send Signal
UART_A_RTS	DO	UART Port A Ready To Send Signal
UART_B_TX	DO	UART Port B data output
UART_B_RX	DI	UART Port B data input
UART_C_TX	DO	UART Port C data output
UART_C_RX	DI	UART Port C data input

Table 4-12 ISO7816 Interface Signal Description

Signal Name	Type	Description
ISO7816_DATA	DIO	ISO7816 data signal
ISO7816_CLK	DO	ISO7816 clock signal

Table 4-13 TS In Interface Signal Description

Signal Name	Type	Description
TSIN_A_D0	DI	Serial TS input port A data
TSIN_A_CLK	DI	TS input port A clock
TSIN_A_SOP	DI	TS input port A start of stream signal
TSIN_A_VALID	DI	TS input port A date valid signal

Table 4-14 PWM Interface Signal Description

Signal Name	Type	Description
PWM_A / PWM_A_HIZ	DO	PWM channel A output signal, or extended HiZ function of PWM_A
PWM_B / PWM_B_HIZ	DO	PWM channel B output signal, or extended HiZ function of PWM_B

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Signal Name	Type	Description
PWM_C / PWM_C_HIZ	DO	PWM channel C output signal, or extended HiZ function of PWM_C
PWM_D	DO	PWM channel D output signal
PWM_E	DO	PWM channel E output signal
PWM_F	DO	PWM channel F output signal
PWM_G / PWM_G_HIZ	DO	PWM channel G output signal, or extended HiZ function of PWM_G
PWM_H	DO	PWM channel H output signal
PWM_J	DO	PWM channel J output signal

Table 4-15 I2C Interface Signal Description

Signal Name	Type	Description
I2CS_A_SCL	DI	I2C bus A clock input, Slave mode
I2CS_A_SDA	DIO	I2C bus A data input/output, Slave mode
I2CM_A_SCL	DO	I2C bus A clock output, Master mode
I2CM_A_SDA	DIO	I2C bus A data input/output, Master mode
I2CM_B_SCL	DO	I2C bus B clock output, Master mode
I2CM_B_SDA	DIO	I2C bus B data input/output, Master mode
I2CM_C_SCL	DO	I2C bus C clock output, Master mode
I2CM_C_SDA	DIO	I2C bus C data input/output, Master mode
I2CM_D_SCL	DO	I2C bus C clock output, Master mode
I2CM_D_SDA	DIO	I2C bus D data input/output, Master mode
I2CM_E_ SCL	DO	I2C bus C clock output, Master mode
I2CM_E_SDA	DIO	I2C bus E data input/output, Master mode

Table 4-16 eMMC Interface Signal Description

Signal Name	Type	Description
EMMC_D0	DIO	eMMC/NAND data bus bit 0 signal
EMMC_D1	DIO	eMMC/NAND data bus bit 1 signal
EMMC_D2	DIO	eMMC/NAND data bus bit 2 signal
EMMC_D3	DIO	eMMC/NAND data bus bit 3 signal
EMMC_D4	DIO	eMMC/NAND data bus bit 4 signal
EMMC_D5	DIO	eMMC/NAND data bus bit 5 signal
EMMC_D6	DIO	eMMC/NAND data bus bit 6 signal
EMMC_D7	DIO	eMMC/NAND data bus bit 7 signal
EMMC_CLK	DO	eMMC clock signal

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Signal Name	Type	Description
EMMC_CMD	DIO	eMMC command signal
EMMC_NAND_DQS	DIO	eMMC/NAND data strobe

Table 4-17 NAND Signal Description

Signal Name	Type	Description
NAND_ALE	DO	NAND address latch enable
NAND_CE1	DO	NAND chip enable 1
NAND_CLE	DO	NAND command latch enable
NAND_REN_WR	DO	NAND read enable or write/read
NAND_WEN_CLK	DO	NAND write enable or clock

Table 4-18 NOR Interface Signal Description

Signal Name	Type	Description
SPIF_CS	DO	SPI NOR chip select
SPIF_CLK	DO	SPI NOR Serial Clock
SPIF_MO	DIO	SPI NOR 1bit mode Output, 2/4 bit mode data I/O 0
SPIF_MI	DIO	SPI NOR 1bit mode Input, 2/4 bit mode data I/O 1
SPIF_WP	DIO	SPI NOR Write protection output, 4 bit mode data I/O 2
SPIF_HOLD	DIO	SPI bus hold output, 4 bit mode data I/O 3

Table 4-19 HDMI Interface Signal Description

Signal Name	Type	Description
HDMITX_SDA	DIO	HDMI TX DDC_I2C interface data signal
HDMITX_SCL	DO	HDMI TX DDC_I2C interface clock signal
HDMITX_HPD_IN	DI	HDMI TX hot-plug in signal input
CEC_A	DIO	Customer Electronics Control signal
CEC_B	DIO	2nd pin of Customer Electronics Control signal

Table 4-20 SPDIF Interface Signal Description

Signal Name	Type	Description
SPDIF_IN	DI	SPDIF input signal
SPDIF_OUT	DO	SPDIF output signal

Table 4-21 SPI Interface Signal Description

Signal Name	Type	Description
SPI_A_MOSI	DIO	SPI master output, slave input A
SPI_A_MISO	DIO	SPI master input, slave output A

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Signal Name	Type	Description
SPI_A_SCLK	DIO	SPI clock A
SPI_A_SS0	DIO	SPI slave select 0 A
SPI_A_SS1	DIO	SPI slave select 1 A
SPI_A_SS2	DIO	SPI slave select 2 A

Table 4-22 Remote Interface Signal Description

Signal Name	Type	Description
IR_REMOTE_IN	DI	IR remote control input
IR_REMOTE_OUT	DO	IR remote control output

Table 4-23 Time Division Multiplexing Signal Description

Signal Name	Type	Description
MCLK_1	DO	Master clock output 1, for I2S master mode
MCLK_2	DO	Master clock output 2, for I2S master mode
TDM_D0	DIO	Data input/output 0 of TDM
TDM_D1	DIO	Data input/output 1 of TDM
TDM_D2	DIO	Data input/output 2 of TDM
TDM_D3	DIO	Data input/output 3 of TDM
TDM_D4	DIO	Data input/output 4 of TDM
TDM_D5	DIO	Data input/output 5 of TDM
TDM_D6	DIO	Data input/output 6 of TDM
TDM_D7	DIO	Data input/output 7 of TDM
TDM_SCLK0	DO	Bit clock output of TDM
TDM_FS0	DO	Frame sync output of TDM (Word clock of I2S)
TDM_SCLK1	DO	Bit clock output of TDM
TDM_FS1	DO	Frame sync output of TDM (Word clock of I2S)
TDM_SCLK2	DO	Bit clock output of TDM
TDM_FS2	DO	Frame sync output of TDM (Word clock of I2S)

Table 4-24 PDM Signal Description

Signal Name	Type	Description
PDM_DIN0	DI	PDM input data 0 signal
PDM_DIN1	DI	PDM input data 1 signal
PDM_DCLK	DO	PDM output clock signal

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Table 4-25 JTAG Interface Signal Description

Signal Name	Type	Description
JTAG_A_TDO	DO	JTAG data output channel A
JTAG_A _TDI	DI	JTAG data input channel A
JTAG_A_TMS	DI	JTAG Test mode select input channel A
JTAG_A_CLK	DI	JTAG Test clock input channel A
JTAG_B_TDO	DO	JTAG data output channel B
JTAG_B _TDI	DI	JTAG data input channel B
JTAG_B_TMS	DI	JTAG Test mode select input channel B
JTAG_B _CLK	DI	JTAG Test clock input channel B

Table 4-26 Ethernet Interface Signal Description

Signal Name	Type	Description
ETH_LINK_LED	DO	Ethernet link LED indicator
ETH_ACT_LED	DO	Ethernet active LED indicator

Table 4-27 Other Signal Description

Signal Name	Type	Description
GEN_CLK	DO	General clock output, for debug

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5 Operating Conditions

5.1 Absolute Maximum Ratings

The table below gives the absolute maximum ratings. Exposure to stresses beyond those listed in this table may result in permanent device damage, unreliability or both.

Table 5-1 Absolute Maximum Ratings

Characteristic	Value	Unit
VDDCPU Supply Voltage	1.15	V
VDD_EE Supply Voltage	1.02	V
VDDQ Supply Voltage	1.7	V
1.8V Supply Voltage	1.98	V
3.3V Supply Voltage	3.63	V
Input voltage, V_I	-0.3 ~VDDIO+0.3	V
Junction Temperature	125	°C

5.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max	Unit
VDDCPU	Voltage for Cortex A35 CPU	0.68[1]	-	1.03[2]	V
VDD_EE and other 0.8V domain	Voltage for GPU & core logic	0.77	0.8	0.9	V
VDDQ	DDR3/DDR3L/DDR4/LPDDR/ LPDDR4 IO Supply Voltage	1.05	-	1.6	V
AVDD18	1.8V AVDD for HDMI, USB, CVBS, ETHERNET phy and AUDIO	1.71	1.80	1.89	V
AVDD18_AO	1.8V VDD for XTAL, IOVREF, SAR-ADC, GPIOE, PLL	1.71	1.80	1.89	V
AVDD_DDRPLL	Analog power supply for DDRPLL	1.05	-	1.89	V
AVDD33	3.3V AVDD for USB	3.15	3.3	3.45	V
VDDIO	LV mode	1.71	1.80	1.89	V
	HV mode	3.0[3]	3.3	3.45	V
T_J	Operating Junction Temperature	0	—	105[4]	°C
T_A	Operating Ambient Temperature	0	—	70	°C

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Note

1. Minimal VDDCPU voltage is for sleep mode while system runs at very low speed. Higher clock will need higher voltage. Considering the power supply may have 3% deviation, the minimal voltage in actual application should not be set to lower than min spec plus 0.02V.
2. Likewise, maximum VDDCPU voltage in actual application should be lower than the max spec value minus 0.02V. Voltage of VDDCPU will affect CPU speed. Use lower voltage when CPU runs on lower speed to save power. Recommend to use +/-1.5% or higher precision DCDC.
3. GPIO cannot work if VDDIO voltage is out of the spec of LV / HV mode. GPIO output at HV mode will be weaker & max operating speed will be lower if VDDIO are design to 3.0V. Do not design VDDIO to lower than 3.0V in HV mode, recommend to use +/-1.5% or higher precision DCDC to supply power for VDDIO, actual voltage supplies to VDDIO (HV mode) should not be lower than 2.9V.
4. For operating temperature, good heat sink may be needed to guarantee Tj < max spec.

5.3 Ripple Voltage Specifications

Table 5-2 Ripple Voltage Specifications

Power	Max Ripple	Unit	Test State
VDDCPU	40	+/-mV	Run APK StabilityTest
VDD_EE and other 0.8V domain	40	+/-mV	Run APK Basemark ES 2.0 Taiji
DDR3 VDDQ	60	+/-mV	Kernel boot
DDR3L VDDQ	60	+/-mV	Kernel boot
DDR4 VDDQ	40	+/-mV	Kernel boot
AVDD18	30	+/-mV	Kernel boot
VDD18_AO	30	+/-mV	Kernel boot
AVDD33	50	+/-mV	WIFI SCAN
VDDIO LV	60	+/-mV	Kernel boot
VDDIO HV	60	+/-mV	WIFI SCAN

Note

The ripple specifications are for reference only. Customers should perform pressure / performance / reliability tests (high / low temperature tests, wet / heat tests, functional tests, etc.) on the product to confirm system stability.

5.4 Thermal Resistance

Jedec 2P2S board 101.5mm*114.5mm, natural convection, ambient temperature 25°C.

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Symbol	Parameter	Value(°C/ Watt)	Air Flow(m/s)
Θja	Package junction-to-ambiance thermal resistance in nature convection	22.9	0
Θjb	Package junction-to-pcb thermal resistance in nature convection	11.5	0
Θjc	Package junction-to-case thermal resistance in nature convection	11.3	0

Note

1. Due to the thinness of the SOC, DRAM or capacitors placed close to SOC may prevent heat-sink touching SOC top side. A special convex shape heatsink is recommended.
2. These measurement were conducted on a JEDEC defined 2S2P system. For more information, check below JEDEC standards:
   - JESD51-2A: Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)
   - JESD51-8: Integrated Circuit Thermal Test Method Environmental Conditions -Junction-to-Board
   - JESD51-12: Guidelines for Reporting and Using Electronic Package Thermal Information
3. m/s = meters per second

5.5 DC Electrical Characteristics

5.5.1 Normal GPIO Specifications (For DIO_xmA)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{iH(VDDIO=3.3V)}$[3]	High-level input voltage	IOVREF+0.37	-	VDDIO+0.3	V
$V_{iL(VDDIO=3.3V)}$[3]	Low-level input voltage	-0.3	-	IOVREF-0.23	V
$V_{iH(VDDIO=1.8V)}$[3]	High-level input voltage	IOVREF/2+0.3	-	VDDIO+0.3	V
$V_{iL(VDDIO=1.8V)}$[3]	Low-level input voltage	-0.3	-	IOVREF/2-0.3	V
$R_{PU/PD}$	Built-in pull up resistor	-	41K	-	ohm
IoL/IoH(DS=0)[1,4]	GPIO driving capability	0.5	-	-	mA
IoL/IoH(DS=1)[1]	GPIO driving capability	2.5	-	-	mA
IoL/IoH(DS=2)[1]	GPIO driving capability	3	-	-	mA
IoL/IoH(DS=3)[1]	GPIO driving capability	4[2]	-	-	mA

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Symbol	Parameter	Min.	Typ.	Max.	Unit
VOH	Output high level with IoL/IoH loading	VDDIO-0.5	-	-	V
VOL	Output low level with IoL/IoH loading	-	-	0.4	V

Note

1. With Minimal IoL/IoH driving capability loading, IO is garanteed to meet Vol < 0.4V or VOH > (VDDIO-0.5V) spec.
2. Maximal GPIO loading is 6mA for application such as driving LED, which does not care about Vol/Voh spec. Please set DS=3 for such application.
3. VDD18_AO_XTAL supplies power to IOVREF.
4. Do not use this setting, it's too weak for most applications.
5. Test condition: GPIO pin voltage close to 0V.
6. Test condition: GPIO pin voltage close to VDDIO(3.3V).

5.5.2 Open Drain GPIO Specifications (For DIO_OD)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{iH}(OD5V)	High-level input voltage	1.5		5.5	V
V_{iL}(OD5V)	Low-level input voltage	-0.3		0.8	V
V_{iH}(OD3.3V)	High-level input voltage	1.5		3.6	V
V_{iL}(OD3.3V)	Low-level input voltage	-0.3		0.8	V
$R_{PU/PD}$	No built-in pull up/down resistor on OD IO	-	-	-	ohm
Io	OD IO driving low capability	4		6	mA
VOL	Output low level with min Io loading			0.4	V

Note

1. With Minimal IoL driving capability loading, IO is guaranteed to meet Vol<0.4V spec
2. Maximal GPIO loading is 6mA for application such as driving LED, which does not care about Vol spec
3. The V_{iL} / V_{iH} of OD PAD is irrelevant to VDDIO voltage.
4. "OD 5V" means that in applications such as I2C, use a resistor greater than 1Kohm to pull it up to 5V. Do not connect the pad directly to the 5V power supply.

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5.5.3 DDR3/DDR3L/DDR4/LPDDR4 SDRAM Specifications

Table 5-3 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDQ	IO supply voltage (DDR3)	1.425	1.50	1.57	V
VDDQ	IO supply voltage (DDR3L)	1.283	1.35	1.45	V
VDDQ	IO supply voltage (DDR4)	1.14	1.20	1.30	V
VDDQ	IO supply voltage (LPDDR4)	1.06	1.1	1.17	V
Vref	Input reference supply voltage	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V

Note

The minimal VDDQ voltage in sleep mode is defined by memory.

Table 5-4 DC specifications - DDR3/DDR3L Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIH	DC input voltage high	Vref + 0.100		VDDQ	V
VIL	DC input voltage low	VSSQ		Vref-0.100	V
VOH	DC output logic high	0.8*VDDQ			V
VOL	DC output logic low			0.2*VDDQ	V
RTT	Input termination resistance to VDDQ/2	100 54 36	120 60 40	140 66 44	ohm

Table 5-5 DC specifications – DDR4 Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VdlVW_total	Rx Mask voltage-p-p total			136	mv
VOH	DC output logic high	0.9*VDDQ			V
VOL	DC output logic low			0.1*VDDQ	V
RTT	Input termination resistance to VDDQ	200	240	280	ohm
		100	120	140	
		67	80	93	
		50	60	70	
		42	48	56	
		34	40	46	
		28	34	40	

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Table 5-6 DC Specifications – LPDDR4 Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VOH	DC output logic high	0.9*VDDQ	-	-	V
VOL	DC output logic low	-	-	0.1*VDDQ	V
RTT	Input termination resistance to VDDQ	216	240	264	ohm
		108	120	132	
		72	80	88	
		54	60	66	
		43.2	48	52.8	
		36	40	44	

5.6 Recommended Oscillator Electrical Characteristics

The SoC requires the 24MHz oscillator for generating the main clock source.

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_o	Nominal Frequency		24		MHz	
$\Delta f/f_o$	Frequency Tolerance	-30		30	ppm	At 25 ℃
		-50		50	ppm	At -20~85 ℃
C_L	Load Capacitance	7.5	12	12.5	pF	
ESR	Equivalent Series Resistance			100	oHm	

Note

1. 10ppm Tolerance is preferred if 24MHz XTAL is also driving WIFI module.
2. For user external clock source, please connect input clock output to SYS_OSCIN , let SYS_OSCOUT floating.
3. The threshold of Xin inverter is around 0.9V (Xin range: -0.3V to +2.1V). Therefore, Following suggestion for input clock.
   - Suggestion 1: Without DC blocking capacitor, use a higher Vpp output TCXO. The high voltage should be higher than 1.35V (VSWING >1.35V, 0V to >1.35V).
   - Suggestion 2: With DC blocking capacitor, re-bias the middle voltage at 0.9V, VSWING >2*0.45V;

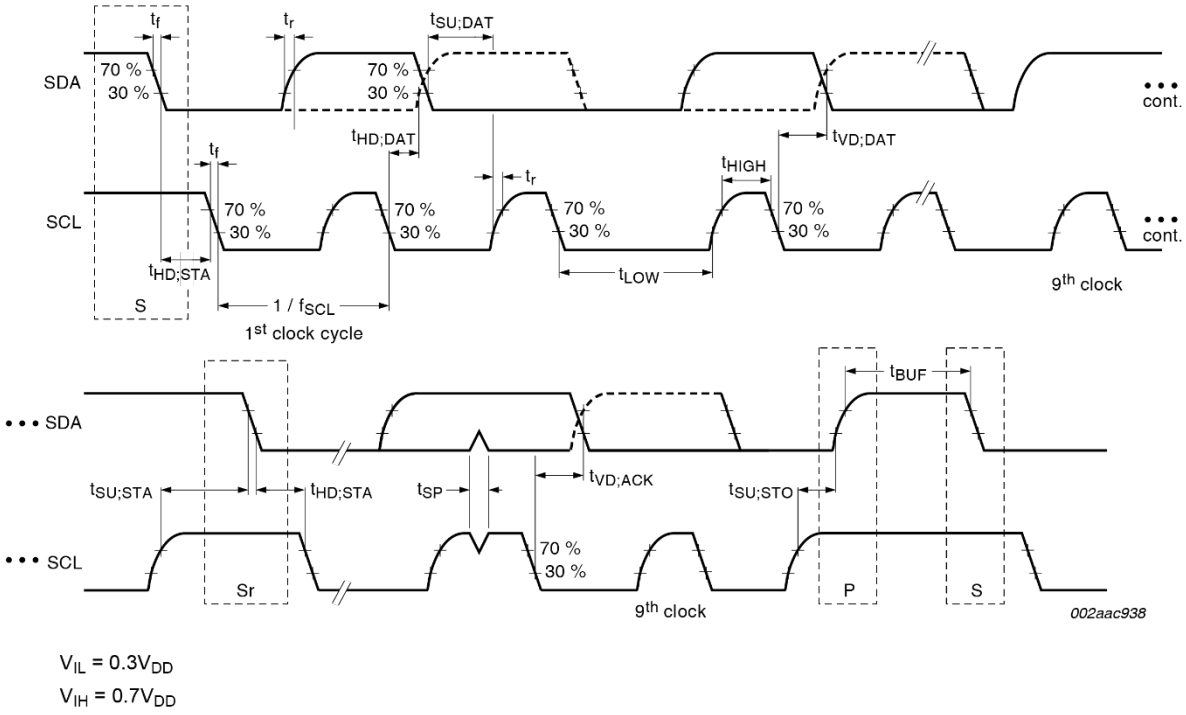
5.7 Timing Information

5.7.1 I2C Timing Specification

The I2C master interface Fast/Standard mode timing specifications are shown below.

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Figure 5-1 I2C Interface Timing Diagram, FS mode



$V_{IL} = 0.3V_{DD}$

$V_{IH} = 0.7V_{DD}$

Table 5-7 I2C Interface Timing Specification, SF mode

Symbol	Parameter	Standard-mode		Fast-mode		Unit
		Min.	Max	Min	Max	
tR	Rise time of SDA and SCL signals	-	1000	-	300	ns
tF	Fall time of SDA and SCL signals	-	300	-	300	ns
fSCL	SCL clock frequency	-	100	-	400	KHz
tLOW	LOW period of the SCL clock	4.7	-	1.3	-	μs
tHIGH	HIGH period of the SCL clock	4	-	0.6	-	μs
tSu;STA	Setup time for START	4.7	-	0.6	-	μs
tSu;DAT	Setup time for SDA	250	-	100	-	ns
tSu;STO	Setup time for STOP	4	-	0.6	-	μs
tHd;STA	Hold time for START	4	-	0.6	-	μs

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Symbol	Parameter	Standard-mode		Fast-mode		Unit
		Min.	Max	Min	Max	
tHd;DAT	Hold time for SDA	0	3.45	0	0.9	µs
tBuf	Bus free time between stop and start	4.7	-	1.3	-	µs

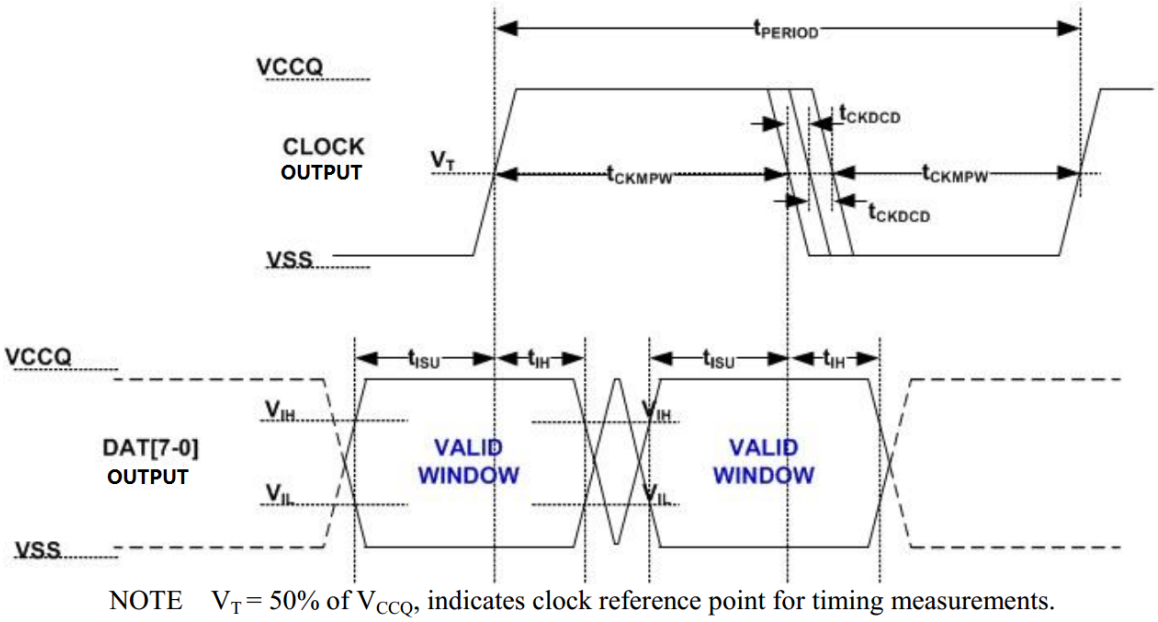
Note

- Open drain does not support driver strength adjustment.

5.7.2 EMMC/SD Timing Specification

Timing specification for EMMC and SDIO are shown as below.

Figure 5-2 EMMC HS400 Data Output Timing



NOTE $V_T = 50\%$ of V_{CCQ}, indicates clock reference point for timing measurements.

Table 5-8 HS400 Timing Specification

Symbol	Parameter	Min	Max	Unit
tPERIOD	Cycle time data transfer mode	5	-	ns
SR	Slew rate	1.125	-	V/ns
tCKDCD	Duty cycle distortion	0	0.3	ns
tCKMPW	Minimum pulse width	2.2	-	ns
tISU	input set-up time	1.4	-	ns
tIH	input hold time	0.8	-	ns

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Symbol	Parameter	Min	Max	Unit
tISUddr	input set-up time	0.4	-	ns
tIHddr	input hold time	0.4	-	ns

Figure 5-3 EMMC HS200 Data Output Timing

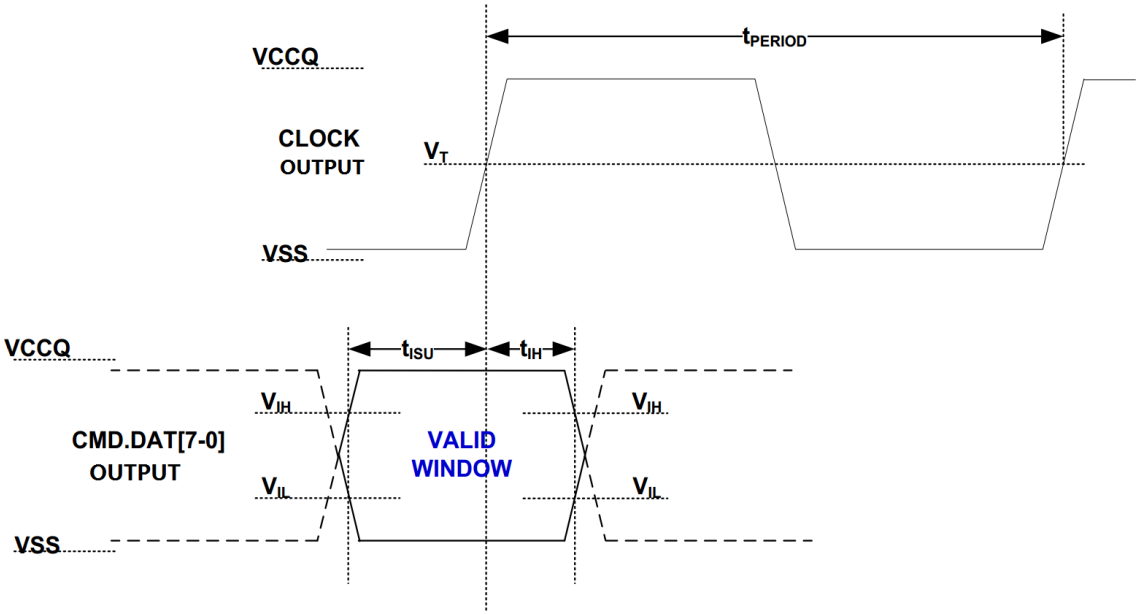


Table 5-9 HS200 Timing Specification

Symbol	Parameter	Min	Max	Unit
tPERIOD	Cycle time data transfer mode	5	-	ns
tISU	output set-up time	1.4	-	ns
tIH	output hold time	0.8	-	ns

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Figure 5-4 EMMC HS400 Data Input Timing

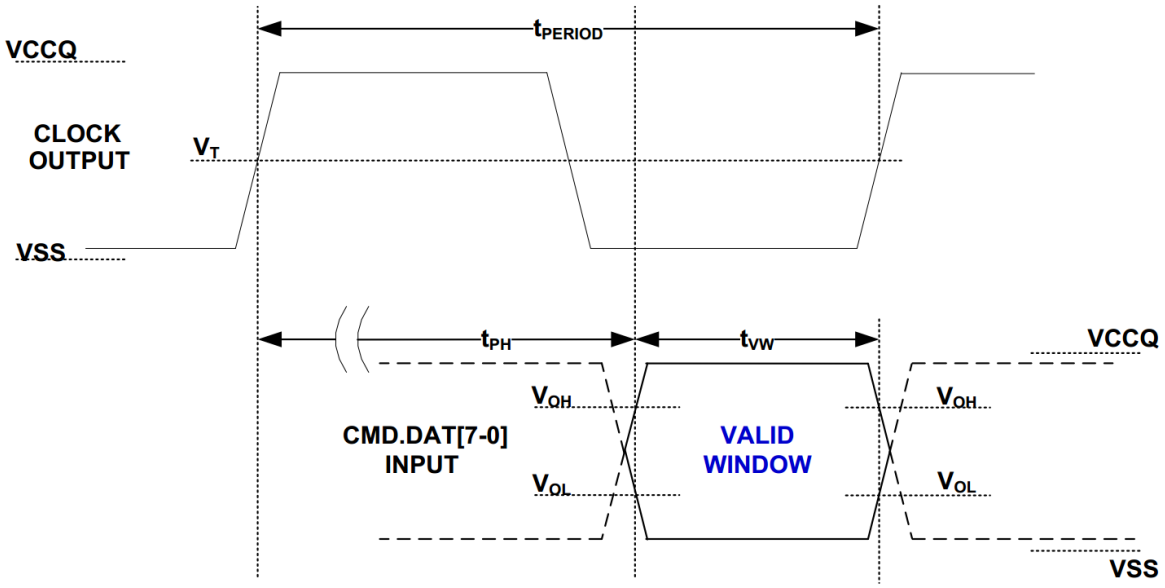


Table 5-10 HS400 Data Input Timing Specification

Symbol	Parameter	Min	Max	Unit
tPERIOD	Cycle time data transfer mode	5	-	ns
SR	Slew rate	1.125	-	V/ns
tCKDCD	Duty cycle distortion	0	0.2	ns
tCKMPW	Minimum pulse width	2	-	ns
tRQ	Input skew	-	0.4	ns
tRQH	input hold skew	-	0.4	ns

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Figure 5-5 EMMC HS200 Data Input Timing

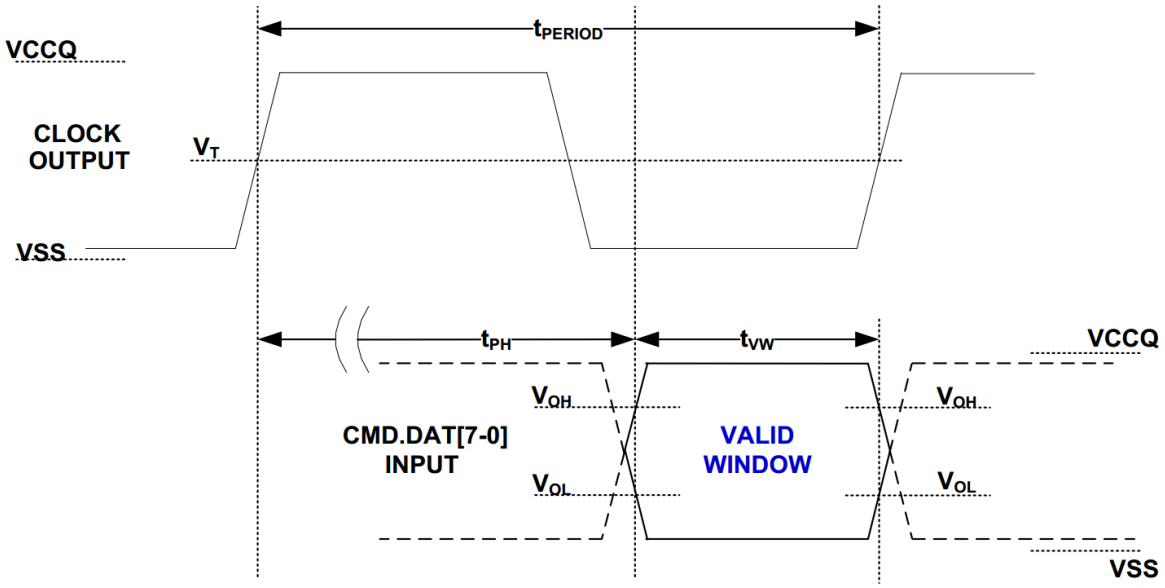
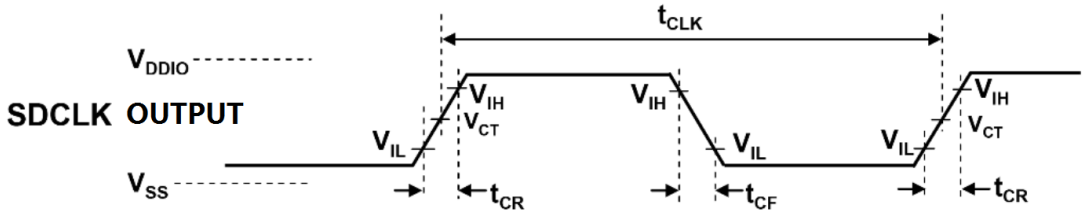


Table 5-11 HS200 Timing Specification

Symbol	Parameter	Min	Max	Unit
tPH	Device output momentary phase from CLK input to CMD or DAT line output. Does not include a longterm temperature drift.	0	2	UI
ΔTPH	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (TVW) from last system Tuning procedure ΔTPH is 2600ps for ΔT from -25 °C to 125 °C during operation.	-350(ΔT=-20deg.C)	1550(ΔT=90deg.C)	ps
tVW	Valid Data Simple window	0.575	-	UI

Figure 5-6 SDIO (SDR104) Clock Signal Timing Diagram



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Table 5-12 SDIO (SDR104) Clock Timing Specification

Symbol	Parameter (SDR104 Mode)	Min	Max	Unit
tCLK	clock period Data Transfer Mode (PP)	4.8	-	ns
Duty	Clock Duty	30	70	%
tCR	clock rise time	-	0.96	ns
tCF	clock fall time	-	0.96	ns

Figure 5-7 SDIO (SDR104) Output Timing Diagram

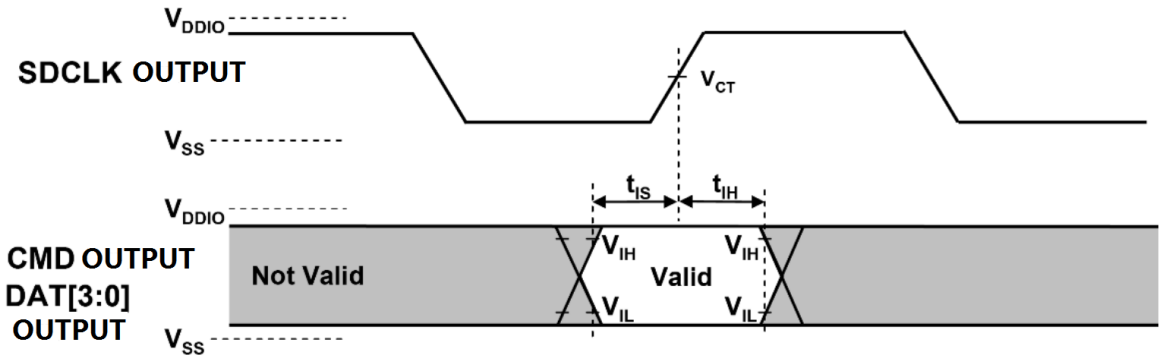


Table 5-13 SDIO (SDR104) Output Timing Specification

Inputs CMD, DAT (referenced to CLK)				
Symbol	**Parameter**	**Min**	**Max**	**Unit**
tIS	input set-up time	1.4	-	ns
tIH	input hold time	0.8	-	ns

Note

SD card interface uses SDIO protocol.

5.7.3 NAND Timing Specification

Nand timing specifications are shown as below.

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Figure 5-8 Async Waveform for Command/Address/Data Output Timing

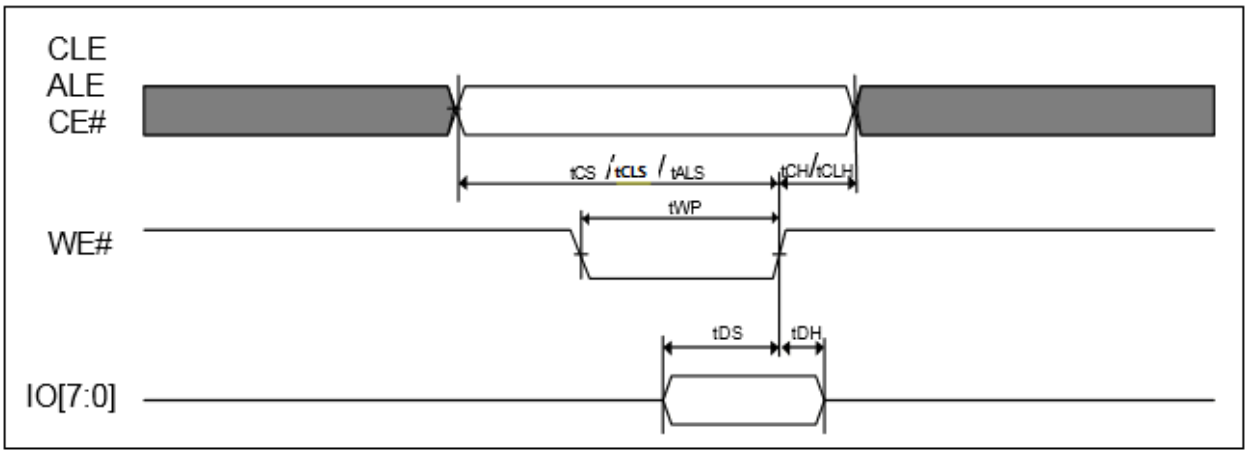
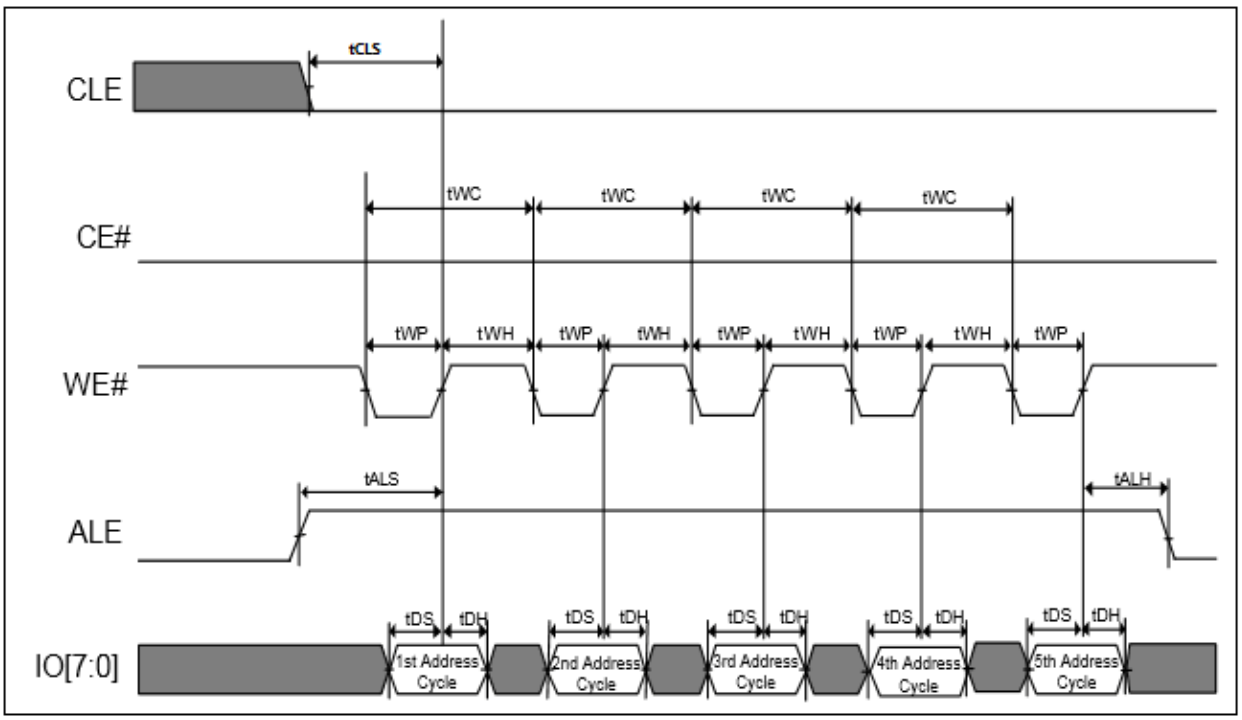


Figure 5-9 Async Waveform for Address Output Cycle



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Figure 5-10 Async Waveform for Sequential Data Read Cycle(After Read)-EOD Mode

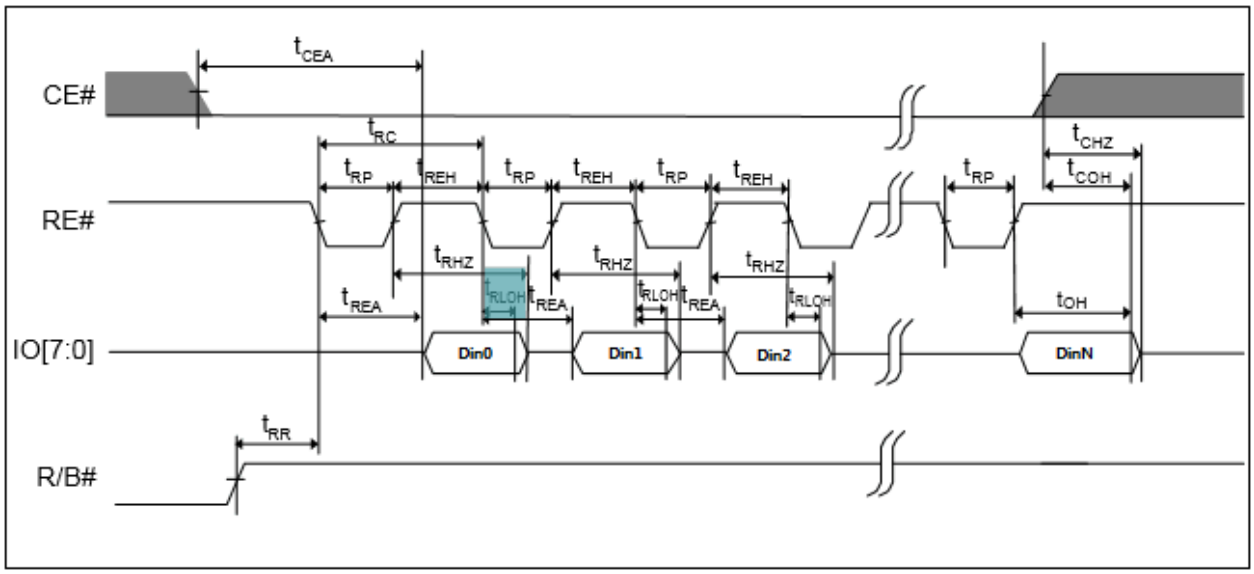


Table 5-14 Nand Timing Specifications

Symbol	Parameter (Asyn-chronous) (mode 5)	Min	Max	Unit
tCLS	CLE setup time	10	-	ns
tCLH	CLE hold time	5	-	ns
tALS	ALE setup	10	-	ns
tALH	ALE hold	5	-	ns
tDS	Data setup time	7	-	ns
tDH	Data hold time	5	-	ns
tWC	WE# cycle time	20	-	ns
tWP	WE# pulse width	10	-	ns
tWH	WE# high lold time	7	-	ns
tREA	RE# access time	-	16	ns
tOH	Data output hold time	15	-	ns
tRLOH	RE#-low to data hold time (EDO)	5	-	ns
tRP	RE# pulse width	10	-	ns
tREH	RE# high hold time	7	-	ns
tRC	RE# cycle time	20	-	ns

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5.7.4 SPICC Timing Specification

Figure 5-11 SPICC Timing Diagram

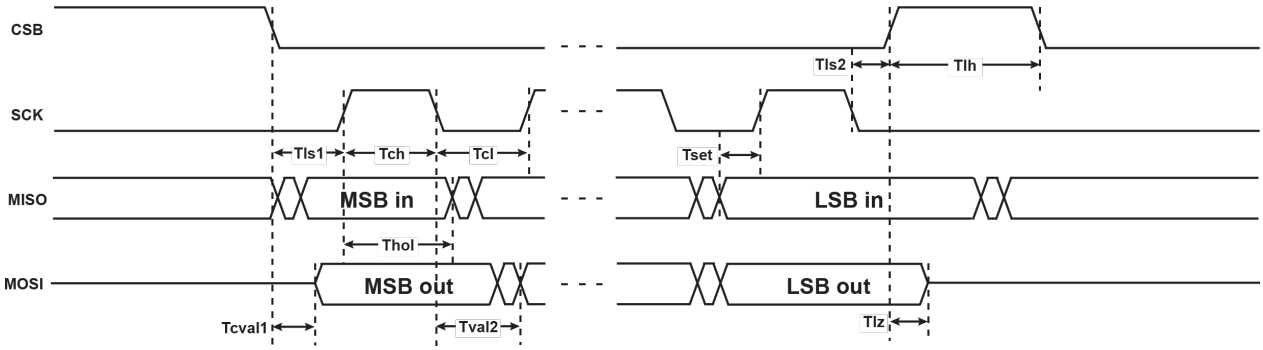
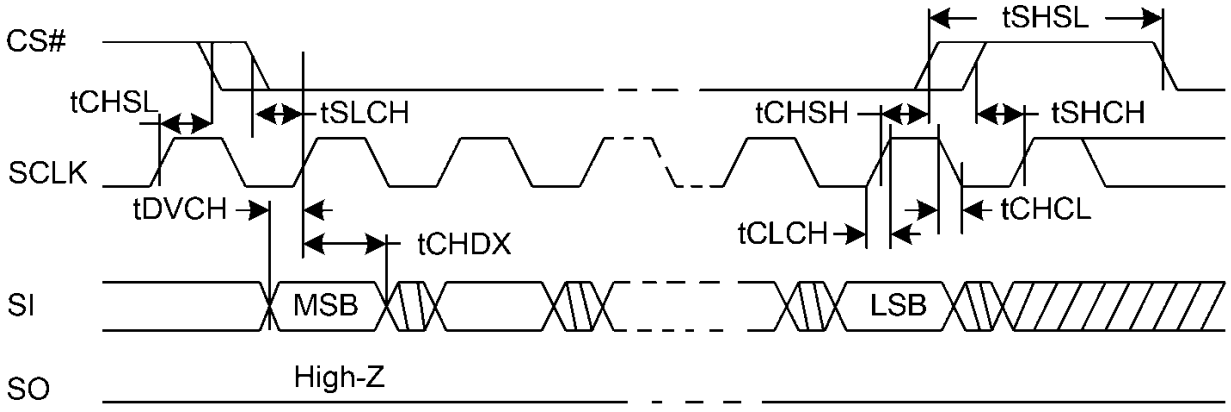


Table 5-15 SPICC Master Timing Specification

Symbol	Description	Min.	Max.	Unit
fCLK	Clock Frequency	1	80	MHz
TCH	Clock high time	5		ns
TCL	Clock low time	5		ns
TLS1	CS fall to First Rising CLK Edge	50		ns
TSET	Data input Setup Time	4		ns
THOL	Data input Hold Time	4		ns
TLH	Minimum idling time between transfers (minimum ss high time)	5		ns

5.7.5 SPIFC Timing Specification

Figure 5-12 SPIFC Serial Input Timing Diagram



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Figure 5-13 SPIFC Out Timing Diagram

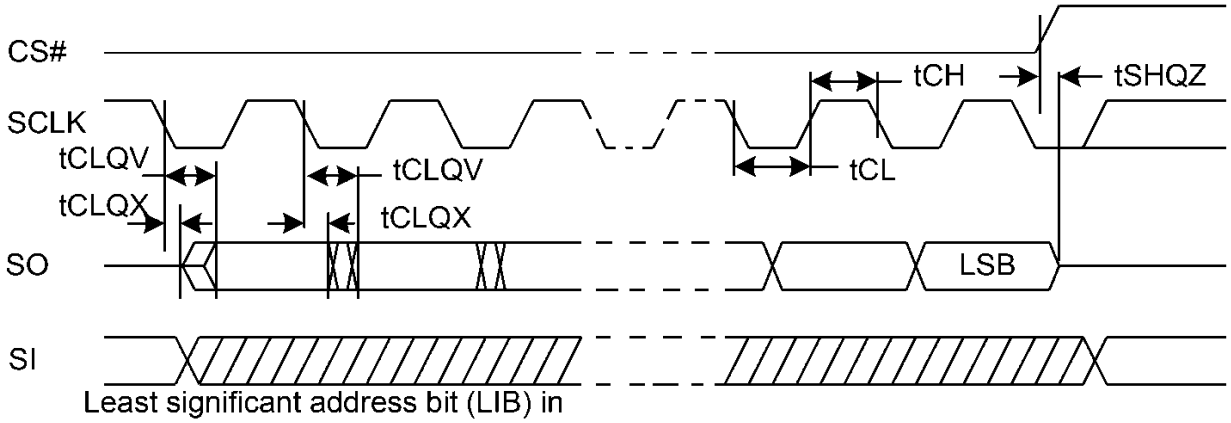


Table 5-16 SPIFC Master Timing Specification

Symbol	Parameter (Clock 41.7MHz)	Min	Max	Unit
fRSCLK	Clock Frequency for READ instructions		50	Mhz
tCH	Clock High Time	8		ns
tCL	Clock Low Time	8		ns
tCLCH	Clock Rise Time (peak to peak)	0.1		V/ns
tCHCL	Clock Fall Time (peak to peak)	0.1		V/ns
tSLCH	CS# Active Setup Time (relative to SCLK)	4	-	ns
tCHSH	CS# Active Hold Time (relative to SCLK)	4	-	ns
tDVCH	Data In Setup Time	2	-	ns
tCHDX	Data In Hold Time	3	-	ns
tSHQZ	Output Disable Time (relative to CS#)		8	ns
tCLQV	Clock Low to Output Valid		6	ns
tCLQX	Output Hold Time	1		ns

5.7.6 Audio Timing Specification

There are two modes for the audio I2S/TDM interface: Master mode and Slave mode, as shown below.

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Figure 5-14 I2S/TDM Timing Diagram, Master Mode

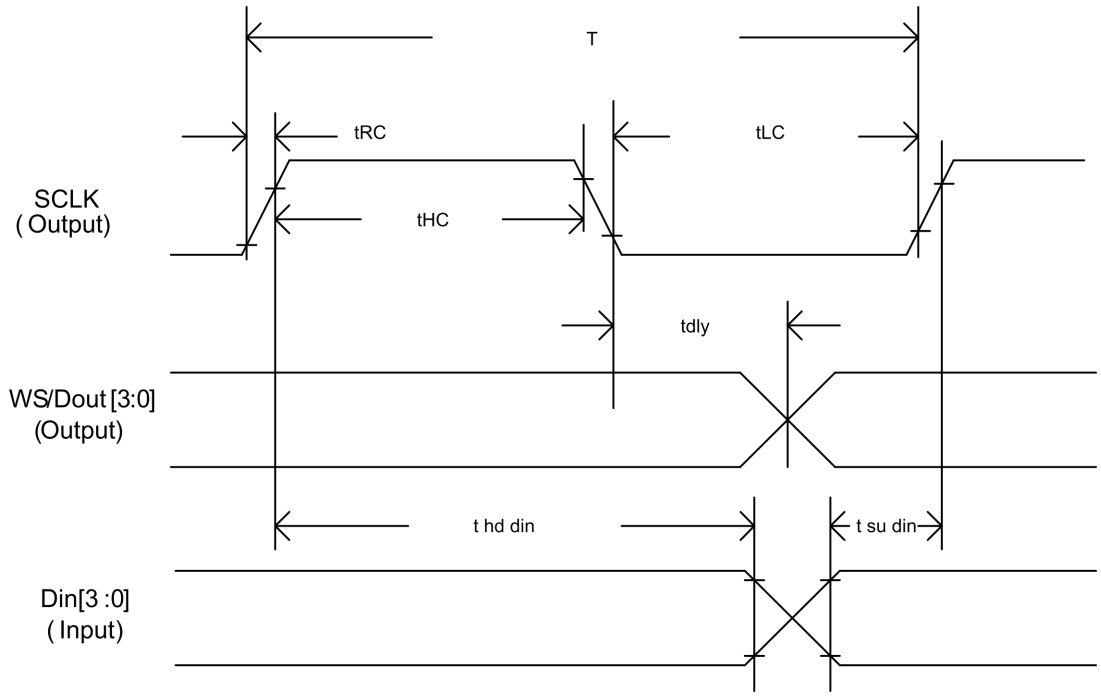


Table 5-17 Audio I2S/TDM Timing Specification, Transmitter, Master Mode

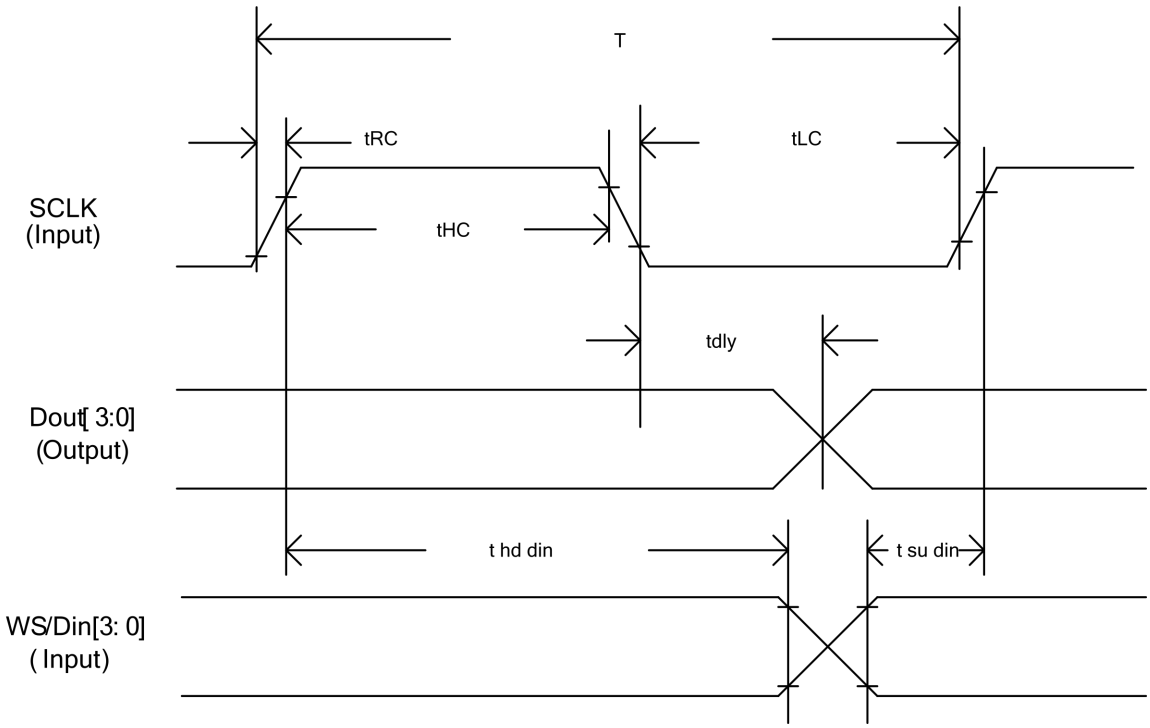
Transmitter (master mode)					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
T	Clock period	10			ns
tHC	High level of SCLK	0.4			T
tLC	Low level of SCLK	0.4			T
tRC	Edge time of SCLK			0.8	ns
tdly	Delay from SCLK to WS	-2	3	5	
tsuin	Setup time of Din	4			ns
thdin	Hold time of Din	4			ns

Note

Measure Pointrefers to VIH, ViL parameter of Normal GPIO Specifications.

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Figure 5-15 2S/TDM Timing Diagram, Slave Mode



Transmitter (slave mode)					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**unit**
T(out)	Clock period	40			ns
T(in)	Clock period	10			ns
tHC	High level of SCLK	0.4			T
tLC	Low level of SCLK	0.4			T
tRC	Edge time of SCLK			0.8	ns
tsu in	Setup time of WS/Din	4			ns
thd in	Hold time of WS/ Din	4			ns
tdly	Delay between SCLK and Dout	2	12	15	ns

Note

Measure Pointrefers to VIH, ViL parameter of Normal GPIO Specifications.

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5.7.7 PDM Timing Specification

Figure 5-16 PDM Timing Diagram

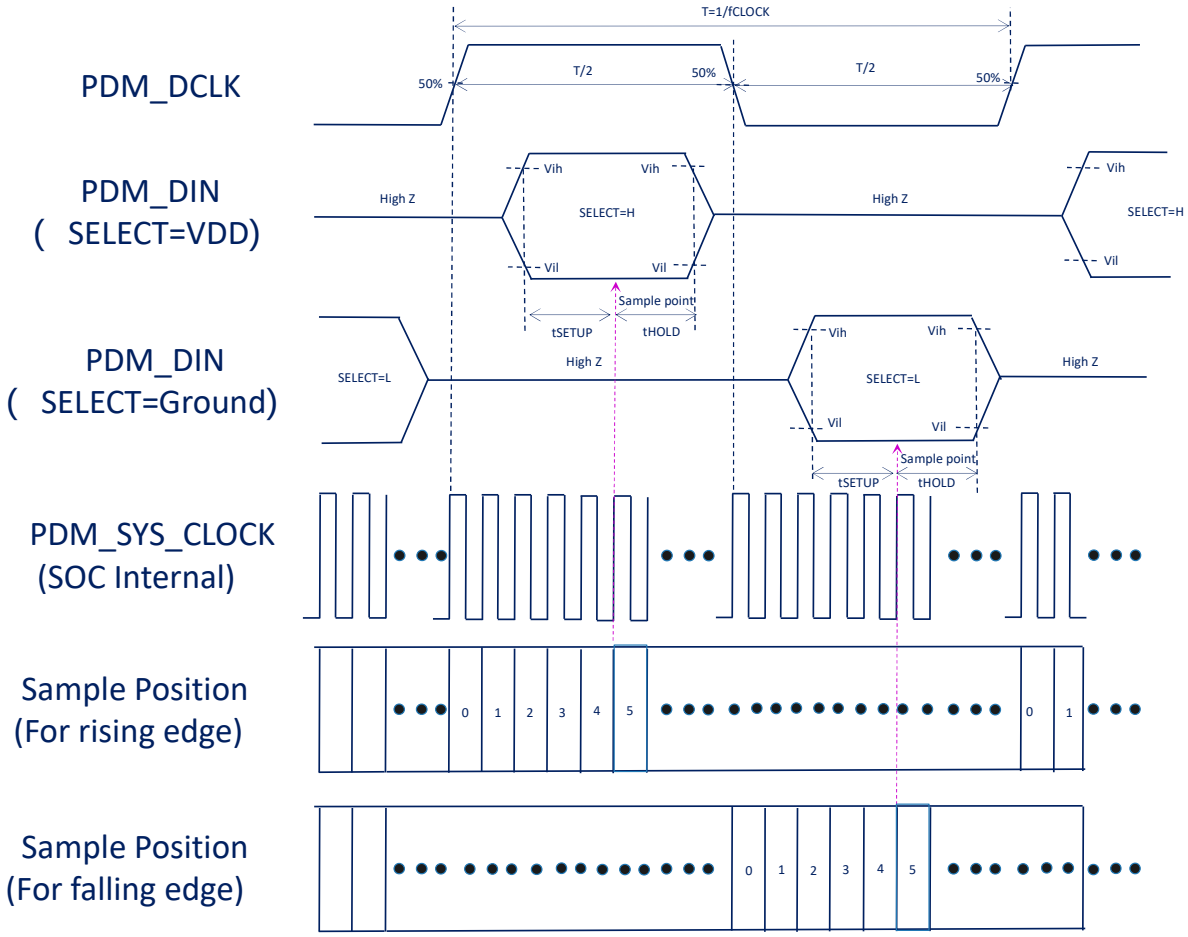


Table 5-18 PDM Timing Specification

Parameter	Symbol	Min.	Typ.	Max.	Units.
PDM clock period	tDCLK	200			ns
PDM clock duty cycle	tHIGH/tLOW	48%		52%	tDCLK
PDM Data setup time	tSETUP	20			ns
PDM Data hold time	tHOLD	20			ns
Sys clock period	tSYSCLK	5	7.5		ns

Note

1. Default PDM_SYS_CLOCK=133MHz.
2. For Sample position, please refer to PDM register PDM_CHAN_CTRL,PDM_CHAN_CTRL1.

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5.7.8 UART Timing Specification

Figure 5-17 UART Timing Diagram

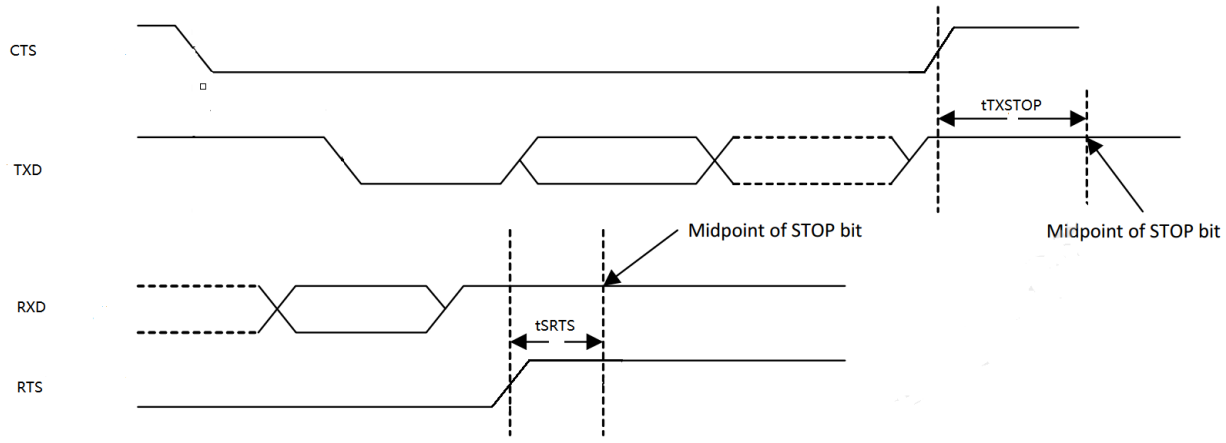


Table 5-19 UART Timing Specification

Parameter	Symbole	Min.	Max.	Units.
Delay time, CTS high before midpoint of stop bit	tTXSTOP	-	0.5	Bit Periods
Delay time, midpoint of stop bit to RTS hgih	tSRTS	-	0.5	Bit Periods

5.8 Power On Config

3 Boot pins are used as power on config (POC) pins, to set the booting sequence.

POC setting is latched at the rising edge of reset signal.

3 POC pins are all pull high internal, CPU will try to boot from nand/eMMC first, if fails then try to boot from SD CARD, still fails then try to boot from USB (PC).

External 4.7K ohm pull down resistors can be used to change the POC setting. The resistors should be placed on right location, avoid stubs on high speed signals.

The SoC's Power On Configuration is listed as following:

Table 5-20 Power On Configuration Pin Table

POC	Boot Pin	Name	Pull low	Pull high
POC_1	GPIOB_1	STORAGE_1	SPINAND boot first	-
POC_2	GPIOB_2	STORAGE_2	NAND Flash boot first	-
POC_4	GPIOB_4	SDCARD_FIRST	SDCARD boot first	Default storage boot
POC_5	GPIOB_5	USB_FIRST	USB boot first	Default storage boot

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Table 5-21 Booting Sequence Diagram

No.	GPIOB_5 POC5	GPIOB_4 POC4	GPIOB_2 POC2	GPIOB_1 POC1	1st	2nd	3rd	4th	5th
1	0	0	0	0	SD	SPINOR	eMMC	NAND	USB
2	0	0	0	1	SD	NAND	eMMC	SPI-NAND	USB
3	0	0	1	0	SD	SPI-NAND	eMMC	NAND	USB
4	0	0	1	1	SD	eMMC	NAND	SPI-NAND	USB
5	0	1	0	0	USB	SPINOR	eMMC	NAND	SD
6	0	1	0	1	USB	NAND	eMMC	SPI-NAND	SD
7	0	1	1	0	USB	SPI-NAND	eMMC	NAND	SD
8	0	1	1	1	USB	eMMC	NAND	SPI-NAND	SD
9	1	0	0	0	SD	SPINOR	eMMC	NAND	USB
10	1	0	0	1	SD	NAND	eMMC	SPI-NAND	USB
11	1	0	1	0	SD	SPI-NAND	eMMC	NAND	USB
12	1	0	1	1	SD	eMMC	NAND	SPI-NAND	USB
13	1	1	0	0	SPINOR	eMMC	NAND	SD	USB
14	1	1	0	1	NAND	eMMC	SPI-NAND	SD	USB
15	1	1	1	0	SPI-NAND	eMMC	NAND	SD	USB
16	1	1	1	1	eMMC	NAND	SPI-NAND	SD	USB

5.9 Power On Reset

The POR(Power On Reset) monitors VDDIO_D power voltage and compares it to a threshold Voltage.

RESET_N pin is low (SOC is reset mode) when VDDIO_D is below threshold,

Force SOC enter reset mode via key to GND serial 100R resitor.

Note

1. Place 1nF capacitors on RESET_N Pin.
2. VDDIO_D power pin is only support 3.3V, not allow to power off in sleep mode.

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Figure 5-18 POR Wave Diagram

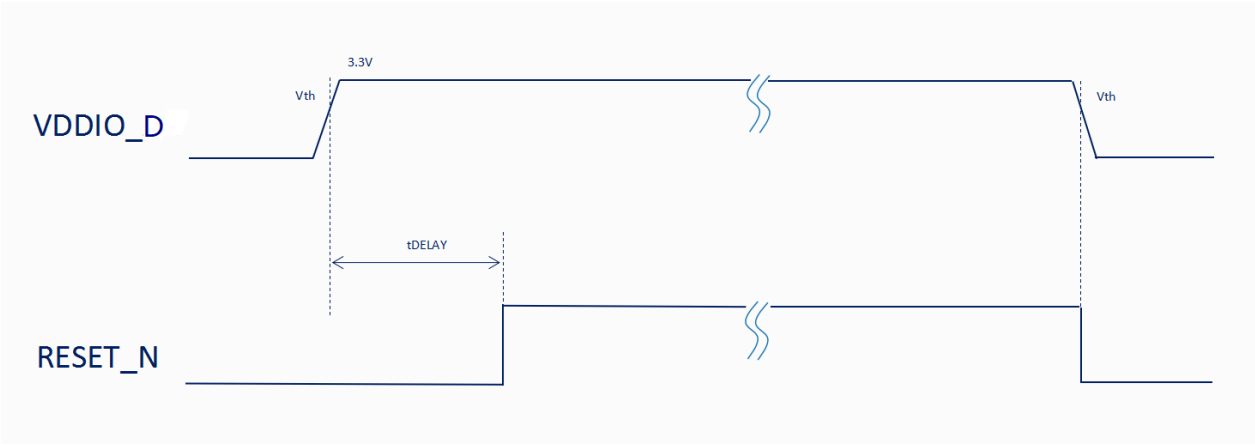
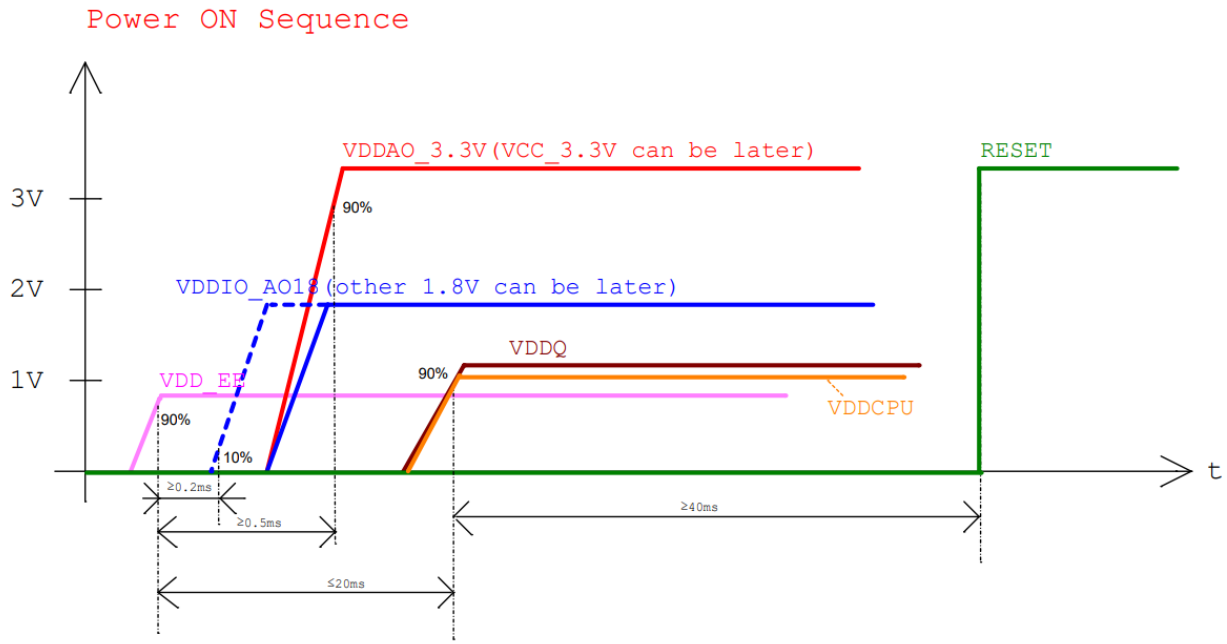


Table 5-22 POR Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Reset threshold for power up	Vth+	-	-	2.9	V
Reset threshold for power down	Vth-	2.5	-	-	V
Reset delay time	tDELAY	109	170	218	ms

5.10 Recommended Power on Sequence

Example power on sequence:



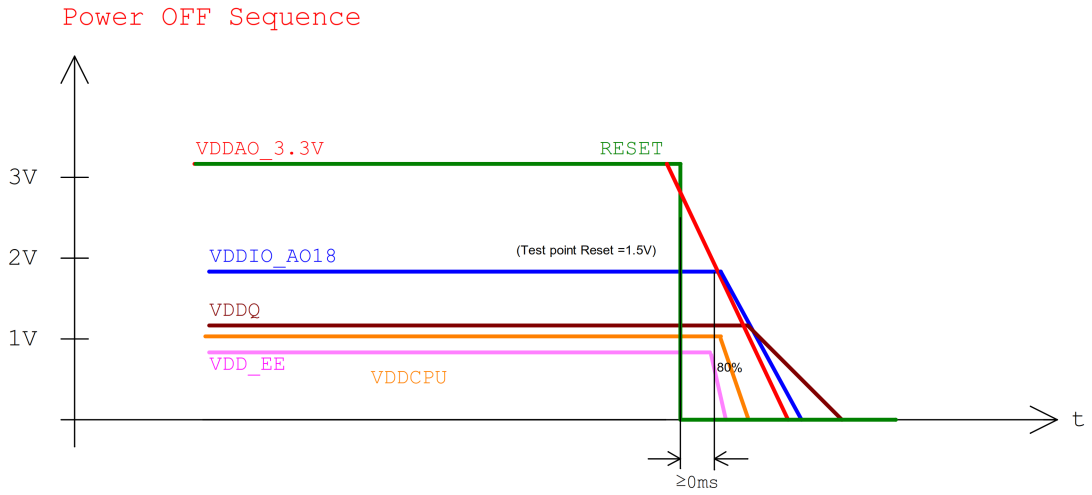
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Note

1. All test values refer to 90% or 10% of typical power voltage.
2. VDDAO_3.3V & VCC3.3V should ramp up > 0.5ms later than VDD_EE.
3. All power sources should get stable within 20ms (except for DDR_VDDQ).
4. No sequence requirement between VDDCPU & DDR_VDDQ and other power source.
5. VDDIO_AO18(10%) should ramp up > 0.2ms later than VDD_EE(90%).
6. VDDIO_AO18 should ramps up earlier than or at the same time with VDDAO_3.3V & VCC3.3V, VDDAO_3.3V & VCC3.3V should never be 2.5V higher than VDDIO_AO18.
7. In some designs, VDDCPU & VDD_EE are merged to VCC_CORE, the power on sequence should be same as VDD_EE.
8. RESET_n should keep low for at least 40ms after power up (except DDR_VDDQ).

Please refer to reference schematics.

The power off sequence is shown in the following figure.



5.11 Power Consumption

Note

Value listed here is estimated typical max value tested. Enough margin in circuit needs to be reserved.

Symbol	Maximum Current (mA)	Note
VDDCPU	1600	-
VDD_EE	1900	-
VDDQ	1600	Total power of controller and 4pcs DDR4 memory

Symbol	Typical Current (mA)	Maximum Current (mA)	Note
AVDD18_AO	18.88	56	-
AVDD_DDRPLL	8	10	-

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Symbol	Typical Current (mA)	Maximum Current (mA)	Note
AVDD18_USB	25	40	-
AVDD33_USB	1	1.5	-
AVDD0V8_ HDMI	11	14	-
AVDD18_HDMI	25	30	-
AVDD18_ETH	33	40	-
AVDD18_ CVBS_DVB	41	60	-
AVDD18_ AUDIO	3.7	5	-

Note

VDDIO=1.8V, DS=3, output 200MHz clock:

1. IO pad itself consumes about 1.4mA.
2. Driving 50mm trace will consumes about 2.8mA more current.
3. Base #2, add 10pF cap will consumes about 3.6mA more current, total about 7.8mA.
4. When VDDIO=3.3V, GPIO consumes about 70% higher.
5. Internal & external pull down resistor consumes more current.

5.12 Storage and Baking Conditions

The processor is moisture-sensitive device of MSL level 3, defined by IPC/JEDEC J-STD-020. Please follow the storage and backing guidelines.

1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).
2. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
   a. Mounted with 168 hours of factory conditions ≤30°C/60% RH, or
   b. Stored per J-STD-033
3. Devices require bake, before mounting, if Humidity Indicator Card reads >10%.
4. If baking is required, refer IPC/JEDEC J-STB-033 for baking process.

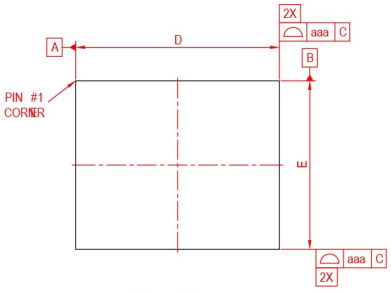
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6 Mechanical Dimensions

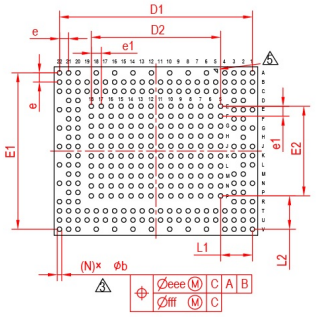
The SoC comes in a 22x18 ball matrix WBBGA RoHS package. The mechanical dimensions are given in millimeters as the following figures.

Figure 6-1 Dimensions

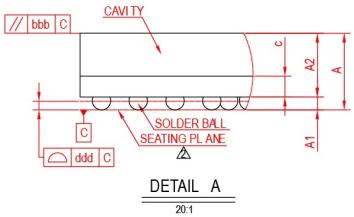
symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.350	---	---	0.053
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.990	1.040	1.090	0.039	0.041	0.043
c	0.300	0.340	0.380	0.012	0.013	0.015
D	13.200	13.300	13.400	0.520	0.524	0.528
E	10.900	11.000	11.100	0.429	0.433	0.437
D1	---	12.600	---	---	0.496	---
E1	---	10.200	---	---	0.402	---
D2	---	8.450	---	---	0.333	---
E2	---	5.850	---	---	0.230	---
L1	---	2.075	---	---	0.082	---
L2	---	2.175	---	---	0.086	---
e	---	0.600	---	---	0.024	---
e1	---	0.650	---	---	0.026	---
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Di am	0.300			0.012		
N	315			315		
MD/ME	22/18			22/18		



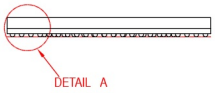
Top View



Bott om Vi ew



DETAIL A
20:1



Si de View

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7 System

This chapter describes the S905Y4 system architecture.

7.1 Memory Map

Memory map of S905Y4 is listed in the following table.

Table 7-1 Memory Map

START	END	REGION (NORMAL)
FFFF8000	FFFFFFFF	ROM_MMU
FFFF2000	FFFF7FFF	ROM_DFU
FFFE0000	FFFF1FFF	ROM_MAIN
FFF08000	FFFDFFFF	reserved
FFF00000	FFF07FFF	gic
FFE00000	FFEFFFFF	gpv/nic
FF600000	FFDFFFFF	coresight/cpu_dbg
FF050000	FF5FFFFF	reserved
FF040000	FF04FFFF	ge2d
FF000000	FF03FFFF	vpu
FE500000	FEFFFFFF	reserved
FE480000	FE4FFFFF	reserved
FE440000	FE47FFFF	SECTOP
FE400000	FE43FFFF	mali
FE380000	FE3FFFFF	reserved
FE370000	FE37FFFF	resrved
FE360000	FE36FFFF	resrved
FE350000	FE35FFFF	demod_comb
FE340000	FE34FFFF	reserved
FE330000	FE33FFFF	audio
FE320000	FE32FFFF	dos
FE310000	FE31FFFF	reserved
FE300000	FE30FFFF	hdmitx
FE0A0000	FE2FFFFF	reserved
FE09E000	FE09FFFF	aucpu
FE09C000	FE09DFFF	aocpu
FE09A000	FE09BFFF	reserved
FE098000	FE099FFF	reserved
FE096000	FE097FFF	reserved
FE094000	FE095FFF	reserved
FE092000	FE093FFF	reserved

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START	END	REGION (NORMAL)
FE090000	FE091FFF	axi_sram
FE08E000	FE08FFFF	reserved
FE08C000	FE08DFFF	emmcC
FE08A000	FE08BFFF	emmcB
FE088000	FE089FFF	emmcA
FE086000	FE087FFF	reserved
FE084000	FE085FFF	ir_top
FE082000	FE083FFF	reserved
FE080000	FE081FFF	uart_e
FE07E000	FE07FFFF	uart_d
FE07C000	FE07DFFF	uart_c
FE07A000	FE07BFFF	uart_b
FE078000	FE079FFF	uart_a
FE076000	FE077FFF	reserved
FE074000	FE075FFF	reserved
FE072000	FE073FFF	reserved
FE070000	FE071FFF	reserved
FE06E000	FE06FFFF	i2c_m_e
FE06C000	FE06DFFF	i2c_m_d
FE06A000	FE06BFFF	i2c_m_c
FE068000	FE069FFF	i2c_m_b
FE066000	FE067FFF	i2c_m_a
FE064000	FE065FFF	i2c_s_a
FE062000	FE063FFF	reserved
FE060000	FE061FFF	pwm_ij
FE05E000	FE05FFFF	pwm_gh
FE05C000	FE05DFFF	pwm_ef
FE05A000	FE05BFFF	pwm_cd
FE058000	FE059FFF	pwm_ab
FE056000	FE057FFF	spifc
FE054000	FE055FFF	reserved
FE052000	FE053FFF	reserved
FE050000	FE051FFF	spicc_0
FE04E000	FE04FFFF	reserved
FE04C000	FE04DFFF	reserved
FE04A000	FE04BFFF	reserved
FE048000	FE049FFF	msr_clk

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START	END	REGION (NORMAL)
FE046000	FE047FFF	aififo
FE044000	FE045FFF	cec
FE042000	FE043FFF	RSA
FE040000	FE041FFF	reserved
FE03E000	FE03FFFF	usb_ph1
FE03C000	FE03DFFF	usb_ph0
FE03A000	FE03BFFF	usb_comb
FE038000	FE039FFF	Smart Card
FE036000	FE037FFF	dmc
FE034000	FE035FFF	reserved
FE032000	FE033FFF	htx_hdcp22 Note: The same HDCP2.2 register sets support both HDCP 2.2 and HDCP 2.3.
FE030000	FE031FFF	reserved
FE02E000	FE02FFFF	startup
FE02C000	FE02DFFF	reserved
FE02A000	FE02BFFF	reserved
FE028000	FE029FFF	eth_phy
FE026000	FE027FFF	sar_adc
FE024000	FE025FFF	eth_top
FE022000	FE023FFF	temp_sensor_ddr
FE020000	FE021FFF	temp_sensor_pll
FE01E000	FE01FFFF	reserved
FE01C000	FE01DFFF	reserved
FE01A000	FE01BFFF	acodec_ctrl
FE018000	FE019FFF	reserved
FE016000	FE017FFF	reserved
FE014000	FE015FFF	reserved
FE012000	FE013FFF	capu
FE010000	FE011FFF	sys_ctrl
FE00E000	FE00FFFF	cpu_ctrl
FE00C000	FE00DFFF	pwr_ctrl
FE00A000	FE00BFFF	irq_ctrl
FE008000	FE009FFF	ana_ctrl
FE006000	FE007FFF	mailbox
FE004000	FE005FFF	pad_ctrl
FE002000	FE003FFF	reset_ctrl

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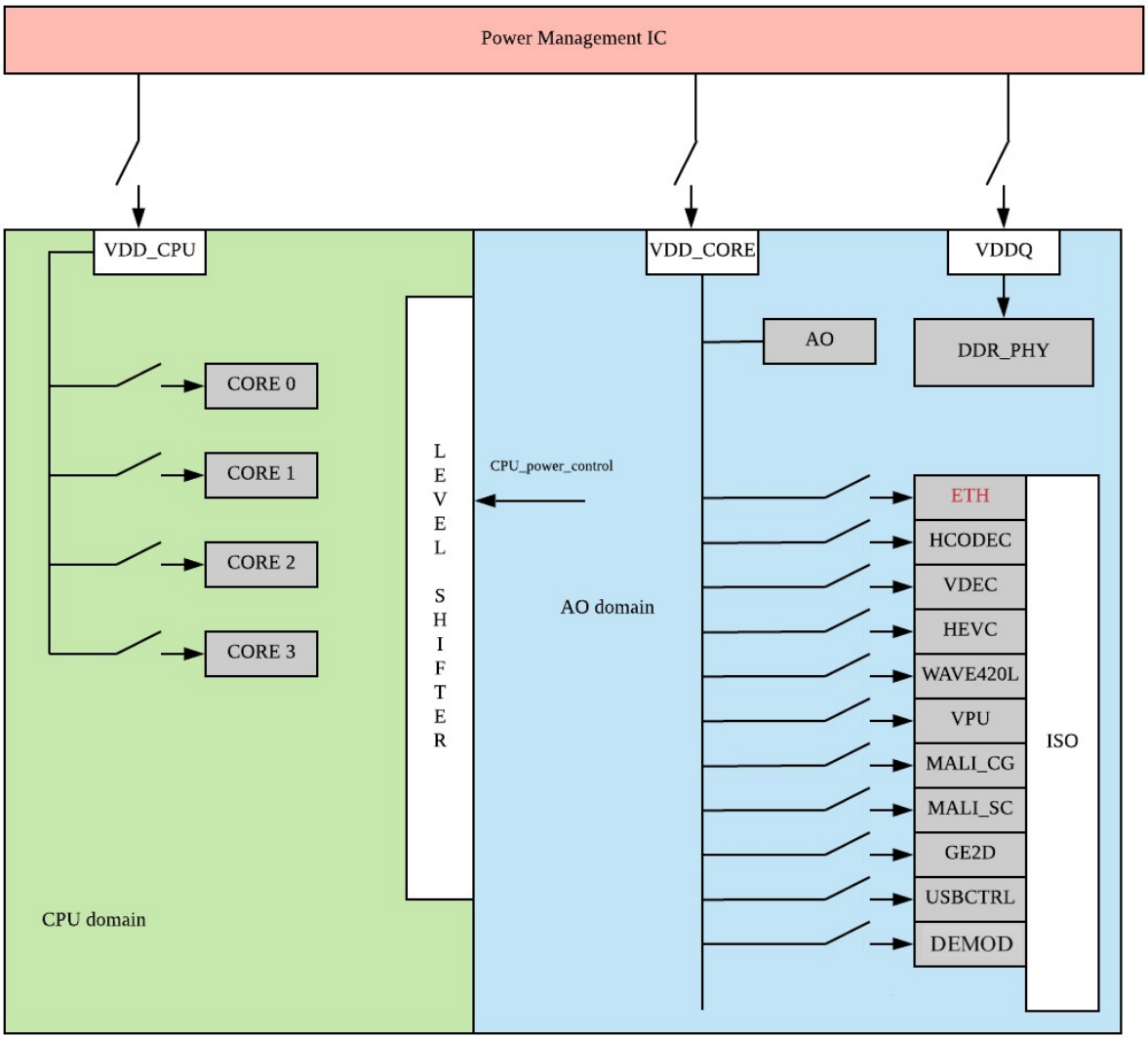
START	END	REGION (NORMAL)
FE000000	FE001FFF	clk_ctrl
FDF00000	FDFFFFFF	reserved
FDE00000	FDEFFFFF	usb0
FDD00000	FDDFFFFF	usb1
FDC10000	FDCFFFFF	reserved
FDC00000	FDC0FFFF	eth
FDB00000	FDBFFFFF	reserved
FD000000	FDAFFFFF	reserved
FC000000	FCFFFFFF	ddr_ctrl
F8000000	FBFFFFFF	reserved
F7048000	F7FFFFFF	reserved
F7000000	F7047FFF	axi srama
F5000000	F6FFFFFF	reserved
F1000000	F4FFFFFF	flash

7.2 Power Domain

The following figure shows the power domain of S905Y4.

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Figure 7-1 Power Domain



7.2.1 Overview

This chapter describes the power domain.

1. CPU work at VDD_CPU; all other work at VDD_CORE.
2. All power control include:
   - PWR_OFF(wr/rd): set 1 will cut power supply;
   - PWR_ACK(rd): the status of power status; 1: power is off; 0: power is on;
   - ISO_EN(wr/rd): set 1 will isolate output;
   - FOCRST(wr/rd): set 1 will keep module as reset status;
   - MEMPD(wr/rd):
     set 2'b11 will power off memory; the power of memory is different path from logic;
3. For MALI power domain: CG(core group) and SC(shader core), the power control is inside of IP.
4. For CPU, the power control support FSM; the details descripted blow.

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5. For other common power domain, all PWR_ACK/PWR_OFF/ISO_EN/FOCRST will follow the same sequence for each bit connection, and MEMPD will connect by different sequence.

Bit	Module	Default
31		
30		
29		
28		
27		
26		
25		
24	DEMOE	OFF
23	ETH	ON
22		
21		
20		
19		
18		
17		
16	GE2D	OFF
15		
14	USBCTRL	ON
13		
12	VPU	OFF
11		
10	DOS_VDEC	OFF
9	DOS_HEVC	OFF
8		
7		
6		
5		
4		
3		
2		
1		
0		

7.2.2 Register Description

For below registers the base address is 0xfe00c000.

Each register final address = BASE + address * 4.

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The following lists describe the mapping between each PWRCTRL register and its address.

PWRCTRL_PWR_ACK0 0xfe00c000
PWRCTRL_PWR_ACK1 0xfe00c004
PWRCTRL_PWR_OFF0 0xfe00c010
PWRCTRL_PWR_OFF1 0xfe00c014
PWRCTRL_ISO_EN0 0xfe00c020
PWRCTRL_ISO_EN1 0xfe00c024
PWRCTRL_FOCRST0 0xfe00c030
PWRCTRL_FOCRST1 0xfe00c034
PWRCTRL_MEM_PD0 0xfe00c040
PWRCTRL_MEM_PD1 0xfe00c044
PWRCTRL_MEM_PD2 0xfe00c048
PWRCTRL_MEM_PD3 0xfe00c04c
PWRCTRL_MEM_PD4 0xfe00c050
PWRCTRL_MEM_PD5 0xfe00c054
PWRCTRL_MEM_PD6 0xfe00c058
PWRCTRL_MEM_PD7 0xfe00c05c
PWRCTRL_MEM_PD8 0xfe00c060
PWRCTRL_MEM_PD9 0xfe00c064
PWRCTRL_MEM_PD10 0xfe00c068
PWRCTRL_MEM_PD11 0xfe00c06c
PWRCTRL_MEM_PD12 0xfe00c070
PWRCTRL_MEM_PD13 0xfe00c074
PWRCTRL_MEM_PD14 0xfe00c078
PWRCTRL_MEM_PD15 0xfe00c07c
PWRCTRL_CPU0_AUTO_OFF_CTRL0 0xfe00c100
PWRCTRL_CPU0_AUTO_OFF_CTRL1 0xfe00c104
PWRCTRL_CPU0_AUTO_OFF_CTRL2 0xfe00c108
PWRCTRL_CPU0_AUTO_OFF_CTRL3 0xfe00c10c
PWRCTRL_CPU0_AUTO_OFF_CTRL4 0xfe00c110
PWRCTRL_CPU0_TIMER_TH_01 0xfe00c120
PWRCTRL_CPU0_TIMER_TH_23 0xfe00c124
PWRCTRL_CPU0_TIMER_TH_45 0xfe00c128
PWRCTRL_CPU0_TIMER_TH_67 0xfe00c12c
PWRCTRL_CPU0_TIMER_TH_89 0xfe00c130
PWRCTRL_CPU0_IRQ_MASK0 0xfe00c140
PWRCTRL_CPU0_IRQ_MASK1 0xfe00c144
PWRCTRL_CPU0_IRQ_MASK2 0xfe00c148

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PWRCTRL_CPU0_IRQ_MASK3 0xfe00c14c
PWRCTRL_CPU0_IRQ_MASK4 0xfe00c150
PWRCTRL_CPU0_IRQ_MASK5 0xfe00c154
PWRCTRL_CPU0_IRQ_MASK6 0xfe00c158
PWRCTRL_CPU0_IRQ_MASK7 0xfe00c15c
PWRCTRL_CPU0_MEMPD_INIT_SET 0xfe00c180
PWRCTRL_CPU0_MEMPD_OFF_SET 0xfe00c184
PWRCTRL_CPU0_MEMPD_ON_A_SET 0xfe00c188
PWRCTRL_CPU0_MEMPD_ON_B_SET 0xfe00c18c
PWRCTRL_CPU0_MEMPD_ON_C_SET 0xfe00c190
PWRCTRL_CPU0_MEMPD_ON_D_SET 0xfe00c194
PWRCTRL_CPU0_MEMPD_STS 0xfe00c198
PWRCTRL_CPU0_FSM_STS0 0xfe00c19c
PWRCTRL_CPU0_FSM_STS1 0xfe00c1a0
PWRCTRL_CPU0_FSM_STS2 0xfe00c1a4
PWRCTRL_CPU0_FSM_START_OFF 0xfe00c1b4
PWRCTRL_CPU0_FSM_START_ON 0xfe00c1b8
PWRCTRL_CPU0_FSM_JUMP 0xfe00c1bc
PWRCTRL_CPU1_AUTO_OFF_CTRL0 0xfe00c1c0
PWRCTRL_CPU1_AUTO_OFF_CTRL1 0xfe00c1c4
PWRCTRL_CPU1_AUTO_OFF_CTRL2 0xfe00c1c8
PWRCTRL_CPU1_AUTO_OFF_CTRL3 0xfe00c1cc
PWRCTRL_CPU1_AUTO_OFF_CTRL4 0xfe00c1d0
PWRCTRL_CPU1_TIMER_TH_01 0xfe00c1e0
PWRCTRL_CPU1_TIMER_TH_23 0xfe00c1e4
PWRCTRL_CPU1_TIMER_TH_45 0xfe00c1e8
PWRCTRL_CPU1_TIMER_TH_67 0xfe00c1ec
PWRCTRL_CPU1_TIMER_TH_89 0xfe00c1f0
PWRCTRL_CPU1_IRQ_MASK0 0xfe00c200
PWRCTRL_CPU1_IRQ_MASK1 0xfe00c204
PWRCTRL_CPU1_IRQ_MASK2 0xfe00c208
PWRCTRL_CPU1_IRQ_MASK3 0xfe00c20c
PWRCTRL_CPU1_IRQ_MASK4 0xfe00c210
PWRCTRL_CPU1_IRQ_MASK5 0xfe00c214
PWRCTRL_CPU1_IRQ_MASK6 0xfe00c218
PWRCTRL_CPU1_IRQ_MASK7 0xfe00c21c
PWRCTRL_CPU1_MEMPD_INIT_SET 0xfe00c240
PWRCTRL_CPU1_MEMPD_OFF_SET 0xfe00c244

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PWRCTRL_CPU1_MEMPD_ON_A_SET 0xfe00c248
PWRCTRL_CPU1_MEMPD_ON_B_SET 0xfe00c24c
PWRCTRL_CPU1_MEMPD_ON_C_SET 0xfe00c250
PWRCTRL_CPU1_MEMPD_ON_D_SET 0xfe00c254
PWRCTRL_CPU1_MEMPD_STS 0xfe00c258
PWRCTRL_CPU1_FSM_STS0 0xfe00c25c
PWRCTRL_CPU1_FSM_STS1 0xfe00c260
PWRCTRL_CPU1_FSM_STS2 0xfe00c264
PWRCTRL_CPU1_FSM_START_OFF 0xfe00c274
PWRCTRL_CPU1_FSM_START_ON 0xfe00c278
PWRCTRL_CPU1_FSM_JUMP 0xfe00c27c
PWRCTRL_CPU2_AUTO_OFF_CTRL0 0xfe00c280
PWRCTRL_CPU2_AUTO_OFF_CTRL1 0xfe00c284
PWRCTRL_CPU2_AUTO_OFF_CTRL2 0xfe00c288
PWRCTRL_CPU2_AUTO_OFF_CTRL3 0xfe00c28c
PWRCTRL_CPU2_AUTO_OFF_CTRL4 0xfe00c290
PWRCTRL_CPU2_TIMER_TH_01 0xfe00c2a0
PWRCTRL_CPU2_TIMER_TH_23 0xfe00c2a4
PWRCTRL_CPU2_TIMER_TH_45 0xfe00c2a8
PWRCTRL_CPU2_TIMER_TH_67 0xfe00c2ac
PWRCTRL_CPU2_TIMER_TH_89 0xfe00c2b0
PWRCTRL_CPU2_IRQ_MASK0 0xfe00c2c0
PWRCTRL_CPU2_IRQ_MASK1 0xfe00c2c4
PWRCTRL_CPU2_IRQ_MASK2 0xfe00c2c8
PWRCTRL_CPU2_IRQ_MASK3 0xfe00c2cc
PWRCTRL_CPU2_IRQ_MASK4 0xfe00c2d0
PWRCTRL_CPU2_IRQ_MASK5 0xfe00c2d4
PWRCTRL_CPU2_IRQ_MASK6 0xfe00c2d8
PWRCTRL_CPU2_IRQ_MASK7 0xfe00c2dc
PWRCTRL_CPU2_MEMPD_INIT_SET 0xfe00c300
PWRCTRL_CPU2_MEMPD_OFF_SET 0xfe00c304
PWRCTRL_CPU2_MEMPD_ON_A_SET 0xfe00c308
PWRCTRL_CPU2_MEMPD_ON_B_SET 0xfe00c30c
PWRCTRL_CPU2_MEMPD_ON_C_SET 0xfe00c310
PWRCTRL_CPU2_MEMPD_ON_D_SET 0xfe00c314
PWRCTRL_CPU2_MEMPD_STS 0xfe00c318
PWRCTRL_CPU2_FSM_STS0 0xfe00c31c
PWRCTRL_CPU2_FSM_STS1 0xfe00c320

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PWRCTRL_CPU2_FSM_STS2 0xfe00c324
PWRCTRL_CPU2_FSM_START_OFF 0xfe00c334
PWRCTRL_CPU2_FSM_START_ON 0xfe00c338
PWRCTRL_CPU2_FSM_JUMP 0xfe00c33c
PWRCTRL_CPU3_AUTO_OFF_CTRL0 0xfe00c340
PWRCTRL_CPU3_AUTO_OFF_CTRL1 0xfe00c344
PWRCTRL_CPU3_AUTO_OFF_CTRL2 0xfe00c348
PWRCTRL_CPU3_AUTO_OFF_CTRL3 0xfe00c34c
PWRCTRL_CPU3_AUTO_OFF_CTRL4 0xfe00c350
PWRCTRL_CPU3_TIMER_TH_01 0xfe00c360
PWRCTRL_CPU3_TIMER_TH_23 0xfe00c364
PWRCTRL_CPU3_TIMER_TH_45 0xfe00c368
PWRCTRL_CPU3_TIMER_TH_67 0xfe00c36c
PWRCTRL_CPU3_TIMER_TH_89 0xfe00c370
PWRCTRL_CPU3_IRQ_MASK0 0xfe00c380
PWRCTRL_CPU3_IRQ_MASK1 0xfe00c384
PWRCTRL_CPU3_IRQ_MASK2 0xfe00c388
PWRCTRL_CPU3_IRQ_MASK3 0xfe00c38c
PWRCTRL_CPU3_IRQ_MASK4 0xfe00c390
PWRCTRL_CPU3_IRQ_MASK5 0xfe00c394
PWRCTRL_CPU3_IRQ_MASK6 0xfe00c398
PWRCTRL_CPU3_IRQ_MASK7 0xfe00c39c
PWRCTRL_CPU3_MEMPD_INIT_SET 0xfe00c3c0
PWRCTRL_CPU3_MEMPD_OFF_SET 0xfe00c3c4
PWRCTRL_CPU3_MEMPD_ON_A_SET 0xfe00c3c8
PWRCTRL_CPU3_MEMPD_ON_B_SET 0xfe00c3cc
PWRCTRL_CPU3_MEMPD_ON_C_SET 0xfe00c3d0
PWRCTRL_CPU3_MEMPD_ON_D_SET 0xfe00c3d4
PWRCTRL_CPU3_MEMPD_STS 0xfe00c3d8
PWRCTRL_CPU3_FSM_STS0 0xfe00c3dc
PWRCTRL_CPU3_FSM_STS1 0xfe00c3e0
PWRCTRL_CPU3_FSM_STS2 0xfe00c3e4
PWRCTRL_CPU3_FSM_START_OFF 0xfe00c3f4
PWRCTRL_CPU3_FSM_START_ON 0xfe00c3f8
PWRCTRL_CPU3_FSM_JUMP 0xfe00c3fc
PWRCTRL_CPUTOP_AUTO_OFF_CTRL0 0xfe00c400
PWRCTRL_CPUTOP_AUTO_OFF_CTRL1 0xfe00c404
PWRCTRL_CPUTOP_AUTO_OFF_CTRL2 0xfe00c408

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PWRCTRL_CPUTOP_AUTO_OFF_CTRL3 0xfe00c40c
PWRCTRL_CPUTOP_AUTO_OFF_CTRL4 0xfe00c410
PWRCTRL_CPUTOP_TIMER_TH_01 0xfe00c420
PWRCTRL_CPUTOP_TIMER_TH_23 0xfe00c424
PWRCTRL_CPUTOP_TIMER_TH_45 0xfe00c428
PWRCTRL_CPUTOP_TIMER_TH_67 0xfe00c42c
PWRCTRL_CPUTOP_TIMER_TH_89 0xfe00c430
PWRCTRL_CPUTOP_IRQ_MASK0 0xfe00c440
PWRCTRL_CPUTOP_IRQ_MASK1 0xfe00c444
PWRCTRL_CPUTOP_IRQ_MASK2 0xfe00c448
PWRCTRL_CPUTOP_IRQ_MASK3 0xfe00c44c
PWRCTRL_CPUTOP_IRQ_MASK4 0xfe00c450
PWRCTRL_CPUTOP_IRQ_MASK5 0xfe00c454
PWRCTRL_CPUTOP_IRQ_MASK6 0xfe00c458
PWRCTRL_CPUTOP_IRQ_MASK7 0xfe00c45c
PWRCTRL_CPUTOP_MEMPD_INIT_SET 0xfe00c480
PWRCTRL_CPUTOP_MEMPD_OFF_SET 0xfe00c484
PWRCTRL_CPUTOP_MEMPD_ON_A_SET 0xfe00c488
PWRCTRL_CPUTOP_MEMPD_ON_B_SET 0xfe00c48c
PWRCTRL_CPUTOP_MEMPD_ON_C_SET 0xfe00c490
PWRCTRL_CPUTOP_MEMPD_ON_D_SET 0xfe00c494
PWRCTRL_CPUTOP_MEMPD_STS 0xfe00c498
PWRCTRL_CPUTOP_FSM_STS0 0xfe00c49c
PWRCTRL_CPUTOP_FSM_STS1 0xfe00c4a0
PWRCTRL_CPUTOP_FSM_STS2 0xfe00c4a4
PWRCTRL_CPUTOP_FSM_START_OFF 0xfe00c4b4
PWRCTRL_CPUTOP_FSM_START_ON 0xfe00c4b8
PWRCTRL_CPUTOP_FSM_JUMP 0xfe00c4bc

PWRCTRL_PWR_ACK0

Read only, the status of each power domain.

PWRCTRL_ISO_EN0

Isolation the interface of each power domain.

PWRCTRL_PWR_OFF0

Power off each power domain.

Table 7-2 PWRCTRL_MEM_PD0

Bit(s)	R/W	Default	Description
31:0	R/W	0xFFFFF-FFF	DOS_VDEC

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Table 7-3 PWRCTRL_MEM_PD1

Bit(s)	R/W	Default	Description
31:0	R/W	0xFFFFFF-FF	RESERVED

Table 7-4 PWRCTRL_MEM_PD2

Bit(s)	R/W	Default	Description
31:0	R/W	0xFFFFF-FFF	DOS_HEVC

Table 7-5 PWRCTRL_MEM_PD3

Bit(s)	R/W	Default	Description
31:0	R/W	0xFFFF-FFFF	RESERVED

Table 7-6 PWRCTRL_MEM_PD4

Bit(s)	R/W	Default	Description
15:0	R/W	0xFFFFFFFF	AUDIO

Table 7-7 PWRCTRL_MEM_PD5

Bit(s)	R/W	Default	Description
31:0	R/W	0xFFFFF-FFF	vpu

Table 7-8 PWRCTRL_MEM_PD6

Bit(s)	R/W	Default	Description
31:0	R/W	0xFFFF-FFFF	vpu

Table 7-9 PWRCTRL_MEM_PD7

Bit(s)	R/W	Default	Description
31:0	R/W	0xFFFFFF-FF	vpu

Table 7-10 PWRCTRL_MEM_PD8

Bit(s)	R/W	Default	Description
31:0	R/W	0xFFFFFFF-F	vpu

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Table 7-11 PWRCTRL_MEM_PD9

Bit(s)	R/W	Default	Description
31:0	R/W	0xFFFFFFF-F	vpu

Table 7-12 PWRCTRL_MEM_PD10

Bit(s)	R/W	Default	Description
1:0	R/W	0x0	DMC

Table 7-13 PWRCTRL_MEM_PD11

Bit(s)	R/W	Default	Description
31:30	R/W	0x0	USBCTRL
29:26	R/W	0xF	RESERVED
25:18	R/W	0xFF	GE2D
17:16	R/W	0x0	DDR
15:8	R/W	0xFF	HDMI
7:6	R/W	0x3	
5:4	R/W	0x3	AUCPU
3:2	R/W	0x0	ETH
1:0	R/W	0x3	

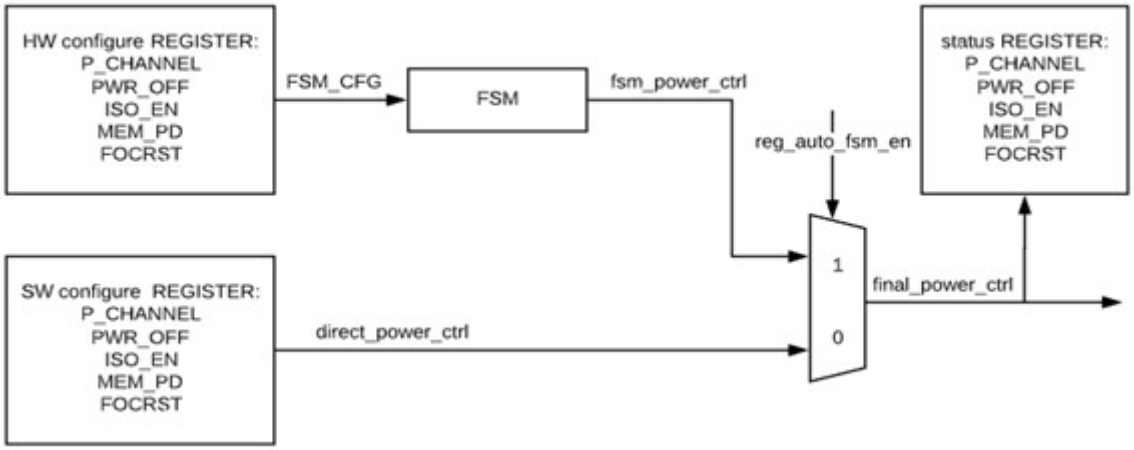
Table 7-14 PWRCTRL_MEM_PD12/13/14/15

Bit(s)	R/W	Default	Description
31:0	R/W	0xFFFFFFF-F	demod

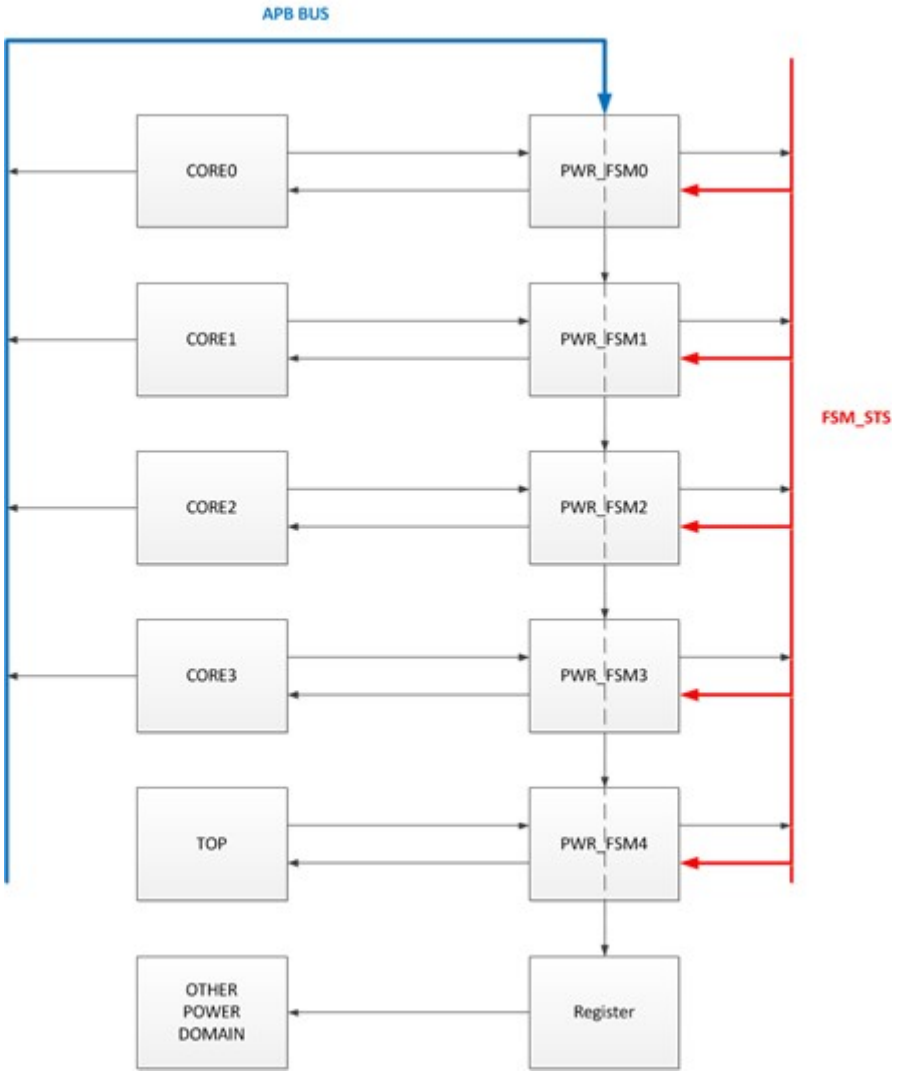
For each CPU power domain, they need power off by itself, so PWR_CTRL include 7 PWR_FSM which can update power related signal by HW.

		Register write permission			
	default	TEE	REE	JTAG	AOCPU
CPU_CORE0	ON	Yes	No	Yes	No
CPU_CORE1	OFF	Yes	No	Yes	No
CPU_CORE2	OFF	Yes	No	Yes	No
CPU_CORE3	OFF	Yes	No	Yes	No
CPU_TOP	ON	Yes	No	Yes	No

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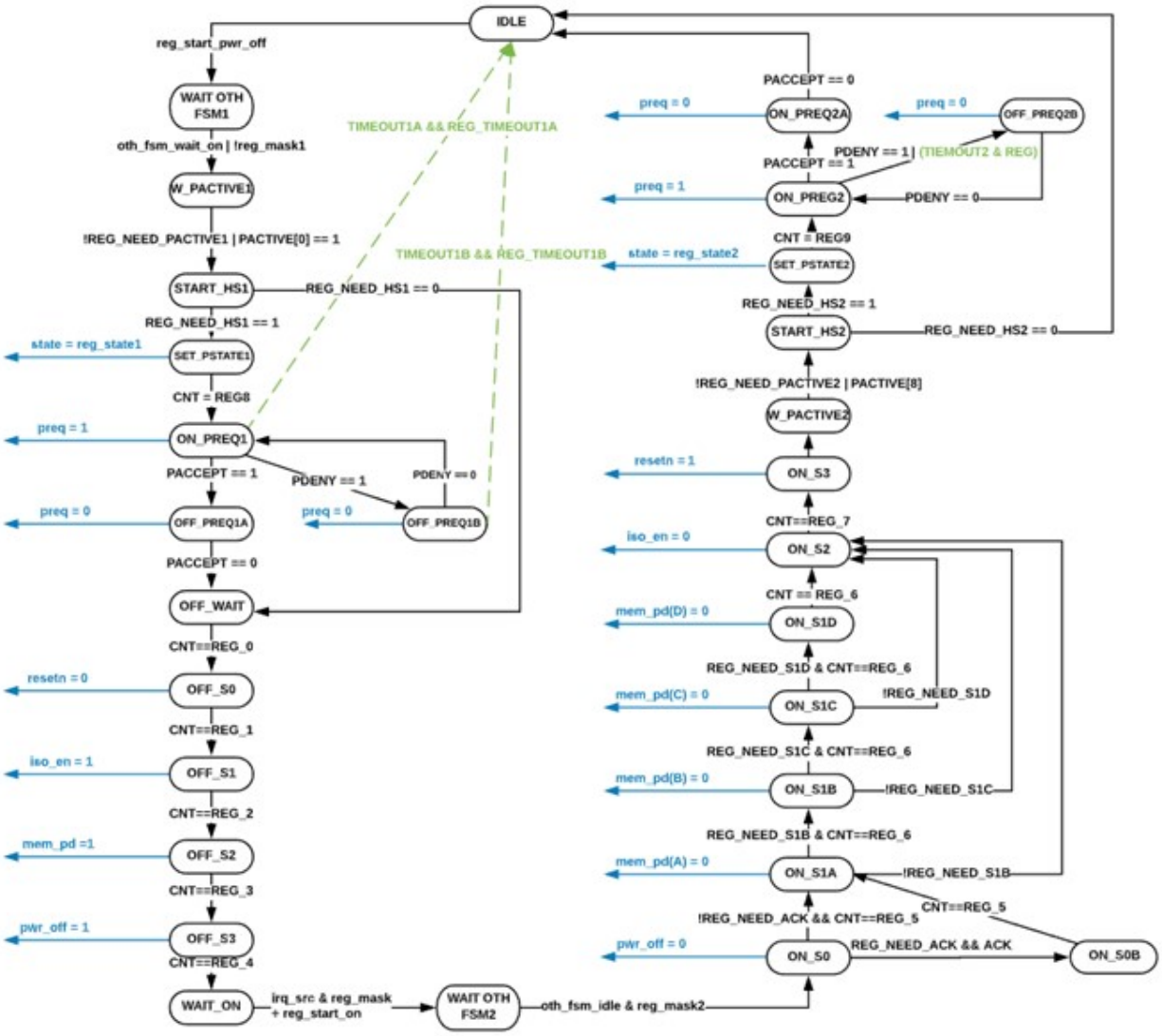


We can off/on these 7 cpu/dsp power domain in serial. For example, off cpu_core0 -> off cpu_top; on cpu_top -> on cpu_core0, so all FSM_STS will send to each FSM.



The power FSM design as blow:

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1. configure all related register first;
2. start_pwr_off;
3. wait for other pwr_fsm status, check is it finished power off flow;
4. start handshake if need (A35 do not need handshake);
5. start power off flow by sequency;
6. wait for interrupt to start power on;
7. wait for other pwr_fsm status, check is it finished power on flow;
8. start power on flow by sequency;
9. start handshake if need;

Table 7-15 PWRCTRL_AUTO_OFF_CTRL0

Bit(s)	R/W	Default	Description
31	R/W	0	REG_FSM_EN
30	R/W	0	REG_GATE_ALL_ON; force all clock gate are on;
29	R/W	0	REG_NEED_ACK_EN; set 1 ,ON_S0 will jump to ON_S0B
27	R/W	0	REG_ACK_INV, set 1, will invert PWR_ACK;

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Bit(s)	R/W	Default	Description
25:24	R/W	0	REG_TIMER_CNT_TICK_SEL; 0:timer_tick = sys_clk; 1:timer_tick = 1us; 2:timer_tick = 10us; 3:timer_tick = 100us;
23	R/W	0	REG_NEED_ON_S1B; set 1, ON_S1A will jump to ON_S1B;
22	R/W	0	REG_NEED_ON_S1C; set 1, ON_S1B will jump to ON_S1C;
21	R/W	0	REG_NEED_ON_S1D; set 1, ON_S1C will jump to ON_S1D;
20	R/W	0	REG_SET_PSTATE; set 1, force pstate = REG_PSTATE;
19	R/W	0	REG_ON_NEED_HS; set 1, START_HS2 will jump to SET_PSTATE2;
18	R/W	0	REG_ON_NEED_PACTIVE; set 1 will force WAIT_PACTIVE2 jump to START_HS2;
17	R/W	0	REG_OFF_NEED_HS; set 1, START_HS1 will jump to SET_PSTATE1;
16	R/W	0	REG_OFF_NEED_PACTIVE; set 1 will force WAIT_PACTIVE1 jump to START_HS1;
11	R/W	0	REG_PWROFF_OFF_SET; PWR_OFF value when FSM_STS = OFF_S3;
10	R/W	0	REG_PWROFF_ON_SET; PWR_OFF value when FSM_STS = ON_S0;
8	R/W	0	REG_PWROFF_INIT_SET; PWR_OFF value when REG_FSM_EN = 0;
7	R/W	0	REG_ISOEN_OFF_SET; ISO_EN value when FSM_STS = OFF_S1;
6	R/W	0	REG_ISOEN_ON_SET; ISO_EN value when FSM_STS = ON_S2;
4	R/W	0	REG_ISOEN_INIT_SET; ISO_EN value when REG_FSM_EN = 0;
3	R/W	0	REG_FOCRST_OFF_SET; FOC_RST value when FSM_STS = OFF_S0;
2	R/W	0	REG_FOCRST_ON_SET; FOC_RST value when FSM_STS = ON_S3;
0	R/W	0	REG_FOCRST_INIT_SET; FOC_RST value when REG_FSM_EN = 0;

Table 7-16 PWRCTRL_*_AUTO_OFF_CTRL1**

Bit(s)	R/W	Default	Description
30:24	R/W	0	reg_timeout_cnt_th_off_b
20:16	R/W	0	reg_fsm_jump_sts

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Bit(s)	R/W	Default	Description
15:8	R/W	0	reg_oth_fsm_on_mask; bit7: reserved; bit6: set 1, FSM_STS will move to ON_S0 when DSPB is IDLE bit5: set 1, FSM_STS will move to ON_S0 when DSPA is IDLE bit4: set 1, FSM_STS will move to ON_S0 when CPU_TOP is IDLE bit3: set 1, FSM_STS will move to ON_S0 when CPU_CORE3 is IDLE bit2: set 1, FSM_STS will move to ON_S0 when CPU_CORE2 is IDLE bit1: set 1, FSM_STS will move to ON_S0 when CPU_CORE1 is IDLE bit0: set 1, FSM_STS will move to ON_S0 when CPU_CORE0 is IDLE
7:0	R/W	0	reg_oth_fsm_off_mask; bit7: reserved; bit6: set 1, FSM_STS will move to WAIT_PACTIVE1 when DSPB is WAIT_ON bit5: set 1, FSM_STS will move to WAIT_PACTIVE1 when DSPA is WAIT_ON bit4: set 1, FSM_STS will move to WAIT_PACTIVE1 when CPU_TOP is WAIT_ON bit3: set 1, FSM_STS will move to WAIT_PACTIVE1 when CPU_CORE3 is WAIT_ON bit2: set 1, FSM_STS will move to WAIT_PACTIVE1 when CPU_CORE2 is WAIT_ON bit1: set 1, FSM_STS will move to WAIT_PACTIVE1 when CPU_CORE1 is WAIT_ON bit0: set 1, FSM_STS will move to WAIT_PACTIVE1 when CPU_CORE0 is WAIT_ON

Table 7-17 PWRCTRL_*_AUTO_OFF_CTRL2**

Bit(s)	R/W	Default	Description
31:16	R/W	0	reg_timeout_cnt_th_on_a
15:0	R/W	0	reg_timeout_cnt_th_off_a

Table 7-18 PWRCTRL_*_AUTO_OFF_CTRL3**

Bit(s)	R/W	Default	Description
23:16	R/W	0	PSTATE value when REG_SET_PSATE = 0
15:8	R/W	0	PSTATE value when FSM_STS = SET_PSTATE1
7:0	R/W	0	PSTATE value when FSM_STS = SET_PSTATE2

Table 7-19 PWRCTRL_*_AUTO_OFF_CTRL4**

Bit(s)	R/W	Default	Description
15:8	R/W	0	irq_clr, each bit can clear pwr_fsm internal irq status;
7:0	R/W	0	irq_en, each bit can enable internal irq to system;

Table 7-20 PWRCTRL_*_TIMER_TH_01**

Bit(s)	R/W	Default	Description
31:16	R/W	0	timer count threshold 1; from OFF_S0 to OFF_S1;
15:0	R/W	0	timer count threshold 0; from OFF_WAIT to OFF_S0;

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Table 7-21 PWRCTRL_*_TIMER_TH_23**

Bit(s)	R/W	Default	Description
31:16	R/W	0	timer count threshold 3; from OFF_S2 to OFF_S3;
15:0	R/W	0	timer count threshold 2; from OFF_S1 to OFF_S2;

Table 7-22 PWRCTRL_*_TIMER_TH_45**

Bit(s)	R/W	Default	Description
31:16	R/W	0	timer count threshold 5; from ON_S0/S0B to ON_S1A;
15:0	R/W	0	timer count threshold 4; from OFF_S3 to WAIT_ON;

Table 7-23 PWRCTRL_*_TIMER_TH_67**

Bit(s)	R/W	Default	Description
31:16	R/W	0	timer count threshold 7; from ON_S2 to ON_S3;
15:0	R/W	0	timer count threshold 6; from ON_S1A/S1B/S1C/S1D to ON_S1B/S1C/S1D/S2;

Table 7-24 PWRCTRL_*_TIMER_TH_89**

Bit(s)	R/W	Default	Description
31:16	R/W	0	timer count threshold 9; from SET_PSTATE2 to ON_PREQ2;
15:0	R/W	0	timer count threshold 8; from SET_PSTATE1 to ON_PREQ1;

Table 7-25 PWRCTRL_*_IRQ_MASK0~7**

Bit(s)	R/W	Default	Description
255:0	R/W	0	each bit: 1: jump to WAIT_OTH_FSM2 by this irq;

Table 7-26 PWRCTRL_*_MEMPD_INIT_SET**

Bit(s)	R/W	Default	Description
31:0	R/W	0	MEMPD value when REG_FSM_EN = 0

Table 7-27 PWRCTRL_*_MEMPD_OFF_SET**

Bit(s)	R/W	Default	Description
31:0	R/W	0	MEMPD value when FSM_STS = OFF_S2

Table 7-28 PWRCTRL_*_MEMPD_ON_A_SET**

Bit(s)	R/W	Default	Description
31:0	R/W	0	MEMPD value when FSM_STS = ON_S1A

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Table 7-29 PWRCTRL_*_MEMPD_ON_B_SET**

Bit(s)	R/W	Default	Description
31:0	R/W	0	MEMPD value when FSM_STS = ON_S1B

Table 7-30 PWRCTRL_*_MEMPD_ON_C_SET**

Bit(s)	R/W	Default	Description
31:0	R/W	0	MEMPD value when FSM_STS = ON_S1C

Table 7-31 PWRCTRL_*_MEMPD_D_SET**

Bit(s)	R/W	Default	Description
31:0	R/W	0	MEMPD value when FSM_STS = ON_S1D

Table 7-32 PWRCTRL_*_MEMPD_STS**

Bit(s)	R/W	Default	Description
31:0	R	0	final MEM_PD output

Table 7-33 PWRCTRL_*_FSM_STS0**

Bit(s)	R/W	Default	Description

31:24	R	0	FSM_PWR internal irq sts;
			bit7: timeout_cnt_a > reg_timeout_cnt_th_off_a when FSM_STS = OFF_PREQ1;
			bit6: timeout_cnt_a > reg_timeout_cnt_th_on_a when FSM_STS = ON_PREQ1;
			bit5: timeout_cnt_b > reg_timeout_cnt_th_off_b when FSM_STS = OFF_PREQ1B;
			bit4: FSM_STS change to ON_START_HS;
			bit4: FSM_STS change to ON_S1A;
			bit3: FSM_STS change to OFF_WAIT;
			bit2: FSM_STS change to WAIT_ON;
			bit0: FSM_STS change to IDLE;

23:17	R	0	timeout_cnt_b add by FSM sts change: from ON_PREQ1 to OFF_PREQ1B; clear at FSM sts is OFF_PREQ1A and SET_PSTATE1
16:12	R	0	current FSM sts: 0:IDLE 1:WAIT_OTH_FSM1 2:WAIT_PACTIVE1 3:START_HS1 4:SET_PSTATE1 5:ON_PREQ1 6:OFF_PREQ1B 7:OFF_PREQ1A 8:OFF_WAIT 9:OFF_S0 10:OFF_S1 11:OFF_S2 12:OFF_S3 16:WAIT_ON 17:WAIT_OTH_FSM2

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Bit(s)	R/W	Default	Description
			18:ON_S0 19:ON_S0B 20:ON_S1A 21:ON_S1B 22:ON_S1C 23:ON_S1D 24:ON_S2 25:ON_S3 26:WAIT_PACTIVE2 27:START_HS2 28:SET_PACTIVE2 29:ON_PREQ2 30:OFF_PREQ2B 31:OFF_PREQ2A
11	R	0	final PREQ output
10	R	0	final PWR_OFF output
9	R	0	final FOC_RST output
8	R	0	final ISO_EN output
7:0	R	0	final PSTATE output

Table 7-34 PWRCTRL_*_FSM_STS1**

Bit(s)	R/W	Default	Description
31:16	R	0	timeout_cnt_a add by clock when FSM sts is ON_PREQ1/ON_PREQ2; clear if FSM sts is other sts;
15:0	R	0	r_timer_cnt add by timer_tick; clear if FSM sts changed;

Table 7-35 PWRCTRL_*_FSM_STS2**

Bit(s)	R/W	Default	Description
29:25	R	0	history5
24:20	R	0	history4
19:15	R	0	history3
14:10	R	0	history2
9::5	R	0	history1
4:0	R	0	history0

Table 7-36 PWRCTRL_*_FSM_START_OFF**

Bit(s)	R/W	Default	Description
31:0	W	0	write any value will force FSM start from IDLE to WAIT_OTH_FSM1

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Table 7-37 PWRCTRL_*_FSM_START_ON**

Bit(s)	R/W	Default	Description
31:0	W	0	write any value will force FSM start from WAIT_ON to WAIT_OTH_FSM2

Table 7-38 PWRCTRL_*_FSM_JUMP**

Bit(s)	R/W	Default	Description
31:0	W	0	write any value will force FSM jump to reg_fsm_jump_sts

7.3 System Booting

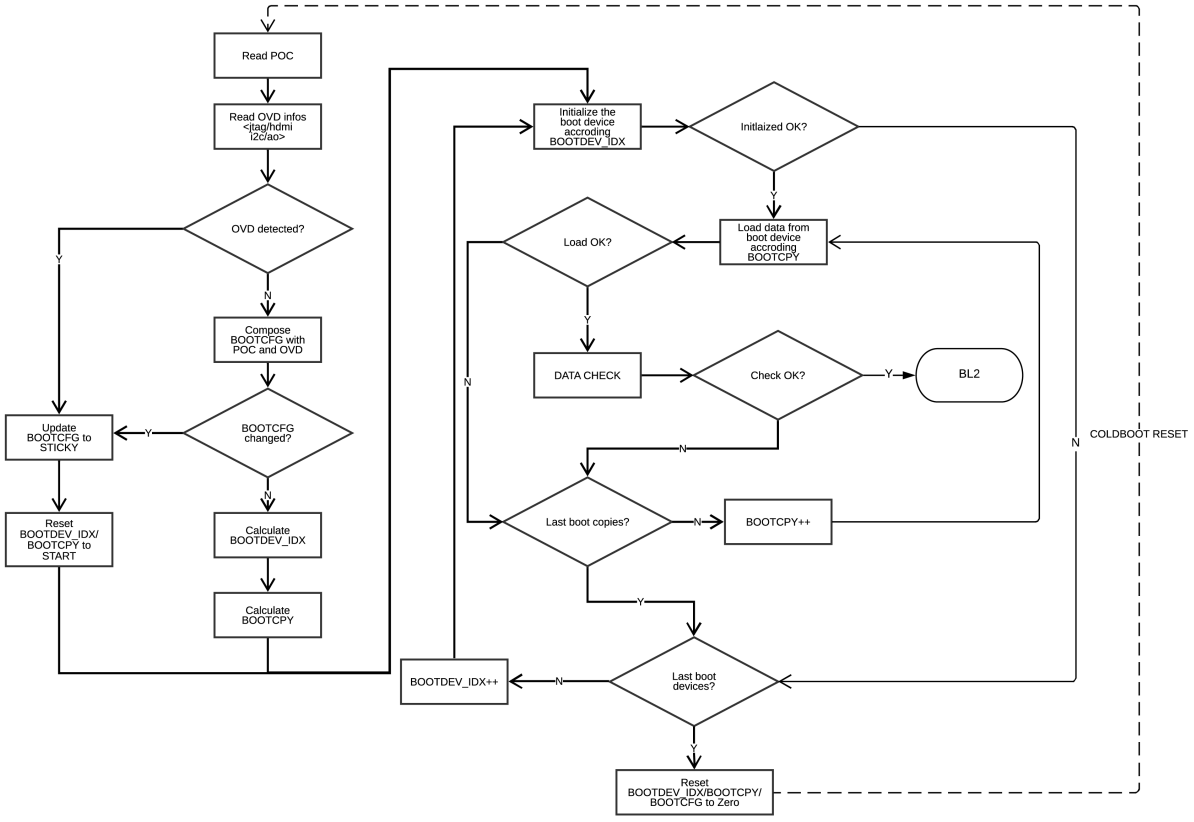
7.3.1 Overview

This part describes the power–on mode configuration of the SoC, which include two portions: Cortex-M3 for security control and A35 for others.

7.3.2 Power-on Flow Chart

The following figure illustrates the SoC's power on sequence.

Figure 7-2 Power-on Flow Chart



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7.4 CPU

The Cortex-A35 subsystem of the chip is highly configurable with low power consumption.

The Cortex-A35 processor features are:

- Full implementation of the ARMv8-A A64, A32, and T32 instruction sets.
- Both the AArch32 and AArch64 execution states at all Exception levels (EL0 to EL3).
- In-order pipeline with direct and indirect branch prediction.
- Separate Level 1 (L1) data and instruction side memory systems with a Memory Management Unit (MMU).
- Level 2 (L2) memory system that provides cluster memory coherency.
- Unified system L2 cache.
- Cache protection in the form of Error Correction Code (ECC) or parity on all RAM instances, except for the L2 victim RAM. There are two implementation options:
  - CPU cache protection.
  - Snoop Control Unit (SCU)-L2 cache protection.
- TrustZone
- Optional data engine that implements the Advanced SIMD and floating-point architecture support.
- Optional Cryptographic Extension. This architectural extension is only available if the data engine is present.
- ARMv8 debug logic.
- Performance Monitoring Unit (PMU).
- Optional Embedded Trace Macrocell (ETM) that supports instruction trace only.
- Optional Generic Interrupt Controller (GIC) CPU interface to connect to an external distributor.
- Generic Timers supporting 64-bit count input from an external system counter.

7.5 GPU

The Mali-G31 MP2 GPU is a hardware accelerator for 2D and 3D graphics system which compatible with the following graphics standards: OpenGL ES 3.2 Vulkan 1.1 and OpenCL 1.2. The developers can follow the ARM and Khronos official reference documents for programming details.

7.6 Clock

7.6.1 Overview

The clock and reset unit is an APB slave module that is designed for generating all of the internal and system clocks, resets of chip. The SoC uses an external 24MHz crystal; there are 9 internal PLLs: SYS_PLL/GP0_PLL/HIFI_PLL/ETHPHY_PLL/USBPHY_PLL0/1/ADC_PLL/MPLL/HDMI_PLL/DDR_PLL, these PLLs generate clock sources, as shown in the following table.

TYPE	OUTPUT CLOCK	MAX FREQ	INTERNAL DIV	Spread Spectrum
SYS_PLL	SYS_CLK_OUT	6G	/1 /2 /4 /8 /16 /32	yes
GP0_PLL	GP0_CLK_OUT	6G	/1 /2 /4 /8 /16 /32	yes
HIFI_PLL	HIFI_CLK_OUT	6G	/1 /2 /4 /8	yes
ETHPHY_PLL	ETH_CLK	500M(fixed)		

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TYPE	OUTPUT CLOCK	MAX FREQ	INTERNAL DIV	Spread Spectrum
USBPHY_PLL0/1	USB_CLK0/1	480M(fixed)		
ADC_PLL	ADC_DPLL_INTCLK	6G		
MPLL	FCLK_DIV2_CPU	1G(fixed)		
	FCLK_DIV3_CPU	666M(fixed)		
	MPLL_CLK_OUT_ DIV2_GPIO	1G(fixed)		
	MPLL_CLK_OUT_ DIV2	1G(fixed)		
	MPLL_CLK_OUT_ DIV2p5	800M(fixed)		
	MPLL_CLK_OUT_ DIV3	666M(fixed)		
	MPLL_CLK_OUT_ DIV4	500M(fixed)		
	MPLL_CLK_OUT_ DIV5	400M(fixed)		
	MPLL_CLK_OUT_ DIV7	285.7M(fixed)		
	MPLL_DDS_CLK0	500M	Up to /32	
	MPLL_DDS_CLK1	500M	Up to /32	
	MPLL_DDS_CLK2	500M	Up to /32	yes
	MPLL_DDS_CLK3	500M	Up to /32	yes
HDMI_PLL	HDMI_CLK_OUT	6G	/1/2/4/8/16	yes
	HDMI_CLK_OUT2	6G	/1/2/4/8/16/32/64	yes
DDR_PLL	DDR_CLK4X_OUT	4.8G	/4 /6 /8 /12 /16 /8 /12 /16 /24 /32	yes
	DDR_CLK_OUT	4.8G	/2 /3 /4 /6 /8	No

7.6.2 Clock Control

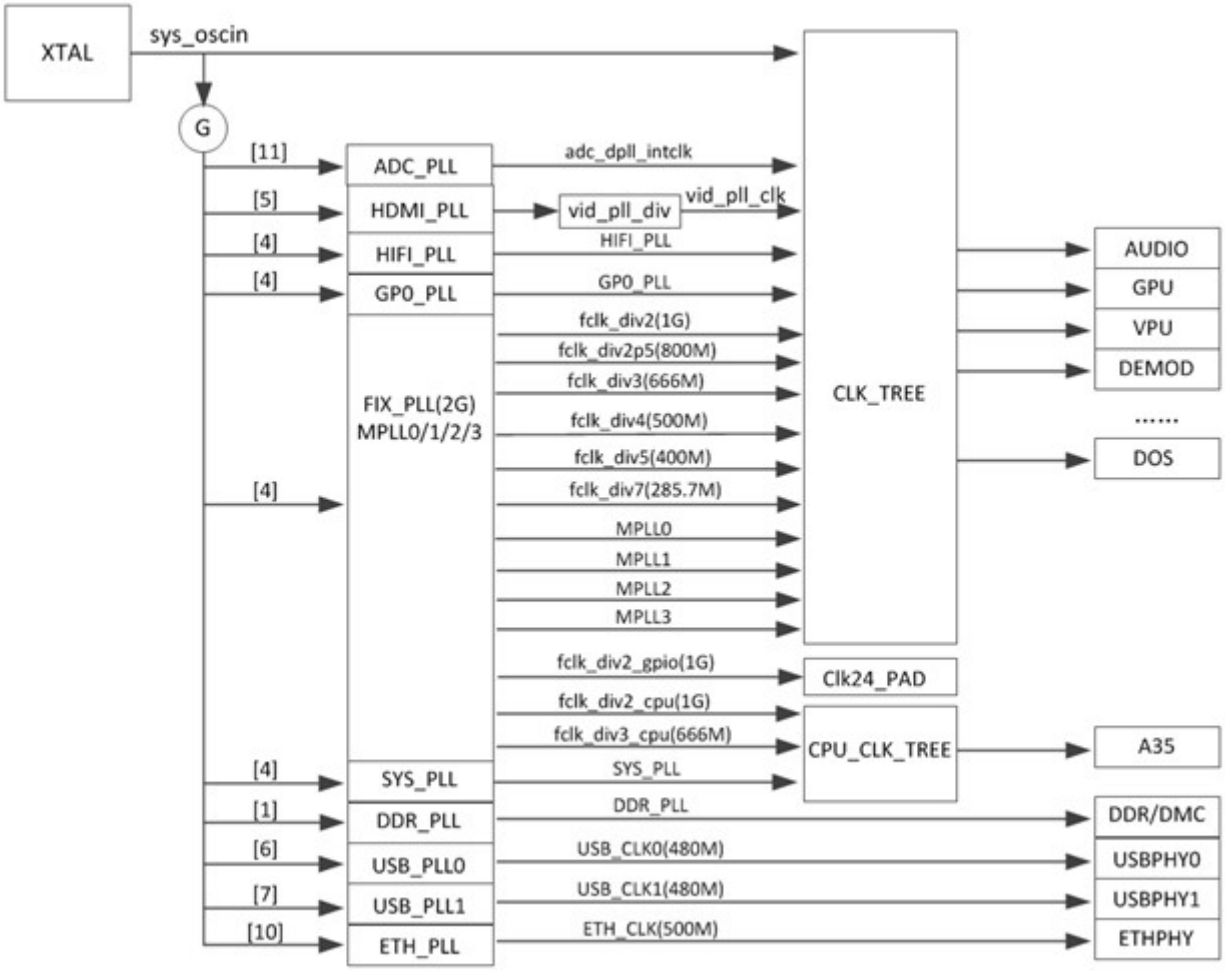
7.6.2.1 Overview

The chip includes:

- External 24Mhz crystal
- MPLL(FIXPLL)/SYS_PLL/HDMI_PLL/GP0_PLL/DDR_PLL/HIFI_PLL/ETHPHY_PLL/USBPHY_ PLL0/1
- These internal PLL will generated clock source

The figure is as follows.

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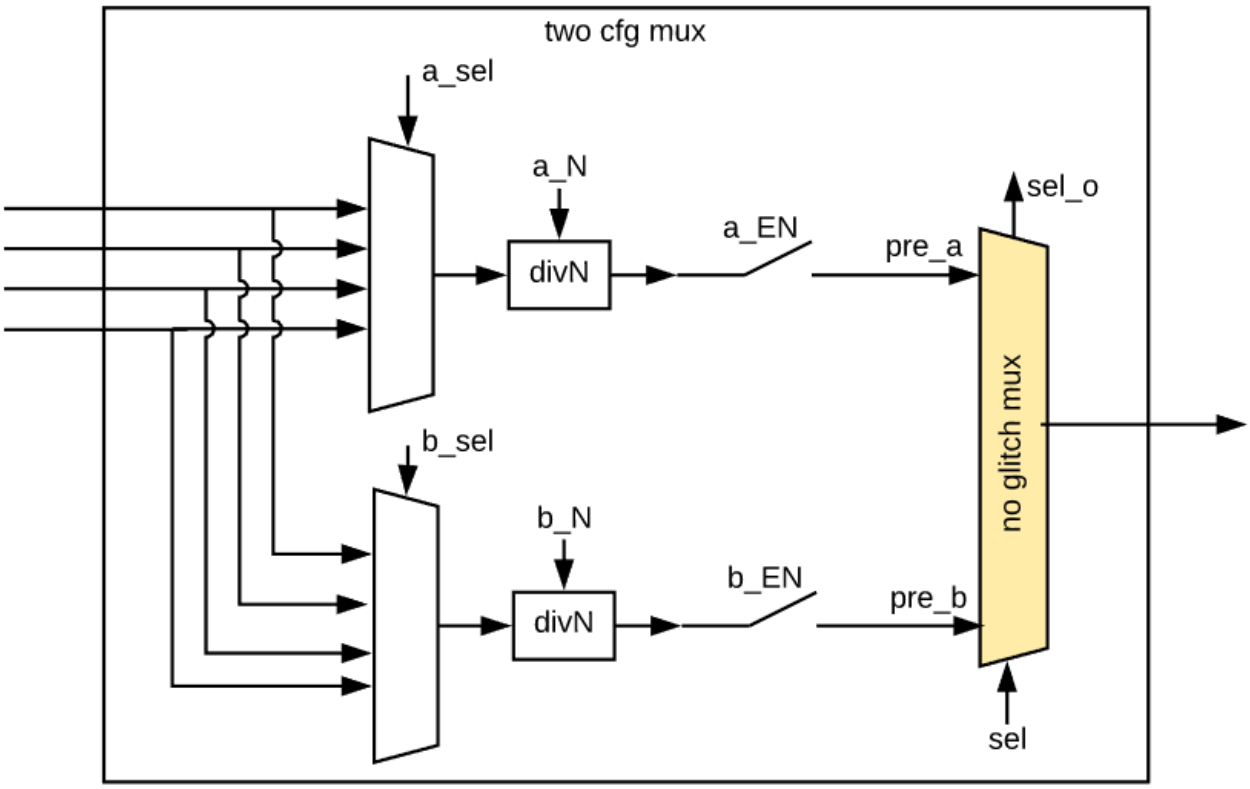


Two cfg mux is a special module for dynamic switch clock frequency.

It can generate two different clock sources by two muxs and divN.

Then selected by a “glitch free mux”.

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7.6.2.2 Register Description

For below registers the base address is 0xfe000000.

Each register final address = BASE + address * 4.

The following lists describe the mapping between each CLK_CTRL register and its address.

CLKCTRL_OSCIN_CTRL 0xfe000004

CLKCTRL_RTC_BY_OSCIN_CTRL0 0xfe000008

CLKCTRL_RTC_BY_OSCIN_CTRL1 0xfe00000c

CLKCTRL_RTC_CTRL 0xfe000010

CLKCTRL_CHECK_CLK_RESULT 0xfe000014

CLKCTRL_MBIST_ATSPEED_CTRL 0xfe000018

CLKCTRL_LOCK_BIT_REG0 0xfe000020

CLKCTRL_LOCK_BIT_REG1 0xfe000024

CLKCTRL_LOCK_BIT_REG2 0xfe000028

CLKCTRL_LOCK_BIT_REG3 0xfe00002c

CLKCTRL_PROT_BIT_REG0 0xfe000030

CLKCTRL_PROT_BIT_REG1 0xfe000034

CLKCTRL_PROT_BIT_REG2 0xfe000038

CLKCTRL_PROT_BIT_REG3 0xfe00003c

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```
CLKCTRL_SYS_CLK_CTRL0            0xfe000040
CLKCTRL_SYS_CLK_EN0_REG0         0xfe000044
CLKCTRL_SYS_CLK_EN0_REG1         0xfe000048
CLKCTRL_SYS_CLK_EN0_REG2         0xfe00004c
CLKCTRL_SYS_CLK_EN0_REG3         0xfe000050
CLKCTRL_SYS_CLK_EN1_REG0         0xfe000054
CLKCTRL_SYS_CLK_EN1_REG1         0xfe000058
CLKCTRL_SYS_CLK_EN1_REG2         0xfe00005c
CLKCTRL_SYS_CLK_EN1_REG3         0xfe000060
CLKCTRL_SYS_CLK_VPU_EN0          0xfe000064
CLKCTRL_SYS_CLK_VPU_EN1          0xfe000068
CLKCTRL_AXI_CLK_CTRL0            0xfe00006c
CLKCTRL_TST_CTRL0                0xfe000080
CLKCTRL_TST_CTRL1                0xfe000084
CLKCTRL_CECA_CTRL0               0xfe000088
CLKCTRL_CECA_CTRL1               0xfe00008c
CLKCTRL_CECB_CTRL0               0xfe000090
CLKCTRL_CECB_CTRL1               0xfe000094
CLKCTRL_SC_CLK_CTRL              0xfe000098
//`define CLKCTRL_DSPA_CLK_CTRL0       10'h27
//`define CLKCTRL_DSPB_CLK_CTRL0       10'h28
CLKCTRL_RAMA_CLK_CTRL0           0xfe0000a4
CLKCTRL_CLK12_24_CTRL            0xfe0000a8
CLKCTRL_VID_CLK_CTRL             0xfe0000c0
CLKCTRL_VID_CLK_CTRL2            0xfe0000c4
CLKCTRL_VID_CLK_DIV              0xfe0000c8
CLKCTRL_VIID_CLK_DIV             0xfe0000cc
CLKCTRL_VIID_CLK_CTRL            0xfe0000d0
CLKCTRL_HDMI_CLK_CTRL            0xfe0000e0
CLKCTRL_VID_PLL_CLK_DIV          0xfe0000e4
CLKCTRL_VPU_CLK_CTRL             0xfe0000e8
CLKCTRL_VPU_CLKB_CTRL            0xfe0000ec
CLKCTRL_VPU_CLKC_CTRL            0xfe0000f0
CLKCTRL_VID_LOCK_CLK_CTRL        0xfe0000f4
CLKCTRL_VDIN_MEAS_CLK_CTRL       0xfe0000f8
CLKCTRL_VAPBCLK_CTRL             0xfe0000fc
CLKCTRL_HDCP22_CLK_CTRL          0xfe000100
//`define CLKCTRL_MIPIDSI_PHY_CLK_CTRL   10'h41
```


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```
CLKCTRL_CDAC_CLK_CTRL              0xfe000108
//`define CLKCTRL_MIPI_CSI_PHY_CLK_CTRL   10'h43
//`define CLKCTRL_CSI2_ADAPT_CLK_CTRL     10'h44
CLKCTRL_VDEC_CLK_CTRL              0xfe000140
CLKCTRL_VDEC2_CLK_CTRL             0xfe000144
CLKCTRL_VDEC3_CLK_CTRL             0xfe000148
CLKCTRL_VDEC4_CLK_CTRL             0xfe00014c
//`define CLKCTRL_WAVE420L_CLK_CTRL       10'h54
//`define CLKCTRL_WAVE420L_CLK_CTRL2      10'h55
CLKCTRL_TS_CLK_CTRL                0xfe000158
CLKCTRL_MALI_CLK_CTRL              0xfe00015c
//`define CLKCTRL_VIPNANOQ_CLK_CTRL       10'h58
CLKCTRL_ETH_CLK_CTRL               0xfe000164
CLKCTRL_NAND_CLK_CTRL              0xfe000168
CLKCTRL_SD_EMMC_CLK_CTRL           0xfe00016c
//`define CLKCTRL_BT656_CLK_CTRL         10'h5C
CLKCTRL_SPICC_CLK_CTRL             0xfe000174
CLKCTRL_GEN_CLK_CTRL               0xfe000178
CLKCTRL_SAR_CLK_CTRL0              0xfe00017c
CLKCTRL_PWM_CLK_AB_CTRL            0xfe000180
CLKCTRL_PWM_CLK_CD_CTRL            0xfe000184
CLKCTRL_PWM_CLK_EF_CTRL            0xfe000188
CLKCTRL_PWM_CLK_GH_CTRL            0xfe00018c
CLKCTRL_PWM_CLK_IJ_CTRL            0xfe000190
CLKCTRL_DEMOD_CLK_CTRL             0xfe000200
CLKCTRL_TIMESTAMP_CTRL             0xfe000400
CLKCTRL_TIMESTAMP_CTRL1            0xfe000404
CLKCTRL_TIMESTAMP_CTRL2            0xfe00040c
CLKCTRL_TIMESTAMP_RD0              0xfe000410
CLKCTRL_TIMESTAMP_RD1              0xfe000414
CLKCTRL_TIMEBASE_CTRL0             0xfe000418
CLKCTRL_TIMEBASE_CTRL1             0xfe00041c
CLKCTRL_EFUSE_CPU_CFG01            0xfe000480
CLKCTRL_EFUSE_CPU_CFG2             0xfe000484
CLKCTRL_EFUSE_ENCP_CFG0            0xfe000488
CLKCTRL_EFUSE_MALI_CFG01           0xfe00048c
CLKCTRL_EFUSE_HEVCB_CFG01          0xfe000490
CLKCTRL_EFUSE_HEVCB_CFG2           0xfe000494
```


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CLKCTRL_EFUSE_LOCK 0xfe000498

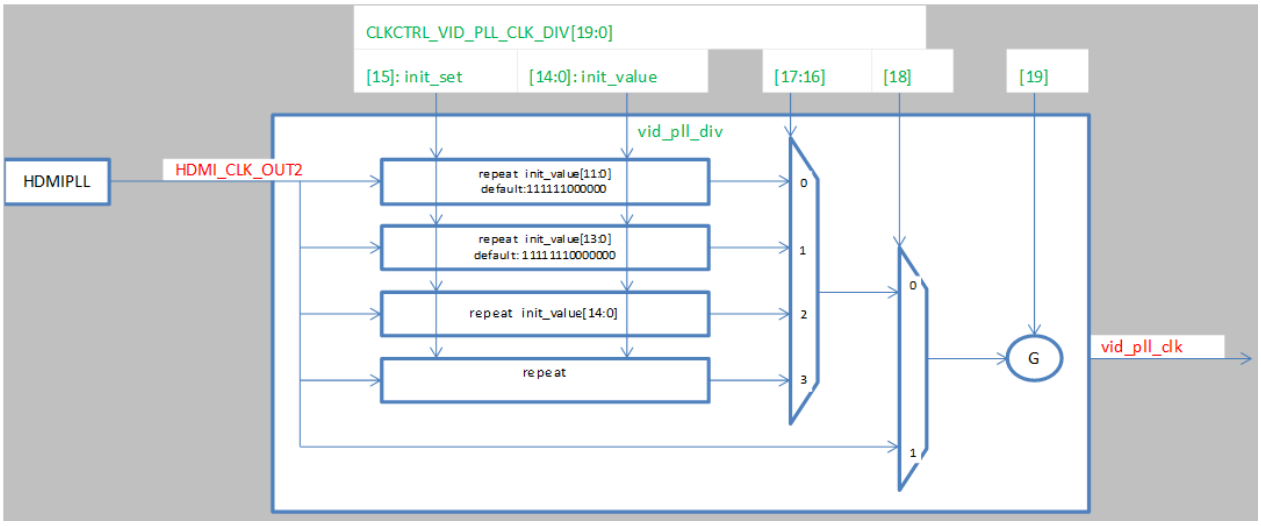
Table 7-39 CLKCTRL_OSCIN_CTRL

Osc from XTAL pad will connect all PLL and some analog modules:

And it will gated by reg_oscin_ctrl;

Bit(s)	R/W	Default	Description
11	R/W	1	clock gate en; xtal ->ADC_PLL
10	R/W	1	clock gate en; xtal -> ETH_PLL
9	R/W	1	clock gate en; xtal -> USBCTRL
7	R/W	1	clock gate en; xtal -> USB_PLL1
6	R/W	1	clock gate en; xtal -> USB_PLL0
5	R/W	1	clock gate en; xtal -> HDMIPLL
4	R/W	1	clock gate en; xtal -> PLL_TOP(FIXPLL/HIFIPLL/SYSPLL/GP0PLL)
2	R/W	2	clock gate en; xtal -> DDR_PHY
1	R/W	1	clock gate en; xtal -> DDR_PLL

Table 7-40 CLKCTRL_VID_PLL_CLK_DIV



Bit(s)	R/W	Default	Description
31~24	R	0	RESERVED
23~20	R/W	0	Reserved
19	R/W	0	CLK_FINAL_EN
18	R/W	0	CLK_DIV1

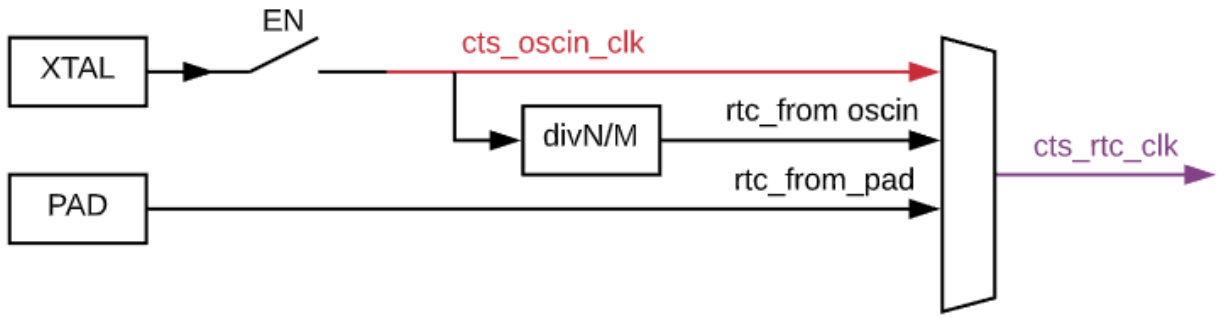
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Bit(s)	R/W	Default	Description
17~16	R/W	0	CLK_SEL
15	R/W	0	SET_PRESET
14-0	R/W	0	SHIFT_PRESET

Table 7-41 CLKCTRL_RTC_BY_OSCIN_CTRL0

RTC clock is a low frequency clock which needn't PLL.

It can be generated by XTAL of from PAD.



Bit(s)	R/W	Default	Description
31	R/W	0	clock in gate en
30	R/W	0	clock out gate en
28	R/W	0	0: freq_out = freq_in / N0; 1: freq_out = freq_in/((N0*M0+N1*M1)/(M0+M1)) Because XTAL is 24MHz only, so it can't generate some frequency like 32768Hz. If need 24KHz, set N0=1000 and this bit = 0, then rtc_clk = 24M/1000= 24KHz. If need 32768Hz, set N0=733, N1=732, M0 =2, M1=3, and this bit=1, then rtc_clk = 24M/(733*2+732*3)*(2+3)= 32768.9787Hz
23:12	R/W	0	clock div N1, if you want div8, set to 7
11:0	R/W	0	clock div N0, if you want div8, set to 7

Table 7-42 CLKCTRL_RTC_BY_OSCIN_CTRL1

Bit(s)	R/W	Default	Description
24	R/W	0	1: force clock_out = clock_in
23:12	R/W	0	clock div M1, if you want div8, set to 7
11:0	R/W	0	clock div M0, if you want div8, set to 7

Table 7-43 CLKCTRL_RTC_CTRL

Bit(s)	R/W	Default	Description
31	R	0	mux1 sel o
30	R	0	mux0b sel o

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Bit(s)	R/W	Default	Description
29	R	0	mux0a sel o
1:0	R/W	0	cts_rtc_clk source select: 0: oscin; 1:rtc from oscin div(N0/N1); 2:rtc from PAD; 3:off;

Table 7-44 CLKCTRL_CHECK_CLK_RESULT

Bit(s)	R/W	Default	Description
2	R	0	cts_encp_clk frequency check result
1	R	0	cts_hevcb_clk frequency check result
0	R	0	cts_mali_clk frequency check result

Table 7-45 CLKCTRL_MBIST_ATSPEED_CTRL

Bit(s)	R/W	Default	Description
0	R/W	0	0: mbist clk will select oscine; 1: mbist clk will select cts_***_clk;

Table 7-46 CLKCTRL_LOCK/PROT_BIT_REG0~3

Lock/prot are two different registers, they all can lock one clk_ctrl register by different bit.

The different of lock/prot is lock can write 1 only and prot can write both 0 and 1.

bit	reg0	reg1	reg2
0	CLKCTRL_OSCIN_CTRL	CLKCTRL_VIID_CLK_CTRL	CLKCTRL_SYS_CLK_EN1_REG1
1	CLKCTRL_VID_PLL_CLK_DIV	CLKCTRL_VIID_CLK_DIV	CLKCTRL_SYS_CLK_EN1_REG2
2	CLKCTRL_VID_CLK_CTRL	CLKCTRL_VID_LOCK_CLK_CTRL	CLKCTRL_SYS_CLK_EN1_REG3
3	CLKCTRL_VID_CLK_CTRL2	RESERVED	CLKCTRL_RTC_BY_OSCIN_CTRL0
4	CLKCTRL_VID_CLK_DIV	CLKCTRL_CDAC_CLK_CTRL	CLKCTRL_RTC_BY_OSCIN_CTRL1
5	CLKCTRL_HDMI_CLK_CTRL	CLKCTRL_SPICC_CLK_CTRL	CLKCTRL_RTC_CTRL
6	CLKCTRL_HDCP22_CLK_CTRL	CLKCTRL_PWM_CLK_AB_CTRL	CLKCTRL_RAMA_CLK_CTRL0
7	CLKCTRL_SC_CLK_CTRL	CLKCTRL_PWM_CLK_CD_CTRL	CLKCTRL_CLK12_24_CTRL
8	CLKCTRL_CECA_CTRL0	CLKCTRL_PWM_CLK_EF_CTRL	
9	CLKCTRL_CECA_CTRL1	CLKCTRL_PWM_CLK_GH_CTRL	

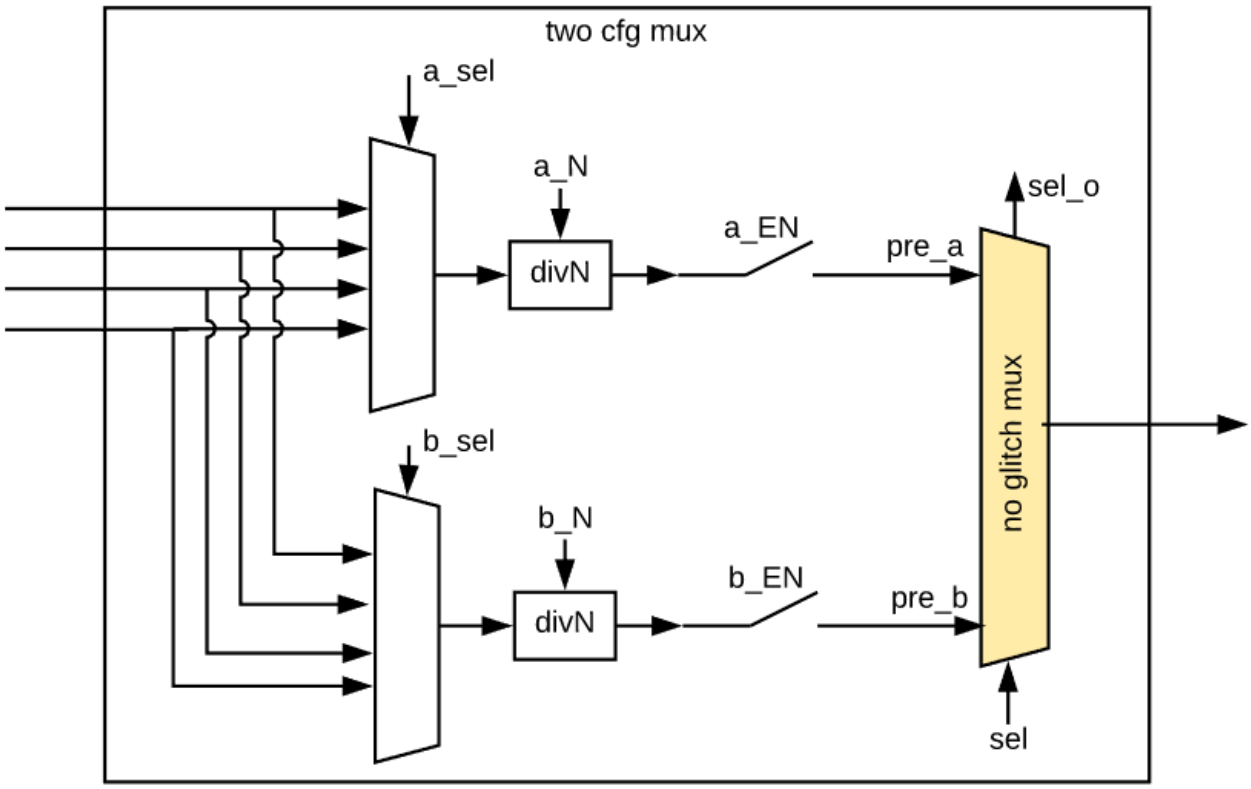
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bit	reg0	reg1	reg2
10	CLKCTRL_CECB_CTRL0	CLKCTRL_PWM_CLK_IJ_CTRL	
11	CLKCTRL_CECB_CTRL1	CLKCTRL_ETH_CLK_CTRL	
12	CLKCTRL_TST_CTRL0	RESERVED	
13	CLKCTRL_TST_CTRL1	CLKCTRL_TS_CLK_CTRL	
14	CLKCTRL_MALI_CLK_CTRL	CLKCTRL_TIME-STAMP_CTRL	
15	CLKCTRL_VDEC_CLK_CTRL	CLKCTRL_TIME-STAMP_CTRL1	
16	CLKCTRL_VDEC2_CLK_CTRL	CLKCTRL_TIME-STAMP_CTRL2	CLKCTRL_DEMOD_CLK_CTRL
17	CLKCTRL_VDEC3_CLK_CTRL	CLKCTRL_TIME-BASE_CTRL0	
18	CLKCTRL_VDEC4_CLK_CTRL	CLKCTRL_TIME-BASE_CTRL1	
19	RESERVED	CLKCTRL_SAR_CLK_CTRL0	
20	RESERVED	RESERVED	
21	CLKCTRL_VPU_CLK_CTRL	RESERVED	
22	CLKCTRL_VPU_CLKC_CTRL	CLKCTRL_SYS_CLK_CTRL0	
23	CLKCTRL_VAPBCLK_CTRL	CLKCTRL_AXI_CLK_CTRL0	
24	CLKCTRL_VPU_CLKB_CTRL	CLKCTRL_MBIST_ATSPEED_CTRL	
25	CLKCTRL_GEN_CLK_CTRL	CLKCTRL_SYS_CLK_VPU_EN0	
26	RESERVED	CLKCTRL_SYS_CLK_VPU_EN1	
27	CLKCTRL_VDIN_MEAS_CLK_CTRL	CLKCTRL_SYS_CLK_EN0_REG0	
28	CLKCTRL_NAND_CLK_CTRL	CLKCTRL_SYS_CLK_EN0_REG1	
29	CLKCTRL_SD_EMMC_CLK_CTRL	CLKCTRL_SYS_CLK_EN0_REG2	
30		CLKCTRL_SYS_CLK_EN0_REG3	
31		CLKCTRL_SYS_CLK_EN1_REG0	

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Table 7-47 AO_PWM_PWM_A: PWM_A_DUTY_CYCLE 0x0

SYS_CLK is a system level clock, most of control bus and some data bus worked on this clock domain.

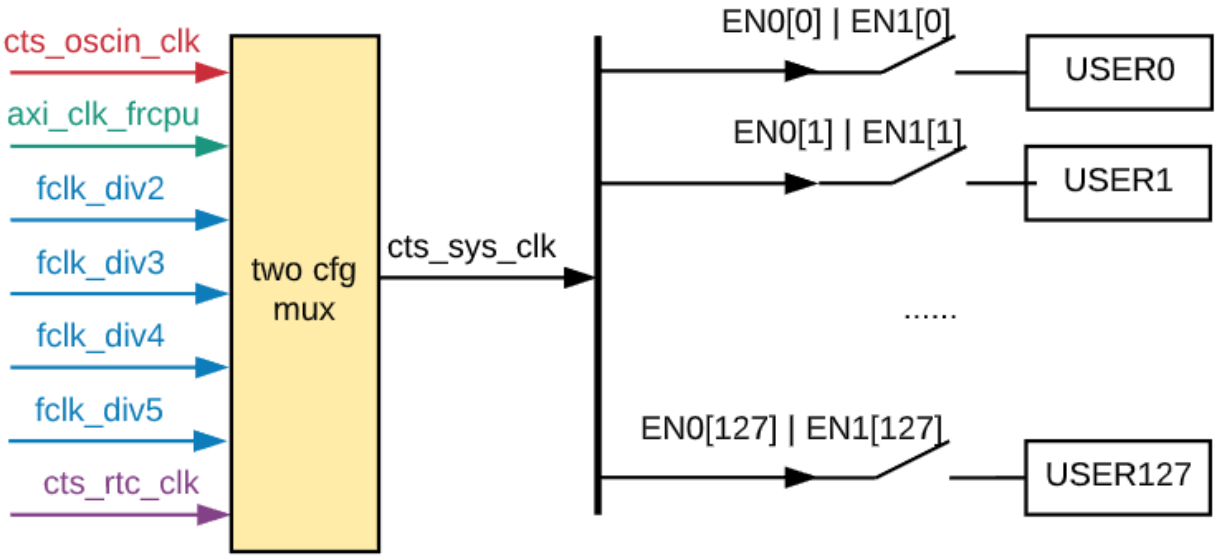


Bit(s)	R/W	Default	Description
31	R	0	no glitch mux sel out, if it's not equal to sel in for long time, mean the FSM is dead because no clock in
29	R/W	0	pre_b clock gate en
28:26	R/W	0	pre_b source select: 0:cts_oscin_clk; 1:fclk_div2; 2:fclk_div3; 3:fclk_div4 4:fclk_div5 5:axi_clk_frcpu 7:cts_rtc_clk
25:16	R/W	0	pre_b div N, if you want div8, set to 7
15	R/W	0	no gilitch mux sel in 0: select pre_a; 1: select pre_b;
13	R/W	1	pre_a clock gate en

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Bit(s)	R/W	Default	Description
12:10	R/W	0	pre_a source select: 0:cts_oscin_clk; 1:fclk_div2; 2:fclk_div3; 3:fclk_div4 4:fclk_div5 5:axi_clk_frcpu 7:cts_rtc_clk
9:0	R/W	0	pre_a div N, if you want div8, set to 7

Table 7-48 CLKCTRL_SYS_CLK_EN0_REG0~3/ CLKCTRL_SYS_CLK_EN1_REG0~3



Each bit will enabled one user, if some bits are not defined, mean they are reserved.

Bit	User
127	
126	
125	
124	
123	
122	
121	
120	
119	
118	
117	
116	
115	
114	

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Bit	User
113	
112	
111	
110	
109	
108	
107	pwm_ij
106	pwm_gh
105	pwm_ef
104	pwm_cd
103	pwm_ab
102	
101	
100	
99	
98	
97	
96	
95	
94	gic
93	
92	sar_adc
91	
90	
89	vpu_intr
88	
87	
86	
85	dspa
84	
83	cpu_debug
82	rsa
81	
80	
79	
78	
77	
76	

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Bit	User
75	mmc_apb
74	hdcp22
73	
72	usb1toddr
71	
70	
69	i2c_s_a
68	hdmitx_apb
67	i2c_m_f
66	i2c_m_e
65	i2c_m_d
64	i2c_m_c
63	i2c_m_b
62	i2c_m_a
61	
60	
59	
58	usb
57	
56	
55	
54	spicc1
53	spicc0
52	ge2d
51	
50	
49	
48	ts_pll
47	ts_ddr
46	
45	
44	
43	aififo
42	
41	uart_e
40	uart_d
39	uart_c

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Bit	User
38	uart_b
37	uart_a
36	
35	eth
34	
33	
32	audio
31	ir_ctrl
30	msr_clk
29	spifc
28	acodec
27	smartcard
26	nand/emmcC
25	sdemmcB
24	sdemmcA
23	
22	
21	
20	
19	
18	
17	
16	cec
15	
14	aucpu
13	aocpu
12	
11	
10	
9	
8	
7	
6	mali
5	
4	ethphy
3	
2	

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Bit	User
1	dos
0	ddr

Table 7-49 CLKCTRL_SYS_CLK_VPU_EN0/ CLKCTRL_SYS_CLK_VPU_EN1

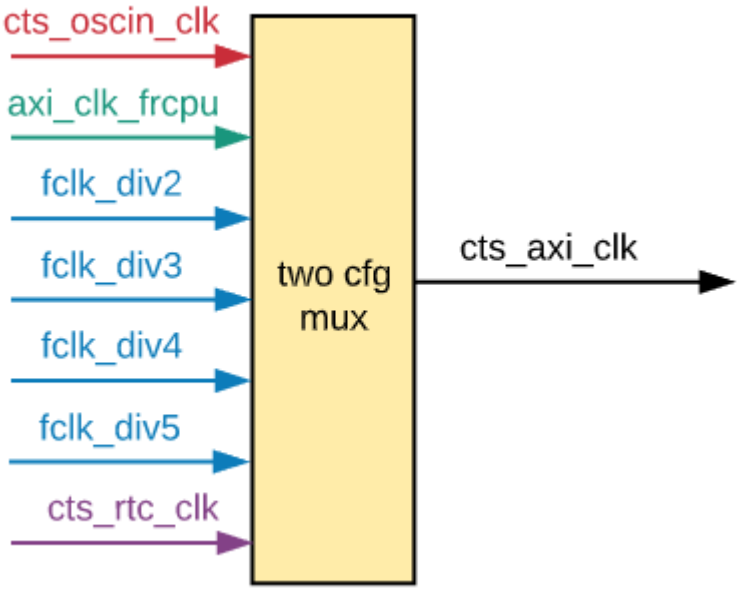
The same as CLKCTRL_SYS_CLK_EN0 & EN1, but it's connect to VPU and gate clock internal.

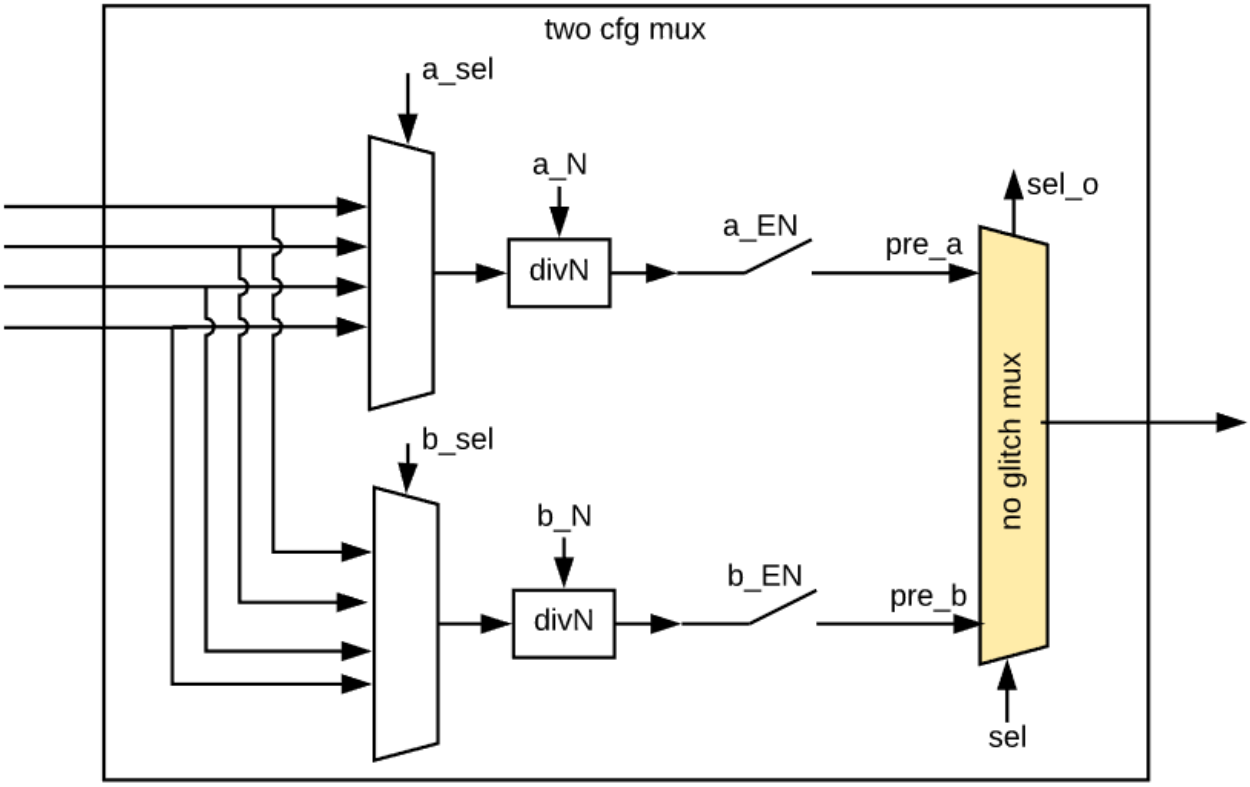
Bit(s)	R/W	Default	Description
26:22	R/W	0x1f	clk_vclk2_gate_en[13:9]
20	R/W	1	gclk_other_enc480p
10	R/W	1	clk_vclk3_gate_en
9:1	R/W	0x1ff	clk_vclk2_gate_en[8:0]

Table 7-50 CLKCTRL_AXI_CLK_CTRL0

AXI_CLK is a high speed clock for most of data bus.

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Bit(s)	R/W	Default	Description
31	R	0	no glitch mux sel out, if it's not equal to sel in for long time, mean the FSM is dead because no clock in
29	R/W	0	pre_b clock gate en
28:26	R/W	0	pre_b source select: 0:cts_oscin_clk; 1:fclk_div2; 2:fclk_div3; 3:fclk_div4 4:fclk_div5

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Bit(s)	R/W	Default	Description
			5:axi_clk_frcpu 7:cts_rtc_clk
25:16	R/W	0	pre_b div N, if you want div8, set to 7
15	R/W	0	no gilitch mux sel in 0: select pre_a; 1: select pre_b;
13	R/W	1	pre_a clock gate en
12:10	R/W	0	pre_a source select: 0:cts_oscin_clk; 1:fclk_div2; 2:fclk_div3; 3:fclk_div4 4:fclk_div5 5:axi_clk_frcpu 7:cts_rtc_clk
9:0	R/W	0	pre_a div N, if you want div8, set to 7

Table 7-51 CLKCTRL_TST_CTRL0/1

There are 4 test source can connect to PINMUX.

each pin can select by 2bits of CLKCTRL_TST_CTRL0/1. if 2bits is 2'b00, then src0 divided 32 then output, if 2bits is 2'b01, then src1 output.

The test source list as blow:

Name	select	default	src0	src1	src2	src3
TEST_ OUT19	CTRL1[7:6]	3	deskew_pll_ clk_div32_out	sys_cpu_ring [27]	sys_cpu_ring [3]	sys_cpu_ring [23]
TEST_ OUT18	CTRL1[5:4]	3		sys_cpu_ring [26]	sys_cpu_ring [2]	sys_cpu_ring [22]
TEST_ OUT17	CTRL1[3:2]	3		sys_cpu_ring [25]	sys_cpu_ring [1]	sys_cpu_ring [21]
TEST_ OUT16	CTRL1[1:0]	3		sys_cpu_ring [24]	sys_cpu_ring [0]	sys_cpu_ring [20]
TEST_ OUT15	CTRL0[31:30]	3	sys_pll	sys_pll_lock	sar_ring_osc_ clk	sys_cpu_ring [19]
TEST_ OUT14	CTRL0[29:28]	3	ddr_pll	ddr_pll_lock	osc_ring_ demod1	sys_cpu_ring [18]
TEST_ OUT13	CTRL0[27:26]	3	hdmi_pll	hdmi_pll_lock	osc_ring_ demod0	sys_cpu_ring [17]
TEST_ OUT12	CTRL0[25:24]	3	mpll0	fix_pll_lock	osc_ring_rama	sys_cpu_ring [16]
TEST_ OUT11	CTRL0[23:22]	3	mpll1	fix_pll_lock		sys_cpu_ring [15]
TEST_ OUT10	CTRL0[21:20]	3	mpll2	fix_pll_lock	osc_ring_dos3	sys_cpu_ring [14]
TEST_OUT9	CTRL0[19:18]	3	mpll3	fix_pll_lock	osc_ring_dos2	sys_cpu_ring [13]

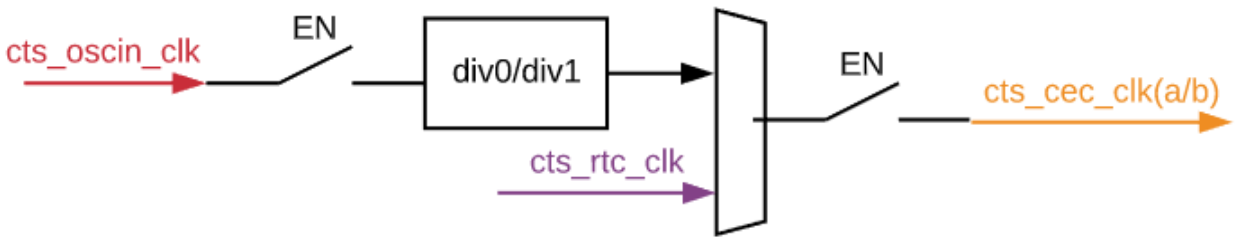
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Name	select	default	src0	src1	src2	src3
TEST_OUT8	CTRL0[17:16]	3	fclk_div5	fix_pll_lock	osc_ring_dos1	sys_cpu_ring [12]
TEST_OUT7	CTRL0[15:14]	3	gp0_pll	gp0_pll_lock	osc_ring_dos0	sys_cpu_ring [11]
TEST_OUT6	CTRL0[13:12]	3	adc_dpll_clk_ b3	adc_dpll_lock	osc_ring_vpu2	sys_cpu_ring [10]
TEST_OUT5	CTRL0[11:10]	3	hifi_pll	hifi_pll_lock	osc_ring_vpu1	sys_cpu_ring [9]
TEST_OUT4	CTRL0[9:8]	3			osc_ring_vpu0	sys_cpu_ring [8]
TEST_OUT3	CTRL0[7:6]	3			osc_ring_gpu2	sys_cpu_ring [7]
TEST_OUT2	CTRL0[5:4]	3	eth_pll	eth_pll_lock	osc_ring_gpu1	sys_cpu_ring [6]
TEST_OUT1	CTRL0[3:2]	3	usb_pll0	usb_pll0_lock	osc_ring_gpu0	sys_cpu_ring [5]
TEST_OUT0	CTRL0[1:0]	3	usb_pll1	usb_pll1_lock	osc_ring_dmc	sys_cpu_ring [4]

Table 7-52 CLKCTRL_CECA/B_CLK_CTRL0

CEC_CLK always run at 32768Hz, it will generated by XTAL, but for more accuracy, it can div by two counter.

Please refer to RTC_CLK for N1/N2 usage.



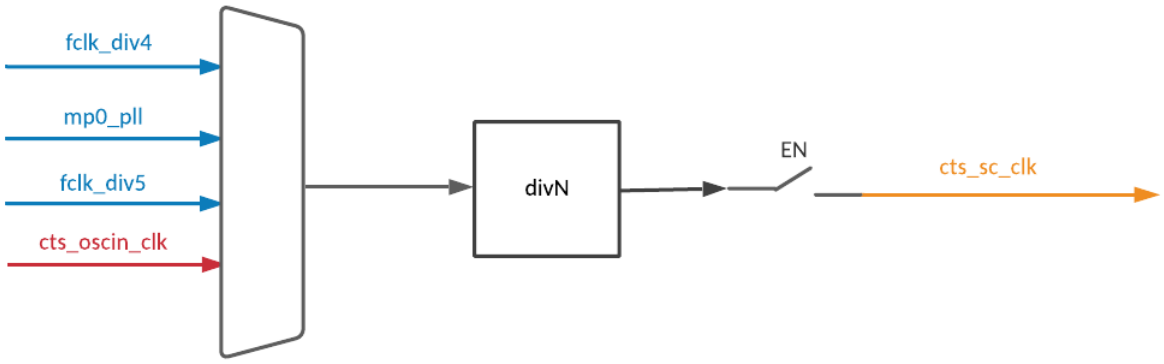
Bit(s)	R/W	Default	Description
31	R/W	0	Gclk_in:0:disable clk in;1:enable clk in;
30	R/W	0	Gclk_out: 0:disable clk out; 1: enable clk out;
29-28	R/W	0	Div_list_max: 0:only use clk_div0; 1:use clk_div0/clk_div1 in turn;
27-24	R/W	7	Reserved
23-12	R/W	731	Div_tcnt1: freq_clk_div1 = freq_clk_in/div_tcnt1;
11-0	R/W	732	Div_tcnt0: freq_clk_div0 = freq_clk_in/div_tcnt0;

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Table 7-53 CLKCTRL_CECA/B_CLK_CTRL1

Bit(s)	R/W	Default	Description
31	R/W	0	clk_sel for cts_cec_clk 0: from clock divider 1: from cts_rtc_clk
30-25	R	0	Reserved
24	R/W	0	Divide_by_1: 1: clk_out = clk_in; 0: clk_out = clk_div0 or 1;
23-12	R/W	10	Cycle_tcnt1 After Cycle_tcnt1 times clk_div1, clk_out will equal clk_div0; Need set div_list_max = 1;
11-0	R/W	7	Cycle_tcnt0 After Cycle_tcnt0 times clk_div, clk_out will equal clk_div1; Need set div_list_max = 1;

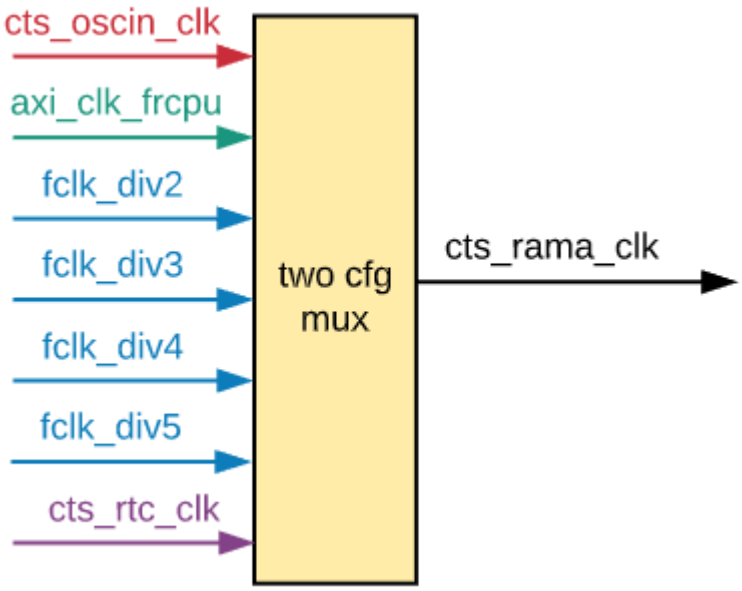
Table 7-54 CLKCTRL_SC_CLK_CTRL

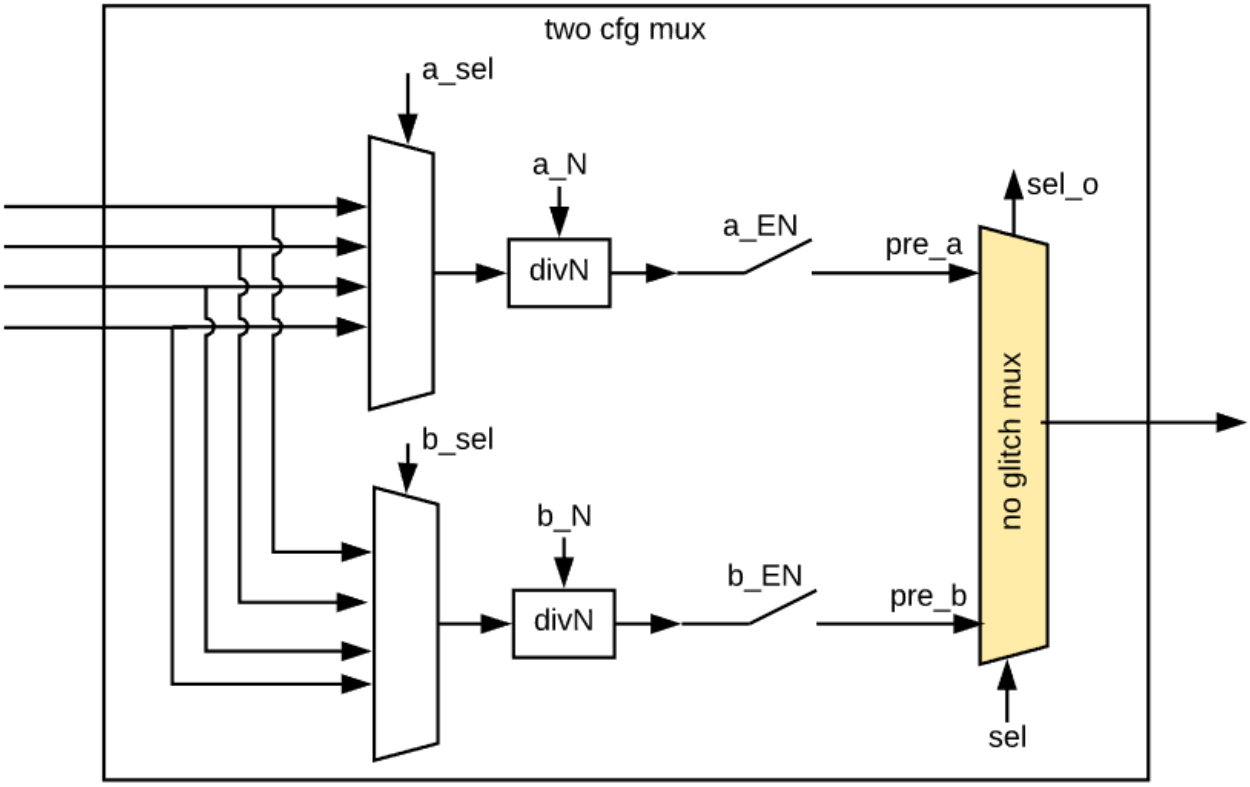


Bit(s)	R/W	Default	Description
10:9	R/W	0	clk_sel for cts_sc_clk(smart card) 0: from fclk_div4; 1: from fclk_div3; 2: from fclk_div5; 3: from cts_oscin_clk;
8	R/W	0	clock enable
7:0	R/W	0	div N, if you want div8, set to 7

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Table 7-55 CLKCTRL_RAMA_CLK_CTRL0





Bit(s)	R/W	Default	Description
31	R	0	no glitch mux sel out, if it's not equal to sel in for long time, mean the FSM is dead because no clock in
29	R/W	0	pre_b clock gate en
28:26	R/W	0	pre_b source select: 0:cts_oscin_clk; 1:fclk_div2; 2:fclk_div3;

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Bit(s)	R/W	Default	Description
			3:fclk_div4; 4:fclk_div5; 5:axi_clk_frcpu; 6:fclk_div7; 7:cts_rtc_clk
25:16	R/W	0	pre_b div N, if you want div8, set to 7
15	R/W	0	no gilitch mux sel in 0: select pre_a; 1: select pre_b;
13	R/W	0	pre_a clock gate en
12:10	R/W	0	pre_a source select: 0:cts_oscin_clk; 1:fclk_div2; 2:fclk_div3; 3:fclk_div4; 4:fclk_div5; 5:axi_clk_frcpu; 6:fclk_div7; 7:cts_rtc_clk
9:0	R/W	0	pre_a div N, if you want div8, set to 7

CLKCTRL_VID_CLK_DIV/CTRL/CTRL2 + CLKCTRL_VIID_CLK_DIV/CTRL +CLKCTRL_HDMI_CLK_CTRL

All are the video related clock control.

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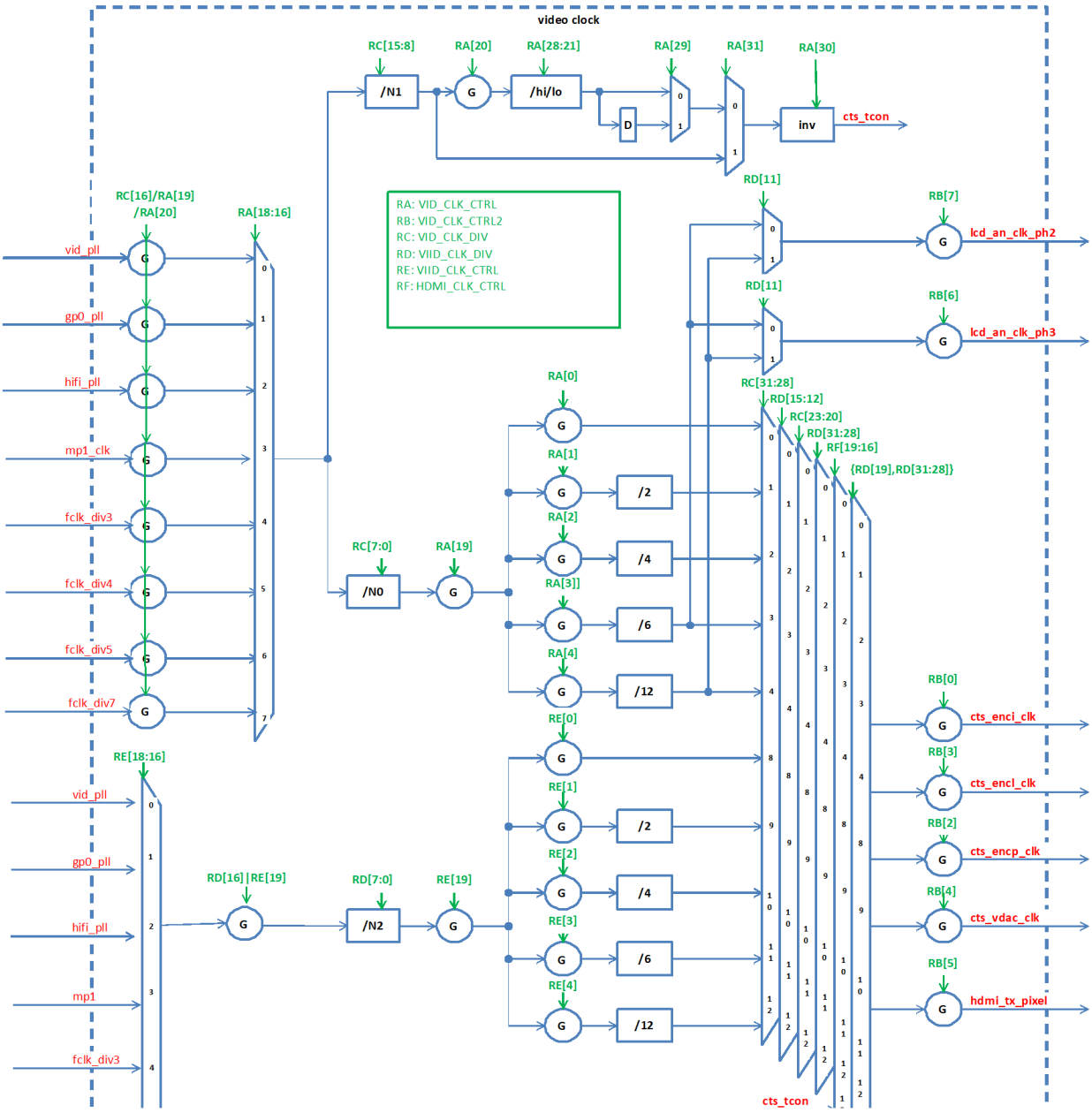


Table 7-56 CLKCTRL_VID_CLK_CTRL

Bit(s)	R/W	Default	Description
31-21	R/W	0	TCON_CLK0_CTRL
20	R/W	0	CLK_EN1
19	R/W	0	CLK_EN0
18-16	R/W	0	CLK_IN_SEL
15	R/W	0	SOFT_RESET
14	R/W	0	PH23_ENABLE
13	R/W	0	DIV12_PH23
12-5	R/W	0	UNUSED

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Bit(s)	R/W	Default	Description
4	R/W	0	DIV12_EN
3	R/W	0	DIV6_EN
2	R/W	0	DIV4_EN
1	R/W	0	DIV2_EN
0	R/W	0	DIV1_EN

Table 7-57 CLKCTRL_VID_CLK_CTRL2

Bit(s)	R/W	Default	Description
31-16	R	0	
15-9	R/W	0	Reserved
8	R/W	0	Atv demod vdac gated clock control
7	R/W	1	LCD_AN_CLK_PHY2 gated clock control. 1 = enable
6	R/W	1	LCD_AN_CLK_PH3 gated clock control
5	R/W	1	HDMI_TX_PIXEL_CLK gated clock control
4	R/W	1	VDAC_clk gated clock control
3	R/W	1	ENCL gated clock control
2	R/W	1	ENCP gated clock control
1	R/W	1	ENCT gated clock control
0	R/W	1	ENCI gated clock control

Table 7-58 CLKCTRL_VID_CLK_DIV

Bit(s)	R/W	Default	Description
31-28	R/W	0	ENCI_CLK_SEL
27-24	R/W	0	ENCP_CLK_SEL
23-20	R/W	0	ENCT_CLK_SEL
19-18	R/W	0	UNUSED
17	R/W	0	CLK_DIV_RESET
16	R/W	0	CLK_DIV_EN
15-8	R/W	1	XD1
7-0	R/W	1	XD0

Table 7-59 CLKCTRL_VIID_CLK_CTRL

Bit(s)	R/W	Default	Description
31-20	R/W	0	Unused
19	R/W	0	V2_cntl_clk_en0

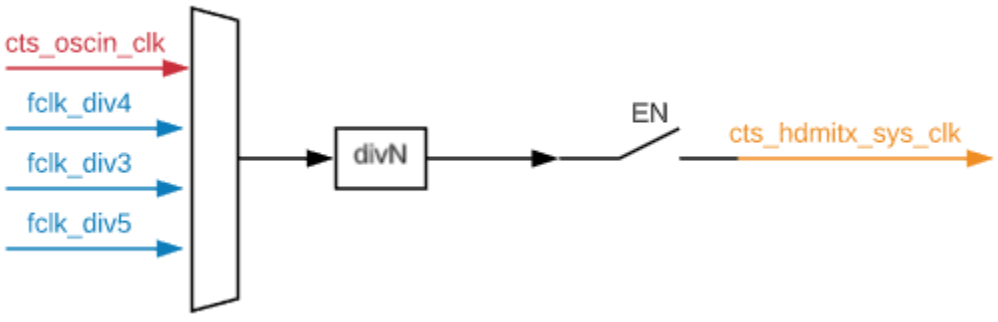
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Bit(s)	R/W	Default	Description
18-16	R/W	0	V2_cntl_clk_in_sel
15	R/W	0	V2_cntl_soft_reset
14-5	R/W	0	Unused
4	R/W	0	V2_cntl_div12_en
3	R/W	0	V2_cntl_div6_en
2	R/W	0	V2_cntl_div4_en
1	R/W	0	V2_cntl_div2_en
0	R/W	0	V2_cntl_div1_en

Table 7-60 CLKCTRL_VIID_CLK_DIV

Bit(s)	R/W	Default	Description
31-28	R/W	0	DAC0_CLK_SEL
27-24	R/W	0	DAC1_CLK_SEL
23-20	R/W	0	DAC2_CLK_SEL
19	R/W	0	Select adc_pll_clk_b2 to be cts_clk_vdac
18	R/W	0	Unused
17	R/W	0	V2_cntl_clk_div_reset
16	R/W	0	V2_cntl_clk_div_en
15-12	R/W	0	Encl_clk_sel
14-8	R/W	0	Unused
7-0	R/W	0	V2_cntl_xd0

Table 7-61 CLKCTRL_HDMI_CLK_CTRL

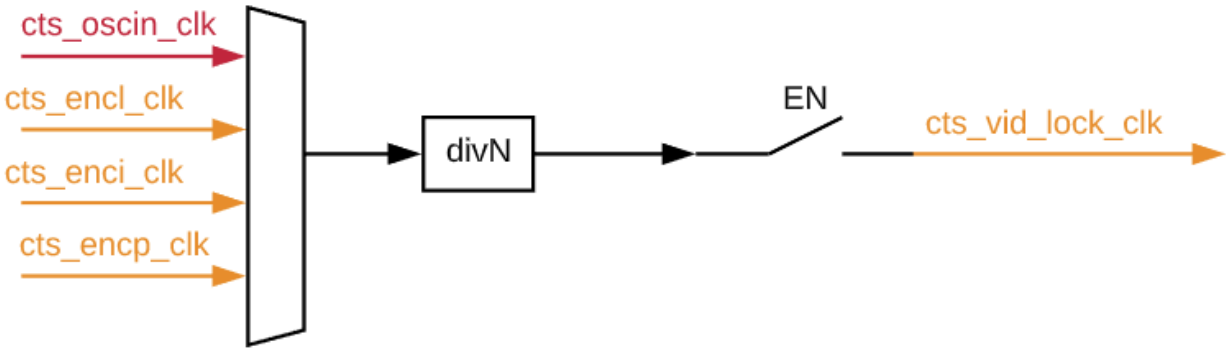


Bit(s)	R/W	Default	Description
31-20	R/W	0	Reserved
19~16	R/W	0	for crt_hdmi_pixel_clk_sel
15~11	R/W	0	Reserved
10~9	R/W	0	CLK_SEL:

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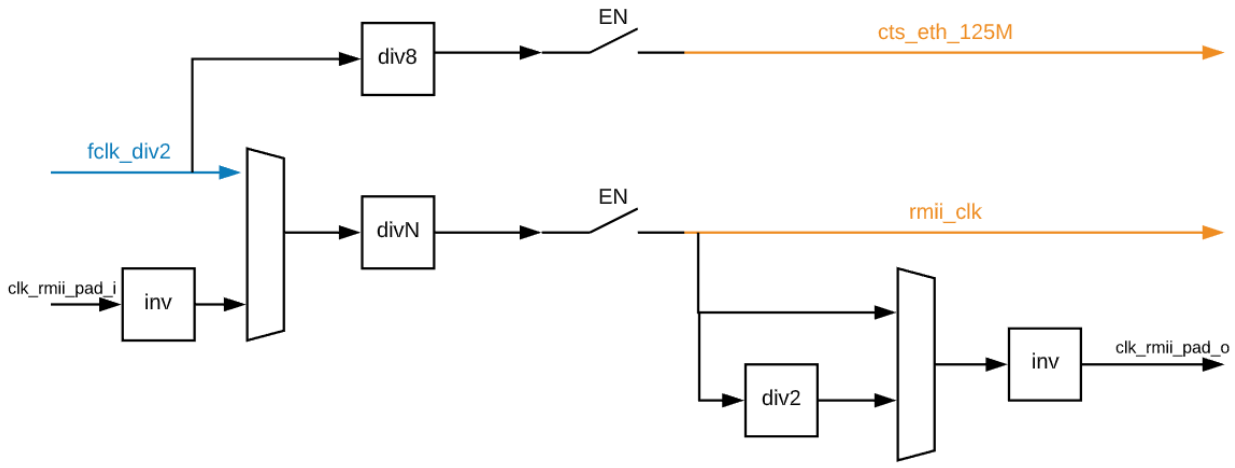
Bit(s)	R/W	Default	Description
			0:oscin; 1:fclk_div4; 2:fclk_div3; 3:fclk_div5;
8	R/W	0	CLK_EN:
7	R/W	0	Reserved
6-0	R/W	0	div N, if you want div8, set to 7

Table 7-62 CLKCTRL_VID_LOCK_CLK_CTRL



Bit(s)	R/W	Default	Description
31~10	R/W	0	reserved
9-8	R/W	0	Clk_sel: 0:cts_oscin_clk 1:cts_encl_clk 2:cts_enci_clk 3:cts_encp_clk
7	R/W	0	Clk_en
6-0	R/W	0	div N, if you want div8, set to 7

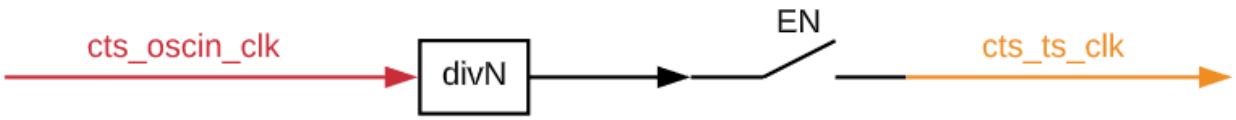
Table 7-63 CLKCTRL_ETH_CLK_CTRL



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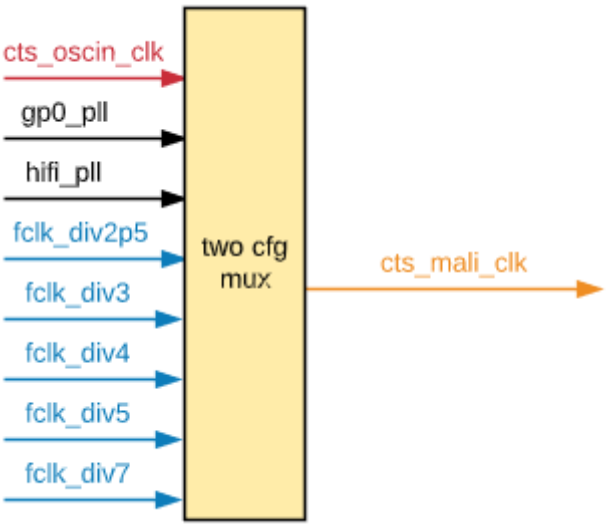
Bit(s)	R/W	Default	Description
17	R/W	0	eth_mac_speed
16	R/W	0	invert clk_rmii_pad_i
13	R/W	0	invert clk_rmii_pad_o
12	R/W	0	clk_rmii_pad_o; 0: rmii_clk; 1: rmii_div2
11:9	R/W	0	rmii_clk; clk_sel; 0: fclk_div2; 7: clk_rmii_pad_i;
8	R/W	0	rmii_clk; clk_en
7	R/W	0	eth_clk125M; clk_en;
6:0	R/W	0	rmii_clk; div N, if you want div8, set to 7

Table 7-64 CLKCTRL_TS_CLK_CTRL



Bit(s)	R/W	Default	Description
8	R/W	0	cts_ts_clk clk_en
7:0	R/W	0	cts_ts_clk div N, if you want div8, set to 7

Table 7-65 CLKCTRL_MALI_CLK_CTRL



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Bit(s)	R/W	Default	Description
31	R/W	0	final mux; 0: select mux_a; 1: select mux_b;
30-28	R/W	0	Reserved
27~25	R/W	0	mux_b CLK_SEL: 0: cts_oscin_clk 1: gp0_pll 2: hifi_pll 3: fclk_div2p5 4: fclk_div3 5: fclk_div4 6: fclk_div5 7: fclk_div7
24	R/W	0	mux_b CLK_EN:
23	R/W	0	Reserved
22~16	R/W	0	mux_b div N, if you want div8, set to 7:
15~12	R/W	0	Reserved
11~9	R/W	0	mux_a CLK_SEL: 0: cts_oscin_clk 1: gp0_pll 2: hifi_pll 3: fclk_div2p5 4: fclk_div3 5: fclk_div4 6: fclk_div5 7: fclk_div7
8	R/W	0	mux_a CLK_EN:
7	R/W	0	Reserved
6-0	R/W	0	mux_a div N, if you want div8, set to 7:

CLKCTRL_VDEC/2/3/4_CLK_CTRL

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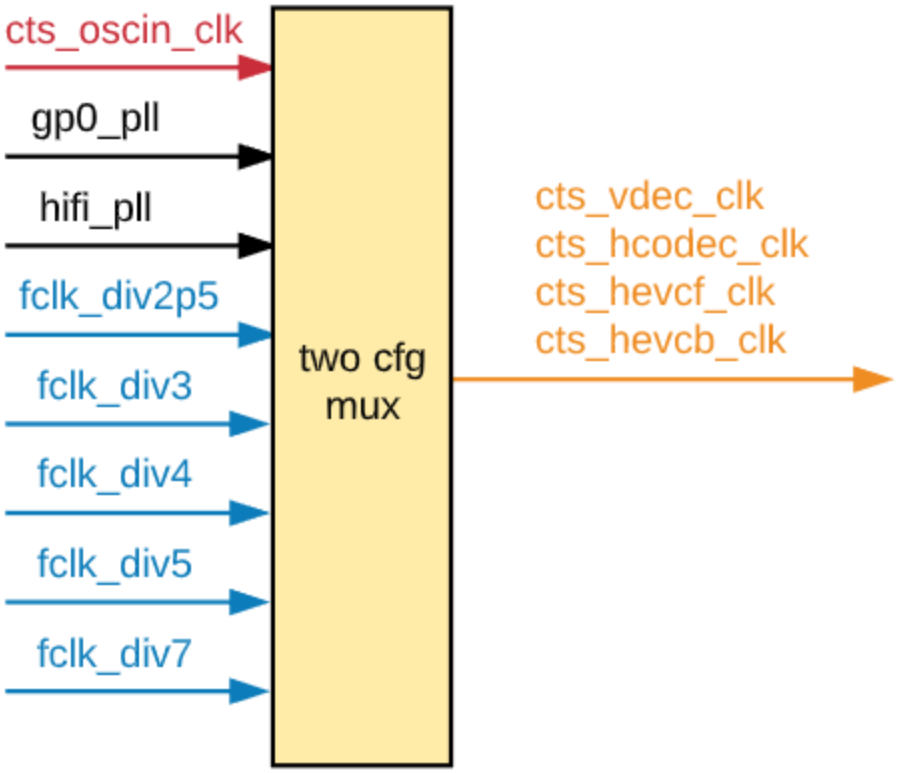


Table 7-66 CLKCTRL_VDEC_CLK_CTRL

Bit(s)	R/W	Default	Description
31-12	R/W	0	Reserved
11~9	R/W	0	cts_vdec_clk, mux_a CLK_SEL: 0:fclk_div2p5; 1:fclk_div3; 2:fclk_div4; 3:fclk_div5; 4:fclk_div7; 5:hifi_pll; 6:gp0pll; 7:oscin;
8	R/W	0	cts_vdec_clk, mux_a CLK_EN:
7	R/W	0	Reserved
6-0	R/W	0	cts_vdec_clk, mux_a div N, if you want div8, set to 7:

Table 7-67 CLKCTRL_VDEC2_CLK_CTRL

Bit(s)	R/W	Default	Description
31-12	R/W	0	Reserved
11~9	R/W	0	cts_hevcf_clk, mux_a: CLK_SEL: 0:fclk_div2p5;

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Bit(s)	R/W	Default	Description
			1:fclk_div3; 2:fclk_div4; 3:fclk_div5; 4:fclk_div7; 5:hifi_pll; 6:gp0pll; 7:oscin;
8	R/W	0	cts_hevcf_clk, mux_a: CLK_EN:
7	R/W	0	Reserved
6-0	R/W	0	cts_hevcf_clk, mux_a: div N, if you want div8, set to 7:

Table 7-68 CLKCTRL_VDEC3_CLK_CTRL

Bit(s)	R/W	Default	Description
31-16	R/W	0	Reserved
15	R/W	0	cts_vdec_clk 0: sel mux_a 1: sel mux_b
11~9	R/W	0	cts_vdec_clk, mux_b CLK_SEL: 0:fclk_div2p5; 1:fclk_div3; 2:fclk_div4; 3:fclk_div5; 4:fclk_div7; 5:hifi_pll; 6:gp0pll; 7:oscin;
8	R/W	0	cts_vdec_clk, mux_b CLK_EN:
7	R/W	0	Reserved
6-0	R/W	0	cts_vdec_clk, mux_b div N, if you want div8, set to 7:

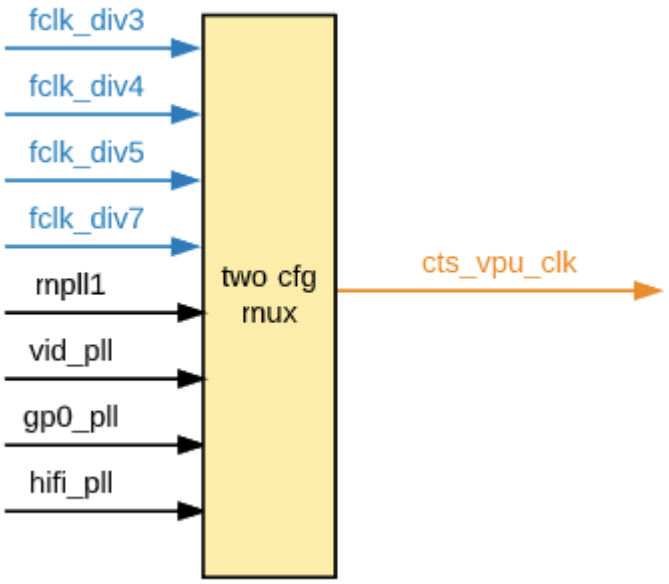
Table 7-69 CLKCTRL_VDEC4_CLK_CTRL

Bit(s)	R/W	Default	Description
31-16	R/W	0	Reserved
15	R/W	0	cts_hevcf_clk: 0: use mux_a 1: use mux_b
11~9	R/W	0	cts_hevcf_clk, mux_b: CLK_SEL: 0:fclk_div2p5; 1:fclk_div3; 2:fclk_div4; 3:fclk_div5; 4:fclk_div7; 5:hifi_pll; 6:gp0pll; 7:oscin;

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Bit(s)	R/W	Default	Description
8	R/W	0	cts_hevcf_clk, mux_b: CLK_EN:
7	R/W	0	Reserved
6-0	R/W	0	cts_hevcf_clk, mux_b: div N, if you want div8, set to 7:

Table 7-70 CLKCTRL_VPU_CLK_CTRL

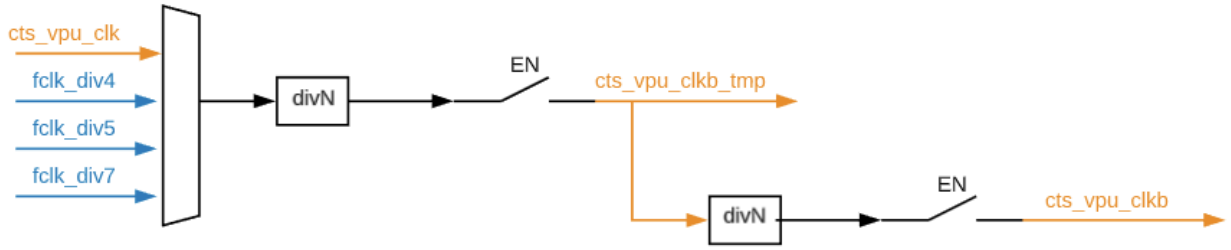


Bit(s)	R/W	Default	Description
31	R/W	0	Final mux sel 0: use mux_a 1: use mux_b
30-29	R/W	0	Reserved
27~25	R/W	0	mux_b CLK_SEL: 0:fclk_div3; 1:fclk_div4; 2:fclk_div5; 3:fclk_div7; 4:mpll1; 5:vid_pll; 6:hifi_pll; 7:gp0_pll;
24	R/W	0	mux_b CLK_EN:
23	R/W	0	Reserved
22~16	R/W	0	mux_b div N, if you want div8, set to 7:
11~9	R/W	0	mux_a CLK_SEL: 0:fclk_div3; 1:fclk_div4; 2:fclk_div5; 3:fclk_div7; 4:mpll1; 5:vid_pll;

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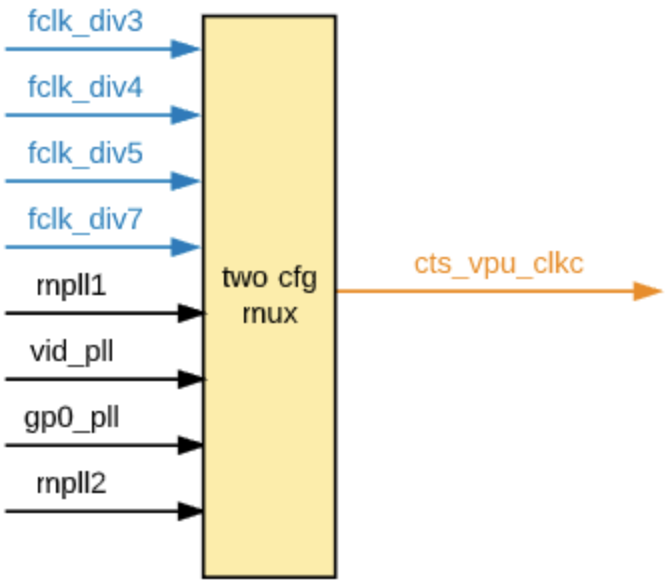
Bit(s)	R/W	Default	Description
			6:hifi_pll; 7:gp0_pll;
8	R/W	0	mux_a CLK_EN:
7	R/W	0	Reserved
6-0	R/W	0	mux_a div N, if you want div8, set to 7:

Table 7-71 CLKCTRL_VPU_CLKB_CTRL



Bit(s)	R/W	Default	Description
31-25	R/W	0	Reserved
24	R/W	0	Cts_vpu_clkb_tmp en
21-20	R/W	0	Cts_vpu_clkb_tmp sel 0:cts_vpu_clk 1:fclk_div4 2:fclk_div5 3:fclk_div7
19-16	R/W	0	Cts_vpu_clkb_tmp div
9	R/W	0	Vpu_clkb_latch_en
8	R/W	0	Vpu_clkb_en
7-0	R/W	0	Vpu_clkb_div

Table 7-72 CLKCTRL_VPU_CLKC_CTRL

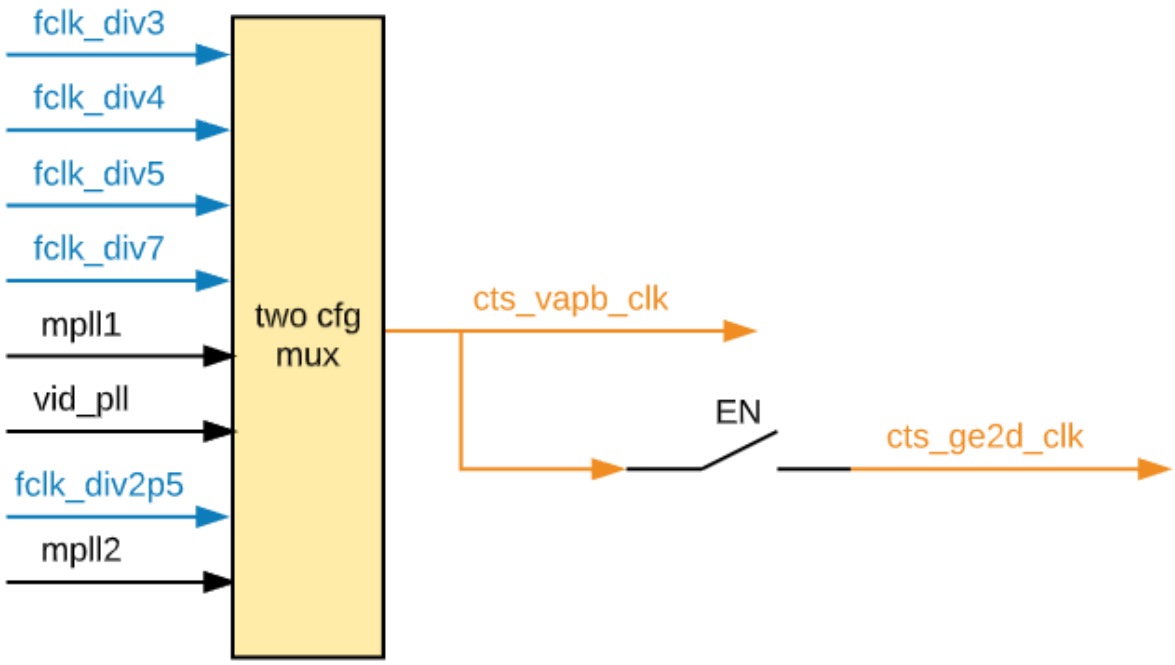


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Bit(s)	R/W	Default	Description
31	R/W	0	Final mux sel 0:mux_a 1:mux_b
30-29	R/W	0	Reserved
27~25	R/W	0	mux_b CLK_SEL: 0:fclk_div4; 1:fclk_div3; 2:fclk_div5; 3:fclk_div7; 4:mpll1; 5:vid_pll; 6:mpll2; 7:gp0pll;
24	R/W	0	mux_b CLK_EN:
23	R/W	0	Reserved
22~16	R/W	0	mux_b div N, if you want div8, set to 7:
15~12			
11~9	R/W	0	mux_a CLK_SEL: 0:fclk_div4; 1:fclk_div3; 2:fclk_div5; 3:fclk_div7; 4:mpll1; 5:vid_pll; 6:mpll2; 7:gp0pll;
8	R/W	0	mux_a CLK_EN:
7	R/W	0	Reserved
6-0	R/W	0	mux_a div N, if you want div8, set to 7:

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Table 7-73 CLKCTRL_VAPBCLK_CTRL

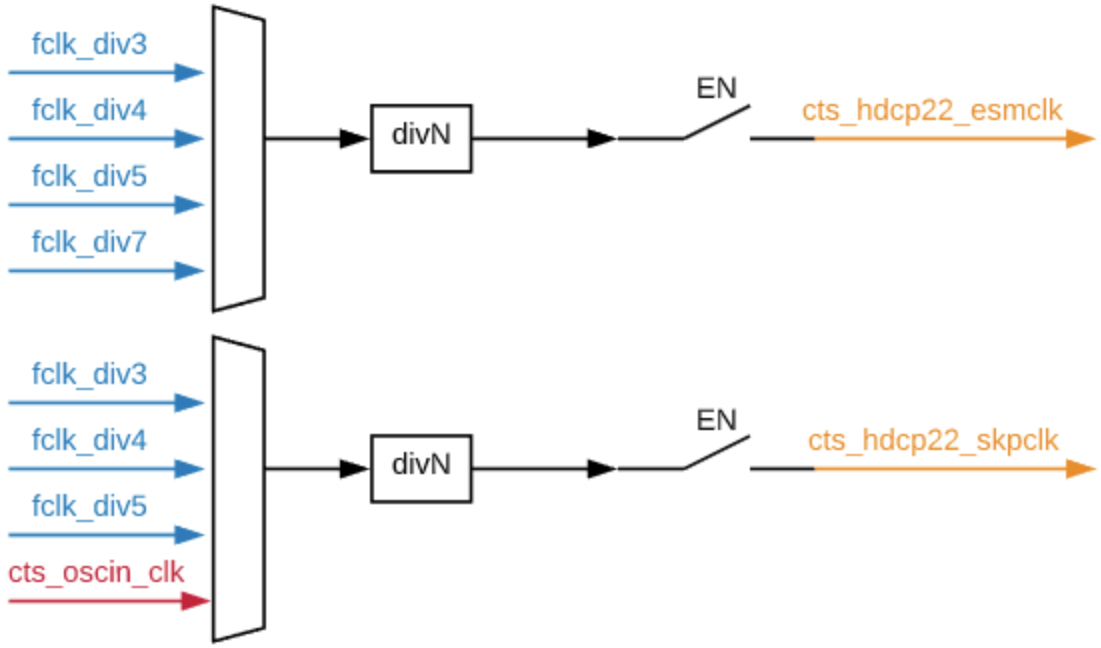


Bit(s)	R/W	Default	Description
31	R/W	0	Final mux sel 0:mux_a 1:mux_b
30	R/W	0	cts_ge2d_clk enable
29	R/W	0	Reserved
27~25	R/W	0	mux_b CLK_SEL: 0:fclk_div4; 1:fclk_div3; 2:fclk_div5; 3:fclk_div7; 4:mpll1; 5:vid_pll; 6:mpll2; 7:fclk_div2p5
24	R/W	0	mux_b CLK_EN:
23	R/W	0	Reserved
22~16	R/W	0	mux_b div N, if you want div8, set to 7:
15~12			
11~9	R/W	0	mux_a CLK_SEL: 0:fclk_div4; 1:fclk_div3; 2:fclk_div5; 3:fclk_div7; 4:mpll1; 5:vid_pll; 6:mpll2; 7:fclk_div2p5
8	R/W	0	mux_a CLK_EN:

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Bit(s)	R/W	Default	Description
7	R/W	0	Reserved
6-0	R/W	0	mux_a div N, if you want div8, set to 7:

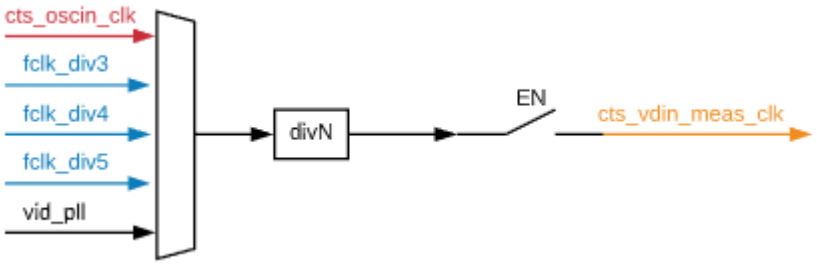
Table 7-74 CLKCTRL_HDCP22_CTRL



Bit(s)	R/W	Default	Description
26-25	R/W	0	cts_hdcp22_skpclk Clk_sel: 0:cts_oscin_clk 1:fclk_div4 2:fclk_div3 3:fclk_div5
24	R/W	0	cts_hdcp22_skpclk Clk_en
22:16	R/W	0	cts_hdcp22_skpclk div N, if you want div8, set to 7
10:9	R/W	0	cts_hdcp22_esmclk Clk_sel: 0:fclk_div7 1:fclk_div4 2:fclk_div3 3:fclk_div5
8	R/W	0	cts_hdcp22_esmclk Clk_en
6:0	R/W	0	cts_hdcp22_esmclk div N, if you want div8, set to 7

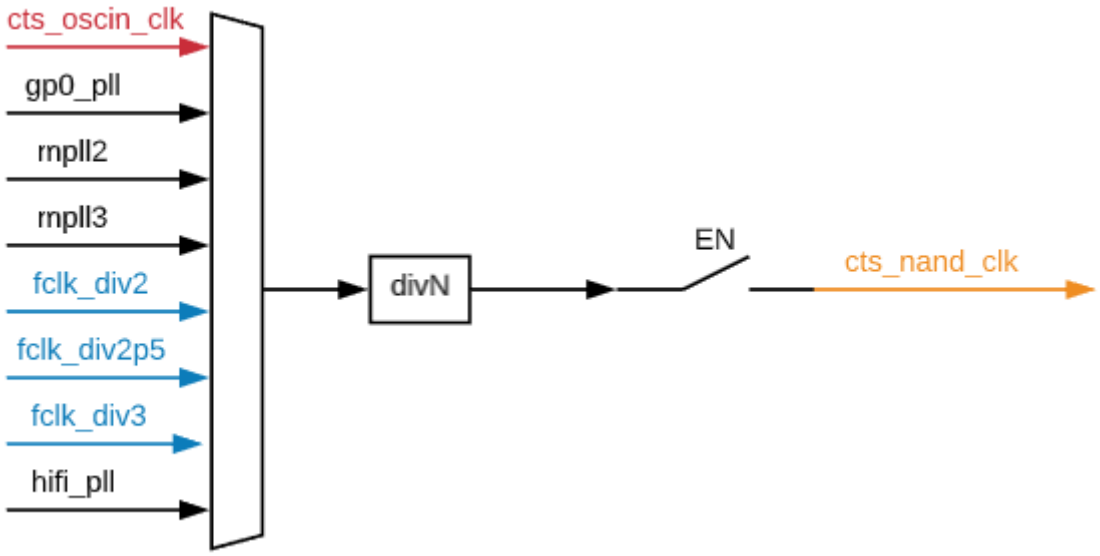
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Table 7-75 CLKCTRL_VDIN_MEAS_CLK_CTRL



Bit(s)	R/W	Default	Description
11-9	R/W	0	cts_vdin_meas_clk CLK_SEL: 0:oscin; 1:fclk_div4; 2:fclk_div3; 3:fclk_div5; 4:vid_pll;
8	R/W	0	cts_vdin_meas_clk CLK_EN:
6:0	R/W	0	cts_vdin_meas_clk div N, if you want div8, set to 7

Table 7-76 CLKCTRL_NAND_CLK_CTRL

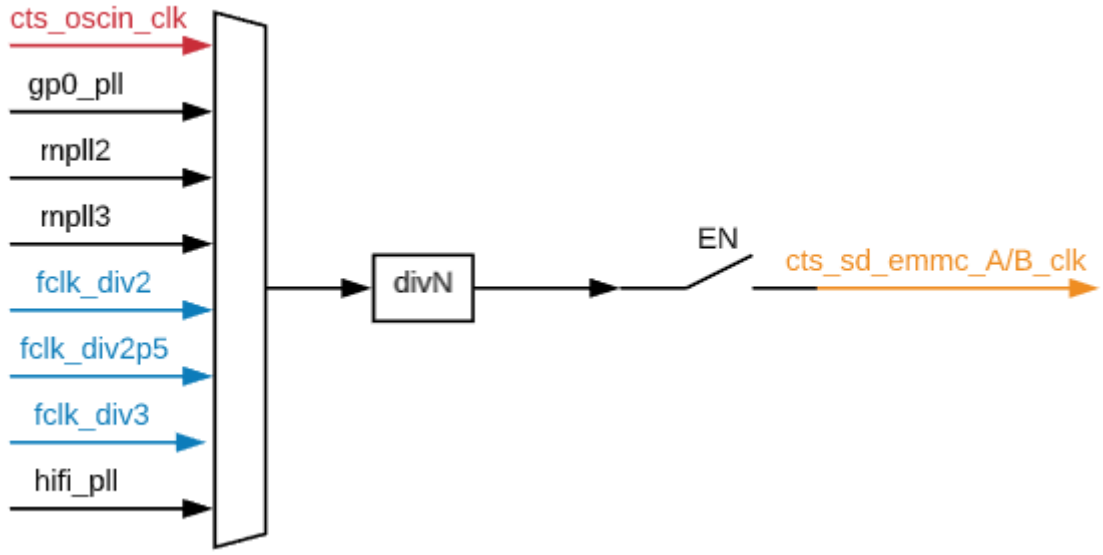


Bit(s)	R/W	Default	Description
31-12	R/W	0	unused
11-9	R/W	0	CLK_SEL: 0:cts_oscin_clk 1:fclk_div2 2:fclk_div3 3:hifi_pll_clk 4:fclk_div2p5 5:mp2_clk_out 6:mp3_clk_out 7:gp0_pll_clk

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Bit(s)	R/W	Default	Description
8			Reserved
7	R/W	1	CLK_EN:
6-0	R/W	0	div N, if you want div8, set to 7

Table 7-77 CLKCTRL_SD_EMMC_CLK_CTRL



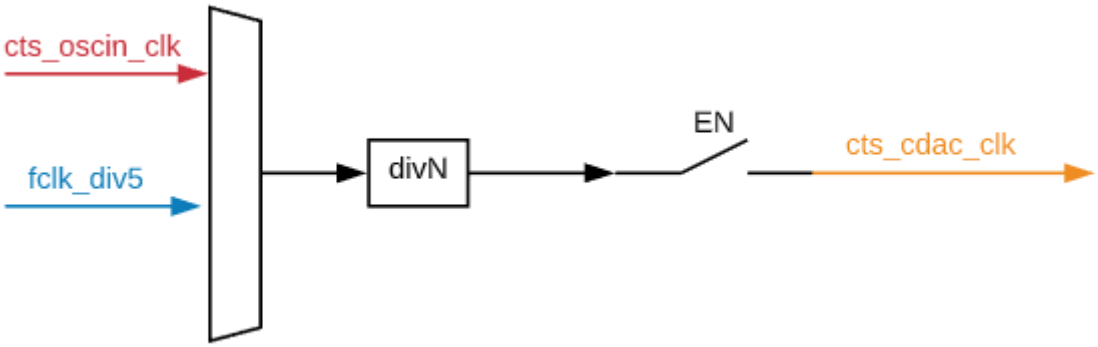
Bit(s)	R/W	Default	Description
31-28	R/W	0	unused
27-25	R/W	0	Sd_emmc_B_CLK_SEL: 0:cts_oscin_clk 1:fclk_div2 2:fclk_div3 3:hifi_pll_clk 4:fclk_div2p5 5:mp2_clk_out 6:mp3_clk_out 7:gp0_pll_clk
24	R/W		Reserved
23	R/W	1	Sd_emmc_B_CLK_EN:
22-16	R/W	0	Sd_emmc_B_CLK div N, if you want div8, set to 7
15-12	R/W	0	reseverd
11-9	R/W	0	Sd_emmc_A_CLK_SEL: 0:cts_oscin_clk 1:fclk_div2 2:fclk_div3 3:hifi_pll_clk 4:fclk_div2p5 5:mp2_clk_out 6:mp3_clk_out 7:gp0_pll_clk
8	R/W		Reserved

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Bit(s)	R/W	Default	Description
7	R/W	1	Sd_emmc_A_CLK_EN:
6-0	R/W	0	Sd_emmc_A_CLK div N, if you want div8, set to 7

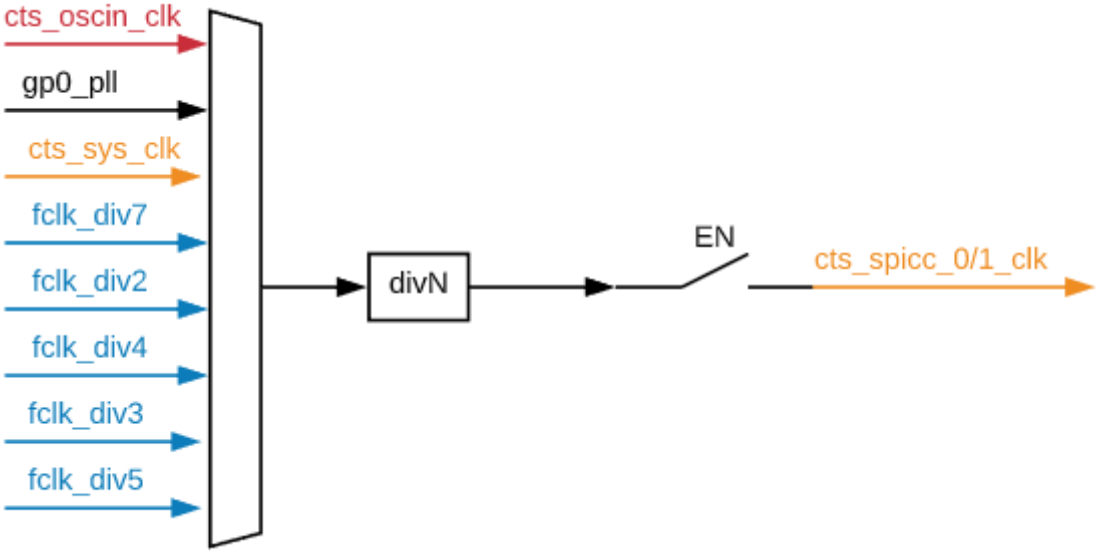
Table 7-78 CLKCTRL_CDAC_CLK_CTRL

This clock generated for vdac(cvbs).



Bit(s)	R/W	Default	Description
20	R/W	0	vdac_clk_c clk_en
17:16	R/W	0	vdac_clk_c clk_sel 0:osc; 1:fclk_div5;
15:0	R/W	0	vdac_clk_c: div N, if you want div8, set to 7

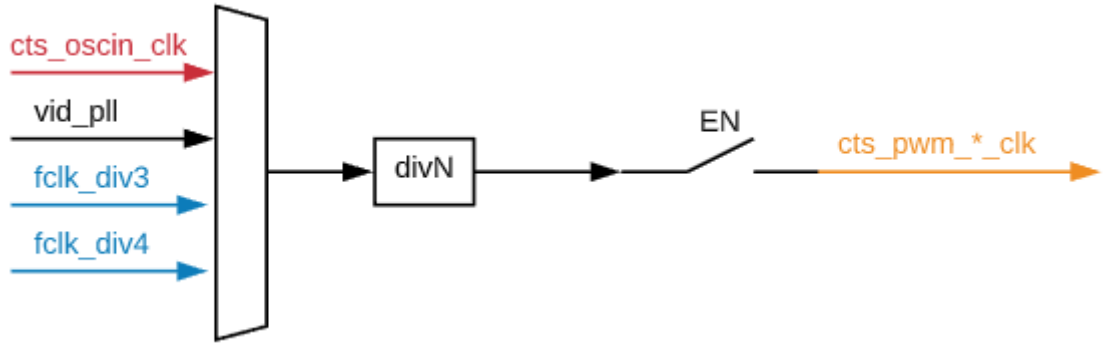
Table 7-79 CLKCTRL_SPICC_CLK_CTRL



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Bit(s)	R/W	Default	Description
9:7	R/W	0	spicc_0_clk clk_sel 0:osc; 1:sys_clk 2:fclk_div4; 3:fclk_div3; 4:fclk_div2; 5:fclk_div5; 6:fclk_div7; 7:gp0_pll;
6	R/W	0	spicc_0_clk clk_en
5:0	R/W	0	spicc_0_clk div N, if you want div8, set to 7

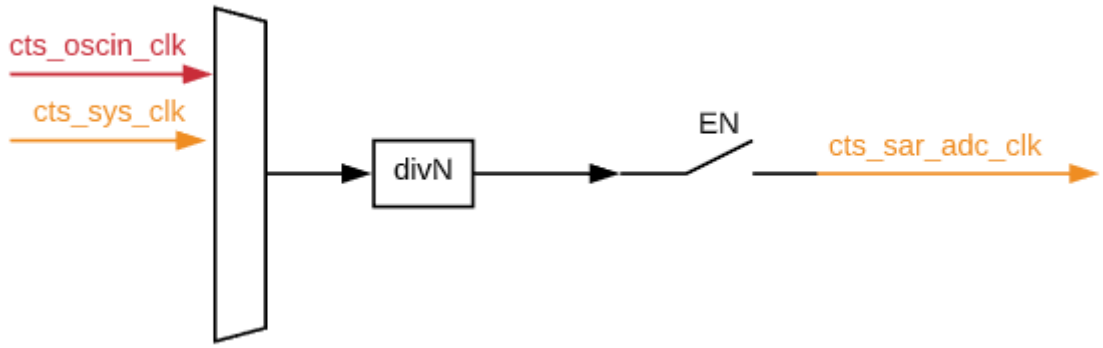
Table 7-80 CLKCTRL_PWM_CLK__CTRL**



Bit(s)	R/W	Default	Description
26:25	R/W	0	cts_pwm_j/h/f/d/b_clk clk_sel: 0: osin 1: vid_pll 2: fclk_div4 3: fclk_fiv3
24	R/W	0	cts_pwm_j/h/f/d/b_clk clk_en
23:16	R/W	0	cts_pwm_j/h/f/d/b_clk div N, if you want div8, set to 7
10:9	R/W	0	cts_pwm_i/g/e/c/a_clk clk_sel: 0: osin 1: vid_pll 2: fclk_div4 3: fclk_fiv3
8	R/W	0	cts_pwm_i/g/e/c/a_clk clk_en
7:0	R/W	0	cts_pwm_i/g/e/c/a_clk div N, if you want div8, set to 7

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Table 7-81 CLKCTRL_SAR_CLK_CTRL



Bit(s)	R/W	Default	Description
10:9	R/W	0	clk_sel: 0: osin 1: cts_sys_clkl
8	R/W	0	clk_en
7:0	R/W	0	div N, if you want div8, set to 7

Table 7-82 CLKCTRL_GEN_CLK_CTRL

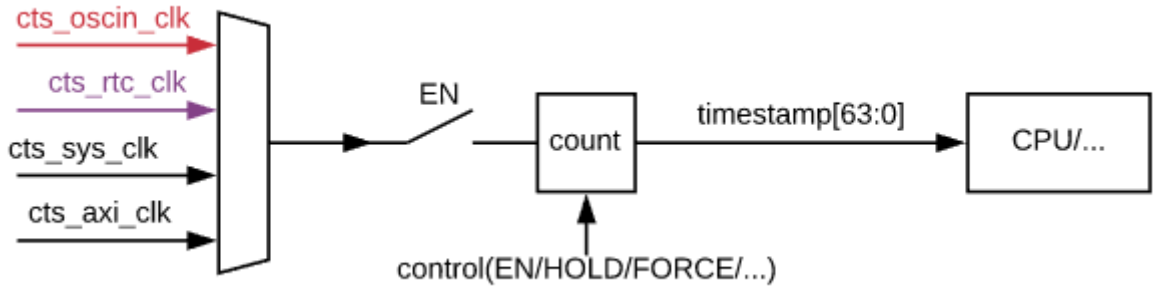
This register can control a special “GEN_CLK” which is designed for debug/monitor some internal clock quality, especially all PLL output. “GEN_CLK” will connect to one PAD(output).

Bit(s)	R/W	Default	Description
16:12	R/W	0	gen_clk source select 0: cts_oscin_clk; 1:cts_rtc_clk; 2:sys_pll_div16; 3:ddr_pll_div32 4: vid_pll 5: gp0_pll 6: gp1_pll 7: hifi_pll 12:clk_msr_src(select from all internal clock except PLLs); 16: ACODEC_DAC1 17: sys_cpu_clk_div16 19: fclk_div2 20: fclk_div2p5 21: fclk_div3 22: fclk_div4 23: fclk_div5 24: fclk_div7 25: mpll0 26: mpll1 27: mpll2 28: mpll3
11	R/W	0	gen_clk gate en
10:0	R/W	0	gen_clk div N, if you want div8, set to 7

Table 7-83 CLKCTRL_TIMESTAMP_CTRL0

CPU and some module need a timestamp signal.

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Bit(s)	R/W	Default	Description
14	R/W	0	1: hold count val;
13	R/W	0	1: force count val = {ctrl2,ctrl1}
12	R/W	1	enable
11:10	R/W	0	clk source sel: 0:cts_oscin_clk; 1:cts_rtc_clk; 2:cts_sys_clk; 3:axi_clk;
9	R/W	1	clk gate en
8:0	R/W	23	clk div N, if you want div8, set to 7

Table 7-84 CLKCTRL_TIMESTAMP_CTRL1

Bit(s)	R/W	Default	Description
31-0	R/W	0	force value[31:0]

Table 7-85 CLKCTRL_TIMESTAMP_CTRL2

Bit(s)	R/W	Default	Description
31-0	R/W	0	force value[63:32]

Table 7-86 CLKCTRL_TIMESTAMP_VAL0

Bit(s)	R/W	Default	Description
31-0	R/W	0	count val [31:0], need update by write any value first

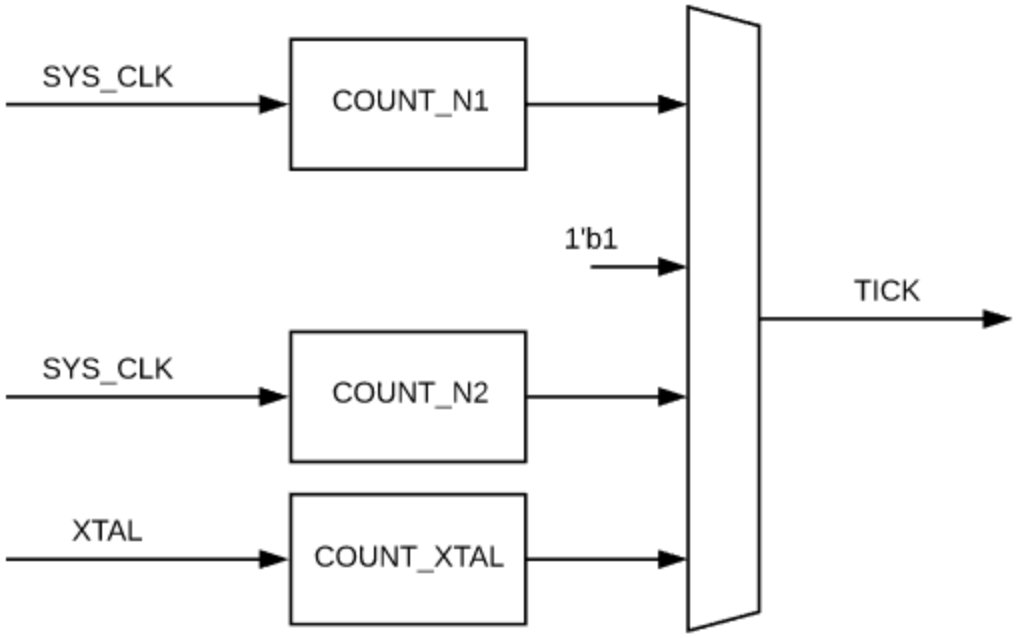
Table 7-87 CLKCTRL_TIMESTAMP_VAL1

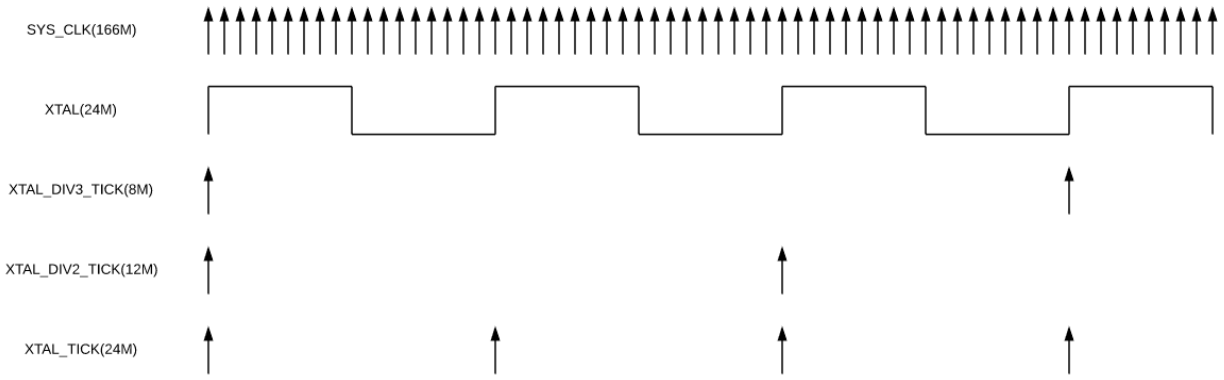
Bit(s)	R/W	Default	Description
31-0	R	0	count val [63:32], need update by write val0 register any value first

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Table 7-88 CLKCTRL_TIMEBASE_CTRL0

Some module need a fixed frequency tick as reference like UART, the tick will generated by a count which has 3 clock sources. if XTAL changed frequency, need change this register.





Bit(s)	R/W	Default	Description
31:24	R/W	0	N1, if you want div8, set to 8
23:19	R/W	0	N2, if you want div8, set to 8
18	R/W	0	1: enable xtal(24M) tick
17	R/W	1	Crystal clock enable.
16	R/W	0	Soft Reset
15:14	R/W	0	1MS_TICK: 0 = use (100US_TICK/10), 1 = hold to 1, 2 = use counter1, 3 = use counter 2
13:12	R/W	0	100US_TICK: 0 = use (10US_TICK/10), 1 = hold to 1, 2 = use counter1, 3 = use counter 2
11:10	R/W	0	10US_TICK: 0 = use (1US_TICK/10), 1 = hold to 1, 2 = use counter1, 3 = use counter 2

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Bit(s)	R/W	Default	Description
9:8	R/W	0	1US_TICK: 0 = use (Crystal/XTAL_DIV), 1 = hold to 1, 2 = use counter1, 3 = use counter 2
7:6	R/W	0	XTAL_DIV3_TICK: 0 = use Crystal/3, 1 = hold to 1, 2 = use counter1, 3 = use counter 2
5:0	R/W	24	XTAL_DIV, if you want div24000, set to 24

Table 7-89 CLKCTRL_TIMEBASE_CTRL1

Bit(s)	R/W	Default	Description
1	R/W	0	1: sync xtal_div2 by fall edge of xtal;
0	R/W	0	1: enable xtal_div2(12M) tick

Table 7-90 CLKCTRL_EFUSE_CPU_CFG01

Bit(s)	R/W	Default	Description
31:16	R/W	0xffff	efuse lock cpu clk cfg1; cfg1 must < cfg0;
15:0	R/W	0xffff	efuse lock cpu clk cfg0;

Table 7-91 CLKCTRL_EFUSE_CPU_CFG2

Bit(s)	R/W	Default	Description
15:0	R/W	0xffff	efuse lock cpu clk cfg2; cfg2 must < cfg1;

Table 7-92 CLKCTRL_EFUSE_ENCP_CFG0

Bit(s)	R/W	Default	Description
15:0	R/W	0xffff	efuse lock cts_encp_clk cfg0

Table 7-93 CLKCTRL_EFUSE_MALI_CFG01

Bit(s)	R/W	Default	Description
31:16	R/W	0xffff	efuse lock cts_mali_clk cfg1, cfg1 must < cfg0
15:0	R/W	0xffff	efuse lock cts_mali_clk cfg0

Table 7-94 CLKCTRL_EFUSE_HEVCB_CFG01

Bit(s)	R/W	Default	Description
31:16	R/W	0xffff	efuse lock cts_hevcb_clk cfg1, cfg1 must < cfg0.in fact used for cts_ hevcf_clk
15:0	R/W	0xffff	efuse lock cts_hevcb_clk cfg0.in fact used for cts_hevcf_clk

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Table 7-95 CLKCTRL_EFUSE_HEVCB_CFG2

Bit(s)	R/W	Default	Description
15:0	R/W	0xffff	efuse lock cts_hevcb_clk cfg2, cfg2 must < cfg1.in fact used for cts_ hevcf_clk

Table 7-96 CLKCTRL_EFUSE_LOCK

Each bit is write 1 once, and after write 1, will lock one EFUSE_***_CFG register.

Bit(s)	R/W	Default	Description
3	R/W	0	lock EFUSE_HEVCB_CFG01/2
2	R/W	0	lock EFUSE_MALI_CFG01
1	R/W	0	lock EFUSE_ENCP_CFG0
0	R/W	0	lock EFUSE_CPU_CFG01/2

Table 7-97 CLKCTRL_DEMOD_CLK_CTRL

Cts_demod_core_clk & adc_extclk_in is controlled by register reg_demod_clk_ctrl.

Bit(s)	R/W	Default	Description
27:25	R/W	0	adc_extclk_in clk_sel: 0: osin 1: fclk_div7 2: fclk_div4 3: adc_dpll_intclk
24	R/W	0	adc_extclk_in clk_en
22:16	R/W	0	adc_extclk_in div N, if you want div8, set to 7
10:9	R/W	0	cts_demod_core_clk clk_sel: 0: osin 1: fclk_div7 2: fclk_div4 3: adc_dpll_intclk
8	R/W	0	cts_demod_core_clk clk_en
6:0	R/W	0	cts_demod_core_clk div N, if you want div8, set to 7

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Table 7-98 CLKCTRL_CLK12_24_CTRL

Bit(s)	R/W	Default	Description
19~13	R/	0	RESERVED

11	R/W	0	crt_clk24_en; for CLK12M_24M(refer to pinmux define)
			set 1 :CLK12M_24M = 24M;
			set 0 : CLK12M_24M = 0;

10	R/W	0	clk24_div2_en; for CLK12M_24M(refer to pinmux define)
			need set crt_clk24_en = 1 first;
			set 1 :CLK12M_24M = 12M;
			set 0 : CLK12M_24M = 24M;

7.6.3 Clock Measure

Clock source is as follows:

Table 7-99 Clock Measure Source

No.	Clock Measure Source
222	cts_enc0_clk
221	cts_enc1_clk
220	cts_enc2_clk
219	cts_enc0_if_clk
218	am_ring_osc_clk_out[32]
217	am_ring_osc_clk_out[31]
216	am_ring_osc_clk_out[30]
215	am_ring_osc_clk_out[29]
214	am_ring_osc_clk_out[28]
213	am_ring_osc_clk_out[27]
212	am_ring_osc_clk_out[26]
211	am_ring_osc_clk_out[25]
210	am_ring_osc_clk_out[24]
209	am_ring_osc_clk_out[23]
208	am_ring_osc_clk_out[22]
207	am_ring_osc_clk_out[21]
206	am_ring_osc_clk_out[20]
205	vid_pll2_div_clk_out
204	vid_pll1_div_clk_out
203	mipi_csi_phy0__clk_out
202	mipi_csi_phy1__clk_out

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No.	Clock Measure Source
201	mipi_csi_phy2__clk_out
200	mipi_csi_phy3__clk_out
199	am_ring_osc_clk_out[19]
198	am_ring_osc_clk_out[18]
197	am_ring_osc_clk_out[17]
196	am_ring_osc_clk_out[16]
195	am_ring_osc_clk_out[15]
194	am_ring_osc_clk_out[14]
193	am_ring_osc_clk_out[13]
192	am_ring_osc_clk_out[12]
191	am_ring_osc_clk_out[11]
190	am_ring_osc_clk_out[10]
189	am_ring_osc_clk_out[9]
188	am_ring_osc_clk_out[8]
187	am_ring_osc_clk_out[7]
186	am_ring_osc_clk_out[6]
185	am_ring_osc_clk_out[5]
184	am_ring_osc_clk_out[4]
183	am_ring_osc_clk_out[3]
182	am_ring_osc_clk_out[2]
181	am_ring_osc_clk_out[1]
180	am_ring_osc_clk_out[0]
179	rng_ring_3
178	rng_ring_2
177	rng_ring_1
176	rng_ring_0
175	
174	
173	a73_sys_cpu_clk_div16
172	a73_sys_pll_div16
171	mclk_pll_clk
170	cts_ACLKM
169	pwm_a_clk

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No.	Clock Measure Source
168	pwm_b_clk
167	pwm_c_clk
166	pwm_d_clk
165	pwm_e_clk
164	pwm_f_clk
163	pwm_ao_a_clk
162	pwm_ao_b_clk
161	pwm_ao_c_clk
160	pwm_ao_d_clk
159	pwm_ao_e_clk
158	pwm_ao_f_clk
157	pwm_ao_g_clk
156	pwm_ao_h_clk
155	
154	
153	
152	
151	
150	
149	
148	earcrx_pll_dmac_ck
147	audio_resampleb_clk
146	audio_pdm_dclk
145	audio_spdifin_mst_clk
144	audio_spdifout_mst_clk
143	audio_spdifoutb_mst_clk
142	audio_pdm_sysclk
141	audio_resamplea_clk
140	audio_tdmin_a_sclk
139	audio_tdmin_b_sclk
138	audio_tdmin_c_sclk
137	audio_tdmin_lb_sclk
136	audio_tdmout_a_sclk

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No.	Clock Measure Source
135	audio_tdmout_b_sclk
134	audio_tdmout_c_sclk
133	audio_locker_in_clk
132	audio_locker_out_clk
131	acodec_dac_clk_x128
130	audio_vad_clk
129	
128	
127	
126	
125	
124	ts_nna_clk
123	ts_a53_clk
122	ts_a73_clk
121	cts_ts_clk(temp sensor)
120	
119	cts_anakin_clk
118	cts_spicc_0_clk
117	cts_spicc_1_clk
116	i_gpio_msr
115	cts_sd_emmc_clk_A
114	cts_sd_emmc_clk_B
113	cts_sd_emmc_clk_C
112	
111	cts_sar_adc_clk
110	cts_sc_clk(smartcard)
109	cts_dsi0_phy_clk
108	cts_dsi1_phy_clk
107	
106	
105	hdmirx_dsd_clk
104	hdmirx_aud_clk
103	hdmirx_vid_clk

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No.	Clock Measure Source
102	cts_hdmirx_meter_clk
101	cts_hdmirx_acr_ref_clk
100	cts_hdmirx_aud_pll_clk
99	cts_hevcf_clk
98	cts_hevcb_clk
97	cts_hcodec_clk
96	cts_wave521_bclk
95	cts_wave521_cclk
94	cts_wave521_aclk
93	cts_vdec_clk
92	
91	
90	
89	
88	
87	cts_spicc_2_clk
86	cts_spicc_3_clk
85	cts_spicc_4_clk
84	cts_spicc_5_clk
83	cts_hdmi_tx_pnx_clk
82	cts_hdmitx_aud_clk
81	cts_hdmitx_200m_clk
80	cts_hdmitx_prif_clk
79	
78	cts_hdmitx_fe_clk
77	cts_hdmitx_sys_clk
76	HDMITX_TMDS_CLK
75	
74	
73	cts_mipi_isp_clk
72	cts_mipi_csi_phy_clk
71	
70	cts_dsi_a_meas_clk

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No.	Clock Measure Source
69	cts_aud_sck
68	cts_aud_pll_clk
67	cts_ge2d_clk
66	cts_vapbclk
65	cts_vid_lock_clk
64	cts_vpu_clkc
61	cts_vpu_clk
63	cts_vpu_clkb_tmp
62	cts_vpu_clkb
60	cts_vdin_meas_clk
59	cts_hdmi_tx_pixel_clk
58	lcd_an_clk_ph3
57	lcd_an_clk_ph2
56	mod_tcon_clko
55	cts_vpu_clk_buf
54	cts_vdac_clk
53	
52	
51	hdmi_vid_pll_clk
50	vid_pll0_div_clk_out
49	cts_hdmirx_hdcp2x_eclk
48	cts_hdmirx_cfg_clk
47	cts_hdmirx_2m_clk
46	cts_hdmirx_5m_clk
45	hdmirx_apll_clk_audio
44	hdmirx_cable_clk
43	hdmirx_tmds_clk
42	hdmirx_apll_clk_out_div
41	cts_dsi_b_meas_clk
40	ephy_test_clk
39	eth_phy_plltxclk
38	eth_phy_rxclk
37	co_tx_clk

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No.	Clock Measure Source
36	co_rx_clk
35	mod_eth_rx_clk_rmii
34	co_clkin_to_mac
33	cts_eth_clk_rmii
32	cts_eth_clk125Mhz
31	mod_eth_tx_clk
30	mod_eth_phy_ref_clk
29	cts_gdc_clk
28	cts_amlgdc_clk
27	paie1_clk_inn
26	paie1_clk_inp
25	earcrx_pll_ckout
24	ddr0_dpll_pt_clk
23	sys_pll_div16
22	eth_mppll_50m_ckout
21	gp1_pll_clk
20	gp0_pll_clk
19	hifi_pll_clk
18	mpll_clk_test_out
17	
16	
15	mpll_clk_50m
14	mp3_clk_out
13	mp2_clk_out
12	mp1_clk_out
11	mp0_clk_out
10	fclk_div5
9	
8	cts_cecb_clk
7	cts_ceca_clk
6	sys_cpu_clk_div16
5	cts_mali_clk
4	cts_dspb_clk

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No.	Clock Measure Source
3	cts_dspa_clk
2	cts_rtc_clk
1	cts_axi_clk
0	cts_sys_clk

Register Address

For below registers the base address is 0xfe048000.

Each register final address = BASE + address * 4.

The following lists describe the mapping between each MSR_CLK register and its address.

- MSR_CLK_REG0 0xfe048000
- MSR_CLK_REG1 0xfe048004
- MSR_CLK_REG2 0xfe048008
- MSR_CLK_REG3 0xfe04800c
- MSR_CLK_REG4 0xfe048010
- MSR_CLK_REG5 0xfe048014
- MSR_CLK_DUTY 0xfe048018

Register Description

Table 7-100 MSR_CLK_DUTY

Bit(s)	R/W	Default	Description
31-16	R	0	DUTY_CNT_HIGH: This value represents the HIGH-count during duty cycle measurements
15-0	R	0	DUTY_CNT_LOW: This value represents the LOW-count during duty cycle measurements

Table 7-101 MSR_CLK_REG0

Bit(s)	R/W	Default	Description
31	R	0	BUSY: If this bit is set to 1, then the measure logic is busy
30-29	R	0	PROCESS_COUNT: This is a counter that simply increments every time a measurement is started
28	R	0	Limit Error
27-20	R/W	0	MSR_CLK_MUX_SEL: Selects the clock to measure. See example C-code
19	R/W	0	CLK_EN: The incoming clock is gated to prevent glitches from entering the measurement logic. Set this bit to 1 once the external clock has been established and is stable.
18	RW	0	One_shot_enable
17	R/W	0	CONT_EN: Set this bit to 1 to enable continuous frequency measurements

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Bit(s)	R/W	Default	Description
16	R/W	0	ENABLE: This is a general enable to enable the clock measurement circuit. If CONT_EN is set to 1 above, then the circuit will continually measure. If CONT_EN is set to 0, then the circuit will make one measurement. To restart another measurement, you must set ENABLE low then high.
15-0	R/W	0	MSR_TIME: This value establishes the gate time of the measurement with a 1uS resolution. The measurement module will count I2S MCLK clocks for N uS

Table 7-102 MSR_CLK_REG1

Bit(s)	R/W	Default	Description
31	R	0	DCYCLE_MSR_DONE: If this bit is set to 1, then the duty cycle measurement is done
30	R/W	0	unused
29	R/W	0	DCYCLE_ENABLE: Set this bit to enable start a duty cycle measurement
28	R/W	0	DCYCLE_CLK_EN: Set this bit to enable the high-frequency duty cycle clock
27-20	R/W	0	DCYCLE_TCNT: This value represents the number of uS to measure. This value should be less than 252.
19-0	R/W	0	unused

Table 7-103 MSR_CLK_REG2

Bit(s)	R/W	Default	Description
19-0	R	0	MEASURED_VALUE: This is the count of cycles measured during the programmed gate time.

Table 7-104 MSR_CLK_REG3

Bit(s)	R/W	Default	Description
19-0	R	0	Min_exp

Table 7-105 MSR_CLK_REG4

Bit(s)	R/W	Default	Description
19-0	R	0	Max_exp

Table 7-106 MSR_CLK_REG5

Bit(s)	R/W	Default	Description
0	R	0	Start_p

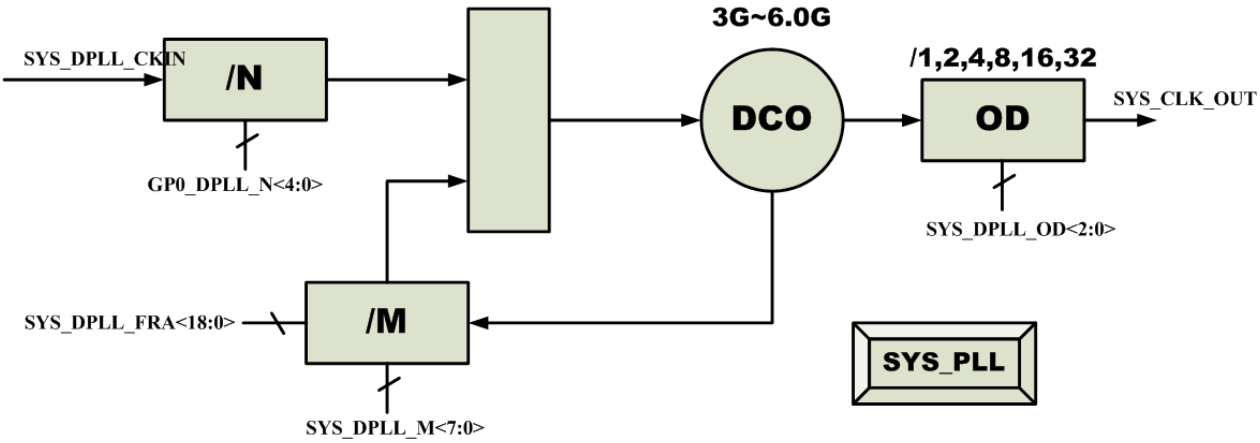
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7.6.4 Frequency Calculation

7.6.4.1 SYS_PLL

SYS_PLL diagram is shown in the following figure.

Figure 7-3 SYS_PLL



DCO frequency is calculated with the following equation:

$$f_{DCO} = f_{REF} \cdot (M + frac)/N$$

OD control table is as following.

Table 7-107 SYS_PLL OD Control

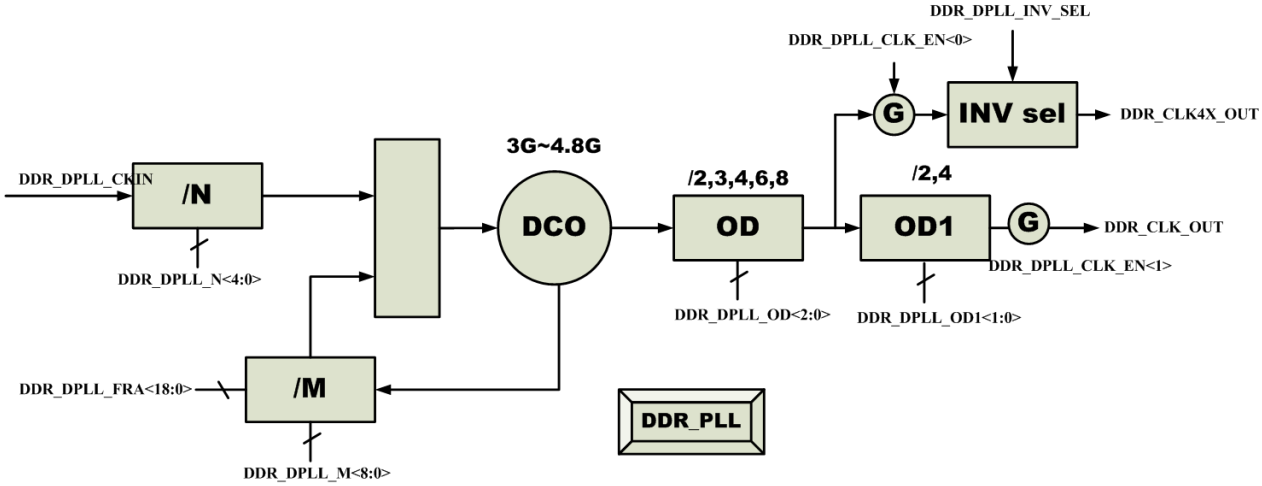
Block	Register	Function
OD	SYS_DPLL_OD<2:0>	000:/1
		001:/2
		010:/4
		011:/8
		100:/16
		101:/32

7.6.4.2 DDR_PLL

DDR_PLL diagram is shown in the following figure.

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Figure 7-4 DDR_PLL



OD control table is as following.

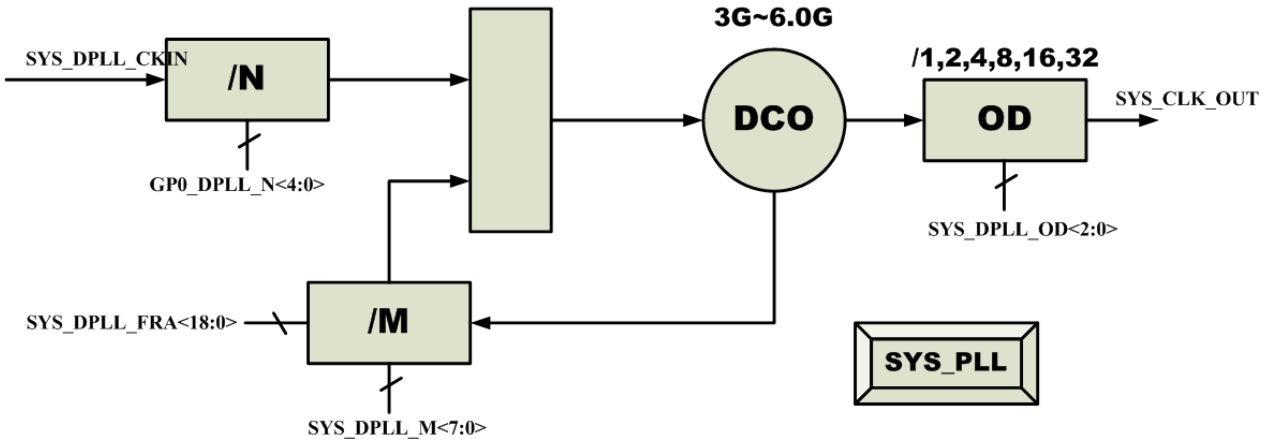
Table 7-108 DDR_PLL OD Control

Block	Register	Function
OD	DDR_DPLL_OD<2:0>	000: /2
		001:/3
		010:/4
		011:/6
		100:/8
OD1	DDR_DPLL_OD1<1:0>	*0:/2
		*1:/4

7.6.4.3 GP0_PLL

GP0_PLL diagram is shown in the following figure.

Figure 7-5 GP0_PLL



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DCO frequency is calculated with the following equation:

$$f_{DCO} = f_{REF} \cdot (M + frac)/N$$

OD control table is as following.

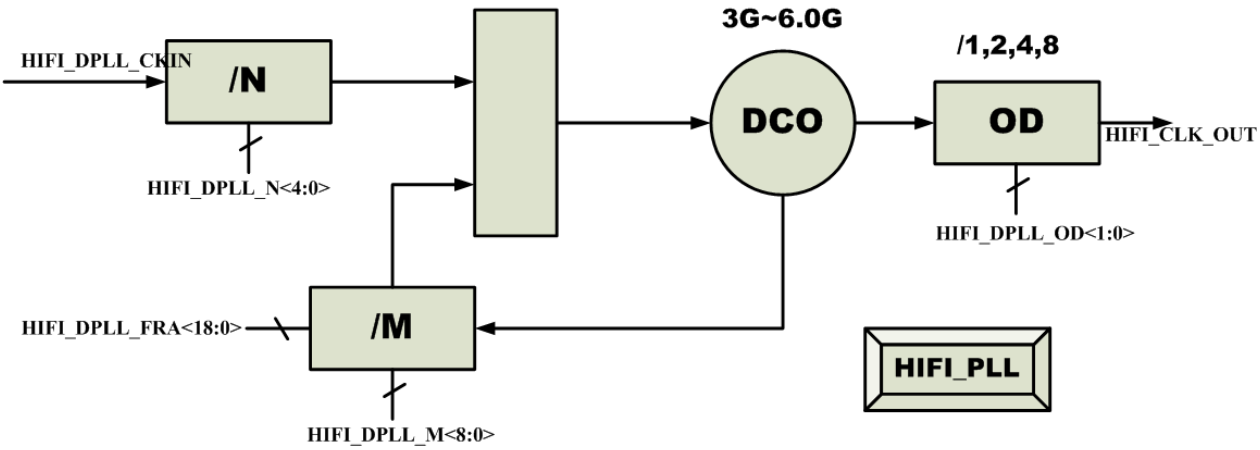
Table 7-109 GP0_PLL OD Control

Block	Register	Function
OD	GP0_DPLL_OD<2:0>	000:/1
		001:/2
		010:/4
		011:/8
		100:/16
		101:/32

7.6.4.4 HIFI PLL

HIFI PLL diagram is shown in the following figure.

Figure 7-6 HIFI PLL



DCO frequency is calculated with the following equation:

$$f_{DCO} = f_{REF} \cdot (M + frac)/N$$

OD control table is as following.

Table 7-110 HIFI PLL OD Control

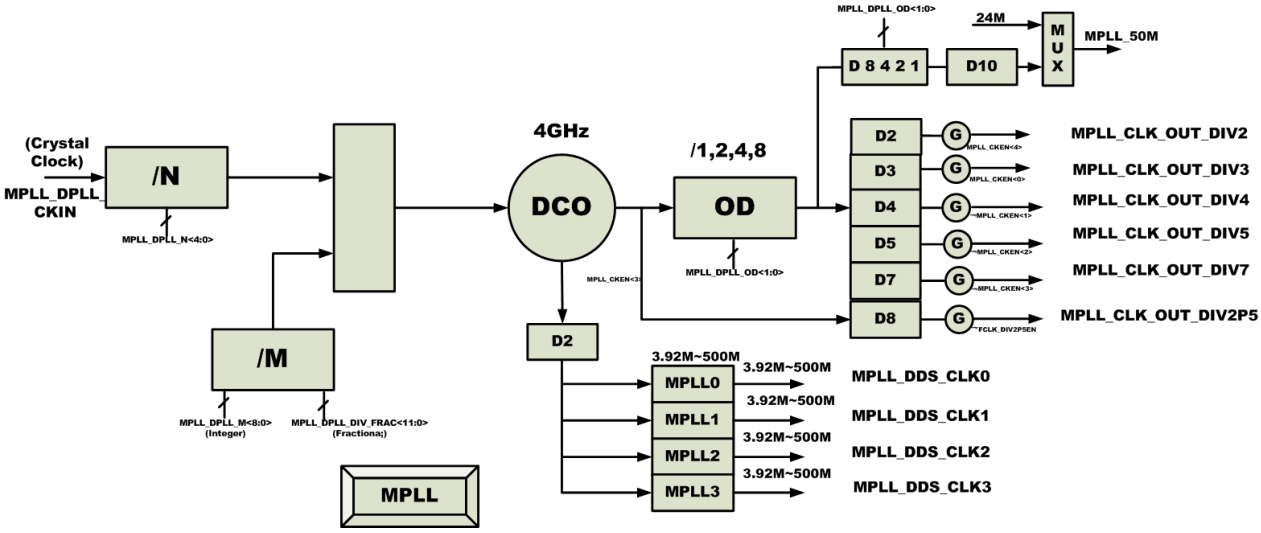
Block	Register	Function
OD	HIFI_DPLL_OD<1:0>	00:/1
		01:/2
		10:/4
		10:/8

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7.6.4.5 MPLL

MPLL diagram is shown in the following figure.

Figure 7-7 MPLL



DCO frequency is calculated with the following equation:

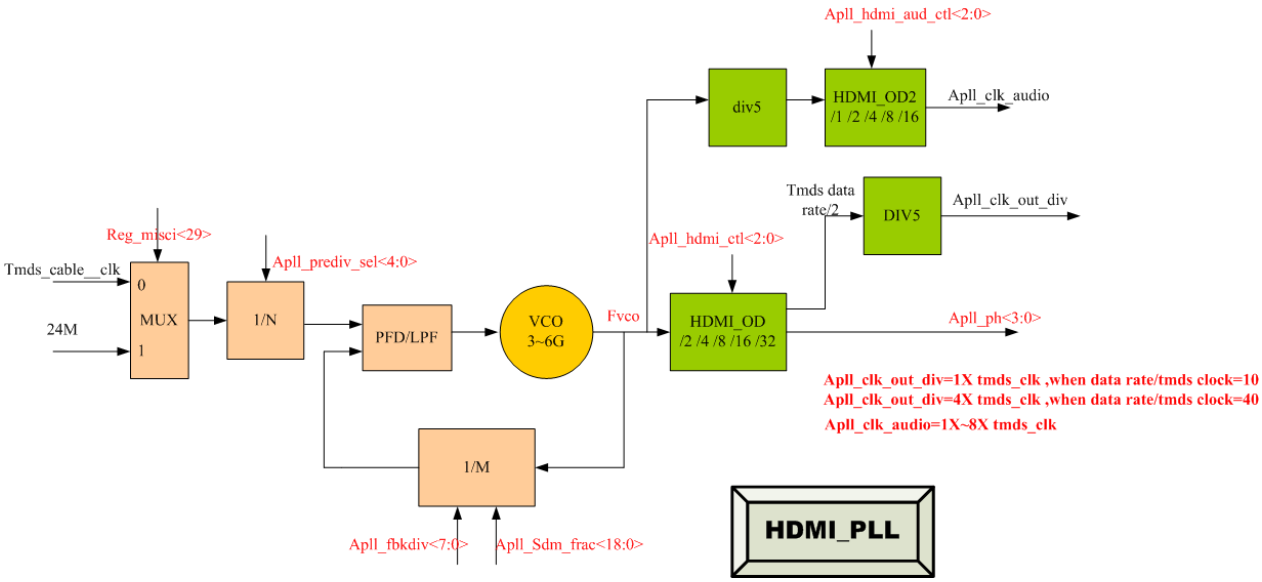
$$Fout_2G=Fref*M*OD_FB/N$$

$$MPLL_CLK_OUT2=f(N2_integer, SDM_IN) = \left(\frac{2Ghz}{(N2_integer + \frac{SDM_IN}{16384})}\right)$$

7.6.4.6 HDMI PLL

HDMI PLL diagram is shown in the following figure.

Figure 7-8 HDMI PLL



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OD control table is as following.

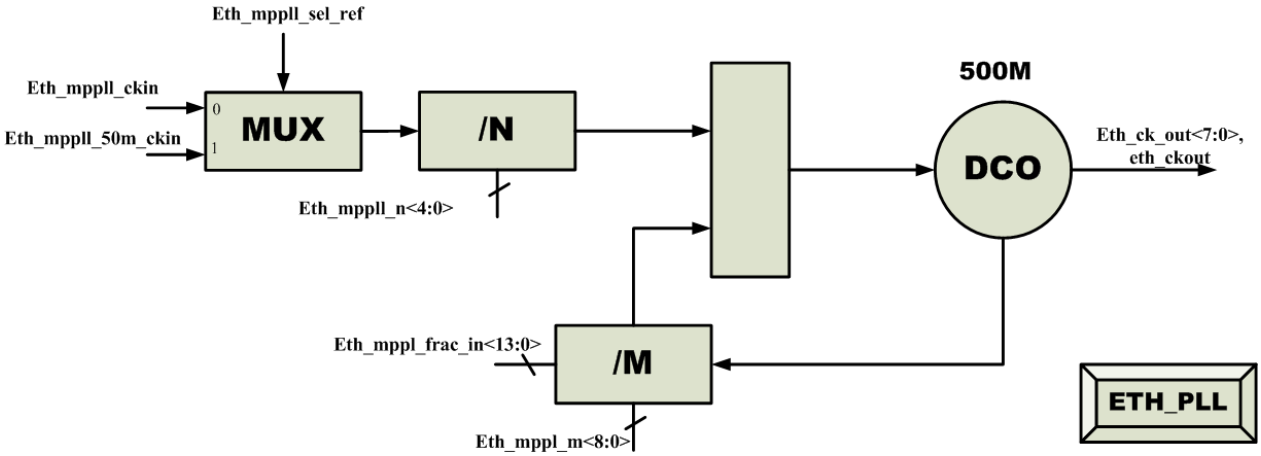
Table 7-111 HDMI PLL OD Control

Block	Register	Function
HDMI_OD	Apll_hdmi_ctrl<2:0>	001: /2
		010:/4
		011:/8
		100:/16
		101:/32
HDMI_OD2	Apll_hdmi_aud_ctrl<2:0>	000: /1
		001:/2
		010:/4
		011:/8
		100:/16

7.6.4.7 ETH PLL

ETH PLL diagram is shown in the following figure.

Figure 7-9 ETH PLL



DCO frequency is 500M.

The ETH PLL fractional value weight table is shown below.

Table 7-112 ETH PLL Fractional Value Weight Table

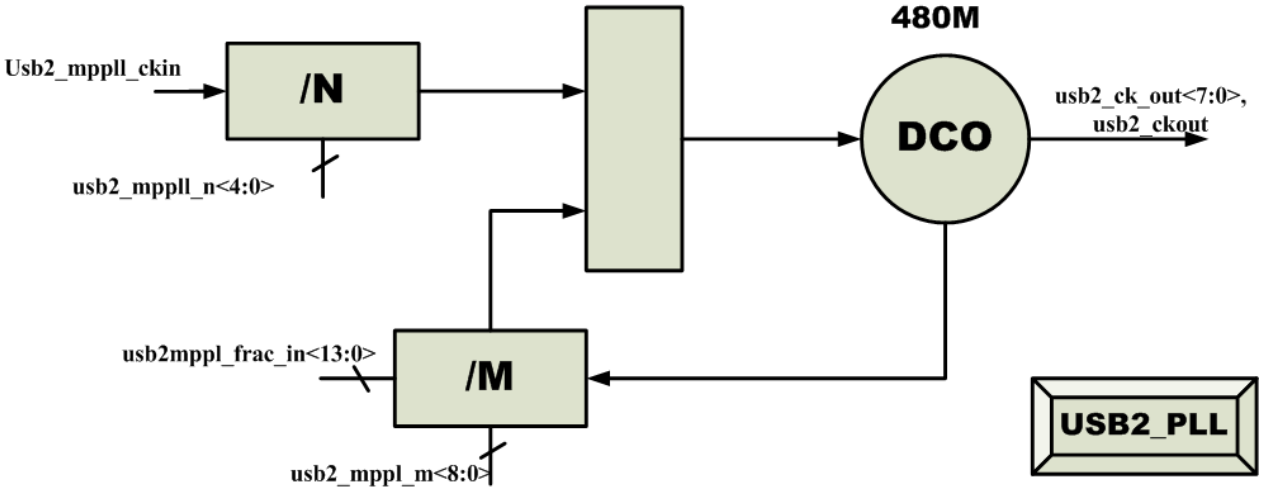
	Bit13	Bit12	Bit11	Bit10	..	..	..	..	..	..	..	Bit0
Weig-ht	1/2	1/2^2	1/2^3	1/2^4	..	..	..	..	..	..	..	1/ 2^14

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7.6.4.8 USB PLL

USB PLL diagram is shown in the following figure.

Figure 7-10 USB PLL



DCO frequency is 480M.

The USB PLL fractional value weight table is shown below.

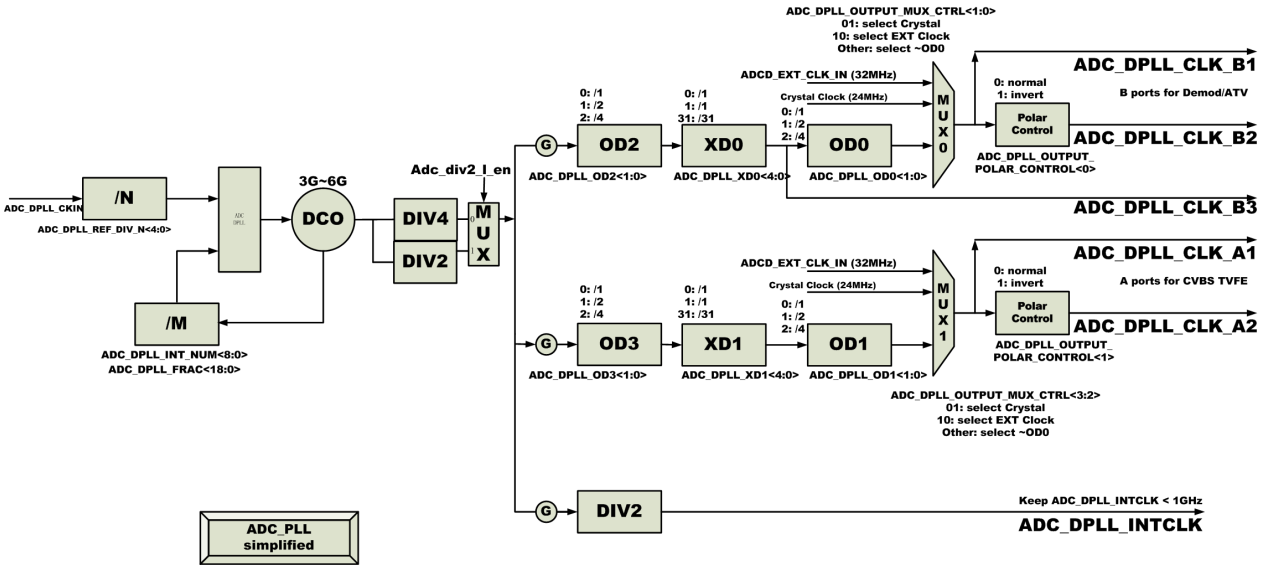
Table 7-113 USB PLL Fractional Value Weight Table

	Bit13	Bit12	Bit11	Bit10	..	..	..	..	..	..	..	Bit0
Weig-ht	1/2	1/2^2	1/2^3	1/2^4	..	..	..	..	..	..	..	1/ 2^14

7.6.4.9 ADC PLL

ADC PLL diagram is shown in the following figure.

Figure 7-11 ADC PLL



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ADC PLL DCO set same ase SYS PLL, output OD same as TXLX ADC PLL.

$$f_{DCO} = f_{REF} \cdot (NUM + frac)/N$$

Take ADC_DPLL_CLK_B2=25M for example

N=1 NUM=200 Frac=0 -> Fdco=4800M

Adc_div2_l_en=0, Fdco/4=1200M

OD2=4 XD0=12 ADC_DPLL_OUTPUT_MUX_CTRL<1:0>=11, ADC_DPLL_CLK_B2=1200/4/12=25M

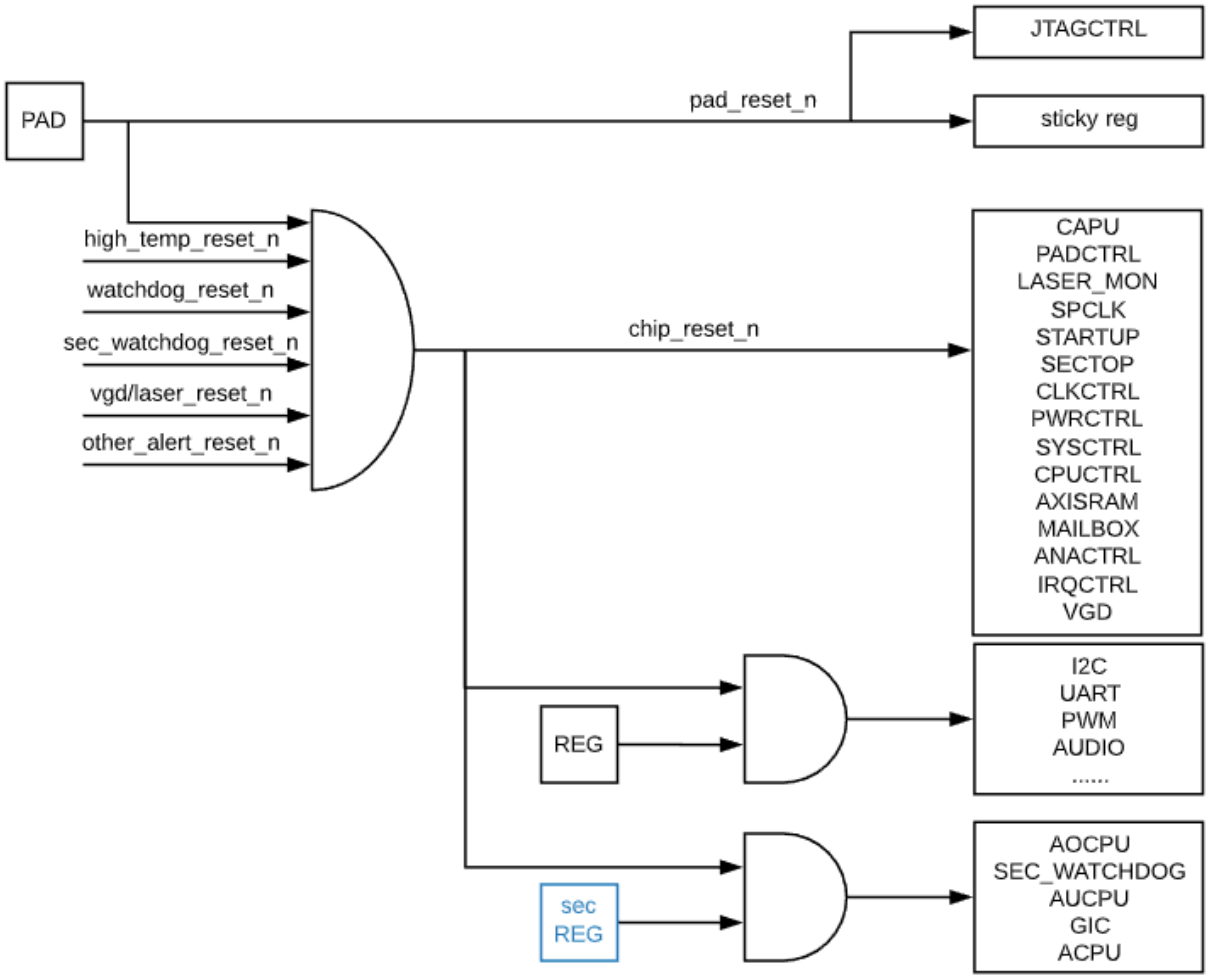
7.7 Reset

7.7.1 Overview

This module is control module level reset which shown on diagram are “REG/SEC_REG”.

And the control of watchdog is here also.

Figure 7-12 Reset Design



RESETn_module is low active.

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RESETn_module = (~RESET_reg & RESET_LEVEL) | RESET_MASK;

If set RESET_reg = 1, will reset the module.

RESET_reg is an auto-recover register which will recover to 0 after some cycles.

If set RESET_LEVEL = 0, will keep RESETn_module as low, mean the module will keep at reset status.

If set RESET_MASK = 1, will keep RESETn_module as high, mean the module will never be reset.

7.7.2 Register Description

Table 7-114 RESETCTRL_RESET0~5

RESET_reg, write each bit to 1 can reset related module, the reset will auto-cover to 0 by HW.

*mean it can reset by power control signals because it need keep reset when power off/on.

Bit(s)	reset0	reset1	reset2	reset3	reset4	reset5	sec_ reset0	sec_ reset1
31	venc*					brg_nic_ all		
30	viu*					brg_nic_ main		
29	hdmi_tx					brg_nic_ sysclk		
28	rdma*					brg_nic_ dsu		
27	venci*		watch-dog			brg_nic_ vapb		
26	vencp*		afifo		nand/ emmc			
25	vdac*		cec		sdemm-c_b			
24	vencl*		acodec		sdemm-c_a	rama		
23	vid_lock*							
22	hdmitxphy							
21	ge2d*				i2c_m_e			
20	vdi6*	Demod*			i2c_m_d			
19	vid_pll_div				i2c_m_c			
18	vcbus*		sar_adc		i2c_m_b			
17	brg_vcbus_ dec		spifc		i2c_m_a			
16	hdmitx_apb*	Ethernet*	msr_clk		i2c_s_a		gic	
15								cpu3*
14					uart_e			cpu2*
13					uart_d	brg_ hevcb_ pipl1		cpu1*

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Bit(s)	reset0	reset1	reset2	reset3	reset4	reset5	sec_ reset0	sec_ reset1
12					uart_c	brg_ hevcf_ pipl1	aucpu_ dma	cpu0*
11			rsa		uart_b		aucpu_ core	cpu_ core3*
10					uart_a		aucpu_ por	cpu_ core2*
9	usbphy21		spicc_0			brg_ma- li_pipl1	aucpu	cpu_ core1*
8	usbphy20		smart_ card		pwm_ij		sec_ watch- dog	cpu_ core0*
7					pwm_gh	brg_ma- li_pipl0		cpu_dlk_ div*
6		dos			pwm_ef	brg_cpu_ pipl0		cpu_ capb3*
5		dos_apb			pwm_cd	brg_vpu_ pipl0		cpu_rom
4	usbctrl*	ddr			pwm_ab	brg_ ge2d_ pipl0		cpu_ax*i
3	usb_ddr3	ddr_apb	tempsen- sor_pll			brg_hco- dec_ pipl0		Cpu_l2
2	usb_ddr2	mali	tempsen- sor_ddr				aocpu_ por	cpu_p*
1	usb_ddr1	mali_apb	ir_ctrl			brg_ hevcf_ pipl0	aocpu_ core	cpu_ mbist
0	usb_ddr0	audio	abus_arb			brg_ vdec_ pipl0	aocpu	

For below registers the base address is 0xfe002000.

Each register final address = BASE + address * 4.

The following lists describe the mapping between each RESET_CTRL register and its address.

RESETCTRL_RESET0 0xfe002000

RESETCTRL_RESET1 0xfe002004

RESETCTRL_RESET2 0xfe002008

RESETCTRL_RESET3 0xfe00200c

RESETCTRL_RESET4 0xfe002010

RESETCTRL_RESET5 0xfe002014

RESETCTRL_RESET0_LEVEL 0xfe002040

RESETCTRL_RESET1_LEVEL 0xfe002044

RESETCTRL_RESET2_LEVEL 0xfe002048

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RESETCTRL_RESET3_LEVEL 0xfe00204c
RESETCTRL_RESET4_LEVEL 0xfe002050
RESETCTRL_RESET5_LEVEL 0xfe002054
RESETCTRL_RESET0_MASK 0xfe002080
RESETCTRL_RESET1_MASK 0xfe002084
RESETCTRL_RESET2_MASK 0xfe002088
RESETCTRL_RESET3_MASK 0xfe00208c
RESETCTRL_RESET4_MASK 0xfe002090
RESETCTRL_RESET5_MASK 0xfe002094
RESETCTRL_RESET_HOLD_CYC 0xfe0020c0
RESETCTRL_WATCHDOG_CTRL0 0xfe002100
RESETCTRL_WATCHDOG_CTRL1 0xfe002104
RESETCTRL_WATCHDOG_CNT 0xfe002108
RESETCTRL_WATCHDOG_CLR 0xfe00210c
RESETCTRL_SEC_WATCHDOG_CTRL0 0xfe002110
RESETCTRL_SEC_WATCHDOG_CTRL1 0xfe002114
RESETCTRL_SEC_WATCHDOG_CNT 0xfe002118
RESETCTRL_SEC_WATCHDOG_CLR 0xfe00211c
RESETCTRL_SEC_RESET0 0xfe002140
RESETCTRL_SEC_RESET1 0xfe002144
RESETCTRL_SEC_RESET0_LEVEL 0xfe002180
RESETCTRL_SEC_RESET1_LEVEL 0xfe002184
RESETCTRL_SEC_RESET0_MASK 0xfe0021c0
RESETCTRL_SEC_RESET1_MASK 0xfe0021c4
RESETCTRL_RESET0_LOCK 0xfe002200
RESETCTRL_RESET1_LOCK 0xfe002204
RESETCTRL_RESET2_LOCK 0xfe002208
RESETCTRL_RESET3_LOCK 0xfe00220c
RESETCTRL_RESET4_LOCK 0xfe002210
RESETCTRL_RESET5_LOCK 0xfe002214
RESETCTRL_SEC_RESET0_LOCK 0xfe002220
RESETCTRL_SEC_RESET1_LOCK 0xfe002224
RESETCTRL_RESET0_PROT 0xfe002240
RESETCTRL_RESET1_PROT 0xfe002244
RESETCTRL_RESET2_PROT 0xfe002248
RESETCTRL_RESET3_PROT 0xfe00224c
RESETCTRL_RESET4_PROT 0xfe002250
RESETCTRL_RESET5_PROT 0xfe002254

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RESETCTRL_SEC_RESET0_PROT 0xfe002260

RESETCTRL_SEC_RESET1_PROT 0xfe002264

RESETCTRL_SEC_RESET0

Write each bit to 1 can reset related module, the reset will auto-recover to 0 by HW.

RESETCTRL_RESET0~5_LEVEL

Write each bit to 0 will hold reset as 1.

The list refer to resetctrl_reset0~5

RESETCTRL_SEC_RESET0_LEVEL

Write each bit to 0 will hold reset as 1.

Refer to resetctrl_sec_reset0

RESETCTRL_RESET0~5_MASK

Write each bit to 1 will hold reset as 0.

The list refer to resetctrl_reset0~5

RESETCTRL_SEC_RESET0_MASK

Write each bit to 1 will hold reset as 0.

The list refer to resetctrl_sec_reset0

RESETCTRL_RESET0~5_LOCK

Each bit can write 1 only

Write each bit to 1 will lock reg reset/level/mask.

The list refer to resetctrl_reset0~5

RESETCTRL_SEC_RESET0_LOCK

Each bit can write 1 only

Write each bit to 1 will lock reg reset/level/mask.

The list refer to resetctrl_sec_reset0

RESETCTRL_RESET0~5_PROT

Write each bit to 1 will protect(can’t write) reg reset/level/mask.

The list refer to resetctrl_reset0~5

RESETCTRL_SEC_RESET0_PROT

Write each bit to 1 will protect(can’t write) reg reset/level/mask.

The list refer to resetctrl_sec_reset0

Table 7-115 RESETCTRL_RESET_HOLD_CYC

Bit(s)	R/W	Default	Description
4:0	R/W	3	the cycle number of auto-recover

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Table 7-116 RESETCTRL_WATCHDOG_CTRL0

Bit(s)	R/W	Default	Description
31	R	0	watchdog status(RESET value)
27	R/W	0	the RESET OUT value when watchdog_en = 0; high active;
25	R/W	0	Clk_div_en
24	R/W	1	Clk_en
23	R/W	0	Interrupt_en
22	R/W	0	reset_n_en
19	R/W	0	Clk_sel 0: cts_oscin_clk; 1:cts_sys_clk;
18	R/W	0	Watchdog_en
17-0	R/W	23999	Clk_div_tcnt

Table 7-117 RESETCTRL_WATCHDOG_CTRL1

Bit(s)	R/W	Default	Description
17	R/W	0	Gpio_pulse
16	R/W	0	Gpio_polarity
15-0	R/W	0	Gpio_pulse_tcnt

Table 7-118 RESETCTRL_WATCHDOG_CNT

Bit(s)	R/W	Default	Description
31-16	R	0	Watchdog count read
15-0	R/W	0	Watchdog_count set

Table 7-119 RESETCTRL_WATCHDOG_CLR

Bit(s)	R/W	Default	Description
31:0	W	0	write any value will clear watchdog status

RESETCTRL_SEC_WATCHDOG_CTRL0

RESETCTRL_SEC_WATCHDOG_CTRL1

RESETCTRL_SEC_WATCHDOG_CNT

RESETCTRL_SEC_WATCHDOG_CLR

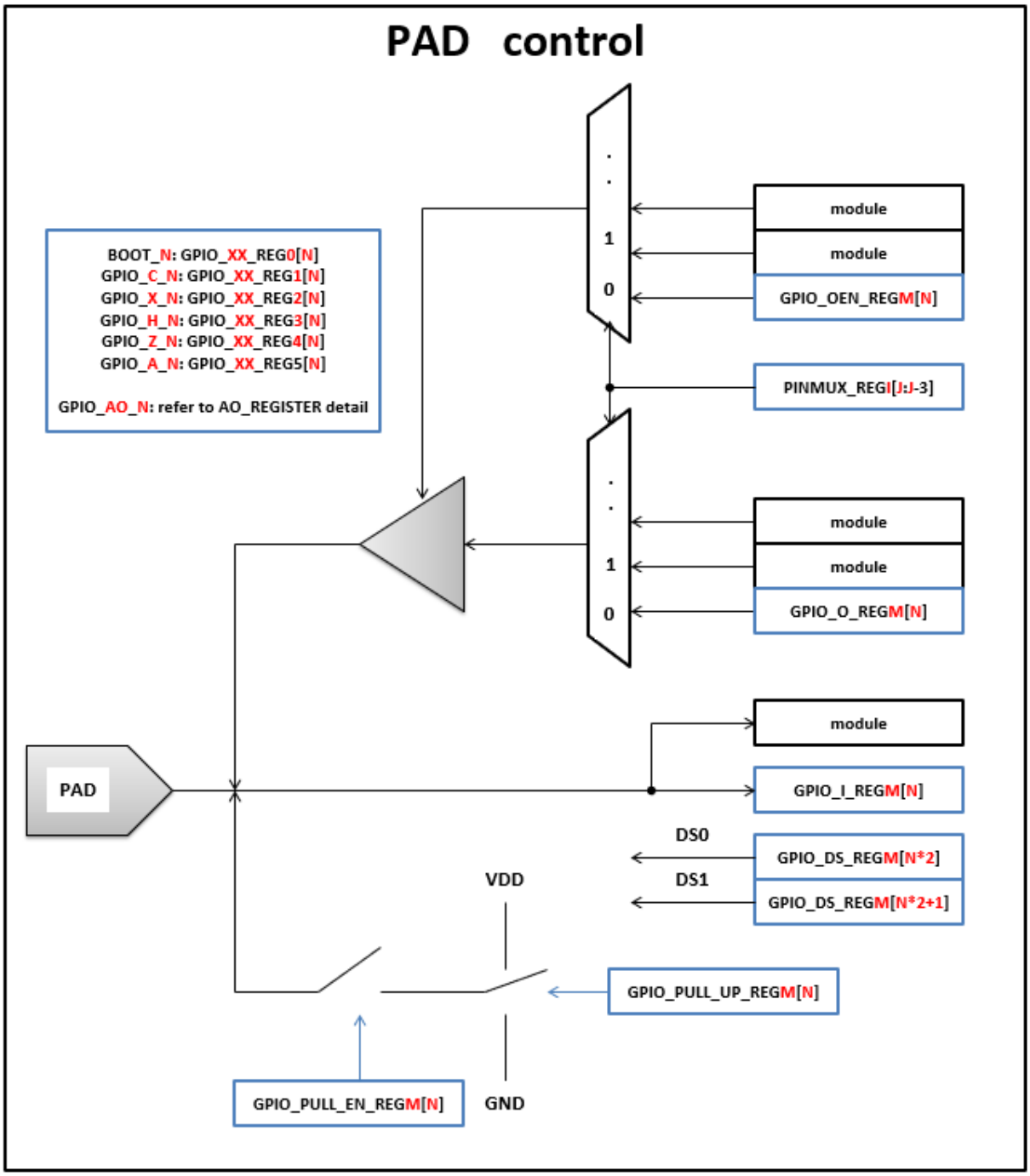
7.8 GPIO

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7.8.1 Overview

The SOC has a number of multi-function digital I/O pads that can be multiplexed to a number of internal resources (e.g. PWM generators, SDIO controllers). When a digital I/O is not being used for any specific purpose, it is converted to a general purpose GPIO pin. A GPIO pin can be statically set to high/low logical levels. The structure of a GPIO is given below.

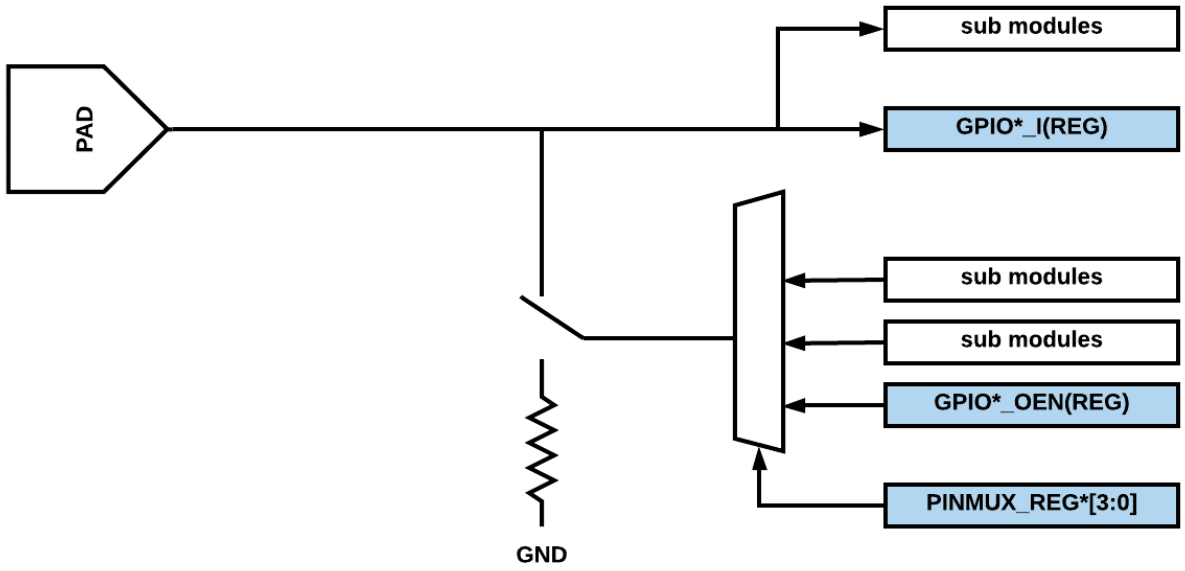
Figure 7-13 GPIO Structure



GPIOC_7 and GPIOH_0/1/2/3 are OD PAD, each OD PAD include 3 register.

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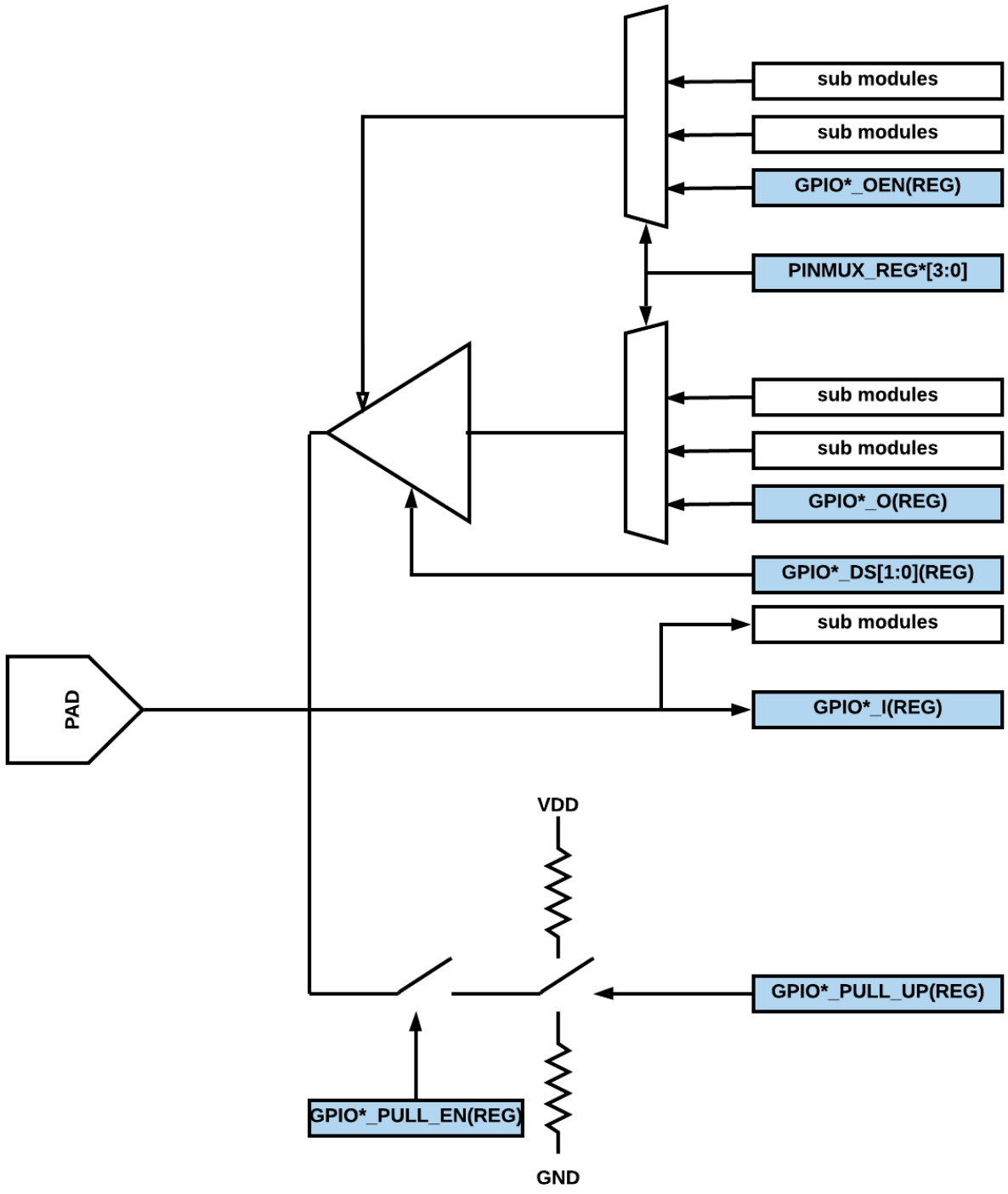
Figure 7-14 OD PAD Structure



All other PAD are GPIO PAD, each GPIO PAD include 7 registers.

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Figure 7-15 GPIO PAD Structure



7.8.2 GPIO Multiplex Function

The GPIO multiplex functions are shown in the sections below.

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Table 7-120 GPIOZ_x Multi-Function Pin

Pin Name	Control Register	Control Bit	Func1	Func2	Func3	Func4	Func5	Func6	Func7
GPIOZ_0	PADCTRL_PIN_MUX_REG6	[3:0]	TDM_FS2	TSin_A_CLK	SDCARD_D0	SPI_A_MISO	UART_D_TX		
GPIOZ_1		[7:4]	TDM_SCLK2	TSin_A_SOP	SDCARD_D1	SPI_A_MOSI	UART_D_RX		
GPIOZ_2		[11:8]	TDM_D4	TSin_A_VALID	SDCARD_D2	SPI_A_CLK	UART_D_CTS		
GPIOZ_3		[15:12]	TDM_D5	TSin_A_D0	SDCARD_D3	SPI_A_SS0	UART_D_RTS		
GPIOZ_4		[19:16]	TDM_D6		SDCARD_CLK	SPI_A_SS1	PWM_G		
GPIOZ_5		[23:20]	TDM_D7		SDCARD_CMD	SPI_A_SS2	PWM_F		
GPIOZ_6		[27:24]	MCLK_2	DTV_A_IF_AGC			PWM_E		
GPIOZ_7		[31:28]		DTV_B_IF_AGC				DISEQC_OUT	
GPIOZ_8	PADCTRL_PIN_MUX_REG7	[3:0]		I2CM_D_SDA	UART_E_TX				
GPIOZ_9		[7:4]	SPDIF_OUT	I2CM_D_SCL	UART_E_RX				GEN_CLK
GPIOZ_10		[11:8]	DTV_A_IF_AGC	DTV_A_RF_AGC	PDM_DIN1				
GPIOZ_11		[15:12]	UART_E_TX	DTV_B_RF_AGC	PDM_DIN0	I2CM_E_SCL			
GPIOZ_12		[19:16]	UART_E_RX		PDM_DCLK	I2CM_E_SDA			GEN_CLK

Table 7-121 GPIOC_x Multi-Function Pin

Pin Name	Control Register	Control Bit	Func1	Func2	Func3	Func4
GPIOC_0	PADCTRL_PIN_MUX_REG9	[3:0]	SDCARD_D0	JTAG2_TDO	PDM_DIN1	TDM_D2
GPIOC_1		[7:4]	SDCARD_D1	JTAG2_TDI	PDM_DIN0	TDM_D3
GPIOC_2		[11:8]	SDCARD_D2	UART_B_RX	I2CM_E_SCL	TDM_FS1
GPIOC_3		[15:12]	SDCARD_D3	UART_B_TX	I2CM_E_SDA	TDM_SCLK1
GPIOC_4		[19:16]	SDCARD_CLK	JTAG2_CLK	PDM_DCLK	MCLK_1
GPIOC_5		[23:20]	SDCARD_CMD	JTAG2_TMS	ISO7816_CLK	TDM_D4
GPIOC_6		[27:24]		I2CM_B_SDA	ISO7816_DATA	TDM_D5
GPIOC_7		[31:28]		I2CM_B_SCL		

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Table 7-122 GPIOX_x Multi-Function Pin

Pin Name	Control Register	Control Bit	Func1	Func2	Func3	Func4	Func5
GPIOX_0	PADCTRL_PIN_MUX_REG3	[3:0]	SDIO_D0				
GPIOX_1		[7:4]	SDIO_D1				
GPIOX_2		[11:8]	SDIO_D2				
GPIOX_3		[15:12]	SDIO_D3				
GPIOX_4		[19:16]	SDIO_CLK				
GPIOX_5		[23:20]	SDIO_CMD				
GPIOX_6		[27:24]	PWM_A				
GPIOX_7		[31:28]	PWM_F				
GPIOX_8	PADCTRL_PIN_MUX_REG4	[3:0]	TDM_D1	PDM_DIN0	SPI_A_MOSI	PWM_C	
GPIOX_9		[7:4]	TDM_D0	PDM_DIN1	SPI_A_MISO		
GPIOX_10		[11:8]	TDM_FS0		SPI_A_SS0	I2CS_A_SDA	I2CM_D_SDA
GPIOX_11		[15:12]	TDM_SCLK0	PDM_DCLK	SPI_A_CLK	I2CS_A_SCL	I2CM_D_SCL
GPIOX_12		[19:16]	UART_A_TX				
GPIOX_13		[23:20]	UART_A_RX				
GPIOX_14		[27:24]	UART_A_CTS				
GPIOX_15		[31:28]	UART_A_RTS				
GPIOX_16	PADCTRL_PIN_MUX_REG5	[3:0]	PWM_E				
GPIOX_17		[7:4]	I2CM_B_SDA				
GPIOX_18		[11:8]	I2CM_B_SCL				
GPIOX_19		[15:12]	PWM_B				

Table 7-123 GPIOH_x Multi-Function Pin

Pin Name	Control Register	Control Bit	Func1	Func2	Func3	Func4	Func5	Func6
GPIOH_0	PADCTR-L_PIN_MUX_REGB	[3:0]	HDMITX_SDA	I2CM_C_SDA				
GPIOH_1		[7:4]	HDMITX_SCL	I2CM_C_SCL				
GPIOH_2		[11:8]	HDMITX_HPD_IN					
GPIOH_3		[15:12]	AO_CEC_A	AO_CEC_B				

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Pin Name	Control Register	Control Bit	Func1	Func2	Func3	Func4	Func5	Func6
GPIOH_4		[19:16]	SPDIF_OUT	UART_D_TX		MCLK_1	SPI_A_MISO	
GPIOH_5		[23:20]	SPDIF_IN	UART_D_RX		TDM_SCLK1	SPI_A_MOSI	
GPIOH_6		[27:24]	I2CM_B_SDA	UART_D_CTS	PWM_D	TDM_FS1	SPI_A_CLK	
GPIOH_7		[31:28]	I2CM_B_SCL	UART_D_RTS	PWM_I	TDM_D2	SPI_A_SS0	
GPIOH_8	PADCTR-L_PIN_MUX_REGC	[3:0]	I2CM_C_SDA	ISO7816_CLK	PDM_DCLK	TDM_D3		
GPIOH_9		[7:4]	I2CM_C_SCL	ISO7816_DATA	PDM_DIN0	TDM_D4		
GPIOH_10		[11:8]	ETH_LINK_LED	UART_E_TX	PDM_DIN1			
GPIOH_11		[15:12]	ETH_ACT_LED	UART_E_RX				GEN_CLK

Table 7-124 GPIOE_x Multi-Function Pin

Pin Name	Control Register	Control Bit	Func1	Func2	Func3
GPIOE_0	PADCTRL_PIN_MUX_REGI	[3:0]	I2CM_A_SDA	UART_B_TX	PWM_H
GPIOE_1		[7:4]	I2CM_A_SCL	UART_B_RX	PWM_J

Table 7-125 GPIOD_x Multi-Function Pin

Pin Name	Control Register	Control Bit	Func1	Func2	Func3	Func4	Func5	Func6
GPIOD_0	PADCTR-L_PIN_MUX_REGG	[3:0]	UART_B_TX					
GPIOD_1		[7:4]	UART_B_RX					
GPIOD_2		[11:8]	UART_B_CTS	I2CM_E_SCL	UART_C_TX	CLK_32K_IN	MIC_MUTE_EN	
GPIOD_3		[15:12]	UART_B_RTS	I2CM_E_SDA	UART_C_RX		MIC_MUTE_KEY	
GPIOD_4		[19:16]	IR_RE-MOTE_OUT	MCLK_1	PWM_B	PWM_B_HIZ		
GPIOD_5		[23:20]	IR_RE-MOTE_INPUT					
GPIOD_6		[27:24]	JTAG_CLK	TDM_SCLK1	PWM_A	PWM_A_HIZ	I2CM_B_SDA	
GPIOD_7		[31:28]	JTAG_TMS	TDM_FS1	PWM_C	PWM_C_HIZ	I2CM_B_SCL	

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Pin Name	Control Register	Control Bit	Func1	Func2	Func3	Func4	Func5	Func6
GPIOD_8	PADCTR-L_PIN_MUX_REGH	[3:0]	JTAG_TDI	TDM_D4	PWM_D	PDM_DCLK		
GPIOD_9		[7:4]	JTAG_TDO	TDM_D3	PWM_I	PDM_DIN0		
GPIOD_10		[11:8]	CLK12M_24M	TDM_D2		PDM_DIN1	I2CM_C_SDA	GEN_CLK
GPIOD_11		[15:12]	PWM_G_HIZ	PWM_G			I2CM_C_SCL	

Table 7-126 GPIOB_x Multi-Function Pin

Pin Name	Control Register	Control Bit	Fun1	Func2	Func3
GPIOB_0	PADCTR-L_PIN_MUX_REG0	3:0	EMMC_D0		
GPIOB_1		7:4	EMMC_D1		
GPIOB_2		11:8	EMMC_D2		
GPIOB_3		15:12	EMMC_D3		SPIF_HOLD
GPIOB_4		19:16	EMMC_D4		SPIF_MO
GPIOB_5		23:20	EMMC_D5		SPIF_MI
GPIOB_6		27:24	EMMC_D6		SPIF_CLK
GPIOB_7		31:28	EMMC_D7		SPIF_WP
GPIOB_8	PADCTR-L_PIN_MUX_REG1	3:0	EMMC_CLK	NAND_WEN_CLK	
GPIOB_9		7:4		NAND_ALE	
GPIOB_10		11:8	EMMC_CMD	NAND_REN_WR	
GPIOB_11		15:12	EMMC_DS	NAND_CLE	
GPIOB_12		19:16		NAND_CE0	
GPIOB_13		23:20			SPIF_CS

7.8.3 Register Description

For below registers the base address is 0xfe004000.

Each register final address = BASE + address * 4.

The following lists describe the mapping between each PAD_CTRL register and its address.

PADCTRL_PIN_MUX_REG0 0xfe004000

PADCTRL_PIN_MUX_REG1 0xfe004004

//define PADCTRL_PIN_MUX_REG2 8'h02

PADCTRL_PIN_MUX_REG3 0xfe00400c

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PADCTRL_PIN_MUX_REG4 0xfe004010
PADCTRL_PIN_MUX_REG5 0xfe004014
PADCTRL_PIN_MUX_REG6 0xfe004018
PADCTRL_PIN_MUX_REG7 0xfe00401c
//define PADCTRL_PIN_MUX_REG8 8'h08
PADCTRL_PIN_MUX_REG9 0xfe004024
//define PADCTRL_PIN_MUX_REGA 8'h0a
PADCTRL_PIN_MUX_REGB 0xfe00402c
PADCTRL_PIN_MUX_REGC 0xfe004030
//define PADCTRL_PIN_MUX_REGD 8'h0d
//define PADCTRL_PIN_MUX_REGE 8'h0e
//define PADCTRL_PIN_MUX_REGF 8'h0f
PADCTRL_PIN_MUX_REGG 0xfe004040
PADCTRL_PIN_MUX_REGH 0xfe004044
PADCTRL_PIN_MUX_REGI 0xfe004048
//define PADCTRL_PIN_MUX_REGJ 8'h13
PADCTRL_GPIO_IRQ_CTRL0 0xfe004080
PADCTRL_GPIO_IRQ_CTRL1 0xfe004084
PADCTRL_GPIO_IRQ_CTRL2 0xfe004088
PADCTRL_GPIO_IRQ_CTRL3 0xfe00408c
PADCTRL_GPIO_IRQ_CTRL4 0xfe004090
PADCTRL_GPIO_IRQ_CTRL5 0xfe004094
PADCTRL_GPIO_IRQ_CTRL6 0xfe004098
PADCTRL_GPIO_IRQ_CTRL7 0xfe00409c
PADCTRL_WORLD_SYNC_CTRL0 0xfe0040a0
PADCTRL_GPIO_MSR_CTRL0 0xfe0040a4
PADCTRL_MISC_CTRL0 0xfe0040a8
PADCTRL_GPIOZ_I 0xfe0040c0
PADCTRL_GPIOZ_O 0xfe0040c4
PADCTRL_GPIOZ_OEN 0xfe0040c8
PADCTRL_GPIOZ_PULL_EN 0xfe0040cc
PADCTRL_GPIOZ_PULL_UP 0xfe0040d0
PADCTRL_GPIOZ_LOCK 0xfe0040d4
PADCTRL_GPIOZ_PROT 0xfe0040d8
PADCTRL_GPIOZ_DS 0xfe0040dc
PADCTRL_GPIOX_I 0xfe004100
PADCTRL_GPIOX_O 0xfe004104
PADCTRL_GPIOX_OEN 0xfe004108

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PADCTRL_GPIOX_PULL_EN 0xfe00410c
PADCTRL_GPIOX_PULL_UP 0xfe004110
PADCTRL_GPIOX_LOCK 0xfe004114
PADCTRL_GPIOX_PROT 0xfe004118
PADCTRL_GPIOX_DS 0xfe00411c
PADCTRL_GPIOX_DS_EXT 0xfe004120
PADCTRL_GPIOH_I 0xfe004140
PADCTRL_GPIOH_O 0xfe004144
PADCTRL_GPIOH_OEN 0xfe004148
PADCTRL_GPIOH_PULL_EN 0xfe00414c
PADCTRL_GPIOH_PULL_UP 0xfe004150
PADCTRL_GPIOH_LOCK 0xfe004154
PADCTRL_GPIOH_PROT 0xfe004158
PADCTRL_GPIOH_DS 0xfe00415c
PADCTRL_GPIOD_I 0xfe004180
PADCTRL_GPIOD_O 0xfe004184
PADCTRL_GPIOD_OEN 0xfe004188
PADCTRL_GPIOD_PULL_EN 0xfe00418c
PADCTRL_GPIOD_PULL_UP 0xfe004190
PADCTRL_GPIOD_LOCK 0xfe004194
PADCTRL_GPIOD_PROT 0xfe004198
PADCTRL_GPIOD_DS 0xfe00419c
PADCTRL_GPIOE_I 0xfe0041c0
PADCTRL_GPIOE_O 0xfe0041c4
PADCTRL_GPIOE_OEN 0xfe0041c8
PADCTRL_GPIOE_PULL_EN 0xfe0041cc
PADCTRL_GPIOE_PULL_UP 0xfe0041d0
PADCTRL_GPIOE_LOCK 0xfe0041d4
PADCTRL_GPIOE_PROT 0xfe0041d8
PADCTRL_GPIOE_DS 0xfe0041dc
PADCTRL_GPIOC_I 0xfe004200
PADCTRL_GPIOC_O 0xfe004204
PADCTRL_GPIOC_OEN 0xfe004208
PADCTRL_GPIOC_PULL_EN 0xfe00420c
PADCTRL_GPIOC_PULL_UP 0xfe004210
PADCTRL_GPIOC_LOCK 0xfe004214
PADCTRL_GPIOC_PROT 0xfe004218
PADCTRL_GPIOC_DS 0xfe00421c

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PADCTRL_GPIOB_I 0xfe004240
PADCTRL_GPIOB_O 0xfe004244
PADCTRL_GPIOB_OEN 0xfe004248
PADCTRL_GPIOB_PULL_EN 0xfe00424c
PADCTRL_GPIOB_PULL_UP 0xfe004250
PADCTRL_GPIOB_LOCK 0xfe004254
PADCTRL_GPIOB_PROT 0xfe004258
PADCTRL_GPIOB_DS 0xfe00425c
//define PADCTRL_GPIOA_I 8'hA0
//define PADCTRL_GPIOA_O 8'hA1
//define PADCTRL_GPIOA_OEN 8'hA2
//define PADCTRL_GPIOA_PULL_EN 8'hA3
//define PADCTRL_GPIOA_PULL_UP 8'hA4
//define PADCTRL_GPIOA_LOCK 8'hA5
//define PADCTRL_GPIOA_PROT 8'hA6
//define PADCTRL_GPIOA_DS 8'hA7
PADCTRL_TESTN_I 0xfe0042c0
PADCTRL_TESTN_O 0xfe0042c4
PADCTRL_TESTN_OEN 0xfe0042c8
PADCTRL_TESTN_PULL_EN 0xfe0042cc
PADCTRL_TESTN_PULL_UP 0xfe0042d0
PADCTRL_TESTN_LOCK 0xfe0042d4
PADCTRL_TESTN_PROT 0xfe0042d8
PADCTRL_TESTN_DS 0xfe0042dc
PADCTRL_ANALOG_I 0xfe004300
PADCTRL_ANALOG_EN 0xfe004304
PADCTRL_LOCK_PIN_MUX0 0xfe004340
PADCTRL_LOCK_PIN_MUX1 0xfe004344
PADCTRL_LOCK_PIN_MUX2 0xfe004348
PADCTRL_LOCK_PIN_MUX3 0xfe00434c
PADCTRL_LOCK_PIN_MUX4 0xfe004350
PADCTRL_PROT_PIN_MUX0 0xfe004360
PADCTRL_PROT_PIN_MUX1 0xfe004364
PADCTRL_PROT_PIN_MUX2 0xfe004368
PADCTRL_PROT_PIN_MUX3 0xfe00436c
PADCTRL_PROT_PIN_MUX4 0xfe004370
PADCTRL_MUTE_CTRL 0xfe004380
PADCTRL_MUTE_TDM_DISA 0xfe004384

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PADCTRL_DEBUG_SEL 0xfe004388

7.8.3.1 Pin MUX Registers

Table 7-127 PADCTRL_PIN_MUX_REG0

Bit(s)	R/W	Default	Description
31:28	R/W	0	gpioB_7_sel
27:24	R/W	0	gpioB_6_sel
23:20	R/W	0	gpioB_5_sel
19:16	R/W	0	gpioB_4_sel
15:12	R/W	0	gpioB_3_sel
11:8	R/W	0	gpioB_2_sel
7:4	R/W	0	gpioB_1_sel
3:0	R/W	0	gpioB_0_sel

Table 7-128 PADCTRL_PIN_MUX_REG1

Bit(s)	R/W	Default	Description
23:20	R/W	0	gpioB_13_sel
19:16	R/W	0	gpioB_12_sel
15:12	R/W	0	gpioB_11_sel
11:8	R/W	0	gpioB_10_sel
7:4	R/W	0	gpioB_9_sel
3:0	R/W	0	gpioB_8_sel

Table 7-129 PADCTRL_PIN_MUX_REG3

Bit(s)	R/W	Default	Description
31:28	R/W	0	gpioX_7_sel
27:24	R/W	0	gpioX_6_sel
23:20	R/W	0	gpioX_5_sel
19:16	R/W	0	gpioX_4_sel
15:12	R/W	0	gpioX_3_sel
11:8	R/W	0	gpioX_2_sel
7:4	R/W	0	gpioX_1_sel
3:0	R/W	0	gpioX_0_sel

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Table 7-130 PADCTRL_PIN_MUX_REG4

Bit(s)	R/W	Default	Description
31:28	R/W	0	gpioX_15_sel
27:24	R/W	0	gpioX_14_sel
23:20	R/W	0	gpioX_13_sel
19:16	R/W	0	gpioX_12_sel
15:12	R/W	0	gpioX_11_sel
11:8	R/W	0	gpioX_10_sel
7:4	R/W	0	gpioX_9_sel
3:0	R/W	0	gpioX_8_sel

Table 7-131 PADCTRL_PIN_MUX_REG5

Bit(s)	R/W	Default	Description
15:12	R/W	0	gpioX_19_sel
11:8	R/W	0	gpioX_18_sel
7:4	R/W	0	gpioX_17_sel
3:0	R/W	0	gpioX_16_sel

Table 7-132 PADCTRL_PIN_MUX_REG6

Bit(s)	R/W	Default	Description
31:28	R/W	0	gpioZ_7_sel
27:24	R/W	0	gpioZ_6_sel
23:20	R/W	0	gpioZ_5_sel
19:16	R/W	0	gpioZ_4_sel
15:12	R/W	0	gpioZ_3_sel
11:8	R/W	0	gpioZ_2_sel
7:4	R/W	0	gpioZ_1_sel
3:0	R/W	0	gpioZ_0_sel

Table 7-133 PADCTRL_PIN_MUX_REG7

Bit(s)	R/W	Default	Description
19:16	R/W	0	gpioZ_12_sel
15:12	R/W	0	gpioZ_11_sel
11:8	R/W	0	gpioZ_10_sel
7:4	R/W	0	gpioZ_9_sel
3:0	R/W	0	gpioZ_8_sel

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Table 7-134 PADCTRL_PIN_MUX_REG9

Bit(s)	R/W	Default	Description
31:28	R/W	0	gpioC_7_sel
27:24	R/W	0	gpioC_6_sel
23:20	R/W	2	gpioC_5_sel
19:16	R/W	2	gpioC_4_sel
15:12	R/W	0	gpioC_3_sel
11:8	R/W	0	gpioC_2_sel
7:4	R/W	2	gpioC_1_sel
3:0	R/W	2	gpioC_0_sel

Table 7-135 PADCTRL_PIN_MUX_REGB

Bit(s)	R/W	Default	Description
31:28	R/W	0	gpioH_7_sel
27:24	R/W	0	gpioH_6_sel
23:20	R/W	0	gpioH_5_sel
19:16	R/W	0	gpioH_4_sel
15:12	R/W	0	gpioH_3_sel
11:8	R/W	0	gpioH_2_sel
7:4	R/W	0	gpioH_1_sel
3:0	R/W	0	gpioH_0_sel

Table 7-136 PADCTRL_PIN_MUX_REGC

Bit(s)	R/W	Default	Description
15:12	R/W	0	gpioH_11_sel
11:8	R/W	0	gpioH_10_sel
7:4	R/W	0	gpioH_9_sel
3:0	R/W	0	gpioH_8_sel

Table 7-137 PADCTRL_PIN_MUX_REGG

Bit(s)	R/W	Default	Description
31:28	R/W	0	gpioD_7_sel
27:24	R/W	0	gpioD_6_sel
23:20	R/W	0	gpioD_5_sel
19:16	R/W	0	gpioD_4_sel

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Bit(s)	R/W	Default	Description
15:12	R/W	0	gpioD_3_sel
11:8	R/W	0	gpioD_2_sel
7:4	R/W	0	gpioD_1_sel
3:0	R/W	0	gpioD_0_sel

Table 7-138 PADCTRL_PIN_MUX_REGH

Bit(s)	R/W	Default	Description
15:12	R/W	0	gpioD_11_sel
11:8	R/W	0	gpioD_10_sel
7:4	R/W	0	gpioD_9_sel
3:0	R/W	0	gpioD_8_sel

Table 7-139 PADCTRL_PIN_MUX_REGI

Bit(s)	R/W	Default	Description
7:4	R/W	0	gpioE_1_sel
3:0	R/W	0	gpioE_0_sel

7.8.3.2 PADCTRL_GPIOx Registers

Table 7-140 PADCTRL_GPIOZ_I

Bit(s)	R/W	Default	Description
12:0	R	0	

Table 7-141 PADCTRL_GPIOZ_O

Bit(s)	R/W	Default	Description
12:0	R/W	0x1FFF	

Table 7-142 PADCTRL_GPIOZ_OEN

Bit(s)	R/W	Default	Description
12:0	R/W	0x1FFF	

Table 7-143 PADCTRL_GPIOZ_PULL_EN

Bit(s)	R/W	Default	Description
12:0	R/W	0x1FFF	

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Table 7-144 PADCTRL_GPIOZ_PULL_UP

Bit(s)	R/W	Default	Description
12:0	R/W	0x72B	

Table 7-145 PADCTRL_GPIOZ_DS

Bit(s)	R/W	Default	Description
25:0	R/W	0x2AA_AAAA	

Table 7-146 PADCTRL_GPIOZ_LOCK

Bit(s)	R/W	Default	Description
12:0	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 … can write 1 only

Table 7-147 PADCTRL_GPIOZ_PROT

Bit(s)	R/W	Default	Description
12:0	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 … can write 0 or 1

Table 7-148 PADCTRL_GPIOX_I

Bit(s)	R/W	Default	Description
19:0	R	0	

Table 7-149 PADCTRL_GPIOX_O

Bit(s)	R/W	Default	Description
19:0	R/W	0xF_FFFF	

Table 7-150 PADCTRL_GPIOX_OEN

Bit(s)	R/W	Default	Description
19:0	R/W	0x1_FFFF	

Table 7-151 PADCTRL_GPIOX_PULL_EN

Bit(s)	R/W	Default	Description
19:0	R/W	0x7_FFFF	

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Table 7-152 PADCTRL_GPIOX_PULL_UP

Bit(s)	R/W	Default	Description
19:0	R/W	0x5_FFBF	

Table 7-153 PADCTRL_GPIOX_DS

Bit(s)	R/W	Default	Description
31:0	R/W	0xAAAA_AAAA	

Table 7-154 PADCTRL_GPIOX_DS_EXT

Bit(s)	R/W	Default	Description
7:0	R/W	0xAA	GPIOX_19, GPIOX_18, GPIOX_17,GPIOX_16

Table 7-155 PADCTRL_GPIOX_LOCK

Bit(s)	R/W	Default	Description
19:0	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 … can write 1 only

Table 7-156 PADCTRL_GPIOX_PROT

Bit(s)	R/W	Default	Description
19:0	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 … can write 0 or 1

Table 7-157 PADCTRL_GPIOH_I

Bit(s)	R/W	Default	Description
11:0	R	0	

Table 7-158 PADCTRL_GPIOH_O

Bit(s)	R/W	Default	Description
11:0	R/W	0xFFF	

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Table 7-159 PADCTRL_GPIOH_OEN

Bit(s)	R/W	Default	Description
11:0	R/W	0xFFF	

Table 7-160 PADCTRL_GPIOH_PULL_EN

Bit(s)	R/W	Default	Description
11:0	R/W	0xFF0	

Table 7-161 PADCTRL_GPIOH_PULL_UP

Bit(s)	R/W	Default	Description
11:0	R/W	0x340	

Table 7-162 PADCTRL_GPIOH_DS

Bit(s)	R/W	Default	Description
23:0	R/W	0xAA_AAAA	

Table 7-163 PADCTRL_GPIOH_LOCK

Bit(s)	R/W	Default	Description
11:0	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 … can write 1 only

Table 7-164 PADCTRL_GPIOH_PROT

Bit(s)	R/W	Default	Description
11:0	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 … can write 0 or 1

Table 7-165 PADCTRL_GPIOD_I

Bit(s)	R/W	Default	Description
11:0	R	0	

Table 7-166 PADCTRL_GPIOD_O

Bit(s)	R/W	Default	Description
11:0	R/W	0xFFF	

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Table 7-167 PADCTRL_GPIOD_OEN

Bit(s)	R/W	Default	Description
11:0	R/W	0xFFF	

Table 7-168 PADCTRL_GPIOD_PULL_EN

Bit(s)	R/W	Default	Description
11:0	R/W	0xFFF	

Table 7-169 PADCTRL_GPIOD_PULL_UP

Bit(s)	R/W	Default	Description
11:0	R/W	0x52B	

Table 7-170 PADCTRL_GPIOD_DS

Bit(s)	R/W	Default	Description
23:0	R/W	0xAA_AAAA	

Table 7-171 PADCTRL_GPIOD_LOCK

Bit(s)	R/W	Default	Description
11:0	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 … can write 1 only

Table 7-172 PADCTRL_GPIOD_PROT

Bit(s)	R/W	Default	Description
11:	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 … can write 0 or 1

Table 7-173 PADCTRL_GPIOE_I

Bit(s)	R/W	Default	Description
1:0	R	0	

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Table 7-174 PADCTRL_GPIOE_O

Bit(s)	R/W	Default	Description
1:0	R/W	0x7	

Table 7-175 PADCTRL_GPIOE_OEN

Bit(s)	R/W	Default	Description
1:0	R/W	0x7	

Table 7-176 PADCTRL_GPIOE_PULL_EN

Bit(s)	R/W	Default	Description
1:0	R/W	0x0	

Table 7-177 PADCTRL_GPIOE_PULL_UP

Bit(s)	R/W	Default	Description
1:0	R/W	0x0	

Table 7-178 PADCTRL_GPIOE_DS

Bit(s)	R/W	Default	Description
3:0	R/W	0xA	

Table 7-179 PADCTRL_GPIOE_LOCK

Bit(s)	R/W	Default	Description
1:0	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 can write 1 only

Table 7-180 PADCTRL_GPIOE_PROT

Bit(s)	R/W	Default	Description
1:0	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 can write 0 or 1

Table 7-181 PADCTRL_GPIOC_I

Bit(s)	R/W	Default	Description
7:0	R	0	

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Table 7-182 PADCTRL_GPIOC_O

Bit(s)	R/W	Default	Description
7:0	R/W	0xFF	

Table 7-183 PADCTRL_GPIOC_OEN

Bit(s)	R/W	Default	Description
7:0	R/W	0xFF	

Table 7-184 PADCTRL_GPIOC_PULL_EN

Bit(s)	R/W	Default	Description
7:0	R/W	0x7F	

Table 7-185 PADCTRL_GPIOC_PULL_UP

Bit(s)	R/W	Default	Description
7:0	R/W	0x7F	

Table 7-186 PADCTRL_GPIOC_DS

Bit(s)	R/W	Default	Description
15:0	R/W	0xAAAA	

Table 7-187 PADCTRL_GPIOC_LOCK

Bit(s)	R/W	Default	Description
7:0	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 … can write 1 only

Table 7-188 PADCTRL_GPIOC_PROT

Bit(s)	R/W	Default	Description
7:0	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 … can write 0 or 1

Table 7-189 PADCTRL_GPIOB_I

Bit(s)	R/W	Default	Description
13:0	R	0	

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Table 7-190 PADCTRL_GPIOB_O

Bit(s)	R/W	Default	Description
13:0	R/W	0x3FFF	

Table 7-191 PADCTRL_GPIOB_OEN

Bit(s)	R/W	Default	Description
13:0	R/W	0x3FFF	

Table 7-192 PADCTRL_GPIOB_PULL_EN

Bit(s)	R/W	Default	Description
13:0	R/W	0x3FFF	

Table 7-193 PADCTRL_GPIOB_PULL_UP

Bit(s)	R/W	Default	Description
13:0	R/W	0x7FF	

Table 7-194 PADCTRL_GPIOB_DS

Bit(s)	R/W	Default	Description
27:0	R/W	0xAAA_AAAA	

Table 7-195 PADCTRL_GPIOB_LOCK

Bit(s)	R/W	Default	Description
13:0	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 … can write 1 only

Table 7-196 PADCTRL_GPIOB_PROT

Bit(s)	R/W	Default	Description
13:0	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 … can write 0 or 1

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7.8.3.3 PADCTRL_LOCK/PROT_PIN_MUX

Table 7-197 PADCTRL_LOCK/PROT_PIN_MUX_REG0

Lock and prot are two different register which can lock one pin_mux_sel.

The different is lock can write 1 only; prot can write 0 or 1;

Bit(s)	R/W	Default	Description
31	R/W	0	lock gpioX_7
…	R/W	0	…
24	R/W	0	lock gpioX_0
15	R/W	0	lock gpioB_15
…	R/W	0	…
0	R/W	0	lock gpioB_0

Table 7-198 PADCTRL_LOCK/PROT_PIN_MUX_REG1

Lock and prot are two different register which can lock one pin_mux_sel.

The different is lock can write 1 only; prot can write 0 or 1.

Bit(s)	R/W	Default	Description
28	R/W	0	lock gpioZ_12
…	R/W	0	…
16	R/W	0	lock gpioZ_0
11	R/W	0	lock gpioX_19
…	R/W	0	…
0	R/W	0	lock gpioX_8

Table 7-199 PADCTRL_LOCK/PROT_PIN_MUX_REG2

Lock and prot are two different register which can lock one pin_mux_sel.

The different is lock can write 1 only; prot can write 0 or 1.

Bit(s)	R/W	Default	Description
31	R/W	0	lock gpioH_7
…	R/W	0	…
24	R/W	0	lock gpioH_0
15	R/W	0	lock gpioC_7
…	R/W	0	…
8	R/W	0	lock gpioC_0

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Table 7-200 PADCTRL_LOCK/PROT_PIN_MUX_REG3

Lock and prot are two different register which can lock one pin_mux_sel.

The different is lock can write 1 only; prot can write 0 or 1;

Bit(s)	R/W	Default	Description
3	R/W	0	lock gpioH_11
…	R/W	0	…
0	R/W	0	lock gpioH_8

Table 7-201 PADCTRL_LOCK/PROT_PIN_MUX_REG4

Lock and prot are two different register which can lock one pin_mux_sel.

The different is lock can write 1 only; prot can write 0 or 1;

Bit(s)	R/W	Default	Description
17	R/W	0	lock gpioE_1
16	R/W	0	lock gpioE_0
11	R/W	0	lock gpioD_11
…	R/W	0	…
0	R/W	0	lock gpioD_0

7.8.3.4 PADCTRL Other Registers

Table 7-202 PADCTRL_WORLDSYNC_CTRL0

Bit(s)	R/W	Default	Description
7	R/W	0	world_sync_i enable
6:0	R/W	0	source select; from gpio src list

Table 7-203 PADCTRL_GPIO_MSR_CTRL0

Bit(s)	R/W	Default	Description
7	R/W	0	gpio_msr enable
6:0	R/W	0	source select; from gpio src list

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Table 7-204 PADCTRL_MISC_CTRL0

Bit(s)	R/W	Default	Description
1	R/W	0x0	1: select JTAG_TDI/TMS/TCK from PAD_JTAG_*_2
0	R/W	0x0	1: enable PWR_ON signal from PWR_CTRL to TEST_N; need set PADCTRL_TESTN_O to 1 first.

Table 7-205 PADCTRL_TESTN_I

Bit(s)	R/W	Default	Description
0	R	0	

Table 7-206 PADCTRL_TESTN_O

Bit(s)	R/W	Default	Description
0	R/W	0	

Table 7-207 PADCTRL_TESTN_OEN

Bit(s)	R/W	Default	Description
0	R/W	1	

Table 7-208 PADCTRL_TESTN_PULL_EN

Bit(s)	R/W	Default	Description
0	R/W	1	

Table 7-209 PADCTRL_TESTN_PULL_UP

Bit(s)	R/W	Default	Description
0	R/W	1	

Table 7-210 PADCTRL_TESTN_DS

Bit(s)	R/W	Default	Description
1:0	R/W	2	

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Table 7-211 PADCTRL_TESTN_LOCK

Bit(s)	R/W	Default	Description
0	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 … can write 1 only

Table 7-212 PADCTRL_TESTN_PROT

Bit(s)	R/W	Default	Description
0	R/W	0x0	each bit can lock one pad's oen/pullen/pullup/ds bit0 lock gpio*_0 bit1 lock gpio*_1 … can write 0 or 1

Table 7-213 PADCTRL_MUTE_CTRL

We can mute audio in by HW, the control register is write once.

And after configured, it can lock some PAD usage and detect pulse or level to mute audio in path.

These two register are sticky ,can reset by pad only.

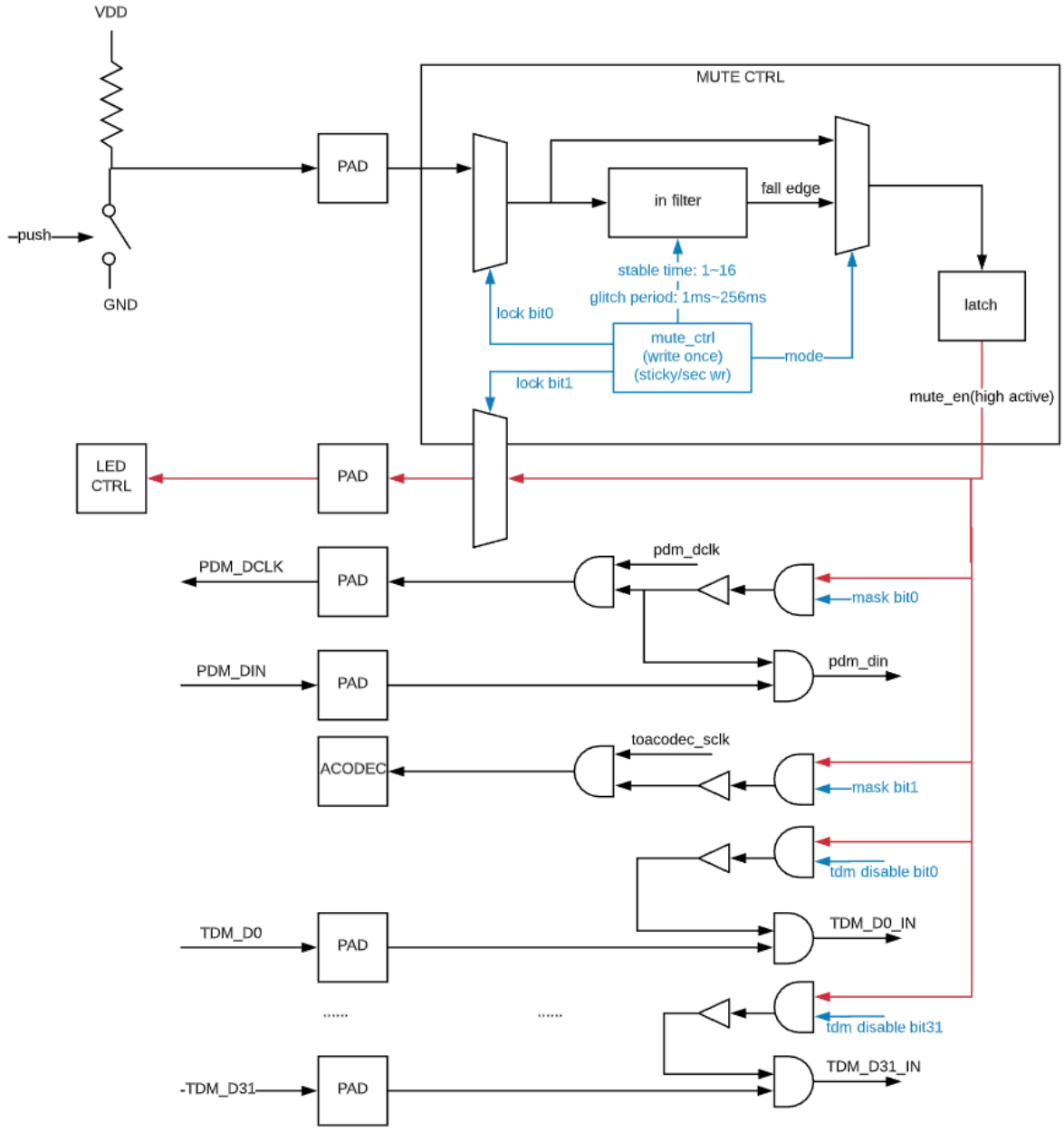
Notice: When write PADCTRL_MUTE_CTRL will lock both PADCTRL_MUTE_CTRL & PADCTRL_TDM_DISA, so must write PADCTRL_TDM_DISA first.

Bit(s)	R/W	Default	Description
31	R/W	0	lock_pinmux_key, if 1 will lock gpioD_3_sel as 5, input mute_key only
30	R/W	0	lock_pinmux_en, if 1 will lock gpioD_2_sel as 5, output mute_en only
29	R/W	0	mute_mode: 0: detect mute_key as level; 1: detect mute_key as pulse;
17:16	R/W	0	mute_mask[1:0]; bit1: mute acodec bit0: mute pdm;
11:8	R/W	0	filter_stable[3:0]; for captured data, if bit(stable+1)=1 and bit(stable to 0) are all 0, that's mean detected one pulse.
7:0	R/W	0	filter_period[7:0], unit is ms, will capture mute_key when cnt= period;

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Table 7-214 PADCTRL_MUTE_TDM_DISA

Bit(s)	R/W	Default	Description
7	R/W	0	mute TDM_D7 to 1
…	R/W	0	…
1	R/W	0	mute TDM_D1 to 1
0	R/W	0	mute TDM_D0 to 1



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Table 7-215 PADCTRL_DEBUG_SEL

Bit(s)	R/W	Default	Description
16	R/W	0x0	1: enable debug_in to eth_ debug_in;
3:0	R/W	0x0	debug out sel: 1:sel eth_debug_out; 2:sel ap trace;debug_o_ 17=trace_clk;debug_o_ 16=trace_ctrl;debug_o_ 15_0=trace_out; 6:sel acodec_debug_bus; else:debug out 20'd0;

7.9 Interrupt Control

7.9.1 Overview

Generic Interrupt Controller (GIC) is a centralized resource that supports and manages interrupts in a system. For more details about GIC, please refer to the ARM GIC Architecture Specification V2.0.

7.9.2 Interrupt Source

There are 256 interrupt sources in the chip. All of the interrupts are connected to the integrated GIC in Cortex-A35 while the AO-CPU see a sub-set of the interrupts. The control Bits of AO-CPU interrupt are listed in the following table.

A55 GIC Bit	Interrupt Source
255	ASSIST_MBOX3
254	ASSIST_MBOX2
253	ASSIST_MBOX1
252	ASSIST_MBOX0
251	MBOX_IRQ3
250	MBOX_IRQ2
249	MBOX_IRQ1
248	MBOX_IRQ0
247	IRQOUT3
246	IRQOUT2
245	IRQOUT1
244	IRQOUT0
243	FIQOUT3
242	FIQOUT2
241	FIQOUT1
240	FIQOUT0
239	

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A55 GIC Bit	Interrupt Source
238	L2FLUSHDONE
237	STANDBYWFIL2
236	PMUIRQ_3
235	PMUIRQ_2
234	PMUIRQ_1
233	PMUIRQ_0
232	ERRIRQ
231	CTIIRQ_OR
230	VCPUMNTIRQ_OR
229	COMMIRQ_OR
228	PMUIRQ_OR
227	COREINSTRRUN3
226	COREINSTRRUN2
225	COREINSTRRUN1
224	COREINSTRRUN0
223	
222	
221	DEMOD_IRQ
220	VPU_SEC
219	MUTE
218	
217	GE2D
216	CUSAD
215	RDMA_DONE
214	VID1_WR
213	VID0_WR
212	VDIN1_VSYNC
211	VDIN1_HSYNC
210	VDIN0_VSYNC
209	VDIN0_HSYNC
208	INT_VENC_VX1
207	LC_CURVE
206	VPU_CRASH
205	HTX_HDCP22
204	HDMI_TX
203	DI_PRE

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A55 GIC Bit	Interrupt Source
202	DI_POST
201	VIFF_EMPTY
200	VIU1_MAIL_AFBC
199	VIU1_WM
198	VIU1_DOLBY
197	VIU1_VSYNC
196	VIU1_HSYNC
195	VIU1_LINE
194	VIU2_VSYNC
193	VIU2_HSYNC
192	VIU2_LINE
191	STANDBYWFI_3
190	STANDBYWFI_2
189	STANDBYWFI_1
188	STANDBYWFI_0
187	
186	
185	
184	
183	SPICC0
182	SPIFC
181	SAR_ADC
180	CEC_B
179	CEC_A
178	SD_EMMC_C
177	SD_EMMC_B
176	SD_EMMC_A
175	NAND
174	SMARTCARD
173	
172	UART_E
171	UART_D
170	UART_C
169	UART_B
168	UART_A
167	USB_VBUSDIG

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A55 GIC Bit	Interrupt Source
166	S_I2C_A
165	M_I2C_F
164	M_I2C_E
163	M_I2C_D
162	M_I2C_C
161	M_I2C_B
160	M_I2C_A
159	
158	
157	
156	
155	DEMUX_DMA_IRQ
154	MALI_PP3
153	MALI_PPMMU2
152	MALI_PP2
151	MALI_PPMMU1
150	MALI_PP1
149	MALI_PPMMU0
148	MALI_PP0
147	MALI_PMU
146	MALI_PP
145	MALI_GPMMU
144	MALI_GP
143	
142	
141	
140	
139	
138	
137	
136	
135	
134	
133	SECTOP_1
132	SECTOP_0
131	USB2_DEV
130	

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A55 GIC Bit	Interrupt Source
129	USB_IDDIG
128	
127	HCODEC2DOS_31
126	HCODEC2DOS_30
125	HCODEC2DOS_29
124	HCODEC2DOS_28
123	HCODEC2DOS_27
122	HCODEC2DOS_26
121	HCODEC2DOS_25
120	HCODEC2DOS_4
119	HCODEC2DOS_23
118	HCODEC2DOS_22
117	HCODEC2DOS_21
116	HCODEC2DOS_20
115	HCODEC2DOS_19
114	HCODEC2DOS_18
113	HCODEC2DOS_17
112	HCODEC2DOS_16
111	HCODEC2DOS_15
110	HCODEC2DOS_14
109	HCODEC2DOS_13
108	HCODEC2DOS_12
107	HCODEC2DOS_11
106	HCODEC2DOS_10
105	HCODEC2DOS_9
104	HCODEC2DOS_8
103	HCODEC2DOS_7
102	HCODEC2DOS_6
101	HCODEC2DOS_5
100	HCODEC2DOS_4
99	HCODEC2DOS_3
98	HCODEC2DOS_2
97	HCODEC2DOS_1
96	HCODEC2DOS_0
95	

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A55 GIC Bit	Interrupt Source
94	
93	MBOX_SLOW2
92	MBOX_SLOW1
91	MBOX_SLOW0
90	
89	
88	
87	
86	
85	
84	
83	
82	
81	
80	
79	
78	DMC_MON
77	AUCPU_IRQ
76	ETH_LPI
75	ETH_PHY_OR
74	ETH_GMAC
73	ETH_LPI_INTR
72	ETH_PHY8
71	ETH_PHY7
70	ETH_PHY6
69	ETH_PHY5
68	ETH_PHY4
67	ETH_PHY3
66	ETH_PHY2
65	ETH_PHY1
64	ETH_PHY0
63	SEC_WATCHDOG
62	DMC
61	DMC_SEC
60	DMC_TEST
59	PWRCTRL_IRQ7

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A55 GIC Bit	Interrupt Source
58	PWRCTRL_IRQ6
57	PWRCTRL_IRQ5
56	PWRCTRL_IRQ4
55	PWRCTRL_IRQ3
54	PWRCTRL_IRQ2
53	PWRCTRL_IRQ1
52	PWRCTRL_IRQ0
51	AUDIO_EXCEPTION
50	DEMOD_DEMUX_IRQ
49	SP_MBOX1_IRQ
48	AUDIO_IRQ16
47	SP_MBOX0_IRQ
46	AUDIO_FRDDR_D
45	AUDIO_TODDR_D
44	AUDIO_VAD_FS
43	AUDIO_SPDIFIN_LB
42	AUDIO_FRHDMIRX
41	AUDIO_LOCKER
40	AUDIO_FRDDR_E
39	AUDIO_VAD_FLAG
38	AUDIO_FRDDR_C
37	AUDIO_FRDDR_B
36	AUDIO_FRDDR_A
35	AUDIO_SPDIFIN
34	AUDIO_TODDR_C
33	AUDIO_TODDR_B
32	AUDIO_TODDR_A
31	TS_DDR
30	TS_PLL
29	DMA_5
28	DMA_4
27	DMA_3
26	DMA_2
25	DMA_1
24	DMA_0

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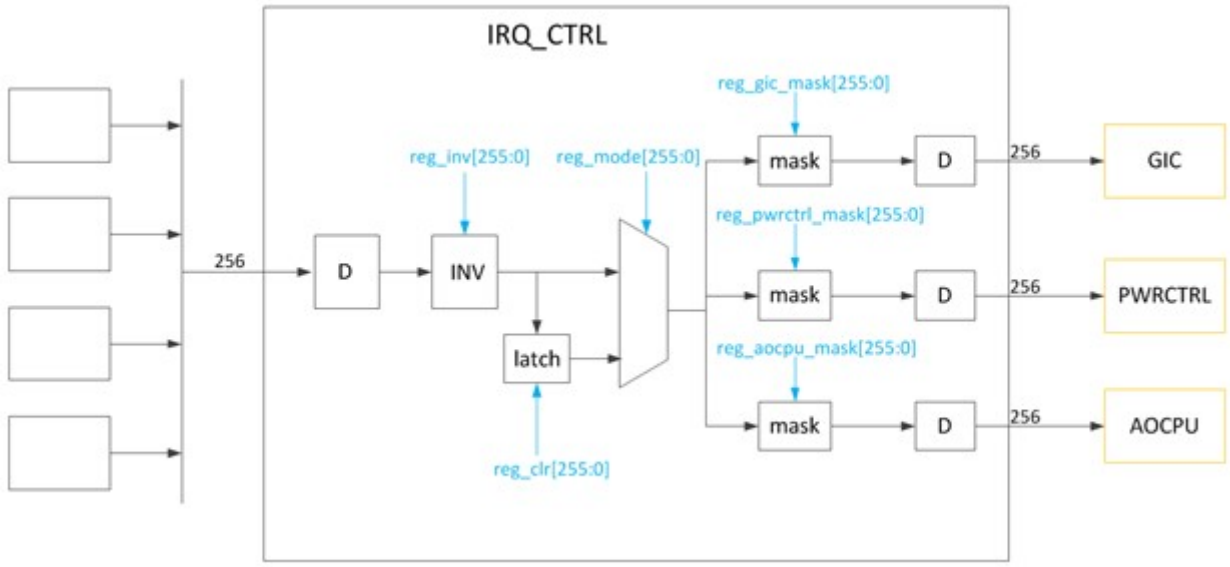
A55 GIC Bit	Interrupt Source
23	IR_TX
22	IR_RX
21	GPIO_11
20	GPIO_10
19	GPIO_09
18	GPIO_08
17	GPIO_07
16	GPIO_06
15	GPIO_05
14	GPIO_04
13	GPIO_03
12	GPIO_02
11	GPIO_01
10	GPIO_00
9	WATCHDOG
8	SEC_TIMERA
7	TIMERJ
6	TIMERI
5	TIMERH
4	TIMERG
3	TIMERD
2	TIMERC
1	TIMERB
0	TIMERA

7.9.3 Register Description

irq_ctrl include:

- collect all irq source together and sync it;
- add invert or latch if needed;
- send to different desitination after masked;
- all register are TEE W/R only except REG_CLR;
- all register are TEE W/R only except REG_CLR;

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For below registers the base address is 0xfe00a000.

Each register final address = BASE + address * 4.

The following lists describe the mapping between each IRQ_CTRL register and its address.

IRQCTRL_IRQ_INV0 0xfe00a000

IRQCTRL_IRQ_INV1 0xfe00a004

IRQCTRL_IRQ_INV2 0xfe00a008

IRQCTRL_IRQ_INV3 0xfe00a00c

IRQCTRL_IRQ_INV4 0xfe00a010

IRQCTRL_IRQ_INV5 0xfe00a014

IRQCTRL_IRQ_INV6 0xfe00a018

IRQCTRL_IRQ_INV7 0xfe00a01c

IRQCTRL_MASK0_GIC 0xfe00a040

IRQCTRL_MASK1_GIC 0xfe00a044

IRQCTRL_MASK2_GIC 0xfe00a048

IRQCTRL_MASK3_GIC 0xfe00a04c

IRQCTRL_MASK4_GIC 0xfe00a050

IRQCTRL_MASK5_GIC 0xfe00a054

IRQCTRL_MASK6_GIC 0xfe00a058

IRQCTRL_MASK7_GIC 0xfe00a05c

//`define IRQCTRL_MASK0_DSP 8'h20

//`define IRQCTRL_MASK1_DSP 8'h21

//`define IRQCTRL_MASK2_DSP 8'h22

//`define IRQCTRL_MASK3_DSP 8'h23

//`define IRQCTRL_MASK4_DSP 8'h24

//`define IRQCTRL_MASK5_DSP 8'h25

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```
//`define IRQCTRL_MASK6_DSP     8'h26
//`define IRQCTRL_MASK7_DSP     8'h27
IRQCTRL_MASK0_PWRCTRL          0xfe00a0c0
IRQCTRL_MASK1_PWRCTRL          0xfe00a0c4
IRQCTRL_MASK2_PWRCTRL          0xfe00a0c8
IRQCTRL_MASK3_PWRCTRL          0xfe00a0cc
IRQCTRL_MASK4_PWRCTRL          0xfe00a0d0
IRQCTRL_MASK5_PWRCTRL          0xfe00a0d4
IRQCTRL_MASK6_PWRCTRL          0xfe00a0d8
IRQCTRL_MASK7_PWRCTRL          0xfe00a0dc
IRQCTRL_MASK0_AOCPU            0xfe00a100
IRQCTRL_MASK1_AOCPU            0xfe00a104
IRQCTRL_MASK2_AOCPU            0xfe00a108
IRQCTRL_MASK3_AOCPU            0xfe00a10c
IRQCTRL_MASK4_AOCPU            0xfe00a110
IRQCTRL_MASK5_AOCPU            0xfe00a114
IRQCTRL_MASK6_AOCPU            0xfe00a118
IRQCTRL_MASK7_AOCPU            0xfe00a11c
IRQCTRL_IRQ_MODE0              0xfe00a140
IRQCTRL_IRQ_MODE1              0xfe00a144
IRQCTRL_IRQ_MODE2              0xfe00a148
IRQCTRL_IRQ_MODE3              0xfe00a14c
IRQCTRL_IRQ_MODE4              0xfe00a150
IRQCTRL_IRQ_MODE5              0xfe00a154
IRQCTRL_IRQ_MODE6              0xfe00a158
IRQCTRL_IRQ_MODE7              0xfe00a15c
IRQCTRL_IRQ_LATCH0             0xfe00a180
IRQCTRL_IRQ_LATCH1             0xfe00a184
IRQCTRL_IRQ_LATCH2             0xfe00a188
IRQCTRL_IRQ_LATCH3             0xfe00a18c
IRQCTRL_IRQ_LATCH4             0xfe00a190
IRQCTRL_IRQ_LATCH5             0xfe00a194
IRQCTRL_IRQ_LATCH6             0xfe00a198
IRQCTRL_IRQ_LATCH7             0xfe00a19c
IRQCTRL_IRQ_LATCH_CLR0         0xfe00a1c0
IRQCTRL_IRQ_LATCH_CLR1         0xfe00a1c4
IRQCTRL_IRQ_LATCH_CLR2         0xfe00a1c8
IRQCTRL_IRQ_LATCH_CLR3         0xfe00a1cc
```


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IRQCTRL_IRQ_LATCH_CLR4 0xfe00a1d0

IRQCTRL_IRQ_LATCH_CLR5 0xfe00a1d4

IRQCTRL_IRQ_LATCH_CLR6 0xfe00a1d8

IRQCTRL_IRQ_LATCH_CLR7 0xfe00a1dc

IRQCTRL_LOCK_BIT 0xfe00a200

IRQCTRL_PROT_BIT 0xfe00a204

Table 7-216 IRQCTRL_IRQ_INV0~7

Bits	R/W	Defaults	Description
255:0	R/W	0	if set 1, will invert irq level

Table 7-217 IRQCTRL_IRQ_MODE0~7

Bits	R/W	Defaults	Description
255:0	R/W	0	if set 1, will select latched irq; if set 0, will select original irq source;

Table 7-218 IRQCTRL_IRQ_LATCH0~7

Bits	R/W	Defaults	Description
255:0	R	0	the latched irq value

Table 7-219 IRQCTRL_IRQ_LATCH_CLR0~7

Bits	R/W	Defaults	Description
255:0	R/W	0	if set 1, will keep latched irq to low

Table 7-220 IRQCTRL_IRQ_MASK0~7_*

Bits	R/W	Defaults	Description
255:0	R/W	all 1	if set 0, will keep irq as low

Table 7-221 IRQCTRL_LOCK_BIT

Bits	R/W	Defaults	Description
6	R/W	0	write 1 once, if set 1 ,will lock all IRQ_MODE
4	R/W	0	write 1 once, if set 1 ,will lock all IRQ_MASK_ AOCPU
3	R/W	0	write 1 once, if set 1 ,will lock all IRQ_MASK_ PWRCTRL

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Bits	R/W	Defaults	Description
2	R/W	0	write 1 once, if set 1 ,will lock all IRQ_MASK_DSP
1	R/W	0	write 1 once, if set 1 ,will lock all IRQ_MASK_GIC
0	R/W	0	write 1 once, if set 1 ,will lock all IRQ_INV

Table 7-222 IRQCTRL_PROT_BIT

Bits	R/W	Defaults	Description
6	R/W	0	if set 1 ,will lock all IRQ_ MODE
4	R/W	0	if set 1 ,will lock all IRQ_ MASK_AOCPU
3	R/W	0	if set 1 ,will lock all IRQ_ MASK_PWRCTRL
2	R/W	0	if set 1 ,will lock all IRQ_ MASK_DSP
1	R/W	0	if set 1 ,will lock all IRQ_ MASK_GIC
0	R/W	0	if set 1 ,will lock all IRQ_ INV

7.10 Timer

7.10.1 Overview

The SOC contains 10 general purpose timers.

7.10.2 General-Purpose Timer

The SOC contains a number of general-purpose timers that can be used as general counters or interrupt generators. Each counter (except TIMER E) can be configured as a periodic counter (for generating periodic interrupts) or a simple count-down and stop counter. Additionally, the timers have a programmable count rate ranging from 1uS to 1mS. The table below outlines the general-purpose timers available in the chip.

Timer	Timebase Options	Counter size	Comment
Timer A	1uS, 10uS, 100uS	16-bits	The 16-bit counter allows the timer to generate interrupts as infrequent as every 65.535 Seconds
Timer B	1uS, 10uS, 100uS	16-bits	
Timer C	1uS, 10uS, 100uS	16-bits	
Timer D	1uS, 10uS, 100uS	16-bits	
Timer E	1uS, 10uS, 100uS	64-bits	Doesn’t generate an interrupt. This is a count up counter that counts from 0 to 0xFFFFFFFF. The counter can be written at any time to reset the value to 0.

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Timer	Timebase Options	Counter size	Comment
Timer F	1uS, 10uS, 100uS	16-bits	
Timer G	1uS, 10uS, 100uS	16-bits	
Timer H	1uS, 10uS, 100uS	16-bits	
Timer I	1uS, 10uS, 100uS	16-bits	
Timer J	1uS, 10uS, 100uS	16-bits	

7.10.3 Register Description

Each register final address = base address+ offset * 4

REGISTER_BASE_ADDR = 0xfe010000

The following lists describe the mapping between each timer register and its address.

SYSCTRL_TIMERA_CTRL 0xfe0100c0

SYSCTRL_TIMERA 0xfe0100c4

SYSCTRL_TIMERB_CTRL 0xfe0100c8

SYSCTRL_TIMERB 0xfe0100cc

SYSCTRL_TIMERC_CTRL 0xfe0100d0

SYSCTRL_TIMERC 0xfe0100d4

SYSCTRL_TIMERD_CTRL 0xfe0100d8

SYSCTRL_TIMERD 0xfe0100dc

SYSCTRL_SEC_TIMERA_CTRL 0xfe0100e0

SYSCTRL_SEC_TIMERA 0xfe0100e4

SYSCTRL_TIMERE_CTRL 0xfe0100e8

SYSCTRL_TIMERE 0xfe0100ec

SYSCTRL_TIMERE_HI 0xfe0100f0

SYSCTRL_TIMERF_CTRL 0xfe0100f4

SYSCTRL_TIMERF 0xfe0100f8

SYSCTRL_TIMERF_HI 0xfe0100fc

SYSCTRL_TIMERG_CTRL 0xfe010100

SYSCTRL_TIMERG 0xfe010104

SYSCTRL_TIMERH_CTRL 0xfe010108

SYSCTRL_TIMERH 0xfe01010c

SYSCTRL_TIMERI_CTRL 0xfe010110

SYSCTRL_TIMERI 0xfe010114

SYSCTRL_TIMERJ_CTRL 0xfe010118

SYSCTRL_TIMERJ 0xfe01011c

SYSCTRL_SEC_TIMERE_CTRL 0xfe010120

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SYSCTRL_SEC_TIMERE 0xfe010124

SYSCTRL_SEC_TIMERE_HI 0xfe010128

SYSCTRL_TIMER90K 0xfe01015c

SYSCTRL_HPG_TIMER 0xfe010164

Table 7-223 SYSCTRL_TIMERA/B/C/D/G/H/I/J_CTRL

Bit(s)	R/W	Default	Description
7	R/W	1	timer en
6	R/W	1	timer mode: 0: generate irq once; 1: generate irq periodic;
1:0	R/W	0	clk_sel: 0: cts_sys_clk; 1:1us; 2:10us; 3:100us

Table 7-224 SYSCTRL_TIMERA/B/C/D/G/H/I/J

Bit(s)	R/W	Default	Description
31:16	R	0	ttimer threshold
15:0	R/W	0	write: clean timer count; set timer threshold. irq will generate when timer count equal to threshold read: timer count value

Table 7-225 SYSCTRL_SEC_TIMERA_CTRL

Bit(s)	R/W	Default	Description
7	R/W	1	timer en
6	R/W	1	timer mode: 0: generate irq once; 1: generate irq periodic;
1:0	R/W	0	clk_sel: 0: cts_sys_clk; 1:1us; 2:10us; 3:100us

Table 7-226 SYSCTRL_SEC_TIMERA

Bit(s)	R/W	Default	Description
31:16	R	0	timer threshold
15:0	R/W	0	write: clean timer count; set timer threshold. irq will generate when timer count equal to threshold read: timer count value

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Table 7-227 SYSCTRL_TIMERE/F_CTRL

Bit(s)	R/W	Default	Description
7	R/W	1	timer en
1:0	R/W	1	clk_sel: 0: cts_sys_clk; 1:1us; 2:10us; 3:100us

Table 7-228 SYSCTRL_TIMERE/F

Bit(s)	R/W	Default	Description
31:0	R/W	0	write: clean timer count; read: update timer count[63:32] to TIMER_HI timer count[31:0]

Table 7-229 SYSCTRL_TIMERE/F_HI

Bit(s)	R/W	Default	Description
31:0	R	0	timer count[63:32]

Table 7-230 SYSCTRL_SEC_TIMERE_CTRL

Bit(s)	R/W	Default	Description
7	R/W	1	timer en
1:0	R/W	1	clk_sel: 0: cts_sys_clk; 1:1us; 2:10us; 3:100us

Table 7-231 SYSCTRL_SEC_TIMERE

Bit(s)	R/W	Default	Description
31:0	R/W	0	write: clean timer count; read: update timer count[63:32] to TIMER_HI timer count[31:0]

Table 7-232 SYSCTRL_SEC_TIMERE_HI

Bit(s)	R/W	Default	Description
31:0	R	0	timer count[63:32]

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Table 7-233 SYSCTRL_TIMER90K

Bit(s)	R/W	Default	Description
15:0	R/W	0x384	90khz timer divider

Table 7-234 SYSCTRL_HPG_TIMER

Bit(s)	R/W	Default	Description
15:0	R/W	0x0	generate h2tmr_irq if timer_cnt equal to HPG_TIMER; the timer_cnt will increment by 90khz timer; the timer_cnt will clear when generated h2tmr_irq;

7.11 Crypto

7.11.1 Overview

The crypto engine is one encrypt/decrypt function accelerator. Crypto engine supports 2 different modes, i.e. SCP (System Control Processor) secure and SCP non secure. The crypto engine has special internal DMA controller to transfer data.

It has the following features.

- Trustzone based Trusted Execution Environment (TEE)
- Secured boot, encrypted OTP, encrypted DRAM with memory integrity checker, hardware key ladder and internal control buses and storage
- Separated secure/non-secure Entropy true RNG
- Pre-region/ID memory security control and electric fence
- Hardware based Trusted Video Path (TVP) , video watermarking and secured contents (needs SecureOS software)
- Secured IO and secured clock

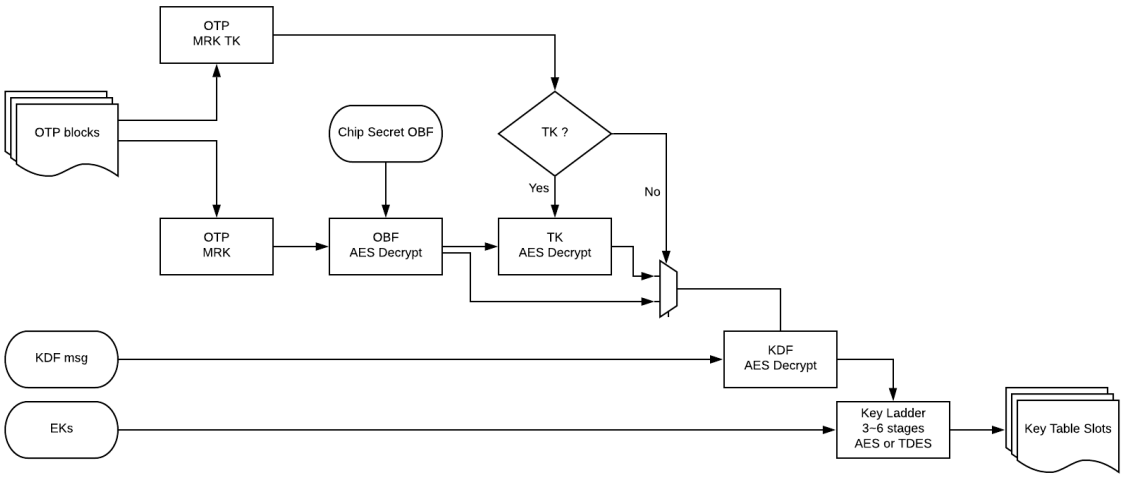
7.11.2 Key Ladder

The Key Ladder is a series of TDES / AES crypto processes that iterates on different user supplied and OTP keys. The key ladder module uses a single AES / TDES crypto module and iterates by using internal storage to hold temporary states.

The key ladder flow figure is shown below.

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Figure 7-16 Key Ladder Flow



The key ladder supports MKL and ETSI modes.

7.11.3 CTR_DRBG

CTR_DRBG contains two main modules, True Random Number Generator (TRNG) and Deterministic Random Number Generator (DRNG).

- True Random Number Generator (TRNG): is realized by using metastability and jitter for random bit generation based on four free running ring oscillator
- Deterministic Random Number Generator (DRNG): which has 32-bit random number generator, is mainly designed to increase the throughput and do post-processing of the Digital TRNG, which will need hundreds cycles to collect entropy.

It supports health test, which contains two functions: repetition count test and adaptive proportion test.

7.11.4 EFUSE

Synopsys Design Ware OTP NVM IP, Previous Kilopass OTP, is selected as OTP IP for this project.

TSMC 12FFC 1.8V 32Kbits

Model: XPM KPTS12FFC32-R08W01

Program x1 bit

Read x8 bits

Internal charge pump, support field programming

32 Kbits OTP is divided into 256 blocks, each block has 128 bits.

The blocks are labeled from 0 to 255.

The bits in each block are labeled from 0 to 127.

OTP controller takes job from users, there are 4 types of tasks.

- Sandwich Read
- Check
- Write
- Test

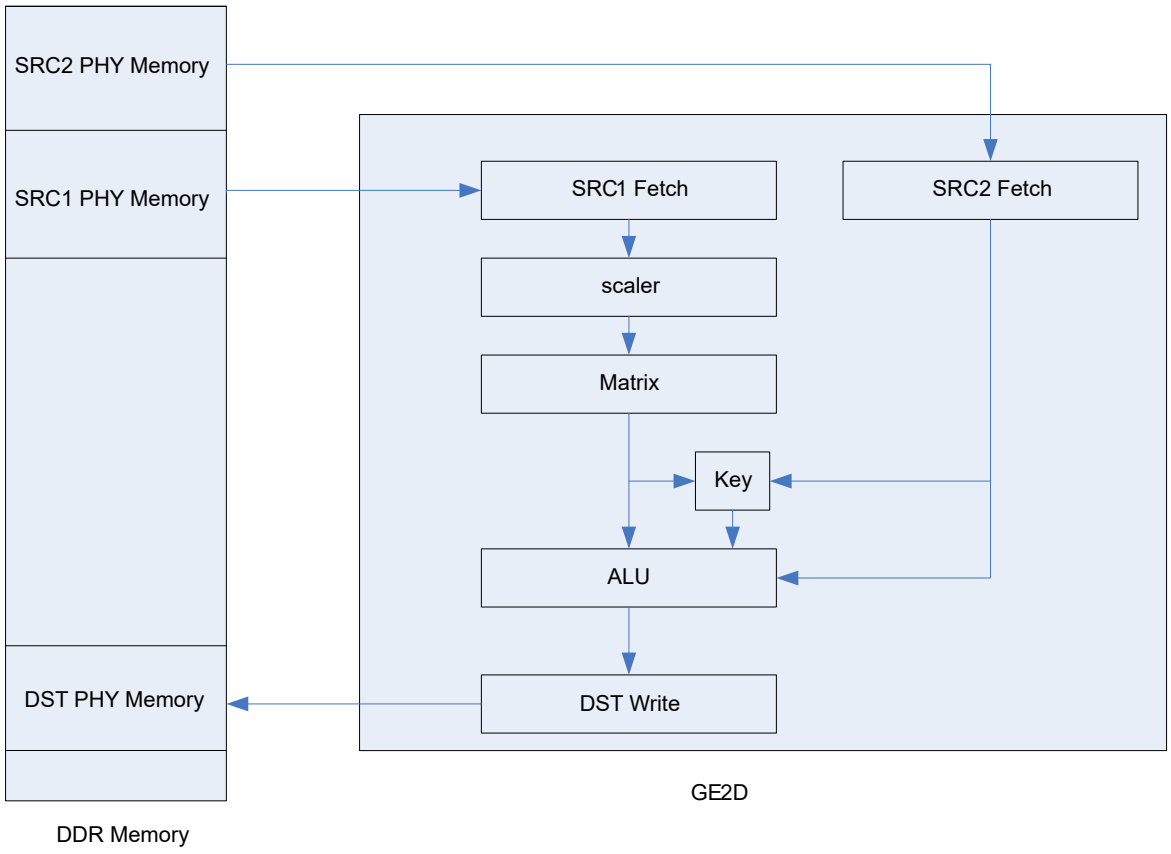
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8 GE2D

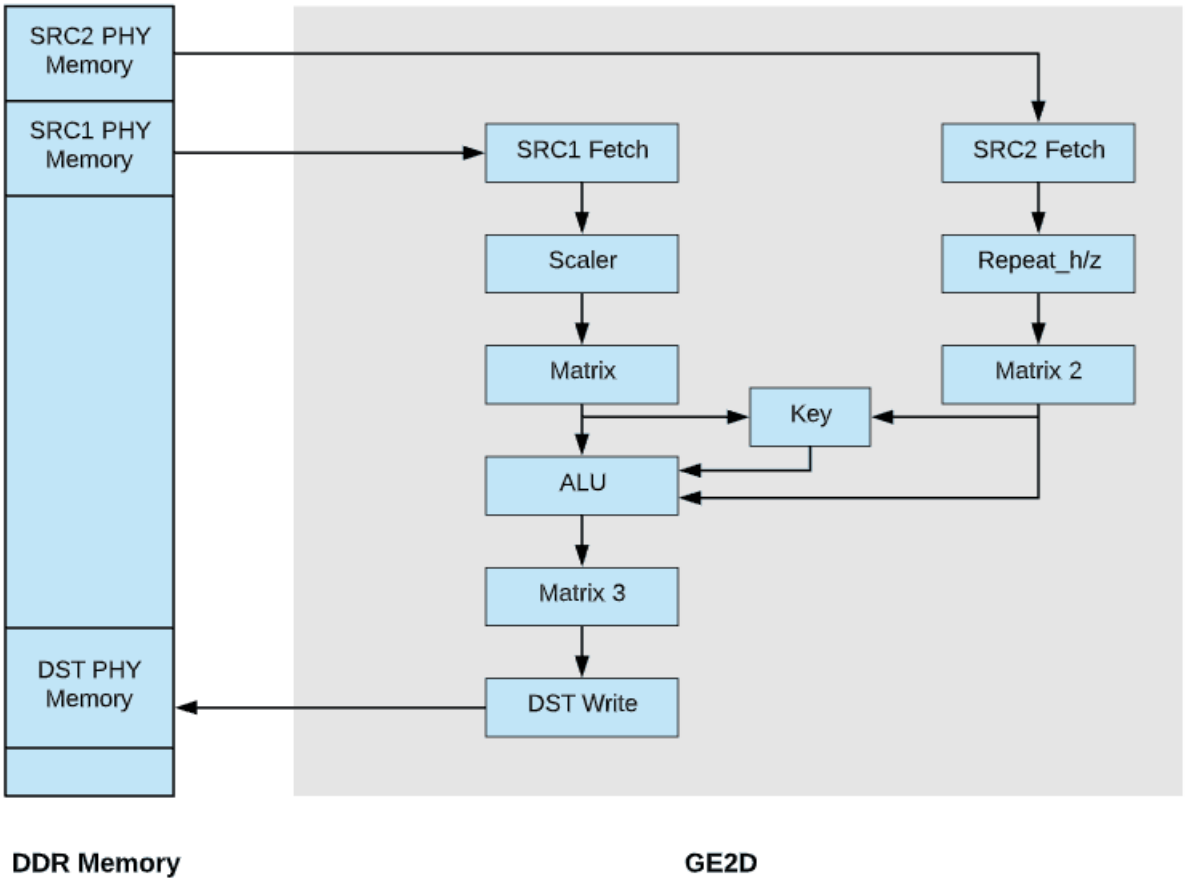
8.1 Overview

The basic structure of GE2D is shown in figure below.

Figure 8-1 GE2D Structure



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8.2 Register Description

Table 8-1 GE2D_GEN_CTRL0 0x8A0

Bit(s)	R/W	Default	Description
31	R/W	0	dst_bytemask_only: Applicable only if dst_bitmask_en=1.
30	R/W	0	dst_bitmask_en: destination bitmask enable. 0: disable; 1: enable.
29	R/W	0	src2_key_en: source2 key enable. 0: disable; 1: enable.
28	R/W	0	src2_key_mode: source2 key mode. 0: mask data when match; 1: mask data when unmatch.
27	R/W	0	src1_key_en: source1 key enable. 0: disable; 1: enable.
26	R/W	0	src1_key_mode: source1 key mode. 0: mask data when match; 1: mask data when unmatch.
25-24	R/W	0	dst1_8b_mode_sel: Destination 1's 8-bit mode component selection. 0: Select Y or R; 1: Select Cb or G; 2: Select Cr or B; 3: Select Alpha.

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Bit(s)	R/W	Default	Description
23	R/W	0	dst_clip_mode: 0: Write inside clip window; 1: Write outside clip window.
22-17	R	0	Unused
16-15	R/W	0	src2_8b_mode_sel: Applicable only when src2_format=0, define the property of the 8-bit output data. 0: The 8-bit output data is for Y or R; 1: The 8-bit output data is for Cb or G; 2: The 8-bit output data is for Cr or B; 3: The 8-bit output data is for Alpha.
14	R/W	0	src2_fill_mode: When the display window is outside the boundary of the clipping window, this field defines how to fill the area outside the clipping window. 0: Fill with the pixels at the boundary of the clipping window; 1: Fill with the default color defined by register GE2D_SRC2_DEF_COLOR.
13-12	R/W	0	src2_pic_struct: Define how source2 reads the picture stored in DDR memory. 0: Read all lines; 1: Reserved; 2: Read even lines only; 3: Read odd lines only.
11	R/W	0	src2_X_yc_ratio: Source2 x direction yc ratio. 0: 1:1; 1: 2:1.
9-7	R	0	Unused
6-5	R/W	0	src1_8b_mode_sel: Applicable only when src1_sep_en =0, src1_format=0 and src1_lut_en=0, define the property of the 8-bit output data. 0: the 8-bit output data is for Y or R; 1: the 8-bit output data is for Cb or G; 2: the 8-bit output data is for Cr or B; 3: the 8-bit output data is for Alpha.
4	R/W	0	src1_fill_mode: When the display window is outside the boundary of the clipping window, this field defines how to fill the area outside the clipping window. 0: Fill with the pixels at the boundary of the clipping window; 1: Fill with the default color defined by register GE2D_SRC1_DEF_COLOR.
3	R/W	0	src1_lut_en: Applicable only when src1_sep_en =0 and src1_format= 0, define whether to enable 8-bit input data to look up a 32-bit pixel for output. 0: Disable; 1: Enable.
2-1	R/W	0	src1_pic_struct: Define how source1 reads the picture stored in DDR memory. 0: Read all lines; 1: Reserved; 2: Read even lines only; 3: Read odd lines only.

Table 8-2 GE2D_GEN_CTRL1 0x8A1

Bit(s)	R/W	Default	Description
31	R/W	0	soft_rst: If true, reset GE2D.
30	R/W	0	dst write response counter reset
29	R/W	0	disable adding dst write response count to busy bit
28-27	R	0	Unused
26	R/W	0	Color_conversion_mode[1] in alu. Mode[1:0]

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Bit(s)	R/W	Default	Description
			3 : color_out = color; 2 : color_out = (color != 255) ? color : color + 1; 1 : color_out = (color < 128) ? color : color + 1; 0 : color_out = (color == 0) ? color : color + 1.
25-24	R/W	0	interrupt_ctrl: If bit[0] true, generate interrupt when one command done; if bit[1] true, generate interrupt when ge2d change from busy to not busy.
23-22	R/W	0x3	src2_burst_size_ctrl: Source2 DDR request burst size control. (Note: data to source2 are stored together in one DDR memory block.) 0: Burst size = 24 x 64-bit; 1: Burst size = 32 x 64-bit; 2: Burst size = 48 x 64-bit; 3: Burst size = 64 x 64-bit.
21-16	R/W	0x3F	src1_burst_size_ctrl: Source1 DDR request burst size control. Bit[21:20] control Y burst size, bit[19:18] control Cb burst size, bit[17:16] control Cr burst size. Each 2-bit is decoded as below: 0: Burst size = 24 x 64-bit; 1: Burst size = 32 x 64-bit; 2: Burst size = 48 x 64-bit; 3: Burst size = 64 x 64-bit.
15-14	R/W	0	dst1_pic_struct: Define how destination 1 write the picture to DDR memory. 0: Write all lines (whole frame); 1: Reserved; 2: Write even lines only (top); 3: Write odd lines only (bottom).
13-12	R/W	0	src_rd_ctrl: Bit[13] if true, force read src1, bit[12] if true, force read src2.
11	R/W	0	dst2_urgent_en: Destination 2 DDR request urgent enable.
10	R/W	0	src1_urgent_en: Source1 DDR request urgent enable.
9	R/W	0	src2_urgent_en: Source2 DDR request urgent enable.
8	R/W	0	dst1_urgent_en: Destination 1 DDR request urgent enable.
7-0	R/W	0	src1_gb_alpha: Source1 global alpha.

Table 8-3 GE2D_GEN_CTRL2 0x8A2

Bit(s)	R/W	Default	Description
31	R/W	0	alpha_conversion_mode[0] in alu. Mode[1:0]: 2,3 : alpha_out = (alpha!=255) ? alpha : alpha + 1; 1 : alpha_out = (alpha < 128) ? alpha : alpha + 1; 0 : alpha_out = (alpha == 0) ? alpha : alpha + 1.
30	R/W	0	Color_conversion_mode[0] in alu. Mode[1:0] 3 : color_out = color; 2 : color_out = (color != 255) ? color : color + 1; 1 : color_out = (color < 128) ? color : color + 1; 0 : color_out = (color == 0) ? color : color + 1.
29	R/W	0	src1_gb_alpha_en in alu. As = src1_gb_alpha_en ? Asr * Ag: Asr
28	R/W	0	dst1_COLOR_round_MODE. 1 = Truncate the full bit color components to required output bit width; 0 = Round (+ 0.5) the full bit color components to required output bit width.
27	R/W	0	src2_COLOR_EXPAND_MODE.

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Bit(s)	R/W	Default	Description
			1 = Expand the color components to 8-bit by padding LSBs with MSBs. E.g. If the input is 5'b11000, the output is expanded to 8'b11000110; 0 = Expand the color components to 8-bit by padding LSBs with 0.
26	R/W	0	src2_ALPHA_EXPAND_MODE. 1 = Expand alpha value to 8-bit by padding LSBs with MSBs. E.g. If the input is 5'b11000, the output is expanded to 8'b11000110; 0 = If input alpha value is all 1, then expand the value to 8-bit by padding LSBs with 1; otherwise, pad LSBs with 0.
25	R/W	0	src1_COLOR_EXPAND_MODE. 1 = Expand the color components to 8-bit by padding LSBs with MSBs. E.g. If the input is 5'b11000, the output is expanded to 8'b11000110; 0 = Expand the color components to 8-bit by padding LSBs with 0.
24	R/W	0	src1_ALPHA_EXPAND_MODE. 1 = Expand alpha value to 8-bit by padding LSBs with MSBs. E.g. If the input is 5'b11000, the output is expanded to 8'b11000110; 0 = If input alpha value is all 1, then expand the value to 8-bit by padding LSBs with 1; otherwise, pad LSBs with 0.
23	R/W	0	dst_little_endian: define the endianess of SRC2 input data. 1 = Little endian; 0 = Big endian.
22-19	R/W	0	dst1_color_map: Applicable to 16-bit, 24-bit and 32-bit pixel, defines the bit-field allocation of the pixel data. For whether to truncate or round full 8-bit to output, refer to ge2d_gen_ctrl2.dst1_color_round_mode. For 16-bit mode (dst1_format=1): 0 = Unused; 1 = 6:5:5 format. Bit[15:10] is Y[7:2] or R[7:2], bit[9:5] is Cb[7:3] or G[7:3], bit[4:0] is Cr[7:3] or B[7:3]; 2 = 8:4:4 format. Bit[15:8] is Y or R, bit[7:4] is Cb[7:4] or G[7:4], bit[3:0] is Cr[7:4] or B[7:4]]; 3 = 6:4:4:2 format. Bit[15:10] is Y[7:2] or R[7:2], bit[9:6] is Cb[7:4] or G[7:4], bit [5:2] is Cr[7:4] or B[7:4], bit[1:0] is Alpha[7:6]; 4 = 4:4:4:4 format. Bit[15:12] is Y[7:4] or R[7:4], bit[11:8] is Cb[7:4] or G[7:4], bit [7:4] is Cr[7:4] or B[7:4], bit[3:0] is Alpha[7:4]; 5 = 5:6:5 format. Bit[15:11] is Y[7:3] or R[7:3], bit[10:5] is Cb[7:2] or G[7:2], bit [4:0] is Cr[7:3] or B[7:3]; 6 = 4:4:4:4 format. Bit[15:12] is Alpha[7:4], bit[11:8] is Y[7:4] or R[7:4], bit[7:4] is Cb[7:4] or G[7:4], bit[3:0] is Cr[7:4] or B[7:4]; 7 = 1:5:5:5 format. Bit[15] is Alpha[7], bit[14:10] is Y[7:3] or R[7:3], bit[9:5] is Cb [7:3] or G[7:3], bit[4:0] is Cr[7:3] or B[7:3]; 8 = 4:6:4:2 format. Bit[15:12] is Y[7:4] or R[7:4], bit[11:6] is Cb[7:2] or G[7:2], bit [5:2] is Cr[7:4] or B[7:4], bit[1:0] is Alpha[1:0]. 9 = CbCr format. Bit[15:8] is Cb, bit[7:0] is Cr; 10 = CrCb format. Bit[15:8] is Cr, bit[7:0] is Cb. For 24-bit mode (dst1_format=2): 0 = RGB 8:8:8 mode. Bit[23:16] is Y or R, bit[15:8] is Cb or G, bit[7:0] is Cr or B; 1 = RGBA 5:6:5:8 mode. Bit[23:19] is Y[7:3] or R[7:3], bit[18:13] is Cb[7:2] or G [7:2], bit[12:8] is Cr[7:3] or B[7:3], bit[7:0] is Alpha; 2 = ARGB 8:5:6:5 mode. Bit[23:16] is Alpha, bit[15:11] is Y[7:3] or R[7:3], bit [10:5] is Cb[7:2] or G[7:2], bit[4:0] is Cr[7:3] or B[7:3]; 3 = RGBA 6:6:6:6 mode. Bit[23:18] is Y[7:2] or R[7:2], bit[17:12] is Cb[7:2] or G [7:2], bit[11:6] is Cr[7:2] or B[7:2], bit[5:0] is Alpha[7:2]; 4 = ARGB 6:6:6:6 mode. Bit[23:18] is Alpha[7:2];, bit[17:12] is Y[7:2] or R[7:2], bit[11:6] is Cb[7:2] or G[7:2], bit[5:0] is Cr[7:2] or B[7:2]; 5 = BGR 8:8:8 mode. Bit[23:16] is Cr or B, bit[15:8] is Cb or G, bit[7:0] is Y or R. For 32-bit mode (dst1_format=3): 0 = RGBA 8:8:8:8 format. Bit[31:24] is Y or R, bit[23:16] is Cb or G; bit[15:8] is Cr or B; bit[7:0] is Alpha; 1 = ARGB 8:8:8:8 format. Bit[31:24] is Alpha, bit[23:16] is Y or R; bit[15:8] is Cb or G; bit[7:0] is Cr or B;

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Bit(s)	R/W	Default	Description
			2 = ABGR 8:8:8:8 format. Bit[31:24] is Alpha, bit[23:16] is Cr or B; bit[15:8] is Cb or G; bit[7:0] is Y or R; 3 = BGRA 8:8:8:8 format. Bit[31:24] is Cr or B, bit[23:16] is Cb or G; bit[15:8] is Y or R; bit[7:0] is Alpha.
18	R/W	0	ALU_MULT_MODE: 1: mult result rounding else truncation
17-16	R/W	0	dst1_format: define output pixel byte-width. 0: Output pixel is 1-byte (8-bit) color component; 1: Output pixel is 2-byte (16-bit), refer to GE2D_GEN_CTRL2.dst1_COLOR_map for further pixel color mapping; 2: Output pixel is 3-byte (24-bit), refer to GE2D_GEN_CTRL2.dst1_COLOR_MAP for further pixel color mapping; 3: Output pixel is 4-byte (32-bit), refer to GE2D_GEN_CTRL2.dst1_COLOR_MAP for further pixel color mapping.
15	R/W	0	src2_little_endian: define the endianess of SRC2 input data. 1 = Little endian; 0 = Big endian.
14-11	R/W	0	src2_color_map: Applicable to 16-bit, 24-bit and 32-bit pixel, defines the bit-field allocation of the pixel data. For expanding the bit-fields to full 8-bit, refer to ge2d_gen_ctrl2.src2_color_expand_mode and ge2d_gen_ctrl2.src2_alpha_expand_mode. For 16-bit mode (src2_format=1): 0 = Unused; 1 = 6:5:5 format. Bit[15:10] is Y[7:2] or R[7:2], bit[9:5] is Cb[7:3] or G[7:3], bit[4:0] is Cr[7:3] or B[7:3], for Alpha value refer to src2_def_color_alpha 0x8af[7:0]; 2 = 8:4:4 format. Bit[15:8] is Y or R, bit[7:4] is Cb[7:4] or G[7:4], bit[3:0] is Cr[7:4] or B[7:4]], for Alpha value refer to src2_def_color_alpha 0x8af[7:0]; 3 = 6:4:4:2 format. Bit[15:10] is Y[7:2] or R[7:2], bit[9:6] is Cb[7:4] or G[7:4], bit [5:2] is Cr[7:4] or B[7:4], bit[1:0] is Alpha[7:6]; 4 = 4:4:4:4 format. Bit[15:12] is Y[7:4] or R[7:4], bit[11:8] is Cb[7:4] or G[7:4], bit [7:4] is Cr[7:4] or B[7:4], bit[3:0] is Alpha[7:4]; 5 = 5:6:5 format. Bit[15:11] is Y[7:3] or R[7:3], bit[10:5] is Cb[7:2] or G[7:2], bit [4:0] is Cr[7:3] or B[7:3], for Alpha value refer to src2_def_color_alpha 0x8af [7:0]; 6 = 4:4:4:4 format. Bit[15:12] is Alpha[7:4], bit[11:8] is Y[7:4] or R[7:4], bit[7:4] is Cb[7:4] or G[7:4], bit[3:0] is Cr[7:4] or B[7:4]; 7 = 1:5:5:5 format. Bit[15] is Alpha[7], bit[14:10] is Y[7:3] or R[7:3], bit[9:5] is Cb [7:3] or G[7:3], bit[4:0] is Cr[7:3] or B[7:3]; 8 = 4:6:4:2 format. Bit[15:12] is Y[7:4] or R[7:4], bit[11:6] is Cb[7:2] or G[7:2], bit [5:2] is Cr[7:4] or B[7:4], bit[1:0] is Alpha[1:0]. For 24-bit mode (src2_format=2): 0 = RGB 8:8:8 mode. Bit[23:16] is Y or R, bit[15:8] is Cb or G, bit[7:0] is Cr or B, for Alpha value refer to src2_def_color_alpha 0x8af[7:0]; 1 = RGBA 5:6:5:8 mode. Bit[23:19] is Y[7:3] or R[7:3], bit[18:13] is Cb[7:2] or G [7:2], bit[12:8] is Cr[7:3] or B[7:3], bit[7:0] is Alpha; 2 = ARGB 8:5:6:5 mode. Bit[23:16] is Alpha, bit[15:11] is Y[7:3] or R[7:3], bit [10:5] is Cb[7:2] or G[7:2], bit[4:0] is Cr[7:3] or B[7:3]; 3 = RGBA 6:6:6:6 mode. Bit[23:18] is Y[7:2] or R[7:2], bit[17:12] is Cb[7:2] or G [7:2], bit[11:6] is Cr[7:2] or B[7:2], bit[5:0] is Alpha[7:2]; 4 = ARGB 6:6:6:6 mode. Bit[23:18] is Alpha[7:2];, bit[17:12] is Y[7:2] or R[7:2], bit[11:6] is Cb[7:2] or G[7:2], bit[5:0] is Cr[7:2] or B[7:2]; 5 = BGR 8:8:8 mode. Bit[23:16] is Cr or B, bit[15:8] is Cb or G, bit[7:0] is Y or R, for Alpha value refer to src2_def_color_alpha 0x8af[7:0]. For 32-bit mode (src2_format=3): 0 = RGBA 8:8:8:8 format. Bit[31:24] is Y or R, bit[23:16] is Cb or G; bit[15:8] is Cr or B; bit[7:0] is Alpha; 1 = ARGB 8:8:8:8 format. Bit[31:24] is Alpha, bit[23:16] is Y or R; bit[15:8] is Cb or G; bit[7:0] is Cr or B; 2 = ABGR 8:8:8:8 format. Bit[31:24] is Alpha, bit[23:16] is Cr or B; bit[15:8] is Cb or G; bit[7:0] is Y or R;

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Bit(s)	R/W	Default	Description
			3 = BGRA 8:8:8:8 format. Bit[31:24] is Cr or B, bit[23:16] is Cb or G; bit[15:8] is Y or R; bit[7:0] is Alpha.
10	R/W	0	alpha_conversion_mode[1] in alu. Mode[1:0]: 2,3 : alpha_out = (alpha!=255) ? alpha : alpha + 1; 1 : alpha_out = (alpha < 128) ? alpha : alpha + 1; 0 : alpha_out = (alpha == 0) ? alpha : alpha + 1.
9-8	R/W	0	src2_format: define input pixel byte-width. 0: Input pixel is 1-byte (8-bit) color component; 1: Input pixel is 2-byte (16-bit), refer to GE2D_GEN_CTRL2.SRC2_COLOR_MAP for further pixel color mapping; 2: Input pixel is 3-byte (24-bit), refer to GE2D_GEN_CTRL2.SRC2_COLOR_MAP for further pixel color mapping; 3: Input pixel is 4-byte (32-bit), refer to GE2D_GEN_CTRL2.SRC2_COLOR_MAP for further pixel color mapping.
7	R/W	0	src1_little_endian: define the endianess of SRC1 input data. 1 = Little endian; 0 = Big endian.
6-3	R/W	0	src1_color_map: Note: If SRC1_DEEPCOLOR=0, the SRC1_COLOR_MAP's definitions is as below. If SRC1_DEEPCOLOR=1, please refer to SRC1_DEEPCOLOR entry for new meaning. Applicable to 16-bit, 24-bit and 32-bit pixel, defines the bit-field allocation of the pixel data. For expanding the bit-fields to full 8-bit, refer to ge2d_gen_ctrl2.src1_color_expand_mode and ge2d_gen_ctrl2.src1_alpha_expand_mode. For 16-bit mode (src1_format=1): 0 = 4:2:2 format (Y0Cb0Y1Cr0); 1 = 6:5:5 format. Bit[15:10] is Y[7:2] or R[7:2], bit[9:5] is Cb[7:3] or G[7:3], bit[4:0] is Cr[7:3] or B[7:3], for Alpha value refer to src1_def_color_alpha 0x8a6[7:0]; 2 = 8:4:4 format. Bit[15:8] is Y or R, bit[7:4] is Cb[7:4] or G[7:4], bit[3:0] is Cr[7:4] or B[7:4]], for Alpha value refer to src1_def_color_alpha 0x8a6[7:0]; 3 = 6:4:4:2 format. Bit[15:10] is Y[7:2] or R[7:2], bit[9:6] is Cb[7:4] or G[7:4], bit [5:2] is Cr[7:4] or B[7:4], bit[1:0] is Alpha[7:6]; 4 = 4:4:4:4 format. Bit[15:12] is Y[7:4] or R[7:4], bit[11:8] is Cb[7:4] or G[7:4], bit [7:4] is Cr[7:4] or B[7:4], bit[3:0] is Alpha[7:4]; 5 = 5:6:5 format. Bit[15:11] is Y[7:3] or R[7:3], bit[10:5] is Cb[7:2] or G[7:2], bit [4:0] is Cr[7:3] or B[7:3], for Alpha value refer to src1_def_color_alpha 0x8a6 [7:0]; 6 = 4:4:4:4 format. Bit[15:12] is Alpha[7:4], bit[11:8] is Y[7:4] or R[7:4], bit[7:4] is Cb[7:4] or G[7:4], bit[3:0] is Cr[7:4] or B[7:4]; 7 = 1:5:5:5 format. Bit[15] is Alpha[7], bit[14:10] is Y[7:3] or R[7:3], bit[9:5] is Cb [7:3] or G[7:3], bit[4:0] is Cr[7:3] or B[7:3]; 8 = 4:6:4:2 format. Bit[15:12] is Y[7:4] or R[7:4], bit[11:6] is Cb[7:2] or G[7:2], bit [5:2] is Cr[7:4] or B[7:4], bit[1:0] is Alpha[1:0]. For 24-bit mode (src1_format=2): 0 = RGB 8:8:8 mode. Bit[23:16] is Y or R, bit[15:8] is Cb or G, bit[7:0] is Cr or B, for Alpha value refer to src1_def_color_alpha 0x8a6[7:0]; 1 = RGBA 5:6:5:8 mode. Bit[23:19] is Y[7:3] or R[7:3], bit[18:13] is Cb[7:2] or G [7:2], bit[12:8] is Cr[7:3] or B[7:3], bit[7:0] is Alpha; 2 = ARGB 8:5:6:5 mode. Bit[23:16] is Alpha, bit[15:11] is Y[7:3] or R[7:3], bit [10:5] is Cb[7:2] or G[7:2], bit[4:0] is Cr[7:3] or B[7:3]; 3 = RGBA 6:6:6:6 mode. Bit[23:18] is Y[7:2] or R[7:2], bit[17:12] is Cb[7:2] or G [7:2], bit[11:6] is Cr[7:2] or B[7:2], bit[5:0] is Alpha[7:2]; 4 = ARGB 6:6:6:6 mode. Bit[23:18] is Alpha[7:2];, bit[17:12] is Y[7:2] or R[7:2], bit[11:6] is Cb[7:2] or G[7:2], bit[5:0] is Cr[7:2] or B[7:2]; 5 = BGR 8:8:8 mode. Bit[23:16] is Cr or B, bit[15:8] is Cb or G, bit[7:0] is Y or R, for Alpha value refer to src1_def_color_alpha 0x8a6[7:0]. 14=NV12 format. 8-bit Y and 16-bit CbCr; 15=NV21 format. 8-bit Y and 16-bit CrCb;

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Bit(s)	R/W	Default	Description
			For 32-bit mode (src1_format=3): 0 = RGBA 8:8:8:8 format. Bit[31:24] is Y or R, bit[23:16] is Cb or G; bit[15:8] is Cr or B; bit[7:0] is Alpha; 1 = ARGB 8:8:8:8 format. Bit[31:24] is Alpha, bit[23:16] is Y or R; bit[15:8] is Cb or G; bit[7:0] is Cr or B; 2 = ABGR 8:8:8:8 format. Bit[31:24] is Alpha, bit[23:16] is Cr or B; bit[15:8] is Cb or G; bit[7:0] is Y or R; 3 = BGRA 8:8:8:8 format. Bit[31:24] is Cr or B, bit[23:16] is Cb or G; bit[15:8] is Y or R; bit[7:0] is Alpha.
2	R/W	0	src1_DEEPCOLOR: 1 = Enable deepcolor formats support, the formats are defined by SRC1_FORMAT and SRC1_COLOR_MAP; 0 = Disable deepcolor. The supported deepcolor formats are as below: src1_deep_color=1, src1_format=2'b01, src1_color_map=4'b0000 or 4'b0001: 10-bit 422 in one canvas – 10-bit Y + 10-bit C = 20-bit per pixel in canvas. If src1_color_map=4'b0000, the sequence is Y0Cb0, Y1Cr0, ... If src1_color_map=4'b0001, the sequence is Y0Cr0, Y1Cb0, ... src1_deep_color=1, src1_format=2'b01, src1_color_map=4'b1000 or 4'b1001: 12-bit 422 in one canvas – 12-bit Y + 12-bit C = 24-bit per pixel in canvas. If src1_color_map=4'b1000, the sequence is Y0Cb0, Y1Cr0, ... If src1_color_map=4'b1001, the sequence is Y0Cr0, Y1Cb0, ... src1_deep_color=1, src1_format=2'b10: 10-bit 444 in one canvas – 10-bit Y + 10-bit Cb + 10-bit Cr + 2-bit stuffing = 32-bit per pixel in canvas. If src1_color_map=4'b0000, the sequence is Y0Cb0Cr0, Y1Cb1Cr1, ... If src1_color_map=other value, the sequence is Cr0Cb0Y0, Cr1Cb1Y1, ...
1-0	R/W	0	src1_format: define input pixel byte-width. Note: If SRC1_DEEPCOLOR=0, the SRC1_FORMAT's definitions is as below. If SRC1_DEEPCOLOR=1, please refer to SRC1_DEEPCOLOR entry for new meaning. 0: Input pixel is 1-byte (8-bit), it is either an 8-bit color component or 8-bit address to look up a 32-bit pixel, refer to GE2D_GEN_CTRL0. src1_lut_en 1: Input pixel is 2-byte (16-bit), refer to GE2D_GEN_CTRL2.SRC1_COLOR_MAP for further pixel color mapping; 2: Input pixel is 3-byte (24-bit), refer to GE2D_GEN_CTRL2.SRC1_COLOR_MAP for further pixel color mapping; 3: Input pixel is 4-byte (32-bit), refer to GE2D_GEN_CTRL2.SRC1_COLOR_MAP for further pixel color mapping.

Table 8-4 GE2D_CMD_CTRL 0x8A3

Bit(s)	R/W	Default	Description
31-29	R	0	unused
28	R/W	0	sec_mode: if true, ge2d works with secure domain
15-14	R/W	0	src2_x_interp_ctrl: if true, do interpolation mode
13-12	R/W	0	src2 y repeat: 0 will not repeat, 1 for 1:2, 2 for 1:4, 3 for 1:8
11-10	R/W	0	src2 y repeat: 0 will not repeat, 1 for 1:2, 2 for 1:4, 3 for 1:8
9	R/W	0	src2_fill_color_en: if true, all src2 data use default color.
8	R/W	0	src1_fill_color_en: if true, all src1 data use default color.
7	R/W	0	dst_xy_swap: if true, dst x/y swap.
6	R/W	0	dst_x_rev: if true, dst x direction reversely read.

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Bit(s)	R/W	Default	Description
5	R/W	0	dst_y_rev: if true, dst y direction reversely read.
4	R/W	0	src2_x_rev: if true, src2 x direction reversely read.
3	R/W	0	src2_y_rev: if true, src2 y direction reversely read.
2	R/W	0	src1_x_rev: if true, src1 x direction reversely read.
1	R/W	0	src1_y_rev: if true, src1 y direction reversely read.
0	R/W	0	cbus_cmd_wr: If true, generate a pulse to validate a GE2D command, the command is described by the rest of the field of this register.

Table 8-5 GE2D_STATUS0 0x8A4

Bit(s)	R/W	Default	Description
31-29	R	0	unused
28-17	R	0	dst write response counter, for debug only.
16-7	R	0	dp_status: ge2d_dp status, for debug only.
6	R	0	r1cmd_rdy: read src2 cmd ready.
5	R	0	r2cmd_rdy: read src2 cmd ready.
4	R	0	pdpcmd_v: pre dpcmd ready.
3	R	0	dpcmd_rdy: GE2D dpcmd ready.
2	R	0	buf_cmd_v: GE2D buffer command valid.
1	R	0	curr_cmd_v: GE2D current command valid.
0	R	0	ge2d_busy: GE2D busy.

Table 8-6 GE2D_STATUS1 0x8A5

Bit(s)	R/W	Default	Description
31-30	R	0	unused
29-16	R	0	ge2d_dst1_status, for debug only.
15	R	1	ge2d_rd_src2 core.fifo_empty.
14	R	0	ge2d_rd_src2 core.fifo_overflow.
13-12	R	0	ge2d_rd_src2 core.req_st. Same as req_st_y.
11	R	0	ge2d_rd_src2 cmd_if.cmd_err, true if cmd_format=1.
10	R	0	ge2d_rd_src2 cmd_if.cmd_st, 0=IDLE state, 1=BUSY state.
9	R	1	ge2d_rd_src1 luma_core(chroma_core).fifo_empty.
8	R	0	ge2d_rd_src1 luma_core(chroma_core).fifo_overflow.
7-6	R	0	ge2d_rd_src1 chroma_core.req_st_cr. Same as req_st_y.
5-4	R	0	ge2d_rd_src1 chroma_core.req_st_cb. Same as req_st_y.
3-2	R	0	ge2d_rd_src1 luma_core.req_st_y. 0: IDLE;

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Bit(s)	R/W	Default	Description
			1: WAIT_FIFO_ROOM; 2: REQUEST; 3: WAIT_FINISH.
1	R	0	ge2d_rd_src1 cmd_if.stat_read_window_err, 1=reading/clipping window setting exceed limit.
0	R	0	ge2d_rd_src1 cmd_if.cmd_st, 0=IDLE state, 1=BUSY state.

Table 8-7 GE2D_SRC1_DEF_COLOR 0x8A6

Bit(s)	R/W	Default	Description
31-24	R/W	0	Default Y or R.
23-16	R/W	0x80	Default Cb or G.
15-8	R/W	0x80	Default Cr or B.
7-0	R/W	0	Default Alpha.

Table 8-8 GE2D_SRC1_CLIPX_START_END 0x8A7

Bit(s)	R/W	Default	Description
31	R/W	0	SRC1 clip x start extra, if true, one more data is read for chroma.
30-29	R	0	Unused.
28-16	R/W	0	SRC1 clip x start.
15	R/W	0	SRC1 clip x end extra, if true, one more data is read for chroma.
14-13	R	0	Unused.
12-0	R/W	0x1FFF	SRC1 clip x end.

Table 8-9 GE2D_SRC1_CLIPY_START_END 0x8A8

Bit(s)	R/W	Default	Description
30-29	R	0	Unused.
28-16	R/W	0	SRC1 clip y start.
14-13	R	0	Unused.
12-0	R/W	0x1FFF	SRC1 clip y end.

Table 8-10 GE2D_SRC1_CANVAS 0x8A9

Bit(s)	R/W	Default	Description
24	R/W	0	SRC1 canvas address0, for Y only or Y/Cb/Cr stored together.
7-3	R	0	Unused.
2-0	R/W	0	Blk32 mode

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Table 8-11 GE2D_SRC1_X_START_END 0x8AA

Bit(s)	R/W	Default	Description
31	R/W	0	SRC1 x start extra bit1, if true, one more chroma data is read for x even start chroma data when y/c ratio = 2 or x even/odd start chroma extra data when y/c ratio = 1
30	R/W	0	SRC1 x start extra bit0, if true, one more chroma data is read for x odd start chroma data when y/c ratio = 2
29-16	R/W	0	SRC1 x start, signed data
15	R/W	0	SRC1 x end extra bit1, if true, one more chroma data is read for x odd end chroma data when y/c ratio = 2 or x even/odd end chroma extra data when y/c ratio = 1
14	R/W	0	SRC1 x end extra bit0, if true, one more chroma data is read for x even end chroma data when y/c ratio = 2
13-0	R/W	0	SRC1 x end, signed data.

Table 8-12 GE2D_SRC1_Y_START_END 0x8AB

Bit(s)	R/W	Default	Description
31	R/W	0	SRC1 y start extra bit1, if true, one more chroma line is read for y even start chroma data when y/c ratio = 2 or x even/odd start chroma extra data when y/c ratio = 1
30	R/W	0	SRC1 y start extra bit0, if true, one more chroma line is read for y odd start chroma data when y/c ratio = 2
29-16	R/W	0	SRC1 y start, signed data
15	R/W	0	SRC1 y end extra bit1, if true, one more chroma line is read for y odd end chroma data when y/c ratio = 2 or y even/odd end chroma extra data when y/c ratio = 1
14	R/W	0	SRC1 y end extra bit0, if true, one more chroma line is read for y even end chroma data when y/c ratio = 2
13-0	R/W	0	SRC1 y end, signed data.

Table 8-13 GE2D_SRC1_LUT_ADDR 0x8AC

Bit(s)	R/W	Default	Description
31-9	R	0	Unused.
8	R/W	1	0 = Write LUT, 1 = Read LUT.
7-0	R/W	0	lut_addr: The initial read or write address of the look-up table

Table 8-14 GE2D_SRC1_LUT_DAT 0x8AD

Bit(s)	R/W	Default	Description
31-24	R/W	0	Current LUT entry's Y or R
23-16	R/W	0	Current LUT entry's Cb or G
15-8	R/W	0	Current LUT entry's Cr or B
7-0	R/W	0	Current LUT entry's Alpha.

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Table 8-15 GE2D_SRC1_FMT_CTRL 0x8AE

Bit(s)	R/W	Default	Description
31-20	R	0	Unused.
19	R/W	0	src1_chfmt_rpt_pix: if true, horizontal formatter using repeat to get the pixel, otherwise using interpolation.
18	R/W	0	src1_chfmt_en: horizontal formatter enable.
17	R/W	0	src1_cvfmt_rpt_pix: if true, vertical formatter using repeat to get the pixel, otherwise using interpolation.
16	R/W	0	src1_cvfmt_en: vertical formatter enable.
15-8	R/W	0	src1_x_chr_phase: X direction chroma phase, Bit[15:12] for x direction even start/end chroma phase when y/c ratio = 2 or start/end even/odd chroma phase when y/c ratio = 1; Bit[11:8] for x direction odd start/end chroma phase only when y/c ration = 2.
7-0	R/W	0	src1_y_chr_phase:Y direction chroma phase. Bit[7:4] for y direction even start/end chroma phase when y/c ratio = 2 or start/end even/odd chroma phase when y/c ratio = 1; Bit[3:0] for y direction odd start/end chroma phase only when y/c ration = 2.

Table 8-16 GE2D_SRC2_DEF_COLOR 0x8AF

Bit(s)	R/W	Default	Description
31-24	R/W	0	Default Y or R.
23-16	R/W	0x80	Default Cb or G.
15-8	R/W	0x80	Default Cr or B.
7-0	R/W	0	Default Alpha.

Table 8-17 GE2D_SRC2_CLIPX_START_END 0x8B0

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	SRC2 clip x start.
15-13	R	0	Unused.
12-0	R/W	0x1FFF	SRC2 clip x end.

Table 8-18 GE2D_SRC2_CLIPY_START_END 0x8B1

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	SRC2 clip y start.
15-13	R	0	Unused.
12-0	R/W	0x1FFF	SRC2 clip y end.

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Table 8-19 GE2D_SRC2_X_START_END 0x8B2

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	SRC2 x start.
15-13	R	0	Unused.
12-0	R/W	0	SRC2 x end.

Table 8-20 GE2D_SRC2_Y_START_END 0x8B3

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	SRC2 y start.
15-13	R	0	Unused.
12-0	R/W	0	SRC2 y end.

Table 8-21 GE2D_DST_CLIPX_START_END 0x8B4

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	DST clip x start.
15-13	R	0	Unused.
12-0	R/W	0x1FFF	DST clip x end.

Table 8-22 GE2D_DST_CLIPY_START_END 0x8B5

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	DST clip y start.
15-13	R	0	Unused.
12-0	R/W	0x1FFF	DST clip y end.

Table 8-23 GE2D_DST_X_START_END 0x8B6

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	DST x start.
15-13	R	0	Unused.
12-0	R/W	0	DST x end.

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Table 8-24 GE2D_DST_Y_START_END 0x8B7

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	DST y start.
15-13	R	0	Unused.
12-0	R/W	0	DST y end.

Table 8-25 GE2D_SRC2_DST_CANVAS 0x8B8

Bit(s)	R/W	Default	Description
31-27	R	0	Unused.
26	R/W	0	Dst2 32blk
25	R/W	0	Src2 32blk
24	R/W	0	Dst1 32blk
23-16	R/W	0	DST2 canvas address.
15-8	R/W	0	SRC2 canvas address.
7-0	R/W	0	DST1 canvas address.

Table 8-26 GE2D_VSC_START_PHASE_STEP 0x8B9

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-0	R/W	0x0100-0000	5.24 format.

Table 8-27 GE2D_VSC_PHASE_SLOPE 0x8BA

Bit(s)	R/W	Default	Description
31-25	R	0	Unused.
24-0	R/W	0	Signed data.

Table 8-28 GE2D_VSC_INI_CTRL 0x8BB

Bit(s)	R/W	Default	Description
31	R	0	Unused.
30-29	R/W	0	vertical repeat line0 number.
28-24	R	0	Unused.
23-0	R/W	0	vertical scaler initial phase.

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Table 8-29 GE2D_HSC_START_PHASE_STEP 0x8BC

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-0	R/W	0x0100-0000	5.24 format.

Table 8-30 GE2D_HSC_PHASE_SLOPE 0x8BD

Bit(s)	R/W	Default	Description
31-25	R	0	Unused.
24-0	R/W	0	Signed data.

Table 8-31 GE2D_HSC_INI_CTRL 0x8BE

Bit(s)	R/W	Default	Description
31	R	0	Unused.
30-29	R/W	0	horizontal repeat line0 number.
28-24	R	0	Unused.
23-0	R/W	0	horizontal scaler initial phase.

Table 8-32 GE2D_HSC_ADV_CTRL 0x8BF

Bit(s)	R/W	Default	Description
31-24	R/W	0	advance number in this round, if horizontal scaler is working on dividing mode.
23-0	R/W	0	horizontal scaler advance phase in this round, if horizontal scaler is working on dividing mode.

Table 8-33 GE2D_SC_MISC_CTRL 0x8C0

Bit(s)	R/W	Default	Description
31	R	0	Unused.
30	R/W	0	vsc_nearest_en: vertical nearest mode enable, must set vt_bank_length = 4.
29	R/W	0	hsc_nearest_en: horizontal nearest mode enable, must set hz_bank_length = 4.
28	R/W	0	hsc_div_en: horizontal scaler dividing mode enable.
27-15	R/W	0	hsc_div_length: horizontal dividing length, if bit 25 is enable.
14	R/W	0	pre horizontal scaler enable.
13	R/W	0	pre vertical scale enable.
12	R/W	0	vertical scale enable.
11	R/W	0	horizontal scaler enable.
10	R	0	Unused.
9	R/W	0	HSc_rpt_ctrl: if true, treat horizontal repeat line number(GE2D_HSC_INI_CTRL bit 30:29) as repeating line, otherwise using treat horizontal repeat line number as minus line number.

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Bit(s)	R/W	Default	Description
8	R/W	0	VSc_rpt_ctrl: if true, treat vertical repeat line number(GE2D_VSC_INI_CTRL bit 30:29) as repeating line, otherwise using treat vertical repeat line number as minus line number.
7	R/W	0	vsc_phase0_always_en: if true, always use phase0 in vertical scaler.
6-4	R/W	2	vsc_bank_length: vertical scaler bank length.
3	R/W	0	hsc_phase0_always_en: if true, always use phase0 in horizontal scaler.
2-0	R/W	2	hsc_bank_length: horizontal scaler bank length.

Table 8-34 GE2D_VSC_NRND_POINT 0x8C1

Bit(s)	R/W	Default	Description
31-14	R	0	Unused.
13-0	R	0	vertical scaler next round integer pixel pointer, signed data.

Table 8-35 GE2D_VSC_NRND_PHASE 0x8C2

Bit(s)	R/W	Default	Description
31-24	R	0	Unused.
23-0	R	0	vertical scaler next round phase.

Table 8-36 GE2D_HSC_NRND_POINT 0x8C3

Bit(s)	R/W	Default	Description
31-14	R	0	Unused.
13-0	R	0	horizontal scaler next round integer pixel pointer, signed data.

Table 8-37 GE2D_HSC_NRND_PHASE 0x8C4

Bit(s)	R/W	Default	Description
31-24	R	0	Unused.
23-0	R	0	horizontal scaler next round phase.

Table 8-38 GE2D_MATRIX_PRE_OFFSET 0x8C5

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-20	R/W	0	pre_offset0.
19	R	0	Unused.
18-10	R/W	0	pre_offset1.
9	R	0	Unused.
8-0	R/W	0	pre_offset2.

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Table 8-39 GE2D_MATRIX_COEF00_01 0x8C6

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	coef00.
15-13	R	0	Unused.
12-0	R/W	0	coef01.

Table 8-40 GE2D_MATRIX_COEF02_10 0x8C7

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	Coef02.
15-13	R	0	Unused.
12-0	R/W	0	Coef10.

Table 8-41 GE2D_MATRIX_COEF11_12 0x8C8

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	Coef11.
15-13	R	0	Unused.
12-0	R/W	0	Coef12.

Table 8-42 GE2D_MATRIX_COEF20_21 0x8C9

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	Coef20.
15-13	R	0	Unused.
12-0	R/W	0	Coef21.

Table 8-43 GE2D_MATRIX_COEF22_CTRL 0x8CA

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	coef22.
15-8	R	0	Unused.
7	R/W	0	input y/cb/cr saturation enable.
6-1	R	0	Unused.
0	R/W	0	conversion matrix enable.

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Table 8-44 GE2D_MATRIX_OFFSET 0x8CB

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-20	R/W	0	offset0.
19	R	0	Unused.
18-10	R/W	0	offset1.
9	R	0	Unused.
8-0	R/W	0	offset2.

Table 8-45 GE2D_ALU_OP_CTRL 0x8CC

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-27	R/W	0	Src2 Ad mux. 0:Ad=Adr*Ag, 1:Ad=Adr*Ag*Adr*Ag, 2:Ad=Adr*Ag*Adr, 3:Ad = 1
26-25	R/W	0	SRC1 color multiplier alpha selection. if 00, Cs = Csr if 01, Cs = Csr * Asr * Ag (if source is not premultiplied) if 10, Cs = Csr * Ag (if source is premultipied).
24	R/W	0	SRC2 color multiplier alpha selection. if 0, no multiplier, Cd = Cdr, otherwise, Cd = Cdr * Ad.
23	R	0	Unused.
22-12	R/W	0x010	ALU color operation. Bit[22:20] Blending Mode Parameter. 3'b000: ADD Cs*Fs + Cd*Fd 3'b001: SUBTRACT Cs*Fs - Cd*Fd 3'b010: REVERSE SUBTRACT Cd*Fd - Cs*Fs 3'b011: MIN min(Cs*Fs, Cd*Fd) 3'b100: MAX max(Cs*Fs, Cd*Fd) 3'b101: LOGIC OP Cs op Cd .... reserved Bit[19:16] Source Color Blending Factor CFs. 4'b0000: ZERO 0 4'b0001: ONE 1 4'b0010: SRC_COLOR Cs(RGBs) 4'b0011: ONE_MINUS_SRC_COLOR 1 - Cs(RGBs) 4'b0100: DST_COLOR Cd(RGBd) 4'b0101: ONE_MINUS_DST_COLOR 1 - Cd(RGBd) 4'b0110: SRC_ALPHA As 4'b0111: ONE_MINUS_SRC_ALPHA 1 – As 4'b1000: DST_ALPHA Ad 4'b1001: ONE_MINUS_DST_ALPHA 1 – Ad 4'b1010: CONST_COLOR Cc(RGBc) 4'b1011: ONE_MINUS_CONST_COLOR 1 - Cc(RGBc) 4'b1100: CONST_ALPHA Ac 4'b1101: ONE_MINUS_CONST_ALPHA 1 – Ac 4'b1110: SRC_ALPHA_SATURATE min(As,1-Ad) .... reserved Bit[15:12] dest Color Blending Factor CFd, when bit[22:20]!= LOGIC OP. 4'b0000: ZERO 0 4'b0001: ONE 1 4'b0010: SRC_COLOR Cs(RGBs) 4'b0011: ONE_MINUS_SRC_COLOR 1 - Cs(RGBs) 4'b0100: DST_COLOR Cd(RGBd) 4'b0101: ONE_MINUS_DST_COLOR 1 - Cd(RGBd) 4'b0110: SRC_ALPHA As 4'b0111: ONE_MINUS_SRC_ALPHA 1 – As 4'b1000: DST_ALPHA Ad 4'b1001: ONE_MINUS_DST_ALPHA 1 – Ad 4'b1010: CONST_COLOR Cc(RGBc) 4'b1011: ONE_MINUS_CONST_COLOR 1 - Cc(RGBc) 4'b1100: CONST_ALPHA Ac 4'b1101: ONE_MINUS_CONST_ALPHA 1 – Ac 4'b1110: SRC_ALPHA_SATURATE min(As,1-Ad) .... reserved Bit[15:12] logic operations, when bit[22:20]== LOGIC OP. 4'b0000: CLEAR 0 4'b0001: COPY s 4'b0010: NOOP d 4'b0011: SET 1 4'b0100: COPY_INVERT ~s 4'b0101: INVERT ~d 4'b0110: AND_REVERSE s & ~d 4'b0111: OR_REVERSE s | ~d 4'b1000: AND s & d 4'b1001: OR s | d 4'b1010: NAND ~(s & d) 4'b1011: NOR ~(s | d) 4'b1100: XOR s ^ d 4'b1101:

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Bit(s)	R/W	Default	Description
			EQUIV ~(s ^ d) 4'b1110: AND_INVERTED ~s & d 4'b1111: OR_INVERTED ~s | d
11	R	0	Unused.
10-0	R/W	0x010	ALU alpha operation. Bit[10:8] Blending Equation Math Operation. 3'b000: ADD As*Fs + Ad*Fd 3'b001: SUBTRACT As*Fs - Ad*Fd 3'b010: REVERSE SUBTRACT Ad*Fd - As*Fs 3'b011: MIN min(As*Fs, Ad*Fd) 3'b100: MAX max(As*Fs, Ad*Fd) 3'b101: LOGIC OP As op Ad .... reserved Bit[7:4] Source alpha Blending Factor AFs. 4'b0000 0 4'b0001 1 4'b0010 As 4'b0011 1 - As 4'b0100 Ad 4'b0101 1 – Ad 4'b0110 Ac 4'b0111 1 – Ac .... reserved Bit[3:0] Destination alpha Blending Factor AFd, when bit[10:8] != LOGIC OP. 4'b0000 0 4'b0001 1 4'b0010 As 4'b0011 1 - As 4'b0100 Ad 4'b0101 1 - Ad 4'b0110 Ac 4'b0111 1 - Ac .... reserved Bit[3:0] logic operations, when bit[10:8] == LOGIC OP. 4'b0000: CLEAR 0 4'b0001: COPY s 4'b0010: NOOP d 4'b0011: SET 1 4'b0100: COPY_INVERT ~s 4'b0101: INVERT ~d 4'b0110: AND_REVERSE s & ~d 4'b0111: OR_REVERSE s | ~d 4'b1000: AND s & d 4'b1001: OR s | d 4'b1010: NAND ~(s & d) 4'b1011: NOR ~(s | d) 4'b1100: XOR s ^ d 4'b1101: EQUIV ~(s ^ d) 4'b1110: AND_INVERTED ~s & d 4'b1111: OR_INVERTED ~s | d

Table 8-46 GE2D_ALU_CONST_COLOR 0x8CD

Bit(s)	R/W	Default	Description
31-0	R/W	0x0080-8000	RGBA or YCbCrA.

Table 8-47 GE2D_SRC1_KEY 0x8CE

Bit(s)	R/W	Default	Description
31-0	R/W	0	SRC1 Key.

Table 8-48 GE2D_SRC1_KEY_MASK 0x8CF

Bit(s)	R/W	Default	Description
31-0	R/W	0	SRC1 Key Mask.

Table 8-49 GE2D_SRC2_KEY 0x8D0

Bit(s)	R/W	Default	Description
31-0	R/W	0	SRC2 Key.

Table 8-50 GE2D_SRC2_KEY_MASK 0x8D1

Bit(s)	R/W	Default	Description
31-0	R/W	0	Destination Bit Mask.

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Table 8-51 GE2D_DP_ONOFF_CTRL 0x8D3

Bit(s)	R/W	Default	Description
31	R/W	0	DP onoff mode. 0: on_counter means how many pixels will output before ge2d turns off; 1: on_counter means how many clocks will ge2d turn on before ge2d turns off.
30-16	R/W	0	DP on counter.
15	R/W	0	0: vd_format doesnt have onoff mode, 1: vd format has onoff mode.
14-0	R/W	0	DP off counter.

Because there are many coefficients used in the vertical filter and horizontal filters, indirect access the coefficients of vertical filter and horizontal filter is used. For vertical filter, there are 33 x 4 coefficients. For horizontal filter, there are 33 x 4 coefficients

Table 8-52 GE2D_SCALE_COEF_IDX 0x8D4

Bit(s)	R/W	Default	Description
31-16	R	0	Unused.
15	R/W	0	index increment, if bit9 == 1 then (0: index increase 1, 1: index increase 2) else (index increase 2).
14	R/W	0	1: read coef through cbus enable, just for debug purpose in case when we wanna check the coef in ram in correct or not.
13-10	R	0	Unused.
9	R/W	0	if true, use 9bit resolution coef, other use 8bit resolution coef.
8	R/W	0	type of index, 0: vertical coef; 1: horizontal coef.
7	R	0	Unused.
6-0	R/W	0	coef index.

Table 8-53 GE2D_SCALE_COEF 0x8D5

Bit(s)	R/W	Default	Description
31-0	R/W	0	coefficients for vertical filter and horizontal filter.

Table 8-54 GE2D_SRC_OUTSIDE_ALPHA 0x8D6

Bit(s)	R/W	Default	Description
31-25	R	0	Unused.

24	R/W	0	src2 alpha fill mode: together with GE2D_GEN_CTRL0[14](fill_mode), define what alpha values are used.
			0: repeat innner alpha, 1: fill src2 outside alpha.
			
			for the area outside the clipping window. As below:
			fill_mode=0, alpha_fill_mode=0 : use inner alpha, (or default_alpha if src data have no alpha values);
			fill_mode=0, alpha_fill_mode=1 : use outside_alpha;
			fill_mode=1, alpha_fill_mode=0 : use default_alpha;
			fill_mode=1, alpha_fill_mode=1 : use outside_alpha.

23-16	R/W	16	src2 outside alpha.

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Bit(s)	R/W	Default	Description
15-9	R	0	Unused.
8	R/W	1	src1 alpha fill mode, refer to src2 alpha fill mode above.
7-0	R/W	0	src1 outside alpha.

Table 8-55 GE2D_ANTIFLICK_CTRL0 0x8D8

Bit(s)	R/W	Default	Description
31	R/W	0	antiflick enable
24	R/W	0	1: alpha value for the first line use repeated alpha, 0: use bit 23:16 as the first line alpha
23-16	R/W	0	register value for the first line alpha when bit 24 is 1.
8	R/W	0	1: alpha value for the last line use repeated alpha, 0: use bit 7:0 as the last line alpha
7-0	R/W	0	register value for the last line alpha when bit 8 is 1.

Table 8-56 GE2D_ANTIFLICK_CTRL1 0x8D9

Bit(s)	R/W	Default	Description
25	R/W	0	rgb_sel, 1: antiflick RGBA, 0: antiflick YCbCrA
24	R/W	0	cbcr_en, 1: also filter cbcr in case of antiflicking YCbCrA, 0: no filter on cbcr in case of antiflicking YCbCrA
23-16	R/W	0	R mult coef for converting RGB to Y
15- 8	R/W	0	G mult coef for converting RGB to Y
7-0	R/W	0	B mult coef for converting RGB to Y

Y = (R * y_r + G * y_g + B * y_b) / 256

Table 8-57 GE2D_ANTIFLICK_COLOR_FILT0 0x8DA

Bit(s)	R/W	Default	Description
31-24	R/W	0	Y threhold1, when 0<Y<=th1, use filter0.
23-16	R/W	0	color antiflick filter0 n3
15- 8	R/W	0	color antiflick filter0 n2
7-0	R/W	0	color antiflick filter0 n1

Y = (line_up * n1 + line_center * n2 + line_dn * n3) / 128

Table 8-58 GE2D_ANTIFLICK_COLOR_FILT1 0x8DB

Bit(s)	R/W	Default	Description
31-24	R/W	0	Y threhold2, when th1<Y<=th2, use filter1.
23-16	R/W	0	color antiflick filter1 n3

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Bit(s)	R/W	Default	Description
15- 8	R/W	0	color antiflick filter1 n2
7-0	R/W	0	color antiflick filter1 n1

Table 8-59 GE2D_ANTIFLICK_COLOR_FILT2 0x8DC

Bit(s)	R/W	Default	Description
31-24	R/W	0	Y threhold3, when th2<Y<=th3, use filter2 ; Y>th3, use filter3.
23-16	R/W	0	color antiflick filter2 n3
15- 8	R/W	0	color antiflick filter2 n2
7-0	R/W	0	color antiflick filter2 n1

Table 8-60 GE2D_ANTIFLICK_COLOR_FILT3 0x8DD

Bit(s)	R/W	Default	Description
23-16	R/W	0	color antiflick filter3 n3
15- 8	R/W	0	color antiflick filter3 n2
7-0	R/W	0	color antiflick filter3 n1

Table 8-61 GE2D_ANTIFLICK_ALPHA_FILT0 0x8DE

Bit(s)	R/W	Default	Description
31-24	R/W	0	Alpha threhold1, when 0< Alpha<=th1, use filter0.
23-16	R/W	0	Alpha antiflick filter0 n3
15- 8	R/W	0	Alpha antiflick filter0 n2
7-0	R/W	0	Alpha antiflick filter0 n1

Alpha = (line_up * n1 + line_center * n2 + line_dn * n3) / 128

Table 8-62 GE2D_ANTIFLICK_ALPHA_FILT1 0x8DF

Bit(s)	R/W	Default	Description
31-24	R/W	0	Alpha threhold2, when th1< Alpha<=th2, use filter1.
23-16	R/W	0	Alpha antiflick filter1 n3
15- 8	R/W	0	Alpha antiflick filter1 n2
7-0	R/W	0	Alpha antiflick filter1 n1

Table 8-63 GE2D_ANTIFLICK_ALPHA_FILT2 0x8E0

Bit(s)	R/W	Default	Description
31-24	R/W	0	Alpha threhold3, when th2< Alpha<=th3, use filter2; Alpha>th3, use filter3.
23-16	R/W	0	Alpha antiflick filter2 n3

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Bit(s)	R/W	Default	Description
15- 8	R/W	0	Alpha antiflick filter2 n2
7-0	R/W	0	Alpha antiflick filter2 n1

Table 8-64 GE2D_ANTIFLICK_ALPHA_FILT3 0x8E1

Bit(s)	R/W	Default	Description
23-16	R/W	0	Alpha antiflick filter3 n3
15- 8	R/W	0	Alpha antiflick filter3 n2
7-0	R/W	0	Alpha antiflick filter3 n1

Table 8-65 GE2D_SRC1_RANGE_MAP_Y_CTRL 0x8E3

Bit(s)	R/W	Default	Description
30-22	R/W	0	din_offset (signed data)
21-14	R/W	0	map_coef (unsigned data)
13- 10	R/W	0	map_sr (unsigned data)
9-1	R/W	0	dout_offset (signed data)
0	R/W	0	enable

dout = clipto_0_255(((din + din_offset) * map_coef + ((1 << (map_sr - 1))) >> map_sr + dout_offset)

Table 8-66 GE2D_SRC1_RANGE_MAP_CB_CTRL 0x8E4

Bit(s)	R/W	Default	Description
30-22	R/W	0	din_offset (signed data)
21-14	R/W	0	map_coef (unsigned data)
13- 10	R/W	0	map_sr (unsigned data)
9-1	R/W	0	dout_offset (signed data)
0	R/W	0	enable

dout = clipto_0_255(((din + din_offset) * map_coef + ((1 << (map_sr - 1))) >> map_sr + dout_offset)

Table 8-67 GE2D_SRC1_RANGE_MAP_CR_CTRL 0x8E5

Bit(s)	R/W	Default	Description
30-22	R/W	0	din_offset (signed data)
21-14	R/W	0	map_coef (unsigned data)
13- 10	R/W	0	map_sr (unsigned data)
9-1	R/W	0	dout_offset (signed data)
0	R/W	0	enable

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dout = clipto_0_255(((din + din_offset) * map_coef + ((1 << (map_sr - 1))) >> map_sr + dout_offset)

Table 8-68 GE2D_ARB_BURST_NUM 0x8E6

Bit(s)	R/W	Default	Description
21-16	R/W	0x3f	Src1 prearbitor burst number
13-8	R/W	0x3f	Src2 prearbitor burst number
5-0	R/W	0x3f	dst prearbitor burst number

Table 8-69 GE2D_TID_TOKEN 0x8E7

Bit(s)	R/W	Default	Description
21-16	R/W	0x3f	Src1 ID. High 4bit are thread ID, low 2bits are the token
13-8	R/W	0x3f	Src2 ID. High 4bit are thread ID, low 2bits are the token
5-0	R/W	0x3f	dst ID. High 4bit are thread ID, low 2bits are the token

Table 8-70 GE2D_GEN_CTRL3 0x8E8

Bit(s)	R/W	Default	Description
31-28	R/W	0	dst2_bytemask_val: 1-bit mask for each byte (8-bit). Applicable only if both dst_ bitmask_en=1 and dst_bytemask_only=1.
27-26	R/W	0	dst2_pic_struct: Define how destination 2 write the picture to DDR memory. 0: Write all lines (whole frame); 1: Reserved; 2: Write even lines only (top); 3: Write odd lines only (bottom).
25-24	R/W	0	dst2_8b_mode_sel: Destination 8-bit mode component selection. 0: Select Y or R; 1: Select Cb or G; 2: Select Cr or B; 3: Select Alpha.
23	R	0	Unused
22-19	R/W	0	dst2_color_map: Applicable to 16-bit, 24-bit and 32-bit pixel, defines the bit-field allocation of the pixel data. For whether to truncate or round full 8-bit to output, refer to ge2d_gen_ctrl3.dst2_color_round_mode. For 16-bit mode (dst2_format=1): 0 = Unused; 1 = 6:5:5 format. Bit[15:10] is Y[7:2] or R[7:2], bit[9:5] is Cb[7:3] or G[7:3], bit[4:0] is Cr[7:3] or B[7:3]; 2 = 8:4:4 format. Bit[15:8] is Y or R, bit[7:4] is Cb[7:4] or G[7:4], bit[3:0] is Cr[7:4] or B[7:4]]; 3 = 6:4:4:2 format. Bit[15:10] is Y[7:2] or R[7:2], bit[9:6] is Cb[7:4] or G[7:4], bit [5:2] is Cr[7:4] or B[7:4], bit[1:0] is Alpha[7:6]; 4 = 4:4:4:4 format. Bit[15:12] is Y[7:4] or R[7:4], bit[11:8] is Cb[7:4] or G[7:4], bit [7:4] is Cr[7:4] or B[7:4], bit[3:0] is Alpha[7:4]; 5 = 5:6:5 format. Bit[15:11] is Y[7:3] or R[7:3], bit[10:5] is Cb[7:2] or G[7:2], bit [4:0] is Cr[7:3] or B[7:3]; 6 = 4:4:4:4 format. Bit[15:12] is Alpha[7:4], bit[11:8] is Y[7:4] or R[7:4], bit[7:4] is Cb[7:4] or G[7:4], bit[3:0] is Cr[7:4] or B[7:4]; 7 = 1:5:5:5 format. Bit[15] is Alpha[7], bit[14:10] is Y[7:3] or R[7:3], bit[9:5] is Cb [7:3] or G[7:3], bit[4:0] is Cr[7:3] or B[7:3]; 8 = 4:6:4:2 format. Bit[15:12] is Y[7:4] or R[7:4], bit[11:6] is Cb[7:2] or G[7:2], bit [5:2] is Cr[7:4] or B[7:4], bit[1:0] is Alpha[1:0]; 9 = CbCr format. Bit[15:8] is Cb, bit[7:0] is Cr; 10 = CrCb format. Bit[15:8] is Cr, bit[7:0] is Cb.

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Bit(s)	R/W	Default	Description
			For 24-bit mode (dst2_format=2): 0 = RGB 8:8:8 mode. Bit[23:16] is Y or R, bit[15:8] is Cb or G, bit[7:0] is Cr or B; 1 = RGBA 5:6:5:8 mode. Bit[23:19] is Y[7:3] or R[7:3], bit[18:13] is Cb[7:2] or G [7:2], bit[12:8] is Cr[7:3] or B[7:3], bit[7:0] is Alpha; 2 = ARGB 8:5:6:5 mode. Bit[23:16] is Alpha, bit[15:11] is Y[7:3] or R[7:3], bit [10:5] is Cb[7:2] or G[7:2], bit[4:0] is Cr[7:3] or B[7:3]; 3 = RGBA 6:6:6:6 mode. Bit[23:18] is Y[7:2] or R[7:2], bit[17:12] is Cb[7:2] or G [7:2], bit[11:6] is Cr[7:2] or B[7:2], bit[5:0] is Alpha[7:2]; 4 = ARGB 6:6:6:6 mode. Bit[23:18] is Alpha[7:2];, bit[17:12] is Y[7:2] or R[7:2], bit [11:6] is Cb[7:2] or G[7:2], bit[5:0] is Cr[7:2] or B[7:2]; 5 = BGR 8:8:8 mode. Bit[23:16] is Cr or B, bit[15:8] is Cb or G, bit[7:0] is Y or R. For 32-bit mode (dst2_format=3): 0 = RGBA 8:8:8:8 format. Bit[31:24] is Y or R, bit[23:16] is Cb or G; bit[15:8] is Cr or B; bit[7:0] is Alpha; 1 = ARGB 8:8:8:8 format. Bit[31:24] is Alpha, bit[23:16] is Y or R; bit[15:8] is Cb or G; bit[7:0] is Cr or B; 2 = ABGR 8:8:8:8 format. Bit[31:24] is Alpha, bit[23:16] is Cr or B; bit[15:8] is Cb or G; bit[7:0] is Y or R; 3 = BGRA 8:8:8:8 format. Bit[31:24] is Cr or B, bit[23:16] is Cb or G; bit[15:8] is Y or R; bit[7:0] is Alpha.
18	R	0	Unused
17-16	R/W	0	dst2_format: define DST2 output pixel byte-width. 0: Output pixel is 1-byte (8-bit) color component; 1: Output pixel is 2-byte (16-bit), refer to GE2D_GEN_CTRL3.dst2_COLOR_ map for further pixel color mapping; 2: Output pixel is 3-byte (24-bit), refer to GE2D_GEN_CTRL3.dst2_COLOR_ MAP for further pixel color mapping; 3: Output pixel is 4-byte (32-bit), refer to GE2D_GEN_CTRL3.dst2_COLOR_ MAP for further pixel color mapping.
15	R	0	Unused
14	R/W	0	dst2_COLOR_round_MODE. 1 = Truncate the full bit color components to required output bit width; 0 = Round (+ 0.5) the full bit color components to required output bit width.
13-12	R/W	0	dst2_x_discard_mode: Define how DST2 discard X direction data before writing to DDR. Note: x is post reverse/rotation. 0: No discard; 1: Reserved; 2: discard even x; 3: discard odd x.
11-10	R/W	0	dst2_y_discard_mode: Define how DST2 discard Y direction data before writing to DDR. Note: y is post reverse/rotation. 0: No discard; 1: Reserved; 2: discard even y; 3: discard odd y.
9	R	0	Unused
8	R/W	0	dst2_enable: 0: Disable destination 2; 1: Enable destination 2.
7-6	R	0	Unused
5-4	R/W	0	dst1_x_discard_mode: Define how DST1 discard X direction data before writing to DDR. Note: x is post reverse/rotation. 0: No discard; 1: Reserved; 2: discard even x;

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Bit(s)	R/W	Default	Description
			3: discard odd x.
3-2	R/W	0	dst1_y_discard_mode: Define how DST1 discard Y direction data before writing to DDR. Note: y is post reverse/rotation. 0: No discard; 1: Reserved; 2: discard even y; 3: discard odd y.
1	R	0	Unused
0	R/W	1	dst1_enable: 0: Disable destination 1; 1: Enable destination 1.

Table 8-71 GE2D_STATUS2 0x8E9

Bit(s)	R/W	Default	Description
13-12	R	0	ge2d_dst1.ctrl_status
11	R	0	ge2d_dst1.map_srdy
10	R	0	ge2d_dst1.map_d1_srdy
9	R	0	ge2d_dst1.s_v
8	R	0	ge2d_dst1.ofifo_dout_srdy
7-1	R	0	ge2d_dst1.ofifo_cnt
0	R	0	ge2d_dst1.dst_busy

Table 8-72 GE2D_GEN_CTRL4 0x8EA

Bit(s)	R/W	Default	Description
28	R/W	0	am2axi_len4_mode.
0	R/W	0	dis_dp_hang_bugfix.

Table 8-73 GE2D_GEN_CTRL5 0x8f1

Bit(s)	R/W	Default	Description
8	R/W	0	Src2_gb_alpha_en
7-0	R/W	0	Src2_gb_alpha

Table 8-74 GE2D_MATRIX2_PRE_OFFSET 0x890

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-20	R/W	0	pre_offset0.
19	R	0	Unused.
18-10	R/W	0	pre_offset1.

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Bit(s)	R/W	Default	Description
9	R	0	Unused.
8-0	R/W	0	pre_offset2.

Table 8-75 GE2D_MATRIX2_COEF00_01 0x891

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	coef00.
15-13	R	0	Unused.
12-0	R/W	0	coef01.

Table 8-76 GE2D_MATRIX2_COEF02_10 0x892

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	Coef02.
15-13	R	0	Unused.
12-0	R/W	0	Coef10.

Table 8-77 GE2D_MATRIX2_COEF11_12 0x893

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	Coef11.
15-13	R	0	Unused.
12-0	R/W	0	Coef12.

Table 8-78 GE2D_MATRIX2_COEF20_21 0x894

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	Coef20.
15-13	R	0	Unused.
12-0	R/W	0	Coef21.

Table 8-79 GE2D_MATRIX2_COEF22_CTRL 0x895

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	coef22.
15-8	R	0	Unused.

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Bit(s)	R/W	Default	Description
7	R/W	0	input y/cb/cr saturation enable.
6-1	R	0	Unused.
0	R/W	0	conversion matrix enable.

Table 8-80 GE2D_MATRIX2_OFFSET 0x896

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-20	R/W	0	offset0.
19	R	0	Unused.
18-10	R/W	0	offset1.
9	R	0	Unused.
8-0	R/W	0	offset2.

Table 8-81 GE2D_MATRIX3_PRE_OFFSET 0x897

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-20	R/W	0	pre_offset0.
19	R	0	Unused.
18-10	R/W	0	pre_offset1.
9	R	0	Unused.
8-0	R/W	0	pre_offset2.

Table 8-82 GE2D_MATRIX3_COEF00_01 0x898

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	coef00.
15-13	R	0	Unused.
12-0	R/W	0	coef01.

Table 8-83 GE2D_MATRIX3_COEF02_10 0x899

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	coef02.
15-13	R	0	Unused.
12-0	R/W	0	coef10.

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Table 8-84 GE2D_MATRIX3_COEF11_12 0x89a

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	Coef11.
15-13	R	0	Unused.
12-0	R/W	0	Coef12.

Table 8-85 GE2D_MATRIX3_COEF20_21 0x89b

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	Coef20.
15-13	R	0	Unused.
12-0	R/W	0	Coef21.

Table 8-86 GE2D_MATRIX3_COEF22_CTRL 0x89c

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-16	R/W	0	coef22.
15-8	R	0	Unused.
7	R/W	0	input y/cb/cr saturation enable.
6-1	R	0	Unused.
0	R/W	0	conversion matrix enable.

Table 8-87 GE2D_MATRIX3_OFFSET 0x89d

Bit(s)	R/W	Default	Description
31-29	R	0	Unused.
28-20	R/W	0	offset0.
19	R	0	Unused.
18-10	R/W	0	offset1.
9	R	0	Unused.
8-0	R/W	0	offset2.

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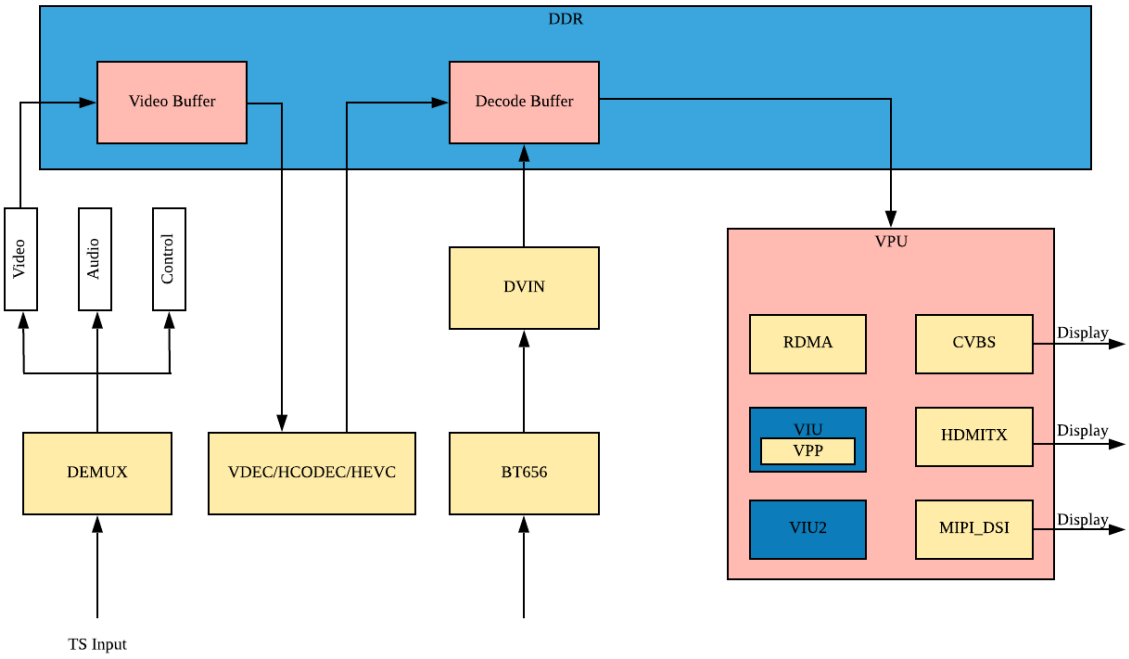
9 Video Path

This section describe the SoC's video path from the following aspects:

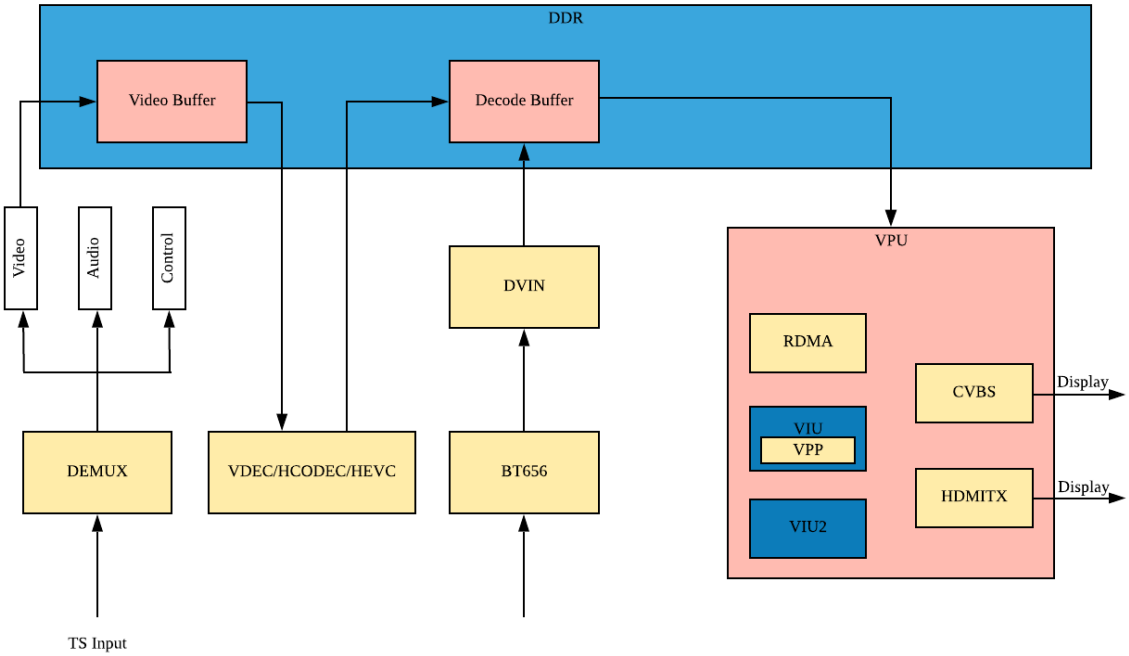
- Video Input
- Video Output
  - RDMA
  - VPP(VIU/VPP)
  - CVBS

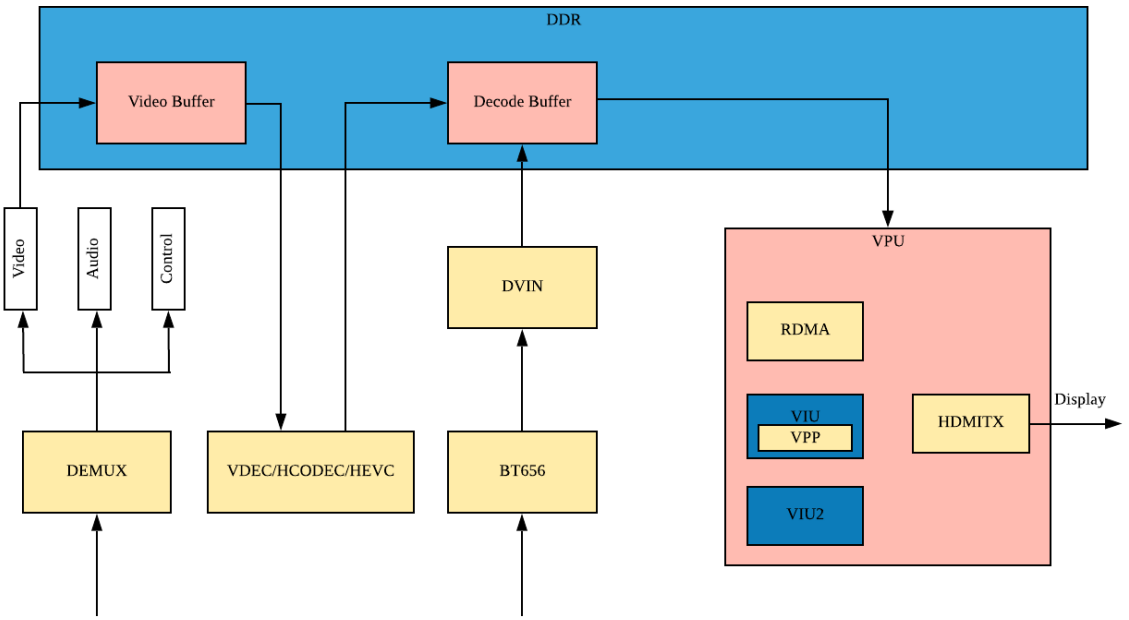
The data path of the video path module is shown in the figure below:

Figure 9-1 Data Path of Video Path



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9.1 Video Input

9.1.1 Features

Support 16 TS streams from demodulators.

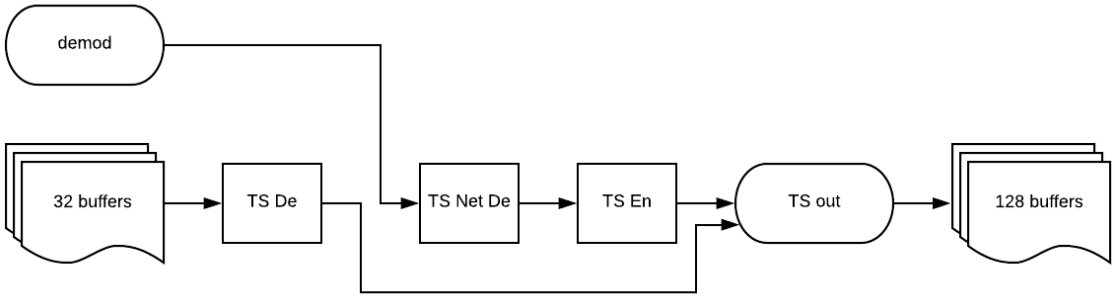
Support 32 TS streams from DDR memory, include TS streams from internet.

Support TS stream local decrypt, network decrypt, local encrypt.

Support multiple TS streams demux and output data in TS, PES or ES format.

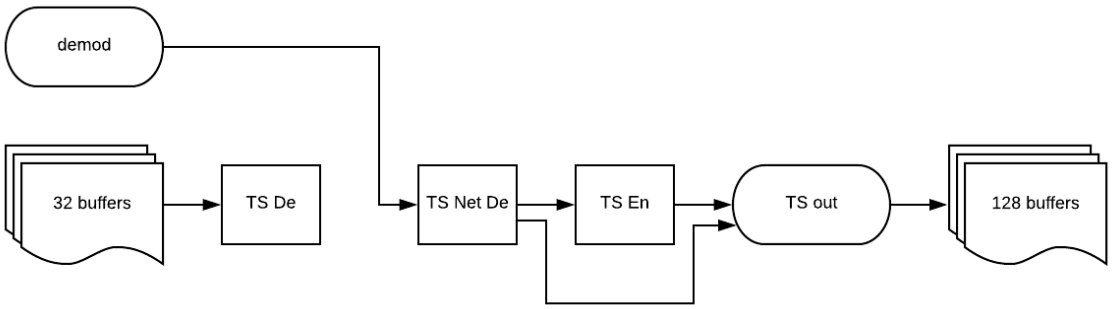
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Figure 9-2 connect to both demod and buffer



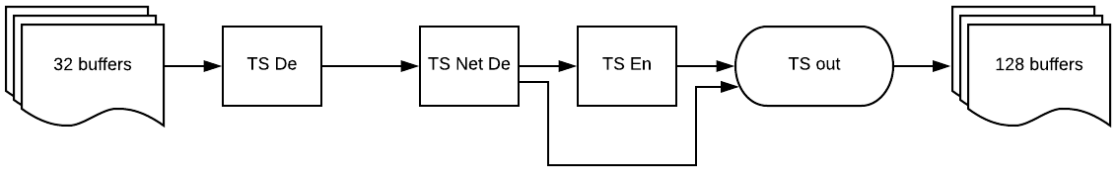
Record programs from Demod and view other programs from Demod or IP buffer

Figure 9-3 connect to demod, play and record



Record and view the same program from Demod, record other programs from Demod, read buffers are not used

Figure 9-4 connect to buffer, play and record



Record programs from IP, view programs from IP or buffer.

View and record the same program is achieved by output TSN packets to both TSE and TSOUT, the packets send to TSOUT with the stream SID MSB flipped.

In case of Demod, only the 32~63 are used, after MSB flipped, the SID is converted from 32~63 to 0~31 for view, the original SID packets are encrypted by local TS encryption and saved.

In case of IP Buffers, only the 0~31 are used, after MSB flipped, the SID is converted from 0~31 to 32~63 for view, the original SID packets are encrypted by local TS encryption and saved.

Setup the SIDs based on use case.

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9.1.2 TS Input

9.1.2.1 Demodulator TS

Demodulator inputs from PINs or from internal demodulator in serial or parallel format

Multiple TS streams can be muxed by adding extra prefix bytes before input into the SOC, the extra bytes are removed by TS input, a side band signal “stream ID” or “SID” is used to identify different TS streams.

Demod TS packet size:

Table 9-1 demod TS interface format

Mode	Size	Note
Standard	188	Physical connection as SID Support 4 TS inputs
Extra bytes	192, 196, 200	Extract SID from extra bytes Support up to 16 SIDs
Extra RS parity	204	Removed by interface

9.1.2.2 Stream from Memory

If a TS stream is downloaded from internet or read from external storage, it is read from DDR memory by TS demux

TS demux supports up to 32 streams data read from DDR memory, TS packet tagged with SID and sent to TS crypto engine, to avoid the same PID from different stream sent to the same TS, 6 bits stream ID is used to separate the same PID case.

Stream ID combined with PID are used to select crypto algorithm and keys.

Secure level of input stream is the same as memory secure level.

When TS read from a memory location with secure level x, then the data is secure level x.

Table 9-2 DDR buffer interface SID

Source	Stream ID (6 bits)	Secure Level (3 bits)
DDR memory	0~31	The same as memory secure level

9.1.3 Crypto Algorithm

Only the following algorithms are supported in TS crypto.

TS Keys are only from Key Table

Host keys, MKL keys, ETSI keys and CAS IP keys are deposited into key table.

Table 9-3 TS descrambler algorithm list

Mode	Algorithm	EMI	TSD 8	TSN 9	TSE 10	IV
0	Pass through	N/A	P	P	P	
1	AES ECB clear end	0021	D	D	E	No IV

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Mode	Algorithm	EMI	TSD 8	TSN 9	TSE 10	IV
2	AES ECB clear front		D	D	E	No IV
3	AES CBC clear end	0022 0023	D	D	E	128 bits
4	AES CBC IDSA	0020	D	D	E	All zero
5	CSA2	0000	-	D	-	No IV
6	DES SCTE41	0031	-	D	-	No IV
7	DES SCTE52	0030	-	D	-	64 bits for CBC 64 bits for short payload
8	TDES ECB clear end	0041	-	D	-	No IV
9	CPCM LSA MDI CBC		D	D	E	MDI
10	CPCM LSA MDD CBC		D	D	E	MDD
11	CSA3	0001	-	D	-	No IV
12	ASA	0010 0011	-	D	-	No IV
13	ASA LIGHT	0012	-	D	-	No IV

Use OTP bits to disable DES SCTE41, DES SCTE52, CSA2, CSA3, CPCM LSA and DES

For mode 3 and mode 7 with 128 bits IV, retrieve the IV from key table IV slots with the flag as IV.

Host deposits the IVs into key table slot 0 to 63.

9.1.4 TS Input

Save TS/PES/ES data into DDR memory by scatter gather memory list.

Support up to 128 buffers, support byte alignment data address and byte length buffers.

9.1.4.1 Descriptor

Table 9-4 TS data read/write descriptor

bytes	7	6	5	4	3	2	1	0
0	byte length [23:0]							
1								
2								
3			loop	eoc	irq	Byte length [26:24]		
4	address 32 bits							
5								

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6	
7	

Each descriptor is 64 bits, prepared by host and saved in DDR memory, the descriptors are stored in continuous memory address, the last descriptor with end of chain field “eoc” set to 1, or set the loop to 1 to loop back to the beginning of descriptor chain.

Memory access supports byte alignment memory read/write, the address can be any byte alignment and length of memory can be any number of bytes.

Maximum single descriptor memory size is 2^27-1 = 128M-1 bytes.

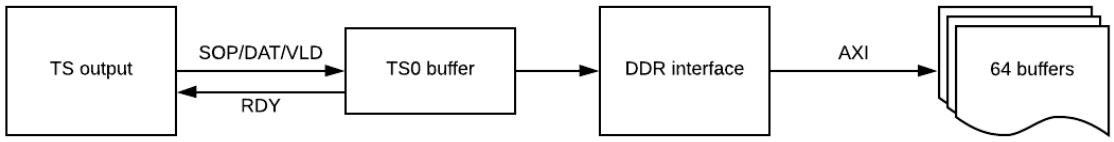
Loop : next descriptor is from beginning, support descriptor loop, send IRQ out when loop back.

Eoc : end of chain, done, send IRQ out

Irq : send IRQ when this descriptor is done.

The DDR memory interface uses 128 bits data bus, the TS crypto module should read/write fraction of 16 bytes first, then process number of 16 byte and finally with a fraction of 16 bytes.

Figure 9-5 TS output DDR interface



9.1.4.2 Output Format

Table 9-5 TS output options

Format	Program	Usage	Details	Secure Level
TS	One	PVR	One program include: Video PID Audio PIDs Subtitle PIDs PCR_PID EMM/ECM PIDs	Encrypted: 0 Clear content: key level
TS	Two+	PVR	Multiple programs	Encrypted: 0 Clear content: key level
TS, PES, ES, PCR registers, PTS/DTS buffer	One	View	Video buffer Audio buffers Subtitle buffers PCR APB registers PTS/DTS buffer	Video ES: key level Audio ES: key level Subtitle: 0 PCR register: 0 PTS/DTS: 0
TS		PAT, EMM, ECM	One SID per buffer	0

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9.1.4.3 TS DMA

32 DMA read channels and 128 write channels

Table 9-6 Read channel data structure

Address	Name	Details	Note
0x0	Ready	[0] semaphore	Read 1 to own read channel Write 1 to release read channel
0x4	Status	[31:24] last_pkt_len [23:22] saved [21:16] read data fifo level [15:14] saved [13:8] in process of read data fifo line [7:4] all chn read cmd [3:0] current chn read cmd	Status, read only
0x8	RCH_CFG	[28] done [27] enable [26] pause [25] clear [23:16] packet length [15:0] read length	Read length: number of bytes per each round robin
0xC	RCH_ADR	Descriptor address	First descriptor address
0x10	RCH_LEN	Total bytes	
0x14	RCH_RD_LEN	number of bytes read	
0x18	RCH_PTR	Current memory address	

Table 9-7 Write channel data structure

Address	Name	Details	Note
0x0	Ready	[0] semaphore	Read 1 to own read channel Write 1 to release read channel
0x4	WCHN_TT_LEN	Wchn total length	
0x8	WCH_CFG	[25] clear [24] unlimited	
0xC	WCH_ADR	Descriptor address	First descriptor address
0x10	WCH_LEN	Total bytes	
0x14	WCH_RD_LEN	Number of bytes written	
0x18	WCH_PTR	Current memory address	

Read TS stream from DDR memory

Support TS stream packet size 188 or 192, when packet size is 192, the extra 4 bytes between TS packet is removed before sent to TS descrambler.

·Acquire the read channel by read register Ready 0x0 and it is 1.

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·Prepare the data descriptor in DDR memory.

·Program the first descriptor address to register RCH_ADR 0xC.

·Total number of bytes to register RCH_LEN 0x10.

·Program RCH_CFG register with packet length, read length and “enable” to 1.

·When done, release Ready by write register 0x0 with 1.

Use similar method to program write channel.

TS DMA APB base address:

APB PADDR[16:14] = 1, APB range 16K bytes

BASE = SECURE_BASE + 0x4000

Table 9-8 read/write channel APB address

APB address	Registers	Note
BASE + RCH_idx * 0x20	32 RCH registers RCH_idx = 0, 1, …, 31	Refer to read channel registers
BASE + 0x1000 + WCH_idx * 0x20	128 WCH registers WCH_idx = 0, 1, ..., 127	Refer to write channel registers
BASE + 0x2000 + Ctrl_register		

Table 9-9 read/write control registers

Address	R/W	Name	Details	Note
BASE + 0x2000	R/W	RCH_INT_MASK	RCH = 0 ~ 31	1 : Mask RCH/WCH INT 0 : Send INT to ACPU
BASE + 0x2004	R/W	WCH_INT_MASK0	WCH = 0 ~ 31	
BASE + 0x2008	R/W	WCH_INT_MASK1	WCH = 32 ~ 63	
BASE + 0x200c	R/W	WCH_INT_MASK2	WCH = 64 ~ 95	
BASE + 0x2010	R/W	WCH_INT_MASK3	WCH = 96 ~ 127	
BASE + 0x2014	R/W	CLEAR_W_BATCH0		
BASE + 0x2018	R/W	CLEAR_W_BATCH1		
BASE + 0x201c	R/W	CLEAR_W_BATCH2		
BASE + 0x2020	R/W	CLEAR_W_BATCH3		
BASE + 0x2024	R/W	CLEAR_RCH	RCH = 0 ~ 31	1 : Clear RCH/ WCH status
BASE + 0x2028	R/W	CLEAR_WCH0	WCH = 0 ~ 31	
BASE + 0x202c	R/W	CLEAR_WCH1	WCH = 32 ~ 63	
BASE + 0x2030	R/W	CLEAR_WCH2	WCH = 64 ~ 95	
BASE + 0x2034	R/W	CLEAR_WCH3	WCH = 96 ~ 127	
BASE + 0x2038	R	RCH_ACTIVE	RCH = 0 ~ 31	1 : RCH/WCH active
BASE + 0x203c	R	WCH_ACTIVE0	WCH = 0 ~ 31	
BASE + 0x2040	R	WCH_ACTIVE1	WCH = 32 ~ 63	
BASE + 0x2044	R	WCH_ACTIVE2	WCH = 64 ~ 95	

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Address	R/W	Name	Details	Note
BASE + 0x2048	R	WCH_ACTIVE3	WCH = 96 ~ 127	
BASE + 0x204C	R	RCH_DONE	RCH = 0 ~ 31	1 : RCH descriptor EOC WCH write RESP received
BASE + 0x2050	R	WCH_DONE0	WCH = 0 ~ 31	
BASE + 0x2054	R	WCH_DONE1	WCH = 32 ~ 63	
BASE + 0x2058	R	WCH_DONE2	WCH = 64 ~ 95	
BASE + 0x205c	R	WCH_DONE3	WCH = 96 ~ 127	
BASE + 0x2060	R	RCH_ERR	RCH = 0 ~ 31	No more RCH descriptor
BASE + 0x2064	R	RCH_LEN_ERR	RCH = 0 ~ 31	RCH descriptor length 0
BASE + 0x2068	R	WCH_ERR0	WCH = 0 ~ 31	WCH descriptor length 0
BASE + 0x206C	R	WCH_ERR1	WCH = 32 ~ 63	
BASE + 0x2070	R	WCH_ERR2	WCH = 64 ~ 95	
BASE + 0x2074	R	WCH_ERR3	WCH = 96 ~ 127	
BASE + 0x2078		DMA_BATCH_END0		
BASE + 0x207C		DMA_BATCH_END0		
BASE + 0x2080		DMA_BATCH_END0		
BASE + 0x2084		DMA_BATCH_END0		
BASE + 0x2088	R	WCH_EOC_DONE0	WCH = 0 ~ 31	WCH descriptor EOC before RESP is received
BASE + 0x208C	R	WCH_EOC_DONE1	WCH = 32 ~ 63	
BASE + 0x2090	R	WCH_EOC_DONE2	WCH = 64 ~ 95	
BASE + 0x2094	R	WCH_EOC_DONE3	WCH = 96 ~ 127	
BASE + 0x2098		UPDT_PKT_SYNC		
BASE + 0x209C		RCH_CFG		
BASE + 0x20A0		WCH_CFG		
BASE + 0x20A4		MEM_PD_CRTL	Memory PD control	
BASE + 0x20A8		DMA_BUS_CFG		
BASE + 0x20AC		DMA_GMW_CFG		
BASE + 0x20B0		DMA_GMR_CFG		

9.2 Video Output

9.2.1 Overview

This section describes the SoC's VPU sub-module, including RDMA sub-module, VIU sub-module, HDMITX sub-module, CVBS sub-module and MIPI_DSI sub-module.

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9.2.2 VPU

VPU is display process unit, the main function is to receive data from decoder/ddr/hdmirx etc, then process the source data in order to get the high-quality video picture, and finally send out the video to the screen by HDMITX/CVBS/MIPI etc.

9.2.3 Register Description

9.2.3.1 VPU Registers

Table 9-10 VPU_CRC_CTRL 0x2701

Bit(s)	R/W	Default	Description
10	R/W	0	vpu axi read channel 2 bist enable
9	R/W	0	vpu axi read channel 1 bist enable
8	R/W	0	vpu axi read channel 0 bist enable
4	R/W	0	vpu axi write channel 1 crc start
3	R/W	0	vpu axi write channel 0 crc start
2	R/W	0	vpu axi read channel 2 crc start
1	R/W	0	vpu axi read channel 1 crc start
0	R/W	0	vpu axi read channel 0 crc start

Table 9-11 VPP_RO_CRC0 0x2702

Bit(s)	R/W	Default	Description
31-0	R	0	vpu axi read 0 crc

Table 9-12 VPP_RO_CRC1 0x2703

Bit(s)	R/W	Default	Description
31-0	R	0	vpu axi read 1 crc

Table 9-13 VPP_RO_CRC2 0x2704

Bit(s)	R/W	Default	Description
31-0	R	0	vpu axi read 2 crc

Table 9-14 VPP_RO_CRC3 0x2705

Bit(s)	R/W	Default	Description
31-0	R	0	vpu axi write 0 cmd crc

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Table 9-15 VPP_RO_CRC4 0x2706

Bit(s)	R/W	Default	Description
31-0	R	0	vpu axi write 0 data crc

Table 9-16 VPP_RO_CRC5 0x2707

Bit(s)	R/W	Default	Description
31-0	R	0	vpu axi write 1 cmd crc

Table 9-17 VPP_RO_CRC6 0x2708

Bit(s)	R/W	Default	Description
31-0	R	0	vpu axi write 1 data crc

Table 9-18 VPP_INTF_CTRL 0x270a

Bit(s)	R/W	Default	Description
18	R/W	1	vpu axi write 1 enable
17	R/W	0	vpu axi write 1 gate clock auto
16	R/W	0	vpu axi write 1 disable clock
14	R/W	1	vpu axi write 0 enable
13	R/W	0	vpu axi write 0 gate clock auto
12	R/W	0	vpu axi write 0 disable clock
10	R/W	1	vpu axi read 2 enable
9	R/W	0	vpu axi read 2 gate clock auto
8	R/W	0	vpu axi read 2 disable clock
6	R/W	1	vpu axi read 1 enable
5	R/W	0	vpu axi read 1 gate clock auto
4	R/W	0	vpu axi read 1 disable clock
2	R/W	1	vpu axi read 0 enable
1	R/W	0	vpu axi read 0 gate clock auto
0	R/W	0	vpu axi read 0 disable clock

Table 9-19 VPP_APB_PROT_CTRL 0x270b

Bit(s)	R/W	Default	Description
21-2	R/W	0	hold number
1	R/W	0	protect enable
0	R/W	0	soft reset

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Table 9-20 VPP_ENC_ERROR 0x270c

Bit(s)	R/W	Default	Description
31-24	R	0	RO enci error count
23-16	R	0	RO encp error count
15-8	R	0	RO encl error count
2	R/W	1	encl afifo error count enable
1	R/W	1	encp afifo error count enable
0	R/W	1	enci afifo error count enable

Table 9-21 VPU_VDIN_PRE_ARB_CTRL 0x2714

Bit(s)	R/W	Default	Description
31	R/W	0	VDIN_PREARB_SOFT_RESET: 1=SW reset vdin_mmc_pre_arb.
30-18	R	0	Reserved.
17	R/W	1	VDIN_ACG_EN: 1=Enable auto-clock gating of vdin_mmc_pre_arb.
16	R/W	0	VDIN_DISABLE_CLK: 1=Disalbe the clock to vdin_mmc_pre_arb.
15-0	R/W	0xffff	VDIN_REQ_EN: vdin_mmc_pre_arb request enable.

Table 9-22 VPU_VDISP_PRE_ARB_CTRL 0x2715

Bit(s)	R/W	Default	Description
31	R/W	0	VDISP_PREARB_SOFT_RESET: 1=SW reset vdisp_mmc_pre_arb.
30-18	R	0	Reserved.
17	R/W	1	VDISP_ACG_EN: 1=Enable auto-clock gating of vdisp_mmc_pre_arb.
16	R/W	0	VDISP_DISABLE_CLK: 1=Disalbe the clock to vdisp_mmc_pre_arb.
15-0	R/W	0xffff	VDISP_REQ_EN: vdisp_mmc_pre_arb request enable.

Table 9-23 VPU_VPUARB2_PRE_ARB_CTRL 0x2716

Bit(s)	R/W	Default	Description
31	R/W	0	VPUARB2_PREARB_SOFT_RESET: 1=SW reset vpuarb2_mmc_pre_arb.
30-18	R	0	Reserved.
17	R/W	1	VPUARB2_ACG_EN: 1=Enable auto-clock gating of vpuarb2_mmc_pre_arb.
16	R/W	0	VPUARB2_DISABLE_CLK: 1=Disalbe the clock to vpuarb2_mmc_pre_arb.
15-0	R/W	0xffff	VPUARB2_REQ_EN: vpuarb2_mmc_pre_arb request enable.

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Table 9-24 VPU_VIU_VENC_MUX_CTRL 0x271a

Bit(s)	R/W	Default	Description
20	R/W	0	Viu_sync_mode_en 1:Viu_sync_mode_en enable// ENCL/P/I vsync send to both viu1 and viu2 Bit[1:0] select data fbettwen viu1 and ENCL/P/I Bit[5:4] select ctrl singal(vsync) bettwen ENCL/P/I and viu1. Bit[3:2] select data and vsync bettwen viu2 and ENCL/P/I 0:Viu_sync_mode_en disable// Bit[1:0] select data and vsync fbettwen viu1 and ENCL/P/I Bit[3:2] select data and vsync bettwen viu2 and ENCL/P/I Bit[5:4] unuse
17-16	W	0	RASP DPI CLOCK SEL : 00 : cph1 01 : cph2 10/11 : cph3
15:6	W	0	reserved
5-4			VIU1_SEL_VENC_CTRL: Select which one of the encl/P/T/L control singal that Viu1 connects to when viu_sync_model enable.unuse when viu_sync_model disable. 0: ENCL 1: ENCI 2: ENCP 3: ENCT
3-2	R/W	0	VIU2_SEL_VENC: Select which one of the encl/P/T/L that Viu2 connects to (both vsync and data). 0: ENCL 1: ENCI 2: ENCP 3: ENCT
1-0	R/W	0	VIU1_SEL_VENC: Select which one of the encl/P/T/L that Viu1 connects to. Only select data when viu_sync_model enable,select both data and vsync when viu_sync_model disable, 0: ENCL 1: ENCI 2: ENCP 3: ENCT

Table 9-25 VPU_HDMI_SETTING 0x271b

Bit(s)	R/W	Default	Description
15-12	R/W	0	RD_RATE: Read rate to the async FIFO between VENC and HDMI. 0: One read every rd_clk 1: One read every 2 rd_clk 2: One read every 3 rd_clk … 15: One read every 16 rd_clk
11-8	R/W	0	WR_RATE: Write rate to the async FIFO between VENC and HDMI. 0: One write every wr_clk 1: One write every 2 wr_clk 2: One write every 3 wr_clk … 15: One write every 16 wr_clk
7-5	R/W	0	DATA_COMP_MAP: Input data is CrYCr(BRG), map the output data to desired format: 0: output CrYCb (BRG) 1: output YCbCr (RGB) 2: output YCrCb (RBG) 3: output CbCrY (GBR) 4: output CbYCr (GRB) 5: output CrCbY (BGR) 6,7: Reserved

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Bit(s)	R/W	Default	Description
4	R/W	0	INV_DVI_CLK: If true, invert the polarity of clock output to external DVI interface. (NOT internal HDMI).
3	R/W	0	INV_VSYNC: If true, invert the polarity of VSYNC input from VENC
2	R/W	0	INV_HSYNC: If true, invert the polarity of HSYNC input from VENC
1-0	R/W	0	SRC_SEL: Select which HDMI source from between ENCI and ENCP. 2'b00: Disable HDMI source 2'b01: Select ENCI data to HDMI 2'b10: Select ENCP data to HDMI

Table 9-26 ENCI_INFO_READ 0x271c

Bit(s)	R/W	Default	Description
31-29	R	0	Current ENCI field status.
28-25	R	0	Reserved
24-16	R	0	Current ENCI line counter status.
15-11	R	0	Reserved
10-0	R	0	Current ENCI pixel counter status.

Table 9-27 ENCP_INFO_READ 0x271d

Bit(s)	R/W	Default	Description
31-29	R	0	Current ENCP field status.
28-16	R	0	Current ENCP line counter status.
15-13	R	0	Reserved
12-0	R	0	Current ENCP pixel counter status.

Table 9-28 ENCT_INFO_READ 0x271e

Bit(s)	R/W	Default	Description
31-29	R	0	Current ENCT field status.
28-16	R	0	Current ENCT line counter status.
15-13	R	0	Reserved
12-0	R	0	Current ENCT pixel counter status.

Table 9-29 ENCL_INFO_READ 0x271f

Bit(s)	R/W	Default	Description
31-29	R	0	Current ENCL field status.
28-16	R	0	Current ENCL line counter status.
15-13	R	0	Reserved
12-0	R	0	Current ENCL pixel counter status.

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Table 9-30 VPU_SW_RESET 0x2720

Bit(s)	R/W	Default	Description
3	R/W	0	vpuarb2_mmc_arb_rst_n
2	R/W	0	vdisp_mmc_arb_rst_n
1	R/W	0	vdin_mmc_arb_rst_n
0	R/W	0	viu_rst_n

Table 9-31 VPU_D2D3_MMC_CTRL 0x2721

Bit(s)	R/W	Default	Description
30	R/W	0	d2d3_depr_req_sel, 0:vdisp_pre_arb, 1: vpuarb2_pre_arb
27-22	R/W	0x3f	d2d3_depr_brst_num
21-16	R/W	0x2d	d2d3_depr_id
14	R/W	0x0	d2d3_depw_req_sel, 0: vdin_pre_arb, 1: vdisp_pre_arb
11-6	R/W	0x3f	d2d3_depw_brst_num
5-0	R/W	0x2e	d2d3_depw_id

Table 9-32 VPU_CONT_MMC_CTRL 0x2722

Bit(s)	R/W	Default	Description
30	R/W	0x0	mtn_contrd_req_sel, 0:vdisp_post_arb, 1: vpuarb2_pre_arb
27-22	R/W	0x3f	mtn_contrd_brst_num
21-16	R/W	0x2b	mtn_contrd_id
14	R/W	0x0	mtn_contwr_req_sel, 0: vdisp_post_arb, 1: vpuarb2_pre_arb
11-6	R/W	0x3f	mtn_contwr_brst_num
5-0	R/W	0x2c	mtn_contwr_id

Table 9-33 VPU_CLK_GATE 0x2723

Bit(s)	R/W	Default	Description
30-18	R/W	0x0	Reserved
17	R/W	0x1	Clk_b control register no latch
16	R/W	0x1	Clk_vib enable
15	R/W	0x1	Gvapbclk enable
14	R/W	0x1	Clk mpeg vlock enable
13	R/W	0x1	Reserved
12	R/W	0x1	Venc_dac_process_clk enable
11	R/W	0x1	Venc_i_top enable
10	R/W	0x1	Venci_int enable

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Bit(s)	R/W	Default	Description
9:8	R/W	0x11	Clk_vib latch sync source select 00: di2ldim_go_field, 01: post_frame_rst;10: pre_frame_rst, 11:viu_go_field
7	R/W	0x1	Reserved
6	R/W	0x1	Vpu_misc_clk enable
5	R/W	0x1	Venc_l_top enable
4	R/W	0x1	Venc_l_int enable
3	R/W	0x1	Venc_p_int enable
2	R/W	0x1	Reserved
1	R/W	0x1	Vi_top clock enable
0	R/W	0x1	Venc_p_top enable

Table 9-34 VPU_HDMI_DATA_OVR 0x2727

Bit(s)	R/W	Default	Description
31	R/W	0	DATA_OVR_EN: Control if override HDMI input data with DATA_OVR[29:0], for display e.g. black or blue screen. 0: No override 1: Enable override
30	R	0	Reserved
29-0	R/W	0	DATA_OVR: programmable pixel data value for override.

Table 9-35 VPU_VPU_PWM_V0 0x2730

Bit(s)	R/W	Default	Description
31	R/W	0	reg_vpu_pwm_inv, 1: invert the pwm signal, active low
30-29	R/W	0	reg_vpu_pwm_src_sel, 00: encl, enct, encp
28-16	R/W	0	reg_vpu_pwm_v_end0
15-14	R/W	0	reg_vpu_pwm_setting_latch_mode
13	R/W	1	reg_vpu_pwm_vs_inv
12-0	R/W	0	reg_vpu_pwm_v_start0

Table 9-36 VPU_VPU_PWM_V1 0x2731

Bit(s)	R/W	Default	Description
28-16	R/W	0	reg_vpu_pwm_v_end1
12-0	R/W	0	reg_vpu_pwm_v_start1

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Table 9-37 VPU_VPU_PWM_V2 0x2732

Bit(s)	R/W	Default	Description
28-16	R/W	0	reg_vpu_pwm_v_end2
12-0	R/W	0	reg_vpu_pwm_v_start2

Table 9-38 VPU_VPU_PWM_V3 0x2733

Bit(s)	R/W	Default	Description
28-16	R/W	0	reg_vpu_pwm_v_end3
12-0	R/W	0	reg_vpu_pwm_v_start3

Table 9-39 VPU_VPU_PWM_H0 0x2734

Bit(s)	R/W	Default	Description
28-16	R/W	0	reg_vpu_pwm_h_end0
12-0	R/W	0	reg_vpu_pwm_h_start0

Table 9-40 VPU_VPU_PWM_H1 0x2735

Bit(s)	R/W	Default	Description
28-16	R/W	0	reg_vpu_pwm_h_end1
12-0	R/W	0	reg_vpu_pwm_h_start1

Table 9-41 VPU_VPU_PWM_H2 0x2736

Bit(s)	R/W	Default	Description
28-16	R/W	0	reg_vpu_pwm_h_end2
12-0	R/W	0	reg_vpu_pwm_h_start2

Table 9-42 VPU_VPU_PWM_H3 0x2737

Bit(s)	R/W	Default	Description
28-16	R/W	0	reg_vpu_pwm_h_end3
12-0	R/W	0	reg_vpu_pwm_h_start3

Table 9-43 VPU_VPU_3D_SYNC1 0x2738

Bit(s)	R/W	Default	Description
31	R/W	0	reg_3dsync_enable, 1: enable 3d sync output
30	R/W	0	3dsync setting vsync latch
29	R/W	0	3dsync go high field polarity: 1, go high while field[0]=1

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Bit(s)	R/W	Default	Description
28-16	R/W	0	reg_3dsync_v_end0
15	R/W	0	3dsync out inv
14	R/W	0	3dsync vbo out inv
13	R/W	1	Vbo 3d en, to v by one, 3d enable
12-0	R/W	0	reg_3dsync_v_start0

Table 9-44 VPU_VPU_3D_SYNC2 0x2739

Bit(s)	R/W	Default	Description
31	R/W	0	Reg_3dsync_field_bit_sel: 1. Keep 3dsync not changed for two fields, i.e. L-L-R-R-L-L-R-R (11001100) 0. Change 3dsync every field i.e. L-R-L-R (1010)
28-16	R/W	0	reg_3dsync_h_end
12-0	R/W	0	reg_3dsync_h_start

Table 9-45 VPU_HDMI_FMT_CTRL 0x2743

Bit(s)	R/W	Default	Description
12 bit to 10 bit dither control register. 10 bit to 8 bit see VPU_HDMI_DITH_CNTL			
21-19	R/W	0	rame count offset for B
18-16	R/W	0	frame count offset for G
15	R/W	0	hcnt hold when de valid
14	R/W	0	RGB frame count seperate
13	R/W	0	dith4x4 : frame random enable
12	R/W	0	dith4x4 enable
11	R/W	0	tunnel enable for DOLBY
10	R/W	0	rounding enable
9-6	R/W	0	Cntl_hdmi_dith10 :
5	R/W	0	Cntl_hdmi_dith_md:
4	R/W	0	Cntl_hdmi_dith_en: dither 10-b to 8-b enable
3-2	R/W	0	Cntl_chroma_dnsmp: Chroma down sample mode when convert to 422 or 420. 0 = use pixel 0; 1 = use pixel 1; 2 = use average;
1-0	R/W	0	Cntl_hdmi_vid_fmt: Control whether to convert ENCP's 444 data to 422 or 420 0 = No convertion; 1 = Convert to 422; 2 = Convert to 420;

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Table 9-46 VPU_VDIN_ASYNC_HOLD_CTRL 0x2744

Bit(s)	R/W	Default	Description
31-24	R/W	‘h18	Wr_hold_num
23-16	R/W	‘h10	Wr_rel_num
15-8	R/W	‘h18	Rd_hold_num
7-0	R/W	‘h10	Rd_rel_num

Table 9-47 VPU_VDISP_ASYNC_HOLD_CTRL 0x2745

Bit(s)	R/W	Default	Description
31-24	R/W	‘h18	Wr_hold_num
23-16	R/W	‘h10	Wr_rel_num
15-8	R/W	‘h18	Rd_hold_num
7-0	R/W	‘h10	Rd_rel_num

Table 9-48 VPU_VPUARB2_ASYNC_HOLD_CTRL 0x2746

Bit(s)	R/W	Default	Description
31-24	R/W	‘h18	Wr_hold_num
23-16	R/W	‘h10	Wr_rel_num
15-8	R/W	‘h18	Rd_hold_num
7-0	R/W	‘h10	Rd_rel_num

Table 9-49 VPU_ARB_URG_CTRL 0x2747

Bit(s)	R/W	Default	Description
11	R/W	0	Rdma_ddr_reg_busy to vpuarb2_urg_ctrl
10	R/W	0	Rdma_ddr_reg_busy to vdisp_urg_ctrl
9	R/W	0	Rdma_ddr_reg_busy to vdin_urg_ctrl
8	R/W	0	Vdin1_lff_urg_ctrl to vpuarb2_urg_ctrl
7	R/W	0	Vdin0_lff_urg_ctrl to vpuarb2_urg_ctrl
6	R/W	0	Vpp_off_urg_ctrl to vpuarb2_urg_ctrl
5	R/W	0	Vdin1_lff_urg_ctrl to vdisp_urg_ctrl
4	R/W	0	Vdin0_lff_urg_ctrl to vdisp_urg_ctrl
3	R/W	0	Vpp_off_urg_ctrl to vdisp_urg_ctrl
2	R/W	0	Vdin1_lff_urg_ctrl to vdin_urg_ctrl
1	R/W	0	Vdin0_lff_urg_ctrl to vdin_urg_ctrl
0	R/W	0	Vpp_off_urg_ctrl to vdin_urg_ctrl

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Table 9-50 VPU_VENCL_DITH_EN 0x2749

R/W	Default	Description
R/W	0	dith_en //dith bettwen vpp and encl_int
R/W	0	dith hsize

Table 9-51 VPU_422TO444_RST 0x274a

Bit(s)	R/W	Default	Description
3	R/W	0	Change output of viu_12bit422to10bit444_vd1 to 10bits 1:cut high 2 bits 0:cut low 2 bits
2	R/W	0	Change output of viu_12bit422to10bit444_encp to 10bits 1:cut high 2 bits 0:cut low 2 bits
1	R/W	0	Soft rst enable of viu_12bit422to10bit444_vd1 module active high
0	R/W	0	Soft rst enable of viu_12bit422to10bit444_encp module active high

Table 9-52 VPU_422TO444_CTRL0 0x274b

Bit(s)	R/W	Default	Description
31	R/W	0	bypass_mode : active high if this bit set high ,viu_12bit422to10bit444_encp work in bypass mode, dout = din
30	/	/	reversed
29	R/W	0	clip10_mode: active high if this bit set high ,viu_12bit422to10bit444_encp work clip10_mode ,output high 10bits value of din and clip data to 10bit,then expand to 12bits according clip_ lend.
28	R/W	0	Clip8_mode: active high if this bit set high ,viu_12bit422to10bit444_encp work clip8_mode ,output high 8bits value of din and clip data to 8bit,then expand to 12bits according clip_lend.
27	R/W	0	clip_lend :active high make output data to 12bits in clip10_mode/clip8_mode/scramble 1;expand bits in high bits 0: ;expand bits low bits
26	R/W	0	scramble_mode :active high viu_12bit422to10bit444_encp module get luma and chroma from 422 format data erery pixel ,then reorginize data to 8bits according to reg_tunnel value(this model can change data from 422 to 444??). Luma = din[35:24] Chroma =odd_pixel?din[23:12]:din[11:0]
25	R/W	0	go_field_en 1:rst odd_pixel to 0 when go_filed come
24	R/W	0	go_line_en 1:rst rst odd_pixel to 0 when go_line come
23	R/W	0	oft_rst_en 1:soft rst rst odd_pixel to 0
22	R/W	0	de_sel : input data de singal 1:chose encp require singal as de 0:close this module
17:15	R/W	0	reg_tunnel_sel_b1 : select high 4 bits for B from {luma,chroma} ,only work in scramble mode: 0:bit[3:0] 1:bit[7:3] 2:bit[11:8] 3:bit[15:12]

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Bit(s)	R/W	Default	Description
			4:bit[19:16] 5:bit[23:20] Default:bit[23:20]
14:12	R/W	0	reg_tunnel_sel_g1 : select high 4 bits for G from {luma,chroma} ,only work in scramble mode: 0:bit[3:0] 1:bit[7:3] 2:bit[11:8] 3:bit[15:12] 4:bit[19:16] 5:bit[23:20] Default:bit[23:20]
11:9	R/W	0	reg_tunnel_sel_r1 : select high 4 bits for R from {luma,chroma} ,only work in scramble mode: 0:bit[3:0] 1:bit[7:3] 2:bit[11:8] 3:bit[15:12] 4:bit[19:16] 5:bit[23:20] Default:bit[23:20]
8:6	R/W	0	reg_tunnel_sel_B0 : select low 4 bits for B from {luma,chroma} ,only work in scramble mode: 0:bit[3:0] 1:bit[7:3] 2:bit[11:8] 3:bit[15:12] 4:bit[19:16] 5:bit[23:20] Default:bit[23:20]
5:3	R/W	0	reg_tunnel_sel_g0 : select low 4 bits for G from {luma,chroma} ,only work in scramble mode: 0:bit[3:0] 1:bit[7:3] 2:bit[11:8] 3:bit[15:12] 4:bit[19:16] 5:bit[23:20] Default:bit[23:20]
2:0	R/W	0	reg_tunnel_sel_r0 : select low 4 bits for R from {luma,chroma} ,only work in scramble mode: 0:bit[3:0] 1:bit[7:3] 2:bit[11:8] 3:bit[15:12] 4:bit[19:16] 5:bit[23:20] Default:bit[23:20]

VPU_422TO444_CTRL1 0x274c Same as VPU_422TO444_CTRL0,viu_12bit422to10bit444_vd1

Table 9-53 VPU_VIU2VDIN_HDN_CTRL 0x2780

Bit(s)	R/W	Default	Description
20	R/W	0	software reset
19-18	R/W	0	reg_viu2vdin_dn_ratio: down-scale ratio: 0->no scale; 1-> 1/2; 2->1/4; 3->reserved
17-16	R/W	0	reg_viu2vdin_flt_mode: filter mode; 0->no filter; 1->[0 2 2 0]/4; 2->[1 1 1 1]/4; 3->[1 3 3 1]/8

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Bit(s)	R/W	Default	Description
15-14	R/W	0	reserved
13-0	R/W	0	reg_viu2vdin_hsize: source horizontal size

Table 9-54 VPU_VIU_ASYNC_MASK 0x2781

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:24	R/W	0	VDIN_STTs_data => VPP
23:20	R/W	0	Nr/di -> ldim
19-18	R/W	0	reg_viu2vdin_dn_ratio: down-scale ratio: 0->no scale; 1-> 1/2; 2->1/4; 3->reserved
11:8	R/W	0	Vpp afbc-> di pre inp
7:4	R/W	0	Mask vd1-> di post input
3:0	R/W	0	Mask di post => VPP_VD1_IN

Table 9-55 VPU_VDIN_MISC_CTRL 0x2782

Bit(s)	R/W	Default	Description
31:26	R/W	0	reserved
25-24	R/W	0	afbce gate clock ctrl
23	R/W	0	afbce_go_field & afbce_go_line select : 0:vdin 1:di
22	R/W	0	vdin_go_field & vdin_go_line select : 0:vdin0 1:vdin1
21	R/W	0	vdin0 output to afbc enc
20	R/W	0	vdin0 output to write mif
19	R/W	0	vdin0 output to mif enable
18	R/W	0	vdin1 output to afbc enc
17	R/W	0	vdin1 output to write mif
16	R/W	0	vdin1 output to mif enable
15	R/W	0	vdin line int enable
14-11	R/W	0	vdin arbiter gate clock ctrl
10	R/W	0	ldim stts data select : 0: vdin0 1:vdin1
9-8	R/W	0	vdin1 write mif fix disable
7-6	R/W	0	vdin0 write mif fix disable
4	R/W	0	Vdin1_wr_rst_n
3	R/W	0	Vdin0_wr_rst_n
2	R/W	0	Nrin_mux_wr_rst_n
1	R/W	0	Vdin1_rst_n
0	R/W	0	Vdin0_rst_n

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Table 9-56 VPU_VIU_VDIN_IF_MUX_CTRL 0x2783

Bit(s)	R/W	Default	Description
28-24	R/W	0	//Select VIU to “VDIN0/VDIN1 source 9” data path , must clear it first before changing the path sel //5’b00000= Disable VIU to VDIN path //5’b00001= Enble VIU of ENC_I domain to VDIN //5’b00010= Enble VIU of ENC_P domain to VDIN //5’b00100= Enble VIU of ENC_T domain to VDIN //5’b01000= Enble VIU WriteBack 1 domain to VDIN //5’b10000= Enble VIU WriteBack 2 domain to VDIN
20-16	R/W	0	//Select VIU Clock to “VDIN0/VDIN1 source 9” clk path , must clear it first before changing the path sel //5’b00000= Disable VIU to VDIN clock //5’b00001= Enble clock VIU of ENC_I domain to VDIN //5’b00010= Enble clock VIU of ENC_P domain to VDIN //5’b00100= Enble clock VIU of ENC_T domain to VDIN //5’b01000= Enble clock VIU WriteBack 1 domain to VDIN //5’b10000= Enble clock VIU WriteBack 2 domain to VDIN
12-8	R/W	0	//Select VIU to “VDIN0/VDIN1 source 7” data path , must clear it first before changing the path sel //5’b00000= Disable VIU to VDIN clock //5’b00001= Enble clock VIU of ENC_I domain to VDIN //5’b00010= Enble clock VIU of ENC_P domain to VDIN //5’b00100= Enble clock VIU of ENC_T domain to VDIN //5’b01000= Enble clock VIU WriteBack 1 domain to VDIN //5’b10000= Enble clock VIU WriteBack 2 domain to VDIN
4-0	R/W	0	//Select Clock to “VDIN0/VDIN1 source 7” , must clear it first before changing the path sel //5’b00000= Disable VIU to VDIN clock //5’b00001= Enble clock VIU of ENC_I domain to VDIN //5’b00010= Enble clock VIU of ENC_P domain to VDIN //5’b00100= Enble clock VIU of ENC_T domain to VDIN //5’b01000= Enble clock VIU WriteBack 1 domain to VDIN //5’b10000= Enble clock VIU WriteBack 2 domain to VDIN

Table 9-57 VPU_VIU2VDIN1_HDN_CTRL 0x2784

Bit(s)	R/W	Default	Description
20	R/W	0	software reset
19-18	R/W	0	reg_viu2vdin2_dn_ratio: down-scale ratio: 0->no scale; 1-> 1/2; 2->1/4; 3->reserved
17-16	R/W	0	reg_viu2vdin2_flt_mode: filter mode; 0->no filter; 1->[0 2 2 0]/4; 2->[1 1 1 1]/4; 3->[1 3 3 1]/8
15-14	R/W	0	reserved
13-0	R/W	0	reg_viu2vdin2_hsize: source horizontal size

Table 9-58 VPU_VENCX_CLK_CTRL 0x2785

Bit(s)	R/W	Default	Description
2	R/W	0	Enci_afifo_clk: 0: cts_vpu_clk_tm 1: cts_vpu_clkc_tm
1	R/W	0	Encl_afifo_clk: 0: cts_vpu_clk_tm 1: cts_vpu_clkc_tm
0	R/W	0	Encp_afifo_clk: 0: cts_vpu_clk_tm 1: cts_vpu_clkc_tm

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Table 9-59 VPU_RDARB_MODE_L1C1 0x2790

Bit(s)	R/W	Default	Description
21:16	R/W	0	rdarb_sel : uns, default = 0 , rdarb_sel [0]==0 slave dc0 connect master port0 rdarb_sel[0]==1 slave dc0 connect master port1 rdarb_sel [1]==0 slave dc1 connect master port0 rdarb_sel[1]==1 slave dc1 connect master port1 rdarb_sel [2]==0 slave dc2 connect master port0 rdarb_sel[2]==1 slave dc2 connect master port1 rdarb_sel [3]==0 slave dc3 connect master port0 rdarb_sel[3]==1 slave dc3 connect master port1 rdarb_sel [4]==0 slave dc4 connect master port0 rdarb_sel[4]==1 slave dc4 connect master port1 rdarb_sel [5]==0 slave dc5 connect master port0 rdarb_sel[5]==1 slave dc5 connect master port1
9:8	R/W	0	rdarb_arb_mode : uns, default = 0 , rdarb_arb_mode [0] master port0 arb way, rdarb_arb_mode [1] master port1 arb way,
3:0	R/W	0	rdarb_gate_clk_ctrl : uns, default = 0 , rdarb_gate_clk_ctrl [1:0] master port0 clk gate control rdarb_gate_clk_ctrl [3:2] master port1 clk gate control

Table 9-60 VPU_RDARB_REQEN_SLV_L1C1 0x2791

Bit(s)	R/W	Default	Description
11:0	R/W	0xfff	rdarb_dc_req_en : unsigned , default = 12'hfff rdarb_dc_req_en [0]: the slv0 req to mst port0 enable, rdarb_dc_req_en [1]: the slv1 req to mst port0 enable, rdarb_dc_req_en [2]: the slv2 req to mst port0 enable, rdarb_dc_req_en [3]: the slv3 req to mst port0 enable, rdarb_dc_req_en [4]: the slv4 req to mst port0 enable, rdarb_dc_req_en [5]: the slv5 req to mst port0 enable, rdarb_dc_req_en [6]: the slv0 req to mst port1 enable, rdarb_dc_req_en [7]: the slv1 req to mst port1 enable, rdarb_dc_req_en [8]: the slv2 req to mst port1 enable, rdarb_dc_req_en [9]: the slv3 req to mst port1 enable, rdarb_dc_req_en [10]: the slv4 req to mst port1 enable, rdarb_dc_req_en [11]: the slv5 req to mst port1 enable,

Table 9-61 VPU_RDARB_WEIGH0_SLV_L1C1 0x2792

Bit(s)	R/W	Default	Description
29:0	R/W	0	rddc_weigh_sxn : unsigned , default = 0 rddc_weigh_sxn [0*6+:6]: the slv0 req weigh number rddc_weigh_sxn [1*6+:6]: the slv1 req weigh number rddc_weigh_sxn [2*6+:6]: the slv2 req weigh number rddc_weigh_sxn [3*6+:6]: the slv3 req weigh number rddc_weigh_sxn [4*6+:6]: the slv4 req weigh number

Table 9-62 VPU_RDARB_WEIGH1_SLV_L1C1 0x2793

Bit(s)	R/W	Default	Description
5:0	R/W	0	rddc_weigh_sxn : unsigned , default = 0 rddc_weigh_sxn [5*6+:6]: the slv5 req weigh number

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Table 9-63 VPU_WRARB_MODE_L1C1 0x2794

Bit(s)	R/W	Default	Description
21:16	R/W	0	wrarb_sel : uns, default = 0 , wrarb_sel [0]==0 slave dc0 connect master port0 wrarb_sel[0]==1 slave dc0 connect master port1 wrarb_sel [1]==0 slave dc1 connect master port0 wrarb_sel[1]==1 slave dc1 connect master port1 wrarb_sel [2]==0 slave dc2 connect master port0 wrarb_sel[2]==1 slave dc2 connect master port1 wrarb_sel [3]==0 slave dc3 connect master port0 wrarb_sel[3]==1 slave dc3 connect master port1 wrarb_sel [4]==0 slave dc4 connect master port0 wrarb_sel[4]==1 slave dc4 connect master port1 wrarb_sel [5]==0 slave dc5 connect master port0 wrarb_sel[5]==1 slave dc5 connect master port1
9:8	R/W	0	wrarb_arb_mode : uns, default = 0 , wrarb_arb_mode [0] master port0 arb way, wrarb_arb_mode [1] master port1 arb way,
3:0	R/W	0	wrarb_gate_clk_ctrl : uns, default = 0 , wrarb_gate_clk_ctrl [1:0] master port0 clk gate control wrarb_gate_clk_ctrl [3:2] master port1 clk gate control

Table 9-64 VPU_WRARB_REQEN_SLV_L1C1 0x2795

Bit(s)	R/W	Default	Description
11:0	R/W	0	wrarb_dc_req_en : unsigned , default = 0 wrarb_dc_req_en [0]: the slv0 req to mst port0 enable, wrarb_dc_req_en [1]: the slv1 req to mst port0 enable, wrarb_dc_req_en [2]: the slv2 req to mst port0 enable, wrarb_dc_req_en [3]: the slv3 req to mst port0 enable, wrarb_dc_req_en [4]: the slv4 req to mst port0 enable, wrarb_dc_req_en [5]: the slv5 req to mst port0 enable, wrarb_dc_req_en [0]: the slv0 req to mst port1 enable, wrarb_dc_req_en [1]: the slv1 req to mst port1 enable, wrarb_dc_req_en [2]: the slv2 req to mst port1 enable, wrarb_dc_req_en [3]: the slv3 req to mst port1 enable, wrarb_dc_req_en [4]: the slv4 req to mst port1 enable, wrarb_dc_req_en [5]: the slv5 req to mst port1 enable,

Table 9-65 VPU_WRARB_WEIGH0_SLV_L1C1 0x2796

Bit(s)	R/W	Default	Description
29:0	R/W	0	wrdc_weigh_sxn : unsigned , default = 0 wrdc_weigh_sxn [0*6+:6]: the slv0 req weigh number wrdc_weigh_sxn [1*6+:6]: the slv1 req weigh number wrdc_weigh_sxn [2*6+:6]: the slv2 req weigh number wrdc_weigh_sxn [3*6+:6]: the slv3 req weigh number wrdc_weigh_sxn [4*6+:6]: the slv4 req weigh number

Table 9-66 VPU_WRARB_WEIGH1_SLV_L1C1 0x2797

Bit(s)	R/W	Default	Description
5:0	R/W	0	wrdc_weigh_sxn : unsigned , default = 0 wrdc_weigh_sxn [5*6+:6]: the slv5 req weigh number

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Table 9-67 VPU_RDWR_ARB_STATUS_L1C1 0x2798

Bit(s)	R/W	Default	Description
3:2	R/W	0	wrarb_arb_busy : unsigned , default = 0
1:0	R/W	0	rdarb_arb_busy : unsigned , default = 0

Table 9-68 VPU_RDARB_MODE_L1C2 0x2799

Bit(s)	R/W	Default	Description
20:16	R/W	0	rdarb_sel : uns, default = 0 , rdarb_sel [0]==0 slave dc0 connect master port0 rdarb_sel[0]==1 slave dc0 connect master port1 rdarb_sel [1]==0 slave dc1 connect master port0 rdarb_sel[1]==1 slave dc1 connect master port1 rdarb_sel [2]==0 slave dc2 connect master port0 rdarb_sel[2]==1 slave dc2 connect master port1 rdarb_sel [3]==0 slave dc3 connect master port0 rdarb_sel[3]==1 slave dc3 connect master port1 rdarb_sel [4]==0 slave dc4 connect master port0 rdarb_sel[4]==1 slave dc4 connect master port1
9:8	R/W	0	rdarb_arb_mode : uns, default = 0 , rdarb_arb_mode [0] master port0 arb way, rdarb_arb_mode [1] master port1 arb way,
3:0	R/W	0	rdarb_gate_clk_ctrl : uns, default = 0 , rdarb_gate_clk_ctrl [1:0] master port0 clk gate control rdarb_gate_clk_ctrl [3:2] master port0 clk gate control

Table 9-69 VPU_RDARB_REQEN_SLV_L1C2 0x279a

Bit(s)	R/W	Default	Description
9:0	R/W	0	rdarb_dc_req_en : unsigned , default = 0 rdarb_dc_req_en [0]: the slv0 req to mst port0 enable, rdarb_dc_req_en [1]: the slv1 req to mst port0 enable, rdarb_dc_req_en [2]: the slv2 req to mst port0 enable, rdarb_dc_req_en [3]: the slv3 req to mst port0 enable, rdarb_dc_req_en [4]: the slv4 req to mst port0 enable, rdarb_dc_req_en [5]: the slv0 req to mst port1 enable, rdarb_dc_req_en [6]: the slv1 req to mst port1 enable, rdarb_dc_req_en [7]: the slv2 req to mst port1 enable, rdarb_dc_req_en [8]: the slv3 req to mst port1 enable, rdarb_dc_req_en [9]: the slv4 req to mst port1 enable,

Table 9-70 VPU_RDARB_WEIGH0_SLV_L1C2 0x279b

Bit(s)	R/W	Default	Description
29:0	R/W	0	rddc_weigh_sxn : unsigned , default = 0 rddc_weigh_sxn [0*6+:6]: the slv0 req weigh number rddc_weigh_sxn [1*6+:6]: the slv1 req weigh number rddc_weigh_sxn [2*6+:6]: the slv2 req weigh number rddc_weigh_sxn [3*6+:6]: the slv3 req weigh number rddc_weigh_sxn [4*6+:6]: the slv4 req weigh number

Table 9-71 VPU_RDWR_ARB_STATUS_L1C2 0x279c

Bit(s)	R/W	Default	Description
1:0	R/W	0	rdarb_arb_busy : unsigned , default = 0

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Table 9-72 VPU_RDARB_MODE_L2C1 0x279d

Bit(s)	R/W	Default	Description
27:16	R/W	0	rdarb_sel : uns, default = 0 , rdarb_sel [0]==0 slave dc0 connect master port0 rdarb_sel[0]==1 slave dc0 connect master port1 rdarb_sel [1]==0 slave dc1 connect master port0 rdarb_sel[1]==1 slave dc1 connect master port1 rdarb_sel [2]==0 slave dc2 connect master port0 rdarb_sel[2]==1 slave dc2 connect master port1 rdarb_sel [3]==0 slave dc3 connect master port0 rdarb_sel[3]==1 slave dc3 connect master port1 rdarb_sel [4]==0 slave dc4 connect master port0 rdarb_sel[4]==1 slave dc4 connect master port1 rdarb_sel [5]==0 slave dc5 connect master port0 rdarb_sel[5]==1 slave dc5 connect master port1
10:8	R/W	0	rdarb_arb_mode : uns, default = 0 , rdarb_arb_mode [0] master port0 arb way, rdarb_arb_mode [1] master port1 arb way,
5:0	R/W	0	rdarb_gate_clk_ctrl : uns, default = 0 , rdarb_gate_clk_ctrl [1:0] master port0 clk gate control rdarb_gate_clk_ctrl [3:2] master port1 clk gate control rdarb_gate_clk_ctrl [5:4] master port2 clk gate control

Table 9-73 VPU_RDARB_REQEN_SLV_L2C1 0x279e

Bit(s)	R/W	Default	Description
17:0	R/W	0	rdarb_dc_req_en : unsigned , default = 0 rdarb_dc_req_en [0]: the slv0 req to mst port0 enable, rdarb_dc_req_en [1]: the slv1 req to mst port0 enable, rdarb_dc_req_en [2]: the slv2 req to mst port0 enable, rdarb_dc_req_en [3]: the slv3 req to mst port0 enable, rdarb_dc_req_en [4]: the slv4 req to mst port0 enable, rdarb_dc_req_en [5]: the slv5 req to mst port0 enable, rdarb_dc_req_en [0]: the slv0 req to mst port1 enable, rdarb_dc_req_en [1]: the slv1 req to mst port1 enable, rdarb_dc_req_en [2]: the slv2 req to mst port1 enable, rdarb_dc_req_en [3]: the slv3 req to mst port1 enable, rdarb_dc_req_en [4]: the slv4 req to mst port1 enable, rdarb_dc_req_en [5]: the slv5 req to mst port1 enable,

Table 9-74 VPU_RDARB_WEIGH0_SLV_L2C1 0x279f

Bit(s)	R/W	Default	Description
29:0	R/W	0	rddc_weigh_sxn : unsigned , default = 0 rddc_weigh_sxn [0*6+:6]: the slv0 req weigh number rddc_weigh_sxn [1*6+:6]: the slv1 req weigh number rddc_weigh_sxn [2*6+:6]: the slv2 req weigh number rddc_weigh_sxn [3*6+:6]: the slv3 req weigh number rddc_weigh_sxn [4*6+:6]: the slv4 req weigh number

Table 9-75 VPU_RDARB_WEIGH1_SLV_L2C1 0x27a0

Bit(s)	R/W	Default	Description
5:0	R/W	0	rddc_weigh_sxn : unsigned , default = 0 rddc_weigh_sxn [5*6+:6]: the slv5 req weigh number

Table 9-76 VPU_RDWR_ARB_STATUS_L2C1 0x27a1

Bit(s)	R/W	Default	Description
3:2	R/W	0	wrarb_arb_busy : unsigned , default = 0
1:0	R/W	0	rdarb_arb_busy : unsigned , default = 0

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Table 9-77 VPU_WRARB_MODE_L2C1 0x27a2

Bit(s)	R/W	Default	Description
19:16	R/W	0	wrarb_sel : uns, default = 0 , wrarb_sel [0]==0 slave dc0 connect master port0 wrarb_sel[0]==1 slave dc0 connect master port1 wrarb_sel [1]==0 slave dc1 connect master port0 wrarb_sel[1]==1 slave dc1 connect master port1 wrarb_sel [2]==0 slave dc2 connect master port0 wrarb_sel[2]==1 slave dc2 connect master port1 wrarb_sel [3]==0 slave dc3 connect master port0 wrarb_sel[3]==1 slave dc3 connect master port1
9:8	R/W	0	wrarb_arb_mode : uns, default = 0 , wrarb_arb_mode [0] master port0 arb way, wrarb_arb_mode [1] master port1 arb way,
3:0	R/W	0	wrarb_gate_clk_ctrl : uns, default = 0 , wrarb_gate_clk_ctrl [1:0] master port0 clk gate control wrarb_gate_clk_ctrl [3:2] master port0 clk gate control

Table 9-78 VPU_WRARB_REQEN_SLV_L2C1 0x27a3

Bit(s)	R/W	Default	Description
7:0	R/W	0	wrarb_dc_req_en : unsigned , default = 0 wrarb_dc_req_en [0]: the slv0 req to mst port0 enable, wrarb_dc_req_en [1]: the slv1 req to mst port0 enable, wrarb_dc_req_en [2]: the slv2 req to mst port0 enable, wrarb_dc_req_en [3]: the slv3 req to mst port0 enable, wrarb_dc_req_en [0]: the slv0 req to mst port1 enable, wrarb_dc_req_en [1]: the slv1 req to mst port1 enable, wrarb_dc_req_en [2]: the slv2 req to mst port1 enable, wrarb_dc_req_en [3]: the slv3 req to mst port1 enable,

Table 9-79 VPU_WRARB_WEIGH0_SLV_L2C1 0x27a4

Bit(s)	R/W	Default	Description
23:0	R/W	0	wrdc_weigh_sxn : unsigned , default = 0 wrdc_weigh_sxn [0*6+:6]: the slv0 req weigh number wrdc_weigh_sxn [1*6+:6]: the slv1 req weigh number wrdc_weigh_sxn [2*6+:6]: the slv2 req weigh number wrdc_weigh_sxn [3*6+:6]: the slv3 req weigh number

Table 9-80 VPU_ASYNC_RD_MODE0 0x27a5

Bit(s)	R/W	Default	Description
18	R/W	0	req_en : unsigned , default = 0 async enable
17:16	R/W	0	clk_gate_ctrl : unsigned , default = 0 async clock gate control
15:12	R/W	4	auto_arugt_weight : unsigned , default = 4
10:9	R/W	0	arugt_sel : unsigned , default = 0 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 00 : use the input arguent
8	R/W	0	arguent_cfg : unsigned , default = 0 register arguent control bit
7:4	R/W	4	rd_hold_num : unsigned , default = 4 hold the read command threshold
3:0	R/W	0	rd_rel_num : unsigned , default = 0 release the read command threshold

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Table 9-81 VPU_ASYNC_RD_MODE1 0x27a6

Bit(s)	R/W	Default	Description
18	R/W	0	req_en : unsigned , default = 0 async enable
17:16	R/W	0	clk_gate_ctrl : unsigned , default = 0 async clock gate control
15:12	R/W	4	auto_arugt_weight : unsigned , default = 4
10:9	R/W	0	arugt_sel : unsigned , default = 0 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 00 : use the input arguent
8	R/W	0	arguent_cfg : unsigned , default = 0 register arguent control bit
7:4	R/W	4	rd_hold_num : unsigned , default = 4 hold the read command threshold
3:0	R/W	0	rd_rel_num : unsigned , default = 0 release the read command threshold

Table 9-82 VPU_ASYNC_RD_MODE2 0x27a7

Bit(s)	R/W	Default	Description
18	R/W	0	req_en : unsigned , default = 0 async enable
17:16	R/W	0	clk_gate_ctrl : unsigned , default = 0 async clock gate control
15:12	R/W	4	auto_arugt_weight : unsigned , default = 4
10:9	R/W	0	arugt_sel : unsigned , default = 0 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 00 : use the input arguent
8	R/W	0	arguent_cfg : unsigned , default = 0 register arguent control bit
7:4	R/W	4	rd_hold_num : unsigned , default = 4 hold the read command threshold
3:0	R/W	0	rd_rel_num : unsigned , default = 0 release the read command threshold

Table 9-83 VPU_ASYNC_RD_MODE3 0x27a8

Bit(s)	R/W	Default	Description
18	R/W	0	req_en : unsigned , default = 0 async enable
17:16	R/W	0	clk_gate_ctrl : unsigned , default = 0 async clock gate control
15:12	R/W	4	auto_arugt_weight : unsigned , default = 4
10:9	R/W	0	arugt_sel : unsigned , default = 0 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 00 : use the input arguent
8	R/W	0	arguent_cfg : unsigned , default = 0 register arguent control bit
7:4	R/W	4	rd_hold_num : unsigned , default = 4 hold the read command threshold
3:0	R/W	0	rd_rel_num : unsigned , default = 0 release the read command threshold

Table 9-84 VPU_ASYNC_RD_MODE4 0x27a9

Bit(s)	R/W	Default	Description
18	R/W	0	req_en : unsigned , default = 0 async enable
17:16	R/W	0	clk_gate_ctrl : unsigned , default = 0 async clock gate control

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Bit(s)	R/W	Default	Description
15:12	R/W	4	auto_arugt_weight : unsigned , default = 4
10:9	R/W	0	arugt_sel : unsigned , default = 0 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 00 : use the input arguent
8	R/W	0	arguent_cfg : unsigned , default = 0 register arguent control bit
7:4	R/W	4	rd_hold_num : unsigned , default = 4 hold the read command threshold
3:0	R/W	0	rd_rel_num : unsigned , default = 0 release the read command threshold

Table 9-85 VPU_ASYNC_WR_MODE0 0x27aa

Bit(s)	R/W	Default	Description
18	R/W	0	req_en : unsigned , default = 0 async enable
17:16	R/W	0	clk_gate_ctrl : unsigned , default = 0 async clock gate control
15:12	R/W	4	auto_arugt_weight : unsigned , default = 4
10:9	R/W	0	arugt_sel : unsigned , default = 0 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 00 : use the input arguent
8	R/W	0	arguent_cfg : unsigned , default = 0 register arguent control bit
7:4	R/W	4	wr_hold_num : unsigned , default = 4 hold the read command threshold
3:0	R/W	0	wr_rel_num : unsigned , default = 0 release the write command threshold

Table 9-86 VPU_ASYNC_WR_MODE1 0x27ab

Bit(s)	R/W	Default	Description
18	R/W	0	req_en : unsigned , default = 0 async enable
17:16	R/W	0	clk_gate_ctrl : unsigned , default = 0 async clock gate control
15:12	R/W	4	auto_arugt_weight : unsigned , default = 4
10:9	R/W	0	arugt_sel : unsigned , default = 0 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 00 : use the input arguent
8	R/W	0	arguent_cfg : unsigned , default = 0 register arguent control bit
7:4	R/W	4	wr_hold_num : unsigned , default = 4 hold the read command threshold
3:0	R/W	0	wr_rel_num : unsigned , default = 0 release the write command threshold

Table 9-87 VPU_ASYNC_WR_MODE2 0x27ac

Bit(s)	R/W	Default	Description
18	R/W	0	req_en : unsigned , default = 0 async enable
17:16	R/W	0	clk_gate_ctrl : unsigned , default = 0 async clock gate control
15:12	R/W	4	auto_arugt_weight : unsigned , default = 4
10:9	R/W	0	arugt_sel : unsigned , default = 0 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 00 : use the input arguent
8	R/W	0	arguent_cfg : unsigned , default = 0 register arguent control bit

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Bit(s)	R/W	Default	Description
7:4	R/W	4	wr_hold_num : unsigned , default = 4 hold the read command threshold
3:0	R/W	0	wr_rel_num : unsigned , default = 0 release the write command threshold

Table 9-88 VPU_ASYNC_STAT 0x27ad

Bit(s)	R/W	Default	Description
18	R/W	0x0	axiwr2_chan_idle : unsigned , RO, axi write channel2 idle state
17	R/W	0x0	axiwr1_chan_idle : unsigned , RO, axi write channel1 idle state
16	R/W	0x0	axiwr0_chan_idle : unsigned , RO, axi write channel0 idle state
4	R/W	0x0	axird4_chan_idle : unsigned , RO, axi read channel4 idle state
3	R/W	0x0	axird3_chan_idle : unsigned , RO, axi read channel3 idle state
2	R/W	0x0	axird2_chan_idle : unsigned , RO, axi read channel2 idle state
1	R/W	0x0	axird1_chan_idle : unsigned , RO, axi read channel1 idle state
0	R/W	0x0	axird0_chan_idle : unsigned , RO, axi read channel0 idle state

Table 9-89 VPU_HDMI_DITH_01_04 0x27f0

Bit(s)	R/W	Default	Description
31-0	R/W	0x8214_1428	dith lut VPU_HDMI_DITH_CNTL[0] : 1 : lut for 10b to 8b 0 : lut for 12b to 10b

Table 9-90 VPU_HDMI_DITH_01_15 0x27f1

Bit(s)	R/W	Default	Description
31-0	R/W	0x4128_2841	dith lut VPU_HDMI_DITH_CNTL[0] : 1 : lut for 10b to 8b 0 : lut for 12b to 10b

Table 9-91 VPU_HDMI_DITH_01_26 0x27f2

Bit(s)	R/W	Default	Description
31-0	R/W	0x2841_4182	dith lut VPU_HDMI_DITH_CNTL[0] : 1 : lut for 10b to 8b 0 : lut for 12b to 10b

Table 9-92 VPU_HDMI_DITH_01_37 0x27f3

Bit(s)	R/W	Default	Description
31-0	R/W	0x1482_8214	dith lut VPU_HDMI_DITH_CNTL[0] : 1 : lut for 10b to 8b 0 : lut for 12b to 10b

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Table 9-93 VPU_HDMI_DITH_10_04 0x27f4

Bit(s)	R/W	Default	Description
31-0	R/W	0x9669_9696	dith lut VPU_HDMI_DITH_CNTL[0] : 1 : lut for 10b to 8b 0 : lut for 12b to 10b

Table 9-94 VPU_HDMI_DITH_10_15 0x27f5

Bit(s)	R/W	Default	Description
31-0	R/W	0x3c3c_6969	dith lut VPU_HDMI_DITH_CNTL[0] : 1 : lut for 10b to 8b 0 : lut for 12b to 10b

Table 9-95 VPU_HDMI_DITH_10_26 0x27f6

Bit(s)	R/W	Default	Description
31-0	R/W	0x6996_9696	dith lut VPU_HDMI_DITH_CNTL[0] : 1 : lut for 10b to 8b 0 : lut for 12b to 10b

Table 9-96 VPU_HDMI_DITH_10_37 0x27f7

Bit(s)	R/W	Default	Description
31-0	R/W	0xc3c3_6969	dith lut VPU_HDMI_DITH_CNTL[0] : 1 : lut for 10b to 8b 0 : lut for 12b to 10b

Table 9-97 VPU_HDMI_DITH_11_04 0x27f8

Bit(s)	R/W	Default	Description
31-0	R/W	0x7deb_ebd7	dith lut VPU_HDMI_DITH_CNTL[0] : 1 : lut for 10b to 8b 0 : lut for 12b to 10b

Table 9-98 VPU_HDMI_DITH_11_15 0x27f9

Bit(s)	R/W	Default	Description
31-0	R/W	0xbed7_d7be	dith lut VPU_HDMI_DITH_CNTL[0] : 1 : lut for 10b to 8b 0 : lut for 12b to 10b

Table 9-99 VPU_HDMI_DITH_11_26 0x27fa

Bit(s)	R/W	Default	Description
31-0	R/W	0xd7be_be7d	dith lut VPU_HDMI_DITH_CNTL[0] : 1 : lut for 10b to 8b 0 : lut for 12b to 10b

Table 9-100 VPU_HDMI_DITH_11_37 0x27fb

Bit(s)	R/W	Default	Description
31-0	R/W	0xeb7d_7deb	dith lut VPU_HDMI_DITH_CNTL[0] : 1 : lut for 10b to 8b 0 : lut for 12b to 10b

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Table 9-101 VPU_HDMI_DITH_CNTL 0x27fc

Bit(s)	R/W	Default	Description
10b to 8b dither control register. 12b to 10b see VPU_HDMI_FMT_CTRL			
21-19	R/W	0	rame count offset for B
18-16	R/W	0	frame count offset for G
15	R/W	0	hcnt hold when de valid
14	R/W	0	RGB frame count seperate
13	R/W	0	dith4x4 : frame random enable
12	R/W	0	dith4x4 enable
11	R/W	0	tunnel enable for DOLBY
10	R/W	0	rounding enable
9-6	R/W	0	Cntl_hdmi_dith10 :
5	R/W	0	Cntl_hdmi_dith_md:
4	R/W	0	Cntl_hdmi_dith_en: dither 10-b to 8-b enable
3	R/W	0	hsync invert
2	R/W	0	vsync invert
0	R/W	0	dither lut sel : 1 : sel 10b to 8b 0: sel 12b to 10b

Table 9-102 VPU_VENCL_DITH_CTRL 0x27e0

Bit(s)	R/W	Default	Description
19-17	R/W	0	dither 2x2 : frame number sel
16	R/W	0	dither 2x2 : frame number random
15-14	R/W	0	Reserved
13-11	R/W	7	G frame number offset
10-8	R/W	3	B frame number offset
7	R/W	0	Reserved
6	R/W	1	dither 4x4 : G/B frame number = B frame number + offset g/b
5	R/W	0	dither 4x4 : frame number random
4	R/W	1	dither 4x4 : enable
3	R/W	0	Reserved
2	R/W	0	dither md
1	R/W	0	rounding enable
0	R/W	1	dither enable

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Table 9-103 VPU_VENCL_DITH_LUT_1 0x27e1

Bit(s)	R/W	Default	Description
31-0	R/W	0x8214_1428	dith lut

Table 9-104 VPU_VENCL_DITH_LUT_2 0x27e2

Bit(s)	R/W	Default	Description
31-0	R/W	0x4128_2841	dith lut

Table 9-105 VPU_VENCL_DITH_LUT_3 0x27e3

Bit(s)	R/W	Default	Description
31-0	R/W	0x2841_4182	dith lut

Table 9-106 VPU_VENCL_DITH_LUT_4 0x27e4

Bit(s)	R/W	Default	Description
31-0	R/W	0x1482_8214	dith lut

Table 9-107 VPU_VENCL_DITH_LUT_5 0x27e5

Bit(s)	R/W	Default	Description
31-0	R/W	0x9669_9696	dith lut

Table 9-108 VPU_VENCL_DITH_LUT_6 0x27e6

Bit(s)	R/W	Default	Description
31-0	R/W	0x3c3c_6969	dith lut

Table 9-109 VPU_VENCL_DITH_LUT_7 0x27e7

Bit(s)	R/W	Default	Description
31-0	R/W	0x6996_9696	dith lut

Table 9-110 VPU_VENCL_DITH_LUT_8 0x27e8

Bit(s)	R/W	Default	Description
31-0	R/W	0xc3c3_6969	dith lut

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Table 9-111 VPU_VENCL_DITH_LUT_9 0x27e9

Bit(s)	R/W	Default	Description
31-0	R/W	0x7deb_ebd7	dith lut

Table 9-112 VPU_VENCL_DITH_LUT_10 0x27ea

Bit(s)	R/W	Default	Description
31-0	R/W	0xbed7_d7be	dith lut

Table 9-113 VPU_VENCL_DITH_LUT_11 0x27eb

Bit(s)	R/W	Default	Description
31-0	R/W	0xd7be_be7d	dith lut

Table 9-114 VPU_VENCL_DITH_LUT_12 0x27ec

Bit(s)	R/W	Default	Description
31-0	R/W	0xeb7d_7deb	dith lut

9.2.3.2 VPU Video Lock Registers

Table 9-115 VPU_VLOCK_CTRL 0x3000

Bit(s)	R/W	Default	Description
31	R/W	0x0	Vid_lock_en: 1: enable video lock module
30	R/W	0x0	Reg_adj_enc: enable video lock to adjust encoder
29	R/W	0x0	Adj_pll: enable video lock to adjust PLL
28	R/W	0x0	Mpeg_vs: set this to 1, then 0, this is software controlled mpeg vsync
27-26	R/W	0x0	Output goes to which module: 0: encl, 1: encp, 2:enci
25-20	R/W	0x0	Output vsync width extend: make sure the vsync width is extended big enough for vpu_vid_lock_clk to sample
19	R/W	0x0	m frac right shift 1 : right shift 2 bit 0 : no shift
18-16	R/W	0x0	Input Vsync source select: 0: unuse, 1: fromhdmi rx , 2:from tv-decoder, 3: from dvin, 4: from dvin, 5: from 2nd bt656
15			Output vsync invert: 1, invert
14			Input vsync invert: 1, invert
13-8	R/W		Input vsync width extend: make sure the vsync width is extended big enough for vpu_vid_lock_clk to sample
7			Force loop1 err enable: 1. Force error of loop1

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Bit(s)	R/W	Default	Description
6			Force loop0 err enable: 1. Force error of loop0
5			Overwrite accum0 enable
4			Loop0 adjust capture enable
3			Loop0 adjust pll enable
2			Overwrite accum1 enable
1			Loop1 adjust capture enable
0			Loop0 adjust pll enable

Table 9-116 VPU_VLOCK_MISC_CTRL 0x3001

Bit(s)	R/W	Default	Description
28	R/W	0x0	for interlace : get average of every two input vsync
26-24	R/W	0x0	Adj_capt_pxgrouprs, make sure the pixel number in one line of encoder is multiples of 2^pxgrouprs
23-16	R/W	0x0	Ifrm_cnt_mod: (output vsync freq)/(input vsync_freq * ifrm_cnt_mod) must be integer
15-8	R/W	0x0	Output vsync frequency
7-0	R/W	0x0	Input vsync frequency

Table 9-117 VPU_VLOCK_LOOP0_ACCUM_LMT 0x3002

Bit(s)	R/W	Default	Description
26-0	R/W	0x0	LOOP0 accumulator limit

Table 9-118 VPU_VLOCK_LOOP0_CTRL0 0x3003

Bit(s)	R/W	Default	Description
31-24	R/W	0x0	Loop0 errclip rate
23-20	R/W	0x0	Loop0_adj_pll_rs, right shift of loop0 adjust pll portion
19-12	R/W	0x0	Loop0_adj_pll_gain, u1.7
11-8	R/W	0x0	Loop0_adj_capt_rs, right shift of loop0 adjust capture portion
7-0	R/W	0x0	Loop0_adj_capt_gain

Table 9-119 VPU_VLOCK_LOOP0_CTRL1 0x3004

Bit(s)	R/W	Default	Description
23-20	R/W	0x0	Loop1_adj_pll_rs
19-12	R/W	0x0	Loop1_adj_pll_gain
11-8	R/W	0x0	Loop1_adj_capt_rs
7-0	R/W	0x0	Loop1_adj_capt_gain

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Table 9-120 VPU_VLOCK_LOOP1_IMISSYNC_MAX 0x3005

Bit(s)	R/W	Default	Description
27-0	R/W	0x0	Loop1 imissync max, input signal is missed after input vsync counter is larger than this max threshold

Table 9-121 VPU_VLOCK_LOOP1_IMISSYNC_MIN 0x3006

Bit(s)	R/W	Default	Description
27-0	R/W	0x0	Loop1 imissync min, input signal is missed after input vsync counter is less than this max threshold

Table 9-122 VPU_VLOCK_OVERWRITE_ACCUM0 0x3007

Bit(s)	R/W	Default	Description
27-0	R/W	0x0	Overwrite value of accum0

Table 9-123 VPU_VLOCK_OVERWRITE_ACCUM1 0x3008

Bit(s)	R/W	Default	Description
27-0	R/W	0x0	Overwrite value of accum1

Table 9-124 VPU_VLOCK_OUTPUT0_CAPT_LMT 0x3009

Bit(s)	R/W	Default	Description
26-0	R/W	0x0	Output0 capture limit

Table 9-125 VPU_VLOCK_OUTPUT0_PLL_LMT 0x300a

Bit(s)	R/W	Default	Description
26-0	R/W	0x0	Output0 pll limit

Table 9-126 VPU_VLOCK_OUTPUT1_CAPT_LMT 0x300b

Bit(s)	R/W	Default	Description
26-0	R/W	0x0	Output1 capture limit

Table 9-127 VPU_VLOCK_OUTPUT1_PLL_LMT 0x300c

Bit(s)	R/W	Default	Description
26-0	R/W	0x0	Output1 pll limit

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Table 9-128 VPU_VLOCK_LOOP1_PHSDIF_TARGET 0x300d

Bit(s)	R/W	Default	Description
27-0	R/W	0x0	Loop1 phase difference target, (input vsync - output vsync) phase distance target

Table 9-129 VPU_VLOCK_RO_LOOP0_ACCUM 0x300e

Bit(s)	R/W	Default	Description
27-0	R	0x0	Read only, loop0 accum result

Table 9-130 VPU_VLOCK_RO_LOOP1_ACCUM 0x300f

Bit(s)	R/W	Default	Description
27-0	R	0x0	Read only, loop1 accum result

Table 9-131 VPU_VLOCK_OROW_OCOL_MAX 0x3010

Bit(s)	R/W	Default	Description
29-16	R/W	0x0	Ocol_max
13-0	R/W	0x0	Orow_max

Table 9-132 VPU_VLOCK_RO_VS_I_D 0x3011

Bit(s)	R/W	Default	Description
27-0	R	0x0	Read only, input vsync counter

Table 9-133 VPU_VLOCK_RO_VS_O_D 0x3012

Bit(s)	R/W	Default	Description
27-0	R	0x0	Read only, output vsync counter

Table 9-134 VPU_VLOCK_RO_LINE_PIX_ADJ 0x3013

Bit(s)	R/W	Default	Description
29-16	R	0x0	Read only, encoder line adjust number
13-0	R	0x0	Read only, encoder pix adjust number

Table 9-135 VPU_VLOCK_RO_OUTPUT_00_01 0x3014

Bit(s)	R/W	Default	Description
31-16	R	0x0	Read only, accum0 output 00
15-0	R	0x0	Read only, accum0 output 01

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Table 9-136 VPU_VLOCK_RO_OUTPUT_10_11 0x3015

Bit(s)	R/W	Default	Description
31-16	R	0x0	Read only, accum1 output 10
15-0	R	0x0	Read only, accum1 output 11

Table 9-137 VPU_VLOCK_MX4096 0x3016

Bit(s)	R/W	Default	Description
20-0	R/W	0x0	Mx4096

Table 9-138 VPU_VLOCK_STBDET_WIN0_WIN1 0x3017

Bit(s)	R/W	Default	Description
15-8	R/W	0x0	Verr_stbdet_win1
7-0	R/W	0x0	Verr_stbdet_win0

Table 9-139 VPU_VLOCK_STBDET_CLP 0x3018

Bit(s)	R/W	Default	Description
15-8	R	0x0	Read only, ro_verr_clp_win1, verr_clp number in win0
7-0	R	0x0	Read only, ro_verr_clp_win0, verr clp number in win1

Table 9-140 VPU_VLOCK_STBDET_ABS_WIN0 0x3019

Bit(s)	R/W	Default	Description
23-0	R	0x0	Read only, ro_verr_abs_win0

Table 9-141 VPU_VLOCK_STBDET_ABS_WIN1 0x301a

Bit(s)	R/W	Default	Description
23-0	R	0x0	Read only, ro_verr_abs_win1

Table 9-142 VPU_VLOCK_STBDET_SGN_WIN0 0x301b

Bit(s)	R/W	Default	Description
23-0	R	0x0	Read only, ro_verr_sgn_win0

Table 9-143 VPU_VLOCK_STBDET_SGN_WIN1 0x301c

Bit(s)	R/W	Default	Description
23-0	R	0x0	Read only, ro_verr_sgn_win1

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Table 9-144 VPU_VLOCK_ADJ_EN_SYNC_CTRL 0x301d

Bit(s)	R/W	Default	Description
31-24	R/W	0x0	PLL adjust enable signal sync ctrl, adj_en_for_pll_end, end counter of adj_en_pll signal fall to 0
23-16	R/W	0x0	PLL adjust enable signal sync ctrl, adj_en_for_pll_start, start counter of adj_en_ pll signal go to 1, start must be larger than end
15-8	R/W	0x0	Adj_en_sync_latch_cnt, this is a delay to latch the adj_en signal
7-0	R/W	0x0	Adj_en_ext_cnt, extend the adj_en signal from vid_lock clock domain to pll sample domain, make sure it's wide enough

Table 9-145 VPU_VLOCK_GCLK_EN 0x301e

Bit(s)	R/W	Default	Description
2	R/W	0x0	Ref clock enable
1	R/W	0x0	Vsout clk enable
0	R/W	0x0	Vsin clk enable

Table 9-146 VPU_VLOCK_LOOP1_ACCUM_LMT 0x301f

Bit(s)	R/W	Default	Description
26-0	R/W	0x0	LOOP1 accumulator limit

Table 9-147 VPU_VLOCK_RO_M_INT_FRAC 0x3020

Bit(s)	R/W	Default	Description
29-16	R	0x0	Read only, m_int to PLL
13-0	R	0x0	Read only, m_frac to PLL

Table 9-148 VPU_VLOCK_RO_PH_DIS 0x3021

Bit(s)	R/W	Default	Description
27-0	R	0x0	phase distance RO

Table 9-149 VPU_VLOCK_RO_PH_ERR 0x3022

Bit(s)	R/W	Default	Description
27-0	R	0x0	phase error RO

Table 9-150 VPU_VLOCK_LOCK_TH 0x3023

Bit(s)	R/W	Default	Description
31-16	R/W	0x0	phase error threshold

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Table 9-151 VPU_VLOCK_LOCK_TH1 0x302b

Bit(s)	R/W	Default	Description
21-0	R/W	0x0	frequency error threshold

Table 9-152 VPU_VLOCK_RO_LCK_FRM 0x3024

Bit(s)	R/W	Default	Description
31-18	R/W	0x0	reserved
17	R/W	0x0	phase lock flag
16	R/W	0x0	frequency lock flag
15-0	R/W	0x0	ro_lock_frame_count

Table 9-153 VPU_VLOCK_WIN0_TH 0x3025

Bit(s)	R/W	Default	Description
23-0	R/W	0x0	reg_win0_th

Table 9-154 VPU_VLOCK_WIN0_RATIO 0x3026

Bit(s)	R/W	Default	Description
7-0	R/W	0x0	reg_win0_ratio

Table 9-155 VPU_VLOCK_WIN0_FILTER_CNTL 0x3027

Bit(s)	R/W	Default	Description
20-0	R/W	0x0	reg_win0_lock_filter_cntl

Table 9-156 VPU_VLOCK_WIN1_TH 0x3028

Bit(s)	R/W	Default	Description
23-0	R/W	0x0	reg_win0_th

Table 9-157 VPU_VLOCK_WIN1_RATIO 0x3029

Bit(s)	R/W	Default	Description
7-0	R/W	0x0	reg_win0_ratio

Table 9-158 VPU_VLOCK_WIN1_FILTER_CNTL 0x302a

Bit(s)	R/W	Default	Description
20-0	R/W	0x0	reg_win0_lock_filter_cntl

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9.2.3.3 VIU Top-Level Registers

Table 9-159 VIU_SW_RESET 0x1A01

Bit(s)	R/W	Default	Description
31	R/W	0	Osd1 afbcd reset
30	R/W	0	hist_spl reset
29	R/W	0	Ldim stts reset
8	R/W	0	Vd2 Dos afbcd reset
7	R/W	0	vpp_reset
6	R/W	0	di_dsr1to2_reset
5	R/W	0	vd2_fmt_reset
4	R/W	0	vd2_reset
3	R/W	0	vd1_fmt_reset
2	R/W	0	vd1_reset
1	R/W	0	osd2_reset
0	R/W	0	osd1_reset

Table 9-160 VIU_SW_RESET0 0x1A02

Bit(s)	R/W	Default	Description
2	R/W	0	Vd1 Dos afbcd reset

Table 9-161 VIU_MISC_CTRL0 0x1a06

Bit(s)	R/W	Default	Description
17	R/W	0	Vdin0_wr_out_ctrl : 0: nr_inp to vdin 1: vdin wr dout
16	R/W	0	Afbc_inp_sel : 0: mif to INP 1: afbc to INP
16	R/W	0	di_mif0_en: vd1(afbc) to di post(if0) enable
8	R/W	0	vsync_int_ctrl : default = 0
6:5	R/W	2	0: close mif data 1: mif to tfbf_downscale: 2: mif to nr , 3: mif to tfbf_downscale & NR
4	R/W		Vpp_di_mif0_sel 0:buf0_data from di_mif0 1: buf0_data from din_post_din
0	R/W	0	scan_reg : default = 0

Table 9-162 VIU_MISC_CTRL1 0x1A07

Bit(s)	R/W	Default	Description
27-22	R/W	0	afbc gate clk ctrl
15:14	R/W	0	Mali afbcd clock gate control
12	R/W	0	Osd1 axi bus select 1 : select mali afbcd 0 : normal osd1

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Bit(s)	R/W	Default	Description
11:8	R/W	0	di_mad_en: di post to vpp enable
7-2	R/W	0	Afbcd2 Clock gate control
1	R/W	0	1 : connect dos afbcd2 to vpp vd1, 0 : connect mif to vpp vd1
0	R/W	0	1 : Dos afbcd2 output to di ; 0 : dos afbcd2 output to vpp

Table 9-163 VIUB_SW_RESET 0x2001

Bit(s)	R/W	Default	Description
31	R/W	0	mcvecwr_mif_rst_n
30	R/W	0	reserved
29	R/W	0	reserved
28	R/W	0	di_cont_rd_mif_rst_n
27	R/W	0	di_cont_wr_mif_rst_n
26	R/W	0	reserved
25	R/W	0	reserved
24	R/W	0	vdin1_wr_rst_n
23	R/W	0	vdin0_wr_rst_n
22	R/W	0	nrin_mux_rst_n
21	R/W	0	vdin1_rst_n
20	R/W	0	vdin0_rst_n
19	R/W	0	di_mad_rst_n
18	R/W	0	di_mtn_rd_mif_rst_n
17	R/W	0	di_mtn_wr_mif_rst_n
16	R/W	0	di_chan2_mif_rst_n
15	R/W	0	dein_wr_mif_rst_n
14	R/W	0	di_nr_wr_mif_rst_n
13	R/W	0	di_mem_fmt_rst_n
12	R/W	0	di_mem_rst_n
11	R/W	0	di_inp_fmt_rst_n
10	R/W	0	di_inp_rst_n
9	R/W	0	di_if1_fmt_rst_n
8	R/W	0	di_if1_rst_n
7-0	R/W	0	RESERVED

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Table 9-164 VIUB_SW_RESET0 0x2002

Bit(s)	R/W	Default	Description
3	R/W	0	di_axi_arb_rst_n
2	R/W	0	mcinford_mif_rst_n
1	R/W	0	mcinfowr_mif_rst_n
0	R/W	0	mcvecrd_mif_rst_n

Table 9-165 DI_AFBCE_CTRL 0x2003

Bit(s)	R/W	Default	Description
29-22	R/W	0	Mem Afbcd1 gate clock control
21-14	R/W	0	Inp Afbcd0 gate clock control
13	R/W	0	mem data sel: 0:normal sel 1:afbc dec0
12	R/W	0	mem afbc1 sel: 0:normal mif 1:afbc dec1
11	R/W	0	inp data sel: 0:normal sel 1:afbc dec0
10	R/W	0	Inp afbc0 sel: 0:normal mif 1:afbc dec0
9	R/W	0	Di inp line buffer ram sel: 1:enable line buffer 0:disable line buffer
8	R/W	0	Di mem line buffer ram sel: 1:enable line buffer 0:disable line buffer
6:5	R/W	0	Afbce_gate clock ctrl
4	R/W	1	Nr channel0_enable, it's a important signal!!!!!!! Should set to 1 1: enable nr write to DDR 0: disable nr write ti DDR
3	R/W	0	Vpp_path_sel: 1: nr channel1 out to vpp(vd1) 0: di post out to vpp(vd1)
2	R/W	0	Afbce_path_sel: 1: di post out to afbce 0: di pre out to afbce
1	R/W	0	Diwr_patch_sel: 1: di dout to afbce 0: di dout to normal mif
0	R/W	0	Nrwr_path_sel: 1: nr channel0 to afbce 0: nr channel0 to normal mif

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Table 9-166 VIUB_MISC_CTRL0 0x2006

Bit(s)	R/W	Default	Description
17	R/W	0	input2pre enable: 1->di inp data from vdin0 0->di inp data from inp_afbc(see bit16)
16	R/W	0	AFBC_INP_SEL: 1->di inp_afbc data from afbc 0->di inp_afbc data from inp mif(ddr)
6:5	R/W	0	0:mask input 1:buf_data ->nr_dscale 2: buf_data->NR 3: buf_data->nr_dscale &NR
4	R/W	0	0:post_din to buf 1: di_mif0 -> buf
3-2	R/W	0	Fix_disable:dein_wr_mif
1-0	R/W	0	Fix_disable: di_nr_wr_mif

Table 9-167 VIUB_GCLK_CTRL0 0x2007

Bit(s)	R/W	Default	Description
31:16	R/W	0	Reserved
15	R/W	0	Di_gate_all,for old di
14	R/W	1	Di_no_clk_gate,for old di
13	R/W	0	reserved
12	R/W	0	Di_post clock enable ,from div clock
11	R/W	0	Mcdi clock enable,from div clock
10	R/W	0	Div clock enable,di slow clock including di&MCDI
9	R/W	0	Mad post clock enable,from mad clock
8	R/W	0	Mad pre clock enable,from mad clock
7:1	R/W		reserved
0	R/W	1	Def=1 di_top_wrap clk enable

Table 9-168 VIUB_GCLK_CTRL1 0x2008

Bit(s)	R/W	Default	Description
31:28	R/W	0	Reserved
27:26	R/W	0	Mcdi pre mif clock gate 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
25:24	R/W	0	Mtn mif clock gate 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
23:22	R/W	0	Nr wrmif clock gate 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
21:20	R/W	0	Chan rdmif clock gate 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
19:18	R/W	0	Mem rdmif clock gate 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
17:16	R/W	0	Inp rdmif clock gate clock gate 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
15:14	R/W	0	reserved
13:12	R/W	0	Mcdi post clock gate 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock

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Bit(s)	R/W	Default	Description
11-10	R/W	0	Mtnrd post mif clock gate 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
9-8	R/W	0	De wrmif clock gate 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
7-6	R/W	0	if2 rdmif clock gate 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
5-4	R/W	0	If1 rdmif clock gate 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
3-2	R/W	0	If0 rdmif clock gate 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
1-0	R/W	0	Mif-sub-arb clock gate 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock

Table 9-169 VIUB_GCLK_CTRL2 0x2009

Bit(s)	R/W	Default	Description
31-14	R/W	0	reserved
13-12	R/W	0	mcdi clock gate ctrl 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
11:10	R/W	0	Nr&dnr blend clock gate ctrl 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
9-8	R/W	0	Dnr clock gate ctrl 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
7-6	R/W	0	nning clock gate ctrl 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
5-4	R/W	0	Mtn det clock gate ctrl 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
3-2	R/W	0	pd clock gate ctrl 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
1-0	R/W	0	Nr clock gate ctrl 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock

Table 9-170 VIUB_GCLK_CTRL3 0x200a

Bit(s)	R/W	Default	Description
31-6	R/W	0	Reserved
5-4	R/W	0	Di blend clock gate ctrl 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
3-2	R/W	0	Ei clock gate ctrl 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock
1-0	R/W	0	Ei_0 clock gate ctrl 2'b00: gate clock ,2'b01: close clock,2'b1x: always clock

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Table 9-171 DI_DBG_CTRL 0x200B

Bit(s)	R/W	Default	Description
31:7	R/W	0	Reserved
6	R/W	0	go_field_sel : 1: post_frame_rst 0: pre_frame_rst
5:0	R/W	0	Debug_sel : 0:diwr_out_mif 1: mtn1_din 2:mtn1_dout 3:nrdm_bld 4:dnr_dm 5:dnr_din 6:ds_dout 7:ds_din 8:deband_din 9:me_mtn 10:mc_info_mif 11:me_din_pipe 12:buf1_dout 13:mem2post 14:cont_buf 15:nr_wr_out 16:mtn_din 17:me_din 18:nr_din 19:dnr_out 20:nr_out 21:contp_mif 22:chan2 23:di_inp_mif 24:di_mem_mif 25:contp2_mif 26:contp_mif 27:chan2_mif 28:di_inp 29:di_mem 30:mcinfo_pipe 31:mad_dout 32:deint_pipe 33:mtnp_mif 34:blend_1_dout 35:blend_buf1_din 36:direct_mux 37:ei_fifo_dout 38:di_buf0 39:mif_mtnp 40:buf2_pipe 41:buf1_pipe 42:mcvec_pipe 43:buf0_pipe

Table 9-172 DI_DBG_CTRL1 0x200C

Bit(s)	R/W	Default	Description
31:16	R/W	0	Rrdy_to_srdy_max_num
15:0	R/W	0	Srdy_to_rrdy_max_num

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Table 9-173 DI_DBG_SRDY_INF 0x200D

Bit(s)	R/W	Default	Description
31:16	RO	0	wait_rrdy_bmax_dbg_cnt
15:0	RO	0	Srdy_to_rrdy_dbg_cnt

Table 9-174 DI_DBG_RRDY_INF 0x200E

Bit(s)	R/W	Default	Description
31:16	RO	0	Wait_srdy_bmax_dbg_cnt
15:0	RO	0	Rrdy_to_srdy_dbg_cnt

Table 9-175 VIU_MISC_CTRL1 0x3107

Bit(s)	R/W	Default	Description
15:14	R/W	0x0	mali_afbcd_gclk_ctrl : mali_afbcd clock gate control[5:4]
12	R/W	0x0	osd1_afbcd_axi_mux : 0 : use the osd mif as input; 1 : use afbcd as input
11:8	R/W	0x0	mali_afbcd_gclk_ctrl : mali_afbcd clock gate control[3:0]
7:2	R/W	0x0	vd2_afbcd_gclk_ctrl : vd2_afbcd clock gate control
1	R/W	0x0	vpp_vd2_din_sel : 0: vpp vd2 sel the mif input; 1: vpp vd2 sel the dos afbcd
0	R/W	0x0	vd2_afbcd_out_sel : 0: vd2_afbcd output to vpp; 1 : vd2_afbcd output to di inp

9.2.3.4 VIU2 Registers

9.2.3.4.1 VIU2 Top-Level Registers

Table 9-176 VIU2_SW_RESET 0x1e01

Bit(s)	R/W	De-fault	Description
31:1	R/W	0	reseve
0	R/W	0	Viu2_osd_reset : // unsigned , default = 0

Table 9-177 VIU2_MISC_CTRL0 0x1e06

Bit	R/W	Default	Description
21:20	R/W	0	Viu2 out_fifo gclk
19:18	R/W	0	Clk of viu2
17	R/W	0	Vpp_reg_gclk
8	R/W	0	Viu2 vsync_int_ctrl : default = 0
0	R/W	0	Viu2 scan_reg : default = 0

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Table 9-178 VIU2_SECURE_REG 0x1e05

Bit	R/W	Default	Description
1	R/W	0	Viu2_matrix out
0	R/W	0	Osd1

Table 9-179 VPP2_OFIFO_SIZE 0x1e27

Bit	R/W	Default	Description
31:20	R/W	0	ofifo_line_lenm1 : //unsigned , default = 0xfff , ofifo line length minus 1
19	R/W	0	vs_ctrl : //unsigned , default = 0 , if true invert input vs
18	R/W	0	hs_ctrl : //unsigned , default = 0 , if true invert input hs
17	R/W	0	force_top_bot_field_en : //unsigned , default = 0 , force top/bottom field, enable
16	R/W	0	fforce_top_bot_field : //unsigned , default = 0 , force top/bottom field, 0: top, 1: bottom
15	R/W	0	force_go_field : //unsigned , default = 0 , force one go_field, one pluse, write only
14	R/W	0	force_go_line : //unsigned , default = 0 , force one go_line, one pluse, write only
13:0	R/W	0	ofifo_size : //unsigned , default = 0x1000 , ofifo size (actually only bit 13:1 is valid), always even number ,max 2048

Table 9-180 VPP2_INT_LINE_NUM 0x1e20

Bit	R/W	Default	Description
12:0	R/W	0x0	interrupt_line_num : //unsigned, default== 0x1fff,line number use to generate interrupt when line == this number

Table 9-181 VPP2_MISC 0x1e26

Bit	R/W	Default	Description
16	R/W	0	Sel_rot_en://sel mif connect to ddr 1:rotation as viu2_mif 0:osd as viu2_mif
5:4	R/W	0	Viu2_mattix gate_clk ctrl
3	R/W	0	/
2	R/W	0	disable_rst_afifo : //unsigned , default = 0 , if true, disable resetting async fifo every vsync, otherwise every vsync the aync fifo will be reseted.
1	R/W	/	/

Table 9-182 VPP2_OFIFO_URG_CTRL 0x1e21

Bit	R/W	Default	Description
31	R/W	0x0	urgent_hold : //unsigned, default== 0, urgent fifo hold enable
28:12	R/W	0x0	urgent_fifo_th : //unsigned, default== 0, urgent fifo hold line threshold
15	R/W	0x0	urgent_ctrl_en : //unsigned, default== 0, urgent_ctrl_en

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Bit	R/W	Default	Description
14	R/W	0x0	urgent_wr : //unsigned, default== 0, urgent_wr, if true for write buffer
13	R/W	0x0	out_inv_en : //unsigned, default== 0, out_inv_en
12	R/W	0x0	urgent_ini_value : //unsigned, default == 0, urgent_ini_value
11:6	R/W	0x0	up_th : //unsigned, default == 0, up_th up threshold
5:0	R/W	0x0	dn_th : //unsigned, default == 0, dn_th dn threshold

Table 9-183 VIU2_OSD1_CTRL_STAT 0x1e30

Bit	R/W	Default	Description
31	R/W	0	osd_cfg_syn_en : // unsigned , default =0 1: module enable sync by go_field 0: normal
30	R/W	0	ENABLE_FREE_CLK. 1 = Use free-running clock; 0 = Use gated clock to save power.
29	R	0	TEST_RD_DSR: Applicable only when OSD debug mode is enabled. 1 = A new pixel is ready at register VIU2_OSD1_TEST_RDDATA; 0 = No data ready.
/	/	/	/
27-24	R	0	OSD_BLK_MODE: the input pixel format of which the current OSD block is being processed. Mali src & normal src have different pixel format value for same format
23-22	R	0	OSD_BLK_PTR: The number of the current OSD block that is being processed.
21	R	0	OSD_ENABLE. 1 = OSD display is enabled; 0 = disabled.
20-12	R/W	0	GLOBAL_ALPHA: legal range 0 – 256. It is a 9-bit value that is multiplied to all output pixel's Alpha value, and then normalized, i.e.: Alpha_tmp = Alpha_internal + (Alpha_internal == 0 ? 0 : 1); Alpha_out = (Alpha_tmp * GLOBAL_ALPHA) / 256;
11	R/W	0	TEST_RD_EN: OSD debug mode enable. 1 = Output pixels are not routed to VPP, instead they are presented on registers VIU2_OSD1_TEST_RDDATA, for CPU to read. 0 = Normal mode, pixels are output to VPP.
10-9	R/W	0	unused
8-5	R/W	0	CTRL_MTCH_Y: For OSD 444, 422 or 16-bit (COLOR_MATRIX = 0 or 1) mode, the input pixels contain no Alpha information, in order to associated the output pixel with an Alpha value, the following steps are taken: If TC_ALPHA_EN = 0, then all output pixels use a default Alpha value 0xFF; If TC_ALPHA_EN = 1, then the Alpha value is looked up by matching the pixel's Y/Cb/Cr against four Alpha registers' Y/Cb/Cr. If the pixel matches any one of the Alpha registers, then this register's Alpha value is used; If the pixel matches with more than one of the Alpha registers, then the lower Alpha register takes priority, e.g. use Alpha Reg0's value if the pixel match both Alpha Reg0 and Reg1; If no match, then use default Alpha value 0xFF. There are two ways of matching: one way is that the pixel has to compare all Y, Cb and Cr value with the Alpha registers; the other way is that the pixel only has to compare Y value with the Alpha registers. CTRL_MTCH_Y defines which way is used to determine a match. Bit[0] is for matching Alpha register 0: 1 = only need to compare Y; 0 = compare all Y, Cb and Cr. Bit[1] is for matching Alpha register 1: 1 = only need to compare Y; 0 = compare all Y, Cb and Cr. Bit[2] is for matching Alpha register 2: 1 = only need to compare Y; 0 = compare all Y, Cb and Cr.

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Bit	R/W	Default	Description
			Bit[3] is for matching Alpha register 3: 1 = only need to compare Y; 0 = compare all Y, Cb and Cr.
4	R/W	0	CTRL_422TO444. 1 = Enable conversion of 422 format input to 444 format output; 0 = Disable 422 to 444 conversion.
/	/	/	/
2	R/W	0	osd_mem_mode : // unsigned , default =0 0:canvas_araddr 1: linear_araddr (mali src must use this mode)
1	R/W	0	premult_en : // unsigned , default =0
0	R/W	0	OSD_BLK_ENABLE: Each bit to enable display an OSD block

Table 9-184 VIU2_OSD1_CTRL_STAT2 0x1e4d

Bit	R/W	Default	Description
31-16	R	0	unused
15	R/W	0	unused
14	R/W	0	Replaced_alpha_en
13-6	R/W	0	Replaced_alpha
5-4	R/W	0	Hold_fifo_lines[6:5]
3	R/W	0	RGBYUV_FULL_RANGE: Select coefficients for applicable output range. 1 = output full range 0-255; 0 = output range 16-235.
2	R/W	0	ALPHA_9B_MODE: Define how to expand 8-bit alpha value to 9-bit. 1 = The formula is (Alpha < 128) ? Alpha : Alpha + 1; 0 = The formula is (Alpha == 0) ? Alpha : Alpha + 1.
1	R/W	0	Pedding status cleanup
0	R/W	0	COLOR_EXPAND_MODE. 1 = Expand the color components to 8-bit by padding LSBs with MSBs. E.g. If the input is 5'b11000, the output is expanded to 8'b11000110; 0 = Expand the color components to 8-bit by padding LSBs with 0.

VIU2_OSD1_TCOLOR_AG0 0x1e37

VIU2_OSD1_TCOLOR_AG1 0x1e38

VIU2_OSD1_TCOLOR_AG2 0x1e39

VIU2_OSD1_TCOLOR_AG3 0x1e3a

Define Alpha register 0/1/2/3 values.

Bit	R/W	Default	Description
31-24	R/W	0xFF	Y or R.
23-16	R/W	0xFF	CB or G.
15-8	R/W	0xFF	CR or B.
7-0	R/W	0xFF	ALPHA.

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Table 9-185 VIU2_OSD1_BLK0_CFG_W0 0x1e3b

Defines display block 0/1/2/3’s property, word 0.

Bit	R/W	Default	Description
31	R/W	0	Reserved
30	R/W	0	mali_src_en 1: read data from mali afbcd decoder 0: read data from DDR directly
29	R/W	0	y_rev: 0=normal read, 1=reverse read in Y direction
28	R/W	0	x_rev: 0=normal read, 1=reverse read in X direction
27-24	R/W	0	Reserved
23-16	R/W	0	TBL_ADDR. Virtual canvas LUT entry.
15	R/W	0	LITTLE_ENDIAN: define the of data stored in DDR. 1 = Data stored in DDR memory are of little endian; 0 = Data stored in DDR memory are of big endian.
14	R/W	0	RPT_Y: For reducing data size stored in DDR. 1 = For each line, OSD will display twice; 0 = No repeat, OSD display once per line.
13-12	R/W	0	INTERP_CTRL: If enabled, interpolate a data after each incoming pixels, in order to save DDR bandwidth. 0 = No interpolation; 1 = unused, no interpolation; 2 = Interpolate with preceding pixel value; 3 = Interpolate with the averaged value between the preceding pixel and the next pixel.
11-8	R/W	0	OSD_BLK_MODE: Define the OSD block’s input pixel format according bit30. Bit30 == 0: 0 = 2-bit per pixel, totally 4 colors can be looked up from color palette LUT,Only OSD2 have; 1 = 4-bit per pixel, totally 16 colors can be looked up from color palette LUT,Only OSD2 have; 2 = 8-bit per pixel, totally 256 colors can be looked up from color palette LUT,Only OSD2 have; 3 = 4:2:2 mode. Input 32-bit data for 2 pixels. Bit[31:24] is Y0, bit [23:16] is Cb0, bit[15:8] is Y1, bit [7:0] is Cr0, for Alpha value refer to reg VIU2_OSD1_CTRL_STAT.CTRL_MTCH_Y; 4 = 16-bit mode. Refer to COLOR_MATRIX; 5 = 32-bit mode. Refer to COLOR_MATRIX; 6 = unused; 7 = 24-bit mode. Refer to COLOR_MATRIX; 8-15 = unused; Bit30 == 1: 0□R8 1□8bit yuv422 2□RGB565 3□RGBA5551 4□RGBA4444 5□RGBA8888 7□RGB888 8□10bit yuv422 9□RGBA1010102 Other:unuse
6	R/W	0	TC_ALPHA_EN: refer to reg VIU2_OSD1_CTRL_STAT.CTRL_MTCH_Y. 1 = Enable alpha register matching. 0 = Disable.
5-2	R/W	0	COLOR_MATRIX: Applicable only to 16-bit color mode (OSD_BLK_MODE=4), 32-bit mode (OSD_BLK_MODE=5) and 24-bit mode (OSD_BLK_MODE=7),

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Bit	R/W	Default	Description
			defines the bit-field allocation of the pixel data. For expanding the bit-fields to full 8-bit, refer to VIU2_OSD1_CTRL_STAT2.color_expand_mode For 16-bit mode (OSD_BLK_MODE=4): 0 = 6:5:5 format. Bit[15:10] is Y[7:2] or R[7:2], bit[9:5] is Cb[7:3] or G[7:3], bit[4:0] is Cr[7:3] or B[7:3], for Alpha value refer to reg VIU2_OSD1_CTRL_STAT.CTRL_MTCH_Y; 1 = 8:4:4 format. Bit[15:8] is Y or R, bit[7:4] is Cb[7:4] or G[7:4], bit[3:0] is Cr[7:4] or B[7:4]], for Alpha value refer to reg VIU2_OSD1_CTRL_STAT.CTRL_MTCH_Y; For 32-bit mode (OSD_BLK_MODE=5): 0 = RGBA 8:8:8:8 format. Bit[31:24] is Y or R, bit[23:16] is Cb or G; bit[15:8] is Cr or B; bit[7:0] is Alpha; 1 = ARGB 8:8:8:8 format. Bit[31:24] is Alpha, bit[23:16] is Y or R; bit[15:8] is Cb or G; bit[7:0] is Cr or B; 2 = ABGR 8:8:8:8 format. Bit[31:24] is Alpha, bit[23:16] is Cr or B; bit[15:8] is Cb or G; bit[7:0] is Y or R; 3 = BGRA 8:8:8:8 format. Bit[31:24] is Cr or B, bit[23:16] is Cb or G; bit[15:8] is Y or R; bit[7:0] is Alpha. For 24-bit mode (OSD_BLK_MODE=7): 0 = RGB 8:8:8 mode. Bit[23:16] is Y or R, bit[15:8] is Cb or G, bit[7:0] is Cr or B, for Alpha value refer to reg VIU2_OSD1_CTRL_STAT.CTRL_MTCH_Y; 5 = BGR 8:8:8 mode. Bit[23:16] is Cr or B, bit[15:8] is Cb or G, bit[7:0] is Y or R, for Alpha value refer to reg VIU2_OSD1_CTRL_STAT.CTRL_MTCH_Y.
1	R/W	0	INTERLACE_EN. 1 = Enable interlace mode. 0 = Disable.
0	R/W	0	INTERLACE_SEL_ODD: Applicable only if INTERLACE_EN = 1. 1 = Only output odd lines; 0 = Only output even lines.

Table 9-186 VIU2_OSD1_BLK0_CFG_W1 0x1e3c

Bit	R/W	Default	Description
31-29	R/W	0	Unused.
28-16	R/W	0	X_END. Virtual canvas co-ordinate.
15-13	R/W	0	Unused.
12-0	R/W	0	X_START. Virtual canvas co-ordinate.

Table 9-187 VIU2_OSD1_BLK0_CFG_W2 0x1e3d

Defines display block 0/1/2/3's property, word 2.

Bit	R/W	Default	Description
31-29	R/W	0	Unused.
28-16	R/W	0	Y_END. Virtual canvas co-ordinate.
15-13	R/W	0	Unused.
12-0	R/W	0	Y_START. Virtual canvas co-ordinate.

Table 9-188 VIU2_OSD1_BLK0_CFG_W3 0x1e3e

Defines display block 0/1/2/3's property, word 3.

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Bit	R/W	Default	Description
31-28	R/W	0	Unused.
27-16	R/W	0	H_END. Display horizontal co-ordinate.
15-12	R/W	0	Unused.
11-0	R/W	0	H_START. Display horizontal co-ordinate.

Table 9-189 VIU2_OSD1_BLK0_CFG_W4 0x1e64

Defines display block 0/1/2/3's property, word 4.

Bit	R/W	Default	Description
31-28	R/W	0	Unused.
27-16	R/W	0	V_END. Display vertical co-ordinate.
15-12	R/W	0	Unused.
11-0	R/W	0	V_START. Display vertical co-ordinate.

Table 9-190 VIU2_OSD1_BLK1_CFG_W4 0x1e65

Bit	R/W	Default	Description
31:0	R/W	0	Frame_addr: // unsigned , default =0 Frame_addr in linear_addr

Table 9-191 VIU2_OSD1_BLK2_CFG_W4 0x1e66

Bit	R/W	Default	Description
31:0	R/W	0	Line_stride : // unsigned , default =0 Line_stride in linear_addr

Table 9-192 VIU2_OSD1_FIFO_CTRL_STAT 0x1e4b

Bit	R/W	Default	Description
31	R/W	0	burst_len_sel[2] of [2:0]
30	R/W	0	BYTE_SWAP: In addition to endian control, further define whether to swap upper byte and lower byte within a 16-bit memory word. 1 = Swap, data[15:0] becomes {data[7:0], data[15:8]}; 0 = No swap, data[15:0] is still data[15:0].
29	R/W	0	Div_swap : swap the 2 64bits word in 128bits word
28-24	R/W	0	Fifo_lim : when osd fifo is small than the fifo_lim*16, closed the req port of osd_ rd_mif
23-22	R/W	0	Fifo_ctrl: 00 : for 1 word in 1 burst, 01 : for 2words in 1burst, 10 : for 4 words in 1burst, 11: reserved
21-20	R	0	FIFO_ST: State of the FIFO activity. 0 = Idle; 1 = FIFO requesting; 2 = FIFO request aborting.
19	R	0	FIFO_OVERFLOW.

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Bit	R/W	Default	Description
18-12	R/W	32	FIFO_DEPTH_VAL: Define the depth of FIFO which stores 128-bit data from DDR to be FIFO_DEPTH_VAL * 8.
11-10	R/W	0	BURST_LEN_SEL[1:0] of [2:0]: Define DDR burst request length. 0 = up to 24 per burst; 1 = up to 32 per burst; 2 = up to 48 per burst;/ 3 = up to 64 per burst. 4 = up to 96 per burst, 5 = up to 128 per burst
9-5	R/W	4	HOLD_FIFO_LINES: The number of lines that OSD must wait after VSYNC, before it starts request data from DDR .
4	R/W	0	CLEAR_ERR: One pulse to clear error status.
3	R/W	0	FIFO_SYNC_RST: Set 1 to reset OSD FIFO.
2-1	R/W	0	ENDIAN: define the endianess of the 64-bit data stored in memory, and how to convert. 0 = No convertion; 1 = Convert to {din[31:0], din[63:32]}; 2 = Convert to {din[15:0], din[31:16], din[47:32], din[63:48]}; 3 = Convert to {din[47:32], din[63:48], din[15:0], din[31:16]};
0	R/W	0	URGENT. 1 = Set DDR request priority to be urgent; 0 = Set DDR request priority to be normal.

Table 9-193 VIU2_OSD1_TEST_RDDATA 0x1e4c

During OSD debug mode (VIU2_OSD1_CTRL_STAT.TEST_RD_EN = 1), the output pixels will be presented at this register.

Bit	R/W	Default	Description
31-24	R	0	Y or R.
23:16	R	0	Cb or G.
15-8	R	0	Cr or B.
7-0	R	0	Alpha[8:1].

Table 9-194 VIU2_OSD1_PROT_CTRL 0x1e4e

Bit	R/W	Default	Description
31:16	R/W	0	urgent_ctrl : // unsigned , default =0
15	R.O	0	prot_en : // unsigned , default =0; 1=Borrow PROT's FIFO storage, either for rotate or non-rotate.
12: 0	R.O	0	prot_fifo_size : // unsigned , default =0; effective FIFO size when prot_en=1.

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Table 9-195 VIU2_OSD1_MALI_UNPACK_CTRL 0x1e4f

Bit	R/W	Default	Description
31	R/W	0	mali_unpack_en 1: OSD will unpack mali_src 0: OSD will unpack normal src
28			Alpha_div_en: alpha dividor enable
27:26			Alpha_dividor gating clk
25:24			Alpa_mapping_mode In osd,this bit should be set 0 when Alpha_div_en active,means 8 bits alpha mode
17	/	/	/
16	R/W	0	afbcd_swap_64bit:
15: 12	R/W	1	afbcd_r_reorder,change osd output order when use mali src: 1: r_re = r ; 2: r_re = g; 3: r_re = b; 4: r_re = a; default: r_re = 0;
11: 8		2	afbcd_r_reorder,change osd output order when use mali src: 1: g_re = r ; 2: g_re = g; 3: g_re = b; 4: g_re = a; default: r_re = 0;
7: 4		3	afbcd_r_reorder,change osd output order when use mali src: 1: b_re = r ; 2: b_re = g; 3: b_re = b; 4: b_re = a; default: r_re = 0;
3: 0		4	afbcd_r_reorder,change osd output order when use mali src: 1: a_re = r ; 2: a_re = g; 3: a_re = b; 4: a_re = a; default: r_re = 0;

Table 9-196 VIU2_OSD1_DIMM_CTRL 0x1e4f

Bit	R/W	Default	Description
30	R/W	0	OSD dimm enable,osd out will be one color when this bit active
29:0	R/W	0	Osd_dim_rgb_out ,osd out will be this vaaule when bit30 active

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9.2.3.4.2 VIU2_OSD1_MATRIX Registers

Table 9-197 VIU2_OSD1_MATRIX_COEF00_01 0x1e70

Bits	Name	Memory Access	Description
28-16	R/W	0	Coefficient00, signed, 3.10
12-0	R/W	0	Coefficient01, signed, 3.10

Table 9-198 VIU2_OSD1_MATRIX_COEF02_10 0x1e71

Bits	Name	Memory Access	Description
28-16	R/W	0	Coefficient02, signed, 3.10
12-0	R/W	0	Coefficient10, signed, 3.10

Table 9-199 VIU2_OSD1_MATRIX_COEF11_12 0x1e72

Bits	Name	Memory Access	Description
28-16	R/W	0	Coefficient11, signed, 3.10
12-0	R/W	0	Coefficient12, signed, 3.10

Table 9-200 VIU2_OSD1_MATRIX_COEF20_21 0x1e73

Bits	Name	Memory Access	Description
28-16	R/W	0	Coefficient20, signed, 3.10
12-0	R/W	0	Coefficient21, signed, 3.10

Table 9-201 VIU2_OSD1_MATRIX_COEF22 0x1e74

Bits	Name	Memory Access	Description
18-16	R/W	0	convrs
12-0	R/W	0	Coefficient22, signed, 3.10

Table 9-202 VIU2_OSD1_MATRIX_COEF13_14 0x1e75

Bits	Name	Memory Access	Description
28-16	R/W	0	Coefficient13, signed, 3.10
12-0	R/W	0	Coefficient14, signed, 3.10

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Table 9-203 VIU2_OSD1_MATRIX_COEF23_24 0x1e76

Bits	Name	Memory Access	Description
28-16	R/W	0	Coefficient23, signed, 3.10
12-0	R/W	0	Coefficient24, signed, 3.10

Table 9-204 VIU2_OSD1_MATRIX_COEF15_25 0x1e77

Bits	Name	Memory Access	Description
28-16	R/W	0	Coefficient15, signed, 3.10
12-0	R/W	0	Coefficient25, signed, 3.10

Table 9-205 VIU2_OSD1_MATRIX_CLIP 0x1e78

Bits	Name	Memory Access	Description
31-8	R/W	0x0	reserved
7-5	R/W	0x1	Matrix rs
4-3	R/W	0x10	Matrix clmod 0: only 3x3, 1: pre_offseted_ch1,ch2> pre_offseted_ch0, use the added 2x3 coef 2: pre_offseted_ch1,ch2 > 0, use the added 2x3 coef 3: pre_offseted_ch1,ch2 > 512, use the added 2x3 coef
2-0	R/W	0x10	Matrix clip enable

Table 9-206 VIU2_OSD1_MATRIX_OFFSET0_1 0x1e79

Bits	Name	Memory Access	Description
27-16	R/W	0	Offset0, signed value
11-0	R/W	0	Offset1, signed value

Table 9-207 VIU2_OSD1_MATRIX_OFFSET2 0x1e7a

Bits	Name	Memory Access	Description
11-0	R/W	0	Offset2, signed value

Table 9-208 VIU2_OSD1_MATRIX_PRE_OFFSET0_1 0x1e7b

Bits	Name	Memory Access	Description
27-16	R/W	0	pre_Offset0, signed value
11-0	R/W	0	Pre_Offset1, signed value

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Table 9-209 VIU2_OSD1_MATRIX_PRE_OFFSET2 0x1e7c

Bits	Name	Memory Access	Description
11-0	R/W	0	Pre_Offset2, signed value

Table 9-210 VIU2_OSD1_MATRIX_EN_CTRL 0x1e7d

Bits	Name	Memory Access	Description
5:4	R/W	0	Gate clock ctrl
1	R/W	0	Enable_sync_sel
0	R/W	0	Conv_en_pre

9.2.3.4.3 ROTATION Registers

Table 9-211 VIU2_RMIF_CTRL0 0x1e80

Bit(s)	R/W	Default	Description
21:12	R/W	0	Reg_gclk_ctrl: // default = 0
9	R/W	0	Reg_rot_frm_en : // default = 0
8	R/W	0	Reg_frm_start_sel : // default = 0
6:0	R/W	0	Reg_cntl_hold_lines : // default = 0

Table 9-212 VIU2_RMIF_CTRL1 0x1e81

Bit(s)	R/W	Default	Description
31:24	R/W	0	Reg_canvas_id1 : // default = 0
23:16	R/W	0	Reg_canvas_id0 : // default = 0
15	R/W	0	Reg_canvas_sw_rst : // default = 0
14:12	R/W	0	Reg_cmd_intr_len : // default = 0
11:10	R/W	0	Reg_cmd_reg_size: // default = 0
9:8	R/W	0	Reg_burst_len : // default = 0
7	R/W	0	Reg_swap_64bit : // default = 0
6	R/W	0	Reg_little_endian : // default = 0
5	R/W	0	Reg_y_rev : //default = 0
4	R/W	0	Reg_x_rev : // default = 0
3:0	R/W	0	Reg_pack_mode : // default = 0

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Table 9-213 VIU2_RMIF_CTRL2 0x1e82

Bit(s)	R/W	Default	Description
31:30	R/W	0	Reg_sw_rst : // default = 0
26	R/W	0	Reg_fix_id0_en : // default = 0
25:24	R/W	0	Reg_sync_sel : // default = 0
16:0	R/W	0	Reg_urgent_ctrl : // default = 0

Table 9-214 VIU2_RMIF_SCROPE_X 0x1e83

Bit(s)	R/W	Default	Description
28:16	R/W	0	Reg_x_end: //default = 0
12:0	R/W	0	Reg_x_start : // default = 0

Table 9-215 VIU2_RMIF_SCROPE_Y 0x1e84

Bit(s)	R/W	Default	Description
28:16	R/W	0	Reg_y_end : //default = 0
12:0	R/W	0	Reg_y_start : // default = 0

Table 9-216 VIU2_ROT_BLK_SIZE 0x1e85

Bit(s)	R/W	Default	Description
12:8	R/W	0	Reg_blk_vsize : // default = 0
5:0	R/W	0	Reg_rd_blk_hsize : //default = 0

Table 9-217 VIU2_ROT_LBUF_SIZE 0x1e86

Bit(s)	R/W	Default	Description
29:16	R/W	0	Reg_rot_hsize : // default = 0
11:0	R/W	0	Reg_lbuf_depth: //default = 0

Table 9-218 VIU2_ROT_FMT_CTRL 0x1e87

Bit(s)	R/W	Default	Description
31:24	R/W	0	Reg_fmt_swap_comp : //default = 0
20:8	R/W	0	Reg_fmt_lbuf_size : // default = 0
7:6	R/W	0	Reg_interp_phase : // default = 0
5	R/W	0	Reg_swap_cbcr : // default = 0
4:3	R/W	0	Reg_fmt_422c444 : //default = 0
2	R/W	0	Reg_fmt_444_mode: // default = 0

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Bit(s)	R/W	Default	Description
1	R/W	0	Reg_fmt_line5_mode : // default = 0
0	R/W	0	Reg_fmt_buf_en : // default = 0

Table 9-219 VIU2_ROT_WIND_CTRL 0x1e88

Bit(s)	R/W	Default	Description
31:16	R/W	0	Reg_dout_hold_num : // default = 0
14	R/W	0	Reg_dout_vwin_en : //default = 0
13:0	R/W	0	Reg_dout_vwin_sz0 : // default = 0

Table 9-220 VIU2_ROT_OUT_VCROP 0x1e89

Bit(s)	R/W	Default	Description
28:16	R/W	0	Reg_fmt_vbgn: //default = 0
12:0	R/W	0	Reg_fmt_vend : //default = 0

Table 9-221 VIU2_ROT_BUF_SIZE 0x1e8a

Bit(s)	R/W	Default	Description
9:0	R/W	0	Reg_buf_size : // default = 0

Table 9-222 VPP2_CRC_CHK 0x1eb0

Bit(s)	R/W	Default	Description
31	R/W	0	reg_crc_start // pulse ,write a pulse to start crc
0	R/W	0	reg_crc_en:// crc enable ,start work after vsync

Table 9-223 VPP2_RO_CRCSUM 0x1eb1

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_vpp_crc : //default = 0

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9.2.3.5 DI_AXI_ARB Registers

Table 9-224 DI_RDARB_MODE_L1C1 0x2050

Bit(s)	R/W	Default	Description
21:16	R/W	0	rdarb_sel : uns, default = 0 , rdarb_sel [0]==0 slave dc0 connect master port0 rdarb_sel[0]==1 slave dc0 connect master port1 rdarb_sel [1]==0 slave dc1 connect master port0 rdarb_sel[1]==1 slave dc1 connect master port1 rdarb_sel [2]==0 slave dc2 connect master port0 rdarb_sel[2]==1 slave dc2 connect master port1 rdarb_sel [3]==0 slave dc3 connect master port0 rdarb_sel[3]==1 slave dc3 connect master port1 rdarb_sel [4]==0 slave dc4 connect master port0 rdarb_sel [4]==1 slave dc4 connect master port1 rdarb_sel [5]==0 slave dc5 connect master port0 rdarb_sel[5]==1 slave dc5 connect master port1
9:8	R/W	0	rdarb_arb_mode : uns, default = 0 , rdarb_arb_mode [0] master port0 arb way, rdarb_arb_mode [1] master port1 arb way,
3:0	R/W	0	rdarb_gate_clk_ctrl : uns, default = 0 , rdarb_gate_clk_ctrl [1:0] master port0 clk gate control rdarb_gate_clk_ctrl [3:2] master port1 clk gate control

Table 9-225 DI_RDARB_REQEN_SLV_L1C1 0x2051

Bit(s)	R/W	Default	Description
11:0	R/W	0xfff	rdarb_dc_req_en : unsigned , default = 12'hfff rdarb_dc_req_en [0]: the slv0 req to mst port0 enable, rdarb_dc_req_en [1]: the slv1 req to mst port0 enable, rdarb_dc_req_en [2]: the slv2 req to mst port0 enable, rdarb_dc_req_en [3]: the slv3 req to mst port0 enable, rdarb_dc_req_en [4]: the slv4 req to mst port0 enable, rdarb_dc_req_en [5]: the slv5 req to mst port0 enable, rdarb_dc_req_en [6]: the slv0 req to mst port1 enable, rdarb_dc_req_en [7]: the slv1 req to mst port1 enable, rdarb_dc_req_en [8]: the slv2 req to mst port1 enable, rdarb_dc_req_en [9]: the slv3 req to mst port1 enable, rdarb_dc_req_en [10]: the slv4 req to mst port1 enable, rdarb_dc_req_en [11]: the slv5 req to mst port1 enable,

Table 9-226 DI_RDARB_WEIGH0_SLV_L1C1 0x2052

Bit(s)	R/W	Default	Description
29:0	R/W	0	rddc_weigh_sxn : unsigned , default = 0 rddc_weigh_sxn [0*6+:6]: the slv0 req weigh number rddc_weigh_sxn [1*6+:6]: the slv1 req weigh number rddc_weigh_sxn [2*6+:6]: the slv2 req weigh number rddc_weigh_sxn [3*6+:6]: the slv3 req weigh number rddc_weigh_sxn [4*6+:6]: the slv4 req weigh number

Table 9-227 DI_RDARB_WEIGH1_SLV_L1C1 0x2053

Bit(s)	R/W	Default	Description
5:0	R/W	0	rddc_weigh_sxn : unsigned , default = 0 rddc_weigh_sxn [5*6+:6]: the slv5 req weigh number

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Table 9-228 DI_WRARB_MODE_L1C1 0x2054

Bit(s)	R/W	Default	Description
21:16	R/W	0	wrarb_sel : uns, default = 0 , wrarb_sel [0]==0 slave dc0 connect master port0 wrarb_sel[0]==1 slave dc0 connect master port1 wrarb_sel [1]==0 slave dc1 connect master port0 wrarb_sel[1]==1 slave dc1 connect master port1 wrarb_sel [2]==0 slave dc2 connect master port0 wrarb_sel[2]==1 slave dc2 connect master port1 wrarb_sel [3]==0 slave dc3 connect master port0 wrarb_sel[3]==1 slave dc3 connect master port1 wrarb_sel [4]==0 slave dc4 connect master port0 wrarb_sel[4]==1 slave dc4 connect master port1 wrarb_sel [5]==0 slave dc5 connect master port0 wrarb_sel[5]==1 slave dc5 connect master port1
9:8	R/W	0	wrarb_arb_mode : uns, default = 0 , wrarb_arb_mode [0] master port0 arb way, wrarb_arb_mode [1] master port1 arb way,
3:0	R/W	0	wrarb_gate_clk_ctrl : uns, default = 0 , wrarb_gate_clk_ctrl [1:0] master port0 clk gate control wrarb_gate_clk_ctrl [3:2] master port1 clk gate control

Table 9-229 DI_WRARB_REQEN_SLV_L1C1 0x2055

Bit(s)	R/W	Default	Description
11:0	R/W	0	wrarb_dc_req_en : unsigned , default = 0 wrarb_dc_req_en [0]: the slv0 req to mst port0 enable, wrarb_dc_req_en [1]: the slv1 req to mst port0 enable, wrarb_dc_req_en [2]: the slv2 req to mst port0 enable, wrarb_dc_req_en [3]: the slv3 req to mst port0 enable, wrarb_dc_req_en [4]: the slv4 req to mst port0 enable, wrarb_dc_req_en [5]: the slv5 req to mst port0 enable, wrarb_dc_req_en [0]: the slv0 req to mst port1 enable, wrarb_dc_req_en [1]: the slv1 req to mst port1 enable, wrarb_dc_req_en [2]: the slv2 req to mst port1 enable, wrarb_dc_req_en [3]: the slv3 req to mst port1 enable, wrarb_dc_req_en [4]: the slv4 req to mst port1 enable, wrarb_dc_req_en [5]: the slv5 req to mst port1 enable,

Table 9-230 DI_WRARB_WEIGH0_SLV_L1C1 0x2056

Bit(s)	R/W	Default	Description
29:0	R/W	0	wrdc_weigh_sxn : unsigned , default = 0 wrdc_weigh_sxn [0*6+:6]: the slv0 req weigh number wrdc_weigh_sxn [1*6+:6]: the slv1 req weigh number wrdc_weigh_sxn [2*6+:6]: the slv2 req weigh number wrdc_weigh_sxn [3*6+:6]: the slv3 req weigh number wrdc_weigh_sxn [4*6+:6]: the slv4 req weigh number

Table 9-231 DI_WRARB_WEIGH1_SLV_L1C1 0x2057

Bit(s)	R/W	Default	Description
5:0	R/W	0	wrdc_weigh_sxn : unsigned , default = 0 wrdc_weigh_sxn [5*6+:6]: the slv5 req weigh number

Table 9-232 DI_RDWR_ARB_STATUS_L1C1 0x2058

Bit(s)	R/W	Default	Description
3:2	R/W	0	wrarb_arb_busy : unsigned , default = 0
1:0	R/W	0	rdarb_arb_busy : unsigned , default = 0

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Table 9-233 DI_ARB_DBG_CTRL_L1C1 0x2059

Bit(s)	R/W	Default	Description
31:0	R/W	8	det_cmd_ctrl : unsigned , default = 8

Table 9-234 DI_ARB_DBG_STAT_L1C1 0x205a

Bit(s)	R/W	Default	Description
31:0	R/W	0	det_dbg_stat : unsigned , default = 0

Table 9-235 DI_RDARB_UGT_L1C1 0x205b

Bit(s)	R/W	Default	Description
15:0	R/W	0x0	rdarb_ugt_basic : unsigned , default = {8{2'b1}};

Table 9-236 DI_RDARB_LIMT0_L1C1 0x205c

Bit(s)	R/W	Default	Description
31:0	R/W	0x0	rdarb_req_limt_num : unsigned , default = {2{16'h3f3f}};

Table 9-237 DI_WRARB_UGT_L1C1 0x205d

Bit(s)	R/W	Default	Description
11:0	R/W	0	wrarb_ugt_basic : unsigned , default = 0

Table 9-238 DI_SUB_RDARB_MODE 0x37c0

Bit(s)	R/W	Default	Description
23:16	R/W	0	rdarb_sel : uns, default = 0 , rdarb_sel [0]==0 slave dc0 connect master port0 rdarb_sel[0]==1 slave dc0 connect master port1 rdarb_sel [1]==0 slave dc1 connect master port0 rdarb_sel[1]==1 slave dc1 connect master port1 rdarb_sel [2]==0 slave dc2 connect master port0 rdarb_sel[2]==1 slave dc2 connect master port1 rdarb_sel [3]==0 slave dc3 connect master port0 rdarb_sel[3]==1 slave dc3 connect master port1 rdarb_sel [4]==0 slave dc4 connect master port0 rdarb_sel [4]==1 slave dc4 connect master port1 rdarb_sel [5]==0 slave dc5 connect master port0 rdarb_sel[5]==1 slave dc5 connect master port1 rdarb_sel [6]==0 slave dc5 connect master port0 rdarb_sel[6]==1 slave dc6 connect master port1 rdarb_sel [7]==0 slave dc5 connect master port0 rdarb_sel[7]==1 slave dc7 connect master port1
9:8	R/W	0	rdarb_arb_mode : uns, default = 0 , rdarb_arb_mode [0] master port0 arb way, rdarb_arb_mode [1] master port1 arb way,
3:0	R/W	0	rdarb_gate_clk_ctrl : uns, default = 0 , rdarb_gate_clk_ctrl [1:0] master port0 clk gate control rdarb_gate_clk_ctrl [3:2] master port1 clk gate control

Table 9-239 DI_SUB_RDARB_REQEN_SLV 0x37c1

Bit(s)	R/W	Default	Description
15:0	R/W	0xffff	rdarb_dc_req_en : uns, default = 16'hffff , slv0~slv7 enable to mst.

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Table 9-240 DI_SUB_RDARB_WEIGH0_SLV 0x37c2

Bit(s)	R/W	Default	Description
29:0	R/W	0	rddc_weigh_sxn : unsigned , default = 0 rddc_weigh_sxn [0*6+:6]: the slv0 req weigh number rddc_weigh_sxn [1*6+:6]: the slv1 req weigh number rddc_weigh_sxn [2*6+:6]: the slv2 req weigh number rddc_weigh_sxn [3*6+:6]: the slv3 req weigh number rddc_weigh_sxn [4*6+:6]: the slv4 req weigh number

Table 9-241 DI_SUB_RDARB_WEIGH1_SLV 0x37c3

Bit(s)	R/W	Default	Description
17:0	R/W	0	rddc_weigh_sxn : unsigned , default = 0 rddc_weigh_sxn [0*6+:6]: the slv6 req weigh number rddc_weigh_sxn [1*6+:6]: the slv7 req weigh number rddc_weigh_sxn [2*6+:6]: the slv8 req weigh number

Table 9-242 DI_SUB_RDARB_UGT 0x37c4

Bit(s)	R/W	Default	Description
15:0	R/W	0x0	rdarb_ugt_basic : unsigned , default = {8'{2'h1}} rdarb_ugt_basic [0*1+:2]: 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 10 : use the input arguen rdarb_ugt_basic [1*2+:2]: 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 10 : use the input arguen rdarb_ugt_basic [2*2+:2]: 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 10 : use the input arguen rdarb_ugt_basic [3*2+:2]: 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 10 : use the input arguen rdarb_ugt_basic [4*2+:2]: 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 10 : use the input arguen rdarb_ugt_basic [5*2+:2]: 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 10 : use the input arguen rdarb_ugt_basic [6*2+:2]: 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 10 : use the input arguen rdarb_ugt_basic [7*2+:2]: 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 10 : use the input arguen

Table 9-243 DI_SUB_RDARB_LIMT0 0x37c5

Bit(s)	R/W	Default	Description
31:0	R/W	0x0	rdarb_req_limt_num : unsigned , default = {2{16'h3f3f}}

Table 9-244 DI_SUB_WRARB_MODE 0x37c6

Bit(s)	R/W	Default	Description
21:16	R/W	0	wrarb_sel : uns, default = 0 , wrarb_sel [0]==0 slave dc0 connect master port0 wrarb_sel[0]==1 slave dc0 connect master port1 wrarb_sel [1]==0 slave dc1 connect master port0 wrarb_sel[1]==1 slave dc1 connect master port1 wrarb_sel [2]==0 slave dc2 connect master port0 wrarb_sel[2]==1 slave dc2 connect master port1 wrarb_sel [3]==0 slave dc3 connect master port0 wrarb_sel[3]==1 slave dc3 connect master port1 wrarb_sel [4]==0 slave dc4 connect master port0 wrarb_sel[4]==1 slave dc3 connect master port1 wrarb_sel [5]==0 slave dc5 connect master port0 wrarb_sel[5]==1 slave dc3 connect master port1
8	R/W	0	wrarb_arb_mode : uns, default = 0 , wrarb_arb_mode[0] master port0 arb way,
1:0	R/W	0	wrarb_gate_clk_ctrl : uns, default = 0 , wrarb_gate_clk_ctrl[1:0] master port0 clk gate control

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Table 9-245 DI_SUB_WRARB_REQEN_SLV 0x37c7

Bit(s)	R/W	Default	Description
5:0	R/W	0	wrarb_dc_req_en : unsigned , default = 0 wrarb_dc_req_en [0]: the slv0 req to mst port0 enable, wrarb_dc_req_en [1]: the slv1 req to mst port0 enable, wrarb_dc_req_en [2]: the slv2 req to mst port0 enable, wrarb_dc_req_en [0]: the slv0 req to mst port1 enable, wrarb_dc_req_en [1]: the slv1 req to mst port1 enable, wrarb_dc_req_en [2]: the slv2 req to mst port1 enable,

Table 9-246 DI_SUB_WRARB_WEIGH0_SLV 0x37c8

Bit(s)	R/W	Default	Description
29:0	R/W	0	wrdc_weigh_sxn : unsigned , default = 0 wrdc_weigh_sxn [0*6+:6]: the slv0 req weigh number wrdc_weigh_sxn [1*6+:6]: the slv1 req weigh number wrdc_weigh_sxn [2*6+:6]: the slv2 req weigh number wrdc_weigh_sxn [3*6+:6]: the slv3 req weigh number wrdc_weigh_sxn [4*6+:6]: the slv4 req weigh number

Table 9-247 DI_SUB_WRARB_WEIGH1_SLV 0x37c9

Bit(s)	R/W	Default	Description
5:0	R/W	0	wrdc_weigh_sxn : unsigned , default = 0 the slv5 req weigh number

Table 9-248 DI_SUB_WRARB_UGT 0x37ca

Bit(s)	R/W	Default	Description
11:0	R/W	0x0	rdarb_ugt_basic : unsigned , default = {8'{2'h1}} rdarb_ugt_basic [0*1+:2]: 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 10 : use the input arguen rdarb_ugt_basic [1*2+:2]: 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 10 : use the input arguen rdarb_ugt_basic [2*2+:2]: 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 10 : use the input arguen rdarb_ugt_basic [3*2+:2]: 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 10 : use the input arguen rdarb_ugt_basic [4*2+:2]: 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 10 : use the input arguen rdarb_ugt_basic [5*2+:2]: 00 : use auto fifo arugt generate the output arugt. 01 : use the register bit control 10 : use the input arguen

Table 9-249 DI_SUB_RDWR_ARB_STATUS 0x37cb

Bit(s)	R/W	Default	Description
2	R.O	0	ro_wrarb_arb_busy : unsigned , default = 0
1	R/W	0x0	reserve :
0	R.O	0	ro_rdarb_arb_busy : unsigned , default = 0

Table 9-250 DI_SUB_ARB_DBG_CTRL 0x37cc

Bit(s)	R/W	Default	Description
31:0	R.O	0	ro_det_cmd_ctrl : unsigned , default = 0

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Table 9-251 DI_SUB_ARB_DBG_STAT 0x37cd

Bit(s)	R/W	Default	Description
31:0	R.O	0	ro_det_dbg_stat : unsigned , default = 0

Table 9-252 CONTRD_CTRL1 0x37d0

Bit(s)	R/W	Default	Description
25:24	R/W	0	reg_sync_sel : unsigned , default = 0
23:16	R/W	0	reg_canvas_id : unsigned , default = 0
14:12	R/W	1	reg_cmd_intr_len : unsigned , default = 1
11:10	R/W	1	reg_cmd_req_size : unsigned , default = 1
9:8	R/W	2	reg_burst_len : unsigned , default = 2
7	R/W	0	reg_swap_64bit : unsigned , default = 0
6	R/W	0	reg_little_endian : unsigned , default = 0
5	R/W	0	reg_y_rev : unsigned , default = 0
4	R/W	0	reg_x_rev : unsigned , default = 0
2:0	R/W	1	reg_pack_mode : unsigned , default = 1

Table 9-253 CONTRD_CTRL2 0x37d1

Bit(s)	R/W	Default	Description
31:30	R/W	0	reg_sw_rst : unsigned , default = 0
23:18	R/W	0	reg_gclk_ctrl : unsigned , default = 0
16	R/W	0	urgent
15	R/W	0	auto_urgent_en
14	R/W	0	urgent_wr
7:4	R/W	0	up_th
3:0	R/W	0	dn_th

Table 9-254 CONTRD_SCOPE_X 0x37d2

Bit(s)	R/W	Default	Description
28:16	R/W	0	reg_x_end : unsigned , default = 0
12:0	R/W	0	reg_x_start : unsigned , default = 0

Table 9-255 CONTRD_SCOPE_Y 0x37d3

Bit(s)	R/W	Default	Description
28:16	R/W	0	reg_y_end : unsigned , default = 0
12:0	R/W	0	reg_y_start : unsigned , default = 0

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Table 9-256 CONTRD_RO_STAT 0x37d4

Bit(s)	R/W	Default	Description
15:0	R.O	0	ro_reg_status : unsigned , default = 0

Table 9-257 CONT2RD_CTRL1 0x37d5

Bit(s)	R/W	Default	Description
25:24	R/W	0	reg_sync_sel : unsigned , default = 0
23:16	R/W	0	reg_canvas_id : unsigned , default = 0
14:12	R/W	1	reg_cmd_intr_len : unsigned , default = 1
11:10	R/W	1	reg_cmd_req_size : unsigned , default = 1
9:8	R/W	2	reg_burst_len : unsigned , default = 2
7	R/W	0	reg_swap_64bit : unsigned , default = 0
6	R/W	0	reg_little_endian : unsigned , default = 0
5	R/W	0	reg_y_rev : unsigned , default = 0
4	R/W	0	reg_x_rev : unsigned , default = 0
2:0	R/W	1	reg_pack_mode : unsigned , default = 1

Table 9-258 CONT2RD_CTRL2 0x37d6

Bit(s)	R/W	Default	Description
31:30	R/W	0	reg_sw_rst : unsigned , default = 0
23:18	R/W	0	reg_gclk_ctrl : unsigned , default = 0
16	R/W	0	urgent
15	R/W	0	auto_urgent_en
14	R/W	0	urgent_wr
7:4	R/W	0	up_th
3:0	R/W	0	dn_th

Table 9-259 CONT2RD_SCOPE_X 0x37d7

Bit(s)	R/W	Default	Description
28:16	R/W	0	reg_x_end : unsigned , default = 0
12:0	R/W	0	reg_x_start : unsigned , default = 0

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Table 9-260 CONT2RD_SCOPE_Y 0x37d8

Bit(s)	R/W	Default	Description
28:16	R/W	0	reg_y_end : unsigned , default = 0
12:0	R/W	0	reg_y_start : unsigned , default = 0

Table 9-261 CONT2RD_RO_STAT 0x37d9

Bit(s)	R/W	Default	Description
15:0	R.O	0	ro_reg_status : unsigned , default = 0

Table 9-262 MTNRD_CTRL1 0x37da

Bit(s)	R/W	Default	Description
25:24	R/W	0	reg_sync_sel : unsigned , default = 0
23:16	R/W	0	reg_canvas_id : unsigned , default = 0
14:12	R/W	1	reg_cmd_intr_len : unsigned , default = 1
11:10	R/W	1	reg_cmd_req_size : unsigned , default = 1
9:8	R/W	2	reg_burst_len : unsigned , default = 2
7	R/W	0	reg_swap_64bit : unsigned , default = 0
6	R/W	0	reg_little_endian : unsigned , default = 0
5	R/W	0	reg_y_rev : unsigned , default = 0
4	R/W	0	reg_x_rev : unsigned , default = 0
2:0	R/W	1	reg_pack_mode : unsigned , default = 1

Table 9-263 MTNRD_CTRL2 0x37db

Bit(s)	R/W	Default	Description
31:30	R/W	0	reg_sw_rst : unsigned , default = 0
23:18	R/W	0	reg_gclk_ctrl : unsigned , default = 0
16	R/W	0	urgent
15	R/W	0	auto_urgent_en
14	R/W	0	urgent_wr
7:4	R/W	0	up_th
3:0	R/W	0	dn_th

Table 9-264 MTNRD_SCOPE_X 0x37dc

Bit(s)	R/W	Default	Description
28:16	R/W	0	reg_x_end : unsigned , default = 0
12:0	R/W	0	reg_x_start : unsigned , default = 0

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Table 9-265 MTNRD_SCOPE_Y 0x37dd

Bit(s)	R/W	Default	Description
28:16	R/W	0	reg_y_end : unsigned , default = 0
12:0	R/W	0	reg_y_start : unsigned , default = 0

Table 9-266 MTNRD_RO_STAT 0x37de

Bit(s)	R/W	Default	Description
15:0	R.O	0	ro_reg_status : unsigned , default = 0

Table 9-267 MCVECRD_CTRL1 0x37df

Bit(s)	R/W	Default	Description
25:24	R/W	0	reg_sync_sel : unsigned , default = 0
23:16	R/W	0	reg_canvas_id : unsigned , default = 0
14:12	R/W	1	reg_cmd_intr_len : unsigned , default = 1
11:10	R/W	1	reg_cmd_req_size : unsigned , default = 1
9:8	R/W	2	reg_burst_len : unsigned , default = 2
7	R/W	0	reg_swap_64bit : unsigned , default = 0
6	R/W	0	reg_little_endian : unsigned , default = 0
5	R/W	0	reg_y_rev : unsigned , default = 0
4	R/W	0	reg_x_rev : unsigned , default = 0
2:0	R/W	1	reg_pack_mode : unsigned , default = 1

Table 9-268 MCVECRD_CTRL2 0x37e0

Bit(s)	R/W	Default	Description
31:30	R/W	0	reg_sw_rst : unsigned , default = 0
23:18	R/W	0	reg_gclk_ctrl : unsigned , default = 0
16	R/W	0	urgent
15	R/W	0	auto_urgent_en
14	R/W	0	urgent_wr
7:4	R/W	0	up_th
3:0	R/W	0	dn_th

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Table 9-269 MCVECRD_SCOPE_X 0x37e1

Bit(s)	R/W	Default	Description
28:16	R/W	0	reg_x_end : unsigned , default = 0
12:0	R/W	0	reg_x_start : unsigned , default = 0

Table 9-270 MCVECRD_SCOPE_Y 0x37e2

Bit(s)	R/W	Default	Description
28:16	R/W	0	reg_y_end : unsigned , default = 0
12:0	R/W	0	reg_y_start : unsigned , default = 0

Table 9-271 MCVECRD_RO_STAT 0x37e3

Bit(s)	R/W	Default	Description
15:0	R.O	0	ro_reg_status : unsigned , default = 0

Table 9-272 MCINFRD_CTRL1 0x37e4

Bit(s)	R/W	Default	Description
25:24	R/W	0	reg_sync_sel : unsigned , default = 0
23:16	R/W	0	reg_canvas_id : unsigned , default = 0
14:12	R/W	1	reg_cmd_intr_len : unsigned , default = 1
11:10	R/W	1	reg_cmd_req_size : unsigned , default = 1
9:8	R/W	2	reg_burst_len : unsigned , default = 2
7	R/W	0	reg_swap_64bit : unsigned , default = 0
6	R/W	0	reg_little_endian : unsigned , default = 0
5	R/W	0	reg_y_rev : unsigned , default = 0
4	R/W	0	reg_x_rev : unsigned , default = 0
2:0	R/W	1	reg_pack_mode : unsigned , default = 1

Table 9-273 MCINFRD_CTRL2 0x37e5

Bit(s)	R/W	Default	Description
31:30	R/W	0	reg_sw_rst : unsigned , default = 0
23:18	R/W	0	reg_gclk_ctrl : unsigned , default = 0
16	R/W	0	urgent
15	R/W	0	auto_urgent_en
14	R/W	0	urgent_wr
7:4	R/W	0	up_th
3:0	R/W	0	dn_th

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Table 9-274 MCINFRD_SCOPE_X 0x37e6

Bit(s)	R/W	Default	Description
28:16	R/W	0	reg_x_end : unsigned , default = 0
12:0	R/W	0	reg_x_start : unsigned , default = 0

Table 9-275 MCINFRD_SCOPE_Y 0x37e7

Bit(s)	R/W	Default	Description
28:16	R/W	0	reg_y_end : unsigned , default = 0
12:0	R/W	0	reg_y_start : unsigned , default = 0

Table 9-276 MCINFRD_RO_STAT 0x37e8

Bit(s)	R/W	Default	Description
15:0	R.O	0	ro_reg_status : unsigned , default = 0

Table 9-277 CONTWR_X 0x37e9

Bit(s)	R/W	Default	Description
31:30	R/W	2	burst_len : unsigned , default = 2
29	R/W	0	rev_x : unsigned , default = 0
28:16	R/W	0	start_x : unsigned , default = 0
12:0	R/W	2	end_x : unsigned , default = 2cf

Table 9-278 CONTWR_Y 0x37ea

Bit(s)	R/W	Default	Description
31:30	R/W	0	canvas_id : unsigned , default = 0
29	R/W	0	rev_y : unsigned , default = 0
28:16	R/W	0	start_y : unsigned , default = 0
12:0	R/W	0	end_y : unsigned , default = 0x1df

Table 9-279 CONTWR_CTRL 0x37eb

Bit(s)	R/W	Default	Description
31:16	R/W	0	urgent_ctrl : unsigned , default = 0
15	R/W	0	force_wvalid : unsigned , default = 0
14	R/W	0	canvas_syncen : unsigned , default = 0
13	R/W	1	canvas_wr : unsigned , default = 1

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Bit(s)	R/W	Default	Description
12	R/W	0	req_en : unsigned , default = 0
10	R/W	0	clr_wrrsp : unsigned , default = 0
8	R/W	0	urgent : unsigned , default = 0
7:0	R/W	0	canvas_index : unsigned , default = 0

Table 9-280 CONTWR_CAN_SIZE 0x37ec

Bit(s)	R/W	Default	Description
30:29	R/W	0	reg_rst : unsigned , default = 0
28:16	R/W	0	hsizem1 : unsigned , default = 0x2cf
14	R/W	0	reg_reset : unsigned , default = 0
13	R/W	0	little_endian : unsigned , default = 0
12:0	R/W	0	vsizem1 : unsigned , default = 0x1df

Table 9-281 MTNWR_X 0x37ed

Bit(s)	R/W	Default	Description
31:30	R/W	2	burst_len : unsigned , default = 2
29	R/W	0	rev_x : unsigned , default = 0
28:16	R/W	0	start_x : unsigned , default = 0
12:0	R/W	2	end_x : unsigned , default = 2cf

Table 9-282 MTNWR_Y 0x37ee

Bit(s)	R/W	Default	Description
31:30	R/W	0	canvas_id : unsigned , default = 0
29	R/W	0	rev_y : unsigned , default = 0
28:16	R/W	0	start_y : unsigned , default = 0
12:0	R/W	0	end_y : unsigned , default = 0x1df

Table 9-283 MTNWR_CTRL 0x37ef

Bit(s)	R/W	Default	Description
31:16	R/W	0	urgent_ctrl : unsigned , default = 0
15	R/W	0	force_wvalid : unsigned , default = 0
14	R/W	0	canvas_syncen : unsigned , default = 0
13	R/W	1	canvas_wr : unsigned , default = 1
12	R/W	0	req_en : unsigned , default = 0
10	R/W	0	clr_wrrsp : unsigned , default = 0

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Bit(s)	R/W	Default	Description
8	R/W	0	urgent : unsigned , default = 0
7:0	R/W	0	canvas_index : unsigned , default = 0

Table 9-284 MTNWR_CAN_SIZE 0x37f0

Bit(s)	R/W	Default	Description
30:29	R/W	0	reg_rst : unsigned , default = 0
28:16	R/W	0	hsizem1 : unsigned , default = 0x2cf
14	R/W	0	reg_reset : unsigned , default = 0
13	R/W	0	little_endian : unsigned , default = 0
12:0	R/W	0	vsizem1 : unsigned , default = 0x1df

Table 9-285 MCVECWR_X 0x37f1

Bit(s)	R/W	Default	Description
31:30	R/W	2	burst_len : unsigned , default = 2
29	R/W	0	rev_x : unsigned , default = 0
28:16	R/W	0	start_x : unsigned , default = 0
12:0	R/W	2	end_x : unsigned , default = 2cf

Table 9-286 MCVECWR_Y 0x37f2

Bit(s)	R/W	Default	Description
31:30	R/W	0	canvas_id : unsigned , default = 0
29	R/W	0	rev_y : unsigned , default = 0
28:16	R/W	0	start_y : unsigned , default = 0
12:0	R/W	0	end_y : unsigned , default = 0x1df

Table 9-287 MCVECWR_CTRL 0x37f3

Bit(s)	R/W	Default	Description
31:16	R/W	0	urgent_ctrl : unsigned , default = 0
15	R/W	0	force_wvalid : unsigned , default = 0
14	R/W	0	canvas_syncen : unsigned , default = 0
13	R/W	1	canvas_wr : unsigned , default = 1
12	R/W	0	req_en : unsigned , default = 0
10	R/W	0	clr_wrrsp : unsigned , default = 0
8	R/W	0	urgent : unsigned , default = 0
7:0	R/W	0	canvas_index : unsigned , default = 0

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Table 9-288 MCVECWR_CAN_SIZE 0x37f4

Bit(s)	R/W	Default	Description
30:29	R/W	0	reg_rst : unsigned , default = 0
28:16	R/W	0	hsizem1 : unsigned , default = 0x2cf
14	R/W	0	reg_reset : unsigned , default = 0
13	R/W	0	little_endian : unsigned , default = 0
12:0	R/W	0	vsizem1 : unsigned , default = 0x1df

Table 9-289 MCINFWR_X 0x37f5

Bit(s)	R/W	Default	Description
31:30	R/W	2	burst_len : unsigned , default = 2
29	R/W	0	rev_x : unsigned , default = 0
28:16	R/W	0	start_x : unsigned , default = 0
12:0	R/W	2	end_x : unsigned , default = 2cf

Table 9-290 MCINFWR_Y 0x37f6

Bit(s)	R/W	Default	Description
31:30	R/W	0	canvas_id : unsigned , default = 0
29	R/W	0	rev_y : unsigned , default = 0
28:16	R/W	0	start_y : unsigned , default = 0
12:0	R/W	0	end_y : unsigned , default = 0x1df

Table 9-291 MCINFWR_CTRL 0x37f7

Bit(s)	R/W	Default	Description
31:16	R/W	0	urgent_ctrl : unsigned , default = 0
15	R/W	0	force_wvalid : unsigned , default = 0
14	R/W	0	canvas_syncen : unsigned , default = 0
13	R/W	1	canvas_wr : unsigned , default = 1
12	R/W	0	req_en : unsigned , default = 0
10	R/W	0	clr_wrrsp : unsigned , default = 0
8	R/W	0	urgent : unsigned , default = 0
7:0	R/W	0	canvas_index : unsigned , default = 0

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Table 9-292 MCINFWR_CAN_SIZE 0x37f8

Bit(s)	R/W	Default	Description
30:29	R/W	0	reg_rst : unsigned , default = 0
28:16	R/W	0	hsizem1 : unsigned , default = 0x2cf
14	R/W	0	reg_reset : unsigned , default = 0
13	R/W	0	little_endian : unsigned , default = 0
12:0	R/W	0	vsizem1 : unsigned , default = 0x1df

9.2.3.6 DI_RMEM_IF0 Registers

Table 9-293 DI_IF0_GEN_REG 0x2030

Bit(s)	R/W	Default	Description
31	R/W	0	ENABLE_FREE_CLK. 0: Gated clock for power saving 1: Free-running clock to drive logic
30	R/W	0	SW_RESET: Write 1 to this bit to generate a pulse to reset everything except registers.
29	R/W	0	RESET_ON_GO_FIELD: Define whether to reset state machines on go_field pulse. 0: No reset on go_field 1: go_field reset everything except registers
28	R/W	0	URGENT_CHROMA: Set urgent level for chroma fifo request from DDR. 0: Non urgent 1: Urgent
27	R/W	0	URGENT_LUMA: Set urgent level for luma fifo request from DDR. 0: Non urgent 1: Urgent
26	R/W	0	Chroma_end_at_last line: For chroma line, similar to luma_end_at_last_line, as below. Not used if data are stored together in one canvas.
25	R/W	0	Luma_end_at_last_line: Control whether continue outputting luma line past last line. 0: Repeat the last line or dummy pixels, after past the last line 1: Stop outputting data, once past the last line.
24-19	R/W	4	Hold_lines: After go_field, the number of lines to hold before the module is enabled.
18	R/W	0	LAST_LINE: This bit controls whether we simply repeat the last line or we push dummy pixels. ‘1’ tells the state-machines to repeat the last line using the dummy pixels defined in the register below. ‘0’ indicates that the state-machine should re-read the last line of real data.
17	R	0	Busy status of the state-machines. ‘1’ = busy, ‘0’ = idle
16	R/W	0	DEMUX_MODE: 0 = 4:2:2, 1 = RGB (24-bit). This value is used to control the de-muxing logic when the picture is stored together. When a picture is stored together, the data is read into a single FIFO (the Y FIFO) and must be demultiplexed into the “drain” outputs. In the case of 4:2:2 the data is assumed to be stored in memory in 16-bit chunks: <YCb><YCr><YCb><YCr>,… the Y, Cb and Cr 8-bit values are pulled from the single Y-FIFO and sent out in pairs. This value is only valid when the picture is stored together. If the picture is separated into different canvases, then this bit field is ignored.

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Bit(s)	R/W	Default	Description
15-14	R/W	0	BYTES_PER_PIXEL: This value is used to determine how many bytes are associated with each pixel. 0: This value should be used if the image is stored separately (e.g. RGB or Y, Cb, Cr). 1: This value should be used if the data is 4:2:2 data stored together. In this case each pixel , YCb or YCr, is 16-bits (two bytes). 2: This value should be used if the RGB (24-bit) data is stored together. 3: reserved for future use (alpha RGB).
13-12	R/W	0	DDR_BURST_SIZE_CR: This value is used to control the DDR burst request size for the Cr FIFO. 0: Maximum burst = 24 64-bit values 1: Maximum burst = 32 64-bit values 2: Maximum burst = 48 64-bit values 3: Maximum burst = 64 64-bit values
11-10	R/W	0	DDR_BURST_SIZE_CB: This value is used to control the DDR burst request size for the Cb FIFO. 0: Maximum burst = 24 64-bit values 1: Maximum burst = 32 64-bit values 2: Maximum burst = 48 64-bit values 3: Maximum burst = 64 64-bit values
9-8	R/W	0	DDR_BURST_SIZE_Y: This value is used to control the DDR burst request size for the Y FIFO. 0: Maximum burst = 24 64-bit values 1: Maximum burst = 32 64-bit values 2: Maximum burst = 48 64-bit values 3: Maximum burst = 64 64-bit values
7	R/W	0	MANUAL_START_FRAME: non-latching bit that can be used to simulate the go_ field signal for simulation.
6	R/W	0	CHRO_RPT_LASTL_CTRL: This bit controls whether to allow VPP's chroma-repeat request. 0: Chroma-repeat pulses from VPP are ignored 1: Chroma-repeat pulses from VPP are used.
5	R/W	0	Unused
4	R/W	0	LITTLE_ENDIAN: This bit defines the endianess of the memory data . 0: Pixel data are stored big-endian in memory 1: Chroma-repeat pulses from VPP are used.
3	R/W	0	Chroma_hz_avg: For chroma line output control, similar to luma_hz_avg, as below. Not used if data are stored together in one canvas.
2	R/W	0	Luma_hz_avg: Enable output half amount of data per line to save bandwidth. 0: Output every pixel per line 1: Output half line, each data averaged between every 2 pixels Note: For 4:2:2 mode data stored together in one canvas, only do averaging over luma data.
1	R/W	0	SEPARATE_EN: Set this bit to 1 if the image is in separate canvas locations.
0	R/W	0	ENABLE: This bit is set to 1 to enable the FIFOs and other logic. This bit can be set to 0 to cleanup and put the logic into an IDLE state.

Table 9-294 DI_IF0_CANVAS0 – Picture 0 0x2031

Bit(s)	R/W	Default	Description
31-24	R/W	0	unused
23-16	R/W	0	CANVAS0_ADDR2: Canvas table address for picture 0 for component 2 (Cr FIFO). This value is ignored when the picture is stored together

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Bit(s)	R/W	Default	Description
15-8	R/W	0	CANVAS0_ADDR1: Canvas table address for picture 0 for component 1 (Cb FIFO). This value is ignored when the picture is stored together
7-0	R/W	0	CANVAS0_ADDR0: Canvas table address for picture 0 for component 0 (Y FIFO).

Table 9-295 DI_IF0_LUMA_X0 – Picture 0 0x2032

Bit(s)	R/W	Default	Description
31	R/W	0	Unused
30-16	R/W	0	LUMA_X_END0: Picture 0, luma X end value
15	R/W	0	Unused
14-0	R/W	0	LUMA_X_START0: Picture 0, luma X start value

Table 9-296 DI_IF0_LUMA_Y0 – Picture 0 0x2033

Bit(s)	R/W	Default	Description
31-29	R/W	0	Unused
28-16	R/W	0	LUMA_Y_END0: Picture 0, luma Y end value
15-13	R/W	0	Unused
12-0	R/W	0	LUMA_Y_START0: Picture 0, luma Y start value

Table 9-297 DI_IF0_CHROMA_X0 – Picture 0 0x2034

Bit(s)	R/W	Default	Description
31	R/W	0	Unused
30-16	R/W	0	CHROMA_X_END0: Picture 0, chroma X end value. This value is only used when the picture is not stored together.
15	R/W	0	Unused
14-0	R/W	0	CHROMA _X_START0: Picture 0, chroma X start value. This value is only used when the picture is not stored together.

Table 9-298 DI_IF0_ CHROMA_Y0 – Picture 0 0x2035

Bit(s)	R/W	Default	Description
31-29	R/W	0	Unused
28-16	R/W	0	CHROMA _Y_END0: Picture 0, chroma Y end value. This value is only used when the picture is not stored together.
15-13	R/W	0	Unused
12-0	R/W	0	CHROMA _Y_START0: Picture 0, chroma Y start value. This value is only used when the picture is not stored together.

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Table 9-299 DI_IF0_REPEAT_LOOP – Pictures 0 and 1 0x2036

Bit(s)	R/W	Default	Description
31-24	R/W	0	CHROMA_RPT_LOOP1: Repeat loop for Picture 1. Bits[6:4] = start loop pointer, bits [2:0] = end loop pointer. Bits [7] and [3] are ignored.
23-16	R/W	0	LUMA_RPT_LOOP1: Repeat loop for Picture 1. Bits[6:4] = start loop pointer, bits [2:0] = end loop pointer. Bits [7] and [3] are ignored.
15-8	R/W	0	CHROMA_RPT_LOOP0: Repeat loop for Picture 0. Bits[6:4] = start loop pointer, bits [2:0] = end loop pointer. Bits [7] and [3] are ignored.
7-0	R/W	0	LUMA_RPT_LOOP0: Repeat loop for Picture 0. Bits[6:4] = start loop pointer, bits [2:0] = end loop pointer. Bits [7] and [3] are ignored.

Table 9-300 DI_IF0_LUMA0_RPT_PAT – Picture 0 LUMA repeat pattern 0x2037

Bit(s)	R/W	Default	Description
31-0	R/W	0	Luma repeat/skip pattern for picture 0

Bits	Pattern Index	Pattern description
31-28	7	Repeat/skip pattern: Bit[3] = 0 indicates repeat. Bit[3] = 1 indicates either skip, or output this line and then skip. How to interpret this bit depends on the value of the previous pattern's Bit[3]. If previous Bit[3]=0, then skip; If previous Bit[3]=1, then output this line and then skip. Bits[2:0] indicate the skip / repeat count. Blow is an example of consecutive patterns, the start line is line 0: {0010} Repeat this line (line 0) two more times for a total of three line reads. Proceed to next line (line 1). {0000} Don't repeat this line (line 1). This line will be read just once. Proceed to next line (line 2). {1000} Skip one line (line 2) to get to the next line (line 3). The skip implies that the next line (line 3) should be read at least once. {1011} Read this line (line 3) once, and then skip the next four lines to get to the next line (line 8). The skip implies that the next line (line 8) should be read at least once. {0100} Repeat this line (line 8) four more times for a total of five line read. Proceed to next line (line 9). {1001} Skip two lines to get to the next line (line 11). The skip implies that the next line (line 11) should be read at least once.
27-24	6	See pattern definition above.
23-20	5	See pattern definition above.
19-16	4	See pattern definition above.
15-12	3	See pattern definition above.
11-8	2	See pattern definition above.
7-4	1	See pattern definition above.
3-0	0	See pattern definition above.

Table 9-301 DI_IF0_CHROMA0_RPT_PAT – Picture 0 CHROMA repeat pattern 0x2038

Bit(s)	R/W	Default	Description
31-0	R/W	0	Chroma repeat/skip pattern for picture 0. See picture 0 luma pattern for description. This value is only used when the picture is not stored together.

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Table 9-302 DI_IF0_DUMMY_PIXEL 0x2039

Bit(s)	R/W	Default	Description
31-24	R/W	0	Y or R dummy pixel value
23-16	R/W	0	Cb or G dummy pixel value
15-8	R/W	0	Cr or B dummy pixel value
7-0	R/W	0	unused

Table 9-303 DI_IF0_LUMA_FIFO_SIZE 0x203A

Bit(s)	R/W	Default	Description
8-0	W/R	128	fifo size

Table 9-304 DI_IF0_RANGE_MAP_Y 0x203B

Bit(s)	R/W	Default	Description
31-23	W/R	0	din offset
22-15	W/R	0	range map coef
13-10	W/R	0	range map din offset mult
9-1	W/R	0	dout offset
0	W/R	0	range map enable

Table 9-305 DI_IF0_RANGE_MAP_CB 0x203C

Bit(s)	R/W	Default	Description
31-23	W/R	0	din offset
22-15	W/R	0	range map coef
13-10	W/R	0	range map din offset mult
9-1	W/R	0	dout offset
0	W/R	0	range map enable

Table 9-306 DI_IF0_RANGE_MAP_CR 0x203D

Bit(s)	R/W	Default	Description
31-23	W/R	0	din offset
22-15	W/R	0	range map coef
13-10	W/R	0	range map din offset mult
9-1	W/R	0	dout offset
0	W/R	0	range map enable

Output data range conversion function:

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Y [n] = clip (Round (((Y [n] +DIN_OFFSET) * RANGE_MAP_COEF) / (1<< RANGE_MAP_SR)) +DOUT_OFFSET);

To perform VC-1 range reduction, set the following:

DIN_OFFSET = 0x180 = -128;

RANGE_MAP_COEF = RANGE_MAPY + 9

RANGE_MAP_SR = 3

DOUT_OFFSET = 0x080 = 128

To get the equivalent function:

Y[n] = clip((((Y[n]-128) * (RANGE_MAPY + 9) + 4) >> 3) +128);

Table 9-307 Output data range conversion function

Bit(s)	R/W	Default	Description
31-23	R/W	0	DIN_OFFSET
22-15	R/W	0	RANGE_MAP_COEF
14	R/W	0	unused
13-10	R/W	0	RANGE_MAP_SR
9-1	R/W	0	DOUT_OFFSET
0	R/W	0	RANGE_MAP_EN

Table 9-308 DI_IF0_GEN_REG2 0x203E

Bit(s)	R/W	Default	Description
31-30	R/W	0	unused
29	R/W	0	chroma line read sel
28	R/W	0	luma line read sel
25:24	R/W	0	shift_pat_cr
17:16	R/W	0	shift_pat_cb
9-8	R/W	0	shift_pat_y
6	R/W	0	hold_line[6]
3	R/W	0	y_rev
2	R/W	0	x_rev
1-0	R/W	0	COLOR_MAP: Define color map for NV12 or NV21 mode. Only applicable when VD1_IF0_GEN_REG.SEPARATE_EN = 1. 0: NOT NV12 or NV21; 1: NV12 (CbCr); 2: NV21 (CrCb).

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Table 9-309 DI_IF0_FMT_CTRL 0x203F

Bit(s)	R/W	Default	Description
31	R/W	0	gate_clk_en. 0=No clock gating, free-running; 1=Enable clock gating for power saving.
30	R/W	0	soft_rst. If true, reset formatters.
29	R/W	0	unused
28	R/W	0	if true, horizontal formatter use repeating to generete pixel, otherwise use bilinear interpolation
27-24	R/W	0	horizontal formatter initial phase
23	R/W	0	horizontal formatter repeat pixel 0 enable
22-21	R/W	0	horizontal Y/C ratio, 00: 1:1, 01: 2:1, 10: 4:1
20	R/W	0	horizontal formatter enable
19	R/W	0	if true, always use phase0 while vertical formater, meaning always repeat data, no interpolation
18	R/W	0	if true, disable vertical formatter chroma repeat last line
17	R/W	0	veritcal formatter dont need repeat line on phase0, 1: enable, 0: disable
16	R/W	0	veritcal formatter repeat line 0 enable
15-12	R/W	0	vertical formatter skip line num at the beginning
11-8	R/W	0	vertical formatter initial phase
7-1	R/W	0	vertical formatter phase step (3.4)
0	R/W	0	vertical formatter enable

Table 9-310 DI_IF0_FMT_W 0x2040

Bit(s)	R/W	Default	Description
27-16	R/W	0	horizontal formatter width
11-0	R/W	0	vertical formatter width

9.2.3.7 VPU_AFBCE Registers

DI AFBCE Registers

Table 9-311 DI_AFBCE_ENABLE 0x2060

Bit(s)	R/W	Default	Description
31:20	R/W	0	gclk_ctrl : unsigned , default = 0, gclk_ctrl of afbe submodule : 1) 12'h000 : gatting afbce clock. 2) 12'hfff : free_run afbce clock. 3) 12'h555 : close afbce clock.
19:16	R/W	0	afbce_sync_sel : unsigned , default = 0, shadow some size/scope/mode registers in afbce 1) 4'hf : sync active. 2) 4'h0: sync close.
13	R/W	0	enc_rst_mode : unsigned , default = 0, frame rst mode bits:

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Bit(s)	R/W	Default	Description
			1:use software reset as frame reset by writting a pulse to register *DI_AFBCE_MODE[29].* 0:use vsync as frame reset.
12	R/W	0	enc_en_mode : unsigned , default = 0, DI_AFBCE start mode bits: 1: DI_AFBCE start_up by writting a pulse to register *DI_AFBCE_ENABLE[0].* 0: DI_AFBCE start_up several line after vsync,line number setting by *DI_AFBCE_MODE[22:16].*
8	R/W	0	enc_enable : unsigned , default = 0, 1: open DI_AFBCE module. 0: close DI_AFBCE module.
0	R/W	0	enc_frm_start : DI_AFBCE start_up bits This bits can start afbce by writting high singal when *DI_AFBCE_ENABLE[12] equal 1.*

Table 9-312 DI_AFBCE_MODE 0x2061

Bit(s)	R/W	Default	Description
31:29	R/W	0	soft_rst : unsigned, default = 0 , bit[0] async rst ,soft_ware ctrl async rst bit[1] sync rst ,soft_ware ctrl sync rst bit[2] sync rst by vsync
27:26	R/W	0	rev_mode : unsigned, default = 0 , reverse mode Useless in afbce
25:24	R/W	3	mif_urgent : unsigned, default = 3 , head mif and body mif urgent bit[0] head axi write urgent. bit[1] body axi write urgent.
22:16	R/W	4	hold_line_num : unsigned, default = 4, hold_line_num
15:14	R/W	1	burst_mode : unsigned, default = 1, 0:burst1 1:burst2 2:burst4
0	R/W	0	reg_fmt444_comb : unsigned, default = 0, Put 444_8bit data into 422 12bit buffer,if hsize > 1024(di_afbce) 0r hsize > 2048 (vdin_afbce),this bit should be high. 0: 444 8bit comb mode close 1: 444 8bit comb mode open

Table 9-313 DI_AFBCE_SIZE_IN 0x2062

Bit(s)	R/W	Default	Description
28:16	R/W	1920	hsize : unsigned, default = 1920 , hsize of afbce encoder buffer
12:0	R/W	1080	vsize : unsigned, default = 1080 , vsize of afbce encoder buffer

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Table 9-314 DI_AFBCE_BLK_SIZE_IN 0x2063

Bit(s)	R/W	Default	Description
28:16	R/W	60	hblk_size : unsigned, default = 60 , blk horz size out unit: 32*4 block hblk_size of afbce encoder buffer
12:0	R/W	270	vblk_size : unsigned, default = 270, blk vert size out unit: 32*4 block vblk_size of afbce encoder buffer

Table 9-315 DI_AFBCE_HEAD_BADDR 0x2064

Bit(s)	R/W	Default	Description
31:0	R/W	0x00	head_baddr : unsigned, default = 32'h00,head_baddr

Table 9-316 DI_AFBCE_MIF_SIZE 0x2065

Bit(s)	R/W	Default	Description
29:28	R/W	32	ddr_blk_size : unsigned, default = 32'd1,ddr_blk_size
26:24	R/W	32	cmd_blk_size : unsigned, default = 32'd3,cmd_blk_size
20:16	R/W	32	uncmp_size : unsigned, default = 32'd20 ,uncmp_size of a uncompressed 32*4 block uncmp_size = ((16*uncmp_bits*sblk_num+7)>>3 +31)/32 << 1
15:0	R/W	32	mmu_page_size : unsigned, default = 32'd4096,mmu_page_size 4096/8192

Table 9-317 DI_AFBCE_PIXEL_IN_HOR_SCOPE 0x2066

Bit(s)	R/W	Default	Description
28:16	R/W	1919	enc_win_end_h : unsigned, default = 1919 ,pic scope hor end
12:0	R/W	0	enc_win_bgn_h : unsigned, default = 0 ,pic scope hor bgn

Table 9-318 DI_AFBCE_PIXEL_IN_VER_SCOPE 0x2067

Bit(s)	R/W	Default	Description
28:16	R/W	1079	enc_win_end_v : unsigned, default = 1079 ,pic scope ver end
12:0	R/W	0	enc_win_bgn_v : unsigned, default = 0 ,pic scope ver bgn

Table 9-319 DI_AFBCE_CONV_CTRL 0x2068

Bit(s)	R/W	Default	Description
28:16	R/W	2048	fmt_ybuf_depth : unsigned, default = 2048,fmt_ybuf_depth,fixed
11: 0	R/W	256	lbuf_depth : unsigned, default = 256, lbuf_depth,fixed

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Table 9-320 DI_AFBCE_MIF_HOR_SCOPE 0x2069

Bit(s)	R/W	Default	Description
25:16	R/W	0	blk_end_h : unsigned, default = 0 ,blk scope horend
9:0	R/W	59	blk_bgn_h : unsigned, default = 59 ,blk scope horbgn

Table 9-321 DI_AFBCE_MIF_VER_SCOPE 0x206a

Bit(s)	R/W	Default	Description
27:16	R/W	0	blk_end_v : unsigned, default = 0 ,blk scope ver end
11:0	R/W	269	blk_bgn_v : unsigned, default = 269 ,blk scope ver bgn

Table 9-322 DI_AFBCE_STAT1 0x206b

Bit(s)	R/W	Default	Description
31	R.O	0	ro_frm_end_pulse1 : unsigned, RO,default = 0 ;frame end status
30:0	R.O	0	ro_dbg_top_info1 : unsigned, RO,default = 0 ,ro_dbg_top_info1

Table 9-323 DI_AFBCE_STAT2 0x206c

Bit(s)	R/W	Default	Description
30:0	R.O	0	ro_dbg_top_info2 : unsigned, RO,default = 0 ,ro_dbg_top_info2

Table 9-324 DI_AFBCE_FORMAT 0x206d

Bit(s)	R/W	Default	Description
9: 8	R/W	2	reg_format_mode : // unsigned , RW, default = 2 data format; 0 :YUV444/RGB, 1 :YUV422, 2 :YUV420,
7: 4	R/W	10	reg_compbits_c : // unsigned , RW, default = 10 chroma bitwidth 8 or 10
3: 0	R/W	10	reg_compbits_y : // unsigned , RW, default = 10 luma bitwidth 8 or 10

Table 9-325 DI_AFBCE_MODE_EN 0x206e

Bit(s)	R/W	Default	Description
25	R/W	0	reg_adpt_interleave_ymode : // unsigned , RW, default = 0 force 0 to disable it: no HW implementation
24	R/W	0	reg_adpt_interleave_cmode : // unsigned , RW, default = 0 force 0 to disable it: not HW implementation
23	R/W	1	reg_adpt_yinterleave_luma_ride : // unsigned , RW, default = 1 vertical interleave piece luma reorder ride; 0: no reorder ride; 1: w/4 as ride
22	R/W	1	reg_adpt_yinterleave_chrm_ride : // unsigned , RW, default = 1 vertical interleave piece chroma reorder ride; 0: no reorder ride; 1: w/2 as ride
21	R/W	1	reg_adpt_xinterleave_luma_ride : // unsigned , RW, default = 1 vertical interleave piece luma reorder ride; 0: no reorder ride; 1: w/4 as ride

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Bit(s)	R/W	Default	Description
20	R/W	1	reg_adpt_xinterleave_chrm_ride : // unsigned , RW, default = 1 vertical inter-leave piece chroma reorder ride; 0: no reorder ride; 1: w/2 as ride
18	R/W	0	reg_disable_order_mode_i_6 : // unsigned , RW, default = 0 disable order mode0~6: each mode with one disable bit: 0: no disable, 1: diable
17	R/W	0	reg_disable_order_mode_i_5 : // unsigned , RW, default = 0 disable order mode0~6: each mode with one disable bit: 0: no disable, 1: diable
16	R/W	0	reg_disable_order_mode_i_4 : // unsigned , RW, default = 0 disable order mode0~6: each mode with one disable bit: 0: no disable, 1: diable
15	R/W	0	reg_disable_order_mode_i_3 : // unsigned , RW, default = 0 disable order mode0~6: each mode with one disable bit: 0: no disable, 1: diable
14	R/W	0	reg_disable_order_mode_i_2 : // unsigned , RW, default = 0 disable order mode0~6: each mode with one disable bit: 0: no disable, 1: diable
13	R/W	0	reg_disable_order_mode_i_1 : // unsigned , RW, default = 0 disable order mode0~6: each mode with one disable bit: 0: no disable, 1: diable
12	R/W	0	reg_disable_order_mode_i_0 : // unsigned , RW, default = 0 disable order mode0~6: each mode with one disable bit: 0: no disable, 1: diable
10	R/W	0	reg_minval_yenc_en : // unsigned , RW, default = 0 force disable, final deci-sion to remove this ws 1% performance loss
9	R/W	0	reg_16x4block_enable : // unsigned , RW, default = 0 block as mission, but permit 16x4 block
8	R/W	0	reg_uncompress_split_mode : // unsigned , RW, default = 0 0: no split; 1: split
5	R/W	0	reg_input_padding_uv128 : // unsigned , RW, default = 0 input picture 32x4 block gap mode: 0: pad uv=0; 1: pad uv=128
4	R/W	0	reg_dwds_padding_uv128 : // unsigned , RW, default = 0 downsampled image for double write 32x gap mode: 0: pad uv=0; 1: pad uv=128
3: 1	R/W	0	reg_force_order_mode_value : // unsigned , RW, default = 0 force order mode 0~7
0	R/W	0	reg_force_order_mode_en : // unsigned , RW, default = 0 force order mode enable: 0: no force; 1: forced to force_value

Table 9-326 DI_AFBCE_DWSCALAR 0x206f

Bit(s)	R/W	Default	Description
7: 6	R/W	3	reg_dwscalar_w0 : // unsigned , RW, default = 3 horizontal 1st step scalar mode: 0: 1:1 no scalar; 1: 2:1 data drop (0,2,4, 6) pixel kept; 2: 2:1 data drop (1, 3, 5,7..) pixels kept; 3: avg
5: 4	R/W	0	reg_dwscalar_w1 : // unsigned , RW, default = 0 horizontal 2nd step scalar mode: 0: 1:1 no scalar; 1: 2:1 data drop (0,2,4, 6) pixel kept; 2: 2:1 data drop (1, 3, 5,7..) pixels kept; 3: avg
3: 2	R/W	2	reg_dwscalar_h0 : // unsigned , RW, default = 2 vertical 1st step scalar mode: 0: 1:1 no scalar; 1: 2:1 data drop (0,2,4, 6) pixel kept; 2: 2:1 data drop (1, 3, 5,7..) pixels kept; 3: avg
1: 0	R/W	3	reg_dwscalar_h1 : // unsigned , RW, default = 3 vertical 2nd step scalar mode: 0: 1:1 no scalar; 1: 2:1 data drop (0,2,4, 6) pixel kept; 2: 2:1 data drop (1, 3, 5,7..) pixels kept; 3: avg

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Table 9-327 DI_AFBCE_DEFCOLOR_1 0x2070

Bit(s)	R/W	Default	Description
23:12	R/W	4095	reg_enc_defalutcolor_3 : // unsigned , RW, default = 4095 Picture wise default color value in [Y Cb Cr]
11: 0	R/W	4095	reg_enc_defalutcolor_0 : // unsigned , RW, default = 4095 Picture wise default color value in [Y Cb Cr]

Table 9-328 DI_AFBCE_DEFCOLOR_2 0x2071

Bit(s)	R/W	Default	Description
23:12	R/W	2048	reg_enc_defalutcolor_2 : // unsigned , RW, default = 2048 wise default color value in [Y Cb Cr]
11: 0	R/W	2048	reg_enc_defalutcolor_1 : // unsigned , RW, default = 2048 wise default color value in [Y Cb Cr]

Table 9-329 DI_AFBCE_QUANT_ENABLE 0x2072

Bit(s)	R/W	Default	Description
11	R/W	0	reg_quant_expand_en_1 : // unsigned , RW, default = 0 enable for quantization value expansion
10	R/W	0	reg_quant_expand_en_0 : // unsigned , RW, default = 0 enable for quantization value expansion
9: 8	R/W	0	reg_bcleav_ofst : // signed , RW, default = 0 bcleave ofset to get lower range, especially under lossy, for v1/v2, x=0 is equivalent, default = -1;
4	R/W	0	reg_quant_enable_1 : // unsigned , RW, default = 0 enable for quant to get some lossy
0	R/W	0	reg_quant_enable_0 : // unsigned , RW, default = 0 enable for quant to get some lossy

Table 9-330 DI_AFBCE_IQUANT_LUT_1 0x2073

Bit(s)	R/W	Default	Description
30:28	R/W	0	reg_iquant_yclut_0_11 : // unsigned , RW, default = 0 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
26:24	R/W	1	reg_iquant_yclut_0_10 : // unsigned , RW, default = 1 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
22:20	R/W	2	reg_iquant_yclut_0_9 : // unsigned , RW, default = 2 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
18:16	R/W	3	reg_iquant_yclut_0_8 : // unsigned , RW, default = 3 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
14:12	R/W	4	reg_iquant_yclut_0_7 : // unsigned , RW, default = 4 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
10: 8	R/W	5	reg_iquant_yclut_0_6 : // unsigned , RW, default = 5 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)

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Bit(s)	R/W	Default	Description
6: 4	R/W	5	reg_iquant_yclut_0_5 : // unsigned , RW, default = 5 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
2: 0	R/W	4	reg_iquant_yclut_0_4 : // unsigned , RW, default = 4 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)

Table 9-331 DI_AFBCE_IQUANT_LUT_2 0x2074

Bit(s)	R/W	Default	Description
14:12	R/W	3	reg_iquant_yclut_0_3 : // unsigned , RW, default = 3 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
10: 8	R/W	2	reg_iquant_yclut_0_2 : // unsigned , RW, default = 2 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
6: 4	R/W	1	reg_iquant_yclut_0_1 : // unsigned , RW, default = 1 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
2: 0	R/W	0	reg_iquant_yclut_0_0 : // unsigned , RW, default = 0 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)

Table 9-332 DI_AFBCE_*IQUANT*_LUT_3 0x2075

Bit(s)	R/W	Default	Description
30:28	R/W	0	reg_iquant_yclut_1_11 : // unsigned , RW, default = 0 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
26:24	R/W	1	reg_iquant_yclut_1_10 : // unsigned , RW, default = 1 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
22:20	R/W	2	reg_iquant_yclut_1_9 : // unsigned , RW, default = 2 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
18:16	R/W	3	reg_iquant_yclut_1_8 : // unsigned , RW, default = 3 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
14:12	R/W	4	reg_iquant_yclut_1_7 : // unsigned , RW, default = 4 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
10: 8	R/W	5	reg_iquant_yclut_1_6 : // unsigned , RW, default = 5 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
6: 4	R/W	5	reg_iquant_yclut_1_5 : // unsigned , RW, default = 5 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
2: 0	R/W	4	reg_iquant_yclut_1_4 : // unsigned , RW, default = 4 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)

Table 9-333 DI_AFBCE_IQUANT_LUT_4 0x2076

Bit(s)	R/W	Default	Description
14:12	R/W	3	reg_iquant_yclut_1_3 : // unsigned , RW, default = 3 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
10: 8	R/W	2	reg_iquant_yclut_1_2 : // unsigned , RW, default = 2 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)

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Bit(s)	R/W	Default	Description
6: 4	R/W	1	reg_iquant_yclut_1_1 : // unsigned , RW, default = 1 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
2: 0	R/W	0	reg_iquant_yclut_1_0 : // unsigned , RW, default = 0 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)

Table 9-334 DI_AFBCE_RQUANT_LUT_1 0x2077

Bit(s)	R/W	Default	Description
30:28	R/W	5	reg_rquant_yclut_0_11 : // unsigned , RW, default = 5 quantization lut for bctree leavs, quant=2^lut(bc_leav_r+1), can be calculated from iquant_yclut(fw_setting)
26:24	R/W	5	reg_rquant_yclut_0_10 : // unsigned , RW, default = 5
22:20	R/W	4	reg_rquant_yclut_0_9 : // unsigned , RW, default = 4
18:16	R/W	4	reg_rquant_yclut_0_8 : // unsigned , RW, default = 4
14:12	R/W	3	reg_rquant_yclut_0_7 : // unsigned , RW, default = 3
10: 8	R/W	3	reg_rquant_yclut_0_6 : // unsigned , RW, default = 3
6: 4	R/W	2	reg_rquant_yclut_0_5 : // unsigned , RW, default = 2
2: 0	R/W	2	reg_rquant_yclut_0_4 : // unsigned , RW, default = 2

Table 9-335 DI_AFBCE_RQUANT_LUT_2 0x2078

Bit(s)	R/W	Default	Description
14:12	R/W	1	reg_rquant_yclut_0_3 : // unsigned , RW, default = 1
10: 8	R/W	1	reg_rquant_yclut_0_2 : // unsigned , RW, default = 1
6: 4	R/W	0	reg_rquant_yclut_0_1 : // unsigned , RW, default = 0
2: 0	R/W	0	reg_rquant_yclut_0_0 : // unsigned , RW, default = 0

Table 9-336 DI_AFBCE_RQUANT_LUT_3 0x2079

Bit(s)	R/W	Default	Description
30:28	R/W	5	reg_rquant_yclut_1_11 : // unsigned , RW, default = 5 quantization lut for bctree leavs, quant=2^lut(bc_leav_r+1), can be calculated from iquant_yclut(fw_setting)
26:24	R/W	5	reg_rquant_yclut_1_10 : // unsigned , RW, default = 5
22:20	R/W	4	reg_rquant_yclut_1_9 : // unsigned , RW, default = 4
18:16	R/W	4	reg_rquant_yclut_1_8 : // unsigned , RW, default = 4
14:12	R/W	3	reg_rquant_yclut_1_7 : // unsigned , RW, default = 3
10: 8	R/W	3	reg_rquant_yclut_1_6 : // unsigned , RW, default = 3
6: 4	R/W	2	reg_rquant_yclut_1_5 : // unsigned , RW, default = 2
2: 0	R/W	2	reg_rquant_yclut_1_4 : // unsigned , RW, default = 2

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Table 9-337 DI_AFBCE_RQUANT_LUT_4 0x207a

Bit(s)	R/W	Default	Description
14:12	R/W	1	reg_rquant_yclut_1_3 : // unsigned , RW, default = 1
10: 8	R/W	1	reg_rquant_yclut_1_2 : // unsigned , RW, default = 1
6: 4	R/W	0	reg_rquant_yclut_1_1 : // unsigned , RW, default = 0
2: 0	R/W	0	reg_rquant_yclut_1_0 : // unsigned , RW, default = 0

Table 9-338 DI_AFBCE_YUV_FORMAT_CONV_MODE 0x207b

Bit(s)	R/W	Default	Description
6: 4	R/W	0	reg_444to422_mode : // unsigned , RW, default = 0
2: 0	R/W	0	reg_422to420_mode : // unsigned , RW, default = 0

Table 9-339 DI_AFBCE_DUMMY_DATA 0x207c

Bit(s)	R/W	Default	Description
29: 0	R/W	0	reg_dummy_data : // unsigned , default = 0 ,bit[9:0] v bit[19:10] U bit[29:20] Y

Table 9-340 DI_AFBCE_CLR_FLAG 0x207d

Bit(s)	R/W	Default	Description
2	R/W	0	frm_din_end_clr : // unsigned, default = 0
1	R/W	0	enc_error_clr : // unsigned, default = 0
0	R/W	0	frm_end_clr : // unsigned, default = 0

Table 9-341 DI_AFBCE_STA_FLAGT 0x207e

Bit(s)	R/W	Default	Description
31:28	R.O	0	reverse
27	R.O	0	ro_init_end_flag;//init phas end
26	R.O	0	ro_din_frm_end_flag;//data din finished
25:24	R.O	0	enc_st 0:idle 1:enc 2:hold 3:wait
23:21	R.O	0	emit_st 0:idle 1:tx_bcrot 2:tx_bc_lev 3:tx_zcd 4:tx_tree 5:tx_uncmp 6:tx_redu 7:tx_check
20:15	R.O	0	ro_cmd2bresp_cnt: // unsigned, RO,default = 0

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Bit(s)	R/W	Default	Description
14:9	R.O	0	ro_enc2body_cnt: // unsigned, RO,default = 0
8:3	R.O	0	ro_cmd2wd_cnt: // unsigned, RO,default = 0
2	R.O	0	ro_wr_abort_flag: // unsigned, RO,default = 0
1	R.O	0	ro_enc_error_flag: // unsigned, RO,default = 0
0	R.O	0	ro_frm_end_flag: // unsigned, RO,default = 0

Table 9-342 DI_AFBCE_MMU_NUM 0x207f

Bit(s)	R/W	Default	Description
15: 0	R.O	0	ro_frm_mmu_num : // unsigned, RO,default = 0 ,mmu addr have been used in a frame

Table 9-343 DI_AFBCE_MMU_RMIF_CTRL1 0x2080

Bit(s)	R/W	Default	Description
25:24	R/W	0	reg_sync_sel : // unsigned , default = 0, axi canvas id sync with frm rst
23:16	R/W	0	reg_canvas_id : // unsigned , default = 0, axi canvas id num
14:12	R/W	1	reg_cmd_intr_len : // unsigned , default = 1, interrupt send cmd when how many series axi cmd, 0 =12 1=16 2=24 3=32 4=40 5=48 6=56 7=64
11:10	R/W	1	reg_cmd_req_size : // unsigned , default = 1, how many room fifo have, then axi send series req, 0=16 1=32 2=24 3=64
9:8	R/W	2	reg_burst_len : // unsigned , default = 2, burst type: 0-single 1-bst2 2-bst4
7	R/W	0	reg_swap_64bit : // unsigned , default = 0, 64bits of 128bit swap enable
6	R/W	0	reg_little_endian : // unsigned , default = 0, big endian enable
5	R/W	0	reg_y_rev : // unsigned , default = 0, vertical reverse enable
4	R/W	0	reg_x_rev : // unsigned , default = 0, horizontal reverse enable
2:0	R/W	3	reg_pack_mode : // unsigned , default = 3, 0:4bit 1:8bit 2:16bit 3:32bit 4:64bit 5:128bit

Table 9-344 DI_AFBCE_MMU_RMIF_CTRL2 0x2081

Bit(s)	R/W	Default	Description
31:30	R/W	0	reg_sw_rst : // unsigned , default = 0,
23:18	R/W	0x0	reg_gclk_ctrl :
16:0	R/W	0	reg_urgent_ctrl : // unsigned , default = 0, urgent control reg : 16 reg_ugt_init : urgent initial value 15 reg_ugt_en : urgent enable 14 reg_ugt_type : 1= wrmif 0=rdmif 7 :4 reg_ugt_top_th: urgent top threshold 3 :0 reg_ugt_bot_th: urgent bottom threshold

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Table 9-345 DI_AFBCE_MMU_RMIF_CTRL3 0x2082

Bit(s)	R/W	Default	Description
16	R/W	1	reg_acc_mode : // unsigned , default = 1,
12:0	R/W	4096	reg_stride : // unsigned , default = 4096,

Table 9-346 DI_AFBCE_MMU_RMIF_CTRL4 0x2083

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_baddr : // unsigned , default = 0, reg_mmu_baddr

Table 9-347 DI_AFBCE_MMU_RMIF_SCOPE_X 0x2084

Bit(s)	R/W	Default	Description
28:16	R/W	4095	reg_x_end : // unsigned , default = 4095, the canvas hor end pixel position
12: 0	R/W	0	reg_x_start : // unsigned , default = 0, the canvas hor start pixel position

Table 9-348 DI_AFBCE_MMU_RMIF_SCOPE_Y 0x2085

Bit(s)	R/W	Default	Description
28:16	R/W	0	reg_y_end : // unsigned , default = 0, the canvas ver end pixel position
12: 0	R/W	0	reg_y_start : // unsigned , default = 0, the canvas ver start pixel positio

Table 9-349 DI_AFBCE_MMU_RMIF_RO_STAT 0x2086

Bit(s)	R/W	Default	Description
15:0	R/W	0x0	reg_status : // unsigned , reg_status

Table 9-350 DI_AFBCE_PIP_CTRL 0x208a

Bit(s)	R/W	Default	Description
2	R/W		reg_enc_align_en : //unsigned , RW,default = 1,
1	R/W		reg_pip_ini_ctrl : //unsigned , RW,default = 0,
0	R/W		reg_pip_mode : //unsigned , RW,default = 0,

Table 9-351 DI_AFBCE_ROT_CTRL 0x208b

Bit(s)	R/W	Default	Description
4	R.O	0	reg_rot_en : //unsigned , RW,default = 0, rotation enable
3:0	R/W	8	reg_vstep : //unsigned , RW,default = 8, rotation vstep ,setting acorrding rotation shrink mode

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Table 9-352 DI_AFBCE_DIMM_CTRL 0x208c

Bit(s)	R/W	Default	Description
31	R/W	0	reg_dimm_layer_en : //unsigned , RW,default = 0,dimm_layer enable singal
29:0	R/W	0x0008-0200	reg_dimm_data : //unsigned , RW,default = 29'h00080200,dimm_layer data

Table 9-353 DI_AFBCE_BND_DEC_MISC 0x208d

Bit(s)	R/W	Default	Description
27:26	R/W	0	bnd_dec_rev_mode : //unsigned , RW,default = 0 only pip mode use those bits,ususaly don't need configure
25:24	R/W	3	bnd_dec_mif_urgent : //unsigned , RW,default = 3 only pip mode use those bits,ususaly don't need configure
23:22	R/W	2	bnd_dec_burst_len : //unsigned , RW,default = 2 only pip mode use those bits, ususaly don't need configure
21:20	R/W	1	bnd_dec_ddr_blk_size : //unsigned , RW,default = 1 only pip mode use those bits,ususaly don't need configure
18:16	R/W	3	bnd_dec_cmd_blk_size : //unsigned , RW,default = 3 only pip mode use those bits,ususaly don't need configure
14	R/W	0	bnd_dec_blk_mem_mode : //unsigned , RW,default = 0 only pip mode use those bits,ususaly don't need configure
13	R/W	1	bnd_dec_addr_link_en : //unsigned , RW,default = 1 only pip mode use those bits,ususaly don't need configure
12	R/W	0	bnd_dec_always_body_rden : //unsigned , RW,default = 0 only pip mode use those bits,ususaly don't need configure
11:0	R/W	128	bnd_dec_mif_lbuf_depth : //unsigned , RW,default = 128 only pip mode use those bits,ususaly don't need configure

DI AFBCE1 Registers

Table 9-354 DI_AFBCE1_ENABLE 0x20c0

Bit(s)	R/W	Default	Description
31:20	R/W	0	gclk_ctrl : unsigned , default = 0, gclk_ctrl of afbe submodule : 1) 12'h000 : gatting afbce clock. 2) 12'hfff : free_run afbce clock. 3) 12'h555 : close afbce clock.
19:16	R/W	0	afbce_sync_sel : unsigned , default = 0, shadow some size/scope/mode registers in afbce 1) 4'hf : sync active. 2) 4'h0: sync close.
13	R/W	0	enc_rst_mode : unsigned , default = 0, frame rst mode bits: 1:use software reset as frame reset by writting a pulse to register *DI_AFBCE1_MODE[29].* 0:use vsync as frame reset.
12	R/W	0	enc_en_mode : unsigned , default = 0, DI_AFBCE1 start mode bits: 1: DI_AFBCE1 start_up by writting a pulse to register *DI_AFBCE1_ENABLE[0].* 0: DI_AFBCE1 start_up several line after vsync,line number setting by *DI_AFBCE1_MODE[22:16].*

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Bit(s)	R/W	Default	Description
8	R/W	0	enc_enable : unsigned , default = 0, 1: open DI_AFBCE1 module. 0: close DI_AFBCE1 module.
0	R/W	0	enc_frm_start : DI_AFBCE1 start_up bits This bits can start afbce by writting high singal when *DI_AFBCE1_ENABLE[12] equal 1.*

Table 9-355 DI_AFBCE1_MODE 0x20c1

Bit(s)	R/W	Default	Description
31:29	R/W	0	soft_rst : unsigned, default = 0 , bit[0] async rst ,soft_ware ctrl async rst bit[1] sync rst ,soft_ware ctrl sync rst bit[2] sync rst by vsync
27:26	R/W	0	rev_mode : unsigned, default = 0 , reverse mode Useless in afbce
25:24	R/W	3	mif_urgent : unsigned, default = 3 , head mif and body mif urgent bit[0] head axi write urgent. bit[1] body axi write urgent.
22:16	R/W	4	hold_line_num : unsigned, default = 4, hold_line_num
15:14	R/W	1	burst_mode : unsigned, default = 1, 0:burst1 1:burst2 2:burst4
0	R/W	0	reg_fmt444_comb : unsigned, default = 0, Put 444_8bit data into 422 12bit buffer,if hsize > 1024(DI_AFBCE1) 0r hsize > 2048(vdin_afbce),this bit should be high. 0: 444 8bit comb mode close 1: 444 8bit comb mode open

Table 9-356 DI_AFBCE1_SIZE_IN 0x20c2

Bit(s)	R/W	Default	Description
28:16	R/W	1920	hsize : unsigned, default = 1920 , hsize of afbce encoder buffer
12:0	R/W	1080	vsize : unsigned, default = 1080 , vsize of afbce encoder buffer

Table 9-357 DI_AFBCE1_BLK_SIZE_IN 0x20c3

Bit(s)	R/W	Default	Description
28:16	R/W	60	hblk_size : unsigned, default = 60 , blk horz size out unit: 32*4 block hblk_size of afbce encoder buffer
12:0	R/W	270	vblk_size : unsigned, default = 270, blk vert size out unit: 32*4 block vblk_size of afbce encoder buffer

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Table 9-358 DI_AFBCE1_HEAD_BADDR 0x20c4

Bit(s)	R/W	Default	Description
31:0	R/W	0x00	head_baddr : unsigned, default = 32'h00,head_baddr

Table 9-359 DI_AFBCE1_MIF_SIZE 0x20c5

Bit(s)	R/W	Default	Description
29:28	R/W	32	ddr_blk_size : unsigned, default = 32'd1,ddr_blk_size
26:24	R/W	32	cmd_blk_size : unsigned, default = 32'd3,cmd_blk_size
20:16	R/W	32	uncmp_size : unsigned, default = 32'd20 ,uncmp_size of a uncompressed 32*4 block uncmp_size = ((16*uncmp_bits*sblk_num+7)>>3 +31)/32 << 1
15:0	R/W	32	mmu_page_size : unsigned, default = 32'd4096,mmu_page_size 4096/8192

Table 9-360 DI_AFBCE1_PIXEL_IN_HOR_SCOPE 0x20c6

Bit(s)	R/W	Default	Description
28:16	R/W	1919	enc_win_end_h : unsigned, default = 1919 ,pic scope hor end
12:0	R/W	0	enc_win_bgn_h : unsigned, default = 0 ,pic scope hor bgn

Table 9-361 DI_AFBCE1_PIXEL_IN_VER_SCOPE 0x20c7

Bit(s)	R/W	Default	Description
28:16	R/W	1079	enc_win_end_v : unsigned, default = 1079 ,pic scope ver end
12:0	R/W	0	enc_win_bgn_v : unsigned, default = 0 ,pic scope ver bgn

Table 9-362 DI_AFBCE1_CONV_CTRL 0x20c8

Bit(s)	R/W	Default	Description
28:16	R/W	2048	fmt_ybuf_depth : unsigned, default = 2048,fmt_ybuf_depth,fixed
11: 0	R/W	256	lbuf_depth : unsigned, default = 256, lbuf_depth,fixed

Table 9-363 DI_AFBCE1_MIF_HOR_SCOPE 0x20c9

Bit(s)	R/W	Default	Description
25:16	R/W	0	blk_end_h : unsigned, default = 0 ,blk scope horend
9:0	R/W	59	blk_bgn_h : unsigned, default = 59 ,blk scope horbgn

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Table 9-364 DI_AFBCE1_MIF_VER_SCOPE 0x20ca

Bit(s)	R/W	Default	Description
27:16	R/W	0	blk_end_v : unsigned, default = 0 ,blk scope ver end
11:0	R/W	269	blk_bgn_v : unsigned, default = 269 ,blk scope ver bgn

Table 9-365 DI_AFBCE1_STAT1 0x20cb

Bit(s)	R/W	Default	Description
31	R.O	0	ro_frm_end_pulse1 : unsigned, RO,default = 0 ;frame end status
30:0	R.O	0	ro_dbg_top_info1 : unsigned, RO,default = 0 ,ro_dbg_top_info1

Table 9-366 DI_AFBCE1_STAT2 0x20cc

Bit(s)	R/W	Default	Description
30:0	R.O	0	ro_dbg_top_info2 : unsigned, RO,default = 0 ,ro_dbg_top_info2

Table 9-367 DI_AFBCE1_FORMAT 0x20cd

Bit(s)	R/W	Default	Description
9: 8	R/W	2	reg_format_mode : // unsigned , RW, default = 2 data format; 0 :YUV444/RGB, 1 :YUV422, 2 :YUV420,
7: 4	R/W	10	reg_compbits_c : // unsigned , RW, default = 10 chroma bitwidth 8 or 10
3: 0	R/W	10	reg_compbits_y : // unsigned , RW, default = 10 luma bitwidth 8 or 10

Table 9-368 DI_AFBCE1_MODE_EN 0x20ce

Bit(s)	R/W	Default	Description
25	R/W	0	reg_adpt_interleave_ymode : // unsigned , RW, default = 0 force 0 to disable it: no HW implementation
24	R/W	0	reg_adpt_interleave_cmode : // unsigned , RW, default = 0 force 0 to disable it: not HW implementation
23	R/W	1	reg_adpt_yinterleave_luma_ride : // unsigned , RW, default = 1 vertical interleave piece luma reorder ride; 0: no reorder ride; 1: w/4 as ride
22	R/W	1	reg_adpt_yinterleave_chrm_ride : // unsigned , RW, default = 1 vertical interleave piece chroma reorder ride; 0: no reorder ride; 1: w/2 as ride
21	R/W	1	reg_adpt_xinterleave_luma_ride : // unsigned , RW, default = 1 vertical interleave piece luma reorder ride; 0: no reorder ride; 1: w/4 as ride
20	R/W	1	reg_adpt_xinterleave_chrm_ride : // unsigned , RW, default = 1 vertical interleave piece chroma reorder ride; 0: no reorder ride; 1: w/2 as ride
18	R/W	0	reg_disable_order_mode_i_6 : // unsigned , RW, default = 0 disable order mode0~6: each mode with one disable bit: 0: no disable, 1: diable
17	R/W	0	reg_disable_order_mode_i_5 : // unsigned , RW, default = 0 disable order mode0~6: each mode with one disable bit: 0: no disable, 1: diable

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Bit(s)	R/W	Default	Description
16	R/W	0	reg_disable_order_mode_i_4 : // unsigned , RW, default = 0 disable order mode0~6: each mode with one disable bit: 0: no disable, 1: diable
15	R/W	0	reg_disable_order_mode_i_3 : // unsigned , RW, default = 0 disable order mode0~6: each mode with one disable bit: 0: no disable, 1: diable
14	R/W	0	reg_disable_order_mode_i_2 : // unsigned , RW, default = 0 disable order mode0~6: each mode with one disable bit: 0: no disable, 1: diable
13	R/W	0	reg_disable_order_mode_i_1 : // unsigned , RW, default = 0 disable order mode0~6: each mode with one disable bit: 0: no disable, 1: diable
12	R/W	0	reg_disable_order_mode_i_0 : // unsigned , RW, default = 0 disable order mode0~6: each mode with one disable bit: 0: no disable, 1: diable
10	R/W	0	reg_minval_yenc_en : // unsigned , RW, default = 0 force disable, final decision to remove this ws 1% performance loss
9	R/W	0	reg_16x4block_enable : // unsigned , RW, default = 0 block as mission, but permit 16x4 block
8	R/W	0	reg_uncompress_split_mode : // unsigned , RW, default = 0 0: no split; 1: split
5	R/W	0	reg_input_padding_uv128 : // unsigned , RW, default = 0 input picture 32x4 block gap mode: 0: pad uv=0; 1: pad uv=128
4	R/W	0	reg_dwds_padding_uv128 : // unsigned , RW, default = 0 downsampled image for double write 32x gap mode: 0: pad uv=0; 1: pad uv=128
3: 1	R/W	0	reg_force_order_mode_value : // unsigned , RW, default = 0 force order mode 0~7
0	R/W	0	reg_force_order_mode_en : // unsigned , RW, default = 0 force order mode enable: 0: no force; 1: forced to force_value

Table 9-369 DI_AFBCE1_DWSCALAR 0x20cf

Bit(s)	R/W	Default	Description
7: 6	R/W	3	reg_dwscalar_w0 : // unsigned , RW, default = 3 horizontal 1st step scalar mode: 0: 1:1 no scalar; 1: 2:1 data drop (0,2,4, 6) pixel kept; 2: 2:1 data drop (1, 3, 5,7..) pixels kept; 3: avg
5: 4	R/W	0	reg_dwscalar_w1 : // unsigned , RW, default = 0 horizontal 2nd step scalar mode: 0: 1:1 no scalar; 1: 2:1 data drop (0,2,4, 6) pixel kept; 2: 2:1 data drop (1, 3, 5,7..) pixels kept; 3: avg
3: 2	R/W	2	reg_dwscalar_h0 : // unsigned , RW, default = 2 vertical 1st step scalar mode: 0: 1:1 no scalar; 1: 2:1 data drop (0,2,4, 6) pixel kept; 2: 2:1 data drop (1, 3, 5,7..) pixels kept; 3: avg
1: 0	R/W	3	reg_dwscalar_h1 : // unsigned , RW, default = 3 vertical 2nd step scalar mode: 0: 1:1 no scalar; 1: 2:1 data drop (0,2,4, 6) pixel kept; 2: 2:1 data drop (1, 3, 5,7..) pixels kept; 3: avg

Table 9-370 DI_AFBCE1_DEFCOLOR_1 0x20d0

Bit(s)	R/W	Default	Description
23:12	R/W	4095	reg_enc_defalutcolor_3 : // unsigned , RW, default = 4095 Picture wise default color value in [Y Cb Cr]
11: 0	R/W	4095	reg_enc_defalutcolor_0 : // unsigned , RW, default = 4095 Picture wise default color value in [Y Cb Cr]

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Table 9-371 DI_AFBCE1_DEFCOLOR_2 0x20d1

Bit(s)	R/W	Default	Description
23:12	R/W	2048	reg_enc_defalutcolor_2 : // unsigned , RW, default = 2048 wise default color value in [Y Cb Cr]
11: 0	R/W	2048	reg_enc_defalutcolor_1 : // unsigned , RW, default = 2048 wise default color value in [Y Cb Cr]

Table 9-372 DI_AFBCE1_QUANT_ENABLE 0x20d2

Bit(s)	R/W	Default	Description
11	R/W	0	reg_quant_expand_en_1 : // unsigned , RW, default = 0 enable for quantization value expansion
10	R/W	0	reg_quant_expand_en_0 : // unsigned , RW, default = 0 enable for quantization value expansion
9: 8	R/W	0	reg_bcleav_ofst : // signed , RW, default = 0 bcleave ofset to get lower range, especially under lossy, for v1/v2, x=0 is equivalent, default = -1;
4	R/W	0	reg_quant_enable_1 : // unsigned , RW, default = 0 enable for quant to get some lossy
0	R/W	0	reg_quant_enable_0 : // unsigned , RW, default = 0 enable for quant to get some lossy

Table 9-373 DI_AFBCE1_IQUANT_LUT_1 0x20d3

Bit(s)	R/W	Default	Description
30:28	R/W	0	reg_iquant_yclut_0_11 : // unsigned , RW, default = 0 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
26:24	R/W	1	reg_iquant_yclut_0_10 : // unsigned , RW, default = 1 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
22:20	R/W	2	reg_iquant_yclut_0_9 : // unsigned , RW, default = 2 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
18:16	R/W	3	reg_iquant_yclut_0_8 : // unsigned , RW, default = 3 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
14:12	R/W	4	reg_iquant_yclut_0_7 : // unsigned , RW, default = 4 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
10: 8	R/W	5	reg_iquant_yclut_0_6 : // unsigned , RW, default = 5 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
6: 4	R/W	5	reg_iquant_yclut_0_5 : // unsigned , RW, default = 5 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
2: 0	R/W	4	reg_iquant_yclut_0_4 : // unsigned , RW, default = 4 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)

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Table 9-374 DI_AFBCE1_IQUANT_LUT_2 0x20d4

Bit(s)	R/W	Default	Description
14:12	R/W	3	reg_iquant_yclut_0_3 : // unsigned , RW, default = 3 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
10: 8	R/W	2	reg_iquant_yclut_0_2 : // unsigned , RW, default = 2 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
6: 4	R/W	1	reg_iquant_yclut_0_1 : // unsigned , RW, default = 1 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
2: 0	R/W	0	reg_iquant_yclut_0_0 : // unsigned , RW, default = 0 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)

Table 9-375 DI_AFBCE1_IQUANT_LUT_3 0x20d5

Bit(s)	R/W	Default	Description
30:28	R/W	0	reg_iquant_yclut_1_11 : // unsigned , RW, default = 0 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
26:24	R/W	1	reg_iquant_yclut_1_10 : // unsigned , RW, default = 1 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
22:20	R/W	2	reg_iquant_yclut_1_9 : // unsigned , RW, default = 2 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
18:16	R/W	3	reg_iquant_yclut_1_8 : // unsigned , RW, default = 3 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
14:12	R/W	4	reg_iquant_yclut_1_7 : // unsigned , RW, default = 4 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
10: 8	R/W	5	reg_iquant_yclut_1_6 : // unsigned , RW, default = 5 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
6: 4	R/W	5	reg_iquant_yclut_1_5 : // unsigned , RW, default = 5 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
2: 0	R/W	4	reg_iquant_yclut_1_4 : // unsigned , RW, default = 4 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)

Table 9-376 DI_AFBCE1_IQUANT_LUT_4 0x20d6

Bit(s)	R/W	Default	Description
14:12	R/W	3	reg_iquant_yclut_1_3 : // unsigned , RW, default = 3 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
10: 8	R/W	2	reg_iquant_yclut_1_2 : // unsigned , RW, default = 2 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
6: 4	R/W	1	reg_iquant_yclut_1_1 : // unsigned , RW, default = 1 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
2: 0	R/W	0	reg_iquant_yclut_1_0 : // unsigned , RW, default = 0 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)

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Table 9-377 DI_AFBCE1_RQUANT_LUT_1 0x20d7

Bit(s)	R/W	Default	Description
30:28	R/W	5	reg_rquant_yclut_0_11 : // unsigned , RW, default = 5 quantization lut for bctree leavs, quant=2^lut(bc_leav_r+1), can be calculated from iquant_yclut(fw_setting)
26:24	R/W	5	reg_rquant_yclut_0_10 : // unsigned , RW, default = 5
22:20	R/W	4	reg_rquant_yclut_0_9 : // unsigned , RW, default = 4
18:16	R/W	4	reg_rquant_yclut_0_8 : // unsigned , RW, default = 4
14:12	R/W	3	reg_rquant_yclut_0_7 : // unsigned , RW, default = 3
10: 8	R/W	3	reg_rquant_yclut_0_6 : // unsigned , RW, default = 3
6: 4	R/W	2	reg_rquant_yclut_0_5 : // unsigned , RW, default = 2
2: 0	R/W	2	reg_rquant_yclut_0_4 : // unsigned , RW, default = 2

Table 9-378 DI_AFBCE1_RQUANT_LUT_2 0x20d8

Bit(s)	R/W	Default	Description
14:12	R/W	1	reg_rquant_yclut_0_3 : // unsigned , RW, default = 1
10: 8	R/W	1	reg_rquant_yclut_0_2 : // unsigned , RW, default = 1
6: 4	R/W	0	reg_rquant_yclut_0_1 : // unsigned , RW, default = 0
2: 0	R/W	0	reg_rquant_yclut_0_0 : // unsigned , RW, default = 0

Table 9-379 DI_AFBCE1_RQUANT_LUT_3 0x20d9

Bit(s)	R/W	Default	Description
30:28	R/W	5	reg_rquant_yclut_1_11 : // unsigned , RW, default = 5 quantization lut for bctree leavs, quant=2^lut(bc_leav_r+1), can be calculated from iquant_yclut(fw_setting)
26:24	R/W	5	reg_rquant_yclut_1_10 : // unsigned , RW, default = 5
22:20	R/W	4	reg_rquant_yclut_1_9 : // unsigned , RW, default = 4
18:16	R/W	4	reg_rquant_yclut_1_8 : // unsigned , RW, default = 4
14:12	R/W	3	reg_rquant_yclut_1_7 : // unsigned , RW, default = 3
10: 8	R/W	3	reg_rquant_yclut_1_6 : // unsigned , RW, default = 3
6: 4	R/W	2	reg_rquant_yclut_1_5 : // unsigned , RW, default = 2
2: 0	R/W	2	reg_rquant_yclut_1_4 : // unsigned , RW, default = 2

Table 9-380 DI_AFBCE1_RQUANT_LUT_4 0x20da

Bit(s)	R/W	Default	Description
14:12	R/W	1	reg_rquant_yclut_1_3 : // unsigned , RW, default = 1
10: 8	R/W	1	reg_rquant_yclut_1_2 : // unsigned , RW, default = 1

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Bit(s)	R/W	Default	Description
6: 4	R/W	0	reg_rquant_yclut_1_1 : // unsigned , RW, default = 0
2: 0	R/W	0	reg_rquant_yclut_1_0 : // unsigned , RW, default = 0

Table 9-381 DI_AFBCE1_YUV_FORMAT_CONV_MODE 0x20db

Bit(s)	R/W	Default	Description
6: 4	R/W	0	reg_444to422_mode : // unsigned , RW, default = 0
2: 0	R/W	0	reg_422to420_mode : // unsigned , RW, default = 0

Table 9-382 DI_AFBCE1_DUMMY_DATA 0x20dc

Bit(s)	R/W	Default	Description
29: 0	R/W	0	reg_dummy_data : // unsigned , default = 0 ,bit[9:0] v bit[19:10] U bit[29:20] Y

Table 9-383 DI_AFBCE1_CLR_FLAG 0x20dd

Bit(s)	R/W	Default	Description
2	R/W	0	frm_din_end_clr : // unsigned, default = 0
1	R/W	0	enc_error_clr : // unsigned, default = 0
0	R/W	0	frm_end_clr : // unsigned, default = 0

Table 9-384 DI_AFBCE1_STA_FLAGT 0x20de

Bit(s)	R/W	Default	Description
31:28	R.O	0	reverse
27	R.O	0	ro_init_end_flag;//init phas end
26	R.O	0	ro_din_frm_end_flag;//data din finished
25:24	R.O	0	enc_st 0:idle 1:enc 2:hold 3:wait
23:21	R.O	0	emit_st 0:idle 1:tx_bcrot 2:tx_bc_lev 3:tx_zcd 4:tx_tree 5:tx_uncmp 6:tx_redu 7:tx_check
20:15	R.O	0	ro_cmd2bresp_cnt: // unsigned, RO,default = 0
14:9	R.O	0	ro_enc2body_cnt: // unsigned, RO,default = 0
8:3	R.O	0	ro_cmd2wd_cnt: // unsigned, RO,default = 0
2	R.O	0	ro_wr_abort_flag: // unsigned, RO,default = 0

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Bit(s)	R/W	Default	Description
1	R.O	0	ro_enc_error_flag: // unsigned, RO,default = 0
0	R.O	0	ro_frm_end_flag: // unsigned, RO,default = 0

Table 9-385 DI_AFBCE1_MMU_NUM 0x20df

Bit(s)	R/W	Default	Description
15: 0	R.O	0	ro_frm_mmu_num : // unsigned, RO,default = 0 ,mmu addr have been used in a frame

Table 9-386 DI_AFBCE1_MMU_RMIF_CTRL1 0x20e0

Bit(s)	R/W	Default	Description
25:24	R/W	0	reg_sync_sel : // unsigned , default = 0, axi canvas id sync with frm rst
23:16	R/W	0	reg_canvas_id : // unsigned , default = 0, axi canvas id num
14:12	R/W	1	reg_cmd_intr_len : // unsigned , default = 1, interrupt send cmd when how many series axi cmd, 0 =12 1=16 2=24 3=32 4=40 5=48 6=56 7=64
11:10	R/W	1	reg_cmd_req_size : // unsigned , default = 1, how many room fifo have, then axi send series req, 0=16 1=32 2=24 3=64
9:8	R/W	2	reg_burst_len : // unsigned , default = 2, burst type: 0-single 1-bst2 2-bst4
7	R/W	0	reg_swap_64bit : // unsigned , default = 0, 64bits of 128bit swap enable
6	R/W	0	reg_little_endian : // unsigned , default = 0, big endian enable
5	R/W	0	reg_y_rev : // unsigned , default = 0, vertical reverse enable
4	R/W	0	reg_x_rev : // unsigned , default = 0, horizontal reverse enable
2:0	R/W	3	reg_pack_mode : // unsigned , default = 3, 0:4bit 1:8bit 2:16bit 3:32bit 4:64bit 5:128bit

Table 9-387 DI_AFBCE1_MMU_RMIF_CTRL2 0x20e1

Bit(s)	R/W	Default	Description
31:30	R/W	0	reg_sw_rst : // unsigned , default = 0,
23:18	R/W	0x0	reg_gclk_ctrl :
16:0	R/W	0	reg_urgent_ctrl : // unsigned , default = 0, urgent control reg : 16 reg_ugt_init : urgent initial value 15 reg_ugt_en : urgent enable 14 reg_ugt_type : 1= wrmif 0=rdmif 7 :4 reg_ugt_top_th: urgent top threshold 3 :0 reg_ugt_bot_th: urgent bottom threshold

Table 9-388 DI_AFBCE1_MMU_RMIF_CTRL3 0x20e2

Bit(s)	R/W	Default	Description
16	R/W	1	reg_acc_mode : // unsigned , default = 1,
12:0	R/W	4096	reg_stride : // unsigned , default = 4096,

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Table 9-389 DI_AFBCE1_MMU_RMIF_CTRL4 0x20e3

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_baddr : // unsigned , default = 0, reg_mmu_baddr

Table 9-390 DI_AFBCE1_MMU_RMIF_SCOPE_X 0x20e4

Bit(s)	R/W	Default	Description
28:16	R/W	4095	reg_x_end : // unsigned , default = 4095, the canvas hor end pixel position
12: 0	R/W	0	reg_x_start : // unsigned , default = 0, the canvas hor start pixel position

Table 9-391 DI_AFBCE1_MMU_RMIF_SCOPE_Y 0x20e5

Bit(s)	R/W	Default	Description
28:16	R/W	0	reg_y_end : // unsigned , default = 0, the canvas ver end pixel position
12: 0	R/W	0	reg_y_start : // unsigned , default = 0, the canvas ver start pixel positio

Table 9-392 DI_AFBCE1_MMU_RMIF_RO_STAT 0x20e6

Bit(s)	R/W	Default	Description
15:0	R/W	0x0	reg_status : // unsigned , reg_status

Table 9-393 DI_AFBCE1_PIP_CTRL 0x20ea

Bit(s)	R/W	Default	Description
2	R/W		reg_enc_align_en : //unsigned , RW,default = 1,
1	R/W		reg_pip_ini_ctrl : //unsigned , RW,default = 0,
0	R/W		reg_pip_mode : //unsigned , RW,default = 0,

Table 9-394 DI_AFBCE1_ROT_CTRL 0x20eb

Bit(s)	R/W	Default	Description
4	R.O	0	reg_rot_en : //unsigned , RW,default = 0, rotation enable
3:0	R/W	8	reg_vstep : //unsigned , RW,default = 8, rotation vstep ,setting acorrding rotation shrink mode

Table 9-395 DI_AFBCE1_DIMM_CTRL 0x20ec

Bit(s)	R/W	Default	Description
31	R/W	0	reg_dimm_layer_en : //unsigned , RW,default = 0,dimm_layer enable singal
29:0	R/W	0x0008-0200	reg_dimm_data : //unsigned , RW,default = 29'h00080200,dimm_layer data

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Table 9-396 DI_AFBCE1_BND_DEC_MISC 0x20ed

Bit(s)	R/W	Default	Description
27:26	R/W	0	bnd_dec_rev_mode : //unsigned , RW,default = 0 only pip mode use those bits,ususaly don't need configure
25:24	R/W	3	bnd_dec_mif_urgent : //unsigned , RW,default = 3 only pip mode use those bits,ususaly don't need configure
23:22	R/W	2	bnd_dec_burst_len : //unsigned , RW,default = 2 only pip mode use those bits, ususaly don't need configure
21:20	R/W	1	bnd_dec_ddr_blk_size : //unsigned , RW,default = 1 only pip mode use those bits,ususaly don't need configure
18:16	R/W	3	bnd_dec_cmd_blk_size : //unsigned , RW,default = 3 only pip mode use those bits,ususaly don't need configure
14	R/W	0	bnd_dec_blk_mem_mode : //unsigned , RW,default = 0 only pip mode use those bits,ususaly don't need configure
13	R/W	1	bnd_dec_addr_link_en : //unsigned , RW,default = 1 only pip mode use those bits,ususaly don't need configure
12	R/W	0	bnd_dec_always_body_rden : //unsigned , RW,default = 0 only pip mode use those bits,ususaly don't need configure
11:0	R/W	128	bnd_dec_mif_lbuf_depth : //unsigned , RW,default = 128 only pip mode use those bits,ususaly don't need configure

9.2.3.8 VIUB Registers (slow clock)

DI_IF2_GEN_REG 0x2010

Same as DI_IF1_GEN_REG

DI_IF2_CANVAS0 0x2011

Same as DI_IF1_CANVAS0

DI_IF2_LUMA_X0 0x2012

Same as DI_IF1_LUMA_X0

DI_IF2_LUMA_Y0 0x2013

Same as DI_IF1_LUMA_Y0

DI_IF2_CHROMA_X0 0x2014

Same as DI_IF1_CHROMA_X0

DI_IF2_CHROMA_Y0 0x2015

Same as DI_IF1_CHROMA_Y0

DI_IF2_RPT_LOOP 0x2016

Same as DI_IF1_RPT_LOOP

DI_IF2_LUMA0_RPT_PAT 0x2017

Same as DI_IF1_LUMA0_RPT_PAT

DI_IF2_CHROMA0_RPT_PAT 0x2018

Same as DI_IF1_CHROMA0_RPT_PAT

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DI_IF2_DUMMY_PIXEL 0x2019

Same as DI_IF1_DUMMY_PIXEL

DI_IF2_LUMA_FIFO_SIZE 0x201a

Same as DI_IF1_LUMA_FIFO_SIZE

DI_IF2_RANGE_MAP_Y 0x201b

Same as DI_IF1_RANGE_MAP_Y

DI_IF2_RANGE_MAP_CB 0x201c

Same as DI_IF1_RANGE_MAP_CB

DI_IF2_RANGE_MAP_CR 0x201d

Same as DI_IF1_RANGE_MAP_CR

DI_IF2_GEN_REG2 0x201e

Same as DI_IF1_GEN_REG2

DI_IF2_FMT_CTRL 0x201f

Same as DI_IF1_FMT_CTRL

DI_IF2_FMT_W 0x2020

Same as DI_IF1_FMT_W

DI_IF2_URGENT_CTRL 0x2021

Same as DI_IF1_URGENT_CTRL

Table 9-397 DI_IF0_GEN_REG3 0x2042

Bit(s)	R/W	Default	Description
11-10	R/W	0	cntl_dbg_mode
9-8	R/W	0	cntl_bits_mode : 0->8bit 1->10bit 422 2->10bit 444
6-4	R/W	3	cntl_blk_len
2-1	R/W	1	cntl_burst_len
0	R/W	1	cntl_64bit_rev

Table 9-398 DI_IF1_GEN_REG3 0x20a7

Bit(s)	R/W	Default	Description
11-10	R/W	0	cntl_dbg_mode
9-8	R/W	0	cntl_bits_mode : 0->8bit 1->10bit 422 2->10bit 444
6-4	R/W	3	cntl_blk_len
2-1	R/W	1	cntl_burst_len
0	R/W	1	cntl_64bit_rev

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Table 9-399 DI_IF2_GEN_REG3 0x2022

Bit(s)	R/W	Default	Description
11-10	R/W	0	cntl_dbg_mode
9-8	R/W	0	cntl_bits_mode : 0->8bit 1->10bit 422 2->10bit 444
6-4	R/W	3	cntl_blk_len
2-1	R/W	1	cntl_burst_len
0	R/W	1	cntl_64bit_rev

Table 9-400 DI_INP_GEN_REG3 0x20a8

Bit(s)	R/W	Default	Description
11-10	R/W	0	cntl_dbg_mode
9-8	R/W	0	cntl_bits_mode : 0->8bit 1->10bit 422 2->10bit 444
6-4	R/W	3	cntl_blk_len
2-1	R/W	1	cntl_burst_len
0	R/W	1	cntl_64bit_rev

Table 9-401 DI_MEM_GEN_REG3 0x20a9

Bit(s)	R/W	Default	Description
11-10	R/W	0	cntl_dbg_mode
9-8	R/W	0	cntl_bits_mode : 0->8bit 1->10bit 422 2->10bit 444
6-4	R/W	3	cntl_blk_len
2-1	R/W	1	cntl_burst_len
0	R/W	1	cntl_64bit_rev

Table 9-402 DI_CHAN2_GEN_REG3 0x20aa

Bit(s)	R/W	Default	Description
11-10	R/W	0	cntl_dbg_mode
9-8	R/W	0	cntl_bits_mode : 0->8bit 1->10bit 422 2->10bit 444
6-4	R/W	3	cntl_blk_len
2-1	R/W	1	cntl_burst_len
0	R/W	1	cntl_64bit_rev

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9.2.3.9 De-Interlace Registers

De-Interlace mif Registers

Table 9-403 DI_IF1_GEN_REG 0x17E8

Bit(s)	R/W	Default	Description
31	W/R	0	enable free clk
30	W/R	0	sw reset : pulse bit
29	W/R	0	reset on go field
28	W/R	0	urgent chroma
27	W/R	0	urgent luma
26	W/R	0	chroma end at last line : 0 = read last line or push dummy after last line; 1 = stop read after last line
25	W/R	0	luma end at last line : 0 = read last line or push dummy after last line; 1 = stop read after last line
24-19	W/R	4	hold line[5:0], see GEN_REG2[6]
18	W/R	1	last line mode: 0 = read last line; 1 = push fixed value
16	W/R	0	demux mode: 0 = 4:2:2 demux; 1 = RGB demuxing from a single FIFO
15-14	W/R	0	bytes per pixel : 0= 1byte per pixel; 1 = 2 bytes per pixel; 2 = 3bytes per pixel
13-12	W/R	0	burst size cr: 0 = 24x64; 1 = 32x64; 2 = 48x64; 3 = 64x64
11-10	W/R	0	burst size cb: 0 = 24x64; 1 = 32x64; 2 = 48x64; 3 = 64x64
9-8	W/R	0	burst size y: 0 = 24x64; 1 = 32x64; 2 = 48x64; 3 = 64x64
7	W/R	0	start frame manual : pulse bit
6	W/R	0	chroma repeat last1
5	W/R	0	Reserved
4	W/R	0	little endian: 0=Pixels are big-endian in memory; 1=Pixel are little-endian in memory
3	W/R	0	chroma hz avg: 0= output pixel by pixel per line; 1= output half line ,average between every 2 pixels
2	W/R	0	luma_hz_avg: 0= output pixel by pixel per line; 1= output half line ,average between every 2 pixels
1	W/R	0	separate_en: Set to 1 to use 3 separate FIFO’s
0	W/R	0	enable

Table 9-404 DI_IF1_GEN_REG2 0x1790

Bit(s)	R/W	Default	Description
31-30	R/W	0	unused
29	R/W	0	chroma line read sel
28	R/W	0	luma line read sel
25-14	W/R	0	shift pat cr
17-16	W/R	0	shift pat cb

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Bit(s)	R/W	Default	Description
9-8	W/R	0	shift pat y
6	W/R	0	hold_lines[6]
3	W/R	0	y_rev: X read direction: 0=default ,normal read; 1=reverse read
2	W/R	0	x_rev: Y read direction: 0=default ,normal read; 1=reverse read
1-0	W/R	0	color map: 0=default color map as defined by “bytes per pixel”; 1=NV12(CbCr); 2=NV21(CrCb)

Table 9-405 DI_IF1_CANVAS0 0x17E9

Bit(s)	R/W	Default	Description
31	W/R	0	canvas addr syncen
23-16	W/R	0	canvas addr2
15-8	W/R	0	canvas addr1
7-0	W/R	0	canvas addr0

Table 9-406 DI_IF1_LUMA_X0 0x17EA

Bit(s)	R/W	Default	Description
30-16	W/R	0	luma_x_end
14-0	W/R	0	luma_x_start

Table 9-407 DI_IF1_LUMA_Y0 0x17EB

Bit(s)	R/W	Default	Description
28-16	W/R	0	luma_y_end
12-0	W/R	0	luma_y_start

Table 9-408 DI_IF1_CHROMA_X0 0x17EC

Bit(s)	R/W	Default	Description
30-16	W/R	0	chroma_x_end
14-0	W/R	0	chroma_x_start

Table 9-409 DI_IF1_CHROMA_Y0 0x17ED

Bit(s)	R/W	Default	Description
28-16	W/R	0	chroma_y_end
12-0	W/R	0	chroma_y_start

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Table 9-410 DI_IF1_RPT_LOOP 0x17EE

Bit(s)	R/W	Default	Description
15-8	W/R	0	chroma repeat loop
7-0	W/R	0	luma repeat loop

Table 9-411 DI_IF1_LUMA0_RPT_PAT 0x17EF

Bit(s)	R/W	Default	Description
31-0	W/R	0	luma repeat pattern

Table 9-412 DI_IF1_CHROMA0_RPT_PAT 0x17F0

Bit(s)	R/W	Default	Description
7-0	W/R	0	chroma repeat loop

Table 9-413 DI_IF1_DUMMY_PIXEL 0x17F1

Bit(s)	R/W	Default	Description
31-0	W/R	0x8080-00	dummy pixel

Table 9-414 DI_IF1_LUMA_FIFO_SIZE 0x17F2

Bit(s)	R/W	Default	Description
8-0	W/R	128	fifo size

Table 9-415 DI_IF1_RANGE_MAP_Y 0x17FC

Bit(s)	R/W	Default	Description
31-23	W/R	0	din offset
22-15	W/R	0	range map coef
13-10	W/R	0	range map din offset mult
9-1	W/R	0	dout offset
0	W/R	0	range map enable

Table 9-416 DI_IF1_RANGE_MAP_CB 0x17FD

Bit(s)	R/W	Default	Description
31-23	W/R	0	din offset
22-15	W/R	0	range map coef
13-10	W/R	0	range map din offset mult
9-1	W/R	0	dout offset
0	W/R	0	range map enable

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Table 9-417 DI_IF1_RANGE_MAP_CR 0x17FE

Bit(s)	R/W	Default	Description
31-23	W/R	0	din offset
22-15	W/R	0	range map coef
13-10	W/R	0	range map din offset mult
9-1	W/R	0	dout offset
0	W/R	0	range map enable

Table 9-418 DI_IF1_URGENT_CTRL 0x17A3

Bit(s)	R/W	Default	Description
13-16	W/R	0	urgent_ctrl_luma: bit 15: auto urgent_en bit 14: urgent_wr bit 7-4: up_threshold bit 3-0: down_threshold
15-0	W/R	0	urgent_ctrl_chroma: bit 15: auto urgent_en bit 14: urgent_wr bit 7-4: up_threshold bit 3-0: down_threshold

Table 9-419 DI_IF1_FMT_CTRL 0x17F3

Bit(s)	R/W	Default	Description
31	R/W	0	gate_clk_en. 0=No clock gating, free-running; 1=Enable clock gating for power saving.
30	R/W	0	soft_rst. If true, reset formatters.
29	R/W	0	unused
28	R/W	0	if true, horizontal formatter use repeating to generete pixel, otherwise use bilinear interpolation
27-24	R/W	0	horizontal formatter initial phase
23	R/W	0	horizontal formatter repeat pixel 0 enable
22-21	R/W	0	horizontal Y/C ratio, 00: 1:1, 01: 2:1, 10: 4:1
20	R/W	0	horizontal formatter enable
19	R/W	0	if true, always use phase0 while vertical formater, meaning always repeat data, no interpolation
18	R/W	0	if true, disable vertical formatter chroma repeat last line
17	R/W	0	veritcal formatter dont need repeat line on phase0, 1: enable, 0: disable
16	R/W	0	veritcal formatter repeat line 0 enable
15-12	R/W	0	vertical formatter skip line num at the beginning
11-8	R/W	0	vertical formatter initial phase

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Bit(s)	R/W	Default	Description
7-1	R/W	0	vertical formatter phase step (3.4)
0	R/W	0	vertical formatter enable

Table 9-420 DI_IF1_FMT_W 0x17F4

Bit(s)	R/W	Default	Description
27-16	R/W	0	horizontal formatter width
12-0	R/W	0	vertical formatter width

Table 9-421 DI_INP_GEN_REG 0x17CE

Bit(s)	R/W	Default	Description
31	W/R	0	enable free clk
30	W/R	0	sw reset : pulse bit
29	W/R	0	reset on go field
28	W/R	0	urgent chroma
27	W/R	0	urgent luma
26	W/R	0	chroma end at last line : 0 = read last line or push dummy after last line; 1 = stop read after last line
25	W/R	0	luma end at last line : 0 = read last line or push dummy after last line; 1 = stop read after last line
24-19	W/R	4	hold line[5:0], see GEN_REG2[6]
18	W/R	1	last line mode: 0 = read last line; 1 = push fixed value
16	W/R	0	demux mode: 0 = 4:2:2 demux; 1 = RGB demuxing from a single FIFO
15-14	W/R	0	bytes per pixel : 0= 1byte per pixel; 1 = 2 bytes per pixel; 2 = 3bytes per pixel
13-12	W/R	0	burst size cr: 0 = 24x64; 1 = 32x64; 2 = 48x64; 3 = 64x64
11-10	W/R	0	burst size cb: 0 = 24x64; 1 = 32x64; 2 = 48x64; 3 = 64x64
9-8	W/R	0	burst size y: 0 = 24x64; 1 = 32x64; 2 = 48x64; 3 = 64x64
7	W/R	0	start frame manual : pulse bit
6	W/R	0	chroma repeat last1
5	W/R	0	Reserved
4	W/R	0	little endian: 0=Pixels are big-endian in memory; 1=Pixel are little-endian in memory
3	W/R	0	chroma hz avg: 0= output pixel by pixel per line; 1= output half line ,average between every 2 pixels
2	W/R	0	luma_hz_avg: 0= output pixel by pixel per line; 1= output half line ,average between every 2 pixels
1	W/R	0	separate_en: Set to 1 to use 3 separate FIFO’s
0	W/R	0	enable

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Table 9-422 DI_INP_GEN_REG2 0x1791

Bit(s)	R/W	Default	Description
29	W/R	0	chroma line read sel
28	W/R	0	luma line read sel
25-14	W/R	0	shift pat cr
17-16	W/R	0	shift pat cb
9-8	W/R	0	shift pat y
6	W/R	0	hold_lines[6]
3	W/R	0	y_rev: X read direction: 0=default ,normal read; 1=reverse read
2	W/R	0	x_rev: Y read direction: 0=default ,normal read; 1=reverse read
1-0	W/R	0	color map: 0=default color map as defined by “bytes per pixel”; 1=NV12(CbCr); 2=NV21(CrCb)

Table 9-423 DI_INP_CANVAS0 0x17CF

Bit(s)	R/W	Default	Description
31	W/R	0	canvas addr syncen
23-16	W/R	0	canvas addr2
15-8	W/R	0	canvas addr1
7-0	W/R	0	canvas addr0

Table 9-424 DI_INP_LUMA_X0 0x17D0

Bit(s)	R/W	Default	Description
30-16	W/R	0	luma_x_end
14-0	W/R	0	luma_x_start

Table 9-425 DI_INP_LUMA_Y0 0x17D1

Bit(s)	R/W	Default	Description
28-16	W/R	0	luma_y_end
12-0	W/R	0	luma_y_start

Table 9-426 DI_INP_CHROMA_X0 0x17D2

Bit(s)	R/W	Default	Description
30-16	W/R	0	chroma_x_end
14-0	W/R	0	chroma_x_start

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Table 9-427 DI_INP_CHROMA_Y0 0x17D3

Bit(s)	R/W	Default	Description
28-16	W/R	0	chroma_y_end
12-0	W/R	0	chroma_y_start

Table 9-428 DI_INP_RPT_LOOP 0x17D4

Bit(s)	R/W	Default	Description
15-8	W/R	0	chroma repeat loop
7-0	W/R	0	luma repeat loop

Table 9-429 DI_INP_LUMA0_RPT_PAT 0x17D5

Bit(s)	R/W	Default	Description
31-0	W/R	0	luma repeat pattern

Table 9-430 DI_INP_CHROMA0_RPT_PAT 0x17D6

Bit(s)	R/W	Default	Description
7-0	W/R	0	chroma repeat loop

Table 9-431 DI_INP_DUMMY_PIXEL 0x17D7

Bit(s)	R/W	Default	Description
31-0	W/R	0x8080-00	dummy pixel

Table 9-432 DI_INP_LUMA_FIFO_SIZE 0x17D8

Bit(s)	R/W	Default	Description
8-0	W/R	128	fifo size

Table 9-433 DI_INP_RANGE_MAP_Y 0x17BA

Bit(s)	R/W	Default	Description
31-23	W/R	0	din offset
22-15	W/R	0	range map coef
13-10	W/R	0	range map din offset mult
9-1	W/R	0	dout offset
0	W/R	0	range map enable

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Table 9-434 DI_INP_RANGE_MAP_CB 0x17BB

Bit(s)	R/W	Default	Description
31-23	W/R	0	din offset
22-15	W/R	0	range map coef
13-10	W/R	0	range map din offset mult
9-1	W/R	0	dout offset
0	W/R	0	range map enable

Table 9-435 DI_INP_RANGE_MAP_CR 0x17BC

Bit(s)	R/W	Default	Description
31-23	W/R	0	din offset
22-15	W/R	0	range map coef
13-10	W/R	0	range map din offset mult
9-1	W/R	0	dout offset
0	W/R	0	range map enable

Table 9-436 DI_INP_URGENT_CTRL 0x17A4

Bit(s)	R/W	Default	Description
13-16	W/R	0	urgent_ctrl_luma: bit 15: auto urgent_en bit 14: urgent_wr bit 7-4: up_threshold bit 3-0: down_threshold
15-0	W/R	0	urgent_ctrl_chroma: bit 15: auto urgent_en bit 14: urgent_wr bit 7-4: up_threshold bit 3-0: down_threshold

Table 9-437 DI_INP_FMT_CTRL 0x17D9

Bit(s)	R/W	Default	Description
31	R/W	0	gate_clk_en. 0=No clock gating, free-running; 1=Enable clock gating for power saving.
30	R/W	0	soft_rst. If true, reset formatters.
29	R/W	0	unused
28	R/W	0	if true, horizontal formatter use repeating to generete pixel, otherwise use bilinear interpolation
27-24	R/W	0	horizontal formatter initial phase
23	R/W	0	horizontal formatter repeat pixel 0 enable
22-21	R/W	0	horizontal Y/C ratio, 00: 1:1, 01: 2:1, 10: 4:1
20	R/W	0	horizontal formatter enable

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Bit(s)	R/W	Default	Description
19	R/W	0	if true, always use phase0 while vertical formater, meaning always repeat data, no interpolation
18	R/W	0	if true, disable vertical formatter chroma repeat last line
17	R/W	0	veritcal formatter dont need repeat line on phase0, 1: enable, 0: disable
16	R/W	0	veritcal formatter repeat line 0 enable
15-12	R/W	0	vertical formatter skip line num at the beginning
11-8	R/W	0	vertical formatter initial phase
7-1	R/W	0	vertical formatter phase step (3.4)
0	R/W	0	vertical formatter enable

Table 9-438 DI_INP_FMT_W 0x17DA

Bit(s)	R/W	Default	Description
27-16	R/W	0	horizontal formatter width
12-0	R/W	0	vertical formatter width

Table 9-439 DI_MEM_GEN_REG 0x17DB

Bit(s)	R/W	Default	Description
31	W/R	0	enable free clk
30	W/R	0	sw reset : pulse bit
29	W/R	0	reset on go field
28	W/R	0	urgent chroma
27	W/R	0	urgent luma
26	W/R	0	chroma end at last line : 0 = read last line or push dummy after last line; 1 = stop read after last line
25	W/R	0	luma end at last line : 0 = read last line or push dummy after last line; 1 = stop read after last line
24-19	W/R	4	hold line[5:0], see GEN_REG2[6]
18	W/R	1	last line mode: 0 = read last line; 1 = push fixed value
16	W/R	0	demux mode: 0 = 4:2:2 demux; 1 = RGB demuxing from a single FIFO
15-14	W/R	0	bytes per pixel : 0= 1byte per pixel; 1 = 2 bytes per pixel; 2 = 3bytes per pixel
13-12	W/R	0	burst size cr: 0 = 24x64; 1 = 32x64; 2 = 48x64; 3 = 64x64
11-10	W/R	0	burst size cb: 0 = 24x64; 1 = 32x64; 2 = 48x64; 3 = 64x64
9-8	W/R	0	burst size y: 0 = 24x64; 1 = 32x64; 2 = 48x64; 3 = 64x64
7	W/R	0	start frame manual : pulse bit
6	W/R	0	chroma repeat last1
5	W/R	0	Reserved

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Bit(s)	R/W	Default	Description
4	W/R	0	little endian: 0=Pixels are big-endian in memory; 1=Pixel are little-endian in memory
3	W/R	0	chroma hz avg: 0= output pixel by pixel per line; 1= output half line ,average between every 2 pixels
2	W/R	0	luma_hz_avg: 0= output pixel by pixel per line; 1= output half line ,average between every 2 pixels
1	W/R	0	separate_en: Set to 1 to use 3 separate FIFO's
0	W/R	0	enable

Table 9-440 DI_MEM_GEN_REG2 0x1792

Bit(s)	R/W	Default	Description
25-14	W/R	0	shift pat cr
17-16	W/R	0	shift pat cb
9-8	W/R	0	shift pat y
6	W/R	0	hold_lines[6]
3	W/R	0	y_rev: X read direction: 0=default ,normal read; 1=reverse read
2	W/R	0	x_rev: Y read direction: 0=default ,normal read; 1=reverse read
1-0	W/R	0	color map: 0=default color map as defined by "bytes per pixel"; 1=NV12(CbCr); 2=NV21(CrCb)

Table 9-441 DI_MEM_CANVAS0 0x17DC

Bit(s)	R/W	Default	Description
31	W/R	0	canvas addr syncen
23-16	W/R	0	canvas addr2
15-8	W/R	0	canvas addr1
7-0	W/R	0	canvas addr0

Table 9-442 DI_MEM_LUMA_X0 0x17DD

Bit(s)	R/W	Default	Description
30-16	W/R	0	luma_x_end
14-0	W/R	0	luma_x_start

Table 9-443 DI_MEM_LUMA_Y0 0x17DE

Bit(s)	R/W	Default	Description
28-16	W/R	0	luma_y_end
12-0	W/R	0	luma_y_start

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Table 9-444 DI_MEM_CHROMA_X0 0x17DF

Bit(s)	R/W	Default	Description
30-16	W/R	0	chroma_x_end
14-0	W/R	0	chroma_x_start

Table 9-445 DI_MEM_CHROMA_Y0 0x17E0

Bit(s)	R/W	Default	Description
28-16	W/R	0	chroma_y_end
12-0	W/R	0	chroma_y_start

Table 9-446 DI_MEM_RPT_LOOP 0x17E1

Bit(s)	R/W	Default	Description
15-8	W/R	0	chroma repeat loop
7-0	W/R	0	luma repeat loop

Table 9-447 DI_MEM_LUMA0_RPT_PAT 0x17E2

Bit(s)	R/W	Default	Description
31-0	W/R	0	luma repeat pattern

Table 9-448 DI_MEM_CHROMA0_RPT_PAT 0x17E3

Bit(s)	R/W	Default	Description
7-0	W/R	0	chroma repeat loop

Table 9-449 DI_MEM_DUMMY_PIXEL 0x17E4

Bit(s)	R/W	Default	Description
31-0	W/R	0x8080-00	dummy pixel

Table 9-450 DI_MEM_LUMA_FIFO_SIZE 0x17E5

Bit(s)	R/W	Default	Description
8-0	W/R	128	fifo size

Table 9-451 DI_MEM_RANGE_MAP_Y 0x17BD

Bit(s)	R/W	Default	Description
31-23	W/R	0	din offset
22-15	W/R	0	range map coef

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Bit(s)	R/W	Default	Description
13-10	W/R	0	range map din offset mult
9-1	W/R	0	dout offset
0	W/R	0	range map enable

Table 9-452 DI_MEM_RANGE_MAP_CB 0x17BE

Bit(s)	R/W	Default	Description
31-23	W/R	0	din offset
22-15	W/R	0	range map coef
13-10	W/R	0	range map din offset mult
9-1	W/R	0	dout offset
0	W/R	0	range map enable

Table 9-453 DI_MEM_RANGE_MAP_CR 0x17BF

Bit(s)	R/W	Default	Description
31-23	W/R	0	din offset
22-15	W/R	0	range map coef
13-10	W/R	0	range map din offset mult
9-1	W/R	0	dout offset
0	W/R	0	range map enable

Table 9-454 DI_MEM_URGENT_CTRL 0x17A5

Bit(s)	R/W	Default	Description
13-16	W/R	0	urgent_ctrl_luma: bit 15: auto urgent_en bit 14: urgent_wr bit 7-4: up_threshold bit 3-0: down_threshold
15-0	W/R	0	urgent_ctrl_chroma: bit 15: auto urgent_en bit 14: urgent_wr bit 7-4: up_threshold bit 3-0: down_threshold

Table 9-455 DI_MEM_FMT_CTRL 0x17E6

Bit(s)	R/W	Default	Description
31	R/W	0	gate_clk_en. 0=No clock gating, free-running; 1=Enable clock gating for power saving.
30	R/W	0	soft_rst. If true, reset formatters.
29	R/W	0	unused

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Bit(s)	R/W	Default	Description
28	R/W	0	if true, horizontal formatter use repeating to generete pixel, otherwise use bilinear interpolation
27-24	R/W	0	horizontal formatter initial phase
23	R/W	0	horizontal formatter repeat pixel 0 enable
22-21	R/W	0	horizontal Y/C ratio, 00: 1:1, 01: 2:1, 10: 4:1
20	R/W	0	horizontal formatter enable
19	R/W	0	if true, always use phase0 while vertical formater, meaning always repeat data, no interpolation
18	R/W	0	if true, disable vertical formatter chroma repeat last line
17	R/W	0	veritcal formatter dont need repeat line on phase0, 1: enable, 0: disable
16	R/W	0	veritcal formatter repeat line 0 enable
15-12	R/W	0	vertical formatter skip line num at the beginning
11-8	R/W	0	vertical formatter initial phase
7-1	R/W	0	vertical formatter phase step (3.4)
0	R/W	0	vertical formatter enable

Table 9-456 DI_MEM_FMT_W 0x17E7

Bit(s)	R/W	Default	Description
27-16	R/W	0	horizontal formatter width
12-0	R/W	0	vertical formatter width

Table 9-457 DI_CHAN2_GEN_REG 0x17F5

Bit(s)	R/W	Default	Description
31	W/R	0	enable free clk
30	W/R	0	sw reset : pulse bit
29	W/R	0	reset on go field
28	W/R	0	urgent chroma
27	W/R	0	urgent luma
26	W/R	0	chroma end at last line : 0 = read last line or push dummy after last line; 1 = stop read after last line
25	W/R	0	luma end at last line : 0 = read last line or push dummy after last line; 1 = stop read after last line
24-19	W/R	4	hold line[5:0], see GEN_REG2[6]
18	W/R	1	last line mode: 0 = read last line; 1 = push fixed value
16	W/R	0	demux mode: 0 = 4:2:2 demux; 1 = RGB demuxing from a single FIFO
15-14	W/R	0	bytes per pixel : 0= 1byte per pixel; 1 = 2 bytes per pixel; 2 = 3bytes per pixel
13-12	W/R	0	burst size cr: 0 = 24x64; 1 = 32x64; 2 = 48x64; 3 = 64x64
11-10	W/R	0	burst size cb: 0 = 24x64; 1 = 32x64; 2 = 48x64; 3 = 64x64

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Bit(s)	R/W	Default	Description
9-8	W/R	0	burst size y: 0 = 24x64; 1 = 32x64; 2 = 48x64; 3 = 64x64
7	W/R	0	start frame manual : pulse bit
6	W/R	0	chroma repeat last1
5	W/R	0	Reserved
4	W/R	0	little endian: 0=Pixels are big-endian in memory; 1=Pixel are little-endian in memory
3	W/R	0	chroma hz avg: 0= output pixel by pixel per line; 1= output half line ,average between every 2 pixels
2	W/R	0	luma_hz_avg: 0= output pixel by pixel per line; 1= output half line ,average between every 2 pixels
1	W/R	0	separate_en: Set to 1 to use 3 separate FIFO’s
0	W/R	0	enable

Table 9-458 DI_CHAN2_GEN_REG2 0x17B7

Bit(s)	R/W	Default	Description
25-14	W/R	0	shift pat cr
17-16	W/R	0	shift pat cb
9-8	W/R	0	shift pat y
6	W/R	0	hold_lines[6]
3	W/R	0	y_rev: X read direction: 0=default ,normal read; 1=reverse read
2	W/R	0	x_rev: Y read direction: 0=default ,normal read; 1=reverse read
1-0	W/R	0	color map: 0=default color map as defined by “bytes per pixel”; 1=NV12(CbCr); 2=NV21(CrCb)

Table 9-459 DI_CHAN2_CANVAS0 0x17F6

Bit(s)	R/W	Default	Description
31	W/R	0	canvas addr syncen
23-16	W/R	0	canvas addr2
15-8	W/R	0	canvas addr1
7-0	W/R	0	canvas addr0

Table 9-460 DI_CHAN2_LUMA_X0 0x17F7

Bit(s)	R/W	Default	Description
30-16	W/R	0	luma_x_end
14-0	W/R	0	luma_x_start

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Table 9-461 DI_CHAN2_LUMA_Y0 0x17F8

Bit(s)	R/W	Default	Description
28-16	W/R	0	luma_y_end
12-0	W/R	0	luma_y_start

Table 9-462 DI_CHAN2_CHROMA_X0 0x17F9

Bit(s)	R/W	Default	Description
30-16	W/R	0	chroma_x_end
14-0	W/R	0	chroma_x_start

Table 9-463 DI_CHAN2_CHROMA_Y0 0x17FA

Bit(s)	R/W	Default	Description
28-16	W/R	0	chroma_y_end
12-0	W/R	0	chroma_y_start

Table 9-464 DI_CHAN2_RPT_LOOP 0x17FB

Bit(s)	R/W	Default	Description
15-8	W/R	0	chroma repeat loop
7-0	W/R	0	luma repeat loop

Table 9-465 DI_CHAN2_LUMA0_RPT_PAT 0x17B0

Bit(s)	R/W	Default	Description
31-0	W/R	0	luma repeat pattern

Table 9-466 DI_CHAN2_CHROMA0_RPT_PAT 0x17B1

Bit(s)	R/W	Default	Description
7-0	W/R	0	chroma repeat loop

Table 9-467 DI_CHAN2_DUMMY_PIXEL 0x17B2

Bit(s)	R/W	Default	Description
31-0	W/R	0x8080-00	dummy pixel

Table 9-468 DI_CHAN2_LUMA_FIFO_SIZE 0x17B3

Bit(s)	R/W	Default	Description
8-0	W/R	128	fifo size

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Table 9-469 DI_CHAN2_RANGE_MAP_Y 0x17B4

Bit(s)	R/W	Default	Description
31-23	W/R	0	din offset
22-15	W/R	0	range map coef
13-10	W/R	0	range map din offset mult
9-1	W/R	0	dout offset
0	W/R	0	range map enable

Table 9-470 DI_CHAN2_RANGE_MAP_CB 0x17B5

Bit(s)	R/W	Default	Description
31-23	W/R	0	din offset
22-15	W/R	0	range map coef
13-10	W/R	0	range map din offset mult
9-1	W/R	0	dout offset
0	W/R	0	range map enable

Table 9-471 DI_CHAN2_RANGE_MAP_CR 0x17B6

Bit(s)	R/W	Default	Description
31-23	W/R	0	din offset
22-15	W/R	0	range map coef
13-10	W/R	0	range map din offset mult
9-1	W/R	0	dout offset
0	W/R	0	range map enable

Table 9-472 DI_CHAN2_URGENT_CTRL 0x17A6

Bit(s)	R/W	Default	Description
13-16	W/R	0	urgent_ctrl_luma: bit 15: auto urgent_en bit 14: urgent_wr bit 7-4: up_threshold bit 3-0: down_threshold
15-0	W/R	0	urgent_ctrl_chroma: bit 15: auto urgent_en bit 14: urgent_wr bit 7-4: up_threshold bit 3-0: down_threshold

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Table 9-473 DI_CHAN2_FMT_CTRL 0x17B8

Bit(s)	R/W	Default	Description
31	R/W	0	gate_clk_en. 0=No clock gating, free-running; 1=Enable clock gating for power saving.
30	R/W	0	soft_rst. If true, reset formatters.
29	R/W	0	unused
28	R/W	0	if true, horizontal formatter use repeating to generete pixel, otherwise use bilinear interpolation
27-24	R/W	0	horizontal formatter initial phase
23	R/W	0	horizontal formatter repeat pixel 0 enable
22-21	R/W	0	horizontal Y/C ratio, 00: 1:1, 01: 2:1, 10: 4:1
20	R/W	0	horizontal formatter enable
19	R/W	0	if true, always use phase0 while vertical formater, meaning always repeat data, no interpolation
18	R/W	0	if true, disable vertical formatter chroma repeat last line
17	R/W	0	veritcal formatter dont need repeat line on phase0, 1: enable, 0: disable
16	R/W	0	veritcal formatter repeat line 0 enable
15-12	R/W	0	vertical formatter skip line num at the beginning
11-8	R/W	0	vertical formatter initial phase
7-1	R/W	0	vertical formatter phase step (3.4)
0	R/W	0	vertical formatter enable

Table 9-474 DI_CHAN2_FMT_W 0x17B9

Bit(s)	R/W	Default	Description
27-16	R/W	0	horizontal formatter width
12-0	R/W	0	vertical formatter width

Table 9-475 DI_NRWR_CTRL 0x17C2

Bit(s)	R/W	Default	Description
31	R/W	0	Pending_ddr_wrrsp_nrwr
30	R/W	0	Nrwr_reg_swap
29-26	R/W	0	Nrwr_burst_lim
25	R/W	0	Nrwr_canvas_syncen
24	R/W	0	Nrwr_no_clk_gate
23-22	R/W	0	Nrwr_rgb_mode , 0: 4:2:2 to one canvas; 1: 4:4:4 to one canvas; 2: Y to luma canvas, CbCr to chroma canvas, for NV12/21; 3: Reserved.
21-20	R/W	0	Nrwr_hconv_mode
19-18	R/W	0	Nrwr_vconv_mode
17	R/W	0	Nrwr_swap_cbcr

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Bit(s)	R/W	Default	Description
16	R/W	0	Nrwr_urgent
15-8	R/W	0	Nrwr_canvas_index_chroma
7-0	R/W	0	Nrwr_canvas_index_luma

Table 9-476 DI_NRWR_X 0x17C0

Bit(s)	R/W	Default	Description
31	R/W	0	Nrwr_little_endian
30	R/W	0	Nrwr_rev_x
29-16	R/W	0	Nrwr_start_x
15-14	R/W	0	nrwr_words_lim[3:2]
13-0			Nrwr_end_x

Table 9-477 DI_NRWR_Y 0x17C1

Bit(s)	R/W	Default	Description
31-30	R/W	1	Nrwr_words_lim[1:0]
29	R/W	0	Nrwr_rev_y
28-16	R/W	0	Nrwr_start_y
15	R/W	0	Nrwr_ext_en
14	R/W	1	Nrwr bit10 mode
12-0	R/W	0	Nrwr_end_y

Table 9-478 DI_DIWR_CTRL 0x17C8

Bit(s)	R/W	Default	Description
31	R/W	0	Pending_ddr_wrrsp_Diwr
30	R/W	0	Diwr_reg_swap
29-26	R/W	0	Diwr_burst_lim
25	R/W	0	Diwr_canvas_syncen
24	R/W	0	Diwr_no_clk_gate
23-22	R/W	0	Diwr_rgb_mode , 0: 4:2:2 to one canvas; 1: 4:4:4 to one canvas; 2: Y to luma canvas, CbCr to chroma canvas, for NV12/21; 3: Reserved.
21-20	R/W	0	Diwr_hconv_mode
19-18	R/W	0	Diwr_vconv_mode
17	R/W	0	Diwr_swap_cbcr
16	R/W	0	Diwr_urgent

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Bit(s)	R/W	Default	Description
15-8	R/W	0	Diwr_canvas_index_chroma
7-0	R/W	0	Diwr_canvas_index_luma

Table 9-479 DI_DIWR_X 0x17C6

Bit(s)	R/W	Default	Description
31	R/W	0	Diwr_little_endian
30	R/W	0	Diwr_rev_x
29-16	R/W	0	Diwr_start_x
15-14	R/W	0	Diwr_words_lim[3:2]
13-0			Diwr_end_x

Table 9-480 DI_DIWR_Y 0x17C7

Bit(s)	R/W	Default	Description
31-30	R/W	1	Diwr_words_lim[1:0]
29	R/W	0	Diwr_rev_y
28-16	R/W	0	Diwr_start_y
15	R/W	0	Diwr_ext_en
14	R/W	1	Diwr bit10 mode
12-0	R/W	0	Diwr_end_y

Table 9-481 DI_CONTWR_X 0x17A0

Bit(s)	R/W	Default	Description
30	R/W	0	rev_x
29-16	R/W	0	start_x
13-0	R/W	0	end_x

Table 9-482 DI_CONTWR_Y 0x17A1

Bit(s)	R/W	Default	Description
29	R/W	0	rev_x
28-16	R/W	0	start_x
12-0	R/W	0	end_x

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Table 9-483 DI_CONTWR_CTRL 0x17A2

Bit(s)	R/W	Default	Description
31	R/W	0	write : clear wrrsp; read : Pending_ddr_wrrsp
11	R/W	0	canvas sync_enable
10	R/W	0	bits per pixel
8	R/W	0	urgent
7-0	R/W	0	canvas_index

Table 9-484 DI_MTNWR_X 0x17C3

Bit(s)	R/W	Default	Description
30	R/W	0	rev_x
29-16	R/W	0	start_x
13-0	R/W	0	end_x

Table 9-485 DI_MTNWR_Y 0x17C4

Bit(s)	R/W	Default	Description
29	R/W	0	rev_x
28-16	R/W	0	start_x
12-0	R/W	0	end_x

Table 9-486 DI_MTNWR_CTRL 0x17C5

Bit(s)	R/W	Default	Description
31	R/W	0	write : clear wrrsp; read : Pending_ddr_wrrsp
11	R/W	0	canvas sync_enable
10	R/W	0	bits per pixel
8	R/W	0	urgent
7-0	R/W	0	canvas_index

Table 9-487 DI_MTNRD_X 0x17CB

Bit(s)	R/W	Default	Description
29-16	R/W	0	start_x
13-0	R/W	0	end_x

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Table 9-488 DI_MTNRD_Y 0x17CC

Bit(s)	R/W	Default	Description
28-16	R/W	0	start_x
12-0	R/W	0	end_x

Table 9-489 DI_MTNRD_CTRL 0x17CD

Bit(s)	R/W	Default	Description
23	R/W	0	canvas sync_enable
22	R/W	0	bits per pixel
18	R/W	0	x flip
17	R/W	0	y flip
16	R/W	0	urgent
15-8	R/W	0	canvas_index

Table 9-490 DI_CONTRD_X 0x17A3

Bit(s)	R/W	Default	Description
29-16	R/W	0	start_x
13-0	R/W	0	end_x

Table 9-491 DI_CONTRD_Y 0x17A4

Bit(s)	R/W	Default	Description
28-16	R/W	0	start_x
12-0	R/W	0	end_x

Table 9-492 DI_CONTRD2_X 0x17A5

Bit(s)	R/W	Default	Description
29-16	R/W	0	start_x
13-0	R/W	0	end_x

Table 9-493 DI_CONTRD2_Y 0x17A6

Bit(s)	R/W	Default	Description
28-16	R/W	0	start_x
12-0	R/W	0	end_x

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Table 9-494 DI_CONTRD_CTRL 0x17A7

Bit(s)	R/W	Default	Description
24	R/W	0	canvas sync_enable
23	R/W	0	contp bits per pixel
22	R/W	0	contp2 bits per pixel
18	R/W	0	contp x flip
17	R/W	0	contp y flip
18	R/W	0	contp2 x flip
17	R/W	0	contp2 y flip
16	R/W	0	urgent
15-8	R/W	0	contp2 canvas_index
7-0	R/W	0	contp canvas_index

Table 9-495 MCDI_MCVECWR_X 0x2f92

Bit(s)	R/W	Default	Description
29	R/W	0	rev_x
28-16	R/W	0	start_x
12-0	R/W	0	end_x

Table 9-496 MCDI_MCVECWR_Y 0x2f93

Bit(s)	R/W	Default	Description
29	R/W	0	rev_y
28-16	R/W	0	start_y
12-0	R/W	0	end_y

Table 9-497 MCDI_MCVECWR_CTRL 0x2f94

Bit(s)	R/W	Default	Description
31-16	R/W	0	urgent_ctrl: bit 15: auto urgent_en bit 14: urgent_wr bit 7-4: up_threshold bit 3-0: down_threshold
14	R/W	0	canvas sync enable
13	R/W	0	canvas_wr
12	R/W	0	req_en
11	R/W	0	fix disable
10	R/W	0	clear wrrsp
9	R/W	0	no clk gate

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Bit(s)	R/W	Default	Description
8	R/W	0	urgent
7-0	R/W	0	canvas index

Table 9-498 MCDI_MCVECRD_X 0x2f95

Bit(s)	R/W	Default	Description
30	R/W	0	x flip
28-16	R/W	0	start_x
12-0	R/W	0	end_x

Table 9-499 MCDI_MCVECRD_Y 0x2f96

Bit(s)	R/W	Default	Description
30	R/W	0	y flip
28-16	R/W	0	start_y
12-0	R/W	0	end_y

Table 9-500 MCDI_MCVECRD_CTRL 0x2f97

Bit(s)	R/W	Default	Description
31-16	R/W	0	urgent_ctrl: bit 15: auto urgent_en bit 14: urgent_wr bit 7-4: up_threshold bit 3-0: down_threshold
10	R/W	0	canvas sync enable
9	R/W	0	req_en
8	R/W	0	urgent
7-0	R/W	0	canvas index

Table 9-501 MCDI_MCINFOWR_X 0x2f98

Bit(s)	R/W	Default	Description
29	R/W	0	rev_x
28-16	R/W	0	start_x
12-0	R/W	0	end_x

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Table 9-502 MCDI_MCINFOWR_Y 0x2f99

Bit(s)	R/W	Default	Description
29	R/W	0	rev_y
28-16	R/W	0	start_y
12-0	R/W	0	end_y

Table 9-503 MCDI_MCINFOWR_CTRL 0x2f9a

Bit(s)	R/W	Default	Description
31-16	R/W	0	urgent_ctrl: bit 15: auto urgent_en bit 14: urgent_wr bit 7-4: up_threshold bit 3-0: down_threshold
14	R/W	0	canvas sync enable
13	R/W	0	canvas_wr
12	R/W	0	req_en
11	R/W	0	fix disable
10	R/W	0	clear wrrsp
9	R/W	0	no clk gate
8	R/W	0	urgent
7-0	R/W	0	canvas index

Table 9-504 MCDI_MCINFORD_X 0x2f9b

Bit(s)	R/W	Default	Description
30	R/W	0	x flip
28-16	R/W	0	start_x
12-0	R/W	0	end_x

Table 9-505 MCDI_MCINFORD_Y 0x2f9c

Bit(s)	R/W	Default	Description
30	R/W	0	y flip
28-16	R/W	0	start_y
12-0	R/W	0	end_y

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Table 9-506 MCDI_MCINFORD_CTRL 0x2f9d

Bit(s)	R/W	Default	Description
31-16	R/W	0	urgent_ctrl: bit 15: auto urgent_en bit 14: urgent_wr bit 7-4: up_threshold bit 3-0: down_threshold
10	R/W	0	canvas sync enable
9	R/W	0	req_en
8	R/W	0	urgent
7-0	R/W	0	canvas index

Table 9-507 MCDI_MCVECWR_CANVAS_SIZE 0x2f65

Bit(s)	R/W	Default	Description
28-16	R/W	0	hsizem1
12-0	R.W	0	vsizem1

Table 9-508 MCDI_MCVECRD_CANVAS_SIZE 0x2f66

Bit(s)	R/W	Default	Description
28-16	R/W	0	hsizem1
12-0	R.W	0	vsizem1

Table 9-509 MCDI_MCINFOWR_CANVAS_SIZE 0x2f67

Bit(s)	R/W	Default	Description
28-16	R/W	0	hsizem1
12-0	R.W	0	vsizem1

Table 9-510 MCDI_MCINFORD_CANVAS_SIZE 0x2f68

Bit(s)	R/W	Default	Description
28-16	R/W	0	hsizem1
12-0	R.W	0	vsizem1

Di mad registers

Table 9-511 DI_PRE_GL_CTRL 0x20ab

Bit(s)	R/W	Default	Description
31	W/R	0	pre count enable
30	W/R	0	pre count reset
29:16	W/R	0x20	total line number for pre count

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Bit(s)	R/W	Default	Description
15	W	0	pre mif manual start
13:0	W/R	0xc	the line number of pre frame reset

Table 9-512 DI_PRE_GL_THD 0x20ac

Bit(s)	R/W	Default	Description
21:16	W/R	10	DI PRE hold line number
15:0	W/R	1920	H total pixel number for pre count

Table 9-513 DI_POST_GL_CTRL 0x20ad

Bit(s)	R/W	Default	Description
31	W/R	0	post count enable
30	W/R	0	post count reset
29:16	W/R	0x20	total line number for post count
15	W	0	post mif manual start
13:0	W/R	0xc	the line number of post frame reset

Table 9-514 DI_POST_GL_THD 0x20ae

Bit(s)	R/W	Default	Description
21:16	W/R	10	DI POST hold line number
15:0	W/R	1920	H total pixel number for post count

Table 9-515 DI_PRE_CTRL 0x1700

Bit(s)	R/W	Default	Description
31	W/R		cbus_pre_frame_rst
30	W/R		cbus_pre_soft_rst
29	W/R		pre_field_num
28	W/R		di mem mif bypass : 1:bypass
27:26	W/R		mode_444c422
25	W/R		di_cont_read_en
24:23	W/R		mode_422c444
22	W/R		mtn_after_nr
21:16	W/R		pre_hold_fifo_lines
21	W/R		pre field num for nr
20	W/R		pre field num for pulldown
19	W/R		pre field num for mcdi

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Bit(s)	R/W	Default	Description
18	W/R		pd_mtn_swap
17	W/R		reg_me_autoen
16	W/R		reg_me_en
15	W/R		nr_wr_by
14	W/R		use_vdin_go_line
13	W/R		di_prevdin_en
12	W/R		di_pre_viu_link
11	W/R		di_chan3_enable
10	W/R		di_mcinfo_rd_mif en
9	W/R		di_buf2_en
8	W/R		di_chan2_en
7	W/R		prenr_hist_en
6	W/R		chan2_hist_en
5	W/R		hist_check_en
4	W/R		check_after_nr
3	W/R		check222p_en
2	W/R		check322p_en
1	W/R		mtn_en
0	W/R		nr_en

Table 9-516 DI_POST_CTRL 0x1701

Bit(s)	R/W	Default	Description
31	W/R		cbus_post_frame_rst
30	W/R		cbus_post_soft_rst
29	W/R		post_field_num
21:16	W/R		post_hold_fifo_lines
14	W/R		mc vector invert 1:invert 0:no invert
13	W/R		prepost_link
12	W/R		di_post_viu_link
11	W/R		di_post_repeat
10	W/R		di_post_drop_1st
9	W/R		mif0_to_vpp_en
8	W/R		di_vpp_out_en
7	W/R		di_wr_bk_en
6	W/R		di_mux_en

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Bit(s)	R/W	Default	Description
5	W/R		di_blend_en
4	W/R		di_mtnp_read_en
3	W/R		di_mcvec_read_en
2	W/R		di_ei_en
1	W/R		di_buf1_en
0	W/R		di_buf0_en

Table 9-517 DI_POST_SIZE 0x1702

Bit(s)	R/W	Default	Description
31:29	W/R	0	diwr_field_mode
28:16	W/R	0	vsize1post
12:0	W/R	0	hsize1post

Table 9-518 DI_PRE_SIZE 0x1703

Bit(s)	R/W	Default	Description
31:29	W/R	0	nrwr_field_mode
28:16	W/R	0	vsize1pre
12:0	W/R	0	hsize1pre

Table 9-519 DI_EI_CTRL0 0x1704

Bit(s)	R/W	Default	Description
23:16	W/R		ei0_filter[2:+] abs_diff_left>filter && ...right>filter && ...top>filter && ...bot>filter -> filter
15:8	W/R		ei0_threshold[2:+]
3	W/R		ei0_vertical
2	W/R		ei0_bpscf2
1	W/R		ei0_bpsfar1

Table 9-520 DI_EI_CTRL1 0x1705

Bit(s)	R/W	Default	Description
31:24	W/R		ei0_diff
23:16	W/R		ei0_angle45
15:8	W/R		ei0_peak
7:0	W/R		ei0_cross

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Table 9-521 DI_EI_CTRL2 0x1706

Bit(s)	R/W	Default	Description
31:24	W/R		ei0_close2
23:16	W/R		ei0_close1
15:8	W/R		ei0_far2
7:0	W/R		ei0_far1

Table 9-522 DI_NR_CTRL0 0x1707

Bit(s)	R/W	Default	Description
26	W/R		nr_cue_en
25	W/R		nr2_en

Table 9-523 DI_NR_CTRL1 0x1708

Bit(s)	R/W	Default	Description
31:30	W/R		mot_p1txtcore_mode
29:24	W/R		mot_p1txtcore_clmt
21:16	W/R		mot_p1txtcore_ylmt
15:8	W/R		mot_p1txtcore_crate
7:0	W/R		mot_p1txtcore_yrate

Table 9-524 DI_NR_CTRL2 0x1709

Bit(s)	R/W	Default	Description
29:24	W/R		mot_curtxtcore_clmt
21:16	W/R		mot_curtxtcore_ylmt
15:8	W/R		mot_curtxtcore_crate
7:0	W/R		mot_curtxtcore_yrate

Table 9-525 DI_CANVAS_URGENT0 0x170a

Bit(s)	R/W	Default	Description
26	R/W	0	di write mif bvalid_sel: 1. Bvalid_singnal from bus, 0: bytes_wr handshakes
25	R/W	0	di write mif burst last sel: 1. All kind of burst last signal include ext_data_last. 0. Used the normal burst last signal
24:16	W/R	0	Di write mif urgent ctrl
9	R/W	0	nr write mif bvalid_sel: 1. Bvalid_singnal from bus, 0: bytes_wr handshakes
8	R/W	0	nr write mif burst last sel: 1. All kind of burst last signal include ext_data_last. 0. Used the normal burst last signal
7:0	W/R	0	Nr write mif urgent ctrl

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Table 9-526 DI_MTN_CTRL 0x170b

Bit(s)	R/W	Default	Description
31	W/R	0	reg_mtn_1_en if 0x170b[0]=1 (DI_MTN_CTRL)
30	W/R	0	reg_mtn_init if 0x170b[0]=1 (DI_MTN_CTRL)
29	W/R	0	reg_di2nr_txt_en if 0x170b[0]=1 (DI_MTN_CTRL)
28	W/R	0	reg_di2nr_txt_mode if 0x170b[0]=1 (DI_MTN_CTRL)
27:24	W/R	0	reg_mtn_def if 0x170b[0]=1 (DI_MTN_CTRL)
23: 0	W/R	0	reserved

Table 9-527 DI_MTN_CTRL1 0x170c

Bit(s)	R/W	Default	Description
17	W/R		Invert NR field
16	W/R		Invert pulldown field
15	W/R		Invert mcdi field
14	W/R		Swap line0 and line2 of mtn input data
13	W/R		me enable
12	W/R		me autoenable
11:8	W/R		mtn_paramtnthd
7:0	W/R		mtn_paraftthd

Table 9-528 DI_BLEND_CTRL 0x170d

Bit(s)	R/W	Default	Description
31	W/R		blend_1_en
30	W/R		blend_mtn_lpf
28	W/R		post_mb_en
27	W/R		blend_mtn3p_max
26	W/R		blend_mtn3p_min
25	W/R		blend_mtn3p_ave
24	W/R		blend_mtn3p_maxtb
23	W/R		blend_mtn_flt_en
22	W/R		blend_data_flt_en
21:20	W/R		blend_top_mode 00: mtn, 01: weave mode, 10: bob mode, 11 : blend mode
19	W/R		blend_reg3_enable
18	W/R		blend_reg2_enable
17	W/R		blend_reg1_enable

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Bit(s)	R/W	Default	Description
16	W/R		blend_reg0_enable
15:14	W/R		blend_reg3_mode
13:12	W/R		blend_reg2_mode
11:10	W/R		blend_reg1_mode
9:8	W/R		blend_reg0_mode
7:0	W/R		kdeint

Table 9-529 DI_ARB_CTRL 0x170f

Bit(s)	R/W	Default	Description
31:26	W/R	0x20	Di_arb_thd1
25:20	W/R	0x20	Di_arb_thd0
19	W/R	0	Di_arb_tid_mode
18	W/R	0	Di_arb_arb_mode
17	W/R	0	Di_arb_acg_en
16	W/R	0	Di_arb_disable_clk
15:0	W/R	0	Di_arb_req_en

Table 9-530 DI_BLEND_REG0_X 0x1710

Bit(s)	R/W	Default	Description
28:16	W/R		blend_reg0_startx
12:0	W/R		blend_reg0_endx

Table 9-531 DI_BLEND_REG0_Y 0x1711

Bit(s)	R/W	Default	Description

Table 9-532 DI_BLEND_REG1_X 0x1712

Bit(s)	R/W	Default	Description

Table 9-533 DI_BLEND_REG1_Y 0x1713

Bit(s)	R/W	Default	Description

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Table 9-534 DI_BLEND_REG2_X 0x1714

Bit(s)	R/W	Default	Description

Table 9-535 DI_BLEND_REG2_Y 0x1715

Bit(s)	R/W	Default	Description

Table 9-536 DI_BLEND_REG3_X 0x1716

Bit(s)	R/W	Default	Description

Table 9-537 DI_BLEND_REG3_Y 0x1717

Bit(s)	R/W	Default	Description

Table 9-538 DI_EI_CTRL4 0x171a

Bit(s)	R/W	Default	Description
29	W/R	0	reg_ei_caldrt_amblike2_biasvertical
28:24	W/R	21	reg_ei_caldrt_addxla2list_drtmax
23	W/R	0	N/A
22:20	W/R	1	reg_ei_caldrt_addxla2list_signm0th
19	W/R	1	reg_ei_caldrt_addxla2list_mode
18:16	W/R	3	reg_ei_signm_sad_cor_rate
15:12	W/R	3	reg_ei_signm_sadi_cor_rate
11:6	W/R	2	reg_ei_signm_sadi_cor_ofst
5:0	W/R	4	reg_ei_signm_sad_ofst

Table 9-539 DI_EI_CTRL5 0x171b

Bit(s)	R/W	Default	Description
30:28	W/R	5	reg_ei_caldrt_cnflcctchk_frcverthrd
27	W/R	0	N/A
26:24	W/R	2	reg_ei_caldrt_cnflctchk_mg
23:22	W/R	1	reg_ei_caldrt_cnflctchk_ws
21	W/R	1	reg_ei_caldrt_cnflctchk_en
20	W/R	1	reg_ei_caldrt_verfrc_final_en

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Bit(s)	R/W	Default	Description
19	W/R	0	reg_ei_caldrt_verfrc_retimflt_en
18:16	W/R	3	reg_ei_caldrt_verftc_eithratemth
15	W/R	0	reg_ei_caldrt_verfrc_retiming_en
14:12	W/R	2	reg_ei_caldrt_verfrc_bothratemth
11:9	W/R	0	reg_ei_caldrt_ver_thrd
8:4	W/R	4	reg_ei_caldrt_addxla2list_drtmin
3:0	W/R	15	reg_ei_caldrt_addxla2list_drtlimit

Table 9-540 DI_EI_CTRL6 0x171c

Bit(s)	R/W	Default	Description
31:24	W/R	80	reg_ei_caldrt_abext_sad12thhig
23:16	W/R	35	reg_ei_caldrt_abext_sad00thlow
15:8	W/R	28	reg_ei_caldrt_abext_sad12thlow
6:4	W/R	1	reg_ei_caldrt_abext_ratemth
2:0	W/R	5	reg_ei_caldrt_abext_drtthrd

Table 9-541 DI_EI_CTRL7 0x171d

Bit(s)	R/W	Default	Description
29	W/R	1	reg_ei_caldrt_xlanopeak_codien
28:24	W/R	15	reg_ei_caldrt_xlanopeak_drtmax
23	W/R	1	reg_ei_caldrt_xlanopeak_en
22:20	W/R	3	reg_ei_caldrt_abext_monotrnd_alpha
19:18	W/R	1	reg_ei_caldrt_abext_mononum12_thrd
17:16	W/R	1	reg_ei_caldrt_abext_mononum00_thrd
15:12	W/R	6	reg_ei_caldrt_abext_sad00rate
11:8	W/R	6	reg_ei_caldrt_abext_sad12rate
7:0	W/R	80	reg_ei_caldrt_abext_sad00thhig

Table 9-542 DI_EI_CTRL8 0x171e

Bit(s)	R/W	Default	Description
30:28	W/R	2	reg_ei_assign_headtail_magin
26:24	W/R	3	reg_ei_retime_lastcurpncnfltchk_mode
22:21	W/R	0	reg_ei_retime_lastcurpncnfltchk_drtth
13:11	W/R	3	reg_ei_caldrt_amblike2_drtmg
10:8	W/R	1	reg_ei_caldrt_amblike2_valmg

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Bit(s)	R/W	Default	Description
7:4	W/R	10	reg_ei_caldrt_amblike2_alpha
3:0	W/R	4	reg_ei_caldrt_amblike2_drtth

Table 9-543 DI_EI_CTRL9 0x171f

Bit(s)	R/W	Default	Description
31:28	W/R	7	reg_ei_caldrt_hcnfcheck_frcvert_xla_th3
27	W/R	1	reg_ei_caldrt_hcnfcheck_frcvert_xla_en
26:24	W/R	4	reg_ei_caldrt_conf_drtth
23:20	W/R	11	reg_ei_caldrt_conf_absdrtth
19:18	W/R	2	reg_ei_caldrt_abcheck_mode1
17:16	W/R	1	reg_ei_caldrt_abcheck_mode0
15:12	W/R	11	reg_ei_caldrt_abcheck_drtth1
11:8	W/R	11	reg_ei_caldrt_abcheck_drtth0
6:4	W/R	3	reg_ei_caldrt_abpnchk1_th
1	W/R	1	reg_ei_caldrt_abpnchk1_en
0	W/R	1	reg_ei_caldrt_abpnchk0_en

Table 9-544 DI_EI_CTRL10 0x1793

Bit(s)	R/W	Default	Description
31:28	W/R	0	reg_ei_caldrt_hstrrgchk_drtth
27:24	W/R	8	reg_ei_caldrt_hstrrgchk_frcverthrd
23:20	W/R	4	reg_ei_caldrt_hstrrgchk_mg
19	W/R	0	reg_ei_caldrt_hstrrgchk_1sidnul
18	W/R	0	reg_ei_caldrt_hstrrgchk_excpcnf
17:16	W/R	2	reg_ei_caldrt_hstrrgchk_ws
15	W/R	1	reg_ei_caldrt_hstrrgchk_en
14:13	W/R	2	reg_ei_caldrt_hpncheck_mode
12	W/R	0	reg_ei_caldrt_hpncheck_mute
11:9	W/R	3	reg_ei_caldrt_hcnfcheck_mg2
8:6	W/R	2	reg_ei_caldrt_hcnfcheck_mg1
5:4	W/R	2	reg_ei_caldrt_hcnfcheck_mode
3:0	W/R	9	reg_ei_caldrt_hcnfcheck_frcvert_xla_th5

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Table 9-545 DI_EI_CTRL11 0x179e

Bit(s)	R/W	Default	Description
30:29	W/R	2	reg_ei_amb_detect_mode
28:24	W/R	8	reg_ei_amb_detect_winth
23:21	W/R	3	reg_ei_amb_decide_rppth
20:19	W/R	1	reg_ei_retime_lastmappncnfltchk_drtth
18:16	W/R	2	reg_ei_retime_lastmappncnfltchk_mode
15:14	W/R	2	reg_ei_retime_lastmapvertfrcchk_mode
13:12	W/R	3	reg_ei_retime_lastvertfrcchk_mode
11:8	W/R	0	reg_ei_retime_lastpnchk_drtth
6	W/R	1	reg_ei_retime_lastpnchk_en
5:4	W/R	3	reg_ei_retime_mode
3	W/R	1	reg_ei_retime_last_en
2	W/R		reg_ei_retime_ab_en
1	W/R	1	reg_ei_caldrt_hstrvertfrcchk_en
0	W/R	0	reg_ei_caldrt_hstrrgchk_mode

Table 9-546 DI_EI_CTRL12 0x179f

Bit(s)	R/W	Default	Description
31:28	W/R	13	reg_ei_drtdelay2_lmt
27:26	W/R	2	reg_ei_drtdelay2_notver_lrwin
25:24	W/R	3	reg_ei_drtdelay_mode
23	W/R	0	reg_ei_drtdelay2_mode
22:20	W/R	0	reg_ei_assign_xla_signm0th
19	W/R	1	reg_ei_assign_pkbiasvert_en
18	W/R	1	reg_ei_assign_xla_en
17:16	W/R	0	reg_ei_assign_xla_mode
15:12	W/R	2	reg_ei_assign_nlfilter_magin
11:8	W/R	5	reg_ei_localsearch_maxrange
7:4	W/R	0	reg_ei_xla_drtth
3:0	W/R	3	reg_ei_flatmsad_thrd

Table 9-547 DI_EI_CTRL13 0x17a8

Bit(s)	R/W	Default	Description
27:24	W/R	15	reg_ei_int_drt2x_chrdrt_limit
23:20	W/R	0	reg_ei_int_drt16x_core

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Bit(s)	R/W	Default	Description
19:16	W/R	2	reg_ei_int_drtdelay2_notver_cancv
15:8	W/R	20	reg_ei_int_drtdelay2_notver_sadth
7:0	W/R	20	reg_ei_int_drtdelay2_vlddrt_sadth

Table 9-548 DI_EI_DRT_CTRL 0x2028

Bit(s)	R/W	Default	Description
31	W/R	0	reg_rectg_en: Low angle enable.
30	W/R	0	reg_recbld_en: New and old drt blend enable.
29:28	W/R	2	reg_rectg_ws : window sideto calculate the reference direction: 0:1x1; 1:1x3; 2:1x5; 3:1x7
27			reserved
26:24	W/R	2	reg_abq_margin : top and bottom curve trend quantilization margin of noise for direction assignments.
23			reserved
22:20	W/R	3	reg_trend_mg : the Margin of the top/bot trend.
19:16	W/R	1	reg_int_d16xc1 : Coring to drtf.
15:14			reserved
13:8	W/R	40	reg_int_chlmt1: Limit to drtf(16x) for chroma angle
7			reserved
6:4	W/R	5	reg_nscheck_thrd:check whether the pixels id noise or not.
3			reserved
2:0	W/R	7	reg_horsl_ws: window side to check the existent number of low angle drt, if the number < the value, drt=raw drt.

Table 9-549 DI_EI_DRT_PIXTH 0x2029

Bit(s)	R/W	Default	Description
31:24	W/R	22	reg_min_pix: the threshold of min pix of photos, < threshold the pix do not participate in the monotonic trend calculation.
23:16	W/R	203	reg_max_pix:the threshold of max pix of photos, >threshold the pix do not participate in the monotonic trend calculation.
15:8	W/R	50	reg_dmaxmin_thrdma: the max pixel and min pixel difference is larger than the value the trend existent.
7:0	W/R	30	reg_dmaxmin_thrdmi: the max pixel and min pixel difference is smaller than the value the trend non-existent.

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Table 9-550 DI_EI_DRT_CORRPIXTH 0x202a

Bit(s)	R/W	Default	Description
31:24	W/R	40	reg_newcorrpix_maxthrd:the new low angle drt sad threshold.
23:16	W/R	60	reg_corrpix_diffthrd: the top and bottom pixel difference is larger than the value, the case may be ultra-low angle.
15:8	W/R	10	reg_corrpix_minthrd: the difference of top and bottom pixel is smaller than the value, the drt may be raw drt.
7:0	W/R	20	reg_corrpix_maxthrd: the difference of top and bottom pixel is larger than the value, the drt may be raw drt.

Table 9-551 DI_EI_DRT_RECTG_WAVE 0x202b

Bit(s)	R/W	Default	Description
31:29			reserved
28:24	W/R	0	reg_max_pixwave: the wave of the max pix threshold, prevent min pix close to reg_max_pix caused the number between max and min pix zeros.
23:21			reserved
20:16	W/R	15	reg_pix_wave: the wave of the max and min pix, the max pixel smaller than the value or the min pixel larger than the value, may be the ultra-low angle case.
15:14			reserved
13:8	W/R	40	reg_maxdrt_thrd: the threshold of the low angle max drt.
7:0	W/R	20	reg_wave_thrd:in bilateral cases tow pixel difference is smaller than the value, the trend between the tow pixel not change.

Table 9-552 DI_EI_DRT_PIX_DIFFTH 0x202c

Bit(s)	R/W	Default	Description
31:24	W/R	32	reg_newraw_thrd: the old drt and new drt transition threshold.
23:16	W/R	10	reg_tb_max_thrd: the threshold of top and bottom max or min pixel.
15:8	W/R	20	reg_diffpix_thrd: Max-Min<the value,the trend is non-existent.
7:6			reserved
5:0	W/R	5	reg_bilt_trendnumt: in bilateral cases the difference between the top and bottom pixel number of the monotonic trend smaller than the value is low angle.

Table 9-553 DI_EI_DRT_UNBITREND_TH 0x202d

Bit(s)	R/W	Default	Description
31:29			reserved
28:24	W/R	10	reg_trend_numb:in bilateral cases the pixel number of the monotonic trend larger than the value is low angle.
23:21			reserved
20:16	W/R	4	reg_bilt_trendnum:in bilateral cases the pixel number of the trend larger than the value is low angle.

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Bit(s)	R/W	Default	Description
15:13			reserved
12:8	W/R	7	reg_unil_trendnumt: in unilateral cases the difference between the top and bottom pixel number of the monotonic trend smaller than the value is low angle.
7:5			reserved
4:0	W/R	10	reg_trend_num: in unilateral cases the pixel number of the trend larger than the value is ultra-low angle.

Table 9-554 DI_EI_XWIN0 0x1798

Bit(s)	R/W	Default	Description
27:16	W/R		ei_xend0
11:0	W/R		ei_xstart0

Table 9-555 DI_EI_XWIN1 0x1799

Bit(s)	R/W	Default	Description

Table 9-556 DI_MC_REG0_X 0x1720

Bit(s)	R/W	Default	Description
27:16	W/R		mc_reg0_start_x
11:0	W/R		mc_reg0_end_x

Table 9-557 DI_MC_REG0_Y 0x1721

Bit(s)	R/W	Default	Description

Table 9-558 DI_MC_REG1_X 0x1722

Bit(s)	R/W	Default	Description

Table 9-559 DI_MC_REG1_Y 0x1723

Bit(s)	R/W	Default	Description

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Table 9-560 DI_MC_REG2_X 0x1724

Bit(s)	R/W	Default	Description

Table 9-561 DI_MC_REG2_Y 0x1725

Bit(s)	R/W	Default	Description

Table 9-562 DI_MC_REG3_X 0x1726

Bit(s)	R/W	Default	Description

Table 9-563 DI_MC_REG3_Y 0x1727

Bit(s)	R/W	Default	Description

Table 9-564 DI_MC_REG4_X 0x1728

Bit(s)	R/W	Default	Description

Table 9-565 DI_MC_REG4_Y 0x1729

Bit(s)	R/W	Default	Description

Table 9-566 DI_MC_32LVL0 0x172a

Bit(s)	R/W	Default	Description
31:24	W/R		mc_reg2_32lvl
23:16	W/R		mc_reg1_32lvl
15:8	W/R		mc_reg0_32lvl
7:0	W/R		field_32lvl

Table 9-567 DI_MC_32LVL1 0x172b

Bit(s)	R/W	Default	Description
15:8	W/R		mc_reg3_32lvl
7:0	W/R		mc_reg4_32lvl

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Table 9-568 DI_MC_22LVL0 0x172c

Bit(s)	R/W	Default	Description
31:16	W/R		mc_reg0_22lvl
15:0	W/R		field_22lvl

Table 9-569 DI_MC_22LVL1 0x172d

Bit(s)	R/W	Default	Description
31:16	W/R		mc_reg2_22lvl
15:0	W/R		mc_reg1_22lvl

Table 9-570 DI_MC_22LVL2 0x172e

Bit(s)	R/W	Default	Description
31:16	W/R		mc_reg4_22lvl
15:0	W/R		mc_reg3_22lvl

Table 9-571 DI_MC_CTRL 0x172f

Bit(s)	R/W	Default	Description
4	W/R		mc_reg4_en
3	W/R		mc_reg3_en
2	W/R		mc_reg2_en
1	W/R		mc_reg1_en
0	W/R		mc_reg0_en

Table 9-572 DI_INTR_CTRL 0x1730

Bit(s)	R/W	Default	Description
31	W/R	0	When Deint_irq_mode is 0: When predi_int or postdi_int is generated, the interrupt flag will be erected; Deint_irq_mode==1: When the interrupt source of any module inside DI is generated and no Mask operation is performed, the interrupt flag will be erected.
30:26	W/R	0	reserved
25	w/R	0	NrDownscale_int_mask
24	w/R	0	Det3d_int_mask
23	w/R	0	Mcinfowr_int_mask
22	w/R	0	Mcvecwr_int_mask
21	w/R	0	Medi_int_mask
20	w/R	0	Contwr_int_mask
19	w/R	0	Hist_int_mask

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Bit(s)	R/W	Default	Description
18	w/R	0	Diwr_int_mask
17	w/R	0	Mtn_wr_int_mask
16	w/R	0	Nrwr_int_mask
15:10	W/R	0	reserved
9	R		Nrdownscale_done
8	R		Det3d_done
7	R		Mcinfowr_done (not valid in GX)
6	R		Mcvecwr_done (not valid in GX)
5	R		Medi_done(not valid in GX)
4	R		Contwr_done
3	R		Hist_done
2	R		diwr_done
1	R		Mtnwr_done
0	R		Nrwr_done

Table 9-573 DI_INFO_ADDR 0x1731 Addr_0

Bit(s)	R/W	Default	Description
31:0	R		Field_32p , sum of difference between n-2 and n

Table 9-574 Addr_1

Bit(s)	R/W	Default	Description
31:24	R		Field_32max, maximum difference between n-2 and n
23:0	R		Field_32num, numbers of pixels difference > threshold

Table 9-575 Addr_2

Bit(s)	R/W	Default	Description
31:0	R		Field_22p, sum of difference between temporal and vertical difference

Table 9-576 Addr_3

Bit(s)	R/W	Default	Description
15:0	R		Field_22max , maximum difference between temporal and verticaldifference

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Table 9-577 Addr_4

Bit(s)	R/W	Default	Description
23:0	R		Field_22num, pixel sum which difference > threshold

Table 9-578 Addr_5

Bit(s)	R/W	Default	Description
31:0	R		Luma sum

Table 9-579 Addr_6

Bit(s)	R/W	Default	Description
31:0	R		Difference of 32, sum in area 0

Table 9-580 Addr_7

Bit(s)	R/W	Default	Description
31:0	R		Difference of 32, sum in area 1

Table 9-581 Addr_8

Bit(s)	R/W	Default	Description
31:0	R		Difference of 32, sum in area 2

Table 9-582 Addr_9

Bit(s)	R/W	Default	Description
31:0	R		Difference of 32, sum in area 3

Table 9-583 Addr_10

Bit(s)	R/W	Default	Description
31:0	R		Difference of 32, sum in area 4

Table 9-584 Addr_11

Bit(s)	R/W	Default	Description
31:0	R		Difference of 22, sum in area 0

Table 9-585 Addr_12

Bit(s)	R/W	Default	Description
31:0	R		Difference of 22, sum in area 1

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Table 9-586 Addr_13

Bit(s)	R/W	Default	Description
31:0	R		Difference of 22, sum in area 2

Table 9-587 Addr_14

Bit(s)	R/W	Default	Description
31:0	R		Difference of 22, sum in area 3

Table 9-588 Addr_15

Bit(s)	R/W	Default	Description
31:0	R		Difference of 22, sum in area 4

Table 9-589 Addr_16

Bit(s)	R/W	Default	Description
31:0	R		luma, sum in area 0

Table 9-590 Addr_17

Bit(s)	R/W	Default	Description
31:0	R		luma, sum in area 1

Table 9-591 Addr_18

Bit(s)	R/W	Default	Description
31:0	R		luma, sum in area 2

Table 9-592 Addr_19

Bit(s)	R/W	Default	Description
31:0	R		luma, sum in area 3

Table 9-593 Addr_20

Bit(s)	R/W	Default	Description
31:0	R		luma, sum in area 4

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Table 9-594 Addr_21

Bit(s)	R/W	Default	Description
31:24	R		Field_32max, maximum difference between n-2 and n in area0
23:0	R		Field_32num, numbers of pixels difference > threshold in area0

Table 9-595 Addr_22

Bit(s)	R/W	Default	Description
31:24	R		Field_32max, maximum difference between n-2 and n in area1
23:0	R		Field_32num, numbers of pixels difference > threshold in area1

Table 9-596 Addr_23

Bit(s)	R/W	Default	Description
31:24	R		Field_32max, maximum difference between n-2 and n in area2
23:0	R		Field_32num, numbers of pixels difference > threshold in area2

Table 9-597 Addr_24

Bit(s)	R/W	Default	Description
31:24	R		Field_32max, maximum difference between n-2 and n in area3
23:0	R		Field_32num, numbers of pixels difference > threshold in area3

Table 9-598 Addr_25

Bit(s)	R/W	Default	Description
31:24	R		Field_32max, maximum difference between n-2 and n in area4
23:0	R		Field_32num, numbers of pixels difference > threshold in area4

Table 9-599 Addr_26

Bit(s)	R/W	Default	Description
31:20	R		Field_22max/16, in area 0
19:0	R		Field_22 num/16, in area 0

Table 9-600 Addr_27

Bit(s)	R/W	Default	Description
31:20	R		Field_22max/16, in area 1
19:0	R		Field_22 num/16, in area 1

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Table 9-601 Addr_28

Bit(s)	R/W	Default	Description
31:20	R		Field_22max/16, in area 2
19:0	R		Field_22 num/16, in area 2

Table 9-602 Addr_29

Bit(s)	R/W	Default	Description
31:20	R		Field_22max/16, in area 3
19:0	R		Field_22 num/16, in area 3

Table 9-603 Addr_30

Bit(s)	R/W	Default	Description
31:20	R		Field_22max/16, in area 4
19:0	R		Field_22 num/16, in area 4

Table 9-604 DI_INFO_DATA 0x1732

Bit(s)	R/W	Default	Description

Table 9-605 DI_PRE_HOLD 0x1733

Bit(s)	R/W	Default	Description
31	R/W	0	cntl_pre_hold_enable
27:16	R/W	0	cntl_pre_hold_count
11:0	R/W	0	cntl_pre_pass_count

Table 9-606 DI_MTN_1_CTRL1 0x1740

Bit(s)	R/W	Default	Description
31	W/R		reg_mtn_1_en if 0x170b[0]=0 (DI_MTN_CTRL)
30	W/R		reg_mtn_init if 0x170b[0]=0 (DI_MTN_CTRL)
29	W/R		reg_di2nr_txt_en if 0x170b[0]=0 (DI_MTN_CTRL)
28	W/R		reg_di2nr_txt_mode if 0x170b[0]=0 (DI_MTN_CTRL)
27:24	W/R		reg_mtn_def if 0x170b[0]=0 (DI_MTN_CTRL)
23:16	W/R	32	reg_DI_cmb_adp_YCrate
15: 8	W/R	32	reg_DI_cmb_adp_2Crate
7: 0	W/R	21	reg_DI_cmb_adp_2Yrate

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Table 9-607 DI_MTN_1_CTRL2 0x1741

Bit(s)	R/W	Default	Description
31:24	W/R	26	reg_DI_m1b_core_Ykinter
23:16	W/R	26	reg_DI_m1b_core_Ckinter
15:8	W/R	58	reg_DI_m1b_core_Ykintra
7:0	W/R	98	reg_DI_m1b_core_Ckintra

Table 9-608 DI_MTN_1_CTRL3 0x1742

Bit(s)	R/W	Default	Description
31:24	W/R	21	reg_DI_m1b_thr_2Yrate
23:16	W/R	32	reg_DI_m1b_thr_2Crate
15: 8	W/R	10	reg_DI_m1b_core_mxcmbY
7: 0	W/R	10	reg_DI_m1b_core_mxcmbC

Table 9-609 DI_MTN_1_CTRL4 0x1743

Bit(s)	R/W	Default	Description
31:24	W/R	1	reg_DI_m1b_coreY
23:16	W/R	0	reg_DI_m1b_coreC
15: 8	W/R	8	reg_DI_m1b_thrd_min
7: 0	W/R	128	reg_DI_m1b_thrd_max

Table 9-610 DI_MTN_1_CTRL5 0x1744

Bit(s)	R/W	Default	Description
31:27	W/R	7	reg_DI_m1b_pp_extnd_num
27:24	W/R	4	reg_DI_m1b_pp_errod_num
21:20	W/R	0	Re_di2nr_txt_mode 0:average of top/bot 1:max; 2: |a+c-2b|;
15: 8	W/R	13	reg_DI_mot_core_Ykinter
7: 0	W/R	13	reg_DI_mot_core_Ckinter

Table 9-611 DI_MTN_1_CTRL6 0x17a9

Bit(s)	R/W	Default	Description
31:24	W/R	13	reg_DI_mot_core_Ykintra
23:16	W/R	90	reg_DI_mot_core_Ckintra
15: 8	W/R	21	reg_DI_mot_cor_2Yrate
7: 0	W/R	32	reg_DI_mot_cor_2Crate

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Table 9-612 DI_MTN_1_CTRL7 0x17aa

Bit(s)	R/W	Default	Description
31:24	W/R	10	reg_DI_mot_core_mxcmbY
23:16	W/R	10	reg_DI_mot_core_mxcmbC
15: 8	W/R	2	reg_DI_mot_coreY
7: 0	W/R	1	reg_DI_mot_coreC

Table 9-613 DI_MTN_1_CTRL8 0x17ab

Bit(s)	R/W	Default	Description
31:24	W/R	26	reg_DI_fmot_core_Ykinter
23:16	W/R	26	reg_DI_fmot_core_Ckinter
15: 8	W/R	38	reg_DI_fmot_core_Ykintra
7: 0	W/R	98	reg_DI_fmot_core_Ckintra

Table 9-614 DI_MTN_1_CTRL9 0x17ac

Bit(s)	R/W	Default	Description
31:24	W/R	13	reg_DI_fmot_cor_2Yrate
23:16	W/R	32	reg_DI_fmot_cor_2Crate
15: 8	W/R	3	reg_DI_fmot_coreY
7: 0	W/R	2	reg_DI_fmot_coreC

Table 9-615 DI_MTN_1_CTRL10 0x17ad

Bit(s)	R/W	Default	Description
27:24	W/R	2	reg_DI_m1b_suremot_num_fld0
19:16	W/R	2	reg_DI_m1b_surestl_num_fld0
11: 8	W/R	6	reg_DI_m1b_suremot_num_fld1
3: 0	W/R	6	reg_DI_m1b_surestl_num_fld1

Table 9-616 DI_MTN_1_CTRL11 0x17ae

Bit(s)	R/W	Default	Description
27:24	W/R	5	reg_DI_m1b_suremot_evn_th
20:16	W/R	8	reg_DI_m1b_suremot_odd_th
11: 8	W/R	3	reg_DI_m1b_surestl_evn_th
6	W/R	0	reg_DI_m1b_suremot_fast_en
5	W/R	0	reg_DI_m1b_surestl_fast_en
4: 0	W/R	4	reg_DI_m1b_surestl_odd_th

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Table 9-617 DI_MTN_1_CTRL12 0x17af

Bit(s)	R/W	Default	Description
31:24	W/R	64	reg_DI_mot_norm_gain
17:16	W/R	2	reg_DI_mot_alpha_lpf
15: 8	W/R	10	reg_DI_m1b_surestl_thrd
4: 0	W/R	4	reg_DI_mot_surestl_gain

Table 9-618 DI_CRC_CHK0 0x17cb

Bit(s)	R/W	Default	Description
0	W	0	di pre crc check start (pulse)

Table 9-619 DI_CRC_CHK1 0x17cc

Bit(s)	R/W	Default	Description
0	W	0	di post crc check start (pulse)

Table 9-620 DI_RO_CRC_NRWR 0x17c3

Bit(s)	R/W	Default	Description
31-0	W	0	nrwr crc output (lock by pre frame rst)

Table 9-621 DI_RO_CRC_MTNWR 0x17c4

Bit(s)	R/W	Default	Description
31-0	W	0	mtnwr crc output (lock by pre frame rst)

Table 9-622 DI_RO_CRC_DEINT 0x17c5

Bit(s)	R/W	Default	Description
31-0	W	0	di post crc output (lock by pre frame rst)

9.2.3.10 NR2 Registers

Table 9-623 DET3D_MOTN_CFG 0x1734

Bit(s)	R/W	Default	Description
16	R/W	0	reg_det3d_intr_en : Det3d interrupt enable
9:8	R/W	0	reg_Det3D_Motion_Mode : U2 Different mode for Motion Calculation of Luma and Chroma: 0 : MotY, 1: (2*MotY + (MotU + MotV))/4; 2: Max(MotY, MotU, MotV); 3:Max(MotY, (MotU+MotV)/2)

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Bit(s)	R/W	Default	Description
7:4	R/W	0	reg_Det3D_Motion_Core_Rate : U4 K Rate to Edge (HV) details for coring of Motion Calculations, normalized to 32
3:0	R/W	0	reg_Det3D_Motion_Core_Thrd : U4 2X: static coring value for Motion Detection.

Table 9-624 DET3D_CB_CFG 0x1735

Bit(s)	R/W	Default	Description
7:4	R/W	0	reg_Det3D_ChessBd_HV_ofst : U4, Noise immune offset for Horizotnal or vertical combing detection.
3:0	R/W	0	reg_Det3D_ChessBd_NHV_ofst : U4, Noise immune offset for NON-Horizotnal or vertical combing detection.

Table 9-625 DET3D_SPLT_CFG 0x1736

Bit(s)	R/W	Default	Description
7:4	R/W	0x0	reg_Det3D_SplitValid_ratio : U4, Ratio between max_value and the avg_value of the edge mapping for split line valid detection. The smaller of this value, the easier of the split line detected.
3:0	R/W	0x0	reg_Det3D_AvgIdx_ratio : U4, Ratio to the avg_value of the edge mapping for split line position estimation. The smaller of this value, the more samples will be added to the estimation.

Table 9-626 DET3D_HV_MUTE 0x1737

Bit(s)	R/W	Default	Description
23:20	R/W	0x0	reg_Det3D_Edge_Ver_Mute : U4 X2: Horizontal pixels to be mute from H/V Edge calculation Top and Bottom border part.
19:16	R/W	0x0	reg_Det3D_Edge_Hor_Mute : U4 X2: Horizontal pixels to be mute from H/V Edge calculation Left and right border part.
15:12	R/W	0x0	reg_Det3D_ChessBd_Ver_Mute : U4 X2: Horizontal pixels to be mute from ChessBoard statistics calculation in middle part
11:8	R/W	0x0	reg_Det3D_ChessBd_Hor_Mute : U4 X2: Horizontal pixels to be mute from ChessBoard statistics calculation in middle part
7:4	R/W	0x0	reg_Det3D_STA8X8_Ver_Mute : U4 1X: Vertical pixels to be mute from 8x8 statistics calculation in each block.
3:0	R/W	0x0	reg_Det3D_STA8X8_Hor_Mute : U4 1X: Horizontal pixels to be mute from 8x8 statistics calculation in each block.

Table 9-627 DET3D_MAT_STA_P1M1 0x1738

Bit(s)	R/W	Default	Description
31:24	R/W	0x0	reg_Det3D_STA8X8_P1_K0_R8 : U8 SAD to SAI ratio to decide P1, normalized to 256 (0.8)
23:16	R/W	0x0	reg_Det3D_STA8X8_P1_K1_R7 : U8 SAD to ENG ratio to decide P1, normalized to 128 (0.5)

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Bit(s)	R/W	Default	Description
15:8	R/W	0x0	reg_Det3D_STA8X8_M1_K0_R6 : U8 SAD to SAI ratio to decide M1, normalized to 64 (1.1)
7:0	R/W	0x0	reg_Det3D_STA8X8_M1_K1_R6 : U8 SAD to ENG ratio to decide M1, normalized to 64 (0.8)

Table 9-628 DET3D_MAT_STA_P1TH 0x1739

Bit(s)	R/W	Default	Description
23:16	R/W	0x0	reg_Det3D_STAYUV_P1_TH_L4 : U8 SAD to ENG Thrd offset to decide P1, X16 (100)
15:8	R/W	0x0	reg_Det3D_STAEDG_P1_TH_L4 : U8 SAD to ENG Thrd offset to decide P1, X16 (80)
7:0	R/W	0x0	reg_Det3D_STAMOT_P1_TH_L4 : U8 SAD to ENG Thrd offset to decide P1, X16 (48)

Table 9-629 DET3D_MAT_STA_M1TH 0x173a

Bit(s)	R/W	Default	Description
23:16	R/W	0x0	reg_Det3D_STAYUV_M1_TH_L4 : U8 SAD to ENG Thrd offset to decide M1, X16 (100)
15:8	R/W	0x0	reg_Det3D_STAEDG_M1_TH_L4 : U8 SAD to ENG Thrd offset to decide M1, X16 (80)
7:0	R/W	0x0	reg_Det3D_STAMOT_M1_TH_L4 : U8 SAD to ENG Thrd offset to decide M1, X16 (64)

Table 9-630 DET3D_MAT_STA_RSFT 0x173b

Bit(s)	R/W	Default	Description
5:4	R/W	0x0	reg_Det3D_STAYUV_RSHFT : U2 YUV statistics SAD and SAI calculation result right shift bits to accommodate the 12bits clipping: 0 : mainly for images <=720x480: 1: mainly for images <=1366x768: 2: mainly for images <=1920X1080: 2; 3: other higher resolutions
3:2	R/W	0x0	reg_Det3D_STAEDG_RSHFT : U2 Horizontal and Vertical Edge Statistics SAD and SAI calculation result right shift bits to accommodate the 12bits clipping: 0 : mainly for images <=720x480: 1: mainly for images <=1366x768: 2: mainly for images <=1920X1080: 2; 3: other higher resolutions
1:0	R/W	0x0	reg_Det3D_STAMOT_RSHFT : U2 Motion SAD and SAI calculation result right shift bits to accommodate the 12bits clipping: 0 : mainly for images <=720x480: 1: mainly for images <=1366x768: 2: mainly for images <=1920X1080: 2; 3: other higher resolutions

Table 9-631 DET3D_MAT_SYMTC_TH 0x173c

Bit(s)	R/W	Default	Description
31:24	R/W	0x0	reg_Det3D_STALUM_symtc_Th : U8 threshold to decide if the Luma statistics is TB or LR symmetric.
23:16	R/W	0x0	reg_Det3D_STACHR_symtc_Th : U8 threshold to decide if the Chroma (UV) statistics is TB or LR symmetric.

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Bit(s)	R/W	Default	Description
15:8	R/W	0x0	reg_Det3D_STAEDG_symtc_Th : U8 threshold to decide if the Horizontal and Vertical Edge statistics is TB or LR symmetric.
7:0	R/W	0x0	reg_Det3D_STAMOT_symtc_Th : U8 threshold to decide if the Motion statistics is TB or LR symmetric.

Table 9-632 DET3D_RO_DET_CB_HOR 0x173d

Bit(s)	R/W	Default	Description
31:16	R.O	0x0	RO_Det3D_ChessBd_NHor_value : U16 X64: number of Pixels of Horizontally Surely NOT matching Chessboard pattern.
15:0	R.O	0x0	RO_Det3D_ChessBd_Hor_value : U16 X64: number of Pixels of Horizontally Surely matching Chessboard pattern.

Table 9-633 DET3D_RO_DET_CB_VER 0x173e

Bit(s)	R/W	Default	Description
31:16	R.O	0x0	RO_Det3D_ChessBd_NVer_value : U16 X64: number of Pixels of Vertically Surely NOT matching Chessboard pattern.
15:0	R.O	0x0	RO_Det3D_ChessBd_Ver_value : U16 X64: number of Pixels of Vertically Surely matching Chessboard pattern.

Table 9-634 DET3D_RO_SPLT_HT 0x173f

Bit(s)	R/W	Default	Description
24	R.O	0x0	RO_Det3D_Split_HT_valid : U1 horizontal LR split border detected valid signal for top half picture
20:16	R.O	0x0	RO_Det3D_Split_HT_pxnum : U5 number of pixels included for the LR split position estimation for top half picture
9:0	R.O	0x0	RO_Det3D_Split_HT_idxX4 : S10 X4: horizontal pixel shifts of LR split position to the (ColMax/2) for top half picture

NR2 REG DEFINE BEGIN////

Table 9-635 NR2_MET_NM_CTRL 0x1745

Bit(s)	R/W	Default	Description
28	R/W	0x0	reg_NM_reset : Reset to the status of the Loop filter.
27:24	R/W	0x0	reg_NM_calc_length : Length mode of the Noise measurement sample number for statistics. 0 : 256 samples; 1: 512 samples; 2: 1024 samples; ¡X: 2^(8+x) samples
23:20	R/W	0x0	reg_NM_inc_step : Loop filter input gain increase step.
19:16	R/W	0x0	reg_NM_dec_step : Loop filter input gain decrease step.
15:8	R/W	0x0	reg_NM_YHPmot_thrd : Luma channel HP portion motion for condition of pixels included in Luma Noise measurement.
7:0	R/W	0x0	reg_NM_CHPmot_thrd : Chroma channel HP portion motion for condition of pixels included in Chroma Noise measurement.

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Table 9-636 NR2_MET_NM_YCTRL 0x1746

Bit(s)	R/W	Default	Description
31:28	R/W	0x0	reg_NM_YPLL_target : Target rate of NM_Ynoise_thrd to mean of the Luma Noise
27:24	R/W	0x0	reg_NM_YLPmot_thrd : Luma channel LP portion motion for condition of pixels included in Luma Noise measurement.
23:16	R/W	0x0	reg_NM_YHPmot_thrd_min : Minimum threshold for Luma channel HP portion motion to decide whether the pixel will be included in Luma noise measurement.
15:8	R/W	0x0	reg_NM_YHPmot_thrd_max : Maximum threshold for Luma channel HP portion motion to decide whether the pixel will be included in Luma noise measurement.
7:0	R/W	0x0	reg_NM_Ylock_rate : Rate to decide whether the Luma noise measurement is lock or not.

Table 9-637 NR2_MET_NM_CCTRL 0x1747

Bit(s)	R/W	Default	Description
31:28	R/W	0x0	reg_NM_CPLL_target : Target rate of NM_Cnoise_thrd to mean of the Chroma Noise
27:24	R/W	0x0	reg_NM_CLPmot_thrd : Chroma channel LP portion motion for condition of pixels included in Chroma Noise measurement.
23:16	R/W	0x0	reg_NM_CHPmot_thrd_min : Minimum threshold for Chroma channel HP portion motion to decide whether the pixel will be included in Chroma noise measurement.
15:8	R/W	0x0	reg_NM_CHPmot_thrd_max : Maximum threshold for Chroma channel HP portion motion to decide whether the pixel will be included in Chroma noise measurement.
7:0	R/W	0x0	reg_NM_Clock_rate : Rate to decide whether the Chroma noise measurement is lock or not;

Table 9-638 NR2_MET_NM_TNR 0x1748

Bit(s)	R/W	Default	Description
25	R.O	0x0	ro_NM_TNR_Ylock : Read-only register to tell ifLuma channel noise measurement is locked or not.
24	R.O	0x0	ro_NM_TNR_Clock : Read-only register to tell if Chroma channel noise measurement is locked or not.
23:12	R.O	0x0	ro_NM_TNR_Ylevel : Read-only register to give Luma channel noise level. It was 16x of pixel difference in 8 bits of YHPmot.
11:0	R.O	0x0	ro_NM_TNR_Clevel : Read-only register to give Chroma channel noise level. It was 16x of pixel difference in 8 bits of CHPmot.

Table 9-639 NR2_MET_NMFRM_TNR_YLEV 0x1749

Bit(s)	R/W	Default	Description
28:0	R.O	0x0	ro_NMFrm_TNR_Ylevel : Frame based Read-only register to give Luma channel noise level within one frame/field.

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Table 9-640 NR2_MET_NMFRM_TNR_YCNT 0x174a

Bit(s)	R/W	Default	Description
23:0	R.O	0x0	ro_NMFrm_TNR_Ycount : Number ofLuma channel pixels included in Frame/ Field based noise level measurement.

Table 9-641 NR2_MET_NMFRM_TNR_CLEV 0x174b

Bit(s)	R/W	Default	Description
28:0	R.O	0x0	ro_NMFrm_TNR_Clevel : Frame based Read-only register to give Chroma channel noise level within one frame/field.

Table 9-642 NR2_MET_NMFRM_TNR_CCNT 0x174c

Bit(s)	R/W	Default	Description
23:0	R.O	0x0	ro_NMFrm_TNR_Ccount : Number of Chroma channel pixels included in Frame/ Field based noise level measurement.

Table 9-643 NR2_3DEN_MODE 0x174d

Bit(s)	R/W	Default	Description
6:4	R/W	0x0	Blend_3dnr_en_r :
2:0	R/W	0x0	Blend_3dnr_en_l :

Table 9-644 NR2_IIR_CTRL 0x174e

Bit(s)	R/W	Default	Description
15:14	R/W	0x0	reg_LP_IIR_8bit_mode : LP IIR membitwidth mode:0: 10bits will be store in memory;1: 9bits will be store in memory; 2 : 8bits will be store in memory;3: 7bits will be store in memory;
13:12	R/W	0x0	reg_LP_IIR_mute_mode : Mode for the LP IIR mute,
11:8	R/W	0x0	reg_LP_IIR_mute_thrd : Threshold of LP IIR mute to avoid ghost:
7:6	R/W	0x0	reg_HP_IIR_8bit_mode : IIR membitwidth mode:0: 10bits will be store in memory;1: 9bits will be store in memory; 2 : 8bits will be store in memory;3: 7bits will be store in memory;
5:4	R/W	0x0	reg_HP_IIR_mute_mode : Mode for theLP IIR mute
3:0	R/W	0x0	reg_HP_IIR_mute_thrd : Threshold of HP IIR mute to avoid ghost

Table 9-645 NR2_SNR_SAD_CFG 0x1751

Bit(s)	R/W	Default	Description
12	R/W	0x1	reg_MATNR_SNR_SAD_CenRPL : U1, Enable signal for Current pixel position SAD to be replaced by SAD_min.0: do not replace Current pixel position SAD by SAD_min;1: do replacements
11:8	R/W	0x3	reg_MATNR_SNR_SAD_coring : Coring value of the intra-frame SAD. sum = (sum - reg_MATNR_SNR_SAD_coring);sum = (sum<0) ? 0: (sum>255)? 255: sum;

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Bit(s)	R/W	Default	Description
6:5	R/W	0x1	reg_MATNR_SNR_SAD_WinMod : Unsigned, Intra-frame SAD matching window mode:0: 1x1; 1: [1 1 1] 2: [1 2 1]; 3: [1 2 2 2 1];
4:0	R/W	0x1	Sad_coef_num : Sad coeffient

Table 9-646 NR2_MATNR_SNR_OS 0x1752

Bit(s)	R/W	Default	Description
7:4	R/W	0x8	reg_MATNR_SNR_COS : SNR Filter overshoot control margin for UV channel (X2 to u10 scale)
3:0	R/W	0xd	reg_MATNR_SNR_YOS : SNR Filter overshoot control margin for luma channel (X2 to u10 scale)

Table 9-647 NR2_MATNR_SNR_NRM_CFG 0x1753

Bit(s)	R/W	Default	Description
23:16	R/W	0x40	reg_MATNR_SNR_NRM_ofst : Edge based SNR boosting normalization offset to SAD_max ;
15:8	R/W	0xff	reg_MATNR_SNR_NRM_max : Edge based SNR boosting normalization Max value
7:0	R/W	0x0	reg_MATNR_SNR_NRM_min : Edge based SNR boosting normalization Min value

Table 9-648 NR2_MATNR_SNR_NRM_GAIN 0x1754

Bit(s)	R/W	Default	Description
15:8	R/W	0x0	reg_MATNR_SNR_NRM_Cgain : Edge based SNR boosting normalization Gain for Chrm channel (norm 32 as 1)
7:0	R/W	0x20	reg_MATNR_SNR_NRM_Ygain : Edge based SNR boosting normalization Gain for Luma channel (norm 32 as 1)

Table 9-649 NR2_MATNR_SNR_LPF_CFG 0x1755

Bit(s)	R/W	Default	Description
23:16	R/W	0xc	reg_MATNR_SNRLPF_SADmaxTH : U8, Threshold to SADmax to use TNRLPF to replace SNRLPF. i.e.if (SAD_max <reg_MATNR_SNRLPF_SADmaxTH) SNRLPF_yuv[k] = TNRLPF_yuv[k];
13:11	R/W	0x2	reg_MATNR_SNRLPF_Cmode : LPF based SNR filtering mode on CHRM channel: 0 : gradient LPF [1 1]/2, 1: gradient LPF [2 1 1]/4; 2: gradient LPF [3 3 2]/8; 3: gradient LPF [5 4 4 3]/16; 4 : TNRLPF; 5 : CurLPF3x3_yuv[]; 6: CurLPF3o3_yuv [] 7: CurLPF3x5_yuv[]
10: 8	R/W	0x2	reg_MATNR_SNRLPF_Ymode : LPF based SNR filtering mode on LUMA channel: 0 : gradient LPF //Bit [1 1]/2, 1: gradient LPF [2 1 1]/4; 2: gradient LPF [3 3 2]/8;3: gradient LPF [5 4 4 3]/16; 4 : TNRLPF; 5 : CurLPF3x3_yuv[]; 6: CurLPF3o3_yuv[] 7: CurLPF3x5_yuv[]
7:4	R/W	0x6	reg_MATNR_SNRLPF_SADmin3TH : Offset threshold to SAD_min to Discard SAD_min3 corresponding pixel in LPF SNR filtering. (X8 to u8 scale)
3:0	R/W	0x4	reg_MATNR_SNRLPF_SADmin2TH : Offset threshold to SAD_min to Discard SAD_min2 corresponding pixel in LPF SNR filtering. (X8 to u8 scale)

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Table 9-650 NR2_MATNR_SNR_USF_GAIN 0x1756

Bit(s)	R/W	Default	Description
15:8	R/W	0x0	reg_MATNR_SNR_USF_Cgain : Un-sharp (HP) compensate back Chrm portion gain, (norm 64 as 1)
7:0	R/W	0x0	reg_MATNR_SNR_USF_Ygain : Un-sharp (HP) compensate back Luma portion gain, (norm 64 as 1)

Table 9-651 NR2_MATNR_SNR_EDGE2B 0x1757

Bit(s)	R/W	Default	Description
15:8	R/W	0x80	reg_MATNR_SNR_Edge2Beta_ofst : U8, Offset for Beta based on Edge.
7:0	R/W	0x10	reg_MATNR_SNR_Edge2Beta_gain : U8. Gain to SAD_min for Beta based on Edge. (norm 16 as 1)

Table 9-652 NR2_MATNR_BETA_EGAIN 0x1758

Bit(s)	R/W	Default	Description
15:8	R/W	0x20	reg_MATNR_CBeta_Egain : U8, Gain to Edge based Beta for Chrm channel. (normalized to 32 as 1)
7:0	R/W	0x20	reg_MATNR_YBeta_Egain : U8, Gain to Edge based Beta for Luma channel. (normalized to 32 as 1)

Table 9-653 NR2_MATNR_BETA_BRT 0x1759

Bit(s)	R/W	Default	Description
31:28	R/W	0x0	reg_MATNR_beta_BRT_limt_hi : U4, Beta adjustment based on Brightness high side Limit. (X16 to u8 scale)
27:24	R/W	0x0	reg_MATNR_beta_BRT_slop_hi : U4, Beta adjustment based on Brightness high side slope. Normalized to 16 as 1
23:16	R/W	0xa0	reg_MATNR_beta_BRT_thrd_hi : U8, Beta adjustment based on Brightness high threshold.(u8 scale)
15:12	R/W	0x6	reg_MATNR_beta_BRT_limt_lo : U4, Beta adjustment based on Brightness low side Limit. (X16 to u8 scale)
11:8	R/W	0x6	reg_MATNR_beta_BRT_slop_lo : U4, Beta adjustment based on Brightness low side slope. Normalized to 16 as 1
7:0	R/W	0x64	reg_MATNR_beta_BRT_thrd_lo : U8, Beta adjustment based on Brightness low threshold.(u8 scale)

Table 9-654 NR2_MATNR_XBETA_CFG 0x175a

Bit(s)	R/W	Default	Description
19:18	R/W	0x0	reg_MATNR_CBeta_use_mode : U2, Beta options (mux) from beta_motion and beta_edge for Chrm channel;
17:16	R/W	0x0	reg_MATNR_YBeta_use_mode : U2, Beta options (mux) from beta_motion and beta_edge for Luma channel;

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Bit(s)	R/W	Default	Description
15: 8	R/W	0x0	reg_MATNR_CBeta_Ofst : U8, Offset to Beta for Chrm channel.(after beta_edge and beta_motion mux)
7: 0	R/W	0x0	reg_MATNR_YBeta_Ofst : U8, Offset to Beta for Luma channel.(after beta_edge and beta_motion mux)

Table 9-655 NR2_MATNR_YBETA_SCL 0x175b

Bit(s)	R/W	Default	Description
31:24	R/W	0x3c	reg_MATNR_YBeta_scale_min : U8, Final step Beta scale low limit for Luma channel;
23:16	R/W	0xff	reg_MATNR_YBeta_scale_max : U8, Final step Beta scale high limit for Luma channe;
15: 8	R/W	0x20	reg_MATNR_YBeta_scale_gain : U8, Final step Beta scale Gain for Luma channel (normalized 32 to 1);
7 : 0	R/W	0x0	reg_MATNR_YBeta_scale_ofst : S8, Final step Beta scale offset for Luma channel ;

Table 9-656 NR2_MATNR_CBETA_SCL 0x175c

Bit(s)	R/W	Default	Description
31:24	R/W	0x0	reg_MATNR_CBeta_scale_min : Final step Beta scale low limit for Chrm channel.Similar to Y
23:16	R/W	0xff	reg_MATNR_CBeta_scale_max : U8, Final step Beta scale high limit for Chrm channel.Similar to Y
15: 8	R/W	0x20	reg_MATNR_CBeta_scale_gain : U8, Final step Beta scale Gain for Chrm channel Similar to Y
7: 0	R/W	0x0	reg_MATNR_CBeta_scale_ofst : S8, Final step Beta scale offset for Chrm channel Similar to Y

Table 9-657 NR2_SNR_MASK 0x175d

Bit(s)	R/W	Default	Description
20:0	R/W	0x0	SAD_MSK : Valid signal in the 3x7 SAD surface

Table 9-658 NR2_SAD2NORM_LUT0 0x175e

Bit(s)	R/W	Default	Description
31:24	R/W	0x72	reg_MATNR_SAD2Norm_LUT_3 : SAD convert normal LUT node 3
23:16	R/W	0x92	reg_MATNR_SAD2Norm_LUT_2 : SAD convert normal LUT node 2
15: 8	R/W	0xab	reg_MATNR_SAD2Norm_LUT_1 : SAD convert normal LUT node 1
7: 0	R/W	0xcd	reg_MATNR_SAD2Norm_LUT_0 : SAD convert normal LUT node 0

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Table 9-659 NR2_SAD2NORM_LUT1 0x175f

Bit(s)	R/W	Default	Description
31:24	R/W	0x1c	reg_MATNR_SAD2Norm_LUT_7 : SAD convert normal LUT node 7
23:16	R/W	0x23	reg_MATNR_SAD2Norm_LUT_6 : SAD convert normal LUT node 6
15: 8	R/W	0x31	reg_MATNR_SAD2Norm_LUT_5 : SAD convert normal LUT node 5
7: 0	R/W	0x4f	reg_MATNR_SAD2Norm_LUT_4 : SAD convert normal LUT node 4

Table 9-660 NR2_SAD2NORM_LUT2 0x1760

Bit(s)	R/W	Default	Description
31:24	R/W	0xf	reg_MATNR_SAD2Norm_LUT_11 : SAD convert normal LUT node 11
23:16	R/W	0x11	reg_MATNR_SAD2Norm_LUT_10 : SAD convert normal LUT node 10
15: 8	R/W	0x13	reg_MATNR_SAD2Norm_LUT_9 : SAD convert normal LUT node 9
7: 0	R/W	0x17	reg_MATNR_SAD2Norm_LUT_8 : SAD convert normal LUT node 8

Table 9-661 NR2_SAD2NORM_LUT3 0x1761

Bit(s)	R/W	Default	Description
31:24	R/W	0x8	reg_MATNR_SAD2Norm_LUT_15 : SAD convert normal LUT node 15
23:16	R/W	0x9	reg_MATNR_SAD2Norm_LUT_14 : SAD convert normal LUT node 14
15:8	R/W	0xa	reg_MATNR_SAD2Norm_LUT_13 : SAD convert normal LUT node 13
7:0	R/W	0xc	reg_MATNR_SAD2Norm_LUT_12 : SAD convert normal LUT node 12

Table 9-662 NR2_EDGE2BETA_LUT0 0x1762

Bit(s)	R/W	Default	Description
31:24	R/W	0x80	reg_MATNR_Edge2Beta_LUT_3 : Edge convert beta LUT node 3
23:16	R/W	0xa0	reg_MATNR_Edge2Beta_LUT_2 : Edge convert beta LUT node 2
15: 8	R/W	0xe0	reg_MATNR_Edge2Beta_LUT_1 : Edge convert beta LUT node 1
7: 0	R/W	0xff	reg_MATNR_Edge2Beta_LUT_0 : Edge convert beta LUT node 0

Table 9-663 NR2_EDGE2BETA_LUT1 0x1763

Bit(s)	R/W	Default	Description
31:24	R/W	0x4	reg_MATNR_Edge2Beta_LUT_7 : Edge convert beta LUT node 7
23:16	R/W	0x10	reg_MATNR_Edge2Beta_LUT_6 : Edge convert beta LUT node 6
15: 8	R/W	0x20	reg_MATNR_Edge2Beta_LUT_5 : Edge convert beta LUT node 5
7: 0	R/W	0x50	reg_MATNR_Edge2Beta_LUT_4 : Edge convert beta LUT node 4

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Table 9-664 NR2_EDGE2BETA_LUT2 0x1a64

Bit(s)	R/W	Default	Description
31:24	R/W	0x0	reg_MATNR_Edge2Beta_LUT_11 : Edge convert beta LUT node 11
23:16	R/W	0x0	reg_MATNR_Edge2Beta_LUT_10 : Edge convert beta LUT node 10
15: 8	R/W	0x0	reg_MATNR_Edge2Beta_LUT_9 : Edge convert beta LUT node 9
7: 0	R/W	0x2	reg_MATNR_Edge2Beta_LUT_8 : Edge convert beta LUT node 8

Table 9-665 NR2_EDGE2BETA_LUT3 0x1765

Bit(s)	R/W	Default	Description
31:24	R/W	0x0	reg_MATNR_Edge2Beta_LUT_15 : Edge convert beta LUT node 15
23:16	R/W	0x0	reg_MATNR_Edge2Beta_LUT_14 : Edge convert beta LUT node 14
15: 8	R/W	0x0	reg_MATNR_Edge2Beta_LUT_13 : Edge convert beta LUT node 13
7: 0	R/W	0x0	reg_MATNR_Edge2Beta_LUT_12 : Edge convert beta LUT node 12

Table 9-666 NR2_MOTION2BETA_LUT0 0x1766

Bit(s)	R/W	Default	Description
31:24	R/W	0x20	reg_MATNR_Mot2Beta_LUT_3 : Motion convert beta LUT node 3
23:16	R/W	0x10	reg_MATNR_Mot2Beta_LUT_2 : Motion convert beta LUT node 2
15: 8	R/W	0x4	reg_MATNR_Mot2Beta_LUT_1 : Motion convert beta LUT node 1
7: 0	R/W	0x0	reg_MATNR_Mot2Beta_LUT_0 : Motion convert beta LUT node 0

Table 9-667 NR2_MOTION2BETA_LUT1 0x1767

Bit(s)	R/W	Default	Description
31:24	R/W	0xc4	reg_MATNR_Mot2Beta_LUT_7 : Motion convert beta LUT node 7
23:16	R/W	0x80	reg_MATNR_Mot2Beta_LUT_6 : Motion convert beta LUT node 6
15: 8	R/W	0x40	reg_MATNR_Mot2Beta_LUT_5 : Motion convert beta LUT node 5
7: 0	R/W	0x30	reg_MATNR_Mot2Beta_LUT_4 : Motion convert beta LUT node 4

Table 9-668 NR2_MOTION2BETA_LUT2 0x1768

Bit(s)	R/W	Default	Description
31:24	R/W	0xff	reg_MATNR_Mot2Beta_LUT_11 : Motion convert beta LUT node 11
23:16	R/W	0xff	reg_MATNR_Mot2Beta_LUT_10 : Motion convert beta LUT node 10
15: 8	R/W	0xf0	reg_MATNR_Mot2Beta_LUT_9 : Motion convert beta LUT node 9
7: 0	R/W	0xe0	reg_MATNR_Mot2Beta_LUT_8 : Motion convert beta LUT node 8

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Table 9-669 NR2_MOTION2BETA_LUT3 0x1769

Bit(s)	R/W	Default	Description
31:24	R/W	0xff	reg_MATNR_Mot2Beta_LUT_15 : Motion convert beta LUT node 15
23:16	R/W	0xff	reg_MATNR_Mot2Beta_LUT_14 : Motion convert beta LUT node 14
15: 8	R/W	0xff	reg_MATNR_Mot2Beta_LUT_13 : Motion convert beta LUT node 13
7: 0	R/W	0xff	reg_MATNR_Mot2Beta_LUT_12 : Motion convert beta LUT node 12

Table 9-670 NR2_MATNR_MTN_CRTL 0x176a

Bit(s)	R/W	Default	Description
25:24	R/W	0x0	reg_MATNR_Vmtn_use_mode : Motion_yuvV channel motion selection mode:0: Vmot;1:Ymot/2 + (Umot+Vmot)/4; 2:Ymot/2 + max(Umot,Vmot)/2; 3: max(Ymot, Umot, Vmot)
21:20	R/W	0x0	reg_MATNR_Umtn_use_mode : Motion_yuvU channel motion selection mode:0: Umot;1:Ymot/2 + (Umot+Vmot)/4; 2:Ymot/2 + max(Umot,Vmot)/2; 3: max(Ymot, Umot, Vmot)
17:16	R/W	0x0	reg_MATNR_Ymtn_use_mode : Motion_yuvLuma channel motion selection mode:0: Ymot, 1: Ymot/2 + (Umot+Vmot)/4; 2: Ymot/2 + max(Umot,Vmot)/2; 3: max(Ymot,Umot, Vmot)
13:12	R/W	0x1	reg_MATNR_mtn_txt_mode : Texture detection mode for adaptive coring of HP motion
9: 8	R/W	0x1	reg_MATNR_mtn_cor_mode : Coring selection mode based on texture detection;
6: 4	R/W	0x8	reg_MATNR_mtn_hpf_mode : video mode of current and previous frame/field for MotHPF_yuv[k] calculation:
2: 0	R/W	0x6	reg_MATNR_mtn_lpf_mode : LPF video mode of current and previous frame/ field for MotLPF_yuv[k] calculation:

Table 9-671 NR2_MATNR_MTN_CRTL2 0x176b

Bit(s)	R/W	Default	Description
18:16	R/W	0x6	reg_MATNR_iir_BS_Ymode : IIR TNR filter Band split filter mode for Luma LPF result generation (Cur and Prev);
15: 8	R/W	0x40	reg_MATNR_mtnb_alpLP_Cgain : Scale of motion_brthp_uv to motion_brtlp_uv, normalized to 32 as 1
7: 0	R/W	0x40	reg_MATNR_mtnb_alpLP_Ygain : Scale of motion_brthp_y to motion_brtlp_y, normalized to 32 as 1

Table 9-672 NR2_MATNR_MTN_COR 0x176c

Bit(s)	R/W	Default	Description
15:12	R/W	0x3	reg_MATNR_mtn_cor_Cofst : Coring Offset for Chroma Motion.
11: 8	R/W	0x3	reg_MATNR_mtn_cor_Cgain : Gain to texture based coring for Chroma Motion. Normalized to 16 as 1
7: 4	R/W	0x3	reg_MATNR_mtn_cor_Yofst : Coring Offset for Luma Motion.
3: 0	R/W	0x3	reg_MATNR_mtn_cor_Ygain : Gain to texture based coring for Luma Motion. Normalized to 16 as 1

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Table 9-673 NR2_MATNR_MTN_GAIN 0x176d

Bit(s)	R/W	Default	Description
31:24	R/W	0x40	reg_MATNR_mtn_hp_Cgain : Gain to MotHPF_yuv[k] Chrm channel for motion calculation, normalized to 64 as 1
23:16	R/W	0x40	reg_MATNR_mtn_hp_Ygain : Gain to MotHPF_yuv[k] Luma channel for motion calculation, normalized to 64 as 1
15: 8	R/W	0x40	reg_MATNR_mtn_lp_Cgain : Gain to MotLPF_yuv[k] Chrm channel for motion calculation, normalized to 32 as 1
7: 0	R/W	0x40	reg_MATNR_mtn_lp_Ygain : Gain to MotLPF_yuv[k] Luma channel for motion calculation, normalized to 32 as 1

Table 9-674 NR2_MATNR_DEGHOST 0x176e

Bit(s)	R/W	Default	Description
30:28	R/W	0	reg_matnr_deghost_mode : // unsigned , default = 0 0:old_deghost; 1:soft_ denoise & strong_deghost; 2:strong_denoise & soft_deghost; 3:strong_denoise & strong_deghost
24:20	R/W	4	reg_matnr_deghost_ygain : // unsigned , default = 4
16:12	R/W	4	reg_matnr_deghost_cgain : // unsigned , default = 4
8	R/W	1	reg_matnr_deghost_en : // unsigned , default = 1 0: disable; 1: enable Enable signal for DeGhost function:0: disable; 1: enable
7: 4	R/W	3	reg_matnr_deghost_cos : // unsigned , default = 3 DeGhost Overshoot margin for UV channel, (X2 to u10 scale)
3: 0	R/W	3	reg_matnr_deghost_yos : // unsigned , default = 3 DeGhost Overshoot margin for Luma channel, (X2 to u10 scale)

Table 9-675 NR2_MATNR_ALPHALP_LUT0 0x176f

Bit(s)	R/W	Default	Description
31:24	R/W	0x40	reg_MATNR_AlphaLP_LUT_3 : Matnr low-pass filter alpha LUT node 3
23:16	R/W	0x80	reg_MATNR_AlphaLP_LUT_2 : Matnr low-pass filter alpha LUT node 2
15: 8	R/W	0x80	reg_MATNR_AlphaLP_LUT_1 : Matnr low-pass filter alpha LUT node 1
7: 0	R/W	0x80	reg_MATNR_AlphaLP_LUT_0 : Matnr low-pass filter alpha LUT node 0

Table 9-676 NR2_MATNR_ALPHALP_LUT1 0x1770

Bit(s)	R/W	Default	Description
31:24	R/W	0xff	reg_MATNR_AlphaLP_LUT_7 : Matnr low-pass filter alpha LUT node 7
23:16	R/W	0x80	reg_MATNR_AlphaLP_LUT_6 : Matnr low-pass filter alpha LUT node 6
15: 8	R/W	0x50	reg_MATNR_AlphaLP_LUT_5 : Matnr low-pass filter alpha LUT node 5
7: 0	R/W	0x40	reg_MATNR_AlphaLP_LUT_4 : Matnr low-pass filter alpha LUT node 4

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Table 9-677 NR2_MATNR_ALPHALP_LUT2 0x1771

Bit(s)	R/W	Default	Description
31:24	R/W	0xff	reg_MATNR_AlphaLP_LUT_11 : Matnr low-pass filter alpha LUT node 11
23:16	R/W	0xff	reg_MATNR_AlphaLP_LUT_10 : Matnr low-pass filter alpha LUT node 10
15: 8	R/W	0xff	reg_MATNR_AlphaLP_LUT_9 : Matnr low-pass filter alpha LUT node 9
7: 0	R/W	0xff	reg_MATNR_AlphaLP_LUT_8 : Matnr low-pass filter alpha LUT node 8

Table 9-678 NR2_MATNR_ALPHALP_LUT3 0x1772

Bit(s)	R/W	Default	Description
31:24	R/W	0xff	reg_MATNR_AlphaLP_LUT_15 : Matnr low-pass filter alpha LUT node 15
23:16	R/W	0xff	reg_MATNR_AlphaLP_LUT_14 : Matnr low-pass filter alpha LUT node 14
15: 8	R/W	0xff	reg_MATNR_AlphaLP_LUT_13 : Matnr low-pass filter alpha LUT node 13
7: 0	R/W	0xff	reg_MATNR_AlphaLP_LUT_12 : Matnr low-pass filter alpha LUT node 12

Table 9-679 NR2_MATNR_ALPHAHP_LUT0 0x1773

Bit(s)	R/W	Default	Description
31:24	R/W	0x40	reg_MATNR_AlphaHP_LUT_3 : Matnr high-pass filter alpha LUT node 3
23:16	R/W	0x80	reg_MATNR_AlphaHP_LUT_2 : Matnr high-pass filter alpha LUT node 2
15: 8	R/W	0x80	reg_MATNR_AlphaHP_LUT_1 : Matnr high-pass filter alpha LUT node 1
7: 0	R/W	0x80	reg_MATNR_AlphaHP_LUT_0 : Matnr high-pass filter alpha LUT node 0

Table 9-680 NR2_MATNR_ALPHAHP_LUT1 0x1774

Bit(s)	R/W	Default	Description
31:24	R/W	0xff	reg_MATNR_AlphaHP_LUT_7 : Matnr high-pass filter alpha LUT node 7
23:16	R/W	0x80	reg_MATNR_AlphaHP_LUT_6 : Matnr high-pass filter alpha LUT node 6
15: 8	R/W	0x50	reg_MATNR_AlphaHP_LUT_5 : Matnr high-pass filter alpha LUT node 5
7: 0	R/W	0x40	reg_MATNR_AlphaHP_LUT_4 : Matnr high-pass filter alpha LUT node 4

Table 9-681 NR2_MATNR_ALPHAHP_LUT2 0x1775

Bit(s)	R/W	Default	Description
31:24	R/W	0xff	reg_MATNR_AlphaHP_LUT_11 : Matnr high-pass filter alpha LUT node 11
23:16	R/W	0xff	reg_MATNR_AlphaHP_LUT_10 : Matnr high-pass filter alpha LUT node 10
15: 8	R/W	0xff	reg_MATNR_AlphaHP_LUT_9 : Matnr high-pass filter alpha LUT node 9
7: 0	R/W	0xff	reg_MATNR_AlphaHP_LUT_8 : Matnr high-pass filter alpha LUT node 8

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Table 9-682 NR2_MATNR_ALPHAHP_LUT3 0x1776

Bit(s)	R/W	Default	Description
31:24	R/W	0xff	reg_MATNR_AlphaHP_LUT_15 : Matnr high-pass filter alpha LUT node 15
23:16	R/W	0xff	reg_MATNR_AlphaHP_LUT_14 : Matnr high-pass filter alpha LUT node 14
15: 8	R/W	0xff	reg_MATNR_AlphaHP_LUT_13 : Matnr high-pass filter alpha LUT node 13
7: 0	R/W	0xff	reg_MATNR_AlphaHP_LUT_12 : Matnr high-pass filter alpha LUT node 12

Table 9-683 NR2_MATNR_MTNB_BRT 0x1777

Bit(s)	R/W	Default	Description
31:28	R/W	0x0	reg_MATNR_mtnb_BRT_limt_hi : Motion adjustment based on Brightness high side Limit. (X16 to u8 scale)
27:24	R/W	0x0	reg_MATNR_mtnb_BRT_slop_hi : Motion adjustment based on Brightness high side slope. Normalized to 16 as 1
23:16	R/W	0xa0	reg_MATNR_mtnb_BRT_thrd_hi : Motion adjustment based on Brightness high threshold.(u8 scale)
15:12	R/W	0x6	reg_MATNR_mtnb_BRT_limt_lo : Motion adjustment based on Brightness low side Limit. (X16 to u8 scale)
11: 8	R/W	0x6	reg_MATNR_mtnb_BRT_slop_lo : Motion adjustment based on Brightness low side slope. Normalized to 16 as 1
7: 0	R/W	0x64	reg_MATNR_mtnb_BRT_thrd_lo : Motion adjustment based on Brightness low threshold.(u8 scale)

Table 9-684 NR2_CUE_MODE 0x1778

Bit(s)	R/W	Default	Description
31:20	R/W	0x0	Reserved
19	R/W	0x0	Cue2_isabv_org_invert1
18	R/W	0x1	Cue2_valid_condition
17:16	R/W	0x1	Cue2_orgline_flt_sel
15:12	R/W	0x4	Cue2_orgline_flt_alph
11	R/W	0x0	Cue2_isabv_org_invert
10	R/W	0x0	Cue2_iscur_org_invert
9	R/W	0x0	Cue_enable_r : Cue right half frame enable
8	R/W	0x0	Cue_enable_l : Cue left half frame enable
6:4	R/W	0x0	reg_CUE_CON_RPLC_mode : U3, CUE pixel chroma replace mode;
3:0	R/W	0x0	reg_CUE_CHRM_FLT_mode : U4, CUE improvement filter mode,

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Table 9-685 NR2_CUE_CON_MOT_TH 0x1779

Bit(s)	R/W	Default	Description
31:24	R/W	0x0	reg_CUE_CON_Cmot_thrd2 : U8, Motion Detection threshold of up/down two rows, Chroma channel in Chroma Up-sampling Error (CUE) Detection (tighter).
23:16	R/W	0x0	reg_CUE_CON_Ymot_thrd2 : U8, Motion Detection threshold of up/mid/down three rows, Luma channel in Chroma Up-sampling Error (CUE) Detection (tighter).
15: 8	R/W	0x0	reg_CUE_CON_Cmot_thrd : U8, Motion Detection threshold of up/down two rows, Chroma channel in Chroma Up-sampling Error (CUE) Detection.
7: 0	R/W	0x0	reg_CUE_CON_Ymot_thrd : U8, Motion Detection threshold of up/mid/down three rows, Luma channel in Chroma Up-sampling Error (CUE) Detection.

Table 9-686 NR2_CUE_CON_DIF0 0x177a

Bit(s)	R/W	Default	Description
15:8	R/W	0x0	reg_CUE_CON_difP1_thrd : U8, P1 field Intra-Field top/below line chroma difference threshold,
7:0	R/W	0x0	reg_CUE_CON_difCur_thrd : U8, Current Field/Frame Intra-Field up/down line chroma difference threshold,

Table 9-687 NR2_CUE_CON_DIF1 0x177b

Bit(s)	R/W	Default	Description
19:16	R/W	0x0	reg_CUE_CON_rate0 : U4, The Krate to decide CUE by relationship between CUE_diflG and CUE_difEG
15: 8	R/W	0x0	reg_CUE_CON_difEG_thrd : U8, Theshold to the difference between current Field/Frame middle line to down line color channel(CUE_difEG).
7: 0	R/W	0x0	reg_CUE_CON_diflG_thrd : U8, Threshold to the difference between P1 field top line to current Field/Frame down line color channel (CUE_diflG).

Table 9-688 NR2_CUE_CON_DIF2 0x177c

Bit(s)	R/W	Default	Description
19:16	R/W	0x0	reg_CUE_CON_rate1 : U4, The Krate to decide CUE by relationship between CUE_difnC and CUE_difEC
15: 8	R/W	0x0	reg_CUE_CON_difEC_thrd : U8, Theshold to the difference between current Field/Frame middle line to up line color channel(CUE_difEC).
7: 0	R/W	0x0	reg_CUE_CON_difnC_thrd : U8, Threshold to the difference between P1 field bot line to current Field/Frame up line color channel (CUE_difnC).

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Table 9-689 NR2_CUE_CON_DIF3 0x177d

Bit(s)	R/W	Default	Description
19:16	R/W	0x0	reg_CUE_CON_rate2 : U4, The Krate to decide CUE by relationship between CUE_difP1 and CUE_difEP1
15: 8	R/W	0x0	reg_CUE_CON_difEP1_thrd : U8, Inter-Field top/below line to current field/frame middle line chroma difference (CUE_difEP1) threshold.
7: 0	R/W	0x0	reg_CUE_CON_difP1_thrd2 : U8, P1 field Intra-Field top/below line chroma difference threshold (tighter),

Table 9-690 NR2_CUE_PRG_DIF 0x177e

Bit(s)	R/W	Default	Description
20	R/W	0x0	reg_CUE_PRG_Enable : Enable bit for progressive video CUE detection.If interlace input video,
19:16	R/W	0x0	reg_CUE_PRG_rate : U3, The Krate to decide CUE by relationship between CUE_difCur and (CUE_difEC+CUE_difEG)
15: 8	R/W	0x0	reg_CUE_PRG_difCEG_thrd : U8, Current Frame Intra-Field up-mid and mid-down line chroma difference threshold for progressive video CUE detection,
7: 0	R/W	0x0	reg_CUE_PRG_difCur_thrd : U8, Current Frame Intra-Field up/down line chroma difference threshold,

Table 9-691 NR2_CONV_MODE 0x177f

Bit(s)	R/W	Default	Description
3:2	R/W	0x0	Conv_c444_mode : The format convert mode about 422 to 444 when data read out line buffer
1:0	R/W	0x0	Conv_c422_mode : the format convert mode about 444 to 422 when data write to line buffer

DET 3D REG DEFINE BEGIN //// 8 'h80~8'h8f

Table 9-692 DET3D_RO_SPLT_HB 0x1780

Bit(s)	R/W	Default	Description
24	R.O	0x0	RO_Det3D_Split_HB_valid : U1 horizontal LR split border detected valid signal for top half picture
20:16	R.O	0x0	RO_Det3D_Split_HB_pxnum : U5 number of pixels included for the LR split position estimation for top half picture
9: 0	R.O	0x0	RO_Det3D_Split_HB_idxX4 : S10 X4: horizontal pixel shifts of LR split position to the (ColMax/2) for top half picture

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Table 9-693 DET3D_RO_SPLT_VL 0x1781

Bit(s)	R/W	Default	Description
24	R.O	0x0	RO_Det3D_Split_VL_valid : U1 horizontal LR split border detected valid signal for top half picture
20:16	R.O	0x0	RO_Det3D_Split_VL_pxnum : U5 number of pixels included for the LR split position estimation for top half picture
9: 0	R.O	0x0	RO_Det3D_Split_VL_idxX4 : S10 X4: horizontal pixel shifts of LR split position to the (ColMax/2) for top half picture

Table 9-694 DET3D_RO_SPLT_VR 0x1782

Bit(s)	R/W	Default	Description
24	R.O	0x0	RO_Det3D_Split_VR_valid : U1 horizontal LR split border detected valid signal for top half picture
20:16	R.O	0x0	RO_Det3D_Split_VR_pxnum : U5 number of pixels included for the LR split position estimation for top half picture
9: 0	R.O	0x0	RO_Det3D_Split_VR_idxX4 : S10 X4: horizontal pixel shifts of LR split position to the (ColMax/2) for top half picture

Table 9-695 DET3D_RO_MAT_LUMA_LR 0x1783

Bit(s)	R/W	Default	Description
15:0	R.O	0x0	RO_Luma_LR_score : S2*8 LUMA statistics left right decision score for each band (8bands vertically), it can be -1/0/1:-1: most likely not LR symmetric 0: not sure 1: most likely LR symmetric
7:0	R.O	0x0	RO_Luma_LR_symtc : U1*8 Luma statistics left right pure symmetric for each band (8bands vertically), it can be 0/1: 0: not sure 1: most likely LR is pure symmetric
4:0	R.O	0x0	RO_Luma_LR_sum : S5 Total score of 8x8 Luma statistics for LR like decision, the larger this score, the more confidence that this is a LR 3D video. It is sum of RO_Luma_LR_score[0~7]

Table 9-696 DET3D_RO_MAT_LUMA_TB 0x1784

Bit(s)	R/W	Default	Description
15:0	R.O	0x0	RO_Luma_TB_score : S2*8 LUMA statistics Top/Bottom decision score for each band (8bands Horizontally),
7:0	R.O	0x0	RO_Luma_TB_symtc : Luma statistics Top/Bottompure symmetric for each band (8bands Horizontally),
4:0	R.O	0x0	RO_Luma_TB_sum : Total score of 8x8 Luma statistics for TB like decision,

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Table 9-697 DET3D_RO_MAT_CHRU_LR 0x1785

Bit(s)	R/W	Default	Description
15:0	R.O	0x0	RO_ChrU_LR_score : S2*8 LUMA statistics left right decision score for each band (8bands vertically),
7:0	R.O	0x0	RO_ChrU_LR_symtc : CHRU statistics left right pure symmetric for each band (8bands vertically),
4:0	R.O	0x0	RO_ChrU_LR_sum : Total score of 8x8 ChrU statistics for LR like decision,

Table 9-698 DET3D_RO_MAT_CHRU_TB 0x1786

Bit(s)	R/W	Default	Description
15:0	R.O	0x0	RO_ChrU_TB_score : S2*8 CHRU statistics Top/Bottom decision score for each band (8bands Horizontally)
7:0	R.O	0x0	RO_ChrU_TB_symtc : CHRU statistics Top/Bottompure symmetric for each band (8bands Horizontally)
4:0	R.O	0x0	RO_ChrU_TB_sum : Total score of 8x8 ChrU statistics for TB like decision

Table 9-699 DET3D_RO_MAT_CHRV_LR 0x1787

Bit(s)	R/W	Default	Description
15:0	R.O	0x0	RO_ChrV_LR_score : S2*8 CHRUstatistics left right decision score for each band (8bands vertically)
7:0	R.O	0x0	RO_ChrV_LR_symtc : CHRV statistics left right pure symmetric for each band (8bands vertically)
4:0	R.O	0x0	RO_ChrV_LR_sum : Total score of 8x8 ChrV statistics for LR like decision

Table 9-700 DET3D_RO_MAT_CHRV_TB 0x1788

Bit(s)	R/W	Default	Description
15:0	R.O	0x0	RO_ChrV_TB_score : CHRV statistics Top/Bottom decision score for each band (8bands Horizontally)
7:0	R.O	0x0	RO_ChrV_TB_symtc : CHRV statistics Top/Bottompure symmetric for each band (8bands Horizontally)
4:0	R.O	0x0	RO_ChrV_TB_sum : Total score of 8x8 ChrV statistics for TB like decision

Table 9-701 DET3D_RO_MAT_HEDG_LR 0x1789

Bit(s)	R/W	Default	Description
15:0	R.O	0x0	RO_Hedg_LR_score : Horizontal Edge statistics left right decision score for each band (8bands vertically)
7:0	R.O	0x0	RO_Hedg_LR_symtc : Horizontal Edge statistics left right pure symmetric for each band (8bands vertically)
4:0	R.O	0x0	RO_Hedg_LR_sum : Total score of 8x8 Hedg statistics for LR like decision

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Table 9-702 DET3D_RO_MAT_HEDG_TB 0x178a

Bit(s)	R/W	Default	Description
15:0	R.O	0x0	RO_Hedg_TB_score : Horizontal Edge statistics Top/Bottom decision score for each band (8bands Horizontally)
7:0	R.O	0x0	RO_Hedg_TB_symtc : Horizontal Edge statistics Top/Bottompure symmetric for each band (8bands Horizontally)
4:0	R.O	0x0	RO_Hedg_TB_sum : Total score of 8x8 Hedg statistics for TB like decision

Table 9-703 DET3D_RO_MAT_VEDG_LR 0x178b

Bit(s)	R/W	Default	Description
15:0	R.O	0x0	RO_Vedg_LR_score : Vertical Edge statistics left right decision score for each band (8bands vertically)
7:0	R.O	0x0	RO_Vedg_LR_symtc : Vertical Edge statistics left right pure symmetric for each band (8bands vertically)
4:0	R.O	0x0	RO_Vedg_LR_sum : Total score of 8x8 Vedg statistics for LR like decision

Table 9-704 DET3D_RO_MAT_VEDG_TB 0x178c

Bit(s)	R/W	Default	Description
15:0	R.O	0x0	RO_Vedg_TB_score : Vertical Edge statistics Top/Bottom decision score for each band (8bands Horizontally)
7:0	R.O	0x0	RO_Vedg_TB_symtc : Vertical Edge statistics Top/Bottompure symmetric for each band (8bands Horizontally)
4:0	R.O	0x0	RO_Vedg_TB_sum : Total score of 8x8 Vedg statistics for TB like decision

Table 9-705 DET3D_RO_MAT_MOTN_LR 0x178d

Bit(s)	R/W	Default	Description
15:0	R.O	0x0	RO_Motn_LR_score : Motion statistics left right decision score for each band (8bands vertically)
7:0	R.O	0x0	RO_Motn_LR_symtc : Motion statistics left right pure symmetric for each band (8bands vertically)
4:0	R.O	0x0	RO_Motn_LR_sum : Total score of 8x8 Motion statistics for LR like decision

Table 9-706 DET3D_RO_MAT_MOTN_TB 0x178e

Bit(s)	R/W	Default	Description
15:0	R.O	0x0	RO_Motn_TB_score : Motion statistics Top/Bottom decision score for each band (8bands Horizontally)
7:0	R.O	0x0	RO_Motn_TB_symtc : Motion statistics Top/Bottompure symmetric for each band (8bands Horizontally)
4:0	R.O	0x0	RO_Motn_TB_sum : Total score of 8x8 Motion statistics for TB like decision

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Table 9-707 DET3D_RO_FRM_MOTN 0x178f

Bit(s)	R/W	Default	Description
15:0	R.O	0x0	RO_Det3D_Frame_Motion : U16 frame based motion value sum for still image decision in FW. mat ram read enter addr

DET3D_RAMRD_ADDR_PORT 0x179a

DET3D_RAMRD_DATA_PORT 0x179b

Table 9-708 NR2_CFR_PARA_CFG0 0x179c

Bit(s)	R/W	Default	Description
8	R/W	0x0	reg_CFR_CurDif_luma_mode : Current Field Top/Bot line Luma difference calculation mode
7:6	R/W	0x0	reg_MACFR_frm_phase : U2 This will be a field based phase register that need to be set by FW phase to phase: this will be calculated based on dbdr_phase of the specific line of this frame. u1 : dbdr_phase=1, center line is DB in current line; dbdr_phase=2, center line is Dr in current line;
5:4	R/W	0x0	reg_CFR_CurDif_tran_mode : U2 Current Field Top/Bot line Luma/Chroma transition level calculation mode,
3:2	R/W	0x0	reg_CFR_alpha_mode : U2 Alpha selection mode for CFR block from curAlp and motAlp i.e. 0: motAlp; 1: (motAlp+curAlp)/2; 2: min(motAlp,curAlp); 3: max(motAlp,curAlp);
1:0	R/W	0x0	reg_CFR_Motion_Luma_mode : U2 LumaMotion Calculation mode for MA-CFR. 0: top/bot Lumma motion; 1: middle Luma Motion 2: top/bot + middle motion; 3: max(top/tot motion, middle motion)

Table 9-709 NR2_CFR_PARA_CFG1 0x179d

Bit(s)	R/W	Default	Description
23:16	R/W	0x0	reg_CFR_alpha_gain : gain to map muxed curAlp and motAlp to alpha that will be used for final blending.
15: 8	R/W	0x0	reg_CFR_Motion_ofst : Offset to Motion to calculate the motAlp, e,g:motAlp= reg_CFR_Motion_ofst- Motion;This register can be seen as the level of motion that we consider it at moving.
7: 0	R/W	0x0	reg_CFR_CurDif_gain : gain to CurDif to map to alpha, normalized to 32;

Table 9-710 NR3_MODE 0x2ff0

Bit(s)	R/W	Default	Description
5	R/W	0x0	reg_3dnr_nr3_vtxt_mode : ;
4	R/W	0x0	reg_3dnr_nr3_cbyy_ignor_coop : ; // u1: ignore coop condition for cbyy motion decision
3	R/W	0x0	reg_3dnr_nr3_ybyc_ignor_cnoop : ; // u1: ignore cnoop condition for ybyc motion decision
2:0	R/W	0x3	reg_3dnr_nr3_suremot_txt_mode : ; // u3: 0: cur, 1:p2; 2: (cur+p2)/2; 3/up: min (cur,p2)

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Table 9-711 NR3_COOP_PARA 0x2ff1

Bit(s)	R/W	Default	Description
21:20	R/W	0x2	reg_3dnr_nr3_coop_mode : ; // u2 0 original pixel 1: [1 2 1]/4 lpf; 2: [1 2 2 2 1]/8; 3: 3x3 lpf
19:16	R/W	0x8	reg_3dnr_nr3_coop_ratio : ; // u4 cur and p2 color oop decision ratio: (avg1< (MAX(sat0,sat2)*ratio/8 + ofst));
15:8	R/W	0x0	reg_3dnr_nr3_coop_ofset : ; // s8 cur and p2 color oop decision ofst: (avg1< (MAX(sat0,sat2)*ratio/8 + ofst));
7:0	R/W	0x0	reg_3dnr_nr3_coop_sat_thrd : ; // u8 cur and p2 color oop decision min(sat0, sat1) threshold;

Table 9-712 NR3_CNOOP_GAIN 0x2ff2

Bit(s)	R/W	Default	Description
23:20	R/W	0x8	reg_3dnr_nr3_cnoop_ratio0 : ; // u4 cur and p2 color noop decision ratio0: (avg1<(MAX(sat0,sat2)*ratio0/8 + ofst0));
19:16	R/W	0x8	reg_3dnr_nr3_cnoop_ratio1 : ; // u4 cur and p2 color noop decision ratio1: (dif1< (MIN(sat0,sat2)*ratio1/8 + ofst1));
15:8	R/W	0x19	reg_3dnr_nr3_cnoop_ofset0 : ; // s8 cur and p2 color noop decision ofset0: (avg1<(MAX(sat0,sat2)*ratio0/8 + ofst0));
7:0	R/W	0x0	reg_3dnr_nr3_cnoop_ofset1 : ; // s8 cur and p2 color noop decision ofset1: (dif1< (MIN(sat0,sat2)*ratio1/8 + ofst1));

Table 9-713 NR3_YMOT_PARA 0x2ff3

Bit(s)	R/W	Default	Description
19	R/W	0x1	reg_3dnr_nr3_ymot_only_en : ; // u1: enable signal for ignor chroma motion: (ytxt)
18	R/W	0x1	reg_3dnr_nr3_ymot_only_cmtmode : ; // u1: 0: cmot=ymot; 1: cmot = MIN(ymot, cmot)
17:16	R/W	0x0	reg_3dnr_nr3_ymot_only_txtmode : ; // u2: 0, min(txt0,txt2); 1, max(txt0,txt2);2, (txt0+txt2)/2; 3: sat(txt0, txt2)
15:8	R/W	0xa	reg_3dnr_nr3_ymot_only_txtthrd : ; // u8: threshold to luma texture to decide use ymot only
7:0	R/W	0x1e	reg_3dnr_nr3_ymot_only_motthrd : ; // u8: threshold to luma motion to decide use ymot only

Table 9-714 NR3_CMOT_PARA 0x2ff4

Bit(s)	R/W	Default	Description
19	R/W	0x1	reg_3dnr_nr3_cmot_only_en : ; // u1: enable signal for ignor luma motion: (ctxt)
18	R/W	0x0	reg_3dnr_nr3_cmot_only_ymtmode : ; // u1: 0: ymot=cmot+ymot/4; 1: ymot = MIN(ymot, cmot)
17:16	R/W	0x0	reg_3dnr_nr3_cmot_only_txtmode : ; // u2: 0, min(txt0,txt2); 1, max(txt0,txt2);2, (txt0+txt2)/2; 3: sat(txt0, txt2)

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Bit(s)	R/W	Default	Description
15:8	R/W	0x14	reg_3dnr_nr3_cmot_only_txtthrd : ; // u8: threshold to chroma texture to decide use cmot only
7:0	R/W	0xf	reg_3dnr_nr3_cmot_only_motthrd : ; // u8: threshold to chroma motion to decide use cmot only

Table 9-715 NR3_SUREMOT_YGAIN 0x2ff5

Bit(s)	R/W	Default	Description
31:24	R/W	0x10	reg_3dnr_nr3_suremot_dec_yrate : ; // u8: (norm 16)lpfMot>(dec_rate*txt +ofst) then force lpfMot*frc_gain+frc_ofset
23:16	R/W	0xc	reg_3dnr_nr3_suremot_dec_yofst : ; // u8: lpfMot>(dec_rate*txt +ofst) then force lpfMot*frc_gain+frc_ofset
15:8	R/W	0x40	reg_3dnr_nr3_suremot_frc_ygain : ; // u8: (norm 8)lpfMot>(dec_rate*txt +ofst) then force lpfMot*frc_gain+frc_ofset
7:0	R/W	0x14	reg_3dnr_nr3_suremot_frc_yofst : ; // u8: lpfMot>(dec_rate*txt +ofst) then force lpfMot*frc_gain+frc_ofset

Table 9-716 NR3_SUREMOT_CGAIN 0x2ff6

Bit(s)	R/W	Default	Description
31:24	R/W	0x22	reg_3dnr_nr3_suremot_dec_crate : ; // u8: (norm 16)lpfMot>(dec_rate*txt +ofst) then force lpfMot*frc_gain+frc_ofset
23:16	R/W	0x26	reg_3dnr_nr3_suremot_dec_cofst : ; // u8: lpfMot>(dec_rate*txt +ofst) then force lpfMot*frc_gain+frc_ofset
15:8	R/W	0x40	reg_3dnr_nr3_suremot_frc_cgain : ; // u8: (norm 8)lpfMot>(dec_rate*txt +ofst) then force lpfMot*frc_gain+frc_ofset
7:0	R/W	0x14	reg_3dnr_nr3_suremot_frc_cofst : ; // u8: lpfMot>(dec_rate*txt +ofst) then force lpfMot*frc_gain+frc_ofset

9.2.3.11 LBUF Registers

Table 9-717 LBUF_TOP_CTRL 0x2fff

Bit(s)	R/W	Default	Description
25:20	R/W	6'd0	gate clk control of line buf . LBUF_TOP_CTRL[25:24] is the clk control of current line linebuffer. LBUF_TOP_CTRL[23:22] is the clk control of previous one line.linebuffer, LBUF_TOP_CTRL[21:20] is the clk control of previous two line linebuffer.
17	R/W	1'b1	lbuf_fmt444_mode; format of data store in linebuf ,high mean store 444 data into linebuf
16	R/W	1'b1	lbuf_line5_mode;Store 5 line or 3 lines in linebuf ,high means 5 lines
12:0	R/W	13'd342	pre_lbuf_size: size of linebuf

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9.2.3.12 DI_SCALE Registers

Table 9-718 DI_SCO_FIFO_CTRL 0x374e

Bit(s)	R/W	Default	Description
28:0	R/W	0x0	sco_fifo_ctrl

Table 9-719 DI_SC_TOP_CTRL 0x374f

Bit(s)	R/W	Default	Description
31	R.O	0	prog_interlace : no use // unsigned , default = 0x0
30	R/W	0	path_sel : 1 : di pre scaler for nr inp 0: di post scaler // unsigned , default = 0x0
29	R/W	0	go_field_sel : 1 : di pre go field 0: di post go filed // unsigned , default = 0x0
28	R/W	0	sw_resets : // unsigned , default = 0x0
27	R/W	0	pps_dummy_data_mode : 1: use low 8 bits 0: use high 8 bits // unsigned , default = 0x0
26	R/W	0	field_inv : field reverse// unsigned , default = 0x0
25	R/W	0	reg_field : no use// unsigned , default = 0x0
5:4	R/W	0	hdr_gclk_ctrl : 01 : no cbus clock for hdr other: free cbus clock for hdr // unsigned , default = 0x0
1	R/W	0	reg_gclk_ctrl : 1 : free clock for di scaler register 0: auto gate for di scalercbus // unsigned , default = 0x0

Table 9-720 DI_SC_DUMMY_DATA 0x3750

Bit(s)	R/W	Default	Description
29:20	R/W	0	VD1_SC_Y : // unsigned , default = 0x10,dummy data used in the VD1 scaler,according VPP_DOLBY_CTRL[17] 1:set 8bit value 2:set 10bit value
19:10	R/W	0	VD1_SC_CB : // unsigned , default = 0x80,dummy data used in the VD1 scaler, according VPP_DOLBY_CTRL[17] 1:set 8bit value 2:set 10bit value
9 :0	R/W	0	VD1_SC_CR : // unsigned , default = 0x80,dummy data used in the VD1 scaler, according VPP_DOLBY_CTRL[17] 1:set 8bit value 2:set 10bit value

Table 9-721 DI_SC_LINE_IN_LENGTH 0x3751

Bit(s)	R/W	Default	Description
13:0	R/W	14	line_in_length : // unsigned , default = 14'd1920,VD1 scaler input hsize

Table 9-722 DI_SC_PIC_IN_HEIGHT 0x3752

Bit(s)	R/W	Default	Description
12:0	R/W	0x1fff	line_in_height : // unsigned , default = 13'h1fff,VD1 scaler input vsize

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Table 9-723 DI_SC_COEF_IDX 0x3753

Bit(s)	R/W	Default	Description
15	R/W	0	index_inc : // unsigned , default = 0x0 ,index increment, if bit9 = 1 then (0: index increase 1, 1: index increase 2) else (index increase 2)
14	R/W	0	rd_cbus_coef_en : // unsigned , default = 0x0 ,1: read coef through cbus enable, just for debug purpose in case when we wanna check the coef in ram in correct or not
13	R/W	0	vf_sep_coef_en : // unsigned , default = 0x0 ,if true, vertical separated coef enable
9	R/W	0	high_reso_en : // unsigned , default = 0x0 ,if true, use 9bit resolution coef, other use 8bit resolution coef
8:7	R/W	0	type_index : // unsigned , default = 0x0 ,type of index, 00: vertical coef, 01: vertical chroma coef: 10: horizontal coef, 11: resevered
6:0	R/W	0	coef_index : // unsigned , default = 0x0 ,coef index

Table 9-724 DI_SC_COEF 0x3754

Bit(s)	R/W	Default	Description
31:24	R/W	0	coef0 : //signed , default = 0x0 , coefficients for vertical filter and horizontal filter
23:16	R/W	0	coef1 : //signed , default = 0x0 , coefficients for vertical filter and horizontal filter
15:8	R/W	0	coef2 : //signed , default = 0x0 , coefficients for vertical filter and horizontal filter
7 :0	R/W	0	coef3 : //signed , default = 0x0 , coefficients for vertical filter and horizontal filter

Table 9-725 DI_VSC_REGION12_STARTP 0x3755

Bit(s)	R/W	Default	Description
28:16	R/W	0	region1_startp : //unsigned , default = 0 ,region1 startp
12:0	R/W	0	region2_startp : //unsigned , default = 0 ,region2 startp

Table 9-726 DI_VSC_REGION34_STARTP 0x3756

Bit(s)	R/W	Default	Description
28:16	R/W	0	region3_startp : //unsigned , default = 0x0438,region3 startp
12:0	R/W	0	region4_startp : //unsigned , default = 0x0438,region4 startp

Table 9-727 DI_VSC_REGION4_ENDP 0x3757

Bit(s)	R/W	Default	Description
12:0	R/W	13	region4_endp : //unsigned , default = 13'd1079 ,region4 endp

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Table 9-728 DI_VSC_START_PHASE_STEP 0x3758

Bit(s)	R/W	Default	Description
27:24	R/W	1	integer_part : //unsigned , default = 1,vertical start phase step, (source/dest)* (2^24),integer part of step
23:0	R/W	0	fraction_part : //unsigned , default = 0,vertical start phase step, (source/dest)* (2^24),fraction part of step

Table 9-729 DI_VSC_REGION0_PHASE_SLOPE 0x3759

Bit(s)	R/W	Default	Description
24:0	R/W	0	region0_phase_slope : //signed , default = 0,vertical scaler region0 phase slope, region0 phase slope

Table 9-730 DI_VSC_REGION1_PHASE_SLOPE 0x375a

Bit(s)	R/W	Default	Description
24:0	R/W	0	region1_phase_slope : //signed , default = 0,region1 phase slope

Table 9-731 DI_VSC_REGION3_PHASE_SLOPE 0x375b

Bit(s)	R/W	Default	Description
24:0	R/W	0	region3_phase_slope : //signed , default = 0,region3 phase slope

Table 9-732 DI_VSC_REGION4_PHASE_SLOPE 0x375c

Bit(s)	R/W	Default	Description
24:0	R/W	0	region4_phase_slope : //signed , default = 0,region4 phase slope

Table 9-733 DI_VSC_PHASE_CTRL 0x375d

Bit(s)	R/W	Default	Description
18:17	R/W	0	vsc_double_line_mode : //unsigned , default = 0, double line mode, input/output line width of vscaler becomes 2X, so only 2 line buffer in this case, use for 3D line by line interleave scaling bit1 true, double the input width and half input height, bit0 true, change line buffer 2 lines instead of 4 lines
16	R.O	0	prog_interlace : //unsigned , default = 0,0: progressive output, 1: interlace output
15	R/W	0	vsc_bot_l0_out_en : //unsigned , default = 0,vertical scaler output line0 in advance or not for bottom field
14:13	R/W	1	vsc_bot_rpt_l0_num : //unsigned , default = 1,vertical scaler initial repeat line0 number for bottom field
11:8	R/W	4	vsc_bot_ini_rcv_num : //unsigned , default = 4,vertical scaler initial receiving number for bottom field
7	R/W	0	vsc_top_l0_out_en : //unsigned , default = 0,vertical scaler output line0 in advance or not for top field

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Bit(s)	R/W	Default	Description
6:5	R/W	1	vsc_top_rpt_l0_num : //unsigned , default = 1,vertical scaler initial repeat line0 number for top field
3:0	R/W	4	vsc_top_ini_rcv_num : //unsigned , default = 4,vertical scaler initial receiving number for top field

Table 9-734 DI_VSC_INI_PHASE 0x375e

Bit(s)	R/W	Default	Description
31:16	R/W	0	vertical scaler field initial phase for bottom field
15:0	R/W	0	vertical scaler field initial phase for top field

Table 9-735 DI_HSC_REGION12_STARTP 0x3760

Bit(s)	R/W	Default	Description
28:16	R/W	0	region1_startp : //unsigned , default = 0,region1 startp
12:0	R/W	0	region2_startp : //unsigned , default = 0,region2 startp

Table 9-736 DI_HSC_REGION34_STARTP 0x3761

Bit(s)	R/W	Default	Description
28:16	R/W	0	region3 : startp //unsigned , default = 0x780,region3 startp
12:0	R/W	0	region4 : startp //unsigned , default = 0x780,region4 startp

Table 9-737 DI_HSC_REGION4_ENDP 0x3762

Bit(s)	R/W	Default	Description
12:0	R/W	13	region4 : startp //unsigned , default = 13'd1919,region4 startp

Table 9-738 DI_HSC_START_PHASE_STEP 0x3763

Bit(s)	R/W	Default	Description
27:24	R/W	1	integer_part : //unsigned , default = 1,integer part of step
23:0	R/W	0	fraction_part : //unsigned , default = 0,fraction part of step

Table 9-739 DI_HSC_REGION0_PHASE_SLOPE 0x3764

Bit(s)	R/W	Default	Description
24:0	R/W	0	region0_phase_slope : //signed , default = 0,region0 phase slope

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Table 9-740 DI_HSC_REGION1_PHASE_SLOPE 0x3765

Bit(s)	R/W	Default	Description
24:0	R/W	0	region0_phase_slope : //signed , default = 0,region1 phase slope

Table 9-741 DI_HSC_REGION3_PHASE_SLOPE 0x3766

Bit(s)	R/W	Default	Description
24:0	R/W	0	region0_phase_slope : //signed , default = 0,region3 phase slope

Table 9-742 DI_HSC_REGION4_PHASE_SLOPE 0x3767

Bit(s)	R/W	Default	Description
24:0	R/W	0	region0_phase_slope : //signed , default = 0,region4 phase slope

Table 9-743 DI_HSC_PHASE_CTRL 0x3768

Bit(s)	R/W	Default	Description
22:21	R/W	1	hsc_rpt_p0_num0 : //unsigned , default = 1 ,horizontal scaler initial repeat pixel0 number0
19:16	R/W	4	hsc_ini_rcv_num0 : //unsigned , default = 4 ,horizontal scaler initial receiving number0
15:0	R/W	0	hsc_ini_phase0 : //unsigned , default = 0 ,horizontal scaler top field initial phase0

Table 9-744 DI_SC_MISC 0x3769

Bit(s)	R/W	Default	Description
22	R/W	0	hsc_len_div2_en : //unsigned , default = 0 ,if true, divide VSC line length 2 as the HSC input length, othwise VSC length length is the same as the VSC line length just for special usage, more flexibilityi
21	R/W	0	lbuf_mode : //unsigned , default = 0 ,if true, prevsc uses lin buffer, otherwise prevsc does not use line buffer, it should be same as prevsc_en
20	R/W	0	prehsc_en : //unsigned , default = 0 ,prehsc_en
19	R/W	0	prevsc_en : //unsigned , default = 0 ,prevsc_en
18	R/W	0	vsc_en : //unsigned , default = 0 ,vsc_en
17	R/W	0	hsc_en : //unsigned , default = 0 ,hsc_en
16	R/W	0	sc_top_en : //unsigned , default = 0 ,scale_top_en
15	R/W	0	sc_vd_en : //unsigned , default = 0 ,video1 scale out enable
12	R/W	1	hsc_nonlinear_4region_en : //unsigned , default = 1 ,if true, region0,region4 are nonlinear regions, otherwise they are not scaling regions, for horizontal scaler
10:8	R/W	0	hsc_bank_length : //unsigned , default = 0 ,horizontal scaler bank length
5	R/W	4	vsc_phase_field_mode : //unsigned , default = 4 ,vertical scaler phase field mode, if true, disable the opposite parity line output, more bandwith needed if output 1080i

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Bit(s)	R/W	Default	Description
4	R/W	0	vsc_nonlinear_4region_en : //unsigned , default = 0 ,if true, region0,region4 are nonlinear regions, otherwise they are not scaling regions, for vertical scaler
2:0	R/W	4	vsc_bank_length : //unsigned , default = 4 ,vertical scaler bank length

Table 9-745 DI_HSC_PHASE_CTRL1 0x376a

Bit(s)	R/W	Default	Description
22:21	R/W	1	hsc_rpt_p0_num0 : //unsigned , default = 1 ,horizontal scaler initial repeat pixel0 number0
19:16	R/W	4	hsc_ini_rcv_num0 : //unsigned , default = 4 ,horizontal scaler initial receiving number0
15:0	R/W	0	hsc_ini_phase0 : //unsigned , default = 0 ,horizontal scaler top field initial phase0

Table 9-746 VPP_SC_MISC 0x1D19

Bit(s)	R/W	Default	Description
22	R/W	0	hsc_len_div2_en : //unsigned , default = 0 ,if true, divide VSC line length 2 as the HSC input length, othwise VSC length length is the same as the VSC line length just for special usage, more flexibilityi
21	R/W	0	lbuf_mode : //unsigned , default = 0 ,if true, prevsc uses lin buffer, otherwise prevsc does not use line buffer, it should be same as prevsc_en
20	R/W	0	prehsc_en : //unsigned , default = 0 ,prehsc_en
19	R/W	0	prevsc_en : //unsigned , default = 0 ,prevsc_en
18	R/W	0	vsc_en : //unsigned , default = 0 ,vsc_en
17	R/W	0	hsc_en : //unsigned , default = 0 ,hsc_en
16	R/W	0	sc_top_en : //unsigned , default = 0 ,scale_top_en
15	R/W	0	sc_vd_en : //unsigned , default = 0 ,video1 scale out enable
12	R/W	1	hsc_nonlinear_4region_en : //unsigned , default = 1 ,if true, region0,region4 are nonlinear regions, otherwise they are not scaling regions, for horizontal scaler
10:8	R/W	0	hsc_bank_length : //unsigned , default = 0 ,horizontal scaler bank length
5	R/W	4	vsc_phase_field_mode : //unsigned , default = 4 ,vertical scaler phase field mode, if true, disable the opposite parity line output, more bandwith needed if output 1080i
4	R/W	0	vsc_nonlinear_4region_en : //unsigned , default = 0 ,if true, region0,region4 are nonlinear regions, otherwise they are not scaling regions, for vertical scaler
2:0	R/W	4	vsc_bank_length : //unsigned , default = 4 ,vertical scaler bank length

Table 9-747 DI_HSC_INI_PAT_CTRL 0x376b

Bit(s)	R/W	Default	Description
31:24	R/W	0	prehsc_pattern : //unsigned , default = 0, prehsc pattern, each patten 1 bit, from lsb -> msb
22:20	R/W	0	prehsc_pat_star : //unsigned , default = 0, prehsc pattern start

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Bit(s)	R/W	Default	Description
18:16	R/W	0	prehsc_pat_end : //unsigned , default = 0, prehsc pattern end
15:8	R/W	0	hsc_pattern : //unsigned , default = 0, hsc pattern, each patten 1 bit, from lsb -> msb
6:4	R/W	0	hsc_pat_start : //unsigned , default = 0, hsc pattern start
2:0	R/W	0	hsc_pat_end : //unsigned , default = 0, hsc pattern end

Table 9-748 DI_SC_GCLK_CTRL 0x376c

Bit(s)	R/W	Default	Description
15:0	R/W	0	vpp_sc_gclk_ctrl : //unsigned , default = 0,

Table 9-749 DI_SC_HOLD_LINE 0x376d

Bit(s)	R/W	Default	Description
31:0	R/W	0	sc_hold_line : //unsigned , default = 0,

Table 9-750 DI_HDR_IN_HSIZE 0x376e

Bit(s)	R/W	Default	Description
12:0	R/W	0	hdr input h size

Table 9-751 DI_HDR_IN_VSIZE 0x376f

Bit(s)	R/W	Default	Description
12:0	R/W	0	hdr input v size

Table 9-752 DI_HDR2_CTRL 0x3770

Bit(s)	R/W	Default	Description
20:18	R/W	0	reg_din_swap : // unsigned , default = 0
17	R/W	0	reg_out_fmt : // unsigned , default = 0
16	R/W	0	reg_only_mat : // unsigned , default = 0
13	R/W	0	reg_VDIN0_HDR2_top_en : // unsigned , default = 0
12	R/W	1	reg_cgain_mode : // unsigned , default = 1
7: 6	R/W	1	reg_gmut_mode : // unsigned , default = 1
5	R/W	0	reg_in_shift : // unsigned , default = 0
4	R/W	1	reg_in_fmt : // unsigned , default = 1
3	R/W	1	reg_eo_enable : // unsigned , default = 1
2	R/W	1	reg_oe_enable : // unsigned , default = 1

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Bit(s)	R/W	Default	Description
1	R/W	1	reg_ogain_enable : // unsigned , default = 1
0	R/W	1	reg_cgain_enable : // unsigned , default = 1

Table 9-753 DI_HDR2_CLK_GATE 0x3771

Bit(s)	R/W	Default	Description
31:30	R/W	0	clk_tm : gate clock ctrl (main clock) // unsigned , default = 0
29:28	R/W	0	output : matrix clock gate ctrl // unsigned , default = 0
25:24	R/W	0	input : matrix clock gate ctrl // unsigned , default = 0
23:22	R/W	0	hdr : top cbus clock gate ctrl // unsigned , default = 0
21:20	R/W	0	eotf : cbus clock gate ctrl // unsigned , default = 0
19:18	R/W	0	oetf : cbus clock gate ctrl // unsigned , default = 0
17:16	R/W	0	gamma : mult cbus clock gate ctrl // unsigned , default = 0
15:14	R/W	0	adaptive : cbus scaler clock gate ctrl // unsigned , default = 0
13:12	R/W	0	cgain : cbus clock gate ctrl // unsigned , default = 0
11:10	R/W	0	eotf : clock gate ctrl // unsigned , default = 0
9:8	R/W	0	oetf : clock gate ctrl // unsigned , default = 0
7:6	R/W	0	gamma : mult clock gate ctrl // unsigned , default = 0
5:4	R/W	0	adaptive : scaler clock gate ctrl // unsigned , default = 0
3:2	R/W	0	uv : gain clock gate ctrl // unsigned , default = 0
1:0	R/W	0	cgain : clock gate ctrl // unsigned , default = 0

Table 9-754 DI_HDR2_MATRIXI_COEF00_01 0x3772

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef00 : // signed , default = 0
12:0	R/W	0	coef01 : // signed , default = 0

Table 9-755 DI_HDR2_MATRIXI_COEF02_10 0x3773

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef02 : // signed , default = 0
12:0	R/W	0	coef10 : // signed , default = 0

Table 9-756 DI_HDR2_MATRIXI_COEF11_12 0x3774

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef11 : // signed , default = 0
12:0	R/W	0	coef12 : // signed , default = 0

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Table 9-757 DI_HDR2_MATRIXI_COEF20_21 0x3775

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef20 : // signed , default = 0
12:0	R/W	0	coef21 : // signed , default = 0

Table 9-758 DI_HDR2_MATRIXI_COEF22 0x3776

Bit(s)	R/W	Default	Description
12:0	R/W	0	coef22 : // signed , default = 0

Table 9-759 DI_HDR2_MATRIXI_COEF30_31 0x3777

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef13 : // signed , default = 0
12:0	R/W	0	coef14 : // signed , default = 0

Table 9-760 DI_HDR2_MATRIXI_COEF32_40 0x3778

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef23 : // signed , default = 0
12:0	R/W	0	coef24 : // signed , default = 0

Table 9-761 DI_HDR2_MATRIXI_COEF41_42 0x3779

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef15 : // signed , default = 0
12:0	R/W	0	coef25 : // signed , default = 0

Table 9-762 DI_HDR2_MATRIXI_OFFSET0_1 0x377A

Bit(s)	R/W	Default	Description
26:16	R/W	0	offset0 : // signed , default = 0
10:0	R/W	0	offset1 : // signed , default = 0

Table 9-763 DI_HDR2_MATRIXI_OFFSET2 0x377B

Bit(s)	R/W	Default	Description
10:0	R/W	0	offset2 : // signed , default = 0

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Table 9-764 DI_HDR2_MATRIXI_PRE_OFFSET0_1 0x377C

Bit(s)	R/W	Default	Description
26:16	R/W	0	pre_offset0 : // signed , default = 0
10:0	R/W	0	pre_offset1 : // signed , default = 0

Table 9-765 DI_HDR2_MATRIXI_PRE_OFFSET2 0x377D

Bit(s)	R/W	Default	Description
10:0	R/W	0	pre_offset2 : // signed , default = 0

Table 9-766 DI_HDR2_MATRIXO_COEF00_01 0x377E

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef00 : // signed , default = 0
12:0	R/W	0	coef01 : // signed , default = 0

Table 9-767 DI_HDR2_MATRIXO_COEF02_10 0x377F

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef02 : // signed , default = 0
12:0	R/W	0	coef10 : // signed , default = 0

Table 9-768 DI_HDR2_MATRIXO_COEF11_12 0x3780

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef11 : // signed , default = 0
12:0	R/W	0	coef12 : // signed , default = 0

Table 9-769 DI_HDR2_MATRIXO_COEF20_21 0x3781

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef20 : // signed , default = 0
12:0	R/W	0	coef21 : // signed , default = 0

Table 9-770 DI_HDR2_MATRIXO_COEF22 0x3782

Bit(s)	R/W	Default	Description
12:0	R/W	0	coef22 : // signed , default = 0

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Table 9-771 DI_HDR2_MATRIXO_COEF30_31 0x3783

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef13 : // signed , default = 0
12:0	R/W	0	coef14 : // signed , default = 0

Table 9-772 DI_HDR2_MATRIXO_COEF32_40 0x3784

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef23 : // signed , default = 0
12:0	R/W	0	coef24 : // signed , default = 0

Table 9-773 DI_HDR2_MATRIXO_COEF41_42 0x3785

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef15 : // signed , default = 0
12:0	R/W	0	coef25 : // signed , default = 0

Table 9-774 DI_HDR2_MATRIXO_OFFSET0_1 0x3786

Bit(s)	R/W	Default	Description
26:16	R/W	0	offset0 : // signed , default = 0
10:0	R/W	0	offset1 : // signed , default = 0

Table 9-775 DI_HDR2_MATRIXO_OFFSET2 0x3787

Bit(s)	R/W	Default	Description
10:0	R/W	0	offset2 : // signed , default = 0

Table 9-776 DI_HDR2_MATRIXO_PRE_OFFSET0_1 0x3788

Bit(s)	R/W	Default	Description
26:16	R/W	0	pre_offset0 : // signed , default = 0
10:0	R/W	0	pre_offset1 : // signed , default = 0

Table 9-777 DI_HDR2_MATRIXO_PRE_OFFSET2 0x3789

Bit(s)	R/W	Default	Description
10:0	R/W	0	pre_offset2 : // signed , default = 0

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Table 9-778 DI_HDR2_MATRIXI_CLIP 0x378A

Bit(s)	R/W	Default	Description
19:8	R/W	0	comp_th : // unsigned , default = 0
7:5	R/W	0	conv_rs : // unsigned , default = 0
4:3	R/W	0	clmod : // unsigned , default = 0

Table 9-779 DI_HDR2_MATRIXO_CLIP 0x378B

Bit(s)	R/W	Default	Description
19:8	R/W	0	comp_th : // unsigned , default = 0
7:5	R/W	0	conv_rs : // unsigned , default = 0
4:3	R/W	0	clmod : // unsigned , default = 0

Table 9-780 DI_HDR2_CGAIN_OFFT 0x378C

Bit(s)	R/W	Default	Description
26:16	R/W	0	reg_cgain_oft2 : // signed , default = 0
10:0	R/W	0	reg_cgain_oft1 : // signed , default = 0

Table 9-781 DI_EOTF_LUT_ADDR_PORT 0x378E

Bit(s)	R/W	Default	Description
7:0	R/W	0	eotf_lut_addr : // unsigned , default = 0

Table 9-782 DI_EOTF_LUT_DATA_PORT 0x378F

Bit(s)	R/W	Default	Description
19:0	R/W	0	eotf_lut_data : // unsigned , default = 0

Table 9-783 DI_OETF_LUT_ADDR_PORT 0x3790

Bit(s)	R/W	Default	Description
7:0	R/W	0	oetf_lut_addr : // unsigned , default = 0

Table 9-784 DI_OETF_LUT_DATA_PORT 0x3791

Bit(s)	R/W	Default	Description
11:0	R/W	0	oetf_lut_data : // unsigned , default = 0

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Table 9-785 DI_CGAIN_LUT_ADDR_PORT 0x3792

Bit(s)	R/W	Default	Description
7:0	R/W	0	cgain_lut_addr : // unsigned , default = 0

Table 9-786 DI_CGAIN_LUT_DATA_PORT 0x3793

Bit(s)	R/W	Default	Description
11:0	R/W	0	cgain_lut_data : // unsigned , default = 0

Table 9-787 DI_HDR2_CGAIN_COEF0 0x3794

Bit(s)	R/W	Default	Description
27:16	R/W	0	reg_cgain_coef1 : // unsigned , default = 0
11:0	R/W	0	reg_cgain_coef0 : //unsigned , default = 0

Table 9-788 DI_HDR2_CGAIN_COEF1 0x3795

Bit(s)	R/W	Default	Description
11:0	R/W	0	reg_cgain_coef2 : // unsigned , default = 0

Table 9-789 DI_OGAIN_LUT_ADDR_PORT 0x3796

Bit(s)	R/W	Default	Description
7:0	R/W	0	ogain_lut_addr : // unsigned , default = 0

Table 9-790 DI_OGAIN_LUT_DATA_PORT 0x3797

Bit(s)	R/W	Default	Description
11:0	R/W	0	ogain_lut_data : // unsigned , default = 0

Table 9-791 DI_HDR2_ADPS_CTRL 0x3798

Bit(s)	R/W	Default	Description
6	R/W	1	reg_adpscl_bypass2 : // unsigned , default = 1
5	R/W	1	reg_adpscl_bypass1 : // unsigned , default = 1
4	R/W	1	reg_adpscl_bypass0 : // unsigned , default = 1
1:0	R/W	1	reg_adpscl_mode : // unsigned , default = 1

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Table 9-792 DI_HDR2_ADPS_ALPHA0 0x3799

Bit(s)	R/W	Default	Description
29:16	R/W	0x1000	reg_adpscl_alpha1 : // unsigned , default = 0x1000
13:0	R/W	0x1000	reg_adpscl_alpha0 : // unsigned , default = 0x1000

Table 9-793 DI_HDR2_ADPS_ALPHA1 0x379A

Bit(s)	R/W	Default	Description
27:24	R/W	0xc	reg_adpscl_shift0 : // unsigned , default = 0xc
23:20	R/W	0xc	reg_adpscl_shift1 : // unsigned , default = 0xc
19:16	R/W	0xc	reg_adpscl_shift2 : // unsigned , default = 0xc
13:0	R/W	0x1000	reg_adpscl_alpha2 : // unsigned , default = 0x1000

Table 9-794 DI_HDR2_ADPS_BETA0 0x379B

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta0_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta0 : // unsigned , default = 0xfc000

Table 9-795 DI_HDR2_ADPS_BETA1 0x379C

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta1_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta1 : // unsigned , default = 0xfc000

Table 9-796 DI_HDR2_ADPS_BETA2 0x379D

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta2_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta2 : // unsigned , default = 0xfc000

Table 9-797 DI_HDR2_ADPS_COEF0 0x379E

Bit(s)	R/W	Default	Description
27:16	R/W	460	reg_adpscl_ys_coef1 : // unsigned , default = 460
11:0	R/W	1188	reg_adpscl_ys_coef0 : // unsigned , default = 1188

Table 9-798 DI_HDR2_ADPS_COEF1 0x379F

Bit(s)	R/W	Default	Description
11:0	R/W	104	reg_adpscl_ys_coef2 : // unsigned , default = 104

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Table 9-799 DI_HDR2_GMUT_CTRL 0x37A0

Bit(s)	R/W	Default	Description
3:0	R/W	14	reg_gmut_shift : // unsigned , default = 14

Table 9-800 DI_HDR2_GMUT_COEF0 0x37A1

Bit(s)	R/W	Default	Description
31:16	R/W	674	reg_gmut_coef01 : // unsigned , default = 674
15:0	R/W	1285	reg_gmut_coef00 : // unsigned , default = 1285

Table 9-801 DI_HDR2_GMUT_COEF1 0x37A2

Bit(s)	R/W	Default	Description
31:16	R/W	142	reg_gmut_coef10 : // unsigned , default = 142
15:0	R/W	89	reg_gmut_coef02 : // unsigned , default = 89

Table 9-802 DI_HDR2_GMUT_COEF2 0x37A3

Bit(s)	R/W	Default	Description
31:16	R/W	23	reg_gmut_coef12 : // unsigned , default = 23
15:0	R/W	1883	reg_gmut_coef11 : // unsigned , default = 1883

Table 9-803 DI_HDR2_GMUT_COEF3 0x37A4

Bit(s)	R/W	Default	Description
31:16	R/W	180	reg_gmut_coef21 : // unsigned , default = 180
15:0	R/W	34	reg_gmut_coef20 : // unsigned , default = 34

Table 9-804 DI_HDR2_GMUT_COEF4 0x37A5

Bit(s)	R/W	Default	Description
15:0	R/W	1834	reg_gmut_coef22 : // unsigned , default = 1834

Table 9-805 DI_HDR2_PIPE_CTRL1 0x37A6

Bit(s)	R/W	Default	Description
31:24	R/W	4	vblank_num_oetf : // unsigned , default = 4
23:16	R/W	4	hblank_num_oetf : // unsigned , default = 4
15:8	R/W	10	vblank_num_eotf : // unsigned , default = 10
7:0	R/W	10	hblank_num_eotf : // unsigned , default = 10

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Table 9-806 DI_HDR2_PIPE_CTRL2 0x37A7

Bit(s)	R/W	Default	Description
31:24	R/W	10	vblank_num_cgain : // unsigned , default = 10
23:16	R/W	10	hblank_num_cgain : // unsigned , default = 10
15:8	R/W	11	vblank_num_gmut : // unsigned , default = 11
7:0	R/W	11	hblank_num_gmut : // unsigned , default = 11

Table 9-807 DI_HDR2_PIPE_CTRL3 0x37A8

Bit(s)	R/W	Default	Description
31:24	R/W	22	vblank_num_adps : // unsigned , default = 22
23:16	R/W	2	hblank_num_adps : // unsigned , default = 2
15:8	R/W	4	vblank_num_uv : // unsigned , default = 4
7:0	R/W	4	hblank_num_uv : // unsigned , default = 4

Table 9-808 DI_HDR2_PROC_WIN1 0x37A9

Bit(s)	R/W	Default	Description
28:16	R/W	0	proc_win_h_ed : // unsigned , default = 0
12:0	R/W	0	proc_win_h_st : // unsigned , default = 0

Table 9-809 DI_HDR2_PROC_WIN2 0x37AA

Bit(s)	R/W	Default	Description
31	R/W	0	proc_win_gmut_en : // unsigned , default = 0
30	R/W	0	proc_win_adps_en : // unsigned , default = 0
29	R/W	0	proc_win_cgain_en : // unsigned , default = 0
28:16	R/W	0	proc_win_v_ed : // unsigned , default = 0
12:0	R/W	0	proc_win_v_st : // unsigned , default = 0

Table 9-810 DI_HDR2_MATRIXI_EN_CTRL 0x37AB

Bit(s)	R/W	Default	Description
5:4	R/W	0	matrix_gclk_ctrl : // unsigned , default = 0
1	R/W	0	enable_sync_sel : // unsigned , default = 0
0	R/W	0	matrix_conv_en : // unsigned , default = 0

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Table 9-811 DI_HDR2_MATRIXO_EN_CTRL 0x37AC

Bit(s)	R/W	Default	Description
5:4	R/W	0	matrix_gclk_ctrl : // unsigned , default = 0
1	R/W	0	enable_sync_sel : // unsigned , default = 0
0	R/W	0	matrix_conv_en : // unsigned , default = 0

9.2.3.13 NR_SCALE Registers

Table 9-812 NRDSWR_X 0x37f9

Bit(s)	R/W	Default	Description
31:30	R/W	2	burst_len : unsigned , default = 2
29	R/W	0	rev_x : unsigned , default = 0
28:16	R/W	0	start_x : unsigned , default = 0
12:0	R/W	2	end_x : unsigned , default = 2cf

Table 9-813 NRDSWR_Y 0x37fa

Bit(s)	R/W	Default	Description
31:30	R/W	0	canvas_id : unsigned , default = 0
29	R/W	0	rev_y : unsigned , default = 0
28:16	R/W	0	start_y : unsigned , default = 0
12:0	R/W	0	end_y : unsigned , default = 0x1df

Table 9-814 NRDSWR_CTRL 0x37fb

Bit(s)	R/W	Default	Description
31:16	R/W	0	urgent_ctrl : unsigned , default = 0
15	R/W	0	force_wvalid : unsigned , default = 0
14	R/W	0	canvas_syncen : unsigned , default = 0
13	R/W	1	canvas_wr : unsigned , default = 1
12	R/W	0	req_en : unsigned , default = 0
10	R/W	0	clr_wrrsp : unsigned , default = 0
8	R/W	0	urgent : unsigned , default = 0
7:0	R/W	0	canvas_index : unsigned , default = 0

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Table 9-815 NRDSWR_CAN_SIZE 0x37fc

Bit(s)	R/W	Default	Description
30:29	R/W	0	reg_rst : unsigned , default = 0
28:16	R/W	0	hsizem1 : unsigned , default = 0x2cf
14	R/W	0	reg_reset : unsigned , default = 0
13	R/W	0	little_endian : unsigned , default = 0
12:0	R/W	0	vsizem1 : unsigned , default = 0x1df

Table 9-816 NR_DS_BUF_SIZE 0x3740

Bit(s)	R/W	Default	Description
31:24	R.O	96	dsbuf_rowmax : // unsigned , default = 96
23:16	R/W	128	dsbuf_colmax : // unsigned , default = 128
15: 8	R.O	128	dsbuf_orow : // unsigned , default = 128
7: 0	R/W	128	dsbuf_ocol : // unsigned , default = 128

Table 9-817 NR_DS_CTRL 0x3741

Bit(s)	R/W	Default	Description
30	R/W	0	Nr_ds_enable
29:24	R/W	8	reg_h_step : // unsigned , default = 8 rand lut0
21:16	R/W	8	reg_v_step : // unsigned , default = 8 rand lut0
14:12	R/W	4	reg_haa_sel : // unsigned , default = 4
10: 8	R/W	4	reg_vaa_sel : // unsigned , default = 4
6: 4	R/W	1	reg_use_hphase : // unsigned , default = 1
0	R/W	0	reg_yuv_bldmode : // unsigned , default = 0

Table 9-818 NR_DS_OFFSET 0x3742

Bit(s)	R/W	Default	Description
25:16	R/W	0	reg_h_ofst : // signed , default = 0
9: 0	R/W	0	reg_v_ofst : // signed , default = 0

Table 9-819 NR_DS_BLD_COEF 0x3743

Bit(s)	R/W	Default	Description
23:16	R/W	128	reg_yuv_bldcoef2 : // unsigned , default = 128
15: 8	R/W	64	reg_yuv_bldcoef1 : // unsigned , default = 64
7: 0	R/W	64	reg_yuv_bldcoef0 : // unsigned , default = 64

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9.2.3.14 MCDI Registers

Table 9-820 MCDI_HV_SIZEIN 0x2f00

Bit(s)	R/W	Default	Description
31-29	R/W		reserved
28-16	R/W	1024	reg_mcdi_hsize image horizontal size (number of cols) default=1024
15-13	R/W		reserved
12-0	R/W	1024	reg_mcdi_vsize image vertical size (number of rows) default=1024

Table 9-821 MCDI_HV_BLKSIZEIN 0x2f01

Bit(s)	R/W	Default	Description
31	R/W	0	reg_mcdi_vrev default = 0
30	R/W	0	reg_mcdi_hrev default = 0
29-28	R/W		reserved
27-16	R/W	1024	reg_mcdi_blkhsize image horizontal blk size (number of cols) default=1024
15-13	R/W		reserved
11-0	R/W	1024	reg_mcdi_blkvsize image vertical blk size (number of rows) default=1024

Table 9-822 MCDI_BLKTOTAL 0x2f02

Bit(s)	R/W	Default	Description
31-24	R/W		reserved
23-0	R/W	0	reg_mcdi_blktotal

Table 9-823 MCDI_MOTINEN 0x2f03

Bit(s)	R/W	Default	Description
31-2	R/W		reserved
1	R/W	1	reg_mcdi_motionrefen. enable motion refinement of MA, default = 1
0	R/W	1	reg_mcdi_motionparadoxen. enable motion paradox detection, default = 1

Table 9-824 MCDI_CTRL_MODE 0x2f04

Bit(s)	R/W	Default	Description
31-29	R/W		reserved
28	R/W	0	mc info read enable
27-26	R/W	2	reg_mcdi_lmvlocken 0:disable, 1: use max Lmv, 2: use no-zero Lmv, lmv lock enable mode, default = 2
25	R/W	1	reg_mcdi_reldetrptchken 0-unable; 1: enableenable repeat pattern check (not repeat mv detection) in rel det part, default = 1

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Bit(s)	R/W	Default	Description
24	R/W	1	reg_mcdi_reldetgmvpd22chken 0-unable; 1: enable enable pull-down 22 mode check in gmv lock mode for rel det, default = 1
23	R/W	1	reg_mcdi_pd22chken 0-unable; 1: enable enable pull-down 22 mode check (lock) function, default = 1
22	R/W	1	reg_mcdi_reldetlpfen 0-unable; 1: enable enable det value lpf, default = 1
21	R/W	1	reg_mcdi_reldetlmvpd22chken 0-unable; 1: enable enable pull-down 22 mode check in lmv lock mode for rel det, default = 1
20	R/W	1	reg_mcdi_reldetlmvdifchken 0-unable; 1: enable enable lmv dif check in lmv lock mode for rel det, default = 1
19	R/W	1	reg_mcdi_reldetgmvdifchken 0-unable; 1: enable enable lmv dif check in lmv lock mode for rel det, default = 1
18	R/W	1	reg_mcdi_reldetpd22chken 0-unable; 1: enable enable pull-down 22 mode check for rel det refinement, default = 1
17	R/W	1	reg_mcdi_reldetfrqchken 0-unable; 1: enable enable mv frequency check in rel det, default = 1
16	R/W		reg_mcdi_qmeen 0-unable; 1: enable enable quarter motion estimation, defautl = 1
15	R/W	1	reg_mcdi_refrptmven 0-unable; 1: enable use repeat mv in refinement, default = 1
14	R/W	1	reg_mcdi_refgmven 0-unable; 1: enable use gmv in refinement, default = 1
13	R/W	1	reg_mcdi_reflmven 0-unable; 1: enable use lmvs in refinement, default = 1
12	R/W	1	reg_mcdi_refnmven 0-unable; 1: enable use neighoring mvs in refinement, default = 1
11	R/W		reserved
10	R/W	1	reg_mcdi_referrfrqchken 0-unable; 1: enable enable mv frquency check while finding min err in ref, default = 1
9	R/W	1	reg_mcdi_refen 0-unable; 1: enable enable mv refinement, default = 1
8	R/W	1	reg_mcdi_horlineen 0-unable; 1: enable enable horizontal lines detection by sad map, default = 1
7	R/W	1	reg_mcdi_highvertfrqdeten 0-unable; 1: enable enable high vertical frequency pattern detection, default = 1
6	R/W	1	reg_mcdi_gmvlocken 0-unable; 1: enable enable gmv lock mode, default = 1
5	R/W	1	reg_mcdi_rptmven 0-unable; 1: enable enable repeat pattern detection, default = 1
4	R/W	1	reg_mcdi_gmven 0-unable; 1: enable enable global motion estimation, default = 1
3	R/W	1	reg_mcdi_lmven0-unable; 1: enable enable line mv estimation for hme, default = 1
2	R/W	1	reg_mcdi_chkedgeen0-unable; 1: enable enable check edge function, default = 1
1	R/W	1	reg_mcdi_txtdeten 0-unable; 1: enable enable texture detection, default = 1

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Table 9-825 MCDI_UNI_MVDST 0x2f05

Bit(s)	R/W	Default	Description
31-20	R/W		reserved
19-17	R/W	1	reg_mcdi_unimvdstabsseg0 segment0 for uni-mv abs, default = 1
16-12	R/W	15	reg_mcdi_unimvdstabsseg1 segment1 for uni-mv abs, default = 15
11-8	R/W	2	reg_mcdi_unimvdstabsdifgain0 2/2, gain0 of uni-mv abs dif for segment0, normalized 2 to '1', default = 2
7-5	R/W	2	reg_mcdi_unimvdstabsdifgain1 2/2, gain1 of uni-mv abs dif for segment1, normalized 2 to '1', default = 2
4-2	R/W	2	reg_mcdi_unimvdstabsdifgain2 2/2, gain2 of uni-mv abs dif beyond segment1, normalized 2 to '1', default = 2
1-0	R/W	0	reg_mcdi_unimvdstsgnshft shift for neighboring distance of uni-mv, default = 0

Table 9-826 MCDI_BI_MVDST 0x2f06

Bit(s)	R/W	Default	Description
31-20	R/W		reserved
19-17	R/W	1	reg_mcdi_bimvdstabsseg0 segment0 for bi-mv abs, default = 1
16-12	R/W	9	reg_mcdi_bimvdstabsseg1 segment1 for bi-mv abs, default = 9
11-8	R/W	6	reg_mcdi_bimvdstabsdifgain0 6/2, gain0 of bi-mv abs dif for segment0, normalized 2 to '1', default = 6
7-5	R/W	3	reg_mcdi_bimvdstabsdifgain1 3/2, gain1 of bi-mvabs dif for segment1, normalized 2 to '1', default = 3
4-2	R/W	2	reg_mcdi_bimvdstabsdifgain2 2/2, gain2 of bi-mvabs dif beyond segment1, normalized 2 to '1', default = 2
1-0	R/W	0	reg_mcdi_bimvdstsgnshft shift for neighboring distance of bi-mv, default = 0

Table 9-827 MCDI_SAD_GAIN 0x2f07

Bit(s)	R/W	Default	Description
31-19	R/W		reserved
18-17	R/W	3	reg_mcdi_unisadcorepxlgain uni-sad core pixels gain, default = 3
16	R/W	0	reg_mcdi_unisadcorepxlnormen enable uni-sad core pixels normalization, default = 0
15-11	R/W		reserved
10-9	R/W	3	reg_mcdi_bisadcorepxlgain bi-sad core pixels gain, default = 3
8	R/W	1	reg_mcdi_bisadcorepxlnormen enable bi-sad core pixels normalization, default = 1
7-3	R/W		reserved
2-1	R/W	3	reg_mcdi_biqsadcorepxlgain bi-qsad core pixels gain, default = 3
0	R/W	1	reg_mcdi_biqsadcorepxlnormen enable bi-qsad core pixels normalization, default = 1

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Table 9-828 MCDI_TXT_THD 0x2f08

Bit(s)	R/W	Default	Description
31-24	R/W		reserved
23-16	R/W	24	reg_mcdi_txtminmaxdifthd, min max dif threshold (>=) for texture detection, default = 24
15-8	R/W	9	reg_mcdi_txtmeandifthd, mean dif threshold (<) for texture detection, default = 9
7-3	R/W		reserved
2-0	R/W	2	reg_mcdi_txtdetthd, texture detecting threshold, 0~4, default = 2

Table 9-829 MCDI_FLT_MODESEL 0x2f09

Bit(s)	R/W	Default	Description
31	R/W		reserved
30-28	R/W	1	reg_mcdi_flthorlineselmode mode for horizontal line detecting flat calculation, default = 1, same as below
27	R/W		reserved
26-24	R/W	4	reg_mcdi_fltgmvselmode mode for gmv flat calculation, default = 4, same as below
23	R/W		reserved
22-20	R/W	2	reg_mcdi_fltsadselmode mode for sad flat calculation, default = 2, same as below
19	R/W		reserved
18-16	R/W	3	reg_mcdi_fltbadwselmode mode for badw flat calculation, default = 3, same as below
15	R/W		reserved
14-12	R/W	4	reg_mcdi_fltrptmvselmode mode for repeat mv flat calculation, default = 4, same as below
11	R/W		reserved
10-8	R/W	4	reg_mcdi_fltbadrelselmode mode for bad rel flat calculation, default = 4, same as below
7	R/W		reserved
6-4	R/W	2	reg_mcdi_fltcolcfdselmode mode for col cfd flat calculation, default = 2, same as below
3	R/W		reserved
2-0	R/W	2	reg_mcdi_fltpd22chkselmode mode for pd22 check flat calculation, default = 2, 0:cur dif h, 1: cur dif v, 2: pre dif h, 3: pre dif v, 4: cur flt, 5: pre flt, 6: cur+pre, 7: max all(cur,pre)

Table 9-830 MCDI_CHK_EDGE_THD 0x2f0a

Bit(s)	R/W	Default	Description
23-28	R/W		reserved.
27-24	R/W	1	reg_mcdi_chkedgedifsadthd. thd (<=) for sad dif check, 0~8, default = 1
23-16	R/W		reserved.

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Bit(s)	R/W	Default	Description
15-12	R/W	15	reg_mcdi_chkedgemaxedgethd. max drt of edge, default = 15
11-8	R/W	2	reg_mcdi_chkedgeminedgethd. min drt of edge, default = 2
7	R/W		reserved.
6-0	R/W	14	reg_mcdi_chkedgevdifthd. thd for vertical dif in check edge, default = 14

Table 9-831 MCDI_CHK_EDGE_GAIN_OFFST 0x2f0b

Bit(s)	R/W	Default	Description
31-24	R/W		reserved.
23-20	R/W	4	reg_mcdi_chkedgedifthd1. thd1 for edge dif check (<=), default = 4
19-16	R/W	15	reg_mcdi_chkedgedifthd0. thd0 for edge dif check (>=), default = 15
-15	R/W		reserved.
14-10	R/W	24	reg_mcdi_chkedgechklen. total check length for edge check, 1~24 (>0), default = 24
9-8	R/W	1	reg_mcdi_chkedgeedgesel. final edge select mode, 0: original start edge, 1: lpf start edge, 2: orignal start+end edge, 3: lpf start+end edge, default = 1
7-3	R/W	4	reg_mcdi_chkedgesaddstgain. distance gain for sad calc while getting edges, default = 4
2	R/W		reg_mcdi_chkedgechkmode. edge used in check mode, 0- original edge, 1: lpf edge, defautl = 1
1	R/W		reg_mcdi_chkedgestartedge. edge mode for start edge, 0- original edge, 1: lpf edge, defautl = 0
0	R/W	0	reg_mcdi_chkedgeedgelpf. edge lpf mode, 0-[0,2,4,2,0], 1:[1,2,2,2,1], default = 0

Table 9-832 MCDI_LMV_RT0x2f0c

Bit(s)	R/W	Default	Description
31-24	R/W	32	Reg_mcdi_lmv_vx_gain
14-12	R/W		reg_mcdi_lmvvalidmode valid mode for lmv calc., 100b: use char det, 010b: use flt, 001b: use hori flg
11-10	R/W	1	reg_mcdi_lmvgainmvmode four modes of mv selection for lmv weight caluclua-tion, default = 1
// // lst(x-1	R/W		x,x+1); 1- cur(x-4,x-3), lst(x,x+1); 2: cur(x-5,x-4,x-3), lst(x-1,x,x+1,x+2,x+3); 3: cur(x-6,x-5,x-4,x-3), lst(x-1,x,x+1,x+2);
9	R/W	0	reg_mcdi_lmvinitmode initial lmvs at first row of input field, 0- intial value = 0; 1: inital = 32 (invalid), default = 0
8	R/W		reserved
7-4	R/W	5	reg_mcdi_lmvrt0 ratio of max mv, default = 5
3-0	R/W	5	reg_mcdi_lmvrt1 ratio of second max mv, default = 5

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Table 9-833 MCDI_LMV_GAINTHD 0x2f0d

Bit(s)	R/W	Default	Description
31-24	R/W	96	reg_mcdi_lmvvxmaxgain max gain of lmv weight, default = 96
23	R/W		reserved
22-20	R/W	1	reg_mcdi_lmvdifthd0 dif threshold 0 (<) for small lmv, default = 1
19-17	R/W	2	reg_mcdi_lmvdifthd1 dif threshold 1 (<) for median lmv, default = 2
16-14	R/W	3	reg_mcdi_lmvdifthd2 dif threshold 2 (<) for large lmv, default = 3
13-8	R/W	20	reg_mcdi_lmvnumlmt least/limit number of (total number - max0), default = 20
7-0	R/W	9	reg_mcdi_lmvfltthd flt cnt thd (<) for lmv, default = 9

Table 9-834 MCDI_RPTMV_THD0 0x2f0e

Bit(s)	R/W	Default	Description
31-25	R/W	64	reg_mcdi_rptmvslpthd2 slope thd (>=) between i and i+3/i-3 (i+4/i-4), default = 64
24-20	R/W	4	reg_mcdi_rptmvslpthd1 slope thd (>=) between i and i+2/i-2, default = 4
19-10	R/W	300	reg_mcdi_rptmvampthd2 amplitude thd (>=) between max and min, when count cycles, default = 300
9-0	R/W	400	reg_mcdi_rptmvampthd1 amplitude thd (>=) between average of max and min, default = 400

Table 9-835 MCDI_RPTMV_THD1 0x2f0f

Bit(s)	R/W	Default	Description
31-28	R/W		reserved
27-25	R/W	2	reg_mcdi_rptmvcyccntthd thd (>=) of total cycles count, default = 2
24-21	R/W	3	reg_mcdi_rptmvcycdifthd dif thd (<) of cycles length, default = 3
20-18	R/W	1	reg_mcdi_rptmvcycvldthd thd (>) of valid cycles number, default = 1
17-15	R/W	2	reg_mcdi_rptmvhalfcycminthd min length thd (>=) of half cycle, default = 2
14-11	R/W	5	reg_mcdi_rptmvhalfcycdifthd neighboring half cycle length dif thd (<), default = 5
10-8	R/W	2	reg_mcdi_rptmvminmaxcntthd least number of valid max and min, default = 2
7-5	R/W	2	reg_mcdi_rptmvcycminthd min length thd (>=) of cycles, default = 2
4-0	R/W	17	reg_mcdi_rptmvcycmaxthd max length thd (<) of cycles, default = 17

Table 9-836 MCDI_RPTMV_THD2 0x2f10

Bit(s)	R/W	Default	Description
31-24	R/W		reserved
23-16	R/W	8	reg_mcdi_rptmvhdifthd0 higher hdif thd (>=) (vertical edge) for rpt detection, default = 8

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Bit(s)	R/W	Default	Description
15-8	R/W	4	reg_mcdi_rptmvhdifthd1 hdif thd (>=) (slope edge) for rpt detection, default = 4
7-0	R/W	1	reg_mcdi_rptmvvdifthd vdif thd (>=) (slope edge) for rpt detection, default = 1

Table 9-837 MCDI_RPTMV_SAD 0x2f11

Bit(s)	R/W	Default	Description
31-26	R/W		reserved
25-16	R/W	336	reg_mcdi_rptmvsaddifthdgain 7x3x(16/16), gain for sad dif thd in rpt mv detection, 0~672, normalized 16 as '1', default = 336
15-10	R/W		reserved
9-0	R/W	16	reg_mcdi_rptmvsaddifthdoffst offset for sad dif thd in rpt mv detection, -512~511, default = 16

Table 9-838 MCDI_RPTMV_FLG 0x2f12

Bit(s)	R/W	Default	Description
31-18	R/W		reserved
17-16	R/W	2	reg_mcdi_rptmvmode select mode of mvs for repeat motion estimation, 0: hmv, 1: qmv/2, 2 or 3: qmv/4, default = 2
15-8	R/W	64	reg_mcdi_rptmvflgcntthd thd (>=) of min count number for rptmv of whole field, for rptmv estimation, default = 64
7-5	R/W		reserved
4-0	R/W		reg_mcdi_rptmvflgcntrt 4/32, ratio for repeat mv flag count, normalized 32 as '1', set 31 to 32,

Table 9-839 MCDI_RPTMV_GAIN 0x2f13

Bit(s)	R/W	Default	Description
31-24	R/W	96	reg_mcdi_rptmvlftgain up repeat mv gain for hme, default = 96
23-16	R/W	32	reg_mcdi_rptmvuplftgain up left repeat mv gain for hme, default = 32
15-8	R/W	64	reg_mcdi_rptmvupgain up repeat mv gain for hme, default = 64
7-0	R/W	32	reg_mcdi_rptmvuprightgain up right repeat mv gain for hme, default = 32

Table 9-840 MCDI_GMV_RT0x2f14

Bit(s)	R/W	Default	Description
31	R/W		reserved
30-24	R/W	32	reg_mcdi_gmvmtnrt0 ratio 0 for motion senario, set 127 to 128, normalized 128 as '1', default =32
23	R/W		reserved
22-16	R/W	56	reg_mcdi_gmvmtnrt1 ratio 1 for motion senario, set 127 to 128, normalized 128 as '1', default = 56

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Bit(s)	R/W	Default	Description
15	R/W		reserved
14-8	R/W	56	reg_mcdi_gmvstlrt0 ratio 0 for still senario, set 127 to 128, normalized 128 as '1', default = 56
7	R/W		reserved
6-0	R/W	80	reg_mcdi_gmvstlrt1 ratio 1 for still senario, set 127 to 128, normalized 128 as '1', default = 80

Table 9-841 MCDI_GMV_GAIN 0x2f15

Bit(s)	R/W	Default	Description
31-25	R/W	100	reg_mcdi_gmvzeromvlockrt0 ratio 0 for locking zero mv, set 127 to 128, normalized 128 as '1', default = 100
24-18	R/W	112	reg_mcdi_gmvzeromvlockrt1 ratio 1 for locking zero mv, set 127 to 128, normalized 128 as '1', default = 112
17-16	R/W	3	reg_mcdi_gmvvalidmode valid mode for gmv calc., 10b: use flt, 01b: use hori flg, default = 3
15-8	R/W	0	reg_mcdi_gmvvxgain gmv's vx gain when gmv locked for hme, default = 0
7-0	R/W	3	reg_mcdi_gmvfltthd flat thd (<) for gmv calc. default = 3

Table 9-842 MCDI_HOR_SADOFST 0x2f16

Bit(s)	R/W	Default	Description
31-25	R/W		reserved
24-16	R/W	21	reg_mcdi_horsaddifthdgain 21*1/8, gain/divisor for sad dif threshold in hor line detection, normalized 8 as '1', default = 21
15-8	R/W	0	reg_mcdi_horsaddifthdoffst offset for sad dif threshold in hor line detection, -128~127, default = 0
7-0	R/W	24	reg_mcdi_horvdifthd threshold (>=) of vertical dif of next block for horizontal line detection, default = 24

Table 9-843 MCDI_REF_MV_NUM 0x2f17

Bit(s)	R/W	Default	Description
31-2	R/W		reserved
1-0	R/W	0	reg_mcdi_refmcmode. motion compensated mode used in refinement, 0: pre, 1: next, 2: (pre+next)/2, default = 0

Table 9-844 MCDI_REF_BADW_THD_GAIN0x2f18

Bit(s)	R/W	Default	Description
31-28	R/W		reserved
27-24	R/W	6	reg_mcdi_refbadwcnt2gain. gain for badwv count num==3, default = 6
23-20	R/W	3	reg_mcdi_refbadwcnt1gain. gain for badwv count num==2, default = 3
19-16	R/W	1	reg_mcdi_refbadwcnt0gain. gain for badwv count num==1, default = 1

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Bit(s)	R/W	Default	Description
15-12	R/W	4	reg_mcdi_refbadwthd3. threshold 3 for detect badweave with largest average luma, default = 4
11-8	R/W	3	reg_mcdi_refbadwthd2. threshold 2 for detect badweave with third smallest average luma, default = 3
7-4	R/W	2	reg_mcdi_refbadwthd1. threshold 1 for detect badweave with second smallest average luma, default = 2
3-0	R/W	1	reg_mcdi_refbadwthd0. threshold 0 for detect badweave with smallest average luma, default = 1

Table 9-845 MCDI_REF_BADW_SUM_GAIN0x2f19

Bit(s)	R/W	Default	Description
31-13	R/W		reserved
12-8	R/W	8	reg_mcdi_refbadwsumgain0. sum gain for r channel, 0~16, default = 8
7-5	R/W		reserved
4	R/W	0	reg_mcdi_refbadwcalcmode. mode for badw calculation, 0-sum, 1:max, default = 0
3-0	R/W		reserved

Table 9-846 MCDI_REF_BS_THD_GAIN 0x2f1a

Bit(s)	R/W	Default	Description
31-28	R/W	2	reg_mcdi_refbsudgain1. up & down block stregth gain1, normalized to 8 as '1', default = 2
27-24	R/W	4	reg_mcdi_refbsudgain0. up & down block stregth gain0, normalized to 8 as '1', default = 4
23-19	R/W		reserved
18-16	R/W	0	reg_mcdi_refbslftgain. left block strength gain, default = 0
15-13	R/W		reserved
12-8	R/W	16	reg_mcdi_refbsthd1. threshold 1 for detect block stregth in refinment, default = 16
7-5	R/W		reserved
4-0	R/W	8	reg_mcdi_refbsthd0. threshold 0 for detect block stregth in refinment, default = 8

Table 9-847 MCDI_REF_ERR_GAIN0 0x2f1b

Bit(s)	R/W	Default	Description
31	R/W		reserved
30-24	R/W	48	reg_mcdi_referrnbrdstgain. neighoring mv distances gain for err calc. in ref, normalized to 8 as '1', default = 48
23-20	R/W		reserved
19-16	R/W	4	reg_mcdi_referrbsgain. bs gain for err calc. in ref, normalized to 8 as '1', default = 4

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Bit(s)	R/W	Default	Description
15	R/W		reserved
14-8	R/W	64	reg_mcdi_referrbadwgain. badw gain for err calc. in ref, normalized to 8 as '1', default = 64
7-4	R/W		reserved
3-0	R/W	4	reg_mcdi_referrsadgain. sad gain for err calc. in ref, normalized to 8 as '1', default = 4

Table 9-848 MCDI_REF_ERR_GAIN1 0x2f1c

Bit(s)	R/W	Default	Description
31-20	R/W		reserved
19-16	R/W	4	reg_mcdi_referrchkedgegain. check edge gain for err calc. in ref, normalized to 8 as '1', default = 4
15-12	R/W		reserved
11-8	R/W	0	reg_mcdi_referrlmvgain. (locked) lmv gain for err calc. in ref, normalized to 8 as '1', default = 0
7-4	R/W		reserved
3-0	R/W	0	reg_mcdi_referrgmvgain. (locked) gmv gain for err calc. in ref, normalized to 8 as '1', default = 0

Table 9-849 MCDI_REF_ERR_FRQ_CHK 0x2f1d

Bit(s)	R/W	Default	Description
31-28	R/W		reserved
27-24	R/W	10	reg_mcdi_referrfrqgain. gain for mv frquency, normalized to 4 as '1', default = 10
23-21	R/W		reserved
20-16	R/W	31	reg_mcdi_referrfrqmax. max gain for mv frquency check, default = 31
15	R/W		reserved
14-12	R/W	3	reg_mcdi_ref_errfrqmvdifthd2. mv dif threshold 2 (<) for mv frquency check, default = 3
11	R/W		reserved
10-8	R/W	2	reg_mcdi_ref_errfrqmvdifthd1. mv dif threshold 1 (<) for mv frquency check, default = 2
7	R/W		reserved
6-4	R/W	1	reg_mcdi_ref_errfrqmvdifthd0. mv dif threshold 0 (<) for mv frquency check, default = 1
3-0	R/W		reserved

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Table 9-850 MCDI_QME_LPF_MSK 0x2f1e

Bit(s)	R/W	Default	Description
31-28	R/W		reserved
27-24	R/W	7	reg_mcdi_qmechkedgelpfmsk0. lpf mask0 for chk edge in qme, 0~8, msk1 = (8-msk0), normalized to 8 as '1', default = 7
23-20	R/W		reserved
19-16	R/W	7	reg_mcdi_qmebslpfmsk0. lpf mask0 for bs in qme, 0~8, msk1 = (8-msk0), normalized to 8 as '1', default = 7
15-12	R/W		reserved
11-8	R/W	7	reg_mcdi_qmebadwlpfmsk0. lpf mask0 for badw in qme, 0~8, msk1 = (8-msk0), normalized to 8 as '1', default = 7
7-4	R/W		reserved
3-0	R/W	7	reg_mcdi_qmesadlpfmsk0. lpf mask0 for sad in qme, 0~8, msk1 = (8-msk0), normalized to 8 as '1', default = 7

Table 9-851 MCDI_REL_DIF_THD_02 0x2f1f

Bit(s)	R/W	Default	Description
31-24	R/W		reserved.
23-16	R/W	9	reg_mcdi_reldifthd2. thd (<) for (hdif+vdif), default = 9
15-8	R/W	5	reg_mcdi_reldifthd1. thd (<) for (vdif), default = 5
7-0	R/W	48	reg_mcdi_reldifthd0. thd (>=) for (hdif-vdif), default = 48

Table 9-852 MCDI_REL_DIF_THD_34 0x2f20

Bit(s)	R/W	Default	Description
31-16	R/W		reserved.
15-8	R/W	255	reg_mcdi_reldifthd4. thd (<) for (hdif), default = 255
7-0	R/W	48	reg_mcdi_reldifthd3. thd (>=) for (vdif-hdif), default = 48

Table 9-853 MCDI_REL_BADW_GAIN_OFFST_01 0x2f21

Bit(s)	R/W	Default	Description
31-24	R/W	0	reg_mcdi_relbadwoffst1. offset for badw adj, for flat block, -128~127, default = 0
23-16	R/W	128	reg_mcdi_relbadwgain1. gain for badw adj, for flat block, default = 128
15-8	R/W	0	reg_mcdi_relbadwoffst0. offset for badw adj, for vertical block, -128~127, default = 0
7-0	R/W	160	reg_mcdi_relbadwgain0. gain for badw adj, for vertical block, default = 160

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Table 9-854 MCDI_REL_BADW_GAIN_OFFST_23 0x2f22

Bit(s)	R/W	Default	Description
31-24	R/W	0	reg_mcdi_relbadwoffst3. offset for badw adj, for other block, -128~127, default = 0
23-16	R/W	48	reg_mcdi_relbadwgain3. gain for badw adj, for other block, default = 48
15-8	R/W	0	reg_mcdi_relbadwoffst2. offset for badw adj, for horizontal block, -128~127, default = 0
7-0	R/W	48	reg_mcdi_relbadwgain2. gain for badw adj, for horizontal block, default = 48

Table 9-855 MCDI_REL_BADW_THD_GAIN_OFFST 0x2f23

Bit(s)	R/W	Default	Description
31-23	R/W		reserved.
22-16	R/W	0	reg_mcdi_relbadwoffst. offset for badw thd adj, -64~63, default = 0
15-8	R/W		reserved.
7-0	R/W	16	reg_mcdi_relbadwthdgain. gain0 for badw thd adj, normalized to 16 as '1', default = 16

Table 9-856 MCDI_REL_BADW_THD_MIN_MAX 0x2f24

Bit(s)	R/W	Default	Description
31-18	R/W		reserved.
17-8	R/W	256	reg_mcdi_relbadwthdmax. max for badw thd adj, default = 256
7-0	R/W	16	reg_mcdi_relbadwthdmin. min for badw thd adj, default = 16

Table 9-857 MCDI_REL_SAD_GAIN_OFFST_01 0x2f25

Bit(s)	R/W	Default	Description
31-24	R/W	0	reg_mcdi_relsadoffst1. offset for sad adj, for flat block, -128~127, default = 0
23-20	R/W		reserved.
19-16	R/W	8	reg_mcdi_relsadgain1. gain for sad adj, for flat block, normalized to 8 as '1', default = 8
15-8	R/W	0	reg_mcdi_relsadoffst0. offset for sad adj, for vertical block, -128~127, default = 0
7-4	R/W		reserved.
3-0	R/W	6	reg_mcdi_relsadgain0. gain for sad adj, for vertical block, normalized to 8 as '1', default = 6

Table 9-858 MCDI_REL_SAD_GAIN_OFFST_23 0x2f26

Bit(s)	R/W	Default	Description
31-24	R/W	0	reg_mcdi_relsadoffst3. offset for sad adj, for other block, -128~127, default = 0
23-20	R/W		reserved.

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Bit(s)	R/W	Default	Description
19-16	R/W	8	reg_mcdi_relsadgain3. gain for sad adj, for other block, normalized to 8 as '1', default = 8
15-8	R/W	0	reg_mcdi_relsadoffst2. offset for sad adj, for horizontal block, -128~127, default = 0
7-4	R/W		reserved.
3-0	R/W	12	reg_mcdi_relsadgain2. gain for sad adj, for horizontal block, normalized to 8 as '1', default = 12

Table 9-859 MCDI_REL_SAD_THD_GAIN_OFFST 0x2f27

Bit(s)	R/W	Default	Description
31-24	R/W		reserved.
23-16	R/W	0	reg_mcdi_relsadoffst. offset for sad thd adj, -128~127, default = 0
15-10	R/W		reserved.
9-0	R/W	42	reg_mcdi_relsadthdgain. gain for sad thd adj, 21*2/16, normalized to 16 as '1', default = 42

Table 9-860 MCDI_REL_SAD_THD_MIN_MAX 0x2f28

Bit(s)	R/W	Default	Description
31-27	R/W		reserved.
26-16	R/W	672	reg_mcdi_relsadthdmax. max for sad thd adj, 21*32, default = 672
15-9	R/W		reserved.
8-0	R/W	42	reg_mcdi_relsadthdmin. min for sad thd adj, 21*2, default = 42

Table 9-861 MCDI_REL_DET_GAIN_00 0x2f29

Bit(s)	R/W	Default	Description
31-21	R/W		reserved.
20-16	R/W	8	reg_mcdi_reldetbsgain0. gain0 (gmv locked) for bs, for det. calc. normalized to 16 as '1', default = 8
15-14	R/W		reserved.
13-8	R/W	12	reg_mcdi_reldetbadwgain0. gain0 (gmv locked) for badw, for det. calc. normalized to 16 as '1', default = 12
7-5	R/W		reserved.
4-0	R/W	8	reg_mcdi_reldetsadgain0. gain0 (gmv locked) for qsad, for det. calc. normalized to 16 as '1', default = 8

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Table 9-862 MCDI_REL_DET_GAIN_01 0x2f2a

Bit(s)	R/W	Default	Description
31-14	R/W		reserved.
12-8	R/W	2	reg_mcdi_reldetchkedgegain0. gain0 (gmv locked) for chk_edge, for det. calc. normalized to 16 as '1', default = 2
7	R/W		reserved.
6-0	R/W	24	reg_mcdi_reldetnbrdstgain0. gain0 (gmv locked) for neighoring dist, for det. calc. normalized to 16 as '1', default = 24

Table 9-863 MCDI_REL_DET_GAIN_10 0x2f2b

Bit(s)	R/W	Default	Description
31-21	R/W		reserved.
20-16	R/W	0	reg_mcdi_reldetbsgain1. gain1 (lmv locked) for bs, for det. calc. normalized to 16 as '1', default = 0
15-14	R/W		reserved.
13-8	R/W	8	reg_mcdi_reldetbadwgain1. gain1 (lmv locked) for badw, for det. calc. normalized to 16 as '1', default = 8
7-5	R/W		reserved.
4-0	R/W	8	reg_mcdi_reldetsadgain1. gain1 (lmv locked) for qsad, for det. calc. normalized to 16 as '1', default = 8

Table 9-864 MCDI_REL_DET_GAIN_11 0x2f2c

Bit(s)	R/W	Default	Description
31-14	R/W		reserved.
12-8	R/W	0	reg_mcdi_reldetchkedgegain1. gain1 (lmv locked) for chk_edge, for det. calc. normalized to 16 as '1', default = 0
7	R/W		reserved.
6-0	R/W	24	reg_mcdi_reldetnbrdstgain1. gain1 (lmv locked) for neighoring dist, for det. calc. normalized to 16 as '1', default = 24

Table 9-865 MCDI_REL_DET_GAIN_20 0x2f2d

Bit(s)	R/W	Default	Description
31-21	R/W		reserved.
20-16	R/W	12	reg_mcdi_reldetbsgain2. gain2 (no locked) for bs, for det. calc. normalized to 16 as '1', default = 12
15-14	R/W		reserved.
13-8	R/W	32	reg_mcdi_reldetbadwgain2. gain2 (no locked) for badw, for det. calc. normalized to 16 as '1', default = 32
7-5	R/W		reserved.
4-0	R/W	16	reg_mcdi_reldetsadgain2. gain2 (no locked) for qsad, for det. calc. normalized to 16 as '1', default = 16

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Table 9-866 MCDI_REL_DET_GAIN_21 0x2f2e

Bit(s)	R/W	Default	Description
31-26	R/W		reserved
25-16	R/W	0	reg_mcdi_reldetoffst. offset for rel calculation, for det. calc. -512~511, default = 0
15-14	R/W		reserved.
12-8	R/W	10	reg_mcdi_reldetchkedgegain2. gain2 (no locked) for chk_edge, for det. calc. normalized to 16 as '1', default = 10
7	R/W		reserved.
6-0	R/W	32	reg_mcdi_reldetnbrdstgain2. gain2 (no locked) for neighoring dist, for det. calc. normalized to 16 as '1', default = 32

Table 9-867 MCDI_REL_DET_GMV_DIF_CHK 0x2f2f

Bit(s)	R/W	Default	Description
31-24	R/W		reserved.
23-16	R/W	0	reg_mcdi_reldetgmvfltthd. flat thd (>=) for gmv lock decision, default = 0
15	R/W		reserved.
14-12	R/W	3	reg_mcdi_reldetgmvdifthd. dif thd (>=) for current mv different from gmv for gmv dif check, actually used in Lmv lock check, default = 3
11	R/W		reserved.
10-8	R/W	1	reg_mcdi_reldetgmvdifmin. min mv dif for gmv dif check, default = 1, note: dif between reg_mcdi_rel_det_gmv_dif_max and reg_mcdi_rel_det_gmv_dif_min should be; 0,1,3,7, not work for others
7-4	R/W	4	reg_mcdi_reldetgmvdifmax. max mv dif for gmv dif check, default = 4
3-1	R/W		reserved
0	R/W	0	reg_mcdi_reldetgmvdifmvmode. mv mode used for gmv dif check, 0- use refmv, 1: use qmv, default = 0

Table 9-868 MCDI_REL_DET_LMV_DIF_CHK 0x2f30

Bit(s)	R/W	Default	Description
31-24	R/W		reserved.
23-16	R/W	12	reg_mcdi_reldetlmvfltthd. flat thd (>=) for lmv lock decision, default = 12
15-14	R/W		reserved.
13-12	R/W	1	reg_mcdi_reldetlmvlockchkmode. lmv lock check mode, 0:cur Lmv, 1: cur & (last | next), 2: last & cur & next Lmv, default = 1
11	R/W		reserved.
10-8	R/W	1	reg_mcdi_reldetlmvdifmin. min mv dif for lmv dif check, default = 1, note: dif between reg_mcdi_rel_det_lmv_dif_max and reg_mcdi_rel_det_lmv_dif_min should be; 0,1,3,7, not work for others
7-4	R/W	4	reg_mcdi_reldetlmvdifmax. max mv dif for lmv dif check, default = 4

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Bit(s)	R/W	Default	Description
3-1	R/W		reserved
0	R/W	0	reg_mcdi_reldetlmvdifmvmode. mv mode used for lmv dif check, 0- use refmv, 1: use qmv, default = 0

Table 9-869 MCDI_REL_DET_FRQ_CHK 0x2f31

Bit(s)	R/W	Default	Description
31-12	R/W		reserved.
11-8	R/W	10	reg_mcdi_reldetfrqgain. gain for frequency check, normalized to 4 as '1', default = 10
7-5	R/W		reserved
4-0	R/W	31	reg_mcdi_reldetfrqmax. max value for frequency check, default = 31

Table 9-870 MCDI_REL_DET_PD22_CHK 0x2f32

Bit(s)	R/W	Default	Description
31-18	R/W		reserved.
30-21	R/W	512	reg_mcdi_reldetpd22chkoffst1. offset for pd22 check happened, default = 512
20-16	R/W	12	reg_mcdi_reldetpd22chkgain1. gain for pd22 check happened, normalized to 8 as '1', default = 12
14-5	R/W	512	reg_mcdi_reldetpd22chkoffst0. offset for pd22 check happened, default = 512
4-0	R/W	12	reg_mcdi_reldetpd22chkgain0. gain for pd22 check happened, normalized to 8 as '1', default = 12

Table 9-871 MCDI_REL_DET_RPT_CHK_ROW 0x2f33

Bit(s)	R/W	Default	Description
31-27	R/W		reserved
26-16	R/W	2047	reg_mcdi_reldetrptchkendrow. end row (<) number for repeat check, default = 2047
15-11	R/W		reserved
10-0	R/W	0	reg_mcdi_reldetrptchkstartrow. start row (>=) number for repeat check, default = 0

Table 9-872 MCDI_REL_DET_RPT_CHK_GAIN_QMV 0x2f34

Bit(s)	R/W	Default	Description
31-30	R/W		reserved
29-24	R/W	15	reg_mcdi_reldetrptchkqmvmax. max thd (<) of abs qmv for repeat check, default = 15, note that quarter mv's range is -63~63
23-22	R/W		reserved
21-16	R/W	10	reg_mcdi_reldetrptchkqmvmin. min thd (>=) of abs qmv for repeat check, default = 10, note that quarter mv's range is -63~63

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Bit(s)	R/W	Default	Description
15	R/W		reserved/
14-4	R/W	512	reg_mcdi_reldetrptchkoffst. offset for repeat check, default = 512
3-0	R/W	4	reg_mcdi_reldetrptchkgain. gain for repeat check, normalized to 8 as '1', default = 4

Table 9-873 MCDI_REL_DET_RPT_CHK_THD_0 0x2f35

Bit(s)	R/W	Default	Description
31-24	R/W		reserved
23-16	R/W	255	reg_mcdi_reldetrptchkzerosadthd. zero sad thd (<) for repeat check, default = 255
15-14	R/W		reserved.
13-8	R/W	16	reg_mcdi_reldetrptchkzerobadwthd. zero badw thd (>=) for repeat check, default = 16
7-4	R/W		reserved
3-0	R/W	5	reg_mcdi_reldetrptchkfrqdifthd. frequency dif thd (<) for repeat check, 0~10, default = 5

Table 9-874 MCDI_REL_DET_RPT_CHK_THD_1 0x2f36

Bit(s)	R/W	Default	Description
31-16	R/W		reserved
15-8	R/W	16	reg_mcdi_reldetrptchkvdifthd. vertical dif thd (<) for repeat check, default = 16
7-0	R/W	16	reg_mcdi_reldetrptchkhdifthd. horizontal dif thd (>=) for repeat check, default = 16

Table 9-875 MCDI_REL_DET_LPF_DIF_THD 0x2f37

Bit(s)	R/W	Default	Description
31-24	R/W	9	reg_mcdi_reldetlpfdifthd3. hdif thd (<) for lpf selection of horizontal block, default = 9
23-16	R/W	48	reg_mcdi_reldetlpfdifthd2. vdif-hdif thd (>=) for lpf selection of horizontal block, default = 48
15-8	R/W	9	reg_mcdi_reldetlpfdifthd1. vdif thd (<) for lpf selection of vertical block, default = 9
7-0	R/W	48	reg_mcdi_reldetlpfdifthd0. hdif-vdif thd (>=) for lpf selection of vertical block, default = 48

Table 9-876 MCDI_REL_DET_LPF_MSK_00_03 0x2f38

Bit(s)	R/W	Default	Description
31-29	R/W		reserved
28-24	R/W	1	reg_mcdi_reldetlpfmsk03. det lpf mask03 for gmv/lmv locked mode, 0~16, default = 1

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Bit(s)	R/W	Default	Description
23-21	R/W		reserved
20-16	R/W	1	reg_mcdi_reldetlpfmsk02. det lpf mask02 for gmv/lmv locked mode, 0~16, default = 1
15-13	R/W		reserved
12-8	R/W	5	reg_mcdi_reldetlpfmsk01. det lpf mask01 for gmv/lmv locked mode, 0~16, default = 5
7-5	R/W		reserved
4-0	R/W	8	reg_mcdi_reldetlpfmsk00. det lpf mask00 for gmv/lmv locked mode, 0~16, default = 8

Table 9-877 MCDI_REL_DET_LPF_MSK_04_12 0x2f39

Bit(s)	R/W	Default	Description
31-29	R/W		reserved
28-24	R/W	0	reg_mcdi_reldetlpfmsk12. det lpf mask12 for vertical blocks, 0~16, default = 0
23-21	R/W		reserved
20-16	R/W	0	reg_mcdi_reldetlpfmsk11. det lpf mask11 for vertical blocks, 0~16, default = 0
15-13	R/W		reserved
12-8	R/W	16	reg_mcdi_reldetlpfmsk10. det lpf mask10 for vertical blocks, 0~16, default = 16
7-5	R/W		reserved
4-0	R/W	1	reg_mcdi_reldetlpfmsk04. det lpf mask04 for gmv/lmv locked mode, 0~16, default = 1

Table 9-878 MCDI_REL_DET_LPF_MSK_13_21 0x2f3a

Bit(s)	R/W	Default	Description
31-29	R/W		reserved
28-24	R/W	6	reg_mcdi_reldetlpfmsk21. det lpf mask21 for horizontal blocks, 0~16, default = 6
23-21	R/W		reserved
20-16	R/W	8	reg_mcdi_reldetlpfmsk20. det lpf mask20 for horizontal blocks, 0~16, default = 8
15-13	R/W		reserved
12-8	R/W	0	reg_mcdi_reldetlpfmsk14. det lpf mask14 for vertical blocks, 0~16, default = 0
7-5	R/W		reserved
4-0	R/W	0	reg_mcdi_reldetlpfmsk13. det lpf mask13 for vertical blocks, 0~16, default = 0

Table 9-879 MCDI_REL_DET_LPF_MSK_22_30 0x2f3b

Bit(s)	R/W	Default	Description
31-29	R/W		reserved
28-24	R/W	16	reg_mcdi_reldetlpfmsk30. det lpf mask30 for other blocks, 0~16, default = 16

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Bit(s)	R/W	Default	Description
23-21	R/W		reserved
20-16	R/W	1	reg_mcdi_reldetlpfmsk24. det lpf mask24 for horizontal blocks, 0~16, default = 1
15-13	R/W		reserved
12-8	R/W	0	reg_mcdi_reldetlpfmsk23. det lpf mask23 for horizontal blocks, 0~16, default = 0
7-5	R/W		reserved
4-0	R/W	1	reg_mcdi_reldetlpfmsk22. det lpf mask22 for horizontal blocks, 0~16, default = 1

Table 9-880 MCDI_REL_DET_LPF_MSK_31_34 0x2f3c

Bit(s)	R/W	Default	Description
31-29	R/W		reserved
28-24	R/W	0	reg_mcdi_reldetlpfmsk34. det lpf mask34 for other blocks, 0~16, default = 0
23-21	R/W		reserved
20-16	R/W	0	reg_mcdi_reldetlpfmsk33. det lpf mask33 for other blocks, 0~16, default = 0
15-13	R/W		reserved
12-8	R/W	0	reg_mcdi_reldetlpfmsk32. det lpf mask32 for other blocks, 0~16, default = 0
7-5	R/W		reserved
4-0	R/W	0	reg_mcdi_reldetlpfmsk31. det lpf mask31 for other blocks, 0~16, default = 0

Table 9-881 MCDI_REL_DET_MIN 0x2f3d

Bit(s)	R/W	Default	Description
31-7	R/W		reserved
6-0	R/W	16	reg_mcdi_reldetmin. min of detected value, default = 16

Table 9-882 MCDI_REL_DET_LUT_0_3 0x2f3e

Bit(s)	R/W	Default	Description
31-24	R/W	8	reg_mcdi_reldetmaplut3. default = 8
23-16	R/W	4	reg_mcdi_reldetmaplut2. default = 4
15-8	R/W	2	reg_mcdi_reldetmaplut1. default = 2
7-0	R/W	0	reg_mcdi_reldetmaplut0. default = 0

Table 9-883 MCDI_REL_DET_LUT_4_7 0x2f3f

Bit(s)	R/W	Default	Description
31-24	R/W	64	reg_mcdi_reldetmaplut7. default = 64
23-16	R/W	48	reg_mcdi_reldetmaplut6. default = 48

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Bit(s)	R/W	Default	Description
15-8	R/W	32	reg_mcdi_reldetmaplut5. default = 32
7-0	R/W	16	reg_mcdi_reldetmaplut4. default = 16

Table 9-884 MCDI_REL_DET_LUT_8_11 0x2f40

Bit(s)	R/W	Default	Description
31-24	R/W	160	reg_mcdi_reldetmaplut11. default = 160
23-16	R/W	128	reg_mcdi_reldetmaplut10. default = 128
15-8	R/W	96	reg_mcdi_reldetmaplut9. default = 96
7-0	R/W	80	reg_mcdi_reldetmaplut8. default = 80

Table 9-885 MCDI_REL_DET_LUT_12_150x2f41

Bit(s)	R/W	Default	Description
31-24	R/W	255	reg_mcdi_reldetmaplut15. default = 255
23-16	R/W	240	reg_mcdi_reldetmaplut14. default = 240
15-8	R/W	224	reg_mcdi_reldetmaplut13. default = 224
7-0	R/W	192	reg_mcdi_reldetmaplut12. default = 192

Table 9-886 MCDI_REL_DET_COL_CFD_THD 0x2f42

Bit(s)	R/W	Default	Description
31-24	R/W	5	reg_mcdi_reldetcolcfdfltthd. thd for flat smaller than (<) of column cofidence, default = 5
23-16	R/W	160	reg_mcdi_reldetcolcfdthd1. thd for rel larger than (>=) in rel calc. mode col confidence without gmv locking, default = 160
15-8	R/W	100	reg_mcdi_reldetcolcfdthd0. thd for rel larger than (>=) in rel calc. mode col confidence when gmv locked, default = 100
7-2	R/W	16	reg_mcdi_reldetcolcfdbadwthd. thd for badw larger than (>=) in qbadw calc. mode of column cofidence, default = 16
1	R/W		reserved
0	R/W	0	reg_mcdi_reldetcolcfdcalcmode. calc. mode for column cofidence, 0- use rel, 1: use qbadw, default = 0

Table 9-887 MCDI_REL_DET_COL_CFD_AVG_LUMA 0x2f43

Bit(s)	R/W	Default	Description
31-24	R/W	235	reg_mcdi_reldetcolcfdavgmin1. avg luma min1 (>=) for column cofidence, valid between 16~235, default = 235
23-16	R/W	235	reg_mcdi_reldetcolcfdavgmax1. avg luma max1 (<) for column cofidence, valid between 16~235, default = 235

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Bit(s)	R/W	Default	Description
15-8	R/W	16	reg_mcdi_reldetcolcfdavgmin0. avg luma min0 (>=) for column cofidence, valid between 16~235, default = 16
7-0	R/W	21	reg_mcdi_reldetcolcfdavgmax0. avg luma max0 (<) for column cofidence, valid between 16~235, default = 21

Table 9-888 MCDI_REL_DET_BAD_THD_00x2f44

Bit(s)	R/W	Default	Description
31-16	R/W		reserved
15-8	R/W	120	reg_mcdi_reldetbadsadthd. thd (>=) for bad sad, default = 120 (480/4)
7-6	R/W		reserved
5-0	R/W	12	reg_mcdi_reldetbadbadwthd. thd (>=) for bad badw, 0~42, default = 12

Table 9-889 MCDI_REL_DET_BAD_THD_10x2f45

Bit(s)	R/W	Default	Description
31-24	R/W		reserved
23-16	R/W	4	reg_mcdi_reldetbadrelfltthd. thd (>=) of flat for bad rel detection, default = 4
15-8	R/W	160	reg_mcdi_reldetbadrelthd1. thd (>=) for bad rel without gmv/lmv locked, default = 160
7-0	R/W	120	reg_mcdi_reldetbadrelthd0. thd (>=) for bad rel with gmv/lmv locked, default = 120

Table 9-890 MCDI_PD22_CHK_THD 0x2f46

Bit(s)	R/W	Default	Description
31-25	R/W		reserved
24-16	R/W	64	reg_mcdi_pd22chksaddifthd. sad dif thd (>=) for (pd22chksad - qsad) for pd22 check, default = 64
15-14	R/W		reserved
13-8	R/W	2	reg_mcdi_pd22chkqmvthd. thd (>=) of abs qmv for pd22 check, default = 2
7-0	R/W	4	reg_mcdi_pd22chkfltthd. thd (>=) of flat for pd22 check, default = 4

Table 9-891 MCDI_PD22_CHK_GAIN_OFFST_0 0x2f47

Bit(s)	R/W	Default	Description
31-24	R/W	0	reg_mcdi_pd22chkedgeoffst0. offset0 of pd22chkedge from right film22 phase, -128~127, default = 0
23-21	R/W		reserved
20-16	R/W	16	reg_mcdi_pd22chkedgegain0. gain0 of pd22chkedge from right film22 phase, normalized to 16 as '1', default = 16
15-12	R/W		reserved

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Bit(s)	R/W	Default	Description
11-8	R/W	0	reg_mcdi_pd22chkbadwoffst0. offset0 of pd22chkbadw from right film22 phase, -8~7, default = 0
7-5	R/W		reserved
4-0	R/W	8	reg_mcdi_pd22chkbadwgain0. gain0 of pd22chkbadw from right film22 phase, normalized to 16 as '1', default = 8

Table 9-892 MCDI_PD22_CHK_GAIN_OFFST_1 0x2f48

Bit(s)	R/W	Default	Description
31-24	R/W	0	reg_mcdi_pd22chkedgeoffst1. offset1 of pd22chkedge from right film22 phase, -128~127, default = 0
23-21	R/W		reserved
20-16	R/W	16	reg_mcdi_pd22chkedgegain1. gain1 of pd22chkedge from right film22 phase, normalized to 16 as '1', default = 16
15-12	R/W		reserved
11-8	R/W	0	reg_mcdi_pd22chkbadwoffst1. offset1 of pd22chkbadw from right film22 phase, -8~7, default = 0
7-5	R/W		reserved
4-0	R/W	12	reg_mcdi_pd22chkbadwgain1. gain1 of pd22chkbadw from right film22 phase, normalized to 16 as '1', default = 12

Table 9-893 MCDI_LMV_LOCK_CNT_THD_GAIN 0x2f49

Bit(s)	R/W	Default	Description
31-20	R/W		reserved
19-16	R/W	6	reg_mcdi_lmvlockcntmax. max lmv lock count number, default = 6
15-12	R/W	0	reg_mcdi_lmvlockcntoffst. offset for lmv lock count, -8~7, default = 0
11-8	R/W	8	reg_mcdi_lmvlockcntgain. gain for lmv lock count, normalized 8 as '1', 15 is set to 16, default = 8
7-5	R/W		reserved
4-0	R/W	4	reg_mcdi_lmvlockcntthd. lmv count thd (>=) before be locked, 1~31, default = 4

Table 9-894 MCDI_LMV_LOCK_ABS_DIF_THD 0x2f4a

Bit(s)	R/W	Default	Description
31-27	R/W		reserved
26-24	R/W	1	reg_mcdi_lmvlockdifthd2. lmv dif thd for third part, before locked, default = 1
23	R/W		reserved
22-20	R/W	1	reg_mcdi_lmvlockdifthd1. lmv dif thd for second part, before locked, default = 1
19	R/W		reserved
18-16	R/W	1	reg_mcdi_lmvlockdifthd0. lmv dif thd for first part, before locked, default = 1

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Bit(s)	R/W	Default	Description
15-13	R/W		reserved
12-8	R/W	24	reg_mcdi_lmvlockabsmax. max abs (<) of lmv to be locked, default = 24
7-5	R/W		reserved
4-0	R/W	1	reg_mcdi_lmvlockabsmin. min abs (>=) of lmv to be locked, default = 1

Table 9-895 MCDI_LMV_LOCK_ROW 0x2f4b

Bit(s)	R/W	Default	Description
31-27	R/W		reserved
26-16	R/W	2047	reg_mcdi_lmvlockendrow. end row (<) for lmv lock, default = 2047
15-11	R/W		reserved
10-0	R/W	0	reg_mcdi_lmvlockstartrow. start row (>=) for lmv lock, default = 0

Table 9-896 MCDI_LMV_LOCK_RT_MODE 0x2f4c

Bit(s)	R/W	Default	Description
31-27	R/W		reserved
26-24	R/W	2	reg_mcdi_lmvlockextmode. extend lines for lmv lock check, check how many lines for lmv locking, default = 2
23-16	R/W	32	reg_mcdi_lmvlockfltcntrt. ratio of flt cnt for lock check, normalized 256 as '1', 255 is set to 256, default = 32
15-8	R/W	48	reg_mcdi_lmvlocklmvcntrt1. ratio when use non-zero lmv for lock check, normalized 256 as '1', 255 is set to 256, default = 48
7-0	R/W	106	reg_mcdi_lmvlocklmvcntrt0. ratio when use max lmv for lock check, normalized 256 as '1', 255 is set to 256, default = 106

Table 9-897 MCDI_GMV_LOCK_CNT_THD_GAIN 0x2f4d

Bit(s)	R/W	Default	Description
31-20	R/W		reserved
19-16	R/W	6	reg_mcdi_gmvlockcntmax. max gmv lock count number, default = 6
15-12	R/W	0	reg_mcdi_gmvlockcntoffst. offset for gmv lock count, -8~7, default = 0
11-8	R/W	8	reg_mcdi_gmvlockcntgain. gain for gmv lock count, normalized 8 as '1', 15 is set to 16, default = 8
7-5	R/W		reserved
4-0	R/W	4	reg_mcdi_gmvlockcntthd. gmv count thd (>=) before be locked, 1~31, default = 4

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Table 9-898 MCDI_GMV_LOCK_ABS_DIF_THD 0x2f4e

Bit(s)	R/W	Default	Description
31-27	R/W		reserved
26-24	R/W	3	reg_mcdi_gmvlockdifthd2. gmv dif thd for third part, before locked, default = 3
23	R/W		reserved
22-20	R/W	2	reg_mcdi_gmvlockdifthd1. gmv dif thd for second part, before locked, default = 2
19	R/W		reserved
18-16	R/W	1	reg_mcdi_gmvlockdifthd0. gmv dif thd for first part, before locked, default = 1
15-13	R/W		reserved
12-8	R/W	15	reg_mcdi_gmvlockabsmax. max abs of gmv to be locked, default = 15
7-5	R/W		reserved
4-0	R/W	1	reg_mcdi_gmvlockabsmin. min abs of gmv to be locked, default = 1

Table 9-899 MCDI_HIGH_VERT_FRQ_DIF_THD 0x2f4f

Bit(s)	R/W	Default	Description
31-0	R/W	103680	reg_mcdi_highvertfrqfldavgdifthd. high_vert_frq field average luma dif thd (>=), 3*Blk_Width*Blk_Height, set by software, default = 103680

Table 9-900 MCDI_HIGH_VERT_FRQ_DIF_DIF_THD 0x2f50

Bit(s)	R/W	Default	Description
31-0	R/W	103680	reg_mcdi_highvertfrqfldavgdifdifthd. high_vert_frq field average luma dif's dif thd (<), 3*Blk_Width*Blk_Height, set by software, default = 103680

Table 9-901 MCDI_HIGH_VERT_FRQ_RT_GAIN 0x2f51

Bit(s)	R/W	Default	Description
31-20	R/W		reserved
19-16	R/W	4	reg_mcdi_highvertfrqcntthd. high_vert_frq count thd (>=) before locked, 1~31, default = 4
15-8	R/W	24	reg_mcdi_highvertfrqbadsadrt. ratio for high_vert_frq bad sad count, normalized 256 as '1', 255 is set to 256, default = 24
7-0	R/W	130	reg_mcdi_highvertfrqbadbadwrt. ratio for high_vert_frq badw count, normalized 256 as '1', 255 is set to 256, default = 130

Table 9-902 MCDI_MOTION_PARADOX_THD 0x2f52

Bit(s)	R/W	Default	Description
31-29	R/W		reserved
28-24	R/W	4	reg_mcdi_motionparadoxcntthd. motion paradox count thd (>=) before locked, 1~31, default = 4
23-22	R/W		reserved

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Bit(s)	R/W	Default	Description
21-16	R/W	32	reg_mcdi_motionparadoxgmvthd. abs gmv thd (<) of motion paradox, 0~32, note that 32 means invalid gmv, be careful, default = 32
15-0	R/W		reserved

Table 9-903 MCDI_MOTION_PARADOX_RT0x2f53

Bit(s)	R/W	Default	Description
31-24	R/W		reserved
23-16	R/W	24	reg_mcdi_motionparadoxbadsadrt. ratio for field bad sad count of motion paradox, normalized 256 as '1', 255 is set to 256, default = 24
15-8	R/W	120	reg_mcdi_motionparadoxbadrelrt. ratio for field bad reliabilty count of motion paradox, normalized 256 as '1', 255 is set to 256, default = 120
7-0	R/W	218	reg_mcdi_motionparadoxmtnrt. ratio for field motion count of motion paradox, normalized 256 as '1', 255 is set to 256, default = 218

Table 9-904 MCDI_MOTION_REF_THD 0x2f54

Bit(s)	R/W	Default	Description
31-24	R/W		reserved
23-20	R/W	15	reg_mcdi_motionrefoffst. motion ref additive offset, default = 15
19-16	R/W	8	reg_mcdi_motionrefgain. motion ref gain, normalized 8 as '1', default = 8
15-13	R/W		reserved
12-8	R/W	1	reg_mcdi_motionrefrptmvthd. abs thd (>=) of rpt mv (0~31, 32 means invalid) for motion ref, default = 1
7-2	R/W	2	reg_mcdi_motionrefqmvthd. min thd (>=) of abs qmv for motion ref, note that quarter mv's range is -63~63, default = 2
1-0	R/W	1	reg_mcdi_motionreflpfmode. Mv and (8 x repeat flg) 's lpf mode of motion refinement, 0: no lpf, 1: [1 2 1], 2: [1 2 2 2 1], default = 1

Table 9-905 MCDI_REL_COL_REF_RT 0x2f55

Bit(s)	R/W	Default	Description
31-8	R/W		reserved
7-0	R/W	135	reg_mcdi_relcolrefrt. ratio for column cofidence level against column number, for refinement, default = 135

Table 9-906 MCDI_PD22_CHK_THD_RT 0x2f56

Bit(s)	R/W	Default	Description
31-27	R/W		reserved
26-16	R/W	1	reg_mcdi_pd22chkfltcntrt. ratio for flat count of field pulldown 22 check, normalized 2048 as '1', 2047 is set to 2048, default = 1
15-8	R/W	100	reg_mcdi_pd22chkcntrt. ratio of pulldown 22 check count, normalized 256 as '1', 255 is set to 256, default = 100

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Bit(s)	R/W	Default	Description
7-5	R/W		reserved
4-0	R/W	4	reg_mcdi_pd22chkcntthd. thd (>=) for pd22 count before locked, 1~31, default = 4

Table 9-907 MCDI_CHAR_DET_DIF_THD 0x2f57

Bit(s)	R/W	Default	Description
31-24	R/W		reserved
23-16	R/W	64	reg_mcdi_chardetminmaxdifthd. thd (>=) for dif between min and max value, default = 64
15-8	R/W	17	reg_mcdi_chardetmaxdifthd. thd (<) for dif between max value, default = 17
7-0	R/W	17	reg_mcdi_chardetmindifthd. thd (<) for dif between min value, default = 17

Table 9-908 MCDI_CHAR_DET_CNT_THD 0x2f58

Bit(s)	R/W	Default	Description
31-21	R/W		reserved
20-16	R/W	18	reg_mcdi_chardettotcntthd. thd (>=) for total count, 0~21, default = 18
15-13	R/W		reserved
12-8	R/W	1	reg_mcdi_chardetmaxcntthd. thd (>=) for max count, 0~21, default = 1
7-5	R/W		reserved
4-0	R/W	1	reg_mcdi_chardetmincntthd. thd (>=) for min count, 0~21, default = 1

Table 9-909 MCDI_PD_22_CHK_WND0_X 0x2f59

Bit(s)	R/W	Default	Description
28-16	R/W	719	reg_mcdi_pd22chkwnd0_x1
12-0	R/W	0	reg_mcdi_pd22chkwnd0_x0

Table 9-910 MCDI_PD_22_CHK_WND0_Y 0x2f5a

Bit(s)	R/W	Default	Description
28-16	R/W	39	reg_mcdi_pd22chkwnd0_y1
12-0	R/W	0	reg_mcdi_pd22chkwnd0_y0

Table 9-911 MCDI_PD_22_CHK_WND1_X 0x2f5b

Bit(s)	R/W	Default	Description
28-16	R/W	719	reg_mcdi_pd22chkwnd1_x1
12-0	R/W	0	reg_mcdi_pd22chkwnd1_x0

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Table 9-912 MCDI_PD_22_CHK_WND1_Y 0x2f5c

Bit(s)	R/W	Default	Description
28-16	R/W	199	reg_mcdi_pd22chkwnd1_y1
12-0	R/W	40	reg_mcdi_pd22chkwnd1_y0

Table 9-913 MCDI_PD_22_CHK_FRC_LMV 0x2f5d

Bit(s)	R/W	Default	Description
10	R/W	1	reg_mcdi_pd22chklmvchk2
9	R/W	0	reg_mcdi_pd22chklmvchk1
8	R/W	0	reg_mcdi_pd22chklmvchk0
6	R/W	0	reg_mcdi_pd22chkfrcpd2
5	R/W	0	reg_mcdi_pd22chkfrcpd1
4	R/W	0	reg_mcdi_pd22chkfrcpd0
2	R/W	1	reg_mcdi_pd22chkfrcvof2
1	R/W	0	reg_mcdi_pd22chkfrcvof1
0	R/W	0	reg_mcdi_pd22chkfrcvof0

Table 9-914 MCDI_PD_22_CHK_FRC_LMV 0x2f5e

Bit(s)	R/W	Default	Description
26	R/W	0	reg_mcdi_pd22chkflg2
25	R/W	0	reg_mcdi_pd22chkflg1
24	R/W	0	reg_mcdi_pd22chkflg
23-16	R/W	1	reg_mcdi_pd22chkcnt2
15-8	R/W	0	reg_mcdi_pd22chkcnt1
7-0	R/W	0	reg_mcdi_pd22chkcnt

Table 9-915 MCDI_FIELD_MV 0x2f60

Bit(s)	R/W	Default	Description
31-24	R/W		reg_mcdi_pd22chkcnt
23-16	R/W		reg_mcdi_fieldgmvcnt
15	R/W		reg_mcdi_pd22chkflg
14	R/W		reg_mcdi_fieldgmvlock
13-8	R/W		reg_mcdi_fieldrptmv. last field rpt mv
7-6	R/W		reserved
5-0	R/W		reg_mcdi_fieldgmv. last field gmv

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Table 9-916 MCDI_FIELD_HVF_PRDX_CNT 0x2f61

Bit(s)	R/W	Default	Description
31-24	R/W		reg_mcdi_motionparadoxcnt.
23-17	R/W		reserved
16	R/W		reg_mcdi_motionparadoxflg.
15-8	R/W		reg_mcdi_highvertfrqcnt.
7-4	R/W		reserved
3-2	R/W		reg_mcdi_highvertfrqphase.
1	R/W		reserved
0	R/W		reg_mcdi_highvertfrqflg.

Table 9-917 MCDI_FIELD_LUMA_AVG_SUM_0 0x2f62

Bit(s)	R/W	Default	Description
31-0	R/W		reg_mcdi_fld_luma_avg_sum0.

Table 9-918 MCDI_FIELD_LUMA_AVG_SUM_1 0x2f63

Bit(s)	R/W	Default	Description
31-0	R/W		reg_mcdi_fld_luma_avg_sum1.

Table 9-919 MCDI_YCBCR_BLEND_CRTL 0x2f64

Bit(s)	R/W	Default	Description
31-16	R/W		reserved
15-8	R/W	0	reg_mcdi_ycbcrblendgain. ycbcr blending gain for cbcr in ycbcr. default = 0
7-2	R/W		reserved.
1-0	R/W	2	reg_mcdi_ycbcrblendmode. 0:y+cmb(cb,cr), 1:med(r,g,b), 2:max(r,g,b), default = 2

Table 9-920 MCDI_LMVLCKSTEXT_0 0x2f69

Bit(s)	R/W	Default	Description
27-16	R/W		reg_mcdi_lmvlckstext_1
11-0	R/W		reg_mcdi_lmvlckstext_0

Table 9-921 MCDI_LMVLCKSTEXT_1 0x2f6a

Bit(s)	R/W	Default	Description
31	R/W	1	reg_mcdi_refnewmode
30	R/W	1	reg_mcdi_reflmvlck_en

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Bit(s)	R/W	Default	Description
29:28	R/W	0	reg_mcdi_lmvlckupdw_ext
27:16	R/W	8	reg_mcdi_lmvlckmin
11:0	R/W	0	reg_mcdi_lmvlckstext_2

Table 9-922 MCDI_LMVLCKEDEXT_0 0x2f6b

Bit(s)	R/W	Default	Description
27:16	R/W	0	reg_mcdi_lmvlckedext_1
11:0	R/W	0	reg_mcdi_lmvlckedext_0

Table 9-923 MCDI_LMVLCKEDEXT_1 0x2f6c

Bit(s)	R/W	Default	Description
11:0	R/W	0	reg_mcdi_lmvlckedext_2

Table 9-924 MCDI_MC_CRTL 0x2f70

Bit(s)	R/W	Default	Description
31-20	R/W	0	reserved
19	R/W	0	reg buf1 enable (if1)
18	R/W	0	reg buf2 enable (if2)
17	R/W	0	reg mv invert
16	R/W	0	mcvec force 0
15	R/W	0	buf2 always en
14-12	R/W	0	reg_mcdi_mcvec_offset: 0: disable 1: 1 pixel offset of mcvec 2: 2 pixel offset of mcvec 3: 3 pixel offset of mcvec 4: 4 pixel offset of mcvec
11	R/w	0	reg_di_weave_both_side
10	R/W	0	reg_mcdi_mc_uv_en: mc for uv if needed, else use ma of uv
9-8	R/W	1	reg_mcdi_mcpreflg. flag to use previous field for MC, 0-forward field, 1: previous field,2-use forward & previous. default = 1
7	R/W	1	reg_mcdi_mcrelrefbycolcfden. enable rel refinement by column cofidence in mc blending, default = 1
6-5	R/W	0	reg_mcdi_mclpfen. enable mc pixles/rel lpf, 0:disable, 1: lpf rel, 2: lpf mc pxls, 3: lpf both rel and mc pxls, default = 0
4-2	R/W	0	reg_mcdi_mcdebugmode. enable mc debug mode, 0:disable, 1: split left/right, 2: split top/bottom, 3: debug mv, 4: debug rel, default = 0
1-0	R/W	1	reg_mcdi_mcen. mcdi enable mode, 0:disable, 1: blend with ma, 2: full mc, default = 1

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Table 9-925 MCDI_MC_LPF_MSK_0 0x2f71

Bit(s)	R/W	Default	Description
31-29	R/W		reserved
28	R		blend output ready
27	R		mcvec read input ready
26	R		mtn read input ready, same as bit24
25	R		ei dout ready (if0)
24	R		mtn read input ready
23	R		if2 input ready
22	R		if1 input ready
21	R		blend input ready
20-16	R/W	0	reg_mcdi_mclpfmsk02. mc lpf coef. 2 for pixel 0 of current block, normalized 16 as '1', default = 0
15-13	R/W		reserved
12-8	R/W	9	reg_mcdi_mclpfmsk01. mc lpf coef. 1 for pixel 0 of current block, normalized 16 as '1', default = 9
7-5	R/W		reserved
4-0	R/W	7	reg_mcdi_mclpfmsk00. mc lpf coef. 0 for pixel 0 of current block, normalized 16 as '1', default = 7

Table 9-926 MCDI_MC_LPF_MSK_1 0x2f72

Bit(s)	R/W	Default	Description
31-29	R/W		reserved
28-21	R		debug info
20-16	R/W	0	reg_mcdi_mclpfmsk12. mc lpf coef. 2 for pixel 1 of current block, 0~16, normalized 16 as '1', default = 0
15-13	R/W		reserved
12-8	R/W	11	reg_mcdi_mclpfmsk11. mc lpf coef. 1 for pixel 1 of current block, 0~16, normalized 16 as '1', default = 11
7-5	R/W		reserved
4-0	R/W	5	reg_mcdi_mclpfmsk10. mc lpf coef. 0 for pixel 1 of current block, 0~16, normalized 16 as '1', default = 5

Table 9-927 MCDI_MC_LPF_MSK_2 0x2f73

Bit(s)	R/W	Default	Description
31-29	R/W		reserved
28-21	R		debug info
20-16	R/W	1	reg_mcdi_mclpfmsk22. mc lpf coef. 2 for pixel 2 of current block, 0~16, normalized 16 as '1', default = 1
15-13	R/W		reserved

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Bit(s)	R/W	Default	Description
12-8	R/W	14	reg_mcdi_mclpfmsk21. mc lpf coef. 1 for pixel 2 of current block, 0~16, normalized 16 as '1', default = 14
7-5	R/W		reserved
4-0	R/W	1	reg_mcdi_mclpfmsk20. mc lpf coef. 0 for pixel 2 of current block, 0~16, normalized 16 as '1', default = 1

Table 9-928 MCDI_MC_LPF_MSK_3 0x2f74

Bit(s)	R/W	Default	Description
31-29	R/W		reserved
28-21	R		debug info
20-16	R/W	5	reg_mcdi_mclpfmsk32. mc lpf coef. 2 for pixel 3 of current block, 0~16, normalized 16 as '1', default = 5
15-13	R/W		reserved
12-8	R/W	11	reg_mcdi_mclpfmsk31. mc lpf coef. 1 for pixel 3 of current block, 0~16, normalized 16 as '1', default = 11
7-5	R/W		reserved
4-0	R/W	0	reg_mcdi_mclpfmsk30. mc lpf coef. 0 for pixel 3 of current block, 0~16, normalized 16 as '1', default = 0

Table 9-929 MCDI_MC_LPF_MSK_4 0x2f75

Bit(s)	R/W	Default	Description
31-21	R/W		reserved
20-16	R/W	7	reg_mcdi_mclpfmsk42. mc lpf coef. 2 for pixel 4 of current block, 0~16, normalized 16 as '1', default = 7
15-13	R/W		reserved
12-8	R/W	9	reg_mcdi_mclpfmsk41. mc lpf coef. 1 for pixel 4 of current block, 0~16, normalized 16 as '1', default = 9
7-5	R/W		reserved
4-0	R/W	0	reg_mcdi_mclpfmsk40. mc lpf coef. 0 for pixel 4 of current block, 0~16, normalized 16 as '1', default = 0

Table 9-930 MCDI_MC_REL_GAIN_OFFST_0 0x2f76

Bit(s)	R/W	Default	Description
31-26	R/W		reserved
25	R/W	0	reg_mcdi_mcmotionparadoxflg. flag of motion paradox, initial with 0 and read from software, default = 0
24	R/W	0	reg_mcdi_mchighvertfrqflg. flag of high vert frq, initial with 0 and read from software, default = 0
23-16	R/W	128	reg_mcdi_mcmotionparadoxoffst. offset (r+ offset) for rel (MC blending coef.) refinement if motion paradox detected before MC blending before MC blending, default = 128

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Bit(s)	R/W	Default	Description
15-12	R/W		reserved
11-8	R/W	8	reg_mcdi_mcmotionparadoxgain. gain for rel (MC blending coef.) refinement if motion paradox detected before MC blending, normalized 8 as '1', set 15 to 16, default = 8
7-4	R/W	15	reg_mcdi_mchighvertfrqoffst. minus offset (alpha - offset) for motion (MA blending coef.) refinement if high vertical frequency detected before MA blending, default = 15
3-0	R/W	8	reg_mcdi_mchighvertfrqgain. gain for motion (MA blending coef.) refinement if high vertical frequency detected before MA blending, normalized 8 as '1', set 15 to 16, default = 8

Table 9-931 MCDI_MC_REL_GAIN_OFFST_1 0x2f77

Bit(s)	R/W	Default	Description
31-24	R/W	255	reg_mcdi_mcoutofboundrayoffst. offset (rel + offset) for rel (MC blending coef.) refinement if MC pointed out of boundray before MC blending before MC blending, default = 255
23-20	R/W		reserved
19-16	R/W	8	reg_mcdi_mcoutofboundraygain. gain for rel (MC blending coef.) refinement if MC pointed out of boundray before MC blending, normalized 8 as '1', set 15 to 16, default = 8
15-8	R/W	255	reg_mcdi_mcrelrefbycolcfdoffst. offset (rel + offset) for rel (MC blending coef.) refinement if motion paradox detected before MC blending before MC blending, default = 255
7-4	R/W		reserved.
3-0	R/W	8	reg_mcdi_mcrelrefbycolcfdgain. gain for rel (MC blending coef.) refinement if column cofidence failed before MC blending, normalized 8 as '1', set 15 to 16, default = 8

Table 9-932 MCDI_MC_COL_CFD_0 0x2f78

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_0. column cofidence value 0 read from software. initial = 0

Table 9-933 MCDI_MC_COL_CFD_1 0x2f79

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_1. column cofidence value 1 read from software. initial = 0

Table 9-934 MCDI_MC_COL_CFD_2 0x2f7a

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_2. column cofidence value 2 read from software. initial = 0

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Table 9-935 MCDI_MC_COL_CFD_3 0x2f7b

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_3. column cofidence value 3 read from software. initial = 0

Table 9-936 MCDI_MC_COL_CFD_4 0x2f7c

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 4 read from software. initial = 0

Table 9-937 MCDI_MC_COL_CFD_5 0x2f7d

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 5 read from software. initial = 0

Table 9-938 MCDI_MC_COL_CFD_6 0x2f7e

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 6 read from software. initial = 0

Table 9-939 MCDI_MC_COL_CFD_7 0x2f7f

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 7 read from software. initial = 0

Table 9-940 MCDI_MC_COL_CFD_8 0x2f80

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 8 read from software. initial = 0

Table 9-941 MCDI_MC_COL_CFD_9 0x2f81

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 9 read from software. initial = 0

Table 9-942 MCDI_MC_COL_CFD_10 0x2f82

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 10 read from software. initial = 0

Table 9-943 MCDI_MC_COL_CFD_11 0x2f83

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 11 read from software. initial = 0

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Table 9-944 MCDI_MC_COL_CFD_12 0x2f84

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 12 read from software. initial = 0

Table 9-945 MCDI_MC_COL_CFD_13 0x2f85

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 13 read from software. initial = 0

Table 9-946 MCDI_MC_COL_CFD_14 0x2f86

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 14 read from software. initial = 0

Table 9-947 MCDI_MC_COL_CFD_15 0x2f87

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 15 read from software. initial = 0

Table 9-948 MCDI_MC_COL_CFD_16 0x2f88

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 16 read from software. initial = 0

Table 9-949 MCDI_MC_COL_CFD_17 0x2f89

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 17 read from software. initial = 0

Table 9-950 MCDI_MC_COL_CFD_18 0x2f8a

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 18 read from software. initial = 0

Table 9-951 MCDI_MC_COL_CFD_19 0x2f8b

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 19 read from software. initial = 0

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Table 9-952 MCDI_MC_COL_CFD_20 0x2f8c

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 20 read from software. initial = 0

Table 9-953 MCDI_MC_COL_CFD_21 0x2f8d

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 21 read from software. initial = 0

Table 9-954 MCDI_MC_COL_CFD_22 0x2f8e

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 22 read from software. initial = 0

Table 9-955 MCDI_MC_COL_CFD_23 0x2f8f

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 23 read from software. initial = 0

Table 9-956 MCDI_MC_COL_CFD_24 0x2f90

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 24 read from software. initial = 0

Table 9-957 MCDI_MC_COL_CFD_25 0x2f91

Bit(s)	R/W	Default	Description
31-0	R/W		mcdi_mc_col_cfd_4. column cofidence value 25 read from software. initial = 0

Table 9-958 MCDI_RO_FLD_LUMA_AVG_SUM 0x2fa0

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_fldlumaavgsum. block's luma avg sum of current filed (block based). initial = 0

Table 9-959 MCDI_RO_GMV_VLD_CNT 0x2fa1

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_gmvvldcnt. valid gmv's count of pre one filed (block based). initial = 0

Table 9-960 MCDI_RO_RPT_FLG_CNT 0x2fa2

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_rptflgcnt. repeat mv's count of pre one filed (block based). initial = 0

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Table 9-961 MCDI_RO_FLD_BAD_SAD_CNT 0x2fa3

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_fldbadsadcnt. bad sad count of whole pre one field (block based). initial = 0

Table 9-962 MCDI_RO_FLD_BAD_BADW_CNT 0x2fa4

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_fldbadbadwcnt. bad badw count of whole pre one field (block based). initial = 0

Table 9-963 MCDI_RO_FLD_BAD_REL_CNT 0x2fa5

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_fldbadrelcnt. bad rel count of whole pre one field (block based). initial = 0

Table 9-964 MCDI_RO_FLD_MTN_CNT 0x2fa6

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_fldmtncnt. motion count of whole pre one field (pixel based). initial = 0

Table 9-965 MCDI_RO_FLD_VLD_CNT 0x2fa7

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_fldvldcnt. valid motion count of whole pre one field (pixel based). initial = 0

Table 9-966 MCDI_RO_FLD_PD_22_PRE_CNT 0x2fa8

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_fldpd22precnt. prevoius pd22 check count of whole pre one field (block based). initial = 0

Table 9-967 MCDI_RO_FLD_PD_22_FOR_CNT 0x2fa9

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_fldpd22forcnt. forward pd22 check count of whole pre one field (block based). initial = 0

Table 9-968 MCDI_RO_FLD_PD_22_FLT_CNT 0x2faa

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_fldpd22fltcnt. flat count (for pd22 check) of whole pre one field (block based). initial = 0

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Table 9-969 MCDI_RO_HIGH_VERT_FRQ_FLG 0x2fab

Bit(s)	R/W	Default	Description
31-16	R		reserved.
15-8	R		ro_mcdi_highvertfrqcnt. high vertical frequency count till prevoius one field. initial = 0
7-3	R		reserved.
2-1	R		ro_mcdi_highvertfrqphase. high vertical frequency phase of prevoius one field. initial = 2
0	R		ro_mcdi_highvertfrqflg. high vertical frequency flag of prevoius one field. initial = 0

Table 9-970 MCDI_RO_GMV_LOCK_FLG 0x2fac

Bit(s)	R/W	Default	Description
31-16	R		reserved.
15-8	R		ro_mcdi_gmvlckcnt. global mv lock count till prevoius one field. initial = 0
7-2	R		ro_mcdi_gmv. global mv of prevoius one field. -31~31, initial = 32 (invalid value)
1	R		ro_mcdi_zerogmvlckflg. zero global mv lock flag of prevoius one field. initial = 0
0	R		ro_mcdi_gmvlckflg. global mv lock flag of prevoius one field. initial = 0

Table 9-971 MCDI_RO_RPT_MV 0x2fad

Bit(s)	R/W	Default	Description
5-0	R		ro_mcdi_rptmv. repeate mv of prevoius one field. -31~31, initial = 32 (invalid value)

Table 9-972 MCDI_RO_MOTION_PARADOX_FLG 0x2fae

Bit(s)	R/W	Default	Description
31-16	R		reserved.
15-8	R		ro_mcdi_motionparadoxcnt. motion paradox count till prevoius one field. initial = 0
7-1	R		reserved.
0	R		ro_mcdi_motionparadoxflg. motion paradox flag of prevoius one field. initial = 0

Table 9-973 MCDI_RO_PD_22_FLG 0x2faf

Bit(s)	R/W	Default	Description
31-16	R		reserved.
26	R	0	ro_mcdi_pd22flg2. pull down 22 flag of prevoius one field. initial = 0
25	R	0	ro_mcdi_pd22flg1. pull down 22 flag of prevoius one field. initial = 0
24	R	0	ro_mcdi_pd22flg0. pull down 22 flag of prevoius one field. initial = 0

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Bit(s)	R/W	Default	Description
23-16	R	0	ro_mcdi_pd22cnt2. pull down 22 count till prevoius one field. initial = 0
15-8	R	0	ro_mcdi_pd22cnt1. pull down 22 count till prevoius one field. initial = 0
7-0	R	0	ro_mcdi_pd22cnt0. pull down 22 count till prevoius one field. initial = 0

Table 9-974 MCDI_RO_COL_CFD_0 0x2fb0

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_0. column cofidence value 0. initial = 0

Table 9-975 MCDI_RO_COL_CFD_1 0x2fb1

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_1. column cofidence value 1. initial = 0

Table 9-976 MCDI_RO_COL_CFD_2 0x2fb2

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_2. column cofidence value 2. initial = 0

Table 9-977 MCDI_RO_COL_CFD_3 0x2fb3

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_3. column cofidence value 3. initial = 0

Table 9-978 MCDI_RO_COL_CFD_4 0x2fb4

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_4. column cofidence value 4. initial = 0

Table 9-979 MCDI_RO_COL_CFD_5 0x2fb5

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_5. column cofidence value 5. initial = 0

Table 9-980 MCDI_RO_COL_CFD_6 0x2fb6

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_6. column cofidence value 6. initial = 0

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Table 9-981 MCDI_RO_COL_CFD_7 0x2fb7

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_7. column cofidence value 7. initial = 0

Table 9-982 MCDI_RO_COL_CFD_8 0x2fb8

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_8. column cofidence value 8. initial = 0

Table 9-983 MCDI_RO_COL_CFD_9 0x2fb9

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_9. column cofidence value 9. initial = 0

Table 9-984 MCDI_RO_COL_CFD_10 0x2fba

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_10. column cofidence value 10. initial = 0

Table 9-985 MCDI_RO_COL_CFD_11 0x2fbb

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_11. column cofidence value 11. initial = 0

Table 9-986 MCDI_RO_COL_CFD_12 0x2fbc

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_12. column cofidence value 12. initial = 0

Table 9-987 MCDI_RO_COL_CFD_13 0x2fbd

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_13. column cofidence value 13. initial = 0

Table 9-988 MCDI_RO_COL_CFD_14 0x2fbe

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_14. column cofidence value 14. initial = 0

Table 9-989 MCDI_RO_COL_CFD_15 0x2fbf

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_15. column cofidence value 15. initial = 0

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Table 9-990 MCDI_RO_COL_CFD_16 0x2fc0

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_16. column cofidence value 16. initial = 0

Table 9-991 MCDI_RO_COL_CFD_17 0x2fc1

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_17. column cofidence value 17. initial = 0

Table 9-992 MCDI_RO_COL_CFD_18 0x2fc2

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_18. column cofidence value 18. initial = 0

Table 9-993 MCDI_RO_COL_CFD_19 0x2fc3

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_19. column cofidence value 19. initial = 0

Table 9-994 MCDI_RO_COL_CFD_20 0x2fc4

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_20. column cofidence value 20. initial = 0

Table 9-995 MCDI_RO_COL_CFD_21 0x2fc5

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_21. column cofidence value 21. initial = 0

Table 9-996 MCDI_RO_COL_CFD_22 0x2fc6

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_22. column cofidence value 22. initial = 0

Table 9-997 MCDI_RO_COL_CFD_23 0x2fc7

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_23. column cofidence value 23. initial = 0

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Table 9-998 MCDI_RO_COL_CFD_24 0x2fc8

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_24. column cofidence value 24. initial = 0

Table 9-999 MCDI_RO_COL_CFD_25 0x2fc9

Bit(s)	R/W	Default	Description
31-0	R		ro_mcdi_col_cfd_25. column cofidence value 25. initial = 0

Table 9-1000 MCDI_RO_FLD_PD_22_PRE_CNT1 0x2fca

Bit(s)	R/W	Default	Description
31-0	R		previous pd22 check count of whole pre one field(block based). initial = 0

Table 9-1001 MCDI_RO_FLD_PD_22_POR_CNT1 0x2fcb

Bit(s)	R/W	Default	Description
31-0	R		forward pd22 check count of whole pre one field(block based). initial = 0

Table 9-1002 MCDI_RO_FLD_PD_22_FLT_CNT1 0x2fcc

Bit(s)	R/W	Default	Description
31-0	R		flat count(for pd22 check) of whole pre one field(block based). initial = 0

Table 9-1003 MCDI_RO_FLD_PD_22_PRE_CNT2 0x2fcd

Bit(s)	R/W	Default	Description
31-0	R		previous pd22 check count of whole pre one field(block based). initial = 0

Table 9-1004 MCDI_RO_FLD_PD_22_POR_CNT2 0x2fce

Bit(s)	R/W	Default	Description
31-0	R		forward pd22 check count of whole pre one field(block based). initial = 0

Table 9-1005 MCDI_RO_FLD_PD_22_FLT_CNT2 0x2fcf

Bit(s)	R/W	Default	Description
31-0	R		flat count(for pd22 check) of whole pre one field(block based). initial = 0

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Table 9-1006 DIPD_COMB_CTRL0 0x2fd0

Bit(s)	R/W	Default	Description
31-24	W		Cmb_v_dif_min
23-16	W		Cmb_v_dif_max
15-8	W		Cmb_crg_min
7-0	W		Cmb_crg_max

Table 9-1007 DIPD_COMB_CTRL1 0x2fd1

Bit(s)	R/W	Default	Description
31	W		Pd_check_en
29-24	W		Cmb_wv_min3
21-16	W		Cmb_wv_min2
13-8	W		Cmb_wv_min1
5-0	W		Cmb_wv_min0

Table 9-1008 DIPD_COMB_CTRL2 0x2fd2

Bit(s)	R/W	Default	Description
31-28	W		Cmb_wnd_cnt1
25-20	W		Ccnt_cmmin1
19-16	W		Ccnt_mtmin
13-8	W		Ccnt_cmmin
5-0	W		Cmb_wv_min4

Table 9-1009 DIPD_COMB_CTRL3 0x2fd3

Bit(s)	R/W	Default	Description
31	W		Cmb32spcl
17-12	W		Cmb_wnd_mthd
11-4	W		Cmb_abs_nocmb
3-0	W		Cnt_minlen

Table 9-1010 DIPD_COMB_CTRL4 0x2fd4

Bit(s)	R/W	Default	Description
30	W		Flm_stamtn_en
29-28	W		In_horflt

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Bit(s)	R/W	Default	Description
27-20	W		Alpha
19-16	W		Rhtran_ctmtd
15-8	W		Htran_mnth1
7-0	W		Htran_mnth0

Table 9-1011 DIPD_COMB_CTRL5 0x2fd5

Bit(s)	R/W	Default	Description
31-24	W		Fld_mindif
23-16	W		Frm_mindif
13-8	W		Flm_smp_mtn_cnt
7-0	W		Flm_smp_mtn_thd

Table 9-1012 DIPD_RO_COMB_0 0x2fd6

Bit(s)	R/W	Default	Description
31-0	R		frmdif

Table 9-1013 DIPD_RO_COMB_1 0x2fd7

Bit(s)	R/W	Default	Description
31-0	R		Frmdif0

Table 9-1014 DIPD_RO_COMB_2 0x2fd8

Bit(s)	R/W	Default	Description
31-0	R		Frmdif1

Table 9-1015 DIPD_RO_COMB_3 0x2fd9

Bit(s)	R/W	Default	Description
31-0	R		Frmdif2

Table 9-1016 DIPD_RO_COMB_4 0x2fda

Bit(s)	R/W	Default	Description
31-0	R		Frmdif3

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Table 9-1017 DIPD_RO_COMB_5 0x2fdb

Bit(s)	R/W	Default	Description
31-0	R		Frmdif4

Table 9-1018 DIPD_RO_COMB_6 0x2fdc

Bit(s)	R/W	Default	Description
31-0	R		fldif

Table 9-1019 DIPD_RO_COMB_7 0x2fdd

Bit(s)	R/W	Default	Description
31-0	R		Fldif0

Table 9-1020 DIPD_RO_COMB_8 0x2fde

Bit(s)	R/W	Default	Description
31-0	R		Fldif1

Table 9-1021 DIPD_RO_COMB_9 0x2fdf

Bit(s)	R/W	Default	Description
31-0	R		Fldif2

Table 9-1022 DIPD_RO_COMB_10 0x2fe0

Bit(s)	R/W	Default	Description
31-0	R		Fldif3

Table 9-1023 DIPD_RO_COMB_11 0x2fe1

Bit(s)	R/W	Default	Description
31-0	R		Fldif4

Table 9-1024 DIPD_RO_COMB_12 0x2fe2

Bit(s)	R/W	Default	Description
31-0	R		Ro_rt0

Table 9-1025 DIPD_RO_COMB_13 0x2fe3

Bit(s)	R/W	Default	Description
31-0	R		Ro_rt1

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Table 9-1026 DIPD_RO_COMB_14 0x2fe4

Bit(s)	R/W	Default	Description
31-0	R		Ro_rt2

Table 9-1027 DIPD_RO_COMB_15 0x2fe5

Bit(s)	R/W	Default	Description
31-0	R		Ro_rt3

Table 9-1028 DIPD_RO_COMB_16 0x2fe6

Bit(s)	R/W	Default	Description
31-0	R		Ro_rt4

Table 9-1029 DIPD_RO_COMB_17 0x2fe7

Bit(s)	R/W	Default	Description
31-0	R		Ro_rt5

Table 9-1030 DIPD_RO_COMB_18 0x2fe8

Bit(s)	R/W	Default	Description
31-0	R		Ro_rt6

Table 9-1031 DIPD_RO_COMB_19 0x2fe9

Bit(s)	R/W	Default	Description
31-0	R		Ro_rt7

Table 9-1032 DIPD_RO_COMB_20 0x2fea

Bit(s)	R/W	Default	Description
31-0	R		Ro_rt8

Table 9-1033 DIPD_COMB_CTRL5 0x2fd5

Bit(s)	R/W	Default	Description
31-24	W		Fld_mindif
23-16	W		Frm_mindif
13-8	W		Flm_smp_mtn_cnt
7-0	W		Flm_smp_mtn_thd

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Table 9-1034 DIPD_COMB_CTRL6 0x2feb

Bit(s)	R/W	Default	Description
21	Rw	0	Reg_edit_sel
20	Rw	1	Reg_horflt_en
16-12	Rw	7	Reg_combseglen
9-4	Rw	6	Reg_trancombrat
3-0	Rw	4	Reg_combsegmin

9.2.3.16 DNR Registers

Table 9-1035 DNR_CTRL 0x2d00

Bit(s)	R/W	Default	Description
31:20	R/W		reserved
19	R/W		reg_dnr_bufctrl, deblock linebuf control, 0 : 3line 1: 5line, default =1
18	R/W		reg_dnr_dm_bufctrl, demosquito linebuf control, 0 : 3line 1: 5line, default =1
16	R/W		reg_dnr_en
15	R/W		reg_dnr_db_vdbstep , vdb step, 0: 4, 1: 8 . unsigned , default = 1
14	R/W		reg_dnr_db_vdbprten , vdb protectoin enable . unsigned , default = 1
13	R/W		reg_dnr_gbs_difen , enable dif (between LR and LL/RR) condition for gbs stat.. unsigned , default = 0
12	R/W		reg_dnr_luma_en , enable ycbcr2luma module . unsigned , default = 1
11:10	R/W		reg_dnr_db_mod , deblocking mode, 0: disable, 1: horizontal deblocking, 2: vertical deblocking, 3: horizontal & vertical deblocking. unsigned , default = 3
9	R/W		reg_dnr_db_chrmen , enable chroma deblocking . unsigned , default = 1
8	R/W		reg_dnr_hvdif_mod , 0: calc. difs by original Y, 1: by new luma. unsigned , default = 1
7	R/W		reserved
6: 4	R/W		reg_dnr_demo_lften , b0: Y b1:U b2:V . unsigned , default = 7
3	R/W		reserved
2: 0	R/W		reg_dnr_demo_rgten , b0: Y b1:U b2:V . unsigned , default = 7

Table 9-1036 DNR_HVSIZE 0x2d01

Bit(s)	R/W	Default	Description
31:29	R/W		reserved
28:16	R/W		reg_dnr_hsize , hsize . unsigned , default = 0
15:13	R/W		reserved
12: 0	R/W		reg_dnr_vsize , vsize . unsigned , default = 0

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Table 9-1037 DNR_DBLK_BLANK_NUM 0x2d02

Bit(s)	R/W	Default	Description
31:16	R/W		reserved
15: 8	R/W		reg_dblk_hblank_num , deblock hor blank num . unsigned , default = 16
7: 0	R/W		reg_dblk_vblank_num , deblock ver blank num . unsigned , default = 45

Table 9-1038 DNR_BLK_OFFST 0x2d03

Bit(s)	R/W	Default	Description
31: 7	R/W		reserved
6: 4	R/W		reg_dnr_hbofst , horizontal block offset may provide by software calc.. unsigned , default = 0
3	R/W		reserved
2: 0	R/W		reg_dnr_vbofst , vertical block offset may provide by software calc.. unsigned , default = 0

Table 9-1039 DNR_GBS 0x2d04

Bit(s)	R/W	Default	Description
31: 2	R/W		reserved
1: 0	R/W		reg_dnr_gbs , global block strength may update by software calc.. unsigned , default = 0

Table 9-1040 DNR_HBOFFST_STAT 0x2d05

Bit(s)	R/W	Default	Description
31:24	R/W		reg_dnr_hbof_difthd , dif threshold (>=) between LR and LL/RR. unsigned , default = 2
23:16	R/W		reg_dnr_hbof_edgethd , edge threshold (<=) for LR . unsigned , default = 32
15: 8	R/W		reg_dnr_hbof_flatthd , flat threshold (>=) for LR . unsigned , default = 0
7	R/W		reserved
6: 4	R/W		reg_dnr_hbof_delta , delta for weighted bin accumulator. unsigned , default = 1
3	R/W		reserved
2: 0	R/W		reg_dnr_hbof_statmod , statistic mode for horizontal block offset, 0: count flags for 8-bin, 1: count LRs for 8-bin, 2: count difs for 8-bin, 3: count weighted flags for 8-bin, 4: count flags for first 32-bin, 5: count LRs for first 32-bin, 6 or 7: count difs for first 32-bin. unsigned , default = 2

Table 9-1041 DNR_VBOFFST_STAT 0x2d06

Bit(s)	R/W	Default	Description
31:24	R/W		reg_dnr_vbof_difthd , dif threshold (>=) between Up and Dw. unsigned , default = 1
23:16	R/W		reg_dnr_vbof_edgethd , edge threshold (<=) for Up/Dw. unsigned , default = 16

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Bit(s)	R/W	Default	Description
15: 8	R/W		reg_dnr_vbof_flatthd , flat threshold (>=) for Up/Dw. unsigned , default = 0
7	R/W		reserved
6: 4	R/W		reg_dnr_vbof_delta , delta for weighted bin accumulator. unsigned , default = 1
3	R/W		reserved
2: 0	R/W		reg_dnr_vbof_statmod , statistic mode for vertical block offset, 0: count flags for 8-bin, 1: count Ups for 8-bin, 2: count difs for 8-bin, 3: count weighted flags for 8-bin, 4: count flags for first 32-bin, 5: count Ups for first 32-bin, 6 or 7: count difs for first 32-bin. unsigned , default = 2

Table 9-1042 DNR_GBS_STAT 0x2d07

Bit(s)	R/W	Default	Description
31:24	R/W		reg_dnr_gbs_edgethd , edge threshold (<=) for LR . unsigned , default = 32
23:16	R/W		reg_dnr_gbs_flatthd , flat threshold (>=) for LR . unsigned , default = 0
15: 8	R/W		reg_dnr_gbs_varthd , variation threshold (<=) for Lvar/Rvar. unsigned , default = 16
7: 0	R/W		reg_dnr_gbs_difthd , dif threshold (>=) between LR and LL/RR. unsigned , default = 2

Table 9-1043 DNR_STAT_X_START_END 0x2d08

Bit(s)	R/W	Default	Description
31:30	R/W		reserved
29:16	R/W		reg_dnr_stat_xst . unsigned , default = 24
15:14	R/W		reserved
13: 0	R/W		reg_dnr_stat_xed . unsigned , default = HSIZE - 25

Table 9-1044 DNR_STAT_Y_START_END 0x2d09

Bit(s)	R/W	Default	Description
31:30	R/W		reserved
29:16	R/W		reg_dnr_stat_yst . unsigned , default = 24
15:14	R/W		reserved
13: 0	R/W		reg_dnr_stat_yed . unsigned , default = VSIZE - 25

Table 9-1045 DNR_LUMA 0x2d0a

Bit(s)	R/W	Default	Description
31:27	R/W		reserved
28	R/W		Reg_dnr_luma_mode, ycbcr2luma mode selection, default =0
26:24	R/W		reg_dnr_luma_sqrtshft , left shift for fast squart of chroma, [0, 4]. unsigned , default = 2

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Bit(s)	R/W	Default	Description
23:21	R/W		reserved
20:16	R/W		reg_dnr_luma_sqrtoffst , offset for fast squart of chroma. signed , default = 0
15	R/W		reserved
14:12	R/W		reg_dnr_luma_wcmod , theta related to warm/cool segment line, 0: 0, 1: 45, 2: 90, 3: 135, 4: 180, 5: 225, 6: 270, 7: 315. . unsigned , default = 3
11: 8	R/W		reg_dnr_luma_cshft , shift for calc. delta part, 0~8, . unsigned , default = 8
7: 6	R/W		reserved
5: 0	R/W		reg_dnr_luma_cgain , final gain for delta part, 32 normalized to "1". unsigned , default = 4

Table 9-1046 DNR_DB_YEDGE_THD 0x2d0b

Bit(s)	R/W	Default	Description
31:24	R/W		reg_dnr_db_yedgethd0 , edge threshold0 for luma . unsigned , default = 12
23:16	R/W		reg_dnr_db_yedgethd1 , edge threshold1 for luma . unsigned , default = 15
15: 8	R/W		reg_dnr_db_yedgethd2 , edge threshold2 for luma . unsigned , default = 18
7: 0	R/W		reg_dnr_db_yedgethd3 , edge threshold3 for luma . unsigned , default = 25

Table 9-1047 DNR_DB_CEDGE_THD 0x2d0c

Bit(s)	R/W	Default	Description
31:24	R/W		reg_dnr_db_cedgethd0 , edge threshold0 for chroma . unsigned , default = 12
23:16	R/W		reg_dnr_db_cedgethd1 , edge threshold1 for chroma . unsigned , default = 15
15: 8	R/W		reg_dnr_db_cedgethd2 , edge threshold2 for chroma . unsigned , default = 18
7: 0	R/W		reg_dnr_db_cedgethd3 , edge threshold3 for chroma . unsigned , default = 25

Table 9-1048 DNR_DB_HGAP 0x2d0d

Bit(s)	R/W	Default	Description
31:24	R/W		reserved
23:16	R/W		reg_dnr_db_hgapthd , horizontal gap thd (<=) for very sure blockiness . unsigned , default = 8
15: 8	R/W		reg_dnr_db_hgapdifthd , dif thd between hgap and lft/rgt hdifs. unsigned , default = 1
7: 1	R/W		reserved
0	R/W		reg_dnr_db_hgapmod , horizontal gap calc. mode, 0: just use current col x, 1: find max between (x-1, x, x+1) . unsigned , default = 0

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Table 9-1049 DNR_DB_HBS 0x2d0e

Bit(s)	R/W	Default	Description
31: 6	R/W		reserved
5: 4	R/W		reg_dnr_db_hbsup , horizontal bs up value . unsigned , default = 1
3: 2	R/W		reg_dnr_db_hbsmax , max value of hbs for global control. unsigned , default = 3
1: 0	R/W		reg_dnr_db_hgbsthd , gbs thd (>=) for hbs calc. . unsigned , default = 1

Table 9-1050 DNR_DB_HACT 0x2d0f

Bit(s)	R/W	Default	Description
31:16	R/W		reserved
15: 8	R/W		reg_dnr_db_hactthd0 , thd0 of hact, for block classification. unsigned , default = 10
7: 0	R/W		reg_dnr_db_hactthd1 , thd1 of hact, for block classification. unsigned , default = 32

Table 9-1051 DNR_DB_YHDELTA_GAIN 0x2d10

Bit(s)	R/W	Default	Description
31:27	R/W		reserved
26:24	R/W		reg_dnr_db_yhdeltagain1 , (p1-q1) gain for Y's delta calc. when bs=1, normalized 8 as "1" . unsigned , default = 2
23	R/W		reserved
22:20	R/W		reg_dnr_db_yhdeltagain2 , (p1-q1) gain for Y's delta calc. when bs=2, normalized 8 as "1" . unsigned , default = 0
19	R/W		reserved
18:16	R/W		reg_dnr_db_yhdeltagain3 , (p1-q1) gain for Y's delta calc. when bs=3, normalized 8 as "1" . unsigned , default = 0
15	R/W		reserved
14: 8	R/W		reg_dnr_db_yhdeltaadjoffst , offset for adjust Y's hdelta (-64, 63). signed , default = 0
7: 6	R/W		reserved
5: 0	R/W		reg_dnr_db_yhdeltaadjgain , gain for adjust Y's hdelta, normalized 32 as "1" . unsigned , default = 32

Table 9-1052 DNR_DB_YHDELTA2_GAIN 0x2d11

Bit(s)	R/W	Default	Description
31:30	R/W		reserved
29:24	R/W		reg_dnr_db_yhdelta2gain2 , gain for bs=2's adjust Y's hdelta2, normalized 64 as "1" . unsigned , default = 8
23:21	R/W		reserved
20:16	R/W		reg_dnr_db_yhdelta2offst2 , offset for bs=2's adjust Y's hdelta2 (-16, 15). signed , default = 0

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Bit(s)	R/W	Default	Description
15:14	R/W		reserved
13: 8	R/W		reg_dnr_db_yhdelta2gain3 , gain for bs=3's adjust Y's hdelta2, normalized 64 as "1" . unsigned , default = 4
7: 5	R/W		reserved
4: 0	R/W		reg_dnr_db_yhdelta2offst3 , offset for bs=3's adjust Y's hdelta2 (-16, 15). signed , default = 0

Table 9-1053 DNR_DB_CHDELTA_GAIN 0x2d12

Bit(s)	R/W	Default	Description
31:27	R/W		reserved
26:24	R/W		reg_dnr_db_chdeltagain1 , (p1-q1) gain for UV's delta calc. when bs=1, normalized 8 as "1". unsigned , default = 2
23	R/W		reserved
22:20	R/W		reg_dnr_db_chdeltagain2 , (p1-q1) gain for UV's delta calc. when bs=2, normalized 8 as "1". unsigned , default = 0
19	R/W		reserved
18:16	R/W		reg_dnr_db_chdeltagain3 , (p1-q1) gain for UV's delta calc. when bs=3, normalized 8 as "1". unsigned , default = 0
15	R/W		reserved
14: 8	R/W		reg_dnr_db_chdeltaadjoffst , offset for adjust UV's hdelta (-64, 63). signed , default = 0
7: 6	R/W		reserved
5: 0	R/W		reg_dnr_db_chdeltaadjgain , gain for adjust UV's hdelta, normalized 32 as "1". unsigned , default = 32

Table 9-1054 DNR_DB_CHDELTA2_GAIN 0x2d13

Bit(s)	R/W	Default	Description
31:30	R/W		reserved
29:24	R/W		reg_dnr_db_chdelta2gain2 , gain for bs=2's adjust UV's hdelta2, normalized 64 as "1" . unsigned , default = 8
23:21	R/W		reserved
20:16	R/W		reg_dnr_db_chdelta2offst2 , offset for bs=2's adjust UV's hdelta2 (-16, 15). signed , default = 0
15:14	R/W		reserved
13: 8	R/W		reg_dnr_db_chdelta2gain3 , gain for bs=2's adjust UV's hdelta2, normalized 64 as "1" . unsigned , default = 4
7: 5	R/W		reserved
4: 0	R/W		reg_dnr_db_chdelta2offst3 , offset for bs=2's adjust UV's hdelta2 (-16, 15). signed , default = 0

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Table 9-1055 DNR_DB_YC_VEDGE_THD 0x2d14

Bit(s)	R/W	Default	Description
31:16	R/W		reserved
15: 8	R/W		reg_dnr_db_yvedgethd , special Y's edge thd for vdb. unsigned , default = 12
7: 0	R/W		reg_dnr_db_cvedgethd , special UV's edge thd for vdb. unsigned , default = 12

Table 9-1056 DNR_DB_VBS_MISC 0x2d15

Bit(s)	R/W	Default	Description
31:24	R/W		reg_dnr_db_vgapthd , vertical gap thd (<=) for very sure blockiness . unsigned , default = 8
23:16	R/W		reg_dnr_db_vactthd , thd of vact, for block classification . unsigned , default = 10
15: 8	R/W		reg_dnr_db_vgapdifthd , dif thd between vgap and vact. unsigned , default = 4
7: 4	R/W		reserved
3: 2	R/W		reg_dnr_db_vbsmax , max value of vbs for global control. unsigned , default = 2
1: 0	R/W		reg_dnr_db_vgbsthd , gbs thd (>=) for vbs calc. . unsigned , default = 1

Table 9-1057 DNR_DB_YVDELTA_GAIN 0x2d16

Bit(s)	R/W	Default	Description
31:30	R/W		reserved
29:24	R/W		reg_dnr_db_yvdeltaadjgain , gain for adjust Y's vdelta, normalized 32 as "1". unsigned , default = 32
23	R/W		reserved
22:16	R/W		reg_dnr_db_yvdeltaadjoffst , offset for adjust Y's vdelta (-64, 63). signed , default = 0
15:14	R/W		reserved
13: 8	R/W		reg_dnr_db_yvdelta2gain , gain for adjust Y's vdelta2, normalized 64 as "1". unsigned , default = 8
7: 5	R/W		reserved
4: 0	R/W		reg_dnr_db_yvdelta2offst , offset for adjust Y's vdelta2 (-16, 15). signed , default = 0

Table 9-1058 DNR_DB_CVDELTA_GAIN 0x2d17

Bit(s)	R/W	Default	Description
31:30	R/W		reserved
29:24	R/W		reg_dnr_db_cvdeltaadjgain , gain for adjust UV's vdelta, normalized 32 as "1". unsigned , default = 32
23	R/W		reserved
22:16	R/W		reg_dnr_db_cvdeltaadjoffst , offset for adjust UV's vdelta (-64, 63). signed , default = 0
15:14	R/W		reserved

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Bit(s)	R/W	Default	Description
13: 8	R/W		reg_dnr_db_cvdelta2gain , gain for adjust UV's vdelta2, normalized 64 as "1". unsigned , default = 8
7: 5	R/W		reserved
4: 0	R/W		reg_dnr_db_cvdelta2offst , offset for adjust UV's vdelta2 (-16, 15). signed , default = 0

Table 9-1059 DNR_RO_GBS_STAT_LR 0x2d19

Bit(s)	R/W	Default	Description
31: 0	R		ro_gbs_stat_lr . unsigned , default = 0

Table 9-1060 DNR_RO_GBS_STAT_LL 0x2d18

Bit(s)	R/W	Default	Description
31: 0	R		ro_gbs_stat_ll . unsigned , default = 0

Table 9-1061 DNR_RO_GBS_STAT_RR 0x2d1a

Bit(s)	R/W	Default	Description
31: 0	R		ro_gbs_stat_rr . unsigned , default = 0

Table 9-1062 DNR_RO_GBS_STAT_DIF 0x2d1b

Bit(s)	R/W	Default	Description
31: 0	R		ro_gbs_stat_dif . unsigned , default = 0

Table 9-1063 DNR_RO_GBS_STAT_CNT 0x2d1c

Bit(s)	R/W	Default	Description
31: 0	R		ro_gbs_stat_cnt . unsigned , default = 0

Table 9-1064 DNR_RO_HBOF_STAT_CNT_0 0x2d1d

Bit(s)	R/W	Default	Description
31: 0	R		ro_hbof_stat_cnt0 . unsigned , default = 0

Table 9-1065 DNR_RO_HBOF_STAT_CNT_31 0x2d3c

Bit(s)	R/W	Default	Description
31: 0	R		ro_hbof_stat_cnt31 . unsigned , default = 0

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Table 9-1066 DNR_RO_VBOF_STAT_CNT_0 0x2d3d

Bit(s)	R/W	Default	Description
31: 0	R		ro_vbof_stat_cnt0 . unsigned , default = 0

Table 9-1067 DNR_RO_VBOF_STAT_CNT_31 0x2d5c

Bit(s)	R/W	Default	Description
31: 0	R		ro_vbof_stat_cnt31 . unsigned , default = 0

Table 9-1068 DNR_DM_ADP_EN 0x2d5d

Bit(s)	R/W	Default	Description
31:8	R/W		reserved
7	R/W	1	Reg_dnr_scene_change_flag // scence change flag for dnr
6	R/W	1	Reg_dnr_dm_lpf_en // enable lpf fof demosquito filter
5	R/W	1	Reg_dnr_dm_adp_level_en // enable adptive demosquito level
4	R/W	1	Reg_dnr_dm_flag2bdif_en // enable edge flag to blkdif calc
3: 2	R/W	1	Reg_dnr_dm_edgeiir // edge flag iir mode, 0: cur, 1: max(pre,cur), 2,3: choice by org mtn
1	R/W	1	Reg_dnr_dm_dirdifmod // dif mode for direction calc , 0: abs(dif02), 1: (abs(dif01) +abs(dif21))/2
0	R/W	0	Reg_dnr_dm_sur_dir_mod // sure direction mode for cordif calc

Table 9-1069 DNR_DM_EDGE_DIR 0x2d5e

Bit(s)	R/W	Default	Description
31:24	R/W		reserved
23:16	R/W	2	Reg_dnr_dm_dirdifcor // dif coring threshold for direction calc
15:8	R/W	160	Reg_dnr_dm_edgecordifthd // edge flag down when cordif is lager than theshold
7:0	R/W	60	Reg_dnr_dm_mtnrt // motion ration for mtn decision

Table 9-1070 DNR_DM_CTRL 0x2d60

Bit(s)	R/W	Default	Description
31:14	R/W		reserved
13	R/W	1	Reg_dnr_dm_fedgeflag_en, enable edge flag calc. Of each frame
12	R/W	1	Reg_dnr_dm_fedgeflag_cl, clear frame edge flag if needed
11:10	R/W	1	Reg_dnr_dm_fedgeflg_df, user defined edge when fedge_flg_en=0
9	R/W	1	Reg_dnr_dm_en, enable demosquito function
8	R/W	1	Reg_dnr_dm_chrmen, enable chroma proc. For demosquito
7:6	R/W	3	Reg_dnr_dm_level, demosquito level

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Bit(s)	R/W	Default	Description
5:4	R/W	1	Reg_dnr_dm_leveldw0, level down when gbs is small
3:2	R/W	1	Reg_dnr_dm_level_dw1, level down for no edge/flat blocks
1:0	R/W	0	Reg_dnr_dm_gbsthd, small/large threshold for gbs <=

Table 9-1071 DNR_DM_NR_BLND 0x2d61

Bit(s)	R/W	Default	Description
31:25	R/W		reserved
24	R/W	0	reg_dnr_dm_defalpen , 1 to enable user defined alpha for DM/NR blend
23:16	R/W	0	reg_dnr_dm_defalp , user defined alpha for DM/NR blend
15	R/W		reserved
14: 9	R/W	32	reg_dnr_dm_yalpgain , gain for DM/NR alpha, normalized 32 as 1
8: 0	R/W	0	reg_dnr_dm_yalpoffset , offset for DM/NR alpha, singed, (-255, 255)

Table 9-1072 DNR_DM_RNG_THD 0x2d62

Bit(s)	R/W	Default	Description
31:24	R/W		reserved
23:16	R/W	2	reg_dnr_dm_rgnminthd
15: 8	R/W	64	reg_dnr_dm_rgnmaxthd
7: 0	R/W	4	reg_dnr_dm_rgndifthd

Table 9-1073 DNR_DM_RNG_GAIN_OFST 0x2d63

Bit(s)	R/W	Default	Description
31:14	R/W		reserved
13: 8	R/W	16	reg_dnr_dm_rgngain , normalized 16 as 1
7: 0	R/W	0	reg_dnr_dm_rgnofst , unsigned

Table 9-1074 DNR_DM_DIR_MISC 0x2d64

Bit(s)	R/W	Default	Description
31:30	R/W		reserved
29	R/W	1	reg_dnr_dm_diralpen
28:24	R/W	0	reg_dnr_dm_diralpgain
23:22	R/W		reserved
21:16	R/W	0	reg_dnr_dm_diralpofst
15:13	R/W		reserved
12: 8	R/W	0	reg_dnr_dm_diralpmin

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Bit(s)	R/W	Default	Description
7:5	R/W		reserved
4: 0	R/W	31	reg_dnr_dm_diralpmax

Table 9-1075 DNR_DM_COR_DIF 0x2d65

Bit(s)	R/W	Default	Description
31:6	R/W		reserved
5	R/W	1	reg_dnr_dm_cordifprt , enable cordif proctection mode
4:2	R/W	3	reg_dnr_dm_cordifshft
1:0	R/W	3	reg_dnr_dm_cordifmod , 0: use max dir dif as cordif, 1: use max3x3-min3x3 as cordif 2: use min dif as cordif, 3: max's side dif.

Table 9-1076 DNR_DM_FLT_THD 0x2d66

Bit(s)	R/W	Default	Description
31:24	R/W	4	reg_dnr_dm_fltthd00 , block flat threshold0 for block average difference when gbs is small
23:16	R/W	6	reg_dnr_dm_fltthd01 , block flat threshold1 for block average difference when gbs is small
15: 8	R/W	9	reg_dnr_dm_fltthd10 , block flat threshold0 for block average difference when gbs is larger
7: 0	R/W	12	reg_dnr_dm_fltthd11 , block flat threshold1 for block average difference when gbs is larger

Table 9-1077 DNR_DM_VAR_THD 0x2d67

Bit(s)	R/W	Default	Description
31:24	R/W	2	reg_dnr_dm_varthd00 , block variance threshold0 (>=) when gbs is small
23:16	R/W	15	reg_dnr_dm_varthd01 , block variance threshold1 (<=) when gbs is small
15: 8	R/W	3	reg_dnr_dm_varthd10 , block variance threshold0 (>=) when gbs is larger
7: 0	R/W	24	reg_dnr_dm_varthd11 , block variance threshold1 (<=) when gbs is larger

Table 9-1078 DNR_DM_EDGE_DIF_THD 0x2d68

Bit(s)	R/W	Default	Description
31:24	R/W	32	reg_dnr_dm_edgethd0 , block edge threshold (<=) when gbs is small
23:16	R/W	48	reg_dnr_dm_edgethd1 , block edge threshold (<=) when gbs is larger
15: 8	R/W	48	reg_dnr_dm_difthd0 , block dif threshold (<=) when gbs is small
7: 0	R/W	64	reg_dnr_dm_difthd1 , block dif threshold (<=) when gbs is larger

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Table 9-1079 DNR_DM_AVG_THD 0x2d69

Bit(s)	R/W	Default	Description
31:16	R/W		reserved
15: 8	R/W	160	reg_dnr_dm_avgthd0 , block average threshold (>=) when gbs is small
7: 0	R/W	128	reg_dnr_dm_avgthd1 , block average threshold (<=) when gbs is larger

Table 9-1080 DNR_DM_AVG_VAR_DIF_THD 0x2d6a

Bit(s)	R/W	Default	Description
31:16	R/W		reserved
15: 8	R/W	12	reg_dnr_dm_avgdifthd , block average dif threshold(<) between cur and up block for flat block
7: 0	R/W	1	reg_dnr_dm_vardifthd , block variance dif threshold(>=) between cur and up block

Table 9-1081 DNR_DM_EDGE_DIF_THD2 0x2d6b

Bit(s)	R/W	Default	Description
31:24	R/W		reserved
23:16	R/W	24	reg_dnr_dm_varthd2 , block variance threshold (>=) for edge block detect
15: 8	R/W	40	reg_dnr_dm_edgethd2 , block edge threshold (>=)
7: 0	R/W	80	reg_dnr_dm_difthd2 , block dif threshold (>=)

Table 9-1082 DNR_DM_DIF_FLT_MISC 0x2d6c

Bit(s)	R/W	Default	Description
31:28	R/W	0	reg_dnr_dm_ldifoob, pre-defined large dif when pixel out of block
27:24	R/W	0	reg_dnr_dm_bdifoob, pre-defined block dif when pixel out of block
23:16	R/W	200	reg_dnr_dm_fltalp, pre-defined alpha for dm and nr blending when block is flat with mos
15:12	R/W		reserved
11:8	R/W	12	reg_dnr_dm_fltminbdif, pre-defined min block dif for dm filter when block is flat with mos
7	R/W		reserved
6:2	R/W	16	reg_dnr_dm_difnormgain, gain for pixel dif normalization for dm filter.
1	R/W	1	reg_dnr_dm_difnormen , enable pixel dif normalization for dm filter
0	R/W	0	reg_dnr_dm_difupden , enable block dif update using max of left,cur,right difs

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Table 9-1083 DNR_DM_SDIF_LUT0_2 0x2d6d

Bit(s)	R/W	Default	Description
31:21	R/W		reserved
20:16	R/W	16	reg_dnr_dm_sdiflut0, normally 0-16
15:13	R/W		reserved
12:8	R/W	14	reg_dnr_dm_sdiflut1
7:5	R/W		reserved
4:0	R/W	13	reg_dnr_dm_sdiflut2

Table 9-1084 DNR_DM_SDIF_LUT3_5 0x2d6e

Bit(s)	R/W	Default	Description
31:21	R/W		reserved
20:16	R/W	10	reg_dnr_dm_sdiflut3
15:13	R/W		reserved
12:8	R/W	7	reg_dnr_dm_sdiflut4
7:5	R/W		reserved
4:0	R/W	5	reg_dnr_dm_sdiflut5

Table 9-1085 DNR_DM_SDIF_LUT6_8 0x2d6f

Bit(s)	R/W	Default	Description
31:21	R/W		reserved
20:16	R/W	3	reg_dnr_dm_sdiflut6
15:13	R/W		reserved
12:8	R/W	1	reg_dnr_dm_sdiflut7
7:5	R/W		reserved
4:0	R/W	0	reg_dnr_dm_sdiflut8

Table 9-1086 DNR_DM_LDIF_LUT0_2 0x2d70

Bit(s)	R/W	Default	Description
31:21	R/W		reserved
20:16	R/W	0	reg_dnr_dm_ldiflut0
15:13	R/W		reserved
12:8	R/W	4	reg_dnr_dm_ldiflut1
7:5	R/W		reserved
4:0	R/W	12	reg_dnr_dm_ldiflut2

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Table 9-1087 DNR_DM_LDIF_LUT3_5 0x2d71

Bit(s)	R/W	Default	Description
31:21	R/W		reserved
20:16	R/W	14	reg_dnr_dm_ldiflut3
15:13	R/W		reserved
12:8	R/W	15	reg_dnr_dm_ldiflut4
7:5	R/W		reserved
4:0	R/W	16	reg_dnr_dm_ldiflut5

Table 9-1088 DNR_DM_LDIF_LUT6_8 0x2d72

Bit(s)	R/W	Default	Description
31:21	R/W		reserved
20:16	R/W	16	reg_dnr_dm_ldiflut6
15:13	R/W		reserved
12:8	R/W	16	reg_dnr_dm_ldiflut7
7:5	R/W		reserved
4:0	R/W	16	reg_dnr_dm_ldiflut8

Table 9-1089 DNR_DM_DIF2NORM_LUT0_2 0x2d73

Bit(s)	R/W	Default	Description
31:21	R/W		reserved
20:16	R/W	16	reg_dnr_dm_dif2normlut0
15:13	R/W		reserved
12:8	R/W	5	reg_dnr_dm_dif2normlut1
7:5	R/W		reserved
4:0	R/W	3	reg_dnr_dm_dif2normlut2

Table 9-1090 DNR_DM_DIF2NORM_LUT3_5 0x2d74

Bit(s)	R/W	Default	Description
31:21	R/W		reserved
20:16	R/W	2	reg_dnr_dm_dif2normlut3
15:13	R/W		reserved
12:8	R/W	2	reg_dnr_dm_dif2normlut4
7:5	R/W		reserved
4:0	R/W	1	reg_dnr_dm_dif2normlut5

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Table 9-1091 DNR_DM_DIF2NORM_LUT6_8 0x2d75

Bit(s)	R/W	Default	Description
31:21	R/W		reserved
20:16	R/W	1	reg_dnr_dm_dif2normlut6
15:13	R/W		reserved
12:8	R/W	1	reg_dnr_dm_dif2normlut7
7:5	R/W		reserved
4:0	R/W	1	reg_dnr_dm_dif2normlut8

Table 9-1092 DNR_DM_GMS_THD 0x2d76

Bit(s)	R/W	Default	Description
31:16	R/W		reserved
15:8	R/W	0	reg_gms_stat_thd0
7:0	R/W	128	reg_gms_stat_thd1

Table 9-1093 DNR_RO_DM_GMS_STST_CNT 0x2d77

Bit(s)	R/W	Default	Description
31:0	RO		ro_dm_gms_stat_cnt

Table 9-1094 DNR_RO_DM_GMS_STST_MS 0x2d78

Bit(s)	R/W	Default	Description
31:0	RO		ro_dm_gms_stat_ms

Table 9-1095 DNR_DM_EDGE_GAIN 0x2d79

Bit(s)	R/W	Default	Description
31:24	R/W	8	reg_dnr_dm_alpedgegain0 : // unsigned , default = 8 , edge based gain for alpha, normalized 16 as "1"
23:16	R/W	16	reg_dnr_dm_alpedgegain1 : // unsigned , default = 16 , edge based gain for alpha, normalized 16 as "1"
15: 8	R/W	24	reg_dnr_dm_alpedgegain2 : // unsigned , default = 24 , edge based gain for alpha, normalized 16 as "1"
7: 0	R/W	32	reg_dnr_dm_alpedgegain3 : // unsigned , default = 32 , edge based gain for alpha, normalized 16 as "1"

Table 9-1096 DNR_DM_FLG_BDIF 0x2d7a

Bit(s)	R/W	Default	Description
31:24	R/W	0	reg_dnr_dm_flg2bdif0 : // unsigned , default = 0 , (0-16), edge flg to blkdif calc.
23:16	R/W	96	reg_dnr_dm_flg2bdif1 : // unsigned , default = 96 , (0-16), edge flg to blkdif calc.

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Bit(s)	R/W	Default	Description
15: 8	R/W	160	reg_dnr_dm_flg2bdif2 : // unsigned , default = 160 , (0-16), edge flg to blkdif calc.
7: 0	R/W	192	reg_dnr_dm_flg2bdif3 : // unsigned , default = 192 , (0-16), edge flg to blkdif calc.

Table 9-1097 DNR_DM_GBS_RORM 0x2d7b

Bit(s)	R/W	Default	Description
15:12	R/W	0	reg_dnr_dm_gbs4difnorm0 : // unsigned , default = 0 , gbs=0 for dif norm calc.
11: 8	R/W	1	reg_dnr_dm_gbs4difnorm1 : // unsigned , default = 1 , gbs=1 for dif norm calc.
7: 4	R/W	4	reg_dnr_dm_gbs4difnorm2 : // unsigned , default = 4 , gbs=2 for dif norm calc.
3: 0	R/W	6	reg_dnr_dm_gbs4difnorm3 : // unsigned , default = 6 , gbs=3 for dif norm calc.

Table 9-1098 DNR_DM_FLG_LEV 0x2d7c

Bit(s)	R/W	Default	Description
13:12	R/W	1	reg_dnr_dm_flg2lev0 : // unsigned , default = 1 , edge flg to filter level calc.
9: 8	R/W	3	reg_dnr_dm_flg2lev1 : // unsigned , default = 3 , edge flg to filter level calc.
5: 4	R/W	3	reg_dnr_dm_flg2lev2 : // unsigned , default = 3 , edge flg to filter level calc.
1: 0	R/W	3	reg_dnr_dm_flg2lev3 : // unsigned , default = 3 , edge flg to filter level calc.

Table 9-1099 DNR_DM_DIF_FLG_TH 0x2d7d

Bit(s)	R/W	Default	Description
15: 8	R/W	128	reg_dnr_dm_dif2flgthd1 : // unsigned , default = 128 , dif to edge flg threshold 1
7: 0	R/W	192	reg_dnr_dm_dif2flgthd2 : // unsigned , default = 192 , dif to edge flg threshold 2

Table 9-1100 DNR_DM_CALP_GAIN_OFST 0x2d7e

Bit(s)	R/W	Default	Description
21:16	R/W	16	reg_dnr_dm_calpgain : // unsigned , default = 16 , chroma gain for nr/dm alpha, normalized 32 as "1"
8: 0	R/W	-64	reg_dnr_dm_calpoffst : // signed , default = -64 , (-255, 255), chroma offset for nr/dm alpha

Table 9-1101 NR2_POLAR3_MODE 0x2d98

Bit(s)	R/W	Default	Description
19:18	R/W	3	reg_polar3_f02lpf_mod_0 : default = 3 //u2x2: low pass filter mode for field 0 and field2 before polar3 detection; 0 for no lpf, 1: [1 2 1]/4 vert lpf; 2: [1 2 1; 2 4 2; 1 2 1]/16 2d lpf, p1 no hlpf; 2: [1 2 1; 2 4 2; 1 2 1]/16 2d lpf, p1 [1 2 1]/4 hlpf
17:16	R/W	3	reg_polar3_f02lpf_mod_1 : default = 3 //u2x2: low pass filter mode for field 0 and field2 before polar3 detection; 0 for no lpf, 1: [1 2 1]/4 vert lpf; 2: [1 2 1; 2 4 2; 1 2 1]/16 2d lpf, p1 no hlpf; 2: [1 2 1; 2 4 2; 1 2 1]/16 2d lpf, p1 [1 2 1]/4 hlpf

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Bit(s)	R/W	Default	Description
15:8	R/W	5	reg_polar3_dif02_thrd_0 : default = 5 //u8x2: threshold of dif for polar3 detection except for 32 detection, only do polar3 detection on obvious motion, [0] for luma, 1[1] for chroma
7:0	R/W	5	reg_polar3_dif02_thrd_1 : default = 5 //u8x2: threshold of dif for polar3 detection except for 32 detection, only do polar3 detection on obvious motion, [0] for luma, 1[1] for chroma

Table 9-1102 NR2_POLAR3_THRD 0x2d99

Bit(s)	R/W	Default	Description
31:24	R/W	30	reg_polar3_txtf02_thrd_0 : default = 30 //u8x2: threshold to vertical f0f2 texture, if texture larger than this threshold, will not do the polar3 decision.
23:16	R/W	30	reg_polar3_txtf02_thrd_1 : default = 30 //u8x2: threshold to vertical f0f2 texture, if texture larger than this threshold, will not do the polar3 decision.
15:8	R/W	20	reg_polar3_txtf1_thrd_0 : default = 20 //u8x2: threshold to vertical f0f2 texture, if texture larger than this threshold, will not do the polar3 decision.
7:0	R/W	20	reg_polar3_txtf1_thrd_1 : default = 20 //u8x2: threshold to vertical f0f2 texture, if texture larger than this threshold, will not do the polar3 decision.

Table 9-1103 NR2_POLAR3_PARA0 0x2d9a

Bit(s)	R/W	Default	Description
31:28	R/W	6	reg_polar3_rate0_0 : default = 6 //u4x2: delt = rate*dif02/32, e.g. f2<f0, if f1 within((f0+f2)/2 - delt), ((f0+f2)/2 + delt), then polar3_smoothmv++;
27:24	R/W	6	reg_polar3_rate0_1 : default = 6 //u4x2: delt = rate*dif02/32, e.g. f2<f0, if f1 within((f0+f2)/2 - delt), ((f0+f2)/2 + delt), then polar3_smoothmv++;
23:20	R/W	8	reg_polar3_rate1_0 : default = 8 //u4x2: delt = rate*dif02/32, e.g. f2<f0, if f1< ((f0+f2)/2 - delt), then polar3_m1++; if f1>((f0+f2)/2 + delt), then polar3_p1++;
19:16	R/W	8	reg_polar3_rate1_1 : default = 8 //u4x2: delt = rate*dif02/32, e.g. f2<f0, if f1< ((f0+f2)/2 - delt), then polar3_m1++; if f1>((f0+f2)/2 + delt), then polar3_p1++;
15:12	R/W	2	reg_polar3_rate2_0 : default = 2 //u4x2: delt = rate*dif02/32, e.g. f2<f0, if f1< (f2 - delt- ofset2), then polar3_m2++; if f1>((f0 + delt+ ofset2), then polar3_p2++;
11:8	R/W	2	reg_polar3_rate2_1 : default = 2 //u4x2: delt = rate*dif02/32, e.g. f2<f0, if f1< (f2 - delt- ofset2), then polar3_m2++; if f1>((f0 + delt+ ofset2), then polar3_p2++;
7:4	R/W	1	reg_polar3_ofst1_0 : default = 1 //s4x2: delt = rate*dif02/32, e.g. f2<f0, if f1< (f2 - delt- ofset2), then polar3_m2++; if f1>((f0 + delt+ ofset2), then polar3_p2++;
3:0	R/W	1	reg_polar3_ofst1_1 : default = 1 //s4x2: delt = rate*dif02/32, e.g. f2<f0, if f1< (f2 - delt- ofset2), then polar3_m2++; if f1>((f0 + delt+ ofset2), then polar3_p2++;

Table 9-1104 NR2_POLAR3_PARA1 0x2d9b

Bit(s)	R/W	Default	Description
31:24	R/W	48	reg_polar3_rate3_0 : default = 48 //u8x2: delt = rate*dif02/32, e.g. f2<f0, if f1<(f2 - delt- ofset3) or f1>((f0 + delt+ofst3), then polar3_32++;
23:16	R/W	48	reg_polar3_rate3_1 : default = 48 //u8x2: delt = rate*dif02/32, e.g. f2<f0, if f1<(f2 - delt- ofset3) or f1>((f0 + delt+ofst3), then polar3_32++;

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Bit(s)	R/W	Default	Description
15:12	R/W	2	reg_polar3_ofst3_0 : default = 2 //s4x2: delt = rate*dif02/32, e.g. f2<f0, if f1< (f2 - delt-ofst3) or f1>((f0 + delt+ofst3), then polar3_32++;
11:8	R/W	2	reg_polar3_ofst3_1 : default = 2 //s4x2: delt = rate*dif02/32, e.g. f2<f0, if f1< (f2 - delt-ofst3) or f1>((f0 + delt+ofst3), then polar3_32++;
7:4	R/W	2	reg_polar3_ofst2_0 : default = 2 //s4x2: delt = rate*dif02/32, e.g. f2<f0, if f1< (f2 - delt- ofset2), then polar3_m2++; if f1>((f0 + delt+ ofset2), then polar3_p2++;
3:0	R/W	2	reg_polar3_ofst2_1 : default = 2 //s4x2: delt = rate*dif02/32, e.g. f2<f0, if f1< (f2 - delt- ofset2), then polar3_m2++; if f1>((f0 + delt+ ofset2), then polar3_p2++;

Table 9-1105 NR2_POLAR3_CTRL 0x2d9c

Bit(s)	R/W	Default	Description
16	R.O	0	reg_polar3_ro_reset : default = 0 //u1: reset signal of the polar3 read only registers
15:8	R/W	10	reg_polar3_h_mute : default = 10 //u8: horizontally pixels to mute for left right sides for polar3 detection;
7:0	R/W	10	reg_polar3_v_mute : default = 10 //u8: horizontally pixels to mute for top and bottom sides for polar3 detection;

Table 9-1106 NR2_RO_POLAR3_NUMOFPIX 0x2d9d

Bit(s)	R/W	Default	Description
23:0	R.O	0	ro_polar3_numofpix : default = 0 //u24, number of pixels detected as polar3

Table 9-1107 NR2_RO_POLAR3_SMOOTHMV 0x2d9e

Bit(s)	R/W	Default	Description
23:0	R.O	0	ro_polar3_smoothmv : default = 0 //u24, number of pixels with smooth mv, F(t) is close between avg of f(t-1) and f(t+1);

Table 9-1108 NR2_RO_POLAR3_M1 0x2d9f

Bit(s)	R/W	Default	Description
23:0	R.O	0	ro_polar3_m1 : default = 0 //u24, number of pixels with F(t) is close to f(t-1) instead of f(t+1), but in between [f(t-1), f(t+1)];

Table 9-1109 NR2_RO_POLAR3_P1 0x2da0

Bit(s)	R/W	Default	Description
23:0	R.O	0	ro_polar3_p1 : default = 0 //u24, number of pixels with F(t) is close to f(t+1) instead of f(t-1), but in between [f(t-1), f(t+1)];

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Table 9-1110 NR2_RO_POLAR3_M2 0x2da1

Bit(s)	R/W	Default	Description
23:0	R.O	0	ro_polar3_m2 : default = 0 //u24, number of pixels with F(t) is close to f(t-1) instead of f(t+1), but out side of (f(t-1), f(t+1));

Table 9-1111 NR2_RO_POLAR3_P2 0x2da2

Bit(s)	R/W	Default	Description
23:0	R.O	0	ro_polar3_p2 : default = 0 //u24, number of pixels with F(t) is close to f(t+1) instead of f(t-1), but out side of (f(t-1), f(t+1));

Table 9-1112 NR2_RO_POLAR3_32 0x2da3

Bit(s)	R/W	Default	Description
23:0	R.O	0	ro_polar3_32 : default = 0 //u24, number of pixels with F(t) far from [f(t-1),f(t+1)] and f(t-1) is close to f(t+1);

Table 9-1113 NR4_DRT_CTRL 0x2da4

Bit(s)	R/W	Default	Description
31:24	R/W	16	reg_nr4_ydrt_3line_ssd_gain : // unsigned , default = 16 gain to max ssd normalized 16 as '1'
23:16	R/W	16	reg_nr4_ydrt_5line_ssd_gain : // unsigned , default = 16 gain to max ssd normalized 16 as '1'
14:13	R/W	1	reg_nr4_drt_yhsad_mode : // unsigned , default = 1 mode for luma horiztonal sad calc., 0: no vertical lpf, 1: vertical [1 2 1], 2 or 3: vertical [1 2 2 2 1] if 5 lines
12:11	R/W	1	reg_nr4_drt_chsad_mode : // unsigned , default = 1 mode for chroma horiztonal sad calc., 0: no vertical lpf, 1: vertical [1 2 1], 2 or 3: vertical [1 2 2 2 1] if 5 lines
10	R/W	1	reg_nr4_drt_yhsad_hlpf : // unsigned , default = 1 hlpf for luma hsad of drt calculation, 0: no lpf, 1: with [1 2 1] hlpf
9	R/W	1	reg_nr4_drt_yvsad_hlpf : // unsigned , default = 1 hlpf for luma vsad of drt calculation, 0: no lpf, 1: with [1 2 1] hlpf
8	R/W	1	reg_nr4_drt_ydsad_hlpf : // unsigned , default = 1 hlpf for luma dsad of drt calculation, 0: no lpf, 1: with [1 2 1] hlpf
7	R/W	1	reg_nr4_drt_chsad_hlpf : // unsigned , default = 1 hlpf for chrome hsad of drt calculation, 0: no lpf, 1: with [1 2 1] hlpf
6	R/W	1	reg_nr4_drt_cvsad_hlpf : // unsigned , default = 1 hlpf for chroma vsad of drt calculation, 0: no lpf, 1: with [1 2 1] hlpf
5	R/W	1	reg_nr4_drt_cdsad_hlpf : // unsigned , default = 1 hlpf for chroma dsad of drt calculation, 0: no lpf, 1: with [1 2 1] hlpf
4	R/W	1	reg_nr4_ydrt_dif_mode : // unsigned , default = 1 0:y_dif, 1: y_dif + (u_dif + v_dif)/2
3: 2	R/W	2	reg_nr4_cdrt_dif_mode : // unsigned , default = 2 0:(u_dif + v_dif), 1: y_dif/4 + (u_dif + v_dif)*3/4, 2:y_dif/2 + (u_dif + v_dif)/2, 3: y_dif (not recommended)
1:0	R/W		reserved

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Table 9-1114 NR4_DRT_YSAD_GAIN 0x2da5

Bit(s)	R/W	Default	Description
31:24	R/W	16	reg_nr4_ysad_hrz_gain : // unsigned , default = 16 gain for horizontal sad, 16 normalized to "1"
23:16	R/W	20	reg_nr4_ysad_diag_gain : // unsigned , default = 20 gain for diagonal sad, 16 normalized to "1"
15: 8	R/W	16	reg_nr4_ysad_vrt_gain : // unsigned , default = 16 gain for vertical sad, 16 normalized to "1"
5: 0	R/W	6	reg_nr4_drt_ysad_core_rate : // unsigned , default = 6 rate of coring for sad(theta) - sad(theta+pi/2)*rate/64

Table 9-1115 NR4_DRT_CSAD_GAIN 0x2da6

Bit(s)	R/W	Default	Description
31:24	R/W	16	reg_nr4_csad_hrz_gain : // unsigned , default = 16 gain for horizontal sad, 16 normalized to "1"
23:16	R/W	20	reg_nr4_csad_diag_gain : // unsigned , default = 20 gain for diagonal sad, 16 normalized to "1"
15: 8	R/W	16	reg_nr4_csad_vrt_gain : // unsigned , default = 16 gain for vertical sad, 16 normalized to "1"
5: 0	R/W	6	reg_nr4_drt_csad_core_rate : // unsigned , default = 6 rate of coring for sad(theta) - sad(theta+pi/2)*rate/64

Table 9-1116 NR4_DRT_SAD_ALP_CORE 0x2da7

Bit(s)	R/W	Default	Description
23:20	R/W	0	reg_nr4_ydrt_alp_core_rate : // unsigned , default = 0 luma ratio to min_err, alpha = (min_err - (max_err - min_err)*rate + ofst)/max_err * 64; dft = 0/32
19:16	R/W	0	reg_nr4_cdrt_alp_core_rate : // unsigned , default = 0 chroma ratio to min_err, alpha = (min_err - (max_err - min_err)*rate + ofst)/max_err * 64; dft = 0/32
13: 8	R/W	10	reg_nr4_ydrt_alp_core_ofst : // unsigned , default = 10 luma offset to min_err, alpha = (min_err - (max_err - min_err)*rate + ofst)/max_err * 64; dft = 10
5: 0	R/W	10	reg_nr4_cdrt_alp_core_ofst : // unsigned , default = 10 chroma offset to min_err, alpha = (min_err - (max_err - min_err)*rate + ofst)/max_err * 64; dft = 10

Table 9-1117 NR4_DRT_ALP_MINMAX 0x2da8

Bit(s)	R/W	Default	Description
29:24	R/W	0	reg_nr4_ydrt_alp_min : // unsigned , default = 0 luma min value of alpha, dft = 0
21:16	R/W	63	reg_nr4_ydrt_alp_max : // unsigned , default = 63 luma max value of alpha, dft = 63
13: 8	R/W	0	reg_nr4_cdrt_alp_min : // unsigned , default = 0 chroma min value of alpha, dft = 0
5: 0	R/W	63	reg_nr4_cdrt_alp_max : // unsigned , default = 63 chroma max value of alpha, dft = 63

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Table 9-1118 NR4_SNR_CTRL_REG 0x2da9

Bit(s)	R/W	Default	Description
12	R/W	1	reg_nr4_bet2_sel : // unsigned , default = 1
11: 9	R/W	0	reg_nr4_snr2_sel_mode : // unsigned , default = 0 0: no filter, 1: adpgau, adp_ drt_lpf blend; 2: adpgau, drt4_lpf blend; 3: adp_drt_lpf method, 4: drt4_lpf method, 5: adp_drt_ //original image blend, 6: drt4_lpf, original image blend, 7: adpgau method; dft=1
8	R/W	1	reg_nr4_snr2_gaulpf_mode : // unsigned , default = 1 0: 3*5 or 5*5 gaussian lpf; 1: 3*3 (window size) gaussian lpf; dft=1
7: 6	R/W	3	reg_nr4_snr2_alpha0_sad_mode : // unsigned , default = 3 0: max_sad*max_ ssd; 1: max_sad*max_sad; 2: adp_max_sad*max_ssd; 3: adp_max_sad*adp_ max_sad dft=3
5: 4	R/W	2	reg_nr4_snr2_alpha1_sad_mode : // unsigned , default = 2 0: max_sad; 1: cross_max_sad; 2 or 3: adp_sad dft=2
1: 0	R/W	3	reg_nr4_snr2_adp_drtlpf_mode : // unsigned , default = 3 0: adp_drtlpf [2 1 1]/4, 1: adp_drtlpf [4 2 1 1]/8; 2: adp_drtlpf [2 2 2 1 1]/8; 3: adp_drtlpf [7 7 7 6 5]/32; dft=3;

Table 9-1119 NR4_SNR_ALPHA0_MAX_MIN 0x2daa

Bit(s)	R/W	Default	Description
29:23	R/W	127	reg_nr4_snr2_alp0_ymin : // unsigned , default = 127 normalized to 128 as '1'
22:16	R/W	127	reg_nr4_snr2_alp0_ymax : // unsigned , default = 127 normalized to 128 as '1'
13: 7	R/W	127	reg_nr4_snr2_alp0_cmin : // unsigned , default = 127 normalized to 128 as '1'
6: 0	R/W	127	reg_nr4_snr2_alp0_cmax : // unsigned , default = 127 normalized to 128 as '1'

Table 9-1120 NR4_ALP0C_ERR2CURV_LIMIT0 0x2dab

Bit(s)	R/W	Default	Description
31:24	R/W	0	reg_nr4_snr2_alp0_minerr_cpar0 : // unsigned , default = 0 threshold0 of curve to map mierr to alp0 for chroma channel, this will be set value of flat region mierr that no need blur.
23:16	R/W	25	reg_nr4_snr2_alp0_minerr_cpar1 : // unsigned , default = 25 threshold1 of curve to map mierr to alp0 for chroma channel,this will be set value of texture region mierr that can not blur.
15: 8	R/W	40	reg_nr4_snr2_alp0_minerr_cpar5 : // unsigned , default = 40 rate0 (for mierr<th0) of curve to map mierr to alp0 for chroma channel. the larger of the value, the deep of the slope. 0~255.
7: 0	R/W	40	reg_nr4_snr2_alp0_minerr_cpar6 : // unsigned , default = 40 rate1 (for mierr>th1) of curve to map mierr to alp0 for chroma channel. the larger of the value, the deep of the slope. 0~255.

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Table 9-1121 NR4_ALP0C_ERR2CURV_LIMIT1 0x2dac

Bit(s)	R/W	Default	Description
23:16	R/W	127	reg_nr4_snr2_alp0_minerr_cpar2 : // unsigned , default = 127 level limit(for mierr<th0) of curve to map mierr to alp0 for chroma channel, that we can do for flat region. 0~255.
15: 8	R/W	0	reg_nr4_snr2_alp0_minerr_cpar3 : // unsigned , default = 0 level limit(for th0<mierr<th1) of curve to map mierr to alp0 for chroma channel, that we can do for misc region. 0~255.
7: 0	R/W	127	reg_nr4_snr2_alp0_minerr_cpar4 : // unsigned , default = 127 level limit(for mierr>th1) of curve to map mierr to alp0 for chroma channel, that we can do for texture region. 0~255.

Table 9-1122 NR4_ALP0Y_ERR2CURV_LIMIT0 0x2dad

Bit(s)	R/W	Default	Description
31:24	R/W	0	reg_nr4_snr2_alp0_minerr_ypar0 : // unsigned , default = 0 threshold0 of curve to map mierr to alp0 for luma channel, this will be set value of flat region mierr that no need blur. 0~255.
23:16	R/W	25	reg_nr4_snr2_alp0_minerr_ypar1 : // unsigned , default = 25 threshold1 of curve to map mierr to alp0 for luma channel,this will be set value of texture region mierr that can not blur.
15: 8	R/W	40	reg_nr4_snr2_alp0_minerr_ypar5 : // unsigned , default = 40 rate0 (for mierr<th0) of curve to map mierr to alp0 for luma channel. the larger of the value, the deep of the slope. 0~255.
7: 0	R/W	40	reg_nr4_snr2_alp0_minerr_ypar6 : // unsigned , default = 40 rate1 (for mierr>th1) of curve to map mierr to alp0 for luma channel. the larger of the value, the deep of the slope. 0~255.

Table 9-1123 NR4_ALP0Y_ERR2CURV_LIMIT1 0x2dae

Bit(s)	R/W	Default	Description
23:16	R/W	127	reg_nr4_snr2_alp0_minerr_ypar2 : // unsigned , default = 127 level limit(for mierr < th0) of curve to map mierr to alp0 for luma channel, set to alp0 that we can do for flat region. 0~255.
15: 8	R/W	0	reg_nr4_snr2_alp0_minerr_ypar3 : // unsigned , default = 0 level limit(for th0<mierr < th1) of curve to map mierr to alp0 for luma channel, alp0 that we can do for misc region. 0~255.
7: 0	R/W	127	reg_nr4_snr2_alp0_minerr_ypar4 : // unsigned , default = 127 level limit(for mierr > th1) of curve to map mierr to alp0 for luma channel, alp0 that we can do for texture region. 0~255.

Table 9-1124 NR4_SNR_ALPA1_RATE_AND_OFST 0x2daf

Bit(s)	R/W	Default	Description
23:18	R/W	0	reg_nr4_snr2_alp1_ycore_rate : // unsigned , default = 0 normalized 64 as "1"
17:12	R/W	0	reg_nr4_snr2_alp1_ccore_rate : // unsigned , default = 0 normalized 64 as "1"
11: 6	R/W	3	reg_nr4_snr2_alp1_ycore_ofst : // signed , default = 3 normalized 64 as "1"
5: 0	R/W	3	reg_nr4_snr2_alp1_ccore_ofst : // signed , default = 3 normalized 64 as "1"

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Table 9-1125 NR4_SNR_ALPHA1_MAX_MIN 0x2db0

Bit(s)	R/W	Default	Description
23:18	R/W	0	reg_nr4_snr2_alp1_ymin : // unsigned , default = 0 normalized to 64 as '1'
17:12	R/W	63	reg_nr4_snr2_alp1_ymax : // unsigned , default = 63 normalized to 64 as '1'
11: 6	R/W	0	reg_nr4_snr2_alp1_cmin : // unsigned , default = 0 normalized to 64 as '1'
5: 0	R/W	63	reg_nr4_snr2_alp1_cmax : // unsigned , default = 63 normalized to 64 as '1'

Table 9-1126 NR4_ALP1C_ERR2CURV_LIMIT0 0x2db1

Bit(s)	R/W	Default	Description
31:24	R/W	0	reg_nr4_snr2_alp1_minerr_cpar0 : // unsigned , default = 0 annel, this will be set value of flat region mierr that no need directional NR. 0~255.
23:16	R/W	24	reg_nr4_snr2_alp1_minerr_cpar1 : // unsigned , default = 24 hannel,this will be set value of texture region mierr that can not do directional NR. 0~255.
15: 8	R/W	0	reg_nr4_snr2_alp1_minerr_cpar5 : // unsigned , default = 0 a/chroma channel. the larger of the value, the deep of the slope.
7: 0	R/W	20	reg_nr4_snr2_alp1_minerr_cpar6 : // unsigned , default = 20 a/chroma channel. the larger of the value, the deep of the slope. 0~255

Table 9-1127 NR4_ALP1C_ERR2CURV_LIMIT1 0x2db2

Bit(s)	R/W	Default	Description
23:16	R/W	0	reg_nr4_snr2_alp1_minerr_cpar2 : // unsigned , default = 0 will be set to alp1 that we can do for flat region. 0~255.
15: 8	R/W	16	reg_nr4_snr2_alp1_minerr_cpar3 : // unsigned , default = 16 this will be set to alp1 that we can do for misc region. 0~255.
7: 0	R/W	63	reg_nr4_snr2_alp1_minerr_cpar4 : // unsigned , default = 63 will be set to alp1 that we can do for texture region. 0~255.255 before

Table 9-1128 NR4_ALP1Y_ERR2CURV_LIMIT0 0x2db3

Bit(s)	R/W	Default	Description
31:24	R/W	0	reg_nr4_snr2_alp1_minerr_ypar0 : // unsigned , default = 0 thra/chroma channel, this will be set value of flat region mierr that no need directional NR. 0~255.
23:16	R/W	24	reg_nr4_snr2_alp1_minerr_ypar1 : // unsigned , default = 24 thra/chroma channel,this will be set value of texture region mierr that can not do directional NR. 0~255.
15: 8	R/W	0	reg_nr4_snr2_alp1_minerr_ypar5 : // unsigned , default = 0 ratlp1 for luma/chroma channel. the larger of the value, the deep of the slope.
7: 0	R/W	20	reg_nr4_snr2_alp1_minerr_ypar6 : // unsigned , default = 20 ratlp1 for luma/chroma channel. the larger of the value, the deep of the slope. 0~255

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Table 9-1129 NR4_ALP1Y_ERR2CURV_LIMIT1 0x2db4

Bit(s)	R/W	Default	Description
23:16	R/W	0	reg_nr4_snr2_alp1_minerr_ypar2 : // unsigned , default = 0 lev to alp1 for luma/chroma channel, this will be set to alp1 that we can do for flat region. 0~255.
15: 8	R/W	16	reg_nr4_snr2_alp1_minerr_ypar3 : // unsigned , default = 16 levierr to alp1 for luma/chroma channel, this will be set to alp1 that we can do for misc region. 0~255.
7: 0	R/W	63	reg_nr4_snr2_alp1_minerr_ypar4 : // unsigned , default = 63 lev to alp1 for luma/chroma channel, this will be set to alp1 that we can do for texture region. 0~255.255 before

Table 9-1130 NR4_MTN_CTRL 0x2db5

Bit(s)	R/W	Default	Description
1	R/W	1	reg_nr4_mtn_ref_en : // unsigned , default = 1 enable motion refinement, dft = 1
0	R/W	0	reg_nr4_mtn_ref_bet_sel : // unsigned , default = 0 beta selection mode for motion refinement, 0: beta1, 1: beta2, dft = 0

Table 9-1131 NR4_MTN_REF_PAR0 0x2db6

Bit(s)	R/W	Default	Description
31:24	R/W	24	reg_nr4_mtn_ref_par0 : // unsigned , default = 24 par0 for beta to gain, dft =
23:16	R/W	60	reg_nr4_mtn_ref_par1 : // unsigned , default = 60 par1 for beta to gain, dft =
15: 8	R/W	4	reg_nr4_mtn_ref_par2 : // unsigned , default = 4 par2 for beta to gain, dft =
7: 0	R/W	32	reg_nr4_mtn_ref_par3 : // unsigned , default = 32 par3 for beta to gain, dft =

Table 9-1132 NR4_MTN_REF_PAR1 0x2db7

Bit(s)	R/W	Default	Description
23:16	R/W	128	reg_nr4_mtn_ref_par4 : // unsigned , default = 128 par4 for beta to gain, dft =
15: 8	R/W	40	reg_nr4_mtn_ref_par5 : // unsigned , default = 40 par5 for beta to gain, dft =
7: 0	R/W	20	reg_nr4_mtn_ref_par6 : // unsigned , default = 20 par6 for beta to gain, dft =

Table 9-1133 NR4_MCNR_LUMA_ENH_CTRL 0x2db8

Bit(s)	R/W	Default	Description
3	R/W	1	reg_nr4_luma_plus_en : // unsigned , default = 1 enable luma enhancement, dft = 1
2	R/W	1	reg_nr4_luma_plus_wt_mode : // unsigned , default = 1 luma weight calc mode, 0:sqrt(1+x^2), 1: 1+abs(x), dft = 0
1: 0	R/W	1	reg_nr4_luma_plus_orient_mode : // unsigned , default = 1 0: only use previous orient for pre and cur luma plus, 1: 0: only use current orient for pre and cur luma plus

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Table 9-1134 NR4_MCNR_LUMA_STAT_LIMTX 0x2db9

Bit(s)	R/W	Default	Description
29:16	R/W	8	reg_nr4_luma_plus_xst : // unsigned , default = 8 start for luma plus statistic, dft = 8
13: 0	R/W	711	reg_nr4_luma_plus_xed : // unsigned , default = 711 end for luma plus statistic, dft = HSIZE-8-1;

Table 9-1135 NR4_MCNR_LUMA_STAT_LIMTY 0x2dba

Bit(s)	R/W	Default	Description
29:16	R/W	8	reg_nr4_luma_plus_yst : // unsigned , default = 8 start for luma plus statistic, dft = 8
13: 0	R/W	231	reg_nr4_luma_plus_yed : // unsigned , default = 231 end for luma plus statistic, dft = VSIZE-8-1

Table 9-1136 NR4_MCNR_LUMA_DIF_CALC 0x2dbb

Bit(s)	R/W	Default	Description
29:24	R/W	8	reg_nr4_luma_plus_ugain : // unsigned , default = 8 U's gain for luma enhancement, 16 normalized as '1'
21:16	R/W	8	reg_nr4_luma_plus_vgain : // unsigned , default = 8 V's gain for luma enhancement, 16 normalized as '1'
15: 8	R/W	2	reg_nr4_luma_plus_ycor_thd : // unsigned , default = 2 Y coring threshold for difference calc., dft = 0
7: 0	R/W	0	reg_nr4_luma_plus_ccor_thd : // unsigned , default = 0 C coring threshold for difference calc., dft = 0

Table 9-1137 NR4_MCNR_LUMAPRE_CAL_PRAM 0x2dbc

Bit(s)	R/W	Default	Description
25:24	R/W	0	reg_nr4_pre_u_orient : // signed , default = 0 orientation of previous U, initial to 0, and will be updated by software
17:16	R/W	0	reg_nr4_pre_v_orient : // signed , default = 0 orientation of previous V, initial to 0, and will be updated by software
15: 8	R/W	0	reg_nr4_pre_u_mean : // unsigned , default = 0 mean of previous U, initial to 0, and will be updated by software
7: 0	R/W	0	reg_nr4_pre_v_mean : // unsigned , default = 0 mean of previousV, initial to 0, and will be updated by software

Table 9-1138 NR4_MCNR_LUMACUR_CAL_PRAM 0x2dbd

Bit(s)	R/W	Default	Description
25:24	R/W	0	reg_nr4_cur_u_orient : // signed , default = 0 orientation of current U, initial to 0, and will be updated by software
17:16	R/W	0	reg_nr4_cur_v_orient : // signed , default = 0 orientation of current V, initial to 0, and will be updated by software

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Bit(s)	R/W	Default	Description
15: 8	R/W	0	reg_nr4_cur_u_mean : // unsigned , default = 0 mean of current U, initial to 0, and will be updated by software
7: 0	R/W	0	reg_nr4_cur_v_mean : // unsigned , default = 0 mean of current, initial to 0, and will be updated by software

Table 9-1139 NR4_MCNR_MV_CTRL_REG 0x2dbe

Bit(s)	R/W	Default	Description
13:12	R/W	2	reg_nr4_sad_bitw : // unsigned , default = 2 sad bit width (8 + x) before clip to u8, dft = 1
11: 4	R/W	64	reg_nr4_glb_gain : // unsigned , default = 64 global gain calc. by software, 64 is normalized as '1'
3: 0	R/W	8	reg_nr4_mv_err_rsft : // unsigned , default = 8 right shift for mv err calc., dft = 9

Table 9-1140 NR4_MCNR_MV_GAIN0 0x2dbf

Bit(s)	R/W	Default	Description
31:28	R/W	1	reg_nr4_lftmvx_gain : // unsigned , default = 1 left mvx gain for err calc., dft = 1
27:24	R/W	1	reg_nr4_lftmvy_gain : // unsigned , default = 1 left mvy gain for err calc., dft = 1
23:20	R/W	5	reg_nr4_zmvx_gain : // unsigned , default = 5 zero mvx gain for err calc., dft = 2
19:16	R/W	5	reg_nr4_zmvy_gain : // unsigned , default = 5 zero mvy gain for err calc., dft = 4
15:12	R/W	2	reg_nr4_lmvx0_gain : // unsigned , default = 2 line mvx0 gain for err calc., dft = 1
11: 8	R/W	2	reg_nr4_lmvx1_gain : // unsigned , default = 2 line mvx1 gain for err calc., dft = 1
7: 4	R/W	2	reg_nr4_lmvy0_gain : // unsigned , default = 2 line mvy0 gain for err calc., dft = 1
3: 0	R/W	2	reg_nr4_lmvy1_gain : // unsigned , default = 2 line mvy1 gain for err calc., dft = 1

Table 9-1141 NR4_MCNR_LMV_PARM 0x2dc0

Bit(s)	R/W	Default	Description
31:28	R/W	3	reg_nr4_lmv_rt0 : // unsigned , default = 3 ratio of max lmv
27:24	R/W	3	reg_nr4_lmv_rt1 : // unsigned , default = 3 ratio of second max lmv
21:16	R/W	16	reg_nr4_lmv_num_lmt0 : // unsigned , default = 16 lmv0 least/limit number of (total number - zero_bin)
13: 8	R/W	8	reg_nr4_lmv_num_lmt1 : // unsigned , default = 8 lmv1 least/limit number of (total number - zero_bin - max0)
1: 0	R/W	1	reg_nr4_max_sad_rng : // unsigned , default = 1 search range of max2 sad in small region, dft = 1

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Table 9-1142 NR4_MCNR_ALP0_REG 0x2dc1

Bit(s)	R/W	Default	Description
25	R/W	1	reg_nr4_alp0_fail_chk : // unsigned , default = 1 enable check for alp0 fail status
24	R/W	1	reg_nr4_bet0_coef_ref_en : // unsigned , default = 1 bet1 refinement by coef_blt
23:16	R/W	255	reg_nr4_alp0_posad_gain : // unsigned , default = 255 the sad (norm) gain for pixel pointed by MV;
9: 8	R/W	0	reg_nr4_alp0_norm_mode : // unsigned , default = 0 alp0 select sad norm mode, 0: disable, 1: enable dc norm, 2: enable ac norm, 3: enable both (dc/ac) norm, dft = 3
5: 0	R/W	16	reg_nr4_alp0_norm_gain : // unsigned , default = 16 alp0 gain for sad norm, '32' as '1', dft = 1

Table 9-1143 NR4_MCNR_ALP1_AND_BET0_REG 0x2dc2

Bit(s)	R/W	Default	Description
25:24	R/W	3	reg_nr4_alp1_norm_mode : // unsigned , default = 3 alp1 select sad norm mode, 0: disable, 1: enable dc norm, 2: enable ac norm, 3: enable both (dc/ac) norm, dft = 3
21:16	R/W	3	reg_nr4_alp1_norm_gain : // unsigned , default = 3 alp1 gain for sad norm, '32' as '1', dft = 1
9: 8	R/W	3	reg_nr4_bet0_norm_mode : // unsigned , default = 3 bet0 select sad norm mode, 0: disable, 1: enable dc norm, 2: enable ac norm, 3: enable both (dc/ac) norm, dft = 3
5: 0	R/W	8	reg_nr4_bet0_norm_gain : // unsigned , default = 8 bet0 gain for sad norm, '32' as '1', dft = 1

Table 9-1144 NR4_MCNR_BET1_AND_BET2_REG 0x2dc3

Bit(s)	R/W	Default	Description
25:24	R/W	3	reg_nr4_bet1_norm_mode : // unsigned , default = 3 bet1 select sad norm mode, 0: disable, 1: enable dc norm, 2: enable ac norm, 3: enable both (dc/ac) norm, dft = 3
21:16	R/W	8	reg_nr4_bet1_norm_gain : // unsigned , default = 8 bet1 gain for sad norm, '32' as '1', dft = 1
9: 8	R/W	0	reg_nr4_bet2_norm_mode : // unsigned , default = 0 bet2 select sad norm mode, 0: disable, 1: enable dc norm, 2: enable ac norm, 3: enable both (dc/ac) norm, dft = 3
5: 0	R/W	16	reg_nr4_bet2_norm_gain : // unsigned , default = 16 bet2 gain for sad norm, '32' as '1', dft = 1

Table 9-1145 NR4_MCNR_AC_DC_CRTL 0x2dc4

Bit(s)	R/W	Default	Description
11	R/W	1	reg_nr4_dc_mode : // unsigned , default = 1 mode for dc selection,0: Y_lpf, 1: Y_lpf + (U_Lpf+V_lpf)/2,
10	R/W	1	reg_nr4_ac_mode : // unsigned , default = 1 mode for ac selection, 0: Y_abs_dif, 1: Y_abs_dif + (U_abs_dif + V_abs_dif)/2
9	R/W	0	reg_nr4_dc_sel : // unsigned , default = 0 selection mode for dc value, 0: 3x5, 1: 5x5, dft = 1

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Bit(s)	R/W	Default	Description
8	R/W	0	reg_nr4_ac_sel : // unsigned , default = 0 selection mode for ac value, 0: 3x5, 1: 5x5, dft = 1
6: 4	R/W	2	reg_nr4_dc_shft : // unsigned , default = 2 right shift for dc value, dft = 2
2: 0	R/W	0	reg_nr4_ac_shft : // unsigned , default = 0 right shift for ac value, dft = 2

Table 9-1146 NR4_MCNR_CM_CTRL0 0x2dc5

Bit(s)	R/W	Default	Description
28	R/W	0	reg_nr4_cm_skin_prc_bet0 : // unsigned , default = 0 enable skin tone processing for mcnr bet0 calc., dft = 1
27:26	R/W	1	reg_nr4_cm_chrm_sel : // unsigned , default = 1 chrome selection for color match, 0: 1x1, 1: 3X3LPF, 2: 3x5LPF, 3: 5x5LPF for 5lines, 3x5LPF for 3lines, dft = 3
25:24	R/W	1	reg_nr4_cm_luma_sel : // unsigned , default = 1 luma selection for color match, 0: 1x1, 1: 3X3LPF, 2: 3x5LPF, 3: 5x5LPF for 5lines, 3x5LPF for 3lines, dft = 3
23:21	R/W	3	reg_nr4_cm_skin_rshft_bet0 : // unsigned , default = 3 right shift for bet0's skin color gains, dft = 3
20	R/W	1	reg_nr4_cm_var_sel : // unsigned , default = 1 variation selection for color match, 0: 3x5, 1: 5x5 for 5lines, 3x5 for 3lines, dft = 1
19	R/W	1	reg_nr4_cm_green_prc_bet0 : // unsigned , default = 1 enable green processing for mcnr bet0 calc., dft = 1
18:16	R/W	4	reg_nr4_cm_green_rshft_bet0 : // unsigned , default = 4 right shift for bet0's green color gains, dft = 4
15:14	R/W	2	reg_nr4_preflt_mod : // unsigned , default = 2 pre filter mode in mcnr, 0: mv pointed pixel, 1: bilater filter
13:12	R/W	1	reg_nr4_alp1_mode : // unsigned , default = 1 mode for alpha1's sad selection, 0: max sad, 1: three min sads, 2: min sad, 3: co sad
9: 8	R/W	0	reg_nr4_bet0_mode : // unsigned , default = 0 mode for bet0's sad selection, 0: max sad, 1: three min sads, 2: min sad, 3: co sad, else: (co sad) - (min sad)
5: 4	R/W	2	reg_nr4_bet1_mode : // unsigned , default = 2 mode for bet1's sad selection, 0: max sad, 1: three min sads, 2: min sad, 3: co sad, else: (co sad) - (min sad)
1: 0	R/W	1	reg_nr4_bet2_mode : // unsigned , default = 1 mode for bet2's sad selection, 0: max sad, 1: three min sads, 2: min sad, 3: co sad, else: (co sad) - (min sad)

Table 9-1147 NR4_MCNR_CM_PRAM 0x2dc6

Bit(s)	R/W	Default	Description
29	R/W	1	reg_nr4_cm_blue_prc_alp0 : // unsigned , default = 1 enable blue processing for mcnr alpha0 calc., dft = 1
28	R/W	1	reg_nr4_cm_blue_prc_alp1 : // unsigned , default = 1 enable blue processing for mcnr alpha1 calc., dft = 1
27	R/W	1	reg_nr4_cm_skin_prc_alp0 : // unsigned , default = 1 enable skin tone processing for mcnr alpha0 calc., dft = 1
26	R/W	1	reg_nr4_cm_green_prc_alp0 : // unsigned , default = 1 enable green processing for mcnr alpha0 clac., dft = 1

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Bit(s)	R/W	Default	Description
25	R/W	1	reg_nr4_cm_skin_prc_alp1 : // unsigned , default = 1 enable skin tone processing for mcnr alpha0 calc., dft = 1
24	R/W	1	reg_nr4_cm_green_prc_alp1 : // unsigned , default = 1 enable green processing for mcnr alpha1 clac., dft = 1
23:20	R/W	13	reg_nr4_cm_blue_hue_st : // unsigned , default = 13 hue start of blue, dft =
19:16	R/W	15	reg_nr4_cm_blue_hue_ed : // unsigned , default = 15 hue end of blue, dft =
15:12	R/W	7	reg_nr4_cm_green_hue_st : // unsigned , default = 7 hue start of green, dft =
11: 8	R/W	10	reg_nr4_cm_green_hue_ed : // unsigned , default = 10 hue end of green, dft =
7: 4	R/W	5	reg_nr4_cm_skin_hue_st : // unsigned , default = 5 hue start of skin, dft =
3: 0	R/W	6	reg_nr4_cm_skin_hue_ed : // unsigned , default = 6 hue end of skin, dft =

Table 9-1148 NR4_MCNR_CM_RSHFT_ALP0 0x2dc7

Bit(s)	R/W	Default	Description
27:25	R/W	5	reg_nr4_cm_blue_rshft_bet0 : // unsigned , default = 5 right shift for bet0's blue color gains, dft = 5
24	R/W	1	reg_nr4_cm_blue_prc_bet0 : // unsigned , default = 1 enable blue processing for mcnr bet0 calc., dft = 1
22:20	R/W	5	reg_nr4_cm_blue_rshft_alp0 : // unsigned , default = 5 right shift for alpha0/1's blue color gains, dft = 5
18:16	R/W	5	reg_nr4_cm_blue_rshft_alp1 : // unsigned , default = 5 right shift for alpha0/1's blue color gains, dft = 5
14:12	R/W	4	reg_nr4_cm_green_rshft_alp0 : // unsigned , default = 4 right shift for alpha0/1's green color gains, dft = 4
10: 8	R/W	4	reg_nr4_cm_green_rshft_alp1 : // unsigned , default = 4 right shift for alpha0/1's green color gains, dft = 4
6: 4	R/W	3	reg_nr4_cm_skin_rshft_alp0 : // unsigned , default = 3 right shift for alpha0/1's skin color gains, dft = 3
2: 0	R/W	3	reg_nr4_cm_skin_rshft_alp1 : // unsigned , default = 3 right shift for alpha0/1's skin color gains, dft = 3

Table 9-1149 NR4_MCNR_BLUE_CENT 0x2dc8

Bit(s)	R/W	Default	Description
23:16	R/W	157	reg_nr4_cm_blue_centx : // unsigned , default = 157 x coordinate of center of blue, dft =
7: 0	R/W	110	reg_nr4_cm_blue_centy : // unsigned , default = 110 y coordinate of center of blue, dft =

Table 9-1150 NR4_MCNR_BLUE_GAIN_PAR0 0x2dc9

Bit(s)	R/W	Default	Description
31:24	R/W	32	reg_nr4_cm_blue_gain_par0 : // unsigned , default = 32 par0 for blue gain, dft =
23:16	R/W	255	reg_nr4_cm_blue_gain_par1 : // unsigned , default = 255 par1 for blue gain, dft =

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Bit(s)	R/W	Default	Description
15: 8	R/W	4	reg_nr4_cm_blue_gain_par2 : // unsigned , default = 4 par2 for blue gain, dft =
7: 0	R/W	32	reg_nr4_cm_blue_gain_par3 : // unsigned , default = 32 par3 for blue gain, dft =

Table 9-1151 NR4_MCNR_BLUE_GAIN_PAR1 0x2dca

Bit(s)	R/W	Default	Description
23:16	R/W	32	reg_nr4_cm_blue_gain_par4 : // unsigned , default = 32 par4 for blue gain, dft =
15: 8	R/W	32	reg_nr4_cm_blue_gain_par5 : // unsigned , default = 32 par5 for blue gain, dft =
7: 0	R/W	0	reg_nr4_cm_blue_gain_par6 : // unsigned , default = 0 par6 for blue gain, dft =

Table 9-1152 NR4_MCNR_CM_BLUE_CLIP0 0x2dcb

Bit(s)	R/W	Default	Description
23:16	R/W	40	reg_nr4_cm_blue_luma_min : // unsigned , default = 40 luma min for blue color matching, dft =
7: 0	R/W	180	reg_nr4_cm_blue_luma_max : // unsigned , default = 180 luma max for blue color matching, dft =

Table 9-1153 NR4_MCNR_CM_BLUE_CLIP1 0x2dcc

Bit(s)	R/W	Default	Description
31:24	R/W	5	reg_nr4_cm_blue_sat_min : // unsigned , default = 5 saturation min for blue color matching, dft =
23:16	R/W	255	reg_nr4_cm_blue_sat_max : // unsigned , default = 255 saturation max for blue color matching, dft =
15: 8	R/W	0	reg_nr4_cm_blue_var_min : // unsigned , default = 0 variation min for blue color matching, dft =
7: 0	R/W	12	reg_nr4_cm_blue_var_max : // unsigned , default = 12 variation max for blue color matching, dft =

Table 9-1154 NR4_MCNR_GREEN_CENT 0x2dcd

Bit(s)	R/W	Default	Description
23:16	R/W	114	reg_nr4_cm_green_centx : // unsigned , default = 114 x coordinate of center of green, dft =
7: 0	R/W	126	reg_nr4_cm_green_centy : // unsigned , default = 126 y coordinate of center of green, dft =

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Table 9-1155 NR4_MCNR_GREEN_GAIN_PAR0 0x2dce

Bit(s)	R/W	Default	Description
31:24	R/W	16	reg_nr4_cm_green_gain_par0 : // unsigned , default = 16 par0 for green gain, dft =
23:16	R/W	255	reg_nr4_cm_green_gain_par1 : // unsigned , default = 255 par1 for green gain, dft =
15: 8	R/W	255	reg_nr4_cm_green_gain_par2 : // unsigned , default = 255 par2 for green gain, dft =
7: 0	R/W	16	reg_nr4_cm_green_gain_par3 : // unsigned , default = 16 par3 for green gain, dft =

Table 9-1156 NR4_MCNR_GREEN_GAIN_PAR1 0x2dcf

Bit(s)	R/W	Default	Description
23:16	R/W	16	reg_nr4_cm_green_gain_par4 : // unsigned , default = 16 par4 for green gain, dft =
15: 8	R/W	128	reg_nr4_cm_green_gain_par5 : // unsigned , default = 128 par5 for green gain, dft =
7: 0	R/W	0	reg_nr4_cm_green_gain_par6 : // unsigned , default = 0 par6 for green gain, dft =

Table 9-1157 NR4_MCNR_GREEN_CLIP0 0x2dd0

Bit(s)	R/W	Default	Description
23:16	R/W	40	reg_nr4_cm_green_luma_min : // unsigned , default = 40 luma min for green color matching, dft =
7: 0	R/W	160	reg_nr4_cm_green_luma_max : // unsigned , default = 160 luma max for green color matching, dft =

Table 9-1158 NR4_MCNR_GREEN_CLIP2 0x2dd1

Bit(s)	R/W	Default	Description
31:24	R/W	4	reg_nr4_cm_green_sat_min : // unsigned , default = 4 saturation min for green color matching, dft =
23:16	R/W	255	reg_nr4_cm_green_sat_max : // unsigned , default = 255 saturation max for green color matching, dft =
15: 8	R/W	0	reg_nr4_cm_green_var_min : // unsigned , default = 0 variation min for green color matching, dft =
7: 0	R/W	12	reg_nr4_cm_green_var_max : // unsigned , default = 12 variation max for green color matching, dft =

Table 9-1159 NR4_MCNR_SKIN_CENT 0x2dd2

Bit(s)	R/W	Default	Description
23:16	R/W	112	reg_nr4_cm_skin_centx : // unsigned , default = 112 x coordinate of center of skin tone, dft =
7: 0	R/W	149	reg_nr4_cm_skin_centy : // unsigned , default = 149 y coordinate of center of skin tone, dft =

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Table 9-1160 NR4_MCNR_SKIN_GAIN_PAR0 0x2dd3

Bit(s)	R/W	Default	Description
31:24	R/W	20	reg_nr4_cm_skin_gain_par0 : // unsigned , default = 20 par0 for skin gain, dft =
23:16	R/W	255	reg_nr4_cm_skin_gain_par1 : // unsigned , default = 255 par1 for skin gain, dft =
15: 8	R/W	255	reg_nr4_cm_skin_gain_par2 : // unsigned , default = 255 par2 for skin gain, dft =
7: 0	R/W	8	reg_nr4_cm_skin_gain_par3 : // unsigned , default = 8 par3 for skin gain, dft =

Table 9-1161 NR4_MCNR_SKIN_GAIN_PAR1 0x2dd4

Bit(s)	R/W	Default	Description
23:16	R/W	8	reg_nr4_cm_skin_gain_par4 : // unsigned , default = 8 par4 for skin gain, dft =
15: 8	R/W	128	reg_nr4_cm_skin_gain_par5 : // unsigned , default = 128 par5 for skin gain, dft =
7: 0	R/W	0	reg_nr4_cm_skin_gain_par6 : // unsigned , default = 0 par6 for skin gain, dft =

Table 9-1162 NR4_MCNR_SKIN_CLIP0 0x2dd5

Bit(s)	R/W	Default	Description
23:16	R/W	40	reg_nr4_cm_skin_luma_min : // unsigned , default = 40 luma min for skin color matching, dft =
7: 0	R/W	180	reg_nr4_cm_skin_luma_max : // unsigned , default = 180 luma max for skin color matching, dft =

Table 9-1163 NR4_MCNR_SKIN_CLIP1 0x2dd6

Bit(s)	R/W	Default	Description
31:24	R/W	5	reg_nr4_cm_skin_sat_min : // unsigned , default = 5 saturation min for skin color matching, dft =
23:16	R/W	255	reg_nr4_cm_skin_sat_max : // unsigned , default = 255 saturation max for skin color matching, dft =
15: 8	R/W	0	reg_nr4_cm_skin_var_min : // unsigned , default = 0 variation min for skin color matching, dft =
7: 0	R/W	12	reg_nr4_cm_skin_var_max : // unsigned , default = 12 variation max for skin color matching, dft =

Table 9-1164 NR4_MCNR_ALP1_GLB_CTRL 0x2dd7

Bit(s)	R/W	Default	Description
31	R/W	0	reg_nr4_alp1_glb_gain_en : // unsigned , default = 0 alp1 adjust by global gain, dft = 1
30:28	R/W	6	reg_nr4_alp1_glb_gain_lsft : // unsigned , default = 6 alp1 left shift before combine with global gain
27	R/W	1	reg_nr4_bet0_glb_gain_en : // unsigned , default = 1 bet0 adjust by global gain, dft = 1

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Bit(s)	R/W	Default	Description
26:24	R/W	6	reg_nr4_bet0_glb_gain_lsft : // unsigned , default = 6 bet1 left shift before combine with global gain
23	R/W	0	reg_nr4_bet1_glb_gain_en : // unsigned , default = 0 bet1 adjust by global gain, dft = 0
22:20	R/W	6	reg_nr4_bet1_glb_gain_lsft : // unsigned , default = 6 bet1 left shift before combine with global gain
19	R/W	1	reg_nr4_bet2_glb_gain_en : // unsigned , default = 1 bet2 adjust by global gain, dft = 1
18:16	R/W	6	reg_nr4_bet2_glb_gain_lsft : // unsigned , default = 6 bet2 left shift before combine with global gain
15	R/W	1	reg_nr4_alp1_ac_en : // unsigned , default = 1 alp1 adjust by ac, dft = 1
14:12	R/W	5	reg_nr4_alp1_ac_lsft : // unsigned , default = 5 alp1 left shift before combine with ac
11	R/W	0	reg_nr4_bet0_ac_en : // unsigned , default = 0 bet0 adjust by ac, dft = 1
10: 8	R/W	5	reg_nr4_bet0_ac_lsft : // unsigned , default = 5 bet0 left shift before combine with ac
7	R/W	0	reg_nr4_bet1_ac_en : // unsigned , default = 0 bet1 adjust by ac, dft = 1
6: 4	R/W	5	reg_nr4_bet1_ac_lsft : // unsigned , default = 5 bet1 left shift before combine with ac
3	R/W	0	reg_nr4_bet2_ac_en : // unsigned , default = 0 bet2 adjust by ac, dft = 1
2: 0	R/W	5	reg_nr4_bet2_ac_lsft : // unsigned , default = 5 bet2 left shift before combine with ac

Table 9-1165 NR4_MCNR_DC2NORM_LUT0 0x2dd8

Bit(s)	R/W	Default	Description
28:24	R/W	16	reg_nr4_dc2norm_lut0 : // unsigned , default = 16 normal 0~16, dc to norm for alpha adjust, dft =
20:16	R/W	16	reg_nr4_dc2norm_lut1 : // unsigned , default = 16 normal 0~16, dc to norm for alpha adjust, dft =
12: 8	R/W	16	reg_nr4_dc2norm_lut2 : // unsigned , default = 16 normal 0~16, dc to norm for alpha adjust, dft =
4: 0	R/W	16	reg_nr4_dc2norm_lut3 : // unsigned , default = 16 normal 0~16, dc to norm for alpha adjust, dft =

Table 9-1166 NR4_MCNR_DC2NORM_LUT1 0x2dd9

Bit(s)	R/W	Default	Description
28:24	R/W	16	reg_nr4_dc2norm_lut4 : // unsigned , default = 16 normal 0~16, dc to norm for alpha adjust, dft =
20:16	R/W	16	reg_nr4_dc2norm_lut5 : // unsigned , default = 16 normal 0~16, dc to norm for alpha adjust, dft =
12: 8	R/W	16	reg_nr4_dc2norm_lut6 : // unsigned , default = 16 normal 0~16, dc to norm for alpha adjust, dft =
4: 0	R/W	12	reg_nr4_dc2norm_lut7 : // unsigned , default = 12 normal 0~16, dc to norm for alpha adjust, dft =

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Table 9-1167 NR4_MCNR_DC2NORM_LUT2 0x2dda

Bit(s)	R/W	Default	Description
4: 0	R/W	8	reg_nr4_dc2norm_lut8 : // unsigned , default = 8 normal 0~16, dc to norm for alpha adjust, dft =

Table 9-1168 NR4_MCNR_AC2NORM_LUT0 0x2ddb

Bit(s)	R/W	Default	Description
28:24	R/W	2	reg_nr4_ac2norm_lut0 : // unsigned , default = 2 normal 0~16, ac to norm for alpha adjust, dft =
20:16	R/W	16	reg_nr4_ac2norm_lut1 : // unsigned , default = 16 normal 0~16, ac to norm for alpha adjust, dft =
12: 8	R/W	16	reg_nr4_ac2norm_lut2 : // unsigned , default = 16 normal 0~16, ac to norm for alpha adjust, dft =
4: 0	R/W	12	reg_nr4_ac2norm_lut3 : // unsigned , default = 12 normal 0~16, ac to norm for alpha adjust, dft =

Table 9-1169 NR4_MCNR_AC2NORM_LUT1 0x2ddc

Bit(s)	R/W	Default	Description
28:24	R/W	4	reg_nr4_ac2norm_lut4 : // unsigned , default = 4 normal 0~16, ac to norm for alpha adjust, dft =
20:16	R/W	2	reg_nr4_ac2norm_lut5 : // unsigned , default = 2 normal 0~16, ac to norm for alpha adjust, dft =
12: 8	R/W	1	reg_nr4_ac2norm_lut6 : // unsigned , default = 1 normal 0~16, ac to norm for alpha adjust, dft =
4: 0	R/W	1	reg_nr4_ac2norm_lut7 : // unsigned , default = 1 normal 0~16, ac to norm for alpha adjust, dft =

Table 9-1170 NR4_MCNR_AC2NORM_LUT2 0x2ddd

Bit(s)	R/W	Default	Description
4: 0	R/W	1	reg_nr4_ac2norm_lut8 : // unsigned , default = 1 normal 0~16, ac to norm for alpha adjust, dft =

Table 9-1171 NR4_MCNR_SAD2ALP0_LUT0 0x2dde

Bit(s)	R/W	Default	Description
31:24	R/W	255	reg_nr4_sad2alp0_lut0 : // unsigned , default = 255 sad to alpha0 for temporal pixel value, dft = 255
23:16	R/W	252	reg_nr4_sad2alp0_lut1 : // unsigned , default = 252 sad to alpha0 for temporal pixel value, dft = 252

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Bit(s)	R/W	Default	Description
15: 8	R/W	249	reg_nr4_sad2alp0_lut2 : // unsigned , default = 249 sad to alpha0 for temporal pixel value, dft = 249
7: 0	R/W	235	reg_nr4_sad2alp0_lut3 : // unsigned , default = 235 sad to alpha0 for temporal pixel value, dft = 70

Table 9-1172 NR4_MCNR_SAD2ALP0_LUT1 0x2ddf

Bit(s)	R/W	Default	Description
31:24	R/W	185	reg_nr4_sad2alp0_lut4 : // unsigned , default = 185 sad to alpha0 for temporal pixel value, dft = 12
23:16	R/W	70	reg_nr4_sad2alp0_lut5 : // unsigned , default = 70 sad to alpha0 for temporal pixel value, dft = 1
15: 8	R/W	14	reg_nr4_sad2alp0_lut6 : // unsigned , default = 14 sad to alpha0 for temporal pixel value, dft = 0
7: 0	R/W	1	reg_nr4_sad2alp0_lut7 : // unsigned , default = 1 sad to alpha0 for temporal pixel value, dft = 0

Table 9-1173 NR4_MCNR_SAD2ALP0_LUT2 0x2de0

Bit(s)	R/W	Default	Description
31:24	R/W	0	reg_nr4_sad2alp0_lut8 : // unsigned , default = 0 sad to alpha0 for temporal pixel value, dft = 0
23:16	R/W	0	reg_nr4_sad2alp0_lut9 : // unsigned , default = 0 sad to alpha0 for temporal pixel value, dft = 0
15: 8	R/W	0	reg_nr4_sad2alp0_lut10 : // unsigned , default = 0 sad to alpha0 for temporal pixel value, dft = 0
7: 0	R/W	0	reg_nr4_sad2alp0_lut11 : // unsigned , default = 0 sad to alpha0 for temporal pixel value, dft = 0

Table 9-1174 NR4_MCNR_SAD2ALP0_LUT3 0x2de1

Bit(s)	R/W	Default	Description
31:24	R/W	0	reg_nr4_sad2alp0_lut12 : // unsigned , default = 0 sad to alpha0 for temporal pixel value, dft = 0
23:16	R/W	0	reg_nr4_sad2alp0_lut13 : // unsigned , default = 0 sad to alpha0 for temporal pixel value, dft = 0
15: 8	R/W	0	reg_nr4_sad2alp0_lut14 : // unsigned , default = 0 sad to alpha0 for temporal pixel value, dft = 0
7: 0	R/W	0	reg_nr4_sad2alp0_lut15 : // unsigned , default = 0 sad to alpha0 for temporal pixel value, dft = 0

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Table 9-1175 NR4_MCNR_SAD2ALP1_LUT0 0x2de2

Bit(s)	R/W	Default	Description
31:24	R/W	192	reg_nr4_sad2alp1_lut0 : // unsigned , default = 192 sad to alpha1 for temporal blending, dft = 128
23:16	R/W	160	reg_nr4_sad2alp1_lut1 : // unsigned , default = 160 sad to alpha1 for temporal blending, dft = 128
15: 8	R/W	128	reg_nr4_sad2alp1_lut2 : // unsigned , default = 128 sad to alpha1 for temporal blending, dft = 128
7: 0	R/W	96	reg_nr4_sad2alp1_lut3 : // unsigned , default = 96 sad to alpha1 for temporal blending, dft = 64

Table 9-1176 NR4_MCNR_SAD2ALP1_LUT1 0x2de3

Bit(s)	R/W	Default	Description
31:24	R/W	64	reg_nr4_sad2alp1_lut4 : // unsigned , default = 64 sad to alpha1 for temporal blending, dft = 64
23:16	R/W	32	reg_nr4_sad2alp1_lut5 : // unsigned , default = 32 sad to alpha1 for temporal blending, dft = 128
15: 8	R/W	16	reg_nr4_sad2alp1_lut6 : // unsigned , default = 16 sad to alpha1 for temporal blending, dft = 255
7: 0	R/W	8	reg_nr4_sad2alp1_lut7 : // unsigned , default = 8 sad to alpha1 for temporal blending, dft = 255

Table 9-1177 NR4_MCNR_SAD2ALP1_LUT2 0x2de4

Bit(s)	R/W	Default	Description
31:24	R/W	4	reg_nr4_sad2alp1_lut8 : // unsigned , default = 4 sad to alpha1 for temporal blending, dft = 255
23:16	R/W	0	reg_nr4_sad2alp1_lut9 : // unsigned , default = 0 sad to alpha1 for temporal blending, dft = 255
15: 8	R/W	16	reg_nr4_sad2alp1_lut10 : // unsigned , default = 16 sad to alpha1 for temporal blending, dft = 255
7: 0	R/W	64	reg_nr4_sad2alp1_lut11 : // unsigned , default = 64 sad to alpha1 for temporal blending, dft = 255

Table 9-1178 NR4_MCNR_SAD2ALP1_LUT3 0x2de5

Bit(s)	R/W	Default	Description
31:24	R/W	96	reg_nr4_sad2alp1_lut12 : // unsigned , default = 96 sad to alpha1 for temporal blending, dft = 255
23:16	R/W	224	reg_nr4_sad2alp1_lut13 : // unsigned , default = 224 sad to alpha1 for temporal blending, dft = 255
15: 8	R/W	255	reg_nr4_sad2alp1_lut14 : // unsigned , default = 255 sad to alpha1 for temporal blending, dft = 255
7: 0	R/W	255	reg_nr4_sad2alp1_lut15 : // unsigned , default = 255 sad to alpha1 for temporal blending, dft = 255

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Table 9-1179 NR4_MCNR_SAD2BET0_LUT0 0x2de6

Bit(s)	R/W	Default	Description
31:24	R/W	0	reg_nr4_sad2bet0_lut0 : // unsigned , default = 0 sad to beta0 for tnr and mcnr blending, dft = 0
23:16	R/W	2	reg_nr4_sad2bet0_lut1 : // unsigned , default = 2 sad to beta0 for tnr and mcnr blending, dft = 2
15: 8	R/W	4	reg_nr4_sad2bet0_lut2 : // unsigned , default = 4 sad to beta0 for tnr and mcnr blending, dft = 4
7: 0	R/W	8	reg_nr4_sad2bet0_lut3 : // unsigned , default = 8 sad to beta0 for tnr and mcnr blending, dft = 8

Table 9-1180 NR4_MCNR_SAD2BET0_LUT1 0x2de7

Bit(s)	R/W	Default	Description
31:24	R/W	16	reg_nr4_sad2bet0_lut4 : // unsigned , default = 16 sad to beta0 for tnr and mcnr blending, dft = 16
23:16	R/W	32	reg_nr4_sad2bet0_lut5 : // unsigned , default = 32 sad to beta0 for tnr and mcnr blending, dft = 32
15: 8	R/W	48	reg_nr4_sad2bet0_lut6 : // unsigned , default = 48 sad to beta0 for tnr and mcnr blending, dft = 48
7: 0	R/W	64	reg_nr4_sad2bet0_lut7 : // unsigned , default = 64 sad to beta0 for tnr and mcnr blending, dft = 64

Table 9-1181 NR4_MCNR_SAD2BET0_LUT2 0x2de8

Bit(s)	R/W	Default	Description
31:24	R/W	80	reg_nr4_sad2bet0_lut8 : // unsigned , default = 80 sad to beta0 for tnr and mcnr blending, dft = 80
23:16	R/W	96	reg_nr4_sad2bet0_lut9 : // unsigned , default = 96 sad to beta0 for tnr and mcnr blending, dft = 96
15: 8	R/W	112	reg_nr4_sad2bet0_lut10 : // unsigned , default = 112 sad to beta0 for tnr and mcnr blending, dft = 112
7: 0	R/W	128	reg_nr4_sad2bet0_lut11 : // unsigned , default = 128 sad to beta0 for tnr and mcnr blending, dft = 128

Table 9-1182 NR4_MCNR_SAD2BET0_LUT3 0x2de9

Bit(s)	R/W	Default	Description
31:24	R/W	196	reg_nr4_sad2bet0_lut12 : // unsigned , default = 196 sad to beta0 for tnr and mcnr blending, dft = 160
23:16	R/W	224	reg_nr4_sad2bet0_lut13 : // unsigned , default = 224 sad to beta0 for tnr and mcnr blending, dft = 192
15: 8	R/W	255	reg_nr4_sad2bet0_lut14 : // unsigned , default = 255 sad to beta0 for tnr and mcnr blending, dft = 224
7: 0	R/W	255	reg_nr4_sad2bet0_lut15 : // unsigned , default = 255 sad to beta0 for tnr and mcnr blending, dft = 255

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Table 9-1183 NR4_MCNR_SAD2BET1_LUT0 0x2dea

Bit(s)	R/W	Default	Description
31:24	R/W	0	reg_nr4_sad2bet1_lut0 : // unsigned , default = 0 sad to beta1 for deghost blending, dft = 0
23:16	R/W	2	reg_nr4_sad2bet1_lut1 : // unsigned , default = 2 sad to beta1 for deghost blending, dft = 2
15: 8	R/W	4	reg_nr4_sad2bet1_lut2 : // unsigned , default = 4 sad to beta1 for deghost blending, dft = 4
7: 0	R/W	8	reg_nr4_sad2bet1_lut3 : // unsigned , default = 8 sad to beta1 for deghost blending, dft = 8

Table 9-1184 NR4_MCNR_SAD2BET1_LUT1 0x2deb

Bit(s)	R/W	Default	Description
31:24	R/W	16	reg_nr4_sad2bet1_lut4 : // unsigned , default = 16 sad to beta1 for deghost blending, dft = 16
23:16	R/W	32	reg_nr4_sad2bet1_lut5 : // unsigned , default = 32 sad to beta1 for deghost blending, dft = 32
15: 8	R/W	48	reg_nr4_sad2bet1_lut6 : // unsigned , default = 48 sad to beta1 for deghost blending, dft = 48
7: 0	R/W	64	reg_nr4_sad2bet1_lut7 : // unsigned , default = 64 sad to beta1 for deghost blending, dft = 64

Table 9-1185 NR4_MCNR_SAD2BET1_LUT2 0x2dec

Bit(s)	R/W	Default	Description
31:24	R/W	80	reg_nr4_sad2bet1_lut8 : // unsigned , default = 80 sad to beta1 for deghost blending, dft = 80
23:16	R/W	96	reg_nr4_sad2bet1_lut9 : // unsigned , default = 96 sad to beta1 for deghost blending, dft = 96
15: 8	R/W	112	reg_nr4_sad2bet1_lut10 : // unsigned , default = 112 sad to beta1 for deghost blending, dft = 112
7: 0	R/W	128	reg_nr4_sad2bet1_lut11 : // unsigned , default = 128 sad to beta1 for deghost blending, dft = 128

Table 9-1186 NR4_MCNR_SAD2BET1_LUT3 0x2ded

Bit(s)	R/W	Default	Description
31:24	R/W	160	reg_nr4_sad2bet1_lut12 : // unsigned , default = 160 sad to beta1 for deghost blending, dft = 160
23:16	R/W	192	reg_nr4_sad2bet1_lut13 : // unsigned , default = 192 sad to beta1 for deghost blending, dft = 192
15: 8	R/W	224	reg_nr4_sad2bet1_lut14 : // unsigned , default = 224 sad to beta1 for deghost blending, dft = 224
7: 0	R/W	255	reg_nr4_sad2bet1_lut15 : // unsigned , default = 255 sad to beta1 for deghost blending, dft = 255

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Table 9-1187 NR4_MCNR_SAD2BET2_LUT0 0x2dee

Bit(s)	R/W	Default	Description
31:24	R/W	0	reg_nr4_sad2bet2_lut0 : // unsigned , default = 0 sad to beta2 for snr and mcnr blending, dft = 0
23:16	R/W	1	reg_nr4_sad2bet2_lut1 : // unsigned , default = 1 sad to beta2 for snr and mcnr blending, dft = 2
15: 8	R/W	2	reg_nr4_sad2bet2_lut2 : // unsigned , default = 2 sad to beta2 for snr and mcnr blending, dft = 4
7: 0	R/W	4	reg_nr4_sad2bet2_lut3 : // unsigned , default = 4 sad to beta2 for snr and mcnr blending, dft = 8

Table 9-1188 NR4_MCNR_SAD2BET2_LUT1 0x2def

Bit(s)	R/W	Default	Description
31:24	R/W	8	reg_nr4_sad2bet2_lut4 : // unsigned , default = 8 sad to beta2 for snr and mcnr blending, dft = 16
23:16	R/W	16	reg_nr4_sad2bet2_lut5 : // unsigned , default = 16 sad to beta2 for snr and mcnr blending, dft = 32
15: 8	R/W	32	reg_nr4_sad2bet2_lut6 : // unsigned , default = 32 sad to beta2 for snr and mcnr blending, dft = 48
7: 0	R/W	48	reg_nr4_sad2bet2_lut7 : // unsigned , default = 48 sad to beta2 for snr and mcnr blending, dft = 64

Table 9-1189 NR4_MCNR_SAD2BET2_LUT2 0x2df0

Bit(s)	R/W	Default	Description
31:24	R/W	64	reg_nr4_sad2bet2_lut8 : // unsigned , default = 64 sad to beta2 for snr and mcnr blending, dft = 80
23:16	R/W	80	reg_nr4_sad2bet2_lut9 : // unsigned , default = 80 sad to beta2 for snr and mcnr blending, dft = 96
15: 8	R/W	96	reg_nr4_sad2bet2_lut10 : // unsigned , default = 96 sad to beta2 for snr and mcnr blending, dft = 112
7: 0	R/W	112	reg_nr4_sad2bet2_lut11 : // unsigned , default = 112 sad to beta2 for snr and mcnr blending, dft = 128

Table 9-1190 NR4_MCNR_SAD2BET2_LUT3 0x2df1

Bit(s)	R/W	Default	Description
31:24	R/W	128	reg_nr4_sad2bet2_lut12 : // unsigned , default = 128 sad to beta2 for snr and mcnr blending, dft = 160
23:16	R/W	160	reg_nr4_sad2bet2_lut13 : // unsigned , default = 160 sad to beta2 for snr and mcnr blending, dft = 192
15: 8	R/W	224	reg_nr4_sad2bet2_lut14 : // unsigned , default = 224 sad to beta2 for snr and mcnr blending, dft = 224
7: 0	R/W	255	reg_nr4_sad2bet2_lut15 : // unsigned , default = 255 sad to beta2 for snr and mcnr blending, dft = 255

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Table 9-1191 NR4_MCNR_RO_U_SUM 0x2df2

Bit(s)	R/W	Default	Description
31: 0	R.O	0	ro_nr4_u_sum : // unsigned , default = 0 sum of U of current field/frame

Table 9-1192 NR4_MCNR_RO_V_SUM 0x2df3

Bit(s)	R/W	Default	Description
31: 0	R.O	0	ro_nr4_v_sum : // unsigned , default = 0 sum of V of current field/frame

Table 9-1193 NR4_MCNR_RO_GRDU_SUM 0x2df4

Bit(s)	R/W	Default	Description
31: 0	R.O	0	ro_nr4_grdu_sum : // unsigned , default = 0 sum of gradient U of current field/ frame

Table 9-1194 NR4_MCNR_RO_GRDV_SUM 0x2df5

Bit(s)	R/W	Default	Description
31: 0	R.O	0	ro_nr4_grdv_sum : // unsigned , default = 0 sum of gradient V of current field/ frame

Table 9-1195 NR4_TOP_CTRL 0x2dff

Bit(s)	R/W	Default	Description
31:20	R/W	0	reg_gclk_ctrl : // unsigned , default = 0
18	R/W	1	reg_nr4_mcnr_en : // unsigned , default = 1 ncnr enable or bypass, dft = 1
17	R/W	1	reg_nr2_en : // unsigned , default = 1 nr2 enable, dft = 1
16	R/W	1	reg_nr4_en : // unsigned , default = 1 nr4 enable, dft = 1
15	R/W	1	reg_nr2_proc_en : // unsigned , default = 1
14	R/W	1	reg_det3d_en : // unsigned , default = 1
13	R/W	1	di_polar_en : // unsigned , default = 1 do does not have in C
12	R/W	0	reg_cfr_enable : // unsigned , default = 0 0-disable; 1:enable
11: 9	R/W	7	reg_3dnr_enable_l : // unsigned , default = 7 b0: Y b1:U b2:V
8: 6	R/W	7	reg_3dnr_enable_r : // unsigned , default = 7 b0: Y b1:U b2:V
5	R/W	1	reg_nr4_lnbuf_ctrl : // unsigned , default = 1 line buf ctrl for nr4: 0, 3lines, 1, 5lines, dft = 1
4	R/W	0	reg_nr4_snr2_en : // unsigned , default = 0 snr2 enable, 0: use old snr, 1: use new snr2, dft = 1
3	R/W	1	reg_nr4_scene_change_en : // unsigned , default = 1 enable scene change proc. dft = 1
2	R/W	1	nr2_sw_en : // unsigned , default = 1 do does not have in C
0	R/W	0	reg_nr4_scene_change_flg : // unsigned , default = 0 flags for scene change, dft = 0

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Table 9-1196 NR4_MCNR_SAD_GAIN 0x3700

Bit(s)	R/W	Default	Description
24	R/W	0	reg_nr4_bld12vs3_usemaxsad : // unsigned , default = 0 use minsad/maxsad instead of minsad/avgsad to decision if it was texture or flat region, 1: use minsad/maxsad
23:16	R/W	64	reg_nr4_bld12vs3_rate_gain : // unsigned , default = 64 gain to minsad/maxsad or minsad/avgsad before LUT, 64 normalized as "1"
15: 8	R/W	32	reg_nr4_bld1vs2_rate_gain : // unsigned , default = 32 gain to minsad/maxsad or minsad/avgsad before the LUT, 64 normalized as"1"
7: 0	R/W	64	reg_nr4_coefblt_gain : // unsigned , default = 64 gain to final coefblt, normalized 64 as "1"

Table 9-1197 NR4_MCNR_LPF_CTRL 0x3701

Bit(s)	R/W	Default	Description
30:22	R/W	0	reg_nr4_preflt_alpofst : // signed , default = 0 pre filter alpha ofst
21:16	R/W	16	reg_nr4_preflt_alpgain : // unsigned , default = 16 pre filter alpha gain
15:14	R/W	3	reg_nr4_preflt_alpsel : // unsigned , default = 3 pre filter alpha selection for adaptive blending, 0: mv pointed sad, 1: weighted mv pointed sad, 2or3: coefblt
13: 8	R/W	8	reg_nr4_avgsad_gain : // unsigned , default = 8 gain for avg sad before luts
6	R/W	1	reg_nr4_maxsad_mod : // unsigned , default = 1 max sad select mode, 0: mx2_sad, 1: max sad
5	R/W	1	reg_nr4_minsad_mod : // unsigned , default = 1 min sad select mode, 0: sad with min err, 1: min sad
4	R/W	1	reg_nr4_minmaxsad_lpf : // unsigned , default = 1 mode of lpf for minmaxsad, 0: no LPF, 1: [1 2 1]/4
3	R/W	1	reg_nr4_avgsad_lpf : // unsigned , default = 1 mode of lpf for avgsad, 0: no LPF, 1: [1 2 1]/4
2	R/W	1	reg_nr4_minavgsad_ratio_lpf : // unsigned , default = 1 mode of lpf for minsad/avgsad and zmvsad/avgsad, 0: no LPF, 1: [1 2 1]/4
1	R/W	1	reg_nr4_bldvs_lut_lpf : // unsigned , default = 1 mode of lpf for bld12vs3 and bld1vs2 LUT results, 0: no LPF, 1: [1 2 1]/4
0	R/W	1	reg_nr4_final_coef_lpf : // unsigned , default = 1 mode of lpf for final coef_blt_blend123, 0: no LPF, 1: [1 2 1]/4

Table 9-1198 NR4_MCNR_BLD_VS3LUT0 0x3702

Bit(s)	R/W	Default	Description
29:24	R/W	0	reg_nr4_bld12vs3_lut0 : // unsigned , default = 0
21:16	R/W	8	reg_nr4_bld12vs3_lut1 : // unsigned , default = 8
13: 8	R/W	10	reg_nr4_bld12vs3_lut2 : // unsigned , default = 10
5: 0	R/W	11	reg_nr4_bld12vs3_lut3 : // unsigned , default = 11

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Table 9-1199 NR4_MCNR_BLD_VS3LUT1 0x3703

Bit(s)	R/W	Default	Description
29:24	R/W	12	reg_nr4_bld12vs3_lut4 : // unsigned , default = 12
21:16	R/W	14	reg_nr4_bld12vs3_lut5 : // unsigned , default = 14
13: 8	R/W	16	reg_nr4_bld12vs3_lut6 : // unsigned , default = 16
5: 0	R/W	24	reg_nr4_bld12vs3_lut7 : // unsigned , default = 24

Table 9-1200 NR4_MCNR_BLD_VS3LUT2 0x3704

Bit(s)	R/W	Default	Description
29:24	R/W	50	reg_nr4_bld12vs3_lut8 : // unsigned , default = 50
21:16	R/W	58	reg_nr4_bld12vs3_lut9 : // unsigned , default = 58
13: 8	R/W	63	reg_nr4_bld12vs3_lut10 : // unsigned , default = 63
5: 0	R/W	63	reg_nr4_bld12vs3_lut11 : // unsigned , default = 63

Table 9-1201 NR4_MCNR_BLD_VS2LUT0 0x3705

Bit(s)	R/W	Default	Description
29:24	R/W	63	reg_nr4_bld1vs2_lut0 : // unsigned , default = 63
21:16	R/W	32	reg_nr4_bld1vs2_lut1 : // unsigned , default = 32
13: 8	R/W	16	reg_nr4_bld1vs2_lut2 : // unsigned , default = 16
5: 0	R/W	8	reg_nr4_bld1vs2_lut3 : // unsigned , default = 8

Table 9-1202 NR4_MCNR_BLD_VS2LUT1 0x3706

Bit(s)	R/W	Default	Description
29:24	R/W	4	reg_nr4_bld1vs2_lut4 : // unsigned , default = 4
21:16	R/W	2	reg_nr4_bld1vs2_lut5 : // unsigned , default = 2
13: 8	R/W	1	reg_nr4_bld1vs2_lut6 : // unsigned , default = 1
5: 0	R/W	0	reg_nr4_bld1vs2_lut7 : // unsigned , default = 0

Table 9-1203 NR4_COEFBLT_LUT10 0x3707

Bit(s)	R/W	Default	Description
31:24	R/W	0x0	reg_nr4_coefblt_lut10 : // signed , default = -128
23:16	R/W	0x0	reg_nr4_coefblt_lut11 : // signed , default = -128
15: 8	R/W	0x0	reg_nr4_coefblt_lut12 : // signed , default = -126
7: 0	R/W	0x0	reg_nr4_coefblt_lut13 : // signed , default = -124

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Table 9-1204 NR4_COEFBLT_LUT11 0x3708

Bit(s)	R/W	Default	Description
31:24	R/W	0x0	reg_nr4_coefblt_lut14 : // signed , default = -120
23:16	R/W	0x0	reg_nr4_coefblt_lut15 : // signed , default = -110
15: 8	R/W	0x0	reg_nr4_coefblt_lut16 : // signed , default = -100
7: 0	R/W	0x0	reg_nr4_coefblt_lut17 : // signed , default = -90

Table 9-1205 NR4_COEFBLT_LUT12 0x3709

Bit(s)	R/W	Default	Description
31:24	R/W	0x0	reg_nr4_coefblt_lut18 : // signed , default = -56
23:16	R/W	0x0	reg_nr4_coefblt_lut19 : // signed , default = -32
15: 8	R/W	0x0	reg_nr4_coefblt_lut110 : // signed , default = -64
7: 0	R/W	0x0	reg_nr4_coefblt_lut111 : // signed , default = -128

Table 9-1206 NR4_COEFBLT_LUT20 0x370a

Bit(s)	R/W	Default	Description
31:24	R/W	0x0	reg_nr4_coefblt_lut20 : // signed , default = -128
23:16	R/W	0x0	reg_nr4_coefblt_lut21 : // signed , default = -120
15: 8	R/W	0x0	reg_nr4_coefblt_lut22 : // signed , default = -112
7: 0	R/W	0x0	reg_nr4_coefblt_lut23 : // signed , default = -104

Table 9-1207 NR4_COEFBLT_LUT21 0x370b

Bit(s)	R/W	Default	Description
31:24	R/W	0x0	reg_nr4_coefblt_lut24 : // signed , default = -96
23:16	R/W	0x0	reg_nr4_coefblt_lut25 : // signed , default = -88
15: 8	R/W	0x0	reg_nr4_coefblt_lut26 : // signed , default = -76
7: 0	R/W	0x0	reg_nr4_coefblt_lut27 : // signed , default = -64

Table 9-1208 NR4_COEFBLT_LUT22 0x370c

Bit(s)	R/W	Default	Description
31:24	R/W	0x0	reg_nr4_coefblt_lut28 : // signed , default = -48
23:16	R/W	0x0	reg_nr4_coefblt_lut29 : // signed , default = -32
15: 8	R/W	0x0	reg_nr4_coefblt_lut210 : // signed , default = -64
7: 0	R/W	0x0	reg_nr4_coefblt_lut211 : // signed , default = -108

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Table 9-1209 NR4_COEFBLT_LUT30 0x370d

Bit(s)	R/W	Default	Description
31:24	R/W	8	reg_nr4_coefblt_lut30 : // signed , default = 8
23:16	R/W	16	reg_nr4_coefblt_lut31 : // signed , default = 16
15: 8	R/W	24	reg_nr4_coefblt_lut32 : // signed , default = 24
7: 0	R/W	30	reg_nr4_coefblt_lut33 : // signed , default = 30

Table 9-1210 NR4_COEFBLT_LUT31 0x370e

Bit(s)	R/W	Default	Description
31:24	R/W	36	reg_nr4_coefblt_lut34 : // signed , default = 36
23:16	R/W	48	reg_nr4_coefblt_lut35 : // signed , default = 48
15: 8	R/W	70	reg_nr4_coefblt_lut36 : // signed , default = 70
7: 0	R/W	96	reg_nr4_coefblt_lut37 : // signed , default = 96

Table 9-1211 NR4_COEFBLT_LUT32 0x370f

Bit(s)	R/W	Default	Description
31:24	R/W	120	reg_nr4_coefblt_lut38 : // signed , default = 120
23:16	R/W	64	reg_nr4_coefblt_lut39 : // signed , default = 64
15: 8	R/W	16	reg_nr4_coefblt_lut310 : // signed , default = 16
7: 0	R/W	0x0	reg_nr4_coefblt_lut311 : // signed , default = -8

Table 9-1212 NR4_COEFBLT_CONV 0x3710

Bit(s)	R/W	Default	Description
23:16	R/W	0	reg_nr4_coefblt_convmin : // unsigned , default = 0 minimum of coef. bilateral conversion
15: 8	R/W	255	reg_nr4_coefblt_convmax : // unsigned , default = 255 maximum of coef. bilateral conversion
7: 0	R/W	128	reg_nr4_coefblt_convmid : // unsigned , default = 128 value at midpoint of coef. bilateral conversion

Table 9-1213 NR4_DBGWIN_YX0 0x3711

Bit(s)	R/W	Default	Description
29:16	R/W	100	reg_nr4_dgbwin_yx0 : // unsigned , default = 100 ystart for debug window
13: 0	R/W	160	reg_nr4_dgbwin_yx1 : // unsigned , default = 160 yend for debug window

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Table 9-1214 NR4_DBGWIN_YX1 0x3712

Bit(s)	R/W	Default	Description
29:16	R/W	200	reg_nr4_dgbwin_yx2 : // unsigned , default = 200 xstart for debug window
13: 0	R/W	300	reg_nr4_dgbwin_yx3 : // unsigned , default = 300 xend for debug window

Table 9-1215 NR4_NM_X_CFG 0x3713

Bit(s)	R/W	Default	Description
29:16	R/W	8	reg_nr4_nm_xst : // unsigned , default = 8 start for noise meter statistic, dft = 8
13: 0	R/W	711	reg_nr4_nm_xed : // unsigned , default = 711 end for noise meter statistic, dft = HSIZE-8-1;

Table 9-1216 NR4_NM_Y_CFG 0x3714

Bit(s)	R/W	Default	Description
29:16	R/W	8	reg_nr4_nm_yst : // unsigned , default = 8 start for noise meter statistic, dft = 8;
13: 0	R/W	231	reg_nr4_nm_yed : // unsigned , default = 231 end for noise meter statistic, dft = VSIZE-8-1;

Table 9-1217 NR4_NM_SAD_THD 0x3715

Bit(s)	R/W	Default	Description
7: 0	R/W	255	reg_nr4_nm_sad_thd : // unsigned , default = 255 threshold for (flat region) sad count, dft = 4

Table 9-1218 NR4_MCNR_BANDSPLIT_PRAM 0x3716

Bit(s)	R/W	Default	Description
4	R/W	1	reg_nr4_mc_use_bandsplit : // unsigned , default = 1 separate lp and us for mc IIR filter, 0: no BS used; 1: use BS
3	R/W	1	reg_nr4_mc_apply_on_lp : // unsigned , default = 1 use mcnr only on lowpass portion;
2	R/W	1	reg_nr4_mc_apply_on_us : // unsigned , default = 1 use mcnr only on lp complimentary portion;
1: 0	R/W	1	reg_nr4_mc_zmvbs_use_adplpf : // unsigned , default = 1 use adapptive LPF for the zmv pointing data for MCNR, for abs(mvx)<th

Table 9-1219 NR4_MCNR_ALP1_SGN_COR 0x3717

Bit(s)	R/W	Default	Description
31:24	R/W	10	reg_nr4_mc_aph1_sgn_coring0 : // unsigned , default = 10 coring to cur-pre before do sgn decision
23:16	R/W	7	reg_nr4_mc_aph1_sgn_coring1 : // unsigned , default = 7 coring to cur-pre before do sgn decision

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Bit(s)	R/W	Default	Description
15: 8	R/W	90	reg_nr4_mc_aph1_sgn_core_max0 : // unsigned , default = 90 maximum of coring, default = 30/15
7: 0	R/W	15	reg_nr4_mc_aph1_sgn_core_max1 : // unsigned , default = 15 maximum of coring, default = 30/15

Table 9-1220 NR4_MCNR_ALP1_SGN_PRAM 0x3718

Bit(s)	R/W	Default	Description
10	R/W	1	reg_nr4_mc_alp1_sgn_half : // unsigned , default = 1 half block sgn sum mode enable, 0: only use 3x5 whole block sum of sgns; 1: use max(sgn_3x5, sqrt(sgn_left+sgn_righ))
9	R/W	1	reg_nr4_mc_alp1_sgn_frczmv : // unsigned , default = 1 force zmv to calculate the sign_sum;
8	R/W	1	reg_nr4_mc_alp1_sgnmvx_mode : // unsigned , default = 1 blend mode of sgnlut and mvxlut blend mode: 0: sgnlut+ mvxlut; 1: max(sgnlut, mvxlut), default =1
7: 4	R/W	4	reg_nr4_mc_aph1_sgn_crate0 : // unsigned , default = 4 rate to var, norm to 16 as 1, default = 2
3: 0	R/W	2	reg_nr4_mc_aph1_sgn_crate1 : // unsigned , default = 2 rate to var, norm to 16 as 1, default = 2

Table 9-1221 NR4_MCNR_ALP1_MVX_LUT1 0x3719

Bit(s)	R/W	Default	Description
31:28	R/W	14	reg_nr4_mc_alp1_mvx_luty3 : // unsigned , default = 14 alp1 of luma vas mvx (0~7), and alp1 vs mvy(0,1)
27:24	R/W	14	reg_nr4_mc_alp1_mvx_lutc3 : // unsigned , default = 14 alp1 of chrm vas mvx (0~7), and alp1 vs mvy(0,1)
23:20	R/W	12	reg_nr4_mc_alp1_mvx_luty2 : // unsigned , default = 12 alp1 of luma vas mvx (0~7), and alp1 vs mvy(0,1)
19:16	R/W	12	reg_nr4_mc_alp1_mvx_lutc2 : // unsigned , default = 12 alp1 of chrm vas mvx (0~7), and alp1 vs mvy(0,1)
15:12	R/W	5	reg_nr4_mc_alp1_mvx_luty1 : // unsigned , default = 5 alp1 of luma vas mvx (0~7), and alp1 vs mvy(0,1)
11: 8	R/W	5	reg_nr4_mc_alp1_mvx_lutc1 : // unsigned , default = 5 alp1 of chrm vas mvx (0~7), and alp1 vs mvy(0,1)
7: 4	R/W	3	reg_nr4_mc_alp1_mvx_luty0 : // unsigned , default = 3 alp1 of luma vas mvx (0~7), and alp1 vs mvy(0,1)
3: 0	R/W	3	reg_nr4_mc_alp1_mvx_lutc0 : // unsigned , default = 3 alp1 of chrm vas mvx (0~7), and alp1 vs mvy(0,1)

Table 9-1222 NR4_MCNR_ALP1_MVX_LUT2 0x371a

Bit(s)	R/W	Default	Description
31:28	R/W	15	reg_nr4_mc_alp1_mvx_luty7 : // unsigned , default = 15 alp1 of luma vas mvx (0~7), and alp1 vs mvy(0,1)
27:24	R/W	15	reg_nr4_mc_alp1_mvx_lutc7 : // unsigned , default = 15 alp1 of chrm vas mvx (0~7), and alp1 vs mvy(0,1)

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Bit(s)	R/W	Default	Description
23:20	R/W	15	reg_nr4_mc_alp1_mvx_luty6 : // unsigned , default = 15 alp1 of luma vas mvx (0~7), and alp1 vs mvy(0,1)
19:16	R/W	15	reg_nr4_mc_alp1_mvx_lutc6 : // unsigned , default = 15 alp1 of chrm vas mvx (0~7), and alp1 vs mvy(0,1)
15:12	R/W	15	reg_nr4_mc_alp1_mvx_luty5 : // unsigned , default = 15 alp1 of luma vas mvx (0~7), and alp1 vs mvy(0,1)
11: 8	R/W	15	reg_nr4_mc_alp1_mvx_lutc5 : // unsigned , default = 15 alp1 of chrm vas mvx (0~7), and alp1 vs mvy(0,1)
7: 4	R/W	15	reg_nr4_mc_alp1_mvx_luty4 : // unsigned , default = 15 alp1 of luma vas mvx (0~7), and alp1 vs mvy(0,1)
3: 0	R/W	15	reg_nr4_mc_alp1_mvx_lutc4 : // unsigned , default = 15 alp1 of chrm vas mvx (0~7), and alp1 vs mvy(0,1)

Table 9-1223 NR4_MCNR_ALP1_MVX_LUT3 0x371b

Bit(s)	R/W	Default	Description
7: 4	R/W	6	reg_nr4_mc_alp1_mvx_luty8 : // unsigned , default = 6 alp1 of luma vas mvx (0~7), and alp1 vs mvy(0,1)
3: 0	R/W	6	reg_nr4_mc_alp1_mvx_lutc8 : // unsigned , default = 6 alp1 of chrm vas mvx (0~7), and alp1 vs mvy(0,1)

Table 9-1224 NR4_MCNR_ALP1_LP_PRAM 0x371c

Bit(s)	R/W	Default	Description
17:16	R/W	1	reg_nr4_mc_alp1_lp_sel : // unsigned , default = 1 mode for alp1_lp for lp portion IIR, 0: apha1, 1:dc_dif vs ac analysis; 2: gain/ofst of alp1; 3: max of 1/ 2 results
15: 8	R/W	64	reg_nr4_mc_alp1_lp_gain : // unsigned , default = 64 gain to alp1 to get the alp1_lp = alp1*gain/32 + ofset, default =64;
7: 0	R/W	0	reg_nr4_mc_alp1_lp_ofst : // signed , default = 0 offset to alp1 to get the alp1_lp = alp1*gain/32 + ofset, default =10;

Table 9-1225 NR4_MCNR_ALP1_SGN_LUT1 0x371d

Bit(s)	R/W	Default	Description
31:28	R/W	3	reg_nr4_mc_alp1_sgn_lut0 : // unsigned , default = 3 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move
27:24	R/W	3	reg_nr4_mc_alp1_sgn_lut1 : // unsigned , default = 3 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move
23:20	R/W	3	reg_nr4_mc_alp1_sgn_lut2 : // unsigned , default = 3 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move
19:16	R/W	4	reg_nr4_mc_alp1_sgn_lut3 : // unsigned , default = 4 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move
15:12	R/W	5	reg_nr4_mc_alp1_sgn_lut4 : // unsigned , default = 5 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move

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Bit(s)	R/W	Default	Description
11: 8	R/W	6	reg_nr4_mc_alp1_sgn_lut5 : // unsigned , default = 6 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move
7: 4	R/W	7	reg_nr4_mc_alp1_sgn_lut6 : // unsigned , default = 7 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move
3: 0	R/W	8	reg_nr4_mc_alp1_sgn_lut7 : // unsigned , default = 8 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move

Table 9-1226 NR4_MCNR_ALP1_SGN_LUT2 0x371e

Bit(s)	R/W	Default	Description
31:28	R/W	9	reg_nr4_mc_alp1_sgn_lut8 : // unsigned , default = 9 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move
27:24	R/W	10	reg_nr4_mc_alp1_sgn_lut9 : // unsigned , default = 10 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move
23:20	R/W	11	reg_nr4_mc_alp1_sgn_lut10 : // unsigned , default = 11 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move
19:16	R/W	12	reg_nr4_mc_alp1_sgn_lut11 : // unsigned , default = 12 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move
15:12	R/W	13	reg_nr4_mc_alp1_sgn_lut12 : // unsigned , default = 13 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move
11: 8	R/W	14	reg_nr4_mc_alp1_sgn_lut13 : // unsigned , default = 14 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move
7: 4	R/W	15	reg_nr4_mc_alp1_sgn_lut14 : // unsigned , default = 15 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move
3: 0	R/W	15	reg_nr4_mc_alp1_sgn_lut15 : // unsigned , default = 15 alp1 vs x=abs|sgn(cur-pre)|, if x is small, less possibility of flat region move

Table 9-1227 NR4_RO_NM_SAD_SUM 0x371f

Bit(s)	R/W	Default	Description
31: 0	R.O	0	ro_nr4_nm_sad_sum : // unsigned , default = 0 sum of sad, for scene change detectcion, in noise meter

Table 9-1228 NR4_RO_NM_SAD_CNT 0x3720

Bit(s)	R/W	Default	Description
31: 0	R.O	0	ro_nr4_nm_sad_cnt : // unsigned , default = 0 cnt of sad, for scene change detectcion, in noise meter

Table 9-1229 NR4_RO_NM_VAR_SUM 0x3721

Bit(s)	R/W	Default	Description
31: 0	R.O	0	ro_nr4_nm_var_sum : // unsigned , default = 0 sum of var, for noise level detection, in noise meter

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Table 9-1230 NR4_RO_NM_VAR_SCNT 0x3722

Bit(s)	R/W	Default	Description
31: 0	R.O	0	ro_nr4_nm_var_cnt : // unsigned , default = 0 cnt of var, for noise level detection, in noise meter

Table 9-1231 NR4_RO_NM_VAR_MIN_MAX 0x3723

Bit(s)	R/W	Default	Description
21:12	R.O	1023	ro_nr4_nm_min_var : // unsigned , default = 1023 min of var, for noise level detection, in noise meter
9: 0	R.O	0	ro_nr4_nm_max_var : // unsigned , default = 0 max of var, for noise level detection, in noise meter

Table 9-1232 NR4_RO_NR4_DBGPIX_NUM 0x3724

Bit(s)	R/W	Default	Description
27: 0	R.O	0	ro_nr4_dbgpix_num : // unsigned , default = 0 number of pixels statistic invoved (removed?)

Table 9-1233 NR4_RO_NR4_BLDVS2_SUM 0x3725

Bit(s)	R/W	Default	Description
31: 0	R.O	0	ro_nr4_bld1vs2_sum : // unsigned , default = 0 sum of blend_1vs2 with the debug window

Table 9-1234 NR4_BLDVS3_SUM 0x3726

Bit(s)	R/W	Default	Description
31: 0	R.O	0	ro_nr4_bld12vs3_sum : // unsigned , default = 0 sum of blend_12vs3 with the debug window

Table 9-1235 NR4_COEF12_SUM 0x3727

Bit(s)	R/W	Default	Description
31: 0	R.O	0	ro_nr4_coef12_sum : // signed , default = 0 sum of coef_blt_blend12 with the debug window, under 8 bits precision

Table 9-1236 NR4_COEF123_SUM 0x3728

Bit(s)	R/W	Default	Description
31: 0	R.O	0	ro_nr4_coef123_sum : // signed , default = 0 sum of coef_final with the debug window, under 8 bits precision

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Table 9-1237 XLR_CTRL 0x3730

Bit(s)	R/W	Default	Description
22	R/W	1	reg_xlr_en : // unsigned , default = 1 enable bits for xlr function, 1: enable, 0: disable default = 1
21	R/W	1	reg_xlr_side_en : // unsigned , default = 1 enable to filter the above and below lines with xlr filter, default = 1
20	R/W	1	reg_xlr_3lines : // unsigned , default = 1 3 lines version enable default= 0
19:16	R/W	12	reg_xlr_simlp_gain : // unsigned , default = 12 gain to simlp to decide if need the XLR, default= 12
13: 8	R/W	6	reg_xlr_ooplp_gain : // unsigned , default = 6 gain to out-of-phase lp error to decide if need the XLR, birn to 16 as 1, default= 3
7: 0	R/W	64	reg_xlr_dislp_thrd : // unsigned , default = 64 threshold to lp error to discard XLR. default= 80

Table 9-1238 XLR_THRD 0x3731

Bit(s)	R/W	Default	Description
27:24	R/W	3	reg_xlr_txt_core : // unsigned , default = 3 coring to texture default = 3, (3/32)
23:16	R/W	5	reg_xlr_err_thrd2 : // unsigned , default = 5 threshold to error to decide blending coef, 0, 1/4, 1/2, 1.0, defaut= {20, 10, 5}
15: 8	R/W	10	reg_xlr_err_thrd1 : // unsigned , default = 10 threshold to error to decide blending coef, 0, 1/4, 1/2, 1.0, defaut= {20, 10, 5}
7: 0	R/W	20	reg_xlr_err_thrd0 : // unsigned , default = 20 threshold to error to decide blending coef, 0, 1/4, 1/2, 1.0, defaut= {20, 10, 5}

Table 9-1239 XLR_HCT_THRD 0x3732

Bit(s)	R/W	Default	Description
27:26	R/W	1	reg_xlr_hct_step : // unsigned , default = 1 horizontal chroma diff steps, 0: abs[-1 (2) -1]; 1: abs[-1 0 (2) 0 -1], 2: abs[-1 0 0 (2) 0 0 -1]; 3:abs[-1 0 0 0 (2) 0 0 0 -1]
25:24	R/W	1	reg_xlr_hct_lpf : // unsigned , default = 1 horizontal chroma diff low-pass filter enable, 0: no HLPF; 1: [1 2 1]; 2: max[-1:1]; 3: max[-2:2]
23:16	R/W	20	reg_xlr_hct_thr : // unsigned , default = 20 horizontal chroma diff threshold for xlr enable, to save the horozontal no color tran mode
15: 8	R/W	8	reg_xlr_sat_thr : // unsigned , default = 8 saturation threshold for xlr enable, the smaller of the threshold , the more will do xlr;
7: 2	R/W	3	reg_xlr_hmargin : // unsigned , default = 3 left/right number of pixels without xlr;
0	R/W	0	reg_xlr_hpf_only : // unsigned , default = 0 enable for only do xlr filter on high pass portion of the data, instead full data

Table 9-1240 NR_DB_FLT_CTRL 0x3738

Bit(s)	R/W	Default	Description
26	R/W	0	reg_nrdeband_reset1 : // unsigned , default = 0 0 : no reset seed 1: reload chroma seed
25	R/W	0	reg_nrdeband_reset0 : // unsigned , default = 0 0 : no reset seed 1: reload luma seed

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Bit(s)	R/W	Default	Description
24	R/W	0	reg_nrdeband_rgb : // unsigned , default = 0 0 : yuv 1: RGB
23	R/W	1	reg_nrdeband_en11 : // unsigned , default = 1 debanding registers of side lines, [0] for luma, same for below
22	R/W	1	reg_nrdeband_en10 : // unsigned , default = 1 debanding registers of side lines, [1] for chroma, same for below
21	R/W	1	reg_nrdeband_siderand : // unsigned , default = 1 options to use side two lines use the rand, instead of use for the YUV three component of middle line, 0: seed [3]/bandrand[3] for middle line yuv; 1: seed[3]/bandrand[3] for nearby three lines Y;
20	R/W	0	reg_nrdeband_randmode : // unsigned , default = 0 mode of rand noise adding, 0: same noise strength for all difs; else: strenght of noise will not exceed the difs, MIN((pPKReg->reg_nrdeband_bandrand[m]), noise[m])
19:17	R/W	6	reg_nrdeband_bandrand2 : // unsigned , default = 6
15:13	R/W	6	reg_nrdeband_bandrand1 : // unsigned , default = 6
11: 9	R/W	6	reg_nrdeband_bandrand0 : // unsigned , default = 6
7	R/W	1	reg_nrdeband_hpxor1 : // unsigned , default = 1 debanding random hp portion xor, [0] for luma
6	R/W	1	reg_nrdeband_hpxor0 : // unsigned , default = 1 debanding random hp portion xor, [1] for chroma
5	R/W	1	reg_nrdeband_en1 : // unsigned , default = 1 debanding registers, for luma
4	R/W	1	reg_nrdeband_en0 : // unsigned , default = 1 debanding registers, for chroma
3: 2	R/W	2	reg_nrdeband_lpf_mode1 : // unsigned , default = 2 lpf mode, 0: 3x3, 1:3x5; 2: 5x5; 3:5x7
1: 0	R/W	2	reg_nrdeband_lpf_mode0 : // unsigned , default = 2 lpf mode, 0: 3x3, 1:3x5; 2: 5x5; 3:5x7

Table 9-1241 NR_DB_FLT_YC_THRD 0x3739

Bit(s)	R/W	Default	Description
31:28	R/W	9	reg_nrdeband_luma_th3 : // unsigned , default = 9 threshold to |Y-Ylpf|, if < th [0] use lpf
27:24	R/W	7	reg_nrdeband_luma_th2 : // unsigned , default = 7 elseif <th[1] use (lpf*3 + y)/4
23:20	R/W	6	reg_nrdeband_luma_th1 : // unsigned , default = 6 elseif <th[1] use (lpf*3 + y)/ 4elseif < th[2] (lpf*1 + y)/2
19:16	R/W	5	reg_nrdeband_luma_th0 : // unsigned , default = 5 elseif <th[1] use (lpf*3 + y)/ 4elseif elseif < th[3] (lpf*1 + 3*y)/4; else
15:12	R/W	9	reg_nrdeband_chrm_th3 : // unsigned , default = 9 threshold to |Y-Ylpf|, if < th [0] use lpf
11: 8	R/W	7	reg_nrdeband_chrm_th2 : // unsigned , default = 7 elseif < th[1] use (lpf*3 + y)/ 4
7: 4	R/W	6	reg_nrdeband_chrm_th1 : // unsigned , default = 6 elseif < th[1] use (lpf*3 + y)/ 4elseif <th[2] (lpf*1 + y)/2
3: 0	R/W	5	reg_nrdeband_chrm_th0 : // unsigned , default = 5 elseif < th[1] use (lpf*3 + y)/ 4elseif elseif

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Table 9-1242 NR_DB_FLT_RANDLUT 0x373a

Bit(s)	R/W	Default	Description
23:21	R/W	1	reg_nrdeband_randslut7 : // unsigned , default = 1 lut0
20:18	R/W	1	reg_nrdeband_randslut6 : // unsigned , default = 1 lut0
17:15	R/W	1	reg_nrdeband_randslut5 : // unsigned , default = 1 lut0
14:12	R/W	1	reg_nrdeband_randslut4 : // unsigned , default = 1 lut0
11: 9	R/W	1	reg_nrdeband_randslut3 : // unsigned , default = 1 lut0
8: 6	R/W	1	reg_nrdeband_randslut2 : // unsigned , default = 1 lut0
5: 3	R/W	1	reg_nrdeband_randslut1 : // unsigned , default = 1 lut0
2: 0	R/W	1	reg_nrdeband_randslut0 : // unsigned , default = 1 lut0

Table 9-1243 NR_DB_FLT_PXI_THRD 0x373b

Bit(s)	R/W	Default	Description
25:16	R/W	0	reg_nrdeband_yc_th1 : // unsigned , default = 0 to luma/|u/v| for using the denoise
9: 0	R/W	0	reg_nrdeband_yc_th0 : // unsigned , default = 0 to luma/|u/v| for using the denoise

Table 9-1244 NR_DB_FLT_SEED_Y 0x373c

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8240	reg_nrdeband_seed0 : // unsigned , default = 1621438240 noise adding seed for Y. seed[0]= 0x60a52f20; as default

Table 9-1245 NR_DB_FLT_SEED_U 0x373d

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8247	reg_nrdeband_seed1 : // unsigned , default = 1621438247 noise adding seed for U. seed[0]= 0x60a52f27; as default

Table 9-1246 NR_DB_FLT_SEED_V 0x373e

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8242	reg_nrdeband_seed2 : // unsigned , default = 1621438242 noise adding seed for V. seed[0]= 0x60a52f22; as default

Table 9-1247 NR_DB_FLT_SEED3 0x373f

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8242	reg_nrdeband_seed3 : // unsigned , default = 1621438242 noise adding seed for V. seed[0]= 0x60a52f22; as default

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9.2.3.17 VIUB Top-Level Registers

Table 9-1248 VIU_SW_RESET 0x1a01

Bit(s)	R/W	Default	Description
29	R/W	0	di_dsr1to2_reset : // unsigned , default = 0
28	R/W	0	vd2_lbuf_reset : // unsigned , default = 0
27	R/W	0	afbc_dec1_reset : // unsigned , default = 0
26	R/W	0	vd2_reset : // unsigned , default = 0
25	R/W	0	vd1_lbuf_reset : // unsigned , default = 0
24	R/W	0	afbc_dec0_reset : // unsigned , default = 0
23	R/W	0	vd1_reset : // unsigned , default = 0
22	R/W	0	osd1_afbcd_regs_reset : // unsigned , default = 0
21	R/W	0	osd1_afbcd_logic_reset : // unsigned , default = 0 Only active when MALI_AFBCD_TOP_CTRL[23] high
20	R/W	0	afbc_arb_reg_reset : // unsigned , default = 0
19	R/W	0	afbc_arb_reset : // unsigned , default = 0
17	R/W	0	osd4_reset : // unsigned , default = 0
16	R/W	0	osd3_reset : // unsigned , default = 0
15	R/W	0	osd2_reset : // unsigned , default = 0
14	R/W	0	osd1_reset : // unsigned , default = 0
12	R/W	0	vpp_axi_reset : // unsigned , default = 0
8	R/W	0	osd24bld_reset : // unsigned , default = 0
7	R/W	0	osd13bld_reset : // unsigned , default = 0
6	R/W	0	prime_reset : // unsigned , default = 0
5	R/W	0	hist_spl_reset : // unsigned , default = 0
4	R/W	0	ldim_stts_reset : // unsigned , default = 0
3	R/W	0	dolby1b_reset : // unsigned , default = 0
2	R/W	0	dolby1a_reset : // unsigned , default = 0
1	R/W	0	dolby0_reset : // unsigned , default = 0
0	R/W	0	vpp_reset : // unsigned , default = 0

Table 9-1249 VIU_SW_RESET0 0x1a02

Bit(s)	R/W	Default	Description
2	R/W	0	software : reset for mcinford_mif // unsigned , default = 0
1	R/W	0	software : reset for mcinfowr_mif // unsigned , default = 0
0	R/W	0	software : reset for mcvecrd_mif // unsigned , default = 0

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Table 9-1250 VIU_SECURE_REG 0x1a04

Bit(s)	R/W	Default	Description
30-26	R/W	0	Dolby prime secure
25	R/W	0	Vpp probe function: 1:probe enable 0:disable
24	R/W	0	Dolby core3
23-16	R/W	0	Osd test data
9	R/W	0	Write back 1
8	R/W	0	Write back 0
7	R/W	0	Afbc dec1
6	R/W	0	Vd2 mif
5	R/W	0	Afbc dec0
4	R/W	0	Vd1 mif
2	R/W	0	Osd3 : // unsigned , default = 0
1	R/W	0	Osd2 : // unsigned , default = 0
0	R/W	0	osd1 : // unsigned , default = 0

Table 9-1251 DOLBY_INT_STAT 0x1a05

Bit(s)	R/W	Default	Description
3:0	R/W	0	dolby_int_state : // unsigned , default = 0

Table 9-1252 VIU_MISC_CTRL0 0x1a06

Bit(s)	R/W	Default	Description
8	R/W	0	vsync_int_ctrl : default = 0
0	R/W	0	scan_reg : default = 0

Table 9-1253 VIU_MISC_CTRL1 0x1a07

Bit(s)	R/W	Default	Description
31:0	R/W	0	viu_misc_ctrl1 : // unsigned , default = 0

Table 9-1254 VIU_SECURE_REG1 0x1a08

Bit(s)	R/W	Default	Description
31:0	R/W	0	viu_secure_reg1 : // unsigned , default = 0

Table 9-1255 VIU_SECURE_REG2 0x1a09

Bit(s)	R/W	Default	Description
31:0	R/W	0	viu_secure_reg2 : // unsigned , default = 0

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Table 9-1256 VD1_AFBCD0_MISC_CTRL 0x1a0a

Bit(s)	R/W	Default	Description
22	R/W	0	Vd1_afbc0_mem_sel 0: vd_mif share afbc_memory 1: afbc_mif share afbc_ memory
21:20	R/W	0	Afbc_mif_go_field_sel : // unsigned , default = 0 0: go_file 1: go_field_post 2: go_ filed_pre
19:18	R/W	0	vd1_mif_go_field_sel : // unsigned , default = 0 0: go_file 1: go_field_post 2: go_ filed_pre
16	R/W	0	vd1_lbuf_ram_sel : // unsigned , default = 0 0: NO share ram 1: afbc0 share ext ram
15:14	R/W	0	vd1_in_mux_sel : // unsigned , default = 0 0: vd1 to dobly 2: vd1 to primel
13:12	R/W	0	vd1_axi_sel : // unsigned , default = 0 0: afbc0 mif to axi 1: vd1 mif to axi
11	R/W	0	afbc0_osd3_mux_vd1 : // unsigned , default = 0 0: afbc0 to vd1 1: osd3 to vd1
10	R/W	0	afbc_vd1_sel : // unsigned , default = 0 0: vd1_mif to vpp 1: afbc0_mif
9	R/W	0	afbc0_mux_vpp_mad : // unsigned , default = 0 0: afbc0 to vpp 1: afbc0 to di
8	R/W	0	di_mif0_en : // unsigned , default = 0 0: select mif to vpp 1: mif to di
7:0	R/W	0	afbc0_gclk_ctrl : // unsigned , default = 0

Table 9-1257 VD2_AFBCD1_MISC_CTRL 0x1a0b

Bit(s)	R/W	Default	Description
31:24	R/W	0	vd2_osd_mux_alpha : // unsigned , default = 0 config vd2_osd alpha value.
22	R/W	0	Vd2_afbc1_mem_sel 0: vd2_mif share afbc_memory 1: afbc1_mif share afbc_ memory
21:20	R/W	0	Vd2_afbc1_go_field_sel : // unsigned , default = 0 0: go_file 1: go_field_post 2: go_filed_pre
19:18	R/W	0	Vd2_mif_go_field_sel : // unsigned , default = 0 0: go_file 1: go_field_post 2: go_ filed_pre
16	R/W	0	vd2_lbuf_ram_sel : // unsigned , default = 0 0: NO share ram 1: afbc1 share ext ram
15:14	R/W	0	vd2_in_mux_sel : // unsigned , default = 0 0: afbc2_vd2 to vd2 2: osd4 to vd2
13:12	R/W	0	vd2_axi_sel : // unsigned , default = 0 0: afbc1 mif to axi 1: vd2 mif to axi
11	R/W	0	afbc1_osd4_mux_vd1 : // unsigned , default = 0 0: afbc1 to vd1 1: osd4 to vd2
10	R/W	0	afbc_vd2_sel : // unsigned , default = 0 0: vd2_mif to vpp 1: afbc1_mif
9	R/W	0	afbc1_mux_vpp_mad : // unsigned , default = 0 0: afbc1 to vpp 1: afbc1 to di
8	R/W	0	afbc_2mad_out_sel : // unsigned , default = 0 0: select vd1 to di 1: vd2 to di
8:0	R/W	0	Afbc1_gclk_ctrl : // unsigned , default = 0

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Table 9-1258 DOLBY_PATH_CTRL 0x1a0c

Bit(s)	R/W	Default	Description
27:26	R/W	3	vd2_out_mux_sel // dolby_wrap_vd2_out from: 3:dolby_s1 2:primesl 1:dolnb_tv 0:dolby_s0
25:24	R/W	0	vd1_out_mux_sel // dolby_wrap_vd1_out from: 3:dolby_s1 2:primesl 1:dolnb_tv 0:dolby_s0
23	R/W	1	dolby_s1_out_swop //chose dst data 0:to vd1 1:to vd2
22	R/W	0	primesl_out_sel //chose dst data 0:to vd1 1:to vd2
21	R/W	0	dolby_s0_out_swop //chose dst data 0:to vd1 1:to vd2
20	R/W	0	dolby_tv_out_swop //chose dst data 0:to vd1 1:to vd2
19	R/W	1	dolby_s1_in_swop //chose src data 0:from vd1 1:from vd2
18	R/W	0	primesl_in_sel //chose src data 0:from vd1 1:from vd2
17	R/W	0	dolby_s0_in_swop //swap src data 0:bl el 1:bl el swap
16	R/W	0	dolby_tv_in_swop //swap src data 0:bl el 1:bl el swap
12	R/W	0	dolby_bl_el_swop // 0:vd1–>dolby_wrap_vd1 vd2–>dolby_wrap_vd2 1:vd1–>dolby_wrap_vd2 vd2–>dolby_wrap_vd1
11:10	R/W	3	dolby_el_mux_seld // dolby_wrap_vd2_in go to: 3:dolby_s1 2:primesl_vd2 1:dolnb_tv_el 0:dolby_s0_el
9:8	R/W	0	dolby_bl_mux_sel // dolby_wrap_vd1_in go to: 3:dolby_s1 2:primesl_vd1 1:dolnb_tv_bl 0:dolby_s0_bl
7	R/W	0	vpp_osd2_ext_mod : // unsigned , default = 0 // 0: 12bits 1: 10bits
6	R/W	0	vpp_osd1_ext_mod : // unsigned , default = 0 // 0: 12bits 1: 10bits
5	R/W	0	dolby1_vd2_ext_mod : // unsigned , default = 0 // 0: 12bits 1: 10bits
4	R/W	0	dolby0_vd1_ext_mod : // unsigned , default = 0 // 0: 12bits 1: 10bits
3	R/W	0	Osd2_dolby_bypass_en : // unsigned , default = 0
2	R/W	0	Osd1_dolby_bypass_en
1	R/W	0	Vd2_dolby_bypass_en
0	R/W	0	Vd1dolby_bypass_en

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Table 9-1259 WR_BACK_MISC_CTRL 0x1a0d

Bit(s)	R/W	Default	Description
1	R/W	0	wrbak_chan1_hsyn_en : // unsigned , default = 0 vd1 wrbak hsync enable
0	R/W	0	wrbak_chan0_hsyn_en : // unsigned , default = 0 vd0 wrbak hsync enable

Table 9-1260 OSD_PATH_MISC_CTRL 0x1a0e

Bit(s)	R/W	Default	Description
7:4	R/W	0	osd_axi_sel : // unsigned , default = 0 osd_axi_sel[0] 1:OSD1 get data from mali_afbcd 0: OSD1 get data from DDR osd_axi_sel[1] 1:OSD2 get data from mali_afbcd 0: OSD2 get data from DDR osd_axi_sel[2] 1:OSD3 get data from mali_afbcd 0: OSD3 get data from DDR osd_axi_sel[3] reserved
3	R/W	0	osd4_in_mux_sel : // unsigned , default = 0 0: osd4 to vpp 1: vd2_osd4 to vpp
2	R/W	0	osd4_mux_vpp_vd2 : // unsigned , default = 0 0: osd4 to vpp 1: osd4 to vd2
1	R/W	0	osd3_in_mux_sel : // unsigned , default = 0 0: osd3 to vpp 1: vd2_osd3 to vpp
0	R/W	0	osd3_mux_vpp_vd1 : // unsigned , default = 0 0: osd3 to vpp 1: osd3 to vd1

Table 9-1261 MALI_AFBCD_TOP_CTRL 0x1a0f

Bit(s)	R/W	Default	Description
31	R.O	0	ro_mali_dec_active : // unsigned , default = 0
23	R/W	0	Mali afbcd logic rst mode 1:logic rest controll by VIU_SW_RESET[21] 0:logic reset by vsync singal,don’t need software process
17:12	R/W	0	gclk_ctrl_osd1_afbcd : // unsigned , default = 0 mail afbc gate clock
8	R/W	1	axim_data_128b : // unsigned , default = 1 0: axi bus width=64 1: 128bit
6:4	R/W	7	axim_max_len : // unsigned , default = 7
2:0	R/W	5	axim_outstanding_trans : // unsigned , default =5

Table 9-1262 VIU_GCLK_CTRL 0x1a4f

Bit(s)	R/W	Default	Description
7:0	R/W	0	viu_gclk_ctrl : // unsigned , default =0

9.2.3.18 VPP_ARB_CTRL Registers

Table 9-1263 VPP_AFBC_RDARB_MODE 0x3970

Bit(s)	R/W	Default	Description
31-24	R/W	0	unused
23-20	R/W	0	Rdarb_sel

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Bit(s)	R/W	Default	Description
16	R/W	0	Rdarb_arb_mode
1-0	R/W	0	Rdarb_gate_clk_ctrl

Table 9-1264 VPP_AFBC_RDARB_REQEN_SLV 0x3971

Bit(s)	R/W	Default	Description
3-0	R/W	0	Rdarb_dc_req_en 1: Request is valid, 0: Invalid Bit0 : osd1 Bit1 : osd2 Bit2 : osd3 Bit3 : osd4

Table 9-1265 VPP_AFBC_RDARB_WEIGHT0_SLV 0x3972

Bit(s)	R/W	Default	Description
23-0	R/W	0	Rddc_weigh_sxn

Table 9-1266 VPP_AFBC_ARB_DBG_CTRL 0x3974

Bit(s)	R/W	Default	Description
31-0	RO	0	Det_cmd_ctrl

Table 9-1267 VPP_RDARB_MODE 0x3978

Bit(s)	R/W	Default	Description
27-20	R/W	0	Rdarb_sel 1: Request is valid, 0: Invalid Bit20: osd1 Bit21: osd2 Bit22: vd1 Bit23: vd2 Bit24: osd3 Bit25: osd4 Bit26: dolby0 Bit27:mali_afbc
17:16	R/W	0	Rdarb_arb_mode
3-0	R/W	0	Rdarb_gate_clk_ctrl

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Table 9-1268 VPP_RDARB_REQEN_SLV 0x3979

Bit(s)	R/W	Default	Description
15-0	R/W	0	Rdarb_dc_req_en 1: Request is valid, 0: Invalid Bit0: osd1 come from axi_port0 Bit1: osd2 come from axi_port0 Bit2: vd1 come from axi_port0 Bit3: vd2 come from axi_port0 Bit4: osd3 come from axi_port0 Bit5: osd4 come from axi_port0 Bit6: dolby0 come from axi_port0 Bit7:mali_afbc come from axi_port0 Bit8: osd1 come from axi_port1 Bit9: osd2 come from axi_port1 Bit10: vd1 come from axi_port1 Bit11: vd2 come from axi_port1 Bit12: osd3 come from axi_port1 Bit13: osd4 come from axi_port1 Bit14: dolby0 come from axi_port1 Bit15:mali_afbc come from axi_port1

Table 9-1269 VPP_RDARB_WEIGHT0_SLV 0x397a

Bit(s)	R/W	Default	Description
29-0	R/W	0	Rddc_weigh_sxn

Table 9-1270 VPP_RDARB_WEIGHT1_SLV 0x397b

Bit(s)	R/W	Default	Description
17-0	RO	0	Rddc_weigh_sxn

Table 9-1271 VPP_ARB_DBG_CTRL 0x397c

Bit(s)	R/W	Default	Description
31-0	RO	0	Det_cmd_ctrl

9.2.3.19 VD1 Path vd_rmem_if0 Registers

Table 9-1272 VD1_IF0_GEN_REG 0x4800

Bit(s)	R/W	Default	Description
31	R/W	0	ENABLE_FREE_CLK. 0: Gated clock for power saving 1: Free-running clock to drive logic
30	R/W	0	SW_RESET: Write 1 to this bit to generate a pulse to reset everything except registers.
29	R/W	0	RESET_ON_GO_FIELD: Define whether to reset state machines on go_field pulse. 0: No reset on go_field 1: go_field reset everything except registers
28	R/W	0	URGENT_CHROMA: Set urgent level for chroma fifo request from DDR. 0: Non urgent

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Bit(s)	R/W	Default	Description
			1: Urgent
27	R/W	0	URGENT_LUMA: Set urgent level for luma fifo request from DDR. 0: Non urgent 1: Urgent
26	R/W	0	Chroma_end_at_last line: For chroma line, similar to luma_end_at_last_line, as below. Not used if data are stored together in one canvas.
25	R/W	0	Luma_end_at_last_line: Control whether continue outputting luma line past last line. 0: Repeat the last line or dummy pixels, after past the last line 1: Stop outputting data, once past the last line.
24-19	R/W	4	Hold_lines: After go_field, the number of lines to hold before the module is enabled.
18	R/W	0	LAST_LINE: This bit controls whether we simply repeat the last line or we push dummy pixels. ‘1’ tells the state-machines to repeat the last line using the dummy pixels defined in the register below. ‘0’ indicates that the state-machine should re-read the last line of real data.
17	R	0	Busy status of the state-machines. ‘1’ = busy, ‘0’ = idle
16	R/W	0	DEMUX_MODE: 0 = 4:2:2, 1 = RGB (24-bit). This value is used to control the de-muxing logic when the picture is stored together. When a picture is stored together, the data is read into a single FIFO (the Y FIFO) and must be demultiplexed into the “drain” outputs. In the case of 4:2:2 the data is assumed to be stored in memory in 16-bit chunks: <YCb><YCr><YCb><YCr>,… the Y, Cb and Cr 8-bit values are pulled from the single Y-FIFO and sent out in pairs. This value is only valid when the picture is stored together. If the picture is separated into different canvases, then this bit field is ignored.
15-14	R/W	0	BYTES_PER_PIXEL: This value is used to determine how many bytes are associated with each pixel. 0: This value should be used if the image is stored separately (e.g. RGB or Y, Cb, Cr). 1: This value should be used if the data is 4:2:2 data stored together. In this case each pixel , YCb or YCr, is 16-bits (two bytes). 2: This value should be used if the RGB (24-bit) data is stored together. 3: reserved for future use (alpha RGB).
13-12	R/W	0	DDR_BURST_SIZE_CR: This value is used to control the DDR burst request size for the Cr FIFO. 0: Maximum burst = 24 64-bit values 1: Maximum burst = 32 64-bit values 2: Maximum burst = 48 64-bit values 3: Maximum burst = 64 64-bit values
11-10	R/W	0	DDR_BURST_SIZE_CB: This value is used to control the DDR burst request size for the Cb FIFO. 0: Maximum burst = 24 64-bit values 1: Maximum burst = 32 64-bit values 2: Maximum burst = 48 64-bit values 3: Maximum burst = 64 64-bit values
9-8	R/W	0	DDR_BURST_SIZE_Y: This value is used to control the DDR burst request size for the Y FIFO. 0: Maximum burst = 24 64-bit values 1: Maximum burst = 32 64-bit values 2: Maximum burst = 48 64-bit values 3: Maximum burst = 64 64-bit values
7	R/W	0	MANUAL_START_FRAME: non-latching bit that can be used to simulate the go_ field signal for simulation.
6	R/W	0	CHRO_RPT_LASTL_CTRL: This bit controls whether to allow VPP’s chroma-repeat request.

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Bit(s)	R/W	Default	Description
			0: Chroma-repeat pulses from VPP are ignored 1: Chroma-repeat pulses from VPP are used.
5	R/W	0	Unused
4	R/W	0	LITTLE_ENDIAN: This bit defines the endianess of the memory data . 0: Pixel data are stored big-endian in memory 1: Pixel data are stored little-endian in memory
3	R/W	0	Chroma_hz_avg: For chroma line output control, similar to luma_hz_avg, as below. Not used if data are stored together in one canvas.
2	R/W	0	Luma_hz_avg: Enable output half amount of data per line to save bandwidth. 0: Output every pixel per line 1: Output half line, each data averaged between every 2 pixels Note: For 4:2:2 mode data stored together in one canvas, only do averaging over luma data.
1	R/W	0	SEPARATE_EN: Set this bit to 1 if the image is in separate canvas locations.
0	R/W	0	ENABLE: This bit is set to 1 to enable the FIFOs and other logic. This bit can be set to 0 to cleanup and put the logic into an IDLE state.

Table 9-1273 VD1_IF0_CANVAS0 – Picture 0 0x4801

Bit(s)	R/W	Default	Description
31-24	R/W	0	unused
23-16	R/W	0	CANVAS0_ADDR2: Canvas table address for picture 0 for component 2 (Cr FIFO). This value is ignored when the picture is stored together
15-8	R/W	0	CANVAS0_ADDR1: Canvas table address for picture 0 for component 1 (Cb FIFO). This value is ignored when the picture is stored together
7-0	R/W	0	CANVAS0_ADDR0: Canvas table address for picture 0 for component 0 (Y FIFO).

Table 9-1274 VD1_IF0_CANVAS1 – Picture 1 0x4802

Bit(s)	R/W	Default	Description
31-24	R/W	0	unused
23-16	R/W	0	CANVAS1_ADDR2: Canvas table address for picture 1 for component 2 (Cr FIFO). This value is ignored when the picture is stored together
15-8	R/W	0	CANVAS1_ADDR1: Canvas table address for picture 1 for component 1 (Cb FIFO). This value is ignored when the picture is stored together
7-0	R/W	0	CANVAS1_ADDR0: Canvas table address for picture 1 for component 0 (Y FIFO).

Table 9-1275 VD1_IF0_LUMA_X0 – Picture 0 0x4803

Bit(s)	R/W	Default	Description
31	R/W	0	Unused
30-16	R/W	0	LUMA_X_END0: Picture 0, luma X end value
15	R/W	0	Unused
14-0	R/W	0	LUMA_X_START0: Picture 0, luma X start value

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Table 9-1276 VD1_IF0_LUMA_Y0 – Picture 0 0x4804

Bit(s)	R/W	Default	Description
31-29	R/W	0	Unused
28-16	R/W	0	LUMA_Y_END0: Picture 0, luma Y end value
15-13	R/W	0	Unused
12-0	R/W	0	LUMA_Y_START0: Picture 0, luma Y start value

Table 9-1277 VD1_IF0_CHROMA_X0 – Picture 0 0x4805

Bit(s)	R/W	Default	Description
31	R/W	0	Unused
30-16	R/W	0	CHROMA_X_END0: Picture 0, chroma X end value. This value is only used when the picture is not stored together.
15	R/W	0	Unused
14-0	R/W	0	CHROMA _X_START0: Picture 0, chroma X start value. This value is only used when the picture is not stored together.

Table 9-1278 VD1_IF0_ CHROMA_Y0 – Picture 0 0x4806

Bit(s)	R/W	Default	Description
31-29	R/W	0	Unused
28-16	R/W	0	CHROMA _Y_END0: Picture 0, chroma Y end value. This value is only used when the picture is not stored together.
15-13	R/W	0	Unused
12-0	R/W	0	CHROMA _Y_START0: Picture 0, chroma Y start value. This value is only used when the picture is not stored together.

Table 9-1279 VD1_IF0_LUMA_X1 – Picture 1 0x4807

Bit(s)	R/W	Default	Description
31	R/W	0	Unused
30-16	R/W	0	LUMA_X_END1: Picture 1, luma X end value
15	R/W	0	Unused
14-0	R/W	0	LUMA_X_START1: Picture 1, luma X start value

Table 9-1280 VD1_IF0_LUMA_Y1 – Picture 1 0x4808

Bit(s)	R/W	Default	Description
31-29	R/W	0	Unused
28-16	R/W	0	LUMA_Y_END1: Picture 1, luma Y end value

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Bit(s)	R/W	Default	Description
15-13	R/W	0	Unused
12-0	R/W	0	LUMA_Y_START1: Picture 1, luma Y start value

Table 9-1281 VD1_IF0_CHROMA_X1 – Picture 1 0x4809

Bit(s)	R/W	Default	Description
31	R/W	0	Unused
30-16	R/W	0	CHROMA_X_END1: Picture 1, chroma X end value. This value is only used when the picture is not stored together.
15	R/W	0	Unused
14-0	R/W	0	CHROMA _X_START1: Picture 1, chroma X start value. This value is only used when the picture is not stored together.

Table 9-1282 VD1_IF0_ CHROMA_Y1 – Picture 1 0x480A

Bit(s)	R/W	Default	Description
31-29	R/W	0	Unused
28-16	R/W	0	CHROMA _Y_END1: Picture 1, chroma Y end value. This value is only used when the picture is not stored together.
15-13	R/W	0	Unused
12-0	R/W	0	CHROMA _Y_START1: Picture 1, chroma Y start value. This value is only used when the picture is not stored together.

Table 9-1283 VD1_IF0_REPEAT_LOOP – Pictures 0 and 1 0x480B

Bit(s)	R/W	Default	Description
31-24	R/W	0	CHROMA_RPT_LOOP1: Repeat loop for Picture 1. Bits[6:4] = start loop pointer, bits [2:0] = end loop pointer. Bits [7] and [3] are ignored.
23-16	R/W	0	LUMA_RPT_LOOP1: Repeat loop for Picture 1. Bits[6:4] = start loop pointer, bits [2:0] = end loop pointer. Bits [7] and [3] are ignored.
15-8	R/W	0	CHROMA_RPT_LOOP0: Repeat loop for Picture 0. Bits[6:4] = start loop pointer, bits [2:0] = end loop pointer. Bits [7] and [3] are ignored.
7-0	R/W	0	LUMA_RPT_LOOP0: Repeat loop for Picture 0. Bits[6:4] = start loop pointer, bits [2:0] = end loop pointer. Bits [7] and [3] are ignored.

Table 9-1284 VD1_IF0_LUMA0_RPT_PAT – Picture 0 LUMA repeat pattern 0x480C

Bit(s)	R/W	Default	Description
31-0	R/W	0	Luma repeat/skip pattern for picture 0

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Bits	Pattern Index	Pattern description
31-28	7	Repeat/skip pattern: Bit[3] = 0 indicates repeat. Bit[3] = 1 indicates either skip, or output this line and then skip. How to interpret this bit depends on the value of the previous pattern's Bit[3]. If previous Bit[3]=0, then skip; If previous Bit[3]=1, then output this line and then skip. Bits[2:0] indicate the skip / repeat count. Blow is an example of consecutive patterns, the start line is line 0: {0010} Repeat this line (line 0) two more times for a total of three line reads. Proceed to next line (line 1). {0000} Don't repeat this line (line 1). This line will be read just once. Proceed to next line (line 2). {1000} Skip one line (line 2) to get to the next line (line 3). The skip implies that the next line (line 3) should be read at least once. {1011} Read this line (line 3) once, and then skip the next four lines to get to the next line (line 8). The skip implies that the next line (line 8) should be read at least once. {0100} Repeat this line (line 8) four more times for a total of five line read. Proceed to next line (line 9). {1001} Skip two lines to get to the next line (line 11). The skip implies that the next line (line 11) should be read at least once.
27-24	6	See pattern definition above.
23-20	5	See pattern definition above.
19-16	4	See pattern definition above.
15-12	3	See pattern definition above.
11-8	2	See pattern definition above.
7-4	1	See pattern definition above.
3-0	0	See pattern definition above.

Table 9-1285 VD1_IF0_CHROMA0_RPT_PAT – Picture 0 CHROMA repeat pattern 0x480D

Bit(s)	R/W	Default	Description
31-0	R/W	0	Chroma repeat/skip pattern for picture 0. See picture 0 luma pattern for description. This value is only used when the picture is not stored together.

Table 9-1286 VD1_IF0_LUMA1_RPT_PAT – Picture 1 LUMA repeat pattern 0x480E

Bit(s)	R/W	Default	Description
31-0	R/W	0	Luma repeat/skip pattern for picture 1. See picture 0 luma pattern for description.

Table 9-1287 VD1_IF0_CHROMA1_RPT_PAT – Picture 1 CHROMA repeat pattern 0x480F

Bit(s)	R/W	Default	Description
31-0	R/W	0	Chroma repeat/skip pattern for picture 1. See picture 0 luma pattern for description. This value is only used when the picture is not stored together.

Table 9-1288 VD1_IF0_LUMA_PSEL – Picture 0 and 1's LUMA 0x4810

Bit(s)	R/W	Default	Description
31-28	R/W	0	unused
27-26	R/W	0	Luma_psel_mode: controls whether it's single-picture or two-picture mode. {00} Only picture 0 is used. Ignore settings defined in Luma_psel_last_line, Luma_psel_pattern and Luma_psel_loop.

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Bit(s)	R/W	Default	Description
			{01} Only picture 1 is used. Ignore settings defined in Luma_psel_last_line, Luma_psel_pattern and Luma_psel_loop. {1x} Two-picture mode.
25-24	R/W	0	Luma_psel_last_line: select which picture's last line to output, during repeat last line mode. Bit[0]=0, when picture 0 past the last line, use picture 0's last line during repeat last line mode; Bit[0]=1, when picture 0 past the last line, use picture 1's last line during repeat last line mode; Bit[1]=0, when picture 1 past the last line, use picture 0's last line during repeat last line mode; Bit[1]=1, when picture 1 past the last line, use picture 1's last line during repeat last line mode.
23-8	R/W	0	Luma_psel_pattern. If the value of the bit pointed by the loop pointer is 0, output picture 0's luma line, if the bit value is 1, output picture 1's luma line.
7-4	R/W	0	Luma_psel_loop start pointer.
3-0	R/W	0	Luma_psel_loop end pointer.

Table 9-1289 VD1_IF0_CHROMA_PSEL – Picture 0 and 1's CHROMA 0x4811

Bit(s)	R/W	Default	Description
31-28	R/W	0	unused
27-26	R/W	0	Chroma_psel_mode: see luma_psel_mode. This value is only used when the picture is not stored together.
25-24	R/W	0	Chroma_psel_last_line: See luma_psel_last_line. This value is only used when the picture is not stored together.
23-8	R/W	0	Chroma_psel_pattern. If the value of the bit pointed by the loop pointer is 0, output picture 0's chroma line, if the bit value is 1, output picture 1's chroma line. This value is only used when the picture is not stored together.
7-4	R/W	0	Chroma_psel_loop start pointer. This value is only used when the picture is not stored together.
3-0	R/W	0	Chroma_psel_loop end pointer. This value is only used when the picture is not stored together.

Table 9-1290 VD1_IF0_DUMMY_PIXEL 0x4812

Bit(s)	R/W	Default	Description
31-24	R/W	0x00	Y or R dummy pixel value ,8bit
23-16	R/W	0x80	Cb or G dummy pixel value ,8bit
15-8	R/W	0x80	Cr or B dummy pixel value ,8bit
7-0	R/W	0	unused

VD1_RANGE_MAP_Y 0x481A

VD1_RANGE_MAP_CB 0x481B

VD1_RANGE_MAP_CR 0x481C

Output data range conversion function:

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Y [n] = clip (Round (((Y [n] +DIN_OFFSET) * RANGE_MAP_COEF) / (1<<RANGE_MAP_SR)) +DOUT_OFFSET);

To perform VC-1 range reduction, set the following:

DIN_OFFSET = 0x180 = -128;

RANGE_MAP_COEF = RANGE_MAPY + 9

RANGE_MAP_SR = 3

DOUT_OFFSET = 0x080 = 128

To get the equivalent function:

Y[n] = clip((((Y[n]-128) * (RANGE_MAPY + 9) + 4) >> 3) +128);

Bit(s)	R/W	Default	Description
31-23	R/W	0	DIN_OFFSET
22-15	R/W	0	RANGE_MAP_COEF
14	R/W	0	unused
13-10	R/W	0	RANGE_MAP_SR
9-1	R/W	0	DOUT_OFFSET
0	R/W	0	RANGE_MAP_EN

Table 9-1291 VD1_IF0_GEN_REG2 0x481D

Bit(s)	R/W	Default	Description
31-2	R/W	0	unused
1-0	R/W	0	COLOR_MAP: Define color map for NV12 or NV21 mode. Only applicable when VD1_IF0_GEN_REG.SEPARATE_EN = 1. 0: NOT NV12 or NV21; 1: NV12 (CbCr); 2: NV21 (CrCb).

Table 9-1292 VD1_IF0_GEN_REG3 0x4816

Bit(s)	R/W	Default	Description
11-10	R/W	0	cntl_dbg_mode
9-8	R/W	0	cntl_bits_mode : 0->8bit 1->10bit 422 2->10bit 444
6-4	R/W	3	cntl_blk_len
2-1	R/W	1	cntl_burst_len
0	R/W	1	cntl_64bit_rev

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Table 9-1293 VIU_VD1_FMT_CTRL 0x4818

Bit(s)	R/W	Default	Description
31	R/W	0	gate_clk_en. 0=No clock gating, free-running; 1=Enable clock gating for power saving.
30	R/W	0	soft_rst. If true, reset formatters.
29	R/W	0	unused
28	R/W	0	if true, horizontal formatter use repeating to generete pixel, otherwise use bilinear interpolation
27-24	R/W	0	horizontal formatter initial phase
23	R/W	0	horizontal formatter repeat pixel 0 enable
22-21	R/W	0	horizontal Y/C ratio, 00: 1:1, 01: 2:1, 10: 4:1
20	R/W	0	horizontal formatter enable
19	R/W	0	if true, always use phase0 while vertical formater, meaning always repeat data, no interpolation
18	R/W	0	if true, disable vertical formatter chroma repeat last line
17	R/W	0	veritcal formatter dont need repeat line on phase0, 1: enable, 0: disable
16	R/W	0	veritcal formatter repeat line 0 enable
15-12	R/W	0	vertical formatter skip line num at the beginning
11-8	R/W	0	vertical formatter initial phase
7-1	R/W	0	vertical formatter phase step (3.4)
0	R/W	0	vertical formatter enable

Table 9-1294 VIU_VD1_FMT_W 0x4819

Bit(s)	R/W	Default	Description
27-16	R/W	0	horizontal formatter width
11-0	R/W	0	vertical formatter width

VD2 vd_rmem_if0 is same as vd1 vd_rmem_if0 ,BASE_addr is from 0x4800 to 0x4880

DI vd_rmem_if0 is same as vd1 vd_rmem_if0 ,BASE_addr is from 0x4800 to 0x5400-0x5680

9.2.3.20 VD2 Path vd_rmem_if0 Registers

VD2_IF0_GEN_REG 0x3220

Same as VD1_IF0_GEN_REG

VD2_IF0_CANVAS0 0x3221

Same as VD1_IF0_CANVAS0

VD2_IF0_CANVAS1 0x3222

Same as VD1_IF0_CANVAS1

VD2_IF0_LUMA_X0 0x3223

Same as VD1_IF0_LUMA_X0

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VD2_IF0_LUMA_Y0 0x3224

Same as VD1_IF0_LUMA_Y0

VD2_IF0_CHROMA_X0 0x3225

Same as VD1_IF0_CHROMA_X0

VD2_IF0_CHROMA_Y0 0x3226

Same as VD1_IF0_CHROMA_Y0

VD2_IF0_LUMA_X1 0x3227

Same as VD1_IF0_LUMA_X1

VD2_IF0_LUMA_Y1 0x3228

Same as VD1_IF0_LUMA_Y1

VD2_IF0_CHROMA_X1 0x3229

Same as VD1_IF0_CHROMA_X1

VD2_IF0_CHROMA_Y1 0x327A

Same as VD1_IF0_CHROMA_Y1

VD2_IF0_RPT_LOOP 0x322B

Same as VD1_IF0_RPT_LOOP

VD2_IF0_LUMA0_RPT_PAT 0x322C

Same as VD1_IF0_LUMA0_RPT_PAT

VD2_IF0_CHROMA0_RPT_PAT 0x322D

Same as VD1_IF0_CHROMA0_RPT_PAT

VD2_IF0_LUMA1_RPT_PAT 0x322E

Same as VD1_IF0_LUMA1_RPT_PAT

VD2_IF0_CHROMA1_RPT_PAT 0x322F

Same as VD1_IF0_CHROMA1_RPT_PAT

VD2_IF0_LUMA_PSEL 0x3230

Same as VD1_IF0_LUMA_PSEL

VD2_IF0_CHROMA_PSEL 0x3231

Same as VD1_IF0_CHROMA_PSEL

VD2_IF0_DUMMY_PIXEL 0x3232

Same as VD1_IF0_DUMMY_PIXEL

VD2_RANGE_MAP_Y 0x323A

Same as VD1_RANGE_MAP_Y

VD2_RANGE_MAP_CB 0x323B

Same as VD1_RANGE_MAP_CB

VD2_RANGE_MAP_CR 0x323C

Same as VD1_RANGE_MAP_CR

VD2_IF0_GEN_REG2 0x323D

Same as VD1_IF0_GEN_REG2

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VD2_IF0_GEN_REG3 0x3236

Same as VD1_IF0_GEN_REG3

Table 9-1295 VIU_VD2_FMT_CTRL 0x3238

Bit(s)	R/W	Default	Description
31	R/W	0	gate_clk_en. 0=No clock gating, free-running; 1=Enable clock gating for power saving.
30	R/W	0	soft_rst. If true, reset formatters.
28	R/W	0	if true, horizontal formatter use repeating to generete pixel, otherwise use bilinear interpolation
27-24	R/W	0	horizontal formatter initial phase
23	R/W	0	horizontal formatter repeat pixel 0 enable
22-21	R/W	0	horizontal Y/C ratio, 00: 1:1, 01: 2:1, 10: 4:1
20	R/W	0	horizontal formatter enable
19	R/W	0	if true, always use phase0 while vertical formater, meaning always repeat data, no interpolation
18	R/W	0	if true, disable vertical formatter chroma repeat last line
17	R/W	0	veritcal formatter dont need repeat line on phase0, 1: enable, 0: disable
16	R/W	0	veritcal formatter repeat line 0 enable
15-12	R/W	0	vertical formatter skip line num at the beginning
11-8	R/W	0	vertical formatter initial phase
7-1	R/W	0	vertical formatter phase step (3.4)
0	R/W	0	vertical formatter enable

Table 9-1296 VIU_VD2_FMT_W 0x3239

Bit(s)	R/W	Default	Description
27-16	R/W	0	horizontal formatter width
11-0	R/W	0	vertical formatter width

9.2.3.21 Osd_blend Registers

Table 9-1297 VIU_OSD_BLEND_CTRL 0x39b0

Bit(s)	R/W	Default	Description
31:29	R/W	0x0	hold_lines : //unsigned , default = 3'h0, hold_lines(line) after go_field ,module active
28:27	R/W	0x3	blend2_premult_en : //unsigned , default = 2'h3, blend2 input premult label 1:pre-mult input 0:unpremult input
26	R/W	0x1	din0_byp_blend : //unsigned , default = 1'h1, blend_din0 bypass to dout0 1:by-pass 0:blend_din0 input to blend0
25	R/W	0x1	din2_osd_sel : //unsigned , default = 1'h1, blend1_dout bypass to blend2 0: blend1_dout to blend2 1:blend1_dout to dout1

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Bit(s)	R/W	Default	Description
24	R/W	0x1	din3_osd_sel : //unsigned , default = 1'h1, blend1_din3 bypass to dout1 1:bypass 0:blend_din3 input to blend1
23:20	R/W	0x5	blend_din_en : //unsigned , default = 4'h5, blend enable bits ,four bits for four input
19:16	R/W	0x0	din_premult_en : //unsigned , default = 4'h0, input premult label bits,four bits for four input
15:0	R/W	0x2341	din_reoder_sel : //unsigned , default = 16'h2341,osd_blend input reorder exp : din_reoder_sel[3:0] = 1 ,blend_din0 select osd1 din_reoder_sel [3:0] = 2 ,blend_ din0 select osd2 din_reoder_sel [3:0] = 3 ,blend_din0 select osd3 din_reoder_sel [3:0] = else,blend_din0 no src din_reoder_sel [7:4] fot blend_din1

Table 9-1298 VIU_OSD_BLEND_CTRL1 0x39c0

Bit(s)	R/W	Default	Description
17:16	R/W	0	reg_alp1_mapping_mode : //unsigned , default = 0 , osd_blend dout1 alpha divid- or mode 8bit alpha:set 0 9bit alpha:set 3
14:13	R/W	0	reg_div1_gclk_en : //unsigned , default = 0 , osd_blend dout1 alpha dividor gclk_ en
12	R/W	0	reg_div1_alpha_en : //unsigned , default = 0 , osd_blend dout1 alpha dividor gclk_en enable
9:8	R/W	0	osdbld_gclk_ctrl : //unsigned , default = 0 , osdbld_gclk_ctrl
5:4	R/W	0	reg_alp_mapping_mode : //unsigned , default = 0 , osd_blend dout0 alpha dividor mode 8bit alpha:set 0 9bit alpha:set 3
2:1	R/W	0	reg_div_gclk_en : //unsigned , default = 0 , osd_blend dout0 alpha dividor gclk_ en
0	R/W	0	reg_div_alpha_en : //unsigned , default = 0 , osd_blend dout0 alpha dividor gclk_ en enable

Table 9-1299 VIU_OSD_BLEND_DIN0_SCOPE_H 0x39b1

Bit(s)	R/W	Default	Description
28:16	R/W	0x2d0	bld_din0_h_end : ///unsigned , default = 13'h2d0,blend_din0 h_end
12:0	R/W	0x0	bld_din0_h_start : ///unsigned , default = 13'h0 ,blend_din0 h_start

Table 9-1300 VIU_OSD_BLEND_DIN0_SCOPE_V 0x39b2

Bit(s)	R/W	Default	Description
28:16	R/W	0x1e0	bld_din0_v_end : ///unsigned , default = 13'h1e0,blend_din0 v_end
12:0	R/W	0x0	bld_din0_v_start : ///unsigned , default = 13'h0,blend_din0 v_start

Table 9-1301 VIU_OSD_BLEND_DIN1_SCOPE_H 0x39b3

Bit(s)	R/W	Default	Description
28:16	R/W	0x2d0	bld_din1_h_end : ///unsigned , default = 13'h2d0
12:0	R/W	0x0	bld_din1_h_start : ///unsigned , default = 13'h0

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Table 9-1302 VIU_OSD_BLEND_DIN1_SCOPE_V 0x39b4

Bit(s)	R/W	Default	Description
28:16	R/W	0x1e0	bld_din1_v_end : ///unsigned , default = 13'h1e0
12:0	R/W	0x0	bld_din1_v_start : ///unsigned , default = 13'h0

Table 9-1303 VIU_OSD_BLEND_DIN2_SCOPE_H 0x39b5

Bit(s)	R/W	Default	Description
28:16	R/W	0x2d0	bld_din2_h_end : ///unsigned , default = 13'h2d0
12:0	R/W	0x0	bld_din2_h_start : ///unsigned , default = 13'h0

Table 9-1304 VIU_OSD_BLEND_DIN2_SCOPE_V 0x39b6

Bit(s)	R/W	Default	Description
28:16	R/W	0x1e0	bld_din2_v_end : ///unsigned , default = 13'h1e0
12:0	R/W	0x0	bld_din2_v_start : ///unsigned , default = 13'h0

Table 9-1305 VIU_OSD_BLEND_DIN3_SCOPE_H 0x39b7

Bit(s)	R/W	Default	Description
28:16	R/W	0x2d0	bld_din3_h_end : ///unsigned , default = 13'h2d0
12:0	R/W	0x0	bld_din3_h_start : ///unsigned , default = 13'h0

Table 9-1306 VIU_OSD_BLEND_DIN3_SCOPE_V 0x39b8

Bit(s)	R/W	Default	Description
28:16	R/W	0x1e0	bld_din3_v_end : ///unsigned , default = 13'h1e0
12:0	R/W	0x0	bld_din3_v_start : ///unsigned , default = 13'h0

Table 9-1307 VIU_OSD_BLEND_DUMMY_DATA0 0x39b9

Bit(s)	R/W	Default	Description
23:16	R/W	0x00	blend0_dummy_data_y : //unsigned , default = 8'h00
15:8	R/W	0x80	blend0_dummy_data_cb : //unsigned , default = 8'h80
7:0	R/W	0x80	blend0_dummy_data_cr : //unsigned , default = 8'h80

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Table 9-1308 VIU_OSD_BLEND_DUMMY_ALPHA 0x39ba

Bit(s)	R/W	Default	Description
28:20	R/W	0x0	blend0_dummy_alpha : //unsigned , default = 9'h0
19:11	R/W	0x0	blend1_dummy_alpha : //unsigned , default = 9'h0
8:0	R/W	0x0	blend2_dummy_alpha : //unsigned , default = 9'h0

Table 9-1309 VIU_OSD_BLEND_BLEND0_SIZE 0x39bb

Bit(s)	R/W	Default	Description
28:16	R/W	0x1e0	blend0_vsize : //unsigned , default = 13'h1e0,blend0_vsize
12:0	R/W	0x2d0	blend0_hsize : //unsigned , default = 13'h2d0,blend0_hsize

Table 9-1310 VIU_OSD_BLEND_BLEND1_SIZE 0x39bc

Bit(s)	R/W	Default	Description
28:16	R/W	0x1e0	blend1_vsize : //unsigned , default = 13'h1e0
12:0	R/W	0x2d0	blend1_hsize : ///unsigned , default = 13'h2d0

9.2.3.22 Pre/Post Blend Registers

Table 9-1311 VPP_PRE_BLEND_CTRL 0x3960

Bit(s)	R/W	Default	Description
27:20	R/W	0x4	hold_lines : //unsigned , default = 8'h4,blend work after hold_lines line after go_field
1:0	R/W	0x1	gclk_ctrl : //unsigned , default = 16'h1,gating ctrl

Table 9-1312 VPP_PRE_BLEND_BLEND_DUMMY_DATA 0x3961

Bit(s)	R/W	Default	Description
23:16	R/W	0x0	blend0_dummy_data_y : //unsigned , default = 8'h0,blend dummy data
15:8	R/W	0x80	blend0_dummy_data_cb : //unsigned , default = 8'h80,blend dummy data
7:0	R/W	0x80	blend0_dummy_data_cr : //unsigned , default = 8'h80 ,blend dummy data

Table 9-1313 VPP_PRE_BLEND_DUMMY_ALPHA 0x3962

Bit(s)	R/W	Default	Description
28:20	R/W	0x0	blend0_dummy_alpha : //unsigned , default = 9'h0,blend dummy alpha
19:11	R/W	0x0	blend1_dummy_alpha : //unsigned , default = 9'h0,blend dummy alpha
8:0	R/W	0x0	blend2_dummy_alpha : //unsigned , default = 9'h0,blend dummy alpha

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Table 9-1314 VPP_PRE_BLEND2_RO_CURRENT_XY 0x3963

Bit(s)	R/W	Default	Description
28:16	R.O	0x0	ro_current_x : //unsigned , default = 32'h0,blend out x point
12:0	R.O	0x0	ro_current_y : //unsigned , default = 32'h0,blend out x point

Table 9-1315 VPP_POST_PRE_BLEND_CTRL 0x3967

Bit(s)	R/W	Default	Description
27:20	R/W	0x4	hold_lines : //unsigned , default = 8'h4,blend work after hold_lines line after go_ field
1:0	R/W	0x1	gclk_ctrl : //unsigned , default = 16'h1,gating ctrl

Table 9-1316 VPP_POST_BLEND_BLEND_DUMMY_DATA 0x3968

Bit(s)	R/W	Default	Description
23:16	R/W	0x0	blend0_dummy_data_y : //unsigned , default = 8'h0,blend dummy data
15:8	R/W	0x80	blend0_dummy_data_cb : //unsigned , default = 8'h80,blend dummy data
7:0	R/W	0x80	blend0_dummy_data_cr : //unsigned , default = 8'h80 ,blend dummy data

Table 9-1317 VPP_POST-BLEND_DUMMY_ALPHA 0x3969

Bit(s)	R/W	Default	Description
28:20	R/W	0x0	blend0_dummy_alpha : //unsigned , default = 9'h0,blend dummy alpha
19:11	R/W	0x0	blend1_dummy_alpha : //unsigned , default = 9'h0,blend dummy alpha
8:0	R/W	0x0	blend2_dummy_alpha : //unsigned , default = 9'h0,blend dummy alpha

Table 9-1318 VPP_POST_BLEND2_RO_CURRENT_XY 0x396a

Bit(s)	R/W	Default	Description
28:16	R.O	0x0	ro_current_x : //unsigned , default = 32'h0,blend out x point
12:0	R.O	0x0	ro_current_y : //unsigned , default = 32'h0,blend out x point

9.2.3.23 VPU AFBC Registers

Table 9-1319 AFBCDM_ENABLE 0x4840

Bit(s)	R/W	Default	Description
28:23	R/W	0	reg_gclk_ctrl_core : unsigned, default = 0 if ture ,disable clock,otherwise enable clock
22	R/W	0	reg_fmt_size_sw_mode : unsigned, default = 0, 0:hw mode 1:sw mode for format size
21	R/W	1	reg_addr_link_en : unsigned, default = 1, 1:enable

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Bit(s)	R/W	Default	Description
20	R/W	0	reg_fmt444_comb : unsigned, default = 0, 0: 444 8bit uncomb
19	R/W	0	reg_dos_uncomp_mode : unsigned , default = 0
18:16	R/W	4	soft_rst : unsigned , default = 4
13:12	R/W	1	ddr_blk_size : unsigned , default = 1
11:9	R/W	3	cmd_blk_size : unsigend , default = 3
8	R/W	0	dec_enable : unsigned , default = 0
1	R/W	1	head_len_sel : unsigned , default = 1
0	R/W	0	dec_frm_start : unsigned , default = 0

Table 9-1320 AFBCDM_MODE 0x4841

Bit(s)	R/W	Default	Description
29	R/W	0	ddr_sz_mode : uns, default = 0 , 0: fixed block ddr size 1 : unfixed block ddr size;
28	R/W	0	blk_mem_mode : uns, default = 0 , 0: fixed 16x128 size; 1 : fixed 12x128 size
27:26	R/W	0	rev_mode : uns, default = 0 , reverse mode
25:24	R/W	3	mif_urgent : uns, default = 3 , info mif and data mif urgent
22:16	R/W	4	hold_line_num : uns, default = 4 ,
15:14	R/W	2	burst_len : uns, default = 2, 0: burst1 1:burst2 2:burst4
13:8	R/W	0	compbits_yuv : uns, default = 0 , bit 1:0,: y component bitwidth : 00-8bit 01-9bit 10-10bit 11-12bit bit 3:2,: u component bitwidth : 00-8bit 01-9bit 10-10bit 11-12bit bit 5:4,: v component bitwidth : 00-8bit 01-9bit 10-10bit 11-12bit
7:6	R/W	0	vert_skip_y : uns, default = 0 , luma vert skip mode : 00-y0y1, 01-y0, 10-y1, 11-(y0+y1)/2
5:4	R/W	0	horz_skip_y : uns, default = 0 , luma horz skip mode : 00-y0y1, 01-y0, 10-y1, 11-(y0+y1)/2
3:2	R/W	0	vert_skip_uv : uns, default = 0 , chroma vert skip mode : 00-y0y1, 01-y0, 10-y1, 11-(y0+y1)/2
1:0	R/W	0	horz_skip_uv : uns, default = 0 , chroma horz skip mode : 00-y0y1, 01-y0, 10-y1, 11-(y0+y1)/2

Table 9-1321 AFBCDM_SIZE_IN 0x4842

Bit(s)	R/W	Default	Description
28:16	R/W	1920	hsize_in : uns, default = 1920 , pic horz size in unit: pixel
12:0	R/W	1080	vsize_in : uns, default = 1080 , pic vert size in unit: pixel

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Table 9-1322 AFBCDM_DEC_DEF_COLOR 0x4843

Bit(s)	R/W	Default	Description
29:20	R/W	0	def_color_y : uns, default = 0, afbc dec y default setting value
19:10	R/W	0	def_color_u : uns, default = 0, afbc dec u default setting value
9: 0	R/W	0	def_color_v : uns, default = 0, afbc dec v default setting value

Table 9-1323 AFBCDM_CONV_CTRL 0x4844

Bit(s)	R/W	Default	Description
13:12	R/W	2	fmt_mode : uns, default = 2, 0:yuv444 1:yuv422 2:yuv420
11: 0	R/W	256	conv_lbuf_len : uns, default = 256, unit=16 pixel need to set = 2^n

Table 9-1324 AFBCDM_LBUF_DEPTH 0x4845

Bit(s)	R/W	Default	Description
27:16	R/W	128	dec_lbuf_depth : uns, default = 128; // unit= 8 pixel
11:0	R/W	128	mif_lbuf_depth : uns, default = 128;

Table 9-1325 AFBCDM_HEAD_BADDR 0x4846

Bit(s)	R/W	Default	Description
31:0	R/W	0x0	mif_info_baddr : uns, default = 32'h0;

Table 9-1326 AFBCDM_BODY_BADDR 0x4847

Bit(s)	R/W	Default	Description
31:0	R/W	0x0001_0000	mif_data_baddr : uns, default = 32'h0001_0000;

Table 9-1327 AFBCDM_SIZE_OUT 0x4848

Bit(s)	R/W	Default	Description
28:16	R/W	1920	hszie_out: uns, default = 1920 ; // unit: 1 pixel
12:0	R/W	1080	Vsize_out : uns, default = 1080 ; // unit: 1 pixel

Table 9-1328 AFBCDM_OUT_YSCOPE 0x4849

Bit(s)	R/W	Default	Description
28:16	R/W	0	out_vert_bgn : uns, default = 0 ; // unit: 1 pixel
12:0	R/W	1079	out_vert_end : uns, default = 1079 ; // unit: 1 pixel

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Table 9-1329 AFBCDM_STAT 0x484a

Bit(s)	R/W	Default	Description
31:1	RO	0	ro_dbg_top_info : uns, default = 0
0	R/W	0	frm_end_stat : uns, default = 0 frame end status

Table 9-1330 AFBCDM_VD_CFMT_CTRL 0x484b

Bit(s)	R/W	Default	Description
31	R/W	0	cfmt_gclk_bit_dis : uns, default = 0 ; // it true, disable clock, otherwise enable clock
30	R/W	0	cfmt_soft_rst_bit : uns, default = 0 ; // soft rst bit
28	R/W	0	chfmt_rpt_pix : uns, default = 0 ; // if true, horizontal formatter use repeating to generete pixel, otherwise use bilinear interpolation
27:24	R/W	0	chfmt_ini_phase : uns, default = 0 ; // horizontal formatter initial phase
23	R/W	0	chfmt_rpt_p0_en : uns, default = 0 ; // horizontal formatter repeat pixel 0 enable
22:21	R/W	0	chfmt_yc_ratio : uns, default = 0 ; // horizontal Y/C ratio, 00: 1:1, 01: 2:1, 10: 4:1
20	R/W	0	chfmt_en : uns, default = 0 ; // horizontal formatter enable
19	R/W	0	cvfmt_phase0_always_en : uns, default = 0 ; //if true, always use phase0 while vertical formater, meaning always repeat data, no interpolation
18	R/W	0	cvfmt_rpt_last_dis : uns, default = 0 ; //if true, disable vertical formatter chroma repeat last line
17	R/W	0	cvfmt_phase0_nrpt_en : uns, default = 0 ; //veritcal formatter dont need repeat line on phase0, 1: enable, 0: disable
16	R/W	0	cvfmt_rpt_line0_en : uns, default = 0 ; //veritcal formatter repeat line 0 enable
15:12	R/W	0	cvfmt_skip_line_num : uns, default = 0 ; //vertical formatter skip line num at the beginning
11:8	R/W	0	cvfmt_ini_phase : uns, default = 0 ; //vertical formatter initial phase
7:1	R/W	0	cvfmt_phase_step : uns, default = 0 ; //vertical formatter phase step (3.4)
0	R/W	0	cvfmt_en : uns, default = 0 ; //vertical formatter enable

Table 9-1331 AFBCDM_VD_CFMT_W 0x484c

Bit(s)	R/W	Default	Description
28:16	R/W	0x0	cfmt_w : uns, default = 0 ;//horizontal : formatter width
12:0	R/W	0x0	cvfmt_w : uns ,default = 0;//vertical : formatter width

Table 9-1332 AFBC_MIF_VER_SCOPE 0x1aee

Bit(s)	R/W	Default	Description
27:16	R/W	0	mif_blk_bgn_v : uns, default = 0 ; // unit: 32 pixel/block ver
11: 0	R/W	269	mif_blk_end_v : uns, default = 269; // unit: 32 pixel/block ver

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Table 9-1333 AFBCDM_MIF_HOR_SCOPE 0x484d

Bit(s)	R/W	Default	Description
25:16	R/W	0	mif_blk_bgn_h : uns, default = 0 ; // unit: 32 pixel/block hor
9: 0	R/W	59	mif_blk_end_h : uns, default = 59 ; // unit: 32 pixel/block hor

Table 9-1334 AFBCDM_MIF_VER_SCOPE 0x484e

Bit(s)	R/W	Default	Description
27:16	R/W	0	mif_blk_bgn_v : uns, default = 0 ; // unit: 32 pixel/block ver
11: 0	R/W	269	mif_blk_end_v : uns, default = 269; // unit: 32 pixel/block ver

Table 9-1335 AFBCDM_PIXEL_HOR_SCOPE 0x484f

Bit(s)	R/W	Default	Description
28:16	R/W	0	dec_pixel_bgn_h : uns, default = 0 ; // unit: pixel
12: 0	R/W	1919	dec_pixel_end_h : uns, default = 1919 ; // unit: pixel

Table 9-1336 AFBCDM_PIXEL_VER_SCOPE 0x4850

Bit(s)	R/W	Default	Description
28:16	R/W	0	dec_pixel_bgn_v : uns, default = 0 ; // unit: pixel
12: 0	R/W	1079	dec_pixel_end_v : uns, default = 1079 ; // unit: pixel

Table 9-1337 AFBCDM_VD_CFMT_H 0x4851

Bit(s)	R/W	Default	Description
12:0	R/W	142	cfmt : uns, default =142;// vertical : formatter height

Table 9-1338 AFBCDM_IQUANT_ENABLE 0x4852

Bit(s)	R/W	Default	Description
11	R/W	0x0	reg_quant_expand_en_1 : //unsigned, RW, enable for quantization value expansion
10	R/W	0x0	reg_quant_expand_en_0 : //unsigned, RW, enable for quantization value expansion
9: 8	R/W	-1	reg_bcleav_ofst : //signed , RW, default = 0 bcleave ofset to get lower range, especially under lossy, for v1/v2, x=0 is equivalent, default = -1;
4	R/W	0	reg_quant_enable_1 : // unsigned , RW, default = 0 enable for quant to get some lossy
0	R/W	0	reg_quant_enable_0 : // unsigned , RW, default = 0 enable for quant to get some lossy

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Table 9-1339 AFBCDM_IQUANT_LUT_1 0x4853

Bit(s)	R/W	Default	Description
30:28	R/W	0	reg_iquant_yclut_0_11 : // unsigned , RW, default = 0 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
26:24	R/W	1	reg_iquant_yclut_0_10 : // unsigned , RW, default = 1 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
22:20	R/W	2	reg_iquant_yclut_0_9 : // unsigned , RW, default = 2 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
18:16	R/W	3	reg_iquant_yclut_0_8 : // unsigned , RW, default = 3 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
14:12	R/W	4	reg_iquant_yclut_0_7 : // unsigned , RW, default = 4 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
10: 8	R/W	5	reg_iquant_yclut_0_6 : // unsigned , RW, default = 5 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
6: 4	R/W	5	reg_iquant_yclut_0_5 : // unsigned , RW, default = 5 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
2: 0	R/W	4	reg_iquant_yclut_0_4 : // unsigned , RW, default = 4 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)

Table 9-1340 AFBCDM_IQUANT_LUT_2 0x4854

Bit(s)	R/W	Default	Description
14:12	R/W	3	reg_iquant_yclut_0_3 : // unsigned , RW, default = 3 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
10: 8	R/W	2	reg_iquant_yclut_0_2 : // unsigned , RW, default = 2 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
6: 4	R/W	1	reg_iquant_yclut_0_1 : // unsigned , RW, default = 1 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
2: 0	R/W	0	reg_iquant_yclut_0_0 : // unsigned , RW, default = 0 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)

Table 9-1341 AFBCDM_IQUANT_LUT_3 0x4855

Bit(s)	R/W	Default	Description
30:28	R/W	0	reg_iquant_yclut_1_11 : // unsigned , RW, default = 0 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
26:24	R/W	1	reg_iquant_yclut_1_10 : // unsigned , RW, default = 1 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
22:20	R/W	2	reg_iquant_yclut_1_9 : // unsigned , RW, default = 2 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
18:16	R/W	3	reg_iquant_yclut_1_8 : // unsigned , RW, default = 3 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
14:12	R/W	4	reg_iquant_yclut_1_7 : // unsigned , RW, default = 4 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
10: 8	R/W	5	reg_iquant_yclut_1_6 : // unsigned , RW, default = 5 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)

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Bit(s)	R/W	Default	Description
6: 4	R/W	5	reg_iquant_yclut_1_5 : // unsigned , RW, default = 5 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
2: 0	R/W	4	reg_iquant_yclut_1_4 : // unsigned , RW, default = 4 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)

Table 9-1342 AFBCDM_IQUANT_LUT_4 0x4856

Bit(s)	R/W	Default	Description
14:12	R/W	3	reg_iquant_yclut_1_3 : // unsigned , RW, default = 3 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
10: 8	R/W	2	reg_iquant_yclut_1_2 : // unsigned , RW, default = 2 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
6: 4	R/W	1	reg_iquant_yclut_1_1 : // unsigned , RW, default = 1 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)
2: 0	R/W	0	reg_iquant_yclut_1_0 : // unsigned , RW, default = 0 quantization lut for min-tree leavs, iquant=2^lut(bc_leav_q+1)

Table 9-1343 AFBCDM_ROT_CTRL 0x4860

Bit(s)	R/W	Default	Description
31:30	R/W	0	reg_rot_ohds2_mode : uns, default = 0 , rot output format down horizontal drop mode, 0:average , 1:use 0, 2: use 1
29:28	R/W	0	reg_rot_ovds2_mode : uns, default = 0 , rot output format down vertical drop mode, 0:average , 1:use 0, 2: use 1
27	R/W	0	reg_pip_mode : uns, default = 0 , 0:dec_source from vdin/dos 1: dec_source from pip
26:24	R/W	0	reg_rot_uv_vshrk_drop_mode: uns, default = 0, 0: average (1/2: 1:left 2:right) (1/4:1:[0] 2:p[1] 3:[2] 4:[3] , 5:left_121 6:right_121
22:20	R/W	0	reg_rot_uv_hshrk_drop_mode: uns, default = 0, 0: average (1/2: 1:left 2:right) (1/4:1:[0] 2:p[1] 3:[2] 4:[3] , 5:left_121 6:right_121
19:18	R/W	0	reg_rot_uv_vshrk_ratio: uns, default = 0, 0:no shrink 1:1/2 shrink 2:1/4 shrink
17:16	R/W	0	reg_rot_uv_hshrk_ratio: uns, default = 0, 0:no shrink 1:1/2 shrink 2:1/4 shrink
14:12	R/W	0	reg_rot_y_vshrk_drop_mode : uns,default = 0, 0: average (1/2: 1:left 2:right) (1/4:1:[0] 2:p[1] 3:[2] 4:[3] , 5:left_121 6:right_121
10:8	R/W	0	reg_rot_y_hshrk_drop_mode : uns,default = 0, 0: average (1/2: 1:left 2:right) (1/4:1:[0] 2:p[1] 3:[2] 4:[3] , 5:left_121 6:right_121
7:6	R/W	0	reg_rot_y_vshrk_ratio:uns, default =0, 0:disable 1: 1/2 v-shrink 2:1/4 v-shrink
5:4	R/W	0	reg_rot_y_hshrk_ratio:uns, default =0, 0:disable 1: 1/2 h-shrink 2:1/4 h-shrink
3:2	R/W	0	reg_rot_uv422_drop_mode :uns, default = 0, 0:average two pixel 1:keep left 2: keep right
1	R/W	0	reg_rot_uv422_omode : uns,default = 0, When rot input is fmt 422, 0:output_uv422 1:output uv420
0	R/W	0	reg_rot_enable : uns, default = 0, rotation enable

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Table 9-1344 AFBCDM_ROT_SCOPE 0x4861

Bit(s)	R/W	Default	Description
25:20	R/W	0	reg_rot_debug_probe : uns, default= 0; bits [2:0] for y, bits [5:3] for uv 0: iblk_size, 1:oblk_size, 2:iblk_cnt, 3:oblk_cnt, 4:hsize_in, 5:vsize_in, 6:vstep
19	R/W	0	reg_rot_dout_ds_mode_sw: uns, default= 0, 0: use hardware mode, 1: use soft-ware mode
18:17	R/W	0	reg_dout_ds_mode:uns, default = 0 ,rot output format downscale mode : 0 : h_ downscale, 1: v_downscale
16	R/W	1	reg_ifmt_force444: uns, default = 1 : rot input fmt force as 444
15:14	R/W	0	reg_rot_ofmt_mode: uns, default = 0, rot output format mode
13:12	R/W	0	reg_rot_combits_out_y: uns, default = 0 ,rot output combit y
11:10	R/W	0	reg_rot_combits_out_uv: uns, default = 0 ,rot output combit uv
9:8	R/W	0	reg_rot_wrbgn_v: uns, default = 0, rot pic vertical size window begin pixel
4:0	R/W	0	reg_rot_wrbgn_h: uns ,default = 0, rot pic horizontal size window begin pixel

Table 9-1345 AFBCDM_RPLC_CTRL 0x4862

Bit(s)	R/W	Default	Description
31	R/W	0	reg_rplc_inter_corr_en: uns, default = 0 //pip replace inter_frame edge correct enable
30	R/W	0	reg_rplc_dummy_corr_en: uns, default = 0 //pip replace outside of real-pipframe correct enable
29	R/W	1	reg_rplc_byps: uns, default = 1, //pip replace module bypass
28:16	R/W	1080	reg_rplc_vsize_in: uns, default = 1080
12:0	R/W	1920	reg_rplc_hsize_in: uns, default = 1920

Table 9-1346 AFBCDM_RPLC_PICEN 0x4863

Bit(s)	R/W	Default	Description
27:16	R/W	0	reg_rplc_def_color_y: uns, default = 0 //pip replace def_color_y
15:0	R/W	0xffff	Reg_rplc_pic_enable: uns, default =16'hffff, //pip_replace pip_picure enable

Table 9-1347 AFBCDM_RPLC_DEFCOL 0x4864

Bit(s)	R/W	Default	Description
23:12	R/W	0	reg_rplc_def_color_v: uns, default =0, //pip replace def_color_v
11:0	R/W	0	reg_rplc_def_color_u: uns, default =0, //pip replace def_color_u

Table 9-1348 AFBCDM_RPLC_SCPXN_ADDR 0x4865

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_rplc_scpxn_addr: uns, default =0, //pip replace scopes of 16 windows addr

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Table 9-1349 AFBCDM_RPLC_SCPXN_DATA 0x4866

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_rplc_scpxn_data: uns, default = 0, //pip_replace scopes of 16 windows data

Table 9-1350 AFBCDM_ROT_RO_STAT 0x4867

Bit(s)	R/W	Default	Description
31:0	R/O	0	ro_rot_debug: uns, RO ,default = 0, rot some status

VD2_AFBC dec is same as vd1 AFBC dec , BASE_addr isfrom 0x4840 to 0x48c0.

DI AFBC dec is same as vd1 AFBC dec ,BASE_addr is from 0x4840 to 0x5440-0x56c0.

9.2.3.24 VPU Film Grain Registers

Table 9-1351 FGRAIN_CTRL 0x4870

Bit(s)	R/W	Default	Description
25:24	R/W	0	reg_sync_ctrl: [0] 1 to shaddow reg_fgrain_glb_en; [1] to shaddow reg_fgrain_ loc_en.
22	R/W	0	reg_dma_st_clr: write 1 to clear DMA error status, then write to 0
21	R/W	0	reg_hold4dma_scale:1 to wait DMA scale data ready before accept input data
20	R/W	0	reg_hold4dma_tbl: 1 to wait DMA grain table data ready before accept input data
19	R/W	0	reg_cin_uv_swap: 1 to swap U/V input
18	R/W	0	reg_cin_rev:1 to reverse the U/V input order
17	R/W	0	reg_yin_rev:1 to reverse the Y input order
16	R/W	1	reg_fgrain_ext_imode: 0 to indicate the input data is (<<2) in 8bit mode
15	R/W	0	reg_use_par_apply_fgrain:1 to use parameter “apply_fgrain” from DMA table
14	R/W	0	reg_fgrain_last_ln_mode□ 1 to keep film grain noise generator though the input is finished for none-afbc mode
13	R/W	0	reg_fgrain_use_sat4bp: 1 to use SW max/min for output saturation and not (1<<bitdepth)-1/0 when film grain bypass.
12	R/W	1	reg_apply_c_mode:following C code
11	R/W	1	reg_fgrain_tbl_sign_mode:0 to indicate signed bit is not extended in 8bit mode
10	R/W	1	reg_fgrain_tbl_ext_mode: 0 to indicate the grain table value is (<<2) in 8bit mode
9: 8	R/W	2	reg_fmt_mode: 0:444; 1:422; 2:420; 3:reserved. Only 420 have affect, others mode will bypass film grain
7: 6	R/W	1	reg_comp_bits: 0:8bits; 1:10bits, others reserved.
5	R/W	0	reg_rev_mode□1 for vertical scan reverse
4	R/W	0	reg_rev_mode□1 for horizontal scan reverse
2	R/W	1	reg_block_mode: 0: none-afbc mode; 1 afbc mode

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Bit(s)	R/W	Default	Description
1	R/W	0	reg_fgrain_loc_en:frame-based fgrain enable
0	R/W	0	reg_fgrain_glb_en: global-based fgrain enable

Table 9-1352 FGRAIN_WIN_H 0x4871

Bit(s)	R/W	Default	Description
31:16	R/W	3812	reg_win_end_h: horizontal end position of window to do film grain: LSB 5bit should be 0 for afbc mode. For example, if horizontal size is 3840 with no window cut, it will set to (3840-32)
15: 0	R/W	0	reg_win_bgn_h: horizontal start position of window to do film grain: LSB 5bit should be 0 for afbc mode

Table 9-1353 FGRAIN_WIN_V 0x4872

Bit(s)	R/W	Default	Description
31:16	R/W	2156	reg_win_end_v: vertical end position of window to do film grain: LSB 2bit should be 0 for afbc mode. For example, if vertical size is 2160 with no window cut, it will set to (2160-4)
15: 0	R/W	0	reg_win_bgn_v: vertical start position of window to do film grain: LSB 2bit should be 0 for afbc mode

Table 9-1354 FGRAIN_SW_Y_RANGE 0x4873

Bit(s)	R/W	Default	Description
31	R/W	0	reg_fgrain_sw_yrange, 1 to use fgrain_ymin/ymax for saturation. Otherwise use 16/235 when parameter: clip _to_restricted_range =1, 0/255 when clip _to_restricted_range=0.
25:16	R/W	1023	reg_fgrain_ymax: max value for SW saturation
9: 0	R/W	0	reg_fgrain_ymin: min value for SW saturation

Table 9-1355 FGRAIN_SW_C_RANGE 0x4874

Bit(s)	R/W	Default	Description
31	R/W	0	reg_fgrain_sw_crange, 1 to use fgrain_cmin/cmax for saturation. Otherwise use 16/240 when parameter: clip _to_restricted_range =1, 0/255 when clip _to_restricted_range=0.
25:16	R/W	1023	reg_fgrain_cmax: max value for SW saturation
9: 0	R/W	0	reg_fgrain_cmin: min value for SW saturation

Table 9-1356 FGRAIN_GCLK_CTRL_0 0x4875

Bit(s)	R/W	Default	Description
31 :0	R/W	0	reg_fgrain_gclk_ctrl0: Gate clock control.

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Table 9-1357 FGRAIN_GCLK_CTRL_1 0x4876

Bit(s)	R/W	Default	Description
31 :0	R/W	0	reg_fgrain_gclk_ctrl1: Gate clock control.

Table 9-1358 FGRAIN_GCLK_CTRL_2 0x4877

Bit(s)	R/W	Default	Description
31 :0	R/W	0	reg_fgrain_gclk_ctrl2: Gate clock control.

Table 9-1359 FGRAIN_PARAM_ADDR 0x4878

Bit(s)	R/W	Default	Description
31 :0	R/W	0	Parameter table index. it will increase aotomatically when read FGRAIN_PARAM_DATA

Table 9-1360 FGRAIN_PARAM_DATA 0x4879

Bit(s)	R/W	Default	Description
31 :0	RO	0	Parameter table data Index=0: mode parameter is ready scale parameter is ready noise table parameter is ready Index=1: Parameter: apply_grain Parameter: overlap Parameter: chroma_scaling_from_luma Parameter: clip_to_restricted_range Parameter: mc_identity [7:5] Parameter: data depth [11:8] Parameter: y_num_points [15:12] Parameter: cb_num_points [19:16] Parameter: cr_num_points Index=2: [15:0] Parameter: rand seed Index=3: [0] DMA status: 1 to indicate DMA transfer is too slow, finish after input data arrived

VD2 FGRAIN is same as vd1 FGRAIN , BASE_addr is from 0x4870 to 0x48e0

DI FGRAIN is same as vd1 FGRAIN , BASE_addr is from 0x4870 to 0x5440-0x56c0

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9.2.3.25 VPP Registers

Table 9-1361 VPP_DUMMY_DATA 0x1d00

Bit(s)	R/W	Default	Description
29:20	R/W	0	VD1_SC_Y : // unsigned , default = 0x10,dummy data used in the VD1 scaler,according VPP_DOLBY_CTRL[17] 1:set 8bit value 2:set 10bit value
19:10	R/W	0	VD1_SC_CB : // unsigned , default = 0x80,dummy data used in the VD1 scaler, according VPP_DOLBY_CTRL[17] 1:set 8bit value 2:set 10bit value
9 :0	R/W	0	VD1_SC_CR : // unsigned , default = 0x80,dummy data used in the VD1 scaler, according VPP_DOLBY_CTRL[17] 1:set 8bit value 2:set 10bit value

Table 9-1362 VPP_LINE_IN_LENGTH 0x1d01

Bit(s)	R/W	Default	Description
13:0	R/W	14	line_in_length : // unsigned , default = 14'd1920,VD1 scaler input hsize

Table 9-1363 VPP_PIC_IN_HEIGHT 0x1d02

Bit(s)	R/W	Default	Description
12:0	R/W	0x1fff	line_in_height : // unsigned , default = 13'h1fff,VD1 scaler input vsize

Table 9-1364 VPP_PREBLEND_VD1_H_START_END 0x1d1a

Bit(s)	R/W	Default	Description
28:16	R/W	0	start : //unsigned , default = 0x0000 ,preblend video1 horizontal start
12:0	R/W	0	end : //unsigned , default = 0x077f ,preblend video1 horizontal end

Table 9-1365 VPP_PREBLEND_VD1_V_START_END 0x1d1b

Bit(s)	R/W	Default	Description
28:16	R/W	0	start : //unsigned , default = 0x0000 ,preblend video1 vertical start
12:0	R/W	0	end : //unsigned , default = 0x0437 ,preblend video1 vertical end

Table 9-1366 VPP_POSTBLEND_VD1_H_START_END 0x1d1c

Bit(s)	R/W	Default	Description
28:16	R/W	0	start : //unsigned , default = 0x0000 ,postblend video1 horizontal start
12:0	R/W	0	end : //unsigned , default = 0x077f ,postblend video1 horizontal end

Table 9-1367 VPP_POSTBLEND_VD1_V_START_END 0x1d1d

Bit(s)	R/W	Default	Description
31:29	/	/	/
28:16	R/W	0	//unsigned , default = 0x0000 ,postblend video1 vertical start Bit

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Bit(s)	R/W	Default	Description
15:13	/	/	/
12:0		0x077f	//unsigned , default = 0x077f ,postblend video1 vertical end

Table 9-1368 VPP_BLEND_VD2_H_START_END 0x1d1e

Bit(s)	R/W	Default	Description
28:16	R/W	0	start : //unsigned , default = 0x0000 ,preblend/postblend video2 horizontal start
12:0	R/W	0	end : //unsigned , default = 0x077f ,preblend/postblend video2 horizontal end

Table 9-1369 VPP_BLEND_VD2_V_START_END 0x1d1f

Bit(s)	R/W	Default	Description
28:16	R/W	0	start : //unsigned , default = 0x0000 ,preblend/postblend video2 vertical start
12:0	R/W	0	end : //unsigned , default = 0x077f ,preblend/postblend video2 vertical end

Table 9-1370 VPP_PREBLEND_H_SIZE 0x1d20

Bit(s)	R/W	Default	Description
29:16	R/W	14	prebld_v_size : //unsigned , default = 14'd1080 ,preblend output vsize
13:0	R/W	14	prebld_h_size : //unsigned , default = 14'd1920 ,preblend output hsize

Table 9-1371 VPP_POSTBLEND_H_SIZE 0x1d21

Bit(s)	R/W	Default	Description
29:16	R/W	14	postbld_v_size : //unsigned , default = 14'd1080 ,postblend output vsize
13:0	R/W	14	postbld_h_size : //unsigned , default = 14'd1920 ,postblend output hsize

Table 9-1372 VPP hold lines VPP_HOLD_LINES 0x1d22

Bit(s)	R/W	Default	Description
15:8	R/W	4	prebld_hold_lines : //unsigned , default = 4,preblend hold lines
7:0	R/W	4	postbld_hold_lines : //unsigned , default = 4,postblend hold lines

Table 9-1373 VPP_MISC 0x1d26

Bit(s)	R/W	Default	Description
30	R/W	0	Color_manage_en //CM2 top enable
29	R/W	0	vpp_vks_en : //unsigned , default = 0 , vkstone enable
28	R/W	0	color_manage_en : //unsigned , default = 0 , color management enable
27	R/W	0	vd2_use_viu2_out_en : //unsigned , default = 0 , if true, vd2 use viu2 output as the input, otherwise use normal vd2 from memory

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Bit(s)	R/W	Default	Description
26:18	R/W	0	vd2 : alpha //unsigned , default = 0 , video 2 prebld/postbld alpha
8	R/W	1	0: vpp_gamma before 3D_LUT 1: gammar after 3D_lut
7	R/W	1	postbld_en : //unsigned , default = 1 , postblend module enable ,din_reoder_sel of post blend can work when postbld_en high.
6	R/W	0	prebld_en : //unsigned , default = 0 , preblend module enable ,din_reoder_sel of post blend can work when postbld_en high.
3	R/W	0	sr4c1_path_sel : //unsigned , default = 0 , choose sr1 position 1:sr1 bettwen dnlp & CM 0:sr1 bettwen position after postblend
2	R/W	0	disable_rst_afifo : //unsigned , default = 0 , if true, disable resetting async fifo every vsync, otherwise every vsync the aync fifo will be reseted.
1	R/W	0	sr4c0_path_sel : //unsigned , default = 0 , choose sr0 position 1:sr0 bettwen prebld & vd1_scale 0:sr0 bettwen position after dnlp

Table 9-1374 VPP_OFIFO_SIZE 0x1d27

Bit(s)	R/W	Default	Description
31:20	R/W	0	ofifo_line_lenm1 : //unsigned , default = 0xfff , ofifo line length minus 1
19	R/W	0	vs_ctrl : //unsigned , default = 0, if true invert input vs
18	R/W	0	hs_ctrl : //unsigned , default = 0, if true invert input hs
17	R/W	0	force_top_bot_field_en : //unsigned , default = 0, force top/bottom field, enable
16	R/W	0	fforce_top_bot_field : //unsigned , default = 0, force top/bottom field, 0: top, 1: bottom
15	R/W	0	force_go_field : //unsigned , default = 0, force one go_field, one pluse, write only
14	R/W	0	force_go_line : //unsigned , default = 0, force one go_line, one pluse, write only
13:0	R/W	0	ofifo_size : //unsigned , default = 0x1000 , ofifo size (actually only bit 13:1 is valid), always even number ,max 4096

Table 9-1375 VPP_FIFO_STATUS 0x1d28

Bit(s)	R/W	Default	Description
29:25	R.O	0	ro_sco_ff_buf_count : //unsigned , default = 0,current scale out fifo counter
24:14	R.O	0	ro_afifo_count : //unsigned , default = 0,current enc afifo counter
13:1	R.O	0	ro_ofifo_buf_count : //unsigned , default = 0,current vpp line fifo ofifo counter

Table 9-1376 VPP_MATRIX_PROBE_COLOR 0x1d5c

Bit(s)	R/W	Default	Description
31:24	R.O	0	ro_probe_y_l : //unsigned , default = 0,low 8 bits of component 0
23:12	R.O	0	ro_probe_cr : //unsigned , default = 0,component 1
11:0	R.O	0	ro_probe_cb : //unsigned , default = 0,component 2

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Table 9-1377 VPP_MATRIX_PROBE_COLOR1 0x1dd7

Bit(s)	R/W	Default	Description
31	R.O	0x0	ro_probe_pix_v : //it means this probe is valid in the last field/frame
3:0	R.O	0	ro_probe_y_h : //unsigned , default = 0,high 4 bits of component 0

Table 9-1378 VPP_MATRIX_HL_COLOR 0x1d5d

Bit(s)	R/W	Default	Description
23:16	R/W	0	hl_y : //unsigned , default = 0,component 0
15:8	R/W	0	hl_cb : //unsigned , default = 0,component 1
7:0	R/W	0	hl_cr : //unsigned , default = 0,component 2

Table 9-1379 VPP_MATRIX_PROBE_POS 0x1d5e

Bit(s)	R/W	Default	Description
28:16	R/W	0	probe_x : //unsigned , default = 0,probe x, postion
12:0	R/W	0	probe_y : //unsigned , default = 0,probe y, position

Table 9-1380 VPP_MATRIX_CTRL 0x1d5f

Bit(s)	R/W	Default	Description
16	R/W	0	highlight_en : //unsigned , default = 0, highlight enable
15	R/W	0	probe_post : //unsigned , default = 0, if true, probe pixel data after matrix, otherwise probe pixel data before matrix
14:10	R/W	0	probel_sel : //unsigned , default = 0, active when VIU_SECURE_REG[9] high, probel sel : 5'b00001 :vadj1 5'b00010 :vadj2 5'b00100 :osd2 5'b01000 :postbld 5'b10000 :osd1

Table 9-1381 VPP_GAINOFF_CTRL0 0x1d6a

Bit(s)	R/W	Default	Description
31	R/W	0	enable : //unsigned , default = 0, gainoff module enable
30	R/W	0	enable_sel : //unsigned , default = 0, gainoff module enable sync sel
26:16	R/W	0	gain0 : //unsigned , default = 0, gainoff module gain0
10:0	R/W	0	gain1 : //unsigned , default = 0, gainoff module gain1

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Table 9-1382 VPP_GAINOFF_CTRL1 0x1d6b

Bit(s)	R/W	Default	Description
26:16	R/W	0	gain2 : //unsigned , default = 0, gainoff module gain2
(DW +0):0	R/W	0	offset0 : //signed ,bitwidth is DW+1,DW is the chip path data width, default = 0, gainoff module offset0

Table 9-1383 VPP_GAINOFF_CTRL2 0x1d6c

Bit(s)	R/W	Default	Description
(DW +16):16	R/W	0	offset1 : //signed ,bitwidth is DW+1,DW is the chip path data width, default = 0, gainoff module offset1
(DW +0):0	R/W	0	offset2 : //signed , bitwidth is DW+1,DW is the chip path data width,default = 0, gainoff module offset2

Table 9-1384 VPP_GAINOFF_CTRL3 0x1d6d

Bit(s)	R/W	Default	Description
(DW +16):16	R/W	0	pre_offset0 : //signed , bitwidth is DW+1,DW is the chip path data width,default = 0, gainoff module pre_offset0
(DW +0):0	R/W	0	pre_offset1 : //signed , bitwidth is DW+1,DW is the chip path data width,default = 0, gainoff module pre_offset1

Table 9-1385 VPP_GAINOFF_CTRL4 0x1d6e

Bit(s)	R/W	Default	Description
(DW +0):0	R/W	0	pre_offset2 : //signed , bitwidth is DW+1,DW is the chip path data width,default = 0, gainoff module pre_offset2

Table 9-1386 VPP_GAINOFF_GCLK_CTRL 0x1d6f

Bit(s)	R/W	Default	Description
1:0	R/W	0	gainoff_gclk_ctrl : //unsigned , default = 0,gainoff_gclk_ctrl

Table 9-1387 VPP_PREHSC_COEF 0x1d37

Bit(s)	R/W	Default	Description
31:24	R/W	64	prehsc_coef3 //signed
23:16	R/W	0	prehsc_coef2 //signed
15:8	R/W	0	prehsc_coef1 //signed
7:0	R/W	0	prehsc_coef0 //signed

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Table 9-1388 VPP_PRE_SCALE_CTRL 0x1d38

Bit(s)	R/W	Default	Description
10:7	R/W	2	prehsc_flt_num//unsigned 2: 2tap 4:4tap 6:6tap 8:8tap
6:4	R/W	2	prevsc_flt_num//unsiged 2: 2tap 4:4tap
3:2	R/W	1	prehsc_ds_ratio//unsigned 0:(1:1 mode) 1:(2:1 mode)
1:0	R/W	1	prevsc_ds_ratio//unsigned 0:(1:1 mode) 1:(2:1 mode)

Table 9-1389 VPP_PREVSC_COEF 0x1d39

Bit(s)	R/W	Default	Description
15:8	R/W	64	prevsc_coef1 //signed
7:0	R/W	0	prevsc_coef0 //signed

Table 9-1390 VPP_GCLK_CTRL0 0x1d72

Bit(s)	R/W	Default	Description
5:4	R/W	0	ofifo_clk1 : //unsigned , default = 0,gating clock of out linefifo in vpp
3:2	R/W	0	clk0 : //unsigned , default = 0,clk swtich of all vpp module
1	R/W	0	reg_gclk : //unsigned , default = 0,registers gate clk of vpp module

Table 9-1391 VPP_GCLK_CTRL1 0x1d73

Bit(s)	R/W	Default	Description
27:20	R/W	0	gclk_ctrl_wm : //unsigned , default = 0,gating clock of water_mark
18:15	R/W	0	dolby3_gclk_ctrl : //unsigned , default = 0,gating clock of dolby3
3:0	R/W	0	cm_gclk_ctrl : //unsigned , default = 0,gating clock of color manage

Table 9-1392 VPP_MISC1 0x1d76

Bit(s)	R/W	Default	Description
20:12	R/W	0	vd1_prebld_alpha : //unsigned , default = 0,VD1 alpha for preblend
8:0	R/W	0	vd1_postbld_alpha : //unsigned , default = 0,VD1 alpha for postblend

Table 9-1393 VPP_SRSCL_GCLK_CTRL 0x1d77

Bit(s)	R/W	Default	Description
15:8	R/W	0	gclk_ctrl_sr1 : //unsigned , default = 0 , gating clock of sr1
7:0	R/W	0	gclk_ctrl_sr0 : //unsigned , default = 0 , gating clock of sr0

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Table 9-1394 VPP_BLACKEXT_CTRL 0x1d80

Bit(s)	R/W	Default	Description
31:24	R/W	0	blackext_start : //unsigned , default = 0 ,blackext_start
23:16	R/W	0	blackext_slope1 : //unsigned , default = 0 ,blackext_slope1
15:8	R/W	0	blackext_midpt : //unsigned , default = 0 ,blackext_midpt
7:0	R/W	0	blackext_slope2 : //unsigned , default = 0 ,blackext_slope2

Table 9-1395 VPP_DNLP_CTRL_00 0x1d81

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region03 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region02 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region01 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region00 output value

Table 9-1396 VPP_DNLP_CTRL_01 0x1d82

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region07 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region06 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region05 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region04 output value

Table 9-1397 VPP_DNLP_CTRL_02 0x1d83

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region11 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region10 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region09 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region08 output value

Table 9-1398 VPP_DNLP_CTRL_03 0x1d84

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region15 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region14 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region13 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region12 output value

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Table 9-1399 VPP_DNLP_CTRL_04 0x1d85

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region19 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region18 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region17 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region16 output value

Table 9-1400 VPP_DNLP_CTRL_05 0x1d86

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region23 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region22 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region21 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region20 output value

Table 9-1401 VPP_DNLP_CTRL_06 0x1d87

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region27 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region26 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region25 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region24 output value

Table 9-1402 VPP_DNLP_CTRL_07 0x1d88

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region31 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region30 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region29 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region28 output value

Table 9-1403 VPP_DNLP_CTRL_08 0x1d89

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region35 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region34 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region33 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region32 output value

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Table 9-1404 VPP_DNLP_CTRL_09 0x1d8a

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region39 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region38 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region37 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region36 output value

Table 9-1405 VPP_DNLP_CTRL_10 0x1d8b

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region43 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region42 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region41 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region40 output value

Table 9-1406 VPP_DNLP_CTRL_11 0x1d8c

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region47 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region46 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region45 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region44 output value

Table 9-1407 VPP_DNLP_CTRL_12 0x1d8d

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region51 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region50 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region49 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region48 output value

Table 9-1408 VPP_DNLP_CTRL_13 0x1d8e

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region55 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region54 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region53 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region52 output value

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Table 9-1409 VPP_DNLP_CTRL_14 0x1d8f

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region59 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region58 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region57 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region56 output value

Table 9-1410 VPP_DNLP_CTRL_15 0x1d90

Bit(s)	R/W	Default	Description
31:24	R/W	0	data0 : //unsigned , default = 0 ,bottom of region63 output value
23:16	R/W	0	data1 : //unsigned , default = 0 ,bottom of region62 output value
15:8	R/W	0	data2 : //unsigned , default = 0 ,bottom of region61 output value
7:0	R/W	0	data3 : //unsigned , default = 0 ,bottom of region60 output value

Table 9-1411 VPP_SRSHARP0_CTRL 0x1d91

Bit(s)	R/W	Default	Description
28:16	R/W	0	srsharp_demo_split_sz : //unsigned , default = 0 ,srsharp demo top/bot left/right width
5:4	R/W	0	srsharp_demo_disp_post : //unsigned , default = 0 ,srsharp demo display postion
3	R/W	0	srsharp_demo_en : //unsigned , default = 0 ,srsharp demo enable
2	R/W	0	srsharp_c444to422_en : //unsigned , default = 0 ,srsharp format444 convert 422 enable
1	R/W	0	srsharp_buf_en : //unsigned , default = 0 ,srsharp buffer enable
0	R/W	0	srsharp_en : //unsigned , default = 0 ,srsharp enable

Table 9-1412 VPP_SRSHARP1_CTRL 0x1d92

Bit(s)	R/W	Default	Description
28:16	R/W	0	srsharp_demo_split_sz : //unsigned , default = 0 ,srsharp demo top/bot left/right width
5:4	R/W	0	srsharp_demo_disp_post : //unsigned , default = 0 ,srsharp demo display postion
3	R/W	0	srsharp_demo_en : //unsigned , default = 0 ,srsharp demo enable
2	R/W	0	srsharp_c444to422_en : //unsigned , default = 0 ,srsharp format444 convert 422 enable
1	R/W	0	srsharp_buf_en : //unsigned , default = 0 ,srsharp buffer enable
0	R/W	0	srsharp_en : //unsigned , default = 0 ,srsharp enable

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Table 9-1413 VPP_DOLBY_CTRL 0x1d93

Bit(s)	R/W	Default	Description
25:24	R/W	0	dolby3_path_sel : //unsigned , default = 0 ,1:dolby2->osd_mat->post_blend->dolby3->wm 0:dolby2->dolby3->osd_mat->post_blend->wm
20	R/W	0	Wap vpp vd1/vd1 0:unswap 1:swap
17	R/W	0	pps_dummy_data_mode : //unsigned , default = 0 ,pps_dummy_data_mode 1: vd1_scale need setting 8 bits 0:vd1_scale need setting 10 bits
16	/	/	Reserved.
10	R/W	0	vpp_clip_ext_mode2 : //unsigned , default = 0 ,Vpp out clip mode 1:10bit 0:12bit
9	R/W	0	vpp_clip_ext_mode1 : //unsigned , default = 0 ,Vpp Vd2 input clip mode 1:10bit 0:12bit
8	R/W	0	vpp_clip_ext_mode0 : //unsigned , default = 0 ,Vpp Vd1 input clip mode 1:10bit 0:12bit
3	R/W	0	vpp_dolby3_en : //unsigned , default = 0 ,dolby_core3 enable,active high
2	R/W	0	vpp_dpath_sel2 : //unsigned , default = 0 ,by_pass from post2_marix to outbuffer
1	R/W	0	vpp_dpath_sel1 : //unsigned , default = 0 ,by_pass from gainoff to vks
0	R/W	0	vpp_dpath_sel0 : //unsigned , default = 0 ,1: by_pass from preblend to VADJ1 0: unbypass

Table 9-1414 VPP_SYNC_SEL0 0x1d96

Bit(s)	R/W	Default	Description
31:0	R/W	0	sync_sel_bits : //unsigned ,default = 0,sync_sel bits for VPP_DOLBY_CTRL

Table 9-1415 VPP_CCORING_CTRL 0x1da0

Bit(s)	R/W	Default	Description
27:16	R/W	0	reg_bypass_ccoring_ythd : // unsigned , default = 0 , bypass_ccoring_ythd
15:8	R/W	0	ccoring_th : // unsigned , default = 0 , Chroma coring threshold
3:0	R/W	0	ccoring_slope : // unsigned , default = 0 , Chroma coring slope

Table 9-1416 VPP_VE_ENABLE_CTRL 0x1da1

Bit(s)	R/W	Default	Description
29:28	R/W	0	dnlp_gclk_ctrl : // unsigned , default = 0 ,dnlp gclk ctrl
27:26	R/W	0	blackext_gclk_ctrl : // unsigned , default = 0 ,blackext gclk ctrl
25:24	R/W	0	ccoring_gclk_ctrl : // unsigned , default = 0 ,chroma coring gclk ctrl
20	R/W	0	demo_ccoring_enable : // unsigned , default = 0 ,demo chroma coring enable
19	R/W	0	demo_blackext_enable : // unsigned , default = 0 ,demo black enxtension enable
18	R/W	0	demo_dnlp_enable : // unsigned , default = 0 ,demo dynamic nonlinear luma processing enable
15:14	R/W	0	demo_disp_position : // unsigned , default = 0 ,2'b00: demo adjust on top, 2'b01: demo adjust on bottom, 2'b10: demo adjust on left, 2'b11: demo adjust on right

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Bit(s)	R/W	Default	Description
4	R/W	0	ccoring_en : // unsigned , default = 0 , chroma coring enable
3	R/W	0	blackext_en : // unsigned , default = 0 , black enxtension enable
2	R/W	0	dnlp_en : // unsigned , default = 0 , dynamic nonlinear luma processing enable

Table 9-1417 VPP_VE_DEMO_LEFT_TOP_SCREEN_WIDTH 0x1da2

Bit(s)	R/W	Default	Description
12:0	R/W	0	ve_demo_left_top_screen_width : // unsigned , default = 0 demo left or top screen width

Table 9-1418 VPP_VE_DEMO_CENTER_BAR 0x1da3

Bit(s)	R/W	Default	Description
31	R/W	0	ve_demo_center_bar : // unsigned , default = 0 center bar enable
27:24	R/W	0	ve_demo_center_bar : // unsigned , default = 0 center bar width (*2)
23:16	R/W	0	ve_demo_center_bar : // unsigned , default = 0 center bar Cr (*4)
15:8	R/W	0	ve_demo_center_bar : // unsigned , default = 0 center bar Cb (*4)
7:0	R/W	0	ve_demo_center_bar : // unsigned , default = 0 center bar y (*4)

Table 9-1419 VPP_VE_H_V_SIZE 0x1da4

Bit(s)	R/W	Default	Description
28:16	R/W	780	ve_line_length : // unsigned , default = 780 ve_line_length
12:0	R/W	438	ve_pic_height : // unsigned , default = 438 ve_pic_height

Table 9-1420 VPP_OUT_H_V_SIZE 0x1da5

Bit(s)	R/W	Default	Description
28:16	R/W	780	vppout_line_length : / unsigned , default = 780 vd1_scale_out hsize
12:0	R/W	438	vppout_pic_height : // unsigned , default = 438 vd1_scale_out vsize

Table 9-1421 VPP_VDO_MEAS_CTRL 0x1da8

Bit(s)	R/W	Default	Description
10:0	R/W	0	vdo_meas_ctrl : // unsigned , default = 0 vdo_meas_ctrl

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Table 9-1422 VPP_VDO_MEAS_VS_COUNT_HI 0x1da9

Bit(s)	R/W	Default	Description
19 :16	RO	0	ro_ind_meas_count_n // unsigned , default = 0 ind_meas_count_n, every number of sync_span vsyncs, this counter add 1
15 :0,	RO	0	ro_counter_h // unsigned , default = 0 high bit portion of counter

Table 9-1423 VPP_VDO_MEAS_VS_COUNT_LO 0x1daa

Bit(s)	R/W	Default	Description
31 :0	RO	0	ro_counter_l // unsigned , default = 0,low bit portion of counter

Table 9-1424 VPP_INPUT_CTRL 0x1dab

Bit(s)	R/W	Default	Description
11:9	R/W	0	vd2_sel : // unsigned , default = 0, 001: select vd1_din, 010: select vd2_din, 011: select d2d3_l_din, 100: d2d3_r_din, otherwise no selection
8:6	R/W	0	vd1_l_sel : // unsigned , default = 0, 001: select vd1_din, 010: select vd2_din, 011: select d2d3_l_din, 100: d2d3_r_din, otherwise no selection,vd1_l_sel selected cannot be used as the source of vd1_r_sel or vd2_sel
5:3	R/W	0	vd1_r_sel : // unsigned , default = 0, 001: select vd1_din, 010: select vd2_din, 011: select d2d3_l_din, 100: d2d3_r_din, otherwise no selection,useful only vd1_interleave_mode is not 00. And the source vd1_r_sel used can not used for the vd2_sel any more bit 2:0 vd1_interleave_mode // unsigned , default = 0, 000: no interleave, 001: pixel interleaving, 010: line interleaving, 011: 2 pixel interleaving,100: 2 line interleaving

Table 9-1425 VPP_CTI_CTRL2 0x1dac

Bit(s)	R/W	Default	Description
25:24	R/W	0	cti_bpf_sel : // unsigned , default = 0
20:16	R/W	0	cti_blend_factor_gama : // unsigned , default = 0
12:8	R/W	0	cti_blend_factor_beta : // unsigned , default = 0
4:0	R/W	0	cti_blend_factor_alpha : // unsigned , default = 0

Table 9-1426 VPP_WRBAK_CTRL_SEC 0x1dad

Bit(s)	R/W	Default	Description
31	R/W	0	vpp_wrbak_sel // unsigned , default = 0, 1: VPP_WRBAK_CTRL regs set to vpp_wrbak_data_ini,Cbus can't access 0: VPP_WRBAK_CTRL reg can be writen bit
30:0	R/W	0	vpp_wrbak_data_ini // unsigned , default = 0,

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Table 9-1427 VD1_BLEND_SRC_CTRL_SEC 0x1dae

Bit(s)	R/W	Default	Description
31	R/W	0	vd1_blend_src_sel : // unsigned , default = 0, 1: VD1_BLEND_SRC_CTRL regs set to vd1_blend_src_data_ini,Cbus can't access 0: VD1_BLEND_SRC_CTRL reg can be writen
30:0	R/W	0	vd1_blend_src_data_ini : // unsigned , default = 0,

Table 9-1428 VD2_BLEND_SRC_CTRL_SEC 0x1daf

Bit(s)	R/W	Default	Description
31	R/W	0	vd2_blend_src_sel : // unsigned , default = 0, 1: VD2_BLEND_SRC_CTRL regs set to vd1_blend_src_data_ini,Cbus can't access 0: VD2_BLEND_SRC_CTRL reg can be writen
30:0	R/W	0	vd2_blend_src_data_ini : // unsigned , default = 0,

Table 9-1429 OSD1_BLEND_SRC_CTRL_SEC 0x1db0

Bit(s)	R/W	Default	Description
31	R/W	0	osd1_blend_src_sel : // unsigned , default = 0, 1: OSD1_BLEND_SRC_CTRL regs set to osd1_blend_src_data_ini,Cbus can't access 0: OSD1_BLEND_SRC_CTRL reg can be writen
30:0	R/W	0	osd1_blend_src_data_ini : // unsigned , default = 0,

Table 9-1430 OSD2_BLEND_SRC_CTRL_SEC 0x1db1

Bit(s)	R/W	Default	Description
31	R/W	0	osd2_blend_src_sel : // unsigned , default = 0, 1: OSD2_BLEND_SRC_CTRL regs set to osd2_blend_src_data_ini,Cbus can't access 0: OSD2_BLEND_SRC_CTRL reg can be writen
30:0	R/W	0	osd2_blend_src_data_ini : // unsigned , default = 0,

Table 9-1431 VPP_INT_LINE_NUM 0x1dce

Bit(s)	R/W	Default	Description
12:0	R/W	0x0	interrupt_line_num : //unsigned, default== 0x1fff,line number use to generate interrupt when line == this number

Table 9-1432 VPP_OFIFO_URG_CTRL 0x1dd8

Bit(s)	R/W	Default	Description
31	R/W	0x0	urgent_hold : //unsigned, default== 0, urgent fifo hold enable
28:12	R/W	0x0	urgent_fifo_th : //unsigned, default== 0, urgent fifo hold line threshold
15	R/W	0x0	urgent_ctrl_en : //unsigned, default== 0, urgent_ctrl_en
14	R/W	0x0	urgent_wr : //unsigned, default== 0, urgent_wr, if true for write buffer
13	R/W	0x0	out_inv_en : //unsigned, default== 0, out_inv_en

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Bit(s)	R/W	Default	Description
12	R/W	0x0	urgent_ini_value : //unsigned, default == 0, urgent_ini_value
11:6	R/W	0x0	up_th : //unsigned, default == 0, up_th up threshold
5:0	R/W	0x0	dn_th : //unsigned, default == 0, dn_th dn threshold

Table 9-1433 VPP_CLIP_MISC0 0x1dd9

Bit(s)	R/W	Default	Description
29:20	R/W	1023	r : // unsigned, default == 1023, final clip r channel top
19:10	R/W	1023	g : // unsigned, default == 1023, final clip g channel top
9: 0	R/W	1023	b : // unsigned, default == 1023, final clip b channel top

Table 9-1434 VPP_CLIP_MISC1 0x1dda

Bit(s)	R/W	Default	Description
29:20	R/W	0x0	r : // unsigned, default == 0, final clip r channel bottom
19:10	R/W	0x0	g : // unsigned, default == 0, final clip g channel bottom
9: 0	R/W	0x0	b : // unsigned, default == 0, final clip b channel bottom

Table 9-1435 VPP_VD1_CLIP_MISC0 0x1de1

Bit(s)	R/W	Default	Description
29:20	R/W	1023	r : //unsigned, default == 1023, vd1 clip r channel top
19:10	R/W	1023	g : //unsigned, default == 1023, vd1 clip g channel top
9: 0	R/W	1023	b : //unsigned, default == 1023, vd1 clip b channel top

Table 9-1436 VPP_VD1_CLIP_MISC1 0x1de2

Bit(s)	R/W	Default	Description
29:20	R/W	0x0	r : //unsigned, default = 0, vd1 clip r channel bottom
19:10	R/W	0x0	g : //unsigned, default = 0, vd1 clip g channel bottom
9: 0	R/W	0x0	b : //unsigned, default = 0, vd1 clip b channel bottom

Table 9-1437 VPP_VD2_CLIP_MISC0 0x1de3

Bit(s)	R/W	Default	Description
29:20	R/W	1023	r : //unsigned, default = 1023, vd2 clip r channel top
19:10	R/W	1023	g : //unsigned, default = 1023, vd2 clip g channel top
9: 0	R/W	1023	b : //unsigned, default = 1023, vd2 clip b channel top

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Table 9-1438 VPP_VD2_CLIP_MISC1 0x1de4

Bit(s)	R/W	Default	Description
29:20	R/W	0x0	r : // unsigned, default = 0, vd2 clip r channel bottom
19:10	R/W	0x0	g : // unsigned, default = 0, vd2 clip g channel bottom
9: 0	R/W	0x0	b : // unsigned, default = 0, vd2 clip b channel bottom

Table 9-1439 VPP_VD2_HDR_IN_SIZE 0x1df0

Bit(s)	R/W	Default	Description
18:16	R/W	0	vd2_in_v_size : // unsigned, default = 0x2d0, VPP VD2 input vsize
12:0	R/W	0	vd2_in_h_size : // unsigned, default = 0x1e0, VPP VD2 input hsize

Table 9-1440 VPP_OSD1_IN_SIZE 0x1df1

Bit(s)	R/W	Default	Description
18:16	R/W	0	osd1_in_v_size : // unsigned, default = 0x2d0, VPP osd1 input vsize
12:0	R/W	0	osd1_in_h_size : // unsigned, default = 0x1e0, VPP osd1 input hsize

Table 9-1441 VPP_GCLK_CTRL2 0x1df2

Bit(s)	R/W	Default	Description
13:13	R/W	0	vks_gclk_ctrl : // unsigned, default = 0 ,vks gating clock

Table 9-1442 VD2_PPS_DUMMY_DATA 0x1df4

Bit(s)	R/W	Default	Description
23:16	R/W	0x0	Y : //unsigned, default = 0, vd2 scale dummy data
15:8	R/W	0x0	CB : //unsigned, default = 0, vd2 scale dummy data
7: 0	R/W	0x0	CR : //unsigned, default = 0, vd2 scale dummy data

Table 9-1443 VPP_OSD1_BLD_H_SCOPE 0x1df5

Bit(s)	R/W	Default	Description
28:16	R/W	0	blend_osd1_h_start : //unsigned, default = 0x0
12:0	R/W	0	blend_osd1_h_end : //unsigned, default = 0x2d0

Table 9-1444 VPP_OSD1_BLD_V_SCOPE 0x1df6

Bit(s)	R/W	Default	Description
28:16	R/W	0	blend_osd1_v_start : //unsigned, default = 0x0
12:0	R/W	0	blend_osd1_v_end : //unsigned, default = 0x1e0

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Table 9-1445 VPP_OSD2_BLD_H_SCOPE 0x1df7

Bit(s)	R/W	Default	Description
28:16	R/W	0x0	blend_osd2_h_start : //unsigned, default = 0
12:0	R/W	0x0	blend_osd2_h_end : //unsigned, default = 0x2d0

Table 9-1446 VPP_OSD2_BLD_V_SCOPE 0x1df8

Bit(s)	R/W	Default	Description
28:16	R/W	0x0	blend_osd2_v_start : //unsigned, default = 0
12:0	R/W	0x0	blend_osd2_v_end : //unsigned, default = 0x1e0

Table 9-1447 VPP_WRBAK_CTRL 0x1df9

Bit(s)	R/W	Default	Description
27:16	R/W	0	wrbak_din_lnblank : //unsigned, default = 0,
11:8	R/W	0	wrbak_din_only_en : //unsigned, default = 0,
6:4	R/W	0	wrbak_chan1_sel : //unsigned, default = 0,1:vd1 2:vd2 3:osd1 4:osd2 5:posd_ blend
2:0	R/W	0	wrbak_chan0_sel : //unsigned, default = 0,1:vd1 2:vd2 3:osd1 4:osd2 5:posd_ blend

Table 9-1448 VPP_SLEEP_CTRL 0x1dfa

Bit(s)	R/W	Default	Description
31	R/W	1	sleep_always_en : //unsigned, default = 1
30	R/W	0	sleep_always_dis : //unsigned, default = 0
29:16	R/W	0	sleep_line_len : //unsigned, default = 0
15:14	R/W	0	sleep_mode : //unsigned, default = 0
13:0	R/W	0	sleep_beg_line : //unsigned, default = 0

Table 9-1449 VD1_BLEND_SRC_CTRL 0x1dfb

Bit(s)	R/W	Default	Description
16	R/W	0	vd1_postbld_premult : //unsigned, default = 0
11:8	R/W	1	vd1_postbld_src : //unsigned, default = 1 , 0:close 1:vd1 2:vd2 3:osd1 4:osd2
4	R/W	0	vd1_prebld_premult : //unsigned, default = 0
3:0	R/W	1	vd1_prebld_src : //unsigned, default = 1 , 0:close 1:vd1 2:vd2 3:osd1 4:osd2

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Table 9-1450 VD2_BLEND_SRC_CTRL 0x1dfc

Bit(s)	R/W	Default	Description
20	R/W	0	vd2_blend_path_sel : //unsigned, default = 0
16	R/W	0	vd2_postbld_premult : //unsigned, default = 0
11:8	R/W	2	vd2_postbld_src : //unsigned, default = 2 , 0:close 1:vd1 2:vd2 3:osd1 4:osd2
4	R/W	0	vd2_prebld_premult : //unsigned, default = 0
3:0	R/W	0	vd2_prebld_src : //unsigned, default = 0 ,0:close 1:vd1 2:vd2 3:osd1 4:osd2

Table 9-1451 OSD1_BLEND_SRC_CTRL 0x1dfd

Bit(s)	R/W	Default	Description
20	R/W	0	osd1_blend_path_sel : //unsigned, default = 0
16	R/W	0	osd1_postbld_premult : //unsigned, default = 0
11:8	R/W	3	osd1_postbld_src : //unsigned, default = 3 , 0:close 1:vd1 2:vd2 3:osd1 4:osd2
4	R/W	0	osd1_prebld_premult : //unsigned, default = 0
3:0	R/W	0	osd1_prebld_src : //unsigned, default = 0 ,0:close 1:vd1 2:vd2 3:osd1 4:osd2

Table 9-1452 OSD2_BLEND_SRC_CTRL 0x1dfe

Bit(s)	R/W	Default	Description
20	R/W	0	osd2_blend_path_sel : //unsigned, default = 0
16	R/W	0	osd2_postbld_premult : //unsigned, default = 0
11:8	R/W	4	osd2_postbld_src : //unsigned, default = 4 , 0:close 1:vd1 2:vd2 3:osd1 4:osd2
4	R/W	0	osd2_prebld_premult : //unsigned, default = 0
3:0	R/W	0	osd2_prebld_src : //unsigned, default = 0 , 0:close 1:vd1 2:vd2 3:osd1 4:osd2

Table 9-1453 VPP_CRC_CHK 0x1db3

Bit(s)	R/W	Default	Description
0	W	0	vpp crc check start (pulse)

Table 9-1454 VPP_RO_CRCSUM 0x1db2

Bit(s)	R/W	Default	Description
31-0	R	0	vpp crc result (lock by go_field)

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Table 9-1455 VPP_OSD_SCALE_CTRL 0x1dff

Bit(s)	R/W	Default	Description
2	R/W	1	10bit_12bit_ext_mode// 1:add low 2bits 2'b00 0:add high two bits 2'b00 Osd1_scale before osd_blend :this should be 0 Osd1_scale after osd_blend :this should be 1
1	R/W	1	10bit_12bit_ext_mode_bypass Osd1_scale before osd_blend :this should be 0 Osd1_scale after osd_blend :this should be 1
0	R/W	0	Osd1 scale position change 0:after osd_blend 1:before osd_blend

9.2.3.26 CM Registers

Table 9-1456 VPP_CHROMA_ADDR_PORT 0x1d70

Bit(s)	R/W	Default	Description
31-0	R/W	0	Color management address port

Table 9-1457 VPP_CHROMA_DATA_PORT 0x1d71

Bit(s)	R/W	Default	Description
31-0	R/W	0	Color management data port

Color management internal registers is indirectly accessed by the registers VPP_CHROMA_ADDR_PORT and VPP_CHROMA_DATA_PORT.

Color management registers

The example to access the Color management registers is like this:

Wr(VPP_CHROMA_ADDR_PORT);

Wr(VPP_CHROMA_DATA_PORT):

Table 9-1458 REG_CHROMA_CONTROL 0x30

Bit(s)	R/W	Default	Description
31	R/W	0	reg_chroma_en. enable color manage function 1'b1: enable 1'b0: bypass
6	R/W	0	sat_sel. uv_max or u^2+v^2 selected as sat for reference 1'b1: uv_max(default) 1'b0: u^2+v^2
5	R/W	0	uv_adj_en. final uv_adjust enable 1'b1: enable 1'b0: bypass
2	R/W	0	hue_en. rgb to hue enable 1'b1: enable(default) 1'b0: bypass
1-0	R/W	0	csc_sel. define input YUV with different color type 2'b00: 601(16-235) 2'b01: 709(16-235) 2'b10: 601(0-255) 2'b11: 709(0-255)

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Table 9-1459 SAT_BYYB_NODE0 0x200

Bit(s)	R/W	Default	Description
31-24	R/W	0	The 4th node, the same as below
23-16	R/W	0	The 3th node, the same as below
15-8	R/W	0	The 2th node, the same as below
7-0	R/W	0	Signed, The 1th node about saturation gain offset along Y coordinate, the gain normalized to 128 as “1”.

Table 9-1460 SAT_BYYB_NODE1 0x201

Bit(s)	R/W	Default	Description
31-24	R/W	0	The 8th node, the same as below
23-16	R/W	0	The 7th node, the same as below
15-8	R/W	0	The 6th node, the same as below
7-0	R/W	0	Signed, The 5th node about saturation gain offset along Y coordinate, the gain normalized to 128 as “1”.

Table 9-1461 SAT_BYYB_NODE2 0x202

Bit(s)	R/W	Default	Description
31-8	R/W	0	reserved
7-0	R/W	0	Signed, The 9th node about saturation gain offset along Y coordinate, the gain normalized to 128 as “1”.

Table 9-1462 SAT_SRC_NODE 0x203

Bit(s)	R/W	Default	Description
31-28	R/W	0	reserved
27-16	R/W	0x800	unsign, Threshold of input saturation for second & third piece. i.e. it is boundary for reg_CM2_Adj_Sat_via_HS[1][:]and reg_CM2_Adj_Sat_via_HS[2][:]
15-12	R/W	0	reserved
11-0	R/W	0x400	unsign, Threshold of input saturation for first and second piece.i.e. it is boundary for reg_CM2_Adj_Sat_via_HS[0][:] and reg_CM2_Adj_Sat_via_HS[1][:]

Table 9-1463 CM_ENH_SFT_MODE 0x204

Bit(s)	R/W	Default	Description
31-11	R/W	0	reserved
10–8	R/W	0	Hue offset adjustments scale for Reg_CM2_Adj_Hue_via_H[:]& Reg_CM2_Adj_Hue_via_S[:]& Reg_CM2_Adj_Hue_via_Y[:]: 0: no scale up; 1: upscale by 2 - (-128,127)x2; 2: upscale by 4 - (-128,127)x4; 3: upscale by 8 - (-128,127)x8;

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Bit(s)	R/W	Default	Description
7–6	R/W	0	reserved
5-4	R/W	0	Luma offset adjustments scale for reg_CM2_Adj_Luma_via_Hue[i]: 0: no scale up; 1: upscale by2 - (-128,127)x2; 2: upscale by 4 - (-128,127)x4; 3: upscale by 8 - (-128,127)x8;
3-2	R/W	0	Saturation again adjustments scale for reg_CM2_Adj_Sat_via_Y[:][:] &Reg_CM2_Adj_SatGLBgain_via_Y[:]: 0: no scale up/down; 1: dnscale by 2 (-128,127)/2; 2: dnscale by 4 (-128,127)/4; 3: dnscale by 8 (-128,127)/8;
1-0	R/W	0	Saturation again adjustments scale for reg_CM2_Adj_Sat_via_HS[:][:]: 0: no scale up/down; 1: dnscale by 2 (-128,127)/2; 2: dnscale by 4 (-128,127)/4; 3: dnscale by 8 (-128,127)/8;

Table 9-1464 FRM_SIZE 0x205

Bit(s)	R/W	Default	Description
31-29	R/W	0	reserved
28-16	R/W	0x438	The frame height size
15-13	R/W	0	reserved
12-0	R/W	0x780	The frame width size

Table 9-1465 FITLER_CFG 0x206

Bit(s)	R/W	Default	Description
31-5	R/W	0	reserved
4	R/W	0	Horizontal Interleave filter (zero-padding) for 3D considerations: 0: using non-zero padding LPF 1: using zero-padding LPF
3-0	R/W	0	Apply CM on LP portion or original video pixels options: bits[1:0]: is for Luma path control; bits[3:2]: is for U/V path control; 0: no filter but still match the delay; 1: 5 taps LP filter 2: 9 taps LP filter 3: 13 taps LP filter

Table 9-1466 CM_GLOBAL_GAIN 0x207

Bit(s)	R/W	Default	Description
31-28	R/W	0	reserved
27-16	R/W	0x200	Global Saturation Gain for general color adjustments (0~4095 <=> 0~8), 512 normalized to “1”.
15-12	R/W	0	reserved
11-0	R/W	0	Global Hue offsets for general color adjustments (0~4095 <=> 0~360 degree)

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Table 9-1467 CM_ENH_CTL 0x208

Bit(s)	R/W	Default	Description
31-6	R/W	0	reserved
5	R/W	0	CM Bypass 1: Bypass 0: not bypass
4	R/W	0	Enable signal for CM2 Hue adjustments;
3	R/W	0	Enable signal for CM2 Saturation adjustments;
2	R/W	0	Enable signal for CM2 Luma adjustments;
1	R/W	0	cm2_filt_en :apply cm on lp portion enable
0	R/W	0	CM1 enable signal

Table 9-1468 ROI_X_SCOPE 0x209

Bit(s)	R/W	Default	Description
31-29	R/W	0	reserved
28-16	R/W	0	Ending col index of the Region of Interest (ROI)
15-12	R/W	0	reserved
12-0	R/W	0	Start col index of the Region of Interest (ROI)

Table 9-1469 ROI_Y_SCOPE 0x20a

Bit(s)	R/W	Default	Description
31-29	R/W	0	reserved
28-16	R/W	0	Ending col index of the Region of Interest (ROI)
15-13	R/W	0	reserved
12-0	R/W	0	Start col index of the Region of Interest (ROI)

Table 9-1470 POI_XY_DIR 0x20b

Bit(s)	R/W	Default	Description
31-29	R/W	0	reserved
28-16	R/W	0	Row index of the pixel(position) of Interest (POI)
15-13	R/W	0	reserved
12-0	R/W	0	Col index of the pixel(position) of Interest (POI)

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Table 9-1471 COI_Y_SCOPE 0x20c

Bit(s)	R/W	Default	Description
31-16	R/W	0	reserved
15-8	R/W	0	Higher bound of luma value for color of interest (COI), 8bits precision
7-0	R/W	0	Lower bound of luma value for color of interest (COI), 8bits precision

Table 9-1472 COI_H_SCOPE 0x20d

Bit(s)	R/W	Default	Description
31-28	R/W	0	reserved
27-16	R/W	0	Higher bound of Hue value for color of interest (COI),12 8bits precision
15-12	R/W	0	reserved
11-0	R/W	0	Lower bound of Hue value for color of interest (COI), 12 bits precision

Table 9-1473 COI_S_SCOPE 0x20e

Bit(s)	R/W	Default	Description
31-28	R/W	0	reserved
27-16	R/W	0	Higher bound of Sat value for color of interest (COI),12 8bits precision
15-12	R/W	0	reserved
11-0	R/W	0	Lower bound of Sat value for color of interest (COI), 12 bits precision

Table 9-1474 IFO_MODE 0x20f

Bit(s)	R/W	Default	Description
31-8	R/W	0	reserved
7-4	R/W	0	Mode control for COI replacement, bit[3:2] control COI pixels: 0: no replacement for COI pixels 1: disable CM2 enhance for COI pixels; 2: keep COI pixels Y but replace HS by [*HS]; 3: replace COI pixels to [*YHS] bit[1:0] controls non-COI pixels: 0: no replacement for non-COI pixels 1: disable CM2 enhance for non-COI pixels; 2: keep COI pixels Y but replace HS by [*HS]; 3: replace non- COI pixels to [*YHS]
3-0	R/W	0	Enhance mode control of pixels inside and outside Region of Interest (ROI) , bit [3:2] control ROI: 0: enable CM2 processing in ROI; 1: disable CM2 processing in ROI; 2: keep ROI pixels Y but replace HS by [*HS]; 3: ow ROI pixels to [*YHS] bit [1:0] control pixels other than ROI similarly. 0: enable CM2 processing in non-ROI; 1: disable CM2 processing in non-ROI; 2: keep ROI pixels Y but replace HS by [*HS]; 3: ow non-ROI pixels to [*YHS]

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Table 9-1475 POI_RPL_MODE 0x210

Bit(s)	R/W	Default	Description
31-4	R/W	0	reserved
27-16	R/W	0	Reg_cm2_after_v_offset
15-4	R/W	0	Reg_cm2_after_u_offset
3-0	R/W	0	Pixel of interest (POI) replacement mode: 0: no replacements; 1: one pixel of POI position replaced to [*YHS] 2: 3X3 pixels centering POI position replaced to [*YHS] 3: 5X5 pixels centering POI position replaced to [*YHS] … 15: 29X29 pixels centering POI position replaced to [*YHS]

Table 9-1476 DEMO_OWR_YHS 0x211

Bit(s)	R/W	Default	Description
31-24	R/W	0	Saturation value overwriting to ROI/POI/COI; 12bits precision, equal to saturation precision.
23-12	R/W	0	Hue value overwriting to ROI/POI/COI; 12 bits precision, equal to 1/4 hue precision. E.g. { Reg_CM2Demo_OWR_H, 2'h0}
11-0	R/W	0	Luma value overwriting to ROI/POI/COI; 8bits precision, equal to 1/4 luma precision, e.g. { Reg_CM2Demo_OWR_Y, 2'h0}

Table 9-1477 DEMO_POI_Y 0x212

Bit(s)	R/W	Default	Description
31-8	RO	0	Reserved
7-0	RO	0	Luma value for pixel of interest (POI), only get locked higher 8bits

Table 9-1478 DEMO_POI_H 0x213

Bit(s)	R/W	Default	Description
31-12	RO	0	Reserved
11-0	RO	0	Hue value for pixel of interest (POI), only get locked higher 12bits

Table 9-1479 DEMO_POI_S 0x214

Bit(s)	R/W	Default	Description
31-12	RO	0	Reserved
11-0	RO	0	Saturation value for pixel of interest (POI), only get locked higher 12bits

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Table 9-1480 LUMA_ADJ_LIMT 0x215

Bit(s)	R/W	Default	Description
31-28	R/W	0	reserved
23-16	R/W	0	Slope to do the Luma adjust degrade speed based on Saturation. It was normalized to 16 as '1'.
15-12	R/W	0	reserved
11-0	R/W	0	Threshold to saturation to do Luma adjustment degrade. Only pixels' saturation lower than this threshold will degrade the Luma adjustment.

Table 9-1481 SAT_ADJ_LIMT 0x216

Bit(s)	R/W	Default	Description
31-28	R/W	0	reserved
23-16	R/W	0	Slope to do the Sat adjust degrade speed based on Saturation. It was normalized to 16 as '1'.
15-12	R/W	0	reserved
11-0	R/W	0	Threshold to saturation to do Sat adjustment degrade. Only pixels' saturation lower than this threshold will degrade the Luma adjustment.

Table 9-1482 HUE_ADJ_LIMT 0x217

Bit(s)	R/W	Default	Description
31-28	R/W	0	reserved
23-16	R/W	0	Slope to do the Hue adjust degrade speed based on Saturation. It was normalized to 16 as '1'.
15-12	R/W	0	reserved
11-0	R/W	0	Threshold to saturation to do Hue adjustment degrade. Only pixels' saturation lower than this threshold will degrade the Luma adjustment.

Table 9-1483 UVHS_OFST 0x218

Bit(s)	R/W	Default	Description
31-24	R/W	0	reserved
23-12	R/W	0	U offset after CM2, under s10 scale
11-8	R/W	0	reserved
7-0	R/W	0	U offset before CM2, under s10 scale.

Table 9-1484 HUE_CFG_PARA 0x219

Bit(s)	R/W	Default	Description
31-17	R/W	0	reserved
16	R/W	0	Options to protect HUE after CM2 adjustments. This will be added to avoid HUE distortion if Saturation is enhanced too much.
15-13	R/W	0	Hue adjustment via HS the Saturation division mode: 0: 1024/2048/3072, 4095;

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Bit(s)	R/W	Default	Description
			1: 512, 1024, 1536, 2048; 2: 256, 512, 768, 1024; 3: 128, 256, 384, 512; 4: 512/1024/2048/4096; 5: 256/512/1024/2048; 6: 128/256/512/1024; 7: 64,128,256,512
12	R/W	0	Hue slice division mode: 0: 32 pieces, 360/32 degrees each slice; 1/up: first 20 slices with 360/64 degrees each slice, others 360/16 degrees each slices. Notes, this option provide options to get more precise Hue adjustments for FTC/ Red and so on
11-0	R/W	0	Hue offset before CM2 adjustment, this will provide options to divide the Hue slices with a precise offset. But need to compensate back with the global Hue after CM2 adjusments

Table 9-1485 DEMO_SPLT_CFG 0x21a

Bit(s)	R/W	Default	Description
31-22	R/W	0	reserved
21-20	R/W	0	Demo split post
19-16	R/W	0	Demo split width
12-0	R/W	0	Demo split mode

Table 9-1486 DEMO_SPLT_YHS 0x21b

Bit(s)	R/W	Default	Description
31-24	R/W	0	Luma value
23-12	R/W	0	Hue value
11-0	R/W	0	Sat value

Table 9-1487 XVYCC_YSCP_REG 0x21c

Bit(s)	R/W	Default	Description
27:16	R/W	0x3ff	xvycc_y_max
11:0	R/W	0x0	xvycc_y_min

Table 9-1488 XVYCC_USCP_REG 0x21d

Bit(s)	R/W	Default	Description
27:16	R/W	0x3ff	xvycc_u_max
11:0	R/W	0x0	xvycc_u_min

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Table 9-1489 XVYCC_VSCP_REG 0x21e

Bit(s)	R/W	Default	Description
27:16	R/W	0x3ff	xvycc_v_max
11:0	R/W	0x0	xvycc_v_min

Table 9-1490 LUMA_ADJ0_REG 0x21f

Bit(s)	R/W	Default	Description
21:12	R/W	0x0	Reg_cm_luma_blacklevel
11:0	R/W	0x0	Reg_cm_luma_contrast

Table 9-1491 LUMA_ADJ1_REG 0x220

Bit(s)	R/W	Default	Description
28:16	R/W	0x0	Reg_sta_sat_hist_mode
12:0	R/W	0x0	Reg_cm_luma_brightness

Table 9-1492 STA_WIN_XYXY0_REG 0x221

Bit(s)	R/W	Default	Description
29:16	R/W	0x0	Reg_sta_win_xxyy1
13:0	R/W	0x0	Reg_sta_win_xxyy0

Table 9-1493 STA_WIN_XYXY1_REG 0x222

Bit(s)	R/W	Default	Description
29:16	R/W	0x0	Reg_sta_win_xxyy3
13:0	R/W	0x0	Reg_sta_win_xxyy2

Table 9-1494 STA_CFG_REG 0x223

Bit(s)	R/W	Default	Description
31:30	R/W	0x1	Reg_sta_enable
29:24	R/W	0x1d	Reg_sta_hist_scale
23:16	R/W	0x20	Reg_sta_hue_hist_sat_thrd
15:8	R/W	0x1	Reg_sta_blk_thrd
7:0	R/W	0x254	Reg_sta_brt_thrd

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Table 9-1495 STA_SAT_HIST0_REG 0x224

Bit(s)	R/W	Default	Description
24	R/W	0x0	Reg_cm_ro_frame
23:16	R/W	0x80	Reg_sta_sat_hist_rang_thrd2
15:8	R/W	0x40	Reg_sta_sat_hist_rang_thrd1
7:0	R/W	0x0	Reg_sta_sat_hist_rang_thrd0

Table 9-1496 STA_SAT_HIST1_REG 0x225

Bit(s)	R/W	Default	Description
23:16	R/W	0xff	Reg_sta_sat_hist_rang_thrd5
15:8	R/W	0xff	Reg_sta_sat_hist_rang_thrd4
7:0	R/W	0xc0	Reg_sta_sat_hist_rang_thrd3

Table 9-1497 RO_CM_HUE_HIST_BIN0□RO_CM_HUE_HIST_BIN31 0x226□0x245

Bit(s)	R/W	Default	Description
31:0	RO	0x0	RO_CM_HUE_HIST_BIN0~RO_CM_HUE_HIST_BIN31

Table 9-1498 RO_CM_SAT_HIST_BIN0□RO_CM_SAT_HIST_BIN31 0x246□0x265

Bit(s)	R/W	Default	Description
31:0	RO	0x0	RO_CM_SAT_HIST_BIN0~RO_CM_SAT_HIST_BIN31

Table 9-1499 RO_CM_BLK_BIN 0x266

Bit(s)	R/W	Default	Description
31:0	RO	0x0	RO_CM_BLK_BIN

Table 9-1500 RO_CM_BRT_BIN 0x267

Bit(s)	R/W	Default	Description
31:0	RO	0x0	RO_CM_BRT_BIN

the main adjust parameter is saved according to 32 hue node order, one by one. The parameter of each hue node is same. All the parameter for each hue occupy 5 register-addr-space. For the addr-offset aligned, we allocate 8 addr-space to each node parameter, for example,

the parameter of 1th node uses the address space : 0x100, 0x101, 0x102, 0x103, 0x104,

and 2th node uses the address space : 0x108, 0x109, 0x10a, 0x10b, 0x10c,

and 2th node uses the address space : 0x110, 0x111, 0x112, 0x113, 0x114,

… … … …

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Table 9-1501 CM2_ENH_COEF0_H00 0x100

Bit(s)	R/W	Default	Description
31-24	R/W	0	Same as last
23-16	R/W	0	Same as last
15-8	R/W	0	Signed, Saturation gain offset for three pieces saturation on Hue section (totally 32 sections) node 0; the gain normalized to 128 as “1”.
7-0	R/W	0	Signed, Luma offsets for Hue section (totally 32 sections) nodes 0 , range (-128,127)

Table 9-1502 CM2_ENH_COEF1_H00 0x101

Bit(s)	R/W	Default	Description
31-24	R/W	0	Signed, Hue offset for each four pieces Luma region on each Hue section (totally 32 sections) nodes, this is for y=2/4, hue node 0
23-16	R/W	0	Signed, Hue offset for each four pieces Luma region on each Hue section (totally 32 sections) nodes, this is for y=1/4, hue node 0
15-8	R/W	0	Signed, Hue offset for each four pieces Luma region on each Hue section (totally 32 sections) nodes, this is for y=0, hue node 0
7-0	R/W	0	Signed, Hue offset on Hue section (totally 32 sections) node 0

Table 9-1503 CM2_ENH_COEF2_H00 0x102

Bit(s)	R/W	Default	Description
31-24	R/W	0	Signed, Hue offset for each four pieces Saturation region on each Hue section (totally 32 sections) nodes; This is for sat = 1/4, hue node 0
23-16	R/W	0	Signed, Hue offset for each four pieces Saturation region on each Hue section (totally 32 sections) nodes; This is for sat = 0, hue node 0
15-8	R/W	0	Signed, Hue offset for each four pieces Luma region on each Hue section (totally 32 sections) nodes, this is for y=4/4, hue node 0
7-0	R/W	0	Signed, Hue offset for each four pieces Luma region on each Hue section (totally 32 sections) nodes, this is for y=3/4, hue node 0

Table 9-1504 CM2_ENH_COEF3_H00 0x103

Bit(s)	R/W	Default	Description
31-24	R/W	0	Saturation gain offsetfor four pieces Luma on each Hue section (totally 32 sections) nodes; the gain normalized to 128 as “1”. This is for sat = 0, hue node 0
23-16	R/W	0	Signed, Hue offset for each four pieces Saturation region on each Hue section (totally 32 sections) nodes; This is for sat = 4/4, hue node 0
15-8	R/W	0	Signed, Hue offset for each four pieces Saturation region on each Hue section (totally 32 sections) nodes; This is for sat = 3/4, hue node 0
7-0	R/W	0	Signed, Hue offset for each four pieces Saturation region on each Hue section (totally 32 sections) nodes; This is for sat = 2/4, hue node 0

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Table 9-1505 CM2_ENH_COEF4_H00 0x104

Bit(s)	R/W	Default	Description
31-24	R/W	0	Saturation gain offsetfor four pieces Luma on each Hue section (totally 32 sections) nodes; the gain normalized to 128 as “1”. This is for sat = 4/4, hue node 0
23-16	R/W	0	Saturation gain offsetfor four pieces Luma on each Hue section (totally 32 sections) nodes; the gain normalized to 128 as “1”. This is for sat = 3/4, hue node 0
15-8	R/W	0	Saturation gain offsetfor four pieces Luma on each Hue section (totally 32 sections) nodes; the gain normalized to 128 as “1”. This is for sat = 2/4, hue node 0
7-0	R/W	0	Saturation gain offsetfor four pieces Luma on each Hue section (totally 32 sections) nodes; the gain normalized to 128 as “1”. This is for sat = 1/4, hue node 0

CM2_ENH_COEF0_H01 0x108

CM2_ENH_COEF1_H01 0x109

CM2_ENH_COEF2_H01 0x10a

CM2_ENH_COEF3_H01 0x10b

CM2_ENH_COEF4_H01 0x10c

CM2_ENH_COEF0_H02 0x110

CM2_ENH_COEF1_H02 0x111

CM2_ENH_COEF2_H02 0x112

CM2_ENH_COEF3_H02 0x113

CM2_ENH_COEF4_H02 0x114

....

CM2_ENH_COEF0_H31 0x1f8

CM2_ENH_COEF1_H31 0x1f9

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CM2_ENH_COEF2_H31 0x1fa

CM2_ENH_COEF3_H31 0x1fb

CM2_ENH_COEF4_H31 0x1fc

9.2.3.27 VPP OSD1 SCALER Registers

Table 9-1506 VPP_OSD_VSC_PHASE_STEP 0x1dc0

Bit(s)	R/W	Default	Description
27-0	R/W	0x0100-0000	4.24 format

Table 9-1507 VPP_OSD_VSC_INI_PHASE 0x1dc1

Bit(s)	R/W	Default	Description
31-16	R/W	0x0	botttom vertical scaler initial phase
15-0	R/W	0x0	top vertical scaler initial phase

Table 9-1508 VPP_OSD_VSC_CTRL0 0x1dc2

Bit(s)	R/W	Default	Description
25	R/W	0	Repeat last line en : 1:enable repeat last line 0:disable repeat last line
24	R/W	0x0	osd vertical Scaler enable
23	R/W	0x0	osd_prog_interlace 0: current field is progressive, 1: current field is interlace
22-21	R/W	0x0	osd_vsc_double_line_mode, bit1, double input width and half input height, bit0, change line buffer becomes 2 lines
20	R/W	0x0	osd_vsc_phase0_always_en
19	R/W	0x0	osd_vsc_nearest_en
17-16	R/W	0x0	osd_vsc_bot_rpt_l0_num
14-11	R/W	0x0	osd_vsc_bot_ini_rcv_num
9-8	R/W	0x0	osd_vsc_top_rpt_l0_num
6-3	R/W	0x0	osd_vsc_top_ini_rcv_num
2-0	R/W	0x0	osd_vsc_bank_length

Table 9-1509 VPP_OSD_HSC_PHASE_STEP 0x1dc3

Bit(s)	R/W	Default	Description
27-0	R/W	0x0100-0000	4.24 format

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Table 9-1510 VPP_OSD_HSC_INI_PHASE 0x1dc4

Bit(s)	R/W	Default	Description
31-16	R/W	0x0	horizontal scaler initial phase1
15-0	R/W	0x0	horizontal scaler initial phase0

Table 9-1511 VPP_OSD_HSC_CTRL0 0x1dc5

Bit(s)	R/W	Default	Description
22	R/W	0x0	osd horizontal Scaler enable
21	R/W	0x0	osd_hsc_double_pix_mode
20	R/W	0x0	osd_hsc_phase0_always_en
19	R/W	0x0	osd_vsc_nearest_en
17-16	R/W	0x0	osd_hsc_rpt_p0_num1
14-11	R/W	0x0	osd_hsc_ini_rcv_num1
9-8	R/W	0x0	osd_hsc_rpt_p0_num0
6-3	R/W	0x0	osd_hsc_ini_rcv_num0
2-0	R/W	0x0	osd_hsc_bank_length

Table 9-1512 VPP_OSD_HSC_INI_PAT_CTRL 0x1dc6

Bit(s)	R/W	Default	Description
15-8	R/W	0x0	for 3D quincunx sub-sampling. pattern, each patten 1 bit, from lsb -> msb
6-4	R/W	0x0	pattern start
2-0	R/W	0x0	pattern end

Table 9-1513 VPP_OSD_SC_DUMMY_DATA 0x1dc7

Bit(s)	R/W	Default	Description
31-24	R/W	0x0	componet 0 ,data = (dst_data >> 4) ,so 8 bit in 12bit mode, 6bit in 10bit mode
23-16	R/W	0x0	component 1 ,data = (dst_data >> 4) ,so 8 bit in 12bit mode, 6bit in 10bit mode
15-8	R/W	0x0	component 2 ,data = (dst_data >> 4) ,so 8 bit in 12bit mode, 6bit in 10bit mode
7-0	R/W	0x0	component 3 , alpha

Table 9-1514 VPP_OSD_SC_CTRL0 0x1dc8

Bit(s)	R/W	Default	Description
27:16	R/W	0	osd_sc_gclk_ctrl : //unsigned,default = 0,osd_sc_gclk_ctrl
13	R/W	0	osd_sc_din_osd_alpha_mode : //unsigned,default = 0,osc_sc_din_osd2_alpha_mode, 1: (alpha >= 128) ? alpha -1: alpha, 0: (alpha >=1) ? alpha - 1: alpha.
12	R/W	0	osd_sc_dout_alpha_mode : //unsigned,default = 0,osc_sc_alpha_mode, 1: (alpha >= 128) ? alpha + 1: alpha, 0: (alpha >=1) ? alpha + 1: alpha.

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Bit(s)	R/W	Default	Description
11:4	R/W	0	osd_sc_alpha : //unsigned,default = 0,default alpha for vd1 or vd2 if they are selected as the source
3	R/W	0	osd_sc_path_en : //unsigned,default = 0,osd scaler path enable
2	R/W	0	osd_sc_en : //unsigned,default = 0,osd scaler enable

Table 9-1515 VPP_OSD_SCI_WH_M1 0x1dc9

Bit(s)	R/W	Default	Description
28-16	R/W	0x0	OSD scaler input width minus 1
12-0	R/W	0x0	OSD scaler input height minus 1

Table 9-1516 VPP_OSD_SCO_H_START_END 0x1dca

Bit(s)	R/W	Default	Description
27-16	R/W	0x0	OSD scaler output horizontal start
11-0	R/W	0x0	OSD scaler output horizontal end

Table 9-1517 VPP_OSD_SCO_V_START_END 0x1dcb

Bit(s)	R/W	Default	Description
27-16	R/W	0x0	OSD scaler output vertical start
11-0	R/W	0x0	OSD scaler output vertical end

Table 9-1518 VPP_OSD_SCALE_COEF_IDX 0x1dcc

Bit(s)	R/W	Default	Description

15	R/W	0x0	Because there are many coefficients used in the vertical filter and horizontal filters,
			//indirect access the coefficients of vertical filter and horizontal filter is used.
			//For vertical filter, there are 33x4 coefficients
			//For horizontal filter, there are 33x4 coefficients
			//Bit 15 index increment, if bit9 == 1 then (0: index increase 1, 1: index increase 2) else (index increase 2)

14	R/W	0x0	1: read coef through cbus enable, just for debug purpose in case when we wanna check the coef in ram in correct or not
9	R/W	0x0	if true, use 9bit resolution coef, other use 8bit resolution coef
8	R/W	0x0	type of index, 0: vertical coef, 1: horizontal coef
6-0	R/W	0x0	coef index

Table 9-1519 VPP_OSD_SCALE_COEF 0x1dcd

Bit(s)	R/W	Default	Description
31-0	R/W	0x0	

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Table 9-1520 OSD_DB_FLT_CTRL 0x3140

Bit(s)	R/W	Default	Description
26	R/W	1	reg_nrdeband_reset1 : // unsigned , default = 0 0 : no reset seed 1: reload chroma seed
25	R/W	1	reg_nrdeband_reset0 : // unsigned , default = 0 0 : no reset seed 1: reload luma seed
24	R/W	0	reg_nrdeband_rgb : // unsigned , default = 0 0 : yuv 1: RGB
23	R/W	0	reg_nrdeband_en11 : // unsigned , default = 1 debanding registers of side lines, [0] for luma, same for below
22	R/W	0	reg_nrdeband_en10 : // unsigned , default = 1 debanding registers of side lines, [1] for chroma, same for below
21	R/W	1	reg_nrdeband_siderand : // unsigned , default = 1 options to use side two lines use the rand, instead of use for the YUV three component of middle line, 0: seed [3]/bandrand[3] for middle line yuv; 1: seed[3]/bandrand[3] for nearby three lines Y;
20	R/W	0	reg_nrdeband_randmode : // unsigned , default = 0 mode of rand noise adding, 0: same noise strength for all difs; else: strenght of noise will not exceed the difs, MIN((pPKReg->reg_nrdeband_bandrand[m]), noise[m])
19:17	R/W	6	reg_nrdeband_bandrand2 : // unsigned , default = 6
15:13	R/W	6	reg_nrdeband_bandrand1 : // unsigned , default = 6
11: 9	R/W	6	reg_nrdeband_bandrand0 : // unsigned , default = 6
7	R/W	1	reg_nrdeband_hpxor1 : // unsigned , default = 1 debanding random hp portion xor, [0] for luma
6	R/W	1	reg_nrdeband_hpxor0 : // unsigned , default = 1 debanding random hp portion xor, [1] for chroma
5	R/W	0	reg_nrdeband_en1 : // unsigned , default = 1 debanding registers, for luma
4	R/W	0	reg_nrdeband_en0 : // unsigned , default = 1 debanding registers, for chroma
3: 2	R/W	2	reg_nrdeband_lpf_mode1 : // unsigned , default = 2 lpf mode, 0: 3x3, 1:3x5; 2: 5x5; 3:5x7
1: 0	R/W	2	reg_nrdeband_lpf_mode0 : // unsigned , default = 2 lpf mode, 0: 3x3, 1:3x5; 2: 5x5; 3:5x7

Table 9-1521 OSD_DB_FLT_CTRL1 0x3141

Bit(s)	R/W	Default	Description
31:18			reserved
17:16	R/W	2	Reg_osddeband_noise_rs
15:12	R/W	8	Reg_osddeband_randgain
11			reserved
10:8	R/W	6	Reg_osddedband_bandrand5
7			reserved
6: 4	R/W	6	Reg_osddedband_bandrand4
3			reserved
2: 0	R/W	6	Reg_osddeband_bandrand3

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Table 9-1522 OSD_DB_FLT_LUMA_THRD 0x3142

Bit(s)	R/W	Default	Description
31:30			
29:24	R/W	36	reg_nrdeband_luma_th3 : // unsigned , default = 7 elseif <th[1] use (lpf*3 + y)/4
23:22			
21:16	R/W	28	reg_nrdeband_luma_th2 : // unsigned , default = 5 elseif <th[1] use (lpf*3 + y)/ 4elseif elseif <th[3] (lpf*1 + 3*y)/4; else
15:14			
13: 8	R/W	24	reg_nrdeband_luma_th1 : // unsigned , default = 7 elseif <th[1] use (lpf*3 + y)/4
7: 6			
5: 0	R/W	20	reg_nrdeband_luma_th0 : // unsigned , default = 5 elseif <th[1] use (lpf*3 + y)/ 4elseif elseif

Table 9-1523 OSD_DB_FLT_LUMA_THRD 0x3143

Bit(s)	R/W	Default	Description
31:30			
29:24	R/W	36	reg_nrdeband_chrm_th3 : // unsigned , default = 7 elseif <th[1] use (lpf*3 + y)/4
23:22			
21:16	R/W	28	reg_nrdeband_chrm_th2 : // unsigned , default = 5 elseif <th[1] use (lpf*3 + y)/ 4elseif elseif <th[3] (lpf*1 + 3*y)/4; else
15:14			
13: 8	R/W	24	reg_nrdeband_chrm_th1 : // unsigned , default = 7 elseif <th[1] use (lpf*3 + y)/4
7: 6			
5: 0	R/W	20	reg_nrdeband_chrm_th0 : // unsigned , default = 5 elseif <th[1] use (lpf*3 + y)/ 4elseif elseif

Table 9-1524 OSD_DB_FLT_RANDLUT 0x3144

Bit(s)	R/W	Default	Description
23:21	R/W	1	reg_nrdeband_randslut7 : // unsigned , default = 1 lut0
20:18	R/W	1	reg_nrdeband_randslut6 : // unsigned , default = 1 lut0
17:15	R/W	1	reg_nrdeband_randslut5 : // unsigned , default = 1 lut0
14:12	R/W	1	reg_nrdeband_randslut4 : // unsigned , default = 1 lut0
11: 9	R/W	1	reg_nrdeband_randslut3 : // unsigned , default = 1 lut0
8: 6	R/W	1	reg_nrdeband_randslut2 : // unsigned , default = 1 lut0
5: 3	R/W	1	reg_nrdeband_randslut1 : // unsigned , default = 1 lut0
2: 0	R/W	1	reg_nrdeband_randslut0 : // unsigned , default = 1 lut0

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Table 9-1525 OSD_DB_FLT_PXI_THRD 0x3145

Bit(s)	R/W	Default	Description
25:16	R/W	0	reg_nrdeband_yc_th1 : // unsigned , default = 0 to luma/|u/v| for using the denoise
9: 0	R/W	0	reg_nrdeband_yc_th0 : // unsigned , default = 0 to luma/|u/v| for using the denoise

Table 9-1526 OSD_DB_FLT_SEED_Y 0x3146

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8240	reg_nrdeband_seed0 : // unsigned , default = 1621438240 noise adding seed for Y. seed[0]= 0x60a52f20; as default

Table 9-1527 OSD_DB_FLT_SEED_U 0x3147

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8247	reg_nrdeband_seed1 : // unsigned , default = 1621438247 noise adding seed for U. seed[0]= 0x60a52f27; as default

Table 9-1528 OSD_DB_FLT_SEED_V 0x3148

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8242	reg_nrdeband_seed2 : // unsigned , default = 1621438242 noise adding seed for V. seed[0]= 0x60a52f22; as default

Table 9-1529 OSD_DB_FLT_SEED3 0x3149

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8242	reg_nrdeband_seed3 : // unsigned , default = 1621438242 noise adding seed for V. seed[0]= 0x60a52f22; as default

Table 9-1530 OSD_DB_FLT_SEED4 0x314a

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8242	reg_nrdeband_seed4 : // unsigned , default = 1621438242 noise adding seed for V. seed[0]= 0x60a52f22; as default

Table 9-1531 OSD_DB_FLT_SEED5 0x314b

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8242	reg_nrdeband_seed5 : // unsigned , default = 1621438242 noise adding seed for V. seed[0]= 0x60a52f22; as default

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9.2.3.28 VPP OSD2 SCALER Registers

Table 9-1532 SCALER OSD2_VSC_PHASE_STEP 0x3d00

Bit(s)	R/W	Default	Description
27-0	R/W	0x0100-0000	4.24 format

Table 9-1533 OSD2_VSC_INI_PHASE 0x3d01

Bit(s)	R/W	Default	Description
31-16	R/W	0x0	botttom vertical scaler initial phase
15-0	R/W	0x0	top vertical scaler initial phase

Table 9-1534 OSD2_VSC_CTRL0 0x3d02

Bit(s)	R/W	Default	Description
25	R/W	0	Repeat last line en : 1:enable repeat last line 0:disable repeat last line
24	R/W	0x0	osd vertical Scaler enable
23	R/W	0x0	osd_prog_interlace 0: current field is progressive, 1: current field is interlace
22-21	R/W	0x0	osd_vsc_double_line_mode, bit1, double input width and half input height, bit0, change line buffer becomes 2 lines
20	R/W	0x0	osd_vsc_phase0_always_en
19	R/W	0x0	osd_vsc_nearest_en
17-16	R/W	0x0	osd_vsc_bot_rpt_l0_num
14-11	R/W	0x0	osd_vsc_bot_ini_rcv_num
9-8	R/W	0x0	osd_vsc_top_rpt_l0_num
6-3	R/W	0x0	osd_vsc_top_ini_rcv_num
2-0	R/W	0x0	osd_vsc_bank_length

Table 9-1535 OSD2_HSC_PHASE_STEP 0x3d03

Bit(s)	R/W	Default	Description
27-0	R/W	0x0100-0000	4.24 format

Table 9-1536 OSD2_HSC_INI_PHASE 0x3d04

Bit(s)	R/W	Default	Description
31-16	R/W	0x0	horizontal scaler initial phase1
15-0	R/W	0x0	horizontal scaler initial phase0

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Table 9-1537 OSD2_HSC_CTRL0 0x3d05

Bit(s)	R/W	Default	Description
22	R/W	0x0	osd horizontal Scaler enable
21	R/W	0x0	osd_hsc_double_pix_mode
20	R/W	0x0	osd_hsc_phase0_always_en
19	R/W	0x0	osd_vsc_nearest_en
17-16	R/W	0x0	osd_hsc_rpt_p0_num1
14-11	R/W	0x0	osd_hsc_ini_rcv_num1
9-8	R/W	0x0	osd_hsc_rpt_p0_num0
6-3	R/W	0x0	osd_hsc_ini_rcv_num0
2-0	R/W	0x0	osd_hsc_bank_length

Table 9-1538 OSD2_HSC_INI_PAT_CTRL 0x3d06

Bit(s)	R/W	Default	Description
15-8	R/W	0x0	for 3D quincunx sub-sampling. pattern, each patten 1 bit, from lsb -> msb
6-4	R/W	0x0	pattern start
2-0	R/W	0x0	pattern end

Table 9-1539 OSD2_SC_DUMMY_DATA 0x3d07

Bit(s)	R/W	Default	Description
31-24	R/W	0x0	componet 0 ,data = (dst_data >> 4) ,so 8 bit in 12bit mode, 6bit in 10bit mode
23-16	R/W	0x0	component 1 ,data = (dst_data >> 4) ,so 8 bit in 12bit mode, 6bit in 10bit mode
15-8	R/W	0x0	component 2 ,data = (dst_data >> 4) ,so 8 bit in 12bit mode, 6bit in 10bit mode
7-0	R/W	0x0	component 3 , alpha

Table 9-1540 OSD2_SC_CTRL0 0x3d08

Bit(s)	R/W	Default	Description
27:16	R/W	0	osd_sc_gclk_ctrl : //unsigned,default = 0,osd_sc_gclk_ctrl
13	R/W	0	osd_sc_din_osd_alpha_mode : //unsigned,default = 0,osc_sc_din_osd2_alpha_mode, 1: (alpha >= 128) ? alpha -1: alpha, 0: (alpha >=1) ? alpha - 1: alpha.
12	R/W	0	osd_sc_dout_alpha_mode : //unsigned,default = 0,osc_sc_alpha_mode, 1: (alpha >= 128) ? alpha + 1: alpha, 0: (alpha >=1) ? alpha + 1: alpha.
11:4	R/W	0	osd_sc_alpha : //unsigned,default = 0,default alpha for vd1 or vd2 if they are selected as the source
3	R/W	0	osd_sc_path_en : //unsigned,default = 0,osd scaler path enable
2	R/W	0	osd_sc_en : //unsigned,default = 0,osd scaler enable

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Table 9-1541 OSD2_SCI_WH_M1 0x3d09

Bit(s)	R/W	Default	Description
28-16	R/W	0x0	OSD scaler input width minus 1
12-0	R/W	0x0	OSD scaler input height minus 1

Table 9-1542 OSD2_SCO_H_START_END 0x3d0a

Bit(s)	R/W	Default	Description
27-16	R/W	0x0	OSD scaler output horizontal start
11-0	R/W	0x0	OSD scaler output horizontal end

Table 9-1543 OSD2_SCO_V_START_END 0x3d0b

Bit(s)	R/W	Default	Description
27-16	R/W	0x0	OSD scaler output vertical start
11-0	R/W	0x0	OSD scaler output vertical end

Table 9-1544 OSD2_SCALE_COEF_IDX 0x3d18

Bit(s)	R/W	Default	Description

15	R/W	0x0	Because there are many coefficients used in the vertical filter and horizontal filters,
			//indirect access the coefficients of vertical filter and horizontal filter is used.
			//For vertical filter, there are 33x4 coefficients
			//For horizontal filter, there are 33x4 coefficients
			//Bit 15 index increment, if bit9 == 1 then (0: index increase 1, 1: index increase 2) else (index increase 2)

14	R/W	0x0	1: read coef through cbus enable, just for debug purpose in case when we wanna check the coef in ram in correct or not
9	R/W	0x0	if true, use 9bit resolution coef, other use 8bit resolution coef
8	R/W	0x0	type of index, 0: vertical coef, 1: horizontal coef
6-0	R/W	0x0	coef index

Table 9-1545 OSD2_SCALE_COEF 0x3d19

Bit(s)	R/W	Default	Description
31-0	R/W	0x0	

9.2.3.29 VPP OSD_BLD34 SCALER Registers

Table 9-1546 OSD34_VSC_PHASE_STEP 0x3d20

Bit(s)	R/W	Default	Description
27-0	R/W	0x0100-0000	4.24 format

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Table 9-1547 OSD34_VSC_INI_PHASE 0x3d21

Bit(s)	R/W	Default	Description
31-16	R/W	0x0	botttom vertical scaler initial phase
15-0	R/W	0x0	top vertical scaler initial phase

Table 9-1548 OSD34_VSC_CTRL0 0x3d22

Bit(s)	R/W	Default	Description
25	R/W	0	Repeat last line en : 1:enable repeat last line 0:disable repeat last line
24	R/W	0x0	osd vertical Scaler enable
23	R/W	0x0	osd_prog_interlace 0: current field is progressive, 1: current field is interlace
22-21	R/W	0x0	osd_vsc_double_line_mode, bit1, double input width and half input height, bit0, change line buffer becomes 2 lines
20	R/W	0x0	osd_vsc_phase0_always_en
19	R/W	0x0	osd_vsc_nearest_en
17-16	R/W	0x0	osd_vsc_bot_rpt_l0_num
14-11	R/W	0x0	osd_vsc_bot_ini_rcv_num
9-8	R/W	0x0	osd_vsc_top_rpt_l0_num
6-3	R/W	0x0	osd_vsc_top_ini_rcv_num
2-0	R/W	0x0	osd_vsc_bank_length

Table 9-1549 OSD34_HSC_PHASE_STEP 0x3d23

Bit(s)	R/W	Default	Description
27-0	R/W	0x0100-0000	4.24 format

Table 9-1550 OSD34_HSC_INI_PHASE 0x3d24

Bit(s)	R/W	Default	Description
31-16	R/W	0x0	horizontal scaler initial phase1
15-0	R/W	0x0	horizontal scaler initial phase0

Table 9-1551 OSD34_HSC_CTRL0 0x3d25

Bit(s)	R/W	Default	Description
22	R/W	0x0	osd horizontal Scaler enable
21	R/W	0x0	osd_hsc_double_pix_mode
20	R/W	0x0	osd_hsc_phase0_always_en
19	R/W	0x0	osd_vsc_nearest_en

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Bit(s)	R/W	Default	Description
17-16	R/W	0x0	osd_hsc_rpt_p0_num1
14-11	R/W	0x0	osd_hsc_ini_rcv_num1
9-8	R/W	0x0	osd_hsc_rpt_p0_num0
6-3	R/W	0x0	osd_hsc_ini_rcv_num0
2-0	R/W	0x0	osd_hsc_bank_length

Table 9-1552 OSD34_HSC_INI_PAT_CTRL 0x3d26

Bit(s)	R/W	Default	Description
15-8	R/W	0x0	for 3D quincunx sub-sampling. pattern, each patten 1 bit, from lsb -> msb
6-4	R/W	0x0	pattern start
2-0	R/W	0x0	pattern end

Table 9-1553 OSD34_SC_DUMMY_DATA 0x3d27

Bit(s)	R/W	Default	Description
31-24	R/W	0x0	componet 0 ,data = (dst_data >> 4) ,so 8 bit in 12bit mode, 6bit in 10bit mode
23-16	R/W	0x0	component 1 ,data = (dst_data >> 4) ,so 8 bit in 12bit mode, 6bit in 10bit mode
15-8	R/W	0x0	component 2 ,data = (dst_data >> 4) ,so 8 bit in 12bit mode, 6bit in 10bit mode
7-0	R/W	0x0	component 3 , alpha

Table 9-1554 OSD34_SC_CTRL0 0x3d28

Bit(s)	R/W	Default	Description
27:16	R/W	0	osd_sc_gclk_ctrl : //unsigned,default = 0,osd_sc_gclk_ctrl
13	R/W	0	osd_sc_din_osd_alpha_mode : //unsigned,default = 0,osc_sc_din_osd2_alpha_mode, 1: (alpha >= 128) ? alpha -1: alpha, 0: (alpha >=1) ? alpha - 1: alpha.
12	R/W	0	osd_sc_dout_alpha_mode : //unsigned,default = 0,osc_sc_alpha_mode, 1: (alpha >= 128) ? alpha + 1: alpha, 0: (alpha >=1) ? alpha + 1: alpha.
11:4	R/W	0	osd_sc_alpha : //unsigned,default = 0,default alpha for vd1 or vd2 if they are selected as the source
3	R/W	0	osd_sc_path_en : //unsigned,default = 0,osd scaler path enable
2	R/W	0	osd_sc_en : //unsigned,default = 0,osd scaler enable

Table 9-1555 OSD34_SCI_WH_M1 0x3d29

Bit(s)	R/W	Default	Description
28-16	R/W	0x0	OSD scaler input width minus 1
12-0	R/W	0x0	OSD scaler input height minus 1

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Table 9-1556 OSD34_SCO_H_START_END 0x3d2a

Bit(s)	R/W	Default	Description
27-16	R/W	0x0	OSD scaler output horizontal start
11-0	R/W	0x0	OSD scaler output horizontal end

Table 9-1557 OSD34_SCO_V_START_END 0x3d2b

Bit(s)	R/W	Default	Description
27-16	R/W	0x0	OSD scaler output vertical start
11-0	R/W	0x0	OSD scaler output vertical end

Table 9-1558 OSD34_SCALE_COEF_IDX 0x3d1e

Bit(s)	R/W	Default	Description

15	R/W	0x0	Because there are many coefficients used in the vertical filter and horizontal filters,
			//indirect access the coefficients of vertical filter and horizontal filter is used.
			//For vertical filter, there are 33x4 coefficients
			//For horizontal filter, there are 33x4 coefficients
			//Bit 15 index increment, if bit9 == 1 then (0: index increase 1, 1: index increase 2) else (index increase 2)

14	R/W	0x0	1: read coef through cbus enable, just for debug purpose in case when we wanna check the coef in ram in correct or not
9	R/W	0x0	if true, use 9bit resolution coef, other use 8bit resolution coef
8	R/W	0x0	type of index, 0: vertical coef, 1: horizontal coef
6-0	R/W	0x0	coef index

Table 9-1559 OSD34_SCALE_COEF 0x3d1f

Bit(s)	R/W	Default	Description
31-0	R/W	0x0	

9.2.3.30 VPP VD1 SCALER Registers

Because there are many coefficients used in the vertical filter and horizontal filters, indirect access the coefficients of vertical filter and horizontal filter is used. For vertical filter, there are 33x4 coefficients. For horizontal filter, there are 33x4 coefficients.

Table 9-1560 VPP_SCALE_COEF_IDX 0x1d03

Bit(s)	R/W	Default	Description
15	R/W	0	index_inc : // unsigned , default = 0x0 ,index increment, if bit9 == 1 then (0: index increase 1, 1: index increase 2) else (index increase 2)
14	R/W	0	rd_cbus_coef_en : // unsigned , default = 0x0 ,1: read coef through cbus enable, just for debug purpose in case when we wanna check the coef in ram in correct or not

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Bit(s)	R/W	Default	Description
13	R/W	0	vf_sep_coef_en : // unsigned , default = 0x0 ,if true, vertical separated coef enable
9	R/W	0	high_reso_en : // unsigned , default = 0x0 ,if true, use 9bit resolution coef, other use 8bit resolution coef
8:7	R/W	0	type_index : // unsigned , default = 0x0 ,type of index, 00: vertical coef, 01: vertical chroma coef: 10: horizontal coef, 11: resevered
6:0	R/W	0	coef_index : // unsigned , default = 0x0 ,coef index

Table 9-1561 VPP_SCALE_COEF 0x1d04

Bit(s)	R/W	Default	Description
31:24	R/W	0	coef0 : //signed , default = 0x0 , coefficients for vertical filter and horizontal filter
23:16	R/W	0	coef1 : //signed , default = 0x0 , coefficients for vertical filter and horizontal filter
15:8	R/W	0	coef2 : //signed , default = 0x0 , coefficients for vertical filter and horizontal filter
7 :0	R/W	0	coef3 : //signed , default = 0x0 , coefficients for vertical filter and horizontal filter

Table 9-1562 VPP_VSC_REGION12_STARTP 0x1d05

Bit(s)	R/W	Default	Description
28:16	R/W	0	region1_startp : //unsigned , default = 0 ,region1 startp
12:0	R/W	0	region2_startp : //unsigned , default = 0 ,region2 startp

Table 9-1563 VPP_VSC_REGION34_STARTP 0x1d06

Bit(s)	R/W	Default	Description
28:16	R/W	0	region3_startp : //unsigned , default = 0x0438,region3 startp
12:0	R/W	0	region4_startp : //unsigned , default = 0x0438,region4 startp

Table 9-1564 VPP_VSC_REGION4_ENDP 0x1d07

Bit(s)	R/W	Default	Description
12:0	R/W	13	region4_endp : //unsigned , default = 13'd1079 ,region4 endp

Table 9-1565 VPP_VSC_START_PHASE_STEP 0x1d08

Bit(s)	R/W	Default	Description
27:24	R/W	1	integer_part : //unsigned , default = 1,vertical start phase step, (source/dest)* (2^24),integer part of step
23:0	R/W	0	fraction_part : //unsigned , default = 0,vertical start phase step, (source/dest)* (2^24),fraction part of step

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Table 9-1566 VPP_VSC_REGION0_PHASE_SLOPE 0x1d09

Bit(s)	R/W	Default	Description
24:0	R/W	0	region0_phase_slope : //signed , default = 0,vertical scaler region0 phase slope, region0 phase slope

Table 9-1567 VPP_VSC_REGION1_PHASE_SLOPE 0x1d0a

Bit(s)	R/W	Default	Description
24:0	R/W	0	region1_phase_slope : //signed , default = 0,region1 phase slope

Table 9-1568 VPP_VSC_REGION3_PHASE_SLOPE 0x1d0b

Bit(s)	R/W	Default	Description
24:0	R/W	0	region3_phase_slope : //signed , default = 0,region3 phase slope

Table 9-1569 VPP_VSC_REGION4_PHASE_SLOPE 0x1d0c

Bit(s)	R/W	Default	Description
24:0	R/W	0	region4_phase_slope : //signed , default = 0,region4 phase slope

Table 9-1570 VPP_VSC_PHASE_CTRL 0x1d0d

Bit(s)	R/W	Default	Description
18:17	R/W	0	vsc_double_line_mode : //unsigned , default = 0, double line mode, input/output line width of vscaler becomes 2X, so only 2 line buffer in this case, use for 3D line by line interleave scaling bit1 true, double the input width and half input height, bit0 true, change line buffer 2 lines instead of 4 lines
16	R.O	0	prog_interlace : //unsigned , default = 0,0: progressive output, 1: interlace output
15	R/W	0	vsc_bot_l0_out_en : //unsigned , default = 0,vertical scaler output line0 in advance or not for bottom field
14:13	R/W	1	vsc_bot_rpt_l0_num : //unsigned , default = 1,vertical scaler initial repeat line0 number for bottom field
11:8	R/W	4	vsc_bot_ini_rcv_num : //unsigned , default = 4,vertical scaler initial receiving number for bottom field
7	R/W	0	vsc_top_l0_out_en : //unsigned , default = 0,vertical scaler output line0 in advance or not for top field
6:5	R/W	1	vsc_top_rpt_l0_num : //unsigned , default = 1,vertical scaler initial repeat line0 number for top field
3:0	R/W	4	vsc_top_ini_rcv_num : //unsigned , default = 4,vertical scaler initial receiving number for top field

Table 9-1571 VPP_VSC_INI_PHASE 0x1d0e

Bit(s)	R/W	Default	Description
31:16	R/W	0,	//unsigned , default = 0,vertical scaler field initial phase for bottom field Bit 15:0 //unsigned , default = 0,vertical scaler field initial phase for top field

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Table 9-1572 VPP_HSC_REGION12_STARTP 0x1d10

Bit(s)	R/W	Default	Description
28:16	R/W	0	region1_startp : //unsigned , default = 0,region1 startp
12:0	R/W	0	region2_startp : //unsigned , default = 0,region2 startp

Table 9-1573 VPP_HSC_REGION34_STARTP 0x1d11

Bit(s)	R/W	Default	Description
28:16	R/W	0	region3 : startp //unsigned , default = 0x780,region3 startp
12:0	R/W	0	region4 : startp //unsigned , default = 0x780,region4 startp

Table 9-1574 VPP_HSC_REGION4_ENDP 0x1d12

Bit(s)	R/W	Default	Description
12:0	R/W	13	region4 : startp //unsigned , default = 13'd1919,region4 startp

horizontal start phase step, (source/dest)*(2^24)

Table 9-1575 VPP_HSC_START_PHASE_STEP 0x1d13

Bit(s)	R/W	Default	Description
27:24	R/W	1	integer_part : //unsigned , default = 1,integer part of step
23:0	R/W	0	fraction_part : //unsigned , default = 0,fraction part of step

Table 9-1576 VPP_HSC_REGION0_PHASE_SLOPE 0x1d14

Bit(s)	R/W	Default	Description
24:0	R/W	0	region0_phase_slope : //signed , default = 0,region0 phase slope

Table 9-1577 VPP_HSC_REGION1_PHASE_SLOPE 0x1d15

Bit(s)	R/W	Default	Description
24:0	R/W	0	region0_phase_slope : //signed , default = 0,region1 phase slope

Table 9-1578 VPP_HSC_REGION3_PHASE_SLOPE 0x1d16

Bit(s)	R/W	Default	Description
24:0	R/W	0	region0_phase_slope : //signed , default = 0,region3 phase slope

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Table 9-1579 VPP_HSC_REGION4_PHASE_SLOPE 0x1d17

Bit(s)	R/W	Default	Description
24:0	R/W	0	region0_phase_slope : //signed , default = 0,region4 phase slope

Table 9-1580 VPP_HSC_PHASE_CTRL 0x1d18

Bit(s)	R/W	Default	Description
22:21	R/W	1	hsc_rpt_p0_num0 : //unsigned , default = 1 ,horizontal scaler initial repeat pixel0 number0
19:16	R/W	4	hsc_ini_rcv_num0 : //unsigned , default = 4 ,horizontal scaler initial receiving number0
15:0	R/W	0	hsc_ini_phase0 : //unsigned , default = 0 ,horizontal scaler top field initial phase0

Table 9-1581 VPP_SC_MISC 0x1d19

Bit(s)	R/W	Default	Description
24	R/W	0	Repeat last line en : 1:enable repeat last line 0:disable repeat last line
22	R/W	0	hsc_len_div2_en : //unsigned , default = 0 ,if true, divide VSC line length 2 as the HSC input length, othwise VSC length length is the same as the VSC line length just for special usage, more flexibilityi
21	R/W	0	lbuf_mode : //unsigned , default = 0 ,if true, prevsc uses lin buffer, otherwise prevsc does not use line buffer, it should be same as prevsc_en
20	R/W	0	prehsc_en : //unsigned , default = 0 ,prehsc_en
19	R/W	0	prevsc_en : //unsigned , default = 0 ,prevsc_en
18	R/W	0	vsc_en : //unsigned , default = 0 ,vsc_en
17	R/W	0	hsc_en : //unsigned , default = 0 ,hsc_en
16	R/W	0	sc_top_en : //unsigned , default = 0 ,scale_top_en
15	R/W	0	sc_vd_en : //unsigned , default = 0 ,video1 scale out enable
12	R/W	1	hsc_nonlinear_4region_en : //unsigned , default = 1 ,if true, region0,region4 are nonlinear regions, otherwise they are not scaling regions, for horizontal scaler
10:8	R/W	0	hsc_bank_length : //unsigned , default = 0 ,horizontal scaler bank length
5	R/W	4	vsc_phase_field_mode : //unsigned , default = 4 ,vertical scaler phase field mode, if true, disable the opposite parity line output, more bandwith needed if output 1080i
4	R/W	0	vsc_nonlinear_4region_en : //unsigned , default = 0 ,if true, region0,region4 are nonlinear regions, otherwise they are not scaling regions, for vertical scaler
2:0	R/W	4	vsc_bank_length : //unsigned , default = 4 ,vertical scaler bank length

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Table 9-1582 VPP_SCO_FIFO_CTRL 0x1d33

Bit(s)	R/W	Default	Description
27:16	R/W	0	sco_fifo_line_lenm1 : //unsigned , default = 0xfff, scale out fifo line length minus 1
12:0	R/W	0	sco_fifo_size : //unsigned , default = 0x200, scale out fifo size (actually only bit 11:1 is valid, 11:1, max 1024), always even number

for 3D quincunx sub-sampling and horizontal pixel by pixel 3D interleaving

Table 9-1583 VPP_HSC_PHASE_CTRL1 0x1d34

Bit(s)	R/W	Default	Description
27:24	R/W	0	prehsc_mode : //unsigned , default = 0,prehsc_mode, bit 3:2, prehsc odd line interp mode, bit 1:0, prehsc even line interp mode, each 2bit, 00: pix0+pix1/2, average, 01: pix1, 10: pix0
23	R/W	0	hsc_double_pix_mode : //unsigned , default = 0,horizontal scaler double pixel mode
22:21	R/W	1	hsc_rpt_p0_num1 : //unsigned , default = 1,horizontal scaler initial repeat pixel0 number1
19:16	R/W	4	hsc_ini_rcv_num1 : //unsigned , default = 4,horizontal scaler initial receiving number1
15:0	R/W	0	hsc_ini_phase1 : //unsigned , default = 0,horizontal scaler top field initial phase1

Table 9-1584 for 3D quincunx sub-sampling VPP_HSC_INI_PAT_CTRL 0x1d35

Bit(s)	R/W	Default	Description
31:24	R/W	0	prehsc_pattern : //unsigned , default = 0, prehsc pattern, each patten 1 bit, from lsb -> msb
22:20	R/W	0	prehsc_pat_star : //unsigned , default = 0, prehsc pattern start
18:16	R/W	0	prehsc_pat_end : //unsigned , default = 0, prehsc pattern end
15:8	R/W	0	hsc_pattern : //unsigned , default = 0, hsc pattern, each patten 1 bit, from lsb -> msb
6:4	R/W	0	hsc_pat_start : //unsigned , default = 0, hsc pattern start
2:0	R/W	0	hsc_pat_end : //unsigned , default = 0, hsc pattern end

Table 9-1585 VPP_SC_GCLK_CTRL 0x1d35

Bit(s)	R/W	Default	Description
15:0	R/W	0	vpp_sc_gclk_ctrl : //unsigned , default = 0 ,scale clock gate

9.2.3.31 VPP VD2 SCALER Registers

Because there are many coefficients used in the vertical filter and horizontal filters, indirect access the coefficients of vertical filter and horizontal filter is used. For vertical filter, there are 33x4 coefficients. For horizontal filter, there are 33x4 coefficients.

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Table 9-1586 VD2_SCALE_COEF_IDX 0x3943

Bit(s)	R/W	Default	Description
15	R/W	0	index_inc : // unsigned , default = 0x0 ,index increment, if bit9 == 1 then (0: index increase 1, 1: index increase 2) else (index increase 2)
14	R/W	0	rd_cbus_coef_en : // unsigned , default = 0x0 ,1: read coef through cbus enable, just for debug purpose in case when we wanna check the coef in ram in correct or not
13	R/W	0	vf_sep_coef_en : // unsigned , default = 0x0 ,if true, vertical separated coef enable
9	R/W	0	high_reso_en : // unsigned , default = 0x0 ,if true, use 9bit resolution coef, other use 8bit resolution coef
8:7	R/W	0	type_index : // unsigned , default = 0x0 ,type of index, 00: vertical coef, 01: vertical chroma coef: 10: horizontal coef, 11: resevered
6:0	R/W	0	coef_index : // unsigned , default = 0x0 ,coef index

Table 9-1587 VD2_SCALE_COEF 0x3944

Bit(s)	R/W	Default	Description
31:24	R/W	0	coef0 : //signed , default = 0x0 , coefficients for vertical filter and horizontal filter
23:16	R/W	0	coef1 : //signed , default = 0x0 , coefficients for vertical filter and horizontal filter
15:8	R/W	0	coef2 : //signed , default = 0x0 , coefficients for vertical filter and horizontal filter
7 :0	R/W	0	coef3 : //signed , default = 0x0 , coefficients for vertical filter and horizontal filter

Table 9-1588 VD2_VSC_REGION12_STARTP 0x3945

Bit(s)	R/W	Default	Description
28:16	R/W	0	region1_startp : //unsigned , default = 0 ,region1 startp
12:0	R/W	0	region2_startp : //unsigned , default = 0 ,region2 startp

Table 9-1589 VD2_VSC_REGION34_STARTP 0x3946

Bit(s)	R/W		Default
28:16		R/W	region3_startp : //unsigned , default = 0x0438,region3 startp
12:0		R/W	region4_startp : //unsigned , default = 0x0438,region4 startp

Table 9-1590 VD2_VSC_REGION4_ENDP 0x3947

Bit(s)	R/W	Default	Description
12:0	R/W	13	region4_endp : //unsigned , default = 13'd1079 ,region4 endp

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Table 9-1591 VD2_VSC_START_PHASE_STEP 0x3948

Bit(s)	R/W	Default	Description
27:24	R/W	1	integer_part : //unsigned , default = 1,vertical start phase step, (source/dest)* (2^24),integer part of step
23:0	R/W	0	fraction_part : //unsigned , default = 0,vertical start phase step, (source/dest)* (2^24),fraction part of step

Table 9-1592 VD2_VSC_REGION0_PHASE_SLOPE 0x3949

Bit(s)	R/W	Default	Description
24:0	R/W	0	region0_phase_slope : //signed , default = 0,vertical scaler region0 phase slope, region0 phase slope

Table 9-1593 VD2_VSC_REGION1_PHASE_SLOPE 0x394a

Bit(s)	R/W	Default	Description
24:0	R/W	0	region1_phase_slope : //signed , default = 0,region1 phase slope

Table 9-1594 VD2_VSC_REGION3_PHASE_SLOPE 0x394b

Bit(s)	R/W	Default	Description
24:0	R/W	0	region3_phase_slope : //signed , default = 0,region3 phase slope

Table 9-1595 VD2_VSC_REGION4_PHASE_SLOPE 0x394c

Bit(s)	R/W	Default	Description
24:0	R/W	0	region4_phase_slope : //signed , default = 0,region4 phase slope

Table 9-1596 VD2_VSC_PHASE_CTRL 0x394d

Bit(s)	R/W	Default	Description
18:17	R/W	0	vsc_double_line_mode : //unsigned , default = 0, double line mode, input/output line width of vscaler becomes 2X, so only 2 line buffer in this case, use for 3D line by line interleave scaling bit1 true, double the input width and half input height, bit0 true, change line buffer 2 lines instead of 4 lines
16	R.O	0	prog_interlace : //unsigned , default = 0,0: progressive output, 1: interlace output
15	R/W	0	vsc_bot_l0_out_en : //unsigned , default = 0,vertical scaler output line0 in advance or not for bottom field
14:13	R/W	1	vsc_bot_rpt_l0_num : //unsigned , default = 1,vertical scaler initial repeat line0 number for bottom field
11:8	R/W	4	vsc_bot_ini_rcv_num : //unsigned , default = 4,vertical scaler initial receiving number for bottom field
7	R/W	0	vsc_top_l0_out_en : //unsigned , default = 0,vertical scaler output line0 in advance or not for top field

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Bit(s)	R/W	Default	Description
6:5	R/W	1	vsc_top_rpt_l0_num : //unsigned , default = 1,vertical scaler initial repeat line0 number for top field
3:0	R/W	4	vsc_top_ini_rcv_num : //unsigned , default = 4,vertical scaler initial receiving number for top field

Table 9-1597 VD2_VSC_INI_PHASE 0x394e

Bit(s)	R/W	Default	Description
31:16	R/W	0,	//unsigned , default = 0,vertical scaler field initial phase for bottom field Bit 15:0 //unsigned , default = 0,vertical scaler field initial phase for top field

Table 9-1598 VD2_HSC_REGION12_STARTP 0x394f

Bit(s)	R/W	Default	Description
28:16	R/W	0	region1_startp : //unsigned , default = 0,region1 startp
12:0	R/W	0	region2_startp : //unsigned , default = 0,region2 startp

Table 9-1599 VD2_HSC_REGION34_STARTP 0x3950

Bit(s)	R/W	Default	Description
28:16	R/W	0	region3 : startp //unsigned , default = 0x780,region3 startp
12:0	R/W	0	region4 : startp //unsigned , default = 0x780,region4 startp

Table 9-1600 VD2_HSC_REGION4_ENDP 0x3951

Bit(s)	R/W	Default	Description
12:0	R/W	13	region4 : startp //unsigned , default = 13'd1919,region4 startp

horizontal start phase step, (source/dest)*(2^24)

Table 9-1601 VD2_HSC_START_PHASE_STEP 0x3952

Bit(s)	R/W	Default	Description
27:24	R/W	1	integer_part : //unsigned , default = 1,integer part of step
23:0	R/W	0	fraction_part : //unsigned , default = 0,fraction part of step

Table 9-1602 VD2_HSC_REGION0_PHASE_SLOPE 0x3953

Bit(s)	R/W	Default	Description
24:0	R/W	0	region0_phase_slope : //signed , default = 0,region0 phase slope

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Table 9-1603 VD2_HSC_REGION1_PHASE_SLOPE 0x3954

Bit(s)	R/W	Default	Description
24:0	R/W	0	region0_phase_slope : //signed , default = 0,region1 phase slope

Table 9-1604 VD2_HSC_REGION3_PHASE_SLOPE 0x3955

Bit(s)	R/W	Default	Description
24:0	R/W	0	region0_phase_slope : //signed , default = 0,region3 phase slope

Table 9-1605 VD2_HSC_REGION4_PHASE_SLOPE 0x3956

Bit(s)	R/W	Default	Description
24:0	R/W	0	region0_phase_slope : //signed , default = 0,region4 phase slope

Table 9-1606 VD2_HSC_PHASE_CTRL 0x3957

Bit(s)	R/W	Default	Description
22:21	R/W	1	hsc_rpt_p0_num0 : //unsigned , default = 1 ,horizontal scaler initial repeat pixel0 number0
19:16	R/W	4	hsc_ini_rcv_num0 : //unsigned , default = 4 ,horizontal scaler initial receiving number0
15:0	R/W	0	hsc_ini_phase0 : //unsigned , default = 0 ,horizontal scaler top field initial phase0

Table 9-1607 VD2_SC_MISC 0x3958

Bit(s)	R/W	Default	Description
24	R/W	0	Repeat last line en : 1:enable repeat last line 0:disable repeat last line
22	R/W	0	hsc_len_div2_en : //unsigned , default = 0 ,if true, divide VSC line length 2 as the HSC input length, othwise VSC length length is the same as the VSC line length just for special usage, more flexibilityi
21	R/W	0	lbuf_mode : //unsigned , default = 0 ,if true, prevsc uses lin buffer, otherwise prevsc does not use line buffer, it should be same as prevsc_en
20	R/W	0	prehsc_en : //unsigned , default = 0 ,prehsc_en
19	R/W	0	prevsc_en : //unsigned , default = 0 ,prevsc_en
18	R/W	0	vsc_en : //unsigned , default = 0 ,vsc_en
17	R/W	0	hsc_en : //unsigned , default = 0 ,hsc_en
16	R/W	0	sc_top_en : //unsigned , default = 0 ,scale_top_en
15	R/W	0	sc_vd_en : //unsigned , default = 0 ,video1 scale out enable
12	R/W	1	hsc_nonlinear_4region_en : //unsigned , default = 1 ,if true, region0,region4 are nonlinear regions, otherwise they are not scaling regions, for horizontal scaler
10:8	R/W	0	hsc_bank_length : //unsigned , default = 0 ,horizontal scaler bank length
5	R/W	4	vsc_phase_field_mode : //unsigned , default = 4 ,vertical scaler phase field mode, if true, disable the opposite parity line output, more bandwith needed if output 1080i

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Bit(s)	R/W	Default	Description
4	R/W	0	vsc_nonlinear_4region_en : //unsigned , default = 0 ,if true, region0,region4 are nonlinear regions, otherwise they are not scaling regions, for vertical scaler
2:0	R/W	4	vsc_bank_length : //unsigned , default = 4 ,vertical scaler bank length

Table 9-1608 VD2_SCO_FIFO_CTRL 0x3959

Bit(s)	R/W	Default	Description
27:16	R/W	0	sco_fifo_line_lenm1 : //unsigned , default = 0xfff, scale out fifo line length minus 1
12:0	R/W	0	sco_fifo_size : //unsigned , default = 0x200, scale out fifo size (actually only bit 11:1 is valid, 11:1, max 1024), always even number

For 3D quincunx sub-sampling and horizontal pixel by pixel 3D interleaving.

Table 9-1609 VD2_HSC_PHASE_CTRL1 0x395a

Bit(s)	R/W	Default	Description
27:24	R/W	0	prehsc_mode : //unsigned , default = 0,prehsc_mode, bit 3:2, prehsc odd line interp mode, bit 1:0, prehsc even line interp mode, each 2bit, 00: pix0+pix1/2, average, 01: pix1, 10: pix0
23	R/W	0	hsc_double_pix_mode : //unsigned , default = 0,horizontal scaler double pixel mode
22:21	R/W	1	hsc_rpt_p0_num1 : //unsigned , default = 1,horizontal scaler initial repeat pixel0 number1
19:16	R/W	4	hsc_ini_rcv_num1 : //unsigned , default = 4,horizontal scaler initial receiving number1
15:0	R/W	0	hsc_ini_phase1 : //unsigned , default = 0,horizontal scaler top field initial phase1

For 3D quincunx sub-sampling.

Table 9-1610 VD2_HSC_INI_PAT_CTRL 0x395b

Bit(s)	R/W	Default	Description
31:24	R/W	0	prehsc_pattern : //unsigned , default = 0, prehsc pattern, each patten 1 bit, from lsb -> msb
22:20	R/W	0	prehsc_pat_star : //unsigned , default = 0, prehsc pattern start
18:16	R/W	0	prehsc_pat_end : //unsigned , default = 0, prehsc pattern end
15:8	R/W	0	hsc_pattern : //unsigned , default = 0, hsc pattern, each patten 1 bit, from lsb -> msb
6:4	R/W	0	hsc_pat_start : //unsigned , default = 0, hsc pattern start
2:0	R/W	0	hsc_pat_end : //unsigned , default = 0, hsc pattern end

Table 9-1611 VD2_SC_GCLK_CTRL 0x395c

Bit(s)	R/W	Default	Description
15:0	R/W	0	vpp_sc_gclk_ctrl : //unsigned , default = 0 ,scale clock gate

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Table 9-1612 VD2_PREHSC_COEF 0x395d

Bit(s)	R/W	Default	Description
31:24	R/W	64	prehsc_coef3 //signed
23:16	R/W	0	prehsc_coef2 //signed
15:8	R/W	0	prehsc_coef1 //signed
7:0	R/W	0	prehsc_coef0 //signed

Table 9-1613 VD2_PRE_SCALE_CTRL 0x395e

Bit(s)	R/W	Default	Description
10:7	R/W	2	prehsc_flt_num//unsigned 2: 2tap 4:4tap 6:6tap 8:8tap
6:4	R/W	2	prevsc_flt_num//unsiged 2: 2tap 4:4tap
3:2	R/W	1	prehsc_ds_ratio//unsigned 0:(1:1 mode) 1:(2:1 mode)
1:0	R/W	1	prevsc_ds_ratio//unsigned 0:(1:1 mode) 1:(2:1 mode)

Table 9-1614 VD2_PREVSC_COEF 0x395f

Bit(s)	R/W	Default	Description
15:8	R/W	64	prevsc_coef1 //signed
7:0	R/W	0	prevsc_coef0 //signed

9.2.3.32 Supper Scale/ Sharpness Registers

Table 9-1615 SRSHARP0_SHARP_HVSIZE 0x5000

Bit(s)	R/W	Default	Description
28:16	R/W	0d1920	reg_pknr_hsize : . unsigned , default = 1920
12: 0	R/W	0d1080	reg_pknr_vsize : . unsigned , default = 1080

Table 9-1616 SRSHARP0_SHARP_HVBLANK_NUM 0x5001

Bit(s)	R/W	Default	Description
23: 16	R/W	0d8	reg_deband_hblank : . unsigned , default = 8
15: 8	R/W	0d20	reg_pknr_hblank_num : . unsigned , default = 20
7: 0	R/W	0d60	reg_pknr_vblank_num : . unsigned , default = 60

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Table 9-1617 SRSHARP0_NR_GAUSSIAN_MODE 0x5002

Bit(s)	R/W	Default	Description
13□12	R/W	0d0	reg_nr_gau_cnorm: Y adpative coef norm, 0: 128, 1: 256, 2: 512, 3: 1024 .unsigned , default = 0
9□8	R/W	0d0	reg_nr_gau_cnorm: C adpative coef norm, 0: 128, 1: 256, 2: 512, 3: 1024 .unsigned , default = 0
5□4	R/W	0d1	reg_nr_gau_ymode:0 3x3 filter; 1: 5x5 filter, 2/3: adpative coef . unsigned , default = 1
1□0	R/W	0d1	reg_nr_gau_cmode:0 3x3 filter; 1: 5x5 filter, 2/3: adpative coef . unsigned , default = 1

Table 9-1618 SRSHARP0_PK_CON_2CIRHPGAIN_TH_RATE 0x5005

Bit(s)	R/W	Default	Description
31:24	R/W	0d25	reg_pk_cirhpcon2gain0:threshold0 of curve to map hpcon to hpgain for circle hp filter (all 8 direction same). 0~255.. unsigned , default = 25
23:16	R/W	0d60	reg_pk_cirhpcon2gain1:threshold1 of curve to map hpcon to hpgain for circle hp filter (all 8 direction same). 0~255.. unsigned , default = 60
15: 8	R/W	0d80	reg_pk_cirhpcon2gain5:rate0 (for hpcon < th0) of curve to map hpcon to hpgain for circle hp filter (all 8 direction same). 0~255.. unsigned , default = 80
7: 0	R/W	0d20	reg_pk_cirhpcon2gain6:rate1 (for hpcon > th1) of curve to map hpcon to hpgain for circle hp filter (all 8 direction same). 0~255.. unsigned , default = 20

Table 9-1619 SRSHARP0_PK_CON_2CIRHPGAIN_LIMIT 0x5006

Bit(s)	R/W	Default	Description
31:24	R/W	0d96	reg_pk_cirhpcon2gain2:level limit(for hpcon < th0) of curve to map hpcon to hpgain for circle hp filter (all 8 direction same). 0~255.. unsigned , default = 96
23:16	R/W	0d96	reg_pk_cirhpcon2gain3:level limit(for th0 < hpcon < th1) of curve to map hpcon to hpgain for circle hp filter (all 8 direction same). 0~255.. unsigned , default = 96
15: 8	R/W	0d5	reg_pk_cirhpcon2gain4:level limit(for hpcon > th1) of curve to map hpcon to hpgain for circle hp filter (all 8 direction same). 0~255.. unsigned , default = 5

Table 9-1620 SRSHARP0_PK_CON_2CIRBPGAIN_TH_RATE 0x5007

Bit(s)	R/W	Default	Description
31:24	R/W	0d20	reg_pk_cirbpcon2gain0:threshold0 of curve to map bpcon to bpgain for circle bp filter (all 8 direction same). 0~255.. unsigned , default = 20
23:16	R/W	0d50	reg_pk_cirbpcon2gain1:threshold1 of curve to map bpcon to bpgain for circle bp filter (all 8 direction same).. unsigned , default = 50
15: 8	R/W	0d50	reg_pk_cirbpcon2gain5:rate0 (for bpcon < th0) of curve to map bpcon to bpgain for circle bp filter (all 8 direction same). 0~255.. unsigned , default = 50
7: 0	R/W	0d25	reg_pk_cirbpcon2gain6:rate1 (for bpcon > th1) of curve to map bpcon to bpgain for circle bp filter (all 8 direction same). 0~255.. unsigned , default = 25

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Table 9-1621 SRSHARP0_PK_CON_2CIRBPGAIN_LIMIT 0x5008

Bit(s)	R/W	Default	Description
31:24	R/W	0d40	reg_pk_cirbpcon2gain2:level limit(for bpcon < th0) of curve to map bpcon to bpgain for circle bp filter (all 8 direction same). 0~255.. unsigned , default = 40
23:16	R/W	0d40	reg_pk_cirbpcon2gain3:level limit(for th0 < bpcon < th1) of curve to map bpcon to bpgain for circle bp filter (all 8 direction same). 0~255.. unsigned , default = 40
15: 8	R/W	0d5	reg_pk_cirbpcon2gain4:level limit(for bpcon > th1) of curve to map bpcon to bpgain for circle bp filter (all 8 direction same). 0~255.. unsigned , default = 5

Table 9-1622 SRSHARP0_PK_CON_2DRTHPGAIN_TH_RATE 0x5009

Bit(s)	R/W	Default	Description
31:24	R/W	0d25	reg_pk_drthpcon2gain0:threshold0 of curve to map hpcon to hpgain for directional hp filter (best direction). 0~255.. unsigned , default = 25
23:16	R/W	0d60	reg_pk_drthpcon2gain1:threshold1 of curve to map hpcon to hpgain for directional hp filter (best direction). 0~255.. unsigned , default = 60
15: 8	R/W	0d80	reg_pk_drthpcon2gain5:rate0 (for hpcon < th0) of curve to map hpcon to hpgain for directional hp filter (best direction). 0~255.. unsigned , default = 80
7: 0	R/W	0d20	reg_pk_drthpcon2gain6:rate1 (for hpcon > th1) of curve to map hpcon to hpgain for directional hp filter (best direction). 0~255.. unsigned , default = 20

Table 9-1623 SRSHARP0_PK_CON_2DRTHPGAIN_LIMIT 0x500a

Bit(s)	R/W	Default	Description
31:24	R/W	0d90	reg_pk_drthpcon2gain2:level limit(for hpcon < th0) of curve to map hpcon to hpgain for directional hp filter (best direction).. unsigned , default = 90
23:16	R/W	0d96	reg_pk_drthpcon2gain3:level limit(for th0 < hpcon < th1) of curve to map hpcon to hpgain for directional hp filter (best direction). 0~255.. unsigned , default = 96
15: 8	R/W	0d5	reg_pk_drthpcon2gain4:level limit(for hpcon > th1) of curve to map hpcon to hpgain for directional hp filter (best direction). 0~255.. unsigned , default = 5

Table 9-1624 SRSHARP0_PK_CON_2DRTBPGAIN_TH_RATE 0x500b

Bit(s)	R/W	Default	Description
31:24	R/W	0d20	reg_pk_drtbpcon2gain0:threshold0 of curve to map bpcon to bpgain for directional bp filter (best direction). 0~255.. unsigned , default = 20
23:16	R/W	0d50	reg_pk_drtbpcon2gain1:threshold1 of curve to map bpcon to bpgain for directional bp filter (best direction). 0~255.. unsigned , default = 50
15: 8	R/W	0d50	reg_pk_drtbpcon2gain5:rate0 (for bpcon < th0) of curve to map bpcon to bpgain for directional bp filter (best direction). 0~255.. unsigned , default = 50
7: 0	R/W	0d25	reg_pk_drtbpcon2gain6:rate1 (for bpcon > th1) of curve to map bpcon to bpgain for directional bp filter (best direction). 0~255.. unsigned , default = 25

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Table 9-1625 SRSHARP0_PK_CON_2DRTBPGAIN_LIMIT 0x500c

Bit(s)	R/W	Default	Description
31:24	R/W	0d40	reg_pk_drtbpcon2gain2:level limit(for bpcon < th0) of curve to map bpcon to bpgain for directional bp filter (best direction). 0~255.. unsigned , default = 40
23:16	R/W	0d40	reg_pk_drtbpcon2gain3:level limit(for th0 < bpcon < th1) of curve to map bpcon to bpgain for directional bp filter (best direction). 0~255.. unsigned , default = 40
15: 8	R/W	0d5	reg_pk_drtbpcon2gain4:level limit(for bpcon > th1) of curve to map bpcon to bpgain for directional bp filter (best direction). 0~255.. unsigned , default = 5

Table 9-1626 SRSHARP0_PK_CIRFB_LPF_MODE 0x500d

Bit(s)	R/W	Default	Description
29:28	R/W	0d1	reg_cirhp_horz_mode:no horz filter on HP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 . unsigned , default = 1
25:24	R/W	0d1	reg_cirhp_vert_mode:no vert filter on HP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 . unsigned , default = 1
21:20	R/W	0d1	reg_cirhp_diag_mode:filter on HP; 1: [1 2 1]/4; . unsigned , default = 1
13:12	R/W	0d1	reg_cirbp_horz_mode:no horz filter on BP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 . unsigned , default = 1
9: 8	R/W	0d1	reg_cirbp_vert_mode:no vert filter on BP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 . unsigned , default = 1
5: 4	R/W	0d1	reg_cirbp_diag_mode:filter on BP; 1: [1 2 1]/4; . unsigned , default = 1

Table 9-1627 SRSHARP0_PK_DRTFB_LPF_MODE 0x500e

Bit(s)	R/W	Default	Description
29:28	R/W	0d1	reg_drthp_horz_mode:no horz filter on HP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 2 . unsigned , default = 1
25:24	R/W	0d1	reg_drthp_vert_mode:no vert filter on HP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 2 . unsigned , default = 1
21:20	R/W	0d1	reg_drthp_diag_mode:filter on HP; 1: [1 2 1]/4; 1 . unsigned , default = 1
13:12	R/W	0d1	reg_drtbp_horz_mode:no horz filter on BP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 2 . unsigned , default = 1
9: 8	R/W	0d1	reg_drtbp_vert_mode:no vert filter on BP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 2 . unsigned , default = 1
5: 4	R/W	0d1	reg_drtbp_diag_mode:filter on BP; 1: [1 2 1]/4; 1 . unsigned , default = 1

Table 9-1628 SRSHARP0_PK_CIRFB_HP_CORING 0x500f

Bit(s)	R/W	Default	Description
21:16	R/W	0d4	reg_cirhp_horz_core:coring of HP for Horz . unsigned , default = 4
13: 8	R/W	0d4	reg_cirhp_vert_core:coring of HP for Vert . unsigned , default = 4
5: 0	R/W	0d4	reg_cirhp_diag_core:coring of HP for Diag . unsigned , default = 4

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Table 9-1629 SRSHARP0_PK_CIRFB_BP_CORING 0x5010

Bit(s)	R/W	Default	Description
21:16	R/W	0d4	reg_cirbp_horz_core:coring of HP for Horz . unsigned , default = 4
13: 8	R/W	0d4	reg_cirbp_vert_core:coring of HP for Vert . unsigned , default = 4
5: 0	R/W	0d4	reg_cirbp_diag_core:coring of HP for Diag . unsigned , default = 4

Table 9-1630 SRSHARP0_PK_DRTFB_HP_CORING 0x3e11

Bit(s)	R/W	Default	Description
21:16	R/W	0d4	reg_drthp_horz_core:coring of HP for Horz . unsigned , default = 4
13: 8	R/W	0d4	reg_drthp_vert_core:coring of HP for Vert . unsigned , default = 4
5: 0	R/W	0d4	reg_drthp_diag_core:coring of HP for Diag . unsigned , default = 4

Table 9-1631 SRSHARP0_PK_DRTFB_BP_CORING 0x5012

Bit(s)	R/W	Default	Description
21:16	R/W	0d4	reg_drtbp_horz_core:coring of HP for Horz . unsigned , default = 4
13: 8	R/W	0d4	reg_drtbp_vert_core:coring of HP for Vert . unsigned , default = 4
5: 0	R/W	0d4	reg_drtbp_diag_core:coring of HP for Diag . unsigned , default = 4

Table 9-1632 SRSHARP0_PK_CIRFB_BLEND_GAIN 0x5013

Bit(s)	R/W	Default	Description
31:28	R/W	0d8	reg_hp_cir_hgain:normalized 8 as '1' . unsigned , default = 8
27:24	R/W	0d8	reg_hp_cir_vgain:normalized 8 as '1' . unsigned , default = 8
23:20	R/W	0d8	reg_hp_cir_dgain:normalized 8 as '1' . unsigned , default = 8
15:12	R/W	0d8	reg_bp_cir_hgain:normalized 8 as '1' . unsigned , default = 8
11: 8	R/W	0d8	reg_bp_cir_vgain:normalized 8 as '1' . unsigned , default = 8
7: 4	R/W	0d8	reg_bp_cir_dgain:normalized 8 as '1' . unsigned , default = 8

Table 9-1633 SRSHARP0_NR_ALPY_SSD_GAIN_OFST 0x5014

Bit(s)	R/W	Default	Description
15: 8	R/W	0d16	reg_nr_alp0_ssd_gain:gain to max ssd normalized 16 as '1' . unsigned , default = 16
5: 0	R/W	0x0	reg_nr_alp0_ssd_ofst:offset to ssd before dividing to min_err . signed , default = -2

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Table 9-1634 SRSHARP0_NR_ALP0Y_ERR2CURV_TH_RATE 0x5015

Bit(s)	R/W	Default	Description
31:24	R/W	0d10	reg_nr_alp0_minerr_ypar0:threshold0 of curve to map mierr to alp0 for luma channel, this will be set value of flat region mierr that no need blur. 0~255.. unsigned , default = 10
23:16	R/W	0d25	reg_nr_alp0_minerr_ypar1:threshold1 of curve to map mierr to alp0 for luma channel,this will be set value of texture region mierr that can not blur.. unsigned , default = 25
15: 8	R/W	0d80	reg_nr_alp0_minerr_ypar5:rate0 (for mierr < th0) of curve to map mierr to alp0 for luma channel. the larger of the value, the deep of the slope. 0~255.. unsigned , default = 80
7: 0	R/W	0d64	reg_nr_alp0_minerr_ypar6:rate1 (for mierr > th1) of curve to map mierr to alp0 for luma channel. the larger of the value, the deep of the slope. 0~255.. unsigned , default = 64

Table 9-1635 SRSHARP0_NR_ALP0Y_ERR2CURV_LIMIT 0x5016

Bit(s)	R/W	Default	Description
31:24	R/W	0d63	reg_nr_alp0_minerr_ypar2:level limit(for mierr < th0) of curve to map mierr to alp0 for luma channel, this will be set to alp0 that we can do for flat region. 0~255.. unsigned , default = 63
23:16	R/W	0d0	reg_nr_alp0_minerr_ypar3:level limit(for th0 < mierr < th1) of curve to map mierr to alp0 for luma channel, this will be set to alp0 that we can do for misc region. 0~255.. unsigned , default = 0
15: 8	R/W	0d63	reg_nr_alp0_minerr_ypar4:level limit(for mierr > th1) of curve to map mierr to alp0 for luma channel, this will be set to alp0 that we can do for texture region. 0~255.. unsigned , default = 63

Table 9-1636 SRSHARP0_NR_ALP0C_ERR2CURV_TH_RATE 0x5017

Bit(s)	R/W	Default	Description
31:24	R/W	0d10	reg_nr_alp0_minerr_cpar0:threshold0 of curve to map mierr to alp0 for chroma channel, this will be set value of flat region mierr that no need blur.. unsigned , default = 10
23:16	R/W	0d25	reg_nr_alp0_minerr_cpar1:threshold1 of curve to map mierr to alp0 for chroma channel,this will be set value of texture region mierr that can not blur.. unsigned , default = 25
15: 8	R/W	0d80	reg_nr_alp0_minerr_cpar5:rate0 (for mierr < th0) of curve to map mierr to alp0 for chroma channel. the larger of the value, the deep of the slope. 0~255.. unsigned , default = 80
7: 0	R/W	0d64	reg_nr_alp0_minerr_cpar6:rate1 (for mierr > th1) of curve to map mierr to alp0 for chroma channel. the larger of the value, the deep of the slope. 0~255.. unsigned , default = 64

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Table 9-1637 SRSHARP0_NR_ALP0C_ERR2CURV_LIMIT 0x5018

Bit(s)	R/W	Default	Description
31:24	R/W	0d63	reg_nr_alp0_minerr_cpar2:level limit(for mierr < th0) of curve to map mierr to alp0 for chroma channel, this will be set to alp0 that we can do for flat region. 0~255.. unsigned , default = 63
23:16	R/W	0d0	reg_nr_alp0_minerr_cpar3:level limit(for th0 < mierr < th1) of curve to map mierr to alp0 for chroma channel, this will be set to alp0 that we can do for misc region. 0~255.. unsigned , default = 0
15: 8	R/W	0d63	reg_nr_alp0_minerr_cpar4:level limit(for mierr > th1) of curve to map mierr to alp0 for chroma channel, this will be set to alp0 that we can do for texture region. 0~255.. unsigned , default = 63

Table 9-1638 SRSHARP0_NR_ALP0_MIN_MAX 0x5019

Bit(s)	R/W	Default	Description
29:24	R/W	0d2	reg_nr_alp0_ymin:normalized to 64 as '1' . unsigned , default = 2
21:16	R/W	0d63	reg_nr_alp0_ymax:normalized to 64 as '1' . unsigned , default = 63
13: 8	R/W	0d2	reg_nr_alp0_cmin:normalized to 64 as '1' . unsigned , default = 2
5: 0	R/W	0d63	reg_nr_alp0_cmax:normalized to 64 as '1' . unsigned , default = 63

Table 9-1639 SRSHARP0_NR_ALP1_MIERR_CORING 0x501a

Bit(s)	R/W	Default	Description
16	R/W	0d0	reg_nr_alp1_maxerr_mode:0 max err; 1: xerr . unsigned , default = 0
13: 8	R/W	0d0	reg_nr_alp1_core_rate:normalized 64 as "1" . unsigned , default = 0
5: 0	R/W	0d3	reg_nr_alp1_core_ofst:normalized 64 as "1" . signed , default = 3

Table 9-1640 SRSHARP0_NR_ALP1_ERR2CURV_TH_RATE 0x501b

Bit(s)	R/W	Default	Description
31:24	R/W	0d0	reg_nr_alp1_minerr_par0:threshold0 of curve to map mierr to alp1 for luma/chroma channel, this will be set value of flat region mierr that no need directional NR. 0~255.. unsigned , default = 0
23:16	R/W	0d24	reg_nr_alp1_minerr_par1:threshold1 of curve to map mierr to alp1 for luma/chroma channel,this will be set value of texture region mierr that can not do directional NR. 0~255.. unsigned , default = 24
15: 8	R/W	0d0	reg_nr_alp1_minerr_par5:rate0 (for mierr < th0) of curve to map mierr to alp1 for luma/chroma channel. the larger of the value, the deep of the slope.. unsigned , default = 0
7: 0	R/W	0d20	reg_nr_alp1_minerr_par6:rate1 (for mierr > th1) of curve to map mierr to alp1 for luma/chroma channel. the larger of the value, the deep of the slope. 0~255. unsigned , default = 20

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Table 9-1641 SRSHARP0_NR_ALP1_ERR2CURV_LIMIT 0x501c

Bit(s)	R/W	Default	Description
31:24	R/W	0d0	reg_nr_alp1_minerr_par2:level limit(for mierr < th0) of curve to map mierr to alp1 for luma/chroma channel, this will be set to alp1 that we can do for flat region. 0~255.. unsigned , default = 0
23:16	R/W	0d16	reg_nr_alp1_minerr_par3:level limit(for th0 < mierr < th1) of curve to map mierr to alp1 for luma/chroma channel, this will be set to alp1 that we can do for misc region. 0~255.. unsigned , default = 16
15: 8	R/W	0d63	reg_nr_alp1_minerr_par4:level limit(for mierr > th1) of curve to map mierr to alp1 for luma/chroma channel, this will be set to alp1 that we can do for texture region. 0~255.255 before. unsigned , default = 63

Table 9-1642 SRSHARP0_NR_ALP1_MIN_MAX 0x501d

Bit(s)	R/W	Default	Description
29:24	R/W	0d0	reg_nr_alp1_ymin:normalized to 64 as '1' . unsigned , default = 0
21:16	R/W	0d63	reg_nr_alp1_ymax:normalized to 64 as '1' . unsigned , default = 63
13: 8	R/W	0d0	reg_nr_alp1_cmin:normalized to 64 as '1' . unsigned , default = 0
5: 0	R/W	0d63	reg_nr_alp1_cmax:normalized to 64 as '1' . unsigned , default = 63

Table 9-1643 SRSHARP0_PK_ALP2_MIERR_CORING 0x501e

Bit(s)	R/W	Default	Description
16	R/W	0d1	reg_pk_alp2_maxerr_mode:0 max err; 1: xerr . unsigned , default = 1
13: 8	R/W	0d13	reg_pk_alp2_core_rate:normalized 64 as "1" . unsigned , default = 13
5: 0	R/W	0d1	reg_pk_alp2_core_ofst:normalized 64 as "1" . signed , default = 1

Table 9-1644 SRSHARP0_PK_ALP2_ERR2CURV_TH_RATE 0x501f

Bit(s)	R/W	Default	Description
31:24	R/W	0d0	reg_pk_alp2_minerr_par0:threshold0 of curve to map mierr to alp2 for luma channel, this will be set value of flat region mierr that no need peaking.. unsigned , default = 0
23:16	R/W	0d24	reg_pk_alp2_minerr_par1:threshold1 of curve to map mierr to alp2 for luma channel,this will be set value of texture region mierr that can not do peaking. 0~255.. unsigned , default = 24
15: 8	R/W	0d0	reg_pk_alp2_minerr_par5:rate0 (for mierr < th0) of curve to map mierr to alp2 for luma channel. the larger of the value, the deep of the slope. 0~255.. unsigned , default = 0
7: 0	R/W	0d20	reg_pk_alp2_minerr_par6:rate1 (for mierr > th1) of curve to map mierr to alp2 for luma channel. the larger of the value, the deep of the slope. 0~255.. unsigned , default = 20

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Table 9-1645 SRSHARP0_PK_ALP2_ERR2CURV_LIMIT 0x5020

Bit(s)	R/W	Default	Description
31:24	R/W	0d0	reg_pk_alp2_minerr_par2:level limit(for mierr < th0) of curve to map mierr to alp2 for luma channel, this will be set to alp2 that we can do for flat region. 0~255.. unsigned , default = 0
23:16	R/W	0d16	reg_pk_alp2_minerr_par3:level limit(for th0 < mierr < th1) of curve to map mierr to alp2 for luma channel, this will be set to alp2 that we can do for misc region. 0~255.. unsigned , default = 16
15: 8	R/W	0d63	reg_pk_alp2_minerr_par4:level limit(for mierr > th1) of curve to map mierr to alp2 for luma channel, this will be set to alp2 that we can do for texture region. 0~255. default = 63;. unsigned , default = 255

Table 9-1646 SRSHARP0_PK_ALP2_MIN_MAX 0x5021

Bit(s)	R/W	Default	Description
13: 8	R/W	0d0	reg_pk_alp2_min:normalized to 64 as '1' . unsigned , default = 0
5: 0	R/W	0d63	reg_pk_alp2_max:normalized to 64 as '1' . unsigned , default = 63

Table 9-1647 SRSHARP0_PK_FINALGAIN_HP_BP 0x5022

Bit(s)	R/W	Default	Description
17: 16	R/W	0d0	reg_final_gain_rs:right shift bits for the gain normalization, 0 normal to 32 as 1; 1 normal to 64 as 1; -2 normal to 8 as 1; -1 normal to 16 as 1 . signed , default = 0
15: 8	R/W	0d40	reg_hp_final_gain:gain to highpass boost result (including directional/circle blending), normalized 32 as '1', 0~255. 1.25 * 32. unsigned , default = 40
7: 0	R/W	0d30	reg_bp_final_gain:gain to bandpass boost result (including directional/circle blending), normalized 32 as '1', 0~255. 1.25 * 32. unsigned , default = 30

Table 9-1648 SRSHARP0_PK_OS_HORZ_CORE_GAIN 0x5023

Bit(s)	R/W	Default	Description
31:24	R/W	0d8	reg_pk_os_hsidecore:side coring (not to current pixel) to adaptive overshoot margin in horizontal direction. the larger of this value, the less overshoot admitted 0~255;. unsigned , default = 8
15: 8	R/W	0d2	reg_pk_os_hmidcore:midd coring (to current pixel) to adaptive overshoot margin in horizontal direction. the larger of this value, the less overshoot admitted 0~255;. unsigned , default = 2
7: 0	R/W	0d20	reg_pk_os_hmidgain:midd gain (to current pixel) to adaptive overshoot margin in horizontal direction. normalized to 32 as '1'. 0~255;. unsigned , default = 20

Table 9-1649 SRSHARP0_PK_OS_VERT_CORE_GAIN 0x5024

Bit(s)	R/W	Default	Description
31:24	R/W	0d8	reg_pk_os_vsidecore:side coring (not to current pixel) to adaptive overshoot margin in vertical direction. the larger of this value, the less overshoot admitted 0~255;. unsigned , default = 8
23:16	R/W	0d20	reg_pk_os_vsidegain:side gain (not to current pixel) to adaptive overshoot margin in vertical direction. normalized to 32 as '1'. 0~255;. unsigned , default = 20

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Bit(s)	R/W	Default	Description
15: 8	R/W	0d2	reg_pk_os_vmidcore:midd coring (to current pixel) to adaptive overshoot margin in vertical direction. the larger of this value, the less overshoot admitted 0~255;. unsigned , default = 2
7: 0	R/W	0d20	reg_pk_os_vmidgain:midd gain (to current pixel) to adaptive overshoot margin in vertical direction. normalized to 32 as '1'. 0~255;. unsigned , default = 20

Table 9-1650 SRSHARP0_PK_OS_ADPT_MISC 0x5025

Bit(s)	R/W	Default	Description
31:24	R/W	0d40	reg_pk_os_minerr_core:coring to minerr for adaptive overshoot margin. the larger of this value, the less overshoot admitted 0~255;. unsigned , default = 40
23:16	R/W	0d6	reg_pk_os_minerr_gain:gain to minerr based adaptive overshoot margin. normalized to 64 as '1'. 0~255;. unsigned , default = 6
15: 8	R/W	0d200	reg_pk_os_adpt_max:maximum limit adaptive overshoot margin (4x). 0~255; . unsigned , default = 200
7: 0	R/W	0d20	reg_pk_os_adpt_min:minimun limit adaptive overshoot margin (1x). 0~255; . unsigned , default = 20

Table 9-1651 SRSHARP0_PK_OS_STATIC 0x5026

Bit(s)	R/W	Default	Description
29:28	R/W	0d2	reg_pk_osh_mode:0~3: (2x+1) window in H direction . unsigned , default = 2
25:24	R/W	0d2	reg_pk_osv_mode:0~3: (2x+1) window in V direction . unsigned , default = 2
21:12	R/W	0d200	reg_pk_os_down:static negative overshoot margin. 0~1023; . unsigned , default = 200
9: 0	R/W	0d200	reg_pk_os_up:static positive overshoot margin. 0~1023; . unsigned , default = 200

Table 9-1652 SRSHARP0_PK_NR_ENABLE 0x5027

Bit(s)	R/W	Default	Description
3: 2	R/W	0d0	reg_3d_mode : , 0: no 3D; 1: L/R; 2: T/B; 3: horizontal interleaved, dft = 0 //. unsigned , default = 0
1	R/W	0d1	reg_pk_en : . unsigned , default = 1
0	R/W	0d1	reg_nr_en : . unsigned , default = 1

Table 9-1653 SRSHARP0_PK_DRT_SAD_MISC 0x5028

Bit(s)	R/W	Default	Description
31:24	R/W	0d24	reg_pk_sad_ver_gain:gain to sad[4], 16 normalized to "1"; . unsigned , default = 24
23:16	R/W	0d24	reg_pk_sad_hor_gain:gain to sad[0], 16 normalized to "1"; . unsigned , default = 24

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Bit(s)	R/W	Default	Description
10: 9	R/W	0d0	reg_pk_bias_diag:bias towards diag . unsigned , default = 0
4: 0	R/W	0d24	reg_pk_drt_force:force direction of drt peaking filter, h2b: 0:hp drt force, 1: bp drt force; 2: bp+hp drt force, 3: no force;. unsigned , default = 24

Table 9-1654 SRSHARP0_NR_TI_DNLP_BLEND 0x5029

Bit(s)	R/W	Default	Description
10: 8	R/W	0d4	reg_dnlp_input_mode:dnlp input options. 0: org_y; 1: gau_y; 2: gauadp_y; 3: edgadplpf_y; 4: nr_y;5: lti_y; 6: pk_y (before os);7: pk_y (after os). unsigned , default = 4
3: 2	R/W	0d1	reg_nr_cti_blend_mode:blend mode of nr and lti result: 0: nr; 1:cti; 2: (nr+cti)/2; 3:cti + dlt_nr . unsigned , default = 1
1: 0	R/W	0d1	reg_nr_lti_blend_mode:blend mode of nr and lti result: 0: nr; 1:lti; 2: (nr+lti)/2; 3:lti + dlt_nr . unsigned , default = 1

Table 9-1655 SRSHARP0_TI_DIR_CORE_ALPHA 0x502a

Bit(s)	R/W	Default	Description
29:24	R/W	0d10	reg_adp_lti_dir_alp_core_ofst:ofst to min_err, alpha = (min_err - (max_err-min_err)*rate + ofst)/max_err*64; dft=10. unsigned , default = 10
19:16	R/W	0d0	reg_adp_lti_dir_alp_core_rate:ofset to min_err, alpha = (min_err - (max_err-min_err)*rate + ofst)/max_err*64; dft=0/32. unsigned , default = 0
13: 8	R/W	0d0	reg_adp_lti_dir_alpmin:min value of alpha, alpha = (min_err+x +ofst)/max_err*64; dft=10 . unsigned , default = 0
5: 0	R/W	0d63	reg_adp_lti_dir_alpmax:max value of alpha, alpha = (min_err+x +ofst)/max_err*64; dft=63 . unsigned , default = 63

Table 9-1656 SRSHARP0_CTI_DIR_ALPHA 0x502b

Bit(s)	R/W	Default	Description
29:24	R/W	0d5	reg_adp_cti_dir_alp_core_ofst:ofst to min_err, alpha = (min_err - (max_err-min_err)*rate + ofst)/max_err*64; dft=10. unsigned , default = 5
19:16	R/W	0d0	reg_adp_cti_dir_alp_core_rate:ofset to min_err, alpha = (min_err - (max_err-min_err)*rate + ofst)/max_err*64; dft=0/32. unsigned , default = 0
13: 8	R/W	0d0	reg_adp_cti_dir_alpmin:min value of alpha, alpha = (min_err +x+ofst)/max_err*64; dft=10 . unsigned , default = 0
5: 0	R/W	0d63	reg_adp_cti_dir_alpmax:max value of alpha, alpha = (min_err +x+ofst)/max_err*64; dft=63 . unsigned , default = 63

Table 9-1657 SRSHARP0_LTI_CTI_DF_GAIN 0x502c

Bit(s)	R/W	Default	Description
29:24	R/W	0d16	reg_adp_lti_hdf_gain:8 normalized to "1"; default = 16 . unsigned , default = 16
21:16	R/W	0d12	reg_adp_lti_vdf_gain:8 normalized to "1"; default = 12 . unsigned , default = 12

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Bit(s)	R/W	Default	Description
13: 8	R/W	0d16	reg_adp_cti_hdf_gain:8 normalized to "1"; default = 16 . unsigned , default = 16
5: 0	R/W	0d12	reg_adp_cti_vdf_gain:8 normalized to "1"; default = 12 . unsigned , default = 12

Table 9-1658 SRSHARP0_LTI_CTI_DIR_AC_DBG 0x502d

Bit(s)	R/W	Default	Description
30	R/W	0d1	reg_adp_lti_dir_lpf:0: no lpf; 1: [1 2 2 2 1]/8 lpf . unsigned , default = 1
28	R/W	0d0	reg_adp_lti_dir_difmode:0: y_dif; 1: y_dif + (u_dif+v_dif)/2; . unsigned , default = 0
26	R/W	0d1	reg_adp_cti_dir_lpf:0: no lpf; 1: [1 2 2 2 1]/8 lpf dft=1 . unsigned , default = 1
25:24	R/W	0d0	reg_adp_cti_dir_difmode:0: (u_dif+v_dif); 1: y_dif/2 + (u_dif+v_dif)*3/4; 2: y_dif + (u_dif+v_dif)/2; 3: y_dif*2 (not recomended). unsigned , default = 0
23:22	R/W	0d3	reg_adp_hvlti_dcblend_mode:0: hlti_dc; 1:vlti_dc; 2: avg 3; blend on alpha . unsigned , default = 3
21:20	R/W	0d3	reg_adp_hvcti_dcblend_mode:0: hcti_dc; 1:vcti_dc; 2: avg 3; blend on alpha . unsigned , default = 3
19:18	R/W	0d3	reg_adp_hvlti_acblend_mode:hlti_ac; 1:vlti_ac; 2: add 3;:adaptive to alpha . unsigned , default = 3
17:16	R/W	0d3	reg_adp_hvcti_acblend_mode:hcti_ac; 1:vcti_ac; 2: add 3;: adaptive to alpha . unsigned , default = 3
14:12	R/W	0d0	reg_adp_hlti_debug : , for hlti debug, default = 0 . unsigned , default = 0
10: 8	R/W	0d0	reg_adp_vlti_debug : , for vlti debug, default = 0 . unsigned , default = 0
6: 4	R/W	0d0	reg_adp_hcti_debug : , for hcti debug, default = 0 . unsigned , default = 0
2: 0	R/W	0d0	reg_adp_vcti_debug : , for vcti debug, default = 0 . unsigned , default = 0

Table 9-1659 SRSHARP0_HCTI_FLT_CLP_DC 0x502e

Bit(s)	R/W	Default	Description
28	R/W	0d1	reg_adp_hcti_en : , 0: no cti, 1: new cti, default = 1 . unsigned , default = 1
27:26	R/W	0d3	reg_adp_hcti_vdn_flt : , 0: no lpf; 1:[0,2,4,2,0], 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
25:24	R/W	0d2	reg_adp_hcti_hdn_flt : , 0: no lpf; 1:[0, 0, 0, 4, 8, 4, 0, 0, 0], 2:[0, 0, 2, 4, 4, 4, 2, 0, 0], 3: [1, 2, 2, 2, 2, 2, 2, 2, 1], default = 2. unsigned , default = 2
23:22	R/W	0d3	reg_adp_hcti_ddn_flt : , 0: no lpf; 1:[0,2,4,2,0], 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
21:20	R/W	0d2	reg_adp_hcti_lpf0_flt : , 0:no filter; 1:sigma=0.75, 2: sigma = 1.0, 3: sigma = 1.5, default = 2 . unsigned , default = 2
19:18	R/W	0d2	reg_adp_hcti_lpf1_flt : , 0:no filter; 1:sigma= 2.0, 2: sigma = 3.0, 3: sigma = 4.0, default = 2 . unsigned , default = 2
17:16	R/W	0d2	reg_adp_hcti_lpf2_flt : , 0:no filter; 1:sigma=5.0, 2: sigma = 9.0, 3: sigma = 13.0, default = 2 . unsigned , default = 2
15:12	R/W	0d7	reg_adp_hcti_hard_clp_win : , window size, 0~8, default = 7 . unsigned , default = 7

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Bit(s)	R/W	Default	Description
11: 8	R/W	0d3	reg_adp_hcti_hard_win_min : , window size, 0~8, default = 3 . unsigned , default = 3
4	R/W	0d1	reg_adp_hcti_clp_mode : , 0: hard clip, 1: adaptive clip, default = 1 . unsigned , default = 1
2: 0	R/W	0d0	reg_adp_hcti_dc_mode : , 0:dn, 1:lpf0, 2:lpf1, 3:lpf2, 4: lpf3: 5: vdn result; 6/7: org, default = 0 . unsigned , default = 0

Table 9-1660 SRSHARP0_HCTI_BST_GAIN 0x502f

	R/W	Default	Description
31:24	R/W	0d80	reg_adp_hcti_bst_gain0:gain of the bandpass 0 (lpf1-lpf2)- LBP, default = 80 . unsigned , default = 80
23:16	R/W	0d96	reg_adp_hcti_bst_gain1:gain of the bandpass 1 (lpf0-lpf1)- BP, default = 96 . unsigned , default = 96
15: 8	R/W	0d64	reg_adp_hcti_bst_gain2:gain of the bandpass 2 (hdn-lpf0)- HP, default = 64 . unsigned , default = 64
7: 0	R/W	0d16	reg_adp_hcti_bst_gain3:gain of the unsharp band (yuvin-hdn) - US, default = 16 . unsigned , default = 16

Table 9-1661 SRSHARP0_HCTI_BST_CORE 0x5030

Bit(s)	R/W	Default	Description
31:24	R/W	0d0	reg_adp_hcti_bst_core0:core of the bandpass 0 (lpf1-lpf2)- LBP, default = 0 . unsigned , default = 0
23:16	R/W	0d0	reg_adp_hcti_bst_core1:core of the bandpass 1 (lpf0-lpf1)- BP, default = 0 . unsigned , default = 0
15: 8	R/W	0d0	reg_adp_hcti_bst_core2:core of the bandpass 2 (hdn-lpf0)- HP, default = 0 . unsigned , default = 0
7: 0	R/W	0d0	reg_adp_hcti_bst_core3:core of the unsharp band (yuvin-hdn) - US, default = 0 . unsigned , default = 0

Table 9-1662 SRSHARP0_HCTI_CON_2_GAIN_0 0x5031

Bit(s)	R/W	Default	Description
31:29	R/W	0d2	reg_adp_hcti_con_mode:con mode 0:[0, 0,-1, 1, 0, 0, 0]+[0, 0, 0, 1,-1, 0, 0], 1: [0, 0,-1, 0, 1, 0, 0], 2: [0,-1, 0, 0, 0, 1, 0], 3:[-1, 0, 0, 0, 0, 0, 1], 4: .... default = 2. unsigned , default = 2
28:26	R/W	0d3	reg_adp_hcti_dx_mode:dx mode 0: [-1 1 0]; 1~7: [-1 (2x+1)"0" 1], default = 3 . unsigned , default = 3
25:24	R/W	0d1	reg_adp_hcti_con_lpf:lpf mode of the con: 0: [1 2 1]/4; 1:[1 2 2 2 1]/8, default = 1 . unsigned , default = 1
23:16	R/W	0d25	reg_adp_hcti_con_2_gain0 : , default = 25 . unsigned , default = 25
15: 8	R/W	0d60	reg_adp_hcti_con_2_gain1 : , default = 60 . unsigned , default = 60
7: 0	R/W	0d0	reg_adp_hcti_con_2_gain2 : 0;, default = 0 . unsigned , default = 0

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Table 9-1663 SRSHARP0_HCTI_CON_2_GAIN_1 0x5032

Bit(s)	R/W	Default	Description
31:24	R/W	0d96	reg_adp_hcti_con_2_gain3 : 96;, default = 96 . unsigned , default = 96
23:16	R/W	0d5	reg_adp_hcti_con_2_gain4 : 5;, default = 5 . unsigned , default = 5
15: 8	R/W	0d80	reg_adp_hcti_con_2_gain5 : 80;, default = 80 . unsigned , default = 80
7: 0	R/W	0d20	reg_adp_hcti_con_2_gain6 : 20;, default = 20 . unsigned , default = 20

Table 9-1664 SRSHARP0_HCTI_OS_MARGIN 0x5033

Bit(s)	R/W	Default	Description
7: 0	R/W	0d0	reg_adp_hcti_os_margin:margin for hcti overshoot, default = 0 . unsigned , default = 0

Table 9-1665 SRSHARP0_HLTI_FLT_CLP_DC 0x5034

Bit(s)	R/W	Default	Description
28	R/W	0d1	reg_adp_hlti_en : , 0: no cti, 1: new cti, default = 1 . unsigned , default = 1
27:26	R/W	0d2	reg_adp_hlti_vdn_flt : , 0: no lpf; 1:[0,2,4,2,0], 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 2 . unsigned , default = 2
25:24	R/W	0d2	reg_adp_hlti_hdn_flt : , 0: no lpf; 1:[0, 0, 0, 4, 8, 4, 0, 0, 0], 2:[0, 0, 2, 4, 4, 4, 2, 0, 0], 3: [1, 2, 2, 2, 2, 2, 2, 2, 1], default = 2. unsigned , default = 2
23:22	R/W	0d2	reg_adp_hlti_ddn_flt : , 0: no lpf; 1:[0,2,4,2,0], 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 2 . unsigned , default = 2
21:20	R/W	0d2	reg_adp_hlti_lpf0_flt : , 0:no filter; 1:sigma=0.75, 2: sigma = 1.0, 3: sigma = 1.5, default = 2 . unsigned , default = 2
19:18	R/W	0d2	reg_adp_hlti_lpf1_flt : , 0:no filter; 1:sigma= 2.0, 2: sigma = 3.0, 3: sigma = 4.0, default = 2 . unsigned , default = 2
17:16	R/W	0d2	reg_adp_hlti_lpf2_flt : , 0:no filter; 1:sigma=5.0, 2: sigma = 9.0, 3: sigma = 13.0, default = 2 . unsigned , default = 2
15:12	R/W	0d2	reg_adp_hlti_hard_clp_win : , window size, 0~8, default = 2 . unsigned , default = 2
11: 8	R/W	0d1	reg_adp_hlti_hard_win_min : , window size, 0~8, default = 1 . unsigned , default = 1
4	R/W	0d0	reg_adp_hlti_clp_mode : , 0: hard clip, 1: adaptive clip, default = 0 . unsigned , default = 0
2: 0	R/W	0d4	reg_adp_hlti_dc_mode : , 0:dn, 1:lpf0, 2:lpf1, 3:lpf2, 4: lpf3: 5: vdn result; 6/7:org, default = 4 . unsigned , default = 4

Table 9-1666 SRSHARP0_HLTI_BST_GAIN 0x5035

Bit(s)	R/W	Default	Description
31:24	R/W	0d40	reg_adp_hlti_bst_gain0:gain of the bandpass 0 (lpf1-lpf2)- LBP, default = 40 . unsigned , default = 40
23:16	R/W	0d48	reg_adp_hlti_bst_gain1:gain of the bandpass 1 (lpf0-lpf1)- BP, default = 48 . unsigned , default = 48

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Bit(s)	R/W	Default	Description
15: 8	R/W	0d32	reg_adp_hlti_bst_gain2:gain of the bandpass 2 (hdn-lpf0)- HP, default = 32 . unsigned , default = 32
7: 0	R/W	0d16	reg_adp_hlti_bst_gain3:gain of the unsharp band (yuvin-hdn) - US, default = 16 . unsigned , default = 16

Table 9-1667 SRSHARP0_HLTI_BST_CORE 0x5036

Bit(s)	R/W	Default	Description
31:24	R/W	0d5	reg_adp_hlti_bst_core0:core of the bandpass 0 (lpf1-lpf2)- LBP, default = 5 . unsigned , default = 5
23:16	R/W	0d5	reg_adp_hlti_bst_core1:core of the bandpass 1 (lpf0-lpf1)- BP, default = 5 . unsigned , default = 5
15: 8	R/W	0d5	reg_adp_hlti_bst_core2:core of the bandpass 2 (hdn-lpf0)- HP, default = 5 . unsigned , default = 5
7: 0	R/W	0d3	reg_adp_hlti_bst_core3:core of the unsharp band (yuvin-hdn) - US, default = 3 . unsigned , default = 3

Table 9-1668 SRSHARP0_HLTI_CON_2_GAIN_0 0x5037

Bit(s)	R/W	Default	Description
31:29	R/W	0d2	reg_adp_hlti_con_mode:con mode 0:[0, 0,-1, 1, 0, 0, 0]+[0, 0, 0, 1,-1, 0, 0], 1: [0, 0,-1, 0, 1, 0, 0], 2: [0,-1, 0, 0, 0, 1, 0], 3:[-1, 0, 0, 0, 0, 0, 1], 4: ....., default = 2. unsigned , default = 2
28:26	R/W	0d3	reg_adp_hlti_dx_mode:dx mode 0: [-1 1 0]; 1~7: [-1 (2x+1)"0" 1], default = 3 . unsigned , default = 3
25:24	R/W	0d1	reg_adp_hlti_con_lpf:lpf mode of the con: 0: [1 2 1]/4; 1:[1 2 2 2 1]/8, default = 1 . unsigned , default = 1
23:16	R/W	0d25	reg_adp_hlti_con_2_gain0 : 25;, default = 25 . unsigned , default = 25
15: 8	R/W	0d60	reg_adp_hlti_con_2_gain1 : 60;, default = 60 . unsigned , default = 60
7: 0	R/W	0d90	reg_adp_hlti_con_2_gain2 : 0;, default = 90 . unsigned , default = 90

Table 9-1669 SRSHARP0_HLTI_CON_2_GAIN_1 0x5038

Bit(s)	R/W	Default	Description
31:24	R/W	0d96	reg_adp_hlti_con_2_gain3 : 96;, default = 96 . unsigned , default = 96
23:16	R/W	0d95	reg_adp_hlti_con_2_gain4 : 5;, default = 95 . unsigned , default = 95
15: 8	R/W	0d80	reg_adp_hlti_con_2_gain5 : 80;, default = 80 . unsigned , default = 80
7: 0	R/W	0d20	reg_adp_hlti_con_2_gain6 : 20;, default = 20 . unsigned , default = 20

Table 9-1670 SRSHARP0_HLTI_OS_MARGIN 0x5039

Bit(s)	R/W	Default	Description
7: 0	R/W	0d0	reg_adp_hlti_os_margin:margin for hlti overshoot, default = 0 . unsigned , default = 0

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Table 9-1671 SRSHARP0_VLTI_FLT_CON_CLP 0x503a

Bit(s)	R/W	Default	Description
14	R/W	0d1	reg_adp_vlti_en:enable bit of vlti, default = 1 . unsigned , default = 1
13:12	R/W	0d3	reg_adp_vlti_hxn_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
11:10	R/W	0d3	reg_adp_vlti_dxn_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
9: 8	R/W	0d3	reg_adp_vlti_han_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
7: 6	R/W	0d3	reg_adp_vlti_dan_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
5: 4	R/W	0d2	reg_adp_vlti_dx_mode:0:[-1 1] 1:[-1 0 -1]; 2/3: [-1 0 0 0 -1], default = 2 . unsigned , default = 2
2	R/W	0d1	reg_adp_vlti_con_lpf:lpf mode of the con: 0: [1 2 1]/4; 1:[1 2 2 2 1]/8, default = 1 . unsigned , default = 1
0	R/W	0d1	reg_adp_vlti_hard_clp_win:window size; 0: 1x3 window; 1: 1x5 window, default = 1 . unsigned , default = 1

Table 9-1672 SRSHARP0_VLTI_BST_GAIN 0x503b

Bit(s)	R/W	Default	Description
23:16	R/W	0d32	reg_adp_vlti_bst_gain0:gain to boost filter [-1 2 -1];, default = 32 . unsigned , default = 32
15: 8	R/W	0d32	reg_adp_vlti_bst_gain1:gain to boost filter [-1 0 2 0 -1];, default = 32 . unsigned , default = 32
7: 0	R/W	0d32	reg_adp_vlti_bst_gain2:gain to boost filter usf, default = 32 . unsigned , default = 32

Table 9-1673 SRSHARP0_VLTI_BST_CORE 0x503c

Bit(s)	R/W	Default	Description
23:16	R/W	0d5	reg_adp_vlti_bst_core0:coring to boost filter [-1 2 -1];, default = 5 . unsigned , default = 5
15: 8	R/W	0d5	reg_adp_vlti_bst_core1:coring to boost filter [-1 0 2 0 -1];, default = 5 . unsigned , default = 5
7: 0	R/W	0d3	reg_adp_vlti_bst_core2:coring to boost filter usf, default = 3 . unsigned , default = 3

Table 9-1674 SRSHARP0_VLTI_CON_2_GAIN_0 0x503d

Bit(s)	R/W	Default	Description
31:24	R/W	0d25	reg_adp_vlti_con_2_gain0 : 25;, default = 25 . unsigned , default = 25
23:16	R/W	0d69	reg_adp_vlti_con_2_gain1 : 60;, default = 69 . unsigned , default = 60
15: 8	R/W	0d90	reg_adp_vlti_con_2_gain2 : 0;, default = 90 . unsigned , default = 90
7: 0	R/W	0d96	reg_adp_vlti_con_2_gain3 : 96;, default = 96 . unsigned , default = 96

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Table 9-1675 SRSHARP0_VLTI_CON_2_GAIN_1 0x503e

Bit(s)	R/W	Default	Description
31:24	R/W	0d95	reg_adp_vlti_con_2_gain4 : 5;, default = 95 . unsigned , default = 95
23:16	R/W	0d80	reg_adp_vlti_con_2_gain5 : 80;, default = 80 . unsigned , default = 80
15: 8	R/W	0d20	reg_adp_vlti_con_2_gain6 : 20;, default = 20 . unsigned , default = 20
7: 0	R/W	0d0	reg_adp_vlti_os_margin:margin for vlti overshoot, default = 0 . unsigned , default = 0

Table 9-1676 SRSHARP0_VCTI_FLT_CON_CLP 0x503f

Bit(s)	R/W	Default	Description
14	R/W	0d1	reg_adp_vcti_en:enable bit of vlti, default = 1 . unsigned , default = 1
13:12	R/W	0d3	reg_adp_vcti_hxn_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
11:10	R/W	0d3	reg_adp_vcti_dxn_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
9: 8	R/W	0d3	reg_adp_vcti_han_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
7: 6	R/W	0d3	reg_adp_vcti_dan_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
5: 4	R/W	0d2	reg_adp_vcti_dx_mode:0:[-1 1] 1:[-1 0 -1]; 2/3: [-1 0 0 0 -1], default = 2 . unsigned , default = 2
2	R/W	0d1	reg_adp_vcti_con_lpf:lpf mode of the con: 0: [1 2 1]/4; 1:[1 2 2 2 1]/8, default = 1 . unsigned , default = 1
0	R/W	0d1	reg_adp_vcti_hard_clp_win:window size; 0: 1x3 window; 1: 1x5 window, default = 1 . unsigned , default = 1

Table 9-1677 SRSHARP0_VCTI_BST_GAIN 0x5040

Bit(s)	R/W	Default	Description
23:16	R/W	0d0	reg_adp_vcti_bst_gain0:gain to boost filter [-1 2 -1];, default = 0 . unsigned , default = 0
15: 8	R/W	0d0	reg_adp_vcti_bst_gain1:gain to boost filter [-1 0 2 0 -1];, default = 0 . unsigned , default = 0
7: 0	R/W	0d0	reg_adp_vcti_bst_gain2:gain to boost filter usf, default = 0 . unsigned , default = 0

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Table 9-1678 SRSHARP0_VCTI_BST_CORE 0x5041

Bit(s)	R/W	Default	Description
23:16	R/W	0d0	reg_adp_vcti_bst_core0:coring to boost filter [-1 2 -1];, default = 0 . unsigned , default = 0
15: 8	R/W	0d0	reg_adp_vcti_bst_core1:coring to boost filter [-1 0 2 0 -1];, default = 0 . unsigned , default = 0
7: 0	R/W	0d0	reg_adp_vcti_bst_core2:coring to boost filter usf, default = 0 . unsigned , default = 0

Table 9-1679 SRSHARP0_VCTI_CON_2_GAIN_0 0x5042

Bit(s)	R/W	Default	Description
31:24	R/W	0d25	reg_adp_vcti_con_2_gain0 : 25;, default = 25 . unsigned , default = 25
23:16	R/W	0d60	reg_adp_vcti_con_2_gain1 : 60;, default = 60 . unsigned , default = 60
15: 8	R/W	0d90	reg_adp_vcti_con_2_gain2 : 0;, default = 90 . unsigned , default = 90
7: 0	R/W	0d96	reg_adp_vcti_con_2_gain3 : 96;, default = 96 . unsigned , default = 96

Table 9-1680 SRSHARP0_VCTI_CON_2_GAIN_1 0x5043

Bit(s)	R/W	Default	Description
31:24	R/W	0d95	reg_adp_vcti_con_2_gain4 : 5;, default = 95 . unsigned , default = 95
23:16	R/W	0d80	reg_adp_vcti_con_2_gain5 : 80;, default = 80 . unsigned , default = 80
15: 8	R/W	0d20	reg_adp_vcti_con_2_gain6 : 20;, default = 20 . unsigned , default = 20
7: 0	R/W	0d0	reg_adp_vcti_os_margin:margin for vcti overshoot, default = 0 . unsigned , default = 0

Table 9-1681 SRSHARP0_SHARP_3DLIMIT 0x5044

Bit(s)	R/W	Default	Description
28:16	R/W	0d0	reg_3d_mid_width : ,width of left part of 3d input, dft = half size of input width default = 0 . unsigned , default = 960
12: 0	R/W	0d0	reg_3d_mid_height : ,height of left part of 3d input, dft = half size of input height default = 0 . unsigned , default = 540

Table 9-1682 SRSHARP0_DNLP_EN 0x5045

Bit(s)	R/W	Default	Description
15□8	R/W	0d0	reg_dnlp_hblank: . unsigned , default = 8
0	R/W	0d1	reg_dnlp_en : . unsigned , default = 1

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Table 9-1683 SRSHARP0_DEMO_CRTL 0x5056

Bit(s)	R/W	Default	Description
18:17	R/W	0d2	demo_disp_position : . unsigned , default = 2
16	R/W	0d0	demo_hsvsharp_enable : . unsigned , default = 0
12: 0	R/W	0d360	demo_left_top_screen_width: . unsigned , default = 360

Table 9-1684 SRSHARP0_SHARP_SR2_CTRL 0x5057

Bit(s)	R/W	Default	Description
24	R/W	0	reg_sr2_bic_pknr_bypass : bypass peaking/TI/Cubic
23:22	R/W		reserved
21:16	R/W	24	sr2_pk_la_err_dis_rate, low angle and high angle error should not be no less than nearby_error* rate/64
15: 8	R/W	16	sr2_pk_sad_diag_gain, gain to sad[2] and sad[6], 16 normalized to 1
7	R/W	0	sr2_vert_outphs, vertical output pixel phase, 0: 0 phase; 1: 1/2 phase
6	R/W	0	sr2_horz_outphs, horizontal output pixel phase, 0: 0 phase; 1: 1/2 phase
5	R/W	0	sr2_vert_ratio , vertical scale ratio, 0- > 1:1; 1- > 1:2
4	R/W	0	sr2_horz_ratio , horizontal scale ratio, 0- > 1:1; 1- > 1:2
3	R/W	1	sr2_ bic_norm , normalization of bicubical: 0: 128; 1: 64
2	R/W	0	sr2_ enable , 1 to enable super scaler
1	R/W	0	sr2_ sharp_prc_lr_hbic,
0	R/W	0	sr2_ sharp_prc_lr, 1: LTI/CTI/NR/Peaking processing using LR grid. 0: on HR grid; 1:on LR grid, horizontally no upscale, but using simple bic.

Table 9-1685 SRSHARP0_SHARP_SR2_YBIC_HCOEF0 0x5058

Bit(s)	R/W	Default	Description
31:24	R/W	0	sr2_y_bic_hcoeff03, signed
23:16	R/W	0	sr2_y_bic_hcoeff02, signed
15: 8	R/W	64	sr2_y_bic_hcoeff01, signed
7: 0	R/W	0	sr2_y_bic_hcoeff00, signed

Table 9-1686 SRSHARP0_SHARP_SR2_YBIC_HCOEF1 0x5059

Bit(s)	R/W	Default	Description
31:24	R/W	-4	sr2_y_bic_hcoeff13 , signed
23:16	R/W	36	sr2_y_bic_hcoeff12 , signed
15: 8	R/W	36	sr2_y_bic_hcoeff11 , signed
7: 0	R/W	-4	sr2_y_bic_hcoeff10 , signed

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Table 9-1687 SRSHARP0_SHARP_SR2_CBIC_HCOEF0 0x505a

Bit(s)	R/W	Default	Description
31:24	R/W	0	sr2_c_bic_hcoeff03 , signed
23:16	R/W	21	sr2_c_bic_hcoeff02 , signed
15: 8	R/W	22	sr2_c_bic_hcoeff01 , signed
7: 0	R/W	21	sr2_c_bic_hcoeff00 , signed

Table 9-1688 SRSHARP0_SHARP_SR2_CBIC_HCOEF1 0x505b

Bit(s)	R/W	Default	Description
31:24	R/W	-4	sr2_c_bic_hcoeff13 , signed
23:16	R/W	36	sr2_c_bic_hcoeff12 , signed
15: 8	R/W	36	sr2_c_bic_hcoeff11 , signed
7: 0	R/W	-4	sr2_c_bic_hcoeff10 , signed

Table 9-1689 SRSHARP0_SHARP_SR2_YBIC_VCOEF0 0x505c

Bit(s)	R/W	Default	Description
31:24	R/W	0	sr2_y_bic_vcoeff03 , signed
23:16	R/W	0	sr2_y_bic_vcoeff02 , signed
15: 8	R/W	64	sr2_y_bic_vcoeff01 , signed
7: 0	R/W	0	sr2_y_bic_vcoeff00 , signed

Table 9-1690 SRSHARP0_SHARP_SR2_YBIC_VCOEF1 0x505d

Bit(s)	R/W	Default	Description
31:24	R/W	-4	sr2_y_bic_vcoeff13 , signed
23:16	R/W	36	sr2_y_bic_vcoeff12 , signed
15: 8	R/W	36	sr2_y_bic_vcoeff11 , signed
7: 0	R/W	-4	sr2_y_bic_vcoeff10 , signed

Table 9-1691 SRSHARP0_SHARP_SR2_CBIC_VCOEF0 0x505e

Bit(s)	R/W	Default	Description
31:24	R/W	0	sr2_c_bic_vcoeff03 , signed
23:16	R/W	21	sr2_c_bic_vcoeff02 , signed
15: 8	R/W	22	sr2_c_bic_vcoeff01 , signed
7: 0	R/W	21	sr2_c_bic_vcoeff00 , signed

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Table 9-1692 SRSHARP0_SHARP_SR2_CBIC_VCOEF1 0x505f

Bit(s)	R/W	Default	Description
31:24	R/W	-4	sr2_c_bic_vcoeff13 , signed
23:16	R/W	36	sr2_c_bic_vcoeff12 , signed
15: 8	R/W	36	sr2_c_bic_vcoeff11 , signed
7: 0	R/W	-4	sr2_c_bic_vcoeff10 , signed

Table 9-1693 SRSHARP0_SHARP_SR2_MISC 0x5060

Bit(s)	R/W	Default	Description
31:2	R/W		reserved
1	R/W	0	sr2_cmpmux_bef , 0 : no swap for YUV/RGB; 1: swap for YUV/RGB, YUV/RGB-> UVY/GBR
0	R/W	0	sr2_cmpmux_aft , 0 : no swap for YUV/RGB; 1: swap for YUV/RGB, UVY/GBR-> YUV/RGB

Table 9-1694 SRSHARP0_SR3_SAD_CTRL 0x5061

Bit(s)	R/W	Default	Description
31:30	R/W		reserved
29:24	R/W	0d6	reg_sr3_pk_sad_core_rate : rate of coring.
23:22	R/W		reserved
21:16	R/W	0d6	reg_sr3_lti_sad_core_rate : rate of coring.
15:14	R/W		reserved
13:8	R/W	0d6	reg_sr3_cti_sad_core_rate : rate of coring.
7	R/W	0d1	reg_sr3_lti_hsad_mode: mode for hsad of lti calculation, 0:block based; 1: other sharp
6	R/W	0d1	reg_sr3_cti_hsad_mode: mode for hsad of cti calculation, 0:block based; 1: other sharp
5	R/W	0d1	reg_sr3_lti_dsad_mode: mode for dsad of lti calculation, 0:block based; 1: other sharp
4	R/W	0d1	reg_sr3_cti_dsad_mode: mode for dsad of cti calculation, 0:block based; 1: other sharp
3	R/W	0d1	reg_sr3_lti_vsad_mode: mode for vsad of lti calculation, 0:block based; 1: other sharp
2	R/W	0d1	reg_sr3_cti_vsad_mode: mode for vsad of cti calculation, 0:block based; 1: other sharp
1	R/W	0d1	reg_sr3_lti_hsad_hlpf: hlpf for hsad of lti calculation, 0:no hlpf; 1: with [1 2 1] hlpf.
0	R/W	0d1	reg_sr3_cti_hsad_hlpf: hlpf for hsad of cti calculation, 0:no hlpf; 1: with [1 2 1] hlpf.

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Table 9-1695 SRSHARP0_SR3_PK_CTRL0 0x5062

Bit(s)	R/W	Default	Description
31:12	R/W		reserved
11	R/W	0d1	reg_sr3_pk_sad_mode: mode for sad of peaking calculation, 0: block based; 1: other sharp.
10	R/W	0d1	reg_sr3_pk_hsad_hlpf: hlpf for hsad for peaking calculation,0:no hlpf; 1: with [1 2 2 2 1] hlpf.
9	R/W	0d1	reg_sr3_pk_vsad_hlpf: hlpf for vsad for peaking calculation,0:no hlpf; 1: with [1 2 2 2 1] hlpf.
8	R/W	0d1	reg_sr3_pk_dsad_hlpf: hlpf for dsad for peaking calculation,0:no hlpf; 1: with [1 2 2 2 1] hlpf.
7:6	R/W	0d3	reg_sr3_pk_hpdrt_mode: mode for HPdrt filter
5:4	R/W	0d3	reg_sr3_pk_bpdrt_mode: mode for BPdrt filter
3:2	R/W	0d3	reg_pk_drtbld_range: range of the min2 and min direction distance
1	R/W		reserved
0	R/W	0d0	reg_sr3_pk_ti_blend_mode: blend mode of the TI and PK result

Table 9-1696 SRSHARP0_SR3_PK_CTRL1 0x5063

Bit(s)	R/W	Default	Description
31	R/W		reserved
30:28	R/W	0d1	reg_sr3_pk_Hp_hvcon_replace8_maxsad: replace HP hvcon by maxsad
26:24	R/W	0d1	reg_sr3_pk_bp_hvcon_replace8_maxsad: replace BP hvcon by maxsad
23:16	R/W	0d32	reg_sr3_pk_hp_hvcon_replace8lv_gain: gain to local variant before calculating the hv gain for peaking.
15:8	R/W	0d32	reg_sr3_pk_bp_hvcon_replace8lv_gain: gain to local variant before calculating the hv gain for peaking.
7	R/W	0d1	reg_sr3_sad_intlev_mode: interleave detect xerr mode: 0 max; 1: sum
6	R/W	0d1	reg_sr3_sad_intlev_mode1: mode 1 of using diagonal protection: 1: with diagonal protection
5:0	R/W	0d12	reg_sr3_sad_intlev_gain: interleave detection for sad gain applied, normalized to 8 as 1

Table 9-1697 SRSHARP0_DEJ_CTRL 0x5064

Bit(s)	R/W	Default	Description
15:8	R/W	8	reg_sr3_dejaggy_hblank
7:4	R/W		reserved
3:2	R/W	0d3	reg_sr3_dejaggy_sameside_prtct: enable of sr3 dejaggy same side curve protect from filter, [0] for proc path; [1] for ctrl path.
1	R/W	0d1	reg_sr3_dejaggy_sameside_mode: mode of sameside flag decision
0	R/W	0d1	reg_sr3_dejaggy_enable: enable of sr3 dejaggy

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Table 9-1698 SRSHARP0_DEJ_ALPHA 0x5065

Bit(s)	R/W	Default	Description
31:28	R/W	0d0	reg_sr3_dejaggy_ctrlchrm_alpha_1 : alpha for LR video LPF
27:24	R/W	0d15	reg_sr3_dejaggy_ctrlchrm_alpha_0 : alpha for LR video LPF
23:20	R/W	0d0	reg_sr3_dejaggy_ctrlluma_alpha_1 : alpha for LR video LPF
19:16	R/W	0d15	reg_sr3_dejaggy_ctrlluma_alpha_0 : alpha for LR video LPF
15:12	R/W	0d4	reg_sr3_dejaggy_procchrm_alpha_1: alpha for LR video LPF
11:8	R/W	0d6	reg_sr3_dejaggy_procchrm_alpha_0: alpha for LR video LPF
7:4	R/W	0d4	reg_sr3_dejaggy_procluma_alpha_1: alpha for LR video LPF
3:0	R/W	0d6	reg_sr3_dejaggy_procluma_alpha_0: alpha for LR video LPF

Table 9-1699 SRSHARP0_SR3_DRTLPF_EN 0x5066

Bit(s)	R/W	Default	Description
31:15	R/W		reserved
14:8	R/W	0d0	reg_pk_debug_edge
6:4	R/W	0d0	reg_sr3_drtlpf_theta_en
2:0	R/W	0d7	reg_sr3_drtlpf_enable: directional lpf on Y/U/V channels

Table 9-1700 SRSHARP0_SR3_DRTLPF_ALPHA_0 0x5067

Bit(s)	R/W	Default	Description
31:28	R/W		reserved
27:24	R/W	0d9	reg_sr3_drtlpf_alpha_3
23:20	R/W		reserved
19:16	R/W	0d10	reg_sr3_drtlpf_alpha_2
15:12	R/W		reserved
11:8	R/W	0d11	reg_sr3_drtlpf_alpha_1
7:4	R/W		reserved
3:0	R/W	0d12	reg_sr3_drtlpf_alpha_0: directional lpf alpha coef for min_sad/max_sad compare

Table 9-1701 SRSHARP0_SR3_DRTLPF_ALPHA_1 0x5068

Bit(s)	R/W	Default	Description
31:28	R/W		reserved
27:24	R/W	0d1	reg_sr3_drtlpf_alpha_7
23:20	R/W		reserved
19:16	R/W	0d4	reg_sr3_drtlpf_alpha_6
15:12	R/W		reserved

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Bit(s)	R/W	Default	Description
11:8	R/W	0d7	reg_sr3_drtlpf_alpha_5
7:4	R/W		reserved
3:0	R/W	0d8	reg_sr3_drtlpf_alpha_4: directional lpf alpha coef for min_sad/max_sad compare

Table 9-1702 SRSHARP0_SR3_DRTLPF_ALPHA_2 0x5069

Bit(s)	R/W	Default	Description
31:28	R/W		reserved
27:24	R/W	0d0	reg_sr3_drtlpf_alpha_11
23:20	R/W		reserved
19:16	R/W	0d0	reg_sr3_drtlpf_alpha_10
15:12	R/W		reserved
11:8	R/W	0d0	reg_sr3_drtlpf_alpha_9
7:4	R/W		reserved
3:0	R/W	0d0	reg_sr3_drtlpf_alpha_8: directional lpf alpha coef for min_sad/max_sad compare

Table 9-1703 SRSHARP0_SR3_DRTLPF_ALPHA_OFST 0x506a

Bit(s)	R/W	Default	Description
31:28	R/W	0	reg_sr3_drtlpf_alpha_ofst7
27:24	R/W	0	reg_sr3_drtlpf_alpha_ofst6
23:20	R/W	0	reg_sr3_drtlpf_alpha_ofst5
19:16	R/W	-2	reg_sr3_drtlpf_alpha_ofst4
15:12	R/W	0	reg_sr3_drtlpf_alpha_ofst3
11:8	R/W	0	reg_sr3_drtlpf_alpha_ofst2
7:4	R/W	0	reg_sr3_drtlpf_alpha_ofst1
3:0	R/W	-2	reg_sr3_drtlpf_alpha_ofst0: directional lpf alpha coef offset of each direction.

Table 9-1704 SRSHARP0_SR3_DERING_CTRL 0x506b

Bit(s)	R/W	Default	Description
31	R/W		reserved
30:28	R/W	1	reg_sr3_dering_enable: dering enable
27	R/W		reserved
26:24	R/W	3	reg_sr3_dering_varlpf_mode: local variant LPF mode. 0: no filter; 1: errosion 3x3; 2: 3x3 lpf; 3: 3x3 errosion + lpf
23:20	R/W	9	reg_sr3_dering_maxrange: range of dering in LR resolution.
19:18	R/W		reserved

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Bit(s)	R/W	Default	Description
17:16	R/W	2	reg_sr3_dering_lcvar_blend_mode: mode for lcvar calculation. 0:HV blend; 1:diag blend; 2:HV blend + V; 3: HV blend+Diag blend
15:8	R/W	40	reg_sr3_dering_lcvar_gain: gain to local variant and normalized to 32 as 1
7:0	R/W	28	reg_sr3_dering_lcvar_nearby_maxsad_th: threshold to use near side maxsad if that side is larger than this threshold, otherwise use the max one.

Table 9-1705 SRSHARP0_SR3_DERING_LUMA2PKGAIN_0TO3 0x506c

Bit(s)	R/W	Default	Description
31:24	R/W	255	reg_sr3_dering_luma2pkgain3: level limit(for th0 < bpcon < th1) of curve for dering pkgain base on LPF luma level
23:16	R/W	255	reg_sr3_dering_luma2pkgain2: level limit(for bpcon < th0) of curve for dering pkgain base on LPF luma level
15:8	R/W	200	reg_sr3_dering_luma2pkgain1: threshold 1 of curve for dering pkgain based on LPF luma level.
7:0	R/W	30	reg_sr3_dering_luma2pkgain0: threshold 0 of curve for dering pkgain based on LPF luma level.

Table 9-1706 SRSHARP0_SR3_DERING_LUMA2PKGAIN_4TO6 0x506d

Bit(s)	R/W	Default	Description
31:24	R/W		reserved
23:16	R/W	24	reg_sr3_dering_luma2pkgain6: rate1 (for bpcon > th1) of curve for dering pkOS based on LPF luma level.
15:8	R/W	50	reg_sr3_dering_luma2pkgain5: rate0 (for bpcon < th0) of curve for dering pkOS based on LPF luma level.
7:0	R/W	255	reg_sr3_dering_luma2pkgain4: level limit(for bpcon > th1) of curve for dering pkgain base on LPF luma level

Table 9-1707 SRSHARP0_SR3_DERING_LUMA2PKOS_0TO3 0x506e

Bit(s)	R/W	Default	Description
31:24	R/W	255	reg_sr3_dering_luma2pkos3: level limit(for th0 < bpcon < th1) of curve for dering pkOS base on LPF luma level
23:16	R/W	255	reg_sr3_dering_luma2pkos2: level limit(for bpcon < th0) of curve for dering pkOS base on LPF luma level
15:8	R/W	200	reg_sr3_dering_luma2pkos1: threshold 1 of curve for dering pkOS based on LPF luma level.
7:0	R/W	30	reg_sr3_dering_luma2pkos0: threshold 0 of curve for dering pkOS based on LPF luma level.

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Table 9-1708 SRSHARP0_SR3_DERING_LUMA2PKOS_4TO6 0x506f

Bit(s)	R/W	Default	Description
31:24	R/W		reserved
23:16	R/W	24	reg_sr3_dering_luma2pkos6: rate1 (for bpcon > th1) of curve for dering pkOS based on LPF luma level.
15:8	R/W	50	reg_sr3_dering_luma2pkos5: rate0 (for bpcon < th0) of curve for dering pkOS based on LPF luma level.
7:0	R/W	255	reg_sr3_dering_luma2pkos4: level limit(for bpcon > th1) of curve for dering pkOS base on LPF luma level

Table 9-1709 SRSHARP0_SR3_DERING_GAINVS_MADSAD 0x5070

Bit(s)	R/W	Default	Description
31:28	R/W	0	reg_sr3_dering_gainvs_maxsad7
27:24	R/W	0	reg_sr3_dering_gainvs_maxsad6
23:20	R/W	0	reg_sr3_dering_gainvs_maxsad5
19:16	R/W	0	reg_sr3_dering_gainvs_maxsad4
15:12	R/W	0	reg_sr3_dering_gainvs_maxsad3
11:8	R/W	0	reg_sr3_dering_gainvs_maxsad2
7:4	R/W	4	reg_sr3_dering_gainvs_maxsad1
3:0	R/W	8	reg_sr3_dering_gainvs_maxsad0: pkgain vs maxsad value, 8 node interpolations.

Table 9-1710 SRSHARP0_SR3_DERING_GAINVS_VR2MAX 0x5071

Bit(s)	R/W	Default	Description
31:28	R/W	15	reg_sr3_dering_gainvs_vr2max7
27:24	R/W	15	reg_sr3_dering_gainvs_vr2max6
23:20	R/W	15	reg_sr3_dering_gainvs_vr2max5
19:16	R/W	15	reg_sr3_dering_gainvs_vr2max4
15:12	R/W	14	reg_sr3_dering_gainvs_vr2max3
11:8	R/W	12	reg_sr3_dering_gainvs_vr2max2
7:4	R/W	2	reg_sr3_dering_gainvs_vr2max1
3:0	R/W	0	reg_sr3_dering_gainvs_vr2max0: pkgain vs ratio

Table 9-1711 SRSHARP0_SR3_DERING_PARAM0 0x5072

Bit(s)	R/W	Default	Description
31:24	R/W		reserved
23:16	R/W	10	reg_sr3_dering_lcvar_floor
15:8	R/W	32	reg_sr3_dering_vr2max_gain: gain to max before feeding to LUT

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Bit(s)	R/W	Default	Description
7:6	R/W		reserved
5:0	R/W	16	reg_sr3_dering_vr2max_limt: limit of maxsad

Table 9-1712 SRSHARP0_SR3_DRTLPF_THETA 0x5073

Bit(s)	R/W	Default	Description
31:0	R/W	0xfe-c96420	reg_sr3_drtlpf_theta: u4x8 directional lpf beta coef for min_sad/min2_sad compared to x=0:7 correspond to [1:8]/16; 0 means no drtLPF, 15: 100% alpha dependant drtLPF.

Table 9-1713 SRSHARP0_SATPRT_CTRL 0x5074

Bit(s)	R/W	Default	Description
31:28	R/W		reserved
27:16	R/W	5	reg_satprt_sat_core: 4x will be coring to cor(irgb_max-irgb_min) to calculate the oy_delt, the smaller the more protection to color, the larger only the rich color will be protected.
15:8	R/W	64	reg_satprt_sat_rate: rate to cor(irgb_max-irgb_min) to calculate the oy_delt,the larger the more protection to color; norm 16 as 1
7:4	R/W		reserved
3:2	R/W	1	reg_satprt_csc_mode: CSC mode of current yuv input: 0:601; 1:709; 2:BT2020 NCL; 3 reserved
1	R/W	1	reg_satprt_is_lmt: flag telling the YUV is limited range data or full rang data; 1 is limited data
0	R/W	0	reg_satprt_enable: 1 to enable of saturation protection for dnlp adjustments

Table 9-1714 SRSHARP0_SATPRT_DIVM 0x5075

Bit(s)	R/W	Default	Description
31:24	R/W		reserved
23:0	R/W	{128,128,128}	reg_satprt_div_m: u8x3, 1/m, normalized to 128 as 1.

Table 9-1715 SRSHARP0_DB_FLT_CTRL 0x5077

Bit(s)	R/W	Default	Description
26	R/W	0	reg_nrdeband_reset1 : // unsigned , default = 0 0 : no reset seed 1: reload chroma seed
25	R/W	0	reg_nrdeband_reset0 : // unsigned , default = 0 0 : no reset seed 1: reload luma seed
24	R/W	0	reg_nrdeband_rgb : // unsigned , default = 0 0 : yuv 1: RGB
23	R/W	1	reg_nrdeband_en11 : // unsigned , default = 1 debanding registers of side lines, [0] for luma, same for below
22	R/W	1	reg_nrdeband_en10 : // unsigned , default = 1 debanding registers of side lines, [1] for chroma, same for below

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Bit(s)	R/W	Default	Description
21	R/W	1	reg_nrdeband_siderand : // unsigned , default = 1 options to use side two lines use the rand, instead of use for the YUV three component of middle line, 0: seed [3]/bandrand[3] for middle line yuv; 1: seed[3]/bandrand[3] for nearby three lines Y;
20	R/W	0	reg_nrdeband_randmode : // unsigned , default = 0 mode of rand noise adding, 0: same noise strength for all difs; else: strenght of noise will not exceed the difs, MIN((pPKReg- > reg_nrdeband_bandrand[m]), noise[m])
19:17	R/W	6	reg_nrdeband_bandrand2 : // unsigned , default = 6
15:13	R/W	6	reg_nrdeband_bandrand1 : // unsigned , default = 6
11: 9	R/W	6	reg_nrdeband_bandrand0 : // unsigned , default = 6
7	R/W	1	reg_nrdeband_hpxor1 : // unsigned , default = 1 debanding random hp portion xor, [0] for luma
6	R/W	1	reg_nrdeband_hpxor0 : // unsigned , default = 1 debanding random hp portion xor, [1] for chroma
5	R/W	1	reg_nrdeband_en1 : // unsigned , default = 1 debanding registers, for luma
4	R/W	1	reg_nrdeband_en0 : // unsigned , default = 1 debanding registers, for chroma
3: 2	R/W	2	reg_nrdeband_lpf_mode1 : // unsigned , default = 2 lpf mode, 0: 3x3, 1:3x5; 2: 5x5; 3:5x7
1: 0	R/W	2	reg_nrdeband_lpf_mode0 : // unsigned , default = 2 lpf mode, 0: 3x3, 1:3x5; 2: 5x5; 3:5x7

Table 9-1716 SRSHARP0_DB_FLT_RANDLUT 0x5079

Bit(s)	R/W	Default	Description
23:21	R/W	1	reg_nrdeband_randslut7 : // unsigned , default = 1 lut0
20:18	R/W	1	reg_nrdeband_randslut6 : // unsigned , default = 1 lut0
17:15	R/W	1	reg_nrdeband_randslut5 : // unsigned , default = 1 lut0
14:12	R/W	1	reg_nrdeband_randslut4 : // unsigned , default = 1 lut0
11: 9	R/W	1	reg_nrdeband_randslut3 : // unsigned , default = 1 lut0
8: 6	R/W	1	reg_nrdeband_randslut2 : // unsigned , default = 1 lut0
5: 3	R/W	1	reg_nrdeband_randslut1 : // unsigned , default = 1 lut0
2: 0	R/W	1	reg_nrdeband_randslut0 : // unsigned , default = 1 lut0

Table 9-1717 SRSHARP0_DB_FLT_PXI_THRD 0x507a

Bit(s)	R/W	Default	Description
25:16	R/W	0	reg_nrdeband_yc_th1 : // unsigned , default = 0 to luma/|u/v| for using the denoise
9: 0	R/W	0	reg_nrdeband_yc_th0 : // unsigned , default = 0 to luma/|u/v| for using the denoise

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Table 9-1718 SRSHARP0_DB_FLT_SEED_Y 0x507b

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8240	reg_nrdeband_seed0 : // unsigned , default = 1621438240 noise adding seed for Y. seed[0]= 0x60a52f20; as default

Table 9-1719 SRSHARP0_DB_FLT_SEED_U 0x507c

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8247	reg_nrdeband_seed1 : // unsigned , default = 1621438247 noise adding seed for U. seed[0]= 0x60a52f27; as default

Table 9-1720 SRSHARP0_DB_FLT_SEED_V 0x507d

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8242	reg_nrdeband_seed2 : // unsigned , default = 1621438242 noise adding seed for V. seed[0]= 0x60a52f22; as default

Table 9-1721 SRSHARP0_PKGAIN_VSLUMA_LUT_L 0x507e

Bit(s)	R/W	Default	Description
31:28	R/W	5	reg_pkgain_vsluma_lut7
27:24	R/W	6	reg_pkgain_vsluma_lut6
23:20	R/W	6	reg_pkgain_vsluma_lut5
19:16	R/W	6	reg_pkgain_vsluma_lut4
15:12	R/W	7	reg_pkgain_vsluma_lut3
11:8	R/W	10	reg_pkgain_vsluma_lut2
7:4	R/W	12	reg_pkgain_vsluma_lut1
3:0	R/W	8	reg_pkgain_vsluma_lut0

Table 9-1722 SRSHARP0_PKGAIN_VSLUMA_LUT_H 0x507f

Bit(s)	R/W	Default	Description
31:4	R/W		reserved
3:0	R/W	4	reg_pkgain_vsluma_lut8

Table 9-1723 SRSHARP0_PKOSHT_VSLUMA_LUT_L 0x5080

Bit(s)	R/W	Default	Description
31:28	R/W	5	reg_pkosht_vsluma_lut7
27:24	R/W	6	reg_pkosht_vsluma_lut6
23:20	R/W	6	reg_pkosht_vsluma_lut5
19:16	R/W	6	reg_pkosht_vsluma_lut4

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Bit(s)	R/W	Default	Description
15:12	R/W	7	reg_pkosht_vsluma_lut3
11:8	R/W	10	reg_pkosht_vsluma_lut2
7:4	R/W	12	reg_pkosht_vsluma_lut1
3:0	R/W	8	reg_pkosht_vsluma_lut0

Table 9-1724 SRSHARP0_PKOSHT_VSLUMA_LUT_H 0x5081

Bit(s)	R/W	Default	Description
31:4	R/W		reserved
3:0	R/W	4	reg_pkosht_vsluma_lut8

Table 9-1725 SRSHARP0_SATPRT_LMT_RGB1 0x5082

Bit(s)	R/W	Default	Description
27:16	R/W	0d0	reg_satprt_lmt_g:
11: 0	R/W	0d0	reg_satprt_lmt_r: limit of RGB channel, for limited range RGB, 12bits

Table 9-1726 SRSHARP0_SATPRT_LMT_RGB2 0x5083

Bit(s)	R/W	Default	Description
31:16	R/W	0d0	reserved
11: 0	R/W	0d0	reg_satprt_lmt_b: limit of RGB channel, for limited range RGB

Table 9-1727 SRSHARP0_SHARP_GATE_CLK_CTRL_0 0x5084

Bit(s)	R/W	Default	Description
31:0	R/W	0d0	Gate clock control [01:00]: sharp input control unit [03:02]: deband unit [05:04]: dejaggy unit [07:06]: dnlp unit [09:08]: demo control unit [11:10]: horiz interp unit

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Table 9-1728 SRSHARP0_SHARP_GATE_CLK_CTRL_1 0x5085

Bit(s)	R/W	Default	Description
31:0	R/W	0d0	Gate clock control [01:00]: sr_top “pipe_ctrl” [03:02]: drt [05:04]: ssd [07:06]: cubic [09:08]: edi [11:10]: pkgainsad [13:12]: bicomux [15:14]: bicin_fifo [17:16]: lpf4pkgain_fifo [19:18]: min2hvgain_fifo [21:20]: sad4pkgain_fifo [23:22]: dirminmax4xtl_fifo [25:24]: drtsad8_fifo [27:26]: ssdmax_fifo [29:28]: pkminmax_fifo [31:30]: cirdrtgain_fifo

Table 9-1729 SRSHARP0_SHARP_GATE_CLK_CTRL_2 0x5086

Bit(s)	R/W	Default	Description
31:0	R/W	0d0	Gate clock control [01:00]: bufdiff_fifo [03:02]: osvar_fifo [05:04]: pkhvgain unit [07:06]: pkgain unit [09:08]: TI unit [11:10]: pk unit [13:12]: locvar unit [15:14]: hvconc unit

Table 9-1730 SRSHARP0_SHARP_GATE_CLK_CTRL_3 0x5087

Bit(s)	R/W	Default	Description
31:0	R/W	0d0	Gate clock control [01:00]: TI, htl Y [03:02]: TI, vti Y [05:04]: TI, htl U [07:06]: TI, vtl U [09:08]: TI, htl V [11:10]: TI, vtl V [13:12]: TI, lumaminmax_fifo [15:14]: TI, chrmminmax fifo

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Table 9-1731 SRSHARP0_SHARP_DPS_CTRL 0x5088

Bit(s)	R/W	Default	Description
31:0	R/W	0d0	Power saving control : hvcon : nrssd : os filter : cubic 5 lines to 9 lines : dering : locvar : drtlpf : hlti : hcti : vlti : vcti : lti blend : cti blend : htishort (no used) : nr Y filter : nr C filter : nr belnd : pkti blend : os ctrl : pk HP : pk BP [26:24] dejaggy power saving control [30:28] reserved

Table 9-1732 SRSHARP0_DNLP_00 0x5090

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0010-0008	reg_dnlp_ygrid0:dnlp00 . unsigned , default = 32'h00100008

Table 9-1733 SRSHARP0_DNLP_01 0x5091

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0020-0018	reg_dnlp_ygrid1:dnlp01 . unsigned , default = 32'h00200018

Table 9-1734 SRSHARP0_DNLP_02 0x5092

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0030-0028	reg_dnlp_ygrid2:dnlp02 . unsigned , default = 32'h00300028

Table 9-1735 SRSHARP0_DNLP_03 0x5093

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0040-0038	reg_dnlp_ygrid3:dnlp03 . unsigned , default = 32'h00400038

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Table 9-1736 SRSHARP0_DNLP_04 0x5094

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0050-0048	reg_dnlp_ygrid4:dnlp04 . unsigned , default = 32'h00500048

Table 9-1737 SRSHARP0_DNLP_05 0x5095

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0068-005c	reg_dnlp_ygrid5:dnlp05 . unsigned , default = 32'h0068005c

Table 9-1738 SRSHARP0_DNLP_06 0x5096

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0080-0074	reg_dnlp_ygrid6:dnlp06 . unsigned , default = 32'h00800074

Table 9-1739 SRSHARP0_DNLP_07 0x5097

Bit(s)	R/W	Default	Description
31: 0	R/W	0x00-a00090	reg_dnlp_ygrid7:dnlp07 . unsigned , default = 32'h00a00090

Table 9-1740 SRSHARP0_DNLP_08 0x5098

Bit(s)	R/W	Default	Description
31: 0	R/W	0x00-c000b0	reg_dnlp_ygrid8:dnlp08 . unsigned , default = 32'h00c000b0

Table 9-1741 SRSHARP0_DNLP_09 0x5099

Bit(s)	R/W	Default	Description
31: 0	R/W	0x00-e000d0	reg_dnlp_ygrid9:dnlp09 . unsigned , default = 32'h00e000d0

Table 9-1742 SRSHARP0_DNLP_10 0x509a

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0100-00f0	reg_dnlp_ygrid10:dnlp10 . unsigned , default = 32'h010000f0

Table 9-1743 SRSHARP0_DNLP_11 0x509b

Bit(s)	R/W	Default	Description
31: 0	R/W	0x012-c0114	reg_dnlp_ygrid11:dnlp11 . unsigned , default = 32'h012c0114

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Table 9-1744 SRSHARP0_DNLP_12 0x509c

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0154-0140	reg_dnlp_ygrid12:dnlp12 . unsigned , default = 32'h01540140

Table 9-1745 SRSHARP0_DNLP_13 0x509d

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0180-016c	reg_dnlp_ygrid13:dnlp13 . unsigned , default = 32'h0180016c

Table 9-1746 SRSHARP0_DNLP_14 0x509e

Bit(s)	R/W	Default	Description
31: 0	R/W	0x01-c001a0	reg_dnlp_ygrid14:dnlp14 . unsigned , default = 32'h01c001a0

Table 9-1747 SRSHARP0_DNLP_15 0x509f

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0200-01e0	reg_dnlp_ygrid15:dnlp15 . unsigned , default = 32'h020001e0

Table 9-1748 SRSHARP0_DNLP_16 0x50a0

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0240-0220	reg_dnlp_ygrid16:dnlp16 . unsigned , default = 32'h02400220

Table 9-1749 SRSHARP0_DNLP_17 0x50a1

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0280-0260	reg_dnlp_ygrid17:dnlp17 . unsigned , default = 32'h02800260

Table 9-1750 SRSHARP0_DNLP_18 0x50a2

Bit(s)	R/W	Default	Description
31: 0	R/W	0x02-b00298	reg_dnlp_ygrid18:dnlp18 . unsigned , default = 32'h02b00298

Table 9-1751 SRSHARP0_DNLP_19 0x50a3

Bit(s)	R/W	Default	Description
31: 0	R/W	0x02-e002c8	reg_dnlp_ygrid19:dnlp19 . unsigned , default = 32'h02e002c8

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Table 9-1752 SRSHARP0_DNLP_20 0x50a4

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0300-02f0	reg_dnlp_ygrid20:dnlp20 . unsigned , default = 32'h030002f0

Table 9-1753 SRSHARP0_DNLP_21 0x50a5

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0320-0310	reg_dnlp_ygrid21:dnlp21 . unsigned , default = 32'h03200310

Table 9-1754 SRSHARP0_DNLP_22 0x50a6

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0338-032c	reg_dnlp_ygrid22:dnlp22 . unsigned , default = 32'h0338032c

Table 9-1755 SRSHARP0_DNLP_23 0x50a7

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0350-0348	reg_dnlp_ygrid23:dnlp23 . unsigned , default = 32'h03500348

Table 9-1756 SRSHARP0_DNLP_24 0x50a8

Bit(s)	R/W	Default	Description
31: 0	R/W	0x035-c0358	reg_dnlp_ygrid24:dnlp24 . unsigned , default = 32'h035c0358

Table 9-1757 SRSHARP0_DNLP_25 0x50a9

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0368-0360	reg_dnlp_ygrid25:dnlp25 . unsigned , default = 32'h03680360

Table 9-1758 SRSHARP0_DNLP_26 0x50aa

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0378-0370	reg_dnlp_ygrid26:dnlp26 . unsigned , default = 32'h03780370

Table 9-1759 SRSHARP0_DNLP_27 0x50ab

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0388-0380	reg_dnlp_ygrid27:dnlp27 . unsigned , default = 32'h03880380

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Table 9-1760 SRSHARP0_DNLP_28 0x50ac

Bit(s)	R/W	Default	Description
31: 0	R/W	0x03-a00390	reg_dnlp_ygrid28:dnlp28 . unsigned , default = 32'h03a00390

Table 9-1761 SRSHARP0_DNLP_29 0x50ad

Bit(s)	R/W	Default	Description
31: 0	R/W	0x03-c003b0	reg_dnlp_ygrid29:dnlp29 . unsigned , default = 32'h03c003b0

Table 9-1762 SRSHARP0_DNLP_30 0x50ae

Bit(s)	R/W	Default	Description
31: 0	R/W	0x03-e003d0	reg_dnlp_ygrid30:dnlp30 . unsigned , default = 32'h03e003d0

Table 9-1763 SRSHARP0_DNLP_31 0x50af

Bit(s)	R/W	Default	Description
31: 0	R/W	0x03f-c03f0	reg_dnlp_ygrid31:dnlp31 . unsigned , default = 32'h03fc03f0

Table 9-1764 SRSHARP0_SHARP_SYNC_CTRL 0x50b0

Bit(s)	R/W	Default	Description
15:0	R/W	0d0	Shadow control for some setting: 0 to use VSYNC to shadow : SR all bypass : reg_sr2_bic_pknr_bypass [2] : reg_3d_mode [3] : reg_nrdeband_en11 [4]: reg_nrdeband_en10 [5]: reg_nrdeband_en1 [6]: reg_nrdeband_en0 [7]: reg_dejaggy_enable [8]: reg_sr2_sharp_prc_lr [9]: reg_sharp_pk_en [10]:reg_sharp_nr_en [11]:reg_adp_hlti_en [12]:reg_adp_hcti_en [13]:reg_adp_vlti_en [14]:reg_adp_vcti_en [15]:reg_dnlp_en

Table 9-1765 SRSHARP0_NR_GAU_YH_COEF02 0x50b2

Bit(s)	R/W	Default	Description
29:20	R/W	0d32	luma's horizontal adaptive coef0 . signed , default = 32
19:10	R/W	0d32	luma's horizontal adaptive coef1 . signed , default = 32
9:0	R/W	0d16	luma's horizontal adaptive coef2 . signed , default = 16

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Table 9-1766 SRSHARP0_NR_GAU_YH_COEF34 0x50b3

Bit(s)	R/W	Default	Description
19:10	R/W	0d0	luma's horizontal adaptive coef3 . signed , default = 0
9:0	R/W	0d0	luma's horizontal adaptive coef4 . signed , default = 0

Table 9-1767 SRSHARP0_NR_GAU_YV_COEF1 0x50b4

Bit(s)	R/W	Default	Description
29:20	R/W	0d32	luma's vertical adaptive coef0 . signed , default = 32
19:10	R/W	0d32	luma's vertical adaptive coef1 . signed , default = 32
9:0	R/W	0d16	luma's vertical adaptive coef2 . signed , default = 16

Table 9-1768 SRSHARP0_NR_GAU_CH_COEF02 0x50b5

Bit(s)	R/W	Default	Description
29:20	R/W	0d32	chroma's horizontal adaptive coef0 . signed , default = 32
19:10	R/W	0d32	chroma's horizontal adaptive coef1 . signed , default = 32
9:0	R/W	0d16	chroma's horizontal adaptive coef2 . signed , default = 16

Table 9-1769 SRSHARP0_NR_GAU_CH_COEF34 0x50b6

Bit(s)	R/W	Default	Description
19:10	R/W	0d0	chroma's horizontal adaptive coef3 . signed , default = 0
9:0	R/W	0d0	chroma's horizontal adaptive coef4 . signed , default = 0

Table 9-1770 SRSHARP0_NR_GAU_CV_COEF1 0x50b7

Bit(s)	R/W	Default	Description
29:20	R/W	0d32	chroma's vertical adaptive coef0 . signed , default = 32
19:10	R/W	0d32	chroma's vertical adaptive coef1 . signed , default = 32
9:0	R/W	0d16	chroma's vertical adaptive coef2 . signed , default = 16

Table 9-1771 SRSHARP0_DB_FLT_CTRL1 0x50b8

Bit(s)	R/W	Default	Description
17:16	R/W	0d2	reg_nrdeband_noise_rs .unsigned , default = 2
15:12	R/W	0d8	reg_nrdeband_randgain .unsigned , default = 8

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Table 9-1772 SRSHARP0_DB_FLT_LUMA_THRD 0x50b9

Bit(s)	R/W	Default	Description
29:24	R/W	36	reg_nrdeband_luma_th3 : // unsigned , default = 36 threshold to |Y-Ylpf|, if < th[0] use lpf
21:16	R/W	28	reg_nrdeband_luma_th2 : // unsigned , default = 28 elseif < th[1] use (lpf*3 + y)/4
13:8	R/W	24	reg_nrdeband_luma_th1 : // unsigned , default = 24 elseif < th[1] use (lpf*3 + y)/ 4elseif < th[2] (lpf*1 + y)/2
5:0	R/W	20	reg_nrdeband_luma_th0 : // unsigned , default = 20 elseif < th[1] use (lpf*3 + y)/ 4elseif elseif < th[3] (lpf*1 + 3*y)/4; else

Table 9-1773 SRSHARP0_DB_FLT_CHRM_THRD 0x50ba

Bit(s)	R/W	Default	Description
29:24	R/W	36	reg_nrdeband_chrm_th3 : // unsigned , default = 36 threshold to |Y-Ylpf|, if < th[0] use lpf
21:16	R/W	28	reg_nrdeband_chrm_th2 : // unsigned , default = 28 elseif < th[1] use (lpf*3 + y)/4
13:8	R/W	24	reg_nrdeband_chrm_th1 : // unsigned , default = 24 elseif < th[1] use (lpf*3 + y)/ 4elseif < th[2] (lpf*1 + y)/2
5:0	R/W	20	reg_nrdeband_chrm_th0 : // unsigned , default = 20 elseif < th[1] use (lpf*3 + y)/ 4elseif elseif < th[3] (lpf*1 + 3*y)/4; else

Table 9-1774 SRSHARP0_FMETER_CTRL 0x5089

Bit(s)	R/W	Default	Description
11:10	R/W	0	reg_fmeter_vwin_mm : vertical window size, 0:1 cloumn,1:3cloumn, 2or3:5cloumn.unsigned,default = 0
9:8	R/W	0	reg_fmeter_hwin_mm : horizontal window size, 0:1x7, 1:1x9, 2or3: 1x11 .unsigned , default = 0
7	R/W	0	reg_fmeter_d2_mode : selectino filter D2, 0: [0 -2 0 0 2], 1: [-2 0 0 0 2] .unsigned , default = 0
6	R/W	0	reg_fmeter_v2_mode : selection filter V2, 0: [0 -2 0 0 2], 1: [-2 0 0 0 2] .unsigned , default = 0
5:4	R/W	0	reg_fmeter_h2_mode: selection filter H2, 0: [0 0 0 -2 0 0 2 0 0], 1: [-2 0 0 0 2], 2or3: [0-2 0 0 0 0 0 2 0] .unsigned , default = 0
0	R/W	0	reg_freq_meter_en: freq meter enable .unsigned , default = 0

Table 9-1775 SRSHARP0_FMETER_WIN_HOR 0x508a

Bit(s)	R/W	Default	Description
28:16	R/W	1920	reg_fmeter_xwin_ed: window location: hend .unsigned , default = 1920
12:0	R/W	0	reg_fmeter_xwin_st: window location: hstart .unsigned , default = 0

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Table 9-1776 SRSHARP0_FMETER_WIN_VER 0x508b

Bit(s)	R/W	Default	Description
28:16	R/W	1080	reg_fmeter_ywin_ed: window location: vend .unsigned , default = 1080
12:0	R/W	0	reg_fmeter_ywin_st: window location: vstart .unsigned , default = 0

Table 9-1777 SRSHARP0_FMETER_CORING 0x508c

Bit(s)	R/W	Default	Description
31:24	R/W	4	reg_fmeter_low_bound: low bound for threshold .unsigned , default = 4
23:16	R/W	4	reg_fmeter_coring_d: coring of diff before compare with threshold for diagonal frequency .unsigned , default = 4
15:8	R/W	4	reg_fmeter_coring_v: coring of diff before compare with threshold for vertical frequency .unsigned , default = 4
7:0	R/W	4	reg_fmeter_coring_h: coring of diff before compare with threshold for horizontal frequency .unsigned , default = 4

Table 9-1778 SRSHARP0_FMETER_RATIO_H 0x508d

Bit(s)	R/W	Default	Description
21:16	R/W	16	reg_fmeter_ratio_h2: ratio for threshold calc. for horizontal frequency, 16 is normalized as "1" .unsigned , default = 16
13:8	R/W	16	reg_fmeter_ratio_h1: ratio for threshold calc. for horizontal frequency, 16 is normalized as "1" .unsigned , default = 16
5:0	R/W	16	reg_fmeter_ratio_h0: ratio for threshold calc. for horizontal frequency, 16 is normalized as "1" .unsigned , default = 16

Table 9-1779 SRSHARP0_FMETER_RATIO_V 0x508e

Bit(s)	R/W	Default	Description
21:16	R/W	16	reg_fmeter_ratio_v2: ratio for threshold calc. for vertical frequency, 16 is normalized as "1" .unsigned , default = 16
13:8	R/W	16	reg_fmeter_ratio_v1: ratio for threshold calc. for vertical frequency, 16 is normalized as "1" .unsigned , default = 16
5:0	R/W	16	reg_fmeter_ratio_v0: ratio for threshold calc. for vertical frequency, 16 is normalized as "1" .unsigned , default = 16

Table 9-1780 SRSHARP0_FMETER_RATIO_D 0x508f

Bit(s)	R/W	Default	Description
21:16	R/W	16	reg_fmeter_ratio_d2: ratio for threshold calc. for diagonal frequency, 16 is normalized as "1" .unsigned , default = 16
13:8	R/W	16	reg_fmeter_ratio_d1: ratio for threshold calc. for diagonal frequency, 16 is normalized as "1" .unsigned , default = 16
5:0	R/W	16	reg_fmeter_ratio_d0: ratio for threshold calc. for diagonal frequency, 16 is normalized as "1" .unsigned , default = 16

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Table 9-1781 SRSHARP0_RO_FMETER_HCNT_TYPE0 0x5046

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_hcnt_type0: count for horizontal frequency

Table 9-1782 SRSHARP0_RO_FMETER_HCNT_TYPE1 0x5047

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_hcnt_type1: count for horizontal frequency

Table 9-1783 SRSHARP0_RO_FMETER_HCNT_TYPE2 0x5048

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_hcnt_type2: count for horizontal frequency

Table 9-1784 SRSHARP0_RO_FMETER_HCNT_TYPE3 0x5049

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_hcnt_type3: count for horizontal frequency

Table 9-1785 SRSHARP0_RO_FMETER_VCNT_TYPE0 0x504a

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_vcnt_type0: count for vertical frequency

Table 9-1786 SRSHARP0_RO_FMETER_VCNT_TYPE1 0x504b

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_vcnt_type1: count for vertical frequency

Table 9-1787 SRSHARP0_RO_FMETER_VCNT_TYPE2 0x504c

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_vcnt_type2: count for vertical frequency

Table 9-1788 SRSHARP0_RO_FMETER_VCNT_TYPE3 0x504d

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_vcnt_type3: count for vertical frequency

Table 9-1789 SRSHARP0_RO_FMETER_PDCNT_TYPE0 0x504e

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_pdcnt_type0: count for positive diagonal frequency

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Table 9-1790 SRSHARP0_RO_FMETER_PDCNT_TYPE1 0x504f

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_pdcnt_type1: count for positive diagonal frequency

Table 9-1791 SRSHARP0_RO_FMETER_PDCNT_TYPE2 0x5050

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_pdcnt_type2: count for positive diagonal frequency

Table 9-1792 SRSHARP0_RO_FMETER_PDCNT_TYPE3 0x5051

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_pdcnt_type3: count for positive diagonal frequency

Table 9-1793 SRSHARP0_RO_FMETER_NDCNT_TYPE0 0x5052

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_ndcnt_type0: count for negitive diagonal frequency

Table 9-1794 SRSHARP0_RO_FMETER_NDCNT_TYPE1 0x5053

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_ndcnt_type1: count for negitive diagonal frequency

Table 9-1795 SRSHARP0_RO_FMETER_NDCNT_TYPE2 0x5054

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_ndcnt_type2: count for negitive diagonal frequency

Table 9-1796 SRSHARP0_RO_FMETER_NDCNT_TYPE3 0x5055

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_ndcnt_type3: count for negitive diagonal frequency

Table 9-1797 SRSHARP0_SR7_DRTLPF_EN 0x5100

Bit(s)	R/W	Default	Description
31:11			reserved
10	RW	0	reg_sr7_drtlpf_beta_en2: enable of direction ambiguity protection for drt_lpf, beta for drt filter coef base on the x=cal_drt_dif8(min_idx,min2_idx)
9	RW	0	reg_sr7_drtlpf_beta_en1: enable of direction ambiguity protection for drt_lpf, beta for drt filter coef base on the x=cal_drt_dif8(min_idx,min2_idx)

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Bit(s)	R/W	Default	Description
8	RW	0	reg_sr7_drtlpf_beta_en0: enable of direction ambiguity protection for drt_lpf, beta for drt filter coef base on the x=cal_drt_dif8(min_idx,min2_idx)
7:6			reserved
5	RW	0	reg_sr7_drtlpf_edge_en2: enable of direction lpf based on edge strength
4	RW	0	reg_sr7_drtlpf_edge_en1: enable of direction lpf based on edge strength
3	RW	0	reg_sr7_drtlpf_edge_en0: enable of direction lpf based on edge strength
2	RW	1	reg_sr7_drtlpf_sdfd_en2: sdfd gamma (HF burst compare to real edge protection) enable
1	RW	1	reg_sr7_drtlpf_sdfd_en1: sdfd gamma (HF burst compare to real edge protection) enable.
0	RW	1	reg_sr7_drtlpf_sdfd_en0: sdfd gamma (HF burst compare to real edge protection) enable.

Table 9-1798 SRSHARP0_SR7_DRTLPF_BETA 0x5101

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	0	reg_sr7_drtlpf_beta3: beta for drt filter coef base on the x=cal_drt_dif8(min_idx, min2_idx)
11:8	RW	4	reg_sr7_drtlpf_beta2: beta for drt filter coef base on the x=cal_drt_dif8(min_idx, min2_idx)
7:4	RW	8	reg_sr7_drtlpf_beta1: beta for drt filter coef base on the x=cal_drt_dif8(min_idx, min2_idx)
3:0	RW	15	reg_sr7_drtlpf_beta0: beta for drt filter coef base on the x=cal_drt_dif8(min_idx, min2_idx), beta = lut[x-1], the larger of x, means the higher possibility for ambiguilty, beta=0 use org wo lpf.

Table 9-1799 SRSHARP0_SR7_PKBLD_BETA 0x5102

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	0	reg_sr7_pkdrtbld_beta3: beta for drt and cir blend base on the x=cal_drt_dif8 (min_idx,min2_idx)
11:8	RW	4	reg_sr7_pkdrtbld_beta2: beta for drt and cir blend base on the x=cal_drt_dif8 (min_idx,min2_idx)
7:4	RW	8	reg_sr7_pkdrtbld_beta1: beta for drt and cir blend base on the x=cal_drt_dif8 (min_idx,min2_idx)
3:0	RW	15	reg_sr7_pkdrtbld_beta0: beta for drt and cir blend base on the x=cal_drt_dif8 (min_idx,min2_idx), beta = lut[x-1], the larger of x, means the higher possibility for ambiguilty, beta=0 use org wo lpf.

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Table 9-1800 SRSHARP0_SR7_XLTIBLD_BETA 0x5103

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	0	reg_sr7_xlti_dcbld_beta3: beta for denoise and org dc blend base on the x=cal_drt_dif8(min_idx,min2_idx)
11:8	RW	4	reg_sr7_xlti_dcbld_beta2: beta for denoise and org dc blend base on the x=cal_drt_dif8(min_idx,min2_idx)
7:4	RW	8	reg_sr7_xlti_dcbld_beta1: beta for denoise and org dc blend base on the x=cal_drt_dif8(min_idx,min2_idx)
3:0	RW	15	reg_sr7_xlti_dcbld_beta0: beta for denoise and org dc blend base on the x=cal_drt_dif8(min_idx,min2_idx) beta = lut[x-1], the larger of x, means the higher possibility for ambiguilty, beta=0 use org wo lpf.

Table 9-1801 SRSHARP0_SR7_DRTLPF_EDGE0 0x5104

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_drtlpf_edge7: edge lamda for drt lpf base on max_sad [0:16:128~255]
27:24	RW	15	reg_sr7_drtlpf_edge6: edge lamda for drt lpf base on max_sad [0:16:128~255]
23:20	RW	15	reg_sr7_drtlpf_edge5: edge lamda for drt lpf base on max_sad [0:16:128~255]
19:16	RW	15	reg_sr7_drtlpf_edge4: edge lamda for drt lpf base on max_sad [0:16:128~255]
15:12	RW	15	reg_sr7_drtlpf_edge3: edge lamda for drt lpf base on max_sad [0:16:128~255]
11:8	RW	15	reg_sr7_drtlpf_edge2: edge lamda for drt lpf base on max_sad [0:16:128~255]
7:4	RW	15	reg_sr7_drtlpf_edge1: edge lamda for drt lpf base on max_sad [0:16:128~255]
3:0	RW	15	reg_sr7_drtlpf_edge0: edge lamda for drt lpf base on max_sad [0:16:128~255]

Table 9-1802 SRSHARP0_SR7_DRTLPF_EDGE1 0x5105

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_drtlpf_edge15: edge lamda for drt lpf base on max_sad [0:16:128~255]
27:24	RW	15	reg_sr7_drtlpf_edge14: edge lamda for drt lpf base on max_sad [0:16:128~255]
23:20	RW	15	reg_sr7_drtlpf_edge13: edge lamda for drt lpf base on max_sad [0:16:128~255]
19:16	RW	15	reg_sr7_drtlpf_edge12: edge lamda for drt lpf base on max_sad [0:16:128~255]
15:12	RW	15	reg_sr7_drtlpf_edge11: edge lamda for drt lpf base on max_sad [0:16:128~255]
11:8	RW	15	reg_sr7_drtlpf_edge10: edge lamda for drt lpf base on max_sad [0:16:128~255]
7:4	RW	15	reg_sr7_drtlpf_edge9: edge lamda for drt lpf base on max_sad [0:16:128~255]
3:0	RW	15	reg_sr7_drtlpf_edge8: edge lamda for drt lpf base on max_sad [0:16:128~255]

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Table 9-1803 SRSHARP0_SR7_DRTLPF_SDCOR0 0x5106

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_drtlpf_sdcor7: gamma for drt lpf base on SD'[0:16:128~255]
27:24	RW	15	reg_sr7_drtlpf_sdcor6: gamma for drt lpf base on SD'[0:16:128~255]
23:20	RW	15	reg_sr7_drtlpf_sdcor5: gamma for drt lpf base on SD'[0:16:128~255]
19:16	RW	15	reg_sr7_drtlpf_sdcor4: gamma for drt lpf base on SD'[0:16:128~255]
15:12	RW	15	reg_sr7_drtlpf_sdcor3: gamma for drt lpf base on SD'[0:16:128~255]
11:8	RW	15	reg_sr7_drtlpf_sdcor2: gamma for drt lpf base on SD'[0:16:128~255]
7:4	RW	15	reg_sr7_drtlpf_sdcor1: gamma for drt lpf base on SD'[0:16:128~255]
3:0	RW	15	reg_sr7_drtlpf_sdcor0: gamma for drt lpf base on SD'[0:16:128~255]

Table 9-1804 SRSHARP0_SR7_DRTLPF_SDCOR1 0x5107

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_drtlpf_sdcor15: gamma for drt lpf base on SD'[0:16:128~255]
27:24	RW	15	reg_sr7_drtlpf_sdcor14: gamma for drt lpf base on SD'[0:16:128~255]
23:20	RW	15	reg_sr7_drtlpf_sdcor13: gamma for drt lpf base on SD'[0:16:128~255]
19:16	RW	15	reg_sr7_drtlpf_sdcor12: gamma for drt lpf base on SD'[0:16:128~255]
15:12	RW	15	reg_sr7_drtlpf_sdcor11: gamma for drt lpf base on SD'[0:16:128~255]
11:8	RW	15	reg_sr7_drtlpf_sdcor10: gamma for drt lpf base on SD'[0:16:128~255]
7:4	RW	15	reg_sr7_drtlpf_sdcor9: gamma for drt lpf base on SD'[0:16:128~255]
3:0	RW	15	reg_sr7_drtlpf_sdcor8: gamma for drt lpf base on SD'[0:16:128~255]

Table 9-1805 SRSHARP0_SR7_CTIGAIN_SDCOR0 0x5108

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_ctigain_sdcor7: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
27:24	RW	15	reg_sr7_ctigain_sdcor6: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
23:20	RW	15	reg_sr7_ctigain_sdcor5: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
19:16	RW	15	reg_sr7_ctigain_sdcor4: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
15:12	RW	15	reg_sr7_ctigain_sdcor3: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
11:8	RW	15	reg_sr7_ctigain_sdcor2: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
7:4	RW	15	reg_sr7_ctigain_sdcor1: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
3:0	RW	15	reg_sr7_ctigain_sdcor0: adaptive gamma for cti boost gain base on SD'[0:16:128~255]

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Table 9-1806 SRSHARP0_SR7_CTIGAIN_SDCOR1 0x5109

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_ctigain_sdcor15: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
27:24	RW	15	reg_sr7_ctigain_sdcor14: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
23:20	RW	15	reg_sr7_ctigain_sdcor13: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
19:16	RW	15	reg_sr7_ctigain_sdcor12: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
15:12	RW	15	reg_sr7_ctigain_sdcor11: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
11:8	RW	15	reg_sr7_ctigain_sdcor10: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
7:4	RW	15	reg_sr7_ctigain_sdcor9: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
3:0	RW	15	reg_sr7_ctigain_sdcor8: adaptive gamma for cti boost gain base on SD'[0:16:128~255]

Table 9-1807 SRSHARP0_SR7_LTIGAIN_SDCOR0 0x510a

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_ltigain_sdcor7: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
27:24	RW	15	reg_sr7_ltigain_sdcor6: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
23:20	RW	15	reg_sr7_ltigain_sdcor5: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
19:16	RW	15	reg_sr7_ltigain_sdcor4: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
15:12	RW	15	reg_sr7_ltigain_sdcor3: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
11:8	RW	15	reg_sr7_ltigain_sdcor2: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
7:4	RW	15	reg_sr7_ltigain_sdcor1: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
3:0	RW	15	reg_sr7_ltigain_sdcor0: adaptive gamma for lti boost gain base on SD'[0:16:128~255]

Table 9-1808 SRSHARP0_SR7_LTIGAIN_SDCOR1 0x510b

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_ltigain_sdcor15: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
27:24	RW	15	reg_sr7_ltigain_sdcor14: adaptive gamma for lti boost gain base on SD'[0:16:128~255]

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Bit(s)	R/W	Default	Description
23:20	RW	15	reg_sr7_ltigain_sdcor13: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
19:16	RW	15	reg_sr7_ltigain_sdcor12: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
15:12	RW	15	reg_sr7_ltigain_sdcor11: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
11:8	RW	15	reg_sr7_ltigain_sdcor10: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
7:4	RW	15	reg_sr7_ltigain_sdcor9: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
3:0	RW	15	reg_sr7_ltigain_sdcor8: adaptive gamma for lti boost gain base on SD'[0:16:128~255]

Table 9-1809 SRSHARP0_SR7_HLTIBPF_TAP0 0x510c

Bit(s)	R/W	Default	Description
31:24	RW	0	reg_sr7_hlti_bpf_tap153: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0,signed
23:16	RW	-34	reg_sr7_hlti_bpf_tap152: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0,signed
15:8	RW	-1	reg_sr7_hlti_bpf_tap151: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0, signed
7:0	RW	120	reg_sr7_hlti_bpf_tap150: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0,signed

Table 9-1810 SRSHARP0_SR7_HLTIBPF_TAP1 0x510d

Bit(s)	R/W	Default	Description
31:24	RW	2	reg_sr7_hlti_bpf_tap157: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0,signed
23:16	RW	-7	reg_sr7_hlti_bpf_tap156: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0,signed
15:8	RW	1	reg_sr7_hlti_bpf_tap155: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0,signed
7:0	RW	-21	reg_sr7_hlti_bpf_tap154: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0,signed

Table 9-1811 SRSHARP0_SR7_HCTIBPF_TAP0 0x510e

Bit(s)	R/W	Default	Description
31:24	RW	0	reg_sr7_clti_bpf_tap153: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed
23:16	RW	-34	reg_sr7_clti_bpf_tap152: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed

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Bit(s)	R/W	Default	Description
15:8	RW	-1	reg_sr7_clti_bpf_tap151: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed
7:0	RW	120	reg_sr7_clti_bpf_tap150: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed

Table 9-1812 SRSHARP0_SR7_HCTIBPF_TAP1 0x510f

Bit(s)	R/W	Default	Description
31:24	RW	2	reg_sr7_clti_bpf_tap157: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed
23:16	RW	-7	reg_sr7_clti_bpf_tap156: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed
15:8	RW	1	reg_sr7_clti_bpf_tap155: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed
7:0	RW	-21	reg_sr7_clti_bpf_tap154: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed

Table 9-1813 SRSHARP0_SR7_PKLONGBPF_HTAP0 0x5110

Bit(s)	R/W	Default	Description
31:24	RW	-24	reg_sr7_pk_long_bpf_hztap153: tap15 BPF for horizontal peaking filter, only store half of the filter,signed
23:16	RW	-19	reg_sr7_pk_long_bpf_hztap152: tap15 BPF for horizontal peaking filter, only store half of the filter,signed
15:8	RW	31	reg_sr7_pk_long_bpf_hztap151: tap15 BPF for horizontal peaking filter, only store half of the filter,signed
7:0	RW	66	reg_sr7_pk_long_bpf_hztap150: tap15 BPF for horizontal peaking filter, only store half of the filter ,signed

Table 9-1814 SRSHARP0_SR7_PKLONGBPF_HTAP1 0x5111

Bit(s)	R/W	Default	Description
31:24	RW	-6	reg_sr7_pk_long_bpf_hztap157: tap15 BPF for horizontal peaking filter, only store half of the filter,signed
23:16	RW	-10	reg_sr7_pk_long_bpf_hztap156: tap15 BPF for horizontal peaking filter, only store half of the filter,signed
15:8	RW	-1	reg_sr7_pk_long_bpf_hztap155: tap15 BPF for horizontal peaking filter, only store half of the filter,signed
7:0	RW	-4	reg_sr7_pk_long_bpf_hztap154: tap15 BPF for horizontal peaking filter, only store half of the filter,signed

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Table 9-1815 SRSHARP0_SR7_PKLONGHPF_HTAP0 0x5112

Bit(s)	R/W	Default	Description
31:24	RW	27	reg_sr7_pk_long_hpf_hztap153: tap15 HPF for horizontal peaking filter, only store half of the filter,signed
23:16	RW	-15	reg_sr7_pk_long_hpf_hztap152: tap15 HPF for horizontal peaking filter, only store half of the filter,signed
15:8	RW	-32	reg_sr7_pk_long_hpf_hztap151: tap15 HPF for horizontal peaking filter, only store half of the filter,signed
7:0	RW	58	reg_sr7_pk_long_hpf_hztap150: tap15 HPF for horizontal peaking filter, only store half of the filter,signed

Table 9-1816 SRSHARP0_SR7_PKLONGHPF_HTAP1 0x5113

Bit(s)	R/W	Default	Description
31:24	RW	8	reg_sr7_pk_long_hpf_hztap157: tap15 HPF for horizontal peaking filter, only store half of the filter,signed
23:16	RW	-6	reg_sr7_pk_long_hpf_hztap156: tap15 HPF for horizontal peaking filter, only store half of the filter,signed
15:8	RW	-1	reg_sr7_pk_long_hpf_hztap155: tap15 HPF for horizontal peaking filter, only store half of the filter,signed
7:0	RW	-10	reg_sr7_pk_long_hpf_hztap154: tap15 HPF for horizontal peaking filter, only store half of the filter,signed

Table 9-1817 SRSHARP0_SR7_VLTIBPF_TAP0 0x5114

Bit(s)	R/W	Default	Description
31:24	RW	0	reg_sr7_vlti_bpf_tap093: tap09 BPF for vlti (gain3), only store half of the filter, signed
23:16	RW	-41	reg_sr7_vlti_bpf_tap092: tap09 BPF for vlti (gain3), only store half of the filter, signed
15:8	RW	0	reg_sr7_vlti_bpf_tap091: tap09 BPF for vlti (gain3), only store half of the filter, signed
7:0	RW	126	reg_sr7_vlti_bpf_tap090: tap09 BPF for vlti (gain3), only store half of the filter, signed

Table 9-1818 SRSHARP0_SR7_VLTIBPF_TAP1 0x5115

Bit(s)	R/W	Default	Description
31:8			reserved
7:0	RW	-22	reg_sr7_vlti_bpf_tap094: tap09 BPF for vlti (gain3), only store half of the filter, signed

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Table 9-1819 SRSHARP0_SR7_VCTIBPF_TAP0 0x5116

Bit(s)	R/W	Default	Description
31:24	RW	0	reg_sr7_vcti_bpf_tap093: tap09 BPF for vcti (gain3), only store half of the filter, signed
23:16	RW	-41	reg_sr7_vcti_bpf_tap092: tap09 BPF for vcti (gain3), only store half of the filter, signed
15:8	RW	0	reg_sr7_vcti_bpf_tap091: tap09 BPF for vcti (gain3), only store half of the filter, signed
7:0	RW	126	reg_sr7_vcti_bpf_tap090: tap09 BPF for vcti (gain3), only store half of the filter, signed

Table 9-1820 SRSHARP0_SR7_VCTIBPF_TAP1 0x5117

Bit(s)	R/W	Default	Description
31:8			reserved
7:0	RW	-22	reg_sr7_vcti_bpf_tap094: tap09 BPF for vcti (gain3), only store half of the filter,, signed

Table 9-1821 SRSHARP0_SR7_PKLONGBPF_VTAP0 0x5118

Bit(s)	R/W	Default	Description
31:24	RW	-32	reg_sr7_pk_long_bpf_vdtap093: tap09 BPF for vertical and diagonal peaking filter,signed
23:16	RW	-28	reg_sr7_pk_long_bpf_vdtap092: tap09 BPF for vertical and diagonal peaking filter,signed
15:8	RW	30	reg_sr7_pk_long_bpf_vdtap091: tap09 BPF for vertical and diagonal peaking filter,signed
7:0	RW	68	reg_sr7_pk_long_bpf_vdtap090: tap09 BPF for vertical and diagonal peaking filter,signed

Table 9-1822 SRSHARP0_SR7_PKLONGBPF_VTAP1 0x5119

Bit(s)	R/W	Default	Description
31:8			reserved
7:0	RW	-4	reg_sr7_pk_long_bpf_vdtap094: tap09 BPF for vertical and diagonal peaking filter,signed

Table 9-1823 SRSHARP0_SR7_PKLONGHPF_VTAP0 0x511a

Bit(s)	R/W	Default	Description
31:24	RW	30	reg_sr7_pk_long_hpf_vdtap093: tap09 HPF for vertical and diagonal peaking filter,signed
23:16	RW	-28	reg_sr7_pk_long_hpf_vdtap092: tap09 HPF for vertical and diagonal peaking filter,signed

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Bit(s)	R/W	Default	Description
15:8	RW	-31	reg_sr7_pk_long_hpf_vdtap091: tap09 HPF for vertical and diagonal peaking filter,signed
7:0	RW	68	reg_sr7_pk_long_hpf_vdtap090: tap09 HPF for vertical and diagonal peaking filter,signed

Table 9-1824 SRSHARP0_SR7_PKLONGHPF_VTAP1 0x511b

Bit(s)	R/W	Default	Description
31:8			reserved
7:0	RW	-5	reg_sr7_pk_long_hpf_vdtap094: tap09 HPF for vertical and diagonal peaking filter,signed

Table 9-1825 SRSHARP0_SR7_CIRBPLONG_ALP 0x511c

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	15	reg_sr7_cirbp_long_alpha3: alpha to blend bp_long to the cirpk filter corresponding angle (0/45/90/135)
11:8	RW	15	reg_sr7_cirbp_long_alpha2: alpha to blend bp_long to the cirpk filter corresponding angle (0/45/90/135)
7:4	RW	15	reg_sr7_cirbp_long_alpha1: alpha to blend bp_long to the cirpk filter corresponding angle (0/45/90/135)
3:0	RW	15	reg_sr7_cirbp_long_alpha0: alpha to blend bp_long to the cirpk filter corresponding angle (0/45/90/135)

Table 9-1826 SRSHARP0_SR7_CIRHPLONG_ALP 0x511d

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	15	reg_sr7_cirhp_long_alpha3: alpha to blend hp_long to the cirpk filter corresponding angle (0/45/90/135)
11:8	RW	15	reg_sr7_cirhp_long_alpha2: alpha to blend hp_long to the cirpk filter corresponding angle (0/45/90/135)
7:4	RW	15	reg_sr7_cirhp_long_alpha1: alpha to blend hp_long to the cirpk filter corresponding angle (0/45/90/135)
3:0	RW	15	reg_sr7_cirhp_long_alpha0: alpha to blend hp_long to the cirpk filter corresponding angle (0/45/90/135)

Table 9-1827 SRSHARP0_SR7_DRTBPLONG_ALP 0x511e

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	15	reg_sr7_drtbp_long_alpha3: alpha to blend bp_long to the drtpk filter corresponding angle (0/45/90/135)

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Bit(s)	R/W	Default	Description
11:8	RW	15	reg_sr7_drtbp_long_alpha2: alpha to blend bp_long to the drtpk filter corresponding angle (0/45/90/135)
7:4	RW	15	reg_sr7_drtbp_long_alpha1: alpha to blend bp_long to the drtpk filter corresponding angle (0/45/90/135)
3:0	RW	15	reg_sr7_drtbp_long_alpha0: alpha to blend bp_long to the drtpk filter corresponding angle (0/45/90/135)

Table 9-1828 SRSHARP0_SR7_DRTHPLONG_ALP 0x511f

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	15	reg_sr7_drthp_long_alpha3: alpha to blend hp_long to the drtpk filter corresponding angle (0/45/90/135)
11:8	RW	15	reg_sr7_drthp_long_alpha2: alpha to blend hp_long to the drtpk filter corresponding angle (0/45/90/135)
7:4	RW	15	reg_sr7_drthp_long_alpha1: alpha to blend hp_long to the drtpk filter corresponding angle (0/45/90/135)
3:0	RW	15	reg_sr7_drthp_long_alpha0: alpha to blend hp_long to the drtpk filter corresponding angle (0/45/90/135)

Table 9-1829 SRSHARP0_SR7_PKMINMAXCIR_BLD_LUT2D0 0x5120

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_pk_mimaxerr2_cirbld_lut2d7
27:24	RW	0	reg_sr7_pk_mimaxerr2_cirbld_lut2d6
23:20	RW	2	reg_sr7_pk_mimaxerr2_cirbld_lut2d5
19:16	RW	2	reg_sr7_pk_mimaxerr2_cirbld_lut2d4
15:12	RW	4	reg_sr7_pk_mimaxerr2_cirbld_lut2d3
11:8	RW	6	reg_sr7_pk_mimaxerr2_cirbld_lut2d2
7:4	RW	12	reg_sr7_pk_mimaxerr2_cirbld_lut2d1
3:0	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d0: 2D-LUT for alpha2 for cir-PK blender,larger coef means less drt-pk, x-min_err, y-max_err

Table 9-1830 SRSHARP0_SR7_PKMINMAXCIR_BLD_LUT2D1 0x5121

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d15
27:24	RW	0	reg_sr7_pk_mimaxerr2_cirbld_lut2d14
23:20	RW	2	reg_sr7_pk_mimaxerr2_cirbld_lut2d13
19:16	RW	2	reg_sr7_pk_mimaxerr2_cirbld_lut2d12
15:12	RW	4	reg_sr7_pk_mimaxerr2_cirbld_lut2d11
11:8	RW	6	reg_sr7_pk_mimaxerr2_cirbld_lut2d10

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Bit(s)	R/W	Default	Description
7:4	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d9
3:0	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d8

Table 9-1831 SRSHARP0_SR7_PKMINMAXCIR_BLD_LUT2D2 0x5122

Bit(s)	R/W	Default	Description
31:28	RW	6	reg_sr7_pk_mimaxerr2_cirbld_lut2d23
27:24	RW	10	reg_sr7_pk_mimaxerr2_cirbld_lut2d22
23:20	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d21
19:16	RW	2	reg_sr7_pk_mimaxerr2_cirbld_lut2d20
15:12	RW	2	reg_sr7_pk_mimaxerr2_cirbld_lut2d19
11:8	RW	4	reg_sr7_pk_mimaxerr2_cirbld_lut2d18
7:4	RW	6	reg_sr7_pk_mimaxerr2_cirbld_lut2d17
3:0	RW	12	reg_sr7_pk_mimaxerr2_cirbld_lut2d16

Table 9-1832 SRSHARP0_SR7_PKMINMAXCIR_BLD_LUT2D3 0x5123

Bit(s)	R/W	Default	Description
31:28	RW	14	reg_sr7_pk_mimaxerr2_cirbld_lut2d31
27:24	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d30
23:20	RW	4	reg_sr7_pk_mimaxerr2_cirbld_lut2d29
19:16	RW	8	reg_sr7_pk_mimaxerr2_cirbld_lut2d28
15:12	RW	10	reg_sr7_pk_mimaxerr2_cirbld_lut2d27
11:8	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d26
7:4	RW	2	reg_sr7_pk_mimaxerr2_cirbld_lut2d25
3:0	RW	4	reg_sr7_pk_mimaxerr2_cirbld_lut2d24

Table 9-1833 SRSHARP0_SR7_PKMINMAXCIR_BLD_LUT2D4 0x5124

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d35
11:8	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d34
7:4	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d33
3:0	RW	12	reg_sr7_pk_mimaxerr2_cirbld_lut2d32

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Table 9-1834 SRSHARP0_SR7_PKMINMAXLPF_BLD_LUT2D0 0x5125

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_pk_mimaxerr2_lpfbld_lut2d7
27:24	RW	0	reg_sr7_pk_mimaxerr2_lpfbld_lut2d6
23:20	RW	2	reg_sr7_pk_mimaxerr2_lpfbld_lut2d5
19:16	RW	2	reg_sr7_pk_mimaxerr2_lpfbld_lut2d4
15:12	RW	4	reg_sr7_pk_mimaxerr2_lpfbld_lut2d3
11:8	RW	6	reg_sr7_pk_mimaxerr2_lpfbld_lut2d2
7:4	RW	12	reg_sr7_pk_mimaxerr2_lpfbld_lut2d1
3:0	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d0: 2D-LUT for alpha2 for PK lpf along edge blender, lareger coef means less lpf along edge,x-min_err, y-max_err

Table 9-1835 SRSHARP0_SR7_PKMINMAXLPF_BLD_LUT2D1 0x5126

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d15
27:24	RW	0	reg_sr7_pk_mimaxerr2_lpfbld_lut2d14
23:20	RW	2	reg_sr7_pk_mimaxerr2_lpfbld_lut2d13
19:16	RW	2	reg_sr7_pk_mimaxerr2_lpfbld_lut2d12
15:12	RW	4	reg_sr7_pk_mimaxerr2_lpfbld_lut2d11
11:8	RW	6	reg_sr7_pk_mimaxerr2_lpfbld_lut2d10
7:4	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d9
3:0	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d8

Table 9-1836 SRSHARP0_SR7_PKMINMAXLPF_BLD_LUT2D2 0x5127

Bit(s)	R/W	Default	Description
31:28	RW	6	reg_sr7_pk_mimaxerr2_lpfbld_lut2d23
27:24	RW	10	reg_sr7_pk_mimaxerr2_lpfbld_lut2d22
23:20	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d21
19:16	RW	2	reg_sr7_pk_mimaxerr2_lpfbld_lut2d20
15:12	RW	2	reg_sr7_pk_mimaxerr2_lpfbld_lut2d19
11:8	RW	4	reg_sr7_pk_mimaxerr2_lpfbld_lut2d18
7:4	RW	6	reg_sr7_pk_mimaxerr2_lpfbld_lut2d17
3:0	RW	12	reg_sr7_pk_mimaxerr2_lpfbld_lut2d16

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Table 9-1837 SRSHARP0_SR7_PKMINMAXLPF_BLD_LUT2D3 0x5128

Bit(s)	R/W	Default	Description
31:28	RW	14	reg_sr7_pk_mimaxerr2_lpfbld_lut2d31
27:24	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d30
23:20	RW	4	reg_sr7_pk_mimaxerr2_lpfbld_lut2d29
19:16	RW	8	reg_sr7_pk_mimaxerr2_lpfbld_lut2d28
15:12	RW	10	reg_sr7_pk_mimaxerr2_lpfbld_lut2d27
11:8	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d26
7:4	RW	2	reg_sr7_pk_mimaxerr2_lpfbld_lut2d25
3:0	RW	4	reg_sr7_pk_mimaxerr2_lpfbld_lut2d24

Table 9-1838 SRSHARP0_SR7_PKMINMAXLPF_BLD_LUT2D4 0x5129

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d35
11:8	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d34
7:4	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d33
3:0	RW	12	reg_sr7_pk_mimaxerr2_lpfbld_lut2d32

Table 9-1839 SRSHARP0_SR7_PKDRT_BLD_EN 0x512a

Bit(s)	R/W	Default	Description
31:1			reserved
0	RW	0	reg_sr7_pkdrtbld_beta_en: enable of direction ambiguity protection for drt and cir blend

Table 9-1840 SRSHARP0_SR7_DRTDIF_TH 0x512b

Bit(s)	R/W	Default	Description
31:16			reserved
15::8	RW	128	reg_sr7_drtdif_min2sad_th1
7:0	RW	128	reg_sr7_drtdif_min2sad_th0:for min2_sad threshold for ambiguilty ignoring

Table 9-1841 SRSHARP0_SR7_TIBLD_PRT 0x512c

Bit(s)	R/W	Default	Description
31:16			reserved
13	RW	1	reg_sr7_hlti_dcbld_beta_en:enable of denoise protection for dc org and denoise blend
12	RW	1	reg_sr7_vlti_dcbld_beta_en:enable of denoise protection for dc org and denoise blend

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Bit(s)	R/W	Default	Description
11:8	RW	0	reg_sr7_xcti_dcbld_beta1:beta for denoise and org dc blend base on the x=cal_drt_dif4(min_idx,min2_idx)
7:4	RW	15	reg_sr7_xcti_dcbld_beta0:beta for denoise and org dc blend base on the x=cal_drt_dif4(min_idx,min2_idx)
3	RW	1	reg_sr7_hcti_dcbld_beta_en:enable of denoise protection for dc org and denoise blend
2	RW	1	reg_sr7_vcti_dcbld_beta_en:enable of denoise protection for dc org and denoise blend
1	RW	0	reg_sr7_hcti_dcbld_use_ybeta:enable to use beta from hlti
0	RW	0	reg_sr7_vcti_dcbld_use_ybeta:enable to use beta from vlti

Table 9-1842 SRSHARP0_SR7_HTI_OPT_FORCE 0x512d

Bit(s)	R/W	Default	Description
31:6			reserved
5	RW	1	reg_sr7_diag_force_hti1force hti: for diagonal edges luma/chroma, 0: diagonal use vti, 1: diagonal use hti
4	RW	1	reg_sr7_diag_force_hti0:force hti for diagonal edges luma/chroma, 0: diagonal use vti, 1: diagonal use hti
3	RW	1	reg_sr7_horz_force_vti1:force vti for horizontal edges luma/chroma, 0: bias hti, 1: horizontal edge force 100% vti
2	RW	1	reg_sr7_horz_force_vti0:force vti for horizontal edges luma/chroma, 0: bias hti, 1: horizontal edge force 100% vti
1	RW	1	reg_sr7_alph_force_hvsad1:alpha = minsad*64/maxsad, force minsad=sad_h, maxsad=sad_v for alpha calculation
0	RW	1	reg_sr7_alph_force_hvsad0:alpha = minsad*64/maxsad, force minsad=sad_h, maxsad=sad_v for alpha calculation,[0]for luma, [1] for chroma

Table 9-1843 SRSHARP0_SR7_HVTI_FINALGAIN 0x512e

Bit(s)	R/W	Default	Description
31:28			reserved
27:16	RW	256	reg_sr7_hvti_finalgain1: final gain for HVTI boost, for easier level tunning for application
15:12			reserved
11:0	RW	256	reg_sr7_hvti_finalgain0: final gain for HVTI boost, for easier level tunning for application

Table 9-1844 SRSHARP0_SR7_TIOS_SDRATIO 0x512f

Bit(s)	R/W	Default	Description
31:30			reserved
29:24	RW	3	reg_sr7_hti_osmargin_sdratio1:ratio for HTI OS margin adaptive to sd
23:22			reserved

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Bit(s)	R/W	Default	Description
21:16	RW	3	reg_sr7_hti_osmargin_sdratio0:ratio for HTI OS margin adaptive to sd
15:14			reserved
13:8	RW	3	reg_sr7_vti_osmargin_sdratio1:ratio for VTI OS margin adaptive to sd
7:6			reserved
5:0	RW	3	reg_sr7_vti_osmargin_sdratio0:ratio for VTI OS margin adaptive to sd

Table 9-1845 SRSHARP0_SR7_XTI_SDFDEN 0x5130

Bit(s)	R/W	Default	Description
31:1			reserved
1	RW	1	reg_sr7_xtigain_sdfd_en1: adaptive gamma for cti boost gain enable.
0	RW	1	reg_sr7_xtigain_sdfd_en0: adaptive gamma for cti boost gain enable.[0]for luma, [1] for chroma

Table 9-1846 SRSHARP0_SR7_FDSD_PARAM 0x5131

Bit(s)	R/W	Default	Description
31:26			reserved
25	RW	1	reg_fdsd_vlpf_en:use vertical [1 2 1] lpf filter for the fd and sd derivativecalculations
24	RW	1	reg_fdsd_hlpf_en:use horizontal [1 2 1] lpf filter for the fd and sd derivativecalculations
23:20	RW	0	reg_sd_coring_th1:coring to SD'= MAX(SD - FD*ratio - coring,0)
19:16	RW	0	reg_sd_coring_th0:coring to SD'= MAX(SD - FD*ratio - coring,0)
15:14			reserved
13:8	RW	4	reg_sd_coring_ratio2fd1:ratio to FD for adaptive coring to SD'= MAX(SD - FD*ratio - coring,0)
7:6			reserved
5:0	RW	4	reg_sd_coring_ratio2fd0:ratio to FD for adaptive coring to SD'= MAX(SD - FD*ratio - coring,0)

Table 9-1847 SRSHARP0_SR7_TI_BPF_EN 0x5132

Bit(s)	R/W	Default	Description
31:4			reserved
3	RW	1	reg_sr7_hlti_bpf_en:enable of tap09 BPF for hlti (gain3), only store half of the filter
2	RW	1	reg_sr7_hcti_bpf_en:enable of tap09 BPF for hcti (gain3), only store half of the filter
1	RW	1	reg_sr7_vlti_bpf_en:enable of tap09 BPF for vcti (gain3), only store half of the filter
0	RW	1	reg_sr7_vcti_bpf_en:enable of tap09 BPF for vlti (gain3), only store half of the filter

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Table 9-1848 SRSHARP0_SR7_PKLONG_PF_EN 0x5133

Bit(s)	R/W	Default	Description
31:2			reserved
1	RW	1	reg_sr7_pk_long_bpf_en:enable of long BPF for peaking
0	RW	1	reg_sr7_pk_long_hpf_en:enable of long HPF for peaking

Table 9-1849 SRSHARP0_SR7_PKLONG_PF_GAIN 0x5134

Bit(s)	R/W	Default	Description
31:24	RW	64	reg_sr7_pk_long_bpf_hzgain:gain to long horizontal BPF for peaking
23:16	RW	64	reg_sr7_pk_long_bpf_vdgain:gain to long vertical and diagonal BPF for peaking
15:8	RW	64	reg_sr7_pk_long_hpf_hzgain:gain to long horizontal HPF for peaking
7:0	RW	64	reg_sr7_pk_long_hpf_vdgain:gain to long vertical and diagonal HPF for peaking

Table 9-1850 SRSHARP0_SR7_PKMINMAX_BLD 0x5135

Bit(s)	R/W	Default	Description
31:4			reserved
3	RW	1	reg_sr7_pk_mimaxerr2_cirbld_on_bp:enable to use adaptive blender of drtBP vs cirBP alpha2, the larger of cell, the more cirPK results, 0: alp2=lut2d(minerr, maxerr),1:alp2=min_err/maxerr
2	RW	1	reg_sr7_pk_mimaxerr2_cirbld_on_hp:enable to use adaptive blender of drtHP vs cirHP alpha2, the larger of cell, the more cirPK results, 0: alp2=lut2d(minerr, maxerr),1:alp2=min_err/maxerr
1	RW	1	reg_sr7_pk_mimaxerr2_lpfbld_on_bp:enable to use adaptive blender of BP result lpf along edge based on the mimaxsad relationship
0	RW	1	reg_sr7_pk_mimaxerr2_lpfbld_on_hp:enable to use adaptive blender of HP result lpf along edge based on the mimaxsad relationship

Table 9-1851 SRSHARP0_SR7_TI_CONMAXERR_GAIN 0x5136

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	8	reg_sr7_hti_conmaxerr_gain1:con=max(con, maxerr) for the horizontal transition calculation, gain=0, same as s6 and prev, [0] for y and [1] for uv
11:8	RW	8	reg_sr7_hti_conmaxerr_gain0:con=max(con, maxerr) for the horizontal transition calculation, gain=0, same as s6 and prev, [0] for y and [1] for uv
7:4	RW	8	reg_sr7_vti_conmaxerr_gain1:con=max(con, maxerr) for the vertical transition calculation, gain=0, same as s6 and prev, [0] for y and [1] for uv
3:0	RW	8	reg_sr7_vti_conmaxerr_gain0:con=max(con, maxerr) for the vertical transition calculation, gain=0, same as s6 and prev, [0] for y and [1] for uv

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Table 9-1852 SRSHARP0_SR7_CC_PK_ADJ 0x5137

Bit(s)	R/W	Default	Description
31:25			reserved
24	RW	1	reg_sr7_cc_enable:color compensation enable, 0: no CC, 1: with CC
23:22			reserved
21:20	RW	0	reg_sr7_cc_yinp_sel:color compensation input luma selection, 0: org_y; 1: gau_y ; 2:gauadp_y; 3:edgeadp_y (same as dnlp input sel)
19:18	RW	2	reg_sr7_cc_ydlt_sel:color compensation output luma selection, 0: peaking+lti output; 1: dnlp output; 2/3: peaking+lti+dnlp
17:16	RW	1	reg_sr7_cc_sat_norm:normalization of lut cell to saturation. 0: norm to 8 as 1.0, sat[0:23/8]; 1: norm to 16 as 1.0, sat[1/16:31/16]; 2: norm to 32 as 1.0, sat[17/32:47/32]; 3:norm to 64 as 1.0, sat[49/64:79/64]
15:8	RW	64	reg_sr7_cc_ydlt_pscl:prescale to the y-delta (if > 0) before feeding to y-lumadlt, normalized 64 as 1.0
7:0	RW	64	reg_sr7_cc_ydlt_nscl:prescale to the y-delta (if < 0) before feeding to y-lumadlt, normalized 64 as 1.0

Table 9-1853 SRSHARP0_SR7_CC_LUT0 0x5138

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_cc_lut103:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=0
27:24	RW	0	reg_sr7_cc_lut102:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=0
23:20	RW	0	reg_sr7_cc_lut001:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=0
19:16	RW	0	reg_sr7_cc_lut000:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=0
15:12	RW	8	reg_sr7_cc_lut103:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=1/8
11:8	RW	4	reg_sr7_cc_lut102:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=1/8
7:4	RW	2	reg_sr7_cc_lut101:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=1/8
3:0	RW	1	reg_sr7_cc_lut100:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=1/8

Table 9-1854 SRSHARP0_SR7_CC_LUT1 0x5139

Bit(s)	R/W	Default	Description
31:28			reserved
27:24	RW	12	reg_sr7_cc_lut202:valid for y-lumadlt= 1/4, 1/2, 3/4; of x-lumainput=2/8
23:20	RW	8	reg_sr7_cc_lut201:valid for y-lumadlt= 1/4, 1/2, 3/4; of x-lumainput=2/8
19:16	RW	4	reg_sr7_cc_lut200:valid for y-lumadlt= 1/4, 1/2, 3/4; of x-lumainput=2/8
15:12			reserved
11:8	RW	15	reg_sr7_cc_lut302:valid for y-lumadlt= 1/4, 1/2, 3/4; of x-lumainput=3/8
7:4	RW	10	reg_sr7_cc_lut301:valid for y-lumadlt= 1/4, 1/2, 3/4; of x-lumainput=3/8
3:0	RW	5	reg_sr7_cc_lut300:valid for y-lumadlt= 1/4, 1/2, 3/4; of x-lumainput=3/8

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Table 9-1855 SRSHARP0_SR7_CC_LUT2 0x513a

Bit(s)	R/W	Default	Description
31:24			reserved
23:20	RW	15	reg_sr7_cc_lut401:valid for y-lumadlt= 1/4, 1/2 ; of x-lumainput=4/8
19:16	RW	8	reg_sr7_cc_lut400:valid for y-lumadlt= 1/4, 1/2; of x-lumainput=4/8
15:12	RW	13	reg_sr7_cc_lut501:valid for y-lumadlt= 1/4, 1/2; of x-lumainput=5/8
11:8	RW	6	reg_sr7_cc_lut500:valid for y-lumadlt= 1/4, 1/2; of x-lumainput=5/8
7:4	RW	5	reg_sr7_cc_lut600:valid for y-lumadlt= 1/4 of x-lumainput=6/8
3:0	RW	4	reg_sr7_cc_lut700:valid for y-lumadlt= 1/4 of x-lumainput=7/8

Table 9-1856 SRSHARP0_SR7_CC_LUT3 0x513b

Bit(s)	R/W	Default	Description
31:24			reserved
23:20	RW	4	reg_sr7_cc_lut710:valid for y-lumadlt= -1/4,; of x-lumainput=1/8
19:16	RW	5	reg_sr7_cc_lut610:valid for y-lumadlt= -1/4,; of x-lumainput=2/8
15:12	RW	13	reg_sr7_cc_lut511:valid for y-lumadlt= -1/4, -1/2; of x-lumainput=3/8
11:8	RW	6	reg_sr7_cc_lut510:valid for y-lumadlt= -1/4, -1/2; of x-lumainput=3/8
7:4	RW	15	reg_sr7_cc_lut411:valid for y-lumadlt= -1/4, -1/2 of x-lumainput=4/8
3:0	RW	8	reg_sr7_cc_lut410:valid for y-lumadlt= -1/4 , -1/2 of x-lumainput=4/8

Table 9-1857 SRSHARP0_SR7_CC_LUT4 0x513c

Bit(s)	R/W	Default	Description
31:24			reserved
23:20	RW	15	reg_sr7_cc_lut312:valid for y-lumadlt= -1/4,-1/2, -3/4; of x-lumainput=5/8
19:16	RW	10	reg_sr7_cc_lut311:valid for y-lumadlt= -1/4,-1/2, -3/4; of x-lumainput=5/8
15:12	RW	5	reg_sr7_cc_lut310:valid for y-lumadlt= -1/4,-1/2, -3/4; of x-lumainput=5/8
11:8	RW	12	reg_sr7_cc_lut212:valid for y-lumadlt= -1/4, -1/2, -3/4;; of x-lumainput=6/8
7:4	RW	8	reg_sr7_cc_lut211:valid for y-lumadlt= -1/4, -1/2, -3/4; of x-lumainput=6/8
3:0	RW	4	reg_sr7_cc_lut210:valid for y-lumadlt= -1/4, -1/2, -3/4; of x-lumainput=6/8

Table 9-1858 SRSHARP0_SR7_CC_LUT5 0x513d

Bit(s)	R/W	Default	Description
31:28	RW	8	reg_sr7_cc_lut113:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=7/8
27:24	RW	4	reg_sr7_cc_lut112:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=7/8
23:20	RW	2	reg_sr7_cc_lut111:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=7/8
19:16	RW	1	reg_sr7_cc_lut110:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=7/8

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Bit(s)	R/W	Default	Description
15:12	RW	0	reg_sr7_cc_lut013:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=8/8
11:8	RW	0	reg_sr7_cc_lut012:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=8/8
7:4	RW	0	reg_sr7_cc_lut011:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=8/8
3:0	RW	0	reg_sr7_cc_lut010:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=8/8

Table 9-1859 SRSHARP0_SR7_GRAPHIC_CTRL 0x513e

Bit(s)	R/W	Default	Description
31:11			reserved
10	RW	1	reg_sr7_grph_en:enable graphic statistic
9	RW	1	reg_sr7_grph_hflt:horizontal filter, 0: [0 1 -1], 1: [-1 2 -1]
8	RW	1	reg_sr7_grph_vflt: vertical filter, 0: [0 1 -1], 1: [-1 2 -1]
7:0	RW	0	reg_sr7_grph_dif_cor:coring for dif while count for graphic

Table 9-1860 SRSHARP0_SR7_GRAPHIC_THD_GAIN 0x513f

Bit(s)	R/W	Default	Description
31:24	RW	2	reg_sr7_grph_flt_thd: flat threshold for dif while count for graphic.
23:16	RW	40	reg_sr7_grph_dtl_thd:detail threshold for dif while count for graphic
15:8	RW	32	reg_sr7_grph_hgain:horizontal gain for fast squart of hp
7:0	RW	32	reg_sr7_grph_vgain:vertical gain for fast squart of hp

Table 9-1861 SRSHARP0_SR7_RO_GRAPHIC_FLT_CNT 0x5140

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_sr7_grph_flt_cnt:: flat count numbers for graphic

Table 9-1862 SRSHARP0_SR7_RO_GRAPHIC_DTL_CNT 0x5141

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_sr7_grph_dtl_cnt::detail count numbers for graphic

Table 9-1863 SRSHARP0_SR7_CLR_PRT_PARAM 0x5142

Bit(s)	R/W	Default	Description
31:18			reserved
17:16	RW	3	reg_sr7_clr_prct_inpsel:input UV selection for color protection, 0: org; 1: NRout; 2: CTIout; 3: (NR+TIout)/2

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Bit(s)	R/W	Default	Description
15:8	RW	64	reg_sr7_clr_prct_dnlp_gain:gain to de-boost of dnlp_dlt base on color region, norm to 64 as 1.0. set to 0 as disable.
7:0	RW	64	reg_sr7_clr_prct_peak_gain:gain to de-boost of peak_dlt base on color region, norm to 64 as 1.0, set to 0 as disable

Table 9-1864 SRSHARP0_SR7_CLR_PRT_LC_GAIN 0x5143

Bit(s)	R/W	Default	Description
31:24			reserved
23:16	RW	64	reg_sr7_clr_prct_lc_gain2:gain to de-boost of lc_dlt (y/u/v) base on color region, norm to 64 as 1.0, set to 0 as disable
15:8	RW	64	reg_sr7_clr_prct_lc_gain1:gain to de-boost of lc_dlt (y/u/v) base on color region, norm to 64 as 1.0, set to 0 as disable
7:0	RW	64	reg_sr7_clr_prct_lc_gain0:gain to de-boost of lc_dlt (y/u/v) base on color region, norm to 64 as 1.0, set to 0 as disable

Table 9-1865 SRSHARP0_SR7_CLR_PRT_LUT0 0x5144

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut7:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut6:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut5:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut4:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut3:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut2:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut1:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut0:color protection lut, 16 is normalized to 1

Table 9-1866 SRSHARP0_SR7_CLR_PRT_LUT1 0x5145

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut15:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut14:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut13:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut12:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut11:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut10:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut9:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut8:color protection lut, 16 is normalized to 1

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Table 9-1867 SRSHARP0_SR7_CLR_PRT_LUT2 0x5146

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut23:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut22:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut21:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut20:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut19:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut18:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut17:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut16:color protection lut, 16 is normalized to 1

Table 9-1868 SRSHARP0_SR7_CLR_PRT_LUT3 0x5147

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut31:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut30:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut29:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut28:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut27:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut26:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut25:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut24:color protection lut, 16 is normalized to 1

Table 9-1869 SRSHARP0_SR7_CLR_PRT_LUT4 0x5148

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut39:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut38:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut37:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut36:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut35:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut34:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut33:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut32:color protection lut, 16 is normalized to 1

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Table 9-1870 SRSHARP0_SR7_CLR_PRT_LUT5 0x5149

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut47:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut46:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut45:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut44:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut43:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut42:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut41:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut40:color protection lut, 16 is normalized to 1

Table 9-1871 SRSHARP0_SR7_CLR_PRT_LUT6 0x514a

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut55:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut54:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut53:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut52:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut51:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut50:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut49:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut48:color protection lut, 16 is normalized to 1

Table 9-1872 SRSHARP0_SR7_CLR_PRT_LUT7 0x514b

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut63:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut62:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut61:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut60:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut59:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut58:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut57:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut56:color protection lut, 16 is normalized to 1

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Table 9-1873 SRSHARP0_SR7_CLR_PRT_LUT8 0x514c

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut71:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut70:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut69:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut68:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut67:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut66:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut65:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut64:color protection lut, 16 is normalized to 1

Table 9-1874 SRSHARP0_SR7_CLR_PRT_LUT9 0x514d

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut79:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut78:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut77:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut76:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut75:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut74:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut73:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut72:color protection lut, 16 is normalized to 1

Table 9-1875 SRSHARP0_SR7_CLR_PRT_LUT10 0x514e

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut87:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut86:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut85:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut84:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut83:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut82:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut81:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut80:color protection lut, 16 is normalized to 1

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Table 9-1876 SRSHARP0_SR7_CLR_PRT_LUT11 0x514f

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut95:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut94:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut93:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut92:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut91:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut90:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut89:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut88:color protection lut, 16 is normalized to 1

Table 9-1877 SRSHARP0_SR7_CLR_PRT_LUT12 0x5150

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut103:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut102:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut101:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut100:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut99:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut98:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut97:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut96:color protection lut, 16 is normalized to 1

Table 9-1878 SRSHARP0_SR7_CLR_PRT_LUT13 0x5151

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut111:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut110:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut109:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut108:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut107:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut106:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut105:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut104:color protection lut, 16 is normalized to 1

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Table 9-1879 SRSHARP0_SR7_CLR_PRT_LUT14 0x5152

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut119:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut118:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut117:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut116:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut115:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut114:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut113:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut112:color protection lut, 16 is normalized to 1

Table 9-1880 SRSHARP0_SR7_CLR_PRT_LUT15 0x5153

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut127:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut126:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut125:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut124:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut123:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut122:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut121:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut120:color protection lut, 16 is normalized to 1

Table 9-1881 SRSHARP0_SR7_CLR_PRT_LUT16 0x5154

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut135:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut134:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut133:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut132:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut131:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut130:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut129:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut128:color protection lut, 16 is normalized to 1

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Table 9-1882 SRSHARP0_SR7_CLR_PRT_LUT17 0x5155

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut143:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut142:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut141:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut140:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut139:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut138:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut137:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut136:color protection lut, 16 is normalized to 1

Table 9-1883 SRSHARP0_SR7_CLR_PRT_LUT18 0x5156

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut151:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut150:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut149:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut148:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut147:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut146:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut145:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut144:color protection lut, 16 is normalized to 1

Table 9-1884 SRSHARP0_SR7_CLR_PRT_LUT19 0x5157

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut159:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut158:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut157:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut156:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut155:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut154:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut153:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut152:color protection lut, 16 is normalized to 1

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Table 9-1885 SRSHARP0_SR7_CLR_PRT_LUT20 0x5158

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut167:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut166:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut165:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut164:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut163:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut162:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut161:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut160:color protection lut, 16 is normalized to 1

Table 9-1886 SRSHARP0_SR7_CLR_PRT_LUT21 0x5159

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut175:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut174:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut173:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut172:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut171:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut170:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut169:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut168:color protection lut, 16 is normalized to 1

Table 9-1887 SRSHARP0_SR7_CLR_PRT_LUT22 0x515a

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut183:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut182:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut181:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut180:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut179:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut178:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut177:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut176:color protection lut, 16 is normalized to 1

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Table 9-1888 SRSHARP0_SR7_CLR_PRT_LUT23 0x515b

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut191:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut190:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut189:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut188:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut187:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut186:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut185:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut184:color protection lut, 16 is normalized to 1

Table 9-1889 SRSHARP0_SR7_CLR_PRT_LUT24 0x515c

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut199:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut198:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut197:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut196:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut195:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut194:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut193:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut192:color protection lut, 16 is normalized to 1

Table 9-1890 SRSHARP0_SR7_CLR_PRT_LUT25 0x515d

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut207:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut206:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut205:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut204:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut203:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut202:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut201:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut200:color protection lut, 16 is normalized to 1

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Table 9-1891 SRSHARP0_SR7_CLR_PRT_LUT26 0x515e

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut215:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut214:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut213:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut212:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut211:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut210:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut209:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut208:color protection lut, 16 is normalized to 1

Table 9-1892 SRSHARP0_SR7_CLR_PRT_LUT27 0x515f

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut223:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut222:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut221:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut220:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut219:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut218:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut217:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut216:color protection lut, 16 is normalized to 1

Table 9-1893 SRSHARP0_SR7_CLR_PRT_LUT28 0x5160

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut231:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut230:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut229:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut228:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut227:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut226:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut225:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut224:color protection lut, 16 is normalized to 1

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Table 9-1894 SRSHARP0_SR7_CLR_PRT_LUT29 0x5161

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut239:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut238:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut237:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut236:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut235:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut234:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut233:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut232:color protection lut, 16 is normalized to 1

Table 9-1895 SRSHARP0_SR7_CLR_PRT_LUT30 0x5162

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut247:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut246:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut245:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut244:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut243:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut242:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut241:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut240:color protection lut, 16 is normalized to 1

Table 9-1896 SRSHARP0_SR7_CLR_PRT_LUT31 0x5163

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut255:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut254:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut253:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut252:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut251:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut250:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut249:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut248:color protection lut, 16 is normalized to 1

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Table 9-1897 SRSHARP1_SHARP_HVSIZE 0x5200

Bit(s)	R/W	Default	Description
28:16	R/W	0d1920	reg_pknr_hsize : . unsigned , default = 1920
12: 0	R/W	0d1080	reg_pknr_vsize : . unsigned , default = 1080

Table 9-1898 SRSHARP1_SHARP_HVBLANK_NUM 0x5201

Bit(s)	R/W	Default	Description
23: 16	R/W	0d8	reg_deband_hblank : . unsigned , default = 8
15: 8	R/W	0d20	reg_pknr_hblank_num : . unsigned , default = 20
7: 0	R/W	0d60	reg_pknr_vblank_num : . unsigned , default = 60

Table 9-1899 SRSHARP1_NR_GAUSSIAN_MODE 0x5202

Bit(s)	R/W	Default	Description
13□12	R/W	0d0	reg_nr_gau_cnorm: Y adpative coef norm, 0: 128, 1: 256, 2: 512, 3: 1024 .unsigned , default = 0
9□8	R/W	0d0	reg_nr_gau_cnorm: C adpative coef norm, 0: 128, 1: 256, 2: 512, 3: 1024 .unsigned , default = 0
5□4	R/W	0d1	reg_nr_gau_ymode:0 3x3 filter; 1: 5x5 filter, 2/3: adpative coef .unsigned , default = 1
1□0	R/W	0d1	reg_nr_gau_cmode:0 3x3 filter; 1: 5x5 filter, 2/3: adpative coef .unsigned , default = 1

Table 9-1900 SRSHARP1_PK_CON_2CIRHPGAIN_TH_RATE 0x5205

Bit(s)	R/W	Default	Description
31:24	R/W	0d25	reg_pk_cirhpcon2gain0:threshold0 of curve to map hpcon to hpgain for circle hp filter (all 8 direction same). 0~255.. unsigned , default = 25
23:16	R/W	0d60	reg_pk_cirhpcon2gain1:threshold1 of curve to map hpcon to hpgain for circle hp filter (all 8 direction same). 0~255.. unsigned , default = 60
15: 8	R/W	0d80	reg_pk_cirhpcon2gain5:rate0 (for hpcon < th0) of curve to map hpcon to hpgain for circle hp filter (all 8 direction same). 0~255.. unsigned , default = 80
7: 0	R/W	0d20	reg_pk_cirhpcon2gain6:rate1 (for hpcon > th1) of curve to map hpcon to hpgain for circle hp filter (all 8 direction same). 0~255.. unsigned , default = 20

Table 9-1901 SRSHARP1_PK_CON_2CIRHPGAIN_LIMIT 0x5206

Bit(s)	R/W	Default	Description
31:24	R/W	0d96	reg_pk_cirhpcon2gain2:level limit(for hpcon < th0) of curve to map hpcon to hpgain for circle hp filter (all 8 direction same). 0~255.. unsigned , default = 96
23:16	R/W	0d96	reg_pk_cirhpcon2gain3:level limit(for th0 < hpcon < th1) of curve to map hpcon to hpgain for circle hp filter (all 8 direction same). 0~255.. unsigned , default = 96
15: 8	R/W	0d5	reg_pk_cirhpcon2gain4:level limit(for hpcon > th1) of curve to map hpcon to hpgain for circle hp filter (all 8 direction same). 0~255.. unsigned , default = 5

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Table 9-1902 SRSHARP1_PK_CON_2CIRBPGAIN_TH_RATE 0x5207

Bit(s)	R/W	Default	Description
31:24	R/W	0d20	reg_pk_cirbpcon2gain0:threshold0 of curve to map bpcon to bpgain for circle bp filter (all 8 direction same). 0~255.. unsigned , default = 20
23:16	R/W	0d50	reg_pk_cirbpcon2gain1:threshold1 of curve to map bpcon to bpgain for circle bp filter (all 8 direction same).. unsigned , default = 50
15: 8	R/W	0d50	reg_pk_cirbpcon2gain5:rate0 (for bpcon < th0) of curve to map bpcon to bpgain for circle bp filter (all 8 direction same). 0~255.. unsigned , default = 50
7: 0	R/W	0d25	reg_pk_cirbpcon2gain6:rate1 (for bpcon > th1) of curve to map bpcon to bpgain for circle bp filter (all 8 direction same). 0~255.. unsigned , default = 25

Table 9-1903 SRSHARP1_PK_CON_2CIRBPGAIN_LIMIT 0x5208

Bit(s)	R/W	Default	Description
31:24	R/W	0d40	reg_pk_cirbpcon2gain2:level limit(for bpcon < th0) of curve to map bpcon to bpgain for circle bp filter (all 8 direction same). 0~255.. unsigned , default = 40
23:16	R/W	0d40	reg_pk_cirbpcon2gain3:level limit(for th0 < bpcon < th1) of curve to map bpcon to bpgain for circle bp filter (all 8 direction same). 0~255.. unsigned , default = 40
15: 8	R/W	0d5	reg_pk_cirbpcon2gain4:level limit(for bpcon > th1) of curve to map bpcon to bpgain for circle bp filter (all 8 direction same). 0~255.. unsigned , default = 5

Table 9-1904 SRSHARP1_PK_CON_2DRTHPGAIN_TH_RATE 0x5209

Bit(s)	R/W	Default	Description
31:24	R/W	0d25	reg_pk_drthpcon2gain0:threshold0 of curve to map hpcon to hpgain for directional hp filter (best direction). 0~255.. unsigned , default = 25
23:16	R/W	0d60	reg_pk_drthpcon2gain1:threshold1 of curve to map hpcon to hpgain for directional hp filter (best direction). 0~255.. unsigned , default = 60
15: 8	R/W	0d80	reg_pk_drthpcon2gain5:rate0 (for hpcon < th0) of curve to map hpcon to hpgain for directional hp filter (best direction). 0~255.. unsigned , default = 80
7: 0	R/W	0d20	reg_pk_drthpcon2gain6:rate1 (for hpcon > th1) of curve to map hpcon to hpgain for directional hp filter (best direction). 0~255.. unsigned , default = 20

Table 9-1905 SRSHARP1_PK_CON_2DRTHPGAIN_LIMIT 0x520a

Bit(s)	R/W	Default	Description
31:24	R/W	0d90	reg_pk_drthpcon2gain2:level limit(for hpcon < th0) of curve to map hpcon to hpgain for directional hp filter (best direction).. unsigned , default = 90
23:16	R/W	0d96	reg_pk_drthpcon2gain3:level limit(for th0 < hpcon < th1) of curve to map hpcon to hpgain for directional hp filter (best direction). 0~255.. unsigned , default = 96
15: 8	R/W	0d5	reg_pk_drthpcon2gain4:level limit(for hpcon > th1) of curve to map hpcon to hpgain for directional hp filter (best direction). 0~255.. unsigned , default = 5

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Table 9-1906 SRSHARP1_PK_CON_2DRTBPGAIN_TH_RATE 0x520b

Bit(s)	R/W	Default	Description
31:24	R/W	0d20	reg_pk_drtbpcon2gain0:threshold0 of curve to map bpcon to bpgain for directional bp filter (best direction). 0~255.. unsigned , default = 20
23:16	R/W	0d50	reg_pk_drtbpcon2gain1:threshold1 of curve to map bpcon to bpgain for directional bp filter (best direction). 0~255.. unsigned , default = 50
15: 8	R/W	0d50	reg_pk_drtbpcon2gain5:rate0 (for bpcon < th0) of curve to map bpcon to bpgain for directional bp filter (best direction). 0~255.. unsigned , default = 50
7: 0	R/W	0d25	reg_pk_drtbpcon2gain6:rate1 (for bpcon > th1) of curve to map bpcon to bpgain for directional bp filter (best direction). 0~255.. unsigned , default = 25

Table 9-1907 SRSHARP1_PK_CON_2DRTBPGAIN_LIMIT 0x520c

Bit(s)	R/W	Default	Description
31:24	R/W	0d40	reg_pk_drtbpcon2gain2:level limit(for bpcon < th0) of curve to map bpcon to bpgain for directional bp filter (best direction). 0~255.. unsigned , default = 40
23:16	R/W	0d40	reg_pk_drtbpcon2gain3:level limit(for th0 < bpcon < th1) of curve to map bpcon to bpgain for directional bp filter (best direction). 0~255.. unsigned , default = 40
15: 8	R/W	0d5	reg_pk_drtbpcon2gain4:level limit(for bpcon > th1) of curve to map bpcon to bpgain for directional bp filter (best direction). 0~255.. unsigned , default = 5

Table 9-1908 SRSHARP1_PK_CIRFB_LPF_MODE 0x520d

Bit(s)	R/W	Default	Description
29:28	R/W	0d1	reg_cirhp_horz_mode:no horz filter on HP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 . unsigned , default = 1
25:24	R/W	0d1	reg_cirhp_vert_mode:no vert filter on HP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 . unsigned , default = 1
21:20	R/W	0d1	reg_cirhp_diag_mode:filter on HP; 1: [1 2 1]/4; . unsigned , default = 1
13:12	R/W	0d1	reg_cirbp_horz_mode:no horz filter on BP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 . unsigned , default = 1
9: 8	R/W	0d1	reg_cirbp_vert_mode:no vert filter on BP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 . unsigned , default = 1
5: 4	R/W	0d1	reg_cirbp_diag_mode:filter on BP; 1: [1 2 1]/4; . unsigned , default = 1

Table 9-1909 SRSHARP1_PK_DRTFB_LPF_MODE 0x520e

Bit(s)	R/W	Default	Description
29:28	R/W	0d1	reg_drthp_horz_mode:no horz filter on HP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 2 . unsigned , default = 1
25:24	R/W	0d1	reg_drthp_vert_mode:no vert filter on HP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 2 . unsigned , default = 1
21:20	R/W	0d1	reg_drthp_diag_mode:filter on HP; 1: [1 2 1]/4; 1 . unsigned , default = 1
13:12	R/W	0d1	reg_drtbp_horz_mode:no horz filter on BP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 2 . unsigned , default = 1

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Bit(s)	R/W	Default	Description
9: 8	R/W	0d1	reg_drtbp_vert_mode:no vert filter on BP; 1: [1 2 1]/4; 2/3: [1 2 2 2 1]/8 2 . unsigned , default = 1
5: 4	R/W	0d1	reg_drtbp_diag_mode:filter on BP; 1: [1 2 1]/4; 1 . unsigned , default = 1

Table 9-1910 SRSHARP1_PK_CIRFB_HP_CORING 0x520f

Bit(s)	R/W	Default	Description
21:16	R/W	0d4	reg_cirhp_horz_core:coring of HP for Horz . unsigned , default = 4
13: 8	R/W	0d4	reg_cirhp_vert_core:coring of HP for Vert . unsigned , default = 4
5: 0	R/W	0d4	reg_cirhp_diag_core:coring of HP for Diag . unsigned , default = 4

Table 9-1911 SRSHARP1_PK_CIRFB_BP_CORING 0x5210

Bit(s)	R/W	Default	Description
21:16	R/W	0d4	reg_cirbp_horz_core:coring of HP for Horz . unsigned , default = 4
13: 8	R/W	0d4	reg_cirbp_vert_core:coring of HP for Vert . unsigned , default = 4
5: 0	R/W	0d4	reg_cirbp_diag_core:coring of HP for Diag . unsigned , default = 4

Table 9-1912 SRSHARP1_PK_DRTFB_HP_CORING 0x5211

Bit(s)	R/W	Default	Description
21:16	R/W	0d4	reg_drthp_horz_core:coring of HP for Horz . unsigned , default = 4
13: 8	R/W	0d4	reg_drthp_vert_core:coring of HP for Vert . unsigned , default = 4
5: 0	R/W	0d4	reg_drthp_diag_core:coring of HP for Diag . unsigned , default = 4

Table 9-1913 SRSHARP1_PK_DRTFB_BP_CORING 0x5212

Bit(s)	R/W	Default	Description
21:16	R/W	0d4	reg_drtbp_horz_core:coring of HP for Horz . unsigned , default = 4
13: 8	R/W	0d4	reg_drtbp_vert_core:coring of HP for Vert . unsigned , default = 4
5: 0	R/W	0d4	reg_drtbp_diag_core:coring of HP for Diag . unsigned , default = 4

Table 9-1914 SRSHARP1_PK_CIRFB_BLEND_GAIN 0x5213

Bit(s)	R/W	Default	Description
31:28	R/W	0d8	reg_hp_cir_hgain:normalized 8 as '1' . unsigned , default = 8
27:24	R/W	0d8	reg_hp_cir_vgain:normalized 8 as '1' . unsigned , default = 8
23:20	R/W	0d8	reg_hp_cir_dgain:normalized 8 as '1' . unsigned , default = 8
15:12	R/W	0d8	reg_bp_cir_hgain:normalized 8 as '1' . unsigned , default = 8

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Bit(s)	R/W	Default	Description
11: 8	R/W	0d8	reg_bp_cir_vgain:normalized 8 as '1' . unsigned , default = 8
7: 4	R/W	0d8	reg_bp_cir_dgain:normalized 8 as '1' . unsigned , default = 8

Table 9-1915 SRSHARP1_NR_ALPY_SSD_GAIN_OFST 0x5214

Bit(s)	R/W	Default	Description
15: 8	R/W	0d16	reg_nr_alp0_ssd_gain:gain to max ssd normalized 16 as '1' . unsigned , default = 16
5: 0	R/W	0x0	reg_nr_alp0_ssd_ofst:offset to ssd before dividing to min_err . signed , default = -2

Table 9-1916 SRSHARP1_NR_ALP0Y_ERR2CURV_TH_RATE 0x5215

Bit(s)	R/W	Default	Description
31:24	R/W	0d10	reg_nr_alp0_minerr_ypar0:threshold0 of curve to map mierr to alp0 for luma channel, this will be set value of flat region mierr that no need blur. 0~255.. unsigned , default = 10
23:16	R/W	0d25	reg_nr_alp0_minerr_ypar1:threshold1 of curve to map mierr to alp0 for luma channel,this will be set value of texture region mierr that can not blur.. unsigned , default = 25
15: 8	R/W	0d80	reg_nr_alp0_minerr_ypar5:rate0 (for mierr < th0) of curve to map mierr to alp0 for luma channel. the larger of the value, the deep of the slope. 0~255.. unsigned , default = 80
7: 0	R/W	0d64	reg_nr_alp0_minerr_ypar6:rate1 (for mierr > th1) of curve to map mierr to alp0 for luma channel. the larger of the value, the deep of the slope. 0~255.. unsigned , default = 64

Table 9-1917 SRSHARP1_NR_ALP0Y_ERR2CURV_LIMIT 0x5216

Bit(s)	R/W	Default	Description
31:24	R/W	0d63	reg_nr_alp0_minerr_ypar2:level limit(for mierr < th0) of curve to map mierr to alp0 for luma channel, this will be set to alp0 that we can do for flat region. 0~255.. unsigned , default = 63
23:16	R/W	0d0	reg_nr_alp0_minerr_ypar3:level limit(for th0 < mierr < th1) of curve to map mierr to alp0 for luma channel, this will be set to alp0 that we can do for misc region. 0~255.. unsigned , default = 0
15: 8	R/W	0d63	reg_nr_alp0_minerr_ypar4:level limit(for mierr > th1) of curve to map mierr to alp0 for luma channel, this will be set to alp0 that we can do for texture region. 0~255.. unsigned , default = 63

Table 9-1918 SRSHARP1_NR_ALP0C_ERR2CURV_TH_RATE 0x5217

Bit(s)	R/W	Default	Description
31:24	R/W	0d10	reg_nr_alp0_minerr_cpar0:threshold0 of curve to map mierr to alp0 for chroma channel, this will be set value of flat region mierr that no need blur.. unsigned , default = 10
23:16	R/W	0d25	reg_nr_alp0_minerr_cpar1:threshold1 of curve to map mierr to alp0 for chroma channel,this will be set value of texture region mierr that can not blur.. unsigned , default = 25

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Bit(s)	R/W	Default	Description
15: 8	R/W	0d80	reg_nr_alp0_minerr_cpar5:rate0 (for mierr < th0) of curve to map mierr to alp0 for chroma channel. the larger of the value, the deep of the slope. 0~255.. unsigned , default = 80
7: 0	R/W	0d64	reg_nr_alp0_minerr_cpar6:rate1 (for mierr > th1) of curve to map mierr to alp0 for chroma channel. the larger of the value, the deep of the slope. 0~255.. unsigned , default = 64

Table 9-1919 SRSHARP1_NR_ALP0C_ERR2CURV_LIMIT 0x5218

Bit(s)	R/W	Default	Description
31:24	R/W	0d63	reg_nr_alp0_minerr_cpar2:level limit(for mierr < th0) of curve to map mierr to alp0 for chroma channel, this will be set to alp0 that we can do for flat region. 0~255.. unsigned , default = 63
23:16	R/W	0d0	reg_nr_alp0_minerr_cpar3:level limit(for th0 < mierr < th1) of curve to map mierr to alp0 for chroma channel, this will be set to alp0 that we can do for misc region. 0~255.. unsigned , default = 0
15: 8	R/W	0d63	reg_nr_alp0_minerr_cpar4:level limit(for mierr > th1) of curve to map mierr to alp0 for chroma channel, this will be set to alp0 that we can do for texture region. 0~255.. unsigned , default = 63

Table 9-1920 SRSHARP1_NR_ALP0_MIN_MAX 0x5219

Bit(s)	R/W	Default	Description
29:24	R/W	0d2	reg_nr_alp0_ymin:normalized to 64 as '1' . unsigned , default = 2
21:16	R/W	0d63	reg_nr_alp0_ymax:normalized to 64 as '1' . unsigned , default = 63
13: 8	R/W	0d2	reg_nr_alp0_cmin:normalized to 64 as '1' . unsigned , default = 2
5: 0	R/W	0d63	reg_nr_alp0_cmax:normalized to 64 as '1' . unsigned , default = 63

Table 9-1921 SRSHARP1_NR_ALP1_MIERR_CORING 0x521a

Bit(s)	R/W	Default	Description
16	R/W	0d0	reg_nr_alp1_maxerr_mode:0 max err; 1: xerr . unsigned , default = 0
13: 8	R/W	0d0	reg_nr_alp1_core_rate:normalized 64 as "1" . unsigned , default = 0
5: 0	R/W	0d3	reg_nr_alp1_core_ofst:normalized 64 as "1" . signed , default = 3

Table 9-1922 SRSHARP1_NR_ALP1_ERR2CURV_TH_RATE 0x521b

Bit(s)	R/W	Default	Description
31:24	R/W	0d0	reg_nr_alp1_minerr_par0:threshold0 of curve to map mierr to alp1 for luma/chroma channel, this will be set value of flat region mierr that no need directional NR. 0~255.. unsigned , default = 0
23:16	R/W	0d24	reg_nr_alp1_minerr_par1:threshold1 of curve to map mierr to alp1 for luma/chroma channel,this will be set value of texture region mierr that can not do directional NR. 0~255.. unsigned , default = 24

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Bit(s)	R/W	Default	Description
15: 8	R/W	0d0	reg_nr_alp1_minerr_par5:rate0 (for mierr < th0) of curve to map mierr to alp1 for luma/chroma channel. the larger of the value, the deep of the slope.. unsigned , default = 0
7: 0	R/W	0d20	reg_nr_alp1_minerr_par6:rate1 (for mierr > th1) of curve to map mierr to alp1 for luma/chroma channel. the larger of the value, the deep of the slope. 0~255. unsigned , default = 20

Table 9-1923 SRSHARP1_NR_ALP1_ERR2CURV_LIMIT 0x521c

Bit(s)	R/W	Default	Description
31:24	R/W	0d0	reg_nr_alp1_minerr_par2:level limit(for mierr < th0) of curve to map mierr to alp1 for luma/chroma channel, this will be set to alp1 that we can do for flat region. 0~255.. unsigned , default = 0
23:16	R/W	0d16	reg_nr_alp1_minerr_par3:level limit(for th0 < mierr < th1) of curve to map mierr to alp1 for luma/chroma channel, this will be set to alp1 that we can do for misc region. 0~255.. unsigned , default = 16
15: 8	R/W	0d63	reg_nr_alp1_minerr_par4:level limit(for mierr > th1) of curve to map mierr to alp1 for luma/chroma channel, this will be set to alp1 that we can do for texture region. 0~255.255 before. unsigned , default = 63

Table 9-1924 SRSHARP1_NR_ALP1_MIN_MAX 0x521d

Bit(s)	R/W	Default	Description
29:24	R/W	0d0	reg_nr_alp1_ymin:normalized to 64 as '1' . unsigned , default = 0
21:16	R/W	0d63	reg_nr_alp1_ymax:normalized to 64 as '1' . unsigned , default = 63
13: 8	R/W	0d0	reg_nr_alp1_cmin:normalized to 64 as '1' . unsigned , default = 0
5: 0	R/W	0d63	reg_nr_alp1_cmax:normalized to 64 as '1' . unsigned , default = 63

Table 9-1925 SRSHARP1_PK_ALP2_MIERR_CORING 0x521e

Bit(s)	R/W	Default	Description
16	R/W	0d1	reg_pk_alp2_maxerr_mode:0 max err; 1: xerr . unsigned , default = 1
13: 8	R/W	0d13	reg_pk_alp2_core_rate:normalized 64 as "1" . unsigned , default = 13
5: 0	R/W	0d1	reg_pk_alp2_core_ofst:normalized 64 as "1" . signed , default = 1

Table 9-1926 SRSHARP1_PK_ALP2_ERR2CURV_TH_RATE 0x521f

Bit(s)	R/W	Default	Description
31:24	R/W	0d0	reg_pk_alp2_minerr_par0:threshold0 of curve to map mierr to alp2 for luma channel, this will be set value of flat region mierr that no need peaking.. unsigned , default = 0
23:16	R/W	0d24	reg_pk_alp2_minerr_par1:threshold1 of curve to map mierr to alp2 for luma channel,this will be set value of texture region mierr that can not do peaking. 0~255.. unsigned , default = 24

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Bit(s)	R/W	Default	Description
15: 8	R/W	0d0	reg_pk_alp2_minerr_par5:rate0 (for mierr < th0) of curve to map mierr to alp2 for luma channel. the larger of the value, the deep of the slope. 0~255.. unsigned , default = 0
7: 0	R/W	0d20	reg_pk_alp2_minerr_par6:rate1 (for mierr > th1) of curve to map mierr to alp2 for luma channel. the larger of the value, the deep of the slope. 0~255.. unsigned , default = 20

Table 9-1927 SRSHARP1_PK_ALP2_ERR2CURV_LIMIT 0x5220

Bit(s)	R/W	Default	Description
31:24	R/W	0d0	reg_pk_alp2_minerr_par2:level limit(for mierr < th0) of curve to map mierr to alp2 for luma channel, this will be set to alp2 that we can do for flat region. 0~255.. unsigned , default = 0
23:16	R/W	0d16	reg_pk_alp2_minerr_par3:level limit(for th0 < mierr < th1) of curve to map mierr to alp2 for luma channel, this will be set to alp2 that we can do for misc region. 0~255.. unsigned , default = 16
15: 8	R/W	0d63	reg_pk_alp2_minerr_par4:level limit(for mierr > th1) of curve to map mierr to alp2 for luma channel, this will be set to alp2 that we can do for texture region. 0~255. default = 63;. unsigned , default = 255

Table 9-1928 SRSHARP1_PK_ALP2_MIN_MAX 0x5221

Bit(s)	R/W	Default	Description
13: 8	R/W	0d0	reg_pk_alp2_min:normalized to 64 as '1' . unsigned , default = 0
5: 0	R/W	0d63	reg_pk_alp2_max:normalized to 64 as '1' . unsigned , default = 63

Table 9-1929 SRSHARP1_PK_FINALGAIN_HP_BP 0x5222

Bit(s)	R/W	Default	Description
17: 16	R/W	0d0	reg_final_gain_rs:right shift bits for the gain normalization, 0 normal to 32 as 1; 1 normal to 64 as 1; -2 normal to 8 as 1; -1 normal to 16 as 1 . signed , default = 0
15: 8	R/W	0d40	reg_hp_final_gain:gain to highpass boost result (including directional/circle blending), normalized 32 as '1', 0~255. 1.25 * 32. unsigned , default = 40
7: 0	R/W	0d30	reg_bp_final_gain:gain to bandpass boost result (including directional/circle blending), normalized 32 as '1', 0~255. 1.25 * 32. unsigned , default = 30

Table 9-1930 SRSHARP1_PK_OS_HORZ_CORE_GAIN 0x5223

Bit(s)	R/W	Default	Description
31:24	R/W	0d8	reg_pk_os_hsidecore:side coring (not to current pixel) to adaptive overshoot margin in horizontal direction. the larger of this value, the less overshoot admitted 0~255;. unsigned , default = 8
23:16	R/W	0d20	reg_pk_os_hsidegain:side gain (not to current pixel) to adaptive overshoot margin in horizontal direction. normalized to 32 as '1'. 0~255;. unsigned , default = 20

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Bit(s)	R/W	Default	Description
15: 8	R/W	0d2	reg_pk_os_hmidcore:midd coring (to current pixel) to adaptive overshoot margin in horizontal direction. the larger of this value, the less overshoot admitted 0~255;. unsigned , default = 2
7: 0	R/W	0d20	reg_pk_os_hmidgain:midd gain (to current pixel) to adaptive overshoot margin in horizontal direction. normalized to 32 as '1'. 0~255;. unsigned , default = 20

Table 9-1931 SRSHARP1_PK_OS_VERT_CORE_GAIN 0x5224

Bit(s)	R/W	Default	Description
31:24	R/W	0d8	reg_pk_os_vsidecore:side coring (not to current pixel) to adaptive overshoot margin in vertical direction. the larger of this value, the less overshoot admitted 0~255;. unsigned , default = 8
23:16	R/W	0d20	reg_pk_os_vsidegain:side gain (not to current pixel) to adaptive overshoot margin in vertical direction. normalized to 32 as '1'. 0~255;. unsigned , default = 20
15: 8	R/W	0d2	reg_pk_os_vmidcore:midd coring (to current pixel) to adaptive overshoot margin in vertical direction. the larger of this value, the less overshoot admitted 0~255;. unsigned , default = 2
7: 0	R/W	0d20	reg_pk_os_vmidgain:midd gain (to current pixel) to adaptive overshoot margin in vertical direction. normalized to 32 as '1'. 0~255;. unsigned , default = 20

Table 9-1932 SRSHARP1_PK_OS_ADPT_MISC 0x5225

Bit(s)	R/W	Default	Description
31:24	R/W	0d40	reg_pk_os_minerr_core:coring to minerr for adaptive overshoot margin. the larger of this value, the less overshoot admitted 0~255;. unsigned , default = 40
23:16	R/W	0d6	reg_pk_os_minerr_gain:gain to minerr based adaptive overshoot margin. normalized to 64 as '1'. 0~255;. unsigned , default = 6
15: 8	R/W	0d200	reg_pk_os_adpt_max:maximum limit adaptive overshoot margin (4x). 0~255; . unsigned , default = 200
7: 0	R/W	0d20	reg_pk_os_adpt_min:minimun limit adaptive overshoot margin (1x). 0~255; . unsigned , default = 20

Table 9-1933 SRSHARP1_PK_OS_STATIC 0x5226

Bit(s)	R/W	Default	Description
29:28	R/W	0d2	reg_pk_osh_mode:0~3: (2x+1) window in H direction . unsigned , default = 2
25:24	R/W	0d2	reg_pk_osv_mode:0~3: (2x+1) window in V direction . unsigned , default = 2
21:12	R/W	0d200	reg_pk_os_down:static negative overshoot margin. 0~1023; . unsigned , default = 200
9: 0	R/W	0d200	reg_pk_os_up:static positive overshoot margin. 0~1023; . unsigned , default = 200

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Table 9-1934 SRSHARP1_PK_NR_ENABLE 0x5227

Bit(s)	R/W	Default	Description
3: 2	R/W	0d0	reg_3d_mode : , 0: no 3D; 1: L/R; 2: T/B; 3: horizontal interleaved, dft = 0 //. unsigned , default = 0
1	R/W	0d1	reg_pk_en : . unsigned , default = 1
0	R/W	0d1	reg_nr_en : . unsigned , default = 1

Table 9-1935 SRSHARP1_PK_DRT_SAD_MISC 0x5228

Bit(s)	R/W	Default	Description
31:24	R/W	0d24	reg_pk_sad_ver_gain:gain to sad[4], 16 normalized to "1"; . unsigned , default = 24
23:16	R/W	0d24	reg_pk_sad_hor_gain:gain to sad[0], 16 normalized to "1"; . unsigned , default = 24
10: 9	R/W	0d0	reg_pk_bias_diag:bias towards diag . unsigned , default = 0
4: 0	R/W	0d24	reg_pk_drt_force:force direction of drt peaking filter, h2b: 0:hp drt force, 1: bp drt force; 2: bp+hp drt force, 3: no force;. unsigned , default = 24

Table 9-1936 SRSHARP1_NR_TI_DNLP_BLEND 0x5229

Bit(s)	R/W	Default	Description
10: 8	R/W	0d4	reg_dnlp_input_mode:dnlp input options. 0: org_y; 1: gau_y; 2: gauadp_y; 3: edgadplpf_y; 4: nr_y;5: lti_y; 6: pk_y (before os);7: pk_y (after os). unsigned , default = 4
3: 2	R/W	0d1	reg_nr_cti_blend_mode:blend mode of nr and lti result: 0: nr; 1:cti; 2: (nr+cti)/2; 3:cti + dlt_nr . unsigned , default = 1
1: 0	R/W	0d1	reg_nr_lti_blend_mode:blend mode of nr and lti result: 0: nr; 1:lti; 2: (nr+lti)/2; 3:lti + dlt_nr . unsigned , default = 1

Table 9-1937 SRSHARP1_TI_DIR_CORE_ALPHA 0x522a

Bit(s)	R/W	Default	Description
29:24	R/W	0d10	reg_adp_lti_dir_alp_core_ofst:ofst to min_err, alpha = (min_err - (max_err-min_err)*rate + ofst)/max_err*64; dft=10. unsigned , default = 10
19:16	R/W	0d0	reg_adp_lti_dir_alp_core_rate:ofset to min_err, alpha = (min_err - (max_err-min_err)*rate + ofst)/max_err*64; dft=0/32. unsigned , default = 0
13: 8	R/W	0d0	reg_adp_lti_dir_alpmin:min value of alpha, alpha = (min_err+x +ofst)/max_err*64; dft=10 . unsigned , default = 0
5: 0	R/W	0d63	reg_adp_lti_dir_alpmax:max value of alpha, alpha = (min_err+x +ofst)/max_err*64; dft=63 . unsigned , default = 63

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Table 9-1938 SRSHARP1_CTI_DIR_ALPHA 0x522b

Bit(s)	R/W	Default	Description
29:24	R/W	0d5	reg_adp_cti_dir_alp_core_ofst:ofst to min_err, alpha = (min_err - (max_err-min_err)*rate + ofst)/max_err*64; dft=10. unsigned , default = 5
19:16	R/W	0d0	reg_adp_cti_dir_alp_core_rate:ofset to min_err, alpha = (min_err - (max_err-min_err)*rate + ofst)/max_err*64; dft=0/32. unsigned , default = 0
13: 8	R/W	0d0	reg_adp_cti_dir_alpmin:min value of alpha, alpha = (min_err +x+ofst)/max_err*64; dft=10 . unsigned , default = 0
5: 0	R/W	0d63	reg_adp_cti_dir_alpmax:max value of alpha, alpha = (min_err +x+ofst)/max_err*64; dft=63 . unsigned , default = 63

Table 9-1939 SRSHARP1_LTI_CTI_DF_GAIN 0x522c

Bit(s)	R/W	Default	Description
29:24	R/W	0d16	reg_adp_lti_hdf_gain:8 normalized to "1"; default = 16 . unsigned , default = 16
21:16	R/W	0d12	reg_adp_lti_vdf_gain:8 normalized to "1"; default = 12 . unsigned , default = 12
13: 8	R/W	0d16	reg_adp_cti_hdf_gain:8 normalized to "1"; default = 16 . unsigned , default = 16
5: 0	R/W	0d12	reg_adp_cti_vdf_gain:8 normalized to "1"; default = 12 . unsigned , default = 12

Table 9-1940 SRSHARP1_LTI_CTI_DIR_AC_DBG 0x522d

Bit(s)	R/W	Default	Description
30	R/W	0d1	reg_adp_lti_dir_lpf:0: no lpf; 1: [1 2 2 2 1]/8 lpf . unsigned , default = 1
28	R/W	0d0	reg_adp_lti_dir_difmode:0: y_dif; 1: y_dif + (u_dif+v_dif)/2; . unsigned , default = 0
26	R/W	0d1	reg_adp_cti_dir_lpf:0: no lpf; 1: [1 2 2 2 1]/8 lpf dft=1 . unsigned , default = 1
25:24	R/W	0d0	reg_adp_cti_dir_difmode:0: (u_dif+v_dif); 1: y_dif/2 + (u_dif+v_dif)*3/4; 2: y_dif + (u_dif+v_dif)/2; 3: y_dif*2 (not recomended). unsigned , default = 0
23:22	R/W	0d3	reg_adp_hvlti_dcblend_mode:0: hlti_dc; 1:vlti_dc; 2: avg 3; blend on alpha . unsigned , default = 3
21:20	R/W	0d3	reg_adp_hvcti_dcblend_mode:0: hcti_dc; 1:vcti_dc; 2: avg 3; blend on alpha . unsigned , default = 3
19:18	R/W	0d3	reg_adp_hvlti_acblend_mode:hlti_ac; 1:vlti_ac; 2: add 3;:adaptive to alpha . unsigned , default = 3
17:16	R/W	0d3	reg_adp_hvcti_acblend_mode:hcti_ac; 1:vcti_ac; 2: add 3;: adaptive to alpha . unsigned , default = 3
14:12	R/W	0d0	reg_adp_hlti_debug : , for hlti debug, default = 0 . unsigned , default = 0
10: 8	R/W	0d0	reg_adp_vlti_debug : , for vlti debug, default = 0 . unsigned , default = 0
6: 4	R/W	0d0	reg_adp_hcti_debug : , for hcti debug, default = 0 . unsigned , default = 0
2: 0	R/W	0d0	reg_adp_vcti_debug : , for vcti debug, default = 0 . unsigned , default = 0

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Table 9-1941 SRSHARP1_HCTI_FLT_CLP_DC 0x522e

Bit(s)	R/W	Default	Description
28	R/W	0d1	reg_adp_hcti_en : , 0: no cti, 1: new cti, default = 1 . unsigned , default = 1
27:26	R/W	0d3	reg_adp_hcti_vdn_flt : , 0: no lpf; 1:[0,2,4,2,0], 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
25:24	R/W	0d2	reg_adp_hcti_hdn_flt : , 0: no lpf; 1:[0, 0, 0, 4, 8, 4, 0, 0, 0], 2:[0, 0, 2, 4, 4, 4, 2, 0, 0], 3: [1, 2, 2, 2, 2, 2, 2, 2, 1], default = 2. unsigned , default = 2
23:22	R/W	0d3	reg_adp_hcti_ddn_flt : , 0: no lpf; 1:[0,2,4,2,0], 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
21:20	R/W	0d2	reg_adp_hcti_lpf0_flt : , 0:no filter; 1:sigma=0.75, 2: sigma = 1.0, 3: sigma = 1.5, default = 2 . unsigned , default = 2
19:18	R/W	0d2	reg_adp_hcti_lpf1_flt : , 0:no filter; 1:sigma= 2.0, 2: sigma = 3.0, 3: sigma = 4.0, default = 2 . unsigned , default = 2
17:16	R/W	0d2	reg_adp_hcti_lpf2_flt : , 0:no filter; 1:sigma=5.0, 2: sigma = 9.0, 3: sigma = 13.0, default = 2 . unsigned , default = 2
15:12	R/W	0d7	reg_adp_hcti_hard_clp_win : , window size, 0~8, default = 7 . unsigned , default = 7
11: 8	R/W	0d3	reg_adp_hcti_hard_win_min : , window size, 0~8, default = 3 . unsigned , default = 3
4	R/W	0d1	reg_adp_hcti_clp_mode : , 0: hard clip, 1: adaptive clip, default = 1 . unsigned , default = 1
2: 0	R/W	0d0	reg_adp_hcti_dc_mode : , 0:dn, 1:lpf0, 2:lpf1, 3:lpf2, 4: lpf3: 5: vdn result; 6/7: org, default = 0 . unsigned , default = 0

Table 9-1942 SRSHARP1_HCTI_BST_GAIN 0x522f

	R/W	Default	Description
31:24	R/W	0d80	reg_adp_hcti_bst_gain0:gain of the bandpass 0 (lpf1-lpf2)- LBP, default = 80 . unsigned , default = 80
23:16	R/W	0d96	reg_adp_hcti_bst_gain1:gain of the bandpass 1 (lpf0-lpf1)- BP, default = 96 . unsigned , default = 96
15: 8	R/W	0d64	reg_adp_hcti_bst_gain2:gain of the bandpass 2 (hdn-lpf0)- HP, default = 64 . unsigned , default = 64
7: 0	R/W	0d16	reg_adp_hcti_bst_gain3:gain of the unsharp band (yuvin-hdn) - US, default = 16 . unsigned , default = 16

Table 9-1943 SRSHARP1_HCTI_BST_CORE 0x5230

Bit(s)	R/W	Default	Description
31:24	R/W	0d0	reg_adp_hcti_bst_core0:core of the bandpass 0 (lpf1-lpf2)- LBP, default = 0 . unsigned , default = 0
23:16	R/W	0d0	reg_adp_hcti_bst_core1:core of the bandpass 1 (lpf0-lpf1)- BP, default = 0 . unsigned , default = 0
15: 8	R/W	0d0	reg_adp_hcti_bst_core2:core of the bandpass 2 (hdn-lpf0)- HP, default = 0 . unsigned , default = 0
7: 0	R/W	0d0	reg_adp_hcti_bst_core3:core of the unsharp band (yuvin-hdn) - US, default = 0 . unsigned , default = 0

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Table 9-1944 SRSHARP1_HCTI_CON_2_GAIN_0 0x5231

Bit(s)	R/W	Default	Description
31:29	R/W	0d2	reg_adp_hcti_con_mode:con mode 0:[0, 0,-1, 1, 0, 0, 0]+[0, 0, 0, 1,-1, 0, 0], 1: [0, 0,-1, 0, 1, 0, 0], 2: [0,-1, 0, 0, 0, 1, 0], 3:[-1, 0, 0, 0, 0, 0, 0, 1], 4: .... default = 2. unsigned , default = 2
28:26	R/W	0d3	reg_adp_hcti_dx_mode:dx mode 0: [-1 1 0]; 1~7: [-1 (2x+1)"0" 1], default = 3 . unsigned , default = 3
25:24	R/W	0d1	reg_adp_hcti_con_lpf:lpf mode of the con: 0: [1 2 1]/4; 1:[1 2 2 2 1]/8, default = 1 . unsigned , default = 1
23:16	R/W	0d25	reg_adp_hcti_con_2_gain0 : , default = 25 . unsigned , default = 25
15: 8	R/W	0d60	reg_adp_hcti_con_2_gain1 : , default = 60 . unsigned , default = 60
7: 0	R/W	0d0	reg_adp_hcti_con_2_gain2 : 0;, default = 0 . unsigned , default = 0

Table 9-1945 SRSHARP1_HCTI_CON_2_GAIN_1 0x5232

Bit(s)	R/W	Default	Description
31:24	R/W	0d96	reg_adp_hcti_con_2_gain3 : 96;, default = 96 . unsigned , default = 96
23:16	R/W	0d5	reg_adp_hcti_con_2_gain4 : 5;, default = 5 . unsigned , default = 5
15: 8	R/W	0d80	reg_adp_hcti_con_2_gain5 : 80;, default = 80 . unsigned , default = 80
7: 0	R/W	0d20	reg_adp_hcti_con_2_gain6 : 20;, default = 20 . unsigned , default = 20

Table 9-1946 SRSHARP1_HCTI_OS_MARGIN 0x5233

Bit(s)	R/W	Default	Description
7: 0	R/W	0d0	reg_adp_hcti_os_margin:margin for hcti overshoot, default = 0 . unsigned , default = 0

Table 9-1947 SRSHARP1_HLTI_FLT_CLP_DC 0x5234

Bit(s)	R/W	Default	Description
28	R/W	0d1	reg_adp_hlti_en : , 0: no cti, 1: new cti, default = 1 . unsigned , default = 1
27:26	R/W	0d2	reg_adp_hlti_vdn_flt : , 0: no lpf; 1:[0,2,4,2,0], 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 2 . unsigned , default = 2
25:24	R/W	0d2	reg_adp_hlti_hdn_flt : , 0: no lpf; 1:[0, 0, 0, 4, 8, 4, 0, 0, 0], 2:[0, 0, 2, 4, 4, 4, 2, 0, 0], 3: [1, 2, 2, 2, 2, 2, 2, 2, 1], default = 2. unsigned , default = 2
23:22	R/W	0d2	reg_adp_hlti_ddn_flt : , 0: no lpf; 1:[0,2,4,2,0], 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 2 . unsigned , default = 2
21:20	R/W	0d2	reg_adp_hlti_lpf0_flt : , 0:no filter; 1:sigma=0.75, 2: sigma = 1.0, 3: sigma = 1.5, default = 2 . unsigned , default = 2
19:18	R/W	0d2	reg_adp_hlti_lpf1_flt : , 0:no filter; 1:sigma= 2.0, 2: sigma = 3.0, 3: sigma = 4.0, default = 2 . unsigned , default = 2
17:16	R/W	0d2	reg_adp_hlti_lpf2_flt : , 0:no filter; 1:sigma=5.0, 2: sigma = 9.0, 3: sigma = 13.0, default = 2 . unsigned , default = 2

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Bit(s)	R/W	Default	Description
15:12	R/W	0d2	reg_adp_hlti_hard_clp_win : , window size, 0~8, default = 2 . unsigned , default = 2
11: 8	R/W	0d1	reg_adp_hlti_hard_win_min : , window size, 0~8, default = 1 . unsigned , default = 1
4	R/W	0d0	reg_adp_hlti_clp_mode : , 0: hard clip, 1: adaptive clip, default = 0 . unsigned , default = 0
2: 0	R/W	0d4	reg_adp_hlti_dc_mode : , 0:dn, 1:lpf0, 2:lpf1, 3:lpf2, 4: lpf3: 5: vdn result; 6/7:org, default = 4 . unsigned , default = 4

Table 9-1948 SRSHARP1_HLTI_BST_GAIN 0x5235

Bit(s)	R/W	Default	Description
31:24	R/W	0d40	reg_adp_hlti_bst_gain0:gain of the bandpass 0 (lpf1-lpf2)- LBP, default = 40 . unsigned , default = 40
23:16	R/W	0d48	reg_adp_hlti_bst_gain1:gain of the bandpass 1 (lpf0-lpf1)- BP, default = 48 . unsigned , default = 48
15: 8	R/W	0d32	reg_adp_hlti_bst_gain2:gain of the bandpass 2 (hdn-lpf0)- HP, default = 32 . unsigned , default = 32
7: 0	R/W	0d16	reg_adp_hlti_bst_gain3:gain of the unsharp band (yuvin-hdn) - US, default = 16 . unsigned , default = 16

Table 9-1949 SRSHARP1_HLTI_BST_CORE 0x5236

Bit(s)	R/W	Default	Description
31:24	R/W	0d5	reg_adp_hlti_bst_core0:core of the bandpass 0 (lpf1-lpf2)- LBP, default = 5 . unsigned , default = 5
23:16	R/W	0d5	reg_adp_hlti_bst_core1:core of the bandpass 1 (lpf0-lpf1)- BP, default = 5 . unsigned , default = 5
15: 8	R/W	0d5	reg_adp_hlti_bst_core2:core of the bandpass 2 (hdn-lpf0)- HP, default = 5 . unsigned , default = 5
7: 0	R/W	0d3	reg_adp_hlti_bst_core3:core of the unsharp band (yuvin-hdn) - US, default = 3 . unsigned , default = 3

Table 9-1950 SRSHARP1_HLTI_CON_2_GAIN_0 0x5237

Bit(s)	R/W	Default	Description
31:29	R/W	0d2	reg_adp_hlti_con_mode:con mode 0:[0, 0,-1, 1, 0, 0, 0]+[0, 0, 0, 1,-1, 0, 0], 1: [0, 0,-1, 0, 1, 0, 0], 2: [0,-1, 0, 0, 0, 1, 0], 3:[-1, 0, 0, 0, 0, 0, 1], 4: ....., default = 2. unsigned , default = 2
28:26	R/W	0d3	reg_adp_hlti_dx_mode:dx mode 0: [-1 1 0]; 1~7: [-1 (2x+1)"0" 1], default = 3 . unsigned , default = 3
25:24	R/W	0d1	reg_adp_hlti_con_lpf:lpf mode of the con: 0: [1 2 1]/4; 1:[1 2 2 2 1]/8, default = 1 . unsigned , default = 1
23:16	R/W	0d25	reg_adp_hlti_con_2_gain0 : 25;, default = 25 . unsigned , default = 25
15: 8	R/W	0d60	reg_adp_hlti_con_2_gain1 : 60;, default = 60 . unsigned , default = 60
7: 0	R/W	0d90	reg_adp_hlti_con_2_gain2 : 0;, default = 90 . unsigned , default = 90

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Table 9-1951 SRSHARP1_HLTI_CON_2_GAIN_1 0x5238

Bit(s)	R/W	Default	Description
31:24	R/W	0d96	reg_adp_hlti_con_2_gain3 : 96;, default = 96 . unsigned , default = 96
23:16	R/W	0d95	reg_adp_hlti_con_2_gain4 : 5;, default = 95 . unsigned , default = 95
15: 8	R/W	0d80	reg_adp_hlti_con_2_gain5 : 80;, default = 80 . unsigned , default = 80
7: 0	R/W	0d20	reg_adp_hlti_con_2_gain6 : 20;, default = 20 . unsigned , default = 20

Table 9-1952 SRSHARP1_HLTI_OS_MARGIN 0x5239

Bit(s)	R/W	Default	Description
7: 0	R/W	0d0	reg_adp_hlti_os_margin:margin for hlti overshoot, default = 0 . unsigned , default = 0

Table 9-1953 SRSHARP1_VLTI_FLT_CON_CLP 0x523a

Bit(s)	R/W	Default	Description
14	R/W	0d1	reg_adp_vlti_en:enable bit of vlti, default = 1 . unsigned , default = 1
13:12	R/W	0d3	reg_adp_vlti_hxn_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
11:10	R/W	0d3	reg_adp_vlti_dxn_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
9: 8	R/W	0d3	reg_adp_vlti_han_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
7: 6	R/W	0d3	reg_adp_vlti_dan_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
5: 4	R/W	0d2	reg_adp_vlti_dx_mode:0:[-1 1] 1:[-1 0 -1]; 2/3: [-1 0 0 0 -1], default = 2 . unsigned , default = 2
2	R/W	0d1	reg_adp_vlti_con_lpf:lpf mode of the con: 0: [1 2 1]/4; 1:[1 2 2 2 1]/8, default = 1 . unsigned , default = 1
0	R/W	0d1	reg_adp_vlti_hard_clp_win:window size; 0: 1x3 window; 1: 1x5 window, default = 1 . unsigned , default = 1

Table 9-1954 SRSHARP1_VLTI_BST_GAIN 0x523b

Bit(s)	R/W	Default	Description
23:16	R/W	0d32	reg_adp_vlti_bst_gain0:gain to boost filter [-1 2 -1];, default = 32 . unsigned , default = 32
15: 8	R/W	0d32	reg_adp_vlti_bst_gain1:gain to boost filter [-1 0 2 0 -1];, default = 32 . unsigned , default = 32
7: 0	R/W	0d32	reg_adp_vlti_bst_gain2:gain to boost filter usf, default = 32 . unsigned , default = 32

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Table 9-1955 SRSHARP1_VLTI_BST_CORE 0x523c

Bit(s)	R/W	Default	Description
23:16	R/W	0d5	reg_adp_vlti_bst_core0:coring to boost filter [-1 2 -1];, default = 5 . unsigned , default = 5
15: 8	R/W	0d5	reg_adp_vlti_bst_core1:coring to boost filter [-1 0 2 0 -1];, default = 5 . unsigned , default = 5
7: 0	R/W	0d3	reg_adp_vlti_bst_core2:coring to boost filter usf, default = 3 . unsigned , default = 3

Table 9-1956 SRSHARP1_VLTI_CON_2_GAIN_0 0x523d

Bit(s)	R/W	Default	Description
31:24	R/W	0d25	reg_adp_vlti_con_2_gain0 : 25;, default = 25 . unsigned , default = 25
23:16	R/W	0d69	reg_adp_vlti_con_2_gain1 : 60;, default = 69 . unsigned , default = 60
15: 8	R/W	0d90	reg_adp_vlti_con_2_gain2 : 0;, default = 90 . unsigned , default = 90
7: 0	R/W	0d96	reg_adp_vlti_con_2_gain3 : 96;, default = 96 . unsigned , default = 96

Table 9-1957 SRSHARP1_VLTI_CON_2_GAIN_1 0x523e

Bit(s)	R/W	Default	Description
31:24	R/W	0d95	reg_adp_vlti_con_2_gain4 : 5;, default = 95 . unsigned , default = 95
23:16	R/W	0d80	reg_adp_vlti_con_2_gain5 : 80;, default = 80 . unsigned , default = 80
15: 8	R/W	0d20	reg_adp_vlti_con_2_gain6 : 20;, default = 20 . unsigned , default = 20
7: 0	R/W	0d0	reg_adp_vlti_os_margin:margin for vlti overshoot, default = 0 . unsigned , default = 0

Table 9-1958 SRSHARP1_VCTI_FLT_CON_CLP 0x523f

Bit(s)	R/W	Default	Description
14	R/W	0d1	reg_adp_vcti_en:enable bit of vlti, default = 1 . unsigned , default = 1
13:12	R/W	0d3	reg_adp_vcti_hxn_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
11:10	R/W	0d3	reg_adp_vcti_dxn_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
9: 8	R/W	0d3	reg_adp_vcti_han_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
7: 6	R/W	0d3	reg_adp_vcti_dan_flt:0: no dn; 1: [1 2 1]/4; 2 : [1 2 2 2 1]/8 3:[1 0 2 0 1]/4, default = 3 . unsigned , default = 3
5: 4	R/W	0d2	reg_adp_vcti_dx_mode:0:[-1 1] 1:[-1 0 -1]; 2/3: [-1 0 0 0 -1], default = 2 . unsigned , default = 2
2	R/W	0d1	reg_adp_vcti_con_lpf:lpf mode of the con: 0: [1 2 1]/4; 1:[1 2 2 2 1]/8, default = 1 . unsigned , default = 1
0	R/W	0d1	reg_adp_vcti_hard_clp_win:window size; 0: 1x3 window; 1: 1x5 window, default = 1 . unsigned , default = 1

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Table 9-1959 SRSHARP1_VCTI_BST_GAIN 0x5240

Bit(s)	R/W	Default	Description
23:16	R/W	0d0	reg_adp_vcti_bst_gain0:gain to boost filter [-1 2 -1];, default = 0 . unsigned , default = 0
15: 8	R/W	0d0	reg_adp_vcti_bst_gain1:gain to boost filter [-1 0 2 0 -1];, default = 0 . unsigned , default = 0
7: 0	R/W	0d0	reg_adp_vcti_bst_gain2:gain to boost filter usf, default = 0 . unsigned , default = 0

Table 9-1960 SRSHARP1_VCTI_BST_CORE 0x5241

Bit(s)	R/W	Default	Description
23:16	R/W	0d0	reg_adp_vcti_bst_core0:coring to boost filter [-1 2 -1];, default = 0 . unsigned , default = 0
15: 8	R/W	0d0	reg_adp_vcti_bst_core1:coring to boost filter [-1 0 2 0 -1];, default = 0 . unsigned , default = 0
7: 0	R/W	0d0	reg_adp_vcti_bst_core2:coring to boost filter usf, default = 0 . unsigned , default = 0

Table 9-1961 SRSHARP1_VCTI_CON_2_GAIN_0 0x5242

Bit(s)	R/W	Default	Description
31:24	R/W	0d25	reg_adp_vcti_con_2_gain0 : 25;, default = 25 . unsigned , default = 25
23:16	R/W	0d60	reg_adp_vcti_con_2_gain1 : 60;, default = 60 . unsigned , default = 60
15: 8	R/W	0d90	reg_adp_vcti_con_2_gain2 : 0;, default = 90 . unsigned , default = 90
7: 0	R/W	0d96	reg_adp_vcti_con_2_gain3 : 96;, default = 96 . unsigned , default = 96

Table 9-1962 SRSHARP1_VCTI_CON_2_GAIN_1 0x5243

Bit(s)	R/W	Default	Description
31:24	R/W	0d95	reg_adp_vcti_con_2_gain4 : 5;, default = 95 . unsigned , default = 95
23:16	R/W	0d80	reg_adp_vcti_con_2_gain5 : 80;, default = 80 . unsigned , default = 80
15: 8	R/W	0d20	reg_adp_vcti_con_2_gain6 : 20;, default = 20 . unsigned , default = 20
7: 0	R/W	0d0	reg_adp_vcti_os_margin:margin for vcti overshoot, default = 0 . unsigned , default = 0

Table 9-1963 SRSHARP1_SHARP_3DLIMIT 0x5244

Bit(s)	R/W	Default	Description
28:16	R/W	0d0	reg_3d_mid_width : ,width of left part of 3d input, dft = half size of input width default = 0 . unsigned , default = 960
12: 0	R/W	0d0	reg_3d_mid_height : ,height of left part of 3d input, dft = half size of input height default = 0 . unsigned , default = 540

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Table 9-1964 SRSHARP1_DNLP_EN 0x5245

Bit(s)	R/W	Default	Description
15□8	R/W	0d0	reg_dnlp_hblank: . unsigned , default = 8
0	R/W	0d1	reg_dnlp_en : . unsigned , default = 1

Table 9-1965 SRSHARP1_DEMO_CRTL 0x5256

Bit(s)	R/W	Default	Description
18:17	R/W	0d2	demo_disp_position : . unsigned , default = 2
16	R/W	0d0	demo_hsvsharp_enable : . unsigned , default = 0
12: 0	R/W	0d360	demo_left_top_screen_width: . unsigned , default = 360

Table 9-1966 SRSHARP1_SHARP_SR2_CTRL 0x5257

Bit(s)	R/W	Default	Description
24	R/W	0	reg_sr2_bic_pknr_bypass : bypass peaking/TI/Cubic
23:22	R/W		reserved
21:16	R/W	24	sr2_pk_la_err_dis_rate, low angle and high angle error should not be no less than nearby_error* rate/64
15: 8	R/W	16	sr2_pk_sad_diag_gain, gain to sad[2] and sad[6], 16 normalized to 1
7	R/W	0	sr2_vert_outphs, vertical output pixel phase, 0: 0 phase; 1: 1/2 phase
6	R/W	0	sr2_horz_outphs, horizontal output pixel phase, 0: 0 phase; 1: 1/2 phase
5	R/W	0	sr2_vert_ratio , vertical scale ratio, 0- > 1:1; 1- > 1:2
4	R/W	0	sr2_horz_ratio , horizontal scale ratio, 0- > 1:1; 1- > 1:2
3	R/W	1	sr2_ bic_norm , normalization of bicubical: 0: 128; 1: 64
2	R/W	0	sr2_ enable , 1 to enable super scaler
1	R/W	0	sr2_ sharp_prc_lr_hbic,
0	R/W	0	sr2_ sharp_prc_lr, 1: LTI/CTI/NR/Peaking processing using LR grid. 0: on HR grid; 1:on LR grid, horizontally no upscale, but using simple bic.

Table 9-1967 SRSHARP1_SHARP_SR2_YBIC_HCOEF0 0x5258

Bit(s)	R/W	Default	Description
31:24	R/W	0	sr2_y_bic_hcoeff03, signed
23:16	R/W	0	sr2_y_bic_hcoeff02, signed
15: 8	R/W	64	sr2_y_bic_hcoeff01, signed
7: 0	R/W	0	sr2_y_bic_hcoeff00, signed

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Table 9-1968 SRSHARP1_SHARP_SR2_YBIC_HCOEF1 0x5259

Bit(s)	R/W	Default	Description
31:24	R/W	-4	sr2_y_bic_hcoeff13 , signed
23:16	R/W	36	sr2_y_bic_hcoeff12 , signed
15: 8	R/W	36	sr2_y_bic_hcoeff11 , signed
7: 0	R/W	-4	sr2_y_bic_hcoeff10 , signed

Table 9-1969 SRSHARP1_SHARP_SR2_CBIC_HCOEF0 0x525a

Bit(s)	R/W	Default	Description
31:24	R/W	0	sr2_c_bic_hcoeff03 , signed
23:16	R/W	21	sr2_c_bic_hcoeff02 , signed
15: 8	R/W	22	sr2_c_bic_hcoeff01 , signed
7: 0	R/W	21	sr2_c_bic_hcoeff00 , signed

Table 9-1970 SRSHARP1_SHARP_SR2_CBIC_HCOEF1 0x525b

Bit(s)	R/W	Default	Description
31:24	R/W	-4	sr2_c_bic_hcoeff13 , signed
23:16	R/W	36	sr2_c_bic_hcoeff12 , signed
15: 8	R/W	36	sr2_c_bic_hcoeff11 , signed
7: 0	R/W	-4	sr2_c_bic_hcoeff10 , signed

Table 9-1971 SRSHARP1_SHARP_SR2_YBIC_VCOEF0 0x525c

Bit(s)	R/W	Default	Description
31:24	R/W	0	sr2_y_bic_vcoeff03 , signed
23:16	R/W	0	sr2_y_bic_vcoeff02 , signed
15: 8	R/W	64	sr2_y_bic_vcoeff01 , signed
7: 0	R/W	0	sr2_y_bic_vcoeff00 , signed

Table 9-1972 SRSHARP1_SHARP_SR2_YBIC_VCOEF1 0x525d

Bit(s)	R/W	Default	Description
31:24	R/W	-4	sr2_y_bic_vcoeff13 , signed
23:16	R/W	36	sr2_y_bic_vcoeff12 , signed
15: 8	R/W	36	sr2_y_bic_vcoeff11 , signed
7: 0	R/W	-4	sr2_y_bic_vcoeff10 , signed

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Table 9-1973 SRSHARP1_SHARP_SR2_CBIC_VCOEF0 0x525e

Bit(s)	R/W	Default	Description
31:24	R/W	0	sr2_c_bic_vcoeff03 , signed
23:16	R/W	21	sr2_c_bic_vcoeff02 , signed
15: 8	R/W	22	sr2_c_bic_vcoeff01 , signed
7: 0	R/W	21	sr2_c_bic_vcoeff00 , signed

Table 9-1974 SRSHARP1_SHARP_SR2_CBIC_VCOEF1 0x525f

Bit(s)	R/W	Default	Description
31:24	R/W	-4	sr2_c_bic_vcoeff13 , signed
23:16	R/W	36	sr2_c_bic_vcoeff12 , signed
15: 8	R/W	36	sr2_c_bic_vcoeff11 , signed
7: 0	R/W	-4	sr2_c_bic_vcoeff10 , signed

Table 9-1975 SRSHARP1_SHARP_SR2_MISC 0x5260

Bit(s)	R/W	Default	Description
31:2	R/W		reserved
1	R/W	0	sr2_cmpmux_bef , 0 : no swap for YUV/RGB; 1: swap for YUV/RGB, YUV/RGB-> UVY/GBR
0	R/W	0	sr2_cmpmux_aft , 0 : no swap for YUV/RGB; 1: swap for YUV/RGB, UVY/GBR-> YUV/RGB

Table 9-1976 SRSHARP1_SR3_SAD_CTRL 0x5261

Bit(s)	R/W	Default	Description
31:30	R/W		reserved
29:24	R/W	0d6	reg_sr3_pk_sad_core_rate : rate of coring.
23:22	R/W		reserved
21:16	R/W	0d6	reg_sr3_lti_sad_core_rate : rate of coring.
15:14	R/W		reserved
13:8	R/W	0d6	reg_sr3_cti_sad_core_rate : rate of coring.
7	R/W	0d1	reg_sr3_lti_hsad_mode: mode for hsad of lti calculation, 0:block based; 1: other sharp
6	R/W	0d1	reg_sr3_cti_hsad_mode: mode for hsad of cti calculation, 0:block based; 1: other sharp
5	R/W	0d1	reg_sr3_lti_dsad_mode: mode for dsad of lti calculation, 0:block based; 1: other sharp
4	R/W	0d1	reg_sr3_cti_dsad_mode: mode for dsad of cti calculation, 0:block based; 1: other sharp
3	R/W	0d1	reg_sr3_lti_vsad_mode: mode for vsad of lti calculation, 0:block based; 1: other sharp

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Bit(s)	R/W	Default	Description
2	R/W	0d1	reg_sr3_cti_vsad_mode: mode for vsad of cti calculation, 0:block based; 1: other sharp
1	R/W	0d1	reg_sr3_lti_hsad_hlpf: hlpf for hsad of lti calculation, 0:no hlpf; 1: with [1 2 1] hlpf.
0	R/W	0d1	reg_sr3_cti_hsad_hlpf: hlpf for hsad of cti calculation, 0:no hlpf; 1: with [1 2 1] hlpf.

Table 9-1977 SRSHARP1_SR3_PK_CTRL0 0x5262

Bit(s)	R/W	Default	Description
31:12	R/W		reserved
11	R/W	0d1	reg_sr3_pk_sad_mode: mode for sad of peaking calculation, 0: block based; 1: other sharp.
10	R/W	0d1	reg_sr3_pk_hsad_hlpf: hlpf for hsad for peaking calculation,0:no hlpf; 1: with [1 2 2 2 1] hlpf.
9	R/W	0d1	reg_sr3_pk_vsad_hlpf: hlpf for vsad for peaking calculation,0:no hlpf; 1: with [1 2 2 2 1] hlpf.
8	R/W	0d1	reg_sr3_pk_dsad_hlpf: hlpf for dsad for peaking calculation,0:no hlpf; 1: with [1 2 2 2 1] hlpf.
7:6	R/W	0d3	reg_sr3_pk_hpdrt_mode: mode for HPdrt filter
5:4	R/W	0d3	reg_sr3_pk_bpdrt_mode: mode for BPdrt filter
3:2	R/W	0d3	reg_pk_drtbld_range: range of the min2 and min direction distance
1	R/W		reserved
0	R/W	0d0	reg_sr3_pk_ti_blend_mode: blend mode of the TI and PK result

Table 9-1978 SRSHARP1_SR3_PK_CTRL1 0x5263

Bit(s)	R/W	Default	Description
31	R/W		reserved
30:28	R/W	0d1	reg_sr3_pk_Hp_hvcon_replace8_maxsad: replace HP hvcon by maxsad
26:24	R/W	0d1	reg_sr3_pk_bp_hvcon_replace8_maxsad: replace BP hvcon by maxsad
23:16	R/W	0d32	reg_sr3_pk_hp_hvcon_replace8lv_gain: gain to local variant before calculating the hv gain for peaking.
15:8	R/W	0d32	reg_sr3_pk_bp_hvcon_replace8lv_gain: gain to local variant before calculating the hv gain for peaking.
7	R/W	0d1	reg_sr3_sad_intlev_mode: interleave detect xerr mode: 0 max; 1: sum
6	R/W	0d1	reg_sr3_sad_intlev_mode1: mode 1 of using diagonal protection: 1: with diagonal protection
5:0	R/W	0d12	reg_sr3_sad_intlev_gain: interleave detection for sad gain applied, normalized to 8 as 1

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Table 9-1979 SRSHARP1_DEJ_CTRL 0x5264

Bit(s)	R/W	Default	Description
15:8	R/W	8	reg_sr3_dejaggy_hblank
7:4	R/W		reserved
3:2	R/W	0d3	reg_sr3_dejaggy_sameside_prtct: enable of sr3 dejaggy same side curve protect from filter, [0] for proc path; [1] for ctrl path.
1	R/W	0d1	reg_sr3_dejaggy_sameside_mode: mode of sameside flag decision
0	R/W	0d1	reg_sr3_dejaggy_enable: enable of sr3 dejaggy

Table 9-1980 SRSHARP1_DEJ_ALPHA 0x5265

Bit(s)	R/W	Default	Description
31:28	R/W	0d0	reg_sr3_dejaggy_ctrlchrm_alpha_1 : alpha for LR video LPF
27:24	R/W	0d15	reg_sr3_dejaggy_ctrlchrm_alpha_0 : alpha for LR video LPF
23:20	R/W	0d0	reg_sr3_dejaggy_ctrlluma_alpha_1 : alpha for LR video LPF
19:16	R/W	0d15	reg_sr3_dejaggy_ctrlluma_alpha_0 : alpha for LR video LPF
15:12	R/W	0d4	reg_sr3_dejaggy_procchrm_alpha_1: alpha for LR video LPF
11:8	R/W	0d6	reg_sr3_dejaggy_procchrm_alpha_0: alpha for LR video LPF
7:4	R/W	0d4	reg_sr3_dejaggy_procluma_alpha_1: alpha for LR video LPF
3:0	R/W	0d6	reg_sr3_dejaggy_procluma_alpha_0: alpha for LR video LPF

Table 9-1981 SRSHARP1_SR3_DRTLPF_EN 0x5266

Bit(s)	R/W	Default	Description
31:15	R/W		reserved
14:8	R/W	0d0	reg_pk_debug_edge
6:4	R/W	0d0	reg_sr3_drtlpf_theta_en
2:0	R/W	0d7	reg_sr3_drtlpf_enable: directional lpf on Y/U/V channels

Table 9-1982 SRSHARP1_SR3_DRTLPF_ALPHA_0 0x5267

Bit(s)	R/W	Default	Description
31:28	R/W		reserved
27:24	R/W	0d9	reg_sr3_drtlpf_alpha_3
23:20	R/W		reserved
19:16	R/W	0d10	reg_sr3_drtlpf_alpha_2
15:12	R/W		reserved
11:8	R/W	0d11	reg_sr3_drtlpf_alpha_1
7:4	R/W		reserved
3:0	R/W	0d12	reg_sr3_drtlpf_alpha_0: directional lpf alpha coef for min_sad/max_sad compare

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Table 9-1983 SRSHARP1_SR3_DRTLPF_ALPHA_1 0x5268

Bit(s)	R/W	Default	Description
31:28	R/W		reserved
27:24	R/W	0d1	reg_sr3_drtlpf_alpha_7
23:20	R/W		reserved
19:16	R/W	0d4	reg_sr3_drtlpf_alpha_6
15:12	R/W		reserved
11:8	R/W	0d7	reg_sr3_drtlpf_alpha_5
7:4	R/W		reserved
3:0	R/W	0d8	reg_sr3_drtlpf_alpha_4: directional lpf alpha coef for min_sad/max_sad compare

Table 9-1984 SRSHARP1_SR3_DRTLPF_ALPHA_2 0x5269

Bit(s)	R/W	Default	Description
31:28	R/W		reserved
27:24	R/W	0d0	reg_sr3_drtlpf_alpha_11
23:20	R/W		reserved
19:16	R/W	0d0	reg_sr3_drtlpf_alpha_10
15:12	R/W		reserved
11:8	R/W	0d0	reg_sr3_drtlpf_alpha_9
7:4	R/W		reserved
3:0	R/W	0d0	reg_sr3_drtlpf_alpha_8: directional lpf alpha coef for min_sad/max_sad compare

Table 9-1985 SRSHARP1_SR3_DRTLPF_ALPHA_OFST 0x526a

Bit(s)	R/W	Default	Description
31:28	R/W	0	reg_sr3_drtlpf_alpha_ofst7
27:24	R/W	0	reg_sr3_drtlpf_alpha_ofst6
23:20	R/W	0	reg_sr3_drtlpf_alpha_ofst5
19:16	R/W	-2	reg_sr3_drtlpf_alpha_ofst4
15:12	R/W	0	reg_sr3_drtlpf_alpha_ofst3
11:8	R/W	0	reg_sr3_drtlpf_alpha_ofst2
7:4	R/W	0	reg_sr3_drtlpf_alpha_ofst1
3:0	R/W	-2	reg_sr3_drtlpf_alpha_ofst0: directional lpf alpha coef offset of each direction.

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Table 9-1986 SRSHARP1_SR3_DERING_CTRL 0x526b

Bit(s)	R/W	Default	Description
31	R/W		reserved
30:28	R/W	1	reg_sr3_dering_enable: dering enable
27	R/W		reserved
26:24	R/W	3	reg_sr3_dering_varlpf_mode: local variant LPF mode. 0: no filter; 1: errosion 3x3; 2: 3x3 lpf; 3: 3x3 errosion + lpf
23:20	R/W	9	reg_sr3_dering_maxrange: range of dering in LR resolution.
19:18	R/W		reserved
17:16	R/W	2	reg_sr3_dering_lcvar_blend_mode: mode for lcvar calculation. 0:HV blend; 1:diag blend; 2:HV blend + V; 3: HV blend+Diag blend
15:8	R/W	40	reg_sr3_dering_lcvar_gain: gain to local variant and normalized to 32 as 1
7:0	R/W	28	reg_sr3_dering_lcvar_nearby_maxsad_th: threshold to use near side maxsad if that side is larger than this threshold, otherwise use the max one.

Table 9-1987 SRSHARP1_SR3_DERING_LUMA2PKGAIN_0TO3 0x526c

Bit(s)	R/W	Default	Description
31:24	R/W	255	reg_sr3_dering_luma2pkgain3: level limit(for th0 < bpcon < th1) of curve for dering pkgain base on LPF luma level
23:16	R/W	255	reg_sr3_dering_luma2pkgain2: level limit(for bpcon < th0) of curve for dering pkgain base on LPF luma level
15:8	R/W	200	reg_sr3_dering_luma2pkgain1: threshold 1 of curve for dering pkgain based on LPF luma level.
7:0	R/W	30	reg_sr3_dering_luma2pkgain0: threshold 0 of curve for dering pkgain based on LPF luma level.

Table 9-1988 SRSHARP1_SR3_DERING_LUMA2PKGAIN_4TO6 0x526d

Bit(s)	R/W	Default	Description
31:24	R/W		reserved
23:16	R/W	24	reg_sr3_dering_luma2pkgain6: rate1 (for bpcon > th1) of curve for dering pkOS based on LPF luma level.
15:8	R/W	50	reg_sr3_dering_luma2pkgain5: rate0 (for bpcon < th0) of curve for dering pkOS based on LPF luma level.
7:0	R/W	255	reg_sr3_dering_luma2pkgain4: level limit(for bpcon > th1) of curve for dering pkgain base on LPF luma level

Table 9-1989 SRSHARP1_SR3_DERING_LUMA2PKOS_0TO3 0x526e

Bit(s)	R/W	Default	Description
31:24	R/W	255	reg_sr3_dering_luma2pkos3: level limit(for th0 < bpcon < th1) of curve for dering pkOS base on LPF luma level
23:16	R/W	255	reg_sr3_dering_luma2pkos2: level limit(for bpcon < th0) of curve for dering pkOS base on LPF luma level

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Bit(s)	R/W	Default	Description
15:8	R/W	200	reg_sr3_dering_luma2pkos1: threshold 1 of curve for dering pkOS based on LPF luma level.
7:0	R/W	30	reg_sr3_dering_luma2pkos0: threshold 0 of curve for dering pkOS based on LPF luma level.

Table 9-1990 SRSHARP1_SR3_DERING_LUMA2PKOS_4TO6 0x526f

Bit(s)	R/W	Default	Description
31:24	R/W		reserved
23:16	R/W	24	reg_sr3_dering_luma2pkos6: rate1 (for bpcon > th1) of curve for dering pkOS based on LPF luma level.
15:8	R/W	50	reg_sr3_dering_luma2pkos5: rate0 (for bpcon < th0) of curve for dering pkOS based on LPF luma level.
7:0	R/W	255	reg_sr3_dering_luma2pkos4: level limit(for bpcon > th1) of curve for dering pkOS base on LPF luma level

Table 9-1991 SRSHARP1_SR3_DERING_GAINVS_MADSAD 0x5270

Bit(s)	R/W	Default	Description
31:28	R/W	0	reg_sr3_dering_gainvs_maxsad7
27:24	R/W	0	reg_sr3_dering_gainvs_maxsad6
23:20	R/W	0	reg_sr3_dering_gainvs_maxsad5
19:16	R/W	0	reg_sr3_dering_gainvs_maxsad4
15:12	R/W	0	reg_sr3_dering_gainvs_maxsad3
11:8	R/W	0	reg_sr3_dering_gainvs_maxsad2
7:4	R/W	4	reg_sr3_dering_gainvs_maxsad1
3:0	R/W	8	reg_sr3_dering_gainvs_maxsad0: pkgain vs maxsad value, 8 node interpolations.

Table 9-1992 SRSHARP1_SR3_DERING_GAINVS_VR2MAX 0x5271

Bit(s)	R/W	Default	Description
31:28	R/W	15	reg_sr3_dering_gainvs_vr2max7
27:24	R/W	15	reg_sr3_dering_gainvs_vr2max6
23:20	R/W	15	reg_sr3_dering_gainvs_vr2max5
19:16	R/W	15	reg_sr3_dering_gainvs_vr2max4
15:12	R/W	14	reg_sr3_dering_gainvs_vr2max3
11:8	R/W	12	reg_sr3_dering_gainvs_vr2max2
7:4	R/W	2	reg_sr3_dering_gainvs_vr2max1
3:0	R/W	0	reg_sr3_dering_gainvs_vr2max0: pkgain vs ratio

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Table 9-1993 SRSHARP1_SR3_DERING_PARAM0 0x5272

Bit(s)	R/W	Default	Description
31:24	R/W		reserved
23:16	R/W	10	reg_sr3_dering_lcvar_floor
15:8	R/W	32	reg_sr3_dering_vr2max_gain: gain to max before feeding to LUT
7:6	R/W		reserved
5:0	R/W	16	reg_sr3_dering_vr2max_limt: limit of maxsad

Table 9-1994 SRSHARP1_SR3_DRTLPF_THETA 0x5273

Bit(s)	R/W	Default	Description
31:0	R/W	0xfe-c96420	reg_sr3_drtlpf_theta: u4x8 directional lpf beta coef for min_sad/min2_sad compared to x=0:7 correspond to [1:8]/16; 0 means no drtLPF, 15: 100% alpha dependant drtLPF.

Table 9-1995 SRSHARP1_SATPRT_CTRL 0x5274

Bit(s)	R/W	Default	Description
31:28	R/W		reserved
27:16	R/W	5	reg_satprt_sat_core: 4x will be coring to cor(irgb_max-irgb_min) to calculate the oy_delt, the smaller the more protection to color, the larger only the rich color will be protected.
15:8	R/W	64	reg_satprt_sat_rate: rate to cor(irgb_max-irgb_min) to calculate the oy_delt,the larger the more protection to color; norm 16 as 1
7:4	R/W		reserved
3:2	R/W	1	reg_satprt_csc_mode: CSC mode of current yuv input: 0:601; 1:709; 2:BT2020 NCL; 3 reserved
1	R/W	1	reg_satprt_is_lmt: flag telling the YUV is limited range data or full rang data; 1 is limited data
0	R/W	0	reg_satprt_enable: 1 to enable of saturation protection for dnlp adjustments

Table 9-1996 SRSHARP1_SATPRT_DIVM 0x5275

Bit(s)	R/W	Default	Description
31:24	R/W		reserved
23:0	R/W	{128,128,128}	reg_satprt_div_m: u8x3, 1/m, normalized to 128 as 1.

Table 9-1997 SRSHARP1_DB_FLT_CTRL 0x5277

Bit(s)	R/W	Default	Description
26	R/W	0	reg_nrdeband_reset1 : // unsigned , default = 0 0 : no reset seed 1: reload chroma seed
25	R/W	0	reg_nrdeband_reset0 : // unsigned , default = 0 0 : no reset seed 1: reload luma seed

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Bit(s)	R/W	Default	Description
24	R/W	0	reg_nrdeband_rgb : // unsigned , default = 0 0 : yuv 1: RGB
23	R/W	1	reg_nrdeband_en11 : // unsigned , default = 1 debanding registers of side lines, [0] for luma, same for below
22	R/W	1	reg_nrdeband_en10 : // unsigned , default = 1 debanding registers of side lines, [1] for chroma, same for below
21	R/W	1	reg_nrdeband_siderand : // unsigned , default = 1 options to use side two lines use the rand, instead of use for the YUV three component of middle line, 0: seed [3]/bandrand[3] for middle line yuv; 1: seed[3]/bandrand[3] for nearby three lines Y;
20	R/W	0	reg_nrdeband_randmode : // unsigned , default = 0 mode of rand noise adding, 0: same noise strength for all difs; else: strenght of noise will not exceed the difs, MIN((pPKReg- > reg_nrdeband_bandrand[m]), noise[m])
19:17	R/W	6	reg_nrdeband_bandrand2 : // unsigned , default = 6
15:13	R/W	6	reg_nrdeband_bandrand1 : // unsigned , default = 6
11: 9	R/W	6	reg_nrdeband_bandrand0 : // unsigned , default = 6
7	R/W	1	reg_nrdeband_hpxor1 : // unsigned , default = 1 debanding random hp portion xor, [0] for luma
6	R/W	1	reg_nrdeband_hpxor0 : // unsigned , default = 1 debanding random hp portion xor, [1] for chroma
5	R/W	1	reg_nrdeband_en1 : // unsigned , default = 1 debanding registers, for luma
4	R/W	1	reg_nrdeband_en0 : // unsigned , default = 1 debanding registers, for chroma
3: 2	R/W	2	reg_nrdeband_lpf_mode1 : // unsigned , default = 2 lpf mode, 0: 3x3, 1:3x5; 2: 5x5; 3:5x7
1: 0	R/W	2	reg_nrdeband_lpf_mode0 : // unsigned , default = 2 lpf mode, 0: 3x3, 1:3x5; 2: 5x5; 3:5x7

Table 9-1998 SRSHARP1_DB_FLT_YC_THRD 0x5278

Bit(s)	R/W	Default	Description
31:28	R/W	9	reg_nrdeband_luma_th3 : // unsigned , default = 9 threshold to |Y-Ylpf|, if < th[0] use lpf
27:24	R/W	7	reg_nrdeband_luma_th2 : // unsigned , default = 7 elseif < th[1] use (lpf*3 + y)/4
23:20	R/W	6	reg_nrdeband_luma_th1 : // unsigned , default = 6 elseif < th[1] use (lpf*3 + y)/ 4elseif < th[2] (lpf*1 + y)/2
19:16	R/W	5	reg_nrdeband_luma_th0 : // unsigned , default = 5 elseif < th[1] use (lpf*3 + y)/ 4elseif elseif < th[3] (lpf*1 + 3*y)/4; else
15:12	R/W	9	reg_nrdeband_chrm_th3 : // unsigned , default = 9 threshold to |Y-Ylpf|, if < th[0] use lpf
11: 8	R/W	7	reg_nrdeband_chrm_th2 : // unsigned , default = 7 elseif < th[1] use (lpf*3 + y)/4
7: 4	R/W	6	reg_nrdeband_chrm_th1 : // unsigned , default = 6 elseif < th[1] use (lpf*3 + y)/ 4elseif < th[2] (lpf*1 + y)/2
3: 0	R/W	5	reg_nrdeband_chrm_th0 : // unsigned , default = 5 elseif < th[1] use (lpf*3 + y)/ 4elseif elseif

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Table 9-1999 SRSHARP1_DB_FLT_RANDLUT 0x5279

Bit(s)	R/W	Default	Description
23:21	R/W	1	reg_nrdeband_randslut7 : // unsigned , default = 1 lut0
20:18	R/W	1	reg_nrdeband_randslut6 : // unsigned , default = 1 lut0
17:15	R/W	1	reg_nrdeband_randslut5 : // unsigned , default = 1 lut0
14:12	R/W	1	reg_nrdeband_randslut4 : // unsigned , default = 1 lut0
11: 9	R/W	1	reg_nrdeband_randslut3 : // unsigned , default = 1 lut0
8: 6	R/W	1	reg_nrdeband_randslut2 : // unsigned , default = 1 lut0
5: 3	R/W	1	reg_nrdeband_randslut1 : // unsigned , default = 1 lut0
2: 0	R/W	1	reg_nrdeband_randslut0 : // unsigned , default = 1 lut0

Table 9-2000 SRSHARP1_DB_FLT_PXI_THRD 0x527a

Bit(s)	R/W	Default	Description
25:16	R/W	0	reg_nrdeband_yc_th1 : // unsigned , default = 0 to luma/|u/v| for using the denoise
9: 0	R/W	0	reg_nrdeband_yc_th0 : // unsigned , default = 0 to luma/|u/v| for using the denoise

Table 9-2001 SRSHARP1_DB_FLT_SEED_Y 0x527b

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8240	reg_nrdeband_seed0 : // unsigned , default = 1621438240 noise adding seed for Y. seed[0]= 0x60a52f20; as default

Table 9-2002 SRSHARP1_DB_FLT_SEED_U 0x527c

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8247	reg_nrdeband_seed1 : // unsigned , default = 1621438247 noise adding seed for U. seed[0]= 0x60a52f27; as default

Table 9-2003 SRSHARP1_DB_FLT_SEED_V 0x527d

Bit(s)	R/W	Default	Description
31: 0	R/W	162143-8242	reg_nrdeband_seed2 : // unsigned , default = 1621438242 noise adding seed for V. seed[0]= 0x60a52f22; as default

Table 9-2004 SRSHARP1_PKGAIN_VSLUMA_LUT_L 0x527e

Bit(s)	R/W	Default	Description
31:28	R/W	5	reg_pkgain_vsluma_lut7
27:24	R/W	6	reg_pkgain_vsluma_lut6
23:20	R/W	6	reg_pkgain_vsluma_lut5

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Bit(s)	R/W	Default	Description
19:16	R/W	6	reg_pkgain_vsluma_lut4
15:12	R/W	7	reg_pkgain_vsluma_lut3
11:8	R/W	10	reg_pkgain_vsluma_lut2
7:4	R/W	12	reg_pkgain_vsluma_lut1
3:0	R/W	8	reg_pkgain_vsluma_lut0

Table 9-2005 SRSHARP1_PKGAIN_VSLUMA_LUT_H 0x527f

Bit(s)	R/W	Default	Description
31:4	R/W		reserved
3:0	R/W	4	reg_pkgain_vsluma_lut8

Table 9-2006 SRSHARP1_PKOSHT_VSLUMA_LUT_L 0x5280

Bit(s)	R/W	Default	Description
31:28	R/W	5	reg_pkosht_vsluma_lut7
27:24	R/W	6	reg_pkosht_vsluma_lut6
23:20	R/W	6	reg_pkosht_vsluma_lut5
19:16	R/W	6	reg_pkosht_vsluma_lut4
15:12	R/W	7	reg_pkosht_vsluma_lut3
11:8	R/W	10	reg_pkosht_vsluma_lut2
7:4	R/W	12	reg_pkosht_vsluma_lut1
3:0	R/W	8	reg_pkosht_vsluma_lut0

Table 9-2007 SRSHARP1_PKOSHT_VSLUMA_LUT_H 0x5281

Bit(s)	R/W	Default	Description
31:4	R/W		reserved
3:0	R/W	4	reg_pkosht_vsluma_lut8

Table 9-2008 SRSHARP1_SATPRT_LMT_RGB1 0x5282

Bit(s)	R/W	Default	Description
27:16	R/W	0d0	reg_satprt_lmt_g:
11: 0	R/W	0d0	reg_satprt_lmt_r: limit of RGB channel, for limited range RGB, 12bits

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Table 9-2009 SRSHARP1_SATPRT_LMT_RGB2 0x5283

Bit(s)	R/W	Default	Description
31:16	R/W	0d0	reserved
11: 0	R/W	0d0	reg_satprt_lmt_b: limit of RGB channel, for limited range RGB

Table 9-2010 SRSHARP1_SHARP_GATE_CLK_CTRL_0 0x5284

Bit(s)	R/W	Default	Description
31:0	R/W	0d0	Gate clock control [01:00]: sharp input control unit [03:02]: deband unit [05:04]: dejaggy unit [07:06]: dnlp unit [09:08]: demo control unit [11:10]: horiz interp unit

Table 9-2011 SRSHARP1_SHARP_GATE_CLK_CTRL_1 0x5285

Bit(s)	R/W	Default	Description
31:0	R/W	0d0	Gate clock control [01:00]: sr_top “pipe_ctrl” [03:02]: drt [05:04]: ssd [07:06]: cubic [09:08]: edi [11:10]: pkgainsad [13:12]: bicomux [15:14]: bicin_fifo [17:16]: lpf4pkgain_fifo [19:18]: min2hvgain_fifo [21:20]: sad4pkgain_fifo [23:22]: dirminmax4xtl_fifo [25:24]: drtsad8_fifo [27:26]: ssdmax_fifo [29:28]: pkminmax_fifo [31:30]: cirdrtgain_fifo

Table 9-2012 SRSHARP1_SHARP_GATE_CLK_CTRL_2 0x5286

Bit(s)	R/W	Default	Description
31:0	R/W	0d0	Gate clock control [01:00]: bufdiff_fifo [03:02]: osvar_fifo [05:04]: pkhvgain unit [07:06]: pkgain unit [09:08]: TI unit [11:10]: pk unit [13:12]: locvar unit [15:14]: hvconc unit

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Table 9-2013 SRSHARP1_SHARP_GATE_CLK_CTRL_3 0x5287

Bit(s)	R/W	Default	Description
31:0	R/W	0d0	Gate clock control [01:00]: TI, htl Y [03:02]: TI, vti Y [05:04]: TI, htl U [07:06]: TI, vtl U [09:08]: TI, htl V [11:10]: TI, vtl V [13:12]: TI, lumaminmax_fifo [15:14]: TI, chrmminmax fifo

Table 9-2014 SRSHARP1_SHARP_DPS_CTRL 0x5288

Bit(s)	R/W	Default	Description
31:0	R/W	0d0	Power saving control : hvcon : nrssd : os filter : cubic 5 lines to 9 lines : dering : locvar : drtlpf : hlti : hcti : vlti : vcti : lti blend : cti blend : htishort (no used) : nr Y filter : nr C filter : nr belnd : pkti blend : os ctrl : pk HP : pk BP [26:24] dejaggy power saving control [30:28] reserved

Table 9-2015 SRSHARP1_DNLP_00 0x5290

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0010-0008	reg_dnlp_ygrid0:dnlp00 . unsigned , default = 32'h00100008

Table 9-2016 SRSHARP1_DNLP_01 0x5291

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0020-0018	reg_dnlp_ygrid1:dnlp01 . unsigned , default = 32'h00200018

Table 9-2017 SRSHARP1_DNLP_02 0x5292

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0030-0028	reg_dnlp_ygrid2:dnlp02 . unsigned , default = 32'h00300028

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Table 9-2018 SRSHARP1_DNLP_03 0x5293

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0040-0038	reg_dnlp_ygrid3:dnlp03 . unsigned , default = 32'h00400038

Table 9-2019 SRSHARP1_DNLP_04 0x5294

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0050-0048	reg_dnlp_ygrid4:dnlp04 . unsigned , default = 32'h00500048

Table 9-2020 SRSHARP1_DNLP_05 0x5295

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0068-005c	reg_dnlp_ygrid5:dnlp05 . unsigned , default = 32'h0068005c

Table 9-2021 SRSHARP1_DNLP_06 0x5296

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0080-0074	reg_dnlp_ygrid6:dnlp06 . unsigned , default = 32'h00800074

Table 9-2022 SRSHARP1_DNLP_07 0x5297

Bit(s)	R/W	Default	Description
31: 0	R/W	0x00-a00090	reg_dnlp_ygrid7:dnlp07 . unsigned , default = 32'h00a00090

Table 9-2023 SRSHARP1_DNLP_08 0x5298

Bit(s)	R/W	Default	Description
31: 0	R/W	0x00-c000b0	reg_dnlp_ygrid8:dnlp08 . unsigned , default = 32'h00c000b0

Table 9-2024 SRSHARP1_DNLP_09 0x5299

Bit(s)	R/W	Default	Description
31: 0	R/W	0x00-e000d0	reg_dnlp_ygrid9:dnlp09 . unsigned , default = 32'h00e000d0

Table 9-2025 SRSHARP1_DNLP_10 0x529a

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0100-00f0	reg_dnlp_ygrid10:dnlp10 . unsigned , default = 32'h010000f0

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Table 9-2026 SRSHARP1_DNLP_11 0x529b

Bit(s)	R/W	Default	Description
31: 0	R/W	0x012-c0114	reg_dnlp_ygrid11:dnlp11 . unsigned , default = 32'h012c0114

Table 9-2027 SRSHARP1_DNLP_12 0x529c

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0154-0140	reg_dnlp_ygrid12:dnlp12 . unsigned , default = 32'h01540140

Table 9-2028 SRSHARP1_DNLP_13 0x529d

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0180-016c	reg_dnlp_ygrid13:dnlp13 . unsigned , default = 32'h0180016c

Table 9-2029 SRSHARP1_DNLP_14 0x529e

Bit(s)	R/W	Default	Description
31: 0	R/W	0x01-c001a0	reg_dnlp_ygrid14:dnlp14 . unsigned , default = 32'h01c001a0

Table 9-2030 SRSHARP1_DNLP_15 0x529f

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0200-01e0	reg_dnlp_ygrid15:dnlp15 . unsigned , default = 32'h020001e0

Table 9-2031 SRSHARP1_DNLP_16 0x52a0

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0240-0220	reg_dnlp_ygrid16:dnlp16 . unsigned , default = 32'h02400220

Table 9-2032 SRSHARP1_DNLP_17 0x52a1

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0280-0260	reg_dnlp_ygrid17:dnlp17 . unsigned , default = 32'h02800260

Table 9-2033 SRSHARP1_DNLP_18 0x52a2

Bit(s)	R/W	Default	Description
31: 0	R/W	0x02-b00298	reg_dnlp_ygrid18:dnlp18 . unsigned , default = 32'h02b00298

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Table 9-2034 SRSHARP1_DNLP_19 0x52a3

Bit(s)	R/W	Default	Description
31: 0	R/W	0x02-e002c8	reg_dnlp_ygrid19:dnlp19 . unsigned , default = 32'h02e002c8

Table 9-2035 SRSHARP1_DNLP_20 0x52a4

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0300-02f0	reg_dnlp_ygrid20:dnlp20 . unsigned , default = 32'h030002f0

Table 9-2036 SRSHARP1_DNLP_21 0x52a5

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0320-0310	reg_dnlp_ygrid21:dnlp21 . unsigned , default = 32'h03200310

Table 9-2037 SRSHARP1_DNLP_22 0x52a6

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0338-032c	reg_dnlp_ygrid22:dnlp22 . unsigned , default = 32'h0338032c

Table 9-2038 SRSHARP1_DNLP_23 0x52a7

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0350-0348	reg_dnlp_ygrid23:dnlp23 . unsigned , default = 32'h03500348

Table 9-2039 SRSHARP1_DNLP_24 0x52a8

Bit(s)	R/W	Default	Description
31: 0	R/W	0x035-c0358	reg_dnlp_ygrid24:dnlp24 . unsigned , default = 32'h035c0358

Table 9-2040 SRSHARP1_DNLP_25 0x52a9

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0368-0360	reg_dnlp_ygrid25:dnlp25 . unsigned , default = 32'h03680360

Table 9-2041 SRSHARP1_DNLP_26 0x52aa

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0378-0370	reg_dnlp_ygrid26:dnlp26 . unsigned , default = 32'h03780370

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Table 9-2042 SRSHARP1_DNLP_27 0x52ab

Bit(s)	R/W	Default	Description
31: 0	R/W	0x0388-0380	reg_dnlp_ygrid27:dnlp27 . unsigned , default = 32'h03880380

Table 9-2043 SRSHARP1_DNLP_28 0x52ac

Bit(s)	R/W	Default	Description
31: 0	R/W	0x03-a00390	reg_dnlp_ygrid28:dnlp28 . unsigned , default = 32'h03a00390

Table 9-2044 SRSHARP1_DNLP_29 0x52ad

Bit(s)	R/W	Default	Description
31: 0	R/W	0x03-c003b0	reg_dnlp_ygrid29:dnlp29 . unsigned , default = 32'h03c003b0

Table 9-2045 SRSHARP1_DNLP_30 0x52ae

Bit(s)	R/W	Default	Description
31: 0	R/W	0x03-e003d0	reg_dnlp_ygrid30:dnlp30 . unsigned , default = 32'h03e003d0

Table 9-2046 SRSHARP1_DNLP_31 0x52af

Bit(s)	R/W	Default	Description
31: 0	R/W	0x03f-c03f0	reg_dnlp_ygrid31:dnlp31 . unsigned , default = 32'h03fc03f0

Table 9-2047 SRSHARP1_SHARP_SYNC_CTRL 0x52b0

Bit(s)	R/W	Default	Description
15:0	R/W	0d0	Shadow control for some setting: 0 to use VSYNC to shadow : SR all bypass : reg_sr2_bic_pknr_bypass [2] : reg_3d_mode [3] : reg_nrdeband_en11 [4]: reg_nrdeband_en10 [5]: reg_nrdeband_en1 [6]: reg_nrdeband_en0 [7]: reg_dejaggy_enable [8]: reg_sr2_sharp_prc_lr [9]: reg_sharp_pk_en [10]:reg_sharp_nr_en [11]:reg_adp_hlti_en [12]:reg_adp_hcti_en [13]:reg_adp_vlti_en [14]:reg_adp_vcti_en [15]:reg_dnlp_en

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Table 9-2048 SRSHARP1_LC_INPUT_MUX 0x52b1

Bit(s)	R/W	Default	Description
31:7	R/W	0	reserved
6:4	R/W	5	reg_lcinput_ysel: local contrast luma input options 0: org_y; 1: gau_y; 2: gauadp_y; 3: edgadplpf_y; 4: nr_y;5: lti_y; 6: pk_y (before os);7: pk_y (after os)
3	R/W	0	reserved
2:0	R/W	5	reg_lcinput_csel: local contrast chroma input options 0: org_c; 1: gau_c; 2: gauadp_c; 3: edgadplpf_c; 4: nr_c;5: cti_c; 6: pk_c

Table 9-2049 SRSHARP1_NR_GAU_YH_COEF02 0x52b2

Bit(s)	R/W	Default	Description
29:20	R/W	0d32	luma's horizontal adaptive coef0 . signed , default = 32
19:10	R/W	0d32	luma's horizontal adaptive coef1 . signed , default = 32
9:0	R/W	0d16	luma's horizontal adaptive coef2 . signed , default = 16

Table 9-2050 SRSHARP1_NR_GAU_YH_COEF34 0x52b3

Bit(s)	R/W	Default	Description
19:10	R/W	0d0	luma's horizontal adaptive coef3 . signed , default = 0
9:0	R/W	0d0	luma's horizontal adaptive coef4 . signed , default = 0

Table 9-2051 SRSHARP1_NR_GAU_YV_COEF1 0x52b4

Bit(s)	R/W	Default	Description
29:20	R/W	0d32	luma's vertical adaptive coef0 . signed , default = 32
19:10	R/W	0d32	luma's vertical adaptive coef1 . signed , default = 32
9:0	R/W	0d16	luma's vertical adaptive coef2 . signed , default = 16

Table 9-2052 SRSHARP1_NR_GAU_CH_COEF02 0x52b5

Bit(s)	R/W	Default	Description
29:20	R/W	0d32	chroma's horizontal adaptive coef0 . signed , default = 32
19:10	R/W	0d32	chroma's horizontal adaptive coef1 . signed , default = 32
9:0	R/W	0d16	chroma's horizontal adaptive coef2 . signed , default = 16

Table 9-2053 SRSHARP1_NR_GAU_CH_COEF34 0x52b6

Bit(s)	R/W	Default	Description
19:10	R/W	0d0	chroma's horizontal adaptive coef3 . signed , default = 0
9:0	R/W	0d0	chroma's horizontal adaptive coef4 . signed , default = 0

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Table 9-2054 SRSHARP1_NR_GAU_CV_COEF1 0x52b7

Bit(s)	R/W	Default	Description
29:20	R/W	0d32	chroma's vertical adaptive coef0 . signed , default = 32
19:10	R/W	0d32	chroma's vertical adaptive coef1 . signed , default = 32
9:0	R/W	0d16	chroma's vertical adaptive coef2 . signed , default = 16

Table 9-2055 SRSHARP1_DB_FLT_CTRL1 0x52b8

Bit(s)	R/W	Default	Description
17:16	R/W	0d2	reg_nrdeband_noise_rs .unsigned , default = 2
15:12	R/W	0d8	reg_nrdeband_randgain .unsigned , default = 8

Table 9-2056 SRSHARP1_DB_FLT_LUMA_THRD 0x52b9

Bit(s)	R/W	Default	Description
29:24	R/W	36	reg_nrdeband_luma_th3 : // unsigned , default = 36 threshold to |Y-Ylpf|, if < th[0] use lpf
21:16	R/W	28	reg_nrdeband_luma_th2 : // unsigned , default = 28 elseif < th[1] use (lpf*3 + y)/4
13:8	R/W	24	reg_nrdeband_luma_th1 : // unsigned , default = 24 elseif < th[1] use (lpf*3 + y)/ 4elseif < th[2] (lpf*1 + y)/2
5:0	R/W	20	reg_nrdeband_luma_th0 : // unsigned , default = 20 elseif < th[1] use (lpf*3 + y)/ 4elseif elseif < th[3] (lpf*1 + 3*y)/4; else

Table 9-2057 SRSHARP1_DB_FLT_CHRM_THRD 0x52ba

Bit(s)	R/W	Default	Description
29:24	R/W	36	reg_nrdeband_chrm_th3 : // unsigned , default = 36 threshold to |Y-Ylpf|, if < th[0] use lpf
21:16	R/W	28	reg_nrdeband_chrm_th2 : // unsigned , default = 28 elseif < th[1] use (lpf*3 + y)/4
13:8	R/W	24	reg_nrdeband_chrm_th1 : // unsigned , default = 24 elseif < th[1] use (lpf*3 + y)/ 4elseif < th[2] (lpf*1 + y)/2
5:0	R/W	20	reg_nrdeband_chrm_th0 : // unsigned , default = 20 elseif < th[1] use (lpf*3 + y)/ 4elseif elseif < th[3] (lpf*1 + 3*y)/4; else

Table 9-2058 SRSHARP1_LC_TOP_CTRL 0x52c0

Bit(s)	R/W	Default	Description
31:17	R/W	0	reserved
16	R/W	0	reg_lc_sync_ctrl: 0 to shadow reg_lc_enable.
15:8	R/W	8	reg_lc_hblank: blank between two line.
7:5	R/W	0	reserved
4	R/W	0	reg_lc_enable: enable signal for local contrast enhancement, 1-enable; 0 disable

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Bit(s)	R/W	Default	Description
3:1	R/W	0	reserved
0	R/W	0	reg_lc_blkblend_mode:use bilinear interpolation between blocks, 0: no interpolation 1: blender enabled

Table 9-2059 SRSHARP1_LC_HV_NUM 0x52c1

Bit(s)	R/W	Default	Description
31:13	R/W	0	reserved
12:8	R/W	12	reg_lc_blk_hnum: lc processing region number of V, maximum to (STA_LEN_H-1) (0~12)
7:5	R/W	0	reserved
4:0	R/W	8	reg_lc_blk_vnum: lc processing region number of H, maximum to (STA_LEN_V-1) (0~8)

Table 9-2060 SRSHARP1_LC_SAT_LUT_0_1 0x52c2

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	12	reg_lc_satur_lut_0: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	32	reg_lc_satur_lut_1: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2061 SRSHARP1_LC_SAT_LUT_2_3 0x52c3

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	56	reg_lc_satur_lut_2: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	84	reg_lc_satur_lut_3: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2062 SRSHARP1_LC_SAT_LUT_4_5 0x52c4

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	115	reg_lc_satur_lut_4: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	149	reg_lc_satur_lut_5: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

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Table 9-2063 SRSHARP1_LC_SAT_LUT_6_7 0x52c5

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	185	reg_lc_satur_lut_6: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	223	reg_lc_satur_lut_7: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2064 SRSHARP1_LC_SAT_LUT_8_9 0x52c6

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	263	reg_lc_satur_lut_8: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	305	reg_lc_satur_lut_9: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2065 SRSHARP1_LC_SAT_LUT_10_11 0x52c7

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	348	reg_lc_satur_lut_10: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	393	reg_lc_satur_lut_11: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2066 SRSHARP1_LC_SAT_LUT_12_13 0x52c8

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	440	reg_lc_satur_lut_12: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	488	reg_lc_satur_lut_13: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2067 SRSHARP1_LC_SAT_LUT_14_15 0x52c9

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	537	reg_lc_satur_lut_14: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

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Bit(s)	R/W	Default	Description
15:12	R/W	0	reserved
11:0	R/W	588	reg_lc_satur_lut_15: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2068 SRSHARP1_LC_SAT_LUT_16_17 0x52ca

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	640	reg_lc_satur_lut_16: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	694	reg_lc_satur_lut_17: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2069 SRSHARP1_LC_SAT_LUT_18_19 0x52cb

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	748	reg_lc_satur_lut_18: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	804	reg_lc_satur_lut_19: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2070 SRSHARP1_LC_SAT_LUT_20_21 0x52cc

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	861	reg_lc_satur_lut_20: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	919	reg_lc_satur_lut_21: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2071 SRSHARP1_LC_SAT_LUT_22_23 0x52cd

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	978	reg_lc_satur_lut_22: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	1038	reg_lc_satur_lut_23: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

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Table 9-2072 SRSHARP1_LC_SAT_LUT_24_25 0x52ce

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	1099	reg_lc_satur_lut_24: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	1161	reg_lc_satur_lut_25: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2073 SRSHARP1_LC_SAT_LUT_26_27 0x52cf

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	1224	reg_lc_satur_lut_26: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	1287	reg_lc_satur_lut_27: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2074 SRSHARP1_LC_SAT_LUT_28_29 0x52d0

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	1352	reg_lc_satur_lut_28: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	1418	reg_lc_satur_lut_29: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2075 SRSHARP1_LC_SAT_LUT_30_31 0x52d1

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	1485	reg_lc_satur_lut_30: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	1552	reg_lc_satur_lut_31: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2076 SRSHARP1_LC_SAT_LUT_32_33 0x52d2

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	1620	reg_lc_satur_lut_32: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

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Bit(s)	R/W	Default	Description
15:12	R/W	0	reserved
11:0	R/W	1690	reg_lc_satur_lut_33: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2077 SRSHARP1_LC_SAT_LUT_34_35 0x52d3

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	1760	reg_lc_satur_lut_34: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	1830	reg_lc_satur_lut_35: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2078 SRSHARP1_LC_SAT_LUT_36_37 0x52d4

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	1902	reg_lc_satur_lut_36: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	1974	reg_lc_satur_lut_37: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2079 SRSHARP1_LC_SAT_LUT_38_39 0x52d5

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	2047	reg_lc_satur_lut_38: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	2121	reg_lc_satur_lut_39: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2080 SRSHARP1_LC_SAT_LUT_40_41 0x52d6

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	2196	reg_lc_satur_lut_40: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	2271	reg_lc_satur_lut_41: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

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Table 9-2081 SRSHARP1_LC_SAT_LUT_42_43 0x52d7

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	2347	reg_lc_satur_lut_42: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	2424	reg_lc_satur_lut_43: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2082 SRSHARP1_LC_SAT_LUT_44_45 0x52d8

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	2502	reg_lc_satur_lut_44: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	2580	reg_lc_satur_lut_45: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2083 SRSHARP1_LC_SAT_LUT_46_47 0x52d9

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	2659	reg_lc_satur_lut_46: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	2738	reg_lc_satur_lut_47: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2084 SRSHARP1_LC_SAT_LUT_48_49 0x52da

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	2818	reg_lc_satur_lut_48: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	2899	reg_lc_satur_lut_49: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2085 SRSHARP1_LC_SAT_LUT_50_51 0x52db

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	2981	reg_lc_satur_lut_50: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

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Bit(s)	R/W	Default	Description
15:12	R/W	0	reserved
11:0	R/W	3063	reg_lc_satur_lut_51: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2086 SRSHARP1_LC_SAT_LUT_52_53 0x52dc

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	3146	reg_lc_satur_lut_52: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	3229	reg_lc_satur_lut_53: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2087 SRSHARP1_LC_SAT_LUT_54_55 0x52dd

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	3313	reg_lc_satur_lut_54: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	3398	reg_lc_satur_lut_55: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2088 SRSHARP1_LC_SAT_LUT_56_57 0x52de

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	3483	reg_lc_satur_lut_56: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	3569	reg_lc_satur_lut_57: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2089 SRSHARP1_LC_SAT_LUT_58_59 0x52df

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	3655	reg_lc_satur_lut_58: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	3742	reg_lc_satur_lut_59: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

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Table 9-2090 SRSHARP1_LC_SAT_LUT_60_61 0x52e0

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	3830	reg_lc_satur_lut_60: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2
15:12	R/W	0	reserved
11:0	R/W	3918	reg_lc_satur_lut_61: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2091 SRSHARP1_LC_SAT_LUT_62 0x52e1

Bit(s)	R/W	Default	Description
31:12	R/W	0	reserved
11:0	R/W	4007	reg_lc_satur_lut_62: saturation protection curve, normalized to 4096 as 1, default = y=x^1.2

Table 9-2092 SRSHARP1_LC_CURVE_BLK_HIDX_0_1 0x52e2

Bit(s)	R/W	Default	Description
31:30	R/W	0	reserved
29:16	R/W	0	reg_lc_blk_hidx_0: block boundary x-index
15:14	R/W	0	reserved
13:0	R/W	320	reg_lc_blk_hidx_1: block boundary x-index

Table 9-2093 SRSHARP1_LC_CURVE_BLK_HIDX_2_3 0x52e3

Bit(s)	R/W	Default	Description
31:30	R/W	0	reserved
29:16	R/W	640	reg_lc_blk_hidx_2: block boundary x-index
15:14	R/W	0	reserved
13:0	R/W	960	reg_lc_blk_hidx_3: block boundary x-index

Table 9-2094 SRSHARP1_LC_CURVE_BLK_HIDX_4_5 0x52e4

Bit(s)	R/W	Default	Description
31:30	R/W	0	reserved
29:16	R/W	1280	reg_lc_blk_hidx_4: block boundary x-index
15:14	R/W	0	reserved
13:0	R/W	1600	reg_lc_blk_hidx_5: block boundary x-index

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Table 9-2095 SRSHARP1_LC_CURVE_BLK_HIDX_6_7 0x52e5

Bit(s)	R/W	Default	Description
31:30	R/W	0	reserved
29:16	R/W	1920	reg_lc_blk_hidx_6: block boundary x-index
15:14	R/W	0	reserved
13:0	R/W	2240	reg_lc_blk_hidx_7: block boundary x-index

Table 9-2096 SRSHARP1_LC_CURVE_BLK_HIDX_8_9 0x52e6

Bit(s)	R/W	Default	Description
31:30	R/W	0	reserved
29:16	R/W	2560	reg_lc_blk_hidx_8: block boundary x-index
15:14	R/W	0	reserved
13:0	R/W	2880	reg_lc_blk_hidx_9: block boundary x-index

Table 9-2097 SRSHARP1_LC_CURVE_BLK_HIDX_10_11 0x52e7

Bit(s)	R/W	Default	Description
31:30	R/W	0	reserved
29:16	R/W	3200	reg_lc_blk_hidx_10: block boundary x-index
15:14	R/W	0	reserved
13:0	R/W	3520	reg_lc_blk_hidx_11: block boundary x-index

Table 9-2098 SRSHARP1_LC_CURVE_BLK_HIDX_12 0x52e8

Bit(s)	R/W	Default	Description
31:14	R/W	0	reserved
13:0	R/W	3840	reg_lc_blk_hidx_1: block boundary x-index

Table 9-2099 SRSHARP1_LC_CURVE_BLK_VIDX_0_1 0x52e9

Bit(s)	R/W	Default	Description
31:30	R/W	0	reserved
29:16	R/W	0	reg_lc_blk_vidx_0: block boundary y-index
15:14	R/W	0	reserved
13:0	R/W	270	reg_lc_blk_vidx_1: block boundary y-index

Table 9-2100 SRSHARP1_LC_CURVE_BLK_VIDX_2_3 0x52ea

Bit(s)	R/W	Default	Description
31:30	R/W	0	reserved
29:16	R/W	540	reg_lc_blk_vidx_2: block boundary y-index

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Bit(s)	R/W	Default	Description
15:14	R/W	0	reserved
13:0	R/W	810	reg_lc_blk_vidx_3: block boundary y-index

Table 9-2101 SRSHARP1_LC_CURVE_BLK_VIDX_4_5 0x52eb

Bit(s)	R/W	Default	Description
31:30	R/W	0	reserved
29:16	R/W	1080	reg_lc_blk_vidx_4: block boundary y-index
15:14	R/W	0	reserved
13:0	R/W	1350	reg_lc_blk_vidx_5: block boundary y-index

Table 9-2102 SRSHARP1_LC_CURVE_BLK_VIDX_6_7 0x52ec

Bit(s)	R/W	Default	Description
31:30	R/W	0	reserved
29:16	R/W	1620	reg_lc_blk_vidx_6: block boundary y-index
15:14	R/W	0	reserved
13:0	R/W	1890	reg_lc_blk_vidx_7: block boundary y-index

Table 9-2103 SRSHARP1_LC_CURVE_BLK_HIDX_8 0x52ed

Bit(s)	R/W	Default	Description
31:14	R/W	0	reserved
13:0	R/W	2160	reg_lc_blk_vidx_8: block boundary y-index

Table 9-2104 SRSHARP1_LC_YUV2RGB_MAT_0_1 0x52ee

Bit(s)	R/W	Default	Description
31:29	R/W	0	reserved
28:16	R/W	1192	reg_lc_yuv2rgb_mat3x3_0: yuv2rgb 3x3 matrix
15:13	R/W	0	reserved
12:0	R/W	0	reg_lc_yuv2rgb_mat3x3_1: yuv2rgb 3x3 matrix

Table 9-2105 SRSHARP1_LC_YUV2RGB_MAT_2_3 0x52ef

Bit(s)	R/W	Default	Description
31:29	R/W	0	reserved
28:16	R/W	1836	reg_lc_yuv2rgb_mat3x3_2: yuv2rgb 3x3 matrix
15:13	R/W	0	reserved
12:0	R/W	1192	reg_lc_yuv2rgb_mat3x3_3: yuv2rgb 3x3 matrix

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Table 9-2106 SRSHARP1_LC_YUV2RGB_MAT_4_5 0x52f0

Bit(s)	R/W	Default	Description
31:29	R/W	0	reserved
28:16	R/W	-218	reg_lc_yuv2rgb_mat3x3_4: yuv2rgb 3x3 matrix
15:13	R/W	0	reserved
12:0	R/W	-514	reg_lc_yuv2rgb_mat3x3_5: yuv2rgb 3x3 matrix

Table 9-2107 SRSHARP1_LC_YUV2RGB_MAT_6_7 0x52f1

Bit(s)	R/W	Default	Description
31:29	R/W	0	reserved
28:16	R/W	1192	reg_lc_yuv2rgb_mat3x3_6: yuv2rgb 3x3 matrix
15:13	R/W	0	reserved
12:0	R/W	2166	reg_lc_yuv2rgb_mat3x3_7: yuv2rgb 3x3 matrix

Table 9-2108 SRSHARP1_LC_YUV2RGB_MAT_8 0x52f2

Bit(s)	R/W	Default	Description
31:13	R/W	0	reserved
12:0	R/W	0	reg_lc_yuv2rgb_mat3x3_8: yuv2rgb 3x3 matrix

Table 9-2109 SRSHARP1_LC_RGB2YUV_MAT_0_1 0x52f3

Bit(s)	R/W	Default	Description
31:29	R/W	0	reserved
28:16	R/W	187	reg_lc_rgb2yuv_mat3x3_0: rgb2yuv 3x3 matrix
15:13	R/W	0	reserved
12:0	R/W	629	reg_lc_rgb2yuv_mat3x3_1: rgb2yuv 3x3 matrix

Table 9-2110 SRSHARP1_LC_RGB2YUV_MAT_2_3 0x52f4

Bit(s)	R/W	Default	Description
31:29	R/W	0	reserved
28:16	R/W	63	reg_lc_rgb2yuv_mat3x3_2: rgb2yuv 3x3 matrix
15:13	R/W	0	reserved
12:0	R/W	-103	reg_lc_rgb2yuv_mat3x3_3: rgb2yuv 3x3 matrix

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Table 9-2111 SRSHARP1_LC_RGB2YUV_MAT_4_5 0x52f5

Bit(s)	R/W	Default	Description
31:29	R/W	0	reserved
28:16	R/W	-346	reg_lc_rgb2yuv_mat3x3_4: rgb2yuv 3x3 matrix
15:13	R/W	0	reserved
12:0	R/W	450	reg_lc_rgb2yuv_mat3x3_5: rgb2yuv 3x3 matrix

Table 9-2112 SRSHARP1_LC_RGB2YUV_MAT_6_7 0x52f6

Bit(s)	R/W	Default	Description
31:29	R/W	0	reserved
28:16	R/W	450	reg_lc_rgb2yuv_mat3x3_6: rgb2yuv 3x3 matrix
15:13	R/W	0	reserved
12:0	R/W	-409	reg_lc_rgb2yuv_mat3x3_7: rgb2yuv 3x3 matrix

Table 9-2113 SRSHARP1_LC_RGB2YUV_MAT_8 0x52f7

Bit(s)	R/W	Default	Description
31:13	R/W	0	reserved
12:0	R/W	41	reg_lc_rgb2yuv_mat3x3_8: rgb2yuv 3x3 matrix

Table 9-2114 SRSHARP1_LC_YUV2RGB_OFST 0x52f8

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	64	reg_lc_yuv2rgb_ofset_0: yuv2rgb pre-offset to yuv
15:12	R/W	0	reserved
11:0	R/W	512	reg_lc_yuv2rgb_ofset_1: yuv2rgb pre-offset to yuv

Table 9-2115 SRSHARP1_LC_YUV2RGB_CLIP 0x52f9

Bit(s)	R/W	Default	Description
31:30	R/W	0	reserved
29:28	R/W	0	reg_lc_yuv2rgb_rs: matrix normalization right shift extra bits, norm= (1 < < (8 +rs))
27:16	R/W	0	reg_lc_yuv2rgb_clip_0: yuv2rgb converted RGB clipping range
15:12	R/W	0	reserved
11:0	R/W	1023	reg_lc_yuv2rgb_clip_1: yuv2rgb converted RGB clipping range

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Table 9-2116 SRSHARP1_LC_RGB2YUV_OFST 0x52fa

Bit(s)	R/W	Default	Description
31:28	R/W	0	reserved
27:16	R/W	64	reg_lc_rgb2yuv_ofset_0: rgb2yuv post-offset to yuv
15:12	R/W	0	reserved
11:0	R/W	512	reg_lc_rgb2yuv_ofset_1: rgb2yuv post-offset to yuv

Table 9-2117 SRSHARP1_LC_RGB2YUV_CLIP 0x52fb

Bit(s)	R/W	Default	Description
31:30	R/W	0	reserved
29:28	R/W	0	reg_lc_rgb2yuv_rs: matrix normalization right shift extra bits, norm= (1 < < (10 +rs))
27:16	R/W	0	reg_lc_rgb2yuv_clip_0: rgb2yuv converted YUV clipping range
15:12	R/W	0	reserved
11:0	R/W	1023	reg_lc_rgb2yuv_clip_1: rgb2yuv converted YUV clipping range

Table 9-2118 SRSHARP1_LC_MAP_RAM_CTRL 0x52fc

Bit(s)	R/W	Default	Description
31:1	R/W	0	reserved
0	R/W	0	reg_lc_cbus2ram_en: 1 to enable CBUS write/read data to/from LC MAP RAM

Table 9-2119 SRSHARP1_LC_MAP_RAM_ADDR 0x52fd

Bit(s)	R/W	Default	Description
31	W	0	1 to pre-read from LC MAP RAM to CBUS
30:7	R/W	0	reserved
6:4	R/W	0	Vidx of LC MAP RAM
3:0	R/W	0	Hidx of LC MAP RA:

Table 9-2120 SRSHARP1_LC_MAP_RAM_DATA 0x52fe

Bit(s)	R/W	Default	Description
31:30	R/W	0	reserved
29:0	R/W	0	LC MAP RAM data for write/read

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Table 9-2121 SRSHARP1_FMETER_CTRL 0x5289

Bit(s)	R/W	Default	Description
11:10	R/W	0	reg_fmeter_vwin_mm : vertical window size, 0:1 cloumn,1:3cloumn, 2or3:5cloumn.unsigned,default = 0
9:8	R/W	0	reg_fmeter_hwin_mm : horizontal window size, 0:1x7, 1:1x9, 2or3: 1x11 .unsigned , default = 0
7	R/W	0	reg_fmeter_d2_mode : selectino filter D2, 0: [0 -2 0 0 2], 1: [-2 0 0 0 2] .unsigned , default = 0
6	R/W	0	reg_fmeter_v2_mode : selection filter V2, 0: [0 -2 0 0 2], 1: [-2 0 0 0 2] .unsigned , default = 0
5:4	R/W	0	reg_fmeter_h2_mode: selection filter H2, 0: [0 0 0 -2 0 0 2 0 0], 1: [-2 0 0 0 2], 2or3: [0-2 0 0 0 0 0 2 0] .unsigned , default = 0
0	R/W	0	reg_freq_meter_en: freq meter enable .unsigned , default = 0

Table 9-2122 SRSHARP1_FMETER_WIN_HOR 0x528a

Bit(s)	R/W	Default	Description
28:16	R/W	1920	reg_fmeter_xwin_ed: window location: hend .unsigned , default = 1920
12:0	R/W	0	reg_fmeter_xwin_st: window location: hstart .unsigned , default = 0

Table 9-2123 SRSHARP1_FMETER_WIN_VER 0x528b

Bit(s)	R/W	Default	Description
28:16	R/W	1080	reg_fmeter_ywin_ed: window location: vend .unsigned , default = 1080
12:0	R/W	0	reg_fmeter_ywin_st: window location: vstart .unsigned , default = 0

Table 9-2124 SRSHARP1_FMETER_CORING 0x528c

Bit(s)	R/W	Default	Description
31:24	R/W	4	reg_fmeter_low_bound: low bound for threshold .unsigned , default = 4
23:16	R/W	4	reg_fmeter_coring_d: coring of diff before compare with threshold for diagonal frequency .unsigned , default = 4
15:8	R/W	4	reg_fmeter_coring_v: coring of diff before compare with threshold for vertical frequency .unsigned , default = 4
7:0	R/W	4	reg_fmeter_coring_h: coring of diff before compare with threshold for horizontal frequency .unsigned , default = 4

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Table 9-2125 SRSHARP1_FMETER_RATIO_H 0x528d

Bit(s)	R/W	Default	Description
21:16	R/W	16	reg_fmeter_ratio_h2: ratio for threshold calc. for horizontal frequency, 16 is normalized as "1" .unsigned , default = 16
13:8	R/W	16	reg_fmeter_ratio_h1: ratio for threshold calc. for horizontal frequency, 16 is normalized as "1" .unsigned , default = 16
5:0	R/W	16	reg_fmeter_ratio_h0: ratio for threshold calc. for horizontal frequency, 16 is normalized as "1" .unsigned , default = 16

Table 9-2126 SRSHARP1_FMETER_RATIO_V 0x528e

Bit(s)	R/W	Default	Description
21:16	R/W	16	reg_fmeter_ratio_v2: ratio for threshold calc. for vertical frequency, 16 is normalized as "1" .unsigned , default = 16
13:8	R/W	16	reg_fmeter_ratio_v1: ratio for threshold calc. for vertical frequency, 16 is normalized as "1" .unsigned , default = 16
5:0	R/W	16	reg_fmeter_ratio_v0: ratio for threshold calc. for vertical frequency, 16 is normalized as "1" .unsigned , default = 16

Table 9-2127 SRSHARP1_FMETER_RATIO_D 0x528f

Bit(s)	R/W	Default	Description
21:16	R/W	16	reg_fmeter_ratio_d2: ratio for threshold calc. for diagonal frequency, 16 is normalized as "1" .unsigned , default = 16
13:8	R/W	16	reg_fmeter_ratio_d1: ratio for threshold calc. for diagonal frequency, 16 is normalized as "1" .unsigned , default = 16
5:0	R/W	16	reg_fmeter_ratio_d0: ratio for threshold calc. for diagonal frequency, 16 is normalized as "1" .unsigned , default = 16

Table 9-2128 SRSHARP1_RO_FMETER_HCNT_TYPE0 0x5246

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_hcnt_type0: count for horizontal frequency

Table 9-2129 SRSHARP1_RO_FMETER_HCNT_TYPE1 0x5247

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_hcnt_type1: count for horizontal frequency

Table 9-2130 SRSHARP1_RO_FMETER_HCNT_TYPE2 0x5248

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_hcnt_type2: count for horizontal frequency

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Table 9-2131 SRSHARP1_RO_FMETER_HCNT_TYPE3 0x5249

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_hcnt_type3: count for horizontal frequency

Table 9-2132 SRSHARP1_RO_FMETER_VCNT_TYPE0 0x524a

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_vcnt_type0: count for vertical frequency

Table 9-2133 SRSHARP1_RO_FMETER_VCNT_TYPE1 0x524b

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_vcnt_type1: count for vertical frequency

Table 9-2134 SRSHARP1_RO_FMETER_VCNT_TYPE2 0x524c

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_vcnt_type2: count for vertical frequency

Table 9-2135 SRSHARP1_RO_FMETER_VCNT_TYPE3 0x524d

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_vcnt_type3: count for vertical frequency

Table 9-2136 SRSHARP1_RO_FMETER_PDCNT_TYPE0 0x524e

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_pdcnt_type0: count for positive diagonal frequency

Table 9-2137 SRSHARP1_RO_FMETER_PDCNT_TYPE1 0x524f

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_pdcnt_type1: count for positive diagonal frequency

Table 9-2138 SRSHARP1_RO_FMETER_PDCNT_TYPE2 0x5250

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_pdcnt_type2: count for positive diagonal frequency

Table 9-2139 SRSHARP1_RO_FMETER_PDCNT_TYPE3 0x5251

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_pdcnt_type3: count for positive diagonal frequency

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Table 9-2140 SRSHARP1_RO_FMETER_NDCNT_TYPE0 0x5252

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_ndcnt_type0: count for negitive diagonal frequency

Table 9-2141 SRSHARP1_RO_FMETER_NDCNT_TYPE1 0x5253

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_ndcnt_type1: count for negitive diagonal frequency

Table 9-2142 SRSHARP1_RO_FMETER_NDCNT_TYPE2 0x5254

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_ndcnt_type2: count for negitive diagonal frequency

Table 9-2143 SRSHARP1_RO_FMETER_NDCNT_TYPE3 0x5255

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_fmeter_ndcnt_type3: count for negitive diagonal frequency

Table 9-2144 SRSHARP1_SR7_DRTLPF_EN 0x5300

Bit(s)	R/W	Default	Description
31:11			reserved
10	RW	0	reg_sr7_drtlpf_beta_en2: enable of direction ambiguity protection for drt_lpf, beta for drt filter coef base on the x=cal_drt_dif8(min_idx,min2_idx)
9	RW	0	reg_sr7_drtlpf_beta_en1: enable of direction ambiguity protection for drt_lpf, beta for drt filter coef base on the x=cal_drt_dif8(min_idx,min2_idx)
8	RW	0	reg_sr7_drtlpf_beta_en0: enable of direction ambiguity protection for drt_lpf, beta for drt filter coef base on the x=cal_drt_dif8(min_idx,min2_idx)
7:6			reserved
5	RW	0	reg_sr7_drtlpf_edge_en2: enable of direction lpf based on edge strength
4	RW	0	reg_sr7_drtlpf_edge_en1: enable of direction lpf based on edge strength
3	RW	0	reg_sr7_drtlpf_edge_en0: enable of direction lpf based on edge strength
2	RW	1	reg_sr7_drtlpf_sdfd_en2: sdfd gamma (HF burst compare to real edge protection) enable
1	RW	1	reg_sr7_drtlpf_sdfd_en1: sdfd gamma (HF burst compare to real edge protection) enable.
0	RW	1	reg_sr7_drtlpf_sdfd_en0: sdfd gamma (HF burst compare to real edge protection) enable.

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Table 9-2145 SRSHARP1_SR7_DRTLPF_BETA 0x5301

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	0	reg_sr7_drtlpf_beta3: beta for drt filter coef base on the x=cal_drt_dif8(min_idx, min2_idx)
11:8	RW	4	reg_sr7_drtlpf_beta2: beta for drt filter coef base on the x=cal_drt_dif8(min_idx, min2_idx)
7:4	RW	8	reg_sr7_drtlpf_beta1: beta for drt filter coef base on the x=cal_drt_dif8(min_idx, min2_idx)
3:0	RW	15	reg_sr7_drtlpf_beta0: beta for drt filter coef base on the x=cal_drt_dif8(min_idx, min2_idx), beta = lut[x-1], the larger of x, means the higher possibility for ambiguilty, beta=0 use org wo lpf.

Table 9-2146 SRSHARP1_SR7_PKBLD_BETA 0x5302

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	0	reg_sr7_pkdrtbld_beta3: beta for drt and cir blend base on the x=cal_drt_dif8 (min_idx,min2_idx)
11:8	RW	4	reg_sr7_pkdrtbld_beta2: beta for drt and cir blend base on the x=cal_drt_dif8 (min_idx,min2_idx)
7:4	RW	8	reg_sr7_pkdrtbld_beta1: beta for drt and cir blend base on the x=cal_drt_dif8 (min_idx,min2_idx)
3:0	RW	15	reg_sr7_pkdrtbld_beta0: beta for drt and cir blend base on the x=cal_drt_dif8 (min_idx,min2_idx), beta = lut[x-1], the larger of x, means the higher possibility for ambiguilty, beta=0 use org wo lpf.

Table 9-2147 SRSHARP1_SR7_XLTIBLD_BETA 0x5303

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	0	reg_sr7_xlti_dcbld_beta3: beta for denoise and org dc blend base on the x=cal_ drt_dif8(min_idx,min2_idx)
11:8	RW	4	reg_sr7_xlti_dcbld_beta2: beta for denoise and org dc blend base on the x=cal_ drt_dif8(min_idx,min2_idx)
7:4	RW	8	reg_sr7_xlti_dcbld_beta1: beta for denoise and org dc blend base on the x=cal_ drt_dif8(min_idx,min2_idx)
3:0	RW	15	reg_sr7_xlti_dcbld_beta0: beta for denoise and org dc blend base on the x=cal_ drt_dif8(min_idx,min2_idx) beta = lut[x-1], the larger of x, means the higher possibility for ambiguilty, beta=0 use org wo lpf.

Table 9-2148 SRSHARP1_SR7_DRTLPF_EDGE0 0x5304

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_drtlpf_edge7: edge lamda for drt lpf base on max_sad [0:16:128~255]
27:24	RW	15	reg_sr7_drtlpf_edge6: edge lamda for drt lpf base on max_sad [0:16:128~255]

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Bit(s)	R/W	Default	Description
23:20	RW	15	reg_sr7_drtlpf_edge5: edge lamda for drt lpf base on max_sad [0:16:128~255]
19:16	RW	15	reg_sr7_drtlpf_edge4: edge lamda for drt lpf base on max_sad [0:16:128~255]
15:12	RW	15	reg_sr7_drtlpf_edge3: edge lamda for drt lpf base on max_sad [0:16:128~255]
11:8	RW	15	reg_sr7_drtlpf_edge2: edge lamda for drt lpf base on max_sad [0:16:128~255]
7:4	RW	15	reg_sr7_drtlpf_edge1: edge lamda for drt lpf base on max_sad [0:16:128~255]
3:0	RW	15	reg_sr7_drtlpf_edge0: edge lamda for drt lpf base on max_sad [0:16:128~255]

Table 9-2149 SRSHARP1_SR7_DRTLPF_EDGE1 0x5305

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_drtlpf_edge15: edge lamda for drt lpf base on max_sad [0:16:128~255]
27:24	RW	15	reg_sr7_drtlpf_edge14: edge lamda for drt lpf base on max_sad [0:16:128~255]
23:20	RW	15	reg_sr7_drtlpf_edge13: edge lamda for drt lpf base on max_sad [0:16:128~255]
19:16	RW	15	reg_sr7_drtlpf_edge12: edge lamda for drt lpf base on max_sad [0:16:128~255]
15:12	RW	15	reg_sr7_drtlpf_edge11: edge lamda for drt lpf base on max_sad [0:16:128~255]
11:8	RW	15	reg_sr7_drtlpf_edge10: edge lamda for drt lpf base on max_sad [0:16:128~255]
7:4	RW	15	reg_sr7_drtlpf_edge9: edge lamda for drt lpf base on max_sad [0:16:128~255]
3:0	RW	15	reg_sr7_drtlpf_edge8: edge lamda for drt lpf base on max_sad [0:16:128~255]

Table 9-2150 SRSHARP1_SR7_DRTLPF_SDCOR0 0x5306

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_drtlpf_sdcor7: gamma for drt lpf base on SD'[0:16:128~255]
27:24	RW	15	reg_sr7_drtlpf_sdcor6: gamma for drt lpf base on SD'[0:16:128~255]
23:20	RW	15	reg_sr7_drtlpf_sdcor5: gamma for drt lpf base on SD'[0:16:128~255]
19:16	RW	15	reg_sr7_drtlpf_sdcor4: gamma for drt lpf base on SD'[0:16:128~255]
15:12	RW	15	reg_sr7_drtlpf_sdcor3: gamma for drt lpf base on SD'[0:16:128~255]
11:8	RW	15	reg_sr7_drtlpf_sdcor2: gamma for drt lpf base on SD'[0:16:128~255]
7:4	RW	15	reg_sr7_drtlpf_sdcor1: gamma for drt lpf base on SD'[0:16:128~255]
3:0	RW	15	reg_sr7_drtlpf_sdcor0: gamma for drt lpf base on SD'[0:16:128~255]

Table 9-2151 SRSHARP1_SR7_DRTLPF_SDCOR1 0x5307

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_drtlpf_sdcor15: gamma for drt lpf base on SD'[0:16:128~255]
27:24	RW	15	reg_sr7_drtlpf_sdcor14: gamma for drt lpf base on SD'[0:16:128~255]
23:20	RW	15	reg_sr7_drtlpf_sdcor13: gamma for drt lpf base on SD'[0:16:128~255]
19:16	RW	15	reg_sr7_drtlpf_sdcor12: gamma for drt lpf base on SD'[0:16:128~255]

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Bit(s)	R/W	Default	Description
15:12	RW	15	reg_sr7_drtlpf_sdcor11: gamma for drt lpf base on SD'[0:16:128~255]
11:8	RW	15	reg_sr7_drtlpf_sdcor10: gamma for drt lpf base on SD'[0:16:128~255]
7:4	RW	15	reg_sr7_drtlpf_sdcor9: gamma for drt lpf base on SD'[0:16:128~255]
3:0	RW	15	reg_sr7_drtlpf_sdcor8: gamma for drt lpf base on SD'[0:16:128~255]

Table 9-2152 SRSHARP1_SR7_CTIGAIN_SDCOR0 0x5308

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_ctigain_sdcor7: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
27:24	RW	15	reg_sr7_ctigain_sdcor6: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
23:20	RW	15	reg_sr7_ctigain_sdcor5: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
19:16	RW	15	reg_sr7_ctigain_sdcor4: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
15:12	RW	15	reg_sr7_ctigain_sdcor3: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
11:8	RW	15	reg_sr7_ctigain_sdcor2: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
7:4	RW	15	reg_sr7_ctigain_sdcor1: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
3:0	RW	15	reg_sr7_ctigain_sdcor0: adaptive gamma for cti boost gain base on SD'[0:16:128~255]

Table 9-2153 SRSHARP1_SR7_CTIGAIN_SDCOR1 0x5309

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_ctigain_sdcor15: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
27:24	RW	15	reg_sr7_ctigain_sdcor14: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
23:20	RW	15	reg_sr7_ctigain_sdcor13: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
19:16	RW	15	reg_sr7_ctigain_sdcor12: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
15:12	RW	15	reg_sr7_ctigain_sdcor11: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
11:8	RW	15	reg_sr7_ctigain_sdcor10: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
7:4	RW	15	reg_sr7_ctigain_sdcor9: adaptive gamma for cti boost gain base on SD'[0:16:128~255]
3:0	RW	15	reg_sr7_ctigain_sdcor8: adaptive gamma for cti boost gain base on SD'[0:16:128~255]

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Table 9-2154 SRSHARP1_SR7_LTIGAIN_SDCOR0 0x530a

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_ltigain_sdcor7: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
27:24	RW	15	reg_sr7_ltigain_sdcor6: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
23:20	RW	15	reg_sr7_ltigain_sdcor5: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
19:16	RW	15	reg_sr7_ltigain_sdcor4: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
15:12	RW	15	reg_sr7_ltigain_sdcor3: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
11:8	RW	15	reg_sr7_ltigain_sdcor2: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
7:4	RW	15	reg_sr7_ltigain_sdcor1: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
3:0	RW	15	reg_sr7_ltigain_sdcor0: adaptive gamma for lti boost gain base on SD'[0:16:128~255]

Table 9-2155 SRSHARP1_SR7_LTIGAIN_SDCOR1 0x530b

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_ltigain_sdcor15: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
27:24	RW	15	reg_sr7_ltigain_sdcor14: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
23:20	RW	15	reg_sr7_ltigain_sdcor13: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
19:16	RW	15	reg_sr7_ltigain_sdcor12: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
15:12	RW	15	reg_sr7_ltigain_sdcor11: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
11:8	RW	15	reg_sr7_ltigain_sdcor10: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
7:4	RW	15	reg_sr7_ltigain_sdcor9: adaptive gamma for lti boost gain base on SD'[0:16:128~255]
3:0	RW	15	reg_sr7_ltigain_sdcor8: adaptive gamma for lti boost gain base on SD'[0:16:128~255]

Table 9-2156 SRSHARP1_SR7_HLTIBPF_TAP0 0x530c

Bit(s)	R/W	Default	Description
31:24	RW	0	reg_sr7_hlti_bpf_tap153: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0,signed
23:16	RW	-34	reg_sr7_hlti_bpf_tap152: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0,signed

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Bit(s)	R/W	Default	Description
15:8	RW	-1	reg_sr7_hlti_bpf_tap151: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0,signed
7:0	RW	120	reg_sr7_hlti_bpf_tap150: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0,signed

Table 9-2157 SRSHARP1_SR7_HLTIBPF_TAP1 0x530d

Bit(s)	R/W	Default	Description
31:24	RW	2	reg_sr7_hlti_bpf_tap157: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0,signed
23:16	RW	-7	reg_sr7_hlti_bpf_tap156: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0,signed
15:8	RW	1	reg_sr7_hlti_bpf_tap155: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0,signed
7:0	RW	-21	reg_sr7_hlti_bpf_tap154: tap15 BPF for hlti (gain3), only store half of the filter normalized to 256 as 1.0,signed

Table 9-2158 SRSHARP1_SR7_HCTIBPF_TAP0 0x530e

Bit(s)	R/W	Default	Description
31:24	RW	0	reg_sr7_clti_bpf_tap153: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed
23:16	RW	-34	reg_sr7_clti_bpf_tap152: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed
15:8	RW	-1	reg_sr7_clti_bpf_tap151: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed
7:0	RW	120	reg_sr7_clti_bpf_tap150: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed

Table 9-2159 SRSHARP1_SR7_HCTIBPF_TAP1 0x530f

Bit(s)	R/W	Default	Description
31:24	RW	2	reg_sr7_clti_bpf_tap157: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed
23:16	RW	-7	reg_sr7_clti_bpf_tap156: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed
15:8	RW	1	reg_sr7_clti_bpf_tap155: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed
7:0	RW	-21	reg_sr7_clti_bpf_tap154: tap15 BPF for clti (gain3), only store half of the filter normalized to 256 as 1.0,signed

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Table 9-2160 SRSHARP1_SR7_PKLONGBPF_HTAP0 0x5310

Bit(s)	R/W	Default	Description
31:24	RW	-24	reg_sr7_pk_long_bpf_hztap153: tap15 BPF for horizontal peaking filter, only store half of the filter,signed
23:16	RW	-19	reg_sr7_pk_long_bpf_hztap152: tap15 BPF for horizontal peaking filter, only store half of the filter,signed
15:8	RW	31	reg_sr7_pk_long_bpf_hztap151: tap15 BPF for horizontal peaking filter, only store half of the filter,signed
7:0	RW	66	reg_sr7_pk_long_bpf_hztap150: tap15 BPF for horizontal peaking filter, only store half of the filter,signed

Table 9-2161 SRSHARP1_SR7_PKLONGBPF_HTAP1 0x5311

Bit(s)	R/W	Default	Description
31:24	RW	-6	reg_sr7_pk_long_bpf_hztap157: tap15 BPF for horizontal peaking filter, only store half of the filter,signed
23:16	RW	-10	reg_sr7_pk_long_bpf_hztap156: tap15 BPF for horizontal peaking filter, only store half of the filter,signed
15:8	RW	-1	reg_sr7_pk_long_bpf_hztap155: tap15 BPF for horizontal peaking filter, only store half of the filter,signed
7:0	RW	-4	reg_sr7_pk_long_bpf_hztap154: tap15 BPF for horizontal peaking filter, only store half of the filter,signed

Table 9-2162 SRSHARP1_SR7_PKLONGHPF_HTAP0 0x5312

Bit(s)	R/W	Default	Description
31:24	RW	27	reg_sr7_pk_long_hpf_hztap153: tap15 HPF for horizontal peaking filter, only store half of the filter,signed
23:16	RW	-15	reg_sr7_pk_long_hpf_hztap152: tap15 HPF for horizontal peaking filter, only store half of the filter,signed
15:8	RW	-32	reg_sr7_pk_long_hpf_hztap151: tap15 HPF for horizontal peaking filter, only store half of the filter,signed
7:0	RW	58	reg_sr7_pk_long_hpf_hztap150: tap15 HPF for horizontal peaking filter, only store half of the filter,signed

Table 9-2163 SRSHARP1_SR7_PKLONGHPF_HTAP1 0x5313

Bit(s)	R/W	Default	Description
31:24	RW	8	reg_sr7_pk_long_hpf_hztap157: tap15 HPF for horizontal peaking filter, only store half of the filter,signed
23:16	RW	-6	reg_sr7_pk_long_hpf_hztap156: tap15 HPF for horizontal peaking filter, only store half of the filter,signed
15:8	RW	-1	reg_sr7_pk_long_hpf_hztap155: tap15 HPF for horizontal peaking filter, only store half of the filter,signed
7:0	RW	-10	reg_sr7_pk_long_hpf_hztap154: tap15 HPF for horizontal peaking filter, only store half of the filter,signed

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Table 9-2164 SRSHARP1_SR7_VLTIBPF_TAP0 0x5314

Bit(s)	R/W	Default	Description
31:24	RW	0	reg_sr7_vlti_bpf_tap093: tap09 BPF for vlti (gain3), only store half of the filter, signed
23:16	RW	-41	reg_sr7_vlti_bpf_tap092: tap09 BPF for vlti (gain3), only store half of the filter, signed
15:8	RW	0	reg_sr7_vlti_bpf_tap091: tap09 BPF for vlti (gain3), only store half of the filter, signed
7:0	RW	126	reg_sr7_vlti_bpf_tap090: tap09 BPF for vlti (gain3), only store half of the filter, signed

Table 9-2165 SRSHARP1_SR7_VLTIBPF_TAP1 0x5315

Bit(s)	R/W	Default	Description
31:8			reserved
7:0	RW	-22	reg_sr7_vlti_bpf_tap094: tap09 BPF for vlti (gain3), only store half of the filter, signed

Table 9-2166 SRSHARP1_SR7_VCTIBPF_TAP0 0x5316

Bit(s)	R/W	Default	Description
31:24	RW	0	reg_sr7_vcti_bpf_tap093: tap09 BPF for vcti (gain3), only store half of the filter, signed
23:16	RW	-41	reg_sr7_vcti_bpf_tap092: tap09 BPF for vcti (gain3), only store half of the filter, signed
15:8	RW	0	reg_sr7_vcti_bpf_tap091: tap09 BPF for vcti (gain3), only store half of the filter, signed
7:0	RW	126	reg_sr7_vcti_bpf_tap090: tap09 BPF for vcti (gain3), only store half of the filter, signed

Table 9-2167 SRSHARP1_SR7_VCTIBPF_TAP1 0x5317

Bit(s)	R/W	Default	Description
31:8			reserved
7:0	RW	-22	reg_sr7_vcti_bpf_tap094: tap09 BPF for vcti (gain3), only store half of the filter, signed

Table 9-2168 SRSHARP1_SR7_PKLONGBPF_VTAP0 0x5318

Bit(s)	R/W	Default	Description
31:24	RW	-32	reg_sr7_pk_long_bpf_vdtap093: tap09 BPF for vertical and diagonal peaking filter,signed
23:16	RW	-28	reg_sr7_pk_long_bpf_vdtap092: tap09 BPF for vertical and diagonal peaking filter,signed

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Bit(s)	R/W	Default	Description
15:8	RW	30	reg_sr7_pk_long_bpf_vdtap091: tap09 BPF for vertical and diagonal peaking filter,signed
7:0	RW	68	reg_sr7_pk_long_bpf_vdtap090: tap09 BPF for vertical and diagonal peaking filter,signed

Table 9-2169 SRSHARP1_SR7_PKLONGBPF_VTAP1 0x5319

Bit(s)	R/W	Default	Description
31:8			reserved
7:0	RW	-4	reg_sr7_pk_long_bpf_vdtap094: tap09 BPF for vertical and diagonal peaking filter,signed

Table 9-2170 SRSHARP1_SR7_PKLONGHPF_VTAP0 0x531a

Bit(s)	R/W	Default	Description
31:24	RW	30	reg_sr7_pk_long_hpf_vdtap093: tap09 HPF for vertical and diagonal peaking filter,signed
23:16	RW	-28	reg_sr7_pk_long_hpf_vdtap092: tap09 HPF for vertical and diagonal peaking filter,signed
15:8	RW	-31	reg_sr7_pk_long_hpf_vdtap091: tap09 HPF for vertical and diagonal peaking filter,signed
7:0	RW	68	reg_sr7_pk_long_hpf_vdtap090: tap09 HPF for vertical and diagonal peaking filter,signed

Table 9-2171 SRSHARP1_SR7_PKLONGHPF_VTAP1 0x531b

Bit(s)	R/W	Default	Description
31:8			reserved
7:0	RW	-5	reg_sr7_pk_long_hpf_vdtap094: tap09 HPF for vertical and diagonal peaking filter,signed

Table 9-2172 SRSHARP1_SR7_CIRBPLONG_ALP 0x531c

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	15	reg_sr7_cirbp_long_alpha3: alpha to blend bp_long to the cirpk filter corresponding angle (0/45/90/135)
11:8	RW	15	reg_sr7_cirbp_long_alpha2: alpha to blend bp_long to the cirpk filter corresponding angle (0/45/90/135)
7:4	RW	15	reg_sr7_cirbp_long_alpha1: alpha to blend bp_long to the cirpk filter corresponding angle (0/45/90/135)
3:0	RW	15	reg_sr7_cirbp_long_alpha0: alpha to blend bp_long to the cirpk filter corresponding angle (0/45/90/135)

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Table 9-2173 SRSHARP1_SR7_CIRHPLONG_ALP 0x531d

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	15	reg_sr7_cirhp_long_alpha3: alpha to blend hp_long to the cirpk filter corresponding angle (0/45/90/135)
11:8	RW	15	reg_sr7_cirhp_long_alpha2: alpha to blend hp_long to the cirpk filter corresponding angle (0/45/90/135)
7:4	RW	15	reg_sr7_cirhp_long_alpha1: alpha to blend hp_long to the cirpk filter corresponding angle (0/45/90/135)
3:0	RW	15	reg_sr7_cirhp_long_alpha0: alpha to blend hp_long to the cirpk filter corresponding angle (0/45/90/135)

Table 9-2174 SRSHARP1_SR7_DRTBPLONG_ALP 0x531e

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	15	reg_sr7_drtbp_long_alpha3: alpha to blend bp_long to the drtpk filter corresponding angle (0/45/90/135)
11:8	RW	15	reg_sr7_drtbp_long_alpha2: alpha to blend bp_long to the drtpk filter corresponding angle (0/45/90/135)
7:4	RW	15	reg_sr7_drtbp_long_alpha1: alpha to blend bp_long to the drtpk filter corresponding angle (0/45/90/135)
3:0	RW	15	reg_sr7_drtbp_long_alpha0: alpha to blend bp_long to the drtpk filter corresponding angle (0/45/90/135)

Table 9-2175 SRSHARP1_SR7_DRTHPLONG_ALP 0x531f

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	15	reg_sr7_drthp_long_alpha3: alpha to blend hp_long to the drtpk filter corresponding angle (0/45/90/135)
11:8	RW	15	reg_sr7_drthp_long_alpha2: alpha to blend hp_long to the drtpk filter corresponding angle (0/45/90/135)
7:4	RW	15	reg_sr7_drthp_long_alpha1: alpha to blend hp_long to the drtpk filter corresponding angle (0/45/90/135)
3:0	RW	15	reg_sr7_drthp_long_alpha0: alpha to blend hp_long to the drtpk filter corresponding angle (0/45/90/135)

Table 9-2176 SRSHARP1_SR7_PKMINMAXCIR_BLD_LUT2D0 0x5320

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_pk_mimaxerr2_cirbld_lut2d7
27:24	RW	0	reg_sr7_pk_mimaxerr2_cirbld_lut2d6
23:20	RW	2	reg_sr7_pk_mimaxerr2_cirbld_lut2d5
19:16	RW	2	reg_sr7_pk_mimaxerr2_cirbld_lut2d4

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Bit(s)	R/W	Default	Description
15:12	RW	4	reg_sr7_pk_mimaxerr2_cirbld_lut2d3
11:8	RW	6	reg_sr7_pk_mimaxerr2_cirbld_lut2d2
7:4	RW	12	reg_sr7_pk_mimaxerr2_cirbld_lut2d1
3:0	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d0: 2D-LUT for alpha2 for cir-PK blender,larger coef means less drt-pk, x-min_err, y-max_err

Table 9-2177 SRSHARP1_SR7_PKMINMAXCIR_BLD_LUT2D1 0x5321

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d15
27:24	RW	0	reg_sr7_pk_mimaxerr2_cirbld_lut2d14
23:20	RW	2	reg_sr7_pk_mimaxerr2_cirbld_lut2d13
19:16	RW	2	reg_sr7_pk_mimaxerr2_cirbld_lut2d12
15:12	RW	4	reg_sr7_pk_mimaxerr2_cirbld_lut2d11
11:8	RW	6	reg_sr7_pk_mimaxerr2_cirbld_lut2d10
7:4	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d9
3:0	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d8

Table 9-2178 SRSHARP1_SR7_PKMINMAXCIR_BLD_LUT2D2 0x5322

Bit(s)	R/W	Default	Description
31:28	RW	6	reg_sr7_pk_mimaxerr2_cirbld_lut2d23
27:24	RW	10	reg_sr7_pk_mimaxerr2_cirbld_lut2d22
23:20	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d21
19:16	RW	2	reg_sr7_pk_mimaxerr2_cirbld_lut2d20
15:12	RW	2	reg_sr7_pk_mimaxerr2_cirbld_lut2d19
11:8	RW	4	reg_sr7_pk_mimaxerr2_cirbld_lut2d18
7:4	RW	6	reg_sr7_pk_mimaxerr2_cirbld_lut2d17
3:0	RW	12	reg_sr7_pk_mimaxerr2_cirbld_lut2d16

Table 9-2179 SRSHARP1_SR7_PKMINMAXCIR_BLD_LUT2D3 0x5323

Bit(s)	R/W	Default	Description
31:28	RW	14	reg_sr7_pk_mimaxerr2_cirbld_lut2d31
27:24	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d30
23:20	RW	4	reg_sr7_pk_mimaxerr2_cirbld_lut2d29
19:16	RW	8	reg_sr7_pk_mimaxerr2_cirbld_lut2d28
15:12	RW	10	reg_sr7_pk_mimaxerr2_cirbld_lut2d27

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Bit(s)	R/W	Default	Description
11:8	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d26
7:4	RW	2	reg_sr7_pk_mimaxerr2_cirbld_lut2d25
3:0	RW	4	reg_sr7_pk_mimaxerr2_cirbld_lut2d24

Table 9-2180 SRSHARP1_SR7_PKMINMAXCIR_BLD_LUT2D4 0x5324

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d35
11:8	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d34
7:4	RW	15	reg_sr7_pk_mimaxerr2_cirbld_lut2d33
3:0	RW	12	reg_sr7_pk_mimaxerr2_cirbld_lut2d32

Table 9-2181 SRSHARP1_SR7_PKMINMAXLPF_BLD_LUT2D0 0x5325

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_pk_mimaxerr2_lpfbld_lut2d7
27:24	RW	0	reg_sr7_pk_mimaxerr2_lpfbld_lut2d6
23:20	RW	2	reg_sr7_pk_mimaxerr2_lpfbld_lut2d5
19:16	RW	2	reg_sr7_pk_mimaxerr2_lpfbld_lut2d4
15:12	RW	4	reg_sr7_pk_mimaxerr2_lpfbld_lut2d3
11:8	RW	6	reg_sr7_pk_mimaxerr2_lpfbld_lut2d2
7:4	RW	12	reg_sr7_pk_mimaxerr2_lpfbld_lut2d1
3:0	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d0: 2D-LUT for alpha2 for PK lpf along edge blender, lareger coef means less lpf along edge,x-min_err, y-max_err

Table 9-2182 SRSHARP1_SR7_PKMINMAXLPF_BLD_LUT2D1 0x5326

Bit(s)	R/W	Default	Description
31:28	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d15
27:24	RW	0	reg_sr7_pk_mimaxerr2_lpfbld_lut2d14
23:20	RW	2	reg_sr7_pk_mimaxerr2_lpfbld_lut2d13
19:16	RW	2	reg_sr7_pk_mimaxerr2_lpfbld_lut2d12
15:12	RW	4	reg_sr7_pk_mimaxerr2_lpfbld_lut2d11
11:8	RW	6	reg_sr7_pk_mimaxerr2_lpfbld_lut2d10
7:4	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d9
3:0	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d8

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Table 9-2183 SRSHARP1_SR7_PKMINMAXLPF_BLD_LUT2D2 0x5327

Bit(s)	R/W	Default	Description
31:28	RW	6	reg_sr7_pk_mimaxerr2_lpfbld_lut2d23
27:24	RW	10	reg_sr7_pk_mimaxerr2_lpfbld_lut2d22
23:20	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d21
19:16	RW	2	reg_sr7_pk_mimaxerr2_lpfbld_lut2d20
15:12	RW	2	reg_sr7_pk_mimaxerr2_lpfbld_lut2d19
11:8	RW	4	reg_sr7_pk_mimaxerr2_lpfbld_lut2d18
7:4	RW	6	reg_sr7_pk_mimaxerr2_lpfbld_lut2d17
3:0	RW	12	reg_sr7_pk_mimaxerr2_lpfbld_lut2d16

Table 9-2184 SRSHARP1_SR7_PKMINMAXLPF_BLD_LUT2D3 0x5328

Bit(s)	R/W	Default	Description
31:28	RW	14	reg_sr7_pk_mimaxerr2_lpfbld_lut2d31
27:24	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d30
23:20	RW	4	reg_sr7_pk_mimaxerr2_lpfbld_lut2d29
19:16	RW	8	reg_sr7_pk_mimaxerr2_lpfbld_lut2d28
15:12	RW	10	reg_sr7_pk_mimaxerr2_lpfbld_lut2d27
11:8	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d26
7:4	RW	2	reg_sr7_pk_mimaxerr2_lpfbld_lut2d25
3:0	RW	4	reg_sr7_pk_mimaxerr2_lpfbld_lut2d24

Table 9-2185 SRSHARP1_SR7_PKMINMAXLPF_BLD_LUT2D4 0x5329

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d35
11:8	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d34
7:4	RW	15	reg_sr7_pk_mimaxerr2_lpfbld_lut2d33
3:0	RW	12	reg_sr7_pk_mimaxerr2_lpfbld_lut2d32

Table 9-2186 SRSHARP1_SR7_PKDRT_BLD_EN 0x532a

Bit(s)	R/W	Default	Description
31:1			reserved
0	RW	0	reg_sr7_pkdrtbld_beta_en: enable of direction ambiguity protection for drt and cir blend

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Table 9-2187 SRSHARP1_SR7_DRTDIF_TH 0x532b

Bit(s)	R/W	Default	Description
31:16			reserved
15::8	RW	128	reg_sr7_drtdif_min2sad_th1
7:0	RW	128	reg_sr7_drtdif_min2sad_th0:for min2_sad threshold for ambiguilty ignoring

Table 9-2188 SRSHARP1_SR7_TIBLD_PRT 0x532c

Bit(s)	R/W	Default	Description
31:16			reserved
13	RW	1	reg_sr7_hlti_dcbld_beta_en:enable of denoise protection for dc org and denoise blend
12	RW	1	reg_sr7_vlti_dcbld_beta_en:enable of denoise protection for dc org and denoise blend
11:8	RW	0	reg_sr7_xcti_dcbld_beta1:beta for denoise and org dc blend base on the x=cal_drt_dif4(min_idx,min2_idx)
7:4	RW	15	reg_sr7_xcti_dcbld_beta0:beta for denoise and org dc blend base on the x=cal_drt_dif4(min_idx,min2_idx)
3	RW	1	reg_sr7_hcti_dcbld_beta_en:enable of denoise protection for dc org and denoise blend
2	RW	1	reg_sr7_vcti_dcbld_beta_en:enable of denoise protection for dc org and denoise blend
1	RW	0	reg_sr7_hcti_dcbld_use_ybeta:enable to use beta from hlti
0	RW	0	reg_sr7_vcti_dcbld_use_ybeta:enable to use beta from vlti

Table 9-2189 SRSHARP1_SR7_HTI_OPT_FORCE 0x532d

Bit(s)	R/W	Default	Description
31:6			reserved
5	RW	1	reg_sr7_diag_force_hti1force hti: for diagonal edges luma/chroma, 0: diagonal use vti, 1: diagonal use hti
4	RW	1	reg_sr7_diag_force_hti0:force hti for diagonal edges luma/chroma, 0: diagonal use vti, 1: diagonal use hti
3	RW	1	reg_sr7_horz_force_vti1:force vti for horizontal edges luma/chroma, 0: bias hti, 1: horizontal edge force 100% vti
2	RW	1	reg_sr7_horz_force_vti0:force vti for horizontal edges luma/chroma, 0: bias hti, 1: horizontal edge force 100% vti
1	RW	1	reg_sr7_alph_force_hvsad1:alpha = minsad*64/maxsad, force minsad=sad_h, maxsad=sad_v for alpha calculation
0	RW	1	reg_sr7_alph_force_hvsad0:alpha = minsad*64/maxsad, force minsad=sad_h, maxsad=sad_v for alpha calculation,[0]for luma, [1] for chroma

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Table 9-2190 SRSHARP1_SR7_HVTI_FINALGAIN 0x532e

Bit(s)	R/W	Default	Description
31:28			reserved
27:16	RW	256	reg_sr7_hvti_finalgain1: final gain for HVTI boost, for easier level tunning for application
15:12			reserved
11:0	RW	256	reg_sr7_hvti_finalgain0: final gain for HVTI boost, for easier level tunning for application

Table 9-2191 SRSHARP1_SR7_TIOS_SDRATIO 0x532f

Bit(s)	R/W	Default	Description
31:30			reserved
29:24	RW	3	reg_sr7_hti_osmargin_sdratio1:ratio for HTI OS margin adaptive to sd
23:22			reserved
21:16	RW	3	reg_sr7_hti_osmargin_sdratio0:ratio for HTI OS margin adaptive to sd
15:14			reserved
13:8	RW	3	reg_sr7_vti_osmargin_sdratio1:ratio for VTI OS margin adaptive to sd
7:6			reserved
5:0	RW	3	reg_sr7_vti_osmargin_sdratio0:ratio for VTI OS margin adaptive to sd

Table 9-2192 SRSHARP1_SR7_XTI_SDFDEN 0x5330

Bit(s)	R/W	Default	Description
31:1			reserved
1	RW	1	reg_sr7_xtigain_sdfd_en1: adaptive gamma for cti boost gain enable.
0	RW	1	reg_sr7_xtigain_sdfd_en0: adaptive gamma for cti boost gain enable.[0]for luma, [1] for chroma

Table 9-2193 SRSHARP1_SR7_FDSD_PARAM 0x5331

Bit(s)	R/W	Default	Description
31:26			reserved
25	RW	1	reg_fdsd_vlpf_en:use vertical [1 2 1] lpf filter for the fd and sd derivativecalculations
24	RW	1	reg_fdsd_hlpf_en:use horizontal [1 2 1] lpf filter for the fd and sd derivativecalculations
23:20	RW	0	reg_sd_coring_th1:coring to SD'= MAX(SD - FD*ratio - coring,0)
19:16	RW	0	reg_sd_coring_th0:coring to SD'= MAX(SD - FD*ratio - coring,0)
15:14			reserved
13:8	RW	4	reg_sd_coring_ratio2fd1:ratio to FD for adaptive coring to SD'= MAX(SD - FD*ratio - coring,0)

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Bit(s)	R/W	Default	Description
7:6			reserved
5:0	RW	4	reg_sd_coring_ratio2fd0:ratio to FD for adaptive coring to SD'= MAX(SD - FD*ratio - coring,0)

Table 9-2194 SRSHARP1_SR7_TI_BPF_EN 0x5332

Bit(s)	R/W	Default	Description
31:4			reserved
3	RW	1	reg_sr7_hlti_bpf_en:enable of tap09 BPF for hlti (gain3), only store half of the filter
2	RW	1	reg_sr7_hcti_bpf_en:enable of tap09 BPF for hcti (gain3), only store half of the filter
1	RW	1	reg_sr7_vlti_bpf_en:enable of tap09 BPF for vcti (gain3), only store half of the filter
0	RW	1	reg_sr7_vcti_bpf_en:enable of tap09 BPF for vlti (gain3), only store half of the filter

Table 9-2195 SRSHARP1_SR7_PKLONG_PF_EN 0x5333

Bit(s)	R/W	Default	Description
31:2			reserved
1	RW	1	reg_sr7_pk_long_bpf_en:enable of long BPF for peaking
0	RW	1	reg_sr7_pk_long_hpf_en:enable of long HPF for peaking

Table 9-2196 SRSHARP1_SR7_PKLONG_PF_GAIN 0x5334

Bit(s)	R/W	Default	Description
31:24	RW	64	reg_sr7_pk_long_bpf_hzgain:gain to long horizontal BPF for peaking
23:16	RW	64	reg_sr7_pk_long_bpf_vdgain:gain to long vertical and diagonal BPF for peaking
15:8	RW	64	reg_sr7_pk_long_hpf_hzgain:gain to long horizontal HPF for peaking
7:0	RW	64	reg_sr7_pk_long_hpf_vdgain:gain to long vertical and diagonal HPF for peaking

Table 9-2197 SRSHARP1_SR7_PKMINMAX_BLD 0x5335

Bit(s)	R/W	Default	Description
31:4			reserved
3	RW	1	reg_sr7_pk_mimaxerr2_cirbld_on_bp:enable to use adaptive blender of drtBP vs cirBP alpha2, the larger of cell, the more cirPK results, 0: alp2=lut2d(minerr, maxerr),1:alp2=min_err/maxerr
2	RW	1	reg_sr7_pk_mimaxerr2_cirbld_on_hp:enable to use adaptive blender of drtHP vs cirHP alpha2, the larger of cell, the more cirPK results, 0: alp2=lut2d(minerr, maxerr),1:alp2=min_err/maxerr

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Bit(s)	R/W	Default	Description
1	RW	1	reg_sr7_pk_mimaxerr2_lpfbld_on_bp:enable to use adaptive blender of BP result lpf along edge based on the mimaxsad relationship
0	RW	1	reg_sr7_pk_mimaxerr2_lpfbld_on_hp:enable to use adaptive blender of HP result lpf along edge based on the mimaxsad relationship

Table 9-2198 SRSHARP1_SR7_TI_CONMAXERR_GAIN 0x5336

Bit(s)	R/W	Default	Description
31:16			reserved
15:12	RW	8	reg_sr7_hti_conmaxerr_gain1:con=max(con, maxerr) for the horizontal transition calculation, gain=0, same as s6 and prev, [0] for y and [1] for uv
11:8	RW	8	reg_sr7_hti_conmaxerr_gain0:con=max(con, maxerr) for the horizontal transition calculation, gain=0, same as s6 and prev, [0] for y and [1] for uv
7:4	RW	8	reg_sr7_vti_conmaxerr_gain1:con=max(con, maxerr) for the vertical transition calculation, gain=0, same as s6 and prev, [0] for y and [1] for uv
3:0	RW	8	reg_sr7_vti_conmaxerr_gain0:con=max(con, maxerr) for the vertical transition calculation, gain=0, same as s6 and prev, [0] for y and [1] for uv

Table 9-2199 SRSHARP1_SR7_CC_PK_ADJ 0x5337

Bit(s)	R/W	Default	Description
31:25			reserved
24	RW	1	reg_sr7_cc_enable:color compensation enable, 0: no CC, 1: with CC
23:22			reserved
21:20	RW	0	reg_sr7_cc_yinp_sel:color compensation input luma selection, 0: org_y; 1: gau_y ; 2:gauadp_y; 3:edgeadp_y (same as dnlp input sel)
19:18	RW	2	reg_sr7_cc_ydlt_sel:color compensation output luma selection, 0: peaking+lti output; 1: dnlp output; 2/3: peaking+lti+dnlp
17:16	RW	1	reg_sr7_cc_sat_norm:normalization of lut cell to saturation. 0: norm to 8 as 1.0, sat[0:23/8]; 1: norm to 16 as 1.0, sat[1/16:31/16]; 2: norm to 32 as 1.0, sat[17/32:47/32]; 3:norm to 64 as 1.0, sat[49/64:79/64]
15:8	RW	64	reg_sr7_cc_ydlt_pscl:prescale to the y-delta (if > 0) before feeding to y-lumadlt, normalized 64 as 1.0
7:0	RW	64	reg_sr7_cc_ydlt_nscl:prescale to the y-delta (if < 0) before feeding to y-lumadlt, normalized 64 as 1.0

Table 9-2200 SRSHARP1_SR7_CC_LUT0 0x5338

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_cc_lut103:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=0
27:24	RW	0	reg_sr7_cc_lut102:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=0
23:20	RW	0	reg_sr7_cc_lut001:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=0
19:16	RW	0	reg_sr7_cc_lut000:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=0
15:12	RW	8	reg_sr7_cc_lut103:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=1/8

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Bit(s)	R/W	Default	Description
11:8	RW	4	reg_sr7_cc_lut102:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=1/8
7:4	RW	2	reg_sr7_cc_lut101:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=1/8
3:0	RW	1	reg_sr7_cc_lut100:valid for y-lumadlt= 1/4, 1/2, 3/4, 1.0; of x-lumainput=1/8

Table 9-2201 SRSHARP1_SR7_CC_LUT1 0x5339

Bit(s)	R/W	Default	Description
31:28			reserved
27:24	RW	12	reg_sr7_cc_lut202:valid for y-lumadlt= 1/4, 1/2, 3/4; of x-lumainput=2/8
23:20	RW	8	reg_sr7_cc_lut201:valid for y-lumadlt= 1/4, 1/2, 3/4; of x-lumainput=2/8
19:16	RW	4	reg_sr7_cc_lut200:valid for y-lumadlt= 1/4, 1/2, 3/4; of x-lumainput=2/8
15:12			reserved
11:8	RW	15	reg_sr7_cc_lut302:valid for y-lumadlt= 1/4, 1/2, 3/4; of x-lumainput=3/8
7:4	RW	10	reg_sr7_cc_lut301:valid for y-lumadlt= 1/4, 1/2, 3/4; of x-lumainput=3/8
3:0	RW	5	reg_sr7_cc_lut300:valid for y-lumadlt= 1/4, 1/2, 3/4; of x-lumainput=3/8

Table 9-2202 SRSHARP1_SR7_CC_LUT2 0x533a

Bit(s)	R/W	Default	Description
31:24			reserved
23:20	RW	15	reg_sr7_cc_lut401:valid for y-lumadlt= 1/4, 1/2 ; of x-lumainput=4/8
19:16	RW	8	reg_sr7_cc_lut400:valid for y-lumadlt= 1/4, 1/2; of x-lumainput=4/8
15:12	RW	13	reg_sr7_cc_lut501:valid for y-lumadlt= 1/4, 1/2; of x-lumainput=5/8
11:8	RW	6	reg_sr7_cc_lut500:valid for y-lumadlt= 1/4, 1/2; of x-lumainput=5/8
7:4	RW	5	reg_sr7_cc_lut600:valid for y-lumadlt= 1/4 of x-lumainput=6/8
3:0	RW	4	reg_sr7_cc_lut700:valid for y-lumadlt= 1/4 of x-lumainput=7/8

Table 9-2203 SRSHARP1_SR7_CC_LUT3 0x533b

Bit(s)	R/W	Default	Description
31:24			reserved
23:20	RW	4	reg_sr7_cc_lut710:valid for y-lumadlt= -1/4,; of x-lumainput=1/8
19:16	RW	5	reg_sr7_cc_lut610:valid for y-lumadlt= -1/4,; of x-lumainput=2/8
15:12	RW	13	reg_sr7_cc_lut511:valid for y-lumadlt= -1/4, -1/2; of x-lumainput=3/8
11:8	RW	6	reg_sr7_cc_lut510:valid for y-lumadlt= -1/4, -1/2; of x-lumainput=3/8
7:4	RW	15	reg_sr7_cc_lut411:valid for y-lumadlt= -1/4, -1/2 of x-lumainput=4/8
3:0	RW	8	reg_sr7_cc_lut410:valid for y-lumadlt= -1/4 , -1/2 of x-lumainput=4/8

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Table 9-2204 SRSHARP1_SR7_CC_LUT4 0x533c

Bit(s)	R/W	Default	Description
31:24			reserved
23:20	RW	15	reg_sr7_cc_lut312:valid for y-lumadlt= -1/4,-1/2, -3/4; of x-lumainput=5/8
19:16	RW	10	reg_sr7_cc_lut311:valid for y-lumadlt= -1/4,-1/2, -3/4; of x-lumainput=5/8
15:12	RW	5	reg_sr7_cc_lut310:valid for y-lumadlt= -1/4,-1/2, -3/4; of x-lumainput=5/8
11:8	RW	12	reg_sr7_cc_lut212:valid for y-lumadlt= -1/4, -1/2, -3/4;; of x-lumainput=6/8
7:4	RW	8	reg_sr7_cc_lut211:valid for y-lumadlt= -1/4, -1/2, -3/4; of x-lumainput=6/8
3:0	RW	4	reg_sr7_cc_lut210:valid for y-lumadlt= -1/4, -1/2, -3/4; of x-lumainput=6/8

Table 9-2205 SRSHARP1_SR7_CC_LUT5 0x533d

Bit(s)	R/W	Default	Description
31:28	RW	8	reg_sr7_cc_lut113:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=7/8
27:24	RW	4	reg_sr7_cc_lut112:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=7/8
23:20	RW	2	reg_sr7_cc_lut111:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=7/8
19:16	RW	1	reg_sr7_cc_lut110:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=7/8
15:12	RW	0	reg_sr7_cc_lut013:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=8/8
11:8	RW	0	reg_sr7_cc_lut012:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=8/8
7:4	RW	0	reg_sr7_cc_lut011:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=8/8
3:0	RW	0	reg_sr7_cc_lut010:valid for y-lumadlt= -1/4, -1/2, -3/4, -1.0; of x-lumainput=8/8

Table 9-2206 SRSHARP1_SR7_GRAPHIC_CTRL 0x533e

Bit(s)	R/W	Default	Description
31:11			reserved
10	RW	1	reg_sr7_grph_en:enable graphic statistic
9	RW	1	reg_sr7_grph_hflt:horizontal filter, 0: [0 1 -1], 1: [-1 2 -1]
8	RW	1	reg_sr7_grph_vflt: vertical filter, 0: [0 1 -1], 1: [-1 2 -1]
7:0	RW	0	reg_sr7_grph_dif_cor:coring for dif while count for graphic

Table 9-2207 SRSHARP1_SR7_GRAPHIC_THD_GAIN 0x533f

Bit(s)	R/W	Default	Description
31:24	RW	2	reg_sr7_grph_flt_thd: flat threshold for dif while count for graphic.
23:16	RW	40	reg_sr7_grph_dtl_thd:detail threshold for dif while count for graphic
15:8	RW	32	reg_sr7_grph_hgain:horizontal gain for fast squart of hp
7:0	RW	32	reg_sr7_grph_vgain:vertical gain for fast squart of hp

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Table 9-2208 SRSHARP1_SR7_RO_GRAPHIC_FLT_CNT 0x5340

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_sr7_grph_flt_cnt:: flat count numbers for graphic

Table 9-2209 SRSHARP1_SR7_RO_GRAPHIC_DTL_CNT 0x5341+

Bit(s)	R/W	Default	Description
31:0	RO	0	ro_sr7_grph_dtl_cnt::detail count numbers for graphic

Table 9-2210 SRSHARP1_SR7_CLR_PRT_PARAM 0x5342

Bit(s)	R/W	Default	Description
31:18			reserved
17:16	RW	3	reg_sr7_clr_prct_inpsel:input UV selection for color protection, 0: org; 1: NRout; 2: CTIout; 3: (NR+TIout)/2
15:8	RW	64	reg_sr7_clr_prct_dnlp_gain:gain to de-boost of dnlp_dlt base on color region, norm to 64 as 1.0. set to 0 as disable.
7:0	RW	64	reg_sr7_clr_prct_peak_gain:gain to de-boost of peak_dlt base on color region, norm to 64 as 1.0, set to 0 as disable

Table 9-2211 SRSHARP1_SR7_CLR_PRT_LC_GAIN 0x5343

Bit(s)	R/W	Default	Description
31:24			reserved
23:16	RW	64	reg_sr7_clr_prct_lc_gain2:gain to de-boost of lc_dlt (y/u/v) base on color region, norm to 64 as 1.0, set to 0 as disable
15:8	RW	64	reg_sr7_clr_prct_lc_gain1:gain to de-boost of lc_dlt (y/u/v) base on color region, norm to 64 as 1.0, set to 0 as disable
7:0	RW	64	reg_sr7_clr_prct_lc_gain0:gain to de-boost of lc_dlt (y/u/v) base on color region, norm to 64 as 1.0, set to 0 as disable

Table 9-2212 SRSHARP1_SR7_CLR_PRT_LUT0 0x5344

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut7:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut6:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut5:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut4:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut3:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut2:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut1:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut0:color protection lut, 16 is normalized to 1

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Table 9-2213 SRSHARP1_SR7_CLR_PRT_LUT1 0x5345

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut15:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut14:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut13:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut12:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut11:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut10:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut9:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut8:color protection lut, 16 is normalized to 1

Table 9-2214 SRSHARP1_SR7_CLR_PRT_LUT2 0x5346

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut23:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut22:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut21:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut20:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut19:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut18:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut17:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut16:color protection lut, 16 is normalized to 1

Table 9-2215 SRSHARP1_SR7_CLR_PRT_LUT3 0x5347

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut31:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut30:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut29:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut28:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut27:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut26:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut25:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut24:color protection lut, 16 is normalized to 1

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Table 9-2216 SRSHARP1_SR7_CLR_PRT_LUT4 0x5348

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut39:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut38:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut37:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut36:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut35:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut34:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut33:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut32:color protection lut, 16 is normalized to 1

Table 9-2217 SRSHARP1_SR7_CLR_PRT_LUT5 0x5349

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut47:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut46:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut45:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut44:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut43:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut42:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut41:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut40:color protection lut, 16 is normalized to 1

Table 9-2218 SRSHARP1_SR7_CLR_PRT_LUT6 0x534a

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut55:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut54:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut53:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut52:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut51:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut50:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut49:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut48:color protection lut, 16 is normalized to 1

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Table 9-2219 SRSHARP1_SR7_CLR_PRT_LUT7 0x534b

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut63:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut62:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut61:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut60:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut59:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut58:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut57:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut56:color protection lut, 16 is normalized to 1

Table 9-2220 SRSHARP1_SR7_CLR_PRT_LUT8 0x534c

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut71:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut70:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut69:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut68:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut67:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut66:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut65:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut64:color protection lut, 16 is normalized to 1

Table 9-2221 SRSHARP1_SR7_CLR_PRT_LUT9 0x534d

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut79:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut78:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut77:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut76:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut75:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut74:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut73:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut72:color protection lut, 16 is normalized to 1

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Table 9-2222 SRSHARP1_SR7_CLR_PRT_LUT10 0x534e

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut87:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut86:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut85:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut84:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut83:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut82:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut81:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut80:color protection lut, 16 is normalized to 1

Table 9-2223 SRSHARP1_SR7_CLR_PRT_LUT11 0x534f

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut95:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut94:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut93:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut92:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut91:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut90:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut89:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut88:color protection lut, 16 is normalized to 1

Table 9-2224 SRSHARP1_SR7_CLR_PRT_LUT12 0x5350

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut103:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut102:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut101:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut100:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut99:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut98:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut97:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut96:color protection lut, 16 is normalized to 1

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Table 9-2225 SRSHARP1_SR7_CLR_PRT_LUT13 0x5351

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut111:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut110:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut109:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut108:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut107:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut106:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut105:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut104:color protection lut, 16 is normalized to 1

Table 9-2226 SRSHARP1_SR7_CLR_PRT_LUT14 0x5352

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut119:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut118:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut117:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut116:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut115:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut114:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut113:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut112:color protection lut, 16 is normalized to 1

Table 9-2227 SRSHARP1_SR7_CLR_PRT_LUT15 0x5353

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut127:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut126:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut125:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut124:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut123:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut122:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut121:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut120:color protection lut, 16 is normalized to 1

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Table 9-2228 SRSHARP1_SR7_CLR_PRT_LUT16 0x5354

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut135:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut134:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut133:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut132:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut131:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut130:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut129:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut128:color protection lut, 16 is normalized to 1

Table 9-2229 SRSHARP1_SR7_CLR_PRT_LUT17 0x5355

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut143:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut142:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut141:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut140:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut139:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut138:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut137:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut136:color protection lut, 16 is normalized to 1

Table 9-2230 SRSHARP1_SR7_CLR_PRT_LUT18 0x5356

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut151:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut150:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut149:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut148:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut147:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut146:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut145:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut144:color protection lut, 16 is normalized to 1

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Table 9-2231 SRSHARP1_SR7_CLR_PRT_LUT19 0x5357

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut159:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut158:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut157:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut156:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut155:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut154:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut153:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut152:color protection lut, 16 is normalized to 1

Table 9-2232 SRSHARP1_SR7_CLR_PRT_LUT20 0x5358

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut167:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut166:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut165:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut164:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut163:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut162:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut161:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut160:color protection lut, 16 is normalized to 1

Table 9-2233 SRSHARP1_SR7_CLR_PRT_LUT21 0x5359

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut175:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut174:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut173:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut172:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut171:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut170:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut169:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut168:color protection lut, 16 is normalized to 1

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Table 9-2234 SRSHARP1_SR7_CLR_PRT_LUT22 0x535a

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut183:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut182:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut181:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut180:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut179:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut178:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut177:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut176:color protection lut, 16 is normalized to 1

Table 9-2235 SRSHARP1_SR7_CLR_PRT_LUT23 0x535b

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut191:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut190:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut189:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut188:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut187:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut186:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut185:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut184:color protection lut, 16 is normalized to 1

Table 9-2236 SRSHARP1_SR7_CLR_PRT_LUT24 0x535c

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut199:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut198:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut197:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut196:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut195:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut194:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut193:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut192:color protection lut, 16 is normalized to 1

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Table 9-2237 SRSHARP1_SR7_CLR_PRT_LUT25 0x535d

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut207:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut206:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut205:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut204:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut203:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut202:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut201:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut200:color protection lut, 16 is normalized to 1

Table 9-2238 SRSHARP1_SR7_CLR_PRT_LUT26 0x535e

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut215:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut214:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut213:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut212:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut211:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut210:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut209:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut208:color protection lut, 16 is normalized to 1

Table 9-2239 SRSHARP1_SR7_CLR_PRT_LUT27 0x535f

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut223:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut222:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut221:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut220:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut219:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut218:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut217:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut216:color protection lut, 16 is normalized to 1

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Table 9-2240 SRSHARP1_SR7_CLR_PRT_LUT28 0x5360

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut231:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut230:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut229:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut228:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut227:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut226:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut225:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut224:color protection lut, 16 is normalized to 1

Table 9-2241 SRSHARP1_SR7_CLR_PRT_LUT29 0x5361

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut239:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut238:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut237:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut236:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut235:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut234:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut233:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut232:color protection lut, 16 is normalized to 1

Table 9-2242 SRSHARP1_SR7_CLR_PRT_LUT30 0x5362

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut247:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut246:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut245:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut244:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut243:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut242:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut241:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut240:color protection lut, 16 is normalized to 1

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Table 9-2243 SRSHARP1_SR7_CLR_PRT_LUT31 0x5363

Bit(s)	R/W	Default	Description
31:28	RW	0	reg_sr7_clr_prct_lut255:color protection lut, 16 is normalized to 1
27:24	RW	0	reg_sr7_clr_prct_lut254:color protection lut, 16 is normalized to 1
23:20	RW	0	reg_sr7_clr_prct_lut253:color protection lut, 16 is normalized to 1
19:16	RW	0	reg_sr7_clr_prct_lut252:color protection lut, 16 is normalized to 1
15:12	RW	0	reg_sr7_clr_prct_lut251:color protection lut, 16 is normalized to 1
11:8	RW	0	reg_sr7_clr_prct_lut250:color protection lut, 16 is normalized to 1
7:4	RW	0	reg_sr7_clr_prct_lut249:color protection lut, 16 is normalized to 1
3:0	RW	0	reg_sr7_clr_prct_lut248:color protection lut, 16 is normalized to 1

9.2.3.33 VKSTONE Registers

Table 9-2244 VKS_CTRL 0x3100

Bit(s)	R/W	Default	Description
31	W	1	reg_vks_en : // unsigned , default = 1 enable signal of the vks function need set high in every frme
30	R/W	1	reg_vks_scl_mode0 : // unsigned , default = 1 : b0 mode of vks ofset mode, 0: offset= offset; 1: offset= offset*step= ofset/scale;
29	R/W	1	reg_vks_scl_mode1 : // unsigned , default = 1 : b0 mode of vks ofset mode, 0: offset= offset; 1: offset= offset*step= ofset/scale;
28	R/W	1	reg_vks_fill_mode : // unsigned , default = 1 mode of out-of-boundary fill, 0 extension, 1: fill with the fill_value
27:26	R/W	1	reg_vks_row_inp_mode : // unsigned , default = 1 , interpolation mode from 16pieces ofset/step to each line ofset and step; 0: linear interpolation; 1: cubic interpolation (using ccoef)
25	R/W	0	reg_vks_border_ext_mode0 : // unsigned , default = 0 , extend mode of the border data of luma and chroma, 0: copy the most border one; 1: extropolate the border one
24	R/W	0	reg_vks_border_ext_mode1 : // unsigned , default = 0 , extend mode of the border data of luma and chroma, 0: copy the most border one; 1: extropolate the border one
23	R/W	1	reg_vks_obuf_mode0 : // unsigned , default = 1 , mode of output buffer left/right side. 0: no precalculate active pixels during output fill region; 1: precaclc active pixels during output fill regions
22	R/W	1	reg_vks_obuf_mode1 : // unsigned , default = 1 , mode of output buffer left/right side. 0: no precalculate active pixels during output fill region; 1: precaclc active pixels during output fill regions
21:20	R/W	3	reg_vks_obuf_mrgn0 : // unsigned , default = 3 , margin pixels for left right most active pixel to the fill pixels to avoid jump
19:18	R/W	3	reg_vks_obuf_mrgn1 : // unsigned , default = 3 , margin pixels for left right most active pixel to the fill pixels to avoid jump

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Bit(s)	R/W	Default	Description
17:16	R/W	2	reg_vks_phs_qmode : // unsigned , default = 2 , interpolation mode of the phase, 0: floor to 1/64 phase; 1: round to 1/64 phase; 2/3 linear intp
15: 0	R/W	11651	reg_vks_row_scl : // unsigned , default = 11651 , scale of row to make it fit to the 16 pieces, scl = (2^23)/RowMax

Table 9-2245 VKS_OUT_WIN_SIZE 0x3101

Bit(s)	R/W	Default	Description
29:16	R/W	1280	reg_vks_ocolmax : // unsigned , default = 1280 output outer window col number, decided by the projector
13: 0	R/W	720	reg_vks_orowmax : // unsigned , default = 720 output outer window row number, decided by the projector

Table 9-2246 VKS_PRELPF_YCOEF0 0x3102

Bit(s)	R/W	Default	Description
31:24	R/W	0x0	reg_vks_prelpf_ycoef0 : // signed , default = -128 coef of horizontal luma prelpf for Keystone, normalized 128 as '1'
23:16	R/W	0	reg_vks_prelpf_ycoef1 : // signed , default = 0 coef of horizontal luma prelpf for Keystone, normalized 128 as '1'
15: 8	R/W	0	reg_vks_prelpf_ycoef2 : // signed , default = 0 coef of horizontal luma prelpf for Keystone, normalized 128 as '1'
7: 0	R/W	0	reg_vks_prelpf_ycoef3 : // signed , default = 0 coef of horizontal luma prelpf for Keystone, normalized 128 as '1'

Table 9-2247 VKS_PRELPF_YCOEF1 0x3103

Bit(s)	R/W	Default	Description
15: 8	R/W	0	reg_vks_prelpf_ycoef4 : // signed , default = 0 coef of horizontal luma prelpf for Keystone, normalized 128 as '1'
7: 0	R/W	0	reg_vks_prelpf_ycoef5 : // signed , default = 0 coef of horizontal luma prelpf for Keystone, normalized 128 as '1'

Table 9-2248 VKS_PRELPF_CCOEF0 0x3104

Bit(s)	R/W	Default	Description
31:24	R/W	0x0	reg_vks_prelpf_ccoef0 : // signed , default = -128 mode of horizontal chroma prelpf for Keystone, normalized 128 as '1'
23:16	R/W	0	reg_vks_prelpf_ccoef1 : // signed , default = 0 mode of horizontal chroma prelpf for Keystone, normalized 128 as '1'
15: 8	R/W	0	reg_vks_prelpf_ccoef2 : // signed , default = 0 mode of horizontal chroma prelpf for Keystone, normalized 128 as '1'
7: 0	R/W	0	reg_vks_prelpf_ccoef3 : // signed , default = 0 mode of horizontal chroma prelpf for Keystone, normalized 128 as '1'

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Table 9-2249 VKS_PRELPF_CCOEF1 0x3105

Bit(s)	R/W	Default	Description
15: 8	R/W	0	reg_vks_prelpf_ccoef4 : // signed , default = 0 mode of horizontal chroma prelpf for Keystone, normalized 128 as '1'
7: 0	R/W	0	reg_vks_prelpf_ccoef5 : // signed , default = 0 mode of horizontal chroma prelpf for Keystone, normalized 128 as '1'

Table 9-2250 VKS_FILL_VAL 0x3106

Bit(s)	R/W	Default	Description
23:16	R/W	0	reg_vks_fill_value0 : // unsigned , default = 0 , border fill color define. yuv: [0 128 128]; rgb:[0 0 0] ,use 8 bits in 12bit path,6bits in 10bit path
15: 8	R/W	128	reg_vks_fill_value1 : // unsigned , default = 128 , border fill color define. yuv: [0 128 128]; rgb:[0 0 0] ,use 8 bits in 12bit path,6bits in 10bit path
7: 0	R/W	128	reg_vks_fill_value2 : // unsigned , default = 128 , border fill color define. yuv: [0 128 128]; rgb:[0 0 0] ,use 8 bits in 12bit path,6bits in 10bit path

Table 9-2251 VKS_IWIN_HSIZE 0x3107

Bit(s)	R/W	Default	Description
29:16	R/W	160	reg_vks_iwinx0 : // unsigned , default = 160 , input start-col and end-col;
13: 0	R/W	1279	reg_vks_iwinx1 : // unsigned , default = 1279 , input start-col and end-col;

Table 9-2252 VKS_IWIN_VSIZE 0x3108

Bit(s)	R/W	Default	Description
29:16	R/W	0	reg_vks_iwiny0 : // unsigned , default = 0 , input start-row and end-row;
13: 0	R/W	719	reg_vks_iwiny1 : // unsigned , default = 719 , input start-row and end-row;

Table 9-2253 VKS_TOP_MISC 0x3109

Bit(s)	R/W	Default	Description
18	R/W	1	reg_flt_en : // unsigned , default = 1
17	R/W	0	reg_frm_rst : // unsigned , default = 0
16	R/W	0	reg_ctrl_sync : // unsigned , default = 0
15: 8	R/W	4	blank_num : // unsigned , default = 4
7: 0	R/W	9	flt_blank_num : // unsigned , default = 9

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Table 9-2254 VKS_START_CTRL 0x310a

Bit(s)	R/W	Default	Description
16	R/W	0	reg_vks_en_mode : // unsigned , default = 0
15: 0	R/W	5	reg_hold_phnum : // unsigned , default = 5

Table 9-2255 VKS_LBUF_SIZE 0x310b

Bit(s)	R/W	Default	Description
11: 0	R/W	1024	reg_lbuf_depth : // unsigned , default = 1024

Table 9-2256 VKS_PARA_ADDR_PORT 0x310e

Bit(s)	R/W	Default	Description
31: 0	R/W	3ff	Access address for vkstone para_lut,start address must be 0x09

Table 9-2257 VKS_PARA_DATA_PORT 0x310f

Bit(s)	R/W	Default	Description
31: 0	R/W	/	Data access for vkstone para lut

Below are the detail registers of VKS_PARA_DATA_PORT and VKS_PARA_ADDR_PORT control:

Table 9-2258 VKS_SCL_OFFSET00 ~ VKS_SCL_OFFSET16 0X09~0X19

Bit(s)	R/W	Default	Description
31:20			reserved
19: 0	R/W	/	Left offset of the input pixel offset from the left 12bits pixel and 8 bits float phase

Table 9-2259 VKS_SCL_STEP00 ~ VKS_SCL_STEP16 0X1A~0X2A

Bit(s)	R/W	Default	Description
24:20			reserved
23: 0	R/W	/	Unsigned reg_scl_stepx for ratio of each line(defined piece),step:4.20 opxium = (ipxium << 20)/step scale:4.2 = 1/step

Table 9-2260 VKS_PPS_YCOEF00 ~ VKS_PPS_YCOEF32 0X2B~0X4B

Bit(s)	R/W	Default	Description
31:24	R/W	/	Signed reg_vks_ycoef0 Poly_phase scalar coef
23:16	R/W	/	Signed reg_vks_ycoef1 Poly_phase scalar coef
15:8	R/W	/	Signed reg_vks_ycoef2 Poly_phase scalar coef
7: 0	R/W	/	Signed reg_vks_ycoef3 Poly_phase scalar coef

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Table 9-2261 VKS_PPS_CCOEF00 ~ VKS_PPS_CCOEF32 0X4C~0X6C

Bit(s)	R/W	Default	Description
31:24	R/W	/	Signed reg_vks_ccoef0 Poly_phase scalar coef
23:16	R/W	/	Signed reg_vks_ccoef1 Poly_phase scalar coef
15:8	R/W	/	Signed reg_vks_ccoef2 Poly_phase scalar coef
7: 0	R/W	/	Signed reg_vks_ccoef3 Poly_phase scalar coef

9.2.3.34 OSD1 Registers

Table 9-2262 VIU_OSD1_CTRL_STAT 0x1A10

Bit(s)	R/W	Default	Description
31	R/W	0	osd_cfg_syn_en : // unsigned , default =0 1: module enable sync by go_field 0: normal
30	R/W	0	ENABLE_FREE_CLK. 1 = Use free-running clock; 0 = Use gated clock to save power.
29	R	0	TEST_RD_DSR: Applicable only when OSD debug mode is enabled. 1 = A new pixel is ready at register VIU_OSD1_TEST_RDDATA; 0 = No data ready.
/	/	/	/
27-24	R	0	OSD_BLK_MODE: the input pixel format of which the current OSD block is being processed. Mali src & normal src have different pixel format value for same format
23-22	R	0	OSD_BLK_PTR: The number of the current OSD block that is being processed.
21	R	0	OSD_ENABLE. 1 = OSD display is enabled; 0 = disabled.
20-12	R/W	0	GLOBAL_ALPHA: legal range 0 – 256. It is a 9-bit value that is multiplied to all output pixel's Alpha value, and then normalized, i.e.: Alpha_tmp = Alpha_internal + (Alpha_internal == 0 ? 0 : 1); Alpha_out = (Alpha_tmp * GLOBAL_ALPHA) / 256;
11	R/W	0	TEST_RD_EN: OSD debug mode enable. 1 = Output pixels are not routed to VPP, instead they are presented on registers VIU_OSD1_TEST_RDDATA, for CPU to read. 0 = Normal mode, pixels are output to VPP.
10-9	R/W	0	unused
8-5	R/W	0	CTRL_MTCH_Y: For OSD 444, 422 or 16-bit (COLOR_MATRIX = 0 or 1) mode, the input pixels contain no Alpha information, in order to associated the output pixel with an Alpha value, the following steps are taken: If TC_ALPHA_EN = 0, then all output pixels use a default Alpha value 0xFF; If TC_ALPHA_EN = 1, then the Alpha value is looked up by matching the pixel's Y/Cb/Cr against four Alpha registers' Y/Cb/Cr. If the pixel matches any one of the Alpha registers, then this register's Alpha value is used; If the pixel matches with more than one of the Alpha registers, then the lower Alpha register takes priority, e.g. use Alpha Reg0's value if the pixel match both Alpha Reg0 and Reg1; If no match, then use default Alpha value 0xFF. There are two ways of matching: one way is that the pixel has to compare all Y, Cb and Cr value with the Alpha registers; the other way is that the pixel only has to compare Y value with the Alpha registers. CTRL_MTCH_Y defines which way is used to determine a match. Bit[0] is for matching Alpha register 0: 1 = only need to compare Y; 0 = compare all Y, Cb and Cr.

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Bit(s)	R/W	Default	Description
			Bit[1] is for matching Alpha register 1: 1 = only need to compare Y; 0 = compare all Y, Cb and Cr. Bit[2] is for matching Alpha register 2: 1 = only need to compare Y; 0 = compare all Y, Cb and Cr. Bit[3] is for matching Alpha register 3: 1 = only need to compare Y; 0 = compare all Y, Cb and Cr.
4	R/W	0	CTRL_422TO444. 1 = Enable conversion of 422 format input to 444 format output; 0 = Disable 422 to 444 conversion.
/	/	/	/
2	R/W	0	osd_mem_mode : // unsigned , default =0 0:canvas_araddr 1: linear_araddr (mali src must use this mode)
1	R/W	0	premult_en : // unsigned , default =0
0	R/W	0	OSD_BLK_ENABLE: Each bit to enable display an OSD block

Table 9-2263 VIU_OSD1_CTRL_STAT2 0x1A2d

Bit(s)	R/W	Default	Description
31-16	R	0	unused
15	R/W	0	unused
14	R/W	0	Replaced_alpha_en
13-6	R/W	0	Replaced_alpha
5-4	R/W	0	Hold_fifo_lines[6:5]
3	R/W	0	RGBYUV_FULL_RANGE: Select coefficients for applicable output range. 1 = output full range 0-255; 0 = output range 16-235.
2	R/W	0	ALPHA_9B_MODE: Define how to expand 8-bit alpha value to 9-bit. 1 = The formula is (Alpha < 128) ? Alpha : Alpha + 1; 0 = The formula is (Alpha == 0) ? Alpha : Alpha + 1.
1	R/W	0	Pedding status cleanup
0	R/W	0	COLOR_EXPAND_MODE. 1 = Expand the color components to 8-bit by padding LSBs with MSBs. E.g. If the input is 5'b11000, the output is expanded to 8'b11000110; 0 = Expand the color components to 8-bit by padding LSBs with 0.

VIU_OSD1_TCOLOR_AG0 0x1A17

VIU_OSD1_TCOLOR_AG1 0x1A18

VIU_OSD1_TCOLOR_AG2 0x1A19

VIU_OSD1_TCOLOR_AG3 0x1A1a

Table 9-2264 Define Alpha register 0/1/2/3 values.

Bit(s)	R/W	Default	Description
31-24	R/W	0xFF	Y or R.
23-16	R/W	0xFF	CB or G.

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Bit(s)	R/W	Default	Description
15-8	R/W	0xFF	CR or B.
7-0	R/W	0xFF	ALPHA.

Table 9-2265 VIU_OSD1_BLK0_CFG_W0 0x1A1b Defines display block 0/1/2/3's property, word 0.

Bit(s)	R/W	Default	Description
31	R/W	0	Reserved
30	R/W	0	mali_src_en 1: read data from mali afbcd decoder 0: read data from DDR directly
29	R/W	0	y_rev: 0=normal read, 1=reverse read in Y direction
28	R/W	0	x_rev: 0=normal read, 1=reverse read in X direction
27-24	R/W	0	Reserved
23-16	R/W	0	TBL_ADDR. Virtual canvas LUT entry.
15	R/W	0	LITTLE_ENDIAN: define the of data stored in DDR. 1 = Data stored in DDR memory are of little endian; 0 = Data stored in DDR memory are of big endian.
14	R/W	0	RPT_Y: For reducing data size stored in DDR. 1 = For each line, OSD will display twice; 0 = No repeat, OSD display once per line.
13-12	R/W	0	INTERP_CTRL: If enabled, interpolate a data after each incoming pixels, in order to save DDR bandwidth. 0 = No interpolation; 1 = unused, no interpolation; 2 = Interpolate with preceding pixel value; 3 = Interpolate with the averaged value between the preceding pixel and the next pixel.
11-8	R/W	0	OSD_BLK_MODE: Define the OSD block's input pixel format according bit30. Bit30 == 0: 0 = 2-bit per pixel, totally 4 colors can be looked up from color palette LUT,Only OSD2 have; 1 = 4-bit per pixel, totally 16 colors can be looked up from color palette LUT,Only OSD2 have; 2 = 8-bit per pixel, totally 256 colors can be looked up from color palette LUT,Only OSD2 have; 3 = 4:2:2 mode. Input 32-bit data for 2 pixels. Bit[31:24] is Y0, bit [23:16] is Cb0, bit[15:8] is Y1, bit [7:0] is Cr0, for Alpha value refer to reg VIU_OSD1_CTRL_STAT.CTRL_MTCH_Y; 4 = 16-bit mode. Refer to COLOR_MATRIX; 5 = 32-bit mode. Refer to COLOR_MATRIX; 6 = unused; 7 = 24-bit mode. Refer to COLOR_MATRIX; 8-15 = unused; Bit30 == 1: 0:R8 1:8bit yuv422 2:RGB565 3:RGBA5551 4:RGBA4444 5: RGBA8888 7:RGB888 8:10bit yuv422 9:RGBA1010102 Other:unuse
6	R/W	0	TC_ALPHA_EN: refer to reg VIU_OSD1_CTRL_STAT.CTRL_MTCH_Y. 1 = Enable alpha register matching. 0 = Disable.
5-2	R/W	0	COLOR_MATRIX: Applicable only to 16-bit color mode (OSD_BLK_MODE=4), 32-bit mode (OSD_BLK_MODE=5) and 24-bit mode (OSD_BLK_MODE=7), defines the bit-field allocation of the pixel data. For expanding the bit-fields to full 8-bit, refer to VIU_OSD1_CTRL_STAT2.color_expand_mode and VIU_OSD1_CTRL_STAT2.alpha_expand_mode.

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Bit(s)	R/W	Default	Description
			For 16-bit mode (OSD_BLK_MODE=4): 0 = 6:5:5 format. Bit[15:10] is Y[7:2] or R [7:2], bit[9:5] is Cb[7:3] or G[7:3], bit[4:0] is Cr[7:3] or B[7:3], for Alpha value refer to reg VIU_OSD1_CTRL_STAT.CTRL_MTCH_Y; 1 = 8:4:4 format. Bit[15:8] is Y or R, bit[7:4] is Cb[7:4] or G[7:4], bit[3:0] is Cr[7:4] or B[7:4]], for Alpha value refer to reg VIU_OSD1_CTRL_STAT.CTRL_MTCH_Y; For 32-bit mode (OSD_BLK_MODE=5): 0 = RGBA 8:8:8:8 format. Bit[31:24] is Y or R, bit[23:16] is Cb or G; bit[15:8] is Cr or B; bit[7:0] is Alpha; 1 = ARGB 8:8:8:8 format. Bit[31:24] is Alpha, bit[23:16] is Y or R; bit[15:8] is Cb or G; bit[7:0] is Cr or B; 2 = ABGR 8:8:8:8 format. Bit[31:24] is Alpha, bit[23:16] is Cr or B; bit[15:8] is Cb or G; bit[7:0] is Y or R; 3 = BGRA 8:8:8:8 format. Bit[31:24] is Cr or B, bit [23:16] is Cb or G; bit[15:8] is Y or R; bit[7:0] is Alpha. For 24-bit mode (OSD_BLK_MODE=7): 0 = RGB 8:8:8 mode. Bit[23:16] is Y or R, bit[15:8] is Cb or G, bit[7:0] is Cr or B, for Alpha value refer to reg VIU_OSD1_ CTRL_STAT.CTRL_MTCH_Y; 5 = BGR 8:8:8 mode. Bit[23:16] is Cr or B, bit [15:8] is Cb or G, bit[7:0] is Y or R, for Alpha value refer to reg VIU_OSD1_ CTRL_STAT.CTRL_MTCH_Y.
1	R/W	0	INTERLACE_EN. 1 = Enable interlace mode. 0 = Disable.
0	R/W	0	INTERLACE_SEL_ODD: Applicable only if INTERLACE_EN = 1. 1 = Only output odd lines; 0 = Only output even lines.

Table 9-2266 VIU_OSD1_BLK0_CFG_W1 0x1A1c Defines display block 0/1/2/3's property, word 1.

Bit(s)	R/W	Default	Description
31-29	R/W	0	Unused.
28-16	R/W	0	X_END. Virtual canvas co-ordinate.
15-13	R/W	0	Unused.
12-0	R/W	0	X_START. Virtual canvas co-ordinate.

Table 9-2267 VIU_OSD1_BLK0_CFG_W2 0x1A1d Defines display block 0/1/2/3's property, word 2.

Bit(s)	R/W	Default	Description
31-29	R/W	0	Unused.
28-16	R/W	0	Y_END. Virtual canvas co-ordinate.
15-13	R/W	0	Unused.
12-0	R/W	0	Y_START. Virtual canvas co-ordinate.

Table 9-2268 VIU_OSD1_BLK0_CFG_W3 0x1A1e Defines display block 0/1/2/3's property, word 3.

Bit(s)	R/W	Default	Description
31-28	R/W	0	Unused.
27-16	R/W	0	H_END. Display horizontal co-ordinate.
15-12	R/W	0	Unused.
11-0	R/W	0	H_START. Display horizontal co-ordinate.

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Table 9-2269 VIU_OSD1_BLK0_CFG_W4 0x1A13 Defines display block 0/1/2/3's property, word 4.

Bit(s)	R/W	Default	Description
31-28	R/W	0	Unused.
27-16	R/W	0	V_END. Display vertical co-ordinate.
15-12	R/W	0	Unused.
11-0	R/W	0	V_START. Display vertical co-ordinate.

Table 9-2270 VIU_OSD1_BLK1_CFG_W4 0x1a14

Bit(s)	R/W	Default	Description
31:0	R/W	0	Frame_addr: // unsigned , default =0 Frame_addr in linear_addr

Table 9-2271 VIU_OSD1_BLK2_CFG_W4 0x1a15

Bit(s)	R/W	Default	Description
31:0	R/W	0	Line_stride : // unsigned , default =0 Line_stride in linear_addr

Table 9-2272 VIU_OSD1_FIFO_CTRL_STAT 0x1A2b

Bit(s)	R/W	Default	Description
31	R/W	0	burst_len_sel[2] of [2:0]
30	R/W	0	BYTE_SWAP: In addition to endian control, further define whether to swap upper byte and lower byte within a 16-bit memory word. 1 = Swap, data[15:0] becomes {data[7:0], data[15:8]}; 0 = No swap, data[15:0] is still data[15:0].
29	R/W	0	Div_swap : swap the 2 64bits word in 128bits word
28-24	R/W	0	Fifo_lim : when osd fifo is small than the fifo_lim*16, closed the req port of osd_ rd_mif
23-22	R/W	0	Fifo_ctrl: 00 : for 1 word in 1 burst, 01 : for 2words in 1burst, 10 : for 4 words in 1burst, 11: reserved
21-20	R	0	FIFO_ST: State of the FIFO activity. 0 = Idle; 1 = FIFO requesting; 2 = FIFO request aborting.
19	R	0	FIFO_OVERFLOW.
18-12	R/W	32	FIFO_DEPTH_VAL: Define the depth of FIFO which stores 128-bit data from DDR to be FIFO_DEPTH_VAL * 8.
11-10	R/W	0	BURST_LEN_SEL[1:0] of [2:0]: Define DDR burst request length. 0 = up to 24 per burst; 1 = up to 32 per burst; 2 = up to 48 per burst;/ 3 = up to 64 per burst. 4 = up to 96 per burst, 5 = up to 128 per burst

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Bit(s)	R/W	Default	Description
9-5	R/W	4	HOLD_FIFO_LINES: The number of lines that OSD must wait after VSYNC, before it starts request data from DDR .
4	R/W	0	CLEAR_ERR: One pulse to clear error status.
3	R/W	0	FIFO_SYNC_RST: Set 1 to reset OSD FIFO.
2-1	R/W	0	ENDIAN: define the endianess of the 64-bit data stored in memory, and how to convert. 0 = No convertion; 1 = Convert to {din[31:0], din[63:32]}; 2 = Convert to {din[15:0], din[31:16], din[47:32], din[63:48]}; 3 = Convert to {din[47:32], din[63:48], din[15:0], din[31:16]};
0	R/W	0	URGENT. 1 = Set DDR request priority to be urgent; 0 = Set DDR request priority to be normal.

During OSD debug mode (VIU_OSD1_CTRL_STAT.TEST_RD_EN = 1), the output pixels will be presented at this register.

Table 9-2273 VIU_OSD1_TEST_RDDATA 0x1A2c

Bit(s)	R/W	Default	Description
31-24	R	0	Y or R.
23:16	R	0	Cb or G.
15-8	R	0	Cr or B.
7-0	R	0	Alpha[8:1].

Table 9-2274 VIU_OSD1_PROT_CTRL 0x1a2e

Bit(s)	R/W	Default	Description
31:16	R/W	0	urgent_ctrl : // unsigned , default =0
15	R.O	0	prot_en : // unsigned , default =0; 1=Borrow PROT's FIFO storage, either for rotate or non-rotate.
12: 0	R.O	0	prot_fifo_size : // unsigned , default =0; effective FIFO size when prot_en=1.

Table 9-2275 VIU_OSD1_MALI_UNPACK_CTRL 0x1a2f

Bit(s)	R/W	Default	Description
31	R/W	0	mali_unpack_en 1: OSD will unpack mali_src 0: OSD will unpack normal src
28			Alpha_div_en: alpha dividor enable
27:26			Alpha_dividor gating clk
25:24			Alpa_mapping_mode In osd,this bit should be set 0 when Alpha_div_en active,means 8 bits alpha mode
17	/	/	/
16	R/W	0	afbcd_swap_64bit:

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Bit(s)	R/W	Default	Description
15: 12	R/W	1	afbcd_r_reorder,change osd output order when use mali src: 1: r_re = r ; 2: r_re = g; 3: r_re = b; 4: r_re = a; default: r_re = 0;
11: 8		2	afbcd_r_reorder,change osd output order when use mali src: 1: g_re = r ; 2: g_re = g; 3: g_re = b; 4: g_re = a; default: r_re = 0;
7: 4		3	afbcd_r_reorder,change osd output order when use mali src: 1: b_re = r ; 2: b_re = g; 3: b_re = b; 4: b_re = a; default: r_re = 0;
3: 0		4	afbcd_r_reorder,change osd output order when use mali src: 1: a_re = r ; 2: a_re = g; 3: a_re = b; 4: a_re = a; default: r_re = 0;

Table 9-2276 VIU_OSD1_DIMM_CTRL 0x1adf

Bit(s)	R/W	Default	Description
30	R/W	0	OSD dimm enable,osd out will be one color when this bit active
29:0	R/W	0	Osd_dim_rgb_out ,osd out will be this vaaule when bit30 active

9.2.3.35 OSD2 Registers

VIU_OSD2_CTRL_STAT 0x1a30

See: VIU_OSD1_CTRL_STAT

VIU_OSD2_CTRL_STAT2 0x1a4d

See: VIU_OSD1_CTRL_STAT2

VIU_OSD2_COLOR_ADDR 0x1a31

See: VIU_OSD1_COLOR_ADDR

VIU_OSD2_COLOR 0x1a32

See: VIU_OSD1_COLOR

VIU_OSD2_TCOLOR_AG0 0x1a37

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See: VIU_OSD1_TCOLOR_AG0

VIU_OSD2_TCOLOR_AG1 0x1a38
See: VIU_OSD1_TCOLOR_AG1

VIU_OSD2_TCOLOR_AG2 0x1a39
See: VIU_OSD1_TCOLOR_AG02

VIU_OSD2_TCOLOR_AG3 0x1a3a
See: VIU_OSD1_TCOLOR_AG3

VIU_OSD2_BLK0_CFG_W0 0x1a3b
See: VIU_OSD1_BLK0_CFG_W0

VIU_OSD2_BLK0_CFG_W1 0x1a3c
See: VIU_OSD1_BLK0_CFG_W1

VIU_OSD2_BLK0_CFG_W2 0x1a3d
See: VIU_OSD1_BLK0_CFG_W2

VIU_OSD2_BLK0_CFG_W3 0x1a3e
See: VIU_OSD1_BLK0_CFG_W3

VIU_OSD2_BLK0_CFG_W4 0x1a64
See: VIU_OSD1_BLK0_CFG_W4

VIU_OSD2_BLK1_CFG_W4 0x1a65
See: VIU_OSD2_BLK1_CFG_W4

VIU_OSD2_BLK2_CFG_W4 0x1a66
See: VIU_OSD1_BLK2_CFG_W4

VIU_OSD2_FIFO_CTRL_STAT 0x1a4b
See: VIU_OSD1_FIFO_CTRL_STAT

VIU_OSD2_TEST_RDDATA 0x1a4c
See: VIU_OSD1_TEST_RDDATA

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VIU_OSD2_PROT_CTRL 0x1a4e
See: VIU_OSD1_PROT_CTRL

VIU_OSD2_MALI_UNPACK_CTRL 0x1abd
See: VIU_OSD1_MALI_UNPACK_CTRL

VIU_OSD2_DIMM_CTRL 0x1acf
See: VIU_OSD1_DIMM_CTRL

9.2.3.36 OSD3 Registers

VIU_OSD3_CTRL_STAT 0x3d80
See: VIU_OSD1_CTRL_STAT

VIU_OSD3_CTRL_STAT2 0x3d81
See: VIU_OSD1_CTRL_STAT2

VIU_OSD3_COLOR_ADDR 0x3d82
See: VIU_OSD1_COLOR_ADDR

VIU_OSD3_COLOR 0x3d83
See: VIU_OSD1_COLOR

VIU_OSD3_TCOLOR_AG0 0x3d84
See: VIU_OSD1_TCOLOR_AG0

VIU_OSD3_TCOLOR_AG1 0x3d85
See: VIU_OSD1_TCOLOR_AG1

VIU_OSD3_TCOLOR_AG2 0x3d86
See: VIU_OSD1_TCOLOR_AG02

VIU_OSD3_TCOLOR_AG3 0x3d87
See: VIU_OSD1_TCOLOR_AG3

VIU_OSD3_BLK0_CFG_W0 0x3d88
See: VIU_OSD1_BLK0_CFG_W0

VIU_OSD3_BLK0_CFG_W1 0x3d8c

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See: VIU_OSD1_BLK0_CFG_W1

VIU_OSD3_BLK0_CFG_W2 0x3d90
See: VIU_OSD1_BLK0_CFG_W2

VIU_OSD3_BLK0_CFG_W3 0x3d94
See: VIU_OSD1_BLK0_CFG_W3

VIU_OSD3_BLK0_CFG_W4 0x3d98
See: VIU_OSD1_BLK0_CFG_W4

VIU_OSD3_BLK1_CFG_W4 0x3d99
See: VIU_OSD3_BLK1_CFG_W4

VIU_OSD3_BLK2_CFG_W4 0x3d9a
See: VIU_OSD1_BLK2_CFG_W4

VIU_OSD3_FIFO_CTRL_STAT 0x3d9c
See: VIU_OSD1_FIFO_CTRL_STAT

VIU_OSD3_TEST_RDDATA 0x3d9d
See: VIU_OSD1_TEST_RDDATA

VIU_OSD3_PROT_CTRL 0x3d9e
See: VIU_OSD1_PROT_CTRL

VIU_OSD3_MALI_UNPACK_CTRL 0x3d9f
See: VIU_OSD1_MALI_UNPACK_CTRL

VIU_OSD3_DIMM_CTRL 0x3da0
See: VIU_OSD1_DIMM_CTRL

9.2.3.37 VPP_VD1_MATRIX Registers

Table 9-2277 VPP_VD1_MATRIX_COEF00_01 0x3290

Bit(s)	R/W	Default	Description
28-16	R/W	0	Coefficient00, signed, 3.10
12-0	R/W	0	Coefficient01, signed, 3.10

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Table 9-2278 VPP_VD1_MATRIX_COEF02_10 0x3291

Bit(s)	R/W	Default	Description
28-16	R/W	0	Coefficient02, signed, 3.10
12-0	R/W	0	Coefficient10, signed, 3.10

Table 9-2279 VPP_VD1_MATRIX_COEF11_12 0x3292

Bit(s)	R/W	Default	Description
28-16	R/W	0	Coefficient11, signed, 3.10
12-0	R/W	0	Coefficient12, signed, 3.10

Table 9-2280 VPP_VD1_MATRIX_COEF20_21 0x3293

Bit(s)	R/W	Default	Description
28-16	R/W	0	Coefficient20, signed, 3.10
12-0	R/W	0	Coefficient21, signed, 3.10

Table 9-2281 VPP_VD1_MATRIX_COEF22 0x3294

Bit(s)	R/W	Default	Description
18-16	R/W	0	convrs
12-0	R/W	0	Coefficient22, signed, 3.10

Table 9-2282 VPP_VD1_MATRIX_COEF13_14 0x3295

Bit(s)	R/W	Default	Description
28-16	R/W	0	Coefficient13, signed, 3.10
12-0	R/W	0	Coefficient14, signed, 3.10

Table 9-2283 VPP_VD1_MATRIX_COEF23_24 0x3296

Bit(s)	R/W	Default	Description
28-16	R/W	0	Coefficient23, signed, 3.10
12-0	R/W	0	Coefficient24, signed, 3.10

Table 9-2284 VPP_VD1_MATRIX_COEF15_25 0x3297

Bit(s)	R/W	Default	Description
28-16	R/W	0	Coefficient15, signed, 3.10
12-0	R/W	0	Coefficient25, signed, 3.10

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Table 9-2285 VPP_VD1_MATRIX_CLIP 0x3298

Bit(s)	R/W	Default	Description
31-8	R/W	0x0	reserved
7-5	R/W	0x1	Matrix rs
4-3	R/W	0x10	Matrix clmod 0: only 3x3, 1: pre_offseted_ch1,ch2> pre_offseted_ch0, use the added 2x3 coef 2: pre_offseted_ch1,ch2 > 0, use the added 2x3 coef 3: pre_offseted_ch1,ch2 > 512, use the added 2x3 coef
2-0	R/W	0x10	/

Table 9-2286 VPP_VD1_MATRIX_OFFSET0_1 0x3299

Bit(s)	R/W	Default	Description
27-16	R/W	0	Offset0, signed value
11-0	R/W	0	Offset1, signed value

Table 9-2287 VPP_VD1_MATRIX_OFFSET2 0x329a

Bit(s)	R/W	Default	Description
11-0	R/W	0	Offset2, signed value

Table 9-2288 VPP_VD1_MATRIX_PRE_OFFSET0_1 0x329b

Bit(s)	R/W	Default	Description
27-16	R/W	0	pre_Offset0, signed value
11-0	R/W	0	Pre_Offset1, signed value

Table 9-2289 VPP_VD1_MATRIX_PRE_OFFSET2 0x329c

Bit(s)	R/W	Default	Description
11-0	R/W	0	Pre_Offset2, signed value

Table 9-2290 VPP_VD1_MATRIX_EN_CTRL 0x329d

Bit(s)	R/W	Default	Description
5:4	R/W	0	Gate clock ctrl
1	R/W	0	Enable_sync_sel
0	R/W	0	Conv_en_pre

9.2.3.38 VPP_POST_MATRIX Registers

VPP_POST_MATRIX_COEF00_01 0x32b0

See: VPP_VD1_MATRIX_COEF00_01

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VPP_POST_MATRIX_COEF02_10 0x32b1

See: VPP_VD1_MATRIX_COEF02_10

VPP_POST_MATRIX_COEF11_12 0x32b2

See: VPP_VD1_MATRIX_COEF11_12

VPP_POST_MATRIX_COEF20_21 0x32b3

See: VPP_VD1_MATRIX_COEF20_21

VPP_POST_MATRIX_COEF22 0x32b4

See: VPP_VD1_MATRIX_COEF22

VPP_POST_MATRIX_COEF13_14 0x32b5

See: VPP_VD1_MATRIX_COEF13_14

VPP_POST_MATRIX_COEF23_24 0x32b6

See: VPP_VD1_MATRIX_COEF23_24

VPP_POST_MATRIX_COEF15_25 0x32b7

See: VPP_VD1_MATRIX_COEF15_25

VPP_POST_MATRIX_CLIP 0x32b8

See: VPP_VD1_MATRIX_CLIP

VPP_POST_MATRIX_OFFSET0_1 0x32b9

See: VPP_VD1_MATRIX_OFFSET0_1

VPP_POST_MATRIX_OFFSET2 0x32ba

See: VPP_VD1_MATRIX_OFFSET2

VPP_POST_MATRIX_PRE_OFFSET0_1 0x32bb

See: VPP_VD1_MATRIX_PRE_OFFSET0_1

VPP_POST_MATRIX_PRE_OFFSET2 0x32bc

See: VPP_VD1_MATRIX_PRE_OFFSET2

VPP_POST_MATRIX_EN_CTRL 0x32bd

See: VPP_VD1_MATRIX_EN_CTRL

Table 9-2291 VPP_POST_MATRIX_SAT 0x32c1

Bit(s)	R/W	Default	Description
2	R/W	0	sat_o_en:If true, the output result of post matrix output is saturated
1	R/W	0	sat_i_en:If true, the input result of post matrix output is saturated
0	R/W	0	misc_sat_en:same as sat_i_en

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9.2.3.39 VPP_POST2_MATRIX Registers

VPP_POST2_MATRIX_COEF00_01 0x39a0

See: VPP_VD1_MATRIX_COEF00_01

VPP_POST2_MATRIX_COEF02_10 0x39a1

See: VPP_VD1_MATRIX_COEF02_10

VPP_POST2_MATRIX_COEF11_12 0x39a2

See: VPP_VD1_MATRIX_COEF11_12

VPP_POST2_MATRIX_COEF20_21 0x39a3

See: VPP_VD1_MATRIX_COEF20_21

VPP_POST2_MATRIX_COEF22 0x39a4

See: VPP_VD1_MATRIX_COEF22

VPP_POST2_MATRIX_COEF13_14 0x39a5

See: VPP_VD1_MATRIX_COEF13_14

VPP_POST2_MATRIX_COEF23_24 0x39a6

See: VPP_VD1_MATRIX_COEF23_24

VPP_POST2_MATRIX_COEF15_25 0x39a7

See: VPP_VD1_MATRIX_COEF15_25

VPP_POST2_MATRIX_CLIP 0x39a8

See: VPP_VD1_MATRIX_CLIP

VPP_POST2_MATRIX_OFFSET0_1 0x39a9

See: VPP_VD1_MATRIX_OFFSET0_1

VPP_POST2_MATRIX_OFFSET2 0x39aa

See: VPP_VD1_MATRIX_OFFSET2

VPP_POST2_MATRIX_PRE_OFFSET0_1 0x39ab

See: VPP_VD1_MATRIX_PRE_OFFSET0_1

VPP_POST2_MATRIX_PRE_OFFSET2 0x39ac

See: VPP_VD1_MATRIX_PRE_OFFSET2

VPP_POST2_MATRIX_EN_CTRL 0x39ad

See: VPP_VD1_MATRIX_EN_CTRL

9.2.3.40 VPP_OSD2_MATRIX Registers

VPP_OSD2_MATRIX_COEF00_01 0x3920

See: VPP_VD1_MATRIX_COEF00_01

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VPP_OSD2_MATRIX_COEF02_10 0x3921
See: VPP_VD1_MATRIX_COEF02_10

VPP_OSD2_MATRIX_COEF11_12 0x3922
See: VPP_VD1_MATRIX_COEF11_12

VPP_OSD2_MATRIX_COEF20_21 0x3923
See: VPP_VD1_MATRIX_COEF20_21

VPP_OSD2_MATRIX_COEF22 0x3924
See: VPP_VD1_MATRIX_COEF22

VPP_OSD2_MATRIX_COEF13_14 0x3925
See: VPP_VD1_MATRIX_COEF13_14

VPP_OSD2_MATRIX_COEF23_24 0x3926
See: VPP_VD1_MATRIX_COEF23_24

VPP_OSD2_MATRIX_COEF15_25 0x3927
See: VPP_VD1_MATRIX_COEF15_25

VPP_OSD2_MATRIX_CLIP 0x3928
See: VPP_VD1_MATRIX_CLIP

VPP_OSD2_MATRIX_OFFSET0_1 0x3929
See: VPP_VD1_MATRIX_OFFSET0_1

VPP_OSD2_MATRIX_OFFSET2 0x392a
See: VPP_VD1_MATRIX_OFFSET2

VPP_OSD2_MATRIX_PRE_OFFSET0_1 0x392b
See: VPP_VD1_MATRIX_PRE_OFFSET0_1

VPP_OSD2_MATRIX_PRE_OFFSET2 0x392c
See: VPP_VD1_MATRIX_PRE_OFFSET2

VPP_OSD2_MATRIX_EN_CTRL 0x392d

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See: VPP_VD1_MATRIX_EN_CTRL

9.2.3.41 VPP_WRAP_OSD1_MATRIX Registers

VPP_WRAP_OSD1_MATRIX_COEF00_01 0x3d60
See: VPP_VD1_MATRIX_COEF00_01

VPP_WRAP_OSD1_MATRIX_COEF02_10 0x3d61
See: VPP_VD1_MATRIX_COEF02_10

VPP_WRAP_OSD1_MATRIX_COEF11_12 0x3d62
See: VPP_VD1_MATRIX_COEF11_12

VPP_WRAP_OSD1_MATRIX_COEF20_21 0x3d63
See: VPP_VD1_MATRIX_COEF20_21

VPP_WRAP_OSD1_MATRIX_COEF22 0x3d64
See: VPP_VD1_MATRIX_COEF22

VPP_WRAP_OSD1_MATRIX_COEF13_14 0x3d65
See: VPP_VD1_MATRIX_COEF13_14

VPP_WRAP_OSD1_MATRIX_COEF23_24 0x3d66
See: VPP_VD1_MATRIX_COEF23_24

VPP_WRAP_OSD1_MATRIX_COEF15_25 0x3d67
See: VPP_VD1_MATRIX_COEF15_25

VPP_WRAP_OSD1_MATRIX_CLIP 0x3d68
See: VPP_VD1_MATRIX_CLIP

VPP_WRAP_OSD1_MATRIX_OFFSET0_1 0x3d69
See: VPP_VD1_MATRIX_OFFSET0_1

VPP_WRAP_OSD1_MATRIX_OFFSET2 0x3d6a
See: VPP_VD1_MATRIX_OFFSET2

VPP_WRAP_OSD1_MATRIX_PRE_OFFSET0_1 0x3d6b
See: VPP_VD1_MATRIX_PRE_OFFSET0_1

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VPP_WRAP_OSD1_MATRIX_PRE_OFFSET2 0x3d6c
See: VPP_VD1_MATRIX_PRE_OFFSET2

VPP_WRAP_OSD1_MATRIX_EN_CTRL 0x3d6d
See: VPP_VD1_MATRIX_EN_CTRL

9.2.3.42 VPP_WRAP_OSD2_MATRIX Registers

VPP_WRAP_OSD2_MATRIX_COEF00_01 0x3d70
See: VPP_VD1_MATRIX_COEF00_01

VPP_WRAP_OSD2_MATRIX_COEF02_10 0x3d71
See: VPP_VD1_MATRIX_COEF02_10

VPP_WRAP_OSD2_MATRIX_COEF11_12 0x3d72
See: VPP_VD1_MATRIX_COEF11_12

VPP_WRAP_OSD2_MATRIX_COEF20_21 0x3d73
See: VPP_VD1_MATRIX_COEF20_21

VPP_WRAP_OSD2_MATRIX_COEF22 0x3d74
See: VPP_VD1_MATRIX_COEF22

VPP_WRAP_OSD2_MATRIX_COEF13_14 0x3d75
See: VPP_VD1_MATRIX_COEF13_14

VPP_WRAP_OSD2_MATRIX_COEF23_24 0x3d76
See: VPP_VD1_MATRIX_COEF23_24

VPP_WRAP_OSD2_MATRIX_COEF15_25 0x3d77
See: VPP_VD1_MATRIX_COEF15_25

VPP_WRAP_OSD2_MATRIX_CLIP 0x3d78
See: VPP_VD1_MATRIX_CLIP

VPP_WRAP_OSD2_MATRIX_OFFSET0_1 0x3d79
See: VPP_VD1_MATRIX_OFFSET0_1

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VPP_WRAP_OSD2_MATRIX_OFFSET2 0x3d7a
See: VPP_VD1_MATRIX_OFFSET2

VPP_WRAP_OSD2_MATRIX_PRE_OFFSET0_1 0x3d7b
See: VPP_VD1_MATRIX_PRE_OFFSET0_1

VPP_WRAP_OSD2_MATRIX_PRE_OFFSET2 0x3d7c
See: VPP_VD1_MATRIX_PRE_OFFSET2

VPP_WRAP_OSD2_MATRIX_EN_CTRL 0x3d7d
See: VPP_VD1_MATRIX_EN_CTRL

9.2.3.43 VPP_WRAP_OSD3_MATRIX Registers

VPP_WRAP_OSD3_MATRIX_COEF00_01 0x3db0
See: VPP_VD1_MATRIX_COEF00_01

VPP_WRAP_OSD3_MATRIX_COEF02_10 0x3db1
See: VPP_VD1_MATRIX_COEF02_10

VPP_WRAP_OSD3_MATRIX_COEF11_12 0x3db2
See: VPP_VD1_MATRIX_COEF11_12

VPP_WRAP_OSD3_MATRIX_COEF20_21 0x3db3
See: VPP_VD1_MATRIX_COEF20_21

VPP_WRAP_OSD3_MATRIX_COEF22 0x3db4
See: VPP_VD1_MATRIX_COEF22

VPP_WRAP_OSD3_MATRIX_COEF13_14 0x3db5
See: VPP_VD1_MATRIX_COEF13_14

VPP_WRAP_OSD3_MATRIX_COEF23_24 0x3db6
See: VPP_VD1_MATRIX_COEF23_24

VPP_WRAP_OSD3_MATRIX_COEF15_25 0x3db7
See: VPP_VD1_MATRIX_COEF15_25

VPP_WRAP_OSD3_MATRIX_CLIP 0x3db8

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See: VPP_VD1_MATRIX_CLIP

VPP_WRAP_OSD3_MATRIX_OFFSET0_1 0x3db9
See: VPP_VD1_MATRIX_OFFSET0_1

VPP_WRAP_OSD3_MATRIX_OFFSET2 0x3dba
See: VPP_VD1_MATRIX_OFFSET2

VPP_WRAP_OSD3_MATRIX_PRE_OFFSET0_1 0x3dbb
See: VPP_VD1_MATRIX_PRE_OFFSET0_1

VPP_WRAP_OSD3_MATRIX_PRE_OFFSET2 0x3dbc
See: VPP_VD1_MATRIX_PRE_OFFSET2

VPP_WRAP_OSD3_MATRIX_EN_CTRL 0x3dbd
See: VPP_VD1_MATRIX_EN_CTRL

9.2.3.44 HDR Registers

Table 9-2292 HDR VDIN0_HDR2_CTRL 0x1280

Bit(s)	R/W	Default	Description
20:18	R/W	0	reg_din_swap : // unsigned , default = 0
17	R/W	0	reg_out_fmt : // unsigned , default = 0
16	R/W	0	reg_only_mat : // unsigned , default = 0 ,only use input matrix ,work when hdr disable
15	R/W	0	mat_o_en,//output matrix enable ,only work when hdr enable
14	R/W	0	mat_in_en //input matrix enable ,only work when hdr enable
13	R/W	0	reg_VDIN0_HDR2_top_en : // unsigned , default = 0,hdr enable singal
12	R/W	1	reg_cgain_mode : // unsigned , default = 1
7: 6	R/W	1	reg_gmut_mode : // unsigned , default = 1
5	R/W	0	reg_in_shift : // unsigned , default = 0
4	R/W	1	reg_in_fmt : // unsigned , default = 1
3	R/W	1	reg_eo_enable : // unsigned , default = 1
2	R/W	1	reg_oe_enable : // unsigned , default = 1
1	R/W	1	reg_ogain_enable : // unsigned , default = 1
0	R/W	1	reg_cgain_enable : // unsigned , default = 1

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Table 9-2293 VDIN0_HDR2_CLK_GATE 0x1281

Bit(s)	R/W	Default	Description
31:30	R/W	0	clk_tm : gate clock ctrl (main clock) // unsigned , default = 0
29:28	R/W	0	output : matrix clock gate ctrl// unsigned , default = 0
25:24	R/W	0	input : matrix clock gate ctrl // unsigned , default = 0
23:22	R/W	0	hdr : top cbus clock gate ctrl // unsigned , default = 0
21:20	R/W	0	eotf : cbus clock gate ctrl // unsigned , default = 0
19:18	R/W	0	oetf : cbus clock gate ctrl // unsigned , default = 0
17:16	R/W	0	gamma : mult cbus clock gate ctrl // unsigned , default = 0
15:14	R/W	0	adaptive : cbus scaler clock gate ctrl // unsigned , default = 0
13:12	R/W	0	cgain : cbus clock gate ctrl// unsigned , default = 0
11:10	R/W	0	eotf : clock gate ctrl // unsigned , default = 0
9:8	R/W	0	oetf : clock gate ctrl // unsigned , default = 0
7:6	R/W	0	gamma : mult clock gate ctrl// unsigned , default = 0
5:4	R/W	0	adaptive : scaler clock gate ctrl // unsigned , default = 0
3:2	R/W	0	uv : gain clock gate ctrl // unsigned , default = 0
1:0	R/W	0	cgain : clock gate ctrl // unsigned , default = 0

Table 9-2294 VDIN0_HDR2_MATRIXI_COEF00_01 0x1282

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef00 : // signed , default = 0
12:0	R/W	0	coef01 : // signed , default = 0

Table 9-2295 VDIN0_HDR2_MATRIXI_COEF02_10 0x1283

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef02 : // signed , default = 0
12:0	R/W	0	coef10 : // signed , default = 0

Table 9-2296 VDIN0_HDR2_MATRIXI_COEF11_12 0x1284

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef11 : // signed , default = 0
12:0	R/W	0	coef12 : // signed , default = 0

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Table 9-2297 VDIN0_HDR2_MATRIXI_COEF20_21 0x1285

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef20 : // signed , default = 0
12:0	R/W	0	coef21 : // signed , default = 0

Table 9-2298 VDIN0_HDR2_MATRIXI_COEF22 0x1286

Bit(s)	R/W	Default	Description
12:0	R/W	0	coef22 : // signed , default = 0

Table 9-2299 VDIN0_HDR2_MATRIXI_COEF30_31 0x1287

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef13 : // signed , default = 0
12:0	R/W	0	coef14 : // signed , default = 0

Table 9-2300 VDIN0_HDR2_MATRIXI_COEF32_40 0x1288

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef23 : // signed , default = 0
12:0	R/W	0	coef24 : // signed , default = 0

Table 9-2301 VDIN0_HDR2_MATRIXI_COEF41_42 0x1289

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef15 : // signed , default = 0
12:0	R/W	0	coef25 : // signed , default = 0

Table 9-2302 VDIN0_HDR2_MATRIXI_OFFSET0_1 0x128A

Bit(s)	R/W	Default	Description
26:16	R/W	0	offset0 : // signed , default = 0
10:0	R/W	0	offset1 : // signed , default = 0

Table 9-2303 VDIN0_HDR2_MATRIXI_OFFSET2 0x128B

Bit(s)	R/W	Default	Description
10:0	R/W	0	offset2 : // signed , default = 0

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Table 9-2304 VDIN0_HDR2_MATRIXI_PRE_OFFSET0_1 0x128C

Bit(s)	R/W	Default	Description
26:16	R/W	0	pre_offset0 : // signed , default = 0
10:0	R/W	0	pre_offset1 : // signed , default = 0

Table 9-2305 VDIN0_HDR2_MATRIXI_PRE_OFFSET2 0x128D

Bit(s)	R/W	Default	Description
10:0	R/W	0	pre_offset2 : // signed , default = 0

Table 9-2306 VDIN0_HDR2_MATRIXO_COEF00_01 0x128E

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef00 : // signed , default = 0
12:0	R/W	0	coef01 : // signed , default = 0

Table 9-2307 VDIN0_HDR2_MATRIXO_COEF02_10 0x128F

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef02 : // signed , default = 0
12:0	R/W	0	coef10 : // signed , default = 0

Table 9-2308 VDIN0_HDR2_MATRIXO_COEF11_12 0x1290

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef11 : // signed , default = 0
12:0	R/W	0	coef12 : // signed , default = 0

Table 9-2309 VDIN0_HDR2_MATRIXO_COEF20_21 0x1291

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef20 : // signed , default = 0
12:0	R/W	0	coef21 : // signed , default = 0

Table 9-2310 VDIN0_HDR2_MATRIXO_COEF22 0x1292

Bit(s)	R/W	Default	Description
12:0	R/W	0	coef22 : // signed , default = 0

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Table 9-2311 VDIN0_HDR2_MATRIXO_COEF30_31 0x1293

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef13 : // signed , default = 0
12:0	R/W	0	coef14 : // signed , default = 0

Table 9-2312 VDIN0_HDR2_MATRIXO_COEF32_40 0x1294

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef23 : // signed , default = 0
12:0	R/W	0	coef24 : // signed , default = 0

Table 9-2313 VDIN0_HDR2_MATRIXO_COEF41_42 0x1295

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef15 : // signed , default = 0
12:0	R/W	0	coef25 : // signed , default = 0

Table 9-2314 VDIN0_HDR2_MATRIXO_OFFSET0_1 0x1296

Bit(s)	R/W	Default	Description
26:16	R/W	0	offset0 : // signed , default = 0
10:0	R/W	0	offset1 : // signed , default = 0

Table 9-2315 VDIN0_HDR2_MATRIXO_OFFSET2 0x1297

Bit(s)	R/W	Default	Description
10:0	R/W	0	offset2 : // signed , default = 0

Table 9-2316 VDIN0_HDR2_MATRIXO_PRE_OFFSET0_1 0x1298

Bit(s)	R/W	Default	Description
26:16	R/W	0	pre_offset0 : // signed , default = 0
10:0	R/W	0	pre_offset1 : // signed , default = 0

Table 9-2317 VDIN0_HDR2_MATRIXO_PRE_OFFSET2 0x1299

Bit(s)	R/W	Default	Description
10:0	R/W	0	pre_offset2 : // signed , default = 0

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Table 9-2318 VDIN0_HDR2_MATRIXI_CLIP 0x129A

Bit(s)	R/W	Default	Description
19:8	R/W	0	comp_th : // unsigned , default = 0
7:5	R/W	0	conv_rs : // unsigned , default = 0
4:3	R/W	0	clmod : // unsigned , default = 0

Table 9-2319 VDIN0_HDR2_MATRIXO_CLIP 0x129B

Bit(s)	R/W	Default	Description
19:8	R/W	0	comp_th : // unsigned , default = 0
7:5	R/W	0	conv_rs : // unsigned , default = 0
4:3	R/W	0	clmod : // unsigned , default = 0

Table 9-2320 VDIN0_HDR2_CGAIN_OFFT 0x129C

Bit(s)	R/W	Default	Description
26:16	R/W	0	reg_cgain_oft2 : // signed , default = 0
10:0	R/W	0	reg_cgain_oft1 : // signed , default = 0

Table 9-2321 VDIN0_EOTF_LUT_ADDR_PORT 0x129E

Bit(s)	R/W	Default	Description
7:0	R/W	0	eotf_lut_addr : // unsigned , default = 0

Table 9-2322 VDIN0_EOTF_LUT_DATA_PORT 0x129F

Bit(s)	R/W	Default	Description
19:0	R/W	0	eotf_lut_data : // unsigned , default = 0

Table 9-2323 VDIN0_OETF_LUT_ADDR_PORT 0x12A0

Bit(s)	R/W	Default	Description
7:0	R/W	0	oetf_lut_addr : // unsigned , default = 0

Table 9-2324 VDIN0_OETF_LUT_DATA_PORT 0x12A1

Bit(s)	R/W	Default	Description
11:0	R/W	0	oetf_lut_data : // unsigned , default = 0

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Table 9-2325 VDIN0_CGAIN_LUT_ADDR_PORT 0x12A2

Bit(s)	R/W	Default	Description
7:0	R/W	0	cgain_lut_addr : // unsigned , default = 0

Table 9-2326 VDIN0_CGAIN_LUT_DATA_PORT 0x12A3

Bit(s)	R/W	Default	Description
11:0	R/W	0	cgain_lut_data : // unsigned , default = 0

Table 9-2327 VDIN0_HDR2_CGAIN_COEF0 0x12A4

Bit(s)	R/W	Default	Description
27:16	R/W	0	reg_cgain_coef1 : // unsigned , default = 0
11:0	R/W	0	reg_cgain_coef0 : //unsigned , default = 0

Table 9-2328 VDIN0_HDR2_CGAIN_COEF1 0x12A5

Bit(s)	R/W	Default	Description
11:0	R/W	0	reg_cgain_coef2 : // unsigned , default = 0

Table 9-2329 VDIN0_OGAIN_LUT_ADDR_PORT 0x12A6

Bit(s)	R/W	Default	Description
7:0	R/W	0	ogain_lut_addr : // unsigned , default = 0

Table 9-2330 VDIN0_OGAIN_LUT_DATA_PORT 0x12A7

Bit(s)	R/W	Default	Description
11:0	R/W	0	ogain_lut_data : // unsigned , default = 0

Table 9-2331 VDIN0_HDR2_ADPS_CTRL 0x12A8

Bit(s)	R/W	Default	Description
6	R/W	1	reg_adpscl_bypass2 : // unsigned , default = 1
5	R/W	1	reg_adpscl_bypass1 : // unsigned , default = 1
4	R/W	1	reg_adpscl_bypass0 : // unsigned , default = 1
1:0	R/W	1	reg_adpscl_mode : // unsigned , default = 1

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Table 9-2332 VDIN0_HDR2_ADPS_ALPHA0 0x12A9

Bit(s)	R/W	Default	Description
29:16	R/W	0x1000	reg_adpscl_alpha1 : // unsigned , default = 0x1000
13:0	R/W	0x1000	reg_adpscl_alpha0 : // unsigned , default = 0x1000

Table 9-2333 VDIN0_HDR2_ADPS_ALPHA1 0x12AA

Bit(s)	R/W	Default	Description
27:24	R/W	0xc	reg_adpscl_shift0 : // unsigned , default = 0xc
23:20	R/W	0xc	reg_adpscl_shift1 : // unsigned , default = 0xc
19:16	R/W	0xc	reg_adpscl_shift2 : // unsigned , default = 0xc
13:0	R/W	0x1000	reg_adpscl_alpha2 : // unsigned , default = 0x1000

Table 9-2334 VDIN0_HDR2_ADPS_BETA0 0x12AB

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta0_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta0 : // unsigned , default = 0xfc000

Table 9-2335 VDIN0_HDR2_ADPS_BETA1 0x12AC

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta1_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta1 : // unsigned , default = 0xfc000

Table 9-2336 VDIN0_HDR2_ADPS_BETA2 0x12AD

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta2_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta2 : // unsigned , default = 0xfc000

Table 9-2337 VDIN0_HDR2_ADPS_COEF0 0x12AE

Bit(s)	R/W	Default	Description
27:16	R/W	460	reg_adpscl_ys_coef1 : // unsigned , default = 460
11:0	R/W	1188	reg_adpscl_ys_coef0 : // unsigned , default = 1188

Table 9-2338 VDIN0_HDR2_ADPS_COEF1 0x12AF

Bit(s)	R/W	Default	Description
11:0	R/W	104	reg_adpscl_ys_coef2 : // unsigned , default = 104

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Table 9-2339 VDIN0_HDR2_GMUT_CTRL 0x12B0

Bit(s)	R/W	Default	Description
3:0	R/W	14	reg_gmut_shift : // unsigned , default = 14

Table 9-2340 VDIN0_HDR2_GMUT_COEF0 0x12B1

Bit(s)	R/W	Default	Description
31:16	R/W	674	reg_gmut_coef01 : // unsigned , default = 674
15:0	R/W	1285	reg_gmut_coef00 : // unsigned , default = 1285

Table 9-2341 VDIN0_HDR2_GMUT_COEF1 0x12B2

Bit(s)	R/W	Default	Description
31:16	R/W	142	reg_gmut_coef10 : // unsigned , default = 142
15:0	R/W	89	reg_gmut_coef02 : // unsigned , default = 89

Table 9-2342 VDIN0_HDR2_GMUT_COEF2 0x12B3

Bit(s)	R/W	Default	Description
31:16	R/W	23	reg_gmut_coef12 : // unsigned , default = 23
15:0	R/W	1883	reg_gmut_coef11 : // unsigned , default = 1883

Table 9-2343 VDIN0_HDR2_GMUT_COEF3 0x12B4

Bit(s)	R/W	Default	Description
31:16	R/W	180	reg_gmut_coef21 : // unsigned , default = 180
15:0	R/W	34	reg_gmut_coef20 : // unsigned , default = 34

Table 9-2344 VDIN0_HDR2_GMUT_COEF4 0x12B5

Bit(s)	R/W	Default	Description
15:0	R/W	1834	reg_gmut_coef22 : // unsigned , default = 1834

Table 9-2345 VDIN0_HDR2_PIPE_CTRL1 0x12B6

Bit(s)	R/W	Default	Description
31:24	R/W	4	vblank_num_oetf : // unsigned , default = 4
23:16	R/W	4	hblank_num_oetf : // unsigned , default = 4
15:8	R/W	10	vblank_num_eotf : // unsigned , default = 10
7:0	R/W	10	hblank_num_eotf : // unsigned , default = 10

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Table 9-2346 VDIN0_HDR2_PIPE_CTRL2 0x12B7

Bit(s)	R/W	Default	Description
31:24	R/W	10	vblank_num_cgain : // unsigned , default = 10
23:16	R/W	10	hblank_num_cgain : // unsigned , default = 10
15:8	R/W	11	vblank_num_gmut : // unsigned , default = 11
7:0	R/W	11	hblank_num_gmut : // unsigned , default = 11

Table 9-2347 VDIN0_HDR2_PIPE_CTRL3 0x12B8

Bit(s)	R/W	Default	Description
31:24	R/W	22	vblank_num_adps : // unsigned , default = 22
23:16	R/W	2	hblank_num_adps : // unsigned , default = 2
15:8	R/W	4	vblank_num_uv : // unsigned , default = 4
7:0	R/W	4	hblank_num_uv : // unsigned , default = 4

Table 9-2348 VDIN0_HDR2_PROC_WIN1 0x12B9

Bit(s)	R/W	Default	Description
28:16	R/W	0	proc_win_h_ed : // unsigned , default = 0
12:0	R/W	0	proc_win_h_st : // unsigned , default = 0

Table 9-2349 VDIN0_HDR2_PROC_WIN2 0x12BA

Bit(s)	R/W	Default	Description
31	R/W	0	proc_win_gmut_en : // unsigned , default = 0
30	R/W	0	proc_win_adps_en : // unsigned , default = 0
29	R/W	0	proc_win_cgain_en : // unsigned , default = 0
28:16	R/W	0	proc_win_v_ed : // unsigned , default = 0
12:0	R/W	0	proc_win_v_st : // unsigned , default = 0

Table 9-2350 VDIN0_HDR2_MATRIXI_EN_CTRL 0x12BB

Bit(s)	R/W	Default	Description
5:4	R/W	0	matrix_gclk_ctrl : // unsigned , default = 0
1	R/W	0	enable_sync_sel : // unsigned , default = 0
0	R/W	0	matrix_conv_en : // unsigned , default = 0

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Table 9-2351 VDIN0_HDR2_MATRIXO_EN_CTRL 0x12BC

Bit(s)	R/W	Default	Description
5:4	R/W	0	matrix_gclk_ctrl : // unsigned , default = 0
1	R/W	0	enable_sync_sel : // unsigned , default = 0
0	R/W	0	matrix_conv_en : // unsigned , default = 0

Table 9-2352 VDIN1_HDR2_CTRL 0x1380

Bit(s)	R/W	Default	Description
20:18	R/W	0	reg_din_swap : // unsigned , default = 0
17	R/W	0	reg_out_fmt : // unsigned , default = 0
16	R/W	0	reg_only_mat : // unsigned , default = 0 ,only use input matrix ,work when hdr disable
15	R/W	0	mat_o_en,//output matrix enable ,only work when hdr enable
14	R/W	0	mat_in_en //input matrix enable ,only work when hdr enable
13	R/W	0	reg_VDIN0_HDR2_top_en : // unsigned , default = 0,hdr enable singal
12	R/W	1	reg_cgain_mode : // unsigned , default = 1
7: 6	R/W	1	reg_gmut_mode : // unsigned , default = 1
5	R/W	0	reg_in_shift : // unsigned , default = 0
4	R/W	1	reg_in_fmt : // unsigned , default = 1
3	R/W	1	reg_eo_enable : // unsigned , default = 1
2	R/W	1	reg_oe_enable : // unsigned , default = 1

Table 9-2353 VDIN1_HDR2_CLK_GATE 0x1381

Bit(s)	R/W	Default	Description
31:30	R/W	0	clk_tm : gate clock ctrl (main clock) // unsigned , default = 0
29:28	R/W	0	output : matrix clock gate ctrl// unsigned , default = 0
25:24	R/W	0	input : matrix clock gate ctrl // unsigned , default = 0
23:22	R/W	0	hdr : top cbus clock gate ctrl // unsigned , default = 0
21:20	R/W	0	eotf : cbus clock gate ctrl // unsigned , default = 0
19:18	R/W	0	oetf : cbus clock gate ctrl // unsigned , default = 0
17:16	R/W	0	gamma : mult cbus clock gate ctrl // unsigned , default = 0
15:14	R/W	0	adaptive : cbus scaler clock gate ctrl // unsigned , default = 0
13:12	R/W	0	cgain : cbus clock gate ctrl// unsigned , default = 0
11:10	R/W	0	eotf : clock gate ctrl // unsigned , default = 0
9:8	R/W	0	oetf : clock gate ctrl // unsigned , default = 0
7:6	R/W	0	gamma : mult clock gate ctrl// unsigned , default = 0
5:4	R/W	0	adaptive : scaler clock gate ctrl // unsigned , default = 0

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Bit(s)	R/W	Default	Description
3:2	R/W	0	uv : gain clock gate ctrl // unsigned , default = 0
1:0	R/W	0	cgain : clock gate ctrl // unsigned , default = 0

Table 9-2354 VDIN1_HDR2_MATRIXI_COEF00_01 0x1382

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef00 : // signed , default = 0
12:0	R/W	0	coef01 : // signed , default = 0

Table 9-2355 VDIN1_HDR2_MATRIXI_COEF02_10 0x1383

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef02 : // signed , default = 0
12:0	R/W	0	coef10 : // signed , default = 0

Table 9-2356 VDIN1_HDR2_MATRIXI_COEF11_12 0x1384

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef11 : // signed , default = 0
12:0	R/W	0	coef12 : // signed , default = 0

Table 9-2357 VDIN1_HDR2_MATRIXI_COEF20_21 0x1385

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef20 : // signed , default = 0
12:0	R/W	0	coef21 : // signed , default = 0

Table 9-2358 VDIN1_HDR2_MATRIXI_COEF22 0x1386

Bit(s)	R/W	Default	Description
12:0	R/W	0	coef22 : // signed , default = 0

Table 9-2359 VDIN1_HDR2_MATRIXI_COEF30_31 0x1387

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef13 : // signed , default = 0
12:0	R/W	0	coef14 : // signed , default = 0

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Table 9-2360 VDIN1_HDR2_MATRIXI_COEF32_40 0x1388

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef23 : // signed , default = 0
12:0	R/W	0	coef24 : // signed , default = 0

Table 9-2361 VDIN1_HDR2_MATRIXI_COEF41_42 0x1389

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef15 : // signed , default = 0
12:0	R/W	0	coef25 : // signed , default = 0

Table 9-2362 VDIN1_HDR2_MATRIXI_OFFSET0_1 0x138A

Bit(s)	R/W	Default	Description
26:16	R/W	0	offset0 : // signed , default = 0
10:0	R/W	0	offset1 : // signed , default = 0

Table 9-2363 VDIN1_HDR2_MATRIXI_OFFSET2 0x138B

Bit(s)	R/W	Default	Description
10:0	R/W	0	offset2 : // signed , default = 0

Table 9-2364 VDIN1_HDR2_MATRIXI_PRE_OFFSET0_1 0x138C

Bit(s)	R/W	Default	Description
26:16	R/W	0	pre_offset0 : // signed , default = 0
10:0	R/W	0	pre_offset1 : // signed , default = 0

Table 9-2365 VDIN1_HDR2_MATRIXI_PRE_OFFSET2 0x138D

Bit(s)	R/W	Default	Description
10:0	R/W	0	pre_offset2 : // signed , default = 0

Table 9-2366 VDIN1_HDR2_MATRIXO_COEF00_01 0x138E

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef00 : // signed , default = 0
12:0	R/W	0	coef01 : // signed , default = 0

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Table 9-2367 VDIN1_HDR2_MATRIXO_COEF02_10 0x138F

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef02 : // signed , default = 0
12:0	R/W	0	coef10 : // signed , default = 0

Table 9-2368 VDIN1_HDR2_MATRIXO_COEF11_12 0x1390

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef11 : // signed , default = 0
12:0	R/W	0	coef12 : // signed , default = 0

Table 9-2369 VDIN1_HDR2_MATRIXO_COEF20_21 0x1391

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef20 : // signed , default = 0
12:0	R/W	0	coef21 : // signed , default = 0

Table 9-2370 VDIN1_HDR2_MATRIXO_COEF22 0x1392

Bit(s)	R/W	Default	Description
12:0	R/W	0	coef22 : // signed , default = 0

Table 9-2371 VDIN1_HDR2_MATRIXO_COEF30_31 0x1393

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef13 : // signed , default = 0
12:0	R/W	0	coef14 : // signed , default = 0

Table 9-2372 VDIN1_HDR2_MATRIXO_COEF32_40 0x1394

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef23 : // signed , default = 0
12:0	R/W	0	coef24 : // signed , default = 0

Table 9-2373 VDIN1_HDR2_MATRIXO_COEF41_42 0x1395

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef15 : // signed , default = 0
12:0	R/W	0	coef25 : // signed , default = 0

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Table 9-2374 VDIN1_HDR2_MATRIXO_OFFSET0_1 0x1396

Bit(s)	R/W	Default	Description
26:16	R/W	0	offset0 : // signed , default = 0
10:0	R/W	0	offset1 : // signed , default = 0

Table 9-2375 VDIN1_HDR2_MATRIXO_OFFSET2 0x1397

Bit(s)	R/W	Default	Description
10:0	R/W	0	offset2 : // signed , default = 0

Table 9-2376 VDIN1_HDR2_MATRIXO_PRE_OFFSET0_1 0x1398

Bit(s)	R/W	Default	Description
26:16	R/W	0	pre_offset0 : // signed , default = 0
10:0	R/W	0	pre_offset1 : // signed , default = 0

Table 9-2377 VDIN1_HDR2_MATRIXO_PRE_OFFSET2 0x1399

Bit(s)	R/W	Default	Description
10:0	R/W	0	pre_offset2 : // signed , default = 0

Table 9-2378 VDIN1_HDR2_MATRIXI_CLIP 0x139A

Bit(s)	R/W	Default	Description
19:8	R/W	0	comp_th : // unsigned , default = 0
7:5	R/W	0	conv_rs : // unsigned , default = 0
4:3	R/W	0	clmod : // unsigned , default = 0

Table 9-2379 VDIN1_HDR2_MATRIXO_CLIP 0x139B

Bit(s)	R/W	Default	Description
19:8	R/W	0	comp_th : // unsigned , default = 0
7:5	R/W	0	conv_rs : // unsigned , default = 0
4:3	R/W	0	clmod : // unsigned , default = 0

Table 9-2380 VDIN1_HDR2_CGAIN_OFFT 0x139C

Bit(s)	R/W	Default	Description
26:16	R/W	0	reg_cgain_oft2 : // signed , default = 0
10:0	R/W	0	reg_cgain_oft1 : // signed , default = 0

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Table 9-2381 VDIN1_EOTF_LUT_ADDR_PORT 0x139E

Bit(s)	R/W	Default	Description
7:0	R/W	0	eotf_lut_addr : // unsigned , default = 0

Table 9-2382 VDIN1_EOTF_LUT_DATA_PORT 0x139F

Bit(s)	R/W	Default	Description
19:0	R/W	0	eotf_lut_data : // unsigned , default = 0

Table 9-2383 VDIN1_OETF_LUT_ADDR_PORT 0x13A0

Bit(s)	R/W	Default	Description
7:0	R/W	0	oetf_lut_addr : // unsigned , default = 0

Table 9-2384 VDIN1_OETF_LUT_DATA_PORT 0x13A1

Bit(s)	R/W	Default	Description
11:0	R/W	0	oetf_lut_data : // unsigned , default = 0

Table 9-2385 VDIN1_CGAIN_LUT_ADDR_PORT 0x13A2

Bit(s)	R/W	Default	Description
7:0	R/W	0	cgain_lut_addr : // unsigned , default = 0

Table 9-2386 VDIN1_CGAIN_LUT_DATA_PORT 0x13A3

Bit(s)	R/W	Default	Description
11:0	R/W	0	cgain_lut_data : // unsigned , default = 0

Table 9-2387 VDIN1_HDR2_CGAIN_COEF0 0x13A4

Bit(s)	R/W	Default	Description
27:16	R/W	0	reg_cgain_coef1 : // unsigned , default = 0
11:0	R/W	0	reg_cgain_coef0 : //unsigned , default = 0

Table 9-2388 VDIN1_HDR2_CGAIN_COEF1 0x13A5

Bit(s)	R/W	Default	Description
11:0	R/W	0	reg_cgain_coef2 : // unsigned , default = 0

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Table 9-2389 VDIN1_OGAIN_LUT_ADDR_PORT 0x13A6

Bit(s)	R/W	Default	Description
7:0	R/W	0	ogain_lut_addr : // unsigned , default = 0

Table 9-2390 VDIN1_OGAIN_LUT_DATA_PORT 0x13A7

Bit(s)	R/W	Default	Description
11:0	R/W	0	ogain_lut_data : // unsigned , default = 0

Table 9-2391 VDIN1_HDR2_ADPS_CTRL 0x13A8

Bit(s)	R/W	Default	Description
6	R/W	1	reg_adpscl_bypass2 : // unsigned , default = 1
5	R/W	1	reg_adpscl_bypass1 : // unsigned , default = 1
4	R/W	1	reg_adpscl_bypass0 : // unsigned , default = 1
1:0	R/W	1	reg_adpscl_mode : // unsigned , default = 1

Table 9-2392 VDIN1_HDR2_ADPS_ALPHA0 0x13A9

Bit(s)	R/W	Default	Description
29:16	R/W	0x1000	reg_adpscl_alpha1 : // unsigned , default = 0x1000
13:0	R/W	0x1000	reg_adpscl_alpha0 : // unsigned , default = 0x1000

Table 9-2393 VDIN1_HDR2_ADPS_ALPHA1 0x13AA

Bit(s)	R/W	Default	Description
27:24	R/W	0xc	reg_adpscl_shift0 : // unsigned , default = 0xc
23:20	R/W	0xc	reg_adpscl_shift1 : // unsigned , default = 0xc
19:16	R/W	0xc	reg_adpscl_shift2 : // unsigned , default = 0xc
13:0	R/W	0x1000	reg_adpscl_alpha2 : // unsigned , default = 0x1000

Table 9-2394 VDIN1_HDR2_ADPS_BETA0 0x13AB

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta0_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta0 : // unsigned , default = 0xfc000

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Table 9-2395 VDIN1_HDR2_ADPS_BETA1 0x13AC

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta1_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta1 : // unsigned , default = 0xfc000

Table 9-2396 VDIN1_HDR2_ADPS_BETA2 0x13AD

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta2_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta2 : // unsigned , default = 0xfc000

Table 9-2397 VDIN1_HDR2_ADPS_COEF0 0x13AE

Bit(s)	R/W	Default	Description
27:16	R/W	460	reg_adpscl_ys_coef1 : // unsigned , default = 460
11:0	R/W	1188	reg_adpscl_ys_coef0 : // unsigned , default = 1188

Table 9-2398 VDIN1_HDR2_ADPS_COEF1 0x13AF

Bit(s)	R/W	Default	Description
11:0	R/W	104	reg_adpscl_ys_coef2 : // unsigned , default = 104

Table 9-2399 VDIN1_HDR2_GMUT_CTRL 0x13B0

Bit(s)	R/W	Default	Description
3:0	R/W	14	reg_gmut_shift : // unsigned , default = 14

Table 9-2400 VDIN1_HDR2_GMUT_COEF0 0x13B1

Bit(s)	R/W	Default	Description
31:16	R/W	674	reg_gmut_coef01 : // unsigned , default = 674
15:0	R/W	1285	reg_gmut_coef00 : // unsigned , default = 1285

Table 9-2401 VDIN1_HDR2_GMUT_COEF1 0x13B2

Bit(s)	R/W	Default	Description
31:16	R/W	142	reg_gmut_coef10 : // unsigned , default = 142
15:0	R/W	89	reg_gmut_coef02 : // unsigned , default = 89

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Table 9-2402 VDIN1_HDR2_GMUT_COEF2 0x13B3

Bit(s)	R/W	Default	Description
31:16	R/W	23	reg_gmut_coef12 : // unsigned , default = 23
15:0	R/W	1883	reg_gmut_coef11 : // unsigned , default = 1883

Table 9-2403 VDIN1_HDR2_GMUT_COEF3 0x13B4

Bit(s)	R/W	Default	Description
31:16	R/W	180	reg_gmut_coef21 : // unsigned , default = 180
15:0	R/W	34	reg_gmut_coef20 : // unsigned , default = 34

Table 9-2404 VDIN1_HDR2_GMUT_COEF4 0x13B5

Bit(s)	R/W	Default	Description
15:0	R/W	1834	reg_gmut_coef22 : // unsigned , default = 1834

Table 9-2405 VDIN1_HDR2_PIPE_CTRL1 0x13B6

Bit(s)	R/W	Default	Description
31:24	R/W	4	vblank_num_oetf : // unsigned , default = 4
23:16	R/W	4	hblank_num_oetf : // unsigned , default = 4
15:8	R/W	10	vblank_num_eotf : // unsigned , default = 10
7:0	R/W	10	hblank_num_eotf : // unsigned , default = 10

Table 9-2406 VDIN1_HDR2_PIPE_CTRL2 0x13B7

Bit(s)	R/W	Default	Description
31:24	R/W	10	vblank_num_cgain : // unsigned , default = 10
23:16	R/W	10	hblank_num_cgain : // unsigned , default = 10
15:8	R/W	11	vblank_num_gmut : // unsigned , default = 11
7:0	R/W	11	hblank_num_gmut : // unsigned , default = 11

Table 9-2407 VDIN1_HDR2_PIPE_CTRL3 0x13B8

Bit(s)	R/W	Default	Description
31:24	R/W	22	vblank_num_adps : // unsigned , default = 22
23:16	R/W	2	hblank_num_adps : // unsigned , default = 2
15:8	R/W	4	vblank_num_uv : // unsigned , default = 4
7:0	R/W	4	hblank_num_uv : // unsigned , default = 4

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Table 9-2408 VDIN1_HDR2_PROC_WIN1 0x13B9

Bit(s)	R/W	Default	Description
28:16	R/W	0	proc_win_h_ed : // unsigned , default = 0
12:0	R/W	0	proc_win_h_st : // unsigned , default = 0

Table 9-2409 VDIN1_HDR2_PROC_WIN2 0x13BA

Bit(s)	R/W	Default	Description
31	R/W	0	proc_win_gmut_en : // unsigned , default = 0
30	R/W	0	proc_win_adps_en : // unsigned , default = 0
29	R/W	0	proc_win_cgain_en : // unsigned , default = 0
28:16	R/W	0	proc_win_v_ed : // unsigned , default = 0
12:0	R/W	0	proc_win_v_st : // unsigned , default = 0

Table 9-2410 VDIN1_HDR2_MATRIXI_EN_CTRL 0x13BB

Bit(s)	R/W	Default	Description
5:4	R/W	0	matrix_gclk_ctrl : // unsigned , default = 0
1	R/W	0	enable_sync_sel : // unsigned , default = 0
0	R/W	0	matrix_conv_en : // unsigned , default = 0

Table 9-2411 VDIN1_HDR2_MATRIXO_EN_CTRL 0x13BC

Bit(s)	R/W	Default	Description
5:4	R/W	0	matrix_gclk_ctrl : // unsigned , default = 0
1	R/W	0	enable_sync_sel : // unsigned , default = 0
0	R/W	0	matrix_conv_en : // unsigned , default = 0

Table 9-2412 VD1_HDR2_CTRL 0x3800

Bit(s)	R/W	Default	Description
20:18	R/W	0	reg_din_swap : // unsigned , default = 0
17	R/W	0	reg_out_fmt : // unsigned , default = 0
16	R/W	0	reg_only_mat : // unsigned , default = 0 ,only use input matrix ,work when hdr disable
15	R/W	0	mat_o_en,//output matrix enable ,only work when hdr enable
14	R/W	0	mat_in_en //input matrix enable ,only work when hdr enable
13	R/W	0	reg_VDIN0_HDR2_top_en : // unsigned , default = 0,hdr enable singal
12	R/W	1	reg_cgain_mode : // unsigned , default = 1
7: 6	R/W	1	reg_gmut_mode : // unsigned , default = 1

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Bit(s)	R/W	Default	Description
5	R/W	0	reg_in_shift : // unsigned , default = 0
4	R/W	1	reg_in_fmt : // unsigned , default = 1
3	R/W	1	reg_eo_enable : // unsigned , default = 1
2	R/W	1	reg_oe_enable : // unsigned , default = 1

Table 9-2413 VD1_HDR2_CLK_GATE 0x3801

Bit(s)	R/W	Default	Description
31:30	R/W	0	clk_tm : gate clock ctrl (main clock) // unsigned , default = 0
29:28	R/W	0	output : matrix clock gate ctrl// unsigned , default = 0
25:24	R/W	0	input : matrix clock gate ctrl // unsigned , default = 0
23:22	R/W	0	hdr : top cbus clock gate ctrl // unsigned , default = 0
21:20	R/W	0	eotf : cbus clock gate ctrl // unsigned , default = 0
19:18	R/W	0	oetf : cbus clock gate ctrl // unsigned , default = 0
17:16	R/W	0	gamma : mult cbus clock gate ctrl // unsigned , default = 0
15:14	R/W	0	adaptive : cbus scaler clock gate ctrl // unsigned , default = 0
13:12	R/W	0	cgain : cbus clock gate ctrl// unsigned , default = 0
11:10	R/W	0	eotf : clock gate ctrl // unsigned , default = 0
9:8	R/W	0	oetf : clock gate ctrl // unsigned , default = 0
7:6	R/W	0	gamma : mult clock gate ctrl// unsigned , default = 0
5:4	R/W	0	adaptive : scaler clock gate ctrl // unsigned , default = 0
3:2	R/W	0	uv : gain clock gate ctrl // unsigned , default = 0
1:0	R/W	0	cgain : clock gate ctrl // unsigned , default = 0

Table 9-2414 VD1_HDR2_MATRIXI_COEF00_01 0x3802

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef00 : // signed , default = 0
12:0	R/W	0	coef01 : // signed , default = 0

Table 9-2415 VD1_HDR2_MATRIXI_COEF02_10 0x3803

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef02 : // signed , default = 0
12:0	R/W	0	coef10 : // signed , default = 0

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Table 9-2416 VD1_HDR2_MATRIXI_COEF11_12 0x3804

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef11 : // signed , default = 0
12:0	R/W	0	coef12 : // signed , default = 0

Table 9-2417 VD1_HDR2_MATRIXI_COEF20_21 0x3805

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef20 : // signed , default = 0
12:0	R/W	0	coef21 : // signed , default = 0

Table 9-2418 VD1_HDR2_MATRIXI_COEF22 0x3806

Bit(s)	R/W	Default	Description
12:0	R/W	0	coef22 : // signed , default = 0

Table 9-2419 VD1_HDR2_MATRIXI_COEF30_31 0x3807

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef13 : // signed , default = 0
12:0	R/W	0	coef14 : // signed , default = 0

Table 9-2420 VD1_HDR2_MATRIXI_COEF32_40 0x3808

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef23 : // signed , default = 0
12:0	R/W	0	coef24 : // signed , default = 0

Table 9-2421 VD1_HDR2_MATRIXI_COEF41_42 0x3809

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef15 : // signed , default = 0
12:0	R/W	0	coef25 : // signed , default = 0

Table 9-2422 VD1_HDR2_MATRIXI_OFFSET0_1 0x380A

Bit(s)	R/W	Default	Description
26:16	R/W	0	offset0 : // signed , default = 0
10:0	R/W	0	offset1 : // signed , default = 0

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Table 9-2423 VD1_HDR2_MATRIXI_OFFSET2 0x380B

Bit(s)	R/W	Default	Description
10:0	R/W	0	offset2 : // signed , default = 0

Table 9-2424 VD1_HDR2_MATRIXI_PRE_OFFSET0_1 0x380C

Bit(s)	R/W	Default	Description
26:16	R/W	0	pre_offset0 : // signed , default = 0
10:0	R/W	0	pre_offset1 : // signed , default = 0

Table 9-2425 VD1_HDR2_MATRIXI_PRE_OFFSET2 0x380D

Bit(s)	R/W	Default	Description
10:0	R/W	0	pre_offset2 : // signed , default = 0

Table 9-2426 VD1_HDR2_MATRIXO_COEF00_01 0x380E

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef00 : // signed , default = 0
12:0	R/W	0	coef01 : // signed , default = 0

Table 9-2427 VD1_HDR2_MATRIXO_COEF02_10 0x380F

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef02 : // signed , default = 0
12:0	R/W	0	coef10 : // signed , default = 0

Table 9-2428 VD1_HDR2_MATRIXO_COEF11_12 0x3810

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef11 : // signed , default = 0
12:0	R/W	0	coef12 : // signed , default = 0

Table 9-2429 VD1_HDR2_MATRIXO_COEF20_21 0x3811

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef20 : // signed , default = 0
12:0	R/W	0	coef21 : // signed , default = 0

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Table 9-2430 VD1_HDR2_MATRIXO_COEF22 0x3812

Bit(s)	R/W	Default	Description
12:0	R/W	0	coef22 : // signed , default = 0

Table 9-2431 VD1_HDR2_MATRIXO_COEF30_31 0x3813

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef13 : // signed , default = 0
12:0	R/W	0	coef14 : // signed , default = 0

Table 9-2432 VD1_HDR2_MATRIXO_COEF32_40 0x3814

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef23 : // signed , default = 0
12:0	R/W	0	coef24 : // signed , default = 0

Table 9-2433 VD1_HDR2_MATRIXO_COEF41_42 0x3815

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef15 : // signed , default = 0
12:0	R/W	0	coef25 : // signed , default = 0

Table 9-2434 VD1_HDR2_MATRIXO_OFFSET0_1 0x3816

Bit(s)	R/W	Default	Description
26:16	R/W	0	offset0 : // signed , default = 0
10:0	R/W	0	offset1 : // signed , default = 0

Table 9-2435 VD1_HDR2_MATRIXO_OFFSET2 0x3817

Bit(s)	R/W	Default	Description
10:0	R/W	0	offset2 : // signed , default = 0

Table 9-2436 VD1_HDR2_MATRIXO_PRE_OFFSET0_1 0x3818

Bit(s)	R/W	Default	Description
26:16	R/W	0	pre_offset0 : // signed , default = 0
10:0	R/W	0	pre_offset1 : // signed , default = 0

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Table 9-2437 VD1_HDR2_MATRIXO_PRE_OFFSET2 0x3819

Bit(s)	R/W	Default	Description
10:0	R/W	0	pre_offset2 : // signed , default = 0

Table 9-2438 VD1_HDR2_MATRIXI_CLIP 0x381A

Bit(s)	R/W	Default	Description
19:8	R/W	0	comp_th : // unsigned , default = 0
7:5	R/W	0	conv_rs : // unsigned , default = 0
4:3	R/W	0	clmod : // unsigned , default = 0

Table 9-2439 VD1_HDR2_MATRIXO_CLIP 0x381B

Bit(s)	R/W	Default	Description
19:8	R/W	0	comp_th : // unsigned , default = 0
7:5	R/W	0	conv_rs : // unsigned , default = 0
4:3	R/W	0	clmod : // unsigned , default = 0

Table 9-2440 VD1_HDR2_CGAIN_OFFT 0x381C

Bit(s)	R/W	Default	Description
26:16	R/W	0	reg_cgain_oft2 : // signed , default = 0
10:0	R/W	0	reg_cgain_oft1 : // signed , default = 0

Table 9-2441 VD1_EOTF_LUT_ADDR_PORT 0x381E

Bit(s)	R/W	Default	Description
7:0	R/W	0	eotf_lut_addr : // unsigned , default = 0

Table 9-2442 VD1_EOTF_LUT_DATA_PORT 0x381F

Bit(s)	R/W	Default	Description
19:0	R/W	0	eotf_lut_data : // unsigned , default = 0

Table 9-2443 VD1_OETF_LUT_ADDR_PORT 0x3820

Bit(s)	R/W	Default	Description
7:0	R/W	0	oetf_lut_addr : // unsigned , default = 0

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Table 9-2444 VD1_OETF_LUT_DATA_PORT 0x3821

Bit(s)	R/W	Default	Description
11:0	R/W	0	oetf_lut_data : // unsigned , default = 0

Table 9-2445 VD1_CGAIN_LUT_ADDR_PORT 0x3822

Bit(s)	R/W	Default	Description
7:0	R/W	0	cgain_lut_addr : // unsigned , default = 0

Table 9-2446 VD1_CGAIN_LUT_DATA_PORT 0x3823

Bit(s)	R/W	Default	Description
11:0	R/W	0	cgain_lut_data : // unsigned , default = 0

Table 9-2447 VD1_HDR2_CGAIN_COEF0 0x3824

Bit(s)	R/W	Default	Description
27:16	R/W	0	reg_cgain_coef1 : // unsigned , default = 0
11:0	R/W	0	reg_cgain_coef0 : //unsigned , default = 0

Table 9-2448 VD1_HDR2_CGAIN_COEF1 0x3825

Bit(s)	R/W	Default	Description
11:0	R/W	0	reg_cgain_coef2 : // unsigned , default = 0

Table 9-2449 VD1_OGAIN_LUT_ADDR_PORT 0x3826

Bit(s)	R/W	Default	Description
7:0	R/W	0	ogain_lut_addr : // unsigned , default = 0

Table 9-2450 VD1_OGAIN_LUT_DATA_PORT 0x3827

Bit(s)	R/W	Default	Description
11:0	R/W	0	ogain_lut_data : // unsigned , default = 0

Table 9-2451 VD1_HDR2_ADPS_CTRL 0x3828

Bit(s)	R/W	Default	Description
6	R/W	1	reg_adpscl_bypass2 : // unsigned , default = 1
5	R/W	1	reg_adpscl_bypass1 : // unsigned , default = 1
4	R/W	1	reg_adpscl_bypass0 : // unsigned , default = 1
1:0	R/W	1	reg_adpscl_mode : // unsigned , default = 1

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Table 9-2452 VD1_HDR2_ADPS_ALPHA0 0x3829

Bit(s)	R/W	Default	Description
29:16	R/W	0x1000	reg_adpscl_alpha1 : // unsigned , default = 0x1000
13:0	R/W	0x1000	reg_adpscl_alpha0 : // unsigned , default = 0x1000

Table 9-2453 VD1_HDR2_ADPS_ALPHA1 0x382A

Bit(s)	R/W	Default	Description
27:24	R/W	0xc	reg_adpscl_shift0 : // unsigned , default = 0xc
23:20	R/W	0xc	reg_adpscl_shift1 : // unsigned , default = 0xc
19:16	R/W	0xc	reg_adpscl_shift2 : // unsigned , default = 0xc
13:0	R/W	0x1000	reg_adpscl_alpha2 : // unsigned , default = 0x1000

Table 9-2454 VD1_HDR2_ADPS_BETA0 0x382B

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta0_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta0 : // unsigned , default = 0xfc000

Table 9-2455 VD1_HDR2_ADPS_BETA1 0x382C

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta1_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta1 : // unsigned , default = 0xfc000

Table 9-2456 VD1_HDR2_ADPS_BETA2 0x382D

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta2_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta2 : // unsigned , default = 0xfc000

Table 9-2457 VD1_HDR2_ADPS_COEF0 0x382E

Bit(s)	R/W	Default	Description
27:16	R/W	460	reg_adpscl_ys_coef1 : // unsigned , default = 460
11:0	R/W	1188	reg_adpscl_ys_coef0 : // unsigned , default = 1188

Table 9-2458 VD1_HDR2_ADPS_COEF1 0x382F

Bit(s)	R/W	Default	Description
11:0	R/W	104	reg_adpscl_ys_coef2 : // unsigned , default = 104

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Table 9-2459 VD1_HDR2_GMUT_CTRL 0x3830

Bit(s)	R/W	Default	Description
3:0	R/W	14	reg_gmut_shift : // unsigned , default = 14

Table 9-2460 VD1_HDR2_GMUT_COEF0 0x3831

Bit(s)	R/W	Default	Description
31:16	R/W	674	reg_gmut_coef01 : // unsigned , default = 674
15:0	R/W	1285	reg_gmut_coef00 : // unsigned , default = 1285

Table 9-2461 VD1_HDR2_GMUT_COEF1 0x3832

Bit(s)	R/W	Default	Description
31:16	R/W	142	reg_gmut_coef10 : // unsigned , default = 142
15:0	R/W	89	reg_gmut_coef02 : // unsigned , default = 89

Table 9-2462 VD1_HDR2_GMUT_COEF2 0x3833

Bit(s)	R/W	Default	Description
31:16	R/W	23	reg_gmut_coef12 : // unsigned , default = 23
15:0	R/W	1883	reg_gmut_coef11 : // unsigned , default = 1883

Table 9-2463 VD1_HDR2_GMUT_COEF3 0x3834

Bit(s)	R/W	Default	Description
31:16	R/W	180	reg_gmut_coef21 : // unsigned , default = 180
15:0	R/W	34	reg_gmut_coef20 : // unsigned , default = 34

Table 9-2464 VD1_HDR2_GMUT_COEF4 0x3835

Bit(s)	R/W	Default	Description
15:0	R/W	1834	reg_gmut_coef22 : // unsigned , default = 1834

Table 9-2465 VD1_HDR2_PIPE_CTRL1 0x3836

Bit(s)	R/W	Default	Description
31:24	R/W	4	vblank_num_oetf : // unsigned , default = 4
23:16	R/W	4	hblank_num_oetf : // unsigned , default = 4
15:8	R/W	10	vblank_num_eotf : // unsigned , default = 10
7:0	R/W	10	hblank_num_eotf : // unsigned , default = 10

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Table 9-2466 VD1_HDR2_PIPE_CTRL2 0x3837

Bit(s)	R/W	Default	Description
31:24	R/W	10	vblank_num_cgain : // unsigned , default = 10
23:16	R/W	10	hblank_num_cgain : // unsigned , default = 10
15:8	R/W	11	vblank_num_gmut : // unsigned , default = 11
7:0	R/W	11	hblank_num_gmut : // unsigned , default = 11

Table 9-2467 VD1_HDR2_PIPE_CTRL3 0x3838

Bit(s)	R/W	Default	Description
31:24	R/W	22	vblank_num_adps : // unsigned , default = 22
23:16	R/W	2	hblank_num_adps : // unsigned , default = 2
15:8	R/W	4	vblank_num_uv : // unsigned , default = 4
7:0	R/W	4	hblank_num_uv : // unsigned , default = 4

Table 9-2468 VD1_HDR2_PROC_WIN1 0x3839

Bit(s)	R/W	Default	Description
28:16	R/W	0	proc_win_h_ed : // unsigned , default = 0
12:0	R/W	0	proc_win_h_st : // unsigned , default = 0

Table 9-2469 VD1_HDR2_PROC_WIN2 0x383A

Bit(s)	R/W	Default	Description
31	R/W	0	proc_win_gmut_en : // unsigned , default = 0
30	R/W	0	proc_win_adps_en : // unsigned , default = 0
29	R/W	0	proc_win_cgain_en : // unsigned , default = 0
28:16	R/W	0	proc_win_v_ed : // unsigned , default = 0
12:0	R/W	0	proc_win_v_st : // unsigned , default = 0

Table 9-2470 VD1_HDR2_MATRIXI_EN_CTRL 0x383B

Bit(s)	R/W	Default	Description
5:4	R/W	0	matrix_gclk_ctrl : // unsigned , default = 0
1	R/W	0	enable_sync_sel : // unsigned , default = 0
0	R/W	0	matrix_conv_en : // unsigned , default = 0

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Table 9-2471 VD1_HDR2_MATRIXO_EN_CTRL 0x383C

Bit(s)	R/W	Default	Description
5:4	R/W	0	matrix_gclk_ctrl : // unsigned , default = 0
1	R/W	0	enable_sync_sel : // unsigned , default = 0
0	R/W	0	matrix_conv_en : // unsigned , default = 0

Table 9-2472 VD1_HDR2_HIST_CTRL 0x383D

Bit(s)	R/W	Default	Description
23-16	R/W	0	hist result read index
15-8	R/W	0	gate clock ctrl
5	R/W	0	piecewise mode enable
4	R/W	0	hist window enable
3	R/W	0	data shfit enable
2-0	R/W	0	hist input select 0: e_rgb max 1: e_luma 2/3: e_noliear_sat 4/5: o_before_gamma 6/7 : after_gamma

Table 9-2473 VD1_HDR2_HIST_H_START_END 0x383E

Bit(s)	R/W	Default	Description
28-16	R/W	0	hist h start
12-0	R/W	0	hist h end

Table 9-2474 VD1_HDR2_HIST_V_START_END 0x383F

Bit(s)	R/W	Default	Description
28-16	R/W	0	hist v start
12-0	R/W	0	hist v end

Table 9-2475 VD1_HDR2_HIST_RD 0x3840

Bit(s)	R/W	Default	Description
23-0	R	0	hist 128 bin result

Table 9-2476 VD2_HDR2_CTRL 0x3850

Bit(s)	R/W	Default	Description
20:18	R/W	0	reg_din_swap : // unsigned , default = 0
17	R/W	0	reg_out_fmt : // unsigned , default = 0
16	R/W	0	reg_only_mat : // unsigned , default = 0 ,only use input matrix ,work when hdr disable
15	R/W	0	mat_o_en,//output matrix enable ,only work when hdr enable

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Bit(s)	R/W	Default	Description
14	R/W	0	mat_in_en //input matrix enable ,only work when hdr enable
13	R/W	0	reg_VDIN0_HDR2_top_en : // unsigned , default = 0,hdr enable singal
12	R/W	1	reg_cgain_mode : // unsigned , default = 1
7: 6	R/W	1	reg_gmut_mode : // unsigned , default = 1
5	R/W	0	reg_in_shift : // unsigned , default = 0
4	R/W	1	reg_in_fmt : // unsigned , default = 1
3	R/W	1	reg_eo_enable : // unsigned , default = 1
2	R/W	1	reg_oe_enable : // unsigned , default = 1

Table 9-2477 VD2_HDR2_CLK_GATE 0x3851

Bit(s)	R/W	Default	Description
31:30	R/W	0	clk_tm : gate clock ctrl (main clock) // unsigned , default = 0
29:28	R/W	0	output : matrix clock gate ctrl// unsigned , default = 0
25:24	R/W	0	input : matrix clock gate ctrl // unsigned , default = 0
23:22	R/W	0	hdr : top cbus clock gate ctrl // unsigned , default = 0
21:20	R/W	0	eotf : cbus clock gate ctrl // unsigned , default = 0
19:18	R/W	0	oetf : cbus clock gate ctrl // unsigned , default = 0
17:16	R/W	0	gamma : mult cbus clock gate ctrl // unsigned , default = 0
15:14	R/W	0	adaptive : cbus scaler clock gate ctrl // unsigned , default = 0
13:12	R/W	0	cgain : cbus clock gate ctrl// unsigned , default = 0
11:10	R/W	0	eotf : clock gate ctrl // unsigned , default = 0
9:8	R/W	0	oetf : clock gate ctrl // unsigned , default = 0
7:6	R/W	0	gamma : mult clock gate ctrl// unsigned , default = 0
5:4	R/W	0	adaptive : scaler clock gate ctrl // unsigned , default = 0
3:2	R/W	0	uv : gain clock gate ctrl // unsigned , default = 0
1:0	R/W	0	cgain : clock gate ctrl // unsigned , default = 0

Table 9-2478 VD2_HDR2_MATRIXI_COEF00_01 0x3852

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef00 : // signed , default = 0
12:0	R/W	0	coef01 : // signed , default = 0

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Table 9-2479 VD2_HDR2_MATRIXI_COEF02_10 0x3853

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef02 : // signed , default = 0
12:0	R/W	0	coef10 : // signed , default = 0

Table 9-2480 VD2_HDR2_MATRIXI_COEF11_12 0x3854

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef11 : // signed , default = 0
12:0	R/W	0	coef12 : // signed , default = 0

Table 9-2481 VD2_HDR2_MATRIXI_COEF20_21 0x3855

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef20 : // signed , default = 0
12:0	R/W	0	coef21 : // signed , default = 0

Table 9-2482 VD2_HDR2_MATRIXI_COEF22 0x3856

Bit(s)	R/W	Default	Description
12:0	R/W	0	coef22 : // signed , default = 0

Table 9-2483 VD2_HDR2_MATRIXI_COEF30_31 0x3857

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef13 : // signed , default = 0
12:0	R/W	0	coef14 : // signed , default = 0

Table 9-2484 VD2_HDR2_MATRIXI_COEF32_40 0x3858

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef23 : // signed , default = 0
12:0	R/W	0	coef24 : // signed , default = 0

Table 9-2485 VD2_HDR2_MATRIXI_COEF41_42 0x3859

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef15 : // signed , default = 0
12:0	R/W	0	coef25 : // signed , default = 0

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Table 9-2486 VD2_HDR2_MATRIXI_OFFSET0_1 0x385A

Bit(s)	R/W	Default	Description
26:16	R/W	0	offset0 : // signed , default = 0
10:0	R/W	0	offset1 : // signed , default = 0

Table 9-2487 VD2_HDR2_MATRIXI_OFFSET2 0x385B

Bit(s)	R/W	Default	Description
10:0	R/W	0	offset2 : // signed , default = 0

Table 9-2488 VD2_HDR2_MATRIXI_PRE_OFFSET0_1 0x385C

Bit(s)	R/W	Default	Description
26:16	R/W	0	pre_offset0 : // signed , default = 0
10:0	R/W	0	pre_offset1 : // signed , default = 0

Table 9-2489 VD2_HDR2_MATRIXI_PRE_OFFSET2 0x385D

Bit(s)	R/W	Default	Description
10:0	R/W	0	pre_offset2 : // signed , default = 0

Table 9-2490 VD2_HDR2_MATRIXO_COEF00_01 0x385E

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef00 : // signed , default = 0
12:0	R/W	0	coef01 : // signed , default = 0

Table 9-2491 VD2_HDR2_MATRIXO_COEF02_10 0x385F

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef02 : // signed , default = 0
12:0	R/W	0	coef10 : // signed , default = 0

Table 9-2492 VD2_HDR2_MATRIXO_COEF11_12 0x3860

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef11 : // signed , default = 0
12:0	R/W	0	coef12 : // signed , default = 0

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Table 9-2493 VD2_HDR2_MATRIXO_COEF20_21 0x3861

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef20 : // signed , default = 0
12:0	R/W	0	coef21 : // signed , default = 0

Table 9-2494 VD2_HDR2_MATRIXO_COEF22 0x3862

Bit(s)	R/W	Default	Description
12:0	R/W	0	coef22 : // signed , default = 0

Table 9-2495 VD2_HDR2_MATRIXO_COEF30_31 0x3863

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef13 : // signed , default = 0
12:0	R/W	0	coef14 : // signed , default = 0

Table 9-2496 VD2_HDR2_MATRIXO_COEF32_40 0x3864

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef23 : // signed , default = 0
12:0	R/W	0	coef24 : // signed , default = 0

Table 9-2497 VD2_HDR2_MATRIXO_COEF41_42 0x3865

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef15 : // signed , default = 0
12:0	R/W	0	coef25 : // signed , default = 0

Table 9-2498 VD2_HDR2_MATRIXO_OFFSET0_1 0x3866

Bit(s)	R/W	Default	Description
26:16	R/W	0	offset0 : // signed , default = 0
10:0	R/W	0	offset1 : // signed , default = 0

Table 9-2499 VD2_HDR2_MATRIXO_OFFSET2 0x3867

Bit(s)	R/W	Default	Description
10:0	R/W	0	offset2 : // signed , default = 0

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Table 9-2500 VD2_HDR2_MATRIXO_PRE_OFFSET0_1 0x3868

Bit(s)	R/W	Default	Description
26:16	R/W	0	pre_offset0 : // signed , default = 0
10:0	R/W	0	pre_offset1 : // signed , default = 0

Table 9-2501 VD2_HDR2_MATRIXO_PRE_OFFSET2 0x3869

Bit(s)	R/W	Default	Description
10:0	R/W	0	pre_offset2 : // signed , default = 0

Table 9-2502 VD2_HDR2_MATRIXI_CLIP 0x386A

Bit(s)	R/W	Default	Description
19:8	R/W	0	comp_th : // unsigned , default = 0
7:5	R/W	0	conv_rs : // unsigned , default = 0
4:3	R/W	0	clmod : // unsigned , default = 0

Table 9-2503 VD2_HDR2_MATRIXO_CLIP 0x386B

Bit(s)	R/W	Default	Description
19:8	R/W	0	comp_th : // unsigned , default = 0
7:5	R/W	0	conv_rs : // unsigned , default = 0
4:3	R/W	0	clmod : // unsigned , default = 0

Table 9-2504 VD2_HDR2_CGAIN_OFFT 0x386C

Bit(s)	R/W	Default	Description
26:16	R/W	0	reg_cgain_oft2 : // signed , default = 0
10:0	R/W	0	reg_cgain_oft1 : // signed , default = 0

Table 9-2505 VD2_EOTF_LUT_ADDR_PORT 0x386E

Bit(s)	R/W	Default	Description
7:0	R/W	0	eotf_lut_addr : // unsigned , default = 0

Table 9-2506 VD2_EOTF_LUT_DATA_PORT 0x386F

Bit(s)	R/W	Default	Description
19:0	R/W	0	eotf_lut_data : // unsigned , default = 0

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Table 9-2507 VD2_OETF_LUT_ADDR_PORT 0x3870

Bit(s)	R/W	Default	Description
7:0	R/W	0	oetf_lut_addr : // unsigned , default = 0

Table 9-2508 VD2_OETF_LUT_DATA_PORT 0x3871

Bit(s)	R/W	Default	Description
11:0	R/W	0	oetf_lut_data : // unsigned , default = 0

Table 9-2509 VD2_CGAIN_LUT_ADDR_PORT 0x3872

Bit(s)	R/W	Default	Description
7:0	R/W	0	cgain_lut_addr : // unsigned , default = 0

Table 9-2510 VD2_CGAIN_LUT_DATA_PORT 0x3873

Bit(s)	R/W	Default	Description
11:0	R/W	0	cgain_lut_data : // unsigned , default = 0

Table 9-2511 VD2_HDR2_CGAIN_COEF0 0x3874

Bit(s)	R/W	Default	Description
27:16	R/W	0	reg_cgain_coef1 : // unsigned , default = 0
11:0	R/W	0	reg_cgain_coef0 : //unsigned , default = 0

Table 9-2512 VD2_HDR2_CGAIN_COEF1 0x3875

Bit(s)	R/W	Default	Description
11:0	R/W	0	reg_cgain_coef2 : // unsigned , default = 0

Table 9-2513 VD2_OGAIN_LUT_ADDR_PORT 0x3876

Bit(s)	R/W	Default	Description
7:0	R/W	0	ogain_lut_addr : // unsigned , default = 0

Table 9-2514 VD2_OGAIN_LUT_DATA_PORT 0x3877

Bit(s)	R/W	Default	Description
11:0	R/W	0	ogain_lut_data : // unsigned , default = 0

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Table 9-2515 VD2_HDR2_ADPS_CTRL 0x3878

Bit(s)	R/W	Default	Description
6	R/W	1	reg_adpscl_bypass2 : // unsigned , default = 1
5	R/W	1	reg_adpscl_bypass1 : // unsigned , default = 1
4	R/W	1	reg_adpscl_bypass0 : // unsigned , default = 1
1:0	R/W	1	reg_adpscl_mode : // unsigned , default = 1

Table 9-2516 VD2_HDR2_ADPS_ALPHA0 0x3879

Bit(s)	R/W	Default	Description
29:16	R/W	0x1000	reg_adpscl_alpha1 : // unsigned , default = 0x1000
13:0	R/W	0x1000	reg_adpscl_alpha0 : // unsigned , default = 0x1000

Table 9-2517 VD2_HDR2_ADPS_ALPHA1 0x387A

Bit(s)	R/W	Default	Description
27:24	R/W	0xc	reg_adpscl_shift0 : // unsigned , default = 0xc
23:20	R/W	0xc	reg_adpscl_shift1 : // unsigned , default = 0xc
19:16	R/W	0xc	reg_adpscl_shift2 : // unsigned , default = 0xc
13:0	R/W	0x1000	reg_adpscl_alpha2 : // unsigned , default = 0x1000

Table 9-2518 VD2_HDR2_ADPS_BETA0 0x387B

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta0_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta0 : // unsigned , default = 0xfc000

Table 9-2519 VD2_HDR2_ADPS_BETA1 0x387C

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta1_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta1 : // unsigned , default = 0xfc000

Table 9-2520 VD2_HDR2_ADPS_BETA2 0x387D

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta2_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta2 : // unsigned , default = 0xfc000

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Table 9-2521 VD2_HDR2_ADPS_COEF0 0x387E

Bit(s)	R/W	Default	Description
27:16	R/W	460	reg_adpscl_ys_coef1 : // unsigned , default = 460
11:0	R/W	1188	reg_adpscl_ys_coef0 : // unsigned , default = 1188

Table 9-2522 VD2_HDR2_ADPS_COEF1 0x387F

Bit(s)	R/W	Default	Description
11:0	R/W	104	reg_adpscl_ys_coef2 : // unsigned , default = 104

Table 9-2523 VD2_HDR2_GMUT_CTRL 0x3880

Bit(s)	R/W	Default	Description
3:0	R/W	14	reg_gmut_shift : // unsigned , default = 14

Table 9-2524 VD2_HDR2_GMUT_COEF0 0x3881

Bit(s)	R/W	Default	Description
31:16	R/W	674	reg_gmut_coef01 : // unsigned , default = 674
15:0	R/W	1285	reg_gmut_coef00 : // unsigned , default = 1285

Table 9-2525 VD2_HDR2_GMUT_COEF1 0x3882

Bit(s)	R/W	Default	Description
31:16	R/W	142	reg_gmut_coef10 : // unsigned , default = 142
15:0	R/W	89	reg_gmut_coef02 : // unsigned , default = 89

Table 9-2526 VD2_HDR2_GMUT_COEF2 0x3883

Bit(s)	R/W	Default	Description
31:16	R/W	23	reg_gmut_coef12 : // unsigned , default = 23
15:0	R/W	1883	reg_gmut_coef11 : // unsigned , default = 1883

Table 9-2527 VD2_HDR2_GMUT_COEF3 0x3884

Bit(s)	R/W	Default	Description
31:16	R/W	180	reg_gmut_coef21 : // unsigned , default = 180
15:0	R/W	34	reg_gmut_coef20 : // unsigned , default = 34

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Table 9-2528 VD2_HDR2_GMUT_COEF4 0x3885

Bit(s)	R/W	Default	Description
15:0	R/W	1834	reg_gmut_coef22 : // unsigned , default = 1834

Table 9-2529 VD2_HDR2_PIPE_CTRL1 0x3886

Bit(s)	R/W	Default	Description
31:24	R/W	4	vblank_num_oetf : // unsigned , default = 4
23:16	R/W	4	hblank_num_oetf : // unsigned , default = 4
15:8	R/W	10	vblank_num_eotf : // unsigned , default = 10
7:0	R/W	10	hblank_num_eotf : // unsigned , default = 10

Table 9-2530 VD2_HDR2_PIPE_CTRL2 0x3887

Bit(s)	R/W	Default	Description
31:24	R/W	10	vblank_num_cgain : // unsigned , default = 10
23:16	R/W	10	hblank_num_cgain : // unsigned , default = 10
15:8	R/W	11	vblank_num_gmut : // unsigned , default = 11
7:0	R/W	11	hblank_num_gmut : // unsigned , default = 11

Table 9-2531 VD2_HDR2_PIPE_CTRL3 0x3888

Bit(s)	R/W	Default	Description
31:24	R/W	22	vblank_num_adps : // unsigned , default = 22
23:16	R/W	2	hblank_num_adps : // unsigned , default = 2
15:8	R/W	4	vblank_num_uv : // unsigned , default = 4
7:0	R/W	4	hblank_num_uv : // unsigned , default = 4

Table 9-2532 VD2_HDR2_PROC_WIN1 0x3889

Bit(s)	R/W	Default	Description
28:16	R/W	0	proc_win_h_ed : // unsigned , default = 0
12:0	R/W	0	proc_win_h_st : // unsigned , default = 0

Table 9-2533 VD2_HDR2_PROC_WIN2 0x388A

Bit(s)	R/W	Default	Description
31	R/W	0	proc_win_gmut_en : // unsigned , default = 0
30	R/W	0	proc_win_adps_en : // unsigned , default = 0
29	R/W	0	proc_win_cgain_en : // unsigned , default = 0

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Bit(s)	R/W	Default	Description
28:16	R/W	0	proc_win_v_ed : // unsigned , default = 0
12:0	R/W	0	proc_win_v_st : // unsigned , default = 0

Table 9-2534 VD2_HDR2_MATRIXI_EN_CTRL 0x388B

Bit(s)	R/W	Default	Description
5:4	R/W	0	matrix_gclk_ctrl : // unsigned , default = 0
1	R/W	0	enable_sync_sel : // unsigned , default = 0
0	R/W	0	matrix_conv_en : // unsigned , default = 0

Table 9-2535 VD2_HDR2_MATRIXO_EN_CTRL 0x388C

Bit(s)	R/W	Default	Description
5:4	R/W	0	matrix_gclk_ctrl : // unsigned , default = 0
1	R/W	0	enable_sync_sel : // unsigned , default = 0
0	R/W	0	matrix_conv_en : // unsigned , default = 0

Table 9-2536 OSD1_HDR2_CTRL 0x38A0

Bit(s)	R/W	Default	Description
20:18	R/W	0	reg_din_swap : // unsigned , default = 0
17	R/W	0	reg_out_fmt : // unsigned , default = 0
16	R/W	0	reg_only_mat : // unsigned , default = 0 ,only use input matrix ,work when hdr disable
15	R/W	0	mat_o_en,//output matrix enable ,only work when hdr enable
14	R/W	0	mat_in_en //input matrix enable ,only work when hdr enable
13	R/W	0	reg_VDIN0_HDR2_top_en : // unsigned , default = 0,hdr enable singal
12	R/W	1	reg_cgain_mode : // unsigned , default = 1
7: 6	R/W	1	reg_gmut_mode : // unsigned , default = 1
5	R/W	0	reg_in_shift : // unsigned , default = 0
4	R/W	1	reg_in_fmt : // unsigned , default = 1
3	R/W	1	reg_eo_enable : // unsigned , default = 1
2	R/W	1	reg_oe_enable : // unsigned , default = 1

Table 9-2537 OSD1_HDR2_CLK_GATE 0x38A1

Bit(s)	R/W	Default	Description
31:30	R/W	0	clk_tm : gate clock ctrl (main clock) // unsigned , default = 0
29:28	R/W	0	output : matrix clock gate ctrl// unsigned , default = 0

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Bit(s)	R/W	Default	Description
25:24	R/W	0	input : matrix clock gate ctrl // unsigned , default = 0
23:22	R/W	0	hdr : top cbus clock gate ctrl // unsigned , default = 0
21:20	R/W	0	eotf : cbus clock gate ctrl // unsigned , default = 0
19:18	R/W	0	oetf : cbus clock gate ctrl // unsigned , default = 0
17:16	R/W	0	gamma : mult cbus clock gate ctrl // unsigned , default = 0
15:14	R/W	0	adaptive : cbus scaler clock gate ctrl // unsigned , default = 0
13:12	R/W	0	cgain : cbus clock gate ctrl// unsigned , default = 0
11:10	R/W	0	eotf : clock gate ctrl // unsigned , default = 0
9:8	R/W	0	oetf : clock gate ctrl // unsigned , default = 0
7:6	R/W	0	gamma : mult clock gate ctrl// unsigned , default = 0
5:4	R/W	0	adaptive : scaler clock gate ctrl // unsigned , default = 0
3:2	R/W	0	uv : gain clock gate ctrl // unsigned , default = 0
1:0	R/W	0	cgain : clock gate ctrl // unsigned , default = 0

Table 9-2538 OSD1_HDR2_MATRIXI_COEF00_01 0x38A2

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef00 : // signed , default = 0
12:0	R/W	0	coef01 : // signed , default = 0

Table 9-2539 OSD1_HDR2_MATRIXI_COEF02_10 0x38A3

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef02 : // signed , default = 0
12:0	R/W	0	coef10 : // signed , default = 0

Table 9-2540 OSD1_HDR2_MATRIXI_COEF11_12 0x38A4

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef11 : // signed , default = 0
12:0	R/W	0	coef12 : // signed , default = 0

Table 9-2541 OSD1_HDR2_MATRIXI_COEF20_21 0x38A5

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef20 : // signed , default = 0
12:0	R/W	0	coef21 : // signed , default = 0

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Table 9-2542 OSD1_HDR2_MATRIXI_COEF22 0x38A6

Bit(s)	R/W	Default	Description
12:0	R/W	0	coef22 : // signed , default = 0

Table 9-2543 OSD1_HDR2_MATRIXI_COEF30_31 0x38A7

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef13 : // signed , default = 0
12:0	R/W	0	coef14 : // signed , default = 0

Table 9-2544 OSD1_HDR2_MATRIXI_COEF32_40 0x38A8

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef23 : // signed , default = 0
12:0	R/W	0	coef24 : // signed , default = 0

Table 9-2545 OSD1_HDR2_MATRIXI_COEF41_42 0x38A9

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef15 : // signed , default = 0
12:0	R/W	0	coef25 : // signed , default = 0

Table 9-2546 OSD1_HDR2_MATRIXI_OFFSET0_1 0x38AA

Bit(s)	R/W	Default	Description
26:16	R/W	0	offset0 : // signed , default = 0
10:0	R/W	0	offset1 : // signed , default = 0

Table 9-2547 OSD1_HDR2_MATRIXI_OFFSET2 0x38AB

Bit(s)	R/W	Default	Description
10:0	R/W	0	offset2 : // signed , default = 0

Table 9-2548 OSD1_HDR2_MATRIXI_PRE_OFFSET0_1 0x38AC

Bit(s)	R/W	Default	Description
26:16	R/W	0	pre_offset0 : // signed , default = 0
10:0	R/W	0	pre_offset1 : // signed , default = 0

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Table 9-2549 OSD1_HDR2_MATRIXI_PRE_OFFSET2 0x38AD

Bit(s)	R/W	Default	Description
10:0	R/W	0	pre_offset2 : // signed , default = 0

Table 9-2550 OSD1_HDR2_MATRIXO_COEF00_01 0x38AE

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef00 : // signed , default = 0
12:0	R/W	0	coef01 : // signed , default = 0

Table 9-2551 OSD1_HDR2_MATRIXO_COEF02_10 0x38AF

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef02 : // signed , default = 0
12:0	R/W	0	coef10 : // signed , default = 0

Table 9-2552 OSD1_HDR2_MATRIXO_COEF11_12 0x38B0

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef11 : // signed , default = 0
12:0	R/W	0	coef12 : // signed , default = 0

Table 9-2553 OSD1_HDR2_MATRIXO_COEF20_21 0x38B1

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef20 : // signed , default = 0
12:0	R/W	0	coef21 : // signed , default = 0

Table 9-2554 OSD1_HDR2_MATRIXO_COEF22 0x38B2

Bit(s)	R/W	Default	Description
12:0	R/W	0	coef22 : // signed , default = 0

Table 9-2555 OSD1_HDR2_MATRIXO_COEF30_31 0x38B3

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef13 : // signed , default = 0
12:0	R/W	0	coef14 : // signed , default = 0

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Table 9-2556 OSD1_HDR2_MATRIXO_COEF32_40 0x38B4

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef23 : // signed , default = 0
12:0	R/W	0	coef24 : // signed , default = 0

Table 9-2557 OSD1_HDR2_MATRIXO_COEF41_42 0x38B5

Bit(s)	R/W	Default	Description
28:16	R/W	0	coef15 : // signed , default = 0
12:0	R/W	0	coef25 : // signed , default = 0

Table 9-2558 OSD1_HDR2_MATRIXO_OFFSET0_1 0x38B6

Bit(s)	R/W	Default	Description
26:16	R/W	0	offset0 : // signed , default = 0
10:0	R/W	0	offset1 : // signed , default = 0

Table 9-2559 OSD1_HDR2_MATRIXO_OFFSET2 0x38B7

Bit(s)	R/W	Default	Description
10:0	R/W	0	offset2 : // signed , default = 0

Table 9-2560 OSD1_HDR2_MATRIXO_PRE_OFFSET0_1 0x38B8

Bit(s)	R/W	Default	Description
26:16	R/W	0	pre_offset0 : // signed , default = 0
10:0	R/W	0	pre_offset1 : // signed , default = 0

Table 9-2561 OSD1_HDR2_MATRIXO_PRE_OFFSET2 0x38B9

Bit(s)	R/W	Default	Description
10:0	R/W	0	pre_offset2 : // signed , default = 0

Table 9-2562 OSD1_HDR2_MATRIXI_CLIP 0x38BA

Bit(s)	R/W	Default	Description
19:8	R/W	0	comp_th : // unsigned , default = 0
7:5	R/W	0	conv_rs : // unsigned , default = 0
4:3	R/W	0	clmod : // unsigned , default = 0

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Table 9-2563 OSD1_HDR2_MATRIXO_CLIP 0x38BB

Bit(s)	R/W	Default	Description
19:8	R/W	0	comp_th : // unsigned , default = 0
7:5	R/W	0	conv_rs : // unsigned , default = 0
4:3	R/W	0	clmod : // unsigned , default = 0

Table 9-2564 OSD1_HDR2_CGAIN_OFFT 0x38BC

Bit(s)	R/W	Default	Description
26:16	R/W	0	reg_cgain_oft2 : // signed , default = 0
10:0	R/W	0	reg_cgain_oft1 : // signed , default = 0

Table 9-2565 OSD1_EOTF_LUT_ADDR_PORT 0x38be

Bit(s)	R/W	Default	Description
7:0	R/W	0	eotf_lut_addr : // unsigned , default = 0

Table 9-2566 OSD1_EOTF_LUT_DATA_PORT 0x38bf

Bit(s)	R/W	Default	Description
19:0	R/W	0	eotf_lut_data : // unsigned , default = 0

Table 9-2567 OSD1_OETF_LUT_ADDR_PORT 0x38c0

Bit(s)	R/W	Default	Description
7:0	R/W	0	oetf_lut_addr : // unsigned , default = 0

Table 9-2568 OSD1_OETF_LUT_DATA_PORT 0x38c1

Bit(s)	R/W	Default	Description
11:0	R/W	0	oetf_lut_data : // unsigned , default = 0

Table 9-2569 OSD1_CGAIN_LUT_ADDR_PORT 0x38c2

Bit(s)	R/W	Default	Description
7:0	R/W	0	cgain_lut_addr : // unsigned , default = 0

Table 9-2570 OSD1_CGAIN_LUT_DATA_PORT 0x38c3

Bit(s)	R/W	Default	Description
11:0	R/W	0	cgain_lut_data : // unsigned , default = 0

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Table 9-2571 OSD1_HDR2_CGAIN_COEF0 0x38c4

Bit(s)	R/W	Default	Description
27:16	R/W	0	reg_cgain_coef1 : // unsigned , default = 0
11:0	R/W	0	reg_cgain_coef0 : //unsigned , default = 0

Table 9-2572 OSD1_HDR2_CGAIN_COEF1 0x38c5

Bit(s)	R/W	Default	Description
11:0	R/W	0	reg_cgain_coef2 : // unsigned , default = 0

Table 9-2573 OSD1_OGAIN_LUT_ADDR_PORT 0x38c6

Bit(s)	R/W	Default	Description
7:0	R/W	0	ogain_lut_addr : // unsigned , default = 0

Table 9-2574 OSD1_OGAIN_LUT_DATA_PORT 0x38c7

Bit(s)	R/W	Default	Description
11:0	R/W	0	ogain_lut_data : // unsigned , default = 0

Table 9-2575 OSD1_HDR2_ADPS_CTRL 0x38c8

Bit(s)	R/W	Default	Description
6	R/W	1	reg_adpscl_bypass2 : // unsigned , default = 1
5	R/W	1	reg_adpscl_bypass1 : // unsigned , default = 1
4	R/W	1	reg_adpscl_bypass0 : // unsigned , default = 1
1:0	R/W	1	reg_adpscl_mode : // unsigned , default = 1

Table 9-2576 OSD1_HDR2_ADPS_ALPHA0 0x38c9

Bit(s)	R/W	Default	Description
29:16	R/W	0x1000	reg_adpscl_alpha1 : // unsigned , default = 0x1000
13:0	R/W	0x1000	reg_adpscl_alpha0 : // unsigned , default = 0x1000

Table 9-2577 OSD1_HDR2_ADPS_ALPHA1 0x38ca

Bit(s)	R/W	Default	Description
27:24	R/W	0xc	reg_adpscl_shift0 : // unsigned , default = 0xc
23:20	R/W	0xc	reg_adpscl_shift1 : // unsigned , default = 0xc
19:16	R/W	0xc	reg_adpscl_shift2 : // unsigned , default = 0xc
13:0	R/W	0x1000	reg_adpscl_alpha2 : // unsigned , default = 0x1000

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Table 9-2578 OSD1_HDR2_ADPS_BETA0 0x38cb

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta0_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta0 : // unsigned , default = 0xfc000

Table 9-2579 OSD1_HDR2_ADPS_BETA1 0x38cc

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta1_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta1 : // unsigned , default = 0xfc000

Table 9-2580 OSD1_HDR2_ADPS_BETA2 0x38cd

Bit(s)	R/W	Default	Description
20	R/W	0	reg_adpscl_beta2_s : // unsigned , default = 0
19:0	R/W	0xfc000	reg_adpscl_beta2 : // unsigned , default = 0xfc000

Table 9-2581 OSD1_HDR2_ADPS_COEF0 0x38ce

Bit(s)	R/W	Default	Description
27:16	R/W	460	reg_adpscl_ys_coef1 : // unsigned , default = 460
11:0	R/W	1188	reg_adpscl_ys_coef0 : // unsigned , default = 1188

Table 9-2582 OSD1_HDR2_ADPS_COEF1 0x38cf

Bit(s)	R/W	Default	Description
11:0	R/W	104	reg_adpscl_ys_coef2 : // unsigned , default = 104

Table 9-2583 OSD1_HDR2_GMUT_CTRL 0x38d0

Bit(s)	R/W	Default	Description
3:0	R/W	14	reg_gmut_shift : // unsigned , default = 14

Table 9-2584 OSD1_HDR2_GMUT_COEF0 0x38d1

Bit(s)	R/W	Default	Description
31:16	R/W	674	reg_gmut_coef01 : // unsigned , default = 674
15:0	R/W	1285	reg_gmut_coef00 : // unsigned , default = 1285

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Table 9-2585 OSD1_HDR2_GMUT_COEF1 0x38d2

Bit(s)	R/W	Default	Description
31:16	R/W	142	reg_gmut_coef10 : // unsigned , default = 142
15:0	R/W	89	reg_gmut_coef02 : // unsigned , default = 89

Table 9-2586 OSD1_HDR2_GMUT_COEF2 0x38d3

Bit(s)	R/W	Default	Description
31:16	R/W	23	reg_gmut_coef12 : // unsigned , default = 23
15:0	R/W	1883	reg_gmut_coef11 : // unsigned , default = 1883

Table 9-2587 OSD1_HDR2_GMUT_COEF3 0x38d4

Bit(s)	R/W	Default	Description
31:16	R/W	180	reg_gmut_coef21 : // unsigned , default = 180
15:0	R/W	34	reg_gmut_coef20 : // unsigned , default = 34

Table 9-2588 OSD1_HDR2_GMUT_COEF4 0x38d5

Bit(s)	R/W	Default	Description
15:0	R/W	1834	reg_gmut_coef22 : // unsigned , default = 1834

Table 9-2589 OSD1_HDR2_PIPE_CTRL1 0x38d6

Bit(s)	R/W	Default	Description
31:24	R/W	4	vblank_num_oetf : // unsigned , default = 4
23:16	R/W	4	hblank_num_oetf : // unsigned , default = 4
15:8	R/W	10	vblank_num_eotf : // unsigned , default = 10
7:0	R/W	10	hblank_num_eotf : // unsigned , default = 10

Table 9-2590 OSD1_HDR2_PIPE_CTRL2 0x38d7

Bit(s)	R/W	Default	Description
31:24	R/W	10	vblank_num_cgain : // unsigned , default = 10
23:16	R/W	10	hblank_num_cgain : // unsigned , default = 10
15:8	R/W	11	vblank_num_gmut : // unsigned , default = 11
7:0	R/W	11	hblank_num_gmut : // unsigned , default = 11

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Table 9-2591 OSD1_HDR2_PIPE_CTRL3 0x38d8

Bit(s)	R/W	Default	Description
31:24	R/W	22	vblank_num_adps : // unsigned , default = 22
23:16	R/W	2	hblank_num_adps : // unsigned , default = 2
15:8	R/W	4	vblank_num_uv : // unsigned , default = 4
7:0	R/W	4	hblank_num_uv : // unsigned , default = 4

Table 9-2592 OSD1_HDR2_PROC_WIN1 0x38d9

Bit(s)	R/W	Default	Description
28:16	R/W	0	proc_win_h_ed : // unsigned , default = 0
12:0	R/W	0	proc_win_h_st : // unsigned , default = 0

Table 9-2593 OSD1_HDR2_PROC_WIN2 0x38da

Bit(s)	R/W	Default	Description
31	R/W	0	proc_win_gmut_en : // unsigned , default = 0
30	R/W	0	proc_win_adps_en : // unsigned , default = 0
29	R/W	0	proc_win_cgain_en : // unsigned , default = 0
28:16	R/W	0	proc_win_v_ed : // unsigned , default = 0
12:0	R/W	0	proc_win_v_st : // unsigned , default = 0

Table 9-2594 OSD1_HDR2_MATRIXI_EN_CTRL 0x38db

Bit(s)	R/W	Default	Description
5:4	R/W	0	matrix_gclk_ctrl : // unsigned , default = 0
1	R/W	0	enable_sync_sel : // unsigned , default = 0
0	R/W	0	matrix_conv_en : // unsigned , default = 0

Table 9-2595 OSD1_HDR2_MATRIXO_EN_CTRL 0x38dc

Bit(s)	R/W	Default	Description
5:4	R/W	0	matrix_gclk_ctrl : // unsigned , default = 0
1	R/W	0	enable_sync_sel : // unsigned , default = 0
0	R/W	0	matrix_conv_en : // unsigned , default = 0

Table 9-2596 OSD1_HDR2_HIST_H_START_END 0x38dd

Bit(s)	R/W	Default	Description
28-16	R/W	0	hist h start
12-0	R/W	0	hist h end

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Table 9-2597 OSD1_HDR2_HIST_V_START_END 0x38de

Bit(s)	R/W	Default	Description
28-16	R/W	0	hist v start
12-0	R/W	0	hist v end

Table 9-2598 OSD1_HDR2_HIST_V_START_END 0x38df

Bit(s)	R/W	Default	Description
28-16	R/W	0	hist v start
12-0	R/W	0	hist v end

Table 9-2599 OSD1_HDR2_HIST_RD 0x38e0

Bit(s)	R/W	Default	Description
23-0	R	0	hist 128 bin result

9.2.3.45 VDIN Registers

Table 9-2600 VDIN_TOP_DOUBLE_CTRL 0x410b

Bit(s)	R/W	Default	Description
26-24	R/W	5	Vdin1_interrupt mask
22-20	R/W	5	Vdin0_interrupt mask
19-16	R/W	0x0	Done flag clear
15-0	R/W	0x310	Vdin reorder sel :

Table 9-2601 VDIN_TOP_MISC 0x410d

Bit(s)	R/W	Default	Description
31-26	R/W	0	Sw_reset
18-16	R/W	3	Vdin0_wr_out_ctrl
15	R/W	0	Vdin line int sel: 1:vdin1 line int 0:vdin0 line int
14	R/W	0	Vid2 irq_sel : 1:afbce frm end 0:vid2 write mif done
13-12	R/W	0	Vdin2 fix disable
11-10	R/W	0	Vdin1_fix_disable
9-8	R/W	0	Vdin0_fix_disable
7-4	R/W	0	Vdin arb gclk ctrl
3-2	R/W	0	Afbce gclk ctrl

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Bit(s)	R/W	Default	Description
1	R/W	0	Afbce path sel: 0:vdin 1:di
0	R/W	0	Ldim stts path sel : 0:vdin0 1:vdin1

VDIN0_SCALE_COEF_IDX 0x1200

VDIN0_SCALE_COEF 0x1201

Table 9-2602 VDIN0_COM_CTRL0 0x1202

Bit(s)	R/W	Default	Description
31	R/W	0	mpeg_to_vdin_sel, 0: mpeg source to NR directly, 1: mpeg source pass through here
30	R/W	0	mpeg_field info which can be written by software
29	R/W	0	force go_field, pulse signal
28	R/W	0	force go_line, pulse signal
27	R/W	0	enable mpeg_go_field input signal
26-20	R/W	0	hold lines
19	R/W	0	delay go_field function enable
18-12	R/W	0	delay go_field line number
11-10	R/W	0	component2 output switch, 00: select component0 in, 01: select component1 in, 10: select component2 in
9-8	R/W	0	component1 output switch, 00: select component0 in, 01: select component1 in, 10: select component2 in
7-6	R/W	0	component0 output switch, 00: select component0 in, 01: select component1 in, 10: select component2 in
5	R/W	0	input window selection function enable
4	R/W	0	enable VDIN common data input, otherwise there will be no video data input
3-0	R/W	0	vdin selection, 1: mpeg_in from dram; 2: bt656 input; 3: Reserved (component input); 4: Reserved(tvdecoder input); 5: Reserved(hdmi rx input); 6: reserved(digital video input); 7: Wr_back 0; 8: reserved(MIPI CSI2) ; 9: Wr_back 1; 10: Reserved(second bt656 input); otherwise no input.

Table 9-2603 VDIN0_ACTIVE_MAX_PIX_CNT_STATUS 0x1203

Bit(s)	R/W	Default	Description
28-16	R	0	active_max_pix_cnt, readonly
12-0	R	0	active_max_pix_cnt_shadow, readonly

Table 9-2604 VDIN0_LCNT_STATUS 0x1204

Bit(s)	R/W	Default	Description
28-16	R	0	go_line_cnt, readonly
12-0	R	0	active_line_cnt, readonly

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Table 9-2605 VDIN0_COM_STATUS0 0x1205

Bit(s)	R/W	Default	Description
17	R	0	Vid_wr_pending_ddr_wrrsp
16	R	0	Curr_pic_sec
15	R	0	Curr_pic_sec_sav
14-3	R	0	lfifo_buf_cnt
2	R	0	vdin_direct_done status
1	R	0	vdin_nr_done status
0	R	0	field

Table 9-2606 VDIN0_COM_STATUS1 0x1206

Bit(s)	R/W	Default	Description
31	R	0	vdi4 fifo overflow
29-24	R	0	vdi3_asfifo_cnt
23	R	0	vdi3 fifo overflow
21-16	R	0	vdi3_asfifo_cnt
15	R	0	vdi2 fifo overflow
13-8	R	0	vdi2_asfifo_cnt
7	R	0	vdi1 fifo overflow
5-0	R	0	vdi1_asfifo_cnt

Table 9-2607 VDIN0_LCNT_SHADOW_STATUS 0x1207

Bit(s)	R/W	Default	Description
28-16	R	0	go_line_cnt_shadow, readonly
12-0	R	0	active_line_cnt_shadow, readonly

Table 9-2608 VDIN0_ASFIFO_CTRL0 0x1208

Bit(s)	R/W	Default	Description
31	R/W	0	hv size select 0: write mif size 1:vdin hsc input size
30-28	R/W	0	v de start line number
27-20	R/W	0	v blank
19-12	R/W	0	h blank
10-9	R/W	0	bist pattern 0:horizontal gray scale 1: vertical gray scale 2/3:random data
8	R/W	0	Vdin bist enable : replace vdi6 (loop back path)
7	R/W	0	Vdi1 DE enable
6	R/W	0	Vdi1 go field enable
5	R/W	0	Vdi1 go line enable

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Bit(s)	R/W	Default	Description
4	R/W	0	Vdi1 if true, negative active input vsync
3	R/W	0	Vdi1 if true, negative active input hsync
2	R/W	0	Vdi1 vsync soft reset fifo enable
1	R/W	0	Vdi1 overflow status clear
0	R/W	0	Vdi1 asfifo soft reset, level signal

Table 9-2609 VDIN0_ASFIFO_CTRL1 0x1209

Bit(s)	R/W	Default	Description
23	R/W	0	Vdi4 DE enable
22	R/W	0	Vdi4 go field enable
21	R/W	0	Vdi4 go line enable
20	R/W	0	Vdi4 if true, negative active input vsync
19	R/W	0	Vdi4 if true, negative active input hsync
18	R/W	0	Vdi4 vsync soft reset fifo enable
17	R/W	0	Vdi4 overflow status clear
16	R/W	0	Vdi4 asfifo soft reset, level signal
7	R/W	0	Vdi3 DE enable
6	R/W	0	Vdi3 go field enable
5	R/W	0	Vdi3 go line enable
4	R/W	0	Vdi3 if true, negative active input vsync
3	R/W	0	Vdi3 if true, negative active input hsync
2	R/W	0	Vdi3 vsync soft reset fifo enable
1	R/W	0	Vdi3 overflow status clear
0	R/W	0	Vdi3 asfifo soft reset, level signal

Table 9-2610 VDIN0_WIDTHM1I_WIDTHM1O 0x120a

Bit(s)	R/W	Default	Description
28-16	R/W	0	input width minus 1, after the window function
12-0	R/W	0	output width minus 1

Table 9-2611 VDIN0_SC_MISC_CTRL 0x120b

Bit(s)	R/W	Default	Description
14-8	R/W	0	hsc_ini_pixi_ptr, signed data, only useful when short_lineo_en is true
7	R/W	0	prehsc_en
6	R/W	0	hsc_en

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Bit(s)	R/W	Default	Description
5	R/W	0	hsc_short_lineo_en, short line output enable
4	R/W	0	hsc_nearest_en
3	R/W	0	Hsc_phase0_always_en
2-0	R/W	0	hsc_bank_length

Table 9-2612 VDIN0_HSC_PHASE_STEP 0x120c

Bit(s)	R/W	Default	Description
28-24	R/W	0	integer portion
23-0	R/W	0	fraction portion

Table 9-2613 VDIN0_HSC_INI_CTRL 0x120d

Bit(s)	R/W	Default	Description
30-29	R/W	0	hscale rpt_p0_num
28-24	R/W	0	hscale ini_rcv_num
23-0	R/W	0	hscale ini_phase

Table 9-2614 VDIN0_COM_STATUS2 0x120e

Bit(s)	R/W	Default	Description
23	R	0	Vdi7 fifo overflow
21-16	R	0	Vdi7_asfifo_cnt
15	R	0	Vdi6 fifo overflow
13-8	R	0	Vdi6_asfifo_cnt
7	R	0	vdi5 fifo overflow
5-0	R	0	vdi5_asfifo_cnt

Table 9-2615 VDIN0_ASFIFO_CTRL2 0x120f

Bit(s)	R/W	Default	Description
25	R/W	0	if true, decimation counter sync with first valid DE in the field, //otherwise the decimation counter is not sync with external signal
24	R/W	0	decimation de enable
23-20	R/W	0	decimation phase, which counter value use to decimate,
19-16	R/W	0	decimation number, 0: not decimation, 1: decimation 2, 2: decimation 3 ....
7	R/W	0	Vdi5 DE enable
6	R/W	0	Vdi5 go field enable
5	R/W	0	Vdi5 go line enable
4	R/W	0	Vdi5 if true, negative active input vsync

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Bit(s)	R/W	Default	Description
3	R/W	0	Vdi5 if true, negative active input hsync
2	R/W	0	Vdi5 vsync soft reset fifo enable
1	R/W	0	Vdi5 overflow status clear
0	R/W	0	Vdi5 asfifo soft reset, level signal

Table 9-2616 VDIN0_MATRIX_CTRL 0x1210

Bit(s)	R/W	Default	Description
7	R/W	0	highlight_enable
6	R/W	0	probe_post, if true, probe pixel data after matrix, otherwise probe pixel data before matrix
5-4	R/W	0	probe_sel, 00: select matrix 0, 01: select matrix 1, otherwise select nothing
3-2	R/W	0	matrix coef idx selection, 00: select mat0, 01: select mat1, otherwise slect nothing
1	R/W	0	mat1 conversion matrix enable
0	R/W	0	Mat0 conversion matrix enable

Table 9-2617 VDIN0_MATRIX_COEF00_01 0x1211

Bit(s)	R/W	Default	Description
28-16	R/W	0	coef00
12-0	R/W	0	coef01

Table 9-2618 VDIN0_MATRIX_COEF02_10 0x1212

Bit(s)	R/W	Default	Description
28-16	R/W	0	coef02
12-0	R/W	0	Coef10

Table 9-2619 VDIN0_MATRIX_COEF11_12 0x1213

Bit(s)	R/W	Default	Description
28-16	R/W	0	Coef11
12-0	R/W	0	Coef12

Table 9-2620 VDIN0_MATRIX_COEF20_21 0x1214

Bit(s)	R/W	Default	Description
28-16	R/W	0	Coef20
12-0	R/W	0	coef21

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Table 9-2621 VDIN0_MATRIX_COEF22 0x1215

Bit(s)	R/W	Default	Description
18-16	R/W	0	convrs
7-0	R/W	0	Coef22

Table 9-2622 VDIN0_MATRIX_OFFSET0_1 0x1216

Bit(s)	R/W	Default	Description
26-16	R/W	0	offset0
10-0	R/W	0	Offset1

Table 9-2623 VDIN0_MATRIX_OFFSET2 0x1217

Bit(s)	R/W	Default	Description
10-0	R/W	0	Offset2

Table 9-2624 VDIN0_MATRIX_PRE_OFFSET0_1 0x1218

Bit(s)	R/W	Default	Description
26-16	R/W	0	Pre_offset0
10-0	R/W	0	Pre_Offset1

Table 9-2625 VDIN0_MATRIX_PRE_OFFSET2 0x1219

Bit(s)	R/W	Default	Description
10-0	R/W	0	Pre_Offset2

Table 9-2626 VDIN0_LFIFO_CTRL 0x121a

Bit(s)	R/W	Default	Description
11-0	R/W	0	lfifo_buf_size

Table 9-2627 VDIN0_LFIFO_CTRL 0x121a

Bit(s)	R/W	Default	Description
31	R/W	1	Linebuffer soft reset enable
30	R/W	1	Frame reset enable
28	R/W	0	Discard data enable
18	R/W	0	Vdin channel1 output enable
17	R/W	1	Vdin channel0 output enable
16	R/W	0	Pps_path_sel : 0: pps before linebuffer 1:pps after linebuffer
13-0	R/W	0x1000	lfifo_buf_size

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Table 9-2628 VDIN0_COM_GCLK_CTRL 0x121b

Bit(s)	R/W	Default	Description
15-14	R/W	0	Gate clock control for blackbar detector
13-12	R/W	0	Gate clock control for hist
11-10	R/W	0	Gate clock control for line fifo
9-8	R/W	0	Gate clock control for matrix
7-6	R/W	0	Gate clock control for horizontal scaler
5-4	R/W	0	Gate clock control for pre scaler
3-2	R/W	0	Gate clock control for vdin_com_proc
1-0	R/W	0	Gate clock control for the vdin reg

Table 9-2629 VDIN0_INTF_WIDTHM1 0x121c

Bit(s)	R/W	Default	Description
26	R/W	0	VDIN write mif bvalid_sel: 1. Bvalid_singnal from bus, 0: bytes_wr handshakes
25	R/W	0	VDIN write mif burst last sel: 1. All kind of burst last signal include ext_data_last. 0. Used the normal burst last signal
12-0	R/W	0	VDIN input interface width minus 1, before the window function, after the de decimation

Table 9-2630 VDIN0_WR_CTRL2 0x121f

Bit(s)	R/W	Default	Description
19	R/W	0	Vdin0 wr bit10 mode
18	R/W	0	Data_ext_en 1: send out data if req was interrupt by soft reset 0 : normal mode
17:16	R/W	1	Words lim[1:0] : it would not send out request before Words_lim *16 words were ready
15:12	R/W	1	Burst_ lim : 00 , 1 word in 1burst , 01 ,2 words in 1burst, 10, 4 words in 1burst , 11 reserved
10:9	R/W	0	Words_lim[3:2]
8	R/W	0	1: discard data before line fifo, 0: normal mode
7-0	R/W	0	Write chroma canvas address, for NV12/21 mode.

Table 9-2631 VDIN0_WR_CTRL 0x1220

Bit(s)	R/W	Default	Description
31:30	R/W	0	vdin0_wr_mif_hconv_mode. Applicable only to vdin_write_format=0 or 2. 0=Output every even pixel's CbCr; 1=Output every odd pixel's CbCr; 2=Output an average value per even&odd pair of pixels; 3=Output all CbCr. Only applys to vdin_write_format =2.
29	R/W	0	vdin0_wr_mif_no_clk_gate. If true, enable free-run clock.

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Bit(s)	R/W	Default	Description
28	R/W	0	clear write response counter in the vdin write memory interface
27	R/W	1	eol_sel, 1: use eol as the line end indication, 0: use width as line end indication in the vdin write memory interface
26	R/W	0	vcp_nr_en. Only used in VDIN0. NOT used in VDIN1
25	R/W	1	vcp_wr_en Only used in VDIN0. NOT used in VDIN1
24	R/W	1	vcp_in_en Only used in VDIN0. NOT used in VDIN1
23	R/W	1	vdin frame reset enble, if true, it will provide frame reset during go_field(vsync) to the modules after that
22	R/W	1	vdin line fifo soft reset enable, meaning, if true line fifo will reset during go_field (vsync)
21	R/W	0	vdin direct write done status clear bit
20	R/W	0	vdin NR write done status clear bit
19	R/W	0	Vdin0_wr words swap : swap the 2 64bits word in 128 words
18	R/W	0	vdin0_wr_mif_swap_cbcr. Applicable only to vdin_write_format =2. 0=Output CbCr (NV12); 1=Output CrCb (NV21);
17:16	R/W	0	vdin0_wr_mif_vconv_mode. Applicable only to vdin_write_format=2. 0=Output every even line's CbCr; 1=Output every odd line's CbCr; 2=Reserved; 3=Output all CbCr.
13-12	R/W	0	vdin_write_format, 0: 4:2:2 to one canvas; 1: 4:4:4 to one canvas; 2: Y to luma canvas, CbCr to chroma canvas, for NV12/21; 3: yuv422 full pack mode
11	R/W	0	vdin write canvas double buffer enable, means the canvas address will be latched by vsync before using
9	R/W	0	vdin write request urgent
8	R/W	0	vdin write request enable
7-0	R/W	0	Write canvas address (For NV12/21 mode, it's LUMA canvas)

Table 9-2632 VDIN0_WR_H_START_END 0x1221

Bit(s)	R/W	Default	Description
29	R/W	0	if true, horizontal reverse
28-16	R/W	0	start
12-0	R/W	0	end

Table 9-2633 VDIN0_WR_V_START_END 0x1222

Bit(s)	R/W	Default	Description
29	R/W	0	if true, vertical reverse
28-16	R/W	0	start
12-0	R/W	0	end

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Table 9-2634 VDIN0_VSC_PHASE_STEP 0x1223

Bit(s)	R/W	Default	Description
24-16	R/W	0	integer portion
19-0	R/W	0	fraction portion

Table 9-2635 VDIN0_VSC_INI_CTRL 0x1224

Bit(s)	R/W	Default	Description
23	R/W	0	vsc_en, vertical scaler enable
21	R/W	0	vsc_phase0_always_en, when scale up, you have to set it to 1
20-16	R/W	0	ini skip_line_num
15-0	R/W	0	vscaler ini_phase

Table 9-2636 VDIN0_SCIN_HEIGHTM1 0x1225

Bit(s)	R/W	Default	Description
28-16	R/W	0xc7	Vshrink output height m1
12-0	R/W	0x437	scaler input height minus 1

Table 9-2637 VDIN0_DUMMY_DATA 0x1226

Bit(s)	R/W	Default	Description
23-16	R/W	0	dummy component 0
15-8	R/W	0x80	dummy component 1
7-0	R/W	0x80	dummy component 2

Table 9-2638 VDIN0_MATRIX_PROBE_COLOR 0x1228

Bit(s)	R/W	Default	Description
29-20	R/W	0	component 0
19-10	R/W	0	omponent 1
9-0	R/W	0	component 2

Table 9-2639 VDIN0_MATRIX_HL_COLOR 0x1229

Bit(s)	R/W	Default	Description
23-16	R/W	0	component 0
15-8	R/W	0	component 1
7-0	R/W	0	component 2

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Table 9-2640 VDIN0_MATRIX_PROBE_POS 0x122a

Bit(s)	R/W	Default	Description
28-16	R/W	0	probe x, position
12-0	R/W	0	probe y, postion

Table 9-2641 VDIN0_HIST_CTRL 0x1230

Bit(s)	R/W	Default	Description
31-24	R/W	0	No use
23-16	R/W	0	No use
11	R/W	0	Hist 34bin only mode
10-9	R/W	0	ldim_stts_din_sel, 00: from matrix0 dout, 01: from vsc_dout, 10: from matrix1 dout, 11: form matrix1 din
8	R/W	0	ldim_stts_en
6-5	R/W	0	hist_dnlp_low the real pixels in each bins got by VDIN_DNLP_HISTXX should multiple with 2^(dnlp_low+3)
3-2	R/W	0	hist_din_sel the source used for hist statistics. 2'b00: from MAT0_dout; 2'b01: from vsc_dout; 2'b10: from mat1_dout, 3: mat1_din
1	R/W	0	hist_win_en 1'b0: hist used for full picture; 1'b1: hist used for pixels within hist window
0	R/W	0	hist_spl_en 1'b0: disable hist readback; 1'b1: enable hist readback

Table 9-2642 VDIN0_HIST_H_START_END 0x1231

Bit(s)	R/W	Default	Description
28-16	R/W	0	hist_hstart horizontal start value to define hist window
12-0	R/W	0	hist_hend horizontal end value to define hist window

Table 9-2643 VDIN0_HIST_V_START_END 0x1232

Bit(s)	R/W	Default	Description
28-16	R/W	0	hist_vstart vertical start value to define hist window
12-0	R/W	0	hist_vend vertical end value to define hist window

Table 9-2644 VDIN0_HIST_MAX_MIN 0x1233

Bit(s)	R/W	Default	Description
15-8	R	0	hist_max maximum value
7-0	R	0	hist_min minimum value

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Table 9-2645 VDIN0_HIST_SPL_VAL 0x1234

Bit(s)	R/W	Default	Description
31-0	R	0	hist_spl_rd , counts for the total luma value

Table 9-2646 VDIN0_HIST_SPL_PIX_CNT 0x1235

Bit(s)	R/W	Default	Description
21-0	R	0	hist_spl_pixel_count, counts for the total calculated pixels

Table 9-2647 VDIN0_HIST_CHROMA_SUM 0x1236

Bit(s)	R/W	Default	Description
31-0	R	0	hist_chroma_sum , counts for the total chroma value

//0-255 are splited to 64 bins evenly, and VDIN_DNLP_HISTXX

//are the statistic number of pixels that within each bin.

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 2nd bin
15-0	R	0	counts for the 1st bin

Table 9-2648 VDIN0_DNLP_HIST01 0x1238

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 4th bin
15-0	R	0	counts for the 3rd bin

Table 9-2649 VDIN0_DNLP_HIST02 0x1239

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 6th bin
15-0	R	0	counts for the 5th bin

Table 9-2650 VDIN0_DNLP_HIST03 0x123a

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 8th bin
15-0	R	0	counts for the 7th bin

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Table 9-2651 VDIN0_DNLP_HIST04 0x123b

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 10th bin
15-0	R	0	counts for the 9th bin

Table 9-2652 VDIN0_DNLP_HIST05 0x123c

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 12th bin
15-0	R	0	counts for the 11th bin

Table 9-2653 VDIN0_DNLP_HIST06 0x123d

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 14th bin
15-0	R	0	counts for the 13th bin

Table 9-2654 VDIN0_DNLP_HIST07 0x123e

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 16th bin
15-0	R	0	counts for the 15th bin

Table 9-2655 VDIN0_DNLP_HIST08 0x123f

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 18th bin
15-0	R	0	counts for the 17th bin

Table 9-2656 VDIN0_DNLP_HIST09 0x1240

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 20th bin
15-0	R	0	counts for the 19th bin

Table 9-2657 VDIN0_DNLP_HIST10 0x1241

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 22nd bin
15-0	R	0	counts for the 21st bin

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Table 9-2658 VDIN0_DNLP_HIST11 0x1242

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 24th bin
15-0	R	0	counts for the 23rd bin

Table 9-2659 VDIN0_DNLP_HIST12 0x1243

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 26th bin
15-0	R	0	counts for the 25th bin

Table 9-2660 VDIN0_DNLP_HIST13 0x1244

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 28th bin
15-0	R	0	counts for the 27th bin

Table 9-2661 VDIN0_DNLP_HIST14 0x1245

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 30th bin
15-0	R	0	counts for the 29th bin

Table 9-2662 VDIN0_DNLP_HIST15 0x1246

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 32nd bin
15-0	R	0	counts for the 31st bin

Table 9-2663 VDIN0_DNLP_HIST16 0x1247

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 34th bin
15-0	R	0	counts for the 33rd bin

Table 9-2664 VDIN0_DNLP_HIST17 0x1248

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 36th bin
15-0	R	0	counts for the 35th bin

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Table 9-2665 VDIN0_DNLP_HIST18 0x1249

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 38th bin
15-0	R	0	counts for the 37th bin

Table 9-2666 VDIN0_DNLP_HIST19 0x124a

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 40th bin
15-0	R	0	counts for the 39th bin

Table 9-2667 VDIN0_DNLP_HIST20 0x124b

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 42nd bin
15-0	R	0	counts for the 41st bin

Table 9-2668 VDIN0_DNLP_HIST21 0x124c

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 44th bin
15-0	R	0	counts for the 43rd bin

Table 9-2669 VDIN0_DNLP_HIST22 0x124d

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 46th bin
15-0	R	0	counts for the 45th bin

Table 9-2670 VDIN0_DNLP_HIST23 0x124e

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 48th bin
15-0	R	0	counts for the 47th bin

Table 9-2671 VDIN0_DNLP_HIST24 0x124f

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 50th bin
15-0	R	0	counts for the 49th bin

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Table 9-2672 VDIN0_DNLP_HIST25 0x1250

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 52nd bin
15-0	R	0	counts for the 51st bin

Table 9-2673 VDIN0_DNLP_HIST26 0x1251

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 54th bin
15-0	R	0	counts for the 53rd bin

Table 9-2674 VDIN0_DNLP_HIST27 0x1252

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 56th bin
15-0	R	0	counts for the 55th bin

Table 9-2675 VDIN0_DNLP_HIST28 0x1253

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 58th bin
15-0	R	0	counts for the 57th bin

Table 9-2676 VDIN0_DNLP_HIST29 0x1254

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 60th bin
15-0	R	0	counts for the 59th bin

Table 9-2677 VDIN0_DNLP_HIST30 0x1255

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 62nd bin
15-0	R	0	counts for the 61st bin

Table 9-2678 VDIN0_DNLP_HIST31 0x1256

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 64th bin
15-0	R	0	counts for the 63rd bin

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Table 9-2679 VDIN0_LDIM_STTS_HIST_REGION_IDX 0x1257

Bit(s)	R/W	Default	Description
31	R	0	local dimming max statistic enable
28	R	0	eol enable
27-25	R	0	vertical line overlap number for max finding
24-22	R	0	horizontal pixel overlap number, 0: 17 pix, 1: 9 pix, 2: 5 pix, 3: 3 pix, 4: 0 pix
20	R	0	1,2,1 low pass filter enable before max/hist statistic
19-16	R	0	region H/V position index, refer to VDIN_LDIM_STTS_HIST_SET_REGION
15	R	0	1: region read index auto increase per read to VDIN_LDIM_STTS_HIST_READ_REGION
6-0	R	0	region read index

Table 9-2680 VDIN0_LDIM_STTS_HIST_SET_REGION 0x1258

Bit(s)	R/W	Default	Description
28:16	R	0	if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h0: read/write hvstart0 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h1: read/write hend01 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h2: read/write vend01 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h3: read/write hend23 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h4: read/write vend23 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h5: read/write hend45 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h6: read/write vend45 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'd7: read/write hend67 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h8: read/write vend67 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h9: read/write hend89 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'ha: read/write vend89 //hvstart0, Bit 28:16 row0 vstart, Bit 12:0 col0 hstart //hend01, Bit 28:16 col1 hend, Bit 12:0 col0 hend //vend01, Bit 28:16 row1 vend, Bit 12:0 row0 vend //hend23, Bit 28:16 col3 hend, Bit 12:0 col2 hend //vend23, Bit 28:16 row3 vend, Bit 12:0 row2 vend //hend45, Bit 28:16 col5 hend, Bit 12:0 col4 hend //vend45, Bit 28:16 row5 vend, Bit 12:0 row4 vend //hend67, Bit 28:16 col7 hend, Bit 12:0 col6 hend //vend67, Bit 28:16 row7 vend, Bit 12:0 row6 vend //hend89, Bit 28:16 col9 hend, Bit 12:0 col8 hend //vend89, Bit 28:16 row9 vend, Bit 12:0 row8 vend
12:0	R	0	

Table 9-2681 VDIN0_WR_URGENT_CTRL 0x1257

Bit(s)	R/W	Default	Description
15	R/W	0	Auto urgent enable
14	R/W	0	Urgent write
9	R/W	0	Write done last sel
8	R/W	0	Reg bvalid enable
7-4	R/W	0	Up_threshold
3-0	R/W	0	Down threshold

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Table 9-2682 VDIN0_RO_WRMIF_STATUS 0x1258

Bit(s)	R/W	Default	Description
20-18	R/W	0	C2 sel
17-15	R/W	0	C1 sel
14-12	R/W	0	C0 sel
11-9	R/W	0	Y2 sel
8-6	R/W	0	Y1 sel
5-3	R/W	0	Y0 sel
2	R/W	0	De tunnel enable
1	R	0	Di pre , nr done
0	R	0	Vdin write mif done

Table 9-2683 VDIN0_LDIM_STTS_HIST_READ_REGION 0x1259

Bit(s)	R/W	Default	Description
29:20	R	0	Max_comp2
19:10	R	0	Max_comp1
9:0	R	0	Max_comp0

Table 9-2684 VDIN0_MEAS_CTRL0 0x125a

Bit(s)	R/W	Default	Description
18	R/W	0	reset bit, high active
17	R/W	0	if true, widen hs/vs pulse
16	R/W	0	vsync total counter always accumulating enable
15-12	R/W	0	select hs/vs of video input channel to measure, 0: no selection, 1 vdi1, 2: vid2: 3: vid3, 4:vid4, 5:vdi5, 6:vdi6, 7:vdi7, 8:vdi8, 9:vdi9.
11-4	R/W	0	vsync_span, define how many vsync span need to measure
2-0	R/W	0	meas_hs_index, index to select which HS counter/range

Table 9-2685 VDIN0_MEAS_VS_COUNT_HI 0x125b

Bit(s)	R/W	Default	Description
19-16	R	0	meas_ind_total_count_n, every number of sync_span vsyncs, this count add 1
15-0	R	0	high bit portion of vsync total counter

Table 9-2686 VDIN0_MEAS_VS_COUNT_LO 0x125c

Bit(s)	R/W	Default	Description
31-0	R	0	low bit portion of vsync total counter

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VDIN0_MEAS_HS_RANGE 0x125d

//according to the meas_hs_index in register VDIN_MEAS_CTRL0

//meas_hs_index == 0, first hs range

//meas_hs_index == 1, second hs range

//meas_hs_index == 2, third hs range

//meas_hs_index == 3, fourth hs range

Bit(s)	R/W	Default	Description
28-16	R	0	count_start
12-0	R	0	count_end

VDIN0_MEAS_HS_COUNT 0x125e

//according to the meas_hs_index in register VDIN_MEAS_CTRL0,

//meas_hs_index == 0, first range hs counter,

//meas_hs_index == 1, second range hs

//meas_hs_index == 2, third range hs

//meas_hs_index == 3, fourth range hs

Bit(s)	R/W	Default	Description
23-0	R	0	Hs counter

Table 9-2687 VDIN0_BLKBAR_CTRL1 0x125f

Bit(s)	R/W	Default	Description
8	R/W	0	white_enable
7-0	R/W	0	blkbar_white_level

Table 9-2688 VDIN0_BLKBAR_CTRL0 0x1260

Bit(s)	R/W	Default	Description
31-24	R/W	0	blkbar_black_level threshold to judge a black point
20-8	R/W	0	blkbar_hwidth left and right region width
7-5	R/W	0	blkbar_comp_sel select yin or uin or vin to be the valid input
4	R/W	0	blkbar_sw_statistic_en enable software statistic of each block black points number
3	R/W	0	blkbar_det_en
2-1	R/W	0	blkbar_din_sel, 0:mat0_dout, 1:vsc_dout, 2:mat1_dout, 3:mat1_din
0	R/W	0	Blkbar_det_top_en

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Table 9-2689 VDIN0_BLKBAR_H_START_END 0x1261

Bit(s)	R/W	Default	Description
28-16	R/W	0	blkbar_hstart. Left region start
12-0	R/W	0	blkbar_hend. Right region end

Table 9-2690 VDIN0_BLKBAR_V_START_END 0x1262

Bit(s)	R/W	Default	Description
28-16	R/W	0	blkbar_vstart.
12-0	R/W	0	blkbar_vend.

Table 9-2691 VDIN0_BLKBAR_CNT_THRESHOLD 0x1263

Bit(s)	R/W	Default	Description
19-0	R/W	0	blkbar_cnt_threshold. threshold to judge whether a block is totally black

Table 9-2692 VDIN0_BLKBAR_ROW_TH1_TH2 0x1264

Bit(s)	R/W	Default	Description
28-16	R/W	0	blkbar_row_th1. //threshold of the top blackbar
12-0	R/W	0	blkbar_row_th2 //threshold of the bottom blackbar

Table 9-2693 VDIN0_BLKBAR_IND_LEFT_START_END 0x1265

Bit(s)	R/W	Default	Description
28-16	R	0	blkbar_ind_left_start. horizontal start of the left region in the current searching
12-0	R	0	blkbar_ind_left_end. horizontal end of the left region in the current searching

Table 9-2694 VDIN0_BLKBAR_IND_RIGHT_START_END 0x1266

Bit(s)	R/W	Default	Description
28-16	R	0	blkbar_ind_right_start.horizontal start of the right region in the current searching
12-0	R	0	blkbar_ind_right_end. horizontal end of the right region in the current searching

Table 9-2695 VDIN0_BLKBAR_IND_LEFT1_CNT 0x1267

Bit(s)	R/W	Default	Description
19-0	R	0	blkbar_ind_left1_cnt. Black pixel counter. left part of the left region

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Table 9-2696 VDIN0_BLKBAR_IND_LEFT2_CNT 0x1268

Bit(s)	R/W	Default	Description
19-0	R	0	blkbar_ind_left2_cnt. Black pixel counter. right part of the left region

Table 9-2697 VDIN0_BLKBAR_IND_RIGHT1_CNT 0x1269

Bit(s)	R/W	Default	Description
19-0	R	0	blkbar_ind_right1_cnt. Black pixel counter. left part of the right region

Table 9-2698 VDIN0_BLKBAR_IND_RIGHT2_CNT 0x126a

Bit(s)	R/W	Default	Description
19-0	R	0	blkbar_ind_right2_cnt. Black pixel counter. right part of the right region

Table 9-2699 VDIN0_BLKBAR_STATUS0 0x126b

Bit(s)	R/W	Default	Description
29	R	0	blkbar_ind_black_det_done. LEFT/RIGHT Black detection done
28-16	R	0	blkbar_top_pos. Top black bar position
12-0	R	0	blkbar_bot_pos. Bottom black bar position

Table 9-2700 VDIN0_BLKBAR_STATUS1 0x126c

Bit(s)	R/W	Default	Description
28-16	R	0	blkbar_left_pos. Left black bar posiont
12-0	R	0	blkbar_right_pos. Right black bar position

Table 9-2701 VDIN0_WIN_H_START_END 0x126d

Bit(s)	R/W	Default	Description
28-16	R/W	0	input window H start
12-0	R/W	0	input window H end

Table 9-2702 VDIN0_WIN_V_START_END 0x126e

Bit(s)	R/W	Default	Description
28-16	R/W	0	input window V start
12-0	R/W	0	input window V end

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Table 9-2703 VDIN0_ASFIFO_CTRL3 0x126f

Bit(s)	R/W	Default	Description
31	R/W	0	Vdi9 DE enable
30	R/W	0	Vdi9 go field enable
29	R/W	0	Vdi9 go line enable
28	R/W	0	Vdi9 if true, negative active input vsync
27	R/W	0	Vdi9 if true, negative active input hsync
26	R/W	0	Vdi9 vsync soft reset fifo enable
25	R/W	0	Vdi9 overflow status clear
24	R/W	0	Vdi9 asfifo soft reset, level signal
15	R/W	0	Vdi7 DE enable
14	R/W	0	Vdi7 go field enable
13	R/W	0	Vdi7 go line enable
12	R/W	0	Vdi7 if true, negative active input vsync
11	R/W	0	Vdi7 if true, negative active input hsync
10	R/W	0	Vdi7 vsync soft reset fifo enable
9	R/W	0	Vdi7 overflow status clear
8	R/W	0	Vdi7 asfifo soft reset, level signal
7	R/W	0	Vdi6 DE enable
6	R/W	0	Vdi6 go field enable
5	R/W	0	Vdi6 go line enable
4	R/W	0	Vdi6 if true, negative active input vsync
3	R/W	0	Vdi6 if true, negative active input hsync
2	R/W	0	Vdi6 vsync soft reset fifo enable
1	R/W	0	Vdi6 overflow status clear
0	R/W	0	Vdi6 asfifo soft reset, level signal

Table 9-2704 VDIN0_COM_GCLK_CTRL2 0x1270

Bit(s)	R/W	Default	Description
3-2	R/W	0	Vshrk_clk2 ctrl
1-0	R/W	0	Vshrk_clk1 ctrl

Table 9-2705 VDIN0_VSHRK_CTRL 0x1271

Bit(s)	R/W	Default	Description
27	R/W	0	Vshrk enable
26:25	R/W	0	Vshrk mode, 0: 1/2 shrink, 1: 1/4 shrink, 2: 1/8 shrink

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Bit(s)	R/W	Default	Description
24	R/W	0	Vshrink lpf mode, 1: 0.5,1.5,1.5,0.5 lpf for 1/4 shrink, 0.5,1.5,1.5...for 1/8 shrink
23:0	R/W	0	Vshrink padding dummy data

Table 9-2706 VDIN0_HIST32 0x1272

Bit(s)	R/W	Default	Description
31:0	R	0	Hist 32 mode, [31:16] for white pixel number, 15:0 for black pixel number

Table 9-2707 VDIN0_COM_STATUS3 0x1273

Bit(s)	R/W	Default	Description
7	R	0	Vdi9 fifo overflow
5:0	R	0	Vdi9 asfifo cnt

Table 9-2708 VDIN0_SYNC_MASK 0x1274

Bit(s)	R/W	Default	Description
17	R/W	0	Vsync_mask_en
16	R/W	0	Hsync_mask_en
15-8	R/W	64	Vsync_mask_num: When vsync_mask_en=1, vdin_output_vsync will keep zero for vsync_mask_num*1024 vdin clock cycle after vdin_input_vsync pluse. Example: vdin_clock = 666MHz□vsync_mask_num=255, vdin out vsync will at least keep zero for 0.392ms after one input_vsync
7-0	R/W	64	Hsync_mask_num When hsync_mask_en=1, vdin_output_hsync will keep zero for hsync_mask_num*32 vdin clock cycle after vdin_input_vsync pluse

Table 9-2709 VDIN0_DOLBY_DSC_CTRL0 0x1275

Bit(s)	R/W	Default	Description
31	R/W	0	Dolby check enable
30	R/W	0	Tunnel swap mode enable
29-24	R/W	0	Soft reset control, 29 : dsc, 28~27: crc check, 26~24, reserved
16	R/W	0	Little endian mode
15-0	R/W	0	Monitor metadata position

Table 9-2710 VDIN0_DOLBY_DSC_CTRL1 0x1276

Bit(s)	R/W	Default	Description
31-16	R/W	0	Metadata pixel start position
7-0	R/W	0	Crc check control

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Table 9-2711 VDIN0_DOLBY_DSC_CTRL2 0x1277

Bit(s)	R/W	Default	Description
31	R/W	0	Metadata read enable
30	R/W	0	Metadata read address auto-increment
29-20	R/W	0	Metadata sum
17-0	R/W	0	Tunnel mode channel selection

Table 9-2712 VDIN0_DOLBY_DSC_CTRL3 0x1278

Bit(s)	R/W	Default	Description
15-0	R/W	0	Select metadata position

Table 9-2713 VDIN0_DOLBY_AXI_CTRL0 0x1279

Bit(s)	R/W	Default	Description
31	R/W	0	Memory read enable
30	R/W	0	AXI bus read enable
29	R/W	0	AXI write channel urgent
28	R/W	0	Pack mode little endian
27	R/W	0	AXI bus soft reset
26	R/W	0	Frame reset enable
25	R/W	0	Memory read protection enable
24-16	R/W	0	Memory read sum
15-8	R/W	0	AXI request hold line
7-6	R/W	0	AXI burst length
5	R/W	0	Frame buffer start
4	R/W	0	Buffer start
3-2	R/W	0	AXI status monitor control
1-0	R/W	0	awid

Table 9-2714 VDIN0_DOLBY_ AXI_CTRL1 0x127a

Bit(s)	R/W	Default	Description
31-0	R/W	0	Buffer start address

Table 9-2715 VDIN0_DOLBY_ AXI_CTRL2 0x127b

Bit(s)	R/W	Default	Description
31-16	R/W	0	Buffer size
15-0	R/W	0	Frame buffer size

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Table 9-2716 VDIN0_DOLBY_ AXI_CTRL3 0x127c

Bit(s)	R/W	Default	Description
7-0	R/W	0	Hold cycle

Table 9-2717 VDIN0_WRARB_MODE 0x12c0

Bit(s)	R/W	Default	Description
23:16	R/W	0	wrarb_sel : uns, default = 0 , wrarb_sel [0]==0 slave dc0 connect master port0 wrarb_sel[0]==1 slave dc0 connect master port1 wrarb_sel [1]==0 slave dc1 connect master port0 wrarb_sel[1]==1 slave dc1 connect master port1 wrarb_sel [2]==0 slave dc2 connect master port0 wrarb_sel[2]==1 slave dc2 connect master port1 wrarb_sel [3]==0 slave dc3 connect master port0 wrarb_sel[3]==1 slave dc3 connect master port1 wrarb_sel [4]==0 slave dc4 connect master port0 wrarb_sel[4]==1 slave dc3 connect master port1 wrarb_sel [5]==0 slave dc5 connect master port0 wrarb_sel[5]==1 slave dc3 connect master port1
8	R/W	0	wrarb_arb_mode : uns, default = 0 , wrarb_arb_mode[0] master port0 arb way,
1:0	R/W	0	wrarb_gate_clk_ctrl : uns, default = 0 , wrarb_gate_clk_ctrl[1:0] master port0 clk gate control

Table 9-2718 VDIN0_WRARB_REQEN_SLV 0x12c1

Bit(s)	R/W	Default	Description
7:0	R/W	0	wrarb_dc_req_en : unsigned , default = 0 wrarb_dc_req_en [0]: the slv0 req to mst port0 enable, wrarb_dc_req_en [1]: the slv1 req to mst port0 enable, wrarb_dc_req_en [2]: the slv2 req to mst port0 enable, wrarb_dc_req_en [0]: the slv0 req to mst port1 enable, wrarb_dc_req_en [1]: the slv1 req to mst port1 enable, wrarb_dc_req_en [2]: the slv2 req to mst port1 enable,

Table 9-2719 VDIN0_WRARB_WEIGH0_SLV 0x12C2

Bit(s)	R/W	Default	Description
29:0	R/W	0	wrdc_weigh_sxn : unsigned , default = 0 wrdc_weigh_sxn [0*6+:6]: the slv0 req weigh number wrdc_weigh_sxn [1*6+:6]: the slv1 req weigh number wrdc_weigh_sxn [2*6+:6]: the slv2 req weigh number wrdc_weigh_sxn [3*6+:6]: the slv3 req weigh number wrdc_weigh_sxn [4*6+:6]: the slv4 req weigh number

Table 9-2720 VDIN0_WRARB_WEIGH1_SLV 0x12C3

Bit(s)	R/W	Default	Description
17:0	R/W	0	wrdc_weigh_sxn : unsigned , default = 0 the slv5 req weigh number [0*6+:6],the slv6 req weighnumber [1*6+:6],the slv7 req weighnumber [2*6+:6],

Table 9-2721 VDIN0_RDWR_ARB_STATUS 0x12c4

Bit(s)	R/W	Default	Description
2	R.O	0	ro_wrarb_arb_busy : unsigned , default = 0
1	R/W	0x0	reserve :
0	R.O	0	ro_rdarb_arb_busy : unsigned , default = 0

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Table 9-2722 VDIN0_ARB_DBG_CTRL 0x12c5

Bit(s)	R/W	Default	Description
31:0	R.O	0	ro_det_cmd_ctrl : unsigned , default = 0

Table 9-2723 VDIN0_ARB_DBG_STAT 0x12C6

Bit(s)	R/W	Default	Description
31:0	R.O	0	ro_det_dbg_stat : unsigned , default = 0

Table 9-2724 VDIN0_CRC_CHK 0x12c9

Bit(s)	R/W	Default	Description
0	W	0	vdin crc check start (pulse)

Table 9-2725 VDIN0_RO_CRC 0x12ca

Bit(s)	R/W	Default	Description
31-0	R	0	vdin crc result (lock by go_field)

Table 9-2726 VDIN0_LINE_INT 0x12cb

Bit(s)	R/W	Default	Description
31	R	0	line interrupt flag
30	R	0	write done flag
17	R/W	0	clear line interrupt flag
16	R/W	0	clear write done interrupt flag
15	R/W	0	enable line interrupt
12-0	R/W	0	line interrupt number

Table 9-2727 VDIN0_DSC_CTRL 0x12d0

Bit(s)	R/W	Default	Description
9:4	R/W	36	reg_dithout_switch : ,uns, default = 36;//{2'h2,2'h1,2'h0}
3	R/W	1	reg_detunnel_en : ,uns, default = 1;
2	R/W	0	reg_detunnel_u_start : ,uns, default = 0;
1	R/W	1	reg_vdin_dith_en : ,uns, default = 1;
0	R/W	1	reg_descramble_en : ,uns, default = 1;

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Table 9-2728 VDIN0_CFMT_CTRL 0x12d1

Bit(s)	R/W	Default	Description
8	R/W	0	reg_chfmt_rpt_pix : uns, default = 0 ; // if true, horizontal formatter use repeating to generete pixel, otherwise use bilinear interpolation
7:4	R/W	0	reg_chfmt_ini_phase : uns, default = 0 ; // horizontal formatter initial phase
3	R/W	0	reg_chfmt_rpt_p0_en : uns, default = 0 ; // horizontal formatter repeat pixel 0 enable
2:1	R/W	1	reg_chfmt_yc_ratio : uns, default = 1 ; // horizontal Y/C ratio, 00: 1:1, 01: 2:1, 10: 4:1
0	R/W	1	reg_chfmt_en : uns, default = 1 ; // horizontal formatter enable

Table 9-2729 VDIN0_CFMT_W 0x12d2

Bit(s)	R/W	Default	Description
28:16	R/W	1920	reg_chfmt_w : uns, default = 1920 ;horizontal formatter width
12:0	R/W	960	reg_cvfmt_w : uns, default = 960 ;vertical formatter width

Table 9-2730 VDIN0_SCB_CTRL0 0x12d3

Bit(s)	R/W	Default	Description
11	R/W	1	reg_444c422_gofield_en : uns, default = 1;
10	R/W	1	reg_tunnel_en : uns, default = 1;
9:4	R/W	36	reg_tunnel_outswitch : uns, default = 36;//{2'h2,2'h1,2'h0}
3:2	R/W	0	reg_444c422_mode : uns, default = 0; //0:left 1:right 2,3:avg
1	R/W	0	reg_444c422_bypass : uns, default = 0; 1:bypass

Table 9-2731 VDIN0_SCB_CTRL1 0x12d4

Bit(s)	R/W	Default	Description
28:16	R/W	1920	reg_444c422_hsize : uns, default = 1920 ;horizontal size
12:0	R/W	960	reg_444c422_vsize : uns, default = 960 ;vertical size

Table 9-2732 VDIN0_DSC_HSIZE 0x12d5

Bit(s)	R/W	Default	Description
28:16	R/W	1920	reg_detunnel_hsize : uns, default = 1920 ;
12:0	R/W	1920	reg_dither_hsize : uns, default = 1920 ;

Table 9-2733 VDIN0_DSC_DETUNNEL_SEL 0x12d6

Bit(s)	R/W	Default	Description
17:0	R/W	34658	reg_detunnel_sel : uns, default = 34658; //{3'h1,3'h0,3'h3 ,3'h5,3'h4,3'h2}

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Table 9-2734 VDIN0_DSC_TUNNEL_SEL 0x12d7

Bit(s)	R/W	Default	Description
17:0	R/W	69868	reg_tunnel_sel : uns, default = 69868; //= {3'h2,3'h1 ,3'h0,3'h3 ,3'h5,3'h4};

Table 9-2735 VDIN0_HDR2_SIZE 0x12d8

Bit(s)	R/W	Default	Description
28-16	R/W	0x438	Vdin hdr2 vsize
12-0	R/W	0x780	Vdin hdr2 hsize

Table 9-2736 VDIN0_VSHRK_SIZE_M1 0x12d9

Bit(s)	R/W	Default	Description
28-16	R/W	0x10d	Vshrink input vsize m1
12-0	R/W	0x437	Vshrink input hsize m1

VDIN0_DITH_CTRL 0x12e0

Same as VPU_VENCL_DITH_CTRL

VDIN0_DITH_LUT_1 0x12e1

Same as VPU_VENCL_DITH_LUT_1

VDIN0_DITH_LUT_2 0x12e2

Same as VPU_VENCL_DITH_LUT_2

VDIN0_DITH_LUT_3 0x12e3

Same as VPU_VENCL_DITH_LUT_3

VDIN0_DITH_LUT_4 0x12e4

Same as VPU_VENCL_DITH_LUT_4

VDIN0_DITH_LUT_5 0x12e5

Same as VPU_VENCL_DITH_LUT_5

VDIN0_DITH_LUT_6 0x12e6

Same as VPU_VENCL_DITH_LUT_6

VDIN0_DITH_LUT_7 0x12e7

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Same as VPU_VENCL_DITH_LUT_7

VDIN0_DITH_LUT_8 0x12e8
Same as VPU_VENCL_DITH_LUT_8

VDIN0_DITH_LUT_9 0x12e9
Same as VPU_VENCL_DITH_LUT_9

VDIN0_DITH_LUT_10 0x12ea
Same as VPU_VENCL_DITH_LUT_10

VDIN0_DITH_LUT_10 0x12eb
Same as VPU_VENCL_DITH_LUT_10

VDIN0_DITH_LUT_11 0x12ec
Same as VPU_VENCL_DITH_LUT_11

Table 9-2737 VDIN0_HSK_CTRL 0x12ef

Bit(s)	R/W	Default	Description
22:16	R/W	4	reg_hshrink_size, 2: 1/2 4: 1/4 hshrink, max=64: 1/64 hshrink
12:0	R/W	1920	reg_frm_hsize

Table 9-2738 VDIN0_HSK_COEF_0 0x12f0

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef00

Table 9-2739 VDIN0_HSK_COEF_1 0x12f1

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef01

Table 9-2740 VDIN0_HSK_COEF_2 0x12f2

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef02

Table 9-2741 VDIN0_HSK_COEF_3 0x12f3

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef03

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Table 9-2742 VDIN0_HSK_COEF_4 0x12f4

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef04

Table 9-2743 VDIN0_HSK_COEF_5 0x12f5

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef05

Table 9-2744 VDIN0_HSK_COEF_6 0x12f6

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef06

Table 9-2745 VDIN0_HSK_COEF_7 0x12f7

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef07

Table 9-2746 VDIN0_HSK_COEF_8 0x12f8

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef08

Table 9-2747 VDIN0_HSK_COEF_9 0x12f9

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef09

Table 9-2748 VDIN0_HSK_COEF_10 0x12fa

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef10

Table 9-2749 VDIN0_HSK_COEF_11 0x12fb

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef11

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Table 9-2750 VDIN0_HSK_COEF_12 0x12fc

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef12

Table 9-2751 VDIN0_HSK_COEF_13 0x12fd

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef13

Table 9-2752 VDIN0_HSK_COEF_14 0x12fe

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef14

Table 9-2753 VDIN0_HSK_COEF_15 0x12ff

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef15

VDIN1_SCALE_COEF_IDX 0x1300

VDIN1_SCALE_COEF 0x1301

Table 9-2754 VDIN1_COM_CTRL0 0x1302

Bit(s)	R/W	Default	Description
31	R/W	0	mpeg_to_vdin_sel, 0: mpeg source to NR directly, 1: mpeg source pass through here
30	R/W	0	mpeg_field info which can be written by software
29	R/W	0	force go_field, pulse signal
28	R/W	0	force go_line, pulse signal
27	R/W	0	enable mpeg_go_field input signal
26-20	R/W	0	hold lines
19	R/W	0	delay go_field function enable
18-12	R/W	0	delay go_field line number
11-10	R/W	0	component2 output switch, 00: select component0 in, 01: select component1 in, 10: select component2 in
9-8	R/W	0	component1 output switch, 00: select component0 in, 01: select component1 in, 10: select component2 in
7-6	R/W	0	component0 output switch, 00: select component0 in, 01: select component1 in, 10: select component2 in
5	R/W	0	input window selection function enable

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Bit(s)	R/W	Default	Description
4	R/W	0	enable VDIN common data input, otherwise there will be no video data input
3-0	R/W	0	vdin selection, 1: mpeg_in from dram; 2: bt656 input; 3: Reserved (component input); 4: Reserved(tvdecoder input); 5: Reserved(hdmi rx input); 6: reserved(digital video input); 7: Wr_back 0; 8: reserved(MIPI CSI2) ;9: Wr_back 1; 10: Reserved(second bt656 input); otherwise no input.

Table 9-2755 VDIN1_ACTIVE_MAX_PIX_CNT_STATUS 0x1303

Bit(s)	R/W	Default	Description
28-16	R	0	active_max_pix_cnt, readonly
12-0	R	0	active_max_pix_cnt_shadow, readonly

Table 9-2756 VDIN1_LCNT_STATUS 0x1304

Bit(s)	R/W	Default	Description
28-16	R	0	go_line_cnt, readonly
12-0	R	0	active_line_cnt, readonly

Table 9-2757 VDIN1_COM_STATUS0 0x1305

Bit(s)	R/W	Default	Description
12-3	R	0	lfifo_buf_cnt
2	R	0	vdin_direct_done status
1	R	0	vdin_nr_done status
0	R	0	field

Table 9-2758 VDIN1_COM_STATUS1 0x1306

Bit(s)	R/W	Default	Description
31	R	0	vdi4 fifo overflow
29-24	R	0	vdi3_asfifo_cnt
23	R	0	vdi3 fifo overflow
21-16	R	0	vdi3_asfifo_cnt
15	R	0	vdi2 fifo overflow
13-8	R	0	vdi2_asfifo_cnt
7	R	0	vdi1 fifo overflow
5-0	R	0	vdi1_asfifo_cnt

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Table 9-2759 VDIN1_LCNT_SHADOW_STATUS 0x1307

Bit(s)	R/W	Default	Description
28-16	R	0	go_line_cnt_shadow, readonly
12-0	R	0	active_line_cnt_shadow, readonly

Table 9-2760 VDIN1_ASFIFO_CTRL0 0x1308

Bit(s)	R/W	Default	Description
31	R/W	0	hv size select 0: write mif size 1:vdin hsc input size
30-28	R/W	0	v de start line number
27-20	R/W	0	v blank
19-12	R/W	0	h blank
10-9	R/W	0	bist pattern 0:horizontal gray scale 1: vertical gray scale 2/3:random data
8	R/W	0	Vdin bist enable : replace vdi6 (loop back path)
7	R/W	0	Vdi1 DE enable
6	R/W	0	Vdi1 go field enable
5	R/W	0	Vdi1 go line enable
4	R/W	0	Vdi1 if true, negative active input vsync
3	R/W	0	Vdi1 if true, negative active input hsync
2	R/W	0	Vdi1 vsync soft reset fifo enable
1	R/W	0	Vdi1 overflow status clear
0	R/W	0	Vdi1 asfifo soft reset, level signal

Table 9-2761 VDIN1_ASFIFO_CTRL1 0x1309

Bit(s)	R/W	Default	Description
23	R/W	0	Vdi4 DE enable
22	R/W	0	Vdi4 go field enable
21	R/W	0	Vdi4 go line enable
20	R/W	0	Vdi4 if true, negative active input vsync
19	R/W	0	Vdi4 if true, negative active input hsync
18	R/W	0	Vdi4 vsync soft reset fifo enable
17	R/W	0	Vdi4 overflow status clear
16	R/W	0	Vdi4 asfifo soft reset, level signal
7	R/W	0	Vdi3 DE enable
6	R/W	0	Vdi3 go field enable
5	R/W	0	Vdi3 go line enable
4	R/W	0	Vdi3 if true, negative active input vsync
3	R/W	0	Vdi3 if true, negative active input hsync

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Bit(s)	R/W	Default	Description
2	R/W	0	Vdi3 vsync soft reset fifo enable
1	R/W	0	Vdi3 overflow status clear
0	R/W	0	Vdi3 asfifo soft reset, level signal

Table 9-2762 VDIN1_WIDTHM1I_WIDTHM1O 0x130a

Bit(s)	R/W	Default	Description
28-16	R/W	0	input width minus 1, after the window function
12-0	R/W	0	output width minus 1

Table 9-2763 VDIN1_SC_MISC_CTRL 0x130b

Bit(s)	R/W	Default	Description
14-8	R/W	0	hsc_ini_pixi_ptr, signed data, only useful when short_lineo_en is true
7	R/W	0	prehsc_en
6	R/W	0	hsc_en
5	R/W	0	hsc_short_lineo_en, short line output enable
4	R/W	0	hsc_nearest_en
3	R/W	0	Hsc_phase0_always_en
3	R/W	0	phase0_always_en
2-0	R/W	0	hsc_bank_length

Table 9-2764 VDIN1_HSC_PHASE_STEP 0x130c

Bit(s)	R/W	Default	Description
28-24	R/W	0	integer portion
23-0	R/W	0	fraction portion

Table 9-2765 VDIN1_HSC_INI_CTRL 0x130d

Bit(s)	R/W	Default	Description
30-29	R/W	0	hscale rpt_p0_num
28-24	R/W	0	hscale ini_rcv_num
23-0	R/W	0	hscale ini_phase

Table 9-2766 VDIN1_COM_STATUS2 0x130e

Bit(s)	R/W	Default	Description
23	R	0	Vdi7 fifo overflow
21-16	R	0	Vdi7_asfifo_cnt

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Bit(s)	R/W	Default	Description
15	R	0	Vdi6 fifo overflow
13-8	R	0	Vdi6_asfifo_cnt
7	R	0	vdi5 fifo overflow
5-0	R	0	vdi5_asfifo_cnt

Table 9-2767 VDIN1_ASFIFO_CTRL2 0x130f

Bit(s)	R/W	Default	Description
25	R/W	0	if true, decimation counter sync with first valid DE in the field, //otherwise the decimation counter is not sync with external signal
24	R/W	0	decimation de enable
23-20	R/W	0	decimation phase, which counter value use to decimate,
19-16	R/W	0	decimation number, 0: not decimation, 1: decimation 2, 2: decimation 3 ....
7	R/W	0	Vdi5 DE enable
6	R/W	0	Vdi5 go field enable
5	R/W	0	Vdi5 go line enable
4	R/W	0	Vdi5 if true, negative active input vsync
3	R/W	0	Vdi5 if true, negative active input hsync
2	R/W	0	Vdi5 vsync soft reset fifo enable
1	R/W	0	Vdi5 overflow status clear
0	R/W	0	Vdi5 asfifo soft reset, level signal

Table 9-2768 VDIN1_MATRIX_CTRL 0x1310

Bit(s)	R/W	Default	Description
0	R/W	0	post conversion matrix enable

Table 9-2769 VDIN1_MATRIX_COEF00_01 0x1311

Bit(s)	R/W	Default	Description
28-16	R/W	0	coef00
12-0	R/W	0	coef01

Table 9-2770 VDIN1_MATRIX_COEF02_10 0x1312

Bit(s)	R/W	Default	Description
28-16	R/W	0	coef02
12-0	R/W	0	Coef10

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Table 9-2771 VDIN1_MATRIX_COEF11_12 0x1313

Bit(s)	R/W	Default	Description
28-16	R/W	0	Coef11
12-0	R/W	0	Coef12

Table 9-2772 VDIN1_MATRIX_COEF20_21 0x1314

Bit(s)	R/W	Default	Description
28-16	R/W	0	Coef20
12-0	R/W	0	coef21

Table 9-2773 VDIN1_ 0x1315

Bit(s)	R/W	Default	Description
18-16	R/W	0	convrs
7-0	R/W	0	Coef22

Table 9-2774 VDIN1_MATRIX_OFFSET0_1 0x1316

Bit(s)	R/W	Default	Description
26-16	R/W	0	offset0
10-0	R/W	0	Offset1

Table 9-2775 VDIN1_MATRIX_OFFSET2 0x1317

Bit(s)	R/W	Default	Description
10-0	R/W	0	Offset2

Table 9-2776 VDIN1_MATRIX_PRE_OFFSET0_1 0x1318

Bit(s)	R/W	Default	Description
26-16	R/W	0	Pre_offset0
10-0	R/W	0	Pre_Offset1

Table 9-2777 VDIN1_MATRIX_PRE_OFFSET2 0x1319

Bit(s)	R/W	Default	Description
10-0	R/W	0	Pre_Offset2

Table 9-2778 VDIN1_LFIFO_CTRL 0x131a

Bit(s)	R/W	Default	Description
11-0	R/W	0	lfifo_buf_size

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Table 9-2779 VDIN1_LFIFO_CTRL 0x131a

Bit(s)	R/W	Default	Description
31	R/W	1	Linebuffer soft reset enable
30	R/W	1	Frame reset enable
28	R/W	0	Discard data enable
18	R/W	0	Vdin channel1 output enable
17	R/W	1	Vdin channel0 output enable
16	R/W	0	Pps_path_sel : 0: pps before linebuffer 1:pps after linebuffer
13-0	R/W	0x1000	lfifo_buf_size

Table 9-2780 VDIN1_COM_GCLK_CTRL 0x131b

Bit(s)	R/W	Default	Description
15-14	R/W	0	Gate clock control for blackbar detector
13-12	R/W	0	Gate clock control for hist
11-10	R/W	0	Gate clock control for line fifo
9-8	R/W	0	Gate clock control for matrix
7-6	R/W	0	Gate clock control for horizontal scaler
5-4	R/W	0	Gate clock control for pre scaler
3-2	R/W	0	Gate clock control for vdin_com_proc
1-0	R/W	0	Gate clock control for the vdin reg

Table 9-2781 VDIN1_INTF_WIDTHM1 0x131c

Bit(s)	R/W	Default	Description
26	R/W	0	VDIN write mif bvalid_sel: 1. Bvalid_singnal from bus, 0: bytes_wr handshakes
25	R/W	0	VDIN write mif burst last sel: 1. All kind of burst last signal include ext_data_last. 0. Used the normal burst last signal
12-0	R/W	0	VDIN input interface width minus 1, before the window function, after the de decimation

Table 9-2782 VDIN1_WR_CTRL2 0x131f

Bit(s)	R/W	Default	Description
19	R/W	0	Vdin1 wr bit10 mode
18	R/W	0	Data_ext_en 1: send out data if req was interrupt by soft reset 0 : normal mode
17:16	R/W	1	Words lim[1:0]: it would not send out request before Words_lim *16 words were ready
15:12	R/W	1	Burst_ lim : 00 , 1 word in 1burst , 01 ,2 words in 1burst, 10, 4 words in 1burst , 11 reserved
10:9	R/W	0	Words_lim[3:2]

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Bit(s)	R/W	Default	Description
8	R/W	0	1: discard data before line fifo, 0: normal mode
7-0	R/W	0	Write chroma canvas address, for NV12/21 mode.

Table 9-2783 VDIN1_WR_CTRL 0x1320

Bit(s)	R/W	Default	Description
31-30	R/W	0	vdin1_wr_mif_hconv_mode. Applicable only to vdin_write_format=0 or 2. 0=Output every even pixel's CbCr; 1=Output every odd pixel's CbCr; 2=Output an average value per even&odd pair of pixels; 3=Output all CbCr. Only applys to vdin_write_format =2.
29	R/W	0	vdin1_wr_mif_no_clk_gate. If true, enable free-run clock.
28	R/W	0	clear write response counter in the vdin write memory interface
27	R/W	1	eol_sel, 1: use eol as the line end indication, 0: use width as line end indication in the vdin write memory interface
23	R/W	1	vdin frame reset enble, if true, it will provide frame reset during go_field(vsync) to the modules after that
22	R/W	1	vdin line fifo soft reset enable, meaning, if true line fifo will reset during go_field (vsync)
21	R/W	0	vdin direct write done status clear bit
20	R/W	0	vdin NR write done status clear bit
19	R/W	0	Vdin0_wr words swap : swap the 2 64bits word in 128 words
18	R/W	0	vdin1_wr_mif_swap_cbcr. Applicable only to vdin_write_format =2. 0=Output CbCr (NV12); 1=Output CrCb (NV21);
17:16	R/W	0	vdin1_wr_mif_vconv_mode. Applicable only to vdin_write_format=2. 0=Output every even line's CbCr; 1=Output every odd line's CbCr; 2=Reserved; 3=Output all CbCr.
13-12	R/W	0	vdin_write_format, 0: 4:2:2 to one canvas; 1: 4:4:4 to one canvas; 2: Y to luma canvas, CbCr to chroma canvas, for NV12/21; 3: 422 10 bit full pack mode
11	R/W	0	vdin write canvas double buffer enable, means the canvas address will be latched by vsync before using
9	R/W	0	vdin write request urgent
8	R/W	0	vdin write request enable
7-0	R/W	0	Write canvas address (For NV12/21 mode, it's LUMA canvas)

Table 9-2784 VDIN1_WR_H_START_END 0x1321

Bit(s)	R/W	Default	Description
27-16	R/W	0	start
11-0	R/W	0	end

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Table 9-2785 VDIN1_WR_V_START_END 0x1322

Bit(s)	R/W	Default	Description
27-16	R/W	0	start
11-0	R/W	0	end

Table 9-2786 VDIN1_VSC_PHASE_STEP 0x1323

Bit(s)	R/W	Default	Description
24-16	R/W	0	integer portion
19-0	R/W	0	fraction portion

Table 9-2787 VDIN1_VSC_INI_CTRL 0x1324

Bit(s)	R/W	Default	Description
23	R/W	0	vsc_en, vertical scaler enable
21	R/W	0	vsc_phase0_always_en, when scale up, you have to set it to 1
20-16	R/W	0	ini skip_line_num
15-0	R/W	0	vscaler ini_phase

Table 9-2788 VDIN1_SCIN_HEIGHTM1 0x1325

Bit(s)	R/W	Default	Description
28-16	R/W	0xc7	Vshrink output height m1
12-0	R/W	0x437	scaler input height minus 1

Table 9-2789 VDIN1_DUMMY_DATA 0x1326

Bit(s)	R/W	Default	Description
23-16	R/W	0	dummy component 0
15-8	R/W	0x80	dummy component 1
7-0	R/W	0x80	dummy component 2

Table 9-2790 VDIN1_MATRIX_PROBE_COLOR 0x1328

Bit(s)	R/W	Default	Description
29-20	R/W	0	component 0
19-10	R/W	0	omponent 1
9-0	R/W	0	component 2

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Table 9-2791 VDIN1_MATRIX_HL_COLOR 0x1329

Bit(s)	R/W	Default	Description
23-16	R/W	0	component 0
15-8	R/W	0	component 1
7-0	R/W	0	component 2

Table 9-2792 VDIN1_MATRIX_PROBE_POS 0x132a

Bit(s)	R/W	Default	Description
28-16	R/W	0	probe x, position
12-0	R/W	0	probe y, postion

Table 9-2793 VDIN1_HIST_CTRL 0x1330

Bit(s)	R/W	Default	Description
31-24	R/W	0	Hist pixel white threshold, larger than this will be counted as white pixel number
23-16	R/W	0	Hist pixel black threshold, less than this will be counted as black pixel number
11	R/W	0	Hist 32bin only mode
10-9	R/W	0	ldim_stts_din_sel, 00: from matrix0 dout, 01: from vsc_dout, 10: from matrix1 dout, 11: form matrix1 din
8	R/W	0	ldim_stts_en
6-5	R/W	0	hist_dnlp_low the real pixels in each bins got by VDIN_DNLP_HISTXX should multiple with 2^(dnlp_low+3)
3-2	R/W	0	hist_din_sel the source used for hist statistics. 2'b00: from MAT0_dout; 2'b01: from vsc_dout; 2'b10: from mat1_dout, 3: mat1_din
1	R/W	0	hist_win_en 1'b0: hist used for full picture; 1'b1: hist used for pixels within hist window
0	R/W	0	hist_spl_en 1'b0: disable hist readback; 1'b1: enable hist readback

Table 9-2794 VDIN1_HIST_H_START_END 0x1331

Bit(s)	R/W	Default	Description
28-16	R/W	0	hist_hstart horizontal start value to define hist window
12-0	R/W	0	hist_hend horizontal end value to define hist window

Table 9-2795 VDIN1_HIST_V_START_END 0x1332

Bit(s)	R/W	Default	Description
28-16	R/W	0	hist_vstart vertical start value to define hist window
12-0	R/W	0	hist_vend vertical end value to define hist window

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Table 9-2796 VDIN1_HIST_MAX_MIN 0x1333

Bit(s)	R/W	Default	Description
15-8	R	0	hist_max maximum value
7-0	R	0	hist_min minimum value

Table 9-2797 VDIN1_HIST_SPL_VAL 0x1334

Bit(s)	R/W	Default	Description
31-0	R	0	hist_spl_rd , counts for the total luma value

Table 9-2798 VDIN1_HIST_SPL_PIX_CNT 0x1335

Bit(s)	R/W	Default	Description
21-0	R	0	hist_spl_pixel_count, counts for the total calculated pixels

Table 9-2799 VDIN1_HIST_CHROMA_SUM 0x1336

Bit(s)	R/W	Default	Description
31-0	R	0	hist_chroma_sum , counts for the total chroma value

//0-255 are splited to 64 bins evenly, and VDIN_DNLP_HISTXX

//are the statistic number of pixels that within each bin.

Table 9-2800 VDIN1_DNLP_HIST00 0x1337

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 2nd bin
15-0	R	0	counts for the 1st bin

Table 9-2801 VDIN1_DNLP_HIST01 0x1338

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 4th bin
15-0	R	0	counts for the 3rd bin

Table 9-2802 VDIN1_DNLP_HIST02 0x1339

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 6th bin
15-0	R	0	counts for the 5th bin

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Table 9-2803 VDIN1_DNLP_HIST03 0x133a

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 8th bin
15-0	R	0	counts for the 7th bin

Table 9-2804 VDIN1_DNLP_HIST04 0x133b

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 10th bin
15-0	R	0	counts for the 9th bin

Table 9-2805 VDIN1_DNLP_HIST05 0x133c

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 12th bin
15-0	R	0	counts for the 11th bin

Table 9-2806 VDIN1_DNLP_HIST06 0x133d

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 14th bin
15-0	R	0	counts for the 13th bin

Table 9-2807 VDIN1_DNLP_HIST07 0x133e

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 16th bin
15-0	R	0	counts for the 15th bin

Table 9-2808 VDIN1_DNLP_HIST08 0x133f

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 18th bin
15-0	R	0	counts for the 17th bin

Table 9-2809 VDIN1_DNLP_HIST09 0x1340

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 20th bin
15-0	R	0	counts for the 19th bin

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Table 9-2810 VDIN1_DNLP_HIST10 0x1341

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 22nd bin
15-0	R	0	counts for the 21st bin

Table 9-2811 VDIN1_DNLP_HIST11 0x1342

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 24th bin
15-0	R	0	counts for the 23rd bin

Table 9-2812 VDIN1_DNLP_HIST12 0x1343

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 26th bin
15-0	R	0	counts for the 25th bin

Table 9-2813 VDIN1_DNLP_HIST13 0x1344

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 28th bin
15-0	R	0	counts for the 27th bin

Table 9-2814 VDIN1_DNLP_HIST14 0x1345

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 30th bin
15-0	R	0	counts for the 29th bin

Table 9-2815 VDIN1_DNLP_HIST15 0x1346

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 32nd bin
15-0	R	0	counts for the 31st bin

Table 9-2816 VDIN1_DNLP_HIST16 0x1347

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 34th bin
15-0	R	0	counts for the 33rd bin

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Table 9-2817 VDIN1_DNLP_HIST17 0x1348

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 36th bin
15-0	R	0	counts for the 35th bin

Table 9-2818 VDIN1_DNLP_HIST18 0x1349

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 38th bin
15-0	R	0	counts for the 37th bin

Table 9-2819 VDIN1_DNLP_HIST19 0x134a

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 40th bin
15-0	R	0	counts for the 39th bin

Table 9-2820 VDIN1_DNLP_HIST20 0x134b

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 42nd bin
15-0	R	0	counts for the 41st bin

Table 9-2821 VDIN1_DNLP_HIST21 0x134c

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 44th bin
15-0	R	0	counts for the 43rd bin

Table 9-2822 VDIN1_DNLP_HIST22 0x134d

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 46th bin
15-0	R	0	counts for the 45th bin

Table 9-2823 VDIN1_DNLP_HIST23 0x134e

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 48th bin
15-0	R	0	counts for the 47th bin

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Table 9-2824 VDIN1_DNLP_HIST24 0x134f

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 50th bin
15-0	R	0	counts for the 49th bin

Table 9-2825 VDIN1_DNLP_HIST25 0x1350

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 52nd bin
15-0	R	0	counts for the 51st bin

Table 9-2826 VDIN1_DNLP_HIST26 0x1351

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 54th bin
15-0	R	0	counts for the 53rd bin

Table 9-2827 VDIN1_DNLP_HIST27 0x1352

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 56th bin
15-0	R	0	counts for the 55th bin

Table 9-2828 VDIN1_DNLP_HIST28 0x1353

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 58th bin
15-0	R	0	counts for the 57th bin

Table 9-2829 VDIN1_DNLP_HIST29 0x1354

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 60th bin
15-0	R	0	counts for the 59th bin

Table 9-2830 VDIN1_DNLP_HIST30 0x1355

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 62nd bin
15-0	R	0	counts for the 61st bin

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Table 9-2831 VDIN1_DNLP_HIST31 0x1356

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 64th bin
15-0	R	0	counts for the 63rd bin

Table 9-2832 VDIN1_LDIM_STTS_HIST_REGION_IDX 0x1357

Bit(s)	R/W	Default	Description
31	R	0	local dimming max statistic enable
28	R	0	eol enable
27-25	R	0	vertical line overlap number for max finding
24-22	R	0	horizontal pixel overlap number, 0: 17 pix, 1: 9 pix, 2: 5 pix, 3: 3 pix, 4: 0 pix
20	R	0	1,2,1 low pass filter enable before max/hist statistic
19-16	R	0	region H/V position index, refer to VDIN_LDIM_STTS_HIST_SET_REGION
15	R	0	1: region read index auto increase per read to VDIN_LDIM_STTS_HIST_READ_REGION
6-0	R	0	region read index

Table 9-2833 VDIN1_LDIM_STTS_HIST_SET_REGION 0x1358

Bit(s)	R/W	Default	Description
28:16	R	0	if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h0: read/write hvstart0 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h1: read/write hend01 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h2: read/write vend01 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h3: read/write hend23 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h4: read/write vend23 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h5: read/write hend45 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h6: read/write vend45 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'd7: read/write hend67 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h8: read/write vend67 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'h9: read/write hend89 if VDIN_LDIM_STTS_HIST_REGION_IDX[19:16] == 5'ha: read/write vend89 //hvstart0, Bit 28:16 row0 vstart, Bit 12:0 col0 hstart //hend01, Bit 28:16 col1 hend, Bit 12:0 col0 hend //vend01, Bit 28:16 row1 vend, Bit 12:0 row0 vend //hend23, Bit 28:16 col3 hend, Bit 12:0 col2 hend //vend23, Bit 28:16 row3 vend, Bit 12:0 row2 vend //hend45, Bit 28:16 col5 hend, Bit 12:0 col4 hend //vend45, Bit 28:16 row5 vend, Bit 12:0 row4 vend //hend67, Bit 28:16 col7 hend, Bit 12:0 col6 hend //vend67, Bit 28:16 row7 vend, Bit 12:0 row6 vend //hend89, Bit 28:16 col9 hend, Bit 12:0 col8 hend //vend89, Bit 28:16 row9 vend, Bit 12:0 row8 vend
12:0	R	0	

Table 9-2834 VDIN1_LDIM_STTS_HIST_READ_REGION 0x1359

Bit(s)	R/W	Default	Description
29:20	R	0	Max_comp2
19:10	R	0	Max_comp1
9:0	R	0	Max_comp0

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Table 9-2835 VDIN1_MEAS_CTRL0 0x135a

Bit(s)	R/W	Default	Description
18	R/W	0	reset bit, high active
17	R/W	0	if true, widen hs/vs pulse
16	R/W	0	vsync total counter always accumulating enable
14-12	R/W	0	select hs/vs of video input channel to measure, 0: no selection, 1 vdi1, 2: vid2: 3: vid3, 4:vid4, 5:vdi5, 6:vdi6, 7:vdi7, 8:vdi8, 9:vdi9.
11-4	R/W	0	vsync_span, define how many vsync span need to measure
2-0	R/W	0	meas_hs_index, index to select which HS counter/range

Table 9-2836 VDIN1_MEAS_VS_COUNT_HI 0x135b

Bit(s)	R/W	Default	Description
19-16	R	0	meas_ind_total_count_n, every number of sync_span vsyncs, this count add 1
15-0	R	0	high bit portion of vsync total counter

Table 9-2837 VDIN1_MEAS_VS_COUNT_LO 0x135c

Bit(s)	R/W	Default	Description
31-0	R	0	low bit portion of vsync total counter

VDIN1_MEAS_HS_RANGE 0x135d

//according to the meas_hs_index in register VDIN_MEAS_CTRL0

//meas_hs_index == 0, first hs range

//meas_hs_index == 1, second hs range

//meas_hs_index == 2, third hs range

//meas_hs_index == 3, fourth hs range

Bit(s)	R/W	Default	Description
28-16	R	0	count_start
12-0	R	0	count_end

VDIN1_MEAS_HS_COUNT 0x135e

//according to the meas_hs_index in register VDIN_MEAS_CTRL0,

//meas_hs_index == 0, first range hs counter,

//meas_hs_index == 1, second range hs

//meas_hs_index == 2, third range hs

//meas_hs_index == 3, fourth range hs

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Bit(s)	R/W	Default	Description
23-0	R	0	Hs counter

Table 9-2838 VDIN1_BLKBAR_CTRL1 0x135f

Bit(s)	R/W	Default	Description
8	R/W	0	white_enable
7-0	R/W	0	blkbar_white_level

Table 9-2839 VDIN1_BLKBAR_CTRL0 0x1360

Bit(s)	R/W	Default	Description
31-24	R/W	0	blkbar_black_level threshold to judge a black point
20-8	R/W	0	blkbar_hwidth left and right region width
7-5	R/W	0	blkbar_comp_sel select yin or uin or vin to be the valid input
4	R/W	0	blkbar_sw_statistic_en enable software statistic of each block black points number
3	R/W	0	blkbar_det_en
2-1	R/W	0	blkbar_din_sel
0	R/W	0	Blkbar_det_top_en

Table 9-2840 VDIN1_BLKBAR_H_START_END 0x1361

Bit(s)	R/W	Default	Description
28-16	R/W	0	blkbar_hstart. Left region start
12-0	R/W	0	blkbar_hend. Right region end

Table 9-2841 VDIN1_BLKBAR_V_START_END 0x1362

Bit(s)	R/W	Default	Description
28-16	R/W	0	blkbar_vstart.
12-0	R/W	0	blkbar_vend.

Table 9-2842 VDIN1_BLKBAR_CNT_THRESHOLD 0x1363

Bit(s)	R/W	Default	Description
19-0	R/W	0	blkbar_cnt_threshold. threshold to judge whether a block is totally black

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Table 9-2843 VDIN1_BLKBAR_ROW_TH1_TH2 0x1364

Bit(s)	R/W	Default	Description
28-16	R/W	0	blkbar_row_th1. //threshold of the top blackbar
12-0	R/W	0	blkbar_row_th2 //threshold of the bottom blackbar

Table 9-2844 VDIN1_BLKBAR_IND_LEFT_START_END 0x1365

Bit(s)	R/W	Default	Description
28-16	R	0	blkbar_ind_left_start. horizontal start of the left region in the current searching
12-0	R	0	blkbar_ind_left_end. horizontal end of the left region in the current searching

Table 9-2845 VDIN1_BLKBAR_IND_RIGHT_START_END 0x1366

Bit(s)	R/W	Default	Description
28-16	R	0	blkbar_ind_right_start.horizontal start of the right region in the current searching
12-0	R	0	blkbar_ind_right_end. horizontal end of the right region in the current searching

Table 9-2846 VDIN1_BLKBAR_IND_LEFT1_CNT 0x1367

Bit(s)	R/W	Default	Description
19-0	R	0	blkbar_ind_left1_cnt. Black pixel counter. left part of the left region

Table 9-2847 VDIN1_BLKBAR_IND_LEFT2_CNT 0x1368

Bit(s)	R/W	Default	Description
19-0	R	0	blkbar_ind_left2_cnt. Black pixel counter. right part of the left region

Table 9-2848 VDIN1_BLKBAR_IND_RIGHT1_CNT 0x1369

Bit(s)	R/W	Default	Description
19-0	R	0	blkbar_ind_right1_cnt. Black pixel counter. left part of the right region

Table 9-2849 VDIN1_BLKBAR_IND_RIGHT2_CNT 0x136a

Bit(s)	R/W	Default	Description
19-0	R	0	blkbar_ind_right2_cnt. Black pixel counter. right part of the right region

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Table 9-2850 VDIN1_BLKBAR_STATUS0 0x136b

Bit(s)	R/W	Default	Description
29	R	0	blkbar_ind_black_det_done. LEFT/RIGHT Black detection done
28-16	R	0	blkbar_top_pos. Top black bar position
12-0	R	0	blkbar_bot_pos. Bottom black bar position

Table 9-2851 VDIN1_BLKBAR_STATUS1 0x136c

Bit(s)	R/W	Default	Description
28-16	R	0	blkbar_left_pos. Left black bar posiont
12-0	R	0	blkbar_right_pos. Right black bar position

Table 9-2852 VDIN1_WIN_H_START_END 0x136d

Bit(s)	R/W	Default	Description
28-16	R/W	0	input window H start
12-0	R/W	0	input window H end

Table 9-2853 VDIN1_WIN_V_START_END 0x136e

Bit(s)	R/W	Default	Description
28-16	R/W	0	input window V start
12-0	R/W	0	input window V end

Table 9-2854 VDIN1_ASFIFO_CTRL3 0x136f

Bit(s)	R/W	Default	Description
15	R/W	0	Vdi7 DE enable
14	R/W	0	Vdi7 go field enable
13	R/W	0	Vdi7 go line enable
12	R/W	0	Vdi7 if true, negative active input vsync
11	R/W	0	Vdi7 if true, negative active input hsync
10	R/W	0	Vdi7 vsync soft reset fifo enable
9	R/W	0	Vdi7 overflow status clear
8	R/W	0	Vdi7 asfifo soft reset, level signal
7	R/W	0	Vdi6 DE enable
6	R/W	0	Vdi6 go field enable
5	R/W	0	Vdi6 go line enable
4	R/W	0	Vdi6 if true, negative active input vsync
3	R/W	0	Vdi6 if true, negative active input hsync

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Bit(s)	R/W	Default	Description
2	R/W	0	Vdi6 vsync soft reset fifo enable
1	R/W	0	Vdi6 overflow status clear
0	R/W	0	Vdi6 asfifo soft reset, level signal

Table 9-2855 VDIN1_COM_GCLK_CTRL2 0x1370

Bit(s)	R/W	Default	Description
3-2	R/W	0	Vshrk_clk2 ctrl
1-0	R/W	0	Vshrk_clk1 ctrl

Table 9-2856 VDIN1_VSHRK_CTRL 0x1371

Bit(s)	R/W	Default	Description
27	R/W	0	Vshrk enable
26:25	R/W	0	Vshrk mode, 0: 1/2 shrink, 1: 1/4 shrink, 2: 1/8 shrink
24	R/W	0	Vshrink lpf mode, 1: 0.5,1.5,1.5,0.5 lpf for 1/4 shrink, 0.5,1.5,1.5...for 1/8 shrink
23:0	R/W	0	Vshrink padding dummy data

Table 9-2857 VDIN1_HIST32 0x1372

Bit(s)	R/W	Default	Description
31:0	R	0	Hist 32 mode, [31:16] for white pixel number, 15:0 for black pixel number

Table 9-2858 VDIN1_COM_STATUS3 0x1373

Bit(s)	R/W	Default	Description
7	R	0	Vdi9 fifo overflow
5:0	R	0	Vdi9 asfifo cnt

Table 9-2859 VDIN1_CRC_CHK 0x13c9

Bit(s)	R/W	Default	Description
0	W	0	vdin crc check start (pulse)

Table 9-2860 VDIN1_RO_CRC 0x13ca

Bit(s)	R/W	Default	Description
31-0	R	0	vdin crc result (lock by go_field)

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Table 9-2861 VDIN1_LINE_INT 0x13cb

Bit(s)	R/W	Default	Description
31	R	0	line interrupt flag
30	R	0	write done flag
17	R/W	0	clear line interrupt flag
16	R/W	0	clear write done interrupt flag
15	R/W	0	enable line interrupt
12-0	R/W	0	line interrupt number

Table 9-2862 VDIN1_HDR2_SIZE 0x13d8

Bit(s)	R/W	Default	Description
28-16	R/W	0x438	Vdin hdr2 vsize
12-0	R/W	0x780	Vdin hdr2 hsize

Table 9-2863 VDIN1_VSHRK_SIZE_M1 0x13d9

Bit(s)	R/W	Default	Description
28-16	R/W	0x10d	Vshrink input vsize m1
12-0	R/W	0x437	Vshrink input hsize m1

Table 9-2864 VI_HIST_CTRL 0x2e00

Bit(s)	R/W	Default	Description
17-16	R/W	0	Spl_sft: the splt are right shift by spl_sft, 0: no shift, 1: right shift by 1. 2,3...
14	R/W	0	Hist_34bin_only, bin 32~63 are not valid, there are 34bins, bin0~bin31, and bin 64 for black pixel, bin 65 for white pixel
13-11	R/W	0	Hist_in_sel: 0: vpp_dout, 1: vpp_vd1_din, 2: vpp_vd2_din, 3: osd1, 4:osd2 5: di pre 6: vdin 7: post blend
10-8	R/W	0	Hist_din_comp_mux: mux of each component, din[9:0],[19:10],[29:20] switches
7-5	R/W	0	Hist_dnlp_low: hist number are shift by (hist_dnlp_low + 3). I.e. Dnlp_low =0, >> 3, dnlp_low=1, >> 4
1	R/W	0	Hist_win_en: hist statistic in a window
0	R/W	0	Luma_hist_spl_en, 1: enable the histogram statistic

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Table 9-2865 VDIN1_WRARB_MODE 0x13c0

Bit(s)	R/W	Default	Description
23:16	R/W	0	wrarb_sel : uns, default = 0 , wrarb_sel [0]==0 slave dc0 connect master port0 wrarb_sel[0]==1 slave dc0 connect master port1 wrarb_sel [1]==0 slave dc1 connect master port0 wrarb_sel[1]==1 slave dc1 connect master port1 wrarb_sel [2]==0 slave dc2 connect master port0 wrarb_sel[2]==1 slave dc2 connect master port1 wrarb_sel [3]==0 slave dc3 connect master port0 wrarb_sel[3]==1 slave dc3 connect master port1 wrarb_sel [4]==0 slave dc4 connect master port0 wrarb_sel[4]==1 slave dc3 connect master port1 wrarb_sel [5]==0 slave dc5 connect master port0 wrarb_sel[5]==1 slave dc3 connect master port1
8	R/W	0	wrarb_arb_mode : uns, default = 0 , wrarb_arb_mode[0] master port0 arb way,
1:0	R/W	0	wrarb_gate_clk_ctrl : uns, default = 0 , wrarb_gate_clk_ctrl[1:0] master port0 clk gate control

Table 9-2866 VDIN1_WRARB_REQEN_SLV 0x13c1

Bit(s)	R/W	Default	Description
7:0	R/W	0	wrarb_dc_req_en : unsigned , default = 0 wrarb_dc_req_en [0]: the slv0 req to mst port0 enable, wrarb_dc_req_en [1]: the slv1 req to mst port0 enable, wrarb_dc_req_en [2]: the slv2 req to mst port0 enable, wrarb_dc_req_en [0]: the slv0 req to mst port1 enable, wrarb_dc_req_en [1]: the slv1 req to mst port1 enable, wrarb_dc_req_en [2]: the slv2 req to mst port1 enable,

Table 9-2867 VDIN1_WRARB_WEIGH0_SLV 0x13C2

Bit(s)	R/W	Default	Description
29:0	R/W	0	wrdc_weigh_sxn : unsigned , default = 0 wrdc_weigh_sxn [0*6+:6]: the slv0 req weigh number wrdc_weigh_sxn [1*6+:6]: the slv1 req weigh number wrdc_weigh_sxn [2*6+:6]: the slv2 req weigh number wrdc_weigh_sxn [3*6+:6]: the slv3 req weigh number wrdc_weigh_sxn [4*6+:6]: the slv4 req weigh number

Table 9-2868 VDIN1_WRARB_WEIGH1_SLV 0x13C3

Bit(s)	R/W	Default	Description
17:0	R/W	0	wrdc_weigh_sxn : unsigned , default = 0 the slv5 req weigh number [0*6+:6],the slv6 req weighnumber [1*6+:6],the slv7 req weighnumber [2*6+:6],

Table 9-2869 VDIN1_RDWR_ARB_STATUS 0x13c4

Bit(s)	R/W	Default	Description
2	R.O	0	ro_wrarb_arb_busy : unsigned , default = 0
1	R/W	0x0	reserve :
0	R.O	0	ro_rdarb_arb_busy : unsigned , default = 0

Table 9-2870 VDIN1_ARB_DBG_CTRL 0x13c5

Bit(s)	R/W	Default	Description
31:0	R.O	0	ro_det_cmd_ctrl : unsigned , default = 0

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Table 9-2871 VDIN1_ARB_DBG_STAT 0x13C6

Bit(s)	R/W	Default	Description
31:0	R.O	0	ro_det_dbg_stat : unsigned , default = 0

Table 9-2872 VDIN1_DSC_CTRL 0x13d0

Bit(s)	R/W	Default	Description
9:4	R/W	36	reg_dithout_switch : ,uns, default = 36;//{2'h2,2'h1,2'h0}
3	R/W	1	reg_detunnel_en : ,uns, default = 1;
2	R/W	0	reg_detunnel_u_start : ,uns, default = 0;
1	R/W	1	reg_vdin_dith_en : ,uns, default = 1;
0	R/W	1	reg_descramble_en : ,uns, default = 1;

Table 9-2873 VDIN1_CFMT_CTRL 0x13d1

Bit(s)	R/W	Default	Description
8	R/W	0	reg_chfmt_rpt_pix : uns, default = 0 ; // if true, horizontal formatter use repeating to generete pixel, otherwise use bilinear interpolation
7:4	R/W	0	reg_chfmt_ini_phase : uns, default = 0 ; // horizontal formatter initial phase
3	R/W	0	reg_chfmt_rpt_p0_en : uns, default = 0 ; // horizontal formatter repeat pixel 0 enable
2:1	R/W	1	reg_chfmt_yc_ratio : uns, default = 1 ; // horizontal Y/C ratio, 00: 1:1, 01: 2:1, 10: 4:1
0	R/W	1	reg_chfmt_en : uns, default = 1 ; // horizontal formatter enable

Table 9-2874 VDIN1_CFMT_W 0x13d2

Bit(s)	R/W	Default	Description
28:16	R/W	1920	reg_chfmt_w : uns, default = 1920 ;horizontal formatter width
12:0	R/W	960	reg_cvfmt_w : uns, default = 960 ;vertical formatter width

Table 9-2875 VDIN1_SCB_CTRL0 0x13d3

Bit(s)	R/W	Default	Description
10	R/W	1	reg_tunnel_en : uns, default = 1;
9:4	R/W	36	reg_tunnel_outswitch : uns, default = 36;//{2'h2,2'h1,2'h0}
3:2	R/W	0	reg_444c422_mode : uns, default = 0; //0:left 1:right 2,3:avg
1	R/W	0	reg_444c422_bypass : uns, default = 0; 1:bypass

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Table 9-2876 VDIN1_SCB_CTRL1 0x13d4

Bit(s)	R/W	Default	Description
28:16	R/W	1920	reg_444c422_hsize : uns, default = 1920 ;horizontal size
12:0	R/W	960	reg_444c422_vsize : uns, default = 960 ;vertical size

Table 9-2877 VDIN1_DSC_HSIZE 0x13d5

Bit(s)	R/W	Default	Description
28:16	R/W	1920	reg_detunnel_hsize : uns, default = 1920 ;
12:0	R/W	1920	reg_dither_hsize : uns, default = 1920 ;

Table 9-2878 VDIN1_DSC_DETUNNEL_SEL 0x13d6

Bit(s)	R/W	Default	Description
17:0	R/W	34658	reg_detunnel_sel : uns, default = 34658; //{3'h1,3'h0,3'h3 ,3'h5,3'h4,3'h2}

Table 9-2879 VDIN1_DSC_TUNNEL_SEL 0x13d7

Bit(s)	R/W	Default	Description
17:0	R/W	69868	reg_tunnel_sel : uns, default = 69868; //= {3'h2,3'h1 ,3'h0,3'h3 ,3'h5,3'h4};

Table 9-2880 VDIN1_HDR2_SIZE

Bit(s)	R/W	Default	Description
28-16	R/W	0x438	Vdin hdr2 vsize
12-0	R/W	0x780	Vdin hdr2 hsize

Table 9-2881 VDIN1_VSHRK_SIZE_M1

Bit(s)	R/W	Default	Description
28-16	R/W	0x10d	Vshrink input vsize m1
12-0	R/W	0x437	Vshrink input hsize m1

VDIN1_DITH_CTRL 0x13e0

Same as VPU_VENCL_DITH_CTRL

VDIN1_DITH_LUT_1 0x13e1

Same as VPU_VENCL_DITH_LUT_1

VDIN1_DITH_LUT_2 0x13e2

Same as VPU_VENCL_DITH_LUT_2

VDIN1_DITH_LUT_3 0x13e3

Same as VPU_VENCL_DITH_LUT_3

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VDIN1_DITH_LUT_4 0x13e4

Same as VPU_VENCL_DITH_LUT_4

VDIN1_DITH_LUT_5 0x13e5

Same as VPU_VENCL_DITH_LUT_5

VDIN1_DITH_LUT_6 0x13e6

Same as VPU_VENCL_DITH_LUT_6

VDIN1_DITH_LUT_7 0x13e7

Same as VPU_VENCL_DITH_LUT_7

VDIN1_DITH_LUT_8 0x13e8

Same as VPU_VENCL_DITH_LUT_8

VDIN1_DITH_LUT_9 0x13e9

Same as VPU_VENCL_DITH_LUT_9

VDIN1_DITH_LUT_10 0x13ea

Same as VPU_VENCL_DITH_LUT_10

VDIN1_DITH_LUT_10 0x13eb

Same as VPU_VENCL_DITH_LUT_10

VDIN1_DITH_LUT_11 0x13ec

Same as VPU_VENCL_DITH_LUT_11

Table 9-2882 VDIN1_HSK_CTRL 0x13ef

Bit(s)	R/W	Default	Description
22:16	R/W	4	reg_hshrink_size, 2: 1/2 4: 1/4 hshrink, max=64: 1/64 hshrink
12:0	R/W	1920	reg_frm_hsize

Table 9-2883 VDIN1_HSK_COEF_0 0x13f0

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef00

Table 9-2884 VDIN1_HSK_COEF_1 0x13f1

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef01

Table 9-2885 VDIN1_HSK_COEF_2 0x13f2

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef02

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Table 9-2886 VDIN1_HSK_COEF_3 0x13f3

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef03

Table 9-2887 VDIN1_HSK_COEF_4 0x13f4

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef04

Table 9-2888 VDIN1_HSK_COEF_5 0x13f5

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef05

Table 9-2889 VDIN1_HSK_COEF_6 0x13f6

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef06

Table 9-2890 VDIN1_HSK_COEF_7 0x13f7

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef07

Table 9-2891 VDIN1_HSK_COEF_8 0x13f8

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef08

Table 9-2892 VDIN1_HSK_COEF_9 0x13f9

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef09

Table 9-2893 VDIN1_HSK_COEF_10 0x13fa

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef10

Table 9-2894 VDIN1_HSK_COEF_11 0x13fb

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef11

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Table 9-2895 VDIN1_HSK_COEF_12 0x13fc

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef12

Table 9-2896 VDIN1_HSK_COEF_13 0x13fd

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef13

Table 9-2897 VDIN1_HSK_COEF_14 0x13fe

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef14

Table 9-2898 VDIN1_HSK_COEF_15 0x13ff

Bit(s)	R/W	Default	Description
31:0	R/W	0	reg_hsk_coef15

Table 9-2899 VI_HIST_H_START_END 0x2e01

Bit(s)	R/W	Default	Description
28-16	R/W	0	Hist_hstart, refer to VI_HIST_CTRL[1]
12-0	R/W	0	Hist_hend

Table 9-2900 VI_HIST_V_START_END 0x2e02

Bit(s)	R/W	Default	Description
28-16	R/W	0	Hist_vstart, refer to VI_HIST_CTRL[1]
12-0	R/W	0	Hist_vend

Table 9-2901 VI_HIST_MAX_MIN 0x2e03

Bit(s)	R/W	Default	Description
15-8	R	0	hist_max maximum value
7-0	R	0	hist_min minimum value

Table 9-2902 VI_HIST_SPL_VAL 0x2e04

Bit(s)	R/W	Default	Description
31-0	R	0	hist_spl_rd , counts for the total luma value

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Table 9-2903 VI_HIST_SPL_PIX_CNT 0x2e05

Bit(s)	R/W	Default	Description
21-0	R	0	hist_spl_pixel_count, counts for the total calculated pixels

Table 9-2904 VI_HIST_CHROMA_SUM 0x2e06

Bit(s)	R/W	Default	Description
31-0	R	0	hist_chroma_sum , counts for the total chroma value

//0-255 are splited to 64 bins evenly, and VDIN_DNLP_HISTXX

//are the statistic number of pixels that within each bin.

Table 9-2905 VI_DNLP_HIST00 0x2e07

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 2nd bin
15-0	R	0	counts for the 1st bin

Table 9-2906 VI_DNLP_HIST01 0x2e08

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 4th bin
15-0	R	0	counts for the 3rd bin

Table 9-2907 VI_DNLP_HIST02 0x2e09

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 6th bin
15-0	R	0	counts for the 5th bin

Table 9-2908 VI_DNLP_HIST03 0x2e0a

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 8th bin
15-0	R	0	counts for the 7th bin

Table 9-2909 VI_DNLP_HIST04 0x2e0b

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 10th bin
15-0	R	0	counts for the 9th bin

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Table 9-2910 VI_DNLP_HIST05 0x2e0c

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 12th bin
15-0	R	0	counts for the 11th bin

Table 9-2911 VI_DNLP_HIST06 0x2e0d

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 14th bin
15-0	R	0	counts for the 13th bin

Table 9-2912 VI_DNLP_HIST07 0x2e0e

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 16th bin
15-0	R	0	counts for the 15th bin

Table 9-2913 VI_DNLP_HIST08 0x2e0f

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 18th bin
15-0	R	0	counts for the 17th bin

Table 9-2914 VI_DNLP_HIST09 0x2e10

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 20th bin
15-0	R	0	counts for the 19th bin

Table 9-2915 VI_DNLP_HIST10 0x2e11

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 22nd bin
15-0	R	0	counts for the 21st bin

Table 9-2916 VI_DNLP_HIST11 0x2e12

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 24th bin
15-0	R	0	counts for the 23rd bin

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Table 9-2917 VI_DNLP_HIST12 0x2e13

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 26th bin
15-0	R	0	counts for the 25th bin

Table 9-2918 VI_DNLP_HIST13 0x2e14

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 28th bin
15-0	R	0	counts for the 27th bin

Table 9-2919 VI_DNLP_HIST14 0x2e15

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 30th bin
15-0	R	0	counts for the 29th bin

Table 9-2920 VI_DNLP_HIST15 0x2e16

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 32nd bin
15-0	R	0	counts for the 31st bin

Table 9-2921 VI_DNLP_HIST16 0x2e17

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 34th bin
15-0	R	0	counts for the 33rd bin

Table 9-2922 VI_DNLP_HIST17 0x2e18

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 36th bin
15-0	R	0	counts for the 35th bin

Table 9-2923 VI_DNLP_HIST18 0x2e19

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 38th bin
15-0	R	0	counts for the 37th bin

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Table 9-2924 VI_DNLP_HIST19 0x2e1a

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 40th bin
15-0	R	0	counts for the 39th bin

Table 9-2925 VI_DNLP_HIST20 0x2e1b

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 42nd bin
15-0	R	0	counts for the 41st bin

Table 9-2926 VI_DNLP_HIST21 0x2e1c

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 44th bin
15-0	R	0	counts for the 43rd bin

Table 9-2927 VI_DNLP_HIST22 0x2e1d

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 46th bin
15-0	R	0	counts for the 45th bin

Table 9-2928 VI_DNLP_HIST23 0x2e1e

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 48th bin
15-0	R	0	counts for the 47th bin

Table 9-2929 VI_DNLP_HIST24 0x2e1f

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 50th bin
15-0	R	0	counts for the 49th bin

Table 9-2930 VI_DNLP_HIST25 0x2e20

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 52nd bin
15-0	R	0	counts for the 51st bin

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Table 9-2931 VI_DNLP_HIST26 0x2e21

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 54th bin
15-0	R	0	counts for the 53rd bin

Table 9-2932 VI_DNLP_HIST27 0x2e22

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 56th bin
15-0	R	0	counts for the 55th bin

Table 9-2933 VI_DNLP_HIST28 0x2e23

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 58th bin
15-0	R	0	counts for the 57th bin

Table 9-2934 VI_DNLP_HIST29 0x2e24

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 60th bin
15-0	R	0	counts for the 59th bin

Table 9-2935 VI_DNLP_HIST30 0x2e25

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 62nd bin
15-0	R	0	counts for the 61st bin

Table 9-2936 VI_DNLP_HIST31 0x2e26

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 64th bin
15-0	R	0	counts for the 63rd bin

Table 9-2937 VI_DNLP_HIST31 0x2e27

Bit(s)	R/W	Default	Description
31-16	R	0	counts for the 66th bin, for white pix
15-0	R	0	counts for the 65th bin, for black pix

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Table 9-2938 VI_HIST_PIC_SIZE 0x2e28

Bit(s)	R/W	Default	Description
28-16	R/W	0	Hist_pic_height
12-0	R/W	0	Hist_pic_width

Table 9-2939 VI_HIST_GCLK_CTRL 0x2e2a

Bit(s)	R/W	Default	Description
5-4	R/W	0	Gated clock control of hist_clk
3-2	R/W	0	Gated clock control of clk0
1-0	R/W	0	Gated clock control of hist register clock

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Table 9-2940 VPU_MAFBC_BLOCK_ID 0x3a00

Bit(s)	R/W	Default	Description
31:16	R.O	0x0	PRODUCT_ID : // Contains a product-specific value
15:12	R.O	0x0	VERSION_MAJOR : // Major release number of the AFBC decoder. This is the R part of an RnPn release number.
11:4	R.O	0x0	VERSION_MINOR : // Minor release number of the AFBC decoder. This is the P part of an RnPn release number.
3:0	R.O	0x0	VERSION_STATUS : // The version status of the AFBC decoder release. Starts at 0 and increases by one for each release.

Table 9-2941 VPU_MAFBC_IRQ_RAW_STATUS 0x3a01

Bit(s)	R/W	Default	Description
5	R.O	0x0	SECURE_ID_ERROR : // Activated when an invalid TrustZone Media Protection (TZMP) transaction is detected on the TZMP1 or TZMP2 data fields.
4	R.O	0x0	AXI_ERROR : // Activated when an AXI error is detected.
3	R.O	0x0	DETILING_ERROR : // Activated when a detiling error occurs.
2	R.O	0x0	DECODE_ERROR : // Activated when decoder core indicates a decoder error.
1	R.O	0x0	CONFIGURATION_SWAPPED : // Activated when configuration has been swapped from shadow registers to configuration registers.
0	R.O	0x0	SURFACES_COMPLETED : // Activated when all enabled surfaces have completed and have been fully read out. In continuous mode, this interrupt is triggered each time all surfaces have been read out.

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Table 9-2942 VPU_MAFBC_IRQ_CLEAR 0x3a02

Bit(s)	R/W	Default	Description
5	R/W	0	SECURE_ID_ERROR : // unsigned , default = 0,Writing a 1 to this bit clears the corresponding bit in the IRQ_RAW_STATUS register.
4	R/W	0	AXI_ERROR : // unsigned , default = 0,Writing a 1 to this bit clears the corresponding bit in the IRQ_RAW_STATUS register.
3	R/W	0	DETILING_ERROR : // unsigned , default = 0,Writing a 1 to this bit clears the corresponding bit in the IRQ_RAW_STATUS register.
2	R/W	0	DECODE_ERROR : // unsigned , default = 0,Writing a 1 to this bit clears the corresponding bit in the IRQ_RAW_STATUS register.
1	R/W	0	CONFIGURATION_SWAPPED : // unsigned , default = 0,Writing a 1 to this bit clears the corresponding bit in the IRQ_RAW_STATUS register.
0	R/W	0	SURFACES_COMPLETED : // unsigned , default = 0,Writing a 1 to this bit clears the corresponding bit in the IRQ_RAW_STATUS register.

Table 9-2943 VPU_MAFBC_IRQ_MASK 0x3a03

Bit(s)	R/W	Default	Description
5	R/W	0	SECURE_ID_ERROR : // unsigned , default = 0,When this is set to 1, the corresponding IRQ_RAW_STATUS interrupt is enabled. When this is set to zero, the corresponding IRQ_RAW_STATUS interrupt is disabled.
4	R/W	0	AXI_ERROR : // unsigned , default = 0,When this is set to 1, the corresponding IRQ_RAW_STATUS interrupt is enabled. When this is set to zero, the corresponding IRQ_RAW_STATUS interrupt is disabled.
3	R/W	0	DETILING_ERROR : // unsigned , default = 0,When this is set to 1, the corresponding IRQ_RAW_STATUS interrupt is enabled. When this is set to zero, the corresponding IRQ_RAW_STATUS interrupt is disabled.
2	R/W	0	DECODE_ERROR : // unsigned , default = 0, When this is set to 1, the corresponding IRQ_RAW_STATUS interrupt is enabled. When this is set to zero, the corresponding IRQ_RAW_STATUS interrupt is disabled.
1	R/W	0	CONFIGURATION_SWAPPED : // unsigned , default = 0, When this is set to 1, the corresponding IRQ_RAW_STATUS interrupt is enabled. When this is set to zero, the corresponding IRQ_RAW_STATUS interrupt is disabled.
0	R/W	0	SURFACES_COMPLETED : // unsigned , default = 0, When this is set to 1, the corresponding IRQ_RAW_STATUS interrupt is enabled. When this is set to zero, the corresponding IRQ_RAW_STATUS interrupt is disabled.

Table 9-2944 VPU_MAFBC_IRQ_STATUS 0x3a04

Bit(s)	R/W	Default	Description
5	R.O	0x0	SECURE_ID_ERROR : //When this is set to 1, it asserts the corresponding external interrupt. This signals an interruptrequest to the application processor.
4	R.O	0x0	AXI_ERROR : //When this is set to 1, it asserts the corresponding external interrupt. This signals an interruptrequest to the application processor.
3	R.O	0x0	DETILING_ERROR : //When this is set to 1, it asserts the corresponding external interrupt. This signals an interruptrequest to the application processor.
2	R.O	0x0	DECODE_ERROR : //When this is set to 1, it asserts the corresponding external interrupt. This signals an interruptrequest to the application processor.

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Bit(s)	R/W	Default	Description
1	R.O	0x0	CONFIGURATION_SWAPPED : //When this is set to 1, it asserts the corresponding external interrupt. This signals an interruptrequest to the application processor.
0	R.O	0x0	SURFACES_COMPLETED : //When this is set to 1, it asserts the corresponding external interrupt. This signals an interruptrequest to the application processor.

Table 9-2945 VPU_MAFBC_COMMAND 0x3a05

Bit(s)	R/W	Default	Description
1	R/W	0x0	PENDING_SWAP : //Performs a swap of shadow registers when the current decode operations are completed. After a swap,decoding of the new surfaces starts.
0	R/W	0x0	DIRECT_SWAP : //Performs a swap of shadow registers immediately.Current decode operations are terminated before completion . After termination, decoding of the new surfaces is started

Table 9-2946 VPU_MAFBC_STATUS 0x3a06

Bit(s)	R/W	Default	Description
2	R.O	0x0	ERROR : //When this is 1, it indicates that the AFBC decoder is in an unrecoverable state and must be reset using RESETn to continue operation. This is flagged after a DETILING_ERROR.
1	R.O	0x0	SWAPPING : //When this is 1, the AFBC decoder is swapping surface configurations.
0	R.O	0x0	ACTIVE : //When this is 1, the AFBC decoder is decoding surfaces.

Table 9-2947 VPU_MAFBC_SURFACE_CFG 0x3a07

Bit(s)	R/W	Default	Description
16	R/W	0	CONTINUOUS_DECODING_ENABLE : //unsigned , default = 0,Enables continuous decoding of surfaces when it is set to 1. This bit describes what the decoder does when one set of surfaces has been completed. If this is 1, the decoder immediately begins decoding again. In this case, the configuration for the next surface depends on whether the software has performed a swap operation. If no swap is used, the same configuration is used. If this is 0, the decoder waits for a software input.
3	R/W	0	S3_ENABLE : //unsigned , default = 0,When this is 1, surface 3 enabled.
2	R/W	0	S2_ENABLE : //unsigned , default = 0,When this is 1, surface 2 enabled.
1	R/W	0	S1_ENABLE : //unsigned , default = 0,When this is 1, surface 1 enabled.
0	R/W	0	S0_ENABLE : //unsigned , default = 0,When this is 1, surface 0 enabled.

Table 9-2948 VPU_MAFBC_AXI_CFG 0x3a08

Bit(s)	R/W	Default	Description
7:4	R/W	0	CACHE : //unsigned , default = 0,This value is driven on the ARCACHEM signal.
3:0	R/W	0	QOS : //unsigned , default = 0,This value is driven on the ARQOSM signal.

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Table 9-2949 VPU_MAFBC_HEADER_BUF_ADDR_LOW_S0 0x3a10

Bit(s)	R/W	Default	Description
31:0	R/W	0	HEADER_BUF_ADDR : [31:0] //unsigned , default = 0,Contains bits [31:0] of the header buffer address,Bits [5:0] must be set to 0 for alignment requirements.

Table 9-2950 VPU_MAFBC_HEADER_BUF_ADDR_HIGH_S0 0x3a11

Bit(s)	R/W	Default	Description
15:0	R/W	0	HEADER_BUF_ADDR : [47:32] //unsigned , default = 0,Contains the upper 16 bits of the header buffer address

Table 9-2951 VPU_MAFBC_FORMAT_SPECIFIER_S0 0x3a12

Bit(s)	R/W	Default	Description
19	R/W	0	PAYLOAD_LIMIT_EN : // unsigned , default = 0,Enable payload read address check against the min and max payload address boundaries: 0 Disable 1 Enable. This means that out-of-bound reads output the color black.
18	R/W	0	TILED_HEADER_EN : // unsigned , default = 0,Enables tiled header mode:0 Disable tiled header 1 Enable tiled header
17:16	R/W	0	SUPER_BLOCK_ASPECT : // unsigned , default = 0,Selects superblock aspect ratio 00:16x16 pixels 01:32x8 pixels other:reserved
9	R/W	0	BLOCK_SPLIT : //unsigned , default = 0,Enables block split mode: 0 Block split mode off. 1 Block split mode on.
8	R/W	0	YUV_TRANSFORM : //unsigned , default = 0,Enables the internal YUV transform stage: 0 Internal YUV transform off. 1 Internal YUV transform on.
3:0	R/W	0	PIXEL_FORMAT : //unsigned , default = 0,Contains the pixel format configuration.

Table 9-2952 VPU_MAFBC_BUFFER_WIDTH_S0 0x3a13

Bit(s)	R/W	Default	Description
13:0	R/W	0	BUFFER_WIDTH : //unsigned , default = 0,AFBC buffer width in pixels

Table 9-2953 VPU_MAFBC_BUFFER_HEIGHT_S0 0x3a14

Bit(s)	R/W	Default	Description
13:0	R/W	0	BUFFER_HEIGHT : //unsigned , default = 0,AFBC buffer height in pixels

Table 9-2954 VPU_MAFBC_BOUNDING_BOX_X_START_S0 0x3a15

Bit(s)	R/W	Default	Description
12:0	R/W	0	BUFFER_X_START : //unsigned , default = 0,The AFBC buffer bounding box minimum x value. Given in pixels.

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Table 9-2955 VPU_MAFBC_BOUNDING_BOX_X_END_S0 0x3a16

Bit(s)	R/W	Default	Description
12:0	R/W	0	BUFFER_X_START : //unsigned , default = 0,The AFBC buffer bounding box maximum x value. Given in pixels.

Table 9-2956 VPU_MAFBC_BOUNDING_BOX_Y_START_S0 0x3a17

Bit(s)	R/W	Default	Description
12:0	R/W	0	BUFFER_Y_START : //unsigned , default = 0,The AFBC buffer bounding box minimum y value. Given in pixels.

Table 9-2957 VPU_MAFBC_BOUNDING_BOX_Y_END_S0 0x3a18

Bit(s)	R/W	Default	Description
12:0	R/W	0	BUFFER_Y_START : //unsigned , default = 0,The AFBC buffer bounding box maximum y value. Given in pixels.

Table 9-2958 VPU_MAFBC_OUTPUT_BUF_ADDR_LOW_S0 0x3a19

Bit(s)	R/W	Default	Description
31:0	R/W	0	OUTPUT_BUF_ADDR : [31:0] //unsigned , default = 0,Contains bits [31:0] of the output buffer address.Bits [6:0] must be set to 0 for alignment requirements. The address, frame size, and pixel format allocate area in the detiler SRAM for the current surface . You must ensure that the allocated area does not exceed the available SRAM, or overlap with other surfaces or planes that are defined in the output buffer.

Table 9-2959 VPU_MAFBC_OUTPUT_BUF_ADDR_HIGH_S0 0x3a1a

Bit(s)	R/W	Default	Description
15:0	R/W	0x0	OUTPUT_BUF_ADDR : [47:32] //Contains the upper 16 bits of the output buffer address

Table 9-2960 VPU_MAFBC_OUTPUT_BUF_STRIDE_S0 0x3a1b

Bit(s)	R/W	Default	Description
15:0	R/W	0	OUTPUT_BUF_STRIDE : [15:0] //unsigned , default = 0,Contains bits [15:0] of the output buffer stride.Bits [6:0] must be set to 0 for alignment requirements. The maximum permitted buffer stride is 8192 pixels wide. The byte size depends on the pixel format for the surface.

Table 9-2961 VPU_MAFBC_PREFETCH_CFG_S0 0x3a1c

Bit(s)	R/W	Default	Description
1	R/W	0	PREFETCH_READ_DIRECTION_Y : // unsigned , default = 0,Defines the pre-fetch read direction in Y: 0 Top to bottom 1 Bottom to top
0	R/W	0	PREFETCH_READ_DIRECTION_X : //unsigned , default = 0,Defines the pre-fetch read direction in X 0 Left to righ 1 Right to left

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Table 9-2962 VPU_MAFBC_PAYLOAD_MIN_LOW_S0 0x3a1d

Bit(s)	R/W	Default	Description
31:0	R/W	0	PAYLOAD_MIN_LOW : //unsigned , default = 0, Indicates the lower 32 bits of the AFBC payload buffer minimum address.

Table 9-2963 VPU_MAFBC_PAYLOAD_MIN_HIGH_S0 0x3a1e

Bit(s)	R/W	Default	Description
15:0	R/W	0	PAYLOAD_MIN_HIGH : //unsigned , default = 0, Indicates the higher 16 bits of the AFBC payload buffer minimum address.

Table 9-2964 VPU_MAFBC_PAYLOAD_MAX_LOW_S0 0x3a1f

Bit(s)	R/W	Default	Description
31:0	R/W	0x0	PAYLOAD_MIN_LOW : //unsigned , ndicates the lower 32 bits of the AFBC payload buffer maximum address.

Table 9-2965 VPU_MAFBC_PAYLOAD_MAX_HIGH_S0 0x3a20

Bit(s)	R/W	Default	Description
15:0	R/W	0	PAYLOAD_MIN_HIGH : //unsigned , default = 0, Indicates the higher 16 bits of the AFBC payload buffer maximum address.

VPU_MAFBC_HEADER_BUF_ADDR_LOW_S1 0x3a30

See VPU_MAFBC_HEADER_BUF_ADDR_LOW_S0

VPU_MAFBC_HEADER_BUF_ADDR_HIGH_S1 0x3a31

See VPU_MAFBC_HEADER_BUF_ADDR_HIGH_S0

VPU_MAFBC_FORMAT_SPECIFIER_S1 0x3a32

See VPU_MAFBC_FORMAT_SPECIFIER_S0

VPU_MAFBC_BUFFER_WIDTH_S1 0x3a33

See VPU_MAFBC_BUFFER_WIDTH_S0

VPU_MAFBC_BUFFER_HEIGHT_S1 0x3a34

See VPU_MAFBC_BUFFER_HEIGHT_S0

VPU_MAFBC_BOUNDING_BOX_X_START_S1 0x3a35

See VPU_MAFBC_BOUNDING_BOX_X_START_S0

VPU_MAFBC_BOUNDING_BOX_X_END_S1 0x3a36

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See VPU_MAFBC_BOUNDING_BOX_X_END_S0

VPU_MAFBC_BOUNDING_BOX_Y_START_S1 0x3a37
See VPU_MAFBC_BOUNDING_BOX_Y_START_S0

VPU_MAFBC_BOUNDING_BOX_Y_END_S1 0x3a38
See VPU_MAFBC_BOUNDING_BOX_Y_END_S0

VPU_MAFBC_OUTPUT_BUF_ADDR_LOW_S1 0x3a39
See VPU_MAFBC_OUTPUT_BUF_ADDR_LOW_S0

VPU_MAFBC_OUTPUT_BUF_ADDR_HIGH_S1 0x3a3a
See VPU_MAFBC_OUTPUT_BUF_ADDR_HIGH_S0

VPU_MAFBC_OUTPUT_BUF_STRIDE_S1 0x3a3b
See VPU_MAFBC_OUTPUT_BUF_STRIDE_S0

VPU_MAFBC_PREFETCH_CFG_S1 0x3a3c
See VPU_MAFBC_PREFETCH_CFG_S0

VPU_MAFBC_PAYLOAD_MIN_LOW_S1 0x3a3d
See VPU_MAFBC_PAYLOAD_MIN_LOW_S0

VPU_MAFBC_PAYLOAD_MIN_HIGH_S1 0x3a3e
See VPU_MAFBC_PAYLOAD_MIN_HIGH_S0

VPU_MAFBC_PAYLOAD_MAX_LOW_S1 0x3a3f
See VPU_MAFBC_PAYLOAD_MAX_LOW_S0

VPU_MAFBC_PAYLOAD_MAX_HIGH_S1 0x3a40
See VPU_MAFBC_PAYLOAD_MAX_HIGH_S0

VPU_MAFBC_HEADER_BUF_ADDR_LOW_S2 0x3a50
See VPU_MAFBC_HEADER_BUF_ADDR_LOW_S0

VPU_MAFBC_HEADER_BUF_ADDR_HIGH_S2 0x3a51
See VPU_MAFBC_HEADER_BUF_ADDR_HIGH_S0

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VPU_MAFBC_FORMAT_SPECIFIER_S2 0x3a52
See VPU_MAFBC_FORMAT_SPECIFIER_S0

VPU_MAFBC_BUFFER_WIDTH_S2 0x3a53
See VPU_MAFBC_BUFFER_WIDTH_S0

VPU_MAFBC_BUFFER_HEIGHT_S2 0x3a54
See VPU_MAFBC_BUFFER_HEIGHT_S0

VPU_MAFBC_BOUNDING_BOX_X_START_S2 0x3a55
See VPU_MAFBC_BOUNDING_BOX_X_START_S0

VPU_MAFBC_BOUNDING_BOX_X_END_S2 0x3a56
See VPU_MAFBC_BOUNDING_BOX_X_END_S0

VPU_MAFBC_BOUNDING_BOX_Y_START_S2 0x3a57
See VPU_MAFBC_BOUNDING_BOX_Y_START_S0

VPU_MAFBC_BOUNDING_BOX_Y_END_S2 0x3a58
See VPU_MAFBC_BOUNDING_BOX_Y_END_S0

VPU_MAFBC_OUTPUT_BUF_ADDR_LOW_S2 0x3a59
See VPU_MAFBC_OUTPUT_BUF_ADDR_LOW_S0

VPU_MAFBC_OUTPUT_BUF_ADDR_HIGH_S2 0x3a5a
See VPU_MAFBC_OUTPUT_BUF_ADDR_HIGH_S0

VPU_MAFBC_OUTPUT_BUF_STRIDE_S2 0x3a5b
See VPU_MAFBC_OUTPUT_BUF_STRIDE_S0

VPU_MAFBC_PREFETCH_CFG_S2 0x3a5c
See VPU_MAFBC_PREFETCH_CFG_S0

VPU_MAFBC_PAYLOAD_MIN_LOW_S2 0x3a5d
See VPU_MAFBC_PAYLOAD_MIN_LOW_S0

VPU_MAFBC_PAYLOAD_MIN_HIGH_S2 0x3a5e
See VPU_MAFBC_PAYLOAD_MIN_HIGH_S0

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VPU_MAFBC_PAYLOAD_MAX_LOW_S2 0x3a5f
See VPU_MAFBC_PAYLOAD_MAX_LOW_S0

VPU_MAFBC_PAYLOAD_MAX_HIGH_S2 0x3a60
See VPU_MAFBC_PAYLOAD_MAX_HIGH_S0

VPU_MAFBC_HEADER_BUF_ADDR_LOW_S3 0x3a70
See VPU_MAFBC_HEADER_BUF_ADDR_LOW_S0

VPU_MAFBC_HEADER_BUF_ADDR_HIGH_S3 0x3a71
See VPU_MAFBC_HEADER_BUF_ADDR_HIGH_S0

VPU_MAFBC_FORMAT_SPECIFIER_S3 0x3a72
See VPU_MAFBC_FORMAT_SPECIFIER_S0

VPU_MAFBC_BUFFER_WIDTH_S3 0x3a73
See VPU_MAFBC_BUFFER_WIDTH_S0

VPU_MAFBC_BUFFER_HEIGHT_S3 0x3a74
See VPU_MAFBC_BUFFER_HEIGHT_S0

VPU_MAFBC_BOUNDING_BOX_X_START_S3 0x3a75
See VPU_MAFBC_BOUNDING_BOX_X_START_S0

VPU_MAFBC_BOUNDING_BOX_X_END_S3 0x3a76
See VPU_MAFBC_BOUNDING_BOX_X_END_S0

VPU_MAFBC_BOUNDING_BOX_Y_START_S3 0x3a77
See VPU_MAFBC_BOUNDING_BOX_Y_START_S0

VPU_MAFBC_BOUNDING_BOX_Y_END_S3 0x3a78
See VPU_MAFBC_BOUNDING_BOX_Y_END_S0

VPU_MAFBC_OUTPUT_BUF_ADDR_LOW_S3 0x3a79
See VPU_MAFBC_OUTPUT_BUF_ADDR_LOW_S0

VPU_MAFBC_OUTPUT_BUF_ADDR_HIGH_S3 0x3a7a

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See VPU_MAFBC_OUTPUT_BUF_ADDR_HIGH_S0

VPU_MAFBC_OUTPUT_BUF_STRIDE_S3 0x3a7b
See VPU_MAFBC_OUTPUT_BUF_STRIDE_S0

VPU_MAFBC_PREFETCH_CFG_S3 0x3a7c
See VPU_MAFBC_PREFETCH_CFG_S0

VPU_MAFBC_PAYLOAD_MIN_LOW_S3 0x3a7d
See VPU_MAFBC_PAYLOAD_MIN_LOW_S0

VPU_MAFBC_PAYLOAD_MIN_HIGH_S3 0x3a7e
See VPU_MAFBC_PAYLOAD_MIN_HIGH_S0

VPU_MAFBC_PAYLOAD_MAX_LOW_S3 0x3a7f
See VPU_MAFBC_PAYLOAD_MAX_LOW_S0

VPU_MAFBC_PAYLOAD_MAX_HIGH_S3 0x3a80
See VPU_MAFBC_PAYLOAD_MAX_HIGH_S0

9.2.3.47 Primesl Registers

Table 9-2966 PRIMESL_LUTC_ADDR_PORT 0x3980

Bit(s)	R/W	Default	Description
8: 0	R/W	0	lutc_addr : // unsigned , default = 0 = 'h0,

Table 9-2967 PRIMESL_LUTC_DATA_PORT 0x3981

Bit(s)	R/W	Default	Description
10: 0	R/W	0	lutc_data : // unsigned , default = 0 = 'h0,

Table 9-2968 PRIMESL_LUTP_ADDR_PORT 0x3982

Bit(s)	R/W	Default	Description
8: 0	R/W	0	lutp_addr : // unsigned , default = 0 = 'h0,

Table 9-2969 PRIMESL_LUTP_DATA_PORT 0x3983

Bit(s)	R/W	Default	Description
13: 0	R/W	0	lutp_data : // unsigned , default = 0 = 'h0,

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Table 9-2970 PRIMESL_LUTD_ADDR_PORT 0x3984

Bit(s)	R/W	Default	Description
8: 0	R/W	0	lutd_data : // unsigned , default = 0 = 'h0,

Table 9-2971 PRIMESL_LUTD_DATA_PORT 0x3985

Bit(s)	R/W	Default	Description
11: 0	R/W	0	lutd_data : // unsigned , default = 0 = 'h0,

Table 9-2972 PRIMESL_CTRL0 0x3990

Bit(s)	R/W	Default	Description
29	R/W	0	legacy_mode_en : // unsigned , default = 0 = 'h0
28	R/W	1	clip_en : // unsigned , default = 1 = 'h0
26:16	R/W	0	inv_chroma_ratio : // unsigned , default = 0 = 'h0,
14: 4	R/W	0	inv_y_ratio : // unsigned , default = 0 = 'h0,
3	R/W	0	reg_gclk_ctrl : // unsigned , default = 0 = 'h0,
2: 1	R/W	0	gclk_ctrl : // unsigned , default = 0 = 'h0,
0	R/W	1	primesl_en : // unsigned , default = 1 = 'h0,

Table 9-2973 PRIMESL_CTRL1 0x3991

Bit(s)	R/W	Default	Description
25:16	R/W	0	l_headroom : // unsigned , default = 0 = 'h0,
9: 0	R/W	0	footroom : // unsigned , default = 0 = 'h0,

Table 9-2974 PRIMESL_CTRL2 0x3992

Bit(s)	R/W	Default	Description
9: 0	R/W	0	c_headroom : // unsigned , default = 0 = 'h0,

Table 9-2975 PRIMESL_CTRL3 0x3993

Bit(s)	R/W	Default	Description
29:16	R/W	0	mub : // unsigned , default = 0 = 'h0,
13: 0	R/W	0	mua : // unsigned , default = 0 = 'h0,

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Table 9-2976 PRIMESL_CTRL4 0x3994

Bit(s)	R/W	Default	Description
25:16	R/W	0	oct_7_1 : // signed , default = 0 = 'h0,
9: 0	R/W	0	oct_7_0 : // signed , default = 0 = 'h0,

Table 9-2977 PRIMESL_CTRL5 0x3995

Bit(s)	R/W	Default	Description
25:16	R/W	0	oct_7_3 : // signed , default = 0 = 'h0,
9: 0	R/W	0	oct_7_2 : // signed , default = 0 = 'h0,

Table 9-2978 PRIMESL_CTRL6 0x3996

Bit(s)	R/W	Default	Description
25:16	R/W		oct_7_5 : // signed , default = 0 = 'h0,
9: 0	R/W		oct_7_4 : // signed , default = 0 = 'h0,

Table 9-2979 PRIMESL_CTRL7 0x3997

Bit(s)	R/W	Default	Description
9: 0	R/W	0	oct_7_6 : // signed , default = 0 = 'h0,

Table 9-2980 PRIMESL_CTRL8 0x3998

Bit(s)	R/W	Default	Description
28:16	R/W	0	d_lut_threshold_3_1 : // unsigned , default = 0 = 'h0,
12: 0	R/W	0	d_lut_threshold_3_0 : // unsigned , default = 0 = 'h0,

Table 9-2981 PRIMESL_CTRL9 0x3999

Bit(s)	R/W	Default	Description
12: 0	R/W	0	d_lut_threshold_3_2 : // unsigned , default = 0 = 'h0,

Table 9-2982 PRIMESL_CTRL10 0x399a

Bit(s)	R/W	Default	Description
15:12	R/W	0	d_lut_step_4_3 : // unsigned , default = 0 = 'h0,
11: 8	R/W	0	d_lut_step_4_2 : // unsigned , default = 0 = 'h0,
7: 4	R/W	0	d_lut_step_4_1 : // unsigned , default = 0 = 'h0,
3: 0	R/W	0	d_lut_step_4_0 : // unsigned , default = 0 = 'h0,

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Table 9-2983 PRIMESL_CTRL11 0x399b

Bit(s)	R/W	Default	Description
28:16	R/W	0	rgb2yuv_9_0 : // signed , default = 0 = 'h0,
12: 0	R/W	0	rgb2yuv_9_1 : // signed , default = 0 = 'h0,

Table 9-2984 PRIMESL_CTRL12 0x399c

Bit(s)	R/W	Default	Description
28:16	R/W	0	rgb2yuv_9_2 : // signed , default = 0 = 'h0,
12: 0	R/W	0	rgb2yuv_9_3 : // signed , default = 0 = 'h0,

Table 9-2985 PRIMESL_CTRL13 0x399d

Bit(s)	R/W	Default	Description
28:16	R/W	0	rgb2yuv_9_4 : // signed , default = 0 = 'h0,
12: 0	R/W	0	rgb2yuv_9_5 : // signed , default = 0 = 'h0,

Table 9-2986 PRIMESL_CTRL14 0x399e

Bit(s)	R/W	Default	Description
28:16	R/W	0	rgb2yuv_9_6 : // signed , default = 0 = 'h0,
12: 0	R/W	0	rgb2yuv_9_7 : // signed , default = 0 = 'h0,

Table 9-2987 PRIMESL_CTRL15 0x399f

Bit(s)	R/W	Default	Description
12: 0	R/W	0	rgb2yuv_9_8 : // signed , default = 0 = 'h0,

Table 9-2988 PRIMESL_CTRL16 0x39e0

Bit(s)	R/W	Default	Description
31	R/W	0	reserved
30	R/W	0	byp_s_lut://unsigned
29	R/W	0	byp_d_lut://unsigned
28	R/W	0	byp_mat://unsigned
27	R/W	0	rgb_swap://unsigned
26:24	R/W	0	uv_shift://unsigned
23:22	R/W	0	rgb_shift://unsigned
21:20	R/W	3	rgb_clip://unsigned
19:18	R/W	/	reserved
17:16	R/W	0	rgb_s://unsigned

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Bit(s)	R/W	Default	Description
15:14	R/W	/	reserved
13:0	R/W	1024	reg_s://signed

Table 9-2989 PRIMESL_OMAT_OFFSET0 0x39e1

Bit(s)	R/W	Default	Description
31:28	R/W	/	reserved
27:16	R/W	512	pre_offset0// unsigned , default = 0 = 512,
15:12	R/W	/	reserved
11: 0	R/W	512	pre_offset1: // unsigned , default = 0 = 512,

Table 9-2990 PRIMESL_OMAT_OFFSET1 0x39e2

Bit(s)	R/W	Default	Description
31:28	R/W	/	reserved
27:16	R/W	512	pre_offset2// unsigned , default = 0 = 512,
15:12	R/W	/	reserved
11: 0	R/W	256	Offset0: // unsigned , default = 0 = 512,

Table 9-2991 PRIMESL_OMAT_OFFSET2 0x39e3

Bit(s)	R/W	Default	Description
31:28	R/W	/	reserved
27:16	R/W	2048	offset1// unsigned , default = 0 = 512,
15:12	R/W	/	reserved
11: 0	R/W	2048	offset2: // unsigned , default = 0 = 512,

9.2.3.48 VADJ1/RGB_CONBRI Registers

Table 9-2992 VPP_VADJ1_MISC 0x3280

Bit(s)	R/W	Default	Description
5:4	R/W	0	Gate clk ctrl for vadj1
3	/	/	/
2	R/W	0	Sync enable 1:vadj1 regs work when go_field come 1:vadj1 regs directly
1	R/W	0	minus black level enable for vadj1
0	R/W	0	Module enable

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Table 9-2993 VPP_VADJ1_BLACK_VAL 0X3281

Bit(s)	R/W	Default	Description
26:16	R/W	13'h200	Black_luma
10:0	R/W	13'h40	Black_chroma

Table 9-2994 VPP_VADJ1_Y 0x3282

Bit(s)	R/W	Default	Description
18-8	R/W	0	brightness, signed value
7-0	R/W	0x1d0	contrast, unsigned value, contrast from 0 <= contrast <2

cb' = cb*ma + cr*mb

cr' = cb*mc + cr*md

Table 9-2995 VPP_VADJ1_MA_MB 0x3283

Bit(s)	R/W	Default	Description
25-16	R/W	0x100	MA, signed value, -2 < MA < 2
9-0	R/W	0	MB, signed value ,-2 < MB < 2

Table 9-2996 VPP_VADJ1_MC_MD 0x3284

Bit(s)	R/W	Default	Description
25-16	R/W	0	MC, signed value, -2 < MC < 2
9-0	R/W	0x100	MD, signed value ,-2 < MD < 2

Table 9-2997 VPP_VADJ1_CURV_0 0x3285

Bit(s)	R/W	Default	Description
31:24	R/W	0	vadj1_softcon_curv0_ci, u8
23:12	R/W	0	vadj1_softcon_curv0_b, u12
11:0	R/W	0	vadj1_softcon_curv0_a, s12

Table 9-2998 VPP_VADJ1_CURV_1 0x3286

Bit(s)	R/W	Default	Description
31:13			Reserved
12:4	R/W	0	vadj1_softcon_curv0_g, s9
3			Reserved
2:0	R/W	0	vadj1_softcon_curv0_cs, u3

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Table 9-2999 VPP_VADJ1_CURV_2 0x3287

Bit(s)	R/W	Default	Description
31:24	R/W	0	vadj1_softcon_curv1_ci, u8
23:12	R/W	0	vadj1_softcon_curv1_b, u12
11:0	R/W	0	vadj1_softcon_curv1_a, s12

Table 9-3000 VPP_VADJ1_CURV_3 0x3288

Bit(s)	R/W	Default	Description
31:13			Reserved
12:4	R/W	0	vadj1_softcon_curv1_g, s9
3			Reserved
2:0	R/W	0	vadj1_softcon_curv1_cs, u3

Table 9-3001 VPP_VD1_RGB_CTRST 0x3289

Bit(s)	R/W	Default	Description
31:28			Reserved
27:16	R/W	1024	Vd1_rgb_ctrst: contrast for rgb, normalized 1024 as ‘1.0’
15			Reserved
14:2	R/W	64	Vd1_rgb_ctrst_blklvl: contrast black level to be subtract before and add back after the contrast gain operation
1	R/W	0	Vd1_rgbbst_en: 1 to enable the RGB_BST
0	R/W	1	Vd1_rgb_ctrst_prt: enable signal to protect saturation in rgb (no clipping) during contrast adjustment

Table 9-3002 VPP_VD1_RGB_BRGHT 0x328A

Bit(s)	R/W	Default	Description
31:14			Reserved
13:2	R/W	0	Vd1_rgb_brght: brightness level in rgb domain
1	R/W	1	Vd1_rgb_brght_prt: enable signal to protect saturation in rgb (no clipping) during brightness adjustment
0	R/W	0	Vd1_rgb_ctrst_dlut_x2: Enable signal to do x2 to the dlut cells before subtracting from the normalized gain_max; 0:x1 1:x2

Table 9-3003 VPP_VD1_RGB_DLUT_0_3 0x328B

Bit(s)	R/W	Default	Description
31:24	R/W	255	Vd1_rgbbst_dlut0: Differential gain to normalized gain_max to customized protection curve. e.g. [255 205 171 147 128 113 102 93 85 78 73 68] for protection of not boost for pixels larger than 240
23:16	R/W	205	Vd1_rgbbst_dlut1: same as Vd1_rgbbst_dlut0

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Bit(s)	R/W	Default	Description
15:8	R/W	171	Vd1_rgbbst_dlut2: same as Vd1_rgbbst_dlut0
7:0	R/W	147	Vd1_rgbbst_dlut3: same as Vd1_rgbbst_dlut0

Table 9-3004 VPP_VD1_RGB_DLUT_4_7 0x328c

Bit(s)	R/W	Default	Description
31:24	R/W	128	Vd1_rgbbst_dlut4: same as Vd1_rgbbst_dlut0
23:16	R/W	113	Vd1_rgbbst_dlut5: same as Vd1_rgbbst_dlut0
15:8	R/W	102	Vd1_rgbbst_dlut6: same as Vd1_rgbbst_dlut0
7:0	R/W	93	Vd1_rgbbst_dlut7: same as Vd1_rgbbst_dlut0

Table 9-3005 VPP_VD1_RGB_DLUT_8_11 0x328d

Bit(s)	R/W	Default	Description
31:24	R/W	85	Vd1_rgbbst_dlut8: same as Vd1_rgbbst_dlut0
23:16	R/W	78	Vd1_rgbbst_dlut9: same as Vd1_rgbbst_dlut0
15:8	R/W	73	Vd1_rgbbst_dlut10: same as Vd1_rgbbst_dlut0
7:0	R/W	68	Vd1_rgbbst_dlut11: same as Vd1_rgbbst_dlut0

Table 9-3006 VPP_VADJ2_MISC 0x32a0

Bit(s)	R/W	Default	Description
5:4	R/W	0	Gate clk ctrl for vadj2
3	/	/	/
2	R/W	0	Sync enable 1:vadj2 regs work when go_field come 1:vadj2 regs directly
1	R/W	0	minus black level enable for vadj2
0	R/W	0	Module enable

Table 9-3007 VPP_VADJ2_BLACK_VAL 0X32a1

Bit(s)	R/W	Default	Description
26:16	R/W	13'h200	Black_luma
10:0	R/W	13'h40	Black_chroma

Table 9-3008 VPP_VADJ2_Y 0x32a2

Bit(s)	R/W	Default	Description
18-8	R/W	0	brightness, signed value
7-0	R/W	0x1d0	contrast, unsigned value, contrast from 0 <= contrast <2

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cb' = cb*ma + cr*mb

cr' = cb*mc + cr*md

Table 9-3009 VPP_VADJ2_MA_MB 0x32a3

Bit(s)	R/W	Default	Description
25-16	R/W	0x100	MA, signed value, -2 < MA < 2
9-0	R/W	0	MB, signed value ,-2 < MB < 2

Table 9-3010 VPP_VADJ2_MC_MD 0x32a4

Bit(s)	R/W	Default	Description
25-16	R/W	0	MC, signed value, -2 < MC < 2
9-0	R/W	0x100	MD, signed value ,-2 < MD < 2

Table 9-3011 VPP_VADJ2_CURV_0 0x32a5

Bit(s)	R/W	Default	Description
31:24	R/W	0	Vadj2_softcon_curv0_ci, u8
23:12	R/W	0	Vadj2_softcon_curv0_b, u12
11:0	R/W	0	Vadj2_softcon_curv0_a, s12

Table 9-3012 VPP_VADJ2_CURV_1 0x32a6

Bit(s)	R/W	Default	Description
31:13			Reserved
12:4	R/W	0	Vadj2_softcon_curv0_g, s9
3			Reserved
2:0	R/W	0	Vadj2_softcon_curv0_cs, u3

Table 9-3013 VPP_VADJ2_CURV_2 0x32a7

Bit(s)	R/W	Default	Description
31:24	R/W	0	Vadj2_softcon_curv1_ci, u8
23:12	R/W	0	Vadj2_softcon_curv1_b, u12
11:0	R/W	0	Vadj2_softcon_curv1_a, s12

Table 9-3014 VPP_VADJ2_CURV_3 0x32a8

Bit(s)	R/W	Default	Description
31:13			Reserved
12:4	R/W	0	Vadj2_softcon_curv1_g, s9

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Bit(s)	R/W	Default	Description
3			Reserved
2:0	R/W	0	Vadj2_softcon_curv1_cs, u3

Table 9-3015 VPP_POST_RGB_CTRST 0x32a9

Bit(s)	R/W	Default	Description
31:28			Reserved
27:16	R/W	1024	Post_rgb_ctrst: contrast for rgb, normalized 1024 as ‘1.0’
15:12			Reserved
11:2	R/W	64	Post_rgb_ctrst_blklvl: contrast black level to be subtract before and add back after the contrast gain operation
1	R/W	0	Post_rgbbst_en: 1 to enable the RGB_BST
0	R/W	1	Post_rgb_ctrst_prt: enable signal to protect saturation in rgb (no clipping) during contrast adjustment

Table 9-3016 VPP_POST_RGB_BRGHT 0x32aa

Bit(s)	R/W	Default	Description
31:14			Reserved
13:2	R/W	0	Post_rgb_brght: brightness level in rgb domain
1	R/W	1	Post_rgb_brght_prt: enable signal to protect saturation in rgb (no clipping) during brightness adjustment
0	R/W	0	Post_rgb_ctrst_dlut_x2: Enable signal to do x2 to the dlut cells before subtracting from the normalized gain_max; 0:x1 1:x2

Table 9-3017 VPP_POST_RGB_DLUT_0_3 0x32ab

Bit(s)	R/W	Default	Description
31:24	R/W	255	Post_rgbbst_dlut0: Differential gain to normalized gain_max to customized protection curve. e.g. [255 205 171 147 128 113 102 93 85 78 73 68] for protection of not boost for pixels larger than 240
23:16	R/W	205	Post_rgbbst_dlut1: same as Post_rgbbst_dlut0
15:8	R/W	171	Post_rgbbst_dlut2: same as Post_rgbbst_dlut0
7:0	R/W	147	Post_rgbbst_dlut3: same as Post_rgbbst_dlut0

Table 9-3018 VPP_POST_RGB_DLUT_4_7 0x32ac

Bit(s)	R/W	Default	Description
31:24	R/W	128	Post _rgbbst_dlut4: same as Post_rgbbst_dlut0
23:16	R/W	113	Post _rgbbst_dlut5: same as Post_rgbbst_dlut0
15:8	R/W	102	Post _rgbbst_dlut6: same as Post_rgbbst_dlut0
7:0	R/W	93	Post _rgbbst_dlut7: same as Post_rgbbst_dlut0

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Table 9-3019 VPP_POST_RGB_DLUT_8_11 0x32ad

Bit(s)	R/W	Default	Description
31:24	R/W	85	Post_rgbbst_dlut8: same as Post_rgbbst_dlut0
23:16	R/W	78	Post_rgbbst_dlut9: same as Post_rgbbst_dlut0
15:8	R/W	73	Post_rgbbst_dlut10: same as Post_rgbbst_dlut0
7:0	R/W	68	Post_rgbbst_dlut11: same as Post_rgbbst_dlut0

Table 9-3020 VPP_POST_MATRIX_SAT 0x32c1

Bit(s)	R/W	Default	Description
2	R/W	85	Sato_en
1	R/W	78	Sati_en
0	R/W	73	Misc_sat_en

9.2.3.49 3D LUT Registers

Table 9-3021 3D LUT VPP_LUT3D_CTRL 0x39d0

Bit(s)	R/W	Default	Description
9:8	R/W	0	Gated clock control
7	R/W		reserved
6:4	R/W		reg_lut3d_extnd_en: enable to set LUT value of 1023 to value 1024.
3	R/W		reserved
2	R/W	0	1 to shaddow the “reg_lut3d_enable” by VSYNC
1	R/W		reserved
0	R/W	0	reg_lut3d_enable: 1 to enable 3D LUT

Table 9-3022 VPP_LUT3D_CBUS2RAM_CTRL 0x39d1

Bit(s)	R/W	Default	Description
0	R/W	0	1 to enable CBUS to configure the LUT3D RAMs, 0 for in normal working status.

Table 9-3023 VPP_LUT3D_RAM_ADDR 0x39d2

Bit(s)	R/W	Default	Description
32	R/W	0	LUT3D RAMs Address port

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Table 9-3024 VPP_LUT3D_RAM_DATA 0x39d3

Bit(s)	R/W	Default	Description
32	R/W	0	LUT3D RAMs data port

9.2.3.50 HDMITX Registers

9.2.3.50.1 Register Access

Accessing HDMITX Top-Level and TX Controller IP registers is by directly accessing memory addresses. Due to the difference between the data width of Top-level register and IP register – Top-level 4-byte wide and IP register 1-byte wide, below list the correct ways to access Top-level registers.

Top-level Registers Access

```
#define HDMITX_TOP_BASE_OFFSET0xfe308000
#define HDMITX_TOP_REVOCMEM_ADDR_S0x2000
#define HDMITX_TOP_REVOCMEM_ADDR_E0x365E

void hdmitx_wr_only_TOP (uint32_t addr, uint32_t data) {
if ((addr >= HDMITX_TOP_REVOCMEM_ADDR_S) &&
     (addr <= HDMITX_TOP_REVOCMEM_ADDR_E)) {
        *(volatile uint8_t *)(HDMITX_TOP_BASE_OFFSET+addr) = (uint8_t)(data&0xff);
    } else {
        *(volatile uint32_t *)(HDMITX_TOP_BASE_OFFSET+addr) = (data);
    }
}

uint32_t hdmitx_rd_TOP (uint32_t addr) {
    uint32_t     data;
if ((addr >= HDMITX_TOP_REVOCMEM_ADDR_S) &&
     (addr <= HDMITX_TOP_REVOCMEM_ADDR_E)) {
        data = (uint32_t)(*(volatile uint8_t *)(HDMITX_TOP_BASE_OFFSET+addr));
    } else {
        data = *(volatile uint32_t *)(HDMITX_TOP_BASE_OFFSET+addr);
    }
    return (data);
}
```

HDCP2.2 IP Register Access

Table 9-3025 HDCP2.2 IP register base address

Absolute Address	Address Mnemonic	Description
0xfe032000	ELP_ESM_HPI_REG_BASE	Address base to HDCP2.2 IP register access.

To write to an HDCP2.2 IP register:

*((volatile uint32_t *) (ELP_ESM_HPI_REG_BASE+addr)) = data;

To read from an HDCP2.2 IP register:

data = *((volatile uint32_t *) (ELP_ESM_HPI_REG_BASE+addr));

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9.2.3.50.2 Top-Level Register Description

Table 9-3026 HDMITX Top-Level Registers

Addr	Name	RW	Function
0x000<<2	HDMITX_TOP_SW_RESET	RW	Software reset sub-modules.
0x001<<2	HDMITX_TOP_CLK_CNTL	RW	Clock gating and inversion.
0x002<<2	HDMITX_TOP_HPD_FILTER	RW	HPD and RxSense input glitch filter.
0x003<<2	HDMITX_TOP_INTR_MASKN	RW	Interrupt mask.
0x004<<2	HDMITX_TOP_INTR_STAT	RW	Interrupt status.
0x005<<2	HDMITX_TOP_INTR_STAT_CLR	W	Interrupt clear.
0x006<<2	HDMITX_TOP_BIST_CNTL	RW	Build-In Self Test(BIST) control.
0x007<<2	HDMITX_TOP_SHIFT_PTTN_012	RW	Shift pattern for BIST.
0x008<<2	HDMITX_TOP_SHIFT_PTTN_345	RW	Shift pattern for BIST.
0x009<<2	HDMITX_TOP_SHIFT_PTTN_67	RW	Shift pattern for BIST.
0x00A<<2	HDMITX_TOP_TMDS_CLK_PTTN_01	RW	TMDS clock pattern for generating /10 or /40 rate clock.
0x00B<<2	HDMITX_TOP_TMDS_CLK_PTTN_23	RW	TMDS clock pattern for generating /10 or /40 rate clock.
0x00C<<2	HDMITX_TOP_TMDS_CLK_PTTN_CNTL	RW	TMDS clock pattern for generating /10 or /40 rate clock.
0x00D<<2	HDMITX_TOP_REVOCMEM_STAT	RW	Revocmem status
0x00E<<2	HDMITX_TOP_STAT0	RW	Status.
0x010<<2	HDMITX_TOP_SKP_CNTL_STAT	RW	SKP interface control for HDCP2.2.
0x015<<2	HDMITX_TOP_PKF_0	W	PKF[31:0] for HDCP2.2.
0x016<<2	HDMITX_TOP_PKF_1	W	PKF[63:32] for HDCP2.2.
0x017<<2	HDMITX_TOP_PKF_2	W	PKF[95:64] for HDCP2.2.
0x018<<2	HDMITX_TOP_PKF_3	W	PKF[127:96] for HDCP2.2.
0x019<<2	HDMITX_TOP_DUK_0	W	DUK [31:0] for HDCP2.2.
0x01A<<2	HDMITX_TOP_DUK_1	W	DUK [63:32] for HDCP2.2.
0x01B<<2	HDMITX_TOP_DUK_2	W	DUK [95:64] for HDCP2.2.
0x01C<<2	HDMITX_TOP_DUK_3	W	DUK [127:96] for HDCP2.2.
0x01D<<2	HDMITX_TOP_INFILTER	RW	DDC and CEC input glitch filter control.
0x01E<<2	HDMITX_TOP_NSEC_SCRATCH	RW	Scratch register for non-secure access.
0x01F<<2	HDMITX_TOP_SEC_SCRATCH	RW	Scratch register for secure access.
0x020<<2	HDMITX_TOP_EMP_CNTL0	RW	EMP control.
0x021<<2	HDMITX_TOP_EMP_CNTL1	RW	EMP control.
0x022<<2	HDMITX_TOP_EMP_MEMADDR_START	RW	Mem addr pointer for EMP.
0x023<<2	HDMITX_TOP_EMP_STAT0	R	EMP status.

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Addr	Name	RW	Function
0x024<<2	HDMITX_TOP_EMP_STAT1	R	EMP status.
0x025<<2	HDMITX_TOP_AXI_ASYNC_ CNTL0	RW	AXI async control.
0x026<<2	HDMITX_TOP_AXI_ASYNC_ CNTL1	RW	AXI async control.
0x027<<2	HDMITX_TOP_AXI_ASYNC_STAT0	R	AXI async status.
0x028<<2	HDMITX_TOP_I2C_BUSY_CNT_ MAX	RW	Max I2C idle time after I2C Start.
0x029<<2	HDMITX_TOP_I2C_BUSY_CNT_ STAT	RW	I2C idle time status.
0x02A<<2	HDMITX_TOP_HDCP22_BSOD	RW	HDCP22 BSOD override control.
0x02B<<2	HDMITX_TOP_DDC_CNTL	RW	DDC pull down by SW.
0x030<<2	HDMITX_TOP_DISABLE_NULL	RW	NULL packet disable control.
0x031<<2	HDMITX_TOP_HDCP14_ UNENCRYPT	RW	Programmable color for HDCP1.4 unencrypt state
0x032<<2	HDMITX_TOP_MISC_CNTL	RW	Misc control.
0x033<<2	HDMITX_TOP_SEC_VIDEO_OVR	RW	Secure video protect.
0x034<<2	HDMITX_TOP_HDCP14_MIN_SIZE	RW	Secure video protect.
0x035<<2	HDMITX_TOP_HDCP22_MIN_SIZE	RW	Secure video protect.
0x033<<2	HDMITX_TOP_SEC_VIDEO_OVR	RW	Secure video protect.
0x034<<2	HDMITX_TOP_HDCP14_MIN_SIZE	RW	Secure video protect.
0x035<<2	HDMITX_TOP_HDCP22_MIN_SIZE	RW	Secure video protect.
0x033<<2	HDMITX_TOP_SEC_VIDEO_OVR	RW	Secure video protect.
0x034<<2	HDMITX_TOP_HDCP14_MIN_SIZE	RW	Secure video protect.
0x035<<2	HDMITX_TOP_HDCP22_MIN_SIZE	RW	Secure video protect.
0x2000	HDMITX_TOP_REVOCMEM_ ADDR_S	RW	Map to DWC internal Revoc MEM start address.
0x365E	HDMITX_TOP_REVOCMEM_ ADDR_E	RW	Map to DWC internal Revoc MEM end address.

Table 9-3027 HDMITX_TOP_SW_RESET

Bit	R/W	Default	Description
31:8	R	0	Reserved
15:10	RW	0x3f	Reserved
9	RW	0	sw_reset_i2c: to reset DWC IP's I2C module. 0=Release from reset; 1=Apply reset.
8	RW	1	sw_reset_axiarb: to reset AXI arbitor. 0=Release from reset; 1=Apply reset.
7	RW	1	sw_reset_emp: to reset EMP block. 0=Release from reset;

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Bit	R/W	Default	Description
			1=Apply reset.
6	RW	1	sw_reset_flt: to reset DDC&CEC input glitch filter. 0=Release from reset; 1=Apply reset.
5	RW	1	sw_reset_hdcp22: to reset HDCP2.2 IP. 0=Release from reset; 1=Apply reset.
4	RW	1	sw_reset_phyif: to reset PHY interface. 0=Release from reset; 1=Apply reset.
3	RW	1	sw_reset_intr: to reset interrupt block. 0=Release from reset; 1=Apply reset.
2	RW	1	sw_reset_mem: to reset KSV/REVOC mem. 0=Release from reset; 1=Apply reset.
1	RW	1	sw_reset_rnd: to reset random number interface to HDCP. 0=Release from reset; 1=Apply reset.
0	RW	1	sw_reset_core: To reset TX Controller IP. 0=Release from reset; 1=Apply reset.

Table 9-3028 HDMITX_TOP_CLK_CNTL

Bit	R/W	Default	Description
31	RW	0	free_clk_en: 0= Enable clock gating for power saving; 1= Disable clock gating, enable free-run clock.
30:14	RW	0	Reserved
13	RW	0	axi_clk_en: 1= Enable axi_clk.
12	RW	0	i2s_ws_inv: 1= Invert i2s_ws.
11	RW	0	i2s_clk_inv: 1= Invert i2s_clk.
10	RW	0	spdif_clk_inv: 1= Invert spdif_clk.
9	RW	0	tmds_clk_inv: 1= Invert tmds_clk.
8	RW	0	pixel_clk_inv: 1= Invert pixel_clk.
7	RW	0	hdcp22_skpclk_en: 1= Enable skpclk to HTX_HDCP2.2 IP.
6	RW	0	hdcp22_esmclk_en: 1= Enable esmclk to HTX_HDCP2.2 IP.
5	RW	0	hdcp22_tmdsclk_en: 1= Enable tmds_clk to HDCP2.2 IP.

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Bit	R/W	Default	Description
4	RW	0	Reserved.
3	RW	0	i2s_clk_en: 1= Enable i2s_clk.
2	RW	0	spdif_clk_en: 1= Enable spdif_clk.
1	RW	0	tmds_clk_en: 1= Enable tmds_clk.
0	RW	0	pixel_clk_en: 1= Enable pixel_clk.

Table 9-3029 HDMITX_TOP_HPD_FILTER

Bit	R/W	Default	Description
31:16	R	0	Reserved
31:28	RW	0	rxsense_glitch_width: Filter out glitch <= rxsense_glitch_width.
27:16	RW	0	rxsense_valid_width: Filter out width <= rxsense_valid_width * 1024.
15:12	RW	0	hpd_glitch_width: Filter out glitch <= hpd_glitch_width.
11:0	RW	0	hpd_valid_width: Filter out width <= hpd_valid_width * 1024.

Note

Interrupt MASKN, one bit per interrupt source.

- 0= Disable interrupt source;
- 1= Enable interrupt source.

Table 9-3030 HDMITX_TOP_INTR_MASKN

Bit	R/W	Default	Description
31:9	R	0	Reserved
8	RW	0	hdcp_topology_err
7	RW	0	rxsense_fall
6	RW	0	rxsense_rise
5	RW	0	err_i2c_timeout
4	RW	0	hdcp22_rndnum_err
3	RW	0	nonce_rfrsh_rise
2	RW	0	hpd_fall
1	RW	0	hpd_rise
0	RW	0	TX Controller IP interrupt.

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Note

Interrupt status. For each bit of bit[8:0], write 1 to manually set the interrupt bit, read back the interrupt status.

Table 9-3031 HDMITX_TOP_INTR_STAT

Bit	R/W	Default	Description
31	R	0	Shadowing TX Controller IP interrupt status flag.
30	R	0	Shadowing HDCP2.2 IP interrupt status flag.
29:9	R	0	Reserved
8	RW	0	hdcp_topology_err
7	RW	0	rxsense_fall
6	RW	0	rxsense_rise
5	RW	0	err_i2c_timeout
4	RW	0	hdcp22_rndnum_err
3	RW	0	nonce_rfrsh_rise
2	RW	0	hpd_fall
1	RW	0	hpd_rise
0	RW	0	TX Controller IP interrupt.

Note

↓ Interrupt status clear. For each bit, write 1 to clear the interrupt bit.

Table 9-3032 HDMITX_TOP_INTR_STAT_CLR

Bit	R/W	Default	Description
31:9	R	0	Reserved
8	W	0	hdcp_topology_err
7	W	0	rxsense_fall
6	W	0	rxsense_rise
5	W	0	err_i2c_timeout
4	W	0	hdcp22_rndnum_err
3	W	0	nonce_rfrsh_rise
2	W	0	hpd_fall
1	W	0	hpd_rise
0	W	0	TX Controller IP interrupt.

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Table 9-3033 HDMITX_TOP_BIST_CNTL

Bit	R/W	Default	Description
31:16	R	0	Reserved
15	RW	0	Reserved
14:12	RW	0	tmds_sel: 3'b000=Output zero; 3'b001=Output normal TMDS data; 3'b010=Output PRBS data; 3'b100=Output shift pattern.
11: 9	RW	0	shift_pttn_repeat: 0=New pattern every clk cycle; 1=New pattern every 2 clk cycles; ...; 7=New pattern every 8 clk cycles.
8	RW	0	shift_pttn_en: 1= Eanble shift pattern generator; 0=Disable.
7:5	RW	0	Reserved
4: 3	RW	0	prbs_pttn_mode: 0=PRBS11; 1=PRBS15; 2=PRBS7; 3=PRBS31.
2:1	RW	0	prbs_pttn_width: 0=Idle; 1=Output 8-bit pattern; 2=Output 1-bit pattern; 3=Output 10-bit pattern.
0	RW	0	prbs_pttn_en: 1=Enable PRBS generator; 0=Disable.

Table 9-3034 HDMITX_TOP_SHIFT_PTTN_012

Bit	R/W	Default	Description
31:30	R	0	Reserved
29:20	RW	0	shift_pttn_data[59:50].
19:10	RW	0	shift_pttn_data[69:60].
9:0	RW	0	shift_pttn_data[79:70].

Table 9-3035 HDMITX_TOP_SHIFT_PTTN_345

Bit	R/W	Default	Description
31:30	R	0	Reserved
29:20	RW	0	shift_pttn_data[29:20].
19:10	RW	0	shift_pttn_data[39:30].
9:0	RW	0	shift_pttn_data[49:40].

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Table 9-3036 HDMITX_TOP_SHIFT_PTTN_67

Bit	R/W	Default	Description
31:20	R	0	Reserved
19:10	RW	0	shift_pttn_data[9:0].
9:0	RW	0	shift_pttn_data[19:10].

Table 9-3037 HDMITX_TOP_TMDS_CLK_PTTN_01

Bit	R/W	Default	Description
31:26	R	0	Reserved
25:16	RW	0	tmds_clk_pttn[19:10].
15:10	R	0	Reserved
9:0	RW	0	tmds_clk_pttn[9:0].

Table 9-3038 HDMITX_TOP_TMDS_CLK_PTTN_23

Bit	R/W	Default	Description
31:26	R	0	Reserved
25:16	RW	0	tmds_clk_pttn[39:30].
15:10	R	0	Reserved
9:0	RW	0	tmds_clk_pttn[29:20].

Table 9-3039 HDMITX_TOP_TMDS_CLK_PTTN_CNTL

Bit	R/W	Default	Description
31:2	R	0	Reserved
1	RW	0	shift_tmds_clk_pttn: 1=Enable shifting clk pattern, used when TMDS CLK rate = TMDS character rate /4.
0	W	0	load_tmds_clk_pttn: Write this bit to 1 to load tmds_clk_pttn to HW. Always read back 0.

Table 9-3040 HDMITX_TOP_REVOCMEM_STAT

Bit	R/W	Default	Description
31:2	R	0	Reserved
1	RW	0	revocmem_rd_fail: Read back 1 to indicate Host read REVOC MEM failure, Reading this register automatically clear the failure flag.
0	RW	0	revocmem_wr_fail: Read back 1 to indicate Host write REVOC MEM failure, Reading this register automatically clear the failure flag.

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Table 9-3041 HDMITX_TOP_STAT0

Bit	R/W	Default	Description
31:2	R	0	Reserved
1	R	0	filtered RxSense status: 0= RxSense low; 1= RxSense high.
0	R	0	filtered HPD status: 0= HPD low; 1= HPD high.

Table 9-3042 HDMITX_TOP_SKP_CNTL_STAT

Bit	R/W	Default	Description
31	R	0	Status of nonce_vld signal.
30:4	R	0	Reserved
2	RW	0	DUK_vld:Set to 1 once DUK is written.
1	RW	0	PKF_vld:Set to 1 once PKF is written.

Table 9-3043 HDMITX_TOP_PKF_0

Bit	R/W	Default	Description
31:0	W	0	PKF[31:0]

Table 9-3044 HDMITX_TOP_PKF_1

Bit	R/W	Default	Description
31:0	W	0	PKF[63:32]

Table 9-3045 HDMITX_TOP_PKF_2

Bit	R/W	Default	Description
31:0	W	0	PKF[95:64]

Table 9-3046 HDMITX_TOP_PKF_3

Bit	R/W	Default	Description
31:0	W	0	PKF[127:96]

Table 9-3047 HDMITX_TOP_DUK_0

Bit	R/W	Default	Description
31:0	W	0	DUK[31:0]

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Table 9-3048 HDMITX_TOP_ DUK_1

Bit	R/W	Default	Description
31:0	W	0	DUK[63:32]

Table 9-3049 HDMITX_TOP_ DUK_2

Bit	R/W	Default	Description
31:0	W	0	DUK[95:64]

Table 9-3050 HDMITX_TOP_ DUK_3

Bit	R/W	Default	Description
31:0	W	0	DUK[127:96]

Table 9-3051 HDMITX_TOP_INFILTER

Bit	R/W	Default	Description
31:27	RW	0	Reserved
26:24	RW	0	For DDC infilter: filter internal clock divider. 0=No divide; 1=Divide by 2; 2=Divide by 3; … 7=Divide by 8.
23:16	RW	0	For DDC infilter: sampling clock divider. 0=No divide; 1=Divide the filter sampling clock by 2; 2=Divide the filter sampling clock by 3; … 255=Divide the filter sampling clock by 256;
15:0	RW	0	Reserved

Table 9-3052 HDMITX_TOP_NSEC_SCRATCH

Bit	R/W	Default	Description
31:0	RW	0	Scratch register that can be used for either secure or non-secure reg access.

Table 9-3053 HDMITX_TOP_SEC_SCRATCH

Bit	R/W	Default	Description
31:0	RW	0	Scratch register that can be used for secure reg access only.

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Table 9-3054 HDMITX_TOP_EMP_CNTL0

Bit	R/W	Default	Description
31:16	RW	0	Emppacketsinframe. Number of EMPs to send for the next frame.
15:8	RW	0	Empstartlatency. Defines the number of lines to wait after End-Of-Field, to start sending EMP.
0	RW	0	emp_tx_en. 0=Disable Extended Metadata packet. 1=Enable Extended Metadata packet.

Table 9-3055 HDMITX_TOP_EMP_CNTL1

Bit	R/W	Default	Description
31:19	R	0	Reserved.
18:17	RW	0	emp_endian[1:0]. Bit[0]: 1=EMP data are stored as little Endian in DDR per 64-bit. 0=Big endian. Bit[1]: 1=For each 128-bit, swap high 64-bit to low 64-bit, and low 64-bit to high 64-bit. 0=No swap.
16	RW	0	emp_autoclr_ar_pending. If at the start of DDR read request for the current frame, there is still outstanding requests remaining from the previous frame, this bit defines whether to auto-clear DDR request state machine. 0=The current request will not start until the previous outstanding requests are cleared by normal operation. 1=The state machine is reset and previous outstanding requests are cancelled. The current request starts immediately.
15:0	RW	128	emp_sampleline. All EMP control registers are buffered internally, at the time defined by this field – the number of lines after Vsync rise. Before this time the EMP control registers does not take effect.

Table 9-3056 HDMITX_TOP_EMP_MEMADDR_START

Bit	R/W	Default	Description
31:0	RW	0	Start address of EMP memory pointer for next frame.

Table 9-3057 HDMITX_TOP_EMP_STAT0

Bit	R/W	Default	Description
31:30	RW	0	emp_err[1:0]. Error status of AXI activity. Write 1 to each bit to clear. Bit[0]: 1=AXI RID incorrect. Bit[1]: 1=AXI RRESP error.
29:27	R	0	Reserved.
26:24	R	0	emp_ar_state[2:0]: Status of DDR AXI Address Read state machine. 0=IDLE; 1=WAIT_FIFO_ROOM; 2=WAIT_ARREADY; 3=WAIT_PENDING; 4=DONE.

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Bit	R/W	Default	Description
23:17	R	0	emp_fifo_count[6:0]. FIFO fill level for storing 128-bit DDR data, the result of reading EMP data from DDR.
16:0	R	0	emp_ar_pending. Number of DDR reads that are still outstanding, meaning request has been sent, but Data have yet to be received.

Table 9-3058 HDMITX_TOP_EMP_STAT1

Bit	R/W	Default	Description
31:16	R	0	empdone_cnt_buf [15:0]: Buffered number of EMP sent.
15:0	R	0	empdone_cnt[15:0]: Current number of EMP sent.

Table 9-3059 HDMITX_TOP_AXI_ASYNC_CNTL0

Bit	R/W	Default	Description
31:16	R	0	Reserved.
15:8	RW	128	axi_async_waiting_limit[7:0].
7:5	R	0	Reserved.
4:3	RW	0	axi_urgent[1:0]: DDR request urgent level.
2	RW	0	axi_async_disable_clk. 1=Disable clk to AXI-async module. 0=Enable clk.
1	RW	1	axi_async_auto_gclk_en. 1=Auto clk gate AXI-async module. 0=Free-run clk.
0	RW	1	axi_async_req_en. 1=Enable AXI async interface between EMP's tmds_clk domain to AXI's esm_clk domain. If need to sent EMP, this bit must be enabled. 0=Disable.

Table 9-3060 HDMITX_TOP_AXI_ASYNC_CNTL1

Bit	R/W	Default	Description
31:0	RW	32'h181-01810	axi_async_hold_num.

Table 9-3061 HDMITX_TOP_AXI_ASYNC_STAT0

Bit	R/W	Default	Description
31:1	R	0	Reserved.
0	RW	1	axi_async_chan_idle.

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Table 9-3062 HDMITX_TOP_I2C_BUSY_CNT_MAX

Bit	R/W	Default	Description
31:0	RW	0xffffffff	i2c_busy_cnt_max. After I2C Start bit, if I2C bus is static for more than i2c_busy_cnt_max number of cycles, an error interrupt will happen.

Table 9-3063 HDMITX_TOP_I2C_BUSY_CNT_STAT

Bit	R/W	Default	Description
31:0	R	0	i2c_busy_cnt. Reflect the number of idle cycles after the I2C Start bit, for the latest I2C transaction.

Table 9-3064 HDMITX_TOP_HDCP22_BSOD

Bit	R/W	Default	Description
31	R	0	hdcp22_extbyp_status.
30:29	R	0	Reserved.
28	RW	0	hdcp22_extbyp. To enable this one-off bypass function, set this bit to 1, after read back bit[31]=1, clear this bit to 0. 1=Video display bypass HDCP22 before authentication. After authenticated, display will switch to HDCP22 at ENC_EN=1. One-off action. 0=Do not bypass, original behaviour.
27:26	R	0	Reserved.
25	RW	0	hdcp22_no_bsod. 1=Do not use BSOD to override, no matter from FW or SW. 0=Use the BSOD, original behaviour.
24	RW	0	hdcp22_bsod_override. 1=Overide BSOD value with hdcp_bsod_val. 0=Use the original BSOD value from ESM FW.
23:0	RW	0x8000-80	hdcp22_bsod_val.

Table 9-3065 HDMITX_TOP_DDC_CNTL

Bit	R/W	Default	Description
31:2	R	0	Reserved.
1	RW	1	DSDA pull down. 0=Pull down DSDA. 1=No pull down.
0	RW	1	DSCL pull down. 0=Pull down DSCL. 1=No pull down.

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Note

- To disable NULL, set to 3'b111;
- To enable NULL, set to 3'b110;
- To revert to original behaviour, set to 3'b000.
- Bit[2:1] must be stable throughout operation. Bit[0] can be changed dynamically.

Table 9-3066 HDMITX_TOP_DISABLE_NULL

Bit	R/W	Default	Description
31:3	R	0	Reserved.
2	RW	1	Clear/Set_AVMUTE delay control. 0=Original behaviour. 1=Delay Clear/Set_AVMUTE by 10-cycle.
1	RW	1	Path delay match control. 0=Original behaviour. 1=Delay control/data path by 10-cycle. Must set 1 to disable NULL.
0	RW	0	NULL packet disable control. 0=Enable NULL. Original behaviour. 1=Disable NULL.

Table 9-3067 HDMITX_TOP_HDCP14_UNENCRYPT

Bit	R/W	Default	Description
24	RW	0	1=Overide TMDS channels with this register's color for HDCP1.4 unencrypt state. 0=Original behaviour, color come from DWC IP.
23:16	RW	0	TMDS channel 2 color during HDCP1.4 unencrypt state.
15:8	RW	0	TMDS channel 1 color during HDCP1.4 unencrypt state.
7:0	RW	0	TMDS channel 0 color during HDCP1.4 unencrypt state.

Table 9-3068 HDMITX_TOP_MISC_CNTL

Bit	R/W	Default	Description
0	RW	0	tlgb_fix_off. 0=Fix tmds_encoder's bug of TLGB running disparity error when scramble is on; 1=Original behaviour.

Table 9-3069 HDMITX_TOP_SEC_VIDEO_OVR

There is a HW bit from VPU to indicate if the video content need secure protection, at the input of HDMITX.

When this bit=1, HDMITX_TOP_SEC_VIDEO_OVR, HDMITX_TOP_HDCP14_MIN_SIZE, HDMITX_TOP_HDCP22_MIN_SIZE will be used.

When this bit=0, then these three registers are don't care.

When this bit=1, the rule for HW to judge if the override secure video with HDMITX_TOP_SEC_VIDEO_OVR is as follows:

If the video size < HDMITX_TOP_HDCP14_MIN_SIZE, then no need override, regardless of authentication status.

If the video size >= HDMITX_TOP_HDCP14_MIN_SIZE,

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but < HDMITX_TOP_HDCP22_MIN_SIZE, then override until HDCP1.4 or HDCP2.2 is authenticated.

If the video size >= HDMITX_TOP_HDCP22_MIN_SIZE, then override until HDCP2.2 is authenticated.

Bit	R/W	Default	Description
29:20	RW	0	Video data for tmds channel 2, when override.
19:10	RW	0	Video data for tmds channel 1, when override.
9:0	RW	0	Video data for tmds channel 0, when override.

Table 9-3070 HDMITX_TOP_HDCP14_MIN_SIZE

Bit	R/W	Default	Description
31	RW	0	hdcp14_min_size_v_en
28:16	RW	0	hdcp14_min_size_v[12:0]
15	RW	0	hdcp14_min_size_h_en
13:0	RW	0	hdcp14_min_size_h[13:0]

Table 9-3071 HDMITX_TOP_HDCP22_MIN_SIZE

Bit	R/W	Default	Description
31	RW	0	hdcp22_min_size_v_en
28:16	RW	0	hdcp22_min_size_v[12:0]
15	RW	0	hdcp22_min_size_h_en
13:0	RW	0	hdcp22_min_size_h[13:0]

9.2.3.50.3 Controller Registers

Note

DRM stands for Dynamic Range and Mastering InfoFrame.

Added a_hdcpcfg1 bit[5] and hdcp22reg_ctrl bit[7:6] to optional balance path delays between HDCP22 path, HDCP14 path and non-HDCP path.

Add EMP related register bits.

Add I2C reset.

Add Bstatus read back.

Table 9-3072 ih_fc_stat2 Offset: 0x102

Bits	Name	Memory Access	Description
3	EMP	RW	Active after successful transmission of a total of N packets through DDR-EMP interface. N is programmed by HDMITX_TOP_EMP_CNTL0[31:16]. Value After Reset: 0
2	DRM	RW	Active after successful transmission of an DRM InfoFrame packet. Value After Reset: 0

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Table 9-3073 ih_mute_fc_stat2 Offset: 0x182

Bits	Name	Memory Access	Description
3	EMP	RW	When set to 1, mutes ih_fc_stat2[3]. Value After Reset: 1
2	DRM	RW	When set to 1, mutes ih_fc_stat2[2]. Value After Reset: 1

Table 9-3074 fc_datauto3 Offset: 0x10b7

Bits	Name	Memory Access	Description
6	DRM_ auto	RW	Enables DRM packet insertion Value After Reset: 1

Table 9-3075 fc_rdrb12 Offset: 0x10c4

Bits	Name	Memory Access	Description
7:4	Re-served.		
3:0	DRMfra-meinter-polation	RW	DRM frame interpolation Value After Reset: 0

Table 9-3076 fc_rdrb13 Offset: 0x10c5

Bits	Name	Memory Access	Description
7:4	DRMpa-cketsin-frame	RW	DRM packets per frame Value After Reset: 0
3:0	DRMpa-cketli-nespac-ing	RW	DRM packets line spacing Value After Reset: 0

Table 9-3077 fc_mask2 Offset: 0x10da

Bits	Name	Memory Access	Description
3	EMP	RW	Mask bit for FC_INT2.EMP interrupt bit Value After Reset: 1
2	DRM	RW	Mask bit for FC_INT2.DRM interrupt bit Value After Reset: 1

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Table 9-3078 fc_packet_tx_en Offset: 0x10e3

Bits	Name	Memory Access	Description
7	DRM_ tx_en	RW	DRM transmission control 1: Transmission enabled 0: Transmission disabled Value After Reset: 0

Table 9-3079 fc_drm_hb01 Offset: 0x1168

Bits	Name	Memory Access	Description
7:0	fc_drm_ hb0	RW	Frame composer DRM Packet Header Register 1 Value After Reset: 0

Table 9-3080 fc_drm_hb02 Offset: 0x1169

Bits	Name	Memory Access	Description
7:0	fc_drm_ hb1	RW	Frame composer DRM Packet Header Register 2 Value After Reset: 0

Table 9-3081 fc_drm_pb[0:26] Offset: 0x116a+(i*0x1)

Bits	Name	Memory Access	Description
7:0	fc_drm_ pb	RW	Frame composer DRM Packet Body Register Array Value After Reset: 0

Table 9-3082 fc_dbgforce Offset: 0x1200

Bits	Name	Memory Access	Description
7	forcewoo	RW	Per SolvNet case8000767326: 0=Use bug fix method suggested in case8000767326. 1=Revert to original RTL. Not recommended. Value After Reset: 0

Table 9-3083 a_hdcpcfg1 Offset: 0x5001

Bits	Name	Memory Access	Description
6	hdcp14_ no_ short_ read	RW	1=Read Ri' with explicit address=0x08. 0=Original IP behaviour – short-read. Value After Reset: 0
5	hdcp14_ delmatch	RW	1=Match path delays between HDCP14 path and non-HDCP path. 0=Original IP behaviour. Value After Reset: 0

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Table 9-3084 a_bstatus_hi Offset: 0x5017

Bits	Name	Memory Access	Description
7:0	Bstatus [15:8]	R	HDCP BSTATUS[15:8]. Value After Reset: 0

Table 9-3085 a_bstatus_lo Offset: 0x5018

Bits	Name	Memory Access	Description
7:0	Bstatus [7:0]	R	HDCP BSTATUS[7:0]. Value After Reset: 0

Table 9-3086 hdcp22reg_id Offset: 0x7900

Bits	Name	Memory Access	Description
7	hdcp22_ not_ capable	R	1=HDCP22 Not capable. Value After Reset: 0

Table 9-3087 hdcp22reg_ctrl Offset: 0x7904

Bits	Name	Memory Access	Description
7	hdcp_ byp_ delmatch	RW	1=Match path delays between HDCP path and non-HDCP path. 0=Original IP behaviour. Value After Reset: 0
6	hdcp22_ 14_ delmatch	RW	1=Match path delays between HDCP22 path and HDCP14 path. 0=Original IP behaviour. Value After Reset: 0

Table 9-3088 hdcp22reg_sts Offset: 0x7908

Bits	Name	Memory Access	Description
7	Hdcp22_ capable	R	1=HDCP22 capable. Value After Reset: 0
6	hdcp22_ auth_lost	R	1=HDCP22 authentication lost. Value After Reset: 0
5	hdcp22_ authenti- cated	R	1=HDCP22 authenticated. Value After Reset: 0
4	hdcp22_ auth_fail	R	1=HDCP22 authentication failed. Value After Reset: 0

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Table 9-3089 i2cm_softrstz Offset: 0x7e09

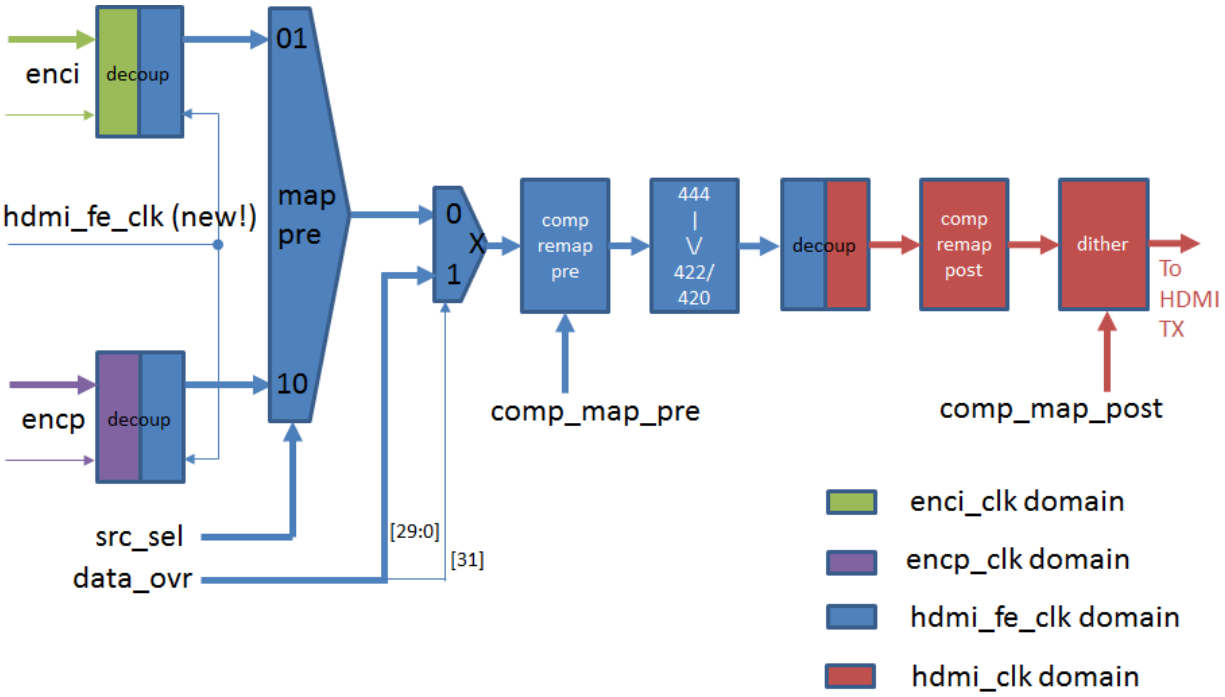
Bits	Name	Memory Access	Description
1	softrst_ idle_cnt_ en	RW	Active by writing a zero and auto cleared to one in the following cycle. Do this to re-enable IDLE counter again. The counter maybe frozen due to some mis-operation from RX on the I2C bus. Value After Reset: 1

9.2.3.50.4 VPU_HDMI_IF Module

Function

VPU_HDMI_IF is a sub-module inside the VPU. It takes video data from either ENCI or ENCP, performs functions such as video component remapping, 444 to 422 or 420 conversion, and dither. Below is the block diagram of the module.

Figure 9-6 VPU_HDMI_IF Function



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Registers

Table 9-3090 vpu_hdmi_setting

Bit	R/W	Default	Description
27:24	RW	0	rd_data_post (New): Read rate to the async FIFO between HDMI_FE_CLK domain and HDMI_CLK domain. 0=One read every hdmi_clk; 1=One read every 2 hdmi_clk; 2=One read every 3 hdmi_clk; … 15=One read every 16 hdmi_clk.
23:20	RW	0	wr_data_post (New): Write rate to the async FIFO between HDMI_FE_CLK domain and HDMI_CLK domain. 0=One write every hdmi_fe_clk; 1=One write every 2 hdmi_fe_clk; 2=One write every 3 hdmi_fe_clk; … 15=One write every 16 hdmi_fe_clk.
18:16	RW	0	comp_map_pre (New): In case the input data is not CrYCb, map the data to CrYCb format, before 444->422/420 conversion. E.g, if input data format is {2, 1, 0} 0=Output {2, 1, 0}; 1=Output {1, 0, 2}; 2=Output {1, 2, 0}; 3=Output {0, 2, 1}; 4=Output {0, 1, 2}; 5=Output {2, 0, 1}; 6,7=Reserved.
15:12	RW	0	rd_data_pre (Original): Read rate to the async FIFO between VENC and HDMI_FE_CLK domain. 0=One read every hdmi_fe_clk; 1=One read every 2 hdmi_fe_clk; 2=One read every 3 hdmi_fe_clk; … 15=One read every 16 hdmi_fe_clk.
11:8	RW	0	wr_data_pre (Original): Write rate to the async FIFO between VENC and HDMI_FE_CLK domain. 0=One write every enc_clk; 1=One write every 2 enc_clk; 2=One write every 3 enc_clk; … 15=One write every 16 enc_clk.
7:5	RW	0	comp_map_post (Original): Input data is CrYCb(BRG), map the output data to desired format. 0=Output {Cr, Y, Cb} or {B, R, G}; 1=Output {Y, Cb, Cr} or {R, G, B}; 2=Output {Y, Cr, Cb} or {R, B, G}; 3=Output {Cb, Cr, Y} or {G, B, R}; 4=Output {Cb, Y, Cr} or {G, R, B}; 5=Output {Cr, Cb, Y} or {B, G, R}; 6,7=Reserved.
4	RW	0	inv_dvi_clk. If true, invert the polarity of clock output to external DVI interface. (NOT internal HDMI).
3	RW	0	inv_vsync: If true, invert the polarity of VSync input from VENC.

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Bit	R/W	Default	Description
2	RW	0	inv_hsync: If true, invert the polarity of HSync input from VENC.
1:0	RW	0	src_sel: Select which HDMI source from between ENCI and ENCP. 2'b00: Disable HDMI source; 2'b01: Select ENCI data to HDMI; 2'b10: Select ENCP data to HDMI; 2'b11: Not allowed.

Table 9-3091 vpu_hdmi_data_ovr

Bit	R/W	Default	Description
31	RW	0	data_ovr_en: Control if override HDMI input data with data_ovr [29:0], for display e.g. black or blue screen. 0: No override; 1: Enable override.
29:20	RW	0	data_ovr[29:20]: Programmable pixel data value for override.
19:10	RW	0	data_ovr[19:10]: Programmable pixel data value for override.
9:0	RW	0	data_ovr[9:0]: Programmable pixel data value for override.

Table 9-3092 vpu_hdmi_fmt_ctrl

Bit	R/W	Default	Description
27:24	RW	0	pix_repeat. Need to program to be the same as HDMI IP internal pixel repeat rate. 0 = No repeat; 1 = Repeat once; ….
23:22	RW	0	chroma_dnsmp_v: Vertical chroma down sample mode when covnert to 422 or 420. 0 = use line 0; 1 = use line 1; 2 = use average.
21:19	RW	0	Frame count offset for B.
18:16	RW	0	Frame count offset for G.
15	RW	0	hcnt hold when de valid.
14	RW	0	RGB frame count separate.
13	RW	0	dith4x4: frame random enable
12	RW	0	dith4x4 enable
11	RW	0	tunnel_en: tunnel enable for DOLBY.
10	RW	0	hdmi_round_en
9:6	RW	0	hdmi_dith10
5	RW	0	hdmi_dith_md
4	RW	0	hdmi_dith_en

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Bit	R/W	Default	Description
3:2	RW	0	chroma_dnsmp_h: Horizontal chroma down sample mode when covnert to 422 or 420. 0 = use pixel 0; 1 = use pixel 1; 2 = use average.
1:0	RW	0	hdmi_vide_fmt: Control whether to convert ENC's 444 data to 422 or 420. 0 = No convertion; 1 = Convert to 422; 2 = Convert to 420.

9.2.3.50.5 Operating Procedures

This section describes how to send EMP or any packets through from DDR.

At Vsync interrupt, SW programs EMP interface and packet data. The configuration and data will be sampled and buffered somewhere in the middle of the current Frame. The packets will be sent during the next Frame's VBlank.

The format of the packet data in DDR memory is as below:

```
-------------------------------- 1st Packet
Addr_S+0:Packet Header HB0 (E.g: EMP=0x7F, DRM=0x87)
Addr_S+1:Packet Header HB1 (E.g: EMP=0x80/0x00/0x40, DRM=InfoFrame_version)
Addr_S+2:Packet Header HB2 (E.g: EMP=Sequence_index, DRM=InfoFrame_length)
Addr_S+3:Packet Header PB0 (E.g: EMP=Payload byte0, DRM=Checksum byte)
Addr_S+4:Packet Header PB1 (E.g: EMP=Payload byte1, DRM=Byte1)
Addr_S+5:Packet Header PB2 (E.g: EMP=Payload byte2, DRM=Byte2)
……
Addr_S+30:Packet Header PB27 (E.g: EMP=Payload byte27, DRM=Byte27)
Addr_S+31:0x00
-------------------------------- 2nd Packet
Addr_S+32:Packet Header HB0
……
Addr_S+63:0x00
-------------------------------- 3rd Packet
……
……
-------------------------------- N-th/Last Packet
Addr_S+32*(N-1):Packet Header HB0
……
Addr_S+32*N-1:0x00
--------------------------------
```

Note

- * Addr_S is the start address of a DDR location to store the packet data, must be 32-byte aligned.
- * N is the total number of packets to send in the next Frame. Need 32**N* byte memory space.
- * All types of packets are supported. For InfoFrame packets, SW must calculate the Checksum.

Program EMP related registers, for details refer to register description section Table 9-3054 to Table 9-3058. You may need to update these below register fields at every Vsync interrupt:

- HDMITX_TOP_EMP_MEMADDR_START – Update with a new *Addr_S* pointer.
- HDMITX_TOP_EMP_CNTL0 [31:16] – Update with a new *N* = number of packets to send.
- HDMITX_TOP_EMP_CNTL0 [0] – Enable or disable sending packets via DDR-EMP interface.

Example Perl script:

```
    my @drm_hb  = (0x87, 0x01, 27);
    my $drm_pb1  = 0;
    my @drm_pb;
    for (my $i = 1; $i <= 27; $i ++) push(@drm_pb, ($drm_pb1++)&0xff);
my $drm_pb0 = &checksum((@drm_hb, @drm_pb));
```


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```
sub checksum
    {
        my @in  = @_;

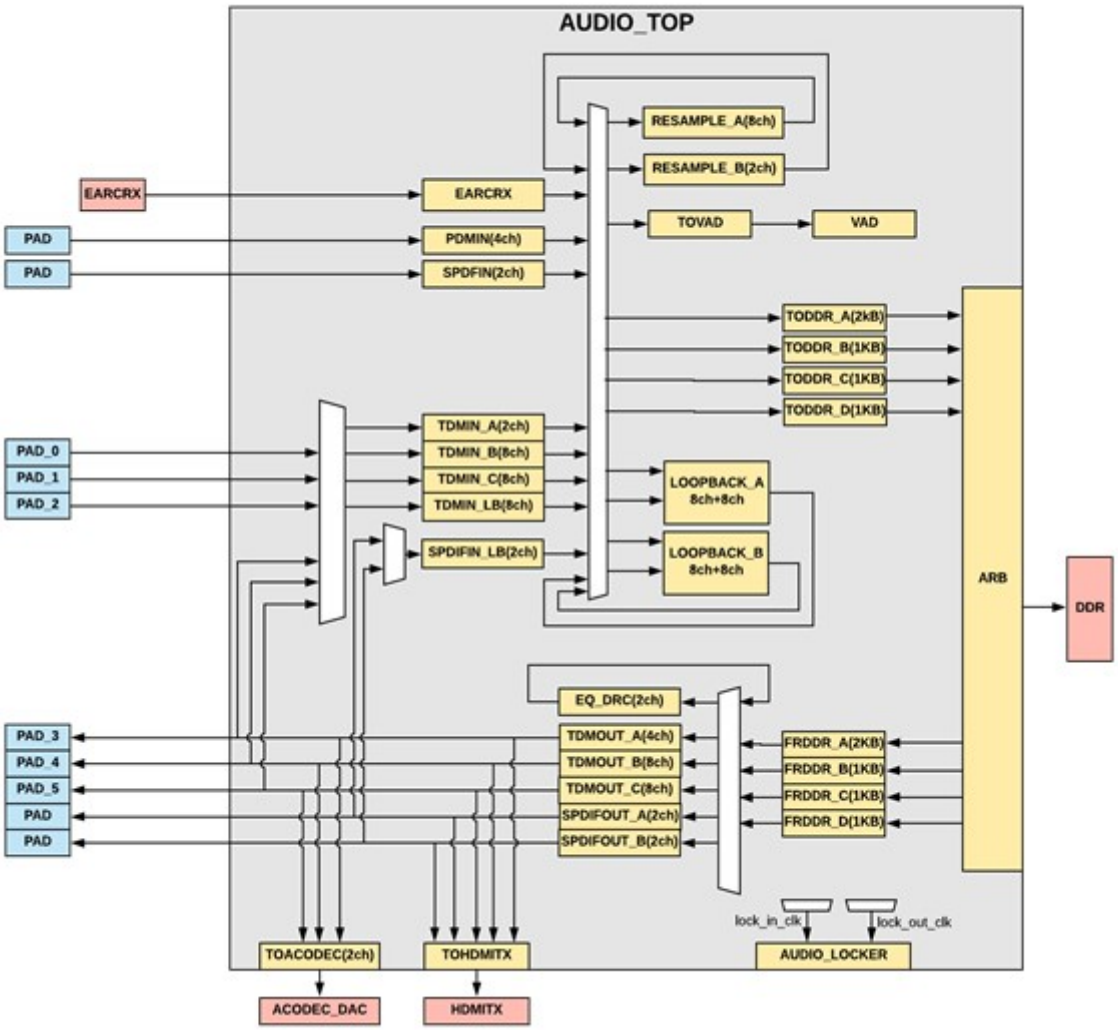
        my $sum = 0;
        for (my $i = 0; $i <= $#in; $i ++) $sum     = ($sum + $in[$i]) & 0xff;
        $sum = (255 - $sum) & 0xff;
        $sum = ($sum + 1) & 0xff;
        $sum;
    }   # checksum
```


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10 Audio Path

The SoC integrates 3 TDM input/output interface, 1 SPDIF input, 2 SPDIF output interface, 1 PDM interface up to 4 channels, 4 TODDR (FIFO) for transfer input data to DDR, 4 FRDDR (FIFO) for transfer data from DDR to output, 1 TDM LB and 1 SPDIF LB and 2 Loopback for AEC, 2 HW resample for clock synchronization, 1 VAD voice wake up, and 1 clock locker detect difference of two clock. Below is the diagram for audio path.

Figure 10-1 Audio Path



10.1 Audio Input

10.1.1 Overview

This section describes TDM input interface, SPDIF input interface PDM input interface and EARC RX interface.

10.1.2 TDM Input Interface

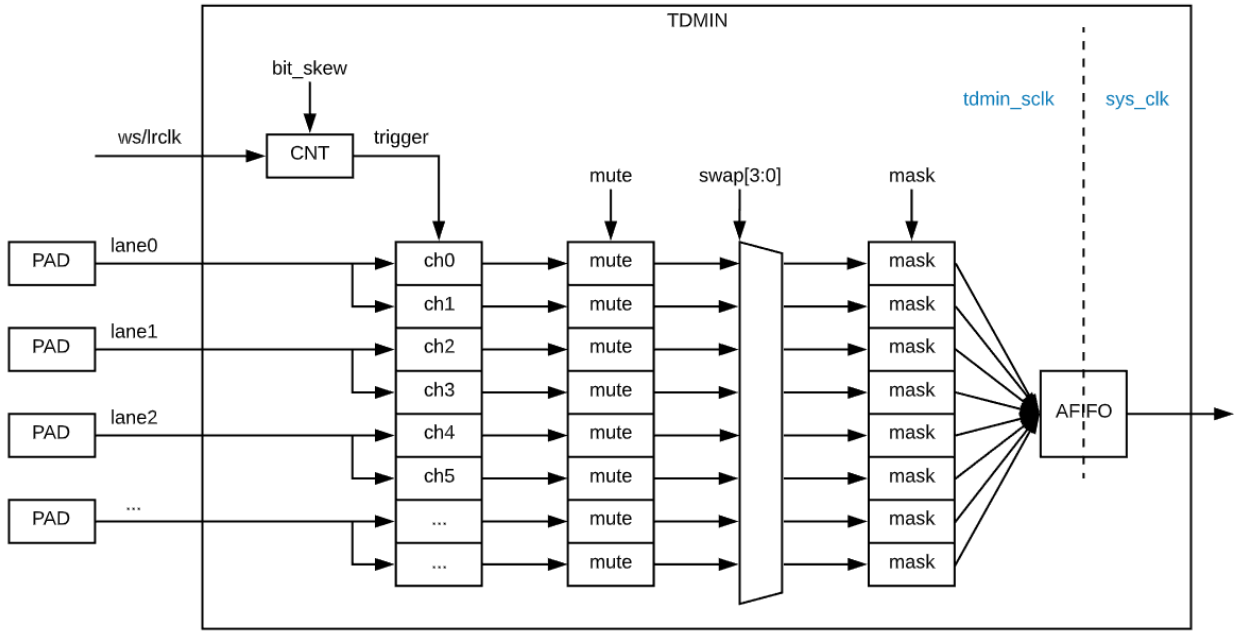
TDM input interface works in the following way:

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- All worked at tdm_sclk before AFIFO,
- Output is worked at sysclk;
- Add skew control between lrclk and data;
- Detect rise or fall edge of lrclk and clear bit_cnt/slot_cnt;
- Shift serial data in to 8 parallel register (max 32bits) ;
- Swap parallel register to sample data;
- Send sample data out in serials by mask/mute configure;

Below is the diagram of TDM input interface.

Figure 10-2 TDM Input



10.1.3 SPDIF Input Interface

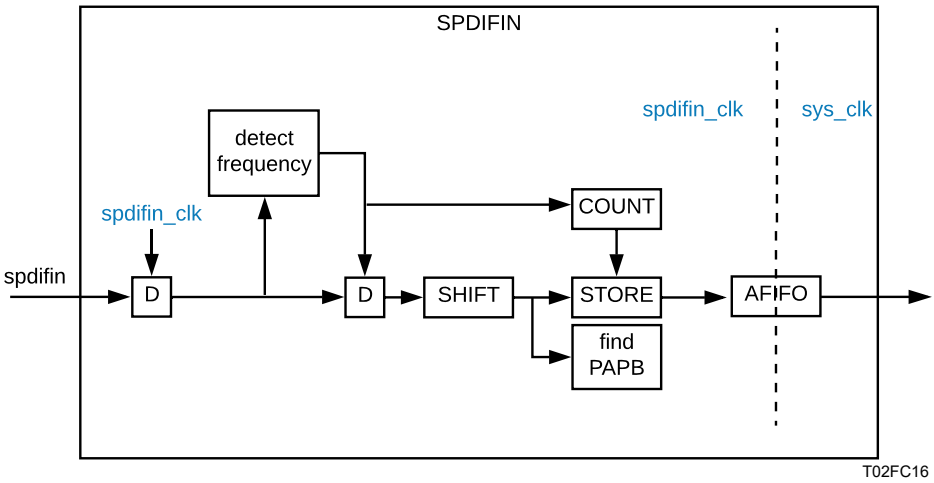
SPDIF input interface works in the following way:

- All worked at spdifin_clk before AFIFO;
- After AFIFO worked at sysclk;
- Detect frequency by rise or fall edge;
- Capture data to shift reg;
- Store data to sample L channel or R channel;
- Detect PaPb if it's IEC60937;

Below is the diagram of SPDIF input interface.

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Figure 10-3 SPDIF Input



10.1.4 PDM

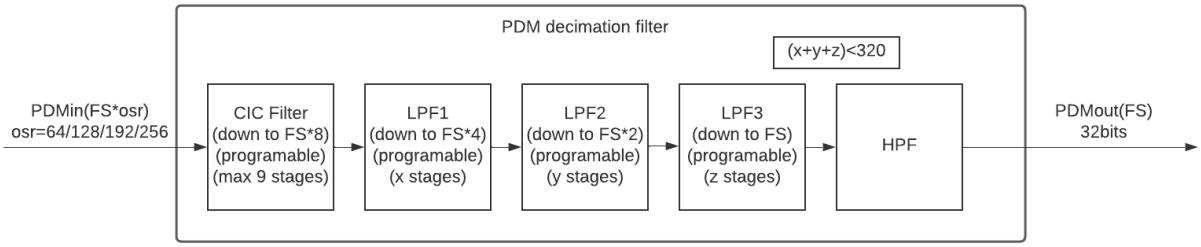
PDM input Decimation Filter is a highly programmable multistage decimation filter. It supports 4 inputs PDM digtal micphone interface. Each channel contains one 9 stage CIC filter, 3 low power filters and a high pass filter. The PDM input bit rate is calculate with fs*OSR. OSR can be 64, 128, 192 or 256.

CIC filter may have 3 to 9 CIC stages and the downsample rate also can be programable.There is a multiplier and shifter to adjust the result to match the accuarcy and CIC bit width.

There are 3 low pass filters which shared a 336x24 Coeffient memory and a 336x28 data memory. That means these 3 filters can be configed upto 336 taps together. The coeffient memory need to be programmed through APB bus. For example, if the filter 1 contains 140 taps, filter2 contains 32 taps, filter 3 contain 146 steps, the filter 1 coefficient will use 0~139 of the coeffient memory address; the filter 2 coefficient will use 140~171 of coefficient memory address and the filter 3 coefficient will use 172~317 of the coeffient memory address. The fillter stage controller will based on the downsample rate, filter taps and the rounding mode of each filter to arrange the filter.

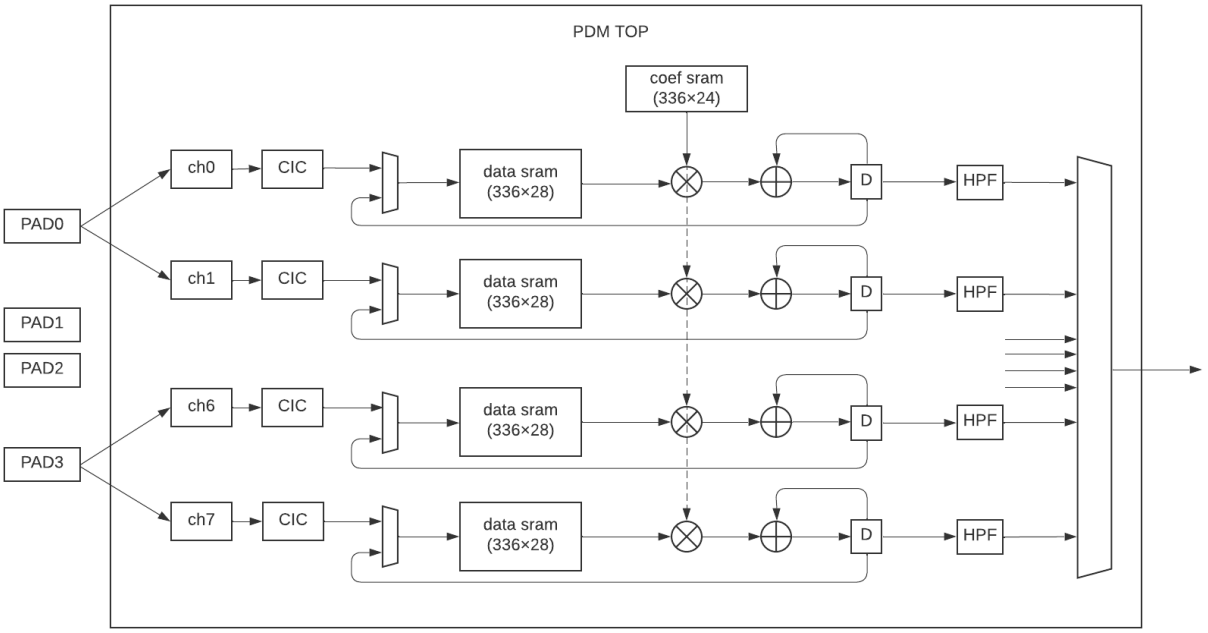
The final high pass filter is used to filter the DC curent.

Figure 10-4 PDM Decimation Filter



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Figure 10-5 PDM Structure



10.2 Audio Output

10.2.1 Overview

This section describes TDM output interface, SPDIF output interface and audio REQ_FRDDR submodule.

10.2.2 TDM Output Interface

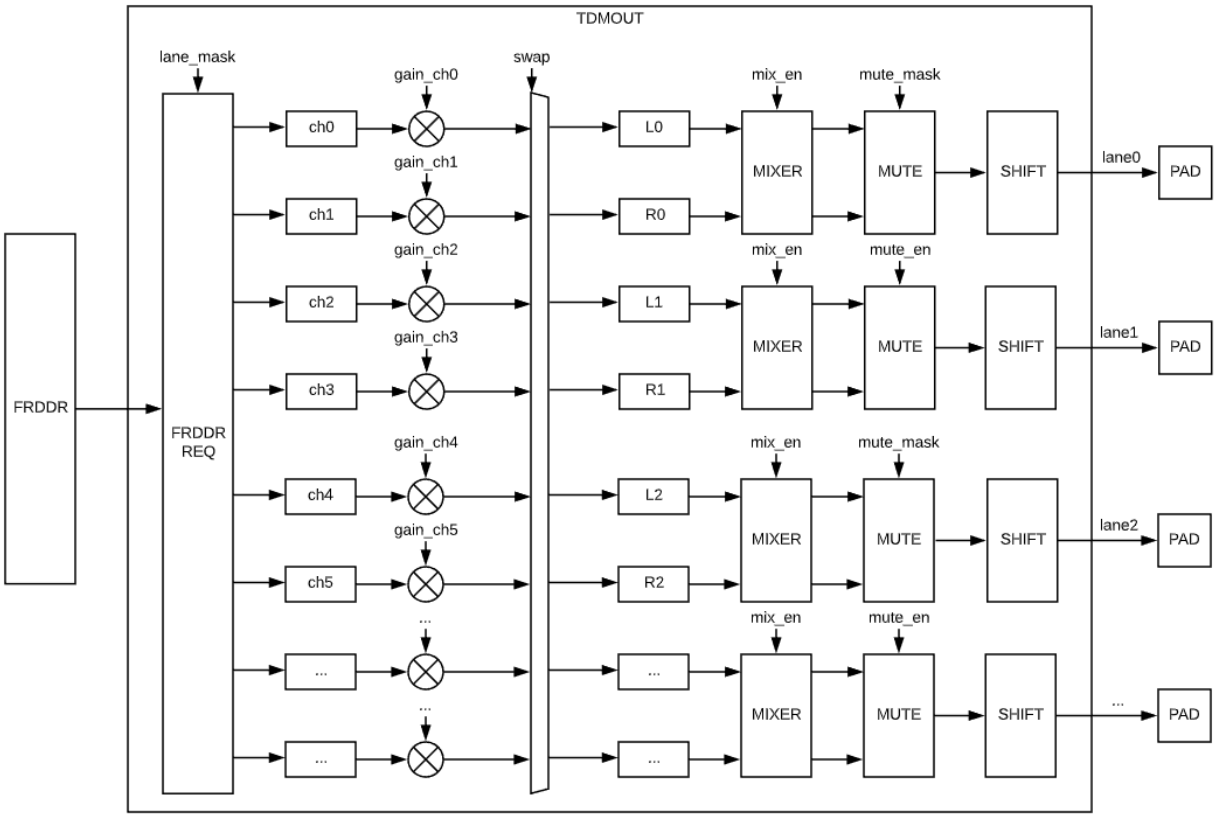
TDM output interface works in the following way:

- All worked at tdm_sclk;
- Detect sample valid by tdm_lrclk rise edge and clear bit_cnt/slot_cnt;
- Request data from FRDDR and store to sample register;
- Swap sample register;
- Shift send out data;

Below is the digram of TDM output interface.

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Figure 10-6 TDM Output



10.2.3 SPDIF Output Interface

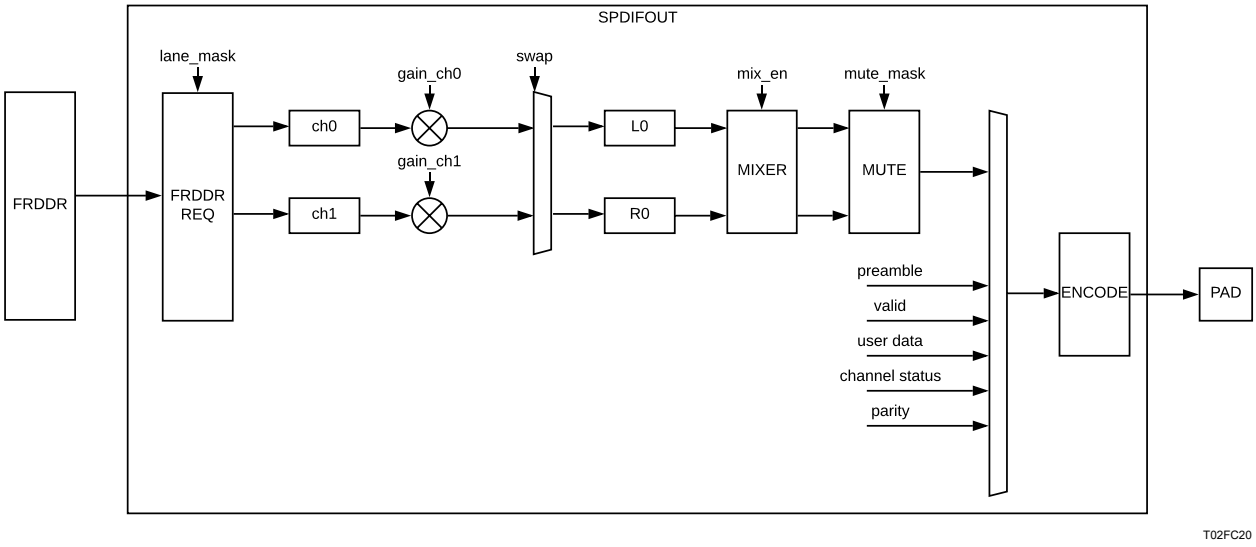
The SPDIF output interface works in the following way:

- All worked at spdifout clk;
- Request data from FRDDR and store to sample L0/R0
- Select data by bit_cnt/slot_cnt and send out;

Below is the digram of SPDIF output interface.

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Figure 10-7 SPDIF Output Interface



The SPDIF (encode) add same source select. The SPDIF out can be the same with i2s 0/1/2/3, and can select before or after eq/drc.

10.2.4 Audio REQ_FRDDR

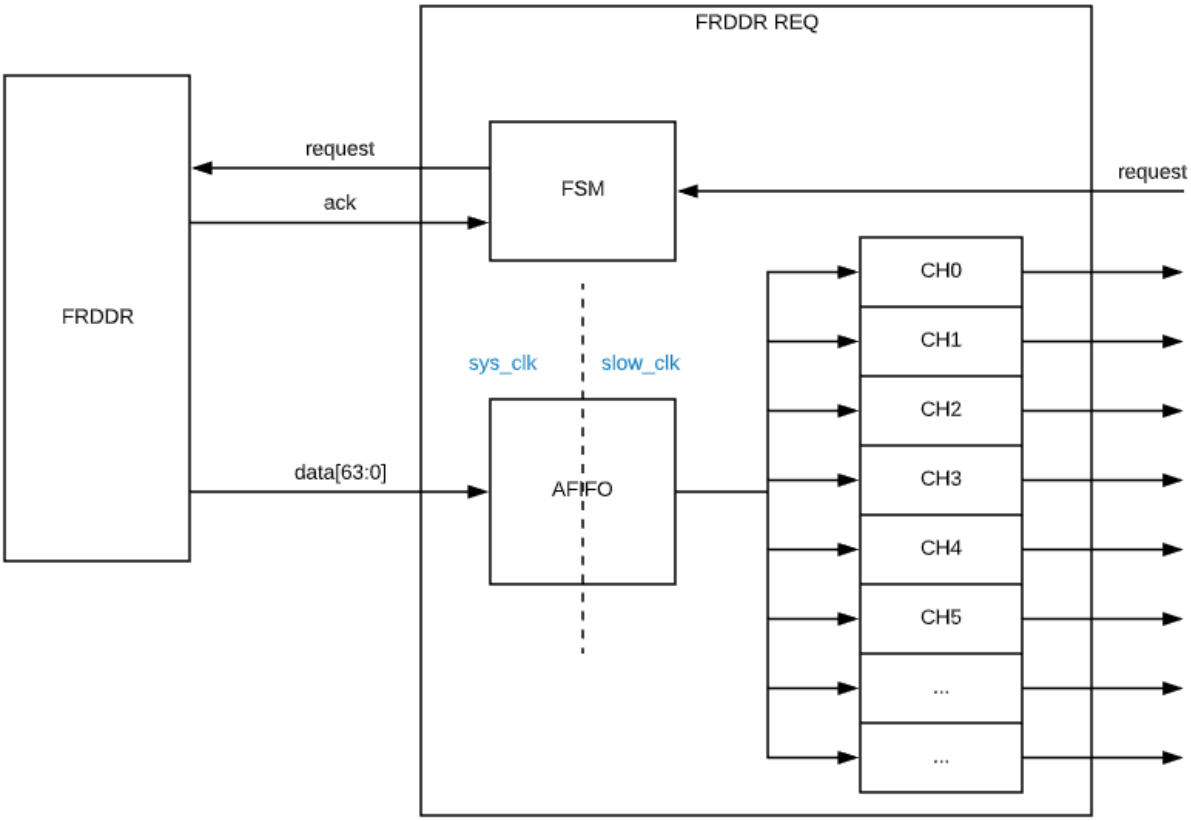
Audio Req_Frddr transfers data from sys clock to out clock and change format in the following way;

- Wait for OUT enable and FRDDR initial done;
- Request first time and fill sample;
- When received update data, it will send request to FRDDR and update sample;

Below is a diagram of Audio REQ_FRDDR.

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Figure 10-8 Audio REQ_FRDDR



10.3 DDR Datapath

10.3.1 Overview

DDR consists of the 2 parts: DDR memory controller (DMC) and AM-DDR PHY. The main features of this module are listed below:

- Support DDR3 SDRAM up to DDR3-2133.
- Support DDR4 SDRAM up to DDR4-2666.
- Support LPDDR4 SDRAM up to LPDDR4-2666.
- Support 32bits and 16bits data mode.
- Unbalanced 16bits DDR3/4 SDRAM size in 32 bits data bus mode.
- Each DDR command buffer contains 64bytes data.
- 32 write command buffer and 32 read command buffer for DDR command generation.
- READ command reordering regardless ID.
- Write command reordering regardless IDs.
- Write and read data coherence.
- Optimized DDR command reordering based on:
  - Priority
  - Rank
  - Bank

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- Bank group interleaving(DDR4)
- Read/write

- 4 level priority control to reduce the latency for the urgent request.
- Unblocking urgent control through Asynchronous FIFO and pipelines.
- Per Port Per ID Security Control through the all security ranges.
- Up to 16 security range can be defined.
- Support up to 16 AXI3/4 and 8 AMBUS(Amlogic) interfaces.
- Optimized AMBUS to support 0~3 burst to improve DDR efficiency and reduce.

Figure 10-9 DDR Interface

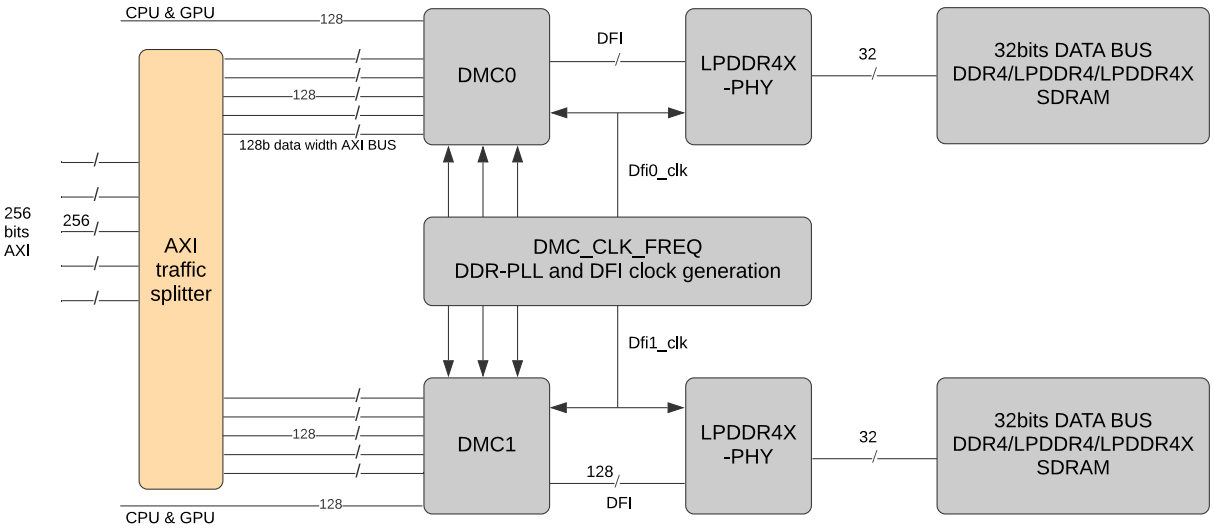
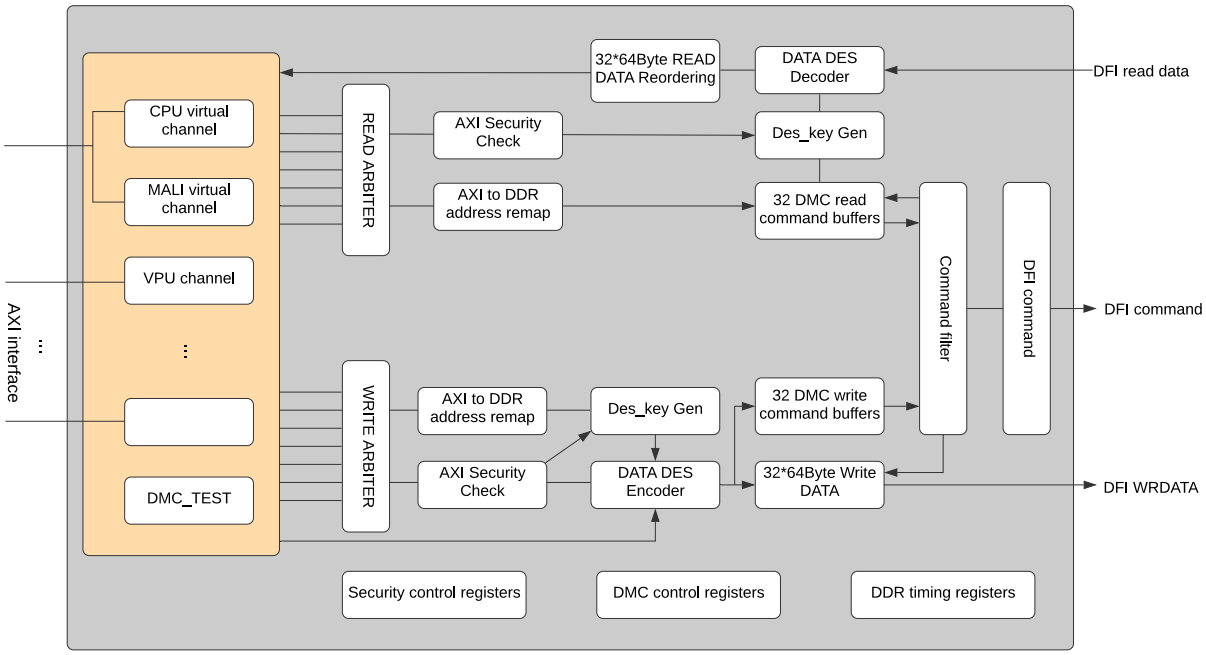


Figure 10-10 DMC Architecture



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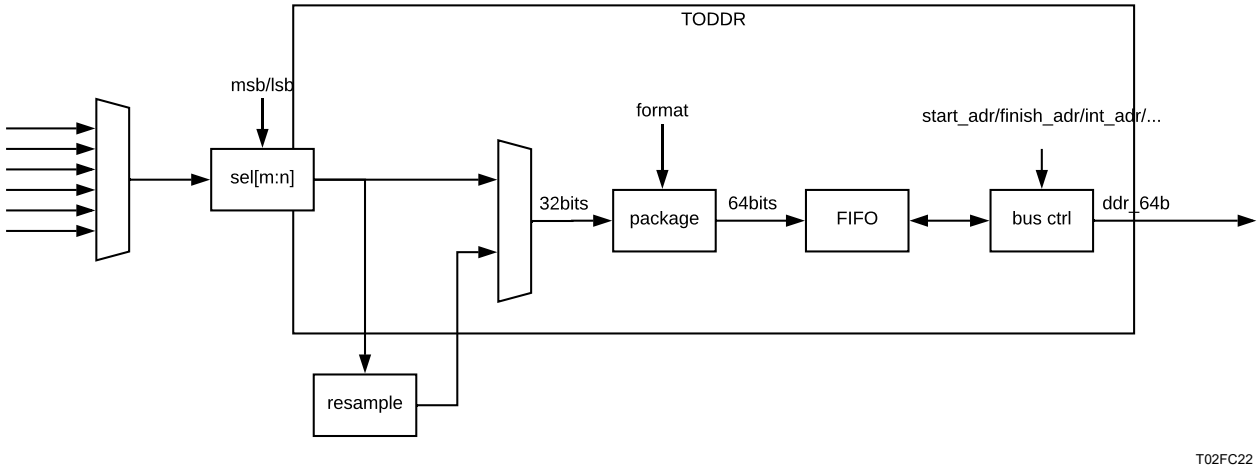
10.3.2 Audio TODDR

The SoC has 5 TODDR(FIFO), TODDR_A's FIFO depth is 4096x64; B/C/D/E are 128x64. TODDR module works in the following way□

- All TODDR work at sysclk;
- Resample if need;
- Change format and package to 64 bits data by configuration;
- Write to fifo;
- Read data from fifo and send to DDR automatically by configuration;

Below is the Diagram of Audio TODDR.

Figure 10-11 Audio TODDR



10.3.3 Audio FRDDR

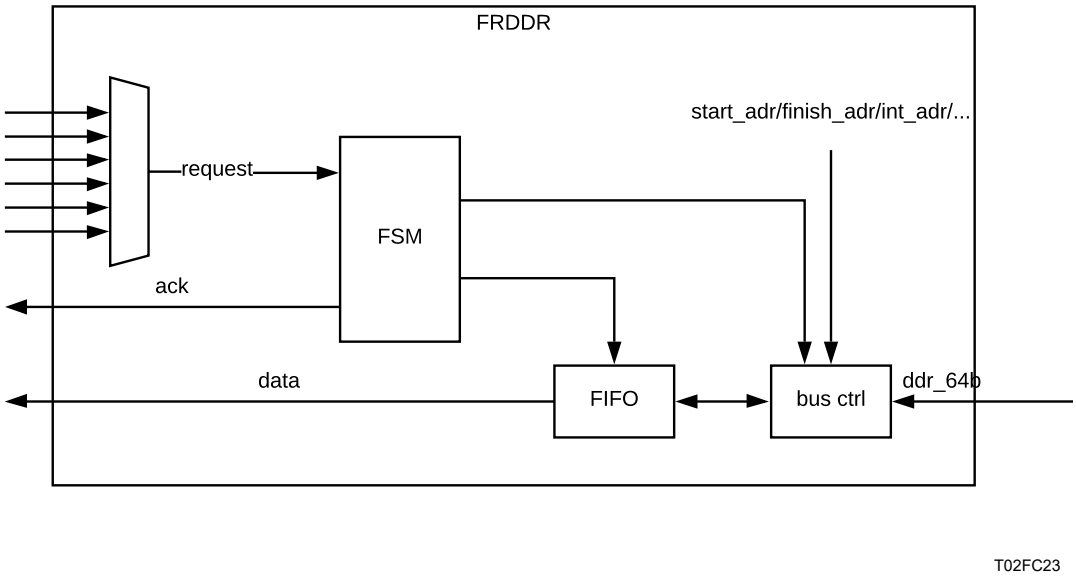
The SoC has 5 FRDDR(FIFO), FRDDR_A's FIFO depth is 256x64, B/C/D/E are 128x64;

- All work at sysclk;
- When enable FRDDR, it will fill FIFO from DDR first;
- When FRDDR receive request, it will read data from fifo and send out;
- FRDDR will fill FIFO automatically by configure;

Below is the Diagram of Audio FRDDR.

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Figure 10-12 Audio FRDDR



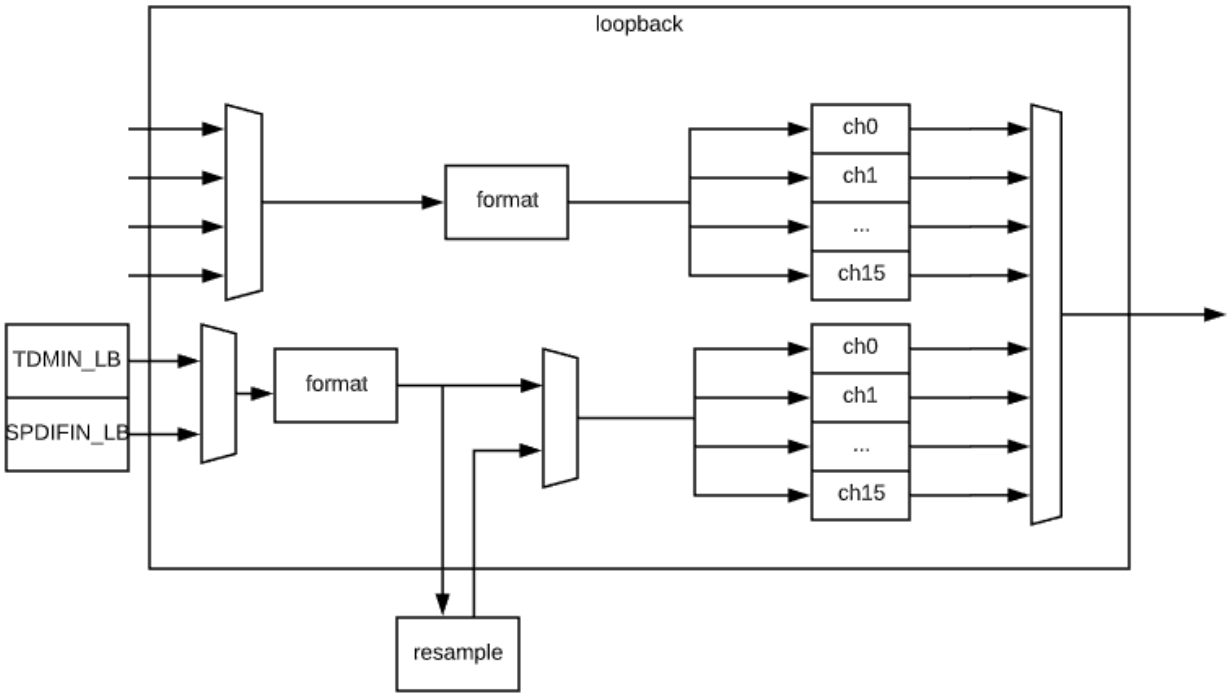
10.4 Audio Loopback

TDMIN_LB can receive one TDMOUT. Loopback can merger with two source in the following way:

- Store one source to temp register;
- When another source arrived, send out direct;
- When finished, send out temp register;

Below is the diagram of audio loopback datapath.

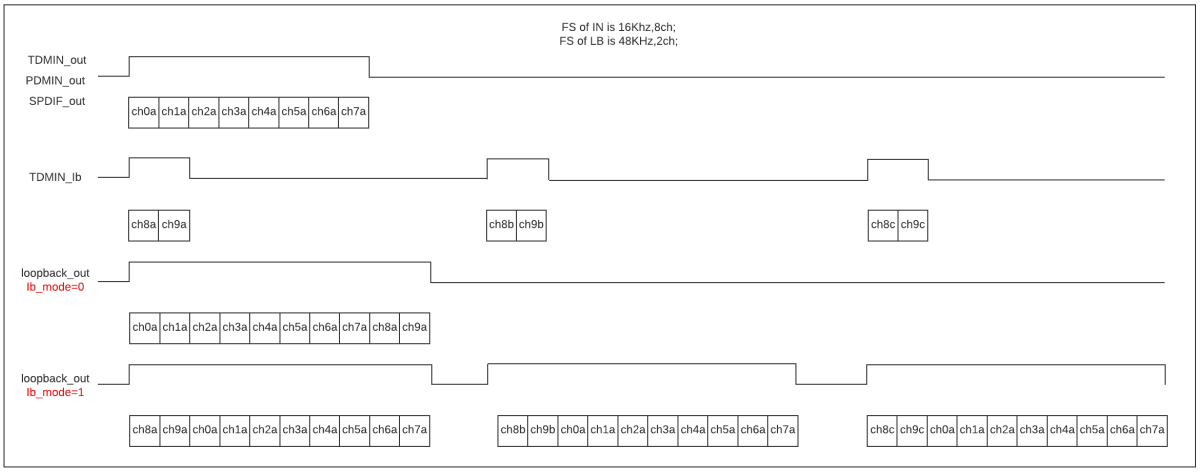
Figure 10-13 Audio Loopback Datapath



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Audio loopback wave form are shown below.

Figure 10-14 Audio Loopback Wave Form



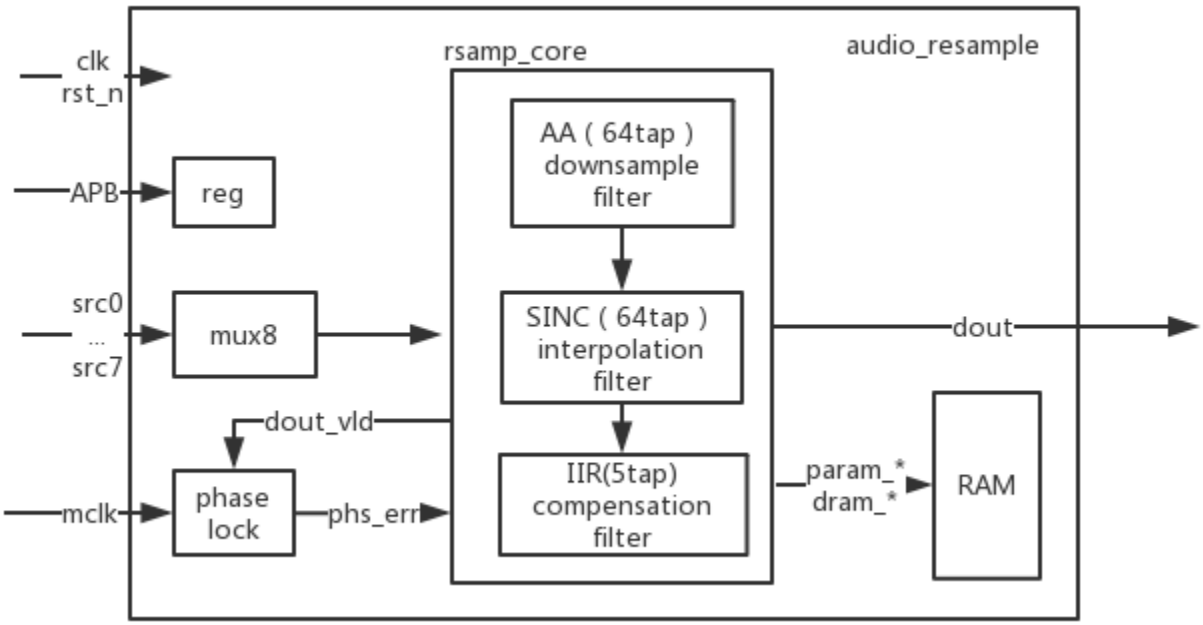
10.5 Audio ResampleA/B

Audio resample changes data from one symbol rate to another symbol rate in the following steps:

1. Max 8 audio sources is supported ,should be muxed to 1 source to audio_resample core.
2. MSB/LSB selection is supported after source mux.
3. Resample core do the symbol rate convert, max 8/32 channel is supported.
   a. If need down sample, aa filter should be on, max 64 tap is supported. 1/2 and 1/4 down sample is supported.
   b. Audio re-sample use sinc filter, max 64tap, 1/2^28 phase precision interpolation.
   c. IIR compensation filter is used for compensate high-frequency damping.
4. Phase lock module is used for input-clock and output-clock symbol rate synchronization.

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Figure 10-15 Audio Resample

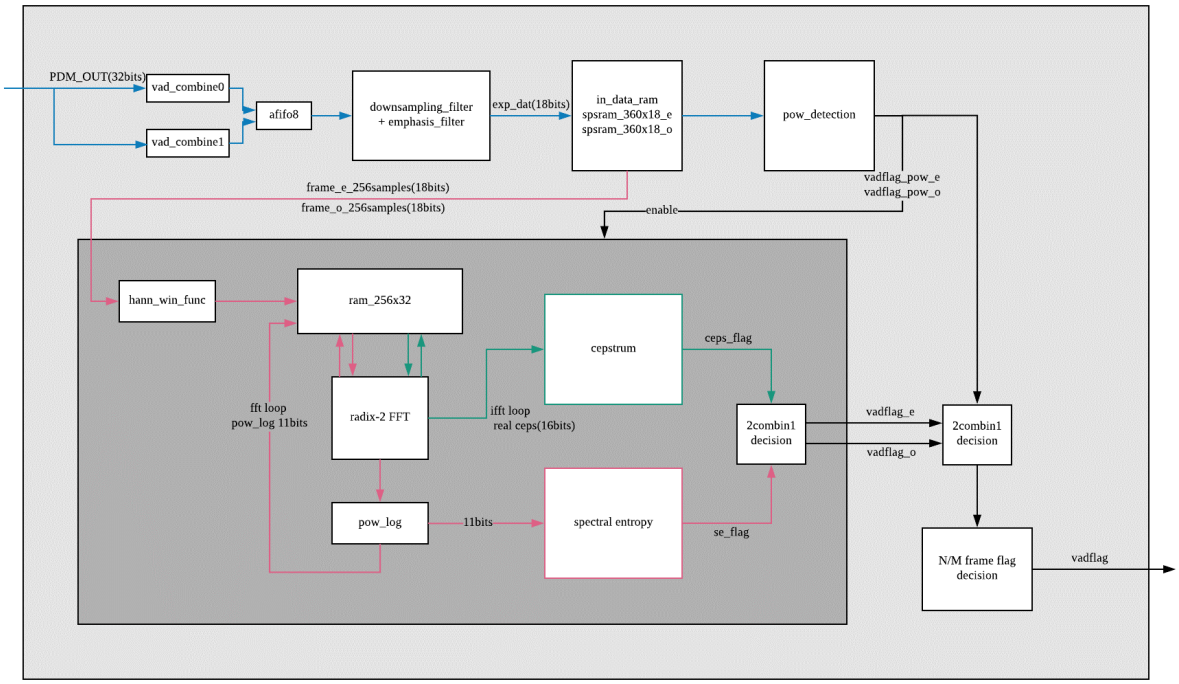


10.6 Audio VAD

VAD will wake up DSP when it determine if voice is present in a particular audio signal. It support 2 channels audio streams searching which combined from PDM filter output audio stream. The audio stream will be down-sampled to 8Kbit/s rate and de-noised before detection processing. VAD can provide power detection, cepstral detection and spectral entropy detection. It will do the detection per 10ms. It contains one 256p FFT function for cepstral and spectral entropy calculation.

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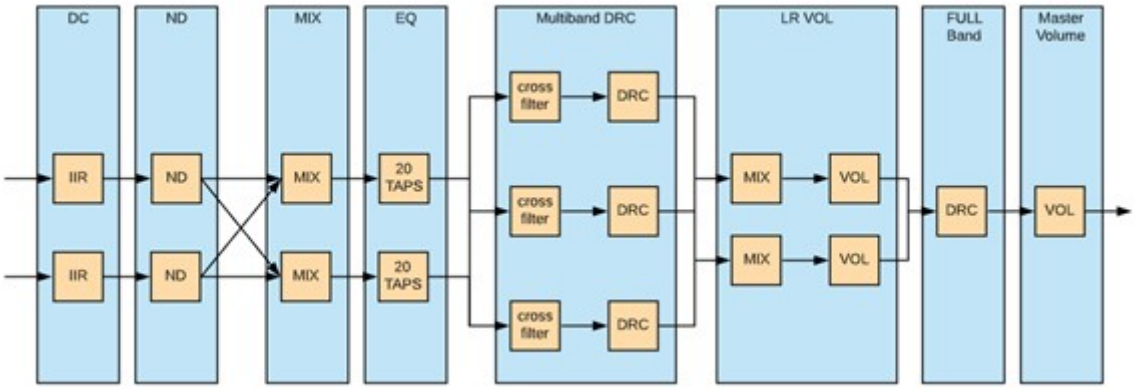
Figure 10-16 Audio VAD



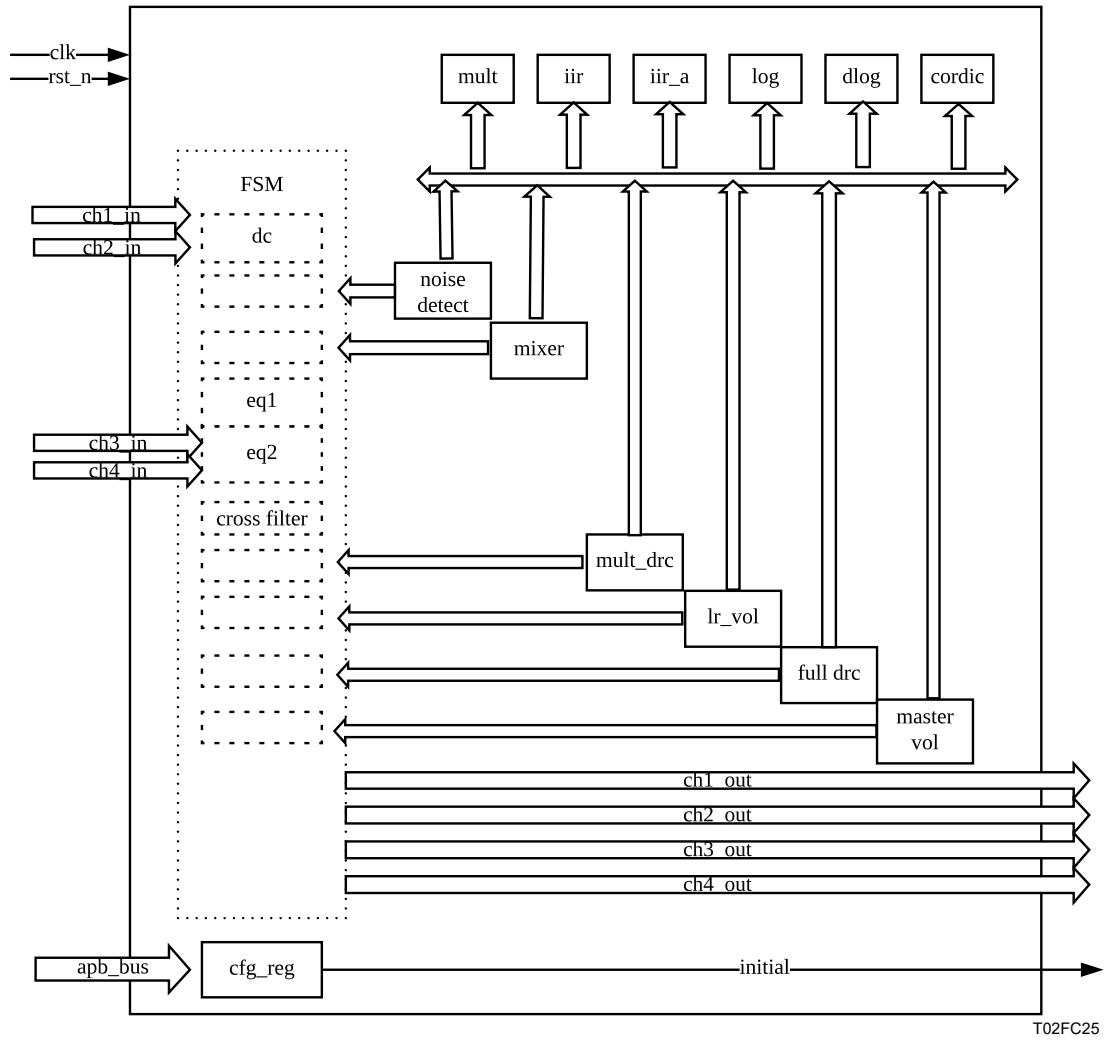
10.7 Audio EQDRC

It support 4 channels audio streams. Two channels do eq and drc, the others only do eq.

The basic structure diagram is shown below.



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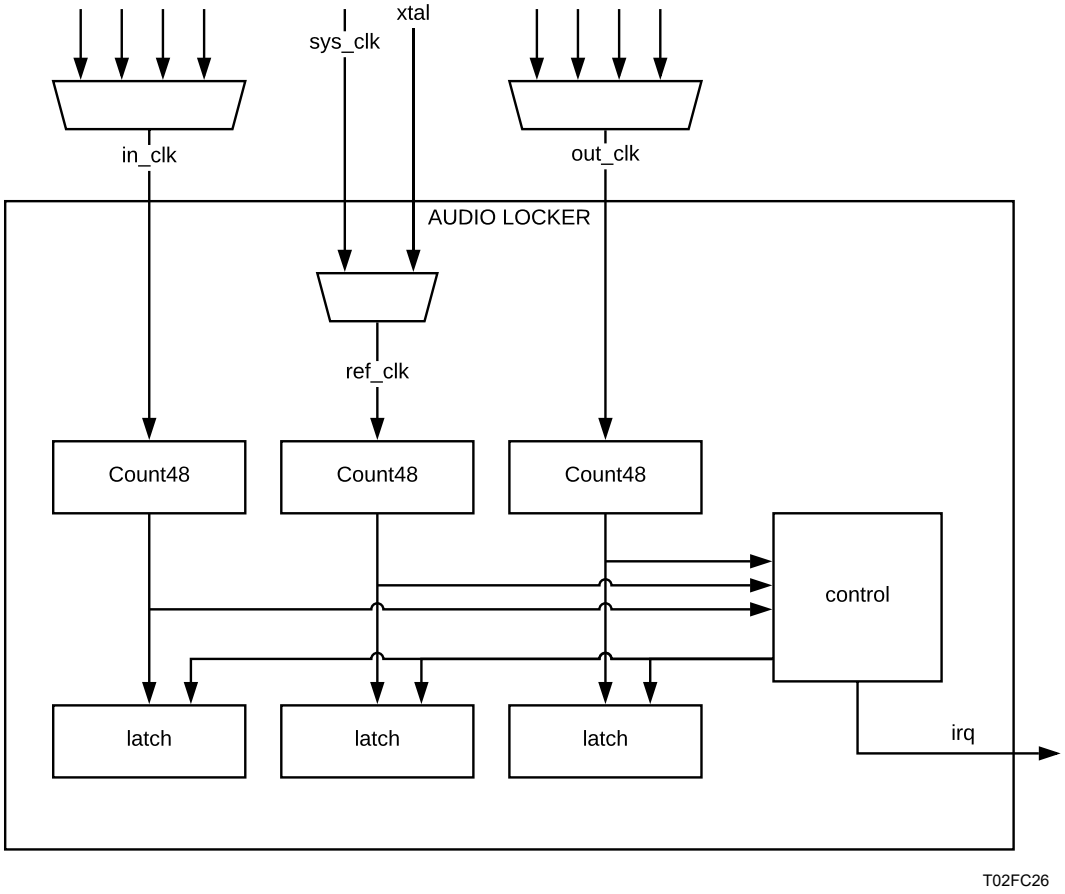
10.8 Audio Locker

The audio input clock and output clock are in different power domain and may have little difference, the difference leads to FIFO problem, the SoC uses Audio Locker module to fix this problem, the basic method is to measure the difference between different clocks and adjust (software dynamically) the clock frequency to make them match.

Below shows the diagram of Audio Locker module.

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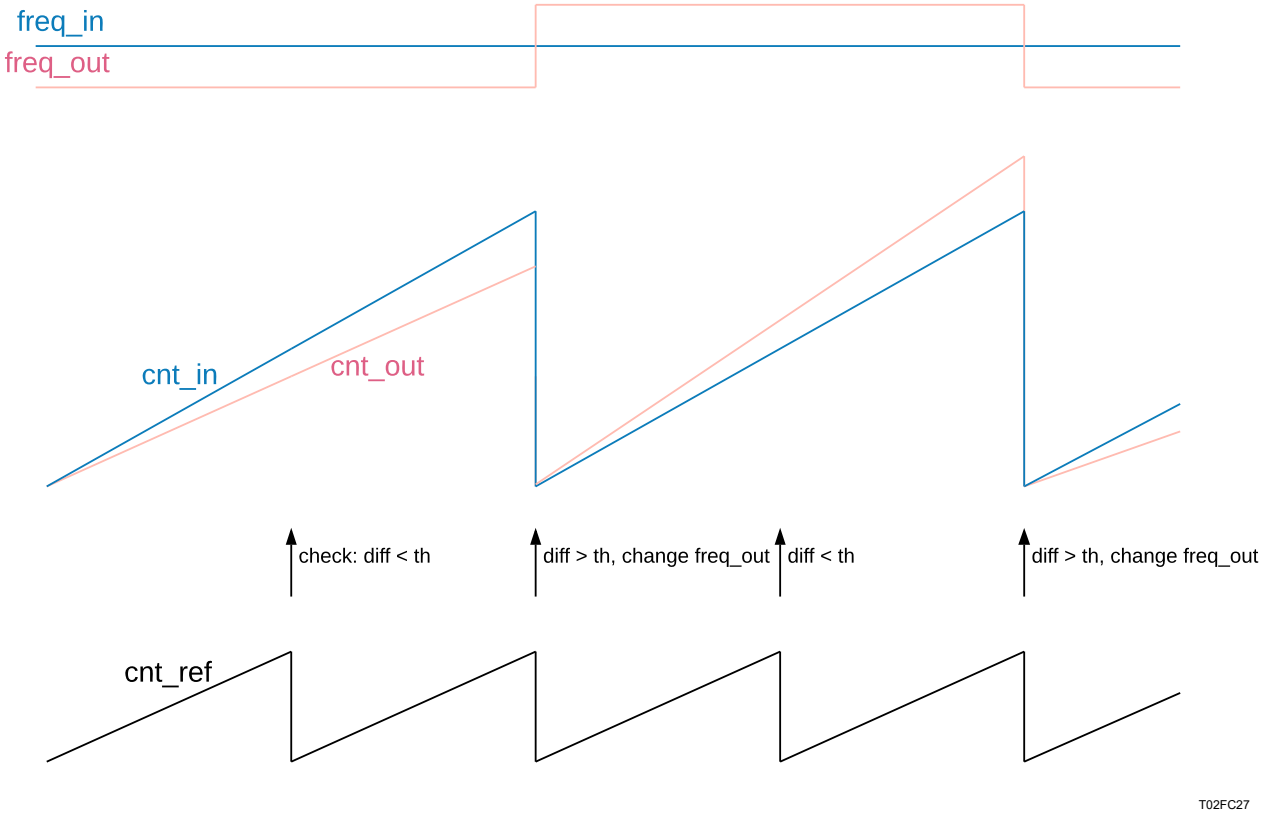
Figure 10-17 Audio Locker



For example: when the diff of two freq creater than threshold is detected, change frequency of clock_ out by SW, will keep clock_out close clock_in.

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Figure 10-18 Audio Locker Example



10.9 Audio Timing Specification

There are two modes for the audio I2S/TDM interface: master mode and slave mode, as shown below.

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Figure 10-19 I2S/TDM Timing Diagram, Master Mode

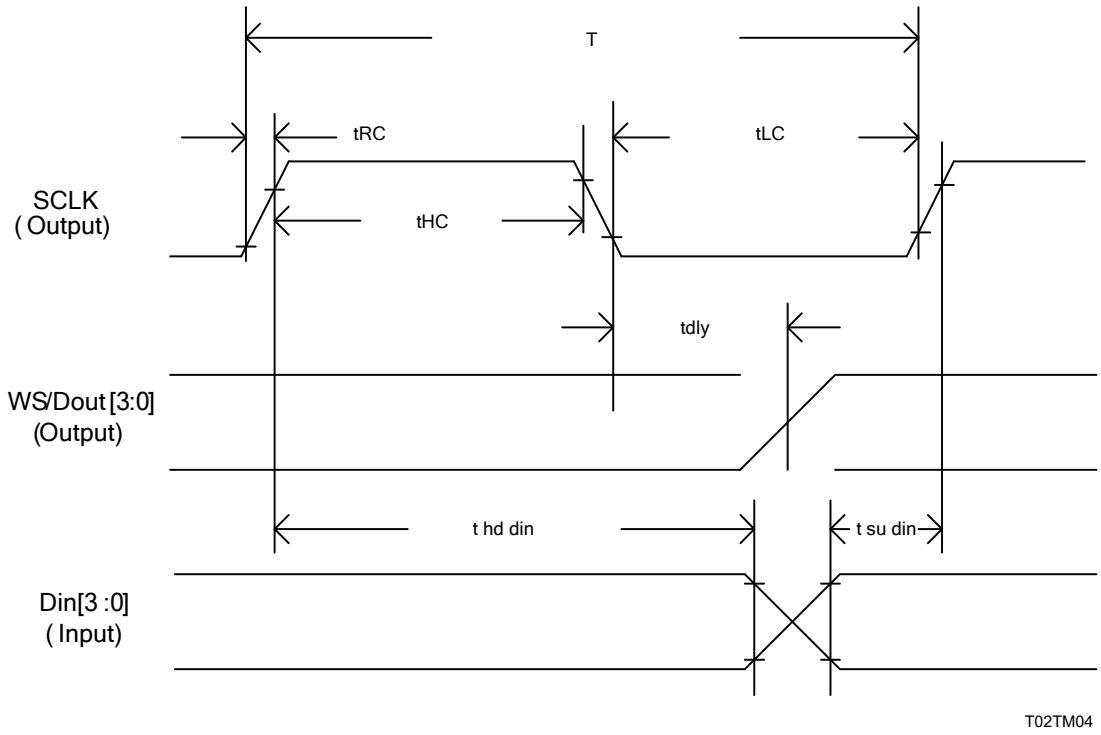


Table 10-1 Audio I2S/TDM Timing Specification, Transmitter, Master Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	Clock period	10			ns
tHC	High level of SCLK	0.4			T
tLC	Low level of SCLK	0.4			T
tRC	Edge time of SCLK			0.8	ns
tdly	Delay from SCLK to WS	-2	3	5	
tsuin	Setup time of WS/Din	4			ns
thdin	Hold time of WS/Din	4			ns

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Figure 10-20 I2S/TDM Timing Diagram, Slave Mode

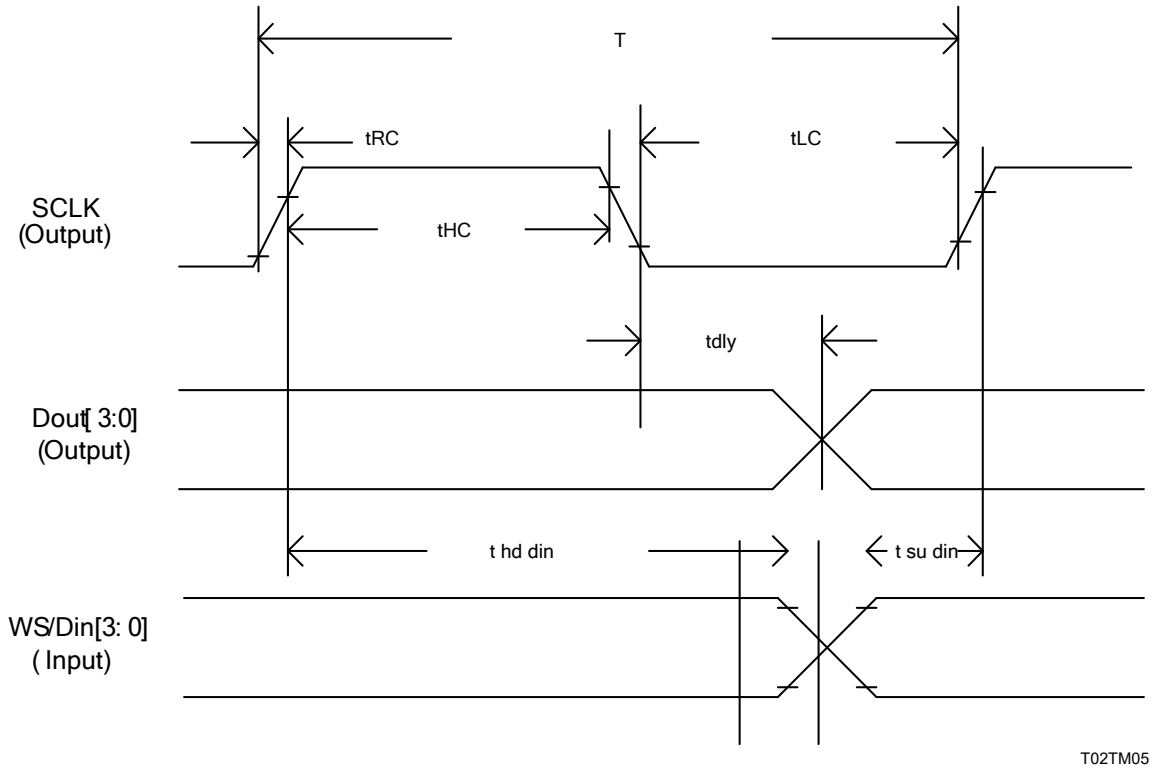


Table 10-2 Audio I2S/TDM Timing Specification, Transmitter, Slave Mode

Symbol	Parameter	Min	Typ	Max	Unit
T(out)	Clock period	40			ns
T(in)	Clock period	10			ns
tHC	High level of SCLK	0.4			T
tLC	Low level of SCLK	0.4			T
tRC	Edge time of SCLK			0.8	ns
tsu in	Setup time of WS/Din	4			ns
thd in	Hold time of WS/Din	4			ns
tdly	Delay between SCLK and Dout	7	12	15	ns

10.10 Register Description

For Below registers:

Registers	Base Address	Range
AUDIO_TOP	0xFE33_0000	4KB
PDM	0xFE33_1000	1KB
LOCKER	0xFE33_1400	1KB

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Registers	Base Address	Range
VAD	0xFE33_1800	1KB
RESAMPLE_A	0xFE33_1C00	1KB
EQDRC	0xFE33_2000	4KB
RESAMPLE_B	0xFFE3_4000	1KB
LOCKER_B	0xFFE3_4400	1KB

Each register final address = module base address+ address * 4

10.10.1 CLK/RESET Registers

Table 10-3 EE_AUDIO_CLK_GATE_EN0 10'h00

Bits	R/W	Default	Description
31	R/W	0x0000-0000	frhdmirx, 0:disable; 1: enable;
30	R/W		fratv, 0:disable; 1: enable;
29	R/W		Spdifin_lb, 0:disable; 1: enable;
28	R/W		Audio locker, 0:disable; 1: enable;
27	R/W		tovad, 0:disable; 1: enable;
26	R/W		resampleB, 0:disable; 1: enable;
25	R/W		reserved
24	R/W		reserved
23	R/W		reserved
22	R/W		eqdrc, 0:disable; 1: enable;
21	R/W		spdifoutB, 0:disable; 1: enable;
20	R/W		reserved
19	R/W		reserved
18	R/W		resampleA, 0:disable; 1: enable;
17	R/W		spdifout, 0:disable; 1: enable;
16	R/W		spdifin, 0:disable; 1: enable;
15	R/W		loopbackA, 0:disable; 1: enable;
14	R/W		toddrc, 0:disable; 1: enable;
13	R/W		toddrb, 0:disable; 1: enable;
12	R/W		toddra, 0:disable; 1: enable;
11	R/W		frddrc, 0:disable; 1: enable;
10	R/W		frddrb, 0:disable; 1: enable;
9	R/W		frddra, 0:disable; 1: enable;
8	R/W		tdmoutc, 0:disable; 1: enable;

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Bits	R/W	Default	Description
7	R/W		tdmoutb, 0:disable; 1: enable;
6	R/W		tmdouta, 0:disable; 1: enable;
5	R/W		tdminlb, 0:disable; 1: enable;
4	R/W		tdminc, 0:disable; 1: enable;
3	R/W		tdminb, 0:disable; 1: enable;
2	R/W		tdmina, 0:disable; 1: enable;
1	R/W		pdm, 0:disable; 1: enable;
0	R/W		ddr_arb, 0:disable; 1: enable;

Table 10-4 EE_AUDIO_CLK_GATE_EN1 10'h01

Bits	R/W	Default	Description
31:3	R/W	0x00000000	reserved
8	R/W		locker_b
7	R/W		resampleb_old
6	R/W		earcrx
5	R/W		earctx
4	R/W		toddrE
3	R/W		frddrE
2	R/W		loopbackB, 0:disable; 1: enable;
1	R/W		toddrd, 0:disable; 1: enable;
0	R/W		frddrd, 0:disable; 1: enable;

Table 10-5 EE_AUDIO_MCLK_A_CTRL 10'h02

Bits	R/W	Default	Description
31	R/W	0x0000-0000	clk_en, 0:disable; 1: enable;
30	R/W		Force_oscin, 0:disable; 1: force clock source as oscin(24M);
26:24	R/W		clk_sel, 0:mp0_pll; 1:mp1_pll; 2:mp2_pll; 3:mp3_pll; 4:hifi_pll; 5:fclk_div3(666M); 6:fclk_div4(500M); 7:cts_oscin(24M);
15:0	R/W		clk_div, the frequency of mclk = pll/(clk_div+1);

EE_AUDIO_MCLK_B_CTRL 10'h03

Same as EE_AUDIO_MCLK_A_CTRL.

EE_AUDIO_MCLK_C_CTRL 10'h04

Same as EE_AUDIO_MCLK_A_CTRL.

EE_AUDIO_MCLK_D_CTRL 10'h05

Same as EE_AUDIO_MCLK_A_CTRL.

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EE_AUDIO_MCLK_E_CTRL 10'h06

Same as EE_AUDIO_MCLK_A_CTRL.

EE_AUDIO_MCLK_F_CTRL 10'h07

Same as EE_AUDIO_MCLK_A_CTRL.

Table 10-6 EE_AUDIO_SW_RESET0 10'h0A

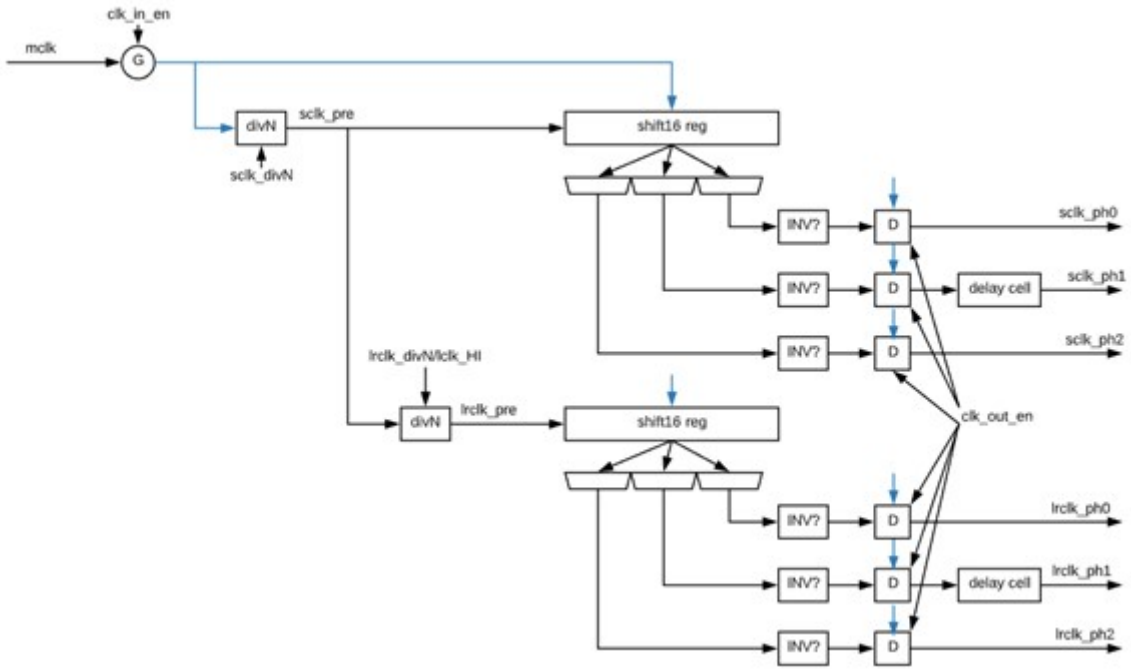
Bits	R/W	Default	Description
31	R/W	0	Frhdmirx
30	R/W	0	Fratv
29	R/W	0	Spdifin_lb
28	R/W	0	Locker
27	R/W	0	Tovad
26	R/W	0	resampleB
25	R/W	0	clk tree
24	R/W	0	tohdmitx
23	R/W	0	toacodec
22	R/W	0	toram
21	R/W	0	powdet
20	R/W	0	ddrarb
19	R/W	0	resample
18	R/W	0	eqdrc
17	R/W	0	spdifin
16	R/W	0	spdifoutB
15	R/W	0	spdifout
14	R/W	0	tdmoutc
13	R/W	0	tdmoutb
12	R/W	0	tdmouta
11	R/W	0	frddrc
10	R/W	0	frddrb
9	R/W	0	frddra
8	R/W	0	toddrc
7	R/W	0	toddrb
6	R/W	0	toddra
5	R/W	0	loopback
4	R/W	0	tdmin_lb
3	R/W	0	tdminc
2	R/W	0	tdminb
1	R/W	0	tdmina
0	R/W	0	pdm

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Table 10-7 EE_AUDIO_SW_RESET1 10'h0B

Bits	R/W	Default	Description
8	R/W	0	lockerB
7	R/W	0	resampleB_old
6	R/W	0	earcRX
5	R/W	0	earcTX
4	R/W	0	frddrE
3	R/W	0	toddrE
2	R/W	0	loopbackB
1	R/W	0	toddrd
0	R/W	0	frddrd

Table 10-8 EE_AUDIO_MST_A_SCLK_CTRL0 10'h10



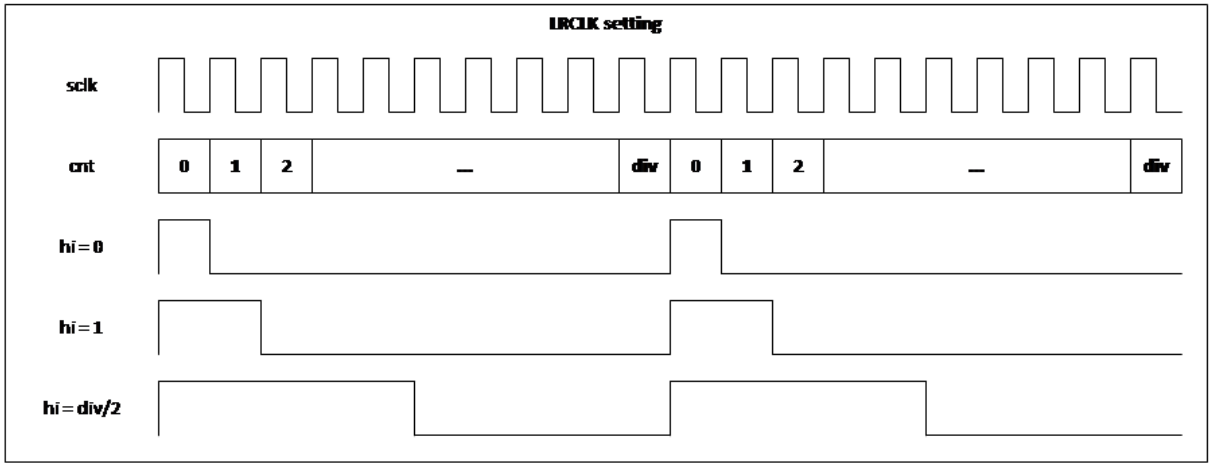
Bits	R/W	Default	Description
31	R/W	0x0000-0000	clk_in_en, 0:disable; 1: enable;
30	R/W		clk_out_en, 0:disable; 1: enable;
29:20	R/W		sclk_divN, the frequency of sclk = mclk/(sclk_divN+1);
19:10	R/W		lrclk_hi, duty cycle of LRCLK, less than lrclk_div; example 0: lrclk_hi = 1, LRCLK will only keep one cycle; example 1: lrclk_hi = lrclk_div/2, LRCLK will be 50/50 duty cycle;
9:0	R/W		lrclk_divN, the frequency of lrclk = sclk/(lrclk_divN+1);

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Table 10-9 EE_AUDIO_MST_A_SCLK_CTRL1 10'h11

Bits	R/W	Default	Description
31:28	R/W	0x0000-0000	sclk_ph0_sel, select from sclk_delay_line(depth is 16)
27:24	R/W		lrclk_ph0_sel, select from lrclk_delay_line(depth is 16)
23:20	R/W		sclk_ph1_sel, select from sclk_delay_line(depth is 16)
19:16	R/W		lrclk_ph1_sel, select from lrclk_delay_line(depth is 16)
15:12	R/W		sclk_ph2_sel, select from sclk_delay_line(depth is 16)
11:8	R/W		lrclk_ph2_sel, select from lrclk_delay_line(depth is 16)
5:0	R/W		clk_inv, invert clk; [5]: lrclk_ph2; [4]: sclk_ph2; [3]: lrclk_ph1; [2]: sclk_ph1; [1]: lrclk_ph0; [0]: sclk_ph0;

Figure 10-21 LRCLK Setting



EE_AUDIO_MST_B_SCLK_CTRL0 10'h12

Same as EE_AUDIO_MST_A_SCLK_CTRL0

EE_AUDIO_MST_B_SCLK_CTRL1 10'h13

Same as EE_AUDIO_MST_A_SCLK_CTRL1

EE_AUDIO_MST_C_SCLK_CTRL0 10'h14

Same as EE_AUDIO_MST_A_SCLK_CTRL0

EE_AUDIO_MST_C_SCLK_CTRL1 10'h15

Same as EE_AUDIO_MST_A_SCLK_CTRL1

EE_AUDIO_MST_D_SCLK_CTRL0 10'h16

Same as EE_AUDIO_MST_A_SCLK_CTRL0

EE_AUDIO_MST_D_SCLK_CTRL1 10'h17

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Same as EE_AUDIO_MST_A_SCLK_CTRL1

EE_AUDIO_MST_E_SCLK_CTRL0 10'h18

Same as EE_AUDIO_MST_A_SCLK_CTRL0

EE_AUDIO_MST_E_SCLK_CTRL1 10'h19

Same as EE_AUDIO_MST_A_SCLK_CTRL1

EE_AUDIO_MST_F_SCLK_CTRL0 10'h1a

Same as EE_AUDIO_MST_A_SCLK_CTRL0

EE_AUDIO_MST_F_SCLK_CTRL1 10'h1b

Same as EE_AUDIO_MST_A_SCLK_CTRL1

Table 10-10 EE_AUDIO_MST_DLY_CTRL0 10'h1c

Bits	R/W	Default	Description
31:24	R/W	0x00000000	reserved
23:20	R/W		mst_sclk_f_ph1_dly_sel;
19:16	R/W		mst_sclk_e_ph1_dly_sel;
15:12	R/W		mst_sclk_d_ph1_dly_sel;
11:8	R/W		mst_sclk_c_ph1_dly_sel;
7:4	R/W		mst_sclk_b_ph1_dly_sel;
3:0	R/W		mst_sclk_a_ph1_dly_sel;

Table 10-11 EE_AUDIO_MST_DLY_CTRL1 10'h1d

Bits	R/W	Default	Description
31:24	R/W	0x00000000	reserved
23:20	R/W		mst_lrclk_f_ph1_dly_sel;
19:16	R/W		mst_lrclk_e_ph1_dly_sel;
15:12	R/W		mst_lrclk_d_ph1_dly_sel;
11:8	R/W		mst_lrclk_c_ph1_dly_sel;
7:4	R/W		mst_lrclk_b_ph1_dly_sel;
3:0	R/W		mst_lrclk_a_ph1_dly_sel;

Table 10-12 EE_AUDIO_CLK_TDMIN_A_CTRL 10'h20

Bits	R/W	Default	Description
31	R/W	0x0000-0000	clk_in_en, 0:disable; 1: enable;
30	R/W		clk_out_en, 0:disable; 1: enable;
29	R/W		sclk_inv, 0:not revert; 1: revert clock;

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Bits	R/W	Default	Description
27:24	R/W		sclk_sel, 0:mst_a_sclk_ph1; 1:mst_b_sclk_ph1; 2:mst_c_sclk_ph1; 3:mst_d_ sclk_ph1; 4:mst_e_sclk_ph1; 5:mst_f_sclk_ph1; 6:i_slv_sclk_a 7:i_slv_sclk_b 8:i_slv_sclk_c 9::i_slv_sclk_d ; 10:i_slv_sclk_e ; 11:i_slv_sclk_f ; 12:i_slv_sclk_g ; 13:i_slv_sclk_h ; 14:i_slv_sclk_i ; 15:i_slv_sclk_j ;
23:20	R/W		lrclk_sel, 0:mst_a_lrclk_ph1; 1:mst_b_lrclk_ph1; 2:mst_c_lrclk_ph1; 3:mst_d_ lrclk_ph1; 4:mst_e_lrclk_ph1; 5:mst_f_lrclk_ph1; 6:i_slv_lrclk_a 7:i_slv_lrclk_b 8:i_slv_lrclk_c 9::i_slv_lrclk_d ; 10:i_slv_lrclk_e ; 11:i_slv_lrclk_f ; 12:i_slv_lrclk_ g ; 13:i_slv_lrclk_h ; 14:i_slv_lrclk_i ; 15:i_slv_lrclk_j ;

EE_AUDIO_CLK_TDMIN_B_CTRL 10'h21

Same as EE_AUDIO_CLK_TDMIN_A_CTRL

EE_AUDIO_CLK_TDMIN_C_CTRL 10'h22

Same as EE_AUDIO_CLK_TDMIN_A_CTRL

EE_AUDIO_CLK_TDMIN_LB_CTRL 10'h23

Same as EE_AUDIO_CLK_TDMIN_A_CTRL

Table 10-13 EE_AUDIO_CLK_TDMOUT_A_CTRL 10'h24

Bits	R/W	Default	Description
31	R/W	0x0000-0000	clk_in_en, 0:disable; 1: enable;
30	R/W		clk_out_en, 0:disable; 1: enable;
29	R/W		sclk_inv, 0:not revert; 1: revert clock;
28	R/W		Sclk_ws_inv, for the capture ws sclk; 0: not revert; 1: revert clock;

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Bits	R/W	Default	Description
27:24	R/W		sclk_sel, 0:mst_a_sclk_ph1; 1:mst_b_sclk_ph1; 2:mst_c_sclk_ph1; 3:mst_d_sclk_ph1; 4:mst_e_sclk_ph1; 5:mst_f_sclk_ph1; 6:i_slv_sclk_a ; 7:i_slv_sclk_b ; 8:i_slv_sclk_c ; 9::i_slv_sclk_d ; 10:i_slv_sclk_e ; 11:i_slv_sclk_f ; 12:i_slv_sclk_g ; 13:i_slv_sclk_h ; 14:i_slv_sclk_i ; 15:i_slv_sclk_j ;
23:20	R/W		lrclk_sel, 0:mst_a_lrclk_ph1; 1:mst_b_lrclk_ph1; 2:mst_c_lrclk_ph1; 3:mst_d_lrclk_ph1; 4:mst_e_lrclk_ph1; 5:mst_f_lrclk_ph1; 6:i_slv_lrclk_a ; 7:i_slv_lrclk_b ; 8:i_slv_lrclk_c ; 9::i_slv_lrclk_d ; 10:i_slv_lrclk_e ; 11:i_slv_lrclk_f ; 12:i_slv_lrclk_g ; 13:i_slv_lrclk_h ; 14:i_slv_lrclk_i ; 15:i_slv_lrclk_j ;

EE_AUDIO_CLK_TDMOUT_B_CTRL 10'h25

Same as EE_AUDIO_CLK_TDMOUT_A_CTRL

EE_AUDIO_CLK_TDMOUT_C_CTRL 10'h26

Same as EE_AUDIO_CLK_TDMOUT_A_CTRL

Table 10-14 EE_AUDIO_CLK_SPDIFIN_CTRL 10'h27

Bits	R/W	Default	Description
31	R/W	0x0000-0000	clk_en, 0:disable; 1: enable;
30	R/W		Force_oscin, 0:disable; 1: force clock source as oscin(24M);

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Bits	R/W	Default	Description
27:24	R/W		clk_sel, 0:mp0_pll; 1:mp1_pll; 2:mp2_pll; 3:mp3_pll; 4:hifi_pll; 5:fclk_div3(666M); 6:fclk_div4(500M); 7:fclk_div5(400M); 8:mst_a_sclk_ph1; 9:mst_b_sclk_ph1; 10:mst_c_sclk_ph1; 11:mst_d_sclk_ph1; 12:mst_e_sclk_ph1; 13:mst_f_sclk_ph1;
7:0	R/W		clk_div, set 7 if need div 8

Table 10-15 EE_AUDIO_CLK_SPDIFOUT_CTRL 10'h28

Bits	R/W	Default	Description
31	R/W	0x0000-0000	clk_en, 0:disable; 1: enable;
30	R/W		Force_oscin, 0:disable; 1: force clock source as oscin(24M);
27:24	R/W		clk_sel, 0:mp0_pll; 1:mp1_pll; 2:mp2_pll; 3:mp3_pll; 4:hifi_pll; 5:fclk_div3(666M); 6:fclk_div4(500M); 7:cts_oscin(24M) 8:mst_a_sclk_ph2; 9:mst_b_sclk_ph2; 10:mst_c_sclk_ph2; 11:mst_d_sclk_ph2; 12:mst_e_sclk_ph2; 13:mst_f_sclk_ph2;
9:0	R/W		clk_div, set 7 if need div 8

Table 10-16 EE_AUDIO_CLK_RESAMPLEA_CTRL 10'h29

Bits	R/W	Default	Description
31	R/W	0x0000-0000	clk_ en, 0:disable; 1: enable;
30	R/W		Force_oscin, 0:disable; 1: force clock source as oscin(24M);

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Bits	R/W	Default	Description
27:24	R/W		sclk_sel, 0:mst_a_mclk; 1:mst_b_mclk; 2:mst_c_mclk; 3:mst_d_mclk; 4:mst_e_mclk; 5:mst_f_mclk; 6:i_slv_sclk_a ; 7:i_slv_sclk_b ; 8:i_slv_sclk_c ; 9::i_slv_sclk_d ; 10:i_slv_sclk_e ; 11:i_slv_sclk_f ; 12:i_slv_sclk_g ; 13:i_slv_sclk_h ; 14:i_slv_sclk_i ; 15:i_slv_sclk_j ;
7:0	R/W		clk_div, set 7 if need div 8

Table 10-17 EE_AUDIO_CLK_LOCKER_CTRL 10'h2a

Bits	R/W	Default	Description
31	R/W	0x0000-0000	lock_out_clk; 0:disable; 1:enable;
30	R/W		Force_oscin for lock_out_clk, 0:disable; 1: force clock source as oscin(24M);
27:24	R/W		sclk_sel, 0:mst_a_mclk; 1:mst_b_mclk; 2:mst_c_mclk; 3:hdmirx_i2s_sclk; 4:world_sync; 5:hdmirx_find_z; 6:i_slv_sclk_a 7:i_slv_sclk_b; 8:i_slv_sclk_c; 9::i_slv_sclk_d ; 10:i_slv_sclk_e ; 11:earcrx_pll_dmac_ck; 12:resample_b_vld; 13:resample_a_vld; 14:earcrx find x/y/z; 15:spdifin find x/y/z ;
23:16	R/W		clk_div, lock_out_clk, set 7 if need div 8;
15	R/W		clk_en, lock_in_clk; 0:disable; 1:enable;
14	R/W		Force_oscin for lock_in_clk, 0:disable; 1: force clock source as oscin(24M);
11:8	R/W		clk_sel, lock_in_clk; 0:mst_a_mclk; 1:mst_b_mclk; 2:mst_c_mclk; 3:mst_d_mclk; 4:mst_e_mclk; 5:mst_f_mclk; 6:i_slv_sclk_a; 7:i_slv_sclk_b 8:i_slv_sclk_c; 9::i_slv_sclk_d; 10:i_slv_sclk_e; 11:earcrx_pll_dmac_ck; 12:resample_b_vld; 13:resample_a_vld; 14:earcrx find x/y/z; 15:spdifin find x/y/z;
7:0	R/W		clk_div, lock_in_clk, set 7 if need div 8

Table 10-18 EE_AUDIO_CLK_PDMIN_CTRL0 10'h2b

Bits	R/W	Default	Description
31	R/W	0x0000-0000	clk_en, 0:disable; 1: enable;
30	R/W		Force_oscin, 0:disable; 1: force clock source as oscin(24M);

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Bits	R/W	Default	Description
26:24	R/W		clk_sel, 0:mp0_pll; 1:mp1_pll; 2:mp2_pll; 3:mp3_pll; 4:hifi_pll; 5:fclk_div3(666M); 6:fclk_div4(500M); 7:cts_oscin(24M);
15:0	R/W		clk_div, set 7 if need div 8

Table 10-19 EE_AUDIO_CLK_PDMIN_CTRL1 10'h2c

Bits	R/W	Default	Description
31	R/W	0x0000-0000	clk_en, 0:disable; 1: enable;
30	R/W		Force_oscin, 0:disable; 1: force clock source as oscin(24M);
26:24	R/W		clk_sel; 0:cts_oscin(24M); 1:mp1_pll; 2:mp2_pll; 3:mp3_pll; 4:hifi_pll; 5:fclk_div3(666M); 6:fclk_div4(500M); 7:fclk_div5(400M);
15:0	R/W		clk_div, set 7 if need div 8

Table 10-20 EE_AUDIO_CLK_SPDIFOUT_B_CTRL 10'h2d

Bits	R/W	Default	Description
31	R/W	0x0000-0000	clk_en, 0:disable; 1: enable;
30	R/W		Force_oscin, 0:disable; 1: force clock source as oscin(24M);
26:24	R/W		clk_sel, 0:mp0_pll; 1:mp1_pll; 2:mp2_pll; 3:mp3_pll; 4:hifi_pll; 5:fclk_div3(666M); 6:fclk_div4(500M); 7:cts_oscin(24M); 8:mst_a_sclk_ph1; 9:mst_b_sclk_ph1; 10:mst_c_sclk_ph1; 11:mst_d_sclk_ph1; 12:mst_e_sclk_ph1; 13:mst_f_sclk_ph1;
9:0	R/W		clk_div, set 7 if need div 8

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Table 10-21 EE_AUDIO_CLK_RESAMPLEB_CTRL 10'h2E

Bits	R/W	Default	Description
31	R/W	0x0000-0000	clk_ en, 0:disable; 1: enable;
30	R/W		Force_oscin, 0:disable; 1: force clock source as oscin(24M);
27:24	R/W		sclk_sel, 0:mst_a_mclk; 1:mst_b_mclk; 2:mst_c_mclk; 3:mst_d_mclk; 4:mst_e_mclk; 5:mst_f_mclk; 6:i_slv_sclk_a ; 7:i_slv_sclk_b ; 8:i_slv_sclk_c ; 9::i_slv_sclk_d ; 10:i_slv_sclk_e ; 11:i_slv_sclk_f ; 12:i_slv_sclk_g ; 13:i_slv_sclk_h ; 14:i_slv_sclk_i ; 15:i_slv_sclk_j ;
7:0	R/W		clk_div, set 7 if need div 8

Table 10-22 EE_AUDIO_CLK_SPDIFIN_LB_CTRL 10'h2F

Bits	R/W	Default	Description
31	R/W	0x0000-0000	clk_en, 0:disable; 1: enable;
30	R/W		Clk_sel: 0: spdif_out_a clk; 1: spdif_out_b clk;
29	R/W		Clk_inv

Table 10-23 EE_AUDIO_CLK_EQDRC_CTRL 10'h30

Bits	R/W	Default	Description
31	R/W	0x0000-0000	clk_en, 0:disable; 1: enable;
30	R/W		Force_oscin, 0:disable; 1: force clock source as oscin(24M);
26:24	R/W		0:cts_oscin(24M) 1:mp1_pll; 2:mp2_pll; 3:mp3_pll; 4:hifi_pll; 5:fclk_div3(666M); 6:fclk_div4(500M); 7:fclk_div5(400M)
15:0	R/W		clk_div, set 7 if need div 8

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Table 10-24 EE_AUDIO_CLK_VAD_CTRL 10'h31

Bits	R/W	Default	Description
31	R/W	0x0000-0000	clk_ en, 0:disable; 1: enable;
30	R/W		Force_oscin, 0:disable; 1: force clock source as oscin(24M);
26:24	R/W		0:cts_oscin(24M); 1:mp1_pll; 2:mp2_pll; 3:mp3_pll; 4:hifi_pll; 5:fclk_div3(666M); 6:fclk_div4(500M); 7:fclk_div5(400M)
15:0	R/W		clk_div, set 7 if need div 8

Table 10-25 EE_AUDIO_EARCTX_CMDC_CLK_CTRL 10'h32

Bits	R/W	Default	Description
31	R/W	0x00000000	clk_en, 0:disable; 1: enable;
30	R/W		Force_oscin, 0:disable; 1: force clock source as oscin(24M);
26:24	R/W		0:cts_oscin(24M); 1:mp1_pll; 2:mp2_pll; 3:mp3_pll; 4:hifi_pll; 5:fclk_div3(666M); 6:fclk_div4(500M); 7:fclk_div5(400M)
15:0	R/W		clk_div, set 7 if need div 8

Table 10-26 EE_AUDIO_EARCTX_DMAC_CLK_CTRL 10'h33

Bits	R/W	Default	Description
31	R/W	0x00000000	clk_en, 0:disable; 1: enable;
30	R/W		Force_oscin, 0:disable; 1: force clock source as oscin(24M);
26:24	R/W		0:cts_oscin(24M); 1:mp1_pll; 2:mp2_pll; 3:mp3_pll; 4:hifi_pll; 5:fclk_div3(666M); 6:fclk_div4(500M); 7:fclk_div5(400M)
15:0	R/W		clk_div, set 7 if need div 8

Table 10-27 EE_AUDIO_EARCRX_CMDC_CLK_CTRL 10'h34

Bits	R/W	Default	Description
31	R/W	0x00000000	clk_en, 0:disable; 1: enable;
30	R/W		Force_oscin, 0:disable; 1: force clock source as oscin(24M);
26:24	R/W		0:cts_oscin(24M); 1:mp1_pll; 2:mp2_pll; 3:mp3_pll; 4:hifi_pll; 5:fclk_div3(666M); 6:fclk_div4(500M); 7:fclk_div5(400M)
15:0	R/W		clk_div, set 7 if need div 8

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Table 10-28 EE_AUDIO_EARCRX_DMAC_CLK_CTRL 10'h35

Bits	R/W	Default	Description
31	R/W	0x00000000	clk_en, 0:disable; 1: enable;
30	R/W		Force_oscin, 0:disable; 1: force clock source as oscin(24M);
26:24	R/W		0:cts_oscin(24M); 1:mp1_pll; 2:mp2_pll; 3:mp3_pll; 4:hifi_pll; 5:fclk_div3(666M); 6: fclk_div4(500M); 7:fclk_div5(400M)
15:0	R/W		clk_div, set 7 if need div 8

Table 10-29 EE_AUDIO_CLK_LOCKERB_CTRL 10'h36

Bits	R/W	Default	Description
31	R/W	0x00000000	lockb_out_clk; 0:disable; 1:enable;
30	R/W		Force_oscin for lock_out_clk, 0:disable; 1: force clock source as oscin(24M);
27:24	R/W		sclk_sel, 0:mst_a_mclk; 1:mst_b_mclk; 2:mst_c_mclk; 3:hdmirx_i2s_sclk; 4:world_sync; 5:hdmirx_find_z; 6:i_slv_sclk_a 7:i_slv_sclk_b 8:i_slv_sclk_c 9::i_slv_sclk_d ; 10:i_slv_sclk_e ; 11:earcrx_pll_dmac_ck ; 12:resample_b_vld; 13:resample_a_vld ; 14:earcrx find x/y/z ; 15:spdifin find x/y/z ;
23:16	R/W		clk_div, lock_out_clk, set 7 if need div 8
15	R/W		clk_en, lock_in_clk; 0:disable; 1:enable;
14	R/W		Force_oscin for lock_in_clk, 0:disable; 1: force clock source as oscin(24M);
11:8	R/W		clk_sel,lock_inb_clk; 0:mst_a_mclk; 1:mst_b_mclk; 2:mst_c_mclk; 3:mst_d_mclk; 4:mst_e_mclk; 5:mst_f_mclk; 6:i_slv_sclk_a; 7:i_slv_sclk_b; 8:i_slv_sclk_c; 9::i_slv_sclk_d; 10:i_slv_sclk_e; 11:earcrx_pll_dmac_ck; 12:resample_b_vld; 13:resample_a_vld; 14:earcrx find x/y/z; 15:spdifin find x/y/z;
7:0	R/W		clk_div, lock_in_clk, set 7 if need div 8

10.10.2 OTHER Registers

Audio include 64 exception irq, the list is below.

Bits	From	Description
63	TODDR_A	CHNUM_SYNC_ERR1: detect write new ch when pop buffer;
62	TODDR_A	CHNUM_SYNC_ERR0: miss CH (cur_chnum_id != reg_chnum_id)
61	TODDR_B	CHNUM_SYNC_ERR1: detect write new ch when pop buffer;
60	TODDR_B	CHNUM_SYNC_ERR0: miss CH (cur_chnum_id != reg_chnum_id)
59	TODDR_C	CHNUM_SYNC_ERR1: detect write new ch when pop buffer;
58	TODDR_C	CHNUM_SYNC_ERR0: miss CH (cur_chnum_id != reg_chnum_id)
57	TODDR_D	CHNUM_SYNC_ERR1: detect write new ch when pop buffer;

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Bits	From	Description
56	TODDR_D	CHNUM_SYNC_ERR0: miss CH (cur_chnum_id != reg_chnum_id)
55	TODDR_E	CHNUM_SYNC_ERR1: detect write new ch when pop buffer;
54	TODDR_E	CHNUM_SYNC_ERR0: miss CH (cur_chnum_id != reg_chnum_id)
53		
52		
51		
50		
49	PDMIN	HPF NOT FINISH
48	PDMIN	HCIC NOT FINISH
47		
46	TDMIN_A	AFIFO OVERFLOW
45	TDMIN_A	SLOT_CNT_ERR, SLOT CNT between two WS_RISE didn't equal to REG_ SLOT_NUM
44	TDMIN_A	BIT_CNT_ERR, BIT CNT between two SLOT didn't equal to REG_BIT_NUM
43		
42	TDMIN_B	AFIFO OVERFLOW
41	TDMIN_B	SLOT_CNT_ERR, SLOT CNT between two WS_RISE didn't equal to REG_ SLOT_NUM
40	TDMIN_B	BIT_CNT_ERR, BIT CNT between two SLOT didn't equal to REG_BIT_NUM
39		
38	TDMIN_C	AFIFO OVERFLOW
37	TDMIN_C	SLOT_CNT_ERR, SLOT CNT between two WS_RISE didn't equal to REG_ SLOT_NUM
36	TDMIN_C	BIT_CNT_ERR, BIT CNT between two SLOT didn't equal to REG_BIT_NUM
35	DDR_ARB	locked for one request for long time (>time_out_cnt)
34	TDMIN_LB	AFIFO OVERFLOW
33	TDMIN_LB	SLOT_CNT_ERR, SLOT CNT between two WS_RISE didn't equal to REG_ SLOT_NUM
32	TDMIN_LB	BIT_CNT_ERR, BIT CNT between two SLOT didn't equal to REG_BIT_NUM
31	LOOPBACK_A	ORIG DATA,CHNUM_SYNC_ERR1: detect write new ch when pop buffer;
30	LOOPBACK_A	ORIG DATA,CHNUM_SYNC_ERR0: miss CH (cur_chnum_id != reg_chnum_id)
29	LOOPBACK_A	INSERT DATA,CHNUM_SYNC_ERR1: detect write new ch when pop buffer;
28	LOOPBACK_A	INSERT DATA,CHNUM_SYNC_ERR0: miss CH (cur_chnum_id != reg_chnum_ id)
27	LOOPBACK_B	ORIG DATA,CHNUM_SYNC_ERR1: detect write new ch when pop buffer;
26	LOOPBACK_B	ORIG DATA,CHNUM_SYNC_ERR0: miss CH (cur_chnum_id != reg_chnum_id)
25	LOOPBACK_B	INSERT DATA,CHNUM_SYNC_ERR1: detect write new ch when pop buffer;
24	LOOPBACK_B	INSERT DATA,CHNUM_SYNC_ERR0: miss CH (cur_chnum_id != reg_chnum_ id)

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Bits	From	Description
23	RESAMPLE_A	CHNUM_SYNC_ERR1: detect write new ch when pop buffer;
22	RESAMPLE_A	CHNUM_SYNC_ERR0: miss CH (cur_chnum_id != reg_chnum_id)
21	RESAMPLE_B	CHNUM_SYNC_ERR1: detect write new ch when pop buffer;
20	RESAMPLE_B	CHNUM_SYNC_ERR0: miss CH (cur_chnum_id != reg_chnum_id)
19		
18		
17	SPDIFIN	Reserved
16	SPDIFIN	afifo overflow
15	SPDIFIN	cyc_cnt err, <min
14	SPDIFIN	cyc_cnt err, > max
13	SPDIFIN	parity_err
12	SPDIFIN	bit_cnt err, >64
11	SPDIFIN	bit_cnt err, !=64
10	SPDIFIN	xyz_err
9	VAD	CHNUM_SYNC_ERR1: detect write new ch when pop buffer;
8	VAD	CHNUM_SYNC_ERR0: miss CH (cur_chnum_id != reg_chnum_id)
7		
6		
5		
4		
3		
2		
1		
0		

Table 10-30 EE_AUDIO_EXCEPTION_IRQ_STS0 10'h380

Bits	R/W	Default	Description
31	R	0x0000-0000	change to high by irq; change to low by clr;

Table 10-31 EE_AUDIO_EXCEPTION_IRQ_STS1 10'h381

Bits	R/W	Default	Description
31	R	0x00000000	change to high by irq; change to low by clr;

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Table 10-32 EE_AUDIO_EXCEPTION_IRQ_MASK0 10'h382

Bits	R/W	Default	Description
31	R	0x00000000	

Table 10-33 EE_AUDIO_EXCEPTION_IRQ_MASK1 10'h383

Bits	R/W	Default	Description
31	R/W	0x00000000	

Table 10-34 EE_AUDIO_EXCEPTION_IRQ_MODE0 10'h384

Bits	R/W	Default	Description
31	R/W	0x0000-0000	each bit: 0: pulse irq; 1: level irq;

Table 10-35 EE_AUDIO_EXCEPTION_IRQ_MODE1 10'h385

Bits	W	Default	Description
31	R/W	0x0000-0000	each bit: 0: pulse irq; 1: level irq;

Table 10-36 EE_AUDIO_EXCEPTION_IRQ_CLR0 10'h386

Bits	R/W	Default	Description
31	R/W	0x0000-0000	each bit can clear each sts bit

Table 10-37 EE_AUDIO_EXCEPTION_IRQ_CLR1 10'h387

Bits	R/W	Default	Description
31	R/W	0x0000-0000	each bit can clear each sts bit

Table 10-38 EE_AUDIO_EXCEPTION_IRQ_INV0 10'h388

Bits	R/W	Default	Description
31	R/W	0x00000000	each bit can invert irq

Table 10-39 EE_AUDIO_EXCEPTION_IRQ_INV1 10'h389

Bits	R/W	Default	Description
31	R/W	0x00000000	each bit can invert irq

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Table 10-40 EE_AUDIO_RSAMP_A_CHNUM_ID0 10'h350

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch3
23:16	R/W		ID of ch2
15:8	R/W		ID of ch1
7:0	R/W		ID of ch0

Table 10-41 EE_AUDIO_RSAMP_A_CHNUM_ID1 10'h351

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch7
23:16	R/W		ID of ch6
15:8	R/W		ID of ch5
7:0	R/W		ID of ch4

Table 10-42 EE_AUDIO_RSAMP_A_CHNUM_ID2 10'h352

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch11
23:16	R/W		ID of ch10
15:8	R/W		ID of ch9
7:0	R/W		ID of ch8

Table 10-43 EE_AUDIO_RSAMP_A_CHNUM_ID3 10'h353

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch15
23:16	R/W		ID of ch14
15:8	R/W		ID of ch13
7:0	R/W		ID of ch12

Table 10-44 EE_AUDIO_RSAMP_A_CHNUM_ID4 10'h354

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch19
23:16	R/W		ID of ch18
15:8	R/W		ID of ch17
7:0	R/W		ID of ch16

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Table 10-45 EE_AUDIO_RSAMP_A_CHNUM_ID5 10'h355

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch23
23:16	R/W		ID of ch22
15:8	R/W		ID of ch21
7:0	R/W		ID of ch20

Table 10-46 EE_AUDIO_RSAMP_A_CHNUM_ID5 10'h356

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch27
23:16	R/W		ID of ch26
15:8	R/W		ID of ch25
7:0	R/W		ID of ch24

Table 10-47 EE_AUDIO_RSAMP_A_CHNUM_ID7 10'h357

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch31
23:16	R/W		ID of ch30
15:8	R/W		ID of ch29
7:0	R/W		ID of ch28

Table 10-48 EE_AUDIO_RSAMP_A_CHNUM_MASK 10'h35E

Bits	R/W	Default	Description

23:16	R/W	0x0000-0000	for resample_C(B_old) stable mask, if set 1, will pull stable signal to low by different conditions
			bit3: resample_out_en changed(from 1 to 0 or from 0 to 1);
			bit2: reg_soft_reset = 1;
			bit1: resample_en_r changed(from 1 to 0 or from 0 to 1);
			bit0: resample_en changed(from 1 to 0 or from 0 to 1);

15:8	R/W		for resample_B stable mask, if set 1, will pull stable signal to low by different conditions
			bit3: reg_rsampl_en = 0;
			bit2: reg_rsamp_rst = 1;
			bit1: reg_output_en = 0;
			bit0:reg_module_bypass changed(from 0 to 1 or from 1 to 0)

7:0	R/W		for resample_A stable mask, if set 1, will pull stable signal to low by different conditions
			bit3: reg_rsampl_en = 0;
			bit2: reg_rsamp_rst = 1;
			bit1: reg_output_en = 0;
			bit0:reg_module_bypass changed(from 0 to 1 or from 1 to 0)

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Table 10-49 EE_AUDIO_RSAMP_A_CHSYNC_CTRL 10'h35F

Bits	R/W	Default	Description
31	R/W	0x0000-0000	bypass_n; 0: out=in; 1: sync data by chnum info;
30	R/W		sw_reset; 1: reset chnum_sync module
29	R/W		mode; 0: work as BUFF_MODE; 1: work as DROP_MODE;
28	R/W		id_se; 0: ID = input valid count; 1: ID= reg_id_***
27	R/W		fix_stable; 1: ignore stable info of input; 0: compensate dat by stable info;
26	R/W		debug_en0, for BUF_MODE only; 1: send chnum info from input; 0: generate new chnum info;
7:0	R/W		chnum_max; if input is 8ch, set this to 7;

EE_AUDIO_RSAMP_B_CHNUM_ID0 10'h360
EE_AUDIO_RSAMP_B_CHNUM_ID1 10'h361
EE_AUDIO_RSAMP_B_CHNUM_ID2 10'h362
EE_AUDIO_RSAMP_B_CHNUM_ID3 10'h363
EE_AUDIO_RSAMP_B_CHNUM_ID4 10'h364
EE_AUDIO_RSAMP_B_CHNUM_ID5 10'h365
EE_AUDIO_RSAMP_B_CHNUM_ID6 10'h366
EE_AUDIO_RSAMP_B_CHNUM_ID7 10'h367
EE_AUDIO_RSAMP_B_CHSYNC_CTRL 10'h36F

10.10.3 TODDR Registers

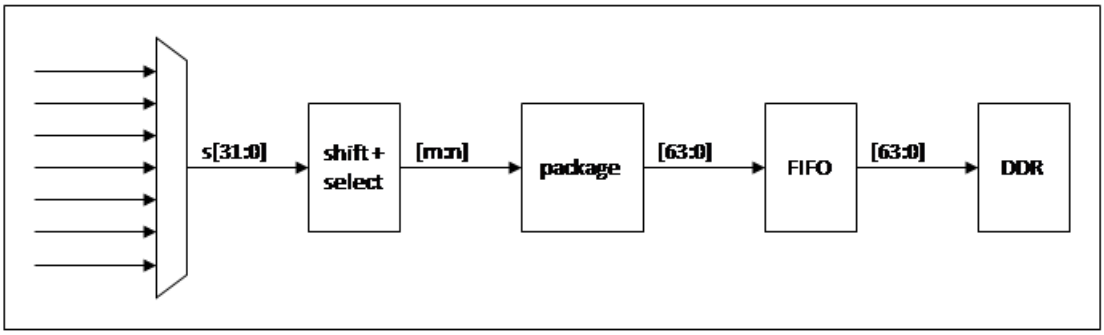
Table 10-50 EE_AUDIO_TODDR_A_CTRL0 10'h40

Bits	R/W	Default	Description
31	R/W	0x0000-0000	reg_toddr_en, 0: disable; 1: enable;
29	R/W		reg_ext_signed, 0: select write to only one buff (start_addr,finish_addr); 1: select write to two buff (start_addr,finish_addr) (start_addrb, finish_addrb);
28	R/W		reg_toddr_endian
27	R/W		Enable_sync_chnum; 1: start store data when first ch ;
26:24	R/W		reg_toddr_int_en
23:16	R/W		[23] : reserved; [22] : reserved; [21] : fifo overflow, write when fifocnt = depth; [20] : fifo overflow, read when fifocnt = 0; [19] : when write to ddr "int_addr" data (only once); [18] : when write to ddr "int_addr" data (repeat); [17] : when write to ddr address match "int_addr"; [16]: when write to ddr address match "finish_addr";
15:13	R/W		reg_toddr_sel, 0: combined data[m:n] without gap; like S0[m:n],S1[m:n],S2[m:n], … 1: combined data[m:n] as 16bits; like {S0[11:0],4'd0},{S1[11:0],4'd0}…

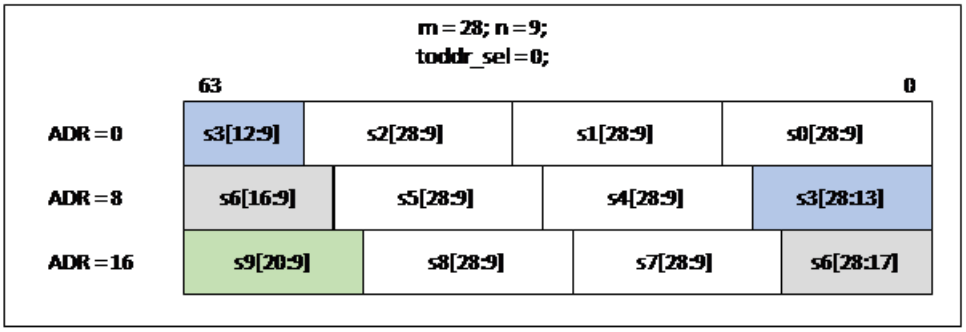
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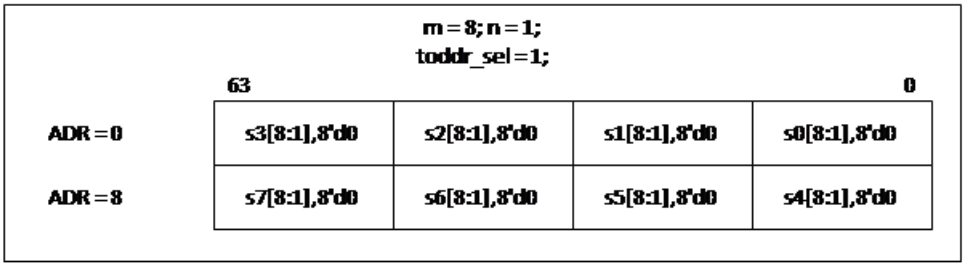
Bits	R/W	Default	Description
			2: combined data[m:n] as 16bits; like {4'd0,S0[11:0]},{4'd0,{S1[11:0]}… 3: combined data[m:n] as 32bits; like {S0[27:4],8'd0},{S1[27:4],8'd0}… 4: combined data[m:n] as 32bits; like {8'd0,S0[27:4]},{8'd0,{S1[27:4]}…
12:8	R/W		reg_toddr_m_sel, the msb positioin in data
7:3	R/W		reg_toddr_n_sel, the lsb position in data
2	R/W		Clear adr/cnt value which captured by vad frame sync
1	R/W		Clear adr/cnt value which captured by vadflag
0	R/W		Ddr bus ugt bit

We can change format before write to DDR: TODDR-format

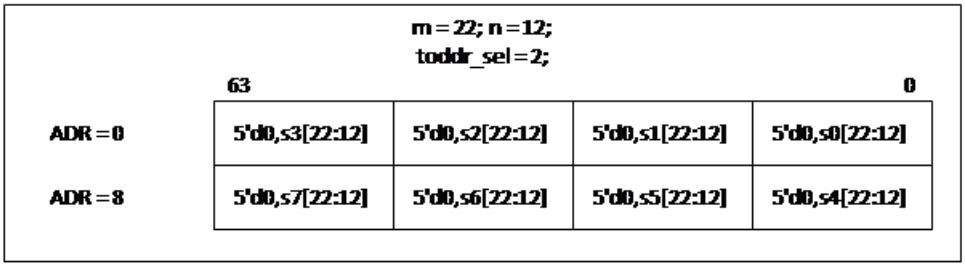


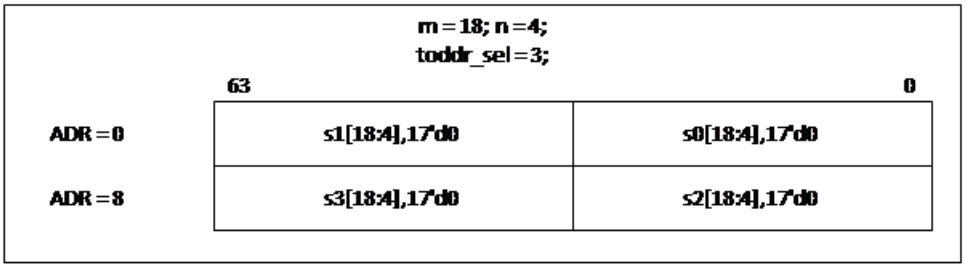
For example:





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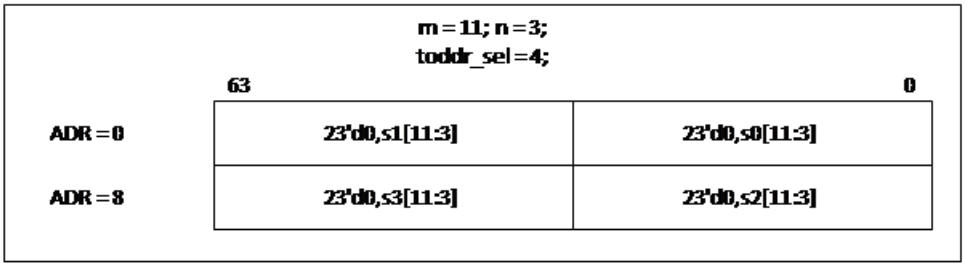


Table 10-51 EE_AUDIO_TODDR_A_CTRL1 10'h41

Bits	R/W	Default	Description
30:26	R/W	0x0000-0000	Src select: 0: tdmin_a; 1: tdmin_b; 2: tdmin_c; 3: spdifin; 4: pdmin; 5: fratv; 6: tdmin_lb; 7: loopback_a; 8: frhdmirx_spdif; 9: loopback_b; 10: spdifin_lb; 11:earc_rx_dmac 12:frhdmirx_dsd 13:resample_a 14:resample_b 15: vad; 16~31:reserved
27	R/W		Select from resample_A
26	R/W		Select from resample_B; need unselect resample_A;
25	R/W		force_finish; the value from 0-> 1: force finish by current address and jump to start_address;

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Bits	R/W	Default	Description
23:12	R/W		reg_fifo_start_rd_th, each time, when fifo_cnt greater than this register, control will start read data from fifo and write to DDR; write length is "reg_fifo_start_rd_th + 1" * 8bytes;
11:8	R/W		reg_status_sel, control status2 source;
7:0	R/W		reg_int_status_clr,clear each bits of int_status register

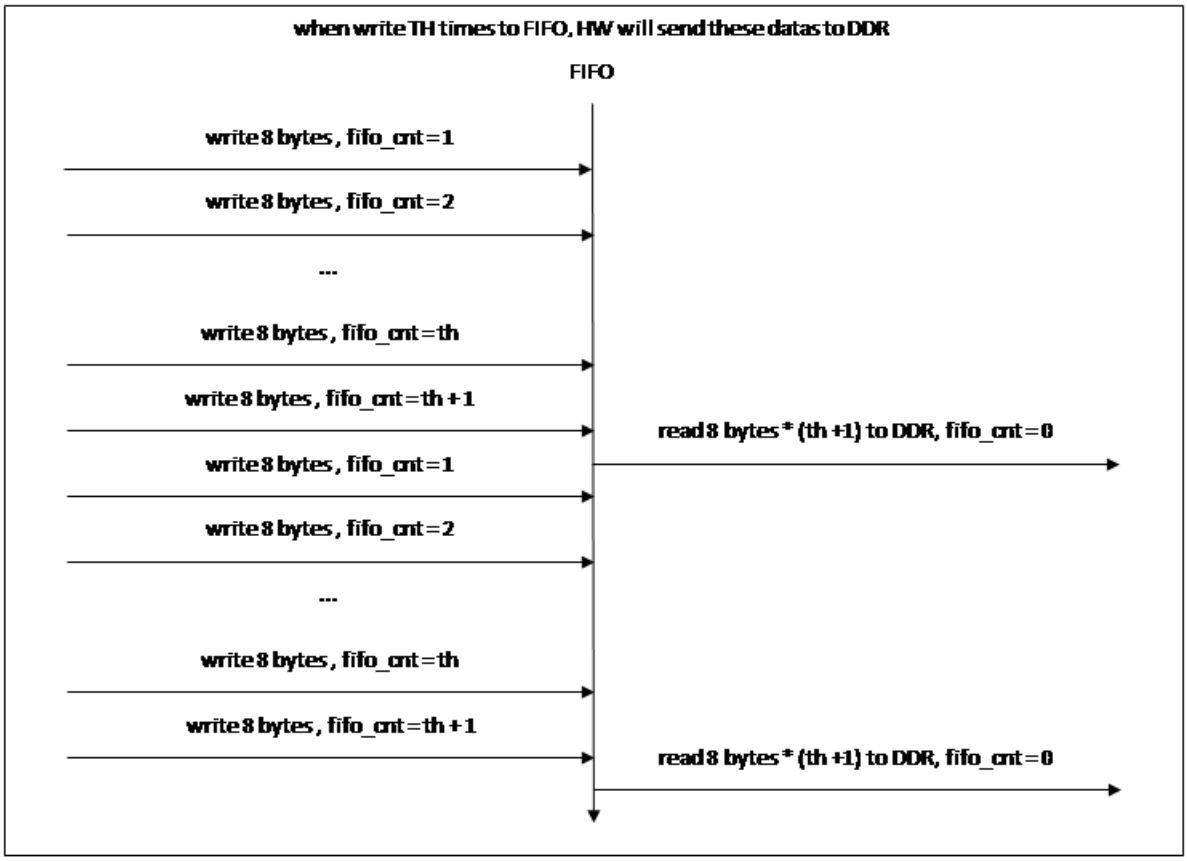


Table 10-52 EE_AUDIO_TODDR_A_START_ADDR 10'h42

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	start_addr, buff_A start address, ignore [2:0]

Table 10-53 EE_AUDIO_TODDR_A_FINISH_ADDR 10'h43

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	finish_addr, buff_A finish address, ignore [2:0]

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Table 10-54 EE_AUDIO_TODDR_A_INT_ADDR 10'h44

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	int_addr, usage A : as an address of interrupt; usage B : as a count of interrupt;

Table 10-55 EE_AUDIO_TODDR_A_STATUS1 10'h45

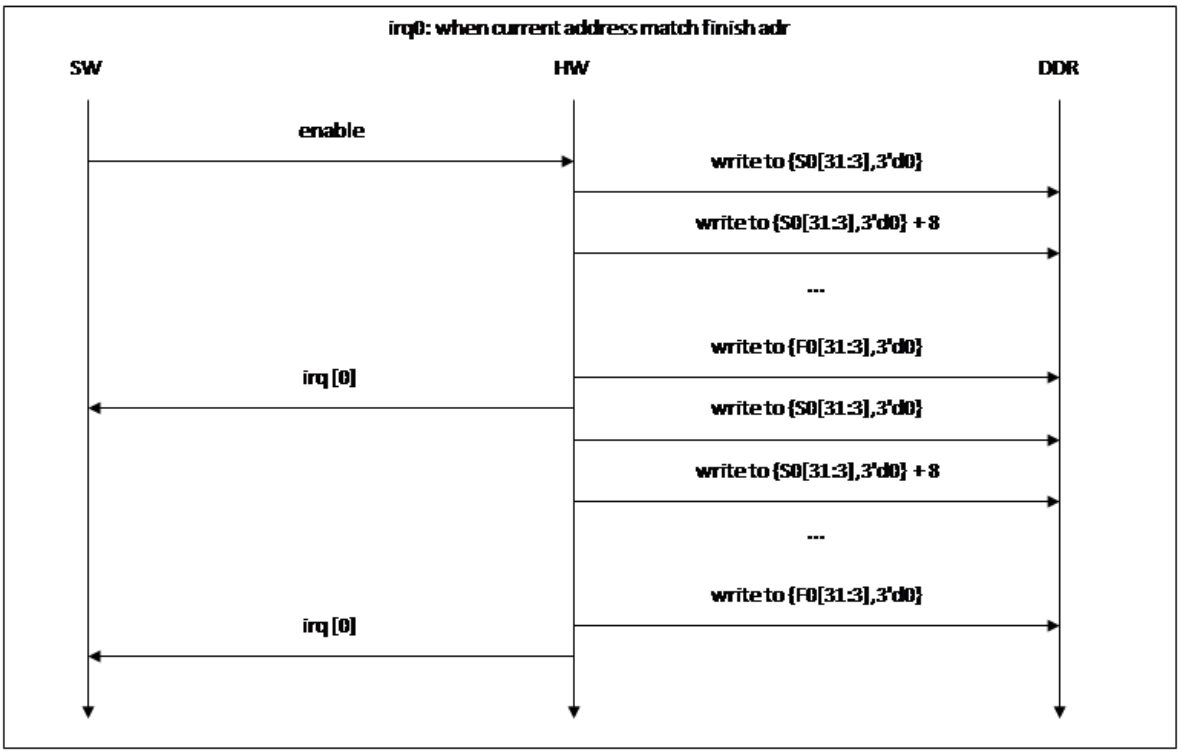
Bits	R/W	Default	Description
25:23	R	0x0000-0000	stop_ddr_status
22	R		stop_ddr_done
21	R/W	0x0000-0000	sel_b_true
20	R/W		sel_b
19:8	R/W		fifo count, the num in fifo
7:0	R/W		int_status, when irq generate, related bit will changed to 1 and can only clear by reg_int_status_clr

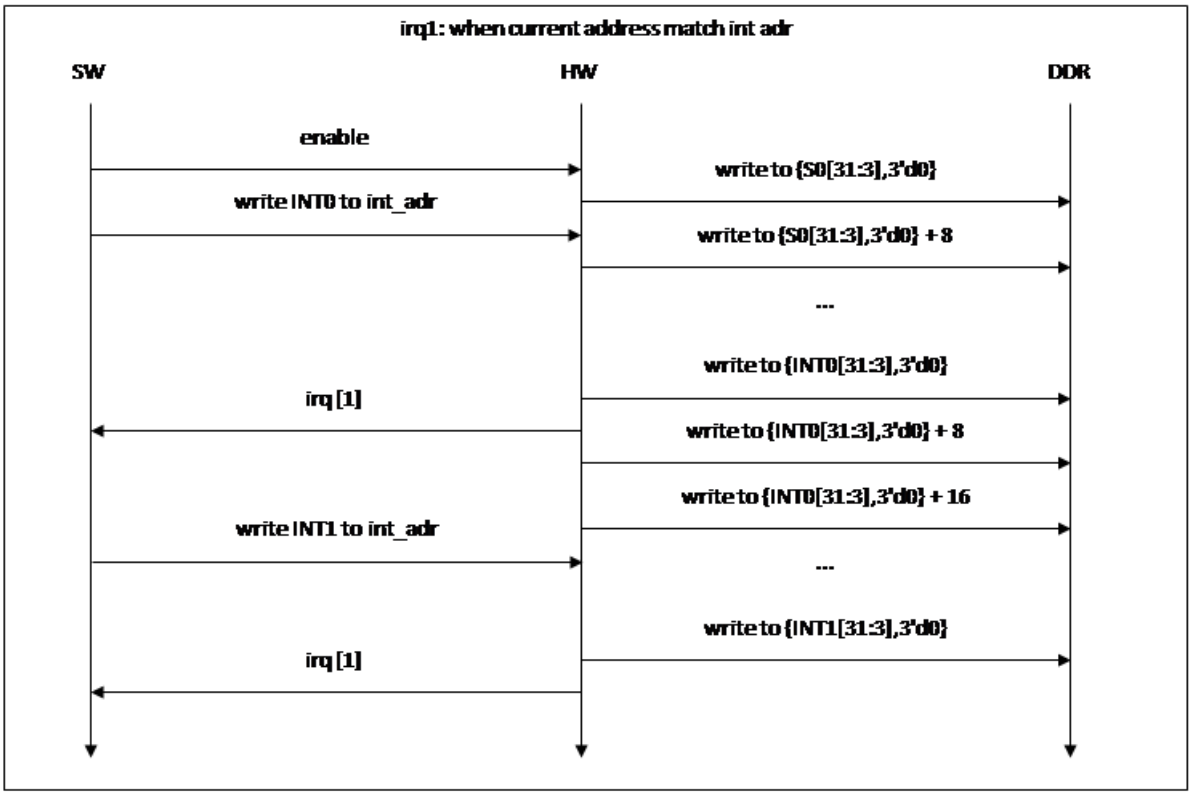
Table 10-56 EE_AUDIO_TODDR_A_STATUS2 10'h46

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	status2, by reg_status_sel: 0: current ddr write address; 1: next finish address; 2: count by ddr reply, current ddr write address; 3: count by ddr reply, next finish address; 4: ddr address captured by vad flag; 5: ddr address captured by vad frame sync; 6: [31:16]: fifo_cnt captured by vad frame sync; [15:0]: fifo_cnt captured by vad flag; 8: ddr address captured by first vad flag; 9: ddr address captured by first vad frame sync;

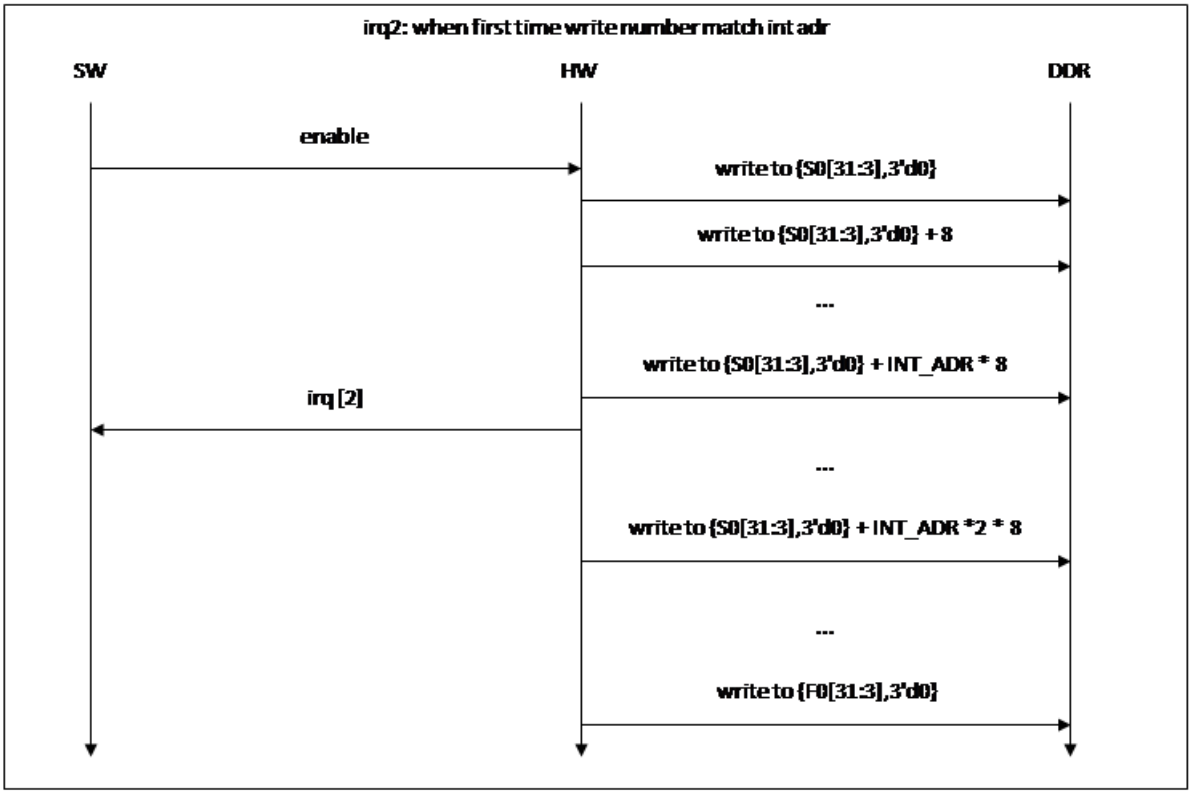
We can generate 8 irq and add them together to CPU. Then can read int_status to know which irq it is:

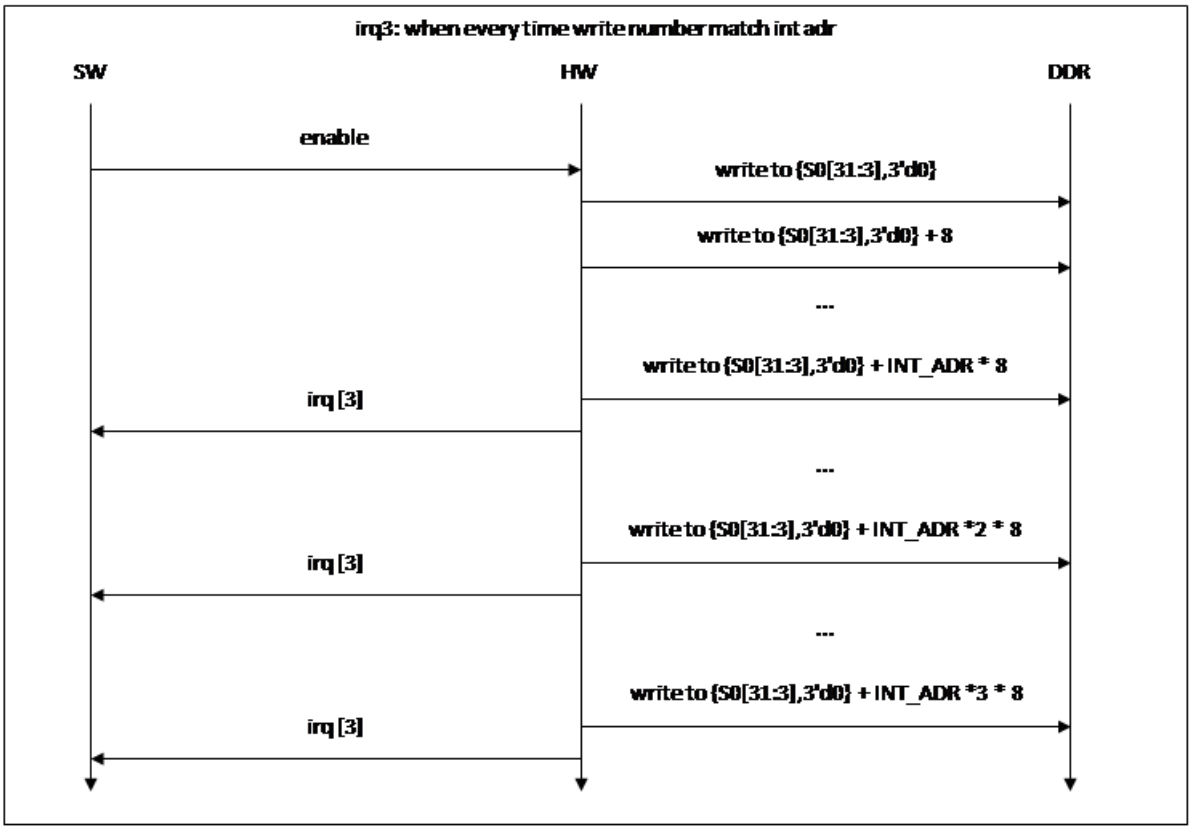
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Table 10-57 EE_AUDIO_TODDR_A_START_ADDRB 10'h47

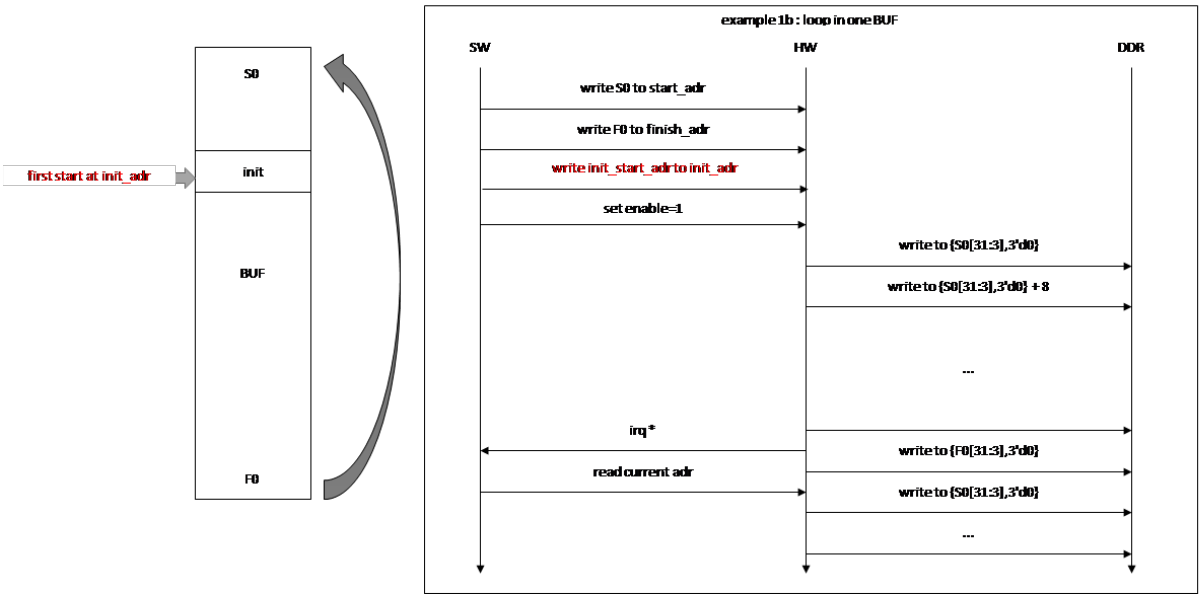
Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	istart_addrb, buff_B start address, ignore [2:0]

Table 10-58 EE_AUDIO_TODDR_A_FINISH_ADDRB 10'h48

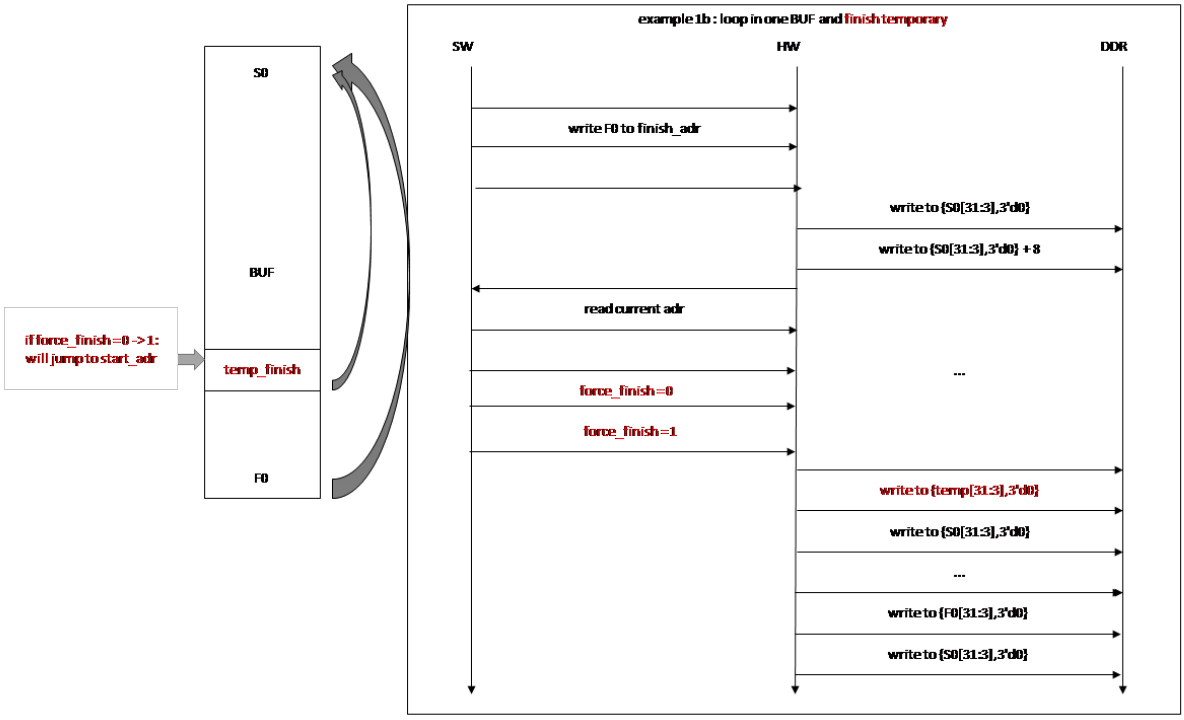
Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	finish_addrb, buff_B finish address, ignore [2:0]

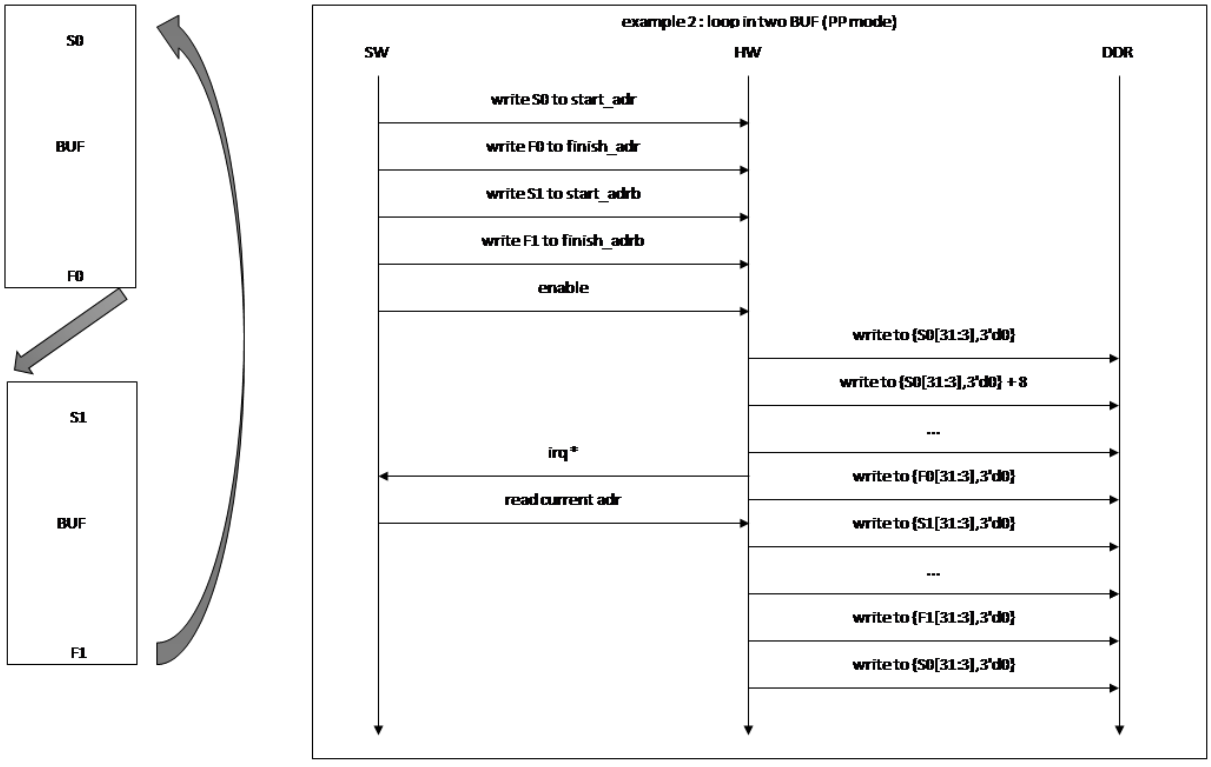
Table 10-59 EE_AUDIO_TODDR_A_INIT_ADDR 10'h49

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	initial address, the first ddr address after enable



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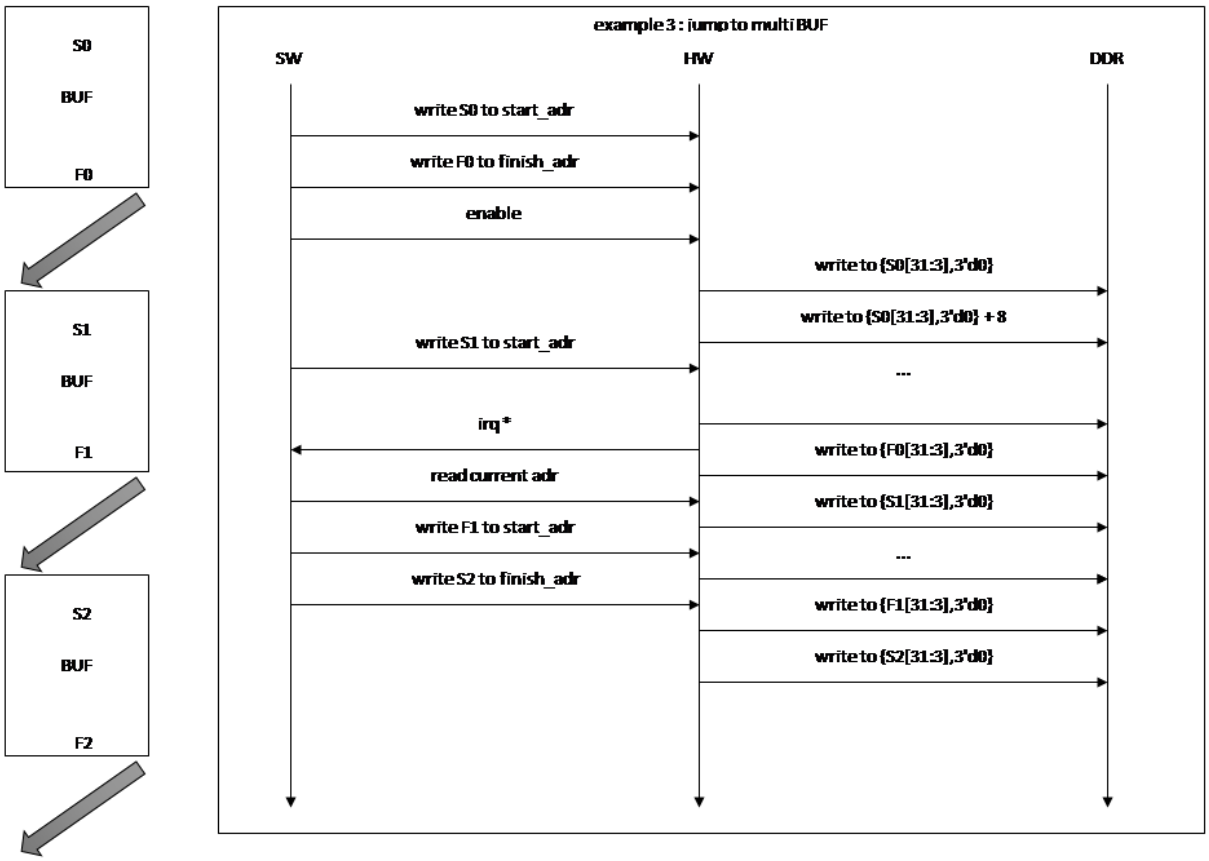


Table 10-60 EE_AUDIO_TODDR_A_CTRL2 10'h4a

Bits	R/W	Default	Description
31	R/W	0x0000-0000	Reserved for hold read. need set 1 before toddr_en =1, then TODDR will hold all data in FIFO. after sometime (etc. VAD detect), set it to 0, TODDR will start flush all data in FIFO to ddr.
30	R/W		reg_stop_ddr; if set from 0 to 1, will: step1: stop write data to FIFO; step2: stop sending request to DDR; step3: keep receiving data from DDR; step4: compare request count and receive count; step5: done if two count matched;
29:28	R/W		Insert_chnum; 3: replace data[9:0] to chnum[9:0]; 2: replace data[3:0] to chnum[3:0]; 1: replace data[0] to chnum[0]; 0: not replace;
23:16	R/W		each bits will set to one interrupt, 0: pulse mode; 1: level mode;
11:0	R/W		Reserved for hold read start offset. when release hold read (bit31), the read point of fifo will equal to current write point + this reg +1. fifo width is 8 Bytes. so if input is 8ch*32bits, this register need set to 3/7/11/… if input is 32ch*32bits, this register need set to 15/31/47/…

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Table 10-61 EE_AUDIO_TODDR_A_CHNUM_ID0 10'h300

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch3
23:16	R/W		ID of ch2
15:8	R/W		ID of ch1
7:0	R/W		ID of ch0

Table 10-62 EE_AUDIO_TODDR_A_CHNUM_ID1 10'h301

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch7
23:16	R/W		ID of ch6
15:8	R/W		ID of ch5
7:0	R/W		ID of ch4

Table 10-63 EE_AUDIO_TODDR_A_CHNUM_ID2 10'h302

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch11
23:16	R/W		ID of ch10
15:8	R/W		ID of ch9
7:0	R/W		ID of ch8

Table 10-64 EE_AUDIO_TODDR_A_CHNUM_ID3 10'h303

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch15
23:16	R/W		ID of ch14
15:8	R/W		ID of ch13
7:0	R/W		ID of ch12

Table 10-65 EE_AUDIO_TODDR_A_CHNUM_ID4 10'h304

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch19
23:16	R/W		ID of ch18
15:8	R/W		ID of ch17
7:0	R/W		ID of ch16

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Table 10-66 EE_AUDIO_TODDR_A_CHNUM_ID5 10'h305

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch23
23:16	R/W		ID of ch22
15:8	R/W		ID of ch21
7:0	R/W		ID of ch20

Table 10-67 EE_AUDIO_TODDR_A_CHNUM_ID6 10'h306

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch27
23:16	R/W		ID of ch26
15:8	R/W		ID of ch25
7:0	R/W		ID of ch24

Table 10-68 EE_AUDIO_TODDR_A_CHNUM_ID7 10'h307

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ID of ch31
23:16	R/W		ID of ch30
15:8	R/W		ID of ch29
7:0	R/W		ID of ch28

Table 10-69 EE_AUDIO_TODDR_A_CHSYNC_CTRL 10’h30F

Bits	R/W	Default	Description
31	R/W	0x0000-0000	bypass_n; 0: out=in; 1: sync data by chnum info;
30	R/W		sw_reset; 1: reset chnum_sync module
29	R/W		mode; 0: work as BUFF_MODE; 1: work as DROP_MODE;
28	R/W		id_se; 0: ID = input valid count; 1: ID= reg_id_***
27	R/W		fix_stable; 1: ignore stable info of input; 0: compensate dat by stable info;
26	R/W		debug_en0, for BUF_MODE only; 1: send chnum info from input; 0: generate new chnum info;
7:0	R/W		chnum_max; if input is 8ch, set this to 7;

EE_AUDIO_TODDR_B_CTRL0 10'h50

EE_AUDIO_TODDR_B_CTRL1 10'h51

EE_AUDIO_TODDR_B_START_ADDR 10'h52

EE_AUDIO_TODDR_B_FINISH_ADDR 10'h53

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EE_AUDIO_TODDR_B_INT_ADDR 10'h54
EE_AUDIO_TODDR_B_STATUS1 10'h55
EE_AUDIO_TODDR_B_STATUS2 10'h56
EE_AUDIO_TODDR_B_START_ADDRB 10'h57
EE_AUDIO_TODDR_B_FINISH_ADDR 10'h58
EE_AUDIO_TODDR_B_INIT_ADDR 10'h59
EE_AUDIO_TODDR_B_CTRL2 10'h5a
EE_AUDIO_TODDR_B_CHNUM_ID0 10'h310
EE_AUDIO_TODDR_B_CHNUM_ID1 10'h311
EE_AUDIO_TODDR_B_CHNUM_ID2 10'h312
EE_AUDIO_TODDR_B_CHNUM_ID3 10'h313
EE_AUDIO_TODDR_B_CHNUM_ID4 10'h314
EE_AUDIO_TODDR_B_CHNUM_ID5 10'h315
EE_AUDIO_TODDR_B_CHNUM_ID6 10'h316
EE_AUDIO_TODDR_B_CHNUM_ID7 10'h317
EE_AUDIO_TODDR_B_CHSYNC_CTRL 10'h31F

EE_AUDIO_TODDR_C_CTRL0 10'h60
EE_AUDIO_TODDR_C_CTRL1 10'h61
EE_AUDIO_TODDR_C_START_ADDR 10'h62
EE_AUDIO_TODDR_C_FINISH_ADDR 10'h63
EE_AUDIO_TODDR_C_INT_ADDR 10'h64
EE_AUDIO_TODDR_C_STATUS1 10'h65
EE_AUDIO_TODDR_C_STATUS2 10'h66
EE_AUDIO_TODDR_C_START_ADDRB 10'h67
EE_AUDIO_TODDR_C_FINISH_ADDR 10'h68
EE_AUDIO_TODDR_C_INIT_ADDR 10'h69
EE_AUDIO_TODDR_C_CTRL2 10'h6a
EE_AUDIO_TODDR_C_CHNUM_ID0 10'h320
EE_AUDIO_TODDR_C_CHNUM_ID1 10'h321
EE_AUDIO_TODDR_C_CHNUM_ID2 10'h322
EE_AUDIO_TODDR_C_CHNUM_ID3 10'h323
EE_AUDIO_TODDR_C_CHNUM_ID4 10'h324
EE_AUDIO_TODDR_C_CHNUM_ID5 10'h325
EE_AUDIO_TODDR_C_CHNUM_ID6 10'h326
EE_AUDIO_TODDR_C_CHNUM_ID7 10'h327
EE_AUDIO_TODDR_C_CHSYNC_CTRL 10'h32F

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EE_AUDIO_TODDR_D_CTRL0 10'h210
EE_AUDIO_TODDR_D_CTRL1 10'h211
EE_AUDIO_TODDR_D_START_ADDR 10'h212
EE_AUDIO_TODDR_D_FINISH_ADDR 10'h213
EE_AUDIO_TODDR_D_INT_ADDR 10'h214
EE_AUDIO_TODDR_D_STATUS1 10'h215
EE_AUDIO_TODDR_D_STATUS2 10'h216
EE_AUDIO_TODDR_D_START_ADDRB 10'h217
EE_AUDIO_TODDR_D_FINISH_ADDR 10'h218
EE_AUDIO_TODDR_D_INIT_ADDR 10'h219
EE_AUDIO_TODDR_D_CTRL2 10'h21a
EE_AUDIO_TODDR_D_CHNUM_ID0 10'h330
EE_AUDIO_TODDR_D_CHNUM_ID1 10'h331
EE_AUDIO_TODDR_D_CHNUM_ID2 10'h332
EE_AUDIO_TODDR_D_CHNUM_ID3 10'h333
EE_AUDIO_TODDR_D_CHNUM_ID4 10'h334
EE_AUDIO_TODDR_D_CHNUM_ID5 10'h335
EE_AUDIO_TODDR_D_CHNUM_ID6 10'h336
EE_AUDIO_TODDR_D_CHNUM_ID7 10'h337
EE_AUDIO_TODDR_D_CHSYNC_CTRL 10'h33F

10.10.4 FRDDR Registers

Table 10-70 EE_AUDIO_FRDDR_A_CTRL0 10'h70

Bits	R/W	Default	Description
31	R/W	0x0000-0000	reg_frddr_en, 0: disable; 1: enable;
30	R/W		reg_frddr_pp_mode, 0: select write to only one buff (start_addr,finish_addr); 1: select write to two buff (start_addr,finish_addr) (start_addrb, finish_addrb);
26:24	R/W		reg_frdd_endian
23:16	R/W		reg_frddr_int_en, [23] : reserved; [22] : reserved; [21] : fifo overflow, write when fifocnt = depth; [20] : fifo overflow, read when fifocnt = 0; [19] : first time when read from ddr "int_addr" data(only once); [18] : once time when read from ddr "int_addr" data(repeat); [17] : when read from ddr address match "int_addr"; [16]: when read from ddr address match "finish_addr";
15:12	R/W		reg_frddr_ack_dly, add delay to frddr ack
0	R/W		Ddr bus ugt setting.

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Table 10-71 EE_AUDIO_FRDDR_A_CTRL1 10'h71

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	reg_fifo_depth, the max depth of fifo; for high bit rates like 384k*32bits*8ch, set this register higher; for low bit rates like 48k*32bits*2ch, set this register lower;
23:16			reg_fifo_start_wr_th, when the fifo cnt less than "reg_fifo_depth - reg_fifo_start_wr_th", start reqeuest and read data from DDR; each time request "reg_fifo_start_wr_th" * 8 bytes data;
12			force finish; when the value changed from 0 to 1; will finished by current address and jump to start address;
11:8			reg_status_sel, control status2 source;
7:0			reg_int_status_clr, clear each bits of int_status register

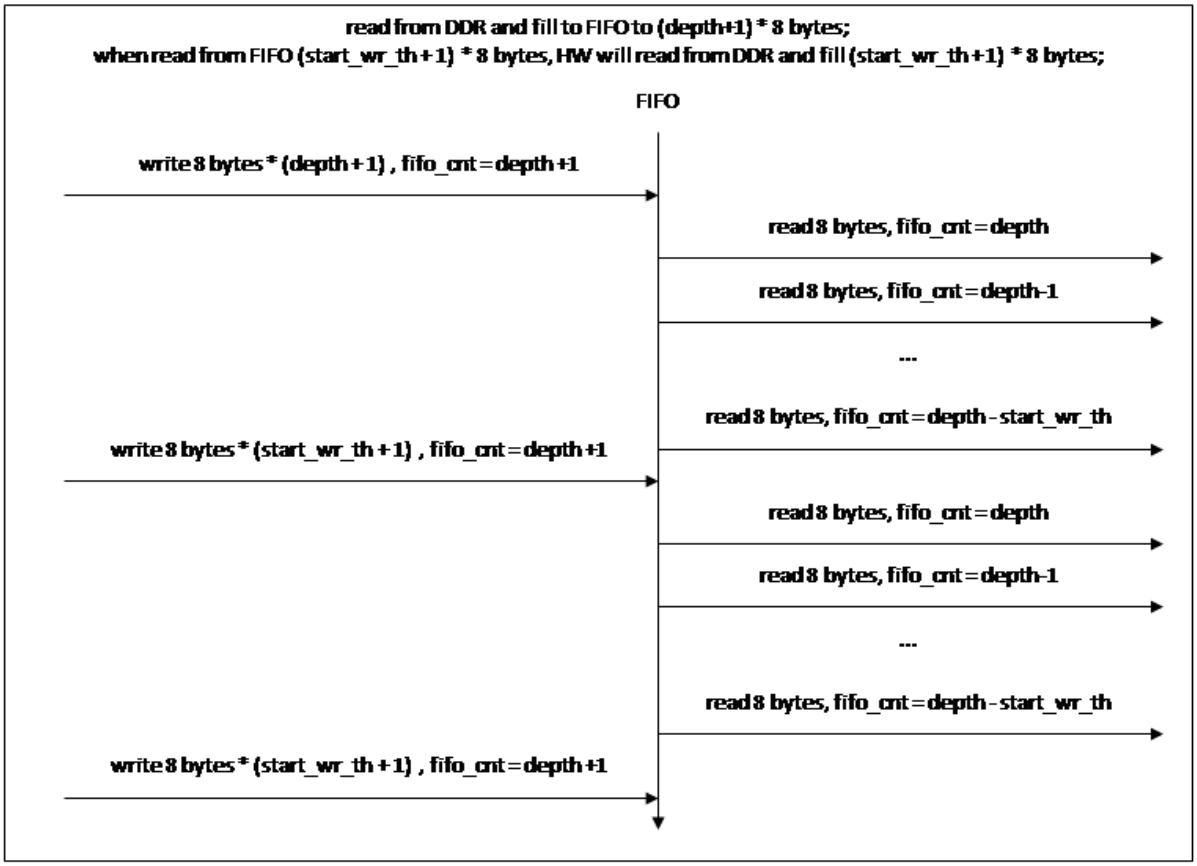


Table 10-72 EE_AUDIO_FRDDR_A_START_ADDR 10'h72

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	start_addr,buff_B start address

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Table 10-73 EE_AUDIO_FRDDR_A_FINISH_ADDR 10'h73

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	finish_addr,buff_B finish address

Table 10-74 EE_AUDIO_FRDDR_A_INT_ADDR 10'h74

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	int_addr,usage A : as an address of interrupt; usage B : as a count of interrupt;

Table 10-75 EE_AUDIO_FRDDR_A_STATUS1 10'h75

Bits	R/W	Default	Description
22:20	R	0x0000-0000	stop_ddr status
19	R		r_selb_true
18	R		r_selb
17	R		stop_ddr_done
16:8	R/W		fifo count, the num in fifo
7:0	R/W		int_status, when irq generate, related bit will changed to 1 and can only clear by reg_int_status_clr

Table 10-76 EE_AUDIO_FRDDR_A_STATUS2 10'h76

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	status2, by reg_status_sel: 0: current ddr write address; 1: next finish address; 2: count by ddr reply, current ddr write address; 3: count by ddr reply, next finish address;

The same design as TODDR:

We can generate 8 irq and add them together to CPU.

Then can read int_status to know it's which irq.

EE_AUDIO_FRDDR_A_START_ADDRB 10'h77

EE_AUDIO_FRDDR_A_FINISH_ADDRB 10'h78

The same design as TODDR:

We have an internal register to store reg_start_adr and reg_finish_adr.

We call them as r_start_adr and r_finish_adr;

Each time, when curr_adr match r_finish_adr, curr_adr will jump to r_start_adr , then update r_start_adr and r_finish_adr;

That's mean SW can write new start adr and finish adr before curr_adr match old finish adr.

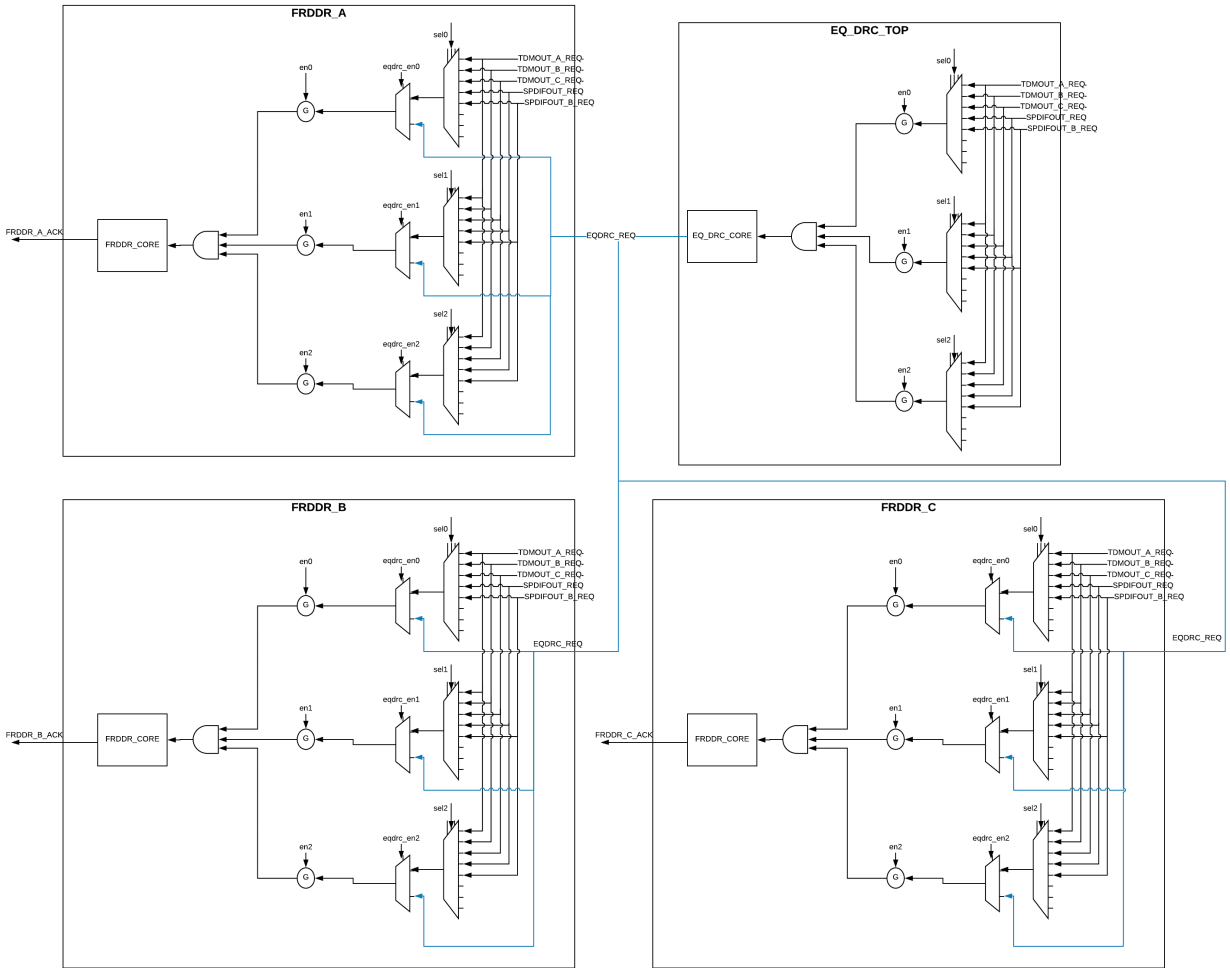
EE_AUDIO_FRDDR_A_INIT_ADDR 10'h79

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Table 10-77 EE_AUDIO_FRDDR_A_CTRL2 10'h7a

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	ch num for share buffer feature; if needn't share buffer, set it as 0; if need share buffer , set it as TDMOUT/SPDIFOUT ch number;
21	R/W		reg_stop_ddr; if set from 0 to 1, will: step1: stop write data to FIFO; step2: stop sending request to DDR; step3: keep receiving data from DDR; step4: compare request count and receive count; step5: done if two count matched;
20	R/W		Src_sel2_en
19	R/W		Src_sel2_eq; 1: select request from EQDRC; 0: select request from TDMOUT/SPDIFOUT;
18:16	R/W		Src_sel2; 0: tdmout_a; 1: tdmout_b; 2: tdmout_c; 3: spdifout; 4: spdifout_b; 5: reserved; 6: reserved; 7: reserved;
12	R/W		Src_sel1_en
11	R/W		Src_sel1_eq; 1: select request from EQDRC; 0: select request from TDMOUT/SPDIFOUT;
10:8	R/W		Src_sel1; 0: tdmout_a; 1: tdmout_b; 2: tdmout_c; 3: spdifout; 4: spdifout_b; 5: reserved; 6: reserved; 7: reserved;
4	R/W		Src_sel0_en
3	R/W		Src_sel0_eq; 1: select request from EQDRC; 0: select request from TDMOUT/SPDIFOUT;
2:0	R/W		Src_sel0; 0: tdmout_a; 1: tdmout_b; 2: tdmout_c; 3: spdifout; 4: spdifout_b; 5: reserved; 6: reserved; 7: reserved;

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EE_AUDIO_FRDDR_B_CTRL0 10'h80

EE_AUDIO_FRDDR_B_CTRL1 10'h81

EE_AUDIO_FRDDR_B_START_ADDR 10'h82

EE_AUDIO_FRDDR_B_FINISH_ADDR 10'h83

EE_AUDIO_FRDDR_B_INT_ADDR 10'h84

EE_AUDIO_FRDDR_B_STATUS1 10'h85

EE_AUDIO_FRDDR_B_STATUS2 10'h86

EE_AUDIO_FRDDR_B_START_ADDRB 10'h87

EE_AUDIO_FRDDR_B_FINISH_ADDR 10'h88

EE_AUDIO_FRDDR_B_INIT_ADDR 10'h89

EE_AUDIO_FRDDR_B_CTRL2 10'h8a

EE_AUDIO_FRDDR_C_CTRL0 10'h90

EE_AUDIO_FRDDR_C_CTRL1 10'h91

EE_AUDIO_FRDDR_C_START_ADDR 10'h92

EE_AUDIO_FRDDR_C_FINISH_ADDR 10'h93

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EE_AUDIO_FRDDR_C_INT_ADDR 10'h94
EE_AUDIO_FRDDR_C_STATUS1 10'h95
EE_AUDIO_FRDDR_C_STATUS2 10'h96
EE_AUDIO_FRDDR_C_START_ADDRB 10'h97
EE_AUDIO_FRDDR_C_FINISH_ADDR 10'h98
EE_AUDIO_FRDDR_C_INIT_ADDR 10'h99
EE_AUDIO_FRDDR_C_CTRL2 10'h9a

EE_AUDIO_FRDDR_D_CTRL0 10'h220
EE_AUDIO_FRDDR_D_CTRL1 10'h221
EE_AUDIO_FRDDR_D_START_ADDR 10'h222
EE_AUDIO_FRDDR_D_FINISH_ADDR 10'h223
EE_AUDIO_FRDDR_D_INT_ADDR 10'h224
EE_AUDIO_FRDDR_D_STATUS1 10'h225
EE_AUDIO_FRDDR_D_STATUS2 10'h226
EE_AUDIO_FRDDR_D_START_ADDRB 10'h227
EE_AUDIO_FRDDR_D_FINISH_ADDR 10'h228
EE_AUDIO_FRDDR_D_INIT_ADDR 10'h229
EE_AUDIO_FRDDR_D_CTRL2 10'h22a

10.10.5 DDR ARB Registers

Table 10-78 EE_AUDIO_ARB_CTRL0 10'ha0

Bits	R/W	Default	Description
31	R/W	0x0000-0000	reg_arb_en, 0:disable; 1: enable;
30	R/W		reg_clr_lock_clk_cnt, 1: clear clk_cnt of lock status;
29	R/W		reg_unlock; 1: will reset the status of DDR arbiter to IDLE;
28	R/W		reg_unlock_no_async; 0: will clear status of DDR ASYNC when set reg_unlock to 1;
27	R/W		reg_reset_async; 1: will reset DDR_ASYNC module;

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Bits	R/W	Default	Description
22:20	R/W		reg_sts_sel, refer to ARB_STS;
15:0	R/W		reg_arb_mask, [9]: frddr_e; [8]: toddr_e; [7]: frddr_d; [6]: frddr_c; [5]: frddr_b; [4]: frddr_a; [3]: toddr_d; [2]: toddr_c; [1]: toddr_b; [0]: toddr_a;

Table 10-79 EE_AUDIO_ARB_CTRL1 10'ha1

Bits	R/W	Default	Description
15:0	R/W	0x0000-0000	reg_lock_timeout_cnt; will generate exception irq if clk_cnt of locked sts greater than this register;

Table 10-80 EE_AUDIO_ARB_STS 10'ha8

Bits	R/W	Default	Description
31:0	R	0x0000-0000	reg_sts_sel = 0: bit31: r_locked; mean arbiter is locked; bit30: c_usr_dc_rdy; mean DDR ASYNC is ready; bit27:22: rd_cnt; mean DDR ASYNC stored read command count; bit21:16: wr_cnt; mean DDR ASYNC stored write command count; bit15:0: r_req_sel; mean arbiter grant to which request; reg_sts_sel = 1: bit31:16: c_req_sel; mean request status; bit15:0 : r_lock_clk_cnt; mean how long locked this time; reg_sts_sel = 2: bit31:16: lock_clk_cnt_max; bit15:0: lock_clk_cnt_min; reg_sts_sel = 3: bit31:28: cnt_id0; bit27:24: cnt_id1; bit23:20: cnt_id2; bit19:16: cnt_id3; bit15:12: cnt_id4; bit11:8: cnt_id5; bit7:4: cnt_id6; bit3:0: cnt_id7; reg_sts_sel = 4: bit31:28: cnt_id8; bit27:24: cnt_id9; bit23:20: cnt_id10; bit19:16: cnt_id11; bit15:12: cnt_id12; bit11:8: cnt_id13; bit7:4: cnt_id14; bit3:0: cnt_id15;

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10.10.6 LoopBack Registers

Table 10-81 EE_AUDIO_LB_A_CTRL0 10'hb0

Bits	R/W	Default	Description
31	R/W	0x0000-0000	reg_lb_en, 0:disable; 1: enable;
30	R/W		reg_lb_mode, 0: out rate = in data rate; 1: out rate = loopback data rate;
29	R/W		reg_ext_signed, 0: extend bits as "0"; 1: extend bits as "msb";
28	R/W		Enable_sync_chnum; 1: start store data when ch_num can match ID;
27	R/W		chnum_sel; 0: chnum[4:0] is fixed value: 0-1-2-…31; 1: chnum[4:0] is valid_cnt; the different is bace mask set;
17:16	R/W		Reg_sts_sel, refer to REG_LB_STATUS.
15:13	R/W		reg_dat_sel, shift [m:n] to [31:0]; 0: right justified, out = { ext,[m:n]}; 1: left justified, out = {[m:n],all0}; 2: right justified, out = { ext,[m:n]}; 3: left justified, out = {[m:n],all0}; 4: right justified, out = { ext,[m:n]};
12:8	R/W		reg_dat_m_sel, the msb positioin in data
7:3	R/W		reg_dat_n_sel, the lsb position in data

Table 10-82 EE_AUDIO_LB_A_CTRL1 10'hb1

Bits	R/W	Default	Description
29	R/W		reg_lb_ext_signed, 0: extend bits as "0"; 1: extend bits as "msb";
28	R/W		Enable_sync_chnum; 1: start store data when ch_num can match ID;
27	R/W		hold_insertion 1: hold insert data store(update) and insert 0 after original data;
24:16			the error condition which can pull stable signal down; 24: orig_sotre_cnt_err; start store with cnt!=0; 23: insert_store_cnt_err; start store with cnt!=0; 22: orig_store_err1; start store but not first ch 21: orig_store_err2; storing but receive first ch 20: insert_store_err1; start store but not first ch 19: insert_store_err2; storing but receive first ch 18: output_en_err; start send when output is not finish; 17: pipe_cnt_err1; cnt>3; 16: pipe_cnt_err2; cnt<0;
15:13			reg_lb_sel, shift [m:n] to [31:0]; 0: right justified, out = {ext,[m:n]}; 1: left justified, out = {[m:n],all0}; 2: right justified, out = { ext,[m:n]}; 3: left justified, out = {[m:n], all0}; 4: right justified, out = { ext,[m:n]};
12:8			reg_lb_m_sel, the msb positioin loopback data
7:3			reg_lb_n_sel, the lsb position loopback data

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Table 10-83 EE_AUDIO_LB_A_CTRL2 10'hb2

Bits	R/W	Default	Description
24:20	R/W	0x0000-0000	data Src select: 0: tdmin_a; 1: tdmin_b; 2: tdmin_c; 3: spdifin; 4: pdmin; 5: fratv; 6: tdmin_lb; 7: loopback_a; 8: frhdmirx_spdif; 9: loopback_b; 10: spdifin_lb; 11:earc_rx_dmac 12:frhdmirx_dsd 13:resample_a 14:resample_b 15: vad; 16~31:reserved
19:16	R/W	0x0000-0000	Dat_ch_num, max channel number of data source; max is 15 (equal 16 ch)
15:0	R/W		Dat_ch_mask, 16bits match 16 ch, set 1 will sending out, set0 will drop off this ch;

Table 10-84 EE_AUDIO_LB_A_CTRL3 10'hb3

Bits	R/W	Default	Description
24:20	R/W	0x0000-0000	LB Src select: 0: tdmin_a; 1: tdmin_b; 2: tdmin_c; 3: spdifin; 4: pdmin; 5: fratv; 6: tdmin_lb; 7: loopback_a; 8: frhdmirx_spdif; 9: loopback_b; 10: spdifin_lb; 11:earc_rx_dmac 12:frhdmirx_dsd 13:resample_a 14:resample_b 15: vad; 16~31:reserved
19:16	R/W		Lb_ch_num, max channel number of data source; max is 15 (equal 16 ch)
15:0	R/W		Lb_ch_mask, 16bits match 16 ch, set 1 will sending out, set0 will drop off this ch;

Table 10-85 EE_AUDIO_ LB_A_DAT_ID0 10'hb4

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	data_ch7_id
23:16	R/W		data_ch6_id

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Bits	R/W	Default	Description
15:8	R/W		data_ch5_id
7:0	R/W		data_ch4_id

Table 10-86 EE_AUDIO_LB_A_DAT_ID1 10'hb5

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	data_ch3_id
23:16	R/W		data_ch2_id
15:8	R/W		data_ch1_id
7:0	R/W		data_ch0_id

Table 10-87 EE_AUDIO_LB_A_DAT_ID2 10'hb6

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	data_ch11_id
23:16	R/W		data_ch10_id
15:8	R/W		data_ch9_id
7:0	R/W		data_ch8_id

Table 10-88 EE_AUDIO_LB_A_DAT_ID3 10'hb7

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	data_ch15_id
23:16	R/W		data_ch14_id
15:8	R/W		data_ch13_id
7:0	R/W		data_ch12_id

Table 10-89 EE_AUDIO_LB_A_ID0 10'hb8

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	lb_data_ch7_id
23:16	R/W		lb_data_ch6_id
15:8	R/W		lb_data_ch5_id
7:0	R/W		lb_data_ch4_id

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Table 10-90 EE_AUDIO_LB_A _ID1 10'hb9

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	lb_data_ch3_id
23:16	R/W		lb_data_ch2_id
15:8	R/W		lb_data_ch1_id
7:0	R/W		lb_data_ch0_id

Table 10-91 EE_AUDIO_LB_A _ID2 10'hba

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	lb_data_ch11_id
23:16	R/W		lb_data_ch10_id
15:8	R/W		lb_data_ch9_id
7:0	R/W		lb_data_ch8_id

Table 10-92 EE_AUDIO_LB_A _ID3 10'hbb

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	lb_data_ch15_id
23:16	R/W		lb_data_ch14_id
15:8	R/W		lb_data_ch13_id
7:0	R/W		lb_data_ch12_id

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Table 10-93 EE_AUDIO_LB_A _STS 10'hbc

Bits	R/W	Default	Description
31:0	R	0x0000-0000	reg_sts_sel = 0: [31:0] = 0; reg_sts_sel = 1: [31]:pipe_cnt_err2; mean pipe cnt decr when it's 0; [30]:pipe_cnt_err1; mean pipe cnt incr when it's 3; [29:28]:pipe_cnt; current pipe cnt value; [27]:output_en_err; when output, received a new start; [26]:insert_storing_err2; it it's receving, but received first ch; [25]:insert_storing_err1, if it's not receving, but received data [24]:orig_storing_err2; it it's receving, but received first ch; [23]:orig_storing_err1, if it's not receving, but received data [22]:1st_send_done, mean finished first time send insert data; [21]:insert_storing, mean it's receiving insert data now; [20]:orig_storing, mean it's receiving insert data now; [19]:insert_store_cnt_err, when first_ch, if store_cnt is not 0, mean error, missed ch or another reason; [9]:orig_store_cnt_err, when first_ch, if store_cnt is not 0, mean error, missed ch or another reason; reg_sts_sel = 2: [31:0]:insert_store_cnt_debug, when start sending data, stored insert dat ch number; reg_sts_sel = 3: [31:0]:orig_store_cnt_debug, when start sending data, stored orig dat ch number;

Table 10-94 EE_AUDIO_LB_A_CHSYNC_CTRL_INSERT 10'hbd

Bits	R/W	Default	Description
31	R/W	0x0000-0000	bypass_n; 0: out=in; 1: enable sync mode;
30	R/W		sw_reset; 1: reset status;
29	R/W		mode_sel; 0: buf sync mode; 1: drop sync mode;
28	R/W		id_sel; 0: by int_cnt; 1: by reg_chnum_id;
27	R/W		fix_stable; 1: will not pull stable low if detect any error;
26	R/W		debug_en0; for buf sync mode only; 0: send new chnum which generated by chnum_sync; 1: send old chnum from buff;
7:0	R/W		chnum_max; if receive 8 ch data, set it to 7;

Table 10-95 EE_AUDIO_LB_A_CHSYNC_CTRL_ORIG 10'hbe

Bits	R/W	Default	Description
31	R/W	0x0000-0000	bypass_n; 0: out=in; 1: enable sync mode;
30	R/W		sw_reset; 1: reset status;
29	R/W		mode_sel;

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Bits	R/W	Default	Description
			0: buf sync mode; 1: drop sync mode;
28	R/W		id_sel; 0: by int_cnt; 1: by reg_chnum_id;
27	R/W		fix_stable; 1: will not pull stable low if detect any error;
26	R/W		debug_en0; for buf sync mode only; 0: send new chnum which generated by chnum_sync; 1: send old chnum from buff;
7:0	R/W		chnum_max; if receive 8 ch data, set it to 7;

EE_AUDIO_LB_B_CTRL0 10'h230

EE_AUDIO_LB_B_CTRL1 10'h231

EE_AUDIO_LB_B_CTRL2 10'h232

EE_AUDIO_LB_B_CTRL3 10'h233

EE_AUDIO_ LB_B_DAT_ID0 10'h234

EE_AUDIO_LB_B_DAT_ID1 10'h235

EE_AUDIO_LB_B_DAT_ID2 10'h236

EE_AUDIO_LB_B_DAT_ID3 10'h237

EE_AUDIO_LB_B_ID0 10'h238

EE_AUDIO_LB_B_ID1 10'h239

EE_AUDIO_LB_B_ID2 10'h23a

EE_AUDIO_LB_B_ID3 10'h23b

EE_AUDIO_LB_B_STS 10'h23c

EE_AUDIO_LB_B_CHSYNC_CTRL_INSERT 10'h23d

EE_AUDIO_LB_B_CHSYNC_CTRL_ORIG 10'h23e

10.10.7 TDM Registers

TDMin_B/C are the same as TDMin_A.

TDMout_B/C are the same as TDMout_A.

TDMin_LB is the same as TDMin_A.

TDM IN & OUT are independent , so need select MCLK/SCLK/LRCLK/DATIN/DATOUT in audio after set CHIP_PIN_MUX.

These pin are from/to CHIP_PIN_MUX module.

MCLK	2	output
SCLK_MST/SLV	3	input/output

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LRCLK_MST/SLV	3	input/output
DAT	32	input/output

Sources of pad_aud_dat_out are:

bit	src	bit	src	bit	src	bit	src
31	0	23	TDMOUT_C bit7	15	TDMOUT_B bit7	7	TDMOUT_A bit7
30	0	22	TDMOUT_C bit6	14	TDMOUT_B bit6	6	TDMOUT_A bit6
29	0	21	TDMOUT_C bit5	13	TDMOUT_B bit5	5	TDMOUT_A bit5
28	0	20	TDMOUT_C bit4	12	TDMOUT_B bit4	4	TDMOUT_A bit4
27	0	19	TDMOUT_C bit3	11	TDMOUT_B bit3	3	TDMOUT_A bit3
26	0	18	TDMOUT_C bit2	10	TDMOUT_B bit2	2	TDMOUT_A bit2
25	0	17	TDMOUT_C bit1	9	TDMOUT_B bit1	1	TDMOUT_A bit1
24	0	16	TDMOUT_C bit0	8	TDMOUT_B bit0	0	TDMOUT_A bit0

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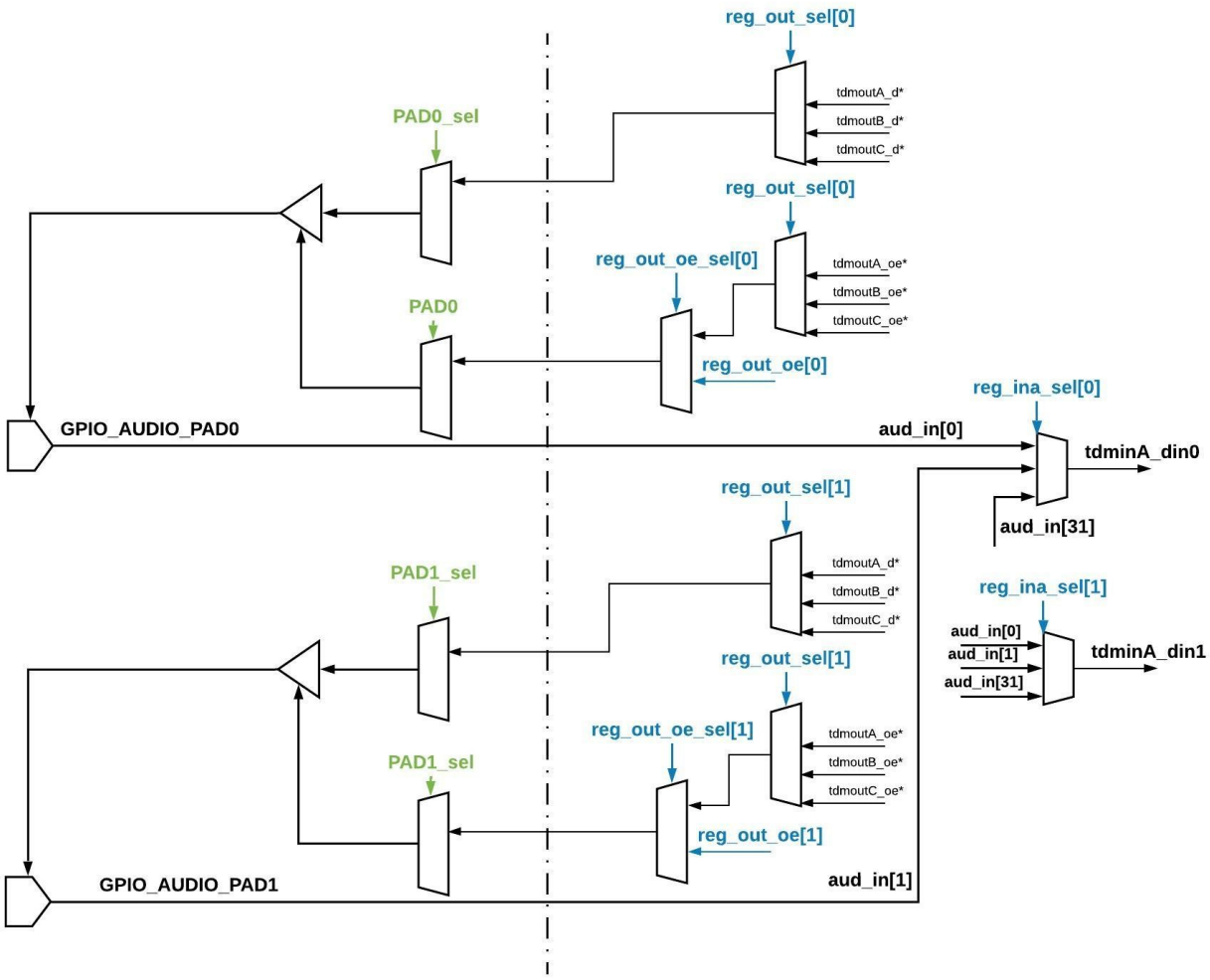


Table 10-96 EE_AUDIO_MCLK_PAD_CTRL0 10'h3A0

Bits	R/W	Default	Description
31	R/W	0	mclk_pad_1_en;
30	R/W	0	mclk_pad_1, force to xtal;
26:24	R/W	0	mclk _pad_1_sel: 0: mclk_a; 1: mclk_b; 2: mclk_c; 3: mclk_d; 4: mclk_e; 5: mclk_f;
23:16	R/W	0	Mclk_pad_1_div: the mclk_pad will div by mclk source; set 7 if need div8
15	R/W	0	mclk_pad_0_en
14	R/W	0	mclk_pad_0, force to xtal;

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Bits	R/W	Default	Description
10:8	R/W	0	mclk _pad_0_sel: 0: mclk_a; 1: mclk_b; 2: mclk_c; 3: mclk_d; 4: mclk_e; 5: mclk_f;
7:0	R/W	0	Mclk_pad_0_div: the mclk_pad will div by mclk source; set 7 if need div8

Table 10-97 EE_AUDIO_MCLK_PAD_CTRL1 10'h3A1

Bits	R/W	Default	Description
15	R/W	0	mclk_pad_2_en
14	R/W	0	mclk_pad_2, force to xtal;
10:8	R/W	0	mclk _pad_2_sel: 0: mclk_a; 1: mclk_b; 2: mclk_c; 3: mclk_d; 4: mclk_e; 5: mclk_f;
7:0	R/W	0	Mclk_pad_2_div: the mclk_pad will div by mclk source; set 7 if need div8

Table 10-98 EE_AUDIO_SCLK_PAD_CTRL0 10'h3A2

Bits	R/W	Default	Description
23	R/W	0	sclk_pad_4_oen: 0: pad work as output; 1: pad work as input;
22:20	R/W	0	sclk_pad_4_sel(when it's output): 0: mst_sclk_a; 1: mst_sclk_b; 2: mst_sclk_c; 3: mst_sclk_d; 4: mst_sclk_e; 5: mst_sclk_f;
19	R/W	0	sclk_pad_3_oen: 0: pad work as output; 1: pad work as input;
18:16	R/W	0	sclk_pad_3_sel(when it's output): 0: mst_sclk_a; 1: mst_sclk_b; 2: mst_sclk_c; 3: mst_sclk_d; 4: mst_sclk_e; 5: mst_sclk_f;
11	R/W	0	sclk_pad_2_oen: 0: pad work as output; 1: pad work as input;
10:8	R/W	0	sclk_pad_2_sel(when it's output):

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Bits	R/W	Default	Description
			0: mst_sclk_a; 1: mst_sclk_b; 2: mst_sclk_c; 3: mst_sclk_d; 4: mst_sclk_e; 5: mst_sclk_f;
7	R/W	0	sclk_pad_1_oen: 0: pad work as output; 1: pad work as input;
6:4	R/W	0	sclk_pad_1_sel(when it's output): 0: mst_sclk_a; 1: mst_sclk_b; 2: mst_sclk_c; 3: mst_sclk_d; 4: mst_sclk_e; 5: mst_sclk_f;
3	R/W	0	sclk_pad_0_oen: 0: pad work as output; 1: pad work as input;
2:0	R/W	0	sclk_pad_0_sel(when it's output): 0: mst_sclk_a; 1: mst_sclk_b; 2: mst_sclk_c; 3: mst_sclk_d; 4: mst_sclk_e; 5: mst_sclk_f;

Table 10-99 EE_AUDIO_SCLK_PAD_CTRL1 10'h3A3

Bits	R/W	Default	Description
23	R/W	0	lrclk_pad_4_oen: 0: pad work as output; 1: pad work as input;
22:20	R/W	0	lrclk_pad_4_sel(when it's output): 0: mst_lrclk_a; 1: mst_lrclk_b; 2: mst_lrclk_c; 3: mst_lrclk_d; 4: mst_lrclk_e; 5: mst_lrclk_f;
19	R/W	0	lrclk_pad_3_oen: 0: pad work as output; 1: pad work as input;
18:16	R/W	0	lrclk_pad_3_sel(when it's output): 0: mst_lrclk_a; 1: mst_lrclk_b; 2: mst_lrclk_c; 3: mst_lrclk_d; 4: mst_lrclk_e; 5: mst_lrclk_f;
11	R/W	0	lrclk_pad_2_oen: 0: pad work as output; 1: pad work as input;
10:8	R/W	0	lrclk_pad_2_sel(when it's output): 0: mst_lrclk_a; 1: mst_lrclk_b;

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Bits	R/W	Default	Description
			2: mst_lrclk_c; 3: mst_lrclk_d; 4: mst_lrclk_e; 5: mst_lrclk_f;
7	R/W	0	lrclk_pad_1_oen: 0: pad work as output; 1: pad work as input;
6:4	R/W	0	lrclk_pad_1_sel(when it's output): 0: mst_lrclk_a; 1: mst_lrclk_b; 2: mst_lrclk_c; 3: mst_lrclk_d; 4: mst_lrclk_e; 5: mst_lrclk_f;
3	R/W	0	lrclk_pad_0_oen: 0: pad work as output; 1: pad work as input;
2:0	R/W	0	lrclk_pad_0_sel(when it's output): 0: mst_lrclk_a; 1: mst_lrclk_b; 2: mst_lrclk_c; 3: mst_lrclk_d; 4: mst_lrclk_e; 5: mst_lrclk_f;

Table 10-100 EE_AUDIO_DAT_PAD_CTRL0 10'h390

Bits	R/W	Default	Description
28:24	R/W	0	tdmin_a dat_in bit3 sel
20:16	R/W	0	tdmin_a dat_in bit2 sel
12:8	R/W	0	tdmin_a dat_in bit1 sel
4:0	R/W	0	tdmin_a dat_in bit0 sel 0: sel TDM_D0; 1: sel TDM_D1; 2: sel TDM_D2; … 31: sel TDM_D31;

Table 10-101 EE_AUDIO_DAT_PAD_CTRL1 10'h391

Bits	R/W	Default	Description
28:24	R/W	0	tdmin_a dat_in bit7 sel
20:16	R/W	0	tdmin_a dat_in bit6 sel
12:8	R/W	0	tdmin_a dat_in bit5 sel
4:0	R/W	0	tdmin_a dat_in bit4 sel

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Table 10-102 EE_AUDIO_DAT_PAD_CTRL2 10'h392

Bits	R/W	Default	Description
28:24	R/W	0	tdmin_b dat_in bit3 sel
20:16	R/W	0	tdmin_b dat_in bit2 sel
12:8	R/W	0	tdmin_b dat_in bit1 sel
4:0	R/W	0	tdmin_b dat_in bit0 sel

Table 10-103 EE_AUDIO_DAT_PAD_CTRL3 10'h393

Bits	R/W	Default	Description
28:24	R/W	0	tdmin_b dat_in bit7 sel
20:16	R/W	0	tdmin_b dat_in bit6 sel
12:8	R/W	0	tdmin_b dat_in bit5 sel
4:0	R/W	0	tdmin_b dat_in bit4 sel

Table 10-104 EE_AUDIO_DAT_PAD_CTRL4 10'h394

Bits	R/W	Default	Description
28:24	R/W	0	tdmin_c dat_in bit3 sel
20:16	R/W	0	tdmin_c dat_in bit2 sel
12:8	R/W	0	tdmin_c dat_in bit1 sel
4:0	R/W	0	tdmin_c dat_in bit0 sel

Table 10-105 EE_AUDIO_DAT_PAD_CTRL5 10'h395

Bits	R/W	Default	Description
28:24	R/W	0	tdmin_c dat_in bit7 sel
20:16	R/W	0	tdmin_c dat_in bit6 sel
12:8	R/W	0	tdmin_c dat_in bit5 sel
4:0	R/W	0	tdmin_c dat_in bit4 sel

Table 10-106 EE_AUDIO_DAT_PAD_CTRL6 10'h396

Bits	R/W	Default	Description
28:24	R/W	0	TDM_D3 out src sel:
20:16	R/W	0	TDM_D2 out src sel:

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Bits	R/W	Default	Description
12:8	R/W	0	TDM_D1 out src sel:
4:0	R/W	0	TDM_D0 out src sel: 0: tdmout_a lane0; 1: tdmout_a lane1; … 7: tdmout_b lane7; 8: tdmout_b lane0; 9: tdmout_b lane1; … 15: tdmout_b lane7; 16: tdmout_c lane0; 17: tdmout_c lane1; … 23: tdmout_c lane7;

Table 10-107 EE_AUDIO_DAT_PAD_CTRL7 10'h397

Bits	R/W	Default	Description
28:24	R/W	0	TDM_D7 out src sel:
20:16	R/W	0	TDM_D6 out src sel:
12:8	R/W	0	TDM_D5 out src sel:
4:0	R/W	0	TDM_D4 out src sel:

Table 10-108 EE_AUDIO_DAT_PAD_CTRL8 10'h398

Bits	R/W	Default	Description
28:24	R/W	0	TDM_D11 out src sel:
20:16	R/W	0	TDM_D10 out src sel:
12:8	R/W	0	TDM_D9 out src sel:
4:0	R/W	0	TDM_D8 out src sel:

Table 10-109 EE_AUDIO_DAT_PAD_CTRL9 10'h399

Bits	R/W	Default	Description
28:24	R/W	0	TDM_D15 out src sel:
20:16	R/W	0	TDM_D14 out src sel:
12:8	R/W	0	TDM_D13 out src sel:
4:0	R/W	0	TDM_D12 out src sel:

Table 10-110 EE_AUDIO_DAT_PAD_CTRLA 10'h39a

Bits	R/W	Default	Description
28:24	R/W	0	TDM_D19 out src sel:
20:16	R/W	0	TDM_D18 out src sel:

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Bits	R/W	Default	Description
12:8	R/W	0	TDM_D17 out src sel:
4:0	R/W	0	TDM_D16 out src sel:

Table 10-111 EE_AUDIO_DAT_PAD_CTRLB 10'h39b

Bits	R/W	Default	Description
28:24	R/W	0	TDM_D23 out src sel:
20:16	R/W	0	TDM_D22 out src sel:
12:8	R/W	0	TDM_D21 out src sel:
4:0	R/W	0	TDM_D20 out src sel:

Table 10-112 EE_AUDIO_DAT_PAD_CTRLC 10'h39c

Bits	R/W	Default	Description
28:24	R/W	0	TDM_D27 out src sel:
20:16	R/W	0	TDM_D26 out src sel:
12:8	R/W	0	TDM_D25 out src sel:
4:0	R/W	0	TDM_D24 out src sel:

Table 10-113 EE_AUDIO_DAT_PAD_CTRLD 10'h39d

Bits	R/W	Default	Description
28:24	R/W	0	TDM_D31 out src sel:
20:16	R/W	0	TDM_D30 out src sel:
12:8	R/W	0	TDM_D29 out src sel:
4:0	R/W	0	TDM_D28 out src sel:

Table 10-114 EE_AUDIO_DAT_PAD_CTRLE 10'h39e

Bits	R/W	Default	Description
31	R/W	0	TDM_D31 oen sel: 0: reg_oen_val bit31; 1: from TDMOUT;
30	R/W	0	TDM_D30 oen sel: 0: reg_oen_val bit30; 1: from TDMOUT;
…	…	…	…
0	R/W	0	TDM_D0 oen sel: 0: reg_oen_val bit0; 1: from TDMOUT;

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Table 10-115 EE_AUDIO_DAT_PAD_CTRLF 10'h39f

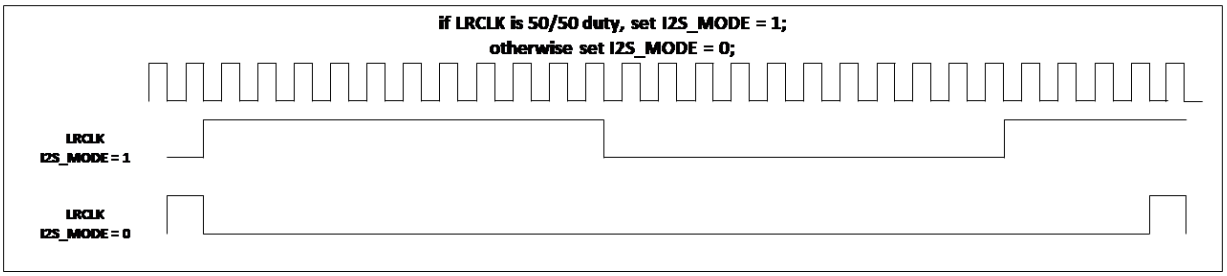
Bits	R/W	Default	Description
31:0	R/W	0	reg_oen_val; 0: output; 1: input; bit31: TDM_D31 bit30: TDM_D30 … bit1: TDM_D1 bit0: TDM_D0

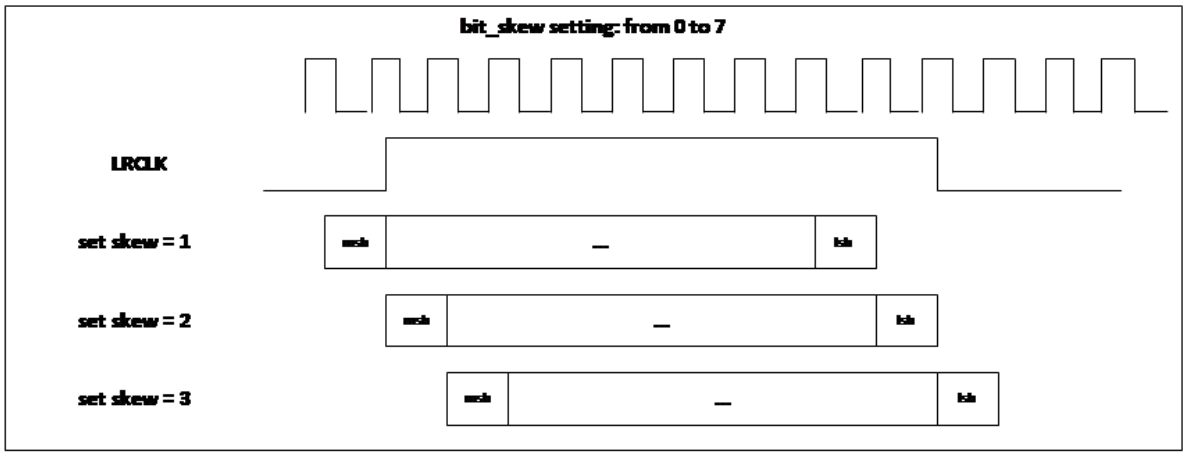
Table 10-116 EE_AUDIO_TDMIN_A_CTRL 10'hc0

Bits	R/W	Default	Description
31	R/W	0x0000-0000	reg_work_enable 0:disable; 1:enable;
30	R/W		reg_i2s_mode,0:tdm mode; 1: i2s mode;
29	R/W		reg_rst_afifo_out_n, reset afifo out side; need set to 1 before reg_rst_afifo_in_n;
28	R/W		reg_rst_afifo_in_n, reset afifo in side; need set 1 after set reg_rst_afifo_out_n to 1;
26	R/W		reg_tdmin_in_resync; force TDMIN stable signal to low, then TDMIN need resync to stable; the condition of stable to high is : detected rise edge of WS
25	R/W		reg_tdmin_in_rev_ws, revert ws(lrclk); 0 :disable; 1: enable;
24	R/W		reg_tdmin_in_rev_dat, revert data; 0:disable; 1:enable;
23:20	R/W		select tdmin src; 0 tdmin_a dat_in 1 tdmin_b dat_in 2 tdmin_c dat_in 3 0 4 hdmirx 5 acodec_adc 6 0 7 0 8 0 9 0 10 0 11 0 12 tdmout_a dat_out 13 tdmout_b dat_out 14 tdmout_c dat_out 15 0
18:16	R/W		reg_tdmin_in_bit_skew, add delay to ws or data for skew modification;
15:13	R/W		reg_stable_mask, each bit can enable one conditioni to pull stable signal to low. bit15: if afifo overflow, will pull stable to low; bit14: if the slot_cnt != reg_tdmin_slot_num, will pull stable to low; bit13: if the bit_cnt != reg_tdmin_bit_num, will pull stable to low;
12:8	R/W		reg_tdmin_slot_num for I2S, it's fixed 0x1. for TDM, the max is 31 which mean 32 slots
7:6	R/W		reg_tdmin_chnum_mode; 0:chnum[7:0] = valid_cnt[7:0] 1:chnum[7:0] = cyc_cnt[3:0] 2:chnum[7:0] = slot_cnt[4:1],cyc_cnt[0] 3:chnum[7:0] = slot_cnt[4:1],cyc_cnt[3:0]

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Bits	R/W	Default	Description
5	R/W		reg_lsb_first, 0: store first bit received to data_store[0]; 1: store first bit received to data_store[31];
4:0	R/W		reg_tdmin_bit_num, bitwidth of each slot, if slot is 16bits, set this register to 15;





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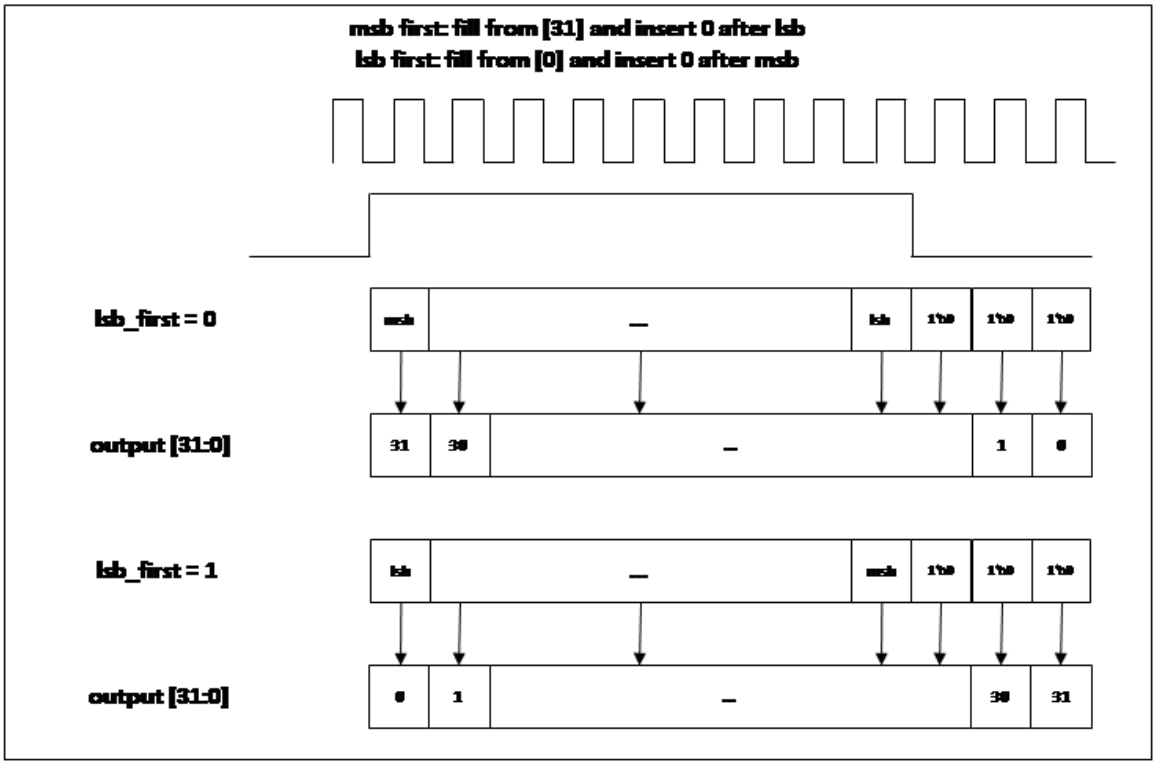


Table 10-117 EE_AUDIO_TDMIN_A_SWAP0 10'hc1

Bits	R/W	Default	Description
31:28	R/W	0x00000000	ch7_sel 0: lane0 left channel; 1: lane0 right channel; 2: lane1 left channel; 3: lane1 right channel; 4: lane2 left channel; 5: lane2 right channel; 6: lane3 left channel; 7: lane3 right channel; 8: lane4 left channel; 9: lane4 right channel; 10: lane5 left channel; 11: lane5 right channel; 12: lane6 left channel; 13: lane6 right channel; 14: lane7 left channel; 15: lane7 right channel;
27:24	R/W		ch6_sel
23:20	R/W		ch5_sel
19:16	R/W		ch4_sel
15:12	R/W		ch3_sel
11:8	R/W		ch2_sel
7:4	R/W		ch1_sel
3:0	R/W		ch0_sel

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Table 10-118 EE_AUDIO_TDMIN_A_SWAP1 10'h260

Bits	R/W	Default	Description
31:28	R/W	0x00000000	ch15_sel
27:24	R/W		ch14_sel
23:20	R/W		ch13_sel
19:16	R/W		ch12_sel
15:12	R/W		ch11_sel
11:8	R/W		ch10_sel
7:4	R/W		ch9_sel
3:0	R/W		ch8_sel

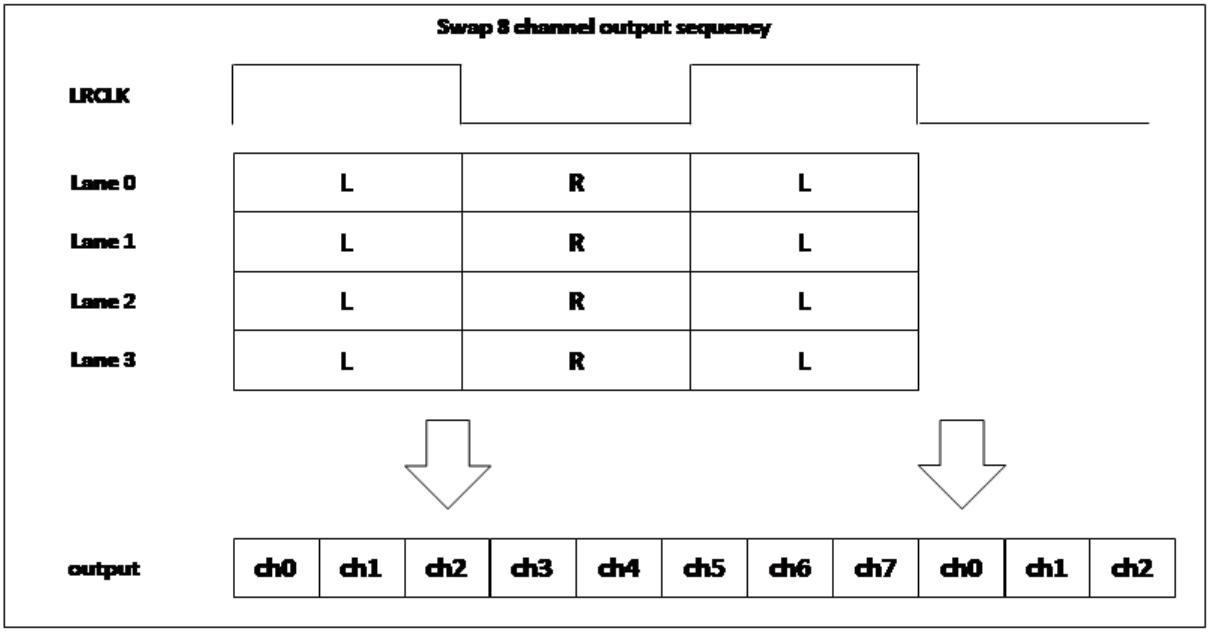


Table 10-119 EE_AUDIO_TDMIN_A_MASK0 10'hc2

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane0_mask, mask each channel in lane0, max is 32 ch;

Table 10-120 EE_AUDIO_TDMIN_A_MASK1 10'hc3

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane1_mask, mask each channel in lane1, max is 32 ch;

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Table 10-121 EE_AUDIO_TDMIN_A_MASK2 10'hc4

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane2_mask, mask each channel in lane2, max is 32 ch;

Table 10-122 EE_AUDIO_TDMIN_A_MASK3 10'hc5

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane3_mask, mask each channel in lane3, max is 32 ch;

Table 10-123 EE_AUDIO_TDMIN_A_MASK4 10'h261

Bits	R/W	Default	Description
31:0	R/W	0x00000000	reg_lane4_mask, mask each channel in lane4, max is 32 ch;

Table 10-124 EE_AUDIO_TDMIN_A_MASK5 10'h262

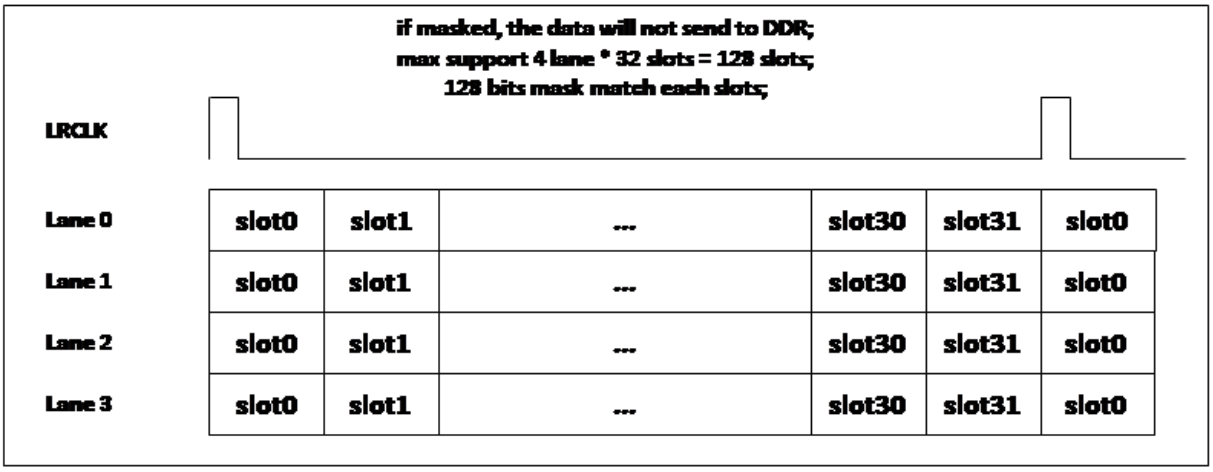
Bits	R/W	Default	Description
31:0	R/W	0x00000000	reg_lane5_mask, mask each channel in lane5, max is 32 ch;

Table 10-125 EE_AUDIO_TDMIN_A_MASK6 10'h263

Bits	R/W	Default	Description
31:0	R/W	0x00000000	reg_lane6_mask, mask each channel in lane6, max is 32 ch;

Table 10-126 EE_AUDIO_TDMIN_A_MASK7 10'h264

Bits	R/W	Default	Description
31:0	R/W	0x00000000	reg_lane7_mask, mask each channel in lane7, max is 32 ch;



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Table 10-127 EE_AUDIO_TDMIN_A_STAT 10'hc6

Bits	R/W	Default	Description
31:29	R	0x0000-0000	afifo_cnt[2:0]
38:24	R		r_input_slot_cnt_max, the maxnum of slot_cnt
23:16	R		r_input_slot_cnt_min, the minnum of slot_cnt
14	R		overflow_flag, overflow flag of afifo
13:10	R		max_fifo_cnt, the maxnum of afifo_cnt
9:5	R		r_input_bit_cnt_max, the maxnum of bit_cnt
4:0	R		r_input_bit_cnt_min, the minnum of bit_cnt

Table 10-128 EE_AUDIO_TDMIN_A_MUTE_VAL 10'hc7

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_tmdin_a_mute_val, when mute , the channel value

Table 10-129 EE_AUDIO_TDMIN_A_MUTE0 10'hc8

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane0_mute, mute each channel in lane0, max is 32 ch;

Table 10-130 EE_AUDIO_TDMIN_A_MUTE1 10'hc9

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane1_mute, mute each channel in lane1, max is 32 ch;

Table 10-131 EE_AUDIO_TDMIN_A_MUTE2 10'hca

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane2_mute, mute each channel in lane2, max is 32 ch;

Table 10-132 EE_AUDIO_TDMIN_A_MUTE3 10'hcb

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane3_mute, mute each channel in lane3, max is 32 ch;

Table 10-133 EE_AUDIO_TDMIN_A_MUTE4 10'h265

Bits	R/W	Default	Description
31:0	R/W	0x000000-00	reg_lane4_mute, mute each channel in lane4, max is 32 ch;

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Table 10-134 EE_AUDIO_TDMIN_A_MUTE5 10'h266

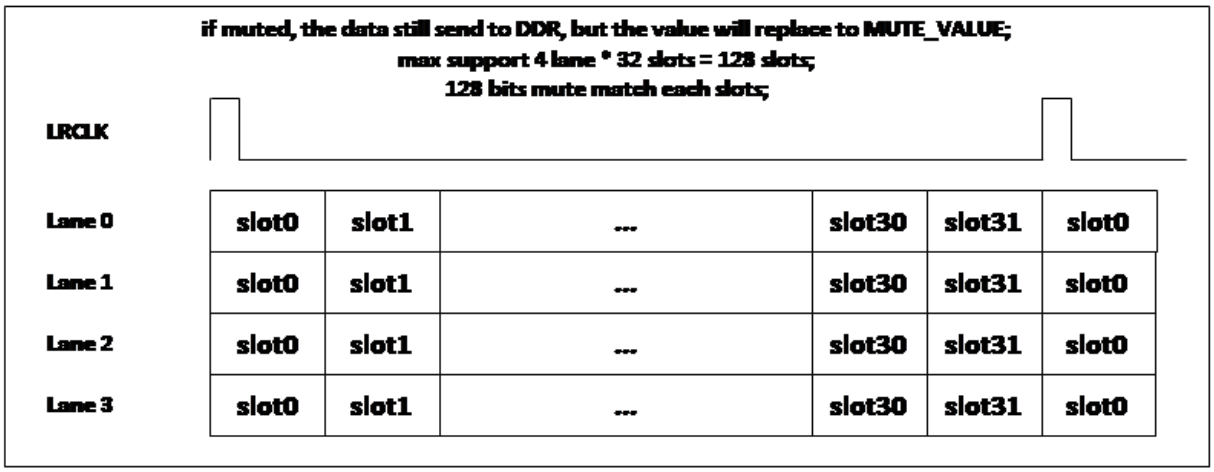
Bits	R/W	Default	Description
31:0	R/W	0x000000-00	reg_lane5_mute, mute each channel in lane5, max is 32 ch;

Table 10-135 EE_AUDIO_TDMIN_A_MUTE6 10'h267

Bits	R/W	Default	Description
31:0	R/W	0x00000000	reg_lane6_mute, mute each channel in lane6, max is 32 ch;

Table 10-136 EE_AUDIO_TDMIN_A_MUTE7 10'h268

Bits	R/W	Default	Description
31:0	R/W	0x00000000	reg_lane7_mute, mute each channel in lane7, max is 32 ch;



EE_AUDIO_TDMIN_B_CTRL 10'hd0
EE_AUDIO_TDMIN_B_SWAP0 10'hd1
EE_AUDIO_TDMIN_B_SWAP1 10'h270
EE_AUDIO_TDMIN_B_MASK0 10'hd2
EE_AUDIO_TDMIN_B_MASK1 10'hd3
EE_AUDIO_TDMIN_B_MASK2 10'hd4
EE_AUDIO_TDMIN_B_MASK3 10'hd5
EE_AUDIO_TDMIN_B_MASK4 10'h271
EE_AUDIO_TDMIN_B_MASK5 10'h272
EE_AUDIO_TDMIN_B_MASK6 10'h273
EE_AUDIO_TDMIN_B_MASK7 10'h274
EE_AUDIO_TDMIN_B_STAT 10'hd6

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EE_AUDIO_TDMIN_B_MUTE_VAL 10'hd7
EE_AUDIO_TDMIN_B_MUTE0 10'hd8
EE_AUDIO_TDMIN_B_MUTE1 10'hd9
EE_AUDIO_TDMIN_B_MUTE2 10'hda
EE_AUDIO_TDMIN_B_MUTE3 10'hdb
EE_AUDIO_TDMIN_B_MUTE4 10'h275
EE_AUDIO_TDMIN_B_MUTE5 10'h276
EE_AUDIO_TDMIN_B_MUTE6 10'h277
EE_AUDIO_TDMIN_B_MUTE7 10'h278

EE_AUDIO_TDMIN_C_CTRL 10'he0
EE_AUDIO_TDMIN_C_SWAP0 10'he1
EE_AUDIO_TDMIN_C_SWAP1 10'h280
EE_AUDIO_TDMIN_C_MASK0 10'he2
EE_AUDIO_TDMIN_C_MASK1 10'he3
EE_AUDIO_TDMIN_C_MASK2 10'he4
EE_AUDIO_TDMIN_C_MASK3 10'he5
EE_AUDIO_TDMIN_C_MASK4 10'h281
EE_AUDIO_TDMIN_C_MASK5 10'h282
EE_AUDIO_TDMIN_C_MASK6 10'h283
EE_AUDIO_TDMIN_C_MASK7 10'h284
EE_AUDIO_TDMIN_C_STAT 10'he6
EE_AUDIO_TDMIN_C_MUTE_VAL 10'he7
EE_AUDIO_TDMIN_C_MUTE0 10'he8
EE_AUDIO_TDMIN_C_MUTE1 10'he9
EE_AUDIO_TDMIN_C_MUTE2 10'hea
EE_AUDIO_TDMIN_C_MUTE3 10'heb
EE_AUDIO_TDMIN_C_MUTE4 10'h285
EE_AUDIO_TDMIN_C_MUTE5 10'h286
EE_AUDIO_TDMIN_C_MUTE6 10'h287
EE_AUDIO_TDMIN_C_MUTE7 10'h288

EE_AUDIO_TDMIN_LB_CTRL 10'hf0
EE_AUDIO_TDMIN_LB_SWAP0 10'hf1
EE_AUDIO_TDMIN_LB_SWAP1 10'h290
EE_AUDIO_TDMIN_LB_MASK0 10'hf2
EE_AUDIO_TDMIN_LB_MASK1 10'hf3

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EE_AUDIO_TDMIN_LB_MASK2 10'hf4
EE_AUDIO_TDMIN_LB_MASK3 10'hf5
EE_AUDIO_TDMIN_LB_MASK4 10'h291
EE_AUDIO_TDMIN_LB_MASK5 10'h292
EE_AUDIO_TDMIN_LB_MASK6 10'h293
EE_AUDIO_TDMIN_LB_MASK7 10'h294
EE_AUDIO_TDMIN_LB_STAT 10'hf6
EE_AUDIO_TDMIN_LB_MUTE_VAL 10'hf7
EE_AUDIO_TDMIN_LB_MUTE0 10'hf8
EE_AUDIO_TDMIN_LB_MUTE1 10'hf9
EE_AUDIO_TDMIN_LB_MUTE2 10'hfa
EE_AUDIO_TDMIN_LB_MUTE3 10'hfb
EE_AUDIO_TDMIN_LB_MUTE4 10'h295
EE_AUDIO_TDMIN_LB_MUTE5 10'h296
EE_AUDIO_TDMIN_LB_MUTE6 10'h297
EE_AUDIO_TDMIN_LB_MUTE7 10'h298

Table 10-137 EE_AUDIO_TDMOUT_A_CTRL0 10'h140

Bits	R/W	Default	Description
31	R/W	0x0000-0000	reg_work_enable, 0:disable; 1:enable;
30	R/W		reg_rst_req_frddr, reset ref_frddr in TDMOUT;
29	R/W		reg_rst_afifo_out_n, reset afifo out side;
28	R/W		reg_rst_afifo_in_n, reset afifo in side; need set 1 after set reg_rst_afifo_out_n to 1;
19:15	R/W		reg_tdm_init_bitnum, initial count value of bitcnt
14:10	R/W		reg_tdm_init_slotnum, initial count value of slotcnt
9:5	R/W		reg_tdmout_slot_num , max value of slotcnt; if each frame has 8 slots, set it to 7;
4:0	R/W		reg_tdmout_bit_num ,max value of bitcnt; if each slot has 16 bits, set it to 15;

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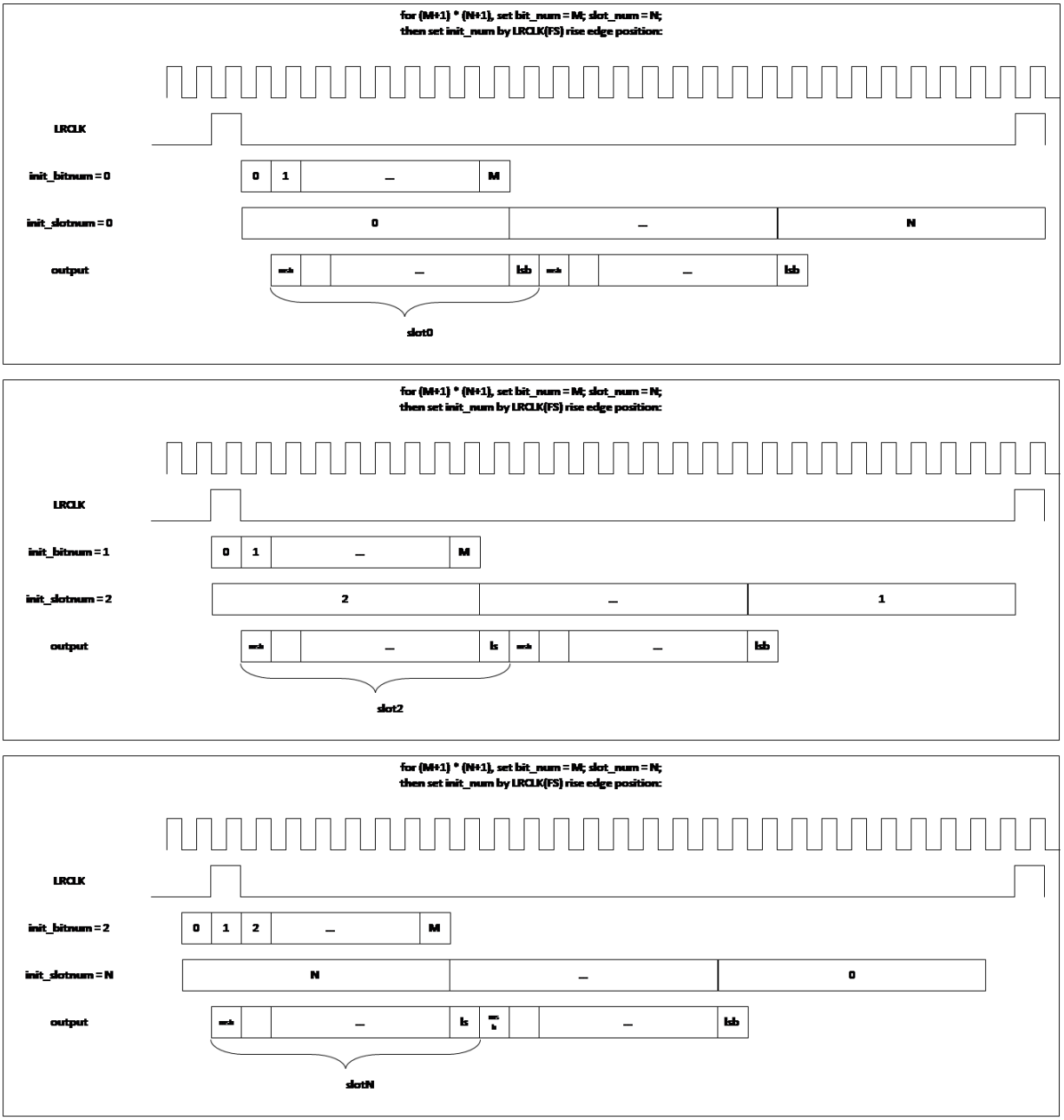


Table 10-138 EE_AUDIO_TDMOUT_A_CTRL1 10'h141

Bits	R/W	Default	Description
31	R/W	0x0000-0000	eq_drc_sel; 1: select eq_drc output;
30	R/W		reg_debug_en,0:disable debug feature; 1: enable;
29	R/W		reg_out_lsb_first, 0: msb first; 1: lsb first;
28	R/W		reg_rev_ws_in, revert ws; 0: disable; 1: enable;
27	R/W		reg_rev_dat, revert data; 0: disable; 1: enable;
26:24	R/W		reg_frddr_sel, 0:frddr_A;1:frddr_B;2:frddr_C; 3:frddr_D;4:frddr_E

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Bits	R/W	Default	Description
23:16	R/W		reg_wait_cnt, wait some time when enable set to 1;then start request data from frddr;
15:14	R/W		reg_gain_shift; 0: data * 1; 1: data * 2; 2: data * 4; 3: data * 8;
12:8	R/W		reg_frddr_msb, msb position of data
6:4	R/W		reg_frddr_type, 0: split 64bits ddr data to 8 sample, each sample need 8 bits; if bitwidth < 8, left-justified; 1: split 64bits ddr data to 4 sample, each sample need 16 bits; if bitwidth < 16, left-justified ; 2: split 64bits ddr data to 4 sample, each sample need 16 bits; if bitwidth < 16, right-justified ; 3: split 64bits ddr data to 2 sample, each sample need 32 bits; if bitwidth < 32, left-justified; 4: split 64bits ddr data to 2 sample, each sample need 32 bits; if bitwidth < 32, right-justified;
3	R/W		reg_keep_req_ddr_init; set 0 will stop sending data if req_ddr stopped by init_done signal pull down.(refer to reg_clr_by_init)
2	R/W		reg_sts_sel;

For position of sample in DDR:

	ddr_data [7:0] (byte)							
type	byte7	byte6	byte5	byte4	byte3	byte2	byte1	byte0
0	s7	s6	s5	s4	s3	s2	s1	s0
	s15	s14	s13	s12	s11	s10	s9	s8
1/2	s3		s2		s1		s0	
	s7		s6		s5		s4	
3/4	s1				s0			
	s3				s2			

For encoder, it will start output[31] first, then output[30], finished at output[32-bit_num]; If lsb_first, will start s[0], then s[1], finished at s[bit_num+1];

	output [31:0] (bit)																														
type	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	s[7]	s[6]	s[5]	s[4]	s[3]	s[2]	s[1]	s[0]	0																							
1	s[15]	s[14]	s[13]	s[12]	s[11]	s[10]	s[9]	s[8]	s[7]	s[6]	s[5]	s[4]	s[3]	s[2]	s[1]	s[0]	0															
2	s[msb]	s[msb-1]	...			s[1]	s[0]	0																								
3	s[31]	s[30]	s[29]	s[28]	s[27]	s[26]	s[25]	s[24]	s[23]	s[22]	s[21]	s[20]	s[19]	s[18]	s[17]	s[16]	s[15]	s[14]	s[13]	s[12]	s[11]	s[10]	s[9]	s[8]	s[7]	s[6]	s[5]	s[4]	s[3]	s[2]	s[1]	s[0]
4	s[msb]	s[msb-1]	...																			s[1]	s[0]	0								

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Table 10-139 EE_AUDIO_TDMOUT_A_CTRL2 10'h2a0

Bits	R/W	Default	Description
31:24	R/W	0x00000000	reg_clr_by_init; when FRDDR is disable, its init_done will pull down, then need clear the status of REQ_FRDDR. 31: clear init_finish; 30:clear data_buff; 29:clear gain related; 28:clear DDR_REQ; 27:clear ack_masked(mean received first init_done); 26:clear afifo in; 25:clear afifo out ; 24:clear bit_cnt/slot_cnt/fit_num/wait_cnt;
7:0	R/W		reg_tdm_lr_mix, [7]: mix l7 and r7; [6]: mix l6 and r6; [5]: mix l5 and r5; [4]: mix l4 and r4; [3]: mix l3 and r3; [2]: mix l2 and r2; [1]: mix l1 and r1; [0]: mix l0 and r0;

Table 10-140 EE_AUDIO_TDMOUT_A_SWAP0 10'h142

Bits	R/W	Default	Description
31:28	R/W	0x00000000	ch7_sel 0: lane0 left channel; 1: lane0 right channel; 2: lane1 left channel; 3: lane1 right channel; 4: lane2 left channel; 5: lane2 right channel; 6: lane3 left channel; 7: lane3 right channel; 8: lane4 left channel; 9: lane4 right channel; 10: lane5 left channel; 11: lane5 right channel; 12: lane6 left channel; 13: lane6 right channel; 14: lane7 left channel; 15: lane7 right channel;
27:24	R/W		ch6_sel
23:20	R/W		ch5_sel
19:16	R/W		ch4_sel
15:12	R/W		ch3_sel
11:8	R/W		ch2_sel
7:4	R/W		ch1_sel
3:0	R/W		ch0_sel

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Table 10-141 EE_AUDIO_TDMOUT_A_SWAP1 10'h2a1

Bits	R/W	Default	Description
31:28	R/W	0x00000000	ch15_sel
27:24	R/W		ch14_sel
23:20	R/W		ch13_sel
19:16	R/W		ch12_sel
15:12	R/W		ch11_sel
11:8	R/W		ch10_sel
7:4	R/W		ch9_sel
3:0	R/W		ch8_sel

Table 10-142 EE_AUDIO_TDMOUT_A_MASK0 10'h143

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane0_mask, mask each channel in lane0, max is 32 ch;

Table 10-143 EE_AUDIO_TDMOUT_A_MASK1 10'h144

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane1_mask, mask each channel in lane1, max is 32 ch;

Table 10-144 EE_AUDIO_TDMOUT_A_MASK2 10'h145

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane2_mask, mask each channel in lane2, max is 32 ch;

Table 10-145 EE_AUDIO_TDMOUT_A_MASK3 10'h146

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane3_mask, mask each channel in lane3, max is 32 ch;

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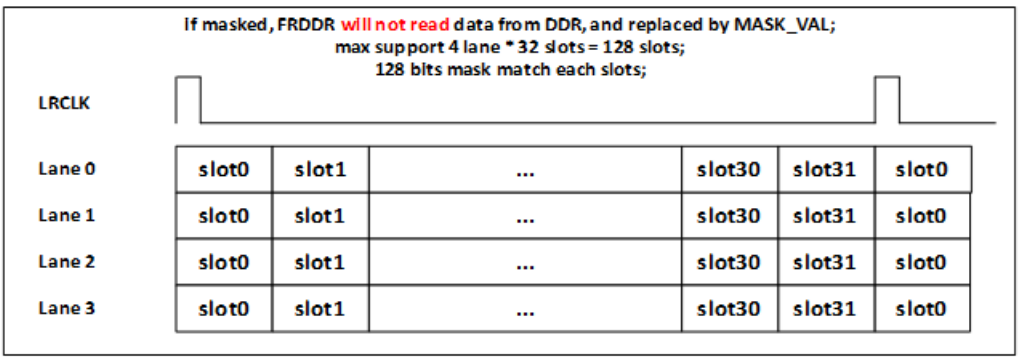


Table 10-146 EE_AUDIO_TDMOUT_A_MASK4 10'h2a4

Bits	R/W	Default	Description
31:0	R/W	0x00000000	reg_lane4_mask, mask each channel in lane4, max is 32 ch;

Table 10-147 EE_AUDIO_TDMOUT_A_MASK5 10'h2a5

Bits	R/W	Default	Description
31:0	R/W	0x00000000	reg_lane5_mask, mask each channel in lane5, max is 32 ch;

Table 10-148 EE_AUDIO_TDMOUT_A_MASK6 10'h2a6

Bits	R/W	Default	Description
31:0	R/W	0x00000000	reg_lane6_mask, mask each channel in lane6, max is 32 ch;

Table 10-149 EE_AUDIO_TDMOUT_A_MASK7 10'h2a7

Bits	R/W	Default	Description
31:0	R/W	0x00000000	reg_lane7_mask, mask each channel in lane7, max is 32 ch;

Table 10-150 EE_AUDIO_TDMOUT_A_MASK_VAL 10'h14f

Bits	R/W	Default	Description
31:0	R/W	0x00000000	reg_tdmout_mask_val, when masked, the channel value

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Table 10-151 EE_AUDIO_TDMOUT_A_STAT 10'h147

Bits	R/W	Default	Description

31:0	R	0x0000-0000	if reg_sts_sel = 1, it's reg_cur_gain_val;
			if reg_sts_sel = 0, it's another sts as blow:
			bit31:29 : fifo_cnt, afifo cnt
			bit28 : up_error, change to 1 if overflow
			bit27:24 : req_frdd_fsm_stat
			bit21 : r_slot_cnt_err
			bit20 : r_bit_cnt_err
			bit16:12 : r_max_slot_cnt
			bit8:4 : r_max_bit_cnt
			bit3 : r_out_en
			bit2 : r_out_en_pre
			bit1 : r_first_fs
			bit0 : c_frdd_init_finish

Table 10-152 EE_AUDIO_TDMOUT_A_GAIN0 10'h148

Bits	R/W	Default	Description
31:24	R/W	0xFF	gain_ch3
23:16	R/W	0xFF	gain_ch2
15:8	R/W	0xFF	gain_ch1
7:0	R/W	0xFF	gain_ch0

Table 10-153 EE_AUDIO_TDMOUT_A_GAIN1 10'h149

Bits	R/W	Defaul9	Description
31:24	R/W	0xFF	gain_ch7
23:16	R/W	0xFF	gain_ch6
15:8	R/W	0xFF	gain_ch5
7:0	R/W	0xFF	gain_ch4

Table 10-154 EE_AUDIO_TDMOUT_A_GAIN2 10'h2a2

Bits	R/W	Default	Description
31:24	R/W	0xFF	gain_ch11
23:16	R/W	0xFF	gain_ch10
15:8	R/W	0xFF	gain_ch9
7:0	R/W	0xFF	gain_ch8

Table 10-155 EE_AUDIO_TDMOUT_A_GAIN3 10'h2a3

Bits	R/W	Default	Description
31:24	R/W	0xFF	gain_ch15
23:16	R/W	0xFF	gain_ch14

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Bits	R/W	Default	Description
15:8	R/W	0xFF	gain_ch13
7:0	R/W	0xFF	gain_ch12

Table 10-156 EE_AUDIO_TDMOUT_A_MUTE_VAL 10'h14a

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_tmdin_a_mute_val, when mute, the channel value

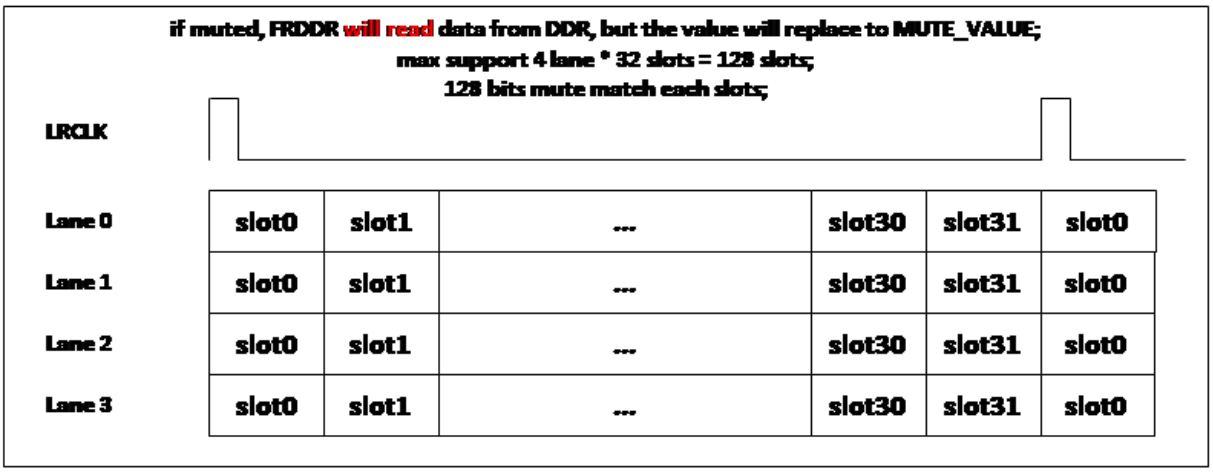


Table 10-157 EE_AUDIO_TDMOUT_A_MUTE0 10'h14b

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane0_mute, mute each channel in lane0, max is 32 ch;

Table 10-158 EE_AUDIO_TDMOUT_A_MUTE1 10'h14c

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane1_mute, mute each channel in lane1, max is 32 ch;

Table 10-159 EE_AUDIO_TDMOUT_A_MUTE2 10'h14d

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane2_mute, mute each channel in lane2 max is 32 ch;

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Table 10-160 EE_AUDIO_TDMOUT_A_MUTE3 10'h14e

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_lane3_mute, mute each channel in lane3, max is 32 ch;

Table 10-161 EE_AUDIO_TDMOUT_A_MUTE4 10'h2a8

Bits	R/W	Default	Description
31:0	R/W	0x00000000	reg_lane4_mute, mute each channel in lane4, max is 32 ch;

Table 10-162 EE_AUDIO_TDMOUT_A_MUTE5 10'h2a9

Bits	R/W	Default	Description
31:0	R/W	0x00000000	reg_lane5_mute, mute each channel in lane5, max is 32 ch;

Table 10-163 EE_AUDIO_TDMOUT_A_MUTE6 10'h2aa

Bits	R/W	Default	Description
31:0	R/W	0x00000000	reg_lane6_mute, mute each channel in lane6 max is 32 ch;

Table 10-164 EE_AUDIO_TDMOUT_A_MUTE7 10'h2ab

Bits	R/W	Default	Description
31:0	R/W	0x00000000	reg_lane7_mute, mute each channel in lane7, max is 32 ch;

Table 10-165 EE_AUDIO_TDMOUT_A_GAIN_EN 10'h2ac

Bits	R/W	Default	Description
31:16	R/W	0x0000-0000	
15	R/W	0x0000-0000	ch15 gain_en; 1: out = in * gain_ch15; 0: out = in;
14	R/W	0x0000-0000	ch14 gain_en; 1: out = in * gain_ch14; 0: out = in;
13	R/W	0x0000-0000	ch13 gain_en; 1: out = in * gain_ch13; 0: out = in;
12	R/W	0x0000-0000	ch12 gain_en; 1: out = in * gain_ch12; 0: out = in;
11	R/W	0x0000-0000	ch11 gain_en; 1: out = in * gain_ch11; 0: out = in;
10	R/W	0x0000-0000	ch10 gain_en; 1: out = in * gain_ch10; 0: out = in;
9	R/W	0x0000-0000	ch9 gain_en; 1: out = in * gain_ch9; 0: out = in;
8	R/W	0x0000-0000	ch8 gain_en; 1: out = in * gain_ch8; 0: out = in;

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Bits	R/W	Default	Description
7	R/W	0x0000-0000	ch7 gain_en; 1: out = in * gain_ch7; 0: out = in;
6	R/W	0x0000-0000	ch6 gain_en; 1: out = in * gain_ch6; 0: out = in;
5	R/W	0x0000-0000	ch5 gain_en; 1: out = in * gain_ch5; 0: out = in;
4	R/W	0x0000-0000	ch4 gain_en; 1: out = in * gain_ch4; 0: out = in;
3	R/W	0x0000-0000	ch3 gain_en; 1: out = in * gain_ch3; 0: out = in;
2	R/W	0x0000-0000	ch2 gain_en; 1: out = in * gain_ch2; 0: out = in;
1	R/W	0x0000-0000	ch1 gain_en; 1: out = in * gain_ch1; 0: out = in;
0	R/W	0x0000-0000	ch0 gain_en; 1: out = in * gain_ch0; 0: out = in;

Table 10-166 EE_AUDIO_TDMOUT_A_GAIN_CTRL 10'h2ad

Bits	R/W	Default	Description
31	R/W	0x0000-0000	reg_gain_step_chg; 0: the current_gain will follow direct to reg_gain change; 1: the current_gain will follow step by step to reg_gain change; etc: change reg_gain from 40 to 50, and gain_step = 3; the currenct_gain will change as: 40->43->46->49->50;
25:24	R/W		reg_cur_gain_sel; 0: cur_gain_sts = ch3,ch2,ch1,ch0; 1: cur_gain_sts = ch7,ch6,ch5,ch4; 2: cur_gain_sts = ch11,ch10,ch9,ch8; 3: cur_gain_sts = ch15,ch14,ch13,ch12;
23:16	R/W		reg_gain_step; modified gain value each time;
15:0	R/W		reg_gain_updt_timer; the period of each change, unit is FS;

EE_AUDIO_TDMOUT_B_CTRL0 10'h150

EE_AUDIO_TDMOUT_B_CTRL1 10'h151

EE_AUDIO_TDMOUT_B_CTRL2 10'h2b0

EE_AUDIO_TDMOUT_B_SWAP0 10'h152

EE_AUDIO_TDMOUT_B_SWAP1 10'h2b1

EE_AUDIO_TDMOUT_B_MASK0 10'h153

EE_AUDIO_TDMOUT_B_MASK1 10'h154

EE_AUDIO_TDMOUT_B_MASK2 10'h155

EE_AUDIO_TDMOUT_B_MASK3 10'h156

EE_AUDIO_TDMOUT_B_MASK4 10'h2b4

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EE_AUDIO_TDMOUT_B_MASK5 10'h2b5
EE_AUDIO_TDMOUT_B_MASK6 10'h2b6
EE_AUDIO_TDMOUT_B_MASK7 10'h2b7
EE_AUDIO_TDMOUT_B_STAT 10'h157
EE_AUDIO_TDMOUT_B_GAIN0 10'h158
EE_AUDIO_TDMOUT_B_GAIN1 10'h159
EE_AUDIO_TDMOUT_B_GAIN2 10'h2b2
EE_AUDIO_TDMOUT_B_GAIN3 10'h2b3
EE_AUDIO_TDMOUT_B_MUTE_VAL 10'h15a
EE_AUDIO_TDMOUT_B_MUTE0 10'h15b
EE_AUDIO_TDMOUT_B_MUTE1 10'h15c
EE_AUDIO_TDMOUT_B_MUTE2 10'h15d
EE_AUDIO_TDMOUT_B_MUTE3 10'h15e
EE_AUDIO_TDMOUT_B_MUTE4 10'h2b8
EE_AUDIO_TDMOUT_B_MUTE5 10'h2b9
EE_AUDIO_TDMOUT_B_MUTE6 10'h2ba
EE_AUDIO_TDMOUT_B_MUTE7 10'h2bb
EE_AUDIO_TDMOUT_B_MASK_VAL 10'h15f
EE_AUDIO_TDMOUT_B_GAIN_EN 10'h2bc
EE_AUDIO_TDMOUT_B_GAIN_CTRL 10'h2bd
EE_AUDIO_TDMOUT_C_CTRL0 10'h160
EE_AUDIO_TDMOUT_C_CTRL1 10'h161
EE_AUDIO_TDMOUT_C_CTRL2 10'h2c0
EE_AUDIO_TDMOUT_C_SWAP0 10'h162
EE_AUDIO_TDMOUT_C_SWAP1 10'h2c1
EE_AUDIO_TDMOUT_C_MASK0 10'h163
EE_AUDIO_TDMOUT_C_MASK1 10'h164
EE_AUDIO_TDMOUT_C_MASK2 10'h165
EE_AUDIO_TDMOUT_C_MASK3 10'h166
EE_AUDIO_TDMOUT_C_MASK4 10'h2b4
EE_AUDIO_TDMOUT_C_MASK5 10'h2b5
EE_AUDIO_TDMOUT_C_MASK6 10'h2b6
EE_AUDIO_TDMOUT_C_MASK7 10'h2b7
EE_AUDIO_TDMOUT_C_STAT 10'h167
EE_AUDIO_TDMOUT_C_GAIN0 10'h168
EE_AUDIO_TDMOUT_C_GAIN1 10'h169
EE_AUDIO_TDMOUT_C_GAIN2 10'h2c2
EE_AUDIO_TDMOUT_C_GAIN3 10'h2c3

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EE_AUDIO_TDMOUT_C_MUTE_VAL 10'h16a
EE_AUDIO_TDMOUT_C_MUTE0 10'h16b
EE_AUDIO_TDMOUT_C_MUTE1 10'h16c
EE_AUDIO_TDMOUT_C_MUTE2 10'h16d
EE_AUDIO_TDMOUT_C_MUTE3 10'h16e
EE_AUDIO_TDMOUT_C_MUTE4 10'h2c8
EE_AUDIO_TDMOUT_C_MUTE5 10'h2c9
EE_AUDIO_TDMOUT_C_MUTE6 10'h2ca
EE_AUDIO_TDMOUT_C_MUTE7 10'h2cb
EE_AUDIO_TDMOUT_C_MASK_VAL 10'h16f
EE_AUDIO_TDMOUT_C_GAIN_EN 10'h2cc
EE_AUDIO_TDMOUT_C_GAIN_CTRL 10'h2cd

10.10.8 SPDIF Registers

Table 10-167 EE_AUDIO_SPDIFIN_CTRL0 10'h100

Bits	R/W	Default	Description
31	R/W	0x0000-0000	reg_work_enable, 0: disable; 1:enable;
30	R/W		reg_chnum_sel, 0: ch_num = 0~383(include frame cnt); 1: ch_num = 0~1(only L/R);
29	R/W		reg_rst_afifo_out_n, reset afifo out side;
28	R/W		reg_rst_afifo_in_n, reset afifo in side; need set 1 after set reg_rst_afifo_out_n to 1;
27	R/W		reg_debug_en, 0:disable debug; 1: enable;
26	R/W		reg_exception_sts_clr;
25	R/W		reg_findpapb_en, 0: disable NonPCM mode; 1: enable;
24	R/W		reg_width_sel, 0: detect sample mode by max_width;1: detect sample mode by min_width;
23:12	R/W		reg_nonpcm2pcm_th, when detected NonPcm mode;if long time (z_cnt >= th) didn't detect PaPb again, will generate interrupt to SW: now changed to PCM mode;
11:8	R/W		reg_ch_status_sel, For EE_AUDIO_SPDIFIN_STAT1
7	R/W		reg_mute_l, 0: disable ; 1: mute channel L;
6	R/W		reg_mute_r, 0: disable ; 1: mute channel R;
5:4	R/W		reg_spdifin_src_sel, 0: PAD of spdifin;1: spdifout;
3	R/W		reg_check_valid, 0: disable valid check ; 1: enable;
2	R/W		reg_check_parity, 0: disable parity check ; 1: enable;
1	R/W		reg_invert_data, 0: disalbe; 1: invert [27:4] to [4:27];
0	R/W		reg_spdifin_phase, 0: disable invert; 1: enable;

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Table 10-168 EE_AUDIO_SPDIFIN_CTRL1 10'h101

Bits	R/W	Default	Description
31	R/W	0x0000-0000	reg_force_sample_mode, 0: auto detect sample mode; 1: force a fixed sample mode;
30:28	R/W		reg_sample_mode
27:20	R/W		reg_interrupt_mask, mask each interrupt;
19:0	R/W		reg_base_timer, define a base timer to detect sample mode changed; need *256;

Table 10-169 EE_AUDIO_SPDIFIN_CTRL2 10'h102

Bits	R/W	Default	Description
29:20	R/W	0x0000-0000	reg_sample_mode0_timer_th
19:10	R/W		reg_sample_mode1_timer_th
9:0	R/W		reg_sample_mode2_timer_th

Table 10-170 EE_AUDIO_SPDIFIN_CTRL3 0x103

Bits	R/W	Default	Description
29:20	R/W	0x0000-0000	reg_sample_mode3_timer_th
19:10	R/W		reg_sample_mode4_timer_th
9:0	R/W		reg_sample_mode5_timer_th

Table 10-171 EE_AUDIO_SPDIFIN_CTRL4 10'h104

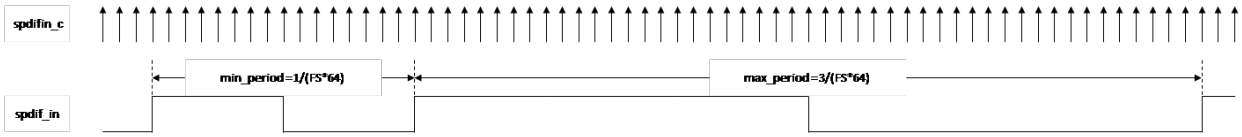
Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	reg_sample_mode0_timer
23:16	R/W		reg_sample_mode1_timer
15:8	R/W		reg_sample_mode2_timer
7:0	R/W		reg_sample_mode3_timer

Table 10-172 EE_AUDIO_SPDIFIN_CTRL5 10'h105

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	reg_sample_mode4_timer
23:16	R/W		reg_sample_mode5_timer
15:8	R/W		reg_sample_mode6_timer

We need automatically detect the frequency of sample rate (FS). It will done by search min_period or max_period of SPDIF IN and compared to thresholds. We can support 7 mode settings.

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For example: If spdifin_clk is 166MHz, and we want support 48KHz and 96KHz.

The min_period of 48KHz is 1/(48000*64) and the counter number by 166MHz is 166000000/(48000*64) = 54;

96KHz counter number is 166000000/(96000*64) = 27;

Then set:

Width_sel = 1;

Mode0_th = (54+27)/2 = 41;

Mode1_th = 0;

Mode0_timer = 27;

Mode1_timer = 13;

Or:

Width_sel = 0;

Mode0_th = (162+81)/2 = 121;

Mode1_th = 0;

Mode0_timer = 27;

Mode1_timer = 13;

More example:

spdifin_clk = 166MHz								
			width_sel = 1			width_sel = 0		
	FS(Hz)	timer	min_ period			max_ period		
mode0	24000	54	108.0729-167	th0	95	324.2187-5	th0	283
mode1	32000	40	81.05468-75	th1	70	243.1640-625	th1	209
mode2	44100	29	58.81519-274	th2	58	176.4455-782	th2	172
mode3	46000	28	56.38586-957	th3	55	169.1576-087	th3	165
mode4	48000	27	54.03645-833	th4	41	162.1093-75	th4	121
mode5	96000	13	27.01822-917	th5	20	81.05468-75	th5	60
mode6	192000	6	13.50911-458			40.52734-375		

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spdifin_clk = 250MHz								
			width_sel = 1			width_sel = 0		
	FS(Hz)	timer	min_ period			max_ period		
mode0	24000	81	162.7604-167	th0	142	488.2812-5	th0	427
mode1	32000	61	122.0703-125	th1	105	366.2109-375	th1	315
mode2	44100	44	88.57709-751	th2	87	265.7312-925	th2	260
mode3	46000	42	84.91847-826	th3	83	254.7554-348	th3	249
mode4	48000	40	81.38020-833	th4	61	244.1406-25	th4	183
mode5	96000	20	40.69010-417	th5	31	122.0703-125	th5	91
mode6	192000	10	20.34505-208			61.03515-625		

spdifin_clk = 400MHz								
			width_sel = 1			width_sel = 0		
	FS(Hz)	timer	min_ period			max_ period		
mode0	24000	130	260.4166-667	th0	228	781.25	th0	683
mode1	32000	97	195.3125	th1	169	585.9375	th1	505
mode2	44100	70	141.7233-56	th2	139	425.1700-68	th2	416
mode3	46000	67	135.8695-652	th3	133	407.6086-957	th3	399
mode4	48000	65	130.2083-333	th4	98	390.625	th4	292
mode5	96000	32	65.10416-667	th5	49	195.3125	th5	146
mode6	192000	16	32.55208-333			97.65625		

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Table 10-173 EE_AUDIO_SPDIFIN_CTRL6 10'h106

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	Reg_clr_internal_sts[7:0]; 7: clear valid bit status; 6: clear parity bit status; 5: clear ch status; 4: clear z_cnt status; 3: clear find_nonpcm status; 2: clear pd_data status; 1: clear pc_data status; 0: clear find_papb status;
23:16	R/W		Reg_clr_interrupt[7:0] for each bit of irq_status[7:0];
14	R/W		enable send out find_z
13	R/W		irq_mode; 0: pulse; 1: level;
12	R/W		update_sample_mode_filter_en 0: by 1 width; 1: by average of 4 width;
8	R/W		reg_papb_ext_sync, 1: add ext "0" sync check for papb; 0: disable;
7:0	R/W		reg_papb_ext_mask, mask 8 channel "0" sync

Table 10-174 EE_AUDIO_SPDIFIN_STAT0 10'h107

Bits	R/W	Default	Description
31	R/W	0x0000-0000	Valid bit
30:28	R/W		r_sample_mode, current sample mode;
27:18	R/W		r_width_min, the min width of two edge;
17:8	R/W		r_width_max, the max width of two edge;
7:0	R/W		r_interrupt_status, interrupt status, need clear by reg_clk_interrupt; [7]: find PaPb; [6]: valid changed; [5]: find nonpcm to pcm (reg_nonpcm2pcm_th) ; [4]: find Pc or Pd changed; [3]: find CH status changed; [2]: find sample mode changed; [1]: find parity error; [0]: find overflow;

Table 10-175 EE_AUDIO_SPDIFIN_STAT1 10'h108

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	channel status, by reg_ch_status_sel; reg_ch_status_sel[3]: 0: channel A; 1: channel B; reg_ch_status_sel[2:0]: 0: ch_status[31:0]; 1: ch_status[63:32]; 2: ch_status[95:64]; 3: ch_status[127:96]; 4: ch_status[159:128]; 5: ch_status[191:160]; 6: pc[15:0],pd[15:0];

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Table 10-176 EE_AUDIO_SPDIFIN_STAT2 10'h109

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	debug status, by reg_ch_status_sel; 0: r_z_width, the width of two preamble Z; 1: {16'd0, frame_cnt_min[7:0], frame_cnt_max[7:0]}; 2: {6'd0,width_min[9:0],2'd0,afifo_cnt[3:0], width_max[9:0]};

Table 10-177 EE_AUDIO_SPDIFIN_MUTE_VAL 10'h10a

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_spdifin_mute_val, when muted, the channel value

Table 10-178 EE_AUDIO_SPDIFIN_CTRL7 10'h10b

Bits	R/W	Default	Description
31	R/W	0x0000-0000	hold_tri_sample 0: stop capture if received triple 0 or 1;
30	R/W		add_ch_r; when unstable, spdifin will stop send data; set this register to 1 will check current status, if missed ch_r, will add one more ch_r which value is 0;
27:20	R/W		stable_mask; condition of pull stable low; 27: xz_err; 26: afifo overflow; 25: cyc_err2; sample width < reg_stable_cyc_min 24: cyc_err1; sample width > reg_stable_cyc_max; 23: parity_err; 22: bit_cnt_err2; >64 21: bit_cnt_err1; != 64 20: xyz_err
19:16	R/W		stable_zcnt; the condition to pull stable high
15:8	R/W		stable_cyc_min
7:0	R/W		stable_cyc_max

Table 10-179 EE_AUDIO_SPDIFOUT_STAT 10'h120

Bits	R/W	Default	Description
31:0	R	0x0000-0000	reg_sts_sel = 0: bit7:5: fifo_cnt, afifo cnt; bit4: up_error, change to 1 if overflow bit3:0: req_frdd_fsm_stat reg_sts_sel = 1: cur_gain_val from REQ_FRDDR;

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Table 10-180 EE_AUDIO_SPDIFOUT_GAIN0 10'h121

Bits	R/W	Default	Description
31:24	R/W	0xFF	gain_ch3
23:16	R/W	0xFF	gain_ch2
15:8	R/W	0xFF	gain_ch1
7:0	R/W	0xFF	gain_ch0

Table 10-181 EE_AUDIO_SPDIFOUT_GAIN1 10'h122

Bits	R/W	Default	Description
31:24	R/W	0xFF	gain_ch7
23:16	R/W	0xFF	gain_ch6
15:8	R/W	0xFF	gain_ch5
7:0	R/W	0xFF	gain_ch4

Table 10-182 EE_AUDIO_SPDIFOUT_CTRL0 10'h123

Bits	R/W	Default	Description
31	R/W	0x0000-0000	reg_work_enable, 0: disable ; 1: enable;
30	R/W		reg_req_frddr_rst; 1: reset REQ_FRDDR in SPDIFOUT;
29	R/W		reg_rst_afifo_out_n, reset afifo out side;
28	R/W		reg_rst_afifo_in_n, reset afifo in side; need set 1 after set reg_rst_afifo_out_n to 1;
27	R/W		reg_hold_start_en; 1: add delay to match TDM out when share buff;
26	R/W		reg_userdata_sel, 0: "user data" = reg_userdata_set; 1: "user data " = data [29];
25	R/W		reg_userdata_set
24	R/W		reg_chdata_sel, 0: "ch status" = reg_chsts0~B ;1: "ch status" = data [30];
23	R/W		reg_mix_lr, 0: disable; 1: L = (L+R)/2; R = (L+R)/2;
22	R/W		reg_mute_l, 0: disable; 1: ch_l_data = reg_mute_val;
21	R/W		reg_mute_r, 0: disable; 1: ch_r_data = reg_mute_val;
20	R/W		reg_data_sel, 0: insert data from 31bits;1: insert data from 27bits;
19	R/W		reg_out_msb_first, 0: lsb first; 1: msb first;
18	R/W		reg_valid_sel, 0: "valid flag" = reg_valid_set; 1: "valid flag" = data [28];
17	R/W		reg_valid_set
16	R/W		reg_parity_mask; initial parity value
15:0	R/W		reg_mask, [15:14]: mask lane7 L/R; [13:12]: mask lane6 L/R; [11:10]: mask lane5 L/R; [9:8]: mask lane4 L/R; [7:6]: mask lane3 L/R; [5:4]: mask lane2 L/R; [3:2]: mask lane1 L/R; [1:0]: mask lane0 L/R;

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Table 10-183 EE_AUDIO_SPDIFOUT_CTRL1 10'h124

Bits	R/W	Default	Description
21	R/W	0x00000000	eq_drc_sel; 1: select eq_drc data;
26:24	R/W		reg_frddr_sel, 0:frddr_A; 1:frddr_B; 2:frddr_C; 3:frddr_D; 4:frddr_E;
23:16	R/W		reg_wait_cnt, wait some time when enable set to 1; then start request data from frddr;
15:14	R/W		reg_gain_shift; 0: data * 1; 1: data * 2; 2: data * 4; 3: data * 8;
12:8	R/W		reg_frddr_msb, msb position of data
7	R/W		Reg_force_start; 1: needn't ack from FRDDR; for only transmit "ch status" usage.
6:4	R/W		reg_frddr_type,0: split 64bits ddr data to 8 sample, each sample need 8 bits; if bitwidth < 8, left-justified; 1: split 64bits ddr data to 4 sample, each sample need 16 bits; if bitwidth < 16, left-justified ; 2: split 64bits ddr data to 4 sample, each sample need 16 bits; if bitwidth < 16, right-justified ; 3: split 64bits ddr data to 2 sample, each sample need 32 bits; if bitwidth < 32, left-justified; 4: split 64bits ddr data to 2 sample, each sample need 32 bits; if bitwidth < 32, right-justified;
3	R/W		reg_keep_req_ddr_init; set 0 will stop sending data if req_ddr stopped by init_done signal pull down.(refer to reg_clr_by_init)
2	R/W		reg_sts_sel;

Table 10-184 EE_AUDIO_SPDIFOUT_PREAMB 10'h125

Bits	R/W	Default	Description
31	R/W	0x0000-0000	set preamble Z, 0: preamble Z = 8'b11101000; 1: reg[7:0];
20	R/W		set preamble Y, 0: preamble Z = 8'b11100100; 1: reg[15:8];
29	R/W		set preamble X, 0: preamble Z = 8'b11100010; 1: reg[23:16];
23:16	R/W		preamble X
15:8	R/W		preamble Y
7:0	R/W		preamble Z

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Table 10-185 EE_AUDIO_SPDIFOUT_SWAP 10'h126

Bits	R/W	Default	Description
31:16	R/W	0x0000-0000	hold start cnt, work when CTRL0[27] = 1;
15:8	R/W		reg_clr_by_init; when FRDDR is disable, its init_done will pull down, then need clear the status of REQ_FRDDR. 15: clear init_finish; 14:clear data_buff; 13:clear gain related; 12:clear DDR_REQ; 11:clear ack_masked(mean received first init_done); 10:clear afifo in; 9:clear afifo out ; 8:clear bit_cnt/slot_cnt/fit_num/wait_cnt;
7:4	R/W		lane0 right ch sel,
3:0	R/W		lane0 left ch sel,

Table 10-186 EE_AUDIO_SPDIFOUT_CHSTS0 10'h127

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	channel A status[31:0]

Table 10-187 EE_AUDIO_SPDIFOUT_CHSTS1 10'h128

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	channel A status[63:32]

Table 10-188 EE_AUDIO_SPDIFOUT_CHSTS2 10'h129

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	channel A status[95:64]

Table 10-189 EE_AUDIO_SPDIFOUT_CHSTS3 10'h12a

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	channel A status[127:96]

Table 10-190 EE_AUDIO_SPDIFOUT_CHSTS4 10'h12b

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	channel A status[159:128]

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Table 10-191 EE_AUDIO_SPDIFOUT_CHSTS5 10'h12cv

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	channel A status[191:160]

Table 10-192 EE_AUDIO_SPDIFOUT_CHSTS6 10'h12d

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	channel B status[31:0]

Table 10-193 EE_AUDIO_SPDIFOUT_CHSTS7 10'h12e

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	channel B status[63:32]

Table 10-194 EE_AUDIO_SPDIFOUT_CHSTS8 10'h12f

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	channel B status[95:64]

Table 10-195 EE_AUDIO_SPDIFOUT_CHSTS9 10'h130

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	channel B status[127:96]

Table 10-196 EE_AUDIO_SPDIFOUT_CHSTSA 10'h131

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	channel B status[159:128]

Table 10-197 EE_AUDIO_SPDIFOUT_CHSTSB 10'h132

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	channel B status[191:160]

Table 10-198 EE_AUDIO_SPDIFOUT_GAIN2 10'h134

Bits	R/W	Default	Description
31:24	R/W	0xFF	gain_ch11
23:16	R/W	0xFF	gain_ch10

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Bits	R/W	Default	Description
15:8	R/W	0xFF	gain_ch9
7:0	R/W	0xFF	gain_ch8

Table 10-199 EE_AUDIO_SPDIFOUT_GAIN3 10'h135

Bits	R/W	Default	Description
31:24	R/W	0xFF	gain_ch15
23:16	R/W	0xFF	gain_ch14
15:8	R/W	0xFF	gain_ch13
7:0	R/W	0xFF	gain_ch12

Table 10-200 EE_AUDIO_SPDIFOUT_GAIN_EN 10'h136

Bits	R/W	Default	Description
31:16	R/W	0x0000-0000	
15	R/W	0x0000-0000	ch15 gain_en; 1: out = in * gain_ch15; 0: out = in;
14	R/W	0x0000-0000	ch14 gain_en; 1: out = in * gain_ch14; 0: out = in;
13	R/W	0x0000-0000	ch13 gain_en; 1: out = in * gain_ch13; 0: out = in;
12	R/W	0x0000-0000	ch12 gain_en; 1: out = in * gain_ch12; 0: out = in;
11	R/W	0x0000-0000	ch11 gain_en; 1: out = in * gain_ch11; 0: out = in;
10	R/W	0x0000-0000	ch10 gain_en; 1: out = in * gain_ch10; 0: out = in;
9	R/W	0x0000-0000	ch9 gain_en; 1: out = in * gain_ch9; 0: out = in;
8	R/W	0x0000-0000	ch8 gain_en; 1: out = in * gain_ch8; 0: out = in;
7	R/W	0x0000-0000	ch7 gain_en; 1: out = in * gain_ch7; 0: out = in;
6	R/W	0x0000-0000	ch6 gain_en; 1: out = in * gain_ch6; 0: out = in;
5	R/W	0x0000-0000	ch5 gain_en; 1: out = in * gain_ch5; 0: out = in;
4	R/W	0x0000-0000	ch4 gain_en; 1: out = in * gain_ch4; 0: out = in;
3	R/W	0x0000-0000	ch3 gain_en; 1: out = in * gain_ch3; 0: out = in;
2	R/W	0x0000-0000	ch2 gain_en; 1: out = in * gain_ch2; 0: out = in;

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Bits	R/W	Default	Description
1	R/W	0x0000-0000	ch1 gain_en; 1: out = in * gain_ch1; 0: out = in;
0	R/W	0x0000-0000	ch0 gain_en; 1: out = in * gain_ch0; 0: out = in;

Table 10-201 EE_AUDIO_SPDIFOUT_GAIN_CTRL 10'h137

Bits	R/W	Default	Description
31	R/W	0x0000-0000	reg_gain_step_chg; 0: the current_gain will follow direct to reg_gain change; 1: the current_gain will follow step by step to reg_gain change; etc: change reg_gain from 40 to 50, and gain_step = 3; the currenct_gain will change as: 40->43->46->49->50;
25:24	R/W		reg_cur_gain_sel; 0: cur_gain_sts = ch3,ch2,ch1,ch0; 1: cur_gain_sts = ch7,ch6,ch5,ch4; 2: cur_gain_sts = ch11,ch10,ch9,ch8; 3: cur_gain_sts = ch15,ch14,ch13,ch12;
23:16	R/W		reg_gain_step; modified gain value each time;
15:0	R/W		reg_gain_updt_timer; the period of each change, unit is FS;

EE_AUDIO_SPDIFOUT_B_STAT 10'h1a0
EE_AUDIO_SPDIFOUT_B _GAIN0 10'h1a1
EE_AUDIO_SPDIFOUT_B _GAIN1 10'h1a2
EE_AUDIO_SPDIFOUT_B _CTRL0 10'h1a3
EE_AUDIO_SPDIFOUT_B _CTRL1 10'h1a4
EE_AUDIO_SPDIFOUT_B _PREAMB 10'h1a5
EE_AUDIO_SPDIFOUT_B _SWAP 10'h1a6
EE_AUDIO_SPDIFOUT_B _CHSTS0 10'h1a7
EE_AUDIO_SPDIFOUT_B _CHSTS1 10'h1a8
EE_AUDIO_SPDIFOUT_B _CHSTS2 10'h1a9
EE_AUDIO_SPDIFOUT_B _CHSTS3 10'h1aa
EE_AUDIO_SPDIFOUT_B _CHSTS4 10'h1ab
EE_AUDIO_SPDIFOUT_B _CHSTS5 10'h1ac
EE_AUDIO_SPDIFOUT_B _CHSTS6 10'h1ad
EE_AUDIO_SPDIFOUT_B _CHSTS7 10'h1ae
EE_AUDIO_SPDIFOUT_B _CHSTS8 10'h1af
EE_AUDIO_SPDIFOUT_B _CHSTS9 10'h1b0
EE_AUDIO_SPDIFOUT_B _CHSTSA 10'h1b1
EE_AUDIO_SPDIFOUT_B _CHSTSB 10'h1b2

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EE_AUDIO_SPDIFOUT_B _MUTE_VAL 10'h1b3

EE_AUDIO_SPDIFOUT_GAIN2 10'h1b4

EE_AUDIO_SPDIFOUT_GAIN3 10'h1b5

EE_AUDIO_SPDIFOUT_GAIN_EN 10'h1b6

EE_AUDIO_SPDIFOUT_GAIN_CTRL 10'h1b7

Table 10-202 EE_AUDIO_SPDIFIN_ LB_CTRL0 10'h1f0

Bits	R/W	Default	Description
31	R/W	0x0000-0000	reg_work_enable, 0: disable; 1:enable;
30	R/W		reg_chnum_sel, 0: ch_num = 0~383(include frame cnt); 1: ch_num = 0~1(only L/R);
29	R/W		reg_rst_afifo_out_n, reset afifo out side;
28	R/W		reg_rst_afifo_in_n, reset afifo in side; need set 1 after set reg_rst_afifo_out_n to 1;
26	R/W		reg_chunm_en; 1: start add ch_cnt to ch_num;
25	R/W		reg_findpapb_en, 0: disable NonPCM mode; 1: enable;
24	R/W		reg_clk_inv; 0: sample spdif by posedge; 1: sample spdif by negedge;
23:12	R/W		reg_nonpcm2pcm_th, when detected NonPcm mode;if long time (z_cnt >= th) didn't detect PaPb again, will generate interrupt to SW: now changed to PCM mode;
11:8	R/W		reg_ch_status_sel, For EE_AUDIO_SPDIFIN_STAT1
7	R/W		reg_mute_l, 0: disable ; 1: mute channel L;
6	R/W		reg_mute_r, 0: disable ; 1: mute channel R;
5:4	R/W		reg_spdifin_src_sel, 0: PAD of spdifin;1: spdifout;
3	R/W		reg_check_valid, 0: disable valid check ; 1: enable;
2	R/W		reg_check_parity, 0: disable parity check ; 1: enable;
1	R/W		reg_invert_data, 0: disalbe; 1: invert [27:4] to [4:27];
0	R/W		reg_spdifin_phase, 0: disable invert; 1: enable;

Table 10-203 EE_AUDIO_SPDIFIN_ LB_CTRL1 10'h1f1

Bits	R/W	Default	Description
27:20	R/W		reg_interrupt_mask, mask each interrupt;

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Table 10-204 EE_AUDIO_SPDIFIN_ LB_CTRL6 10'h1f6

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	Reg_clr_internal_sts[7:0]; 7: clear valid bit status; 6: clear parity bit status; 5: clear ch status; 4: clear z_cnt status; 3: clear find_nonpcm status; 2: clear pd_data status; 1: clear pc_data status; 0: clear find_papb status;
23:16	R/W		Reg_clr_interrupt[7:0] for each bit of irq_status[7:0];
13	R/W		reg_irq_mode; 1: level mode; 0: pulse mode;
8	R/W		reg_papb_ext_sync, 1: add ext "0" sync check for papb; 0: disable;
7:0	R/W		reg_papb_ext_mask, mask 8 channel "0" sync

Table 10-205 EE_AUDIO_SPDIFIN_ LB_STAT0 10'h1f7

Bits	R/W	Default	Description
31	R/W	0x0000-0000	Valid bit
11:8	R/W		afifo_cnt[3:0]
7:0	R/W		r_interrupt_status, interrupt status, need clear by reg_clk_interrupt; [7]: find PaPb; [6]: valid changed; [5]: find nonpcm to pcm (reg_nonpcm2pcm_th) ; [4]: find Pc or Pd changed; [3]: find CH status changed; [1]: find parity error; [0]: find overflow;

Table 10-206 EE_AUDIO_SPDIFIN_ LB_STAT1 10'h1f8

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	channel status, by reg_ch_status_sel; reg_ch_status_sel[3]: 0: channel A; 1: channel B; reg_ch_status_sel[2:0]: 0: ch_status[31:0]; 1: ch_status[63:32]; 2: ch_status[95:64]; 3: ch_status[127:96]; 4: ch_status[159:128]; 5: ch_status[191:160]; 6: pc[15:0],pd[15:0];

Table 10-207 EE_AUDIO_SPDIFIN_ LB_MUTE_VAL 10'h1fa

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	reg_spdifin_mute_val, when muted, the channel value

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10.10.9 Resample Registers

Each register final address = module base address+ address * 4

Table 10-208 AUDIO_RSAMP_CTRL0 0x000

Bits	R/W	Default	Description
2	R/W	0	reg_lock_rst, phase_lock module software reset
1	R/W	0	reg_rsamp_rst, resample_core module software reset
0	R/W	0	reg_sw_rst, resample_top module softwire reset

Table 10-209 AUDIO_RSAMP_CTRL1 0x001

Bits	R/W	Default	Description
25	R/W	0	reg_rsamp_rst_sel 1:resample_core use hardware as reset 0:resample_core use software reg_rsamp_rst as reset
24	R/W	0	reg_module_bypas 1: bypass resamp_top, input source direct output 0: resamp_top work
23:18	R/W	0	reg_gclk_ctrl, clk gate
17:13	R/W	23	reg_in_msb
12	R/W	0	reg_output_en,is used for source switch
11	R/W	0	reg_rsamp_en : It is used to enable the resample module. 1=enable, 0 = disable
10	R/W	0	reg_filt_en :It is used to enable the AA filter to downsample the input data. 1=enable, 0 = disable
9	R/W	0	reg_post_en : It is used to enable the compensation filter. 1= enable , 0= disable
8	R/W	0	reg_inp_mux_mode
3:0	R/W	0	reg_inp_mux

Table 10-210 AUDIO_RSAMP_CTRL2 0x002

Bits	R/W	Default	Description
29:24	R/W	2	reg_chx_size : It is used to set the channel number.
17:16	R/W	0	reg_scl_step 0: 1/1 1: 1/2 2: 1/4
15:8	R/W	63	reg_filt_tap : It is used to set the taps of the AA filter.
7:0	R/W	63	reg_intp_tap : It is used to set the tap of the interpolation filter.

Table 10-211 AUDIO_RSAMP_PHSINIT 0x003

Bits	R/W	Default	Description
27:0	R/W	0	reg_init_phs : It is used to set the initial phase for accumulator.

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Table 10-212 AUDIO_RSAMP_PHSSTEP 0x004

Bits	R/W	Default	Description
30:0	R/W	0x8000000	reg_rsamp_step: It is used to set the step size for accumulator. It can be calculated by: Fs_in/down_ratio/fs_out*2^28, where fs_in is the frequency of input data,fs_out is the frequency of output data,down_ratio is the down sample ratio.

Table 10-213 AUDIO_RSAMP_SHIFT 0x005

Bits	R/W	Default	Description
31:24	R/W	23	reg_rsft_iir : It is used to set the shift bit for compensation IIR filter.
23:16	R/W	21	reg_rsft_blnd :It is used to set the shift bit for blending.
15:8	R/W	31	reg_rsft_sinc : It is used to set the shift bit for interpolation filter.
7:0	R/W	31	reg_rsft_aa □It is used to set the shift bit for anti-alias filter.

Table 10-214 AUDIO_RSAMP_ADJ_CTRL0 0x006

Bits	R/W	Default	Description
2	R/W	0	reg_rsamp_adj_out_inv : It is used to set the direction for adjusting.
1	R/W	0	reg_rsamp_adj_force_en : It is used to enable forcing a adjustment value for accumulator step. 1= enable,0=disable
0	R/W	0	reg_rsamp_adj_en : It is used to enable the auto adjusting module.1= enable, 0=disable

Table 10-215 AUDIO_RSAMP_ADJ_CTRL1 0x007

Bits	R/W	Default	Description
31:16	R/W	8	reg_rsamp_adj_odet_step
15:0	R/W	32768	reg_rsamp_adj_kmax : It is used to set the maximum value after loop filter.

Table 10-216 AUDIO_RSAMP_ADJ_SFT 0x008

Bits	R/W	Default	Description
29	R/W	0	reg_rsamp_adj_dif_sel : It is used to select the input data for adjustment module.
28:24	R/W	9	reg_rsamp_adj_ki : It is used to set the ki of loop filter.
20:16	R/W	1	reg_rsamp_adj_kp : It is used to set the kp of loop filter
12:8	R/W	6	reg_rsamp_adj_ki_sft : It is used to set the shift value after ki multiplier.
5:0	R/W	12	reg_rsamp_adj_out_sft : It is used to set the adjustment output shift value.

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Table 10-217 AUDIO_RSAMP_ADJ_IDET_LEN 0x009

Bits	R/W	Default	Description
31:0	R/W	10000	reg_rsamp_adj_idet_len : It is used to set the detection length for adjustment.

Table 10-218 AUDIO_RSAMP_ADJ_FORCE 0x00a

Bits	R/W	Default	Description
31:0	R/W	8	reg_rsamp_adj_force_err: It is used to set the forcing err.

Table 10-219 AUDIO_RSAMP_ADJ_KI_FORCE 0x00b

Bits	R/W	Default	Description
31:0	R/W	0	reg_rsamp_adj_ki_force : It is used to set a forcing value for ki adjustment.

Table 10-220 AUDIO_RSAMP_RO_STATUS 0x010

Bits	R/W	Default	Description
31:0	R.O	0x0	ro_rsamp_stat : din_chx_chk_err, is_idle_st, rsamp_fifo_over_cnt[7:0]} : It is used report the working state for resample.

Table 10-221 AUDIO_RSAMP_RO_ADJ_FREQ 0x011

Bits	R/W	Default	Description
31:0	R.O	0x0	ro_rsamp_adj_freq : It is used to report the the adjustment frequency.

Table 10-222 AUDIO_RSAMP_RO_ADJ_DIFF_BAK 0x012

Bits	R/W	Default	Description
31:0	R.O	0x0	ro_det_diff_bak : It is used to report the difference for comparator.

Table 10-223 AUDIO_RSAMP_RO_ADJ_DIFF_DLT 0x013

Bits	R/W	Default	Description
31:0	R.O	0x0	ro_det_diff_dlt : It is used to report the difference delta.

Table 10-224 AUDIO_RSAMP_RO_ADJ_PHS_ERR 0x014

Bits	R/W	Default	Description
31:0	R.O	0x0	ro_det_phase_err : It is used to report the detection phase error.

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Table 10-225 AUDIO_RSAMP_RO_ADJ_KI_OUT 0x015

Bits	R/W	Default	Description
31:0	R.O	0x0	ro_rsamp_ki_out : It is used to report the out of integration branch.

Table 10-226 AUDIO_RSAMP_RO_IN_CNT 0x016

Bits	R/W	Default	Description
31:0	R.O	0x0	ro_rsamp_in_cnt : It is used to report the counter of input data .

Table 10-227 AUDIO_RSAMP_RO_OUT_CNT 0x017

Bits	R/W	Default	Description
31:0	R.O	0x0	ro_rsamp_out_cnt : It is used to report the counter of output data.

Table 10-228 AUDIO_RSAMP_POST_COEF0 0x020

Bits	R/W	Default	Description
31:0	R/W	0	reg_post_coef0 : It is used to set the coefficient of compensation filter.

Table 10-229 AUDIO_RSAMP_POST_COEF1 0x021

Bits	R/W	Default	Description
31:0	R/W	0	reg_post_coef1 : It is used to set the coefficient of compensation filter.

Table 10-230 AUDIO_RSAMP_POST_COEF2 0x022

Bits	R/W	Default	Description
31:0	R/W	0	reg_post_coef2 : It is used to set the coefficient of compensation filter.

Table 10-231 AUDIO_RSAMP_POST_COEF3 0x023

Bits	R/W	Default	Description
31:0	R/W	0	reg_post_coef3 : It is used to set the coefficient of compensation filter.

Table 10-232 AUDIO_RSAMP_POST_COEF4 0x024

Bits	R/W	Default	Description
31:0	R/W	0	reg_post_coef4 : It is used to set the coefficient of compensation filter.

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Table 10-233 AUDIO_RSAMP_AA_COEF_ADDR 0x030

Bits	R/W	Default	Description
31:0	R/W	0	reg_aa_coef_addr

Table 10-234 AUDIO_RSAMP_AA_COEF_DATA 0x031

Bits	R/W	Default	Description
31:0	R/W	0	reg_aa_coef_data

Table 10-235 AUDIO_RSAMP_SINC_COEF_ADDR 0x040

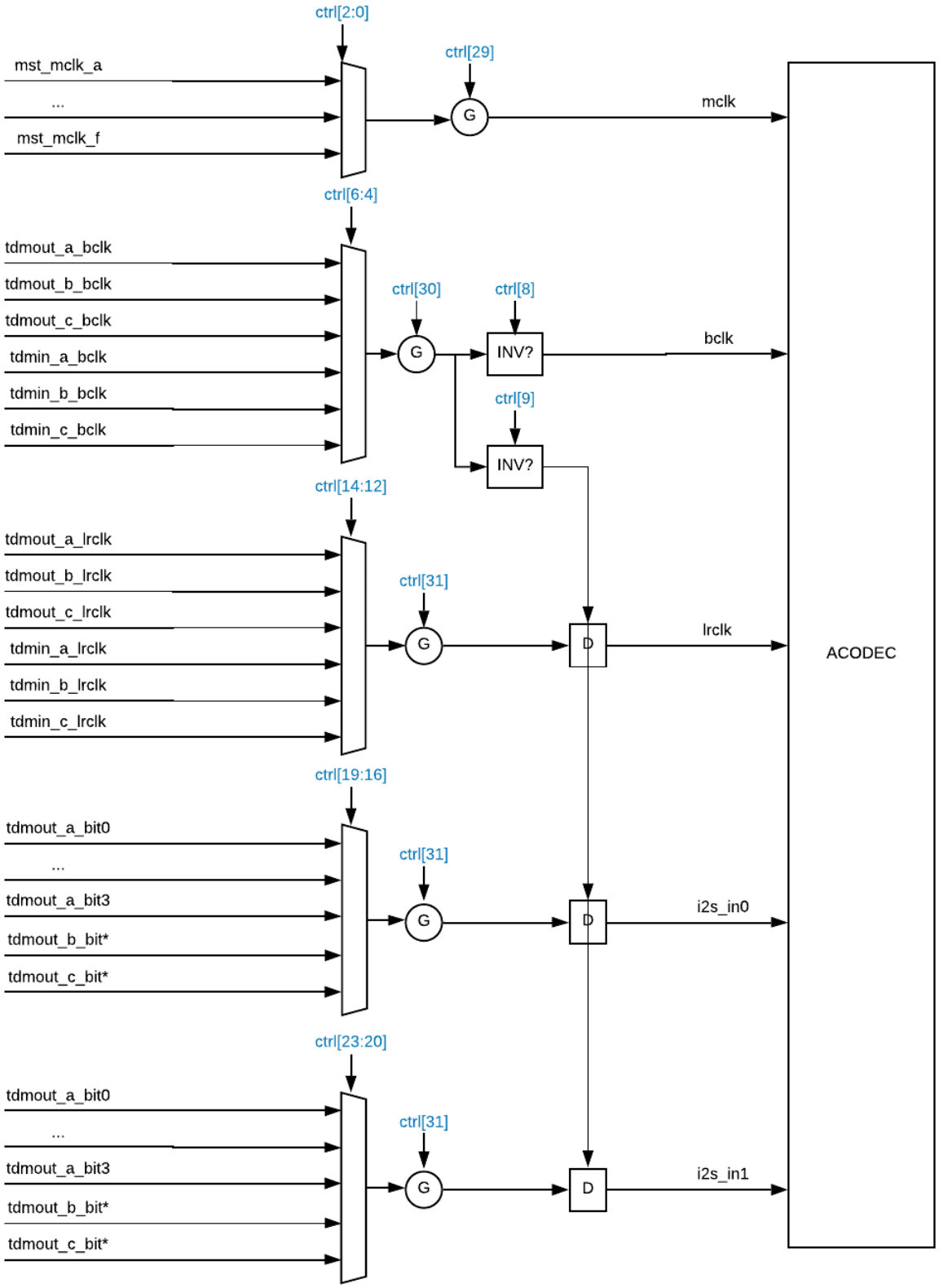
Bits	R/W	Default	Description
31:0	R/W	0	reg_sinc_coef_addr

Table 10-236 AUDIO_RSAMP_SINC_COEF_DATA 0x041

Bits	R/W	Default	Description
31:0	R/W	0	reg_sinc_coef_data

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10.10.10 TOACODEC Registers



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Table 10-237 EE_AUDIO_TOACODEC_CTRL0 10'h1d0

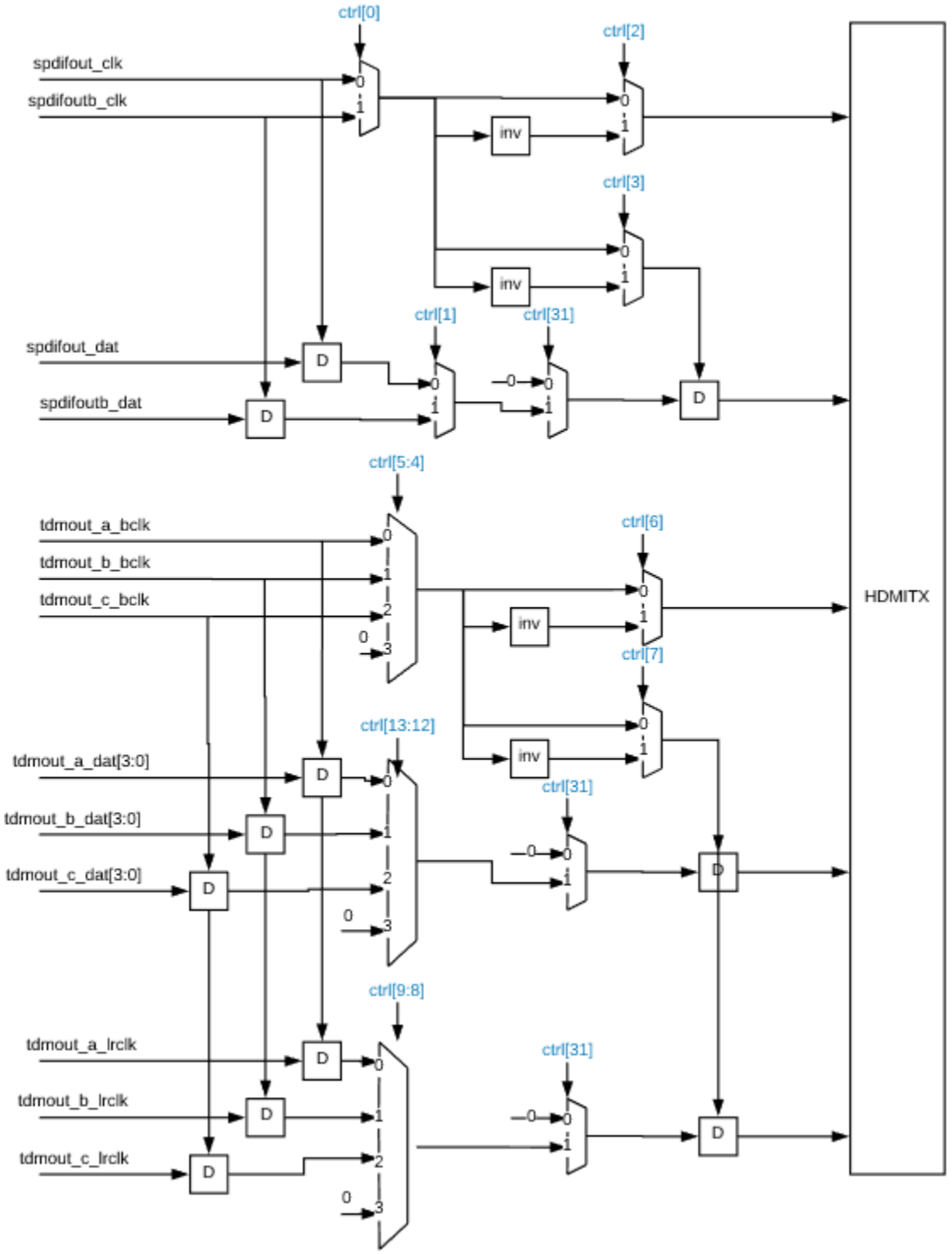
Bits	R/W	Default	Description
31	R/W	0x0000-0000	reg_toacodec_en_dat, 0: disable; 1: enable; step1: enable/disable mclk step2: enable/disable bclk step3: enable/disable dat
30	R/W		reg_toacodec_en_bclk, 0: disable; 1: enable;
29	R/W		reg_toacodec_en_mclk, 0: disable; 1: enable;
26:22	R/W		Dat1_sel: 0: tdmout_a_dat[0]; 1: tdmout_a_dat[1]; 2: tdmout_a_dat[2]; 3: tdmout_a_dat[3]; 4: tdmout_a_dat[4]; 5: tdmout_a_dat[5]; 6: tdmout_a_dat[6]; 7: tdmout_a_dat[7]; 8: tdmout_b_dat[0]; 9: tdmout_b_dat[1]; 10: tdmout_b_dat[2]; 11: tdmout_b_dat[3]; 12: tdmout_b_dat[4]; 13: tdmout_b_dat[5]; 14: tdmout_b_dat[6]; 15: tdmout_b_dat[7]; 16: tdmout_c_dat[0]; 17: tdmout_c_dat[1]; 18: tdmout_c_dat[2]; 19: tdmout_c_dat[3]; 20: tdmout_c_dat[4]; 21: tdmout_c_dat[5]; 22: tdmout_c_dat[6]; 23: tdmout_c_dat[7];
20:16	R/W		Dat0_sel: 0: tdmout_a_dat[0]; 1: tdmout_a_dat[1]; 2: tdmout_a_dat[2]; 3: tdmout_a_dat[3]; 4: tdmout_a_dat[4]; 5: tdmout_a_dat[5]; 6: tdmout_a_dat[6]; 7: tdmout_a_dat[7]; 8: tdmout_b_dat[0]; 9: tdmout_b_dat[1]; 10: tdmout_b_dat[2]; 11: tdmout_b_dat[3]; 12: tdmout_b_dat[4]; 13: tdmout_b_dat[5]; 14: tdmout_b_dat[6]; 15: tdmout_b_dat[7]; 16: tdmout_c_dat[0]; 17: tdmout_c_dat[1]; 18: tdmout_c_dat[2]; 19: tdmout_c_dat[3]; 20: tdmout_c_dat[4]; 21: tdmout_c_dat[5]; 22: tdmout_c_dat[6]; 23: tdmout_c_dat[7];
14:12	R/W		lrclk_sel: 0: tdmout_a_lrclk; 1: tdmout_b_lrclk; 2: tdmout_c_lrclk; 4: tdmin_a_lrclk; 5: tdmin_b_lrclk;

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Bits	R/W	Default	Description
			6: tdmin_c_lrclk;
10	R/W		Lrclk_inv; 1: invert lrclk;
9	R/W		Bclk_cap_inv: The dat_o and lrclk_o will captured for timing balance after select; If this bit set to 1, will use invert bclk to capture;
8	R/W		Bclk_o_inv: if set 1, the final bclk connect to acodec will invert;
6:4	R/W		Bclk_sel: 0: tdmout_a_bclk; 1: tdmout_b_bclk; 2: tdmout_c_bclk; 4: tdmin_a_bclk; 5: tdmin_b_bclk; 6: tdmin_c_bclk;
2:0	R/W		Mclk_sel: 0:mst_mclk_a; 1:mst_mclk_b; 2:mst_mclk_c; 3:mst_mclk_d; 4:mst_mclk_e; 5:mst_mclk_f;

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10.10.11 TOHDMITX Registers



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Table 10-238 EE_AUDIO_TOHDMITX_CTRL0 10'h1d1

Bits	R/W	Default	Description
31	R/W	0x0000-0000	reg_tohdmitx_spdif_en_dat, 0: disable; 1: enable; step1: enable/disable clk; step2: enable/disable dat;
30	R/W		reg_tohdmitx_spdif_en_clk, 0: disable; 1: enable;
29	R/W		reg_tohdmitx_i2s_en_dat, 0: disable; 1: enable; step1: enable/disable clk; step2: enable/disable dat;
28	R/W		reg_tohdmitx_i2s_en_clk, 0: disable; 1: enable;
27:20	R/W		reg_tohdmitx_mclk_div, if need div8, set to 7
19	R/W		reg_tohdmitx_mclk_en;
18:16	R/W		reg_tohdmitx_mclk_sel: 0: mst_mclk_a; 1: mst_mclk_b; 2: mst_mclk_c; 3: mst_mclk_d; 4: mst_mclk_e; 5: mst_mclk_f;
13:12	R/W		dat_sel: 0: tdmout_a_dat; 1: tdmout_b_dat; 2: tdmout_c_dat;
10	R/W		Lrclk_inv;
9:8	R/W		lrclk_sel: 0: tdmout_a_lrclk; 1: tdmout_b_lrclk; 2: tdmout_c_lrclk;
7	R/W		Bclk_cap_inv: The dat_o and lrclk_o will captured for timing balance after select; If this bit set to 1, will use invert bclk to capture;
6	R/W		Bclk_o_inv: if set 1, the final bclk connect to acodec will invert;
5:4	R/W		Bclk_sel: 0: tdmout_a_bclk; 1: tdmout_b_bclk; 2: tdmout_c_bclk;
3	R/W		Spdif_clk_cap_inv: The spdif_dat will captured for timing balance after select; If this bit set to 1, will use invert spdif_clk to capture;
2	R/W		Spdif_clk_o_inv: if set 1, the final bclk connect to hdmitx will invert;
1	R/W		Spdif_sel: 0:spdif_out; 1:spdif_out_b;
0	R/W		Spdif_clk_sel: 0:spdif_clk; 1:spdif_clk_b;

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10.10.12 TOVAD Registers

Table 10-239 EE_AUDIO_TOVAD_CTRL0 10'h1d2

Bits	R/W	Default	Description
31	R/W	0x0000-0000	reg_tovad_en, 0: disable; 1: enable;
30	R/W		reg_tovad_v_sel, 0: level; 1:pulse;
16:12	R/W		ata Src select: 0: tdmin_a; 1: tdmin_b; 2: tdmin_c; 3: spdifin; 4: pdmin; 5: fratv; 6: tdmin_lb; 7: loopback_a; 8: frhdmirx_spdif; 9: loopback_b; 10: spdifin_lb; 11:earc_rx_dmac 12:frhdmirx_dsd 13:resample_a 14:resample_b 15: vad; 16~31:reserved

10.10.13 PDM Registers

Each register final address = module base address+ address * 4

Table 10-240 PDM_CTRL 8'h00

Bits	R/W	Default	Description
31	R/W	0x0000-0000	PDM enable
30	R/W		invert the PDM_DCLK
29	R/W		output mode: 1: 24bits. 0: 32 bits
28	R/W		bypass mode. 1: bypass all filter. directly output the PDM input to DDR. 0: normal mode.
27:20	R/W		pdm_mute_mask[7:0]; [7] mute pdm ch7; … [0] mute pdm ch0;
19	R/W		train_en; 1: check value of capture data;
18	R/W		train_clr; 1: clear training status;
17	R/W		chnum_sel. 0: valid_cnt; 1: mask_cnt;
16	R/W		PDM Asynchronous FIFO soft reset. write 1 to soft reset AFIFO
15:8	R/W		PDM channel reset. 0: to reset each PDM channel. 1: normal mode
7:0	R/W		PDM channel enable. each bit for one channel

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Table 10-241 PDM_HCIC_CTRL1 8'h01

Bits	R/W	Default	Description
31	R/W	0x0000-0000	hcic filter enable. 1 use sinc filter. 0 bypass input to output
29:24	R/W		hcic final gain shift parameter
23:16	R/W		hcic final gain multiplier
8:4	R/W		hcic down sample rate
3:0	R/W		hcic stage number. must be between 3 to 9

Table 10-242 PDM_F1_CTRL 8'h03

Bits	R/W	Default	Description
31	R/W	0x0000-0000	filter 1 enable
17:16	R/W		f1 round mode. 2'b00 : sign bit at bit 49. 28bits output [49:22] round at bit 21. 32bits output [49:18]. 24bits output [49:26] 2'b01 : sign bit at bit 50. 28bits output [50:23] round at bit 22. 32bits output [49:18]. 24bits output [49:26] 2'b10 : sign bit at bit 51. 28bits output [51:24] round at bit 23 32bits output [49:18]. 24bits output [49:26].
15:12	R/W		filter 1 down sample rate
8:0	R/W		filter 1 stage number

Table 10-243 PDM_F2_CTRL 8'h04

Bits	R/W	Default	Description
31	R/W	0x0000-0000	filter 2 enable
17:16	R/W		F2 round mode. 2'b00: round at bit 21. 2'b01: round at bit 22.2'b10: round at bit 23
15:12	R/W		filter 2 down sample rate
8:0	R/W		filter 2 stage number

Table 10-244 PDM_F3_CTRL 8'h05

Bits	R/W	Default	Description
31	R/W	0x0000-0000	filter 3 enable
17:16	R/W		F3 round mode. 2'b00 : round at bit 21. 2'b01 : round at bit 22.2'b10 : round at bit 23
15:12	R/W		filter 3 down sample rate
8:0	R/W		filter 3 stage number

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Table 10-245 PDM_HPF_CTRL 8'h06

Bits	R/W	Default	Description
31	R/W	0x0000-0000	High pass filter enable
20:16	R/W		high pass filter shift steps. 6~19 steps
15:0	R/W		high pass filter output factor

Table 10-246 PDM_CHAN_CTRL 8'h07

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	Chan3 data sample pointer vs edge of the PDM_DCLK
23:16	R/W		Chan2 data sample pointer vs edge of the PDM_DCLK
15:8	R/W		Chan1 data sample pointer vs edge of the PDM_DCLK
7:0	R/W		Chan0 data sample pointer vs edge of the PDM_DCLK

Table 10-247 PDM_CHAN_CTRL1 8'h08

Bits	R/W	Default	Description
31:24	R/W	0x0000-0000	Chan7 data sample pointer vs edge of the PDM_DCLK
23:16	R/W		Chan6 data sample pointer vs edge of the PDM_DCLK
15:8	R/W		Chan5 data sample pointer vs edge of the PDM_DCLK
7:0	R/W		Chan4 data sample pointer vs edge of the PDM_DCLK

Table 10-248 PDM_COEFF_ADDR 8'h09

Bits	R/W	Default	Description
8:0	R/W	0x0000-0000	address of the write/read of coeff data

Table 10-249 PDM_COEFF_DATA 8'h0A

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	write/read data to coeff memory

Table 10-250 PDM_CLKG_CTRL 8'h0B

Bits	R/W	Default	Description
6	R/W	0x0000-0000	filt_ctrl module auto clock gating control
5	R/W		sinc fifo module auto clock gating control
4	R/W		filter module auto clock gating control

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Bits	R/W	Default	Description
3	R/W		apb module auto clock gating control
2	R/W		coeff memory module auto clock gating control
1	R/W		each channel module auto clock gating control
0	R/W		cts_pdm_clk auto clock gating control

Table 10-251 PDM_STS 8'h0C

Bits	R/W	Default	Description
15:12	R	0x0000-0000	afifo count value
11:4	R		train result of 8 ch; 1: diff; 0: same;
1	R/W	0x0000-0000	HPF filter output overflow. means the PCLK is too slow
0	R/W		HCIC filter output overflow. means the CTS_PDM_CLK is too slow. can't finished the filter function.

Table 10-252 PDM_MUTE_VALUE 8'h0D

Bits	R/W	Default	Description
31:0	R/W	0x0000-0000	mute value if mute_mask = 1;

Table 10-253 PDM_MASK_NUM 8'h0E

Bits	R/W	Default	Description
15:0	R/W	0x0000-0000	When PDM power on, there are some invalid data because filter initialize. So set this register can mask these invalid data. If PDM out frequency is 48K, set MASK_NUM = 49 will mask 50/48k = 1.04ms.

Table 10-254 PDM_CHAN_CTRL2 8'h0F

Bits	R/W	Default	Description
7:0	R/W	0x0000-0000	start fiter pointer vs rise edge of the PDM_DCLK need avoid close to data sample pointer which defined by PDM_CHAN_CTRL0/1

10.10.14 LOCKER Registers

Each register final address = module base address+ address * 4

Table 10-255 AUD_LOCK_EN 0X00

Bit(s)	R/W	Default	Description
31:1			reserved
0	R/W	0x0	Audio_lock_en: 0 = disable; 1= enable.

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Table 10-256 AUD_LOCK_SW_RESET 0X01

Bit(s)	R/W	Default	Description
31:1			reserved
0	R/W	0x0	Audio_lock_soft_reset: 1=generate soft reset pulse

Table 10-257 AUD_LOCK_SW_LATCH 0X02

Bit(s)	R/W	Default	Description
31:4			reserved
3	R/W	0x0	omclk2ref software latch: 1= generate the latch pulse
2	R/W	0x0	Ref2omclk software latch: 1= generate the latch pulse
1	R/W	0x0	Ref2imclk software latch: 1= generate the latch pulse
0	R/W	0x0	Imclk2ref software latch: 1= generate the latch pulse

Table 10-258 AUD_LOCK_HW_LATCH 0X03

Bit(s)	R/W	Default	Description
31:4			reserved
3	R/W	0x0	omclk2ref hardware latch enble: 1= enable□0= disable
2	R/W	0x0	Ref2omclk hardware latch enble: 1= enable□0= disable
1	R/W	0x0	Ref2imclk hardware latch enble: 1= enable□0= disable
0	R/W	0x0	Imclk2ref hardware latch enble: 1= enable□0= disable

Table 10-259 AUD_LOCK_REFCLK_SRC 0X04

Bit(s)	R/W	Default	Description
31:2			reserved
1:0	R/W	0x0	Ref clk source sel: 0= pclk; 1=oscinclk; 2,3,reserved

Table 10-260 AUD_LOCK_REFCLK_LAT_INT 0X05

Bit(s)	R/W	Default	Description
31:0			U32 number of reference clock cycles to latch the imclk and omclk

Table 10-261 AUD_LOCK_IMCLK_LAT_INT 0X06

Bit(s)	R/W	Default	Description
31:0			U32 number of imclk clock cycles to latch the reference clock

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Table 10-262 AUD_LOCK_OMCLK_LAT_INT 0X07

Bit(s)	R/W	Default	Description
31:0			U32 number of omclk clock cycles to latch the reference clock

Table 10-263 AUD_LOCK_REFCLK_DS_INT 0X08

Bit(s)	R/W	Default	Description
31:10			reserved
9:0	R/W	0x0	U10 downsample step of reference clock for the couter48ds to be measured, module = x+1

Table 10-264 AUD_LOCK_IMCLK_DS_INT 0X09

Bit(s)	R/W	Default	Description
31:10			reserved
9:0	R/W	0x0	U10 downsample step of imclk for the couter48ds to be measured, module = x+1

Table 10-265 AUD_LOCK_OMCLK_DS_INT 0X0a

Bit(s)	R/W	Default	Description
31:10			reserved
9:0	R/W	0x0	U10 downsample step of omclk for the couter48ds to be measured, module = x +1

Table 10-266 AUD_LOCK_INT_CLR 0X0b

Bit(s)	R/W	Default	Description
31:2			reserved
1	R/W	0x0	It is used to generate pulse to clear the interrupt status
0	R/W	0x0	It is used to generate pulse to clear the interrupt

Table 10-267 AUD_LOCK_GCLK_CTRL 0X0c

Bit(s)	R/W	Default	Description
31:4			reserved
3:2	R/W	0x0	It is used to gate the module clock
1	R/W	0x0	It is used to gate the register clock
0			reserved

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Table 10-268 AUD_LOCK_INT_CTRL 0X0d

Bit(s)	R/W	Default	Description
31:4			reserved
3	R/W	0x0	It is used to mask interrupt for omclk_state
2	R/W	0x0	It is used to mask interrupt for imclk_state
1	R/W	0x0	It is used to mask interrupt for refclk_state1
0	R/W	0x0	It is used to mask interrupt for refclk_state0

Table 10-269 RO_REF2IMCLK_CNT_L 0X10

Bit(s)	R/W	Default	Description
31:0	R	0x0	U48 latched imclk counter48ds of each reg_refclk_latch_interval; Will start from 0 reaching 2^48

Table 10-270 RO_REF2IMCLK_CNT_H 0X11

Bit(s)	R/W	Default	Description
31:16			reserved
15:0	R	0x0	U48 latched imclk counter48ds of each reg_refclk_latch_interval; Will start from 0 reaching 2^48

Table 10-271 RO_REF2OMCLK_CNT_L 0X12

Bit(s)	R/W	Default	Description
31:0	R	0x0	U48 latched omclk counter48ds of each reg_refclk_latch_interval; Will start from 0 reaching 2^48

Table 10-272 RO_REF2OMCLK_CNT_H 0X13

Bit(s)	R/W	Default	Description
31:16			reserved
15:0	R	0x0	U48 latched omclk counter48ds of each reg_refclk_latch_interval; Will start from 0 reaching 2^48

Table 10-273 RO_IMCLK2REF_CNT_L 0X14

Bit(s)	R/W	Default	Description
31:0	R	0x0	U48 latched reference clock counter48ds of each reg_imclk_latch_interval; Will start from 0 reaching 2^48

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Table 10-274 RO_IMCLK2REF_CNT_H 0X15

Bit(s)	R/W	Default	Description
31:16			reserved
15:0	R	0x0	U48 latched reference clock counter48ds of each reg_imclk_latch_interval; Will start from 0 reaching 2^48

Table 10-275 RO_OMCLK2REF_CNT_L 0X16

Bit(s)	R/W	Default	Description
31:0	R	0x0	U48 latched reference clock counter48ds of each reg_omclk_latch_interval; Will start from 0 reaching 2^48

Table 10-276 RO_OMCLK2REF_CNT_H 0X17

Bit(s)	R/W	Default	Description
31:16			reserved
15:0	R	0x0	U48 latched reference clock counter48ds of each reg_omclk_latch_interval; Will start from 0 reaching 2^48

Table 10-277 RO_REFCLK_PKG_CNT 0X18

Bit(s)	R/W	Default	Description
31:16	R	0x0	U16,number of reference clk latch interval period conter for imclk latch
15:0	R	0x0	U16,number of reference clk latch interval period conter for imclk latch

Table 10-278 RO_IMCLK_PKG_CNT 0X19

Bit(s)	R/W	Default	Description
31:16			reserved
15:0	R	0x0	U16,number of imclk latch interval period counter

Table 10-279 RO_OMCLK_PKG_CNT 0X1a

Bit(s)	R/W	Default	Description
31:16			reserved
15:0	R	0x0	U16,number of omclk latch interval period counter

Table 10-280 RO_AUD_LOCK_INT_STATUS 0X1b

Bit(s)	R/W	Default	Description
31:4			reserved
3	R	0x0	It is used to report interrupt status for omclk_state
2	R	0x0	It is used to report interrupt status for imclk_state

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Bit(s)	R/W	Default	Description
1	R	0x0	It is used to report interrupt status for refclk_state1
0	R	0x0	It is used to report interrupt status for refclk_state0

10.10.15 VAD Registers

Each register final address = module base address+ address * 4

Table 10-281 EE_VAD_TOP_CTRL0 8'h0

Bits	R/W	Default	Description
31	R/W	0	vad_en
30	R/W	0	dec_fir_en
29	R/W	0	pre_emp_en
28	R/W	0	pre_ram_en
27	R/W	0	frame_his_en
26	R/W	0	frame_his_save_en
23	R/W	0	ceps_ceps_en
22	R/W	0	ceps_spec_en
21	R/W	0	post_dec_en
20	R/W	0	two_channel_en
10	R/W	0	soft_rst
9	R/W	0	dec_fir_soft_rst
8	R/W	0	pre_emp_soft_rst
7	R/W	0	proc_soft_rst
6	R/W	0	frame_his_soft_rst
5	R/W	0	frame_his_save_soft_rst
4	R/W	0	ceps_win_soft_rst
3	R/W	0	ceps_fft_soft_rst
2	R/W	0	ceps_ceps_soft_rst
1	R/W	0	ceps_spec_soft_rst
0	R/W	0	post_dec_soft_rst

Table 10-282 EE_VAD_TOP_CTRL1 8'h1

Bits	R/W	Default	Description
31:30	R/W	0	vad_clk_gate
29:28	R/W	0	prepare_clk_gate
27:26	R/W	0	proc_clk_gate

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Bits	R/W	Default	Description
25:24	R/W	0	frame_his_clk_gate
23:22	R/W	0	ceps_ceps_clk_gate
21:20	R/W	0	ceps_spec_clk_gate
19:18	R/W	0	ch_sel1_clk_gate
17:16	R/W	0	ch_sel0_clk_gate
7	R/W	0	vad_sw_reset
6	R/W	0	prepare_sw_reset
5	R/W	0	proc_sw_reset
4	R/W	0	frame_his_sw_reset
3	R/W	0	ceps_win_sw_reset
2	R/W	0	ceps_ceps_sw_reset
1	R/W	0	ceps_spec_sw_reset
0	R/W	0	post_dec_sw_reset

Table 10-283 EE_VAD_TOP_CTRL2 8'h2

Bits	R/W	Default	Description
25:24	R/W	0	ch1_shift: 0:0, 1:1, 2:2, 3:3
9:8	R/W	0	ch0_shift: 0:0, 1:1, 2:2, 3:3

Table 10-284 VAD_FIR_CTRL 8'h3

Bits	R/W	Default	Description
29:24	R/W	0	dec_filter_order
15:8	R/W	0	dec_filter_depthm1; >= filter pipe + order
3:0	R/W	0	dec_rate;decimation_rate-1(0~11)

Table 10-285 VAD_FIR_EMP 8'h4

Bits	R/W	Default	Description
9:0	R/W	0	pre_emp_coef :float unsigned

Table 10-286 VAD_FIR_COEF 0 8'h5

Bits	R/W	Default	Description
31:16	R/W	0	dec_coef_0 : 8.1.1.7
15:0	R/W	0	dec_coef_1 : 8.1.1.7

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Table 10-287 VAD_FIR_COEF 1 8'h6

Bits	R/W	Default	Description
31:16	R/W	0	dec_coef_2 : 8.1.1.7
15:0	R/W	0	dec_coef_3 : 8.1.1.7

Table 10-288 VAD_FIR_COEF 2 8'h7

Bits	R/W	Default	Description
31:16	R/W	0	dec_coef_4 : 8.1.1.7
15:0	R/W	0	dec_coef_5 : 8.1.1.7

Table 10-289 VAD_FIR_COEF 3 8'h8

Bits	R/W	Default	Description
31:16	R/W	0	dec_coef_6 : 8.1.1.7
15:0	R/W	0	dec_coef_7 : 8.1.1.7

Table 10-290 VAD_FIR_COEF 4 8'h9

Bits	R/W	Default	Description
31:16	R/W	0	dec_coef_8 : 8.1.1.7
15:0	R/W	0	dec_coef_9 : 8.1.1.7

Table 10-291 VAD_FIR_COEF 5 8'ha

Bits	R/W	Default	Description
31:16	R/W	0	dec_coef_10 : 8.1.1.7
15:0	R/W	0	dec_coef_11 : 8.1.1.7

Table 10-292 VAD_FIR_COEF 6 8'hb

Bits	R/W	Default	Description
31:16	R/W	0	dec_coef_12 : 8.1.1.7
15:0	R/W	0	dec_coef_13 : 8.1.1.7

Table 10-293 VAD_FIR_COEF 7 8'hc

Bits	R/W	Default	Description
31:16	R/W	0	dec_coef_14 : 8.1.1.7
15:0	R/W	0	dec_coef_15 : 8.1.1.7

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Table 10-294 VAD_FIR_COEF 8 8'hd

Bits	R/W	Default	Description
31:16	R/W	0	dec_coef_16 : 8.1.1.7
15:0	R/W	0	dec_coef_17 : 8.1.1.7

Table 10-295 VAD_FIR_COEF 9 8'he

Bits	R/W	Default	Description
31:16	R/W	0	dec_coef_18 : 8.1.1.7
15:0	R/W	0	dec_coef_19 : 8.1.1.7

Table 10-296 VAD_FIR_COEF 10 8'hf

Bits	R/W	Default	Description
31:16	R/W	0	dec_coef_20 : 8.1.1.7
15:0	R/W	0	dec_coef_21 : 8.1.1.7

Table 10-297 VAD_FIR_COEF 11 8'h10

Bits	R/W	Default	Description
31:16	R/W	0	dec_coef_22 : 8.1.1.7
15:0	R/W	0	dec_coef_23 : 8.1.1.7

Table 10-298 VAD_FIR_COEF 12 8'h11

Bits	R/W	Default	Description
31:16	R/W	0	dec_coef_24 : 8.1.1.7

Table 10-299 VAD_FRAME_CTRL0 8'h12

Bits	R/W	Default	Description
31:30	R/W	0	frame_len 0: 64, 1: 128, 2: 256
26:24	R/W	0	pow_diff_dist:0:4, 1:8, 3:16, 5:24
17:16	R/W	0	pow_old_avglen:0:4, 1:8,3:16

Table 10-300 VAD_FRAME_CTRL1 8'h13

Bits	R/W	Default	Description
11:0	R/W	0	pow_rampup_thr: 8.16.0.13, threshold for power ramp up detect

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Table 10-301 VAD_FRAME_CTRL2 8'h14

Bits	R/W	Default	Description
31:16	R/W	0	pow_cur_thr: 10.0.0.52
15:0	R/W	0	pow_cur_thr_high: 10.0.0.52

Table 10-302 VAD_CEP_CTRL0 8'h15

Bits	R/W	Default	Description
29:28	R/W	0	ceps_decision_sel: 0 : ||, 1: &&, 2:naxm 3:maxmin
25:24	R/W	0	decision_sel_each:0 : ||, 1: &&, 2:spectral_entropy 3:ceps
20:16	R/W	0	login_min: 2^(-logn_min),5.5.0, [0~20]
10:0	R/W	0	ceps_log_blk: 11.6.1

Table 10-303 VAD_CEP_CTRL1 8'h16

Bits	R/W	Default	Description
8:0	R/W	0	ceps_weight_step: 9,-3,0

Table 10-304 VAD_CEP_CTRL2 8'h17

Bits	R/W	Default	Description
31:16	R/W	0	ceps_max_thr: 16.9.1
15:0	R/W	0	ceps_maxmin_thr :16.9.1

Table 10-305 VAD_CEP_CTRL3 8'h18

Bits	R/W	Default	Description
31:24	R/W	0	ceps_det_start: [0~128]
23:16	R/W	0	ceps_det_end: [0~128], end>start
14:8	R/W	0	ceps_freq_blk_low: 0: no blk, 1blk[0], 2 blank [255 0 1]…
6:0	R/W	0	ceps_freq_blk_high: 0:no blk,1:blk[128],2 blk[127:129]…

Table 10-306 VAD_CEP_CTRL4 8'h19

Bits	R/W	Default	Description
30:24	R/W	0	spectral_entropy_start: [0~127]
22:16	R/W	0	spectral_entropy_end: [0~127]

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Table 10-307 VAD_CEP_CTRL5 8'h1a

Bits	R/W	Default	Description
27:16	R/W	0	spectral_entropy_thr_max: 12.7.1
11:0	R/W	0	spectral_entropy_thr_min: 12.7.1

Table 10-308 VAD_DEC_CTRL 8'h1b

Bits	R/W	Default	Description
29:28	R/W	0	decision_sel_combine: 0 is &, 1is |,2 is +
20:16	R/W	0	vadflag_confirm_m: <32
5:0	R/W	0	vadflag_confirm_n

Table 10-309 VAD_TOP_STS0 8'h1c

Bits	R/W	Default	Description
4	R	0	Afifo_err
3:0	R	0	lafifo_cnt

Table 10-310 VAD_TOP_STS1 8'h1d

Bits	R/W	Default	Description
20	R	0	Pre_overflow
19	R	0	Pre_fst
18	R	0	Pre_val
17:0	R	0	Pre_dat

Table 10-311 VAD_TOP_STS2 8'h1e

Bits	R/W	Default	Description
18	R	0	Ceps_val
17:0	R	0	Ceps_dat

Table 10-312 VAD_FIR_STS0 8'h1f

Bits	R/W	Default	Description
31:0	R	0	reserved

Table 10-313 VAD_FIR_STS1 8'h20

Bits	R/W	Default	Description
31:-	R	0	reserved

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Table 10-314 VAD_POW_STS0 8'h21

Bits	R/W	Default	Description
31:16	R	0	reserved
15:0	R	0	Pow_o

Table 10-315 VAD_POW_STS1 8'h22

Bits	R/W	Default	Description
31:0	R	0	reserved

Table 10-316 VAD_POW_STS2 8'h23

Bits	R/W	Default	Description
31:0	R	0	reserved

Table 10-317 VAD_FFT_STS0 8'h24

Bits	R/W	Default	Description
31	R	0	Ceps_done_latch
30	R	0	Spec_entropy_done
29	R	0	Cepstrum_done

Table 10-318 VAD_FFT_STS1 8'h25

Bits	R/W	Default	Description
11:0	R	0	Se_o

Table 10-319 VAD_SPE_STS0 8'h26

Bits	R/W	Default	Description
31:16	R	0	Cepsw_o_h
15:0	R	0	Cepsw_o_l

Table 10-320 VAD_SPE_STS1 8'h27

Bits	R/W	Default	Description
31:16	R	0	Cur_pow

Table 10-321 VAD_SPE_STS2 8'h28

Bits	R/W	Default	Description
31:0	R	0	Calc_q_pre

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Table 10-322 VAD_SPE_STS3 8'h29

Bits	R/W	Default	Description
31:0	R	0	Reserved

Table 10-323 VAD_DEC_STS0 8'h2a

Bits	R/W	Default	Description
31:0	R	0	Reserved

Table 10-324 VAD_DEC_STS1 8'h2b

Bits	R/W	Default	Description
31:0	R	0	Reserved

Table 10-325 VAD_LUT_CTRL 8'h2c

Bits	R/W	Default	Description
31	R/W	0	win_lut_w
30	R/W	0	win_lut_r
6:0	R/W	0	win_lut_addr

Table 10-326 VAD_LUT_WR 8'h2d

Bits	R/W	Default	Description
31:0	R/W	0	Win_lut_wr:12.0.0.7

Table 10-327 VAD_LUT_RD 8'h2e

Bits	R/W	Default	Description
31:0	R	0	Win_lut_rd:12.0.0.7

Table 10-328 VAD_IN_SEL0 8'h2f

Bits	R/W	Default	Description
31:0	R/W	0	ch0_sel: reg_vad.gen_vadin_coeff, bit[n] for ch_n enable

Table 10-329 VAD_IN_SEL1 8'h30

Bits	R/W	Default	Description
31:0	R/W	0	Ch1_sel: reg_vad.gen_vadin_coeff, bit[n] for ch_n enable

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Table 10-330 VAD_TO_DDR 8'h31

Bits	R/W	Default	Description
31	R/W	0	vad_to_ddr_en
30	R/W	0	vad_to_ddr_rst
29	R/W	0	vad_to_ddr_eo
27:16	R/W	0	vad_to_ddr_cur_cnt
11:0	R/W	0	vad_to_ddr_max_cnt

10.10.16 EQDRC Registers

Each register final address = module base address+ address * 4

Table 10-331 EE_AED_COEF_RAM_CNTL 10'h0

Bits	R/W	Default	Description
31-10	R/W	0x0	reserved;
9-2	R/W	0x0	addr: read or write the addr of coef ram
1	R/W	0x0	rd/wr: 0 read from coef ram; 1 write to coef ram
0	R/W	0x0	valid: 0 the command had been finish; 1 the command wait to be done

Table 10-332 EE_AED_COEF_RAM_DATA 10'h1

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	data: read from coef ram or write to coef ram

Table 10-333 EE_AED_EQ_EN 10'h2

Bits	R/W	Default	Description
31-2	R/W	0x0	reserved;
1	R/W	0x0	eq2_en: It is used to enable EQ for ch3 and ch4. 1= enable, 0 = bypass.
0	R/W	0x0	eq1_en: It is used to enable EQ for ch1 and ch2. 1= enable, 0 = bypass.

Table 10-334 EE_AED_TAP_CNTL 10'h3

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
9-5	R/W	0xa	eq2_tap: It is used to set the tap for EQ2.
4-0	R/W	0xa	eq1_tap: It is used to set the tap for EQ1.

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Table 10-335 EE_AED_EQ_VOLUME 10'h4

Bits	R/W	Default	Description
31-30	R/W	0x0	volume_step: It is used to set volume adjust step.
29-26	R/W	0x0	reserved;
25-16	R/W	0x0	volume_master: It is used to set master volume.
15-8	R/W	0x0	volume_ch2: It is used to set channel2 volume.
7-0	R/W	0x0	volume_ch1: It is used to set channel1 volume.

Table 10-336 EE_AED_EQ_VOLUME_SLEW_CNT 10'h5

Bits	R/W	Default	Description
31-12	R/W	0x0	reserved;
11-0	R/W	0x0	volume_slew_cnt: It is used to control volume change and mute ramp rate.

Table 10-337 EE_AED_MUTE 10'h6

Bits	R/W	Default	Description
31	R/W	0x0	mute_master: It is used to mute all.
30-2	R/W	0x0	reserved;
1	R/W	0x0	mute_ch2: It is used to mute channel1.
0	R/W	0x0	mute_ch1: It is used to mute channel1.

Table 10-338 EE_AED_DRC_CNTL 10'h7

Bits	R/W	Default	Description
31-6	R/W	0x0	reserved;
5-3	R/W	0x0	drc_tap: It is used to set the power tap for DRC.
2	R/W	0x0	drc_pow_sel: It is used to select the input of gain alpha filter. 0 = dB domain, 1 = decimal domain
1	R/W	0x0	drc_rms_mode: It is used to select the mode of pow calculation. 0 = RMS, 1= peaking
0	R/W	0x0	drc_en: It is used to enable the post DRC. 1= enable, 0 = bypass.

Table 10-339 EE_AED_DRC_RMS_COEF0 10'h8

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for power calculation filter.

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Table 10-340 EE_AED_DRC_RMS_COEF1 10'h9

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for power calculation filter.

Table 10-341 EE_AED_DRC_THD0 10'h0a

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power threshold0 for DRC.

Table 10-342 EE_AED_DRC_THD1 10'h0b

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power threshold1 for DRC.

Table 10-343 EE_AED_DRC_THD2 10'h0c

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power threshold2 for DRC.

Table 10-344 EE_AED_DRC_THD3 10'h0d

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power threshold3 for DRC.

Table 10-345 EE_AED_DRC_THD4 10'h0e

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power threshold4 for DRC.

Table 10-346 EE_AED_DRC_K0 10'h0f

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the k-slope of gain for tap 0.

Table 10-347 EE_AED_DRC_K1 10'h10

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the k-slope of gain for tap 1.

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Table 10-348 EE_AED_DRC_K2 10'h11

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the k-slope of gain for tap 2.

Table 10-349 EE_AED_DRC_K3 10'h12

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the k-slope of gain for tap 3.

Table 10-350 EE_AED_DRC_K4 10'h13

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the k-slope of gain for tap 4.

Table 10-351 EE_AED_DRC_K5 10'h14

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the k-slope of gain for tap 5.

Table 10-352 EE_AED_DRC_THD_OUT0 10'h15

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power threshold_out0 for DRC.

Table 10-353 EE_AED_DRC_THD_OUT1 10'h16

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power threshold_out1 for DRC.

Table 10-354 EE_AED_DRC_THD_OUT2 10'h17

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power threshold_out2 for DRC.

Table 10-355 EE_AED_DRC_THD_OUT3 10'h18

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power threshold_out3 for DRC.

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Table 10-356 EE_AED_DRC_OFFSET 10'h19

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power offset of DRC.

Table 10-357 EE_AED_DRC_RELEASE_COEF00 10'h1a

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-358 EE_AED_DRC_RELEASE_COEF01 10'h1b

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-359 EE_AED_DRC_RELEASE_COEF10 10'h1c

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-360 EE_AED_DRC_RELEASE_COEF11 10'h1d

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-361 EE_AED_DRC_RELEASE_COEF20 10'h1e

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-362 EE_AED_DRC_RELEASE_COEF21 10'h1f

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

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Table 10-363 EE_AED_DRC_RELEASE_COEF30 10'h20

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-364 EE_AED_DRC_RELEASE_COEF31 10'h21

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-365 EE_AED_DRC_RELEASE_COEF40 10'h22

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-366 EE_AED_DRC_RELEASE_COEF41 10'h23

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-367 EE_AED_DRC_RELEASE_COEF50 10'h24

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-368 EE_AED_DRC_RELEASE_COEF51 10'h25

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-369 EE_AED_DRC_ATTACK_COEF00 10'h26

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

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Table 10-370 EE_AED_DRC_ATTACK_COEF01 10'h27

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

Table 10-371 EE_AED_DRC_ATTACK_COEF10 10'h28

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

Table 10-372 EE_AED_DRC_ATTACK_COEF11 10'h29

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

Table 10-373 EE_AED_DRC_ATTACK_COEF20 10'h2a

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

Table 10-374 EE_AED_DRC_ATTACK_COEF21 10'h2b

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

Table 10-375 EE_AED_DRC_ATTACK_COEF30 10'h2c

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

Table 10-376 EE_AED_DRC_ATTACK_COEF31 10'h2d

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

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Table 10-377 EE_AED_DRC_ATTACK_COEF40 10'h2e

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

Table 10-378 EE_AED_DRC_ATTACK_COEF41 10'h2f

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

Table 10-379 EE_AED_DRC_ATTACK_COEF50 10'h30

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

Table 10-380 EE_AED_DRC_ATTACK_COEF51 10'h31

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

Table 10-381 EE_AED_DRC_LOOPBACK_CNTL 10'h32

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
17	R/W	0x0	dis_fifo_rst: 0 if drc_loopback_cnt change, then reset fifo; 1 don`t reset
16	R/W	0x0	drc_loopback_bypass: It is used to set bypass look-ahead mode. 1= bypass.
15-9	R/W	0x0	reserved;
8-0	R/W	0x0	drc_loopback_cnt: It is used to set the look-ahead count.

Table 10-382 EE_AED_MDRC_CNTL 10'h33

Bits	R/W	Default	Description
31-17	R/W	0x0	reserved;
16	R/W	0x0	mdrc_pow_sel: It is used to select the input of gain alpha filter. 0 = dB domain, 1 = decimal domain
15-9	R/W	0x0	reserved;
8	R/W	0x0	mdrc_all_en: It is used to enable the entire multi-band DRC. 1= enable, 0 = bypass.
7-6	R/W	0x0	reserved;

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Bits	R/W	Default	Description
5-3	R/W	0x0	[3] mdrc_rms_mode: It is used to select the band0 mode of pow calculation. 0 = RMS, 1= peaking It is used to select the band1 mode of pow calculation. 0 = RMS, 1= peaking It is used to select the band2 mode of pow calculation. 0 = RMS, 1= peaking
2-0	R/W	0x0	[0] mdrc_en: It is used to enable the band 0 of MDRC. 1= enable, 0 = bypass. It is used to enable the band 1 of MDRC. 1= enable, 0 = bypass. It is used to enable the band 2 of MDRC. 1= enable, 0 = bypass.

Table 10-383 EE_AED_MDRC_RMS_COEF00 10'h34

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for power calculation filter.

Table 10-384 EE_AED_MDRC_RMS_COEF01 10'h35

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for power calculation filter.

Table 10-385 EE_AED_MDRC_RELEASE_COEF00 10'h36

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-386 EE_AED_MDRC_RELEASE_COEF01 10'h37

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-387 EE_AED_MDRC_ATTACK_COEF00 10'h38

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

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Table 10-388 EE_AED_MDRC_ATTACK_COEF01 10'h39

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

Table 10-389 EE_AED_MDRC_THD0 10'h3a

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power threshold for DRC.

Table 10-390 EE_AED_MDRC_K0 10'h3b

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the k-slope of gain.

Table 10-391 EE_AED_MDRC_LOW_GAIN 10'h3c

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the gain for DRC band 0.

Table 10-392 EE_AED_MDRC_OFFSET0 10'h3d

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power offset of DRC.

Table 10-393 EE_AED_MDRC_RMS_COEF10 10'h3e

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for power calculation filter.

Table 10-394 EE_AED_MDRC_RMS_COEF11 10'h3f

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for power calculation filter.

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Table 10-395 EE_AED_MDRC_RELEASE_COEF10 10'h40

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-396 EE_AED_MDRC_RELEASE_COEF11 10'h41

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-397 EE_AED_MDRC_ATTACK_COEF10 10'h42

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

Table 10-398 EE_AED_MDRC_ATTACK_COEF11 10'h43

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

Table 10-399 EE_AED_MDRC_THD1 10'h44

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power threshold for DRC.

Table 10-400 EE_AED_MDRC_K1 10'h45

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the k-slope of gain.

Table 10-401 EE_AED_MDRC_OFFSET1 10'h46

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power offset of DRC.

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Table 10-402 EE_AED_MDRC_MID_GAIN 10'h47

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the gain for DRC band 1.

Table 10-403 EE_AED_MDRC_RMS_COEF20 10'h48

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for power calculation filter.

Table 10-404 EE_AED_MDRC_RMS_COEF21 10'h49

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for power calculation filter.

Table 10-405 EE_AED_MDRC_RELEASE_COEF20 10'h4a

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-406 EE_AED_MDRC_RELEASE_COEF21 10'h4b

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain release filter.

Table 10-407 EE_AED_MDRC_ATTACK_COEF20 10'h4c

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

Table 10-408 EE_AED_MDRC_ATTACK_COEF21 10'h4d

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficient for gain attack filter.

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Table 10-409 EE_AED_MDRC_THD2 10'h4e

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power threshold for DRC.

Table 10-410 EE_AED_MDRC_K2 10'h4f

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the k-slope of gain.

Table 10-411 EE_AED_MDRC_OFFSET2 10'h50

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the power offset of DRC.

Table 10-412 EE_AED_MDRC_HIGH_GAIN 10'h51

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the gain for DRC band 1.

Table 10-413 EE_AED_ED_CNTL 10'h52

Bits	R/W	Default	Description
31-2	R/W	0x0	reserved;
1	R/W	0x0	ed_sign:
0	R/W	0x0	ed_int: soft reset

Table 10-414 EE_AED_DC_EN 10'h53

Bits	R/W	Default	Description
31-1	R/W	0x0	reserved;
0	R/W	0x0	It is used to enable the noise detection. 1= enable, 0 = bypass.

Table 10-415 EE_AED_ND_LOW_THD 10'h54

Bits	R/W	Default	Description
31-24	R/W	0x0	reserved;
23-0	R/W	0x0	It is used to set the low threshold for detection.

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Table 10-416 EE_AED_ND_HIGH_THD 10'h55

Bits	R/W	Default	Description
31-24	R/W	0x0	reserved;
23-0	R/W	0x0	It is used to set the high threshold for detection. If the signal amplitude is bigger than it, the signal is not noise.

Table 10-417 EE_AED_ND_CNT_THD 10'h56

Bits	R/W	Default	Description
31-16	R/W	0x0	reserved;
15-0	R/W	0x0	It is used to set the counter threshold for amplitude detection. If the counter for which the signal is smaller than reg_nd_low_thd continuously is bigger than it, the signal is noise.

Table 10-418 EE_AED_ND_SUM_NUM 10'h57

Bits	R/W	Default	Description
31-16	R/W	0x0	reserved;
15-0	R/W	0x0	It is used to set the statistical number for sum of signal amplitude.

Table 10-419 EE_AED_ND_CZ_SUM 10'h58

Bits	R/W	Default	Description
31-16	R/W	0x0	reserved;
15-0	R/W	0x0	It is used to set the statistical number for zero-crossing.

Table 10-420 EE_AED_ND_SUM_THD0 10'h59

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the low threshold for sum of amplitude.

Table 10-421 EE_AED_ND_SUM_THD1 10'h5a

Bits	R/W	Default	Description
31-0	R/W	0x0	It is used to set the high threshold for sum of amplitude.

Table 10-422 EE_AED_ND_CZ_THD0 10'h5b

Bits	R/W	Default	Description
31-16	R/W	0x0	reserved;
15-0	R/W	0x0	It is used to set the low threshold for zero-crossing number.

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Table 10-423 EE_AED_ND_CZ_THD1 10'h5c

Bits	R/W	Default	Description
31-16	R/W	0x0	reserved;
15-0	R/W	0x0	It is used to set the high threshold for zero-crossing number.

Table 10-424 EE_AED_ND_COND_CNTL 10'h5d

Bits	R/W	Default	Description
31-6	R/W	0x0	reserved;
5	R/W	0x0	Reg_nd_audio_cond2_en: It is used to enable the audio detection for amplitude.
4	R/W	0x0	Reg_nd_audio_cond1_en: It is used to enable the audio detection for amplitude.
3	R/W	0x0	Reg_nd_audio_cond0_en: It is used to enable the audio detection for amplitude.
2	R/W	0x0	Reg_nd_noise_cond2_en: It is used to enable the noise detection for amplitude.
1	R/W	0x0	Reg_nd_noise_cond1_en: It is used to enable the noise detection for amplitude.
0	R/W	0x0	Reg_nd_noise_cond0_en: It is used to enable the noise detection for amplitude.

Table 10-425 EE_AED_ND_RELEASE_COEF0 10'h5e

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficients for release filter when gain adjusting.

Table 10-426 EE_AED_ND_RELEASE_COEF1 10'h5f

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficients for release filter when gain adjusting.

Table 10-427 EE_AED_ND_ATTACK_COEF0 10'h60

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficients for attack filter when gain adjusting.

Table 10-428 EE_AED_ND_ATTACK_COEF1 10'h61

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the coefficients for attack filter when gain adjusting.

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Table 10-429 EE_AED_ND_CNTL 10'h62

Bits	R/W	Default	Description
31-3	R/W	0x0	reserved;
2-1	R/W	0x0	nd_gain_sel: It is used to set the gain when noise is detected. 0 = 1/2 1 = 1/4 2 = 1/8 3 = 0
0	R/W	0x0	It is used to enable the dc cut module. 1= enable, 0 = bypass.

Table 10-430 EE_AED_MIX0_LL 10'h63

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the ch1 gain to ch1 mixer.

Table 10-431 EE_AED_MIX0_RL 10'h64

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the ch2 gain to ch1 mixer.

Table 10-432 EE_AED_MIX0_LR 10'h65

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the ch1 gain to ch2 mixer.

Table 10-433 EE_AED_MIX0_RR 10'h66

Bits	R/W	Default	Description
31-26	R/W	0x0	reserved;
25-0	R/W	0x0	It is used to set the ch2 gain to ch2 mixer.

Table 10-434 EE_AED_CLIP_THD 10'h67

Bits	R/W	Default	Description
31-23	R/W	0x0	reserved;
22-0	R/W	0x0	It is used to set the clipping threshold.

Table 10-435 EE_AED_CH1_ND_SUM_OUT 10'h68

Bits	R/W	Default	Description
31-0	R	0x0	It is used to report the sum of amplitude of ch1.

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Table 10-436 EE_AED_CH2_ND_SUM_OUT 10'h69

Bits	R/W	Default	Description
31-0	R	0x0	It is used to report the sum of amplitude of ch2.

Table 10-437 EE_AED_CH1_ND_CZ_OUT 10'h6a

Bits	R/W	Default	Description
31-16	R	0x0	reserved;
15-0	R	0x0	It is used to report the sum of zero-crossing of ch1.

Table 10-438 EE_AED_CH2_ND_CZ_OUT 10'h6b

Bits	R/W	Default	Description
31-16	R	0x0	reserved;
15-0	R	0x0	It is used to report the sum of zero-crossing of ch2.

Table 10-439 EE_AED_NOISE_STATUS 10'h6c

Bits	R/W	Default	Description
31-7	R	0x0	reserved;
6	R	0x0	It is used to report the noise flag.
5-3	R	0x0	It is used to report the audio state.
2-0	R	0x0	It is used to report the noise state.

Table 10-440 EE_AED_POW_CURRENT_S0 10'h6d

Bits	R/W	Default	Description
-	R	0x0	reserved;
31-0	R	0x0	It is used to report the mdrc0 current power.

Table 10-441 EE_AED_POW_CURRENT_S1 10'h6e

Bits	R/W	Default	Description
-	R	0x0	reserved;
31-0	R	0x0	It is used to report the mdrc1 current power.

Table 10-442 EE_AED_POW_CURRENT_S2 10'h6f

Bits	R/W	Default	Description
-	R	0x0	reserved;
31-0	R	0x0	It is used to report the mdrc2 current power.

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Table 10-443 EE_AED_POW_OUT0 10'h70

Bits	R/W	Default	Description
-	R	0x0	reserved;
31-0	R	0x0	It is used to report the mdrc0 destination power.

Table 10-444 EE_AED_POW_OUT1 10'h71

Bits	R/W	Default	Description
-	R	0x0	reserved;
31-0	R	0x0	It is used to report the mdrc1 destination power.

Table 10-445 EE_AED_POW_OUT2 10'h72

Bits	R/W	Default	Description
-	R	0x0	reserved;
31-0	R	0x0	It is used to report the mdrc2 destination power.

Table 10-446 EE_AED_ADJ_INDEX0 10'h73

Bits	R/W	Default	Description
-	R	0x0	reserved;
31-0	R/W	0x0	It is used to report the mdrc0 adjusting power.

Table 10-447 EE_AED_ADJ_INDEX1 10'h74

Bits	R/W	Default	Description
-	R	0x0	reserved;
31-0	R	0x0	It is used to report the mdrc1 adjusting power.

Table 10-448 EE_AED_ADJ_INDEX2 10'h75

Bits	R/W	Default	Description
-	R	0x0	reserved;
31-0	R	0x0	It is used to report the mdrc2 adjusting power.

Table 10-449 EE_AED_DRC_GAIN_INDEX0 10'h76

Bits	R/W	Default	Description
31-26	R	0x0	reserved;
25-0	R	0x0	It is used to report mdrc0 the gain.

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Table 10-450 EE_AED_DRC_GAIN_INDEX1 10'h77

Bits	R/W	Default	Description
31-26	R	0x0	reserved;
25-0	R	0x0	It is used to report mdrc0 the gain.

Table 10-451 EE_AED_DRC_GAIN_INDEX2 10'h78

Bits	R/W	Default	Description
31-26	R	0x0	reserved;
25-0	R	0x0	It is used to report mdrc0 the gain.

Table 10-452 EE_AED_CH1_VOLUME_STATE 10'h79

Bits	R/W	Default	Description
31-11	R	0x0	reserved;
10-0	R	0x0	It is used to report the volume state of ch1.

Table 10-453 EE_AED_CH2_VOLUME_STATE 10'h7a

Bits	R/W	Default	Description
31-11	R	0x0	reserved;
10-0	R	0x0	It is used to report the volume state of ch2.

Table 10-454 EE_AED_CH1_VOLUME_GAIN 10'h7b

Bits	R/W	Default	Description
31-25	R	0x0	reserved;
25-0	R	0x0	It is used to report the volume gain of ch1.

Table 10-455 EE_AED_CH2_VOLUME_GAIN 10'h7c

Bits	R/W	Default	Description
31-25	R	0x0	reserved;
25-0	R	0x0	It is used to report the volume gain of ch2.

Table 10-456 EE_AED_FULL_POW_CURRENT 10'h7d

Bits	R/W	Default	Description
-	R	0x0	reserved;
31-0	R	0x0	It is used to report the current power.

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Table 10-457 EE_AED_FULL_POW_OUT 10'h7e

Bits	R/W	Default	Description
-	R	0x0	reserved;
31-0	R	0x0	It is used to report the destination power.

Table 10-458 EE_AED_FULL_POW_ADJ 10'h7f

Bits	R/W	Default	Description
-	R	0x0	reserved;
31-0	R	0x0	It is used to report the adjusting power.

Table 10-459 EE_AED_FULL_DRC_GAIN 10'h80

Bits	R/W	Default	Description
31-26	R	0x0	reserved;
25-0	R	0x0	It is used to report the gain.

Table 10-460 EE_AED_MASTER_VOLUME_STATE 10'h81

Bits	R/W	Default	Description
31-11	R	0x0	reserved;
10-0	R	0x0	It is used to report the volume state of master.

Table 10-461 EE_AED_MASTER_VOLUME_GAIN 10'h82

Bits	R/W	Default	Description
31-26	R	0x0	reserved;
25-0	R	0x0	It is used to report the volume gain of master.

Table 10-462 EE_AED_AED_TOP_CTL0 10'h83

Bits	R/W	Default	Description
31	R/W	0x0	reg_start_en:write 1 to start eqdrc function,will auto clear to 0
30	R/W	0x0	reserved;
29-26	R/W	0x0	reg_lane_eq_ch34: eqdrc channel 34 select,can only set one bit valid 0000: audio data to channel 34 will be zero 0001:audio data from lane0 0010:audio data from lane1 0100:audio data from lane2 1000:audio data from lane3
25-18	R/W	0x0	reg_channel_valid: audio channel valid for each bit
17-14	R/W	0x0	reg_lane_eq_ch12: eqdrc channel 12 select,can only set one bit valid 0000: audio data to channel 12 will be zero 0001:audio data from lane0 0010:audio data from lane1

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Bits	R/W	Default	Description
			0100:audio data from lane2 1000:audio data from lane3
13-11	R/W	0x0	reg_data_type:0: split 64bits ddr data to 8 sample, each sample need 8 bits; if bit-width < 8, left-justified; 1: split 64bits ddr data to 4 sample, each sample need 16 bits; if bitwidth < 16, left-justified ; 2: split 64bits ddr data to 4 sample, each sample need 16 bits; if bitwidth < 16, right-justified ; 3: split 64bits ddr data to 2 sample, each sample need 32 bits; if bitwidth < 32, left-justified; 4: split 64bits ddr data to 2 sample, each sample need 32 bits; if bitwidth < 32, right-justified;
10-6	R/W	0x0	reg_data_msb:msb position of data
5-4	R/W	0x0	reg_frddr_source: 0:frddr_A; 1:frddr_B; 2:frddr_C;
2	R/W	0x0	reg_afifo_in_rst: reset afifo in side;
1	R/W	0x0	reg_afifo_out_rst:reset afifo out side;
0	R/W	0x0	req_eqdrc_en:eqdrc module enable

Table 10-463 EE_AED_AED_TOP_CTL1 10'h84

Bits	R/W	Default	Description
23-20	R/W	0x0	reg_ch2_sel:channel 2 data source select
19-16	R/W	0x0	reg_ch1_sel:channel 1 data source select
5	R/W	0x0	reg_eq_ch2_en :channel 2 eq enable
4	R/W	0x0	reg_eq_ch1_en :channel 1 eq enable
3-0	R/W	0x0	reg_channel_valid: Valid channel number -1

Table 10-464 EE_AED_AED_TOP_CTL2 10'h85

Bits	R/W	Default	Description
31	R/W	0x0	reg_ini_done_rst,when enable will auto rst at init_done negedge
30-20	R/W	0x0	reserved;
19-12	R/W	0x0	reg_ack_num: if needn’t share buffer, set it as 0; if need share buffer , set it as TDMOUT/SPDIFOUT ch number;
11	R/W	0x0	reg_req_sel2_en
10-8	R/W	0x0	reg_req_sel2: 0: tdmout_a; 1: tdmout_b; 2: tdmout_c; 3: spdifout; 4: spdifout_b; 5: reserved; 6: reserved; 7: reserved;
7	R/W	0x0	reg_req_sel1_en
6-4	R/W	0x0	reg_req_sel1: 0: tdmout_a; 1: tdmout_b; 2: tdmout_c; 3: spdifout; 4: spdifout_b; 5: reserved; 6: reserved; 7: reserved;

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Bits	R/W	Default	Description
3	R/W	0x0	reg_req_sel0_en
2-0	R/W	0x0	req_req_sel0: 0: tdmout_a; 1: tdmout_b; 2: tdmout_c; 3: spdifout; 4: spdifout_b; 5: reserved; 6: reserved; 7: reserved;

Table 10-465 EE_AED_AED_TOP_ST 10'h86

Bits	R/W	Default	Description
29-20	RO	0x0	tofifo_dat_buf_valid_num
19-10	RO	0x0	frddr_dat_buf_valid_num
9	RO	0x0	r_frddr_init_done
8	RO	0x0	frddr_start
7-4	RO	0x0	afifo_in_cnt
3-0	RO	0x0	afifo_out_cnt

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11 AFIFO

11.1 Register Description

Base address: 0xffd05000

Table 11-1 AIU_AIFIFO_CTRL 0x00

Bit(s)	R/W	Default	Description
13	R/W	0	Aififo request to dcu status
12	R/W	0	Dcu select status
11:5	R/W	0	Aififo word counter number
4:0	R/W	0	How many bits left in the first pop register

Table 11-2 AIU_AIFIFO_STATUS 0x01

Bit(s)	R/W	Default	Description
4:0	R	0x0	How many Bits left in the first pop register

Table 11-3 AIU_AIFIFO_GBIT 0x02

Bit(s)	R/W	Default	Description
15:0	R	0x0	The gb data

Table 11-4 AIU_AIFIFO_CLB 0x03

Bit(s)	R/W	Default	Description
15:0	R	0x0	The gb data

Table 11-5 AIU_MEM_AIFIFO_START_PTR 0x04

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The start address from DDR

Table 11-6 AIU_MEM_AIFIFO_CURR_PTR 0x05

Bit(s)	R/W	Default	Description
31:0	R	0x0	The current address from DDR

Table 11-7 AIU_MEM_AIFIFO_END_PTR 0x06

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The end address from DDR

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Table 11-8 AIU_MEM_AIFIFO_BYTES_AVAIL 0x07

Bit(s)	R/W	Default	Description
15:11	R/W	0	Unused.
10	R/W	0	Set this bit to 1 to enable filling of the FIFO controlled by the buffer level control. If this bit is 0, then use bit[1] to control the enabling of filling
9	R/W	0	This bit is set when data can be popped
8	R/W	0	This bit will be high when we're fetching data from the DDR memory To reset this module, set cntl_enable = 0, and then wait for busy = 0. After that you can pulse cntl_init to start over
7	R/W	0	Just in case endian. last minute byte swap of the data out of the FIFO to getbit
6	R/W	0	Unused.
5:3	R/W	0	
2	R/W	0	Set to 1 to enable reading the DDR memory FIFO and filling the pipeline to get-bit Set cntl_empty_en = cntl_fill_en = 0 when pulsing cntl_init
1	R/W	0	Set to 1 to enable reading data from DDR memory
0	R/W	0	After setting the read pointers, sizes, channel masks and read masks, set this bit to 1 and then to 0 NOTE: You don't need to pulse cntl_init if only the start address is being changed

Table 11-9 AIU_MEM_AIFIFO_CONTROL 0x08

Bit(s)	R/W	Default	Description
15:11		0x0	Unused
10	RW	0x0	Use_level Set This bit to 1 to enable filling of the FIFO controlled by the buffer level control. If This bit is 0, then use Bit[1] to control the enabling of filling
9	RW	0x0	Data Ready. This bit is set when data can be popped
8	RW	0x0	Fill busy This bit will be high when we're fetching data from the DDR memory
7	RW	0x0	Cntl_endian_jic Just in case endian. Last minute byte swap of the data out of the FIFO to get bit
6	RW	0x0	Unused
5:3	RW	0x0	Endian
2	RW	0x0	Cntl_empty_en Set to 1 to enable reading the DDR memory FIFO and filling the pipeline to get-bit
1	RW	0x0	Cntl_fill_en Set to 1 to enable reading data from DDR memory
0	RW	0x0	Cntl_init

Table 11-10 AIU_MEM_AIFIFO_MAN_WP 0x09

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Manual write ptr.

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Table 11-11 AIU_MEM_AIFIFO_MAN_RP 0x0a

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Manual read ptr.

Table 11-12 AIU_MEM_AIFIFO_LEVEL 0x0b

Bit(s)	R/W	Default	Description
1	R/W	0	Set to 1 for manual write pointer mode
0	R/W	0	Set high then low after everything has been initialized

Table 11-13 AIU_MEM_AIFIFO_BUF_CNTL 0x0c

Bit(s)	R/W	Default	Description
1	RW	0x0	manual mode Set to 1 for manual write pointer mode
0	RW	0x0	Init Set high then low after everything has been initialized

Table 11-14 AIU_MEM_AIFIFO_BUF_WRAP_COUNT 0x0d

Bit(s)	R/W	Default	Description
29:24	R/W	0	A_brst_num
21:16	R/W	0	A_id
15:0	R/W	0	level_hold

Table 11-15 AIU_MEM_AIFIFO_MEM_CTL 0x0f

Bit(s)	R/W	Default	Description
31:16	R/W	0	drop_bytes
15:14	R/W	0	drop_status (Read-Only)
13:12	R/W	0	sync_match_position (Read-Only)
11:6	R/W	0	reserved
5:4	R/W	0	TIME_STAMP_NUMBER, 0-32bits, 1-64bits, 2-96bits, 3-128bits
3	R/W	0	stamp_soft_reset
2	R/W	0	TIME_STAMP_length_enable
1	R/W	0	TIME_STAMP_sync64_enable
0	R/W	0	TIME_STAMP_enable

Table 11-16 AIFIFO_TIME_STAMP_CNTL 0x10

Bit(s)	R/W	Default	Description
31:0	R/W	0	TIME_STAMP_SYNC_CODE_0

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Table 11-17 AIFIFO_TIME_STAMP_SYNC_0 0x11

Bit(s)	R/W	Default	Description
31:0	R/W	0	TIME_STAMP_SYNC_CODE_1

Table 11-18 AIFIFO_TIME_STAMP_SYNC_1 0x12

Bit(s)	R/W	Default	Description
31:0	R/W	0	TIME_STAMP_0

Table 11-19 AIFIFO_TIME_STAMP_0 0x13

Bit(s)	R/W	Default	Description
31:0	R/W	0	TIME_STAMP_1

Table 11-20 AIFIFO_TIME_STAMP_1 0x14

Bit(s)	R/W	Default	Description
31:0	R/W	0	TIME_STAMP_2

Table 11-21 AIFIFO_TIME_STAMP_2 0x15

Bit(s)	R/W	Default	Description
31:0	R/W	0	TIME_STAMP_3

Table 11-22 AIFIFO_TIME_STAMP_3 0x16

Bit(s)	R/W	Default	Description
31:0	R/W	0	TIME_STAMP_LENGTH

Table 11-23 AIFIFO_TIME_STAMP_LENGTH 0x17

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_LENGTH

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12 Memory Interface

This chapter describes the SoC's memory interfaces from the following aspects:

- DDR
- NAND
- EMMC/SDIO/SD
- SPICC
- SPIFC

12.1 DDR

12.1.1 Overview

DDR consists of the 2 parts: DDR memory controller (DMC) and AM-DDR PHY. The main features of this module are listed below:

- Support DDR3 SDRAM up to DDR3-2133.
- Support DDR4 SDRAM up to DDR4-2666.
- Support LPDDR4 SDRAM up to LPDDR4-2666.
- Support 32bits and 16bits data mode.
- Unbalanced 16bits DDR3/4 SDRAM size in 32 bits data bus mode.
- Each DDR command buffer contains 64bytes data.
- 32 write command buffer and 32 read command buffer for DDR command generation.
- READ command reordering regardless ID.
- Write command reordering regardless IDs.
- Write and read data coherence.
- Optimized DDR command reordering based on:
  - Priority
  - Rank
  - Bank
  - Bank group interleaving(DDR4)
  - Read/write
- 4 level priority control to reduce the latency for the urgent request.
- Unblocking urgent control through Asynchronous FIFO and pipelines.
- Per Port Per ID Security Control through the all security ranges.
- Up to 16 security range can be defined.
- Support up to 16 AXI3/4 and 8 AMBUS(Amlogic) interfaces.
- Optimized AMBUS to support 0~3 burst to improve DDR efficiency and reduce.

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Figure 12-1 DDR Interface

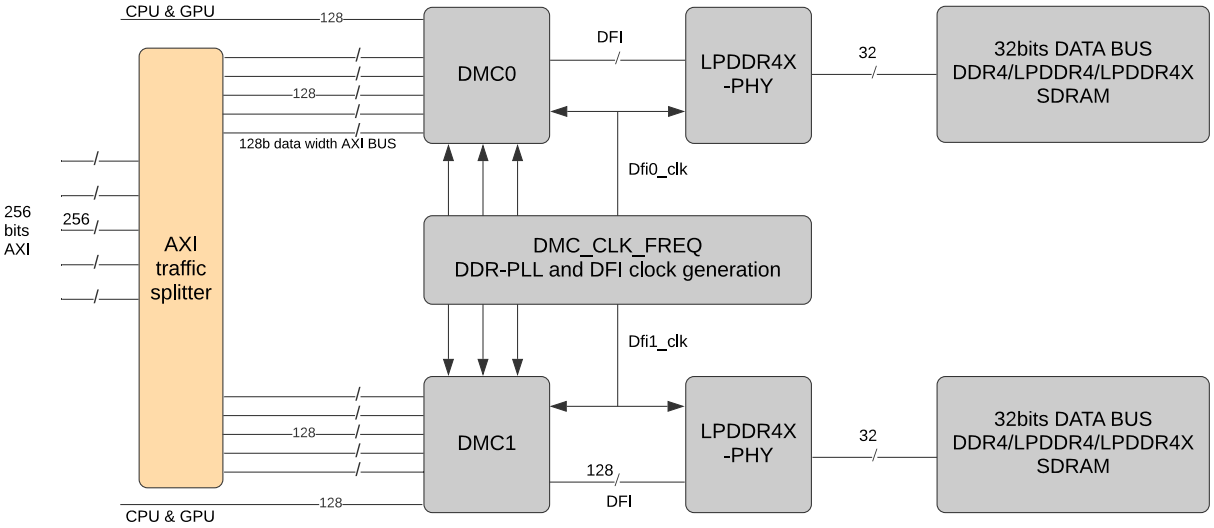
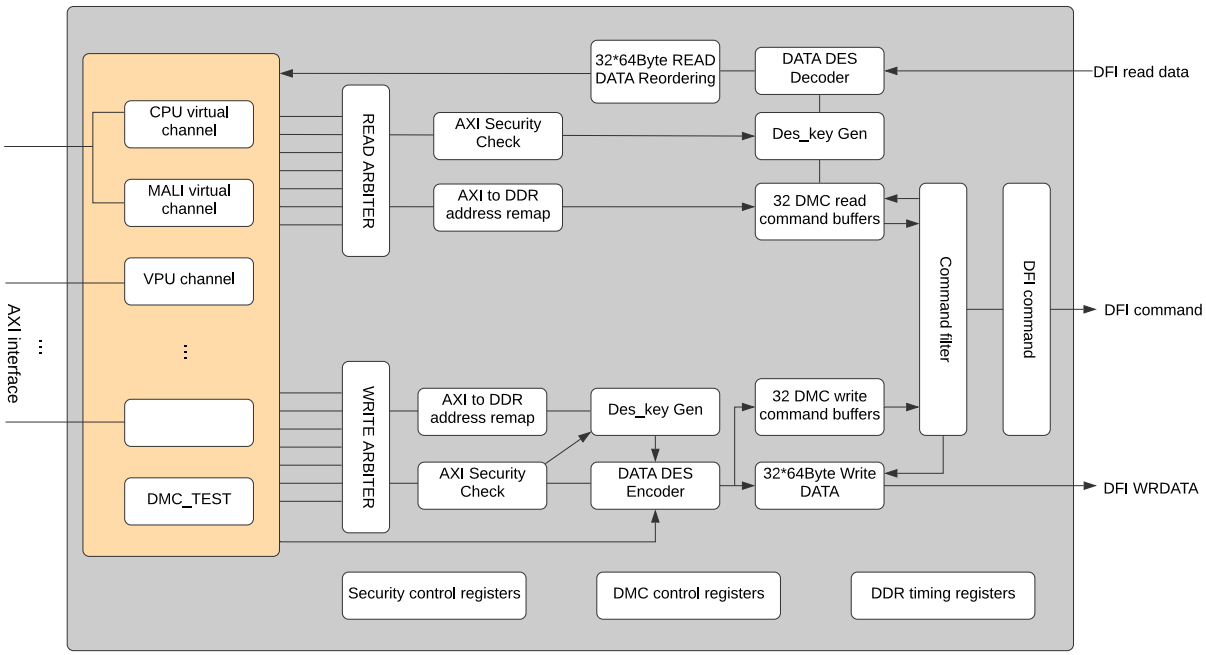


Figure 12-2 DMC Architecture



12.1.2 AXI to DDR Address Remapping

16 Gbytes of total AXI address space is remapped into up to 4 Gbytes of DDR address space per DMC controller for a total of up to 8 Gbytes of DDR. Each 512 Mbytes of interleaved DDR memory can be mapped to a different AXI address. The 32 (16 GB/512 MB) remap registers are defined below:

DMC_AXI2DDRx, x = 0x00 to 0x1F

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Bit	Register
15:8	Rank_base_addr
7:6	Not used
5	Rank_sel
4	Pure_16b
3	16b_in32
2	Not used
1:0	Map_mode

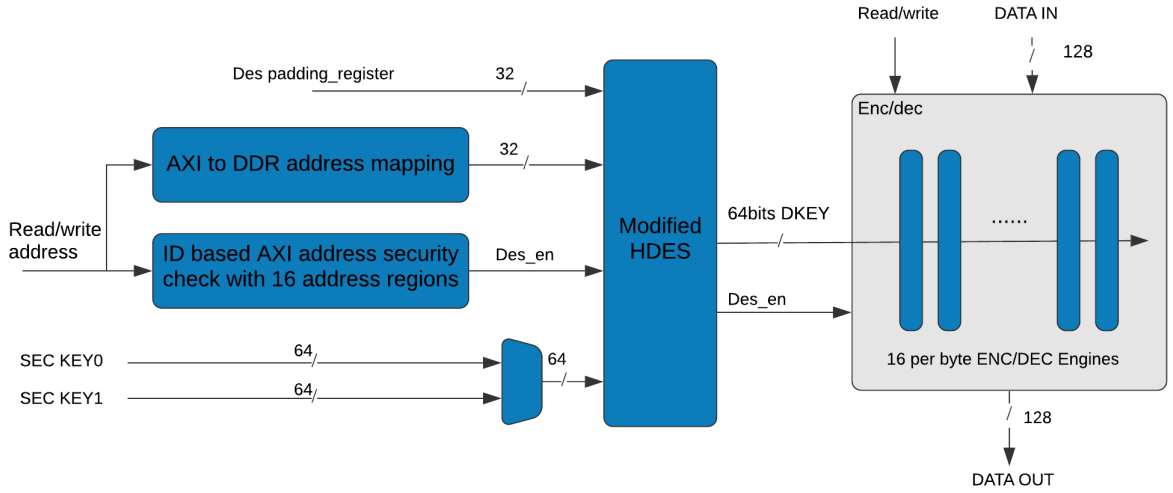
- **Rank_base_addr:** Remaps 256 Mbytes for each DMC controller for a total of 512 Mbytes if interleaved.
- **RANK_SEL:**
  - 1: this address region is in DDR SDRAM RANK1.
  - 0: this address region is in DDR SDRAM RANK0.
- **Pure_16b:** this region is a DDR 16bits data bus area in a 16bits DDR SDRAM.
- **16b_in32:** this region is a DDR 16bits data bus area in the 32bits DDR DATA bus. (2 DDR SDRAMs with different size).
- **Map_mode:**
  - 2'b00, 2'b10: address region is not used by this DMC.
  - 2'b01: address region is mapped to only this DMC in non-interleave mode.
  - 2'b10: region is mapped to both DMC controller using interleaving.

12.1.3 DMC AXI Address Security Region Checking and Data Scrambling

The 16 GB AXI address can be partitioned into 16 security regions inside the DMC. The first 15 regions are defined with start and end addresses with 4KB boundary. The last region is all the remaining address space not defined or enabled in the first 15 regions. Each region has an 8 bit control register and 320 AXI ARUSER/AWUSER master ID-based access control registers to control AXI master access. Each region address space can be overlapped. The security priority is highest for region 0 and decreases all the way down to region 15. For example, if an AXI transaction address exists in security region 0 and region 4, the region 0 security control is used for the transaction.

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Figure 12-3 AXI address security checking and data scrambling



Region_x Control Register

Table 12-1 Register Definition

Bit	Register
7:5	Security_level
4	monitor_en
3	local_des_en
2	Lock
1	Key_sel
0	Enable

- **Security_level:** Region security levels for DMA/DEMUX.
- **monitor_en:** Region monitored by DMC_PROT function. 1= monitored. 0= not monitored.
- **Local_des_en:** 1 = Enable DES scrambling for this region. NOTE: The Regionx_des_policy and Global_des_en bits below affects whether scrambling is actually enabled.
- **Lock:**1 = All region related registers are locked and cannot be changed (includes this control register, 10 ID based control registers and address range register)
- **Key_sel:** Selects security key (0 or 1) when scrambling is enabled
- **Enable:** Region enable bit. (NOTE: Region 15 is always enabled and this bit is ignored)

Global DES Control Register

Table 12-2 Register Definition

Bit	Register
31:16	Regionx_des_policy
15:2	Reserved

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Bit	Register
1	Global_des_en
0	Lock

- **Lock:** 1 = This register and des_padding register are locked and cannot be changed
- **Global_des_en:** 1 = Enable global DES data scrambling
- **Regionx_des_policy:** Each bit decides the scrambling policy for one security region.

  1: Region is DES scrambled if region Local_des_en && Global_des_en.

  0: Region is DES scrambled if region Local_des_en || Global_des_en.

ARUSER/AWUSER Based AXI Bus Security Information

Domain	Master	Bit Assignment							
		bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7:0 (sys level)
BUS MATRIX 0 (10b)	A53						AXI-PROT[2]	AXIPROT[1]	1
	A73						AXI-PROT[2]	AXIPROT[1]	2
	Mali0							PROT-MODE	3
	Mali1							PROT-MODE	4
	BUS MATRIX 0 internal							AXIPROT[1]	5
BUS MATRIX 1 (10b)	NNA0								8
	NNA1								9
	NNA2								10
	NNA3								11
BUS MATRIX 2	HDMI Rx								16
	usb2 controller								17
	dev0 p0 -SPICC0								24
	dev0 p1 -SPICC1								25
	dev0 p2 - SDEMMCA								26
	dev0 p3 - SDEMMCB								27
	dev0 p4 - SDEMMCC								28
	dev0 p5 - SPICC2								29
	dev0 p6 - reserved								30

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Domain	Master	Bit Assignment							
		bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7:0 (sys level)
	dev0 p7 - reserved								31
	dev1 p0 - reserved								32
	dev1 p1-reserved								33
	dev1 p2 -ETH								34
	dev1 p3 -AIFIFO								35
	dev1 p4 -AUDMA								36
	dev1 p5 - SPICC3								37
	dev1 p6 - SPICC4								38
	dev1 p7 - SPICC5								39
BUS MA-TRIX 3	GE2D							AxSEC	48
	GDC								49
	dewarp					AxID[1:0]		AxSEC	50
	vdec	AxUSER[6:0]							51
	hevc f	AxUSER[6:0]							52
	hevc b	AxUSER[6:0]							53
	hcodec	AxUSER[6:0]							54
	wave521						AXI-PROT[2]	AXIPROT [1]	55
BUS MA-TRIX 4 (20b)	demux(awuser)					wr_level[2:0]			63
	demux(ruser)					rd_level[2:0]			63
	ISP0								64
	ISP1								65
	ISP2								66
	ISP3								67
	DSP A						0	0	68
	DSP B						0	0	69
	AO-CPU						0	!HPROT [0]	70
	jtag						0	0	71
	dev2 p0 - AUDIO				AUDIO_SUBID[3:0]				72
	dev2 p1 - DMA	wr_level[2:0]			DMA_SUBID[3:0]				73
	dev2 p1 - DMA (ruser)				RD-ERR	rd_level[2:0]			73

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Domain	Master	Bit Assignment							
		bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7:0 (sys level)
	dev2 p1 - DMA (buser)							WRERR	73
	dev2 p2 - reserved								74
	dev2 p3 - reserved								75
	dev2 p4 - reserved								76
	dev2 p5 - reserved								77
	dev2 p6 - reserved								78
	dev2 p7 - reserved								79
BUS MA-TRIX 5 (20b)	VPU0			AxID[3:0]				AxSEC	80
	VPU1			AxID[3:0]				AxSEC	81
	VPU2			AxID[3:0]				AxSEC	82

```
//the 128 read/write control bits defines as below.
//bit 11:0. for BUS MATRIX 0  domain.
//bit [11:0] = {Bus Matrix 0_non_sec, Bus Matrix 0_sec, mali_non_prot, mali_prot,
//a73_non_sec_inst, a73_sec_inst, a73_non_sec_data, a73_sec_data,
//a53_non_sec_inst, a53_sec_inst, a53_non_sec_data, a53_sec_data };

//bit 15:12 for BUS MATRIX 1 nna domain.
// 15:12 = {nna3, nna2, nna1, nna0}

//bit 37:16 for BUS MATRIX 2 device0
// 37:16 = { not_used, spicc5, spicc4, spicc3, audma, aififo,
// eth, dev0_p1, dev0_p0, dev0_p7, dev0_p6, spicc2, sdemmcc, sdemmcb,
// sdemmca, spicc1, spicc0, not used, usb2, hdmi_rx };

//bit 78:38 for BUS MATRIX 3 ge2d,gdc, hcodec, vdec, hevc, wave521 etc.
//[78:38] Bus Matrix 3_sid_sel = { wave11, wave10, wave01, wave00,
//dewap_nonsec, dewap_sec, gdc, ge2d_nonsec, ge2d_sec,
// hevcf_7, hevcf_6, hevcf_5, hevcf_4, hevcf_3, hevcf_2, hevcf_1, hevcf_0,
//hevcb_7, hevcb_6, hevcb_5, hevcb_4, hevcb_3, hevcb_2, hevcb_1, hevcb_0,
//hcodec_7, hcodec_6, hcodec_5, hcodec_4, hcodec_3, hcodec_2, hcodec_1, hcodec_0,
//vdec_7, vdec_6, vdec_5, vdec_4, vdec_3, vdec_2, vdec_1, vdec_0};
//bit 119:80 for BUS MATRIX 4 device 2 aocpu dsp isp.
// { demux, jtag, dev2_p7, dev2_p6, dev2_p5, dev2_p4, dev2_p3, dev2_p2,
// dma_7, dma_6, dma_5, dma_4, dma_3, dma_2, dma_1, dma_0,
// audio_15, audio_14, audio_13, audio_12, audio_11, audio_10, audio_9, audio_8,
// audio_7, audio_6, audio_5, audio_4, audio_3, audio_2, audio_1, audio_0,
// aocpu_1, aocpu_0, dsp_b, dsp_a, isp3, isp2, isp1, isp0};
//bit 126:120. for Bus Matrix 5 VPU
// { dmc_test, vpu2_nosec, vpu2_sec, vpu1_nosec, vpu1_sec, vpu0_nosec, vpu0_sec}
```

12.1.4 DMC Security Register Bit Assignment

Register Control Bit	Master IDs Security Item	Special Requirement
0	a53_sec_data	
1	a53_non_sec_data	
2	a53_sec_inst	
3	a53_non_sec_inst	

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Register Control Bit	Master IDs Security Item	Special Requirement
4	a73_sec_data	
5	a73_non_sec_data	
6	a73_sec_inst	
7	a73_non_sec_inst	
8	mali_prot	
9	mali_non_prot	
10	Bus Matrix 0_sec	
11	Bus Matrix 0_non_sec	
12	nna0	
13	nna1	
14	nna2	
15	nna3	
16	hdmi_rx	
17	usb2	
18		
19		
20	not used	
21	spicc0	
22	spicc1	
23	sdemmca	
24	sdemmcb	
25	sdemmcc	
26	spicc2	
27	not used	
28	not used	
29	not used	
30	not used	
31	ETHNET	
32	aiffo	
33	audma	
34	spicc3	
35	spicc4	
36	spicc5	
37	not used	
38	vdec_lvl0	
39	vdec_lvl1	
40	vdec_lvl2	

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Register Control Bit	Master IDs Security Item	Special Requirement
41	vdec_lvl3	
42	vdec_lvl4	
43	vdec_lvl5	
44	vdec_lvl6	
45	vdec_lvl7	
46	hcodec_lvl0	
47	hcodec_lvl1	
48	hcodec_lvl2	
49	hcodec_lvl3	
50	hcodec_lvl4	
51	hcodec_lvl5	
52	hcodec_lvl6	
53	hcodec_lvl7	
54	hevcb_lvl0	
55	hevcb_lvl1	
56	hevcb_lvl2	
57	hevcb_lvl3	
58	hevcb_lvl4	
59	hevcb_lvl5	
60	hevcb_lvl6	
61	hevcb_lvl7	
62	hevcf_lvl0	
63	hevcf_lvl1	
64	hevcf_lvl2	
65	hevcf_lvl3	
66	hevcf_lvl4	
67	hevcf_lvl5	
68	hevcf_lvl6	
69	hevc_f_lv7	
70	ge2d_sec	
71	ge2d_nonsec	
72	gdc	
73	dewap_sec	
74	dewap_nonsec	
75	wave_sid0	

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Register Control Bit	Master IDs Security Item	Special Requirement
76	wave_sid1	
77	wave_sid2	
78	wave_sid3	
79	not used	
80	isp0	
81	isp1	
82	isp2	
83	isp3	
84	dsp_a	
85	dsp_b	
86	aocpu_0	
87	aocpu_1	
88	audio_sid0	
89	audio_sid1	
90	audio_sid2	
91	audio_sid3	
92	audio_sid4	
93	audio_sid5	
94	audio_sid6	
95	audio_sid7	
96	audio_sid8	
97	audio_sid9	
98	audio_sid10	
99	audio_sid11	
100	audio_sid12	
101	audio_sid13	
102	audio_sid14	
103	audio_sid15	
104	dma_thread0	sec_lvl <= region_lvl for write
105	dma_thread1	sec_lvl <= region_lvl for write
106	dma_thread2	sec_lvl <= region_lvl for write
107	dma_thread3	sec_lvl <= region_lvl for write
108	dma_thread4	sec_lvl <= region_lvl for write
109	dma_thread5	sec_lvl <= region_lvl for write
110	dma_thread6	sec_lvl <= region_lvl for write

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Register Control Bit	Master IDs Security Item	Special Requirement
111	dma_thread7	sec_lvl <= region_lvl for write
112	dev_port2	
113	dev_port3	
114	dev_port4	
115	dev_port5	
116	dev_prot6	
117	dev_prot7	
118	JTAG	
119	DEMUX	sec_lvl <= region_lvl for write
120	vpu0_sec	
121	vpu0_non-sec	
122	vpu1_sec	
123	vpu1_non_sec	
124	vpu2_sec	
125	vpu2_non_sec	
126	dmc_test	

12.1.5 AXI0 CPU & GPU Virtual Channel

AXI0 channel is from BUS MATRIX 0 for both CPU and GPU. But CPU and GPU have different QOS controls. CPU and GPU traffic are separated into two different virtual channels inside the DMC. The CPU traffic goes directly to AXI port arbiter. The GPU traffic goes through a 16 deep command FIFO before the AXI port arbiter. Inside the DMC, there are different QOS control systems for CPU and GPU channels.

Table 12-3 DMC AXI Port Mapping

AXI0	BUS MATRIX 0	A73, A53, GPU
AXI2	BUS MATRIX 5	3 VPU
AXI3	BUS MATRIX 1	4 NNA
AXI4	BUS MATRIX 2	DEVICE0, DEVICE1, USB, HDMI Rx
AXI5	DMC_TEST	DMC internal
AXI6	BUS MATRIX 3	DOS, GE2d
AXI7	BUS MATRIX 4	DEVICE2, ISP, DEMUX, DSP

12.1.6 DMC AXI Port QoS Control

DMC uses ARQOS[3:0]/AWQOS[3:0] bit fields as the default QoS control input. Inside each AXI port interface, there are several control registers to give additional QoS control. The QoS value is used for AXI port arbitration to decide which AXI request to put in the DMC command buffer. The QoS value of

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each AXI transaction is also used for the DDR command filter to balance the DDR performance and DDR request latency. There are standard QoS control features for all AXI ports and additional special QoS control features for the CPU, GPU, VPU and ISP.

1. Fixed QoS: Forces a fixed QoS value for each AXI port instead of the AXI ARQOS/AWQOS bit field input.
2. Transaction Grouping: Each AXI port can be programmed with transaction grouping that controls how many AXI transactions can be granted together when port wins the arbiter. NOTE: Also called arbitration weight
3. Improve Wait Time: If an AXI port cannot win the arbitration because of higher priority QoS AXI requests, the QoS value can be programmed to increase after waiting a certain number of clock cycles.
4. CPU IRQ/FIQ QoS Control: DMC can set the CPU channel QoS value to a fixed value if the CPU is inside an IRQ or FIQ interrupt.
5. CPU Auto QoS Control: DMC can set the CPU channel QoS value to a fixed value if there is a VPU request or other request inside the DMC.
6. VPU/ISP Urgent Control: DMC can set the VPU/ISP channel QoS value to a fixed value if the urgent control signal is set.
7. VPU Sleep: DMC can use this signal to trigger LPDDR4 PHY retraining.
8. AXI port status registers

12.1.7 DMC TEST Module

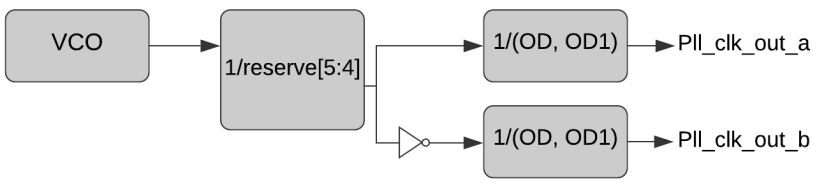
DMC test modules features:

- Increase test data pattern size to 128bursts (32x128).
- Error counters.
- Meets DRAM validation hooks requirements.
- Address use AXI linear address.
- Must use security control to identify the address space to be used.

12.1.8 Clock, Refresh, Retraining and Frequency Change for 2 DMCs

- dmc_clk_freq generates 2 DMC clocks with the same frequency but phase differs and controlled by different PLL control registers.
- Timer inside dmc_clk_freq to trigger both DMCs for auto refresh/retraining/frequency change at the same time.

Figure 12-4 Changes for 2 DMCs



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12.1.9 Register Description

Base address: 0xfe036c00

Table 12-4 AM_DDR_PLL_CNTL0 0x0000

Bit(s)	R/W	Default	Description
29			dpll_reset.
28			dpll_en.
27:26			dpll_clk_en
25			dpll_inv_sel
21:19			od1 OD1[0] : 0 /2, 1: /4. OD1[2:1]. 2'b00: /1, 2'b01: /2. 2'b10 /4. 2'b11: /8.
18:16			od
14:10			dpll_ref_div_n
8:0			dpll_int_num

Table 12-5 AM_DDR_PLL_CNTL1 0x0001

Bit(s)	R/W	Default	Description
18:0			ddr_dpll_frac

Table 12-6 AM_DDR_PLL_CNTL2 0x0002

Bit(s)	R/W	Default	Description
22:20			fref_sel
17:16			os_ssc
15:12			ssc_str_m
8			ssc_en
7:4			ssc_dep_sel
1:0			dpll ss_mode.

Table 12-7 AM_DDR_PLL_CNTL3 0x0003

Bit(s)	R/W	Default	Description
31			afc bypass
30			afc clk sel
29			code new
28			dco_m_en
27			dco_sdm_en
26			div2
25			div mode

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Bit(s)	R/W	Default	Description
24			fast_lock mode
23			fb_pre_div
22			filter_mode
21			fix_en
20			freq_shift_en
19			load
18			load_en
17			lock_f
16			pulse_width_en
15			sdmnc_en
14			sdmnc_mode
13			sdmnc_range
12			tdc_en
11			tdc_mode_sel
10			Ddr_dpll_wait_en

Table 12-8 AM_DDR_PLL_CNTL4 0x0004

Bit(s)	R/W	Default	Description
1:0			pfd_gain
7:4			filter_pvt1
11:8			filter pvt2
13:12			acq_gain
18:16			lambda0
22:20			lambda1
26:24			rou
30:28			alpha

Table 12-9 AM_DDR_PLL_CNTL5 0x0005

Bit(s)	R/W	Default	Description
15:0			reve
21:16			lm_s
27:24			lm_w
30:28			adj_vco_ldo

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Table 12-10 AM_DDR_PLL_CNTL6 0x0006

Bit(s)	R/W	Default	Description
15:0			reve
21:16			lm_s
27:24			lm_w
30:28			adj_vco_ldo

Table 12-11 AM_DDR_PLL_STS 0x0007

Bit(s)	R/W	Default	Description
31			DDR_PLL_LOCK
30:19			not used.
18			DDR_AFC_DONE
17			DDR_PLL_LOCK
16:7			DDR_DPLL_OUT_RSV
6:0			DDR_SDMNC_MONITOR

Table 12-12 DDR_CLK_CNTL 0x0008

Bit(s)	R/W	Default	Description
31			ddr_pll_clk enable. enable the clock from DDR_PLL to clock generation.
30.			ddr_pll_prod_test_en. enable the clock to clock/32 which to clock frequency measurement and production test pin.
29.			not used.
28.			clock generation logic soft reset. 0 = reset.
27.			phy_4xclk phase inverter..
26.			pll_freq divide/2. 1 use pll clock as n_clk.this setting is used for the synopsys DDR PHY PLL fast lock mode.
25			DDRPHY DfiClk/DMC clock selection. 1: AM_PLL clk output /2. 0: di- rectly output from AM_PLL .
24			enable AM_PLL CLK output /2 function. 1: enable. 0: disable. if try to use this clkoutput/2 function.
16			Enable DMC at speed mbist mode.
2.			enable dmc_clk.
1.			not used.
0.			enable LPDDR4-PHY clock

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Table 12-13 DDR_PHY_CTRL 0x0009

Bit(s)	R/W	Default	Description
31	R		DDr PHY power on status.
4.			DDR PHY PwrOkIn pin.
1.			DDR PHY APB soft reset_n.
0.			phy_reset_n.

Table 12-14 AM_DDR_PLL_FREQ1_OD 0x000c

Bit(s)	R/W	Default	Description
8			current FREQ selection. It can be forced to change to select which frequency to select, or it can auto changed by FREQ change hardware.
5:3			OD1.
2:0			OD.

DMC_REG_BASE = 0xfe036000

Table 12-15 DMC_REQ_CTRL 0x0000

Bit(s)	R/W	Default	Description
23.			enable dmc request of ambus chan 7. GE2D interface.
22.			Not used.
21.			enable dmc request of ambus chan 5. DOS VDEC interface.
20.			enable dmc request of ambus chan 4. VPU write interface 1.
19.			enable dmc request of ambus chan 3. VPU write interface 0.
18.			enable dmc request of ambus chan 2. VPU read interface 2.
17.			enable dmc request of ambus chan 1. VPU read interface 1.
16.			enable dmc request of ambus chan 0. VPU read interface 0.
15:12			Not used.
16.			enable dmc request of axibus chan 11 for Demux.
10:8			Not used.
7.			enable dmc request of axibus chan 7 for DEVICE.
6.			
5.			enable dmc request of axibus chan 5.reserved for dmc_test.
4.			enable dmc request of axibus chan 4 for HEVC.
3.			enable dmc request of axibus chan 3 for HDCP/HDMI.
2.			Not used.
1.			enable dmc request of axibus chan 1 for Mali GPU.
0.			enable dmc request of axibus chan 0 for CPU A35.

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Table 12-16 DMC_SOFT_RST 0x0001

Bit(s)	R/W	Default	Description
31~ 24			reserved for future.
23:16			8 AMBUS input interface n_clk domain reset_n signal. 0 normal working mode.
15:0.			16 AXI BUS input intefaces n_clk domain reset_n signal. 0 normal working mode. each bit for one interface.

Table 12-17 DMC_SOFT_RST1 0x0002

Bit(s)	R/W	Default	Description
31~ 24			not used.
23:16			8 am bus interfaces master clock domain reset_n signal. 0 reset. 1: normal working mode.
15:0.			16 AXI bus interfaces master clock domain reset_n signal. 0: reset. 1: normal working mode.

Table 12-18 DMC_SOFT_RST2 0x0003

Bit(s)	R/W	Default	Description
31~ 11.			reserved for future.
10			DMC DFI cmd soft reset_n
9			DMC DFI MISC soft reset_n
8			DMC DFI data soft reset_n
7			DMC DFI dcu soft reset_n
6			DMC siu soft reset_n
5.			DMC test soft reset_n.0 normal working mode.
4.			DMC low power control moudle soft reset_n. 0 normal working mode.
3.			DMC QOS monitor module soft reset_n.0 normal working mode.
2.			DMC register modle soft reset_n. 0 normal working mode.
1.			DMC canvas transfer module soft reset_n.0 normal working mode.
0.			DMC command buffers and command generation modules soft reset.0 = reset. 1

Table 12-19 DMC_RST_STS1 0x0004

Bit(s)	R/W	Default	Description
31~24.			not used.
23~0.			Read only. the DMC_SOFT_RST1 signal in n_clk domain. the purpose of this register is when one of the 2 clocks is too slow or too fast, we can read this register to make sure another clock domain reset is done.

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Table 12-20 DMC_CLKG_CTRL0 0x0006

Bit(s)	R/W	Default	Description
23:16			enable the 8 ambus interfaces both main and n_clk auto clock gating function. each 1 bit for one interface.
15:0.			enable the 16 axi interfaces both main and n_clk auto clock gating function. each 1 bit for one interface.

Table 12-21 DMC_CLKG_CTRL1 0x0007

Bit(s)	R/W	Default	Description
23:16.			force to disable the 8 ambus interfaces both main and n_clk. each 1 bit for one interface.
15:0			force to disable the 16 axi interfaces both main and n_clk. each 1 bit for one interface.

Table 12-22 DMC_CLKG_CTRL2 0x0008

Bit(s)	R/W	Default	Description
12			enable auto clock gating for awcmdfifo.
11			enable auto clock gating for arcmdfifo.
10			enable auto clock gating for dfi command generation
9			enable auto clock gating for dram controller
8			enable auto clock gating for dfi data path.
7.			enable auto clock gating for write rsp generation.
6.			enable auto clock gating for read rsp generation.
5.			enable auto clock gating for ddr0 command filter.
4.			enable auto clock gating for ddr0 write reorder buffer.
3.			enable auto clock gating for ddr0 write data buffer.
2.			enable auto clock gating for ddr0 read reorder buffer.
1.			enable auto clock gating for read canvas.
0.			enable auto clock gating for write canvas.

Table 12-23 DMC_CLKG_CTRL3 0x0009

Bit(s)	R/W	Default	Description
12			force to disable the clock of awcmdfifo.
11			force to disable the clock of arcmdfifo.
10			force to disable the clock of dfi command generation
9			force to disable the clock of dram controller
8			force to disable the clock of dfi data path.
7.			force to disable the clock of write rsp generation.

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Bit(s)	R/W	Default	Description
6.			force to disable the clock of read rsp generation.
5.			force to disable the clock of command filter.
4.			force to disable the clock of write reorder buffer.
3.			force to disable the clock of write data buffer.
2.			force to disable the clock of read reorder buffer.
1.			force to disable the clock of read canvas.
0.			force to disable the clock of write canvas.

DC_CAV_LUT_DATAL 0x0012

low 32 bits of canvas data which need to be configured to canvas memory.

Table 12-24 DC_CAV_LUT_DATAH 0x0013

Bit(s)	R/W	Default	Description
60:58			Endian control. 3'b000: no endian change. 3'b001:
57:56.			Canvas block mode.2 linear mode.
55:			canvas Y direction wrap control. 1 not wrap back.
54:			canvas X direction wrap control. 1 not wrap back.
53:41.			canvas Height.
40:29.			canvas Width, unit 8bytes. must in 32bytes boundary. that means last 2 bits must be 0.
28:0.			canvnas start address. unit. 8 bytes. must be in 32bytes boundary. that means last 2bits must be 0.

Table 12-25 DC_CAV_LUT_ADDR 0x0014

Bit(s)	R/W	Default	Description
9:8			write 90
7:0			256 canvas Look up table address.

DC_CAV_LUT_RDATAL 0x0015

DC_CAV_LUT_RDATAH 0x0016

DC_CAV_BLK_CTRL0 0x0018

DC_CAV_BLK_CTRL1 0x0019

DC_CAV_BLK_CTRL2 0x001a

DC_CAV_BLK_CTRL3 0x001b

DC_CAV_BLK_CTRL4 0x001c

DC_CAV_BLK_CTRL5 0x001d

DC_CAV_BLK_CTRL6 0x001e

DC_CAV_BLK_CTRL7 0x001f

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Table 12-26 DMC_MON_CTRL0 0x0020

Bit(s)	R/W	Default	Description
31.			qos_mon_en. write 1 to trigger the enable. polling this bit 0, means finished.or use interrupt to check finish.
30.			qos_mon interrupt clear. clear the qos monitor result.read 1 = qos mon finish interrupt.
7			BW monitor 7 enable.
6			BW monitor 6 enable.
5			BW monitor 5 enable.
4			BW monitor 4 enable.
3.			BW monitor 3 enable.
2.			BW monitor 2 enable.
1.			BW monitor 1 enable.
0.			BW monitor 0 enable.

Table 12-27 DMC_MON_TIMER 0x0021

Bit(s)	R/W	Default	Description
31:0			Timer for the monitor period.

Table 12-28 DMC_MON_ALL_IDLE_CNT 0x0022

Bit(s)	R/W	Default	Description
23:0			At the test period, the whole MMC all channel IDLE time. unit, dmc clock

Table 12-29 DMC_MON_ALL_BW 0x0023

Bit(s)	R/W	Default	Description
31:0			At the test period, the whole MMC granted data cycles. Unit : dmc clock cycles (16bytes).

Table 12-30 DMC_MON_ALL16_BW 0x0024

Bit(s)	R/W	Default	Description
23:0			At the test period, the whole MMC granted data cycles which goes to 16bits ddr. Unit : dmc clock cycles(16bytes).

Table 12-31 DMC_MON0_CTRL 0x0025

Bit(s)	R/W	Default	Description
31:16			End address[31:16]
15:0			start address[31:16]

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Table 12-32 DMC_MON0_CTRL1 0x0026

Bit(s)	R/W	Default	Description
23:0			BW monitor 0 channel select. 8 ambus port and 16 AXI port selection. 1 bit for one port.

Table 12-33 DMC_MON0_CTRL2 0x0027

Bit(s)	R/W	Default	Description
15:0			BW monitor 0 port select for the selected channel.

Table 12-34 DMC_MON0_BW 0x0028

Bit(s)	R/W	Default	Description
31:0			At the test period, this range granted data cycles for the select channel and ports.

Table 12-35 DMC_MON1_CTRL 0x0029

Bit(s)	R/W	Default	Description
23:0			BW monitor 1 channel select. 8 ambus port and 16 AXI port selection. 1 bit for one port.

Table 12-36 DMC_MON1_CTRL1 0x002a

Bit(s)	R/W	Default	Description
23:0			BW monitor 1 channel select. 8 ambus port and 16 AXI port selection. 1 bit for one port.

Table 12-37 DMC_MON1_CTRL2 0x002b

Bit(s)	R/W	Default	Description
15:0			BW monitor 1 port select for the selected channel.

Table 12-38 DMC_MON1_BW 0x002c

Bit(s)	R/W	Default	Description
31:0			At the test period, this range granted data cycles for the select channel and ports.

Table 12-39 DMC_MON2_CTRL 0x002d

Bit(s)	R/W	Default	Description
31:16			End address[31:16]
15:0			start address[31:16]

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Table 12-40 DMC_MON2_CTRL1 0x002e

Bit(s)	R/W	Default	Description
23:0			BW monitor 2 channel select. 8 ambus port and 16 AXI port selection. 1 bit for one port.

Table 12-41 DMC_MON2_CTRL2 0x002f

Bit(s)	R/W	Default	Description
15:0			BW monitor 2 port select for the selected channel.

Table 12-42 DMC_MON2_BW 0x0030

Bit(s)	R/W	Default	Description
31:0			At the test period, this range granted data cycles for the select channel and ports.

Table 12-43 DMC_MON3_CTRL 0x0031

Bit(s)	R/W	Default	Description
31:16			End address[31:16]
15:0			start address[31:16]

Table 12-44 DMC_MON3_CTRL1 0x0032

Bit(s)	R/W	Default	Description
23:0			BW monitor 3 channel select. 8 ambus port and 16 AXI port selection. 1 bit for one port.

Table 12-45 DMC_MON3_CTRL2 0x0033

Bit(s)	R/W	Default	Description
15:0			BW monitor 3 port select for the selected channel.

Table 12-46 DMC_MON3_BW 0x0034

Bit(s)	R/W	Default	Description
31:0			At the test period, this range granted data cycles for the select channel and ports.

Table 12-47 DMC_MON4_CTRL 0x0035

Bit(s)	R/W	Default	Description
31:16			End address[31:16]
15:0			start address[31:16]

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Table 12-48 DMC_MON4_CTRL1 0x0036

Bit(s)	R/W	Default	Description
23:0			BW monitor 4 channel select. 8 ambus port and 16 AXI port selection. 1 bit for one port.

Table 12-49 DMC_MON4_CTRL2 0x0037

Bit(s)	R/W	Default	Description
15:0			BW monitor 4 port select for the selected channel.

Table 12-50 DMC_MON4_BW 0x0038

Bit(s)	R/W	Default	Description
31:0			At the test period, this range granted data cycles for the select channel and ports.

Table 12-51 DMC_MON5_CTRL 0x0039

Bit(s)	R/W	Default	Description
31:16			End address[31:16]
15:0			start address[31:16]

Table 12-52 DMC_MON5_CTRL1 0x003a

Bit(s)	R/W	Default	Description
23:0			BW monitor 5 channel select. 8 ambus port and 16 AXI port selection. 1 bit for one port.

Table 12-53 DMC_MON5_CTRL2 0x003b

Bit(s)	R/W	Default	Description
15:0			BW monitor 5 port select for the selected channel.

Table 12-54 DMC_MON5_CTRL2 0x003c

Bit(s)	R/W	Default	Description
31:0			at the test period, this range granted data cycles for the select channel and ports

Table 12-55 DMC_MON6_CTRL 0x003d

Bit(s)	R/W	Default	Description
31:16			End address[31:16]
15:0			start address[31:16]

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Table 12-56 DMC_MON6_CTRL1 0x003e

Bit(s)	R/W	Default	Description
23:0			BW monitor 6 channel select. 8 ambus port and 16 AXI port selection. 1 bit for one port.

Table 12-57 DMC_MON6_CTRL2 0x003f

Bit(s)	R/W	Default	Description
15:0			BW monitor 6 port select for the selected channel.

Table 12-58 DMC_MON6_BW 0x0040

Bit(s)	R/W	Default	Description
31:0			At the test period, this range granted data cycles for the select channel and ports.

Table 12-59 DMC_MON7_CTRL 0x0041

Bit(s)	R/W	Default	Description
31:16			End address[31:16]
15:0			start address[31:16]

Table 12-60 DMC_MON7_CTRL1 0x0042

Bit(s)	R/W	Default	Description
23:0			BW monitor 7 channel select. 8 ambus port and 16 AXI port selection. 1 bit for one port.

Table 12-61 DMC_MON7_CTRL2 0x0043

Bit(s)	R/W	Default	Description
15:0			BW monitor 7 port select for the selected channel.

Table 12-62 DMC_MON7_BW 0x0044

Bit(s)	R/W	Default	Description
31:0			At the test period, this range granted data cycles for the select channel and ports.

DMC_CMD_FILTER_CTRL1 0x0050

Reserved.

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Table 12-63 DMC_CMD_FILTER_CTRL2 0x0051

Bit(s)	R/W	Default	Description
31:24.			keep the bank active if there's urgent level 3 read bank hit request.
23:16.			keep the bank active if there's urgent level 2 read bank hit request.
15:8.			keep the bank active if there's urgent level 1 read bank hit request.
7:0.			keep the bank active if there's urgent level 0 read bank hit request.

Table 12-64 DMC_CMD_FILTER_CTRL3 0x0052

Bit(s)	R/W	Default	Description
31.			force wbuf empty.
30:26			wbuf high level number
25:21			wbuf midlevel number
20:16			wbuf low level number
14:10			rbuf high level number
9:5			rbuf middle level number
4:0			rbuf low level number

Table 12-65 DMC_CMD_FILTER_CTRL4 0x0053

Bit(s)	R/W	Default	Description
29:25			tITW.long
24:20			tITW. short
19:12			tAP auto precharge the bank not used if idle that long time.
11:6			write to read accesses if there write hit request.
5:0			read to write accesses if there write hit request.

Table 12-66 DMC_CMD_FILTER_CTRL5 0x0054

Bit(s)	R/W	Default	Description
31:24			Once ddr data bus switch to read, the maximum read command number to give up the bus when there's write request pending for write buffer.
23:16			Once ddr data bus switch to write, the maximum write command number to give up the bus when there's read request pending too long.
15:8			Once ddr data bus switch to read, the minimum read command number to transfer back to write stage if there's still pending read request.
7:0			Once ddr data bus switch to write, the minimum write command number to transfer back to read stage if there's still pending write request.

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Table 12-67 DMC_CMD_FILTER_CTRL6 0x0055

Bit(s)	R/W	Default	Description
31:24			write urgent 3 request pending hold num.
23:16			write urgent 2 request pending hold num.
15:8			write urgent 1 request pending hold num.
7:0			write urgent 0 request pending hold num.

Table 12-68 DMC_CMD_FILTER_CTRL7 0x0056

Bit(s)	R/W	Default	Description
31:24			aw_req_pedning singal assertion after wbuf full.
23:16			aw_req_pending singal hold how long if wbuf not full.
15:8			write to read waiting cycles if there write hit request.
7:0			read to write waiting cycles if there write hit request.

Table 12-69 DMC_CMD_BUFFER_CTRL8 0x0057

Bit(s)	R/W	Default	Description
31:8			Reserved
7:0			rank limit to change to another rank.

Table 12-70 DMC_CMD_BUFFER_CTRL 0x0058

Bit(s)	R/W	Default	Description
31:26			total write buffer number. default 32.
25:20			total read buffer number. default 32.
19:8			reserved.
7:0			aw_pending_inc_num. increase write urgent level 1 when write com- mand waiting to in write buffer that long.

Table 12-71 DMC_CMD_BUFFER_CTRL1 0x0059

Bit(s)	R/W	Default	Description
29:24			read buffer number in non-urgent request.
23:16			read buffer bank miss watch dog threshold.
15:12			read buffer urgent level 3 counter inc weight.
11:8			read buffer urgent level 2 counter inc weight.
7:4			read buffer urgent level 1 counter inc weight.
3:0			read buffer urgent level 0 counter inc weight.

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Table 12-72 DMC_2ARB_CTRL 0x005c

Bit(s)	R/W	Default	Description
32:24.			Waiting limit to use the highest urgent level in the pipelines.
22.			1: allow to increase 2 urgent levels if waiting time is doubled than inc_ugt_limit.
21:12			inc_ugt_limit. if waiting time > inc_ugt_limit, increase the urgent level by one
11:6.			the final arbitration control from AXI bus(port channel 0~7).
5:0.			the final arbitration weight control for Ambus (port channel 8~15).

Table 12-73 DMC_VERSION 0x005f

Bit(s)	R/W	Default	Description
32:0.		0x0100-0008	Read only .

Table 12-74 DMC_AM0_CHAN_CTRL 0x0060

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

Table 12-75 DMC_AM0_HOLD_CTRL 0x0061

Bit(s)	R/W	Default	Description
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-76 DMC_AM0_CHAN_CTRL1 0x0062

Bit(s)	R/W	Default	Description
31:			side band signal used as block other request.
30			side band urgentincrease enable.
29			side band urgent decrease urgent enable.

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Bit(s)	R/W	Default	Description
23:16			when bit 31 enabled, block the ambus related bits read request.
15:0			when bit 31 enabled, block the axi bus related bits read request.

Table 12-77 DMC_AM0_CHAN_CTRL2 0x0063

Bit(s)	R/W	Default	Description
31:24			not used.
23:16			when side band signal used as block other request, and side bank signal is high, block the ambus related bits write request.
15:0			when side band signal used as block other request, and side bank signal is high, block the axi bus related bits write request.

Table 12-78 DMC_AM1_CHAN_CTRL 0x0064

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

Table 12-79 DMC_AM1_HOLD_CTRL 0x0065

Bit(s)	R/W	Default	Description
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-80 DMC_AM1_CHAN_CTRL1 0x0066

Bit(s)	R/W	Default	Description
31:			side band signal used as block other request.
30			side band urgentincrease enable.
29			side band urgent decrease urgent enable.
23:16			when bit 31 enabled, block the ambus related bits read request.
15:0			when bit 31 enabled, block the axi bus related bits read request.

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Table 12-81 DMC_AM1_CHAN_CTRL2 0x0067

Bit(s)	R/W	Default	Description
31:24			not used.
23:16			when side band signal used as block other request, and side bank signal is high, block the ambus related bits write request.
15:0			when side band signal used as block other request, and side bank signal is high, block the axi bus related bits write request.

Table 12-82 DMC_AM2_CHAN_CTRL 0x0068

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

Table 12-83 DMC_AM2_HOLD_CTRL 0x0069

Bit(s)	R/W	Default	Description
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-84 DMC_AM2_CHAN_CTRL1 0x006a

Bit(s)	R/W	Default	Description
31:			side band signal used as block other request.
30			side band urgent increase enable.
29			side band urgent decrease urgent enable.
23:16			when bit 31 enabled, block the ambus related bits read request.
15:0			when bit 31 enabled, block the axi bus related bits read request.

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Table 12-85 DMC_AM2_CHAN_CTRL2 0x006b

Bit(s)	R/W	Default	Description
31:24			not used.
23:16			when side band signal used as block other request, and side bank signal is high, block the ambus related bits write request.
15:0			when side band signal used as block other request, and side bank signal is high, block the axi bus related bits write request.

Table 12-86 DMC_AM3_CHAN_CTRL 0x006c

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

Table 12-87 DMC_AM3_HOLD_CTRL 0x006d

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-88 DMC_AM3_CHAN_CTRL1 0x006e

Bit(s)	R/W	Default	Description
31:			side band signal used as block other request.
30			side band urgent increase enable.
29			side band urgent decrease urgent enable.
23:16			when bit 31 enabled, block the ambus related bits read request.
15:0			when bit 31 enabled, block the axi bus related bits read request.

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Table 12-89 DMC_AM3_CHAN_CTRL2 0x006f

Bit(s)	R/W	Default	Description
31:24			not used.
23:16			when side band signal used as block other request, and side bank signal is high, block the ambus related bits write request.
15:0			when side band signal used as block other request, and side bank signal is high, block the axi bus related bits write request.

Table 12-90 DMC_AM4_CHAN_CTRL 0x0070

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

Table 12-91 DMC_AM4_HOLD_CTRL 0x0071

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-92 DMC_AM4_CHAN_CTRL1 0x0072

Bit(s)	R/W	Default	Description
31:			side band signal used as block other request.
30			side band urgentincrease enable.
29			side band urgent decrease urgent enable.
23:16			when bit 31 enabled, block the ambus related bits read request.
15:0			when bit 31 enabled, block the axi bus related bits read request.

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Table 12-93 DMC_AM4_CHAN_CTRL2 0x0073

Bit(s)	R/W	Default	Description
31:24			not used.
23:16			when bit 31 enabled, block the ambus related bits write request.
15:0			when bit 31 enabled, block the axi bus related bits write request.

Table 12-94 DMC_AM5_CHAN_CTRL 0x0074

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

Table 12-95 DMC_AM5_HOLD_CTRL 0x0075

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-96 DMC_AM6_CHAN_CTRL 0x0078

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

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Table 12-97 DMC_AM6_HOLD_CTRL 0x0079

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-98 DMC_AM7_CHAN_CTRL 0x007c

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

Table 12-99 DMC_AM7_HOLD_CTRL 0x007d

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-100 DMC_AXI0_CHAN_CTRL 0x0080

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.

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Bit(s)	R/W	Default	Description
19.			axi0 default urgent control :1 use AWUGT/ARUGT pins in the port. 0 :use bit [15:14] of this register..
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
15:14			axi0 default urgent level.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			arbiter weight

Table 12-101 DMC_AXI0_HOLD_CTRL 0x0081

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-102 DMC_AXI0_CHAN_CTRL1 0x0082

Bit(s)	R/W	Default	Description
31:28			FIQ status
27:24			IRQ status.
22			AXI0 write urgnet control enable.
21:20			AXI0 write urgent level if there's no other request.
19:18			AXI0 write urgent level if there's VIU request.
17:16			AXI0 write urgent level if there's request other than VIU
11:10			AXI0 FIQ triggered urgent level.
9:8			AXI0 IRQ triggered urgent level.
7			AXI0 IRQ/FIQ controll enable.
6			AXI0 read urgnet control enable.
5:4			AXI0 read urgent level if there's no other request.
3:2			AXI0 read urgent level if there's VIU request.
1:0			AXI0 read urgent level if there's request other than VIU

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Table 12-103 DMC_AXI1_CHAN_CTRL 0x0084

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
19.			axi0 default urgent control :1 use AWUGT/ARUGT pins in the port. 0 :use bit [15:14] of this register..
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
15:14			axi1 default urgent level.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

Table 12-104 DMC_AXI1_HOLD_CTRL 0x0085

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-105 DMC_AXI1_CHAN_CTRL1 0x0086

Bit(s)	R/W	Default	Description
31:28			FIQ status
27:24			IRQ status.
21:20			Mali QOS mode.
19:16			mail QOS high limit.
15:12			mail QOS mit limit.
11			ARMFIQ controlled super urgent enable.
10			ARMFIQ controlled urgent enable.
9.			ARM IRQ controlled super urgent enable.
8.			ARM IRQ controlled urgent enable.
7.			IRQ/FIQ control enable.
6:0			not used.

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Table 12-106 DMC_AXI2_CHAN_CTRL 0x0088

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
19.			axi0 default urgent control :1 use AWUGT/ARUGT pins in the port. 0 :use bit [15:14] of this register.
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
15:14			axi1 default urgent level.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

Table 12-107 DMC_AXI2_HOLD_CTRL 0x0089

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-108 DMC_AXI3_CHAN_CTRL 0x008c

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
19.			axi0 default urgent control :1 use AWUGT/ARUGT pins in the port. 0 :use bit [15:14] of this register..
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
15:14			axi1 default urgent level.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

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Table 12-109 DMC_AXI3_HOLD_CTRL 0x008d

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-110 DMC_AXI4_CHAN_CTRL 0x0090

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
19.			axi0 default urgent control :1 use AWUGT/ARUGT pins in the port. 0 :use bit [15:14] of this register..
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
15:14			axi1 default urgent level.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

Table 12-111 DMC_AXI4_HOLD_CTRL 0x0091

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

DMC_AXI5_CHAN_CTRL 0x0094

DMC_AXI5_HOLD_CTRL 0x0095

DMC_AXI6_CHAN_CTRL 0x0098

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Table 12-112

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
19.			axi0 default urgent control :1 use AWUGT/ARUGT pins in the port. 0 :use bit [15:14] of this register..
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
15:14			axi1 default urgent level.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

Table 12-113 DMC_AXI6_HOLD_CTRL 0x0099

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-114 DMC_AXI7_CHAN_CTRL 0x009c

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
19.			axi0 default urgent control :1 use AWUGT/ARUGT pins in the port. 0 :use bit [15:14] of this register..
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
15:14			axi1 default urgent level.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

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Table 12-115 DMC_AXI7_HOLD_CTRL 0x009d

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-116 DMC_AXI8_CHAN_CTRL 0x00a0

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
19.			axi0 default urgent control :1 use AWUGT/ARUGT pins in the port. 0 :use bit [15:14] of this register..
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
15:14			axi1 default urgent level.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

Table 12-117 DMC_AXI8_HOLD_CTRL 0x00a1

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-118 DMC_AXI9_CHAN_CTRL 0x00a4

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.

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Bit(s)	R/W	Default	Description
29:20			write request pending cycle numberto inc urgent level if not granted.
19.			axi0 default urgent control :1 use AWUGT/ARUGT pins in the port. 0 :use bit [15:14] of this register..
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
15:14			axi1 default urgent level.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

Table 12-119 DMC_AXI9_HOLD_CTRL 0x00a5

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-120 DMC_AXI10_CHAN_CTRL 0x00a8

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
19.			axi0 default urgent control :1 use AWUGT/ARUGT pins in the port. 0 :use bit [15:14] of this register.
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
15:14			axi1 default urgent level.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

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Table 12-121 DMC_AXI10_HOLD_CTRL 0x00a9

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-122 DMC_AXI10_CHAN_CTRL1 0x00aa

Bit(s)	R/W	Default	Description
11			Mali/NNA channel FIQ controlled super urgent enable.
10			Mali/NNA channel FIQ controlled urgent enable.
9.			Mali/NNA channel IRQ controlled super urgent enable.
8.			Mali/NNA channel IRQ controlled urgent enable.
7.			IRQ/FIQ controll enable.
6:0			not used.

Table 12-123 DMC_AXI11_CHAN_CTRL 0x00ac

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
19.			axi0 default urgent control :1 use AWUGT/ARUGT pins in the port. 0 :use bit [15:14] of this register..
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
15:14			axi1 default urgent level.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

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Table 12-124 DMC_AXI11_HOLD_CTRL 0x00ad

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-125 DMC_AXI12_CHAN_CTRL 0x00b0

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.
29:20			write request pending cycle numberto inc urgent level if not granted.
19.			axi0 default urgent control :1 use AWUGT/ARUGT pins in the port. 0 :use bit [15:14] of this register..
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
15:14			axi1 default urgent level.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

Table 12-126 DMC_AXI12_HOLD_CTRL 0x00b1

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-127 DMC_AXI13_CHAN_CTRL 0x00b4

Bit(s)	R/W	Default	Description
31			enable to incr 2 urgent levels if the pending cycles is doubled.
30			enable to incr 3 urgent levels.

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Bit(s)	R/W	Default	Description
29:20			write request pending cycle numberto inc urgent level if not granted.
19.			axi0 default urgent control :1 use AWUGT/ARUGT pins in the port. 0 :use bit [15:14] of this register..
18.			force this channel all request to be super urgent request.
17.			force this channel all request to be urgent request.
16.			force this channel all request to be non urgent request.
15:14			axi1 default urgent level.
13:4			read request pending cycle numberto inc urgent level if not granted.
3:0			canvas arbiter arbiter weight

Table 12-128 DMC_AXI13_HOLD_CTRL 0x00b5

Bit(s)	R/W	Default	Description
31:24			write hold num. max outstanding request number.
23:16			write hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.
15:8			read hold num. max outstanding request number.
7:0			read hold release num. if the outstanding request == hold num, then hold this request unless the outstanding request number below the hold release number, then continue to request.

Table 12-129 DMC_AM0_CHAN_STS 0x00b8

Bit(s)	R/W	Default	Description
31:24	Readonly		READ command counter.
23:16	Readonly		Not used.
15:8	Readonly		Not used.
7:0	Readonly		ARVALID&& !ARREADY waiting counter.

Table 12-130 DMC_AM1_CHAN_STS 0x00b9

Bit(s)	R/W	Default	Description
31:24	Readonly		READ command counter.
23:16	Readonly		Not used.

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Bit(s)	R/W	Default	Description
15:8	Readon-ly		Not used.
7:0	Readon-ly		ARVALID&& !ARREADY waiting counter.

Table 12-131 DMC_AM2_CHAN_STS 0x00ba

Bit(s)	R/W	Default	Description
31:24	Readon-ly		READ command counter.
23:16	Readon-ly		Not used.
15:8	Readon-ly		Not used.
7:0	Readon-ly		ARVALID&& !ARREADY waiting counter.

Table 12-132 DMC_AM3_CHAN_STS 0x00bb

Bit(s)	R/W	Default	Description
31:24	Readon-ly		READ command counter.
23:16	Readon-ly		Write command counter.
15:8	Readon-ly		AWVALID&& !AWREADY waiting counter..
7:0	Readon-ly		ARVALID&& !ARREADY waiting counter.

Table 12-133 DMC_AM4_CHAN_STS 0x00bc

Bit(s)	R/W	Default	Description
31:24	Readon-ly		READ command counter.
23:16	Readon-ly		Write command counter.
15:8	Readon-ly		AWVALID&& !AWREADY waiting counter..
7:0	Readon-ly		ARVALID&& !ARREADY waiting counter.

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Table 12-134 DMC_AM5_CHAN_STS 0x00bd

Bit(s)	R/W	Default	Description
31:24	Readon-ly		READ command counter.
23:16	Readon-ly		Write command counter.
15:8	Readon-ly		AWVALID&& !AWREADY waiting counter..
7:0	Readon-ly		ARVALID&& !ARREADY waiting counter.

Table 12-135 DMC_AM6_CHAN_STS 0x00be

Bit(s)	R/W	Default	Description
31:24	Readon-ly		READ command counter.
23:16	Readon-ly		Write command counter.
15:8	Readon-ly		AWVALID&& !AWREADY waiting counter..
7:0	Readon-ly		ARVALID&& !ARREADY waiting counter.

Table 12-136 DMC_AM7_CHAN_STS 0x00bf

Bit(s)	R/W	Default	Description
31:24	Readon-ly		READ command counter.
23:16	Readon-ly		Write command counter.
15:8	Readon-ly		AWVALID&& !AWREADY waiting counter..
7:0	Readon-ly		ARVALID&& !ARREADY waiting counter.

Table 12-137 DMC_AXI0 _CHAN_STS 0x00c0

Bit(s)	R/W	Default	Description
31:24	Readon-ly		READ command counter.
23:16	Readon-ly		Write command counter.
15:8	Readon-ly		AWVALID&& !AWREADY waiting counter..
7:0	Readon-ly		ARVALID&& !ARREADY waiting counter.

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Table 12-138 DMC_AXI1 _CHAN_STS 0x00c1

Bit(s)	R/W	Default	Description
31:24	Readonly		READ command counter.
23:16	Readonly		Write command counter.
15:8	Readonly		AWVALID&& !AWREADY waiting counter..
7:0	Readonly		ARVALID&& !ARREADY waiting counter.

Table 12-139 DMC_AXI2 _CHAN_STS 0x00c2

Bit(s)	R/W	Default	Description
31:24	Readonly		READ command counter.
23:16	Readonly		Write command counter.
15:8	Readonly		AWVALID&& !AWREADY waiting counter..
7:0	Readonly		ARVALID&& !ARREADY waiting counter.

Table 12-140 DMC_AXI3 _CHAN_STS 0x00c3

Bit(s)	R/W	Default	Description
31:24	Readonly		READ command counter.
23:16	Readonly		Write command counter.
15:8	Readonly		AWVALID&& !AWREADY waiting counter..
7:0	Readonly		ARVALID&& !ARREADY waiting counter.

Table 12-141 DMC_AXI4 _CHAN_STS 0x00c4

Bit(s)	R/W	Default	Description
31:24	Readonly		READ command counter.
23:16	Readonly		Write command counter.
15:8	Readonly		AWVALID&& !AWREADY waiting counter..
7:0	Readonly		ARVALID&& !ARREADY waiting counter.

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Table 12-142 DMC_AXI5 _CHAN_STS 0x00c5

Bit(s)	R/W	Default	Description
31:24	Readon-ly		READ command counter.
23:16	Readon-ly		Write command counter.
15:8	Readon-ly		AWVALID&& !AWREADY waiting counter..
7:0	Readon-ly		ARVALID&& !ARREADY waiting counter.

Table 12-143 DMC_AXI6 _CHAN_STS 0x00c6

Bit(s)	R/W	Default	Description
31:24	Readon-ly		READ command counter.
23:16	Readon-ly		Write command counter.
15:8	Readon-ly		AWVALID&& !AWREADY waiting counter..
7:0	Readon-ly		ARVALID&& !ARREADY waiting counter.

Table 12-144 DMC_AXI7 _CHAN_STS 0x00c7

Bit(s)	R/W	Default	Description
31:24	Readon-ly		READ command counter.
23:16	Readon-ly		Write command counter.
15:8	Readon-ly		AWVALID&& !AWREADY waiting counter..
7:0	Readon-ly		ARVALID&& !ARREADY waiting counter.

Table 12-145 DMC_CHAN_STS 0x00ce

Bit(s)	R/W	Default	Description
27	R		always 1
26	R		ddr0 write data buffer idle. 1 : idle 0: busy.
25	R		always 1.
24	R		ddr0 wbuf idle. 1 : idle 0: busy.
23:16	R		ambus channel idle. 1 : idle 0: busy.
15:0.	R		axibus channel idle. 1 : idle 0: busy.

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Table 12-146 DMC_IRQ_STS 0x00cf

Bit(s)	R/W	Default	Description
31:3			Not used.
2			QOS Monitor interrupt flag. 1: means there's QOS monitor interrup. write 1 to clean this interrupt.
1			WRITE protection interrupt. 1: means there's write protection violation. need to write DMC_PROT_IRQ_CTRL bit 1to clean this bit.
0			read protection interrupt. 1: means there's read protection violation. need to write DMC_PROT_IRQ_CTRL bit 0 to clean this bit.

Table 12-147 DMC_PROT0_RANGE 0x00d0

Bit(s)	R/W	Default	Description
31:16			range end address.
15:0			range start address

Table 12-148 DMC_PROT0_CTRL 0x00d1

Bit(s)	R/W	Default	Description
23:16			each bit to eanble one of the 8 ambus channal for the protection function.
15:0			each bit to enable one of the 15 axi channel input for the protection function.

Table 12-149 DMC_PROT0_CTRL1 0x00d2

Bit(s)	R/W	Default	Description
26			protection 0 read access protection enable.
25			protection 0 write access block function. if enabled, the access wouldn't write to the DDR SDRAM. if not enabled only generate a interrupt, but the access still wrote to DDR.
24			protection range 0 write access protection enable.
15:0			Protection range0 subid selection. If no subid or mult port selected this range shouldbe 0xffff.

Table 12-150 DMC_PROT1_RANGE 0x00d3

Bit(s)	R/W	Default	Description
31:16			range end address.
15:0			range start address

Table 12-151 DMC_PROT1_CTRL 0x00d4

Bit(s)	R/W	Default	Description
23:16			each bit to eanble one of the 8 ambus channal for the protection function.
15:0			each bit to enable one of the 15 channel input for the protection function.

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Table 12-152 DMC_PROT1_CTRL1 0x00d5

Bit(s)	R/W	Default	Description
26			protection range 1 read access protection enable bit.
25			protection 1 write access block function. if enabled, the access wouldn't write to the DDR SDRAM. if not enabled only generate a interrupt, but the access still wrote to DDR.
24			protection range 1 write access protection enable bit.
15:0			Protection range1 subid selection. If no subid or mult port selected this range shouldbe 0xffff.

Table 12-153 DMC_PROT_VIO_0 0x00d6

Bit(s)	R/W	Default	Description
31:0			ddr0 write protection violation address.

Table 12-154 DMC_PROT_VIO_1 0x00d7

Bit(s)	R/W	Default	Description
31:21			not used. always 0.
20			ddr0 protection 1 vilation.
19			ddr0 protection 0 vilation.
18:16			ddr0 write violation AWPROT bits.
15:0			ddr0_write violation ID.

Table 12-155 DMC_PROT_VIO_2 0x00d8

Bit(s)	R/W	Default	Description
31:0			ddr0 read protection violation address.

Table 12-156 DMC_PROT_VIO_3 0x00d9

Bit(s)	R/W	Default	Description
31:21			not used. always 0.
20			ddr0 read protection 1 violation.
19			ddr0 read protection 0 violation.
18:16			ddr0 read violation ARPROT bits.
15:0			ddr0 read violation ID.

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Table 12-157 DMC_PROT_IRQ_CTRL 0x00da

Bit(s)	R/W	Default	Description
2			protect function IRQ enable.
1			write protection violation. write 1 to clean write protection vio registers.
0			read protection violation. write 1 to clean read protection vio registers.

Base address for the following registers: 0xfe037800

Table 12-158 DMC_TEST_STA 0x0000

Bit(s)	R/W	Default	Description
31:0			TEST start address.

Table 12-159 DMC_TEST_EDA 0x0001

Bit(s)	R/W	Default	Description
31:0			TEST end address.

Table 12-160 DMC_TEST_CTRL 0x0002

Bit(s)	R/W	Default	Description
31.			enable test.
30.			when enable test, enable the write to DDR function.
29.			when enable test, enable the read from DDR function.
28.			when enable test, enable the sha calculation function must be same as read ena- ble but without write function.
27.			enable to compare data. when do the read enable to enable the error comparison. suppose the read data should be same as the data in the write buffer.
26.			Not used.
25.			address generation type.0 continuous increase the address in the range of test start address and test end address. 1:test module would pick the random address from test start address and test end address.
24.			done type.0 use the DMC_TEST_NUM register as the counter of test numbers. for write if the write command number == the DMC_TEST_NUM, the write is done. for read if the read command number == the DMC TEST_num, the read id done. for one read command can be repeated repeat number times. 1 :finished at end address.
23.			wdata type.1 the first write is {WD3, WD2,WD1,WD0}, then the latter is the previous data plus a pattern.({ + WD7,+ WD6, + WD5, + WD4}). 0 :the WDATA is the data in write register. 1 compare the sha result with the test sha message registers. 0 dont compare the result.
22:20			read repeat times.for non-sha function, we can define multi times of the read. the test module would repeat the same address repeat times.
19.			limit write.0 no outstanding write request limitation. 1:limit the outstanding write commands to the number of bits [15:8]

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Bit(s)	R/W	Default	Description
18.			limit read.0. no outstanding read request limitation. 1. limit the read outstanding request to the number of bits[7:0].
17:16.			Not used.
15:8			write outstanding commands limit.
7:0			read outstanding commands limit.

Table 12-161 DMC_TEST_NUM 0x0003

Bit(s)	R/W	Default	Description
31:0			How many test command for the test if the DMC_TEST_CTRL bit 24 = 0.

Table 12-162 DMC_TEST_WDG 0x0004

Bit(s)	R/W	Default	Description
31:16.			write response watch dog.
15:0.			read response watch dog.

Table 12-163 DMC_TEST_COMP_MASK 0x0005

Bit(s)	R/W	Default	Description
31:0			1 :to MASK this bit. 0:compare this bit.

Table 12-164 DMC_TEST_WSTRB0 0x0006

Bit(s)	R/W	Default	Description
31:16			the second cycle.
15:0			the first cycle.

Table 12-165 DMC_TEST_WSTRB1 0x0007

Bit(s)	R/W	Default	Description
31:16			the Forth cycle.
15:0			the third cycle.

DMC_TEST_WD0 0x0010

DMC_TEST_WD1 0x0011

DMC_TEST_WD2 0x0012

DMC_TEST_WD3 0x0013

DMC_TEST_WD4 0x0014

DMC_TEST_WD5 0x0015

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DMC_TEST_WD6 0x0016

DMC_TEST_WD7 0x0017

DMC_TEST_WD8 0x0018

DMC_TEST_WD9 0x0019

DMC_TEST_WD10 0x001a

DMC_TEST_WD11 0x001b

DMC_TEST_WD12 0x001c

DMC_TEST_WD13 0x001d

DMC_TEST_WD14 0x001e

DMC_TEST_WD15 0x001f

DMC_TEST_RD0 0x0020

DMC_TEST_RD1 0x0021

DMC_TEST_RD2 0x0022

DMC_TEST_RD3 0x0023

DMC_TEST_RD4 0x0024

DMC_TEST_RD5 0x0025

DMC_TEST_RD6 0x0026

DMC_TEST_RD7 0x0027

DMC_TEST_RD8 0x0028

DMC_TEST_RD9 0x0029

DMC_TEST_RD10 0x002a

DMC_TEST_RD11 0x002b

DMC_TEST_RD12 0x002c

DMC_TEST_RD13 0x002d

DMC_TEST_RD14 0x002e

DMC_TEST_RD15 0x002f

DMC_TEST_ERR_ADDR 0x0040

DMC_TEST_ERR_CNT 0x0041

Table 12-166 DMC_TEST_STS 0x0042

Bit(s)	R/W	Default	Description
31,			test done bit. write 1 to clean.
30,			indicate address err
29:7			not used.
6.			read data resp error(caused by security or rd latency).
5.			test MRR/MPR rd latency error. write 1 clear
4,			sha done.write 1 to clean.
3,			write done.write 1 to clean.

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Bit(s)	R/W	Default	Description
2,			read done. write 1 to clean
1,			write watchdog triggered.write 1 to clean
0,			read watchdog triggered. write 1 to clean.

DMC_TEST_WRCMD_ADDR 0x0043

DMC_TEST_RDCMD_ADDR 0x0044

DMC_TEST_RDRSP_ADDR 0x0045

DMC_SEC_REG_BASE = 0xfe037000

Table 12-167 DMC_SEC_RANGE0_CTRL 0x0000

Bit(s)	R/W	Default	Description
31:16			| 0 | range0_eda | range 0 end address higher 16bits.
15:0			| 0 | range0_sta | range 0 start address higher 16bits.

Table 12-168 DMC_SEC_RANGE0_CTRL1 0x0001

Bit(s)	R/W	Default	Description
7:5			| 0 | range0_secrity_level | range0 security level for DMC and DEMUX only.
4			| 0 | range0_prot_en | range0 allow protect monitor function. 1:allowed. 0:not allowed.
3			| 0 | range0_local_des_en | range0 data describle enable. 1:enable. 0 :disable. this bit works together with GLOBAL_DES_EN to decide this region data describle enable or not.
2			| 0 | range0_lock | lock range 0 registers. write 1 to lock range 0 register. can't change anymore.
1			| 0 | range0_key_sel | range 0 data describle key selection. 1 :key1. 0 :key0.
0			| 0 | range0_en | range 0 enable bit. 1 :enable, 0 :disable.

Table 12-169 DMC_SEC_RANGE1_CTRL 0x0002

Bit(s)	R/W	Default	Description
31:16			| 0 | range1_eda | range 1 end address higher 16bits.
15:0			| 0 | range1_sta | range 1 start address higher 16bits.

Table 12-170 DMC_SEC_RANGE1_CTRL1 0x0003

Bit(s)	R/W	Default	Description
7:5			| 0 | range1_secrity_level | range1 security level for DMC and DEMUX only.
4			| 0 | range1_prot_en | range1 allow protect monitor function. 1:allowed. 0:not allowed.
3			| 0 | range1_local_des_en | range1 data describle enable. 1:enable. 0 :disable. this bit works together with GLOBAL_DES_EN to decide this region data describle enable or not.

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Bit(s)	R/W	Default	Description
2			| 0 | range1_lock | lock range 1 registers. write 1 to lock range 1 register. can't change anymore.
1			| 0 | range1_key_sel | range 1 data describle key selection. 1 :key1. 1 :key0.
0			| 0 | range1_en | range 0 enable bit. 1 :enable, 0 :disable.

Table 12-171 DMC_SEC_RANGE2_CTRL 0x0004

Bit(s)	R/W	Default	Description
31:16			| 0 | range2_eda | range 2 end address higher 16bits.
15:0			| 0 | range2_sta | range 2 start address higher 16bits.

Table 12-172 DMC_SEC_RANGE2_CTRL1 0x0005

Bit(s)	R/W	Default	Description
7:5			| 0 | range2_secrity_level | range2 security level for DMC and DEMUX only.
4			| 0 | range2_prot_en | range2 allow protect monitor function. 1:allowed. 0:not allowed.
3			| 0 | range2_local_des_en | range2 data describle enable. 1:enable. 0 :disable. this bit works together with GLOBAL_DES to decide this region data describle enable or not.
2			| 0 | range2_lock | lock range 2 registers. write 1 to lock range 2 register. can't change anymore.
1			| 0 | range2_key_sel | range 2 data describle key selection. 1 :key1. 1 :key0.
0			| 0 | range2_en | range 2 enable bit. 1 :enable, 0 :disable.

Table 12-173 DMC_SEC_RANGE3_CTRL 0x0006

Bit(s)	R/W	Default	Description
31:16			| 0 | range3_eda | range 3 end address higher 16bits.
15:0			| 0 | range3_sta | range 3 start address higher 16bits.

Table 12-174 DMC_SEC_RANGE3_CTRL1 0x0007

Bit(s)	R/W	Default	Description
7:5			| 0 | range3_secrity_level | range3 security level for DMC and DEMUX only.
4			| 0 | range3_prot_en | range3 allow protect monitor function. 1:allowed. 0:not allowed.
3			| 0 | range3_local_des_en | range3 data describle enable. 1:enable. 0 :disable. this bit works together with GLOBAL_DES to decide this region data describle enable or not.
2			| 0 | range3_lock | lock range 3 registers. write 1 to lock range 3 related registers. can't change anymore.

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Bit(s)	R/W	Default	Description
1			| 0 | range3_key_sel | range 3 data describle key selection. 1 :key1. 1 :key0.
0			| 0 | range3_en | range 3 enable bit. 1 :enable, 0 :disable.

Table 12-175 DMC_SEC_RANGE4_CTRL 0x0008

Bit(s)	R/W	Default	Description
31:16			| 0 | range4_eda | range 4 end address higher 16bits.
15:0			| 0 | range4_sta | range 4 start address higher 16bits.

Table 12-176 DMC_SEC_RANGE4_CTRL1 0x0009

Bit(s)	R/W	Default	Description
7:5			| 0 | range4_secrity_level | range4 security level for DMC and DEMUX only.
4			| 0 | range4_prot_en | range4 allow protect monitor function. 1:allowed. 0:not allowed.
3			| 0 | range4_local_des_en | range4 data describle enable. 1:enable. 0 :disable. this bit works together with GLOBAL_DES to decide this region data describle enable or not.
2			| 0 | range4_lock | lock range 4 registers. write 1 to lock range 4 related registers. can't change anymore.
1			| 0 | range4_key_sel | range 4 data describle key selection. 1 :key1. 1 :key0.
0			| 0 | range4_en | range 4 enable bit. 1 :enable, 0 :disable.

DMC_SEC_RANGE5_CTRL 0x000a

DMC_SEC_RANGE5_CTRL1 0x000b

DMC_SEC_RANGE6_CTRL 0x000c

DMC_SEC_RANGE6_CTRL1 0x000d

DMC_SEC_RANGE7_CTRL 0x000e

DMC_SEC_RANGE7_CTRL1 0x000f

DMC_SEC_RANGE8_CTRL 0x0010

DMC_SEC_RANGE8_CTRL1 0x0011

DMC_SEC_RANGE9_CTRL 0x0012

DMC_SEC_RANGE9_CTRL1 0x0013

DMC_SEC_RANGE10_CTRL 0x0014

DMC_SEC_RANGE10_CTRL1 0x0015

DMC_SEC_RANGE11_CTRL 0x0016

DMC_SEC_RANGE11_CTRL1 0x0017

DMC_SEC_RANGE12_CTRL 0x0018

DMC_SEC_RANGE12_CTRL1 0x0019

DMC_SEC_RANGE13_CTRL 0x001a

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DMC_SEC_RANGE13_CTRL1 0x001b

DMC_SEC_RANGE14_CTRL 0x001c

DMC_SEC_RANGE14_CTRL1 0x001d

DMC_SEC_RANGE15_CTRL1 0x001f

Per range per sub ID access enable.

Each range uses 128 bits read security control register bits and 128 bits write security control register bits. These registers are from DMC_SEC_RANGEx_RID_CTRL0~DMC_SEC_RANGEx_RID_CTRL3 for read access control. And DMC_SEC_RANGEx_WID_CTRL0~DMC_SEC_RANGEx_WID_CTRL3 for write access control.

This 128 bits security register bits define as bellow:

Bit(s)	R/W	Default	Description
127:96			Not used.
95:94			VPU2_RD security control based security flag.
93:92			VPU1_RD/VPU1_WR security control based security flag.
91:90			VPU0_RD/VPU0_WR security control based security flag.
89:88			GE2d control based GE2D security flag.
87:80.			8 bits for VDEC 8 secruity levels.
79:64.			16bits for HEVC 16 security LEVELs.
63:56			Not used.
55:48			for 8 DMA thread ID numbers in device subid number 2.
47.			for device subid number 15. //demod
46.			for device subid number 14. //sana
45.			for device subid number 13. //eth
44.			for device subid number 12. //spicc
43.			for device subid number 11. //sd_emmc_C
42.			for device subid number 10.
41.			for device subid number 9. //parser
40.			for device subid number 8. //parser1
39.			for device subid number 7. //aififo
38			for device subid number 6. //aififo
37.			for device subid number 5. //usb1
36.			for device subid number 4. //not used.
35.			for device subid number 3. //ahb arb0
34.			for device subid number 2. //usb0
33.			for device subid number 1. //usb0.
32.			for device subid number 0.
31:16.			together with bit 63:56 for 16 audio subid numbers.
15.			Not used.
14			For Demux.

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Bit(s)	R/W	Default	Description
13.			
12.			for DMC test.
11:8			for 4 HDMI subid[1:0] numbers.
7:6			Not used.
5:4			for GPU protected video. bit 5: for non-protected video. bit 4. for protected video.
3:0.			For CPU. Each bit for one CPU secure mode. Bit 0 for data secure access. Bit 1 for data non-secure access. Bit 2 for instruction secure access. Bit 3 for instruction non-secure access.

DMC_SEC_RANGE0_RID_CTRL0 0x0020

Range0_rd_sid_en[31:0]

DMC_SEC_RANGE0_RID_CTRL1 0x0021

Range0_rd_sid_en[63:32]

DMC_SEC_RANGE0_RID_CTRL2 0x0022

Range0_rd_sid_en[95:64]

DMC_SEC_RANGE0_RID_CTRL3 0x0023

Range0_rd_sid_en[127:96]

DMC_SEC_RANGE0_RID_CTRL4 0x0024

Not used.

DMC_SEC_RANGE1_RID_CTRL0 0x0026

DMC_SEC_RANGE1_RID_CTRL1 0x0027

DMC_SEC_RANGE1_RID_CTRL2 0x0028

DMC_SEC_RANGE1_RID_CTRL3 0x0029

DMC_SEC_RANGE1_RID_CTRL4 0x002a

DMC_SEC_RANGE2_RID_CTRL0 0x002c

DMC_SEC_RANGE2_RID_CTRL1 0x002d

DMC_SEC_RANGE2_RID_CTRL2 0x002e

DMC_SEC_RANGE2_RID_CTRL3 0x002f

DMC_SEC_RANGE2_RID_CTRL4 0x0030

DMC_SEC_RANGE3_RID_CTRL0 0x0032

DMC_SEC_RANGE3_RID_CTRL1 0x0033

DMC_SEC_RANGE3_RID_CTRL2 0x0034

DMC_SEC_RANGE3_RID_CTRL3 0x0035

DMC_SEC_RANGE3_RID_CTRL4 0x0036

DMC_SEC_RANGE4_RID_CTRL0 0x0038

DMC_SEC_RANGE4_RID_CTRL1 0x0039

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DMC_SEC_RANGE4_RID_CTRL2 0x003a
DMC_SEC_RANGE4_RID_CTRL3 0x003b
DMC_SEC_RANGE4_RID_CTRL4 0x003c
DMC_SEC_RANGE5_RID_CTRL0 0x003e
DMC_SEC_RANGE5_RID_CTRL1 0x003f
DMC_SEC_RANGE5_RID_CTRL2 0x0040
DMC_SEC_RANGE5_RID_CTRL3 0x0041
DMC_SEC_RANGE5_RID_CTRL4 0x0042
DMC_SEC_RANGE6_RID_CTRL0 0x0044
DMC_SEC_RANGE6_RID_CTRL1 0x0045
DMC_SEC_RANGE6_RID_CTRL2 0x0046
DMC_SEC_RANGE6_RID_CTRL3 0x0047
DMC_SEC_RANGE6_RID_CTRL4 0x0048
DMC_SEC_RANGE7_RID_CTRL0 0x004a
DMC_SEC_RANGE7_RID_CTRL1 0x004b
DMC_SEC_RANGE7_RID_CTRL2 0x004c
DMC_SEC_RANGE7_RID_CTRL3 0x004d
DMC_SEC_RANGE7_RID_CTRL4 0x004e
DMC_SEC_RANGE8_RID_CTRL0 0x0050
DMC_SEC_RANGE8_RID_CTRL1 0x0051
DMC_SEC_RANGE8_RID_CTRL2 0x0052
DMC_SEC_RANGE8_RID_CTRL3 0x0053
DMC_SEC_RANGE8_RID_CTRL4 0x0054
DMC_SEC_RANGE9_RID_CTRL0 0x0056
DMC_SEC_RANGE9_RID_CTRL1 0x0057
DMC_SEC_RANGE9_RID_CTRL2 0x0058
DMC_SEC_RANGE9_RID_CTRL3 0x0059
DMC_SEC_RANGE9_RID_CTRL4 0x005a
DMC_SEC_RANGE10_RID_CTRL0 0x005c
DMC_SEC_RANGE10_RID_CTRL1 0x005d
DMC_SEC_RANGE10_RID_CTRL2 0x005e
DMC_SEC_RANGE10_RID_CTRL3 0x005f
DMC_SEC_RANGE10_RID_CTRL4 0x0060
DMC_SEC_RANGE11_RID_CTRL0 0x0062
DMC_SEC_RANGE11_RID_CTRL10x0063
DMC_SEC_RANGE11_RID_CTRL2 0x0064
DMC_SEC_RANGE11_RID_CTRL3 0x0065
DMC_SEC_RANGE11_RID_CTRL4 0x0066

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DMC_SEC_RANGE12_RID_CTRL0 0x0068
DMC_SEC_RANGE12_RID_CTRL1 0x0069
DMC_SEC_RANGE12_RID_CTRL2 0x006a
DMC_SEC_RANGE12_RID_CTRL3 0x006b
DMC_SEC_RANGE12_RID_CTRL4 0x006c
DMC_SEC_RANGE13_RID_CTRL0 0x006e
DMC_SEC_RANGE13_RID_CTRL1 0x006f
DMC_SEC_RANGE13_RID_CTRL2 0x0070
DMC_SEC_RANGE13_RID_CTRL3 0x0071
DMC_SEC_RANGE13_RID_CTRL4 0x0072
DMC_SEC_RANGE14_RID_CTRL0 0x0074
DMC_SEC_RANGE14_RID_CTRL1 0x0075
DMC_SEC_RANGE14_RID_CTRL2 0x0076
DMC_SEC_RANGE14_RID_CTRL3 0x0077
DMC_SEC_RANGE14_RID_CTRL4 0x0078
DMC_SEC_RANGE15_RID_CTRL0 0x007a
DMC_SEC_RANGE15_RID_CTRL1 0x007b
DMC_SEC_RANGE15_RID_CTRL2 0x007c
DMC_SEC_RANGE15_RID_CTRL3 0x007d
DMC_SEC_RANGE15_RID_CTRL4 0x007e
DMC_SEC_RANGE0_WID_CTRL0 0x0080
DMC_SEC_RANGE0_WID_CTRL1 0x0081
DMC_SEC_RANGE0_WID_CTRL2 0x0082
DMC_SEC_RANGE0_WID_CTRL3 0x0083
DMC_SEC_RANGE0_WID_CTRL4 0x0084
DMC_SEC_RANGE1_WID_CTRL0 0x0086
DMC_SEC_RANGE1_WID_CTRL1 0x0087
DMC_SEC_RANGE1_WID_CTRL2 0x0088
DMC_SEC_RANGE1_WID_CTRL3 0x0089
DMC_SEC_RANGE1_WID_CTRL4 0x008a
DMC_SEC_RANGE2_WID_CTRL0 0x008c
DMC_SEC_RANGE2_WID_CTRL1 0x008d
DMC_SEC_RANGE2_WID_CTRL2 0x008e
DMC_SEC_RANGE2_WID_CTRL3 0x008f
DMC_SEC_RANGE2_WID_CTRL4 0x0090
DMC_SEC_RANGE3_WID_CTRL0 0x0092
DMC_SEC_RANGE3_WID_CTRL1 0x0093
DMC_SEC_RANGE3_WID_CTRL2 0x0094

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DMC_SEC_RANGE3_WID_CTRL3 0x0095
DMC_SEC_RANGE3_WID_CTRL4 0x0096
DMC_SEC_RANGE4_WID_CTRL0 0x0098
DMC_SEC_RANGE4_WID_CTRL1 0x0099
DMC_SEC_RANGE4_WID_CTRL2 0x009a
DMC_SEC_RANGE4_WID_CTRL3 0x009b
DMC_SEC_RANGE4_WID_CTRL4 0x009c
DMC_SEC_RANGE5_WID_CTRL0 0x009e
DMC_SEC_RANGE5_WID_CTRL1 0x009f
DMC_SEC_RANGE5_WID_CTRL2 0x00a0
DMC_SEC_RANGE5_WID_CTRL3 0x00a1
DMC_SEC_RANGE5_WID_CTRL4 0x00a2
DMC_SEC_RANGE6_WID_CTRL0 0x00a4
DMC_SEC_RANGE6_WID_CTRL1 0x00a5
DMC_SEC_RANGE6_WID_CTRL2 0x00a6
DMC_SEC_RANGE6_WID_CTRL3 0x00a7
DMC_SEC_RANGE6_WID_CTRL4 0x00a8
DMC_SEC_RANGE7_WID_CTRL0 0x00aa
DMC_SEC_RANGE7_WID_CTRL1 0x00ab
DMC_SEC_RANGE7_WID_CTRL2 0x00ac
DMC_SEC_RANGE7_WID_CTRL3 0x00ad
DMC_SEC_RANGE7_WID_CTRL4 0x00ae
DMC_SEC_RANGE8_WID_CTRL0 0x00b0
DMC_SEC_RANGE8_WID_CTRL1 0x00b1
DMC_SEC_RANGE8_WID_CTRL2 0x00b2
DMC_SEC_RANGE8_WID_CTRL3 0x00b3
DMC_SEC_RANGE8_WID_CTRL4 0x00b4
DMC_SEC_RANGE9_WID_CTRL0 0x00b6
DMC_SEC_RANGE9_WID_CTRL1 0x00b7
DMC_SEC_RANGE9_WID_CTRL2 0x00b8
DMC_SEC_RANGE9_WID_CTRL3 0x00b9
DMC_SEC_RANGE9_WID_CTRL4 0x00ba
DMC_SEC_RANGE10_WID_CTRL0 0x00bc
DMC_SEC_RANGE10_WID_CTRL1 0x00bd
DMC_SEC_RANGE10_WID_CTRL2 0x00be
DMC_SEC_RANGE10_WID_CTRL3 0x00bf
DMC_SEC_RANGE10_WID_CTRL4 0x00c0
DMC_SEC_RANGE11_WID_CTRL0 0x00c2

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DMC_SEC_RANGE11_WID_CTRL1 0x00c3

DMC_SEC_RANGE11_WID_CTRL2 0x00c4

DMC_SEC_RANGE11_WID_CTRL3 0x00c5

DMC_SEC_RANGE11_WID_CTRL4 0x00c6

DMC_SEC_RANGE12_WID_CTRL0 0x00c8

DMC_SEC_RANGE12_WID_CTRL1 0x00c9

DMC_SEC_RANGE12_WID_CTRL2 0x00ca

DMC_SEC_RANGE12_WID_CTRL3 0x00cb

DMC_SEC_RANGE12_WID_CTRL4 0x00cc

DMC_SEC_RANGE13_WID_CTRL0 0x00ce

DMC_SEC_RANGE13_WID_CTRL1 0x00cf

DMC_SEC_RANGE13_WID_CTRL2 0x00d0

DMC_SEC_RANGE13_WID_CTRL3 0x00d1

DMC_SEC_RANGE13_WID_CTRL4 0x00d2

DMC_SEC_RANGE14_WID_CTRL0 0x00d4

DMC_SEC_RANGE14_WID_CTRL1 0x00d5

DMC_SEC_RANGE14_WID_CTRL2 0x00d6

DMC_SEC_RANGE14_WID_CTRL3 0x00d7

DMC_SEC_RANGE14_WID_CTRL4 0x00d8

DMC_SEC_RANGE15_WID_CTRL0 0x00da

DMC_SEC_RANGE15_WID_CTRL1 0x00db

DMC_SEC_RANGE15_WID_CTRL2 0x00dc

DMC_SEC_RANGE15_WID_CTRL3 0x00dd

DMC_SEC_RANGE15_WID_CTRL4 0x00de

Table 12-177 DMC_DES_PADDING 0x00e0

Bit(s)	R/W	Default	Description
31:0			| 0 | des_pading | 32bits address padding used for DES dkey generation.

Table 12-178 DMC_DES_CTRL 0x00e1

Bit(s)	R/W	Default	Description
31			range15_des_en policy :1 range15_des_en = range15_local_des_en && GLOBAL_DES_EN. 0 :range15_des_en = range15_local_des_en || GLOBAL_DES_EN.
30			range14_des_en policy :1 range14_des_en = range14_local_des_en && GLOBAL_DES_EN. 0 :range14_des_en = range14_local_des_en || GLOBAL_DES_EN.
29			range13_des_en policy :1 range13_des_en = range13_local_des_en && GLOBAL_DES_EN. 0 :range13_des_en = range13_local_des_en || GLOBAL_DES_EN.

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Bit(s)	R/W	Default	Description
28			range12_des_en policy :1 range12_des_en = range12_local_des_en && GLOBAL_DES_EN. 0 :range12_des_en = range12_local_des_en || GLOBAL_DES_EN.
27			range11_des_en policy :1 range11_des_en = range11_local_des_en && GLOBAL_DES_EN. 0 :range11_des_en = range11_local_des_en || GLOBAL_DES_EN.
26			range10_des_en policy :1 range11_des_en = range10_local_des_en && GLOBAL_DES_EN. 0 :range10_des_en = range10_local_des_en || GLOBAL_DES_EN.
25			range9_des_en policy :1 range9_des_en = range9_local_des_en && GLOBAL_DES_EN. 0 : range9_des_en = range9_local_des_en || GLOBAL_DES_EN.
24			range8_des_en policy :1 range8_des_en = range8_local_des_en && GLOBAL_DES_EN. 0 : range8_des_en = range8_local_des_en || GLOBAL_DES_EN.
23			range7_des_en policy :1 range7_des_en = range7_local_des_en && GLOBAL_DES_EN. 0 : range7_des_en = range7_local_des_en || GLOBAL_DES_EN.
22			range6_des_en policy :1 range6_des_en = range6_local_des_en && GLOBAL_DES_EN. 0 : range6_des_en = range6_local_des_en || GLOBAL_DES_EN.
21			range5_des_en policy :1 range5_des_en = range5_local_des_en && GLOBAL_DES_EN. 0 : range5_des_en = range5_local_des_en || GLOBAL_DES_EN.
20			range4_des_en policy :1 range4_des_en = range4_local_des_en && GLOBAL_DES_EN. 0 : range4_des_en = range4_local_des_en || GLOBAL_DES_EN.
19			range3_des_en policy :1 range3_des_en = range3_local_des_en && GLOBAL_DES_EN. 0 : range3_des_en = range3_local_des_en || GLOBAL_DES_EN.
18			range2_des_en policy :1 range2_des_en = range2_local_des_en && GLOBAL_DES_EN. 0 : range2_des_en = range2_local_des_en || GLOBAL_DES_EN.
17			range1_des_en policy :1 range1_des_en = range1_local_des_en && GLOBAL_DES_EN. 0 : range1_des_en = range1_local_des_en || GLOBAL_DES_EN.
16			range0_des_en policy :1 range0_des_en = range0_local_des_en && GLOBAL_DES_EN. 0 : range0_des_en = range0_local_des_en || GLOBAL_DES_EN.
1			| 0 | GLOBAL_DES_EN | 1:Global DES enable. 0 :global DES disable. default is 0.
0			| 0 | DES_lock | one time lock bit. after write 1 to this bit, DMC_DES_CTRL, DMC_DES_PADDING can't be write and read.

DMC_DES_KEY0_REG0 0x00e2

DMC_DES_KEY0_REG1 0x00e3

DMC_DES_KEY0_REG2 0x00e4

DMC_DES_KEY0_REG3 0x00e5

DMC_DES_KEY1_REG0 0x00e6

DMC_DES_KEY1_REG1 0x00e7

DMC_DES_KEY1_REG2 0x00e8

DMC_DES_KEY1_REG3 0x00e9

Table 12-179 DDR_APB_SEC_CTRL0 0x00f0

APB access control for dmc request control registers.

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Bit(s)	R/W	Default	Description
31:9			Not used.
8			Lock bit if this bit =1, this register is locked and cann't modified anymore
7:0		0x5	APB access enable for each APB USER ID. 1: enable. 0: disable.

Table 12-180 DDR_APB_SEC_CTRL1 0x00f1

APB access control for DMC DRAM timing parameter and DFI interface registers.

Bit(s)	R/W	Default	Description
31:9			Not used.
8			Lock bit if this bit =1, this register is locked and cann't modified anymore
7:0		0x5	APB access enable for each APB USER ID. 1: enable. 0: disable.

Table 12-181 DDR_APB_SEC_CTRL2 0x00f2

APB access control for DMC PLL clock frequency control registers.

Bit(s)	R/W	Default	Description
31:9			Not used.
8			Lock bit if this bit =1, this register is locked and cann't modified anymore
7:0		0x5	APB access enable for each APB USER ID. 1: enable. 0: disable.

Table 12-182 DDR_APB_SEC_CTRL3 0x00f3

APB access control for DMC sticky registers.

Bit(s)	R/W	Default	Description
31:9			Not used.
8			Lock bit if this bit =1, this register is locked and cann't modified anymore
7:0		0x5	APB access enable for each APB USER ID. 1: enable. 0: disable.

Table 12-183 DDR_APB_SEC_CTRL4 0x00f4

APB access control for DMC test control registers.

Bit(s)	R/W	Default	Description
31:9			Not used.
8			Lock bit if this bit =1, this register is locked and cann't modified anymore
7:0		0x5	APB access enable for each APB USER ID. 1: enable. 0: disable.

Table 12-184 DDR_APB_SEC_CTRL5 0x00f5

APB access control for DMC clk reset control registers.

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Bit(s)	R/W	Default	Description
31:9			Not used.
8			Lock bit if this bit =1, this register is locked and cann't modified anymore
7:0		0x5	APB access enable for each APB USER ID. 1: enable. 0: disable.

Table 12-185 DDR_APB_SEC_CTRL6 0x00f6

APB access control for DMC protection control registers.

Bit(s)	R/W	Default	Description
31:9			Not used.
8			Lock bit if this bit =1, this register is locked and cann't modified anymore
7:0		0x5	APB access enable for each APB USER ID. 1: enable. 0: disable.

Table 12-186 DDR_APB_SEC_CTRL7 0x00f7

APB access control for DMC normal control registers.

Bit(s)	R/W	Default	Description
31:9			Not used.
8			Lock bit if this bit =1, this register is locked and cann't modified anymore
7:0		0x5	APB access enable for each APB USER ID. 1: enable. 0: disable.

Table 12-187 DDR_APB_SEC_CTRL8 0x00f8

APB access control for DDR PHY group control registers.

Bit(s)	R/W	Default	Description
31:24			Not used.
23:16			APB access enable for DDR PHY group 1 register.
8			Lock bit if this bit =1, this register is locked and cann't modified anymore
7:0		0x50005	APB access enable for DDR PHY group0. for each APB USER ID. 1: enable. 0: disable.

Table 12-188 DDR_APB_SEC_CTRL9 0x00f9

APB access control for DMC canvas control registers.

Bit(s)	R/W	Default	Description
31:9			Not used.
8			Lock bit if this bit =1, this register is locked and cann't modified anymore
7:0		0x5	APB access enable for each APB USER ID. 1: enable. 0: disable.

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Table 12-189 DMC_SEC_STATUS 0x00fa

Bit(s)	R/W	Default	Description
31~ 4.			not used.
3			1:normal security register write violation.(APB bus WDATA not equre the register value when APB write).write 1 to clean this bit to 0.
2			sec_alert.1 DMC security register alert function triggered. can't clean. only reset DMC can clear this bit.
1			write security violation.
0.			read security violation.

Table 12-190 DDR_VIO_ADDR0 0x00fb

Bit(s)	R/W	Default	Description
31:0			Write secure violation address.

Table 12-191 DMC_VIO_ADDR1 0x00fc

Bit(s)	R/W	Default	Description
31:24			not used. always 0.
24			ddr0 secure check violation.
23			not used.
22			not used.
21			not used.
20.			not used.
19			ddr0 write address overflow. write out of DDR size.
18:16			ddr0 write violation AWPROT bits.
15:0			ddr0_write violation ID.

Table 12-192 DDR_VIO_ADDR2 0x00fd

Bit(s)	R/W	Default	Description
31:0			read secure violation address.

Table 12-193 DMC_VIO_ADDR3 0x00fe

Bit(s)	R/W	Default	Description
24			ddr0 read secure check violation.
23			not used.
22			not used.
21			ddr0 read trap1 violation
20.			ddr0 read trap0 violation
19			ddr 0 read address overflow. write out of DDR size.

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Bit(s)	R/W	Default	Description
18:16			ddr 0 read violation ARPROT bits.
15:0			ddr 0 read violation ID.

Table 12-194 DMC_DDR_CTRL 0x0100

Bit(s)	R/W	Default	Description
27.			0 cavnas use 64bytes boundary 1 :canvas use 32bytes boundary.
24:22			3'b000 :ddr3 mode. 3'b001 :ddr4 mode. 3'b010 :lpddr3 mode. 3'b011 :lpddr4 mode.
21.			rank1 enable bit. if 1,rank1 used the address map is as bit 5:3 defined.
20			DDR4 BG1 enable bit.
18:			ddrphy_16b, DDR PHY DDR SDRAM data bits width. 1:16bits. 0 :32 bits.
16.			ddr_16b, 1:only use 16bits data in a 32bits DDR PHY data interface. 0 :normal data interface.
7:4			ddr1_size.DDR rank1 size control. 4'b0000 :DDR rank 1 is 128Mbyte. 4'b0001 : DDR rank 1 is 256Mbyte. 4'b0010 :DDR rank 1 is 512Mbyte. 4'b0011 :DDR rank 1 is 1Gbyte. 4'b0100 :DDR rank 1 is 2Gbyte. 4'b0101 :DDR rank 1 is 4Gbyte. 4'b1000 :DDR rank 1 is 192Mbyte. 4'b1001 :DDR rank 1 is 374Mbyte. 4'b1010 :DDR rank 1 is 768Mbyte. 4'b1011 :DDR rank 1 is 1.5Gbyte. 4'b1100 :DDR rank 1 is 3Gbyte. others : reserved.
3:0			ddr0_size. DDR rank0 size control. 4'b0000 :DDR rank 0 is 128Mbyte. 4'b0001 : DDR rank 0 is 256Mbyte. 4'b0010 :DDR rank 0 is 512Mbyte. 4'b0011 :DDR rank 0 is 1Gbyte. 4'b0100 :DDR rank 0 is 2Gbyte. 4'b0101 :DDR rank 0 is 4Gbyte. 4'b1000 :DDR rank 1 is 192Mbyte. 4'b1001 :DDR rank 1 is 374Mbyte. 4'b1010 :DDR rank 1 is 768Mbyte. 4'b1011 :DDR rank 1 is 1.5Gbyte. 4'b1100 :DDR rank 1 is 3Gbyte. others : reserved.

Table 12-195 DDR0_ADDRMAP_0 0x0101

Bit(s)	R/W	Default	Description
29:25			ca8.
24:20			ca7.
19:15			ca6.
14:10			ca5.
9:5			ca4.
4:0			ca3.

Table 12-196 DDR0_ADDRMAP_1 0x0102

Bit(s)	R/W	Default	Description
29:25			ra2.
24:20			ra1.
19:15			ra0.
14:10			ca11.

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Bit(s)	R/W	Default	Description
9:5			ca10.
4:0			ca9.

Table 12-197 DDR0_ADDRMAP_2 0x0103

Bit(s)	R/W	Default	Description
29:25			ra8.
24:20			ra7.
19:15			ra6.
14:10			ra5.
9:5			ra4.
4:0			ra3.

Table 12-198 DDR0_ADDRMAP_3 0x0104

Bit(s)	R/W	Default	Description
29:25			ra14
24:20			ra13
19:15			ra12
14:10			ra11
9:5			ra10
4:0			ra9

Table 12-199 DDR0_ADDRMAP_4 0x0105

Bit(s)	R/W	Default	Description
29:25			ra16 for DDR4 SDRAM
24:20			bg1 for DDR4 SDRAM.
19:15			ba2. or bg0 for DDR4.
14:10			ba1.
9:5			ba0.
4:0			ra15.

Table 12-200 DDR1_ADDRMAP_0 0x0106

Bit(s)	R/W	Default	Description
29:25			ca8.
24:20			ca7.
19:15			ca6.
14:10			ca5.

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Bit(s)	R/W	Default	Description
9:5			ca4.
4:0			ca3.

Table 12-201 DDR1_ADDRMAP_1 0x0107

Bit(s)	R/W	Default	Description
29:25			ra2.
24:20			ra1.
19:15			ra0.
14:10			ca11.
9:5			ca10.
4:0			ca9.

Table 12-202 DDR1_ADDRMAP_2 0x0108

Bit(s)	R/W	Default	Description
29:25			ra8.
24:20			ra7.
19:15			ra6.
14:10			ra5.
9:5			ra4.
4:0			ra3.

Table 12-203 DDR1_ADDRMAP_3 0x0109

Bit(s)	R/W	Default	Description
29:25			ra14
24:20			ra13
19:15			ra12
14:10			ra11
9:5			ra10
4:0			ra9

Table 12-204 DDR1_ADDRMAP_4 0x010a

Bit(s)	R/W	Default	Description
29:25			ra16 for DDR4 SDRAM
24:20			bg1 for DDR4 SDRAM.
19:15			ba2. or bg0 for DDR4.
14:10			ba1.

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Bit(s)	R/W	Default	Description
9:5			ba0.
4:0			ra15.

Table 12-205 DMC_AXI2DDR0 0x0120

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-206 DMC_AXI2DDR1 0x0121

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-207 DMC_AXI2DDR2 0x0122

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-208 DMC_AXI2DDR3 0x0123

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-209 DMC_AXI2DDR4 0x0124

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.

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Bit(s)	R/W	Default	Description
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-210 DMC_AXI2DDR5 0x0125

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-211 DMC_AXI2DDR6 0x0126

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-212 DMC_AXI2DDR7 0x0127

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-213 DMC_AXI2DDR8 0x0128

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-214 DMC_AXI2DDR9 0x0129

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.

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Bit(s)	R/W	Default	Description
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-215 DMC_AXI2DDRA 0x012a

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-216 DMC_AXI2DDRB 0x012b

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-217 DMC_AXI2DDRC 0x012c

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-218 DMC_AXI2DDRD 0x012d

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-219 DMC_AXI2DDRE 0x012e

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.

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Bit(s)	R/W	Default	Description
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-220 DMC_AXI2DDRF 0x012f

Bit(s)	R/W	Default	Description
6			range_valid1 not valid.
5			rank_sel, 0 rank1.
4			ddr_data_width, 0 16bits.
3:0.			remap to one rank of DDR SDRAM linear address[31:28]

Table 12-221 DMC_DDR_CTRL1 0x0130

Bit(s)	R/W	Default	Description
0.			DMC_DDR_LOCK. 1 LOCK DMC_DDR_CTRL, DMC_DDR_CTRL1, DMC_AXI2DDRx, DDR0/1_ADDRMAP_x registers. those register can't modified any more. 0:all these registers can be read/write by secure APB access.

DMC_DRAM_REG_BASE = 0xfe036400

Table 12-222 DMC_DRAM_TMRD 0x0000

Bit(s)	R/W	Default	Description
4:0			tMRD. //MR command cycles, in DDR3/4.in LPDDR4, it should be value of tMRW

Table 12-223 DMC_DRAM_TRFC 0x0001

Bit(s)	R/W	Default	Description
9:0			tRFC

Table 12-224 DMC_DRAM_TRP 0x0002

Bit(s)	R/W	Default	Description
21:16			tRP for precharge all banks.
5:0			tRP for precharge one bank.

Table 12-225 DMC_DRAM_TRTW 0x0003

Bit(s)	R/W	Default	Description
5:0			DDR3/4 mode : tRTW. For LPDDR4 . The total read command -> write command = (RL + BL/2 - tWODTON) + TDQSCK_MAX + tWPRE +RD(tRPST). tRTW = TDQSCK_max + tWPRE + tRD(tRPST) + (delay margin)

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Table 12-226 DMC_DRAM_TCL 0x0004

Bit(s)	R/W	Default	Description
5:0			tCL/tRL. read latency.

Table 12-227 DMC_DRAM_TCWL 0x0005

Bit(s)	R/W	Default	Description
5:0			CWL write latency.

Table 12-228 DMC_DRAM_TRAS 0x0006

Bit(s)	R/W	Default	Description
7:0			tRAS.minimum active to precharge time for same bank.

Table 12-229 DMC_DRAM_TRC 0x0007

Bit(s)	R/W	Default	Description
7:0			tRC.minimum active to active time for same bank.

Table 12-230 DMC_DRAM_TRCD 0x0008

Bit(s)	R/W	Default	Description
7:0			tRCDactive to read/write timing for same bank.

Table 12-231 DMC_DRAM_TRRD 0x0009

Bit(s)	R/W	Default	Description
21:16			tRRD_lactive bank A to active B in same band group for DDR4.
5:0			tRRD/tRRD_sactive bank A to active bank b time. tRRD_s: active bank A to active bank b in different bank groups for DDR4.

Table 12-232 DMC_DRAM_TFAW 0x000a

Bit(s)	R/W	Default	Description
8:0			tFAW.four active command windows

Table 12-233 DMC_DRAM_TRTP 0x000b

Bit(s)	R/W	Default	Description
5:0			tRTP.

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Table 12-234 DMC_DRAM_TWR 0x000c

Bit(s)	R/W	Default	Description
5:0			tWR.

Table 12-235 DMC_DRAM_TWTR 0x000d

Bit(s)	R/W	Default	Description
21:16			tWTR_l For DDR4 WTR_l. FOR DDR3/LPDDR4 same as tWTR_s.
5:0			tWTR.

Table 12-236 DMC_DRAM_TCCD 0x000e

Bit(s)	R/W	Default	Description
19:16			tCCD/tCCD_l.
3:0			tCCD/tCCD_s read to read command time or write to write command time.

Table 12-237 DMC_DRAM_TEXSR 0x000f

Bit(s)	R/W	Default	Description
12:0			tEXSR.EXIT SELF-REFRESH to read/write command.

Table 12-238 DMC_DRAM_TXS 0x0010

Bit(s)	R/W	Default	Description
9:0			tXS.EXIT SELF_REFRESH to other command time

Table 12-239 DMC_DRAM_TXP 0x0011

Bit(s)	R/W	Default	Description
3:0			tXP.EXIT power down to other command time

Table 12-240 DMC_DRAM_TXPDLL 0x0012

Bit(s)	R/W	Default	Description
12:0			tXPDLL,EXIT power down to read/write command time(need to relock PLL).

Table 12-241 DMC_DRAM_TZQCS 0x0013

Bit(s)	R/W	Default	Description
11:0			ZQCS command to other command time.

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Table 12-242 DMC_DRAM_TCKSRE 0x0014

Bit(s)	R/W	Default	Description
4:0			enter self refresh to disable clock time.

Table 12-243 DMC_DRAM_TCKSRX 0x0015

Bit(s)	R/W	Default	Description
4:0			enable clock to exit self refresh time.

Table 12-244 DMC_DRAM_TCKE 0x0016

Bit(s)	R/W	Default	Description
4:0			CKE high or low minimum time.

Table 12-245 DMC_DRAM_TMOD 0x0017

Bit(s)	R/W	Default	Description
4:0			tMOD.MRR/MRW to other command time. in LPDDR4, still use this register but it called tMRD.

Table 12-246 DMC_DRAM_TDQS 0x0018

Bit(s)	R/W	Default	Description
31:28			reserved
27:24			tDQS. the delay for write after read in different rank.
23:20			reserved
19:16			tDQS. the delay for read after write in different rank.
15:12			reserved
11:8			tDQS. the delay for write after write in different rank.
7:4			reserved
3:0			tDQS. the delay for read after read in different rank.

DMC_DRAM_TRSTL 0x0019

Not used.

Table 12-247 DMC_DRAM_TZQLAT 0x001a

Bit(s)	R/W	Default	Description
5:0			ZQ LATCH command to other command timing in LPDDR4 mode.

Table 12-248 DMC_DRAM_TMRR 0x001b

Bit(s)	R/W	Default	Description
7:0			tMRRnot used in DMC.

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Table 12-249 DMC_DRAM_TCKESR 0x001c

Bit(s)	R/W	Default	Description
9:0			tCKESR.CKE low minimum pulse in self refresh mode.

Table 12-250 DMC_DRAM_DFITCTRLDELAY 0x001e

Bit(s)	R/W	Default	Description
3:0			DFI_t_ctrldealy

Table 12-251 DMC_DRAM_DFITPHYWRDATA 0x001f

Bit(s)	R/W	Default	Description
5:0			dfi_t_phy_wrdata.

Table 12-252 DMC_DRAM_DFITPHYWRLAT 0x0020

Bit(s)	R/W	Default	Description
5:0			dfi_t_phy_wrlat.in DDR3/4/LPDDR3 mode WL -5 + 2.

Table 12-253 DMC_DRAM_DFITRDDATAEN 0x0021

Bit(s)	R/W	Default	Description
5:0			dfi_t_rddata_en.in DDR3/4/LPDDR3 mode

Table 12-254 DMC_DRAM_DFITPHYRDLAT 0x0022

Bit(s)	R/W	Default	Description
5:0			dfi_t_rdlat.

Table 12-255 DMC_DRAM_DFITCTRLUPDMIN 0x0023

Bit(s)	R/W	Default	Description
7:0			CTRLUPD_MINminimux clock cycle to maintain CTRLUPD_REQ.

Table 12-256 DMC_DRAM_DFITCTRLUPDMAX 0x0024

Bit(s)	R/W	Default	Description
7:0			CTRLUPD_MAX.maximum clock cycle to maintain CTRLUPD_REQ if no CTRLUPD_ACK response.

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Table 12-257 DMC_DRAM_DFITDRAMCLK 0x0028

Bit(s)	R/W	Default	Description
17			dram clk1 enable.
16			dram clk0 enable.
15:8			DRAM CLK disable waiting time
7:0			DRAM CLK enable timer

Table 12-258 DMC_DRAM_DFITLPRESP 0x002a

Bit(s)	R/W	Default	Description
3:0			dfi_lp_ctrl_req response time. after dfi_lp_ctrl_req asserted, and after response time if there's still no dfi_lp_ack respone, then drop the dfi_lp_ctrl_req.

Table 12-259 DMC_DRAM_TCKECK 0x002c

Bit(s)	R/W	Default	Description
4:0			tCKECKfrom CKE low to assert dfi_dram_clk_disable time. this time + dfi_t_ctrl_delay

Table 12-260 DMC_DRAM_TREFI 0x002d

Bit(s)	R/W	Default	Description
31:24			tZQCI dmc send zqci period.unit is how much auto refresh period.
23:16			pvtidmc send dfi_ctrlupd_req period.unit is one auto refresh period.
15:8			tREFI.dmc send auto refresh command period. unit is 100ns.
7:0			t100ns period. unit is dmc clock cycles

Table 12-261 DMC_DRAM_TSR 0x002e

Bit(s)	R/W	Default	Description
5:0			tSR.self refresh enter to exit time.

Table 12-262 DMC_DRAM_TCCDMW 0x002f

Bit(s)	R/W	Default	Description
5:0			4*tCCD in LPDDR4 mask write.

Table 12-263 DMC_DRAM_TESCKE 0x0030

Bit(s)	R/W	Default	Description
5:0			tESCKE.enter self refresh to power time for LPDDR4.

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Table 12-264 DMC_DRAM_TREFI_DDR3 0x0031

Bit(s)	R/W	Default	Description
7:0.			DDR3 SDRAM tREFI single auto refresh time . the unit is t100ns.

Table 12-265 DMC_DRAM_TZQCAL 0x0032

Bit(s)	R/W	Default	Description
11:0.			ZQCAL for LPDDR4. ZQINIT/ZQoper for DDR3/4 ZQCL command.

DMC_DRAM_T10US 0x0033

Table 12-266 DMC_DRAM_TMRRI 0x0034

Bit(s)	R/W	Default	Description
7:0			tMRRI for MRR

Table 12-267 DMC_DRAM_TXS_FAST 0x0035

Bit(s)	R/W	Default	Description
9:0			DDR4 mode XS_FAST exit self_refrest to zqcl/zqcs/mrs command.

Table 12-268 DMC_DRAM_DFIODTCFG 0x0036

Bit(s)	R/W	Default	Description
12.			rank1 ODT default. default vulue for ODT[1] pins if there’s no read/write activity.
11.			rank1 ODT write sel.enable ODT[1] if there's write occur in rank1.
10.			rank1 ODT write nsel. enable ODT[1] if there’s's write occur in rank0.
9.			rank1 odt read sel.enable ODT[1] if there's read occur in rank1.
8.			rank1 odt read nsel.enable ODT[1] if there's read occur in rank0.
4.			rank0 ODT default. default vulue for ODT[0] pins if there’s no read/write activity.
3.			rank0 ODT write sel.enable ODT[0] if there's write occur in rank0.
2.			rank0 ODT write nsel. enable ODT[0] if there's write occur in rank1.
1.			rank0 odt read sel.enable ODT[0] if there's read occur in rank0.
0.			rank0 odt read nsel.enable ODT[0] if there's read occur in rank1.

Table 12-269 DMC_DRAM_DFIODTCFG1 0x0037

Bit(s)	R/W	Default	Description
27:24			ODT length for BL8 read transfer.
19:16			ODT length for BL8 write transfer.
12:8			ODT latency for reads.suppose to be 0.
4:0			ODT latency for writes.suppose to be 0.

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Table 12-270 DMC_DRAM_TWODTON 0x0038

Bit(s)	R/W	Default	Description
5:0			DRAM write access ODT on time. In DDR3/4 should be same as WL In LPDDR4 ODT enable mode: tODTon + tODTon.min In LPDDR4 ODT disable mode. tWL.

Table 12-271 DMC_DRAM_TRETRAIN 0x0039

Bit(s)	R/W	Default	Description
15:0			LPDDR4 OSCRING retraining timer(units = auto_refresh timer). sync with autorefresh

Table 12-272 DMC_DRAM_PHYADDRON 0x003a

Bit(s)	R/W	Default	Description
5:0		12	PHY_CTRL_ADDR_ON for new PHY. default : 12 unit: DfiClk

Table 12-273 DMC_DRAM_PHYWRON 0x003b

Bit(s)	R/W	Default	Description
6:0			PHY_CTRL_WR _ON for new PHY. unit: ddr clk

Table 12-274 DMC_DRAM_PHYRDON 0x003c

Bit(s)	R/W	Default	Description
6:0			PHY_CTRL_RD_ON for new PHY. unit: ddr clk = 20 + RL + (tDQSCK+ tRPST + tDQSQ)/ddr_clk + BL/2

Table 12-275 DMC_DRAM_ZQCTRL 0x003d

Bit(s)	R/W	Default	Description
31:24.			in LPDDR4 case when to send ZQLAT command to both RANKs of LPDDR4 SDRAM
23:16.			when to send PHY ZQ UPDATE command.
15:8.			when to send ZQCS/ZQCAL to rank1 DDR SDRAM.
7:0.			when to senc ZQCS/ZQCAL to rank0 DDR SDRAM.

DMC_NFQ_TMRD 0x0040

DMC_NFQ_TRFC 0x0041

DMC_NFQ_TRP 0x0042

DMC_NFQ_TRTW 0x0043

DMC_NFQ_TCL 0x0044

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DMC_NFQ_TCWL 0x0045
DMC_NFQ_TRAS 0x0046
DMC_NFQ_TRC 0x0047
DMC_NFQ_TRCD 0x0048
DMC_NFQ_TRRD 0x0049
DMC_NFQ_TFAW 0x004a
DMC_NFQ_TRTP 0x004b
DMC_NFQ_TWR 0x004c
DMC_NFQ_TWTR 0x004d
DMC_NFQ_TCCD 0x004e
DMC_NFQ_TEXSR 0x004f
DMC_NFQ_TXS 0x0050
DMC_NFQ_TXP 0x0051
DMC_NFQ_TXPDLL 0x0052
DMC_NFQ_TZQCS 0x0053
DMC_NFQ_TCKSRE 0x0054
DMC_NFQ_TCKSRX 0x0055
DMC_NFQ_TCKE 0x0056
DMC_NFQ_TMOD 0x0057
DMC_NFQ_TDQS 0x0058
DMC_NFQ_TRSTL 0x0059
DMC_NFQ_TZQLAT 0x005a
DMC_NFQ_TMRR 0x005b
DMC_NFQ_TCKESR 0x005c
DMC_NFQ_TDPD 0x005d
DMC_NFQ_DFITCTRLDELAY 0x005e
DMC_NFQ_DFITPHYWRDATA 0x005f
DMC_NFQ_DFITPHYWRLAT 0x0060
DMC_NFQ_DFITRDDATAEN 0x0061
DMC_NFQ_DFITPHYRDLAT 0x0062
DMC_NFQ_DFITCTRLUPDMIN 0x0063
DMC_NFQ_DFITCTRLUPDMAX 0x0064
DMC_NFQ_DFITREFMSKI 0x0066
DMC_NFQ_DFITCTRLUPDI 0x0067
DMC_NFQ_DFITDRAMCLK 0x0068
DMC_NFQ_DFITLPRESP 0x006a
DMC_NFQ_TCKECK 0x006c
DMC_NFQ_TREFI 0x006d

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DMC_NFQ_TSR 0x006e

DMC_NFQ_TCCDMW 0x006f

DMC_NFQ_TESCKE 0x0070

DMC_NFQ_TREFI_DDR3 0x0071

DMC_NFQ_TZQCAL 0x0072

DMC_NFQ_T10US 0x0073

DMC_NFQ_TMRRI 0x0074

DMC_NFQ_TXS_FAST 0x0075

DMC_NFQ_DFIODTCFG 0x0076

DMC_NFQ_DFIODTCFG1 0x0077

DMC_NFQ_TWODTON 0x0078

DMC_NFQ_TRETRAIN 0x0079

DMC_NFQ_PHYADDRON 0x007a

DMC_NFQ_PHYWRON 0x007b

DMC_NFQ_PHYRDON 0x007c

DMC_NFQ_ZQCTRL 0x007d

DMC_DRAM_DFITPHYUPDTYPE0 0x0080

DMC_DRAM_DFITPHYUPDTYPE1 0x0081

DMC_DRAM_DFITPHYUPDTYPE2 0x0082

DMC_DRAM_DFITPHYUPDTYPE3 0x0083

Table 12-276 DMC_DRAM_MCFG 0x0086

Bit(s)	R/W	Default	Description
31:27			not used.
26:24			rank1_d16_sel. 16bit mode, rank 1 byte selection.
23			not used.
22:20			rank0_d16_sel. 16bit mode, rank 0 byte selection.
19			send PHY ZQ command after siu self refresh exit. 1 : enable. 0 : disable.
18			send retrain command after siu self refresh exit. 1 : enable. 0 : disable.
17.			in DDR3/4 mode, send ZQCL command after exit register triggered self refresh.
16.			send refresh command after finish frequency change. 1 disable.
15.			send refresh command after finish LPDDR4 retraining. 1 disable.
14.			1 cke init high.
13			1 dbi write enable only for LPDDR4.
12.			1 dbi read high inversion.
11.			1 dbi not enabled.
10			1 enable staggered chip select for 2 ranks DRAM.
9			1 enable send auto refresh command to DDR SDRAM when PCTL is in CFG/ STOP state.

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Bit(s)	R/W	Default	Description
8			send auto refr cmd before enter register triggered self refresh
7			send auto refr cmd after exit register triggered self refresh mode.
6			disable dram clock after enter register triggered self refresh.
5			send DFI_LP_REQ to PHY after enter register triggered elf refresh mode.
4			send DRAM to power down mode after enter self refresh. ONLY for LPDDR4.
3			send DFI_CTRLUPD_REQ after exit register triggered self refresh.
2			send ZQCS command after exit register triggered self refresh.
1			enable PHY triggered DFI_PHYUPD_REQ.
0			2T mode. always 1 in DDR3/4 mode.

Table 12-277 DMC_DRAM_ZQ_CTRL 0x0087

Bit(s)	R/W	Default	Description
2			ZQ command must be send in different time.
1			ZQ command can be send at same time.
0			rank0 ZQ only

Table 12-278 DMC_DRAM_DFI_CTRL 0x0089

Bit(s)	R/W	Default	Description
31			siu_dfi_lat err generation enable.1 disable.
20			phy_ctrl_rd_on phy_ctrl_wr_on ignore 16bit mode. 1: sending 0xf in 16bit mode. 0: sending valid byte enable in 16bit mode
19			dfi_init_complete wait enable. 1: after dfi_init_complete, wait additional EXSR time for new command. 0: phy will handle all the timing after dfi_init_complete DMC can do everything they want.
18			dfi_rddata_cs_n polariy. 0: rank0 select = 2'b10. rank1 select = 2'b10. 1: rank0 select = 2'b01, rank1_select = 2'b10.
17			dfi_wrdata_cs_n polariy. 0: rank0 select = 2'b10. rank1 select = 2'b10. 1: rank0 select = 2'b01, rank1_select = 2'b10.
16			force PHY ctrl_on if = 1, phy_ctrl_on singal will keep on.
15			siu_dfi1_lp_en
14			siu_dfi_lp_ack_and
13			siu_dfi_lp_ack_or
12			siu_dfi1_init_start_en
11			siu_dfi_init_com_and
10			siu_dfi_init_com_or
9			siu_dfi1_freq_en
8			siu_dfi1_dram_clk_dis_en

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Bit(s)	R/W	Default	Description
7			siu_dfi_phyupd_type_sel
6			siu_dfi1_phyupd_ack_en
5			siu_dfi_phyupd_req_and
4			siu_dfi_phyupd_req_or
3			siu_dfi_ctrlupd_ack_and
2			siu_dfi_ctrlupd_ack_or
1			siu_dfi1_ctrlupd_req_en
0			siu_dfi1_cmd_en

Table 12-279 DMC_DRAM_DFIINITCFG 0x008a

Bit(s)	R/W	Default	Description
31.			dfi_init_complete status. read only.
15:14			Frequency set 1 dfi_freq_ratio value.
12:8			Frequency set 1 dfi_freq value.
7:6			Frequency set 0 dfi_freq_ratio value.
5:1			Frequency set 0 dfi_freq value.
0.			dfi_init_start value can be use manually config dfi_init_start signal.

Table 12-280 DMC_DRAM_APD_CTRL 0x008c

Bit(s)	R/W	Default	Description
19:			16DFI_LP_WAKEUP value in APD DFI_LP_REQ mode
12			1 fast mode.
11			enable DFI_LP_REQ when enter Auto power down mode.
10			disable DFI_clk_disable when enter auto power down mode.
9:0			0 disable auto power down mode.

Table 12-281 DMC_DRAM_ASR_CTRL 0x008d

Bit(s)	R/W	Default	Description
31			enable RETRAIN PHY after auto self refresh exit. for AM_PHY only.
30.			in DDR3/4 mode, send ZQCL command after exit from auto self refresh mode.
29.			enable PHY clock in LP2 mode.1 disable.
28.			enable dmc wait 10us after LP2 mode exit if it's long time the PHY in LP2 mode.
27:			24 DFI_LP_WAKEUP value in self refresh DFI_LP_REQ mode.
23			send REFRESH command after exit from auto self refersh mode(ASR).
22			send REFERSH command before enter to Auto self refresh mode(ASR).

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Bit(s)	R/W	Default	Description
21			send ZQCS command after exit from Auto self refresh mode(ASR).
20			send dfi_ctrl_upd after exit from ASR mode
19			send power down command when enter ASR mode. //for LPDDR4 only.
18			set the PHY enter LP2 mode after enter ASR mode.
17			send DFI_LP_REQafter enter ASR mode.
16			set DFI_CLK_DISABLE after enter ASR mode.
15:			0.0 disable auto ASR mode.

Table 12-282 DMC_DRAM_REFR_CTRL 0x0092

Bit(s)	R/W	Default	Description
22			dmc to control DFI_CTRLUPD_REQ with zq generation together.
21			dmc to control PHY ZQ generation enable.
20			dmc to control zqlat(in LPDDR4 mode) generation enable.
19			dmc to control zqcs1 generation enable.
18			dmc to control zqcs0 generation enable.
17:8			auto refresh request pending cnt if there's page hit request.
7			retrain enable for auto refresh requent. 1: enable. 0: disable.
6			Disabled auto refresh command if over 16 auto refresh command sent in 2 TREFI_DDR3 period
5			enable dmc send ZQCS command .
4.			enable dmc send DFI_CTRUPD_REQ.
3:1			how many refresh command send for one period. = this number + 1
0.			enable dmc send auto refresh command.

Table 12-283 DMC_DRAM_FREQ_CTRL 0x0093

Bit(s)	R/W	Default	Description
31			write 1 to change frequency read 0: finished.
30			waiting for software to send some manual command. 1 : waiting. 0 : not ready yet.
29:22			not used.
21			after Freqchange send PHY ZQ update.
20			send CTRLUPD_REQ to PHY after freq_change finished.
19:16			how many cycles to send PLL change req after init_complete signal to low.
15.			freq pre config_en. Before freq enter stop state let DMC configure DDR SDRAM.
14.			freq post config_en. After freq enter stop state let DMC configure DDR SDRAM.
13.			send zqcl after freq change in DDR3/4 mode.

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Bit(s)	R/W	Default	Description
12.			send zqcs after freq change. 1 enable. 0 not send.
11.			in AUTO MRW function MRW format.
10.			AUTO MRW function don't do auto MRW.
9.			1 FREQ MRW done. let FREQ change machine continue.
8			FREQ WAIT. 1 when freq change finishes, state machine stop at self refresh state in case there's something need to handle. 0 after freq change finishes the state machine go back to access state.
7			when change PLL setting, disable dmc clock
6			when change PLL setting, disable PHY DfiClk and DfiCtlClk.
5			check vpu_sleep_en ==1 when do FREQ change.if vpu_sleep_en == 0, just wait.
4			nxt frequency selection.1 = freq1. 0 = freq0.
3:1			not used.
0.			current frequency selection.

Table 12-284 DMC_DRAM_SCFG 0x0094

Bit(s)	R/W	Default	Description
2			1 :to ask PCTL enter ACCESS STATE. 0 :deassert the request.
1			1 :to ask PCTL enter SELF REFRESH STATE. 0 :deassert the request.
0			1 :to ask PCTL enter STOP/CONFIG STATE . 0 :deassert the request.

Table 12-285 DMC_DRAM_STAT 0x0095

Bit(s)	R/W	Default	Description
31			rd latency error. 1 means after dfiphytrdlat cycles, the read data still not back.
28:24			dram_sr_state
23:20			stop_st
19:15			sleep_st
14:12			ACCESS STATUS 0 ACCESS is in normal working mode. 1 : ACCESS sending precharege command. 2 : ACCESS sending AUTO REFESH command. 3 : ACCESS sending DIF_CTRLUPD_REQ command. 4 : ACCESS sending ZQCS command to DDR DRAM(ZQCAL for LPDDR4). 5 : ACCESS sending ZQLATCH command to LPDDR4 only.
11:8			APD STATUS APD_IDLE 1 : APD sending PRECHARGE command 2 : APD sending CKE low command 3 : APD sending DISABLE DRAM CLOCK command 4 : APD sending DFI_LP_CTRL_REQ 5 : APD in Auto Power down mode. 6 : APD deassert DFI_LP_CTRL_REQ 7 : APD sending enable DRAM CLOCK command 8 : APD sending out CKE high command.
7:4			DRAM IDLE 1 : DRAM_STOP/DRAM_CFG 2 : DRAM_ACCESS

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Bit(s)	R/W	Default	Description
			3 : DRAM_SLEEP 4 : DRAM APD(AUTO POWER DOWN). 5 : IDLE -> STOP/CONFIG 6 : STOP -> SLEEP 7 : STOP -> ACCESS 8 : ACCESS -> SLEEP. 9 : ACCESS -> STOP A : ACCESS -> APD B : SLEEP -> STOP C : SLEEP -> ACCESS D : APD -> ACCESS
3			reserved.
2			1 DRAM enter normal working state.
1			1 DRAM enter sleep state. self refresh state.
0			1 dram enter cfg state.

Table 12-286 DMC_DRAM_STAT1 0x0096

Bit(s)	R/W	Default	Description
11:8			freq_st. 4'h0 : IDLE 4'h1 : FREQ_CHECK_VPU 4'h2 : FREQ_WAITING_STOP 4'h3 : FREQ_DRAM_CFG. waiting DMC/software to send special MRW/MPC command to configure DDR SDRAM either before Freq change or after freq change. 4'h4 : FREQ_SELF_REFR_ST. 4'h5 : FREQ_SET_DFI_FREQ. 4'h6 : FREQ_DFI_INIT_START_HIGH. 4'h7 : FREQ_CHANGE PLL_ST. 4'h8 : FREQ_UPDATA REG. 4'h9 : FREQ_DFI_INIT_START_LOW. 4'ha : FREQ_WAITING_FINISH 4'hb : FREQ_ZQCS 4'hc : FREQ_ZQ_LATCH 4'hd : FREQ_PVT
7:5			train_st
4:0			dram_phy_st

Table 12-287 DMC_PHY_RETRAINING_CTRL 0x0097

Bit(s)	R/W	Default	Description
31			phy_retraining enable.
30			checkvpu sleep_en.
25:24			retraining dfi_freq[4:3], the [2:0] bit still use the dfi_freq bits to keep the frequency.
23:0			retraining period unit :100ns.

Table 12-288 DMC_DFI_ERR_STAT 0x0098

Bit(s)	R/W	Default	Description
31:			20. not used.
9.			ddr0_dfi_error

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Bit(s)	R/W	Default	Description
8:5			ddr0_dfi_error_info.
4.			ddr1_dfi_error.
3:0			ddr1_dfi_error_info.

Table 12-289 DMC_LP2_TIMER 0x009a

Bit(s)	R/W	Default	Description
15:0			timer setting to measure how long the chip is entered LP2 mode.

DMC_DRAM_COMPLETE_WAIT 0x009b

read only how long to waiting for DFI_INIT_COMPLETE become high after DFI_INIT_START triggered.

Table 12-290 DMC_DRAM_DFI_SWAP_0 0x00a0

Bit(s)	R/W	Default	Description
5:0			dfi_act_n function select 6'h00 :the function itself. 6'h01 :act_n. 6'h02 :ras_n. 6'h03 :cas_n. 6'h04 :we_n. 6'h05 :bg[0]. 6'h06 :bg[1]. 6'h07 :ba[0]. 6'h08 :ba[1]. 6'h09 :ba[2]. 6'h0a :a[0]. 6'h0b :a[1]. 6'h0c :a[2]. 6'h0d :a[3]. 6'h0e :a[4]. 6'h0f :a[5]. 6'h10 :a[6]. 6'h11 :a[7]. 6'h12 :a[8]. 6'h13 :a[9]. 6'h14 :a[10]. 6'h15 :a[11]. 6'h16 :a[12]. 6'h17 :a[13]. 6'h18 :a[14]. 6'h19 :a[15]. 6'h1a :a[16]. 6'h1b :a[17].

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Table 12-291 DMC_DRAM_DFI_SWAP_1 0x00a1

Bit(s)	R/W	Default	Description
5:0			dfi_ras_n function select 6'h00 :the function itself 6'h01 :act_n. 6'h02 :ras_n. 6'h03 :cas_n. 6'h04 :we_n. 6'h05 :bg[0]. 6'h06 :bg[1]. 6'h07 :ba[0]. 6'h08 :ba[1]. 6'h09 :ba[2]. 6'h0a :a[0]. 6'h0b :a[1]. 6'h0c :a[2]. 6'h0d :a[3]. 6'h0e :a[4]. 6'h0f :a[5]. 6'h10 :a[6]. 6'h11 :a[7]. 6'h12 :a[8]. 6'h13 :a[9]. 6'h14 :a[10]. 6'h15 :a[11]. 6'h16 :a[12]. 6'h17 :a[13]. 6'h18 :a[14]. 6'h19 :a[15]. 6'h1a :a[16]. 6'h1b :a[17].

Table 12-292 DMC_DRAM_DFI_SWAP_2 0x00a2

Bit(s)	R/W	Default	Description
5:0			dfi_cas_n function select 6'h00 :the function itself. 6'h01 :act_n. 6'h02 :ras_n. 6'h03 :cas_n. 6'h04 :we_n. 6'h05 :bg[0]. 6'h06 :bg[1]. 6'h07 :ba[0]. 6'h08 :ba[1]. 6'h09 :ba[2]. 6'h0a :a[0]. 6'h0b :a[1]. 6'h0c :a[2]. 6'h0d :a[3]. 6'h0e :a[4]. 6'h0f :a[5]. 6'h10 :a[6]. 6'h11 :a[7]. 6'h12 :a[8]. 6'h13 :a[9]. 6'h14 :a[10]. 6'h15 :a[11]. 6'h16 :a[12]. 6'h17 :a[13]. 6'h18 :a[14]. 6'h19 :a[15]. 6'h1a :a[16]. 6'h1b :a[17].

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Table 12-293 DMC_DRAM_DFI_SWAP_3 0x00a3

Bit(s)	R/W	Default	Description
5:0			dfi_we_n function select 6'h00 :the function itself. 6'h01 :act_n. 6'h02 :ras_n. 6'h03 :cas_n. 6'h04 :we_n. 6'h05 :bg[0]. 6'h06 :bg[1]. 6'h07 :ba[0]. 6'h08 :ba[1]. 6'h09 :ba[2]. 6'h0a :a[0]. 6'h0b :a[1]. 6'h0c :a[2]. 6'h0d :a[3]. 6'h0e :a[4]. 6'h0f :a[5]. 6'h10 :a[6]. 6'h11 :a[7]. 6'h12 :a[8]. 6'h13 :a[9]. 6'h14 :a[10]. 6'h15 :a[11]. 6'h16 :a[12]. 6'h17 :a[13]. 6'h18 :a[14]. 6'h19 :a[15]. 6'h1a :a[16]. 6'h1b :a[17].

Table 12-294 DMC_DRAM_DFI_SWAP_4 0x00a4

Bit(s)	R/W	Default	Description
5:0			dfi_bg0 function select 6'h00 :the function itself. 6'h01 :act_n. 6'h02 :ras_n. 6'h03 :cas_n. 6'h04 :we_n. 6'h05 :bg[0]. 6'h06 :bg[1]. 6'h07 :ba[0]. 6'h08 :ba[1]. 6'h09 :ba[2]. 6'h0a :a[0]. 6'h0b :a[1]. 6'h0c :a[2]. 6'h0d :a[3]. 6'h0e :a[4]. 6'h0f :a[5]. 6'h10 :a[6]. 6'h11 :a[7]. 6'h12 :a[8]. 6'h13 :a[9]. 6'h14 :a[10]. 6'h15 :a[11]. 6'h16 :a[12]. 6'h17 :a[13]. 6'h18 :a[14]. 6'h19 :a[15]. 6'h1a :a[16]. 6'h1b :a[17].

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Table 12-295 DMC_DRAM_DFI_SWAP_5 0x00a5

Bit(s)	R/W	Default	Description
5:0			dfi_bg[1] function select 6'h00 :the function itself. 6'h01 :act_n. 6'h02 :ras_n. 6'h03 :cas_n. 6'h04 :we_n. 6'h05 :bg[0]. 6'h06 :bg[1]. 6'h07 :ba[0]. 6'h08 :ba[1]. 6'h09 :ba[2]. 6'h0a :a[0]. 6'h0b :a[1]. 6'h0c :a[2]. 6'h0d :a[3]. 6'h0e :a[4]. 6'h0f :a[5]. 6'h10 :a[6]. 6'h11 :a[7]. 6'h12 :a[8]. 6'h13 :a[9]. 6'h14 :a[10]. 6'h15 :a[11]. 6'h16 :a[12]. 6'h17 :a[13]. 6'h18 :a[14]. 6'h19 :a[15]. 6'h1a :a[16]. 6'h1b :a[17].

Table 12-296 DMC_DRAM_DFI_SWAP_6 0x00a6

Bit(s)	R/W	Default	Description
5:0			dfi_ba[0] function select 6'h00 :the function itself. 6'h01 :act_n. 6'h02 :ras_n. 6'h03 :cas_n. 6'h04 :we_n. 6'h05 :bg[0]. 6'h06 :bg[1]. 6'h07 :ba[0]. 6'h08 :ba[1]. 6'h09 :ba[2]. 6'h0a :a[0]. 6'h0b :a[1]. 6'h0c :a[2]. 6'h0d :a[3]. 6'h0e :a[4]. 6'h0f :a[5]. 6'h10 :a[6]. 6'h11 :a[7]. 6'h12 :a[8]. 6'h13 :a[9]. 6'h14 :a[10]. 6'h15 :a[11]. 6'h16 :a[12]. 6'h17 :a[13]. 6'h18 :a[14]. 6'h19 :a[15]. 6'h1a :a[16]. 6'h1b :a[17].

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Table 12-297 DMC_DRAM_DFI_SWAP_7 0x00a7

Bit(s)	R/W	Default	Description
5:0			dfi_ba[1] function select 6'h00 :the function itself. 6'h01 :act_n. 6'h02 :ras_n. 6'h03 :cas_n. 6'h04 :we_n. 6'h05 :bg[0]. 6'h06 :bg[1]. 6'h07 :ba[0]. 6'h08 :ba[1]. 6'h09 :ba[2]. 6'h0a :a[0]. 6'h0b :a[1]. 6'h0c :a[2]. 6'h0d :a[3]. 6'h0e :a[4]. 6'h0f :a[5]. 6'h10 :a[6]. 6'h11 :a[7]. 6'h12 :a[8]. 6'h13 :a[9]. 6'h14 :a[10]. 6'h15 :a[11]. 6'h16 :a[12]. 6'h17 :a[13]. 6'h18 :a[14]. 6'h19 :a[15]. 6'h1a :a[16]. 6'h1b :a[17].

Table 12-298 DMC_DRAM_DFI_SWAP_8 0x00a8

Bit(s)	R/W	Default	Description
5:0			dfi_ba[2] function select 6'h00 :the function itself. 6'h01 :act_n. 6'h02 :ras_n. 6'h03 :cas_n. 6'h04 :we_n. 6'h05 :bg[0]. 6'h06 :bg[1]. 6'h07 :ba[0]. 6'h08 :ba[1]. 6'h09 :ba[2]. 6'h0a :a[0]. 6'h0b :a[1]. 6'h0c :a[2]. 6'h0d :a[3]. 6'h0e :a[4]. 6'h0f :a[5]. 6'h10 :a[6]. 6'h11 :a[7]. 6'h12 :a[8]. 6'h13 :a[9]. 6'h14 :a[10]. 6'h15 :a[11]. 6'h16 :a[12]. 6'h17 :a[13]. 6'h18 :a[14]. 6'h19 :a[15]. 6'h1a :a[16]. 6'h1b :a[17].

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Table 12-299 DMC_DRAM_DFI_SWAP_9 0x00a9

Bit(s)	R/W	Default	Description
5:0			dfi_a[0] function select 6'h00 :the function itself. 6'h01 :act_n. 6'h02 :ras_n. 6'h03 :cas_n. 6'h04 :we_n. 6'h05 :bg[0]. 6'h06 :bg[1]. 6'h07 :ba[0]. 6'h08 :ba[1]. 6'h09 :ba[2]. 6'h0a :a[0]. 6'h0b :a[1]. 6'h0c :a[2]. 6'h0d :a[3]. 6'h0e :a[4]. 6'h0f :a[5]. 6'h10 :a[6]. 6'h11 :a[7]. 6'h12 :a[8]. 6'h13 :a[9]. 6'h14 :a[10]. 6'h15 :a[11]. 6'h16 :a[12]. 6'h17 :a[13]. 6'h18 :a[14]. 6'h19 :a[15]. 6'h1a :a[16]. 6'h1b :a[17].

Table 12-300 DMC_DRAM_DFI_SWAP_10 0x00aa

Bit(s)	R/W	Default	Description
5:0			dfi_a[1] function select

Table 12-301 DMC_DRAM_DFI_SWAP_11 0x00ab

Bit(s)	R/W	Default	Description
5:0			dfi_a[2] function select

Table 12-302 DMC_DRAM_DFI_SWAP_12 0x00ac

Bit(s)	R/W	Default	Description
5:0			dfi_a[3] function select

Table 12-303 DMC_DRAM_DFI_SWAP_13 0x00ad

Bit(s)	R/W	Default	Description
5:0			dfi_a[4] function select

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Table 12-304 DMC_DRAM_DFI_SWAP_14 0x00ae

Bit(s)	R/W	Default	Description
5:0			dfi_a[5] function select

Table 12-305 DMC_DRAM_DFI_SWAP_15 0x00af

Bit(s)	R/W	Default	Description
5:0			dfi_a[6] function select

Table 12-306 DMC_DRAM_DFI_SWAP_16 0x00b0

Bit(s)	R/W	Default	Description
5:0			dfi_a[7] function select

Table 12-307 DMC_DRAM_DFI_SWAP_17 0x00b1

Bit(s)	R/W	Default	Description
5:0	DMC_ SEC_		dfi_a[8] function select

Table 12-308 DMC_DRAM_DFI_SWAP_18 0x00b2

Bit(s)	R/W	Default	Description
5:0			dfi_a[9] function select

Table 12-309 DMC_DRAM_DFI_SWAP_19 0x00b3

Bit(s)	R/W	Default	Description
5:0			dfi_a[10] function select

Table 12-310 DMC_DRAM_DFI_SWAP_20 0x00b4

Bit(s)	R/W	Default	Description
5:0			dfi_a[11] function select

Table 12-311 DMC_DRAM_DFI_SWAP_21 0x00b5

Bit(s)	R/W	Default	Description
5:0			dfi_a[12] function select

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Table 12-312 DMC_DRAM_DFI_SWAP_22 0x00b6

Bit(s)	R/W	Default	Description
5:0			dfi_a[13] function select

Table 12-313 DMC_DRAM_DFI_SWAP_23 0x00b7

Bit(s)	R/W	Default	Description
5:0			dfi_a[14] function select

Table 12-314 DMC_DRAM_DFI_SWAP_24 0x00b8

Bit(s)	R/W	Default	Description
5:0			dfi_a[15] function select

Table 12-315 DMC_DRAM_DFI_SWAP_25 0x00b9

Bit(s)	R/W	Default	Description
5:0			dfi_a[16] function select

Table 12-316 DMC_DRAM_DFI_SWAP_26 0x00ba

Bit(s)	R/W	Default	Description
5:0			dfi_a[17] function select

Table 12-317 DMC_DRAM_CMD 0x00d0

Bit(s)	R/W	Default	Description
31.			cmd done.write 0 to clean.
30.			data done. write 0 to clean.
5.			user defined command.
4.			LPDDR4 MPC write data command(MPC WR FIFO).
3.			LPDDR4 MPC read data command (MPC RD Calibration and RD FIFO).
2.			LPDDR4 MPC-1 command (NOP,Start DQS interval.....)
1.			mrr command.
0.			mrw command.

Table 12-318 DMC_DRAM_CMD_CODE 0x00d1

Bit(s)	R/W	Default	Description
31:28			user command case = {act_n, ras_n, cas_n, we_n}
27:26.			128bits data cycles . 0:1 clock cycles; 1:2 clock cycles; 2:3 clock cycles; 3:4 clock cycles. LPDDR4 : 4 clock cycles; DDR3/4/LPDDR3: 2 clock cycles.

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Bit(s)	R/W	Default	Description
25			MRW/MRR/MPC command rank 1 select. 1:select. 0:not select.
24.			MRW/MRR/MPC command rank 0 select. 1:select. 0:not select.
23:16			MR addr. DDR4 case : 18:16 ba[2:0]. 20:19 BG[1:0].
15:0			opcode.

Table 12-319 DMC_DRAM_CMD_TIME 0x00d2

Bit(s)	R/W	Default	Description
31:16			PRECMD timer. //delay how many cycle to start the command.
15:0			POST CMD timer//delay how many cycle after the command execute.

DMC_DRA

M_WSTRB0

0x00d3

DMC_DRA

M_WSTRB1

0x00d4

Table 12-320 DMC_DRAM_RDBI0 0x00d5

Bit(s)	R/W	Default	Description
31:16			the second cycle.
15:0			the first cycle.

Table 12-321 DMC_DRAM_RDBI1 0x00d6

Bit(s)	R/W	Default	Description
31:16			the Forth cycle.
15:0			the third cycle.

DMC_DRAM_WDx and DMC_DRAM_RDx can be used as MRW command as Frequency change . DMC_DRAM_WDx is for Freq1 DRAM MR setting, it would send to DRAM right before FREQ0-> FREQ1 DMC_DRAM_RDx is for Freq0 DRAM MR setting. it would send to DRAM right before FREQ1-> FREQ0. One register can be one MRW command. So total 16 MRW command can be sent to DRAM. //The register formats as defined for MRW command:

Bit(s)	R/W	Default	Description
31			MRW/USER comand enable. 1: enabled command. 0 not enabled.
30			Last MRW/USER command. if this bit =1, After send this command, the DRAM controller will continue to frequency next stage.
29:26			SER COMMAND parameter: in DDR3/DDR4. {act_n, ras_n, cas_n, we_n} value for user command

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Bit(s)	R/W	Default	Description
			//in LPDDR4. bit 16: 1 4 cycles command. 0 2 cycles command.
25		0	MRW/USER command rank 1 select. 1: select. 0: not select.
24		0	MRW/USER command rank 0 select. 1: select. 0: not select.

23:0		0x5	USER command.
			//DDR3: 18:16 bank address. 15:0: address.
			//DDR4: 20:19 bank group address. 18:16: bank address. 15:0 address.
			//LPDDR3: 9:0. rising edge address. 19:10. falling edge address.
			//LPDDR4. 5:0, first edge address, 11:6 second edge address, 17:12: third edge address. 23:18, forth edge address.
			//MRW command format:
			//bit 23:16 MR addr. DDR4 case : 18:16 ba[2:0]. 20:19 BG[1:0].
			//bit 15:0 opcode

DMC_DRAM_WD0 0x00e0

DMC_DRAM_WD1 0x00e1

DMC_DRAM_WD2 0x00e2

DMC_DRAM_WD3 0x00e3

DMC_DRAM_WD4 0x00e4

DMC_DRAM_WD5 0x00e5

DMC_DRAM_WD6 0x00e6

DMC_DRAM_WD7 0x00e7

DMC_DRAM_WD8 0x00e8

DMC_DRAM_WD9 0x00e9

DMC_DRAM_WD10 0x00ea

DMC_DRAM_WD11 0x00eb

DMC_DRAM_WD12 0x00ec

DMC_DRAM_WD13 0x00ed

DMC_DRAM_WD14 0x00ee

DMC_DRAM_WD15 0x00ef

DMC_DRAM_RD0 0x00f0

DMC_DRAM_RD1 0x00f1

DMC_DRAM_RD2 0x00f2

DMC_DRAM_RD3 0x00f3

DMC_DRAM_RD4 0x00f4

DMC_DRAM_RD5 0x00f5

DMC_DRAM_RD6 0x00f6

DMC_DRAM_RD7 0x00f7

DMC_DRAM_RD8 0x00f8

DMC_DRAM_RD9 0x00f9

DMC_DRAM_RD10 0x00fa

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DMC_DRAM_RD11 0x00fb
DMC_DRAM_RD12 0x00fc
DMC_DRAM_RD13 0x00fd
DMC_DRAM_RD14 0x00fe
DMC_DRAM_RD15 0x00ff
REG_BASE: DMC_STICKY_REG_BASE = 0xfe036800
DMC_STICKY_0 0x0000
DMC_STICKY_1 0x0001
DMC_STICKY_2 0x0002
DMC_STICKY_3 0x0003
DMC_STICKY_4 0x0004
DMC_STICKY_5 0x0005
DMC_STICKY_6 0x0006
DMC_STICKY_7 0x0007
DMC_STICKY_8 0x0008
DMC_STICKY_9 0x0009
DMC_STICKY_10 0x000a
DMC_STICKY_11 0x000b
DMC_STICKY_12 0x000c
DMC_STICKY_13 0x000d
DMC_STICKY_14 0x000e
DMC_STICKY_15 0x000f
DMC_STICKY_16 0x0010
DMC_STICKY_17 0x0011
DMC_STICKY_18 0x0012
DMC_STICKY_19 0x0013
DMC_STICKY_20 0x0014
DMC_STICKY_21 0x0015
DMC_STICKY_22 0x0016
DMC_STICKY_23 0x0017
DMC_STICKY_24 0x0018
DMC_STICKY_25 0x0019
DMC_STICKY_26 0x001a
DMC_STICKY_27 0x001b
DMC_STICKY_28 0x001c
DMC_STICKY_29 0x001d
DMC_STICKY_30 0x001e
DMC_STICKY_31 0x001f

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DMC_STICKY_32 0x0020
DMC_STICKY_33 0x0021
DMC_STICKY_34 0x0022
DMC_STICKY_35 0x0023
DMC_STICKY_36 0x0024
DMC_STICKY_37 0x0025
DMC_STICKY_38 0x0026
DMC_STICKY_39 0x0027
DMC_STICKY_40 0x0028
DMC_STICKY_41 0x0029
DMC_STICKY_42 0x002a
DMC_STICKY_43 0x002b
DMC_STICKY_44 0x002c
DMC_STICKY_45 0x002d
DMC_STICKY_46 0x002e
DMC_STICKY_47 0x002f
DMC_STICKY_48 0x0030
DMC_STICKY_49 0x0031
DMC_STICKY_50 0x0032
DMC_STICKY_51 0x0033
DMC_STICKY_52 0x0034
DMC_STICKY_53 0x0035
DMC_STICKY_54 0x0036
DMC_STICKY_55 0x0037
DMC_STICKY_56 0x0038
DMC_STICKY_57 0x0039
DMC_STICKY_58 0x003a
DMC_STICKY_59 0x003b
DMC_STICKY_60 0x003c
DMC_STICKY_61 0x003d
DMC_STICKY_62 0x003e
DMC_STICKY_63 0x003f

12.2 NAND

12.2.1 Overview

This part describe the SOC’s SLC/MLC/TLC NAND Flash with 60-bit ECC.

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12.2.2 Features

The features of SPI NAND are as follows.

- Industry-standard serial peripheral interface.
- Internal ECC parity(BCH-8/BCH-4).
- Density: 1Gbit/2GBits/4Gbits
- 2x/4x bus mode supported

12.2.3 Descriptor Commands

Command “Standby”

All CEs are high, all other signals are “don’t care”, the bits [9:0] specify how many extra NAND cycles the controller stays in “standby”, if the number is “0”, only one NAND cycle, if the number is 10, the controller will stay in “standby” for 11 NAND cycles.

Command “Idle”

CE is low, ALE and CLE is low, WE and RE is high, the NAND bus is taken over by controller, but the bus is let to idle for one NAND cycle, if extra NAND cycles number is set, then extra NAND cycles is idled, useful when NAND controller needs time to switch to another mode, or wait for RB.

Command “Command”

NAND command is sent, CE is low, ALE is low, CLE is high, WE is low and RE is high, usually only one NAND CE is low, all the other 3 should be high, otherwise the NAND command is accepted by multiple Dies and may cause conflict problem, but it is fine when used to reset the NAND, the command itself is sent by bit 7 to bit 0, one command sends one NAND command.

Command “Address”

NAND address cycle, the CE is low, ALE is high, CLE is low, WE is low and RE is high. Usually only one NAND CE is low, all the other 3 CEs should be high. The address is sent in the bit 7 to bit 0, it lasts one NAND cycle.

Command “Data to NAND”

Write NAND bus directly by this command, CE is low, ALE and CLE are low, WE is low and RE is high, the low bit7 to bit 0 is write to NAND flash when this command is done, it lasts one NAND command cycle. Usually used to program NAND features, it is very low efficient to program NAND by this command, could be used to debug NAND flash software.

Command “NAND to Data”

Read NAND bus and save the data to registers, CE is low, ALE and CLE are low, WE is high and RE is low, the NAND output is locked in registers at perfect timing, the extra NAND cycles will make this command repeats extra NAND cycle, if it is “0”, only one byte is locked in registers, since the registers used to lock the data is only 32 bits, extra NAND cycles number larger than 3 will cause the data overflow. This command is used to read status and features from NAND, not for read NAND data, it is very low efficient to read NAND by this command, it could be used to debug NAND software.

Command “Sync Read”

Same as “NAND to Data”, used in synchronous mode, each NAND cycle will read in two bytes in synchronous mode.

Command “RB pin”

Hardware ready/busy detect with timer and interrupt, the timer is bit 4 to bit 0, it is power of 2 NAND cycle, for example, if timer is set to 10, then 2^10 or 1024 NAND cycles is set to timer out the RB

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command. The maximum setting is 31, that is 2^31 NAND cycles. Or 42 seconds when NAND cycle is 20 ns. When the RB waiting is timed out, the hardware is still in “waiting”, an interrupt is sent to CPU, the “RB” command can be programmed to send out interrupt when RB is high when the correspond INT bits is set to high, once RB is high, the command queue advanced to next command, no matter interrupt or not, interrupt setting is “one time setting”, it means one RB command can be programmed with interrupt, the next can be programmed without interrupt. There are few bits in the RB command for software debugging purpose. it can be set to different numbers to tell which RB command is interrupted. CPU can read out the NAND status registers to tell which RB causes interrupt.

Command “RB IO”

Assume the NAND controller is used without ready/busy pin, the ready/busy is checked through status register, This command should be used with NAND read status command, like the old RB command, this command is designed with option to check which IO bits as ready/busy, “IO6”, “IO5” and “IO4”, and “INT6”, “INT5” and “INT4” to issue “IRQ” if “Ready”, time out logic is the same as old RB, in case of “Read” NAND, an extra “0x00” command is needed to switch NAND flash back to “Read” mode.

The RB IO command is associated with CE state, there is no CE option in RB IO command, valid CE from previous command is used.

NAND status is checked every 16 NAND cycles, if not ready when time out, an “IRQ” is issued and timer is reset.

Change to read status mode.

Set proper timer out parameter.

Monitor which IO bits, IO6, IO5 or IO4.

Set IRQ option, set NAND_CFG cmd_irq_en bit.

Return back to read mode if needed.

Command “MEM to NAND”

DMA command to send data from memory to NAND, this command consist of ECC mode, the data is read from DDR memory by NAND controller at 64 bits/system cycle, BCH encoded by hardware and sent to NAND in the fly. The NAND data address can be programmed by register or command “set address”.

The data size can be any number, if ECC is off, the exact number of data bytes are read from DDR memory and sent to NAND without ECC encode, if ECC is on, and final page is not 512 bytes, then “0xff” is appended to the data to make it 512 bytes and send to BCH encoded and send to NAND.

When ECC is off, no spare data bytes are read from DDR, the data is sent exactly the same as DDR. When ECC is on, 2/16/0 bytes of spare bytes are read from DDR and appended to 512/1024 main data, encoded and parity bytes all sent to NAND.

The final BCH code word is rounded to integer number of bytes, see BCH table.

If ECC is OFF, the command writes [13:0] number of bytes to NAND.

If ECC is ON, the command writes “pages” of bytes to NAND.

If “short” is 0, the page size is BCH code data size, 512 or 1024.

If “short” is 1, shortened BCH mode, the page size is “page size”*8 bytes.

The number of pages is up to 63.

Data randomization option, if cmd[19] is set to “1” and the random seed is not equal to “0”, the data and parity written to NAND is randomized with PRBS random number, the same seed must be used to read the page back.

Random seed is set by command “Seed” cmd[14:0], suggest to use NAND physical address as “seed”.

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Command “NAND to MEM”

DMA command to read data from NAND and save to DDR, this command consist of ECC mode, and data size, this command will correct the data by hardware and save the decode result information to DDR too. The data address in DDR is programmed by “set address” command, if not programmed the address increases to next available data space.

When ECC is off, the data is save to DDR without change, the information bytes is also saved in DDR with ECC mode bits off, no spare bytes, when ECC is on, the data is BCH decoded and corrected by hardware, if the data size is less than 512/1024, more data will be read out from NAND, but only the required number of bytes are sent to DDR.

If ECC is OFF, the command reads [13:0] number of bytes from NAND.

If ECC is ON, the command reads “pages” of bytes to NAND.

If “short” is 0, the page size is BCH code data size, 512 or 1024.

If “short” is 1, shortened BCH mode, the page size is “page size”*8 bytes.

The number of pages is up to 63.

Data randomization option is the same as “MEM to NAND”.

Command “Set Address”

DDR address setup command, used to change the memory address when read or write NAND, the D/S bits is for data or spare, “0” for data, “1” for spare, L/H is for low and high 16 bits of address, “0” for low 16 bits, “1” for high 16 bits, the DDR address is 32 bits.

This command has nothing to do with NAND bus, but it will take one NAND command to execute, one NAND idle command is used in time.

Mode	Cmd[18:17]	Description
Data	00	Set Data Address
Info	01	Set Info Address
Status	10	Set Status Address

Command “STS”

Read status and save to DDR memory, the status registers is 32 bits, with

Field	Name	Description
15:0	Sts	Status
23:16	Sts counter	Sequence number
31	Done	This status is valid.

STS 1: read status once, without IRQ.

STS 2: read status twice, with IRQ.

If NAND_CFG[20] Sts_irq_en is set to “1”, the STS 2 command will issue an IRQ to system, if used after NAND read command “N2M”, it guarantees the DMA is done. Because the STS itself is a DMA command, it will wait till the previous DMA command done before its DMA.

STS 2 command resets the sequence number, the sequence number in itself is the number of STS 1’s before IRQ, wrap around to 8 bits.

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Command “Set Seed”

Random seed for data randomizer, any number except 0 starts random number generator, if “N2M” or “M2N” random bit is set, the random number is XORed with data.

Set none zero random seed, in cmd[14:0].

Set cmd[19] of “N2M” or “M2N” to 1, enable scrambler.

Use same seed to program/read the same NAND page.

12.2.4 Register Description

The base address of NAND registers is 0xffe07000, and the final address of each register is listed below.

Table 12-322 NAND Register List

Register Name	Description	Address	R/W
P_NAND_CMD	Write Command and Read Status	Base + 0x00	R/W
P_NAND_CFG	Configuration	Base + 0x04	R/W
P_NAND_DADR	Data Address	Base + 0x08	R/W
P_NAND_IADR	Information Address	Base + 0x0c	R/W
P_NAND_BUF	Read Data Buffer	Base + 0x10	R
P_NAND_INFO	Information	Base + 0x14	R
P_NAND_DC	DDR interface	Base + 0x18	R
P_NAND_ADR	DDR Address	Base + 0x1c	R
P_NAND_DL	DDR Low 32 Bits Data	Base + 0x20	R/W
P_NAND_DH	DDR High 32 Bits Data	Base + 0x24	R/W
P_NAND_CADR	Command Queus Address	Base + 0x28	R/W
P_NAND_SADR	Status Address	Base + 0x2c	R/W
P_NAND_PINS	CS2: SDRAM/NAND pin sharing	Base + 0x30	R/W
P_NAND_VER	Version number	Base + 0x38	R

P_NAND_CMD

Write : Send NAND command to controller, the command format is specified in previous section.

Bit(s)	Name	Description
21:0	Cmd	NAND command sent to NAND queue buffer
30	Cmd_go	When 1, and NAND bus is in waiting Rb mode, due to time out or longer than expected Rb waiting, the command queue will move on by disable RB waiting in current command.
31	Cmd_reset	When 1 the NAND command queue buffer is reset to zero.

Read : Read NAND controller status

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Bit(s)	Name	Description
19:0	Cmd_curr	NAND command current on NAND bus, still going, not finished.
24:20	Cmd_cnt	Number of NAND commands still in NAND command queue buffer, the buffer size is 32.
25	Timer out	When 1 wait Rb command timed out.
26	Rb0	Current Rb0 status, 1: ready, 0: busy.
27	Rb1	Current Rb1 status, 1: ready, 0: busy.
28	Rb2	Current Rb2 status, 1: ready, 0: busy.
29	Rb3	Current Rb3 status, 1: ready, 0: busy.
30	Mem_rdy	When 1, DDR interface is idle and ready to accept memory movement request.
31	Ecc_rdy	When 1, ECC BCH encoder/decoder is idle and read to accept encode or decode activity.

P_NAND_CFG

Bit(s)	Name	Description
4:0	Bus_cyc	The number of system clock cycles in one NAND cycle – 1, for example, if the bus_cyc is 3, then the NAND cycle is 4 system clock cycles, the minimum setting is 3, the maximum setting is 31. program this register according NAND timing mode.
9:5	Bus_tim	The timing to lock the NAND data when read NAND data or status, please refer to “Timing Calculator” for details.
11:10	Sync	00: Async mode 01: Micron Sync mode 10: Toshiba-Samsung toggle mode
12	Cmd_start	When set to “1”, if the NAND controller internal 32 command buffer has less than 16 commands, the command DMA starts reading commands from DDR and saves them to internal buffer, the DMA keeps watching the internal buffer, reads whenever there are less than 16 commands left, if an all “zero” command is met, This bit is cleared and current command DMA is done.
13	Cmd_auto	When set to ‘1’, the command DMA will check the previous command queue end location, whether it is changed from all “zero” back to valid command, the auto check period is 1 ms.
14	Apb_mode	Special NAND mode for ROM boot or debug, when 1, DDR interface is redirected to APB register, all the read/write activities are through APB registers. When used in ROM boot and DDR is not ready.
15	Spare_only	When 1, the NAND controller read NAND with/without ECC, but only save the information bytes into DDR memory, the main data is discarded, designed for software to survey the NAND flash spare bytes and prepare NAND programming.
16	Sync_adj	Used to adjust data timing in sync or toggle mode, 0: default timing, 1: delay 1 system clock cycle.
20	Sts_irq_en	Enable STS IRQ.
21	Cmd_irq_en	Enable RB pin or RB IO IRQ.
26	Oob_on	Set to 1 oob_mode 16/0, Set to 0 no oob bytes.
27	Oob_mode	New in M8 v2,

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Bit(s)	Name	Description
		Set to 1 enable new oob mode. First page 16 bytes, all other pages 0 byte.
28	Dc_ugt	Set NAND controller DDR interface to Urgent mode.
29	Nand_wpn	When 1, the NAND wpn pin is set to low, the NAND is in write protection mode, default to 0, the NAND is not protected.
30	Core_power	When 1, internal NAND controller core clock gating is override to always on. The clock gating is disabled.
31	Top_power	When 1, internal NAND top clock gating is override to always on, the clock gating for top is disabled.

P_NAND_DADR

Set DDR data address by registers, the address is 32 Bits, since the DDR data address can also be set by NAND commands, when both happens at the same time, register setting is ignored, the NAND command setting takes effect. Software should avoid conflict address setting.

P_NAND_IADR

Set DDR information (spare bytes) address by registers, the address is 32 Bits, since the DDR information address can also be set by NAND commands, when both happens at the same time, register setting is ignored, the NAND command setting takes effect. Software should avoid conflict address setting.

P_NAND_BUF

When read NAND status, features or data, the results are buffer in this register, the register is 32 Bits, it can only hold 4 bytes, if the host not doesn't read out the results, it will be over written by the following "read".

P_NAND_INFO

One 32 Bits information per each 512 bytes in ECC mode.

Bit(s)	Name	Description
7:0	Info 0	Information (spare) byte 0, errors already corrected by BCH.
15:8	Info 1	Information (spare) byte 1, errors already corrected by BCH
21:16	Pages	Count down page number in current DMA read, starts from the total page size, count down to 1.
28:24	Errcnt	Number of errors corrected by BCH in current page, 0 means no error in current page, 0x1f means this page is uncorrectable.
29	Unc	When 1, this page is uncorrectable by BCH, this page is bad.
30	Ecc	When 1, current NAND read is with ECC on.
31	Done	When 1, the information content and data read from NAND are valid, otherwise the "read" is not done.

P_NAND_DC

Used for apb_mode, internal NAND controller still uses DDR interface, only the DDR request and DDR grant are redirected from DDR to apb registers, this enables the host to read NAND without DDR, for ROM boot and debug.

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Bit(s)	Name	Description
7:0	Dc_wr_dm	DDR write data mask, Each Bit masks one byte.
8	Dc_wr	When 1, write data from NAND to DDR. When 0, read data from DDR to NAND.
9	Dc_lbrst	When 1, the 64 Bits data is the last in current DDR burst, used with Dc_req.
10	Dc_ugt	When 1, current DDR request of read/write is urgent, in NAND controller, the Dc_ugt is set to 0, none-urgent.
11	Dc_req	When 1, the NAND controller send request to DDR to read or write data, in case of apb_mode, when dc_req is “1”, the host is responsible for send to or receive from NAND controller. Note: this is the only signal the host needs to check when in apb_mode.

P_NAND_ADR

32 Bits DDR address when NAND controller read or write to DDR memory, any address space within the DDR memory installed in the system is valid.

P_NAND_DL

The DDR interface uses 64 Bits width bus, this register is for low 32 Bits, [31:0].

P_NAND_DH

The DDR interface uses 64 Bits width bus, this register is for high 32 Bits, [63:32].

Read and write to this register will generate “grant” and “dc_wr_avail” or “dc_rd_avail”.

Always read or write low 32 Bits first, then read or write to high 32 Bits and NAND controller hardware will generate “grant” and “dc_wr_avail” or “dc_rd_avail”, combined with the data, the DDR address advances to next address.

NAND controller programs NAND flash in apb_mode:

- Check P_NAND_DC till “dc_req” is high.
- Write low 32 Bits to P_NAND_DL.
- Write high 32 Bits to P_NAND_DH.
- Go back to beginning till all the data is written.

NAND controller reads data from NAND flash in apb_mode:

- Check P_NAND_DC till “dc_req” is high.
- Read low 32 Bits from P_NAND_DL.
- Read high 32 Bits from P_NAND_DH.
- Go back to beginning till all the data is read.

Since the DDR interface in NAND controller process the data in group of 16 double words (64 Bits), the software can only check “dc_req” at the beginning of each 16 double words.

P_NAND_CADR

Set command queue memory address, 32 Bits, any memory location.

This address can only be programmed by APB bus.

P_NAND_SADR

Set status memory location, 32 Bits, any memory location.

This address can also be programmed through command queue.

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P_NAND_PINS

Bit(s)	Name	Description
13:0	Pins_len	When pins are acquired by NAND, it will use Pins_len number of NAND bus cycles before releasing pins. Defult is 8.
27:14	Pins_off	When pins are released by NAND, it will wait Pins_off number of NAND bus cycles before sending next request. Default is 2.
31	Not shared	When 1 the pins is not shared, default is 0, pins are shared.

12.3 eMMC/SD

12.3.1 Overview

The SoC has the following features of eMMC/SD.

- Supports SDSC/SDHC/SDXC card
- Supports eMMC and MMC card specification version 5.1 up to HS400 with data content TDES crypto
- 1 bit, 4 Bits, 8 Bits date lines supported (8 Bits only for MMC)
- Descriptor chain architecture, timing tuning and adjustment
- Supports descriptor-based internal DMA controller

This module uses eMMC/SD CONTROLLERs to connect varied SD/MMC Card, or eMMC protocol compatible memory with high throughput.

12.3.2 Pin Description

Table 12-323 Pin Description of eMMC/SD/SDIO Module

Name	Type	Description	Speed (MHz)
CLK	Output	SD eMMC clock, 0~200MHz	200
DS	DS Data strobe for eMMC HS400 mode	-	-
DAT[7:0]	SD Card 4 Bits, eMMC 8 Bits Input/Output/Push-Pull Internal pull-up for pins not used	Data, 1,4,8 mode	200
CMD	Input/Output/Push-Pull/Open-Drain Open-drain for initialization Push-pull for fast command transfer ROD is connected when in open-drain mode.	Command Response	200
Rst_n	eMMC required	Hardware reset	Low
IRQ	SD Card or eMMC not used.	Device interrupt can be replaced by DAT[1]	Low

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12.3.3 eMMC/SD Mode

eMMC Mode

Table 12-324 eMMC Mode

Mode Name	Data Rate	IO Voltage	Bus Width	Frequency	Max Data Transfer
Legacy MMC card	Single	3/1.8V	1, 4, 8	0-26MHz	26MB/s
High Speed SDR	Single	3/1.8V	1,4, 8	0-52MHz	52MB/s
High Speed DDR	Dual	3/1.8V	4, 8	0-52MHz	104MB/s
HS200	Single	1.8V	4, 8	0-200MHz	200MB/s

The HS200 mode offers the following features:

- SDR Data sampling method
- CLK frequency up to 200MHz Data rate – up to 200MB/s
- 4 or 8-bits bus width supported
- Single ended signaling with 4 Drive Strengths
- Signaling levels of 1.8V
- Tuning concept for Read Operations

SD Mode

Table 12-325 SD Mode

Mode Name	Data Rate	IO Voltage	Bus Width	Frequency	Max Data Transfer
Default Speed	Single	3.3V	1, 4	0-25MHz	12.5MB/s
High Speed	Single	3.3V	1, 4	0-50MHz	25MB/s
SDR12	Single	1.8V	1,4	0-25MHz	12.5MB/s
SDR25	Single	1.8V	1,4	0-50MHz	25MB/s
SDR50	Single	1.8V	1,4	0-100MHz	50MB/s
SDR104 (highest)	Single	1.8V	1,4	0-208MHz	104MB/s
DDR50	Dual	1.8V	4	0-50MHz	50MB/s

12.3.4 Descriptor

Structure

The descriptor has a size of 4x32 Bits.

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Table 12-326 Descriptor Structure

byte	7	6	5	4	3	2	1	0
0	length[7:0]							
1	Timeout 4 Bits				End of chain	R1b	block mode	length[8]
2	data num	resp num	resp 128	resp nocrc	Data wr	Data io	No cmd	No resp
3	owner	error	cmd index 6 Bits					
4	cmd argument 32 Bits							
5								
6								
7								
8	data address 32 Bits or data 0-4 bytes [1]Big Endian, [0]SRAM							
9								
10								
11								
12	response address 32 Bits or response irq en [0]SRAM							
13								
14								
15								

Definition

Name	Bits	Description
Length	Cmd_cfg[8:0]	same as spec, copy the content from command argument into this field, different byte size and 512 bytes, different number of blocks and infinite blocks. If the command is operating on bytes, block mode = 0, this field contains the number of bytes to read or write, A value of 0 shall cause 512 bytes to be read to written, if the command is operating on blocks, block mode = 1, this field contains the number of blocks, a value of 0 is infinite number of blocks.
Block_mode	Cmd_cfg[9]	1: the read or write shall be performed on block basis. The block size is from SD/eMMC device, and saved in APB3 register in module. 0: the read or write is byte based.
R1b	Cmd_cfg[10]	1: check the DAT0 busy after received response R1 0: do not check the DAT0 busy state.
End_of_chain	Cmd_cfg[11]	1: it is the end of descriptor chain, the host stops and issues IRQ after this descriptor is done. 0: the host reads next descriptor and continues. The command chain execution is started by write an APB3 register and stopped by the “end of chain” or clear a APB3 start register, or found one descriptor with owner is set to 0.
Timeout	Cmd_cfg[15:12]	2timeout ms when timeout != 0, max timeout 32.768s, when over the time-out limit, error bit is set, IRQ is issued. When timeout is 0, no time limit.
No_resp	Cmd_cfg[16]	1: this command doesn’t have response, used with command doesn’t have response. 0: there is a response. The module waits for response, the response time-out setting is in APB3 register.

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Name	Bits	Description
No_cmd	Cmd_cfg[17]	1: this descriptor doesn't have command in it, it does data DMA only, used with command to read or write SD/eMMC with data from multiple locations.
Data_io	Cmd_cfg[18]	1: there is data action in this descriptor, used with command have data process. 0: there is no data read/write action.
Data_wr	Cmd_cfg[19]	1: host writes data to SD/eMMC 0: host read data from SD/eMMC
Resp_nocrc	Cmd_cfg[20]	1: R3 response doesn't have CRC. 0: host does CRC check.
Resp_128	Cmd_cfg[21]	1: R3 response with 128 Bits information. 0: 32 Bits responses.
Resp_num	Cmd_cfg[22]	1: the resp_addr is the IRQ enable Bits, used to check the response error status, when there is an error, IRQ[14] is issued, the first 4 bytes of response is saved into resp_addr. 0: save response into SRAM or DDR location.
Data_num	Cmd_cfg[23]	1: save 4 bytes of data back into descriptor itself at bytes 8~11.
Cmd_index	Cmd_cfg[29:24]	The SD/eMMC command index. Desc REG wr: 4 reg44, 12 reg4c.
Error	Cmd_cfg[30]	Write back by host. The combined error from command, response, data, includes CRC error and timeout. When it is set the descriptor execution is stopped and an IRQ is issued. The CPU can read SD_EMMC_STATUS register to get detail information.
Owner	Cmd_cfg[31]	Programmed by CPU to 1, cleared by host to 0. 1: the descriptor is valid and owned by host, after it is done, even it has error, the owner bit is cleared, the descriptor is owned by CPU. In case of descriptor chain execution when host found a descriptor with "0" owner bit, it will stop.
Cmd_arg	Desc 4~7 bytes	32 Bits. The actual command argument some of the previous fields are copied from this command argument, the software need to make sure they are consistent. Desc REG wr: new value Data_addr: write mask, 1: change, 0: no change.
Data_addr	Desc 8~11 bytes	32 Bits. If the data_num is 0, the content is data address. If the data_num is 1, ths content is 4 data bytes. When it is an address: Data_addr[0]: 1: SRAM address, 0: DDR address. If the data_addr[31:12] matches with SD_EMMC_BASE, it is SRAM address. Data_addr[1]: 1: 4 bytes big endian, 0: little endian(default).
Resp_addr	Desc 12~15 bytes	32 Bits If the resp_num is 0, the content is resp address. If the resp_num is 1, before execution, it is the response IRQ enable Bits, after execution, it is the first 4 response bytes. When it is an address: Resp_addr[0]: 1: SRAM address, 0: DDR address. If the resp_addr[31:12] matches with SD_EMMC_BASE, it is SRAM address.

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12.3.5 Register Description

Each register final address = module base address+ address * 4

Where module addresses are 0xfe08c000 for port C, 0xfe08a000 for port B, and 0xfe088000 for port A.

Table 12-327 SD_EMMC_CLOCK 0x0

Bit(s)	R/W	Default	Description
30	R/W	0	Cfg_irq_sdio_sleep_ds : 1: select DS as IRQ source during sleep.
29	R/W	0	Cfg_irq_sdio_sleep: 1: enable IRQ sdio when in sleep mode. When DAT1 IRQ, the controller uses PCLK to detect DAT1 level and starts core clock, the core initials IRQ_period and detect DAT1 IRQ.
28	R/W	0	Cfg_always_on: 1: Keep clock always on 0: Clock on/off controlled by activities. Any APB3 access or descriptor execution will turn clock on. Recommended value: 0
27:22	R/W	0	Cfg_rx_delay: RX clock delay line, 6 bits 0: no delay, n: delay n*50ps Maximum delay 3150ps.
21:16	R/W	0	Cfg_tx_delay: TX clock delay line, 6 bits 0: no delay, n: delay n*50ps Maximum delay 63*50ps =3150ps.
15:14	R/W	0	Cfg_sram_pd: Sram power down
13:12			Cfg_rx_phase: RX clock phase 0: 0 phase, 1: 90 phase, 2: 180 phase, 3: 270 phase. Recommended value: 0
11:10	R/W	0	Cfg_tx_phase: TX clock phase 0: 0 phase, 1: 90 phase, 2: 180 phase, 3: 270 phase. Recommended value: 2
9:8	R/W	0	Cfg_co_phase: Core clock phase 0: 0 phase, 1: 90 phase, 2: 180 phase, 3: 270 phase. Recommended value: 2
7:6	R/W	0	Cfg_src: Clock source 0: Crystal 24MHz or other frequencies selected by clock reset test control register. 1: Fix PLL, 1000MHz Recommended value: 1
5:0	R/W	0	Cfg_div: Clock divider Frequency = clock source/cfg_div Clock off: cfg_div==0, the clock is disabled Divider bypass: cfg_div==1, clock source is used as core clock without divider Maximum divider 63.

Table 12-328 SD_EMMC_DELAY1 0x4

Bit(s)	R/W	Default	Description
31:30	R/W	0	Reserved.
29:24	R/W	0	Dly[4]: Data 4 delay line
23:18	R/W	0	Dly[3]: Data 3 delay line
17:12	R/W	0	Dly[2]: Data 2 delay line
11:6	R/W	0	Dly[1]: Data 1 delay line
5:0	R/W	0	Dly[0]: Data 0 delay line Total delay = 50ps * Dly When Dly == 0, no delay. When Dly ==63, 3150ps delay. NOTE: the 50ps is typical delay, actually delay may vary from chip to chip, from different temperature.

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Table 12-329 SD_EMMC_DELAY2 0x8

Bit(s)	R/W	Default	Description
31:30			Reserved.
29:24			Dly[9]: Data 9 delay line
23:18			Dly[8]: Data 8 delay line
17:12			Dly[7]: Data 7 delay line
11:6			Dly[6]: Data 6 delay line
5:0			Dly[5]: Data 5 delay line Total delay = 50ps * Dly When Dly == 0, no delay. When Dly ==63, 3150ps delay. NOTE: the 50ps is typical delay, actually delay may vary from chip to chip, from different temperature.

Table 12-330 SD_EMMC_ADJUST 0xc

Bit(s)	R/W	Default	Description
31:23			Unused
22	R/W	0	Adj_auto 1: Use cali_dut's first falling edge to adjust the timing, set cali_enable to 1 to use this function, simulation shows it can tracking 2.5ns range with 800ppm. 0: disable Working for HS200 mode, set Cali_enable to 1. Enhanced after gxlx project. Use RESP and DAT0 as reference, Separate RESP and DAT0, adjust the timing whenever there is a transition, insert a sample when there is no transition.
21:16	R/W	0	Adj_delay: Resample the input signals when clock index==adj_delay
15	R/W	0	Reserved
14	R/W	0	Cali_rise: 1: test the rising edge, recording rising edge location only. 0: test the falling edge
13	R/W	0	Adj_fixed: Adjust interface timing by resampling the input signals
12	R/W	0	Cali_enable: 1: Enable calibration 0: shut off to save power.
11:8	R/W	0	Cali_sel: Select one signal to be tested Signals are labeled from 0 to 9 the same as delay lines. Only one signal is tested at anytime. For example: Cali_sel == 9, test CMD line.

Table 12-331 SD_EMMC_CALOUT 0x10

Bit(s)	R/W	Default	Description
31:16			Unused
15:8	R		Cali_setup
7	R		Cali_vld: The reading is valid When there is no rising edge or falling edge event, the valid is low, this reading is not valid.
5:0	R		Cali_idx: The event happens at this index, The index starts from rising edge of core clock from 0, 1, 2, …

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Table 12-332 SD_EMMC_ADJ_IDX_LOG 0x20

Bit(s)	R/W	Default	Description
31:30			Current, Auto_adj mode, Current 6 bits adj_idx
29:24			Previous 1
23:18			Previous 2
17:12			Previous 3
11:6			Previous 4
5:0			Previous 5: Last two bits of previous 5

Table 12-333 SD_EMMC_CLKTEST_LOG 0x24

Bit(s)	R/W	Default	Description
31			Clktest_done, Test done
30:0			Clktest_times, Test clock core for 2^Clktest_exp

Table 12-334 SD_EMMC_CLKTEST_OUT 0x28

Bit(s)	R/W	Default	Description
31:0			Clktest_out, All 2^clktest_exp test results add up. Note: divided by 2^clktest_exp and get average clock core period length measured by 50ps delay cells.

Table 12-335 SD_EMMC_EYETEST_LOG 0x2c

Bit(s)	R/W	Default	Description
31			eyetest_done, Test done
30:0			eyetest_times, Test eye for 2^eyetest_exp

Table 12-336 SD_EMMC_EYETEST_OUT0 0x30

Bit(s)	R/W	Default	Description
31:0			All 2^eyetest_exp test results “OR” together.

Table 12-337 SD_EMMC_EYETEST_OUT1 0x34

Bit(s)	R/W	Default	Description
31:0			eyetest_out1, All 2^eyetest_exp test results “OR” together. Total eyeout [62:0] = {Eyetest_out1[30:0], eyetest_out0[31:0]} EYEtest output changed to 64 bits after TXLX and A113 {eyetest_out1, eyetest_out0}

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Table 12-338 SD_EMMC_INTF3 0x38

Bit(s)	R/W	Default	Description
26			Eyetest_sel, 0 : select core clock as eyetest clock. 1 : select DS after delay line as eyetest clock. Eyetest point is DS after delay line.
25:23			NAND_EDO, NAND Async interface EDO position after RE rising edge. [not for SD_eMMC]
22			Sd_intf3, Using SD interface 3
21:18			Ds_sht_exp, 0: DS shift setting never expires, always using the DS_sht_m as shift length. None-zero: 2^ds_sht_exp after 2^ds_sht_exp “ms”, the setting expired The internal FSM will automatically change the Ds shift setting.
17:12			Ds_sht_m, Shift DS by number of 50ps delay cells. If using auto FSM mode, it is the initial value.
11			Eyetest_on, 1: Turn on eye test After eyetest_done, set this bit to 0 to reset eyetest internal registers.
10:6			Eyetest_exp, Repeat the eye test for 2^eyetest_exp times, Or the test results together, report the final results.
5			Clktest_on_m, Manual turn on clock test
4:0			Clktest_exp, Repeat the clock test for 2^clktest_exp times. Add the clock length together, report the sum.

Table 12-339 SD_EMMC_START 0x40

Bit(s)	R/W	Default	Description
31:2	R/W	0	Desc_addr[31:2]: Descriptor address, the last 2 Bits are 0, SRAM: 4 bytes aligned, the valid address range is from 0x200~0x3ff DDR: 8 bytes aligned the valid address is anywhere in DDR, the length of chain is unlimited. Desc_addr = ADDR>>2.
1	R/W	0	Desc_busy: Start/Stop 1: Start command chain execution process. 0: Stop Write 1 to this register starts execution. Write 0 to this register stops execution.
0	R/W	0	Desc_int: SRAM/DDR 1: Read descriptor from internal SRAM, limited to 32 descriptors. 0: Read descriptor from external DDR

Table 12-340 SD_EMMC_CFG 0x44

Bit(s)	R/W	Default	Description
31:28	R/W	0	Cfg_ip_txd_adj: Data 1 interrupt, when in TXD mode, the data 1 irq is a input signal, the round trip delay is uncertain factor, change this cfg to compensate the delay.
27	R/W	0	Cfg_err_abort: 1: abort current read/write and issue IRQ 0: continue on current read/write blocks.
26	R/W	0	Cfg_irq_ds: 1: Use DS pin as SDIO IRQ input, 0: Use DAT1 pin as SDIO IRQ input.
25	R/W	0	Cfg_txd_retry: When TXD CRC error, host sends the block again. The total number of retries of one descriptor is limited to 15, after 15 retries, the TXD_err is set to high.

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Bit(s)	R/W	Default	Description
24	R/W	0	Cfg_txd_add_err: TXD add error test. Test feature, should not be used in normal condition. It will inverted the first CRC Bits of the 3rd block. Block index starts from 0, 1, 2, …
23	R/W	0	Cfg_auto_clk: SD/eMMC Clock Control 1: when BUS is idle and no descriptor is available, automatically turn off clock, to save power. 0:.whenever core clock is on the SD/eMMC clock is ON, it is still on/off during read data from SD/eMMC.
22	R/W	0	Cfg_stop_clk: SD/eMMC Clock Control 1: no clock for external SD/eMMC, used in voltage switch. 0: normal clock, the clock is automatically on/off during reading mode to back off reading in case of DDR slow response.
21	R/W	0	Cfg_cmd_low: Hold CMD as output Low eMMC boot mode.
20	R/W	0	Reserved
19	R/W	0	Cfg_ignore_owner: Use this descriptor even if its owner bit is “0”.
18	R/W	0	Cfg_sdclk_always_on: 1: SD/eMMC clock is always ON 0: SD/eMMC clock is controlled by host. WARNING: Set SD/eMMC clock to always ON, host may lose data when DDR is slow.
17	R/W	0	Cfg_blk_gap_ip: 1: Enable SDIO data block gap interrupt period 0: Disabled.
16	R/W	0	Cfg_out_fall: DDR mode only The command and TXD start from rising edge. Set 1 to start from falling edge.
15:12	R/W	0	Cfg_rc_cc: Wait response-command, command-command gap before next command, 2cfg_rc_cc core clock cycles.
11:8	R/W	0	Cfg_resp_timeout: Wait response till 2cfg_resp_timeout core clock cycles. Maximum 32768 core cycles.
7:4	R/W	0	Cfg_bl_len: Block length 2cfg_bl_len, because internal buffer size is limited to 512 bytes, the cfg_bl_len <=9.
3	R/W	0	Cfg_dc_ugt: 1: DDR access urgent 0: DDR access normal
2	R/W	0	Cfg_ddr: 1: DDR mode 0: SDR mode
1:0	R/W	0	Cfg_bus_width: 0: 1 bit 1: 4 Bits 2: 8 Bits 3: 2 Bits (not supported)

Table 12-341 SD_EMMC_STATUS 0x48

Bit(s)	R/W	Default	Description
31	R		Core_busy: 1: core is busy, desc_busy or sd_emmc_irq or bus_fsm is not idle. 0: core is idle.
30	R		Desc_busy: 1: Desc input process is busy, more descriptors in chain. 0: no more descriptor in chain or desc_err.
29:26	R		Bus_fsm: BUS fsm
25	R		DS: Input data strobe
24	R		CMD_i: Input response signal
23:16	R		DAT_i: Input data signals

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Bit(s)	R/W	Default	Description
15	R/W		IRQ_sdio: SDIO device uses DAT[1] to request IRQ
14	R/W		Resp_status: When resp_num is set to 1, the resp_addr is the response status IRQ enable Bits, if there is an error.
13	R/W		End_of_Chain: End of Chain IRQ, Normal IRQ
12	R/W		Desc_timeout: Descriptor execution time over time limit. The timeout limit is set by descriptor itself. Consider the multiple block read/write, set the proper timeout limits.
11	R/W		Resp_timeout: No response received before time limit. The timeout limit is set by cfg_resp_timeout.
10	R/W		Resp_err: Response CRC error
9	R/W		Desc_err: SD/eMMC controller doesn't own descriptor. The owner bit is "0", set cfg_ignore_owner to ignore this error.
8	R/W		Txd_err: TX data CRC error, For multiple block write, any one of blocks CRC error.
7:0	R/W		Rxd_err: RX data CRC error per wire, for multiple block read, the CRC errors are Ored together.

Table 12-342 SD_EMMC_IRQ_EN 0x4c

Bit(s)	R/W	Default	Description
31:18			unused
17			Cfg_cmd_setup, 1: improve CMD setup time by half SD_CLK cycle. 0: CMD is two cycle aligned with DATA.
16	R/W	0	Cfg_secure: Data read/write with crypto DES
15	R/W	0	en_IRQ_sdio: Enable sdio interrupt.
14	R/W	0	En_resp_status: Response status error.
13	R/W	0	en_End_of_Chain: End of Chain IRQ
12	R/W	0	en_Desc_timeout: Descriptor execution time over time limit.
11	R/W	0	en_Resp_timeout: No response received before time limit.
10	R/W	0	en_Resp_err: Response CRC error
9	R/W	0	en_Desc_err: SD/eMMC controller doesn't own descriptor.
8	R/W	0	En_txd_err: TX data CRC error
7:0	R/W	0	en_Rxd_err: RX data CRC error per wire.

Table 12-343 Descriptor_REG0 0x50

Bit(s)	R/W	Default	Description
31:0	R/W		SD_EMMC_CMD_CFG APB read wait Same as descriptor first word, resp_num = 1, response saved back into descriptor only. Read from this APB will hold APB bus

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Table 12-344 Descriptor_REG1 0x54

Bit(s)	R/W	Default	Description
31:0	R/W		SD_EMMC_CMD_ARG APB write start Same as descriptor second word. Write to this APB address starts execution. If the current desc is busy, it will be executed after current descriptor is done.

Table 12-345 Descriptor_REG2 0x58

Bit(s)	R/W	Default	Description
31:0	R/W		SD_EMMC_CMD_DAT : Same as descriptor third word, 32 Bits data.

Table 12-346 Descriptor_REG3 0x5c

Bit(s)	R/W	Default	Description
31:0	R/W		SD_EMMC_CMD_RSP: Write: response status IRQ enable Bits. Read: Response Bit 31:0

Table 12-347 Descriptor_REG4 0x60

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_CMD_RSP1: Response bit 63:32

Table 12-348 Descriptor_REG5 0x64

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_CMD_RSP2: Response bit 95:64

Table 12-349 Descriptor_REG6 0x68

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_CMD_RSP3: Response bit 127:96

Table 12-350 Descriptor_REG7 0x6c

Bit(s)	R/W	Default	Description
31:0			Reserved

Table 12-351 Current_Next_Descriptor_REG0 0x70

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_CURR_CFG: Current descriptor under execution.

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Table 12-352 Current_Next_Descriptor_REG1 0x74

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_CURR_ARG

Table 12-353 Current_Next_Descriptor_REG2 0x78

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_CURR_DAT

Table 12-354 Current_Next_Descriptor_REG3 0x7c

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_CURR_RSP

Table 12-355 Current_Next_Descriptor_REG4 0x80

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_NEXT_CFG: Next descriptor waiting for execution, already read out from SRAM or DDR, can't be changed.

Table 12-356 Current_Next_Descriptor_REG5 0x84

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_NEXT_ARG

Table 12-357 Current_Next_Descriptor_REG6 0x88

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_NEXT_DAT

Table 12-358 Current_Next_Descriptor_REG7 0x8c

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_NEXT_RSP

Table 12-359 SD_EMMC_RXD 0x90

Bit(s)	R/W	Default	Description
31:25	R		Unused
24:16	R		Data_blk: Rxd Blocks received from BUS Txd blocks received from DDR.
15:10			unused
9:0	R		Data_cnt: Rxd words received from BUS. Txd words received from DDR.

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Table 12-360 SD_EMMC_TXD 0x94

Bit(s)	R/W	Default	Description
31:25			Unused
24:16	R		Txd_blk: Txd BUS block counter
15			unused
14:0	R		Txd_cnt: Txd BUS cycle counter

12.4 Serial Peripheral Interface Communication Controller

12.4.1 Overview

SPI Communication Controller is designed for connecting general SPI protocol compatible module. This controller allows rapid data communication with less software interrupts than conventional serial communications.

12.4.2 Features

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four chip selects to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 64-bit wide by 16-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Both PIO(Programming In/Out interface) and DMA(Direct Memory Access interface) supported

12.4.3 Function

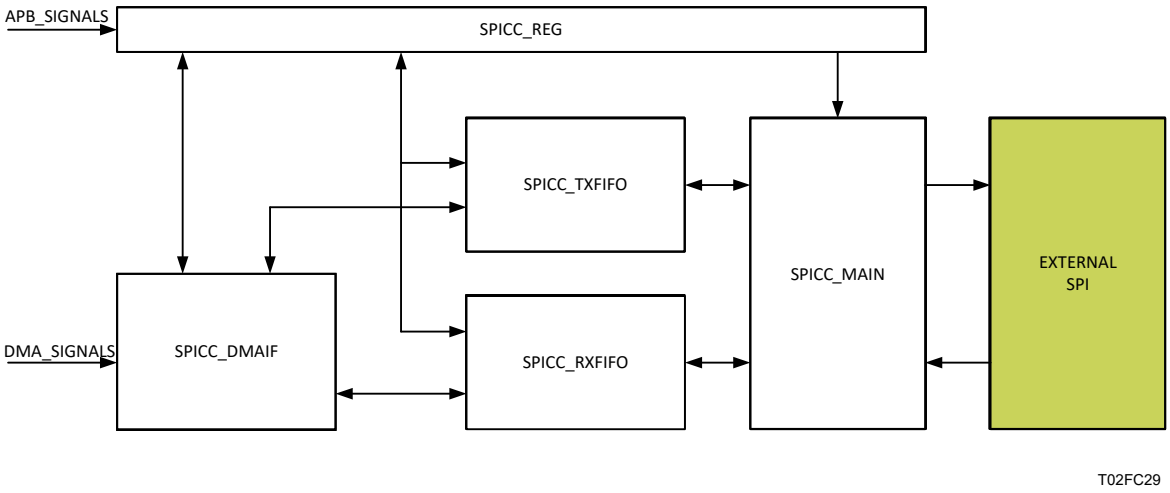
The following are two SPICC modes of operation:

- **Master Mode**—When the SPICC module is configured as a master, it uses a serial link to transfer data between the SPICC and an external device. A chip-enable signal and a clock signal are used to transfer data between these two devices. If the external device is a transmit-only device, the SPICC master's output port can be ignored and used for other purposes. To use the internal TXFIFO and RXFIFO, two auxiliary output signals, SS and SPI_RDY, are used for data transfer rate control. The user can also program the sample period control register to a fixed data transfer rate.
- **Slave Mode**–When the SPICC module is configured as a slave, the user can configure the SPICC Control register to match the external SPI master's timing. In this configuration, SS becomes an input signal, and is used to control data transfers through the Shift register, as well as to load/store the data FIFO.

There are 5 sub-modules in spi communication controller, i. e. spicc_reg, spicc_dmaif, spicc_txfifo, spicc_rxfifo, and spicc_main. Transmitting and receiving are using different channel, that means they have different buffer.

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Figure 12-5 SPICC



Note

- spicc_reg is driven by host cpu, and spicc_reg is responsible for configuring other modules.
- spicc_dmaif is responsible for dealing with DMA operatoins.
- spicc_txfifo contains a transmission FIFO.
- spicc_rxfifo contains a receiving FIFO.
- spicc_main is responsible for main control of basic spi operation.

Here are SPI External Signals:

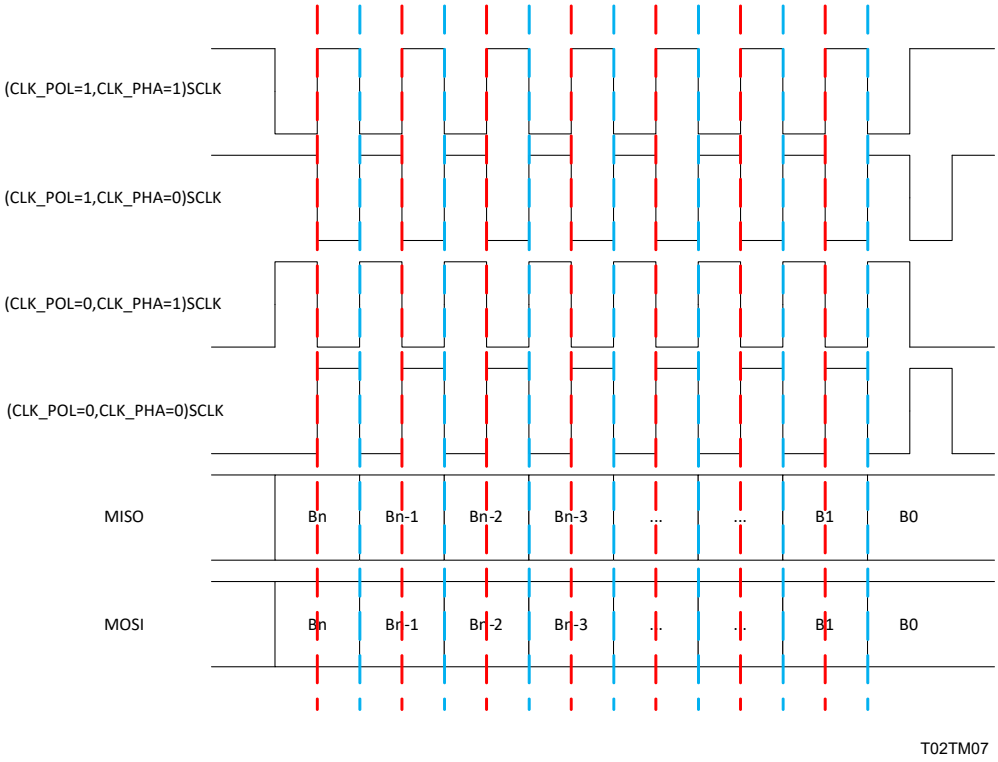
Table 12-361 SPI External Signals

Signal Name	I/O	Description
spicc_sclk	IO	SCLK, SPI Clock
spicc_miso	IO	MISO, Master Input Slave Output
spicc_mosi	IO	MOSI, Master Output Slave In
spicc_ss[3:0]	IO	SS, SPI chip Select, Supports up to 4 slaves.

And here is SPI Generic Timing:

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Figure 12-6 SPI Generic Timing



12.4.4 Register Description

Table 12-362 RXDATA 0xffd13000

Bit(s)	R/W	Default	Description
31:0	R	0	Rx Data

Note

When PIO mode, programmer can get data from this register.

Table 12-363 TXDATA 0xffd13004

Bit(s)	R/W	Default	Description
31:0	W	0	Tx Data

Note

When PIO mode, programmer need send data to this register.

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Table 12-364 CONREG 0xffd13008

Bit(s)	R/W	Default	Description
31:19	RW	0	[13]burst_length ([5:0]bit number of one word/package, [12:6]burst length-1)
18:16	RW	0	[3]data_rate (sclk will be divided by system clock with equation: 2^(data_rate+2), Example: if system clock = 128MHz and data_rate=2, sclk's frequency equals 8MHz)
15:14			Reserved
13:12	RW	0	[2]chip_select (00:select ss_0, 01:select ss_1, 10:select ss_2, 11:select ss_3,)
11:10			Reserved
9:8	RW	0	[2]drctl (0:ignore RDY input, 1:Data ready using pin rdy_i's failing edge, 2:Data ready using pin rdy_i's low level, 3:reserved)
7	RW	0	[1]sspol (0:SS polarity Low active,1:High active)
6	RW	0	[1]ssctl (see details in Note1)
5	RW	0	[1]pha (clock/data phase control, see section 2.2)
4	RW	0	[1]pol (clock polarity control, see section 2.2)
3	RW	0	[1]smc (start mode control, see Note2)
2	RW	0	[1]xch(exchange bit, ATTN:will automatically cleared when burst finished, see Note3)
1	RW	0	[1]mode (0:slave,1:master)
0	RW	0	[1]en (0:spicc disable,1:enable)

Note

- In one burst of master mode, if ssctl ==1, ss will output 1 between each spi transition. And if ssctl ==0, ss will output 0.
- Smc is for start mode control. If smc ==0, burst will start when xch is set to 1'b1; if smc==1, burst will start when txfifo is not empty.
- Setting xch will issue a burst when smc==0, and This bit will be self-cleared after burst is finished.

Table 12-365 INTREG 0xffd1300c

Bit(s)	R/W	Default	Description
31:8			Reserved
7	RW	0	[1]tcen(transfer completed interrrupt enable)
6	RW	0	Reserved
5	RW	0	[1]rfen(rxfifo full interrrupt enable)

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Bit(s)	R/W	Default	Description
4	RW	0	Reserved
3	RW	0	[1]rren(rxfifo ready interrrupt enable)
2	RW	0	[1]tfen(txfifo full interrrupt enable)
1	RW	0	Reserved
0	RW	0	[1]teen(txfifo empty interrrupt enable)

Note

Interrupt Status presents in STATREG.

Table 12-366 DMAREG 0xffd13010

Bit(s)	R/W	Default	Description
31:26	RW	0	[6]DMA Burst Number
25:20	RW	0	[6]DMA Thread ID
19	RW	0	[1]DMA Urgent
18:15	RW	0x7	[4]Number in one Write request burst(0:1,1:2...)
14:11	RW	0x7	[4]Number in one Read request burst(0:1,1:2...)
10:6	RW	0x8	[5]RxFIFO threshold(RxFIFO's count>=thres, will request write)
5:1	RW	0	[5]TxFIFO threshold(TxFIFO's count<=thres, will request read)
0	RW	0	[1]DMA Enable

Table 12-367 STATREG 0xffd13014

Bits	R/W	Defaults	Description
31:8			Reserved
7	RW	0	[1]tc(transfer completed, w1c, see Note1)
6	R	0	Reserved
5	R	0	[1]rf(rxfifo full)
4	R	0	Reserved
3	R	0	[1]rr(rxfifo ready)
2	R	0	[1]tf(txfifo full)
1	R	0	Reserved
0	R	0	[1]te(txfifo empty)

Note

Tc is the status bit which indicates a burst transfer is completed. And a burst transfer should be started by writing xch 1'b1. This bit supports w1c(Write 1 clear).

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Table 12-368 PERIODREG 0xffd13018

Bit(s)	R/W	Default	Description
31:15			Reserved
14:0	RW	0	[15]period(wait cycles, see Note1)

Note

Programmer can add wait cycles through this register if transmission rate need to be controlled.

Table 12-369 TESTREG 0xffd1301c

Bit(s)	R/W	Default	Description
31:23	RW	0	Reserved
23:22	RW	0	[2]fiforst(fifo soft reset)
21:16	RW	0x15	[6]dlyctl(delay control)
15	RW	0	[1]swap(data swap for reading rxfifo)
14	RW	0	[1]lbc(loop back control)
12:10	R	0	[3]smstatus(internal state machine status)
9:5	R	0	[5]rxcnt(internal RxFIFO counter)
4:0	R	0	[5]txcnt(internal TxFIFO counter)

Note

Programmer can only use the TESTREG[9:0], rxcnt(internal RxFIFO counter) and txcnt(internal TxFIFO counter) , and other Bits just for test.

Table 12-370 DRADDR 0xffd13020

Bit(s)	R/W	Default	Description
31:0	RW	0	Read Address of DMA

Table 12-371 DWADDR 0xffd13024

Bit(s)	R/W	Default	Description
31:0	RW	0	Write Address of DMA

Table 12-372 LD_CNTL0 0xffd13028

Bits	R/W	Defaults	Description
31:9	RW	0	Reserved
8	RW	0	dma raddr/waddr load by dma_enable signal
7	RW	0	dma waddr load by vsync irq
6	RW	0	dma raddr load by vsync irq
5	RW	0	dma write counter enable

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Bits	R/W	Defaults	Description
4	RW	0	dma read counter enable
3	RW	0	xch enable set by vsync irq
2	RW	0	dma enable set by vsync irq
1	RW	0	Reserved
0	RW	0	Vsync irq source select

Table 12-373 LD_CNTL1 0xffd1302c

Bits	R/W	Defaults	Description
31:16	RW	0	dma write counter
15:0	RW	0	dma read counter

Table 12-374 LD_RADDR 0xffd13030

Bits	R/W	Defaults	Description
31:0	RW	0	shadow dma read address for load

Table 12-375 LD_WADDR 0xffd13034

Bits	R/W	Defaults	Description
31:0	RW	0	shadow dma write address for load

Table 12-376 ENHANCE_CNTL 0xffd13038

Bits	R/W	Defaults	Description
31:30	R	0	Reserved
29	R/W	0	main clock always on
28	R/W	0	clk-cs delay enable
27	R/W	0	cs_oen enhance enable
26	R/W	0	clk_oen enhance enable
25	R/W	0	mosi_oen enhance enable
24	R/W	0	spi clk select 0: controlled by data_rate in CONREG 1: controlled by enhance_clk_div in ENHANCE_CNTL
23:16	R/W	0	enhance_clk_div
15:0	R/W	0	clk-cs delay value

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Table 12-377 ENHANCE_CNTL1 0xffd1303c

Bits	R/W	Defaults	Description
31:29	R/W	0	enhance_fclk_mosi_oen_dlyctl: mosi_oen delay control in fclk
28	R/W	0	enhance_fclk_mosi_oen_dlyctl_en: enable dlyctl
27:25	R/W	0	enhance_fclk_mosi_o_dlyctl: mosi_o delay control in fclk
24	R/W	0	enhance_fclk_mosi_o_dlyctl_en: enable dlyctl
23:21	R/W	0	enhance_fclk_miso_i_dlyctl: miso_i delay control in fclk
20	R/W	0	enhance_fclk_miso_i_dlyctl_en: enable dlyctl
19:17	R/W	0	enhance_fclk_mosi_i_dlyctl: mosi_i delay control in fclk
16	R/W	0	enhance_fclk_mosi_i_dlyctl_en: enable dlyctl
15	R/W	0	enhance_fclk_en: fclk gate enable
14	R/W	0	enhance_mosi_i_capture_en: enable, 1=select enhance capture function for mosi_i (slave mode)
9:1	R/W	0	enhance_clk_tcnt: adjust capturing timing for miso_i data (master mode). when clk_cnt=enhance_clk_tcnt, capture input data. the value of enhance_clk_tcnt must be less than the most value of clk_cnt. sclk will be divided by system clock with clk_cnt.
0	R/W	0	enhance_miso_i_capture_en: enable, 1=select enhance capture function for miso_i (master mode)

Table 12-378 ENHANCE_CNTL2 0xffd13040

Bits	R/W	Defaults	Description
31	R/W	0	clk_cs_tt delay enable
30:16	R/W	0	clk_cs_tt delay value
15	R/W	0	clk_cs_ti delay enable
14:0	R/W	0	clk_cs_ti delay value

SPICC1: See the registers for SPICC0

12.5 Serial Peripheral Interface Flash Controller

12.5.1 Overview

Serial Peripheral Interface Flash Controller (SPIFC) is designed for connecting varied SPI Flash memory.

12.5.2 Features

- Support three operation modes, NOR Flash mode, Master mode, and Slave mode.
- Support read/write buffer up to 64bytes.
- Support no clock toggling during DUMMY state.
- Support hold by an external pin during a transition.

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- AHB read support byte and halfword.
- Support bit-number rather than byte-number for each stage.
- Support 2/4 wire writing like fast reading
- Support both rising-edge and falling-edge for SPI slave sampling and SPI master sampling.
- Support 1 wire for SPI_D and SPI_Q.
- Support SPI_CK setup and hold time by cycles
- Support 8 bit clock divider, so SPI_CK can be low as 1/256 HCLK
- Support byte-order in a word
- Support no command state, so the command is sent/received in address state by 2/4 wires.
- Support both data input and data output in a transition. SPI_DOUT->(SPI_DUMMY)->SPI_DIN

12.5.3 Register Description

Note

If the bit2 “Backward Compatible” in “SPI User Register” is 1, the registers and functions of this SPI controller are as same as Apollo SPI controller.

To use SPI Flash commands, please set the bit2 “Backward Compatible” in “SPI User Register” as “1”.

Table 12-379 SPI_FLASH_CMD 0xfe056000

Bit(s)	R/W	Default	Description
31	R/W	0	READ command. 1 = read. When it becames 0, the read command is finished. The READ command could be (0xEB, 0x6B, 0xBB, 0x3B, 0x0B, 0x03). By default is 0x0B. One read command will read erilog 32x8bits data. And saved in data cache.
30	R/W	0	WREN command. (0x06)
29	R/W	0	WRDI command. (0x04).
28	R/W	0	RDID command. (0x9f).
27	R/W	0	RDSR command. (0x05).
26	R/W	0	WRSR command. (0x01).
25	R/W	0	Page program command. (0xAD or 0x02).
24	R/W	0	SE command (0x20).
23	R/W	0	BE command (0xD8).
22	R/W	0	CE command.(0xC7).
21	R/W	0	Deep Power Down command(0xB9).
20	R/W	0	RES command. (0xAB).
19	R/W	0	HPM command.(0xA3). (Just For winbond SPI flash).
18	R/W	0	USER defined command.
17:0	R/W	0	Reserved for future.

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Table 12-380 SPI_FLASH_ADDR 0xfe056004

Bit(s)	R/W	Default	Description
31:0	R/W	0	The address[31:0] of the user command

Table 12-381 SPI_FLASH_CTRL 0xfe056008

Bit(s)	R/W	Default	Description
31:27	R/W	0	Reserved.
26	R/W	0	Write bit order. 1 = 0, 1, 2, 3, 4, 5, 6, 7. 0 = 7, 6, 5, 4, 3, 2, 1, 0.
25	R/W	0	Read bit order. . 1 = 0, 1, 2, 3, 4, 5, 6, 7. 0 = 7, 6, 5, 4, 3, 2, 1, 0.
24	R/W	0	Fast read QIO mode.
23	R/W	0	Fast read DIO mode.
22	R/W	0	Write 2 bytes status mode. For some of winbond SPI flash, the status register is 16bits.
21	R/W	1	SPI flash WP pin value if use SPI flash WP pin as write protection.
20	R/W	0	Fast read QOUT mode.
19	R/W	1	1 = SPI share pins with SDRAM. 0 = doesn't share.
18	R/W	0	SPI hold mode. 1=SPI controller would use SPI hold function. 0 = SPI controller won't use hold function. The SPI flash hold pin can be tie high on the board. Or SPI controller can use hold pin as QIO/QOUT mode.
17	R/W	1	1 = enable AHB request. 0 = disable AHB request when you reconfigure SPI controller or running APB bus commands.
16	R/W	0	1 =enable SST SPI Flash aai command. The APB bus PP command will send AAI command.
15	R/W	1	1 = release from Deep Power-Down command is with read electronic signature.
14	R/W	0	Fast read DOUT mode.
13	R/W	1	Fast read mode. AHB bus read requirement and APB bus read command use the command 0x0Bh.
12:0	R/W	0	Reserved for future.

Table 12-382 SPI_FLASH_CTRL1 0xfe05600c

Bit(s)	R/W	Default	Description
31:28	R/W	5	SPI Clock cycles for SPI flash timing requirement tCSH.
27:16	R/W	0xfff	SPI Clock cycles for SPI flash timing requirement tRES.
15:0	R/W	0x0120	System clock cycles for SPI bus timer. In SPI share bus and SPI hold function mode. SPI bus timer used , if SPI use the bus for a limit time, SPI controller will diassert SPI hold pin to halt the SPI Flash, and give the bus control to SDRAM.

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Table 12-383 SPI_FLASH_STATUS 0xfe056010

Bit(s)	R/W	Default	Description
31:24	R/W	0	Reserved.
23:16	R/W	0	For winbond SPI flash, this 8 bits used for DIOmode M7~M0,
15:0	R/W	0	SPI status register value. WRSR command will write this value to SPI flash status. RDSR or RES command will save the read result to this register.

When SPI controller in the slave mode, this register are the status for the SPI master to read out.

Bit(s)	R/W	Default	Description
31:0	R/W	0	In SPI Slave mode, the read status of the user command

Table 12-384 SPI_FLASH_CTRL2 0xfe056014

Bit(s)	R/W	Default	Description
31:28	R/W	0	Delay cycle number of SPI_CS input in SPI slave mode or SPI_CS output in SPI master mode 0= not delay, 1 = delayed by 1 cycle of system clock, 2 = delayed by 2 cycles of system clock , …
27:26	R/W	0	delay mode of SPI_CS input in SPI slave mode or SPI_CS output in SPI master mode 0= not latched by the edges of SPI_CK 1= latched by the falling edges of SPI_CK 2 = latched by the rising edges of SPI_CK
25:23	R/W	0	Delay cycle number of SPI Data from SPI Master to SPI Slave In SPI master mode, it is for data outputs; in SPI slave mode, it is for data inputs. 0= not delay, 1 = delayed by 1 cycle of system clock, 2 = delayed by 2 cycles of system clock , …
22:21	R/W	0	Delay mode of SPI Data from SPI Master to SPI Slave In SPI master mode, it is for data outputs; in SPI slave mode, it is for data inputs. 0= not latched by the edges of SPI_CK 1= latched by the falling edges of SPI_CK 2 = latched by the rising edges of SPI_CK
20:18	R/W	0	Delay cycle number of SPI Data from SPI Slave to SPI Master. In SPI master mode, it is for data inputs; in SPI slave mode, it is for data outputs. 0= not delay, 1 = delayed by 1 cycle of system clock, 2 = delayed by 2 cycles of system clock , …
17:16	R/W	0	Delay mode of SPI Data from SPI Slave to SPI Master. In SPI master mode, it is for data inputs; in SPI slave mode, it is for data outputs. 0= not latched by the edges of SPI_CK 1= latched by the falling edges of SPI_CK 2 = latched by the rising edges of SPI_CK
15:12	R/W	0	In SPI master mode, SPI_CK rising edge mode 4'b1000 = later by 1/4 cycle of SPI_CK 4'b1001 = later by 1/8 cycle of SPI_CK 4'b1010 = later by 1/16 cycle of SPI_CK 4'b1011 = later by 1/32 cycle of SPI_CK 4'b1100 = earlier by 1/4 cycle of SPI_CK 4'b1101 = earlier by 1/8 cycle of SPI_CK 4'b1110 = earlier by 1/16 cycle of SPI_CK 4'b1111 = earlier by 1/32 cycle of SPI_CK Others = Normal
11:8	R/W	0	In SPI master mode, SPI_CK falling edge mode

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Bit(s)	R/W	Default	Description
			4'b1000 = later by 1/4 cycle of SPI_CK 4'b1001 = later by 1/8 cycle of SPI_CK 4'b1010 = later by 1/16 cycle of SPI_CK 4'b1011 = later by 1/32 cycle of SPI_CK 4'b1100 = earlier by 1/4 cycle of SPI_CK 4'b1101 = earlier by 1/8 cycle of SPI_CK 4'b1110 = earlier by 1/16 cycle of SPI_CK 4'b1111 = earlier by 1/32 cycle of SPI_CK Others = Normal
7:4	R/W	1	In master mode, SPI clock cycles for SPI hold timing.
3:0	R/W	1	In master mode, SPI clock sycles for SPI setup timing. SPI setup time and SPI hold time is used to configure how soon the controller can enable spi_cs_n after the controller get the bus and how long the controller still keep the bus after the spi_cs_n become to be high.

Table 12-385 SPI_FLASH_CLOCK 0xfe056018

Bit(s)	R/W	Default	Description
31	R/W	1	1=SPI clock frequency is same as system clock. 0 = SPI clock frequency will use clock divider.
30:18	R/W	0	Clock counter for Pre-scale divider: 0= not pre-scale divider, 1= pre-scale divided by 2, 2= pre-scale divided by 3, ….,
17:12	R/W	0	Clock counter for clock divider.
11:6	R/W	0	Clock high counter in SPI master mode. In SPI slave mode, it is for the delay counter for the rising edges of spi_ck_i
5:0	R/W	0	Clock low counter, in SPI master mode. In SPI slave mode, it is for the delay counter for the falling edges of spi_ck_i If the SPI clock frequcncy = sys_clock_frequency / n. Then the clock divider counter = n – 1; the clock high counter = n /2 – 1; the clock low counter = n– 1; For example, if you want to SPI clock erilog is divided by 2 of the system clock. The clock divider counter = 1, clock high counter = 0, clock low counter = 1. For SPI clock frequency = system clock / 4. The clock divider counter = 3, clock high counter = 1, clock low counter = 3.

Table 12-386 SPI_FLASH_USER 0xfe05601c

Bit(s)	R/W	Default	Description
31	R/W	1	USER command COMMAND bit. 1 = user command includes command. 0 = no command. If some SPI slaves may support 2/4 IO at the first cycle, clear this bit.
30	R/W	0	USER command ADDRESS bit. 1 = user command includes address. 0 = no address.
29	R/W	0	USER command DUMMY bit. 1= user command includes Dummy bytes.
28	R/W	0	USER command DIN bit. 1 = user command includes data in. 0 = no data in.
27	R/W	0	USER command DO bit. 1 = user command includes data output. 0 = no data output. If both DIN and DO are valid, SPI master is firstly in data output state and then in data input state. If all of DUMMY, DO and DIN are valid, SPI master is firstly in data output state and then in dummy state, finally in data input state.

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Bit(s)	R/W	Default	Description
26	R/W	0	USER command dummy idle bit. 1= no SPI clock toggling in dummy state. 0= normal
25	R/W	0	USER command highpart bit for SPI_DOUT stage. It is for data-output in spi master mode and for data-input in spi slave mode. 1 = only high half part of buffer are used. 0 = low half part or the whole 64bytes are used.
24	R/W	0	USER command highpart bit for SPI_DIN stage. It is for data-input in spi master mode and for data-output in spi slave mode. 1 = only high half part of buffer are used. 0 = low half part or the whole 64bytes are used.
23	R/W	0	User command external hold bit for prep. 1 = in prep state, SPI master controller can be hold by the external pin SPI_HOLD
22	R/W	0	User command external hold bit for command. 1 = in command state, SPI master controller can be hold by the external pin SPI_HOLD
21	R/W	0	User command external hold bit for address. 1 = in address state, SPI master controller can be hold by the external pin SPI_HOLD
20	R/W	0	User command external hold bit for dummy. 1 = in dummy state, SPI master controller can be hold by the external pin SPI_HOLD
19	R/W	0	User command external hold bit for data input. 1 = in data input state, SPI master controller can be hold by the external pin SPI_HOLD
18	R/W	0	User command external hold bit for data output. 1 = in data output state, SPI master controller can be hold by the external pin SPI_HOLD
17	R/W	1	User command external hold polarity bit. 1 = high is valid for hold, 0 = low is valid for hold.
16	R/W	0	Single DIO mode: Data output and input apply only 1 wire.
15	R/W	0	Fast write QIO mode.
14	R/W	0	Fast write DIO mode.
13	R/W	0	Fast write QOUT mode.
12	R/W	0	Fast write DOUT mode.
11	R/W	0	Write byte order. 0 = d[7:0], d[15:8], d[23:16], d[31:24]. 1 = d[31:24], d[23:16], d[15:8], d[7:0]
10	R/W	0	Read byte order. . 0 = d[7:0], d[15:8], d[23:16], d[31:24]. 1 = d[31:24], d[23:16], d[15:8], d[7:0]
9:8	R/W	0	AHB endian mode: 0= little-endian; 1= big-endian; 2~3 reserved
7	R/W	0	In SPI master mode, the clock output edge bit: 0 = SPI_CK is inverted, 1 = SPI_CK is not inverted
6	R/W	1	In SPI slave mode, the clock input edge bit: 0 = SPI_CK_I is inverted, 1 = SPI_CK_I is not inverted
5	R/W	0	SPI CS setup bit: 1 = valid in prep state
4	R/W	0	SPI CS hold bit: 1 = valid in done state
3	R/W	0	AHB-read apply the configurations of user-command, such as command value, bit-length,…
2	R/W	1	Backward Compatible: 1 = compatible to Apollo SPI This bit affect the three registers: “SPI Flash Commmand Register”, “SPI Address Register” and “SPI Control Register”

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Bit(s)	R/W	Default	Description
1	R/W	0	AHB-read support 4byte address, when AHB-read apply the configurations of user-command. 1 = 4byte address, 0 = 3byte address
0	R/W	0	In SPI master mode, Enable bit for Data input during SPI_DOUT stage. 1 = enable; 0 = disable This bit shall not be used in 2/4wire or SIO. When this bit is 1, during SPI_DOUT stage, data input are stored into cacheline/ buffer from address 0, i.e., Bit24 is not controlling the start address. The data output can be specified by bit25.

Table 12-387 SPI_FLASH_USER1 0xfe056020

Bit(s)	R/W	Default	Description
31:26	R/W	0	USER command bit number for address state 0 = 1 bit, 1= 2 bits, …
25:17	R/W	0	USER command bit number for data output state 0 = 1 bit, 1= 2 bits, …
16:8	R/W	0	USER command bit number for data input state 0 = 1 bit, 1= 2 bits, …
7:0	R/W	0	USER command cycle number for dummy state 0 = 1 cycle, 1= 2 cycles, …

Table 12-388 SPI_FLASH_USER2 0xfe056024

Bit(s)	R/W	Default	Description
31:28	R/W	0	USER command bit number for command state 0 = 1 bit, 1= 2 bits, …
27:16	R/W	0	Reserved
15:0	R/W	0	The command content of the user command

Table 12-389 SPI_FLASH_USER3 0xfe056028

Bit(s)	R/W	Default	Description
31:0	R/W	0	In SPI Master mode, the address[63:32] of the user command In SPI Slave mode, the write status of the user command

Table 12-390 SPI_FLASH_USER4 0xfe05602c

Bit(s)	R/W	Default	Description
31	R/W	0	Pin swap when it is in DIN stage and SPI data input are 4wire. This feature is for Ubec Zigbee chips. 1 = swap between {spi_q, spi_d_i} and {spi_hold_i, spi_wp_i} 0 = normal
30	R/W	0	In SPI Master mode, CS keep active after a transition. 1 = enable; 0 = disable
29	R/W	0	Idle edge of SPI_CK 0 = low when it is idle 1 = high when it is idle

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Bit(s)	R/W	Default	Description
28:24	R/W	0	Reserved
23	R/W	0	In the SPI slave mode, spi_cs_i polarity: 1= high voltage is active 0= low voltage is active
22:21	R/W	0	In the SPI slave mode, spi_ck_i and spi_cs_i source pins 0=SPI_CK and SPI_CS pins, respectively 1=SPI_CS2 and SPI_CS1 pins, respectively 2=SPI_HOLD and SPI_WP pins, respectively
20	R/W	0	SPI_CS2 and SPI_CS1 pin function MUX 0= spi_ck and spi_cs in the SPI master mode 1= input pads for spi_ck_i and spi_cs_i, respectively, in the SPI slave mode
19	R/W	0	SPI_CK and SPI_CS pin function MUX 0= spi_ck and spi_cs in the SPI master mode 1= input pads for spi_ck_i and spi_cs_i, respectively, in the SPI slave mode
18:17	R/W	0	SPI_HOLD and SPI_WP pin function MUX 0= normal 1= spi_q and spi_d, respectively 2= spi_cs3 and spi_cs2, repectively 3= input pads for spi_ck_i and spi_cs_i, respectively, in the SPI slave mode
16	R/W	0	SPI_D and SPI_Q switch 1= SPI_D and SPI_Q pin-functions are swapped 0= normal
15:11	R/W	0	In Master mode, these are spi_ck MUX bit[4:0] for spi_cs4 (SPI_HOLD pin), spi_cs3 (SPI_WP pin), spi_cs2, spi_cs1 and spi_cs, respectively 1= this pin is spi_ck, if this pin is not idle 0= this pin is spi_cs, if this pin is not idle
10:6	R/W	0	In Master mode, these are polarity bit[4:0] for spi_cs4 (SPI_HOLD pin), spi_cs3 (SPI_WP pin), spi_cs2, spi_cs1 and spi_cs, respectively 1= high voltage is active 0= low voltage is active
5:0	R/W	0x1E	In Master mode, these are idle bit[5:0] for SPI_CK, for spi_cs4 (SPI_HOLD pin), spi_cs3 (SPI_WP pin), spi_cs2, spi_cs1 and spi_cs, respectively 1= idle, i.e., the spi_ck signal is 0 or the spi_cs is at the inactive level 0= active if SPI controller is working

Table 12-391 SPI_FLASH_SLAVE 0xfe056030

Bit(s)	R/W	Default	Description
31	R/W	0	SPI controller SW reset: 1 = reset, 0 = none
30	R/W	0	SPI slave mode: 1 = slave, 0 = master
29	R/W	0	In SPI slave mode, the enable bit for the command of write-buffer-and-read-buffer 0= disable, 1=enable
28	R/W	0	In SPI slave mode, the enable bit for the command of write-status-and-read-status 0= disable, 1=enable
27	R/W	0	SPI slave command define enable 0=Apply the last 3bits of Flash commands and two extra command. 1=Apply the user defined command in SPI Slave register 3
26:4	R/W	0	Reserved
11:10	R/W	0	spi_cs_i recovery mode: 0= and

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Bit(s)	R/W	Default	Description
			1= or 2= normal 3= delayed
9:5	R/W	0	Interrupt enable for bit4:0 1= enable, 0=disable
4	R/W	0	A SPI transition is done. (whatever it is in SPI master mode or SPI slave mode)
3	R/W	0	In SPI slave mode, a status write is done
2	R/W	0	In SPI slave mode, a status read is done
1	R/W	0	In SPI slave mode, a buffer write is done
0	R/W	0	In SPI slave mode, a buffer read is done

Table 12-392 SPI_FLASH_SLAVE1 0xfe056034

Bit(s)	R/W	Default	Description
31:27	R/W	0	In SPI slave mode, status bit number 0 = 1 bit, 1= 2 bits, …
26	R/W	0	In SPI slave mode, status fast read/write enable bit: 1 = enable, 0 = disable
25	R/W	0	In SPI slave mode, status read back enable bit: 1 = reading status is written status in SPI User register 3, 0 = reading status is in SPI Status register.
24:16	R/W	0	In SPI slave mode, buffer bit number 0 = 1 bit, 1= 2 bits, …
15:10	R/W	0	In SPI slave mode, address bit number for reading buffer 0 = 1 bit, 1= 2 bits, …
9:4	R/W	0	In SPI slave mode, address bit number for writing buffer 0 = 1 bit, 1= 2 bits, …
3	R/W	0	In SPI slave mode, dummy enable bit for writing status 1=enable, 0=disable
2	R/W	0	In SPI slave mode, Dummy enable bit for reading status 1=enable, 0=disable
1	R/W	0	In SPI slave mode, Dummy enable bit for writing buffer 1=enable, 0=disable
0	R/W	0	In SPI slave mode, Dummy enable bit for reading buffer 1=enable, 0=disable

Table 12-393 SPI_FLASH_SLAVE2 0xfe056038

Bit(s)	R/W	Default	Description
31:24	R/W	0	In SPI slave mode, Dummy cycle number for writing buffer 0 = 1 cycle, 1= 2 cycles, …
23:16	R/W	0	In SPI slave mode, Dummy cycle number for reading buffer 0 = 1 cycle, 1= 2 cycles, …
15:8	R/W	0	In SPI slave mode, Dummy cycle number for writing status 0 = 1 cycle, 1= 2 cycles, …
7:0	R/W	0	In SPI slave mode, Dummy cycle number for reading status 0 = 1 cycle, 1= 2 cycles, …

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Table 12-394 SPI_FLASH_SLAVE3 0xfe05603c

Bit(s)	R/W	Default	Description
31:24	R/W	0	In SPI slave mode, Command value for writing status, when bit27 “SPI slave command define enable” in SPI Slave register is 1
23:16	R/W	0	In SPI slave mode, Command value for reading status, when bit27 “SPI slave command define enable” in SPI Slave register is 1
15:8	R/W	0	In SPI slave mode, Command value for writing buffer, when bit27 “SPI slave command define enable” in SPI Slave register is 1
7:0	R/W	0	In SPI slave mode, Command value for reading buffer, when bit27 “SPI slave command define enable” in SPI Slave register is 1

Table 12-395 SPI_FLASH_C0~7 0xfe056040~0xfe05605c

Bit(s)	R/W	Default	Description
31:0	R/W	0	Cache line Word 0~7. Cache is used to read data both for AHB or APB read command. Cache is also used for APB page programming etc.

Table 12-396 SPI_FLASH_B8~15 0xfe056060~0xfe05607c

Bit(s)	R/W	Default	Description
31:0	R/W	0	Buffer Word 8. Buffer is used to read/write data only for APB read/write user commands.

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13 I/O Interface

13.1 Universal Serial Bus

13.1.1 Overview

The chip integrates one USB Host and one USB OTG.

13.1.2 Features

The USB2.0 OTG controller features

- Support for the following speeds: High-Speed (HS, 480-Mbps),Full-Speed (FS, 12-Mbps) and Low-Speed (LS, 1.5-Mbps) modes.
- Multiple DMA/non DMA mode access support on the application side.
- Supports up to 16 bidirectional endpoints, including control endpoint 0.
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP).
- Supports up to 16 host channels.
- Supports ACA ID detector, refer to Amlogic USB2.0 OTGID Detector Specification.pdf for detail.

The USB2.0 Host controller features:

- Support for the following speeds: High-Speed (HS, 480-Mbps),Full-Speed (FS, 12-Mbps) and Low-Speed (LS, 1.5-Mbps) modes.
- Multiple DMA/non DMA mode access support on the application side.
- Supports up to 16 host channels.

The USB2.0 PHY features:

- Support for the following speeds: High-Speed (HS, 480-Mbps),Full-Speed (FS, 12-Mbps) and Low-Speed (LS, 1.5-Mbps) modes.

13.1.3 Register Description

Base address:

PHY 20: 0xfe03c000.

PHY 21: 0xfe03e000.

For the following registers, each register's final address= base address + offset *4.

Table 13-1 reg32_00 0x00

Bit(s)	R/W	Default	Description
31:15	R/W	0	reserved
14	R/W	1	reset_FS_LS_Clock_Divider
13	R/W	1	reset_HS_CDR
12	R/W	1	reset_FS_LS_CDR
11:10	R/W	0	reg32_00_11_10_reserved
9:8	R/W	0	reserved
7	R/W	0	usb2_cal_pd

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Bit(s)	R/W	Default	Description
6:4	R/W	0	reserved
3	R/W	0	usb2_rx_fsls_pd
2:1	R/W	0	reserved
0	R/W	0	usb2_tx_hs_pd

Table 13-2 reg32_01 0x04

Bit(s)	R/W	Default	Description
31:24	R/W	0	TBD_3
23:16	R/W	0	TBD_2
15:10	R/W	0	TBD_1
9:2	R/W	0	tx_cfg[7:0]
1:0	R/W	0x0	reserved

Table 13-3 reg32_02 0x08

Bit(s)	R/W	Default	Description
31	RO	0	Phy_status
30	RO	0	cal_en_flag
29:27	RO	0	reg32_02_29_27_reserved
26	RO	0	HS_Disconnect_Status
25	RO	0	HS_Squelch_Status
24	RO	0	PRBS_Sync_Out
23:16	RO	0	Calibration_code_Value_23_16
15:8	RO	0	Calibration_code_Value_15_8
7:0	RO	0	Calibration_code_Value_7_0

Table 13-4 reg32_03 0x0c

Bit(s)	R/W	Default	Description
31:24	R/W	0	TBD_7
23:16	R/W	0	TBD_6
15:8	R/W	0	TBD_5
7:4	R/W	0x2	TBD_4
4:2	R/W	0x1	usb2_disc_trim
2:0	R/W	0	usb2_squelch_trim

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Table 13-5 reg32_04 0x10

Bit(s)	R/W	Default	Description
31:30	R/W	0	i_c2l_bias_trim_3_2
29:28	R/W	0	i_c2l_bias_trim_1_0
27	R/W	0	TEST_Bypass_mode_enable
26	RO	0	i_c2l_cal_done
25	R/W	0	i_c2l_cal_reset_n
24	R/W	0	i_c2l_cal_en
23:16	R/W	0	Calibration_code_Value_23_16
15:8	R/W	0	Calibration_code_Value_15_8
7:0	R/W	0	Calibration_code_Value_7_0

Table 13-6 reg32_05 0x14

Bit(s)	R/W	Default	Description
31:24	R/W	0	i_c2l_obs_7_0
23:22	R/W	0	reg32_05_23_22_reserved
21:20	R/W	0	i_c2l_pll_perfcfg_21_20
19	R/W	0x1	i_c2l_pll_perfcfg_19
18:16	R/W	0	i_c2l_pll_perfcfg_18_16
15:12	R/W	0	i_c2l_pll_perfcfg_15_12
11:10	R/W	0	i_c2l_pll_perfcfg_11_10
9	R/W	0x1	i_c2l_pll_perfcfg_9 (pll_reset)
8	R/W	0x1	i_c2l_pll_perfcfg_8
7:4	R/W	0x7	i_c2l_pll_perfcfg_7_4
3:2	R/W	0x3	i_c2l_pll_perfcfg_3_2
1:0	R/W	0	i_c2l_pll_perfcfg_1_0

Table 13-7 reg32_06 0x18

Bit(s)	R/W	Default	Description
31	R/W	0x1	hub_extra_bit_cntr
30:24	R/W	0	cntr_timeout
23	R/W	0	Internal_loopback
22	R/W	0	reg32_06_22_reserved
21	R/W	0	PCS_Reset_Transmit_State_machine
20	R/W	0	PCS_Reset_Receive_State_machine
19:16	R/W	0xf	fsls_farend_device_disconnect_micro_second_count_11_8

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Bit(s)	R/W	Default	Description
15:12	R/W	0xa	reg32_06_15_12_reserved
11:8	R/W	0	bypass_disc_cntr_3_0
7:0	R/W	0x17	PCS_microsecond_timer_done_count_value_7_0

Table 13-8 reg32_07 0x1c

Bit(s)	R/W	Default	Description
31:24	RO	0	Prbs_Error_count
23:21	R/W	0	reg32_07_23_21_reserved
20:17	R/W	0xf	RX_ERROR_Turn_Around_Timer_Count
16	R/W	0	acceptable_bit_drops
15	R/W	0	host_tristate
14:12	R/W	0x4	fs_ls_minimum_count
11:8	R/W	0xf	cntr_done_value_7_4
7:4	R/W	0xf	cntr_done_value_3_0
3:0	R/W	0	HS_CDR_internal_tap_select

Table 13-9 reg32_08 0x20

Bit(s)	R/W	Default	Description
31:24	R/W	0	Custom_Pattern_2
23:16	R/W	0	Custom_Pattern_1
15:8	R/W	0x4	Custom_Pattern_0
7	R/W	0	Enable_RX_ERROR_Timeout_Mode
6	R/W	0	reset_us_timer
5	R/W	0	PRBS_ERROR_Insert
4	R/W	0	PRBS_comparison_enable
3	R/W	0	PRBS_Enable
2:0	R/W	0	pattern

Table 13-10 reg32_09 0x24

Bit(s)	R/W	Default	Description
31:24	R/W	0	Custom_Pattern_6
23:16	R/W	0	Custom_Pattern_5
15:8	R/W	0	Custom_Pattern_4
7:0	R/W	0	Custom_Pattern_3

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Table 13-11 reg32_10 0x28

Bit(s)	R/W	Default	Description
31:24	R/W	0	Custom_Pattern_10
23:16	R/W	0	Custom_Pattern_9
15:8	R/W	0	Custom_Pattern_8
7:0	R/W	0	Custom_Pattern_7

Table 13-12 reg32_11 0x2c

Bit(s)	R/W	Default	Description
31:24	R/W	0	Custom_Pattern_14
23:16	R/W	0	Custom_Pattern_13
15:8	R/W	0	Custom_Pattern_12
7:0	R/W	0	Custom_Pattern_11

Table 13-13 reg32_12 0x30

Bit(s)	R/W	Default	Description
31:24	R/W	0	Custom_Pattern_18
23:16	R/W	0	Custom_Pattern_17
15:8	R/W	0	Custom_Pattern_16
7:0	R/W	0	Custom_Pattern_15

Table 13-14 reg32_13 0x34

Bit(s)	R/W	Default	Description
31	R/W	0	reg32_13_31_reserved
30	R/W	0	bypass_reg[6]:i_c2l_fsls_rx_en
29	R/W	0	bypass_reg[5]:i_c2l_hs_rx_en
28	R/W	0	bypass_reg[4]:i_c2l_fs_oe
27	R/W	0	bypass_reg[3]:i_c2l_hs_oe
26	R/W	0	bypass_reg[2]:i_c2l_ls_en
25	R/W	0	bypass_reg[1]:i_c2l_fs_en
24	R/W	0	bypass_reg[0]:i_c2l_hs_en
23	R/W	0	Bypass_Host_Disconnect_Enable
22	R/W	0	Bypass_Host_Disconnect_Value
21	R/W	0	Clear_Hold_HS_disconnect
20:16	R/W	0x8	minimum_count_for_sync_detection
15	R/W	0	Update_PMA_signals

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Bit(s)	R/W	Default	Description
14	R/W	0	load_stat
13:8	R/W	0	reg32_13_13_8_reserved
7:0	R/W	0	Custom_Pattern_19

Table 13-15 reg32_14 0x38

Bit(s)	R/W	Default	Description
31:24	R/W	0x03	usb2_reg_cfg
23:16	R/W	0	Bypass_ctrl_15_8 bypass_ctrl[8]: bypass i_rpd_en bypass_ctrl[9]: bypass i_rpu_sw2_en bypass_ctrl[10]: i_rpu_sw1_en bypass_ctrl[11]: reserved bypass_ctrl [12]: pg_rstn bypass_ctrl[13]: pg_data_16_8 bypass_ctrl[14]: assert_se0
15:8	R/W	0	Bypass_ctrl_7_0 bypass_ctrl[0]: hs bypass_ctrl[1]: fs bypass_ctrl[2]: ls bypass_ctrl[3]:hs_out_en bypass_ctrl[4]:fsls_out_en bypass_ctrl[5]:hs_rx_en bypass_ctrl [6]:hls_rx_en
7	R/W	0	reg32_14_7_reserved
6	R/W	0	i_c2l_assert_single_enable_zero
5	R/W	0	i_c2l_data_16_8
4	R/W	0	pg_rstn
3:2	R/W	0	bypass_reg[11:10]:i_rpu_sw1_en
1	R/W	0	bypass_reg[9]:i_rpu_sw2_en
0	R/W	0	bypass_reg[8]: i_rpd_en

Table 13-16 reg32_15 0x3c

Bit(s)	R/W	Default	Description
31:29	R/W	0	reg32_15_31_29_reserved
28:16	R/W	0xfa0	ms_4_cntr
15:8	R/W	0x3c	non_se0_cntr
7:0	R/W	0x3c	se0_cntr

Table 13-17 reg32_16 0x40

Bit(s)	R/W	Default	Description
31	RO	0	usb2_mppll_lock_dig
30	RO	0	usb2_mppll_lock
29	R/W	0	usb2_mppll_reset
28	R/W	0	usb2_mppll_en
27	R/W	0x1	usb2_mppll_fast_lock
26	R/W	0	usb2_mppll_lock_f
25:24	R/W	0x1	usb2_mppll_lock_long

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Bit(s)	R/W	Default	Description
23	R/W	0	usb2_mppll_dco_sdm_en
22	R/W	0x1	usb2_mppll_load
21	R/W	0	usb2_mppll_sdm_en
20	R/W	0	usb2_mppll_tdc_mode
19:15	R/W	0	reg32_16_19_15_reserved
14:10	R/W	0x1	usb2_mppll_n
9	R/W	0	reg32_16_9_reserved
8:0	R/W	0x14	usb2_mppll_m

Table 13-18 reg32_17 0x44

Bit(s)	R/W	Default	Description
31:28	R/W	0x9	usb2_mppll_filter_pvt1
27:24	R/W	0x2	usb2_mppll_filter_pvt2
23	R/W	0	usb2_mppll_filter_mode
22:20	R/W	0x7	usb2_mppll_lambda0
19:17	R/W	0x7	usb2_mppll_lambda1
16	R/W	0	usb2_mppll_fix_en
15:14	R/W	0	reg32_17_15_14_reserved
13:0	R/W	0	usb2_mppll_frac_in

Table 13-19 reg32_18 0x48

Bit(s)	R/W	Default	Description
31	R/W	0	usb2_mppll_acg_range
30:29	R/W	0x3	usb2_mppll_adj_ldo
28:26	R/W	0x3	usb2_mppll_alpha
25:24	R/W	0x1	usb2_mppll_bb_mode
23:22	R/W	0x1	usb2_mppll_bias_adj
21:19	R/W	0x3	usb2_mppll_data_sel
18:16	R/W	0x3	usb2_mppll_rou
15:14	R/W	0	usb2_mppll_pfd_gain
13	R/W	0x1	usb2_mppll_dco_clk_sel
12	R/W	0	usb2_mppll_dco_m_en
11:6	R/W	0x27	usb2_mppll_lk_s
5:2	R/W	0x9	usb2_mppll_lk_w
1:0	R/W	0x1	usb2_mppll_lkw_sel

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Table 13-20 reg32_19 0x4c

Bit(s)	R/W	Default	Description
31	RO	0	usb2_mppll_lock_dig
30	RO	0	usb2_mppll_lock
29:10	RO	0	reg32_19_29_10_reserved
9:0	RO	0	usb2_mppll_reg_out

Table 13-21 reg32_20 0x50

Bit(s)	R/W	Default	Description
31	R/W	0	bypass_cal_done_r5
30:29	R/W	0	usb2_bgr_dbg_1_0
28:24	R/W	0	usb2_bgr_vref_4_0
23:22	R/W	0	squelch_sel: 01: debounce 1; 10: debounce 2; 00/11: no debounce
21	R/W	0	usb2_bgr_start
20:16	R/W	0	usb2_bgr_adj_4_0
15:14	R/W	0	usb2_edgedrv_trim_1_0
13	R/W	0	usb2_edgedrv_en
12:9	R/W	0xf	usb2_dmon_sel_3_0
8	R/W	0	usb2_dmon_en
7	R/W	0	bypass_otg_det
6	R/W	0	usb2_cal_code_r5
5	R/W	0	usb2_amon_en
4	R/W	0x0	usb2_otg_vbusdet_en
3:1	R/W	0x4	usb2_otg_vbus_trim_2_0
0	R/W	0	usb2_otg_iddet_en

Table 13-22 reg32_21 0x54

Bit(s)	R/W	Default	Description
31:26	R/W	0	bypass_chirp_reg [30]: bypass hs chirpK reg [31]: bypass hs term_sel reg
29:28	R/W	0	bypass_chirp_ctrl [28]: bypass hs chirpK [29]: bypass hs term_sel
27:26	R/W		reg32_21_27_26_reserved
25:20	R/W	0	bypass_utmi_reg [21:20]: xcvr_select ctrl reg [22]: term_select ctrl reg [23]: suspend ctrl reg [25:24]: opmode ctrl reg
19:16	R/W	0	bypass_utmi_cntr [16]: bypass xcvr_select [17]: bypass term_select [18]: bypass suspend [19]: bypass opmode
15:8	R/W	0	hs cdr ctrl

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Bit(s)	R/W	Default	Description
7	R/W		hs cdr sel
6	R/W		reg32_21_6_reserved
5:4	R/W	0x2	usb2_otg_aca_trim_1_0
3	R/W	0	usb2_tx_strg_pd
2	R/W	0x0	usb2_otg_aca_en
1	R/W	0x1	usb2_cal_ack_en
0	R/W	0	usb2_bgr_force

Table 13-23 reg32_22 0x58

Bit(s)	R/W	Default	Description
31:14	RO	0	reg32_22_31_14_reserved
[13:6]			hs cdr state
5:3	RO	0	usb2_otg_aca_iddig
2	RO	0	usb2_otg_vbus_vld
1	RO	0	usb2_otg_sess_vld
0	RO	0	usb2_otg_id_dig

Table 13-24 reg32_23 0x5c

Bit(s)	R/W	Default	Description
31:16	RO	0	test_bus_data_int_15_0
15:13		0	ldo_trim
12		1	ldo_en
11		0	new_hs_disc_ctrl[1]
10		0	new_hs_disc_ctrl[0]
9		0	sel_cdr
8		0	pcs_sel
7	R/W	0	orw_test_bus_en
6:1	R/W	0	orw_test_bus_sel_5_0
0	R/W	0	orw_usb2_bgr_en

13.2 Ethernet

13.2.1 Overview

The Ethernet MAC controller provides a complete Ethernet interface from the chip to a Reduced Media Independent Interface(RMII) compliant Ethernet PHY.

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13.2.2 Ethernet Top Registers

Base address: 0xFE024000

Table 13-25 ETHTOP_CNTL0 0x0

Bit(s)	R/W	Default	Description
31	R/W	0	eth_urgent 1: set AHB to DDR interface as urgent
30	R/W	0	clock source select for rgmii_tx_clk 1: use rx_clk as tx_clk
29:27	R/W	0	cali_sel RMII mode Select one signal from {RXDV, RXD1:0} to calibrate.
26	R/W	0	cali_rise RMII mode 0: test falling edge 1: test rising edge
25	R/W	0	cali_start RMII mode Start calibration logic
24:20	R/W	0	adj_skew RMII mode 5 bits correspondent to {RXDV, RXD1:0}, set to 1 will delay the data capture by 1 cycle(fast clock).
19:15	R/W	0	adj_delay Set bit14 to 0. RMII mode Capture input data at clock index equal to adj_delay.
14	R/W	0	adj_setup Set RXDV and RXD setup time, data is aligned with index 0. When set to 1, auto delay and skew
13	R/W	0	adj_enable RMII mode Enable data delay adjustment and calibration logic.
12	R/W	0	clk_en RMII mode Enable TX_CLK and PHY_REF_CLK generator.
11	R/W	0	clk_rmii_i_invert RMII mode Use inverted internal clk_rmii_i to generate 25/2.5 tx_rx_clk.
9:7	R/W	0	rgmii_tx_clk_ratio RMII mode, 000: invalid value. 001: clk_m250 is 250MHz. 010: clk_m250 is 500MHz. 100: clk_m250 is 1000MHz. clk_m250 is “ratio” *250MHz.
6:5	R/W	0	rgmii_tx_clk phase select RMII mode, TX_CLK related to TXD 00: clock delay 0 cycle. 01: clock delay ¼ cycle. 10: clock delay ½ cycle. 11: clock delay ¾ cycle.
4	R/W	0	clock source select for rgmii_tx_clk

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Bit(s)	R/W	Default	Description
			0: clk_m250_src0(fclk_div2) 1: clk_m250_src1(fclk_div4)
3	R/W	0	invert control for rx_clk_or_clk_rmii_i RMII mode CLK_RMII Use inverted signal when set to 1.
2:0	R/W	0	PHY Interface Select Function: These pins select one of the multiple PHY interfaces of MAC. This is sampled only during reset assertion and ignored after that. 3'b100: RMII 3'b000: MII

Table 13-26 ETHTOP_CNTL1 0x4

Bit(s)	R/W	Default	Description
25:21	R/W	0	cfg_txclk_dly Add delay to input TX_CLK for better timing
20:16	R/W	0	cfg_rxclk_dly Add delay to input RX_CLK for better timing
15	R		cali_vld the result is valid
14	R		cali_rise The results is rising edge test or falling edge test.
13:11	R		cali_sel The signal under test.
10	R		cali_act The Calibration logic is waiting for event.
9:5	R		cali_len The RX_CLK length in 1ns.
4:0	R		cali_idx Signal switch position in 1ns.

13.2.3 Ethernet MAC

13.2.3.1 Features

Ethernet MAC has the following features:

- 10/100 MAC 3.70a
- RMII
- AHB 32 Bits internal bus
- RX FIFO 4KB, TX FIFO 2KB
- 2 MAC addresses
- EEE
- Power Management

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13.2.3.2 Register Description

Table 13-27 PRG_ETH_REG0 0xff634540

Bit(s)	R/W	Default	Description
31	R/W	0	Set AHB to DDR interface as urgent.
30	R/W	0	Use RX_CLK as TX_CLK.
29-27	R/W	0	RMII mode Select one signal from {RXDV, RXD[1:0]} to calibrate.
26	R/W	0	RMII mode 0: test falling edge 1: test rising edge
25	R/W	0	RMII mode Start calibration logic
24-20	R/W	0	RMII mode 5 Bits correspondent to {RXDV, RXD[1:0]}, set to 1 will delay the data capture by 1 cycle.
19-15	R/W	0	Set bit14 to 0. RMII mode Capture input data at clock index equal to adj_delay.
14	R/W	0	Set RXDV and RXD setup time, data is aligned with index 0. When set to 1, auto delay and skew
13	R/W	0	RMII mode Enable data delay adjustment and calibration logic.
12	R/W	0	RMII mode Enable TX_CLK and PHY_REF_CLK generator.
11	R/W	0	RMII mode Use inverted internal clk_rmii_i to generate 25/2.5 tx_rx_clk.
10	R/W	0	Generate 25MHz clock for PHY
9-7	R/W	0	RMII mode, 000: invalid value. 001: mp2_clk_out is 250MHz. 010: mp2_clk_out is 500MHz. … Mp2_clk_out is “ratio” *250MHz.
6-5	R/W	0	RMII mode, TX_CLK related to TXD 00: clock delay 0 cycle. 01: clock delay ¼ cycle. 10: clock delay ½ cycle. 11: clock delay ¾ cycle.
4	R	0	Unused
3	R/W	0	RMII mode CLK_RMII Use inverted signal when set to 1.
2	R/W	0	Sideband Descriptor Endianness Control Function: When set high, this signal configures the DMA to transfer descriptors in reverse endianness of the data format. When low (by default), the descriptors are transferred in the same endian format as the data. This signal is sampled during active reset (including soft-reset) only and ignored after reset is de-asserted.

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Bit(s)	R/W	Default	Description
1	R/W	0	Sideband Data Endianness Control Function: When set high, this signal configures the DMA to transfer data in big-endian format. When low (by default), the data is transferred in little-endian format. This signal is sampled during active reset (including soft-reset) only and ignored after reset is de-asserted.
0	R/W	0	PHY Interface Select Function: These pins select one of the multiple PHY interfaces of MAC. This is sampled only during reset assertion and ignored after that. 0: internal value 100: RMII

Table 13-28 PRG_ETH_REG1 0xff634544

Bit(s)	R/W	Default	Description
31-16	R	0	Unused
15	R/W	0	The result is valid
14	R/W	0	The results is rising edge test or falling edge test.
13-11	R/W	0	The signal under test.
10	R/W	0	The Calibration logic is waiting for event.
9-5	R/W	0	The RX_CLK length in 1ns.
4-0	R/W	0	Signal switch position in 1ns.

13.2.4 Ethernet PHY

13.2.4.1 Features

Ethernet PHY has the following features:

- Integrated IEEE 802.3/802.3u compliant 10/100Mbps Ethernet PHY
- Supporting both full and half-duplex for either 10 or 100 Mb/s data rate
- Auto MDIX capable
- Supports wake-on-LAN
- 100 Base-T support
- MII/RMII/SMII interface
- Supports auto-negotiation
- Full set of power down modes
- Interface available to 100Base-FX Fiber-PMD
- Serial Management Interface (SMI)
- Fix configurations for LED status indicators
- Supporting military temperature range -20℃ to 80℃
- Perfect mix of analog and digital lends itself to robustness, portability, and performance
- Multiple input clock options
- Stand-alone core

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13.2.4.2 Register Description

Base Address: 0xFE028000

Table 13-29 ETH_PHY_DBG_CTL0 0x0

Bit(s)	R/W	Default	Description
7:0	R/W	0	ETH digital debug registers

Table 13-30 ETH_PHY_DBG_CTL1 0x4

Bit(s)	R/W	Default	Description
23:0	R/W	0	ETH digital debug registers

Table 13-31 ETH_PHY_DBG_CFG0 0x8

Bit(s)	R/W	Default	Description
31:0	R/W	0	ETH digital debug registers

Table 13-32 ETH_PHY_DBG_CFG1 0xc

Bit(s)	R/W	Default	Description
31:0	R/W	0	ETH digital debug registers

Table 13-33 ETH_PHY_DBG_CFG2 0x10

Bit(s)	R/W	Default	Description
31:0	R/W	0	ETH digital debug registers

Table 13-34 ETH_PHY_DBG_CFG3 0x14

Bit(s)	R/W	Default	Description
31:0	R/W	0	ETH digital debug registers

Table 13-35 ETH_PHY_DBG_CFG4 0x18

Bit(s)	R/W	Default	Description
31:0	R/W	0	ETH digital debug registers

Table 13-36 ETH_PLL_STS 0x40

Bit(s)	R/W	Default	Description
31	R		eth_mppll_lock
30	R		eth_mppll_lock_dig

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Bit(s)	R/W	Default	Description
29:10	R		reserved
9:0	R		eth_mppll_reg_out

Table 13-37 ETH_PLL_CTL0 0x44

Bit(s)	R/W	Default	Description
31	R		eth_mppll_lock
30	R		eth_mppll_lock_dig
29	R/W		eth_mppll_reset
28	R/W		eth_mppll_en
27	R/W		eth_mppll_fast_lock
26	R/W		eth_mppll_lock_f
25:24	R/W		eth_mppll_lock_long
23	R/W		eth_mppll_sel_ref
22	R/W		eth_mppll_load
21	R/W		eth_mppll_sdm_en
20	R/W		eth_mppll_tdc_mode
19:15	R/W		reserved
14:10	R/W		eth_mppll_n
9	R/W		reserved
8:0	R/W		eth_mppll_m

Table 13-38 ETH_PLL_CTL1 0x48

Bit(s)	R/W	Default	Description
31:28	R/W		eth_mppll_filter_pvt1
27:24	R/W		eth_mppll_filter_pvt2
23	R/W		eth_mppll_filter_mode
22:20	R/W		eth_mppll_lambda0
19:17	R/W		eth_mppll_lambda1
16	R/W		eth_mppll_fix_en
15:14	R/W		reserved
13:0	R/W		eth_mppll_frac_in

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Table 13-39 ETH_PLL_CTL2 0x4C

Bit(s)	R/W	Default	Description
31	R/W		eth_mppll_acq_range
30:29	R/W		eth_mppll_adj_ldo
28:26	R/W		eth_mppll_alpha
25:24	R/W		eth_mppll_bb_mode
23:22	R/W		eth_mppll_bias_adj
21:19	R/W		eth_mppll_data_sel
18:16	R/W		eth_mppll_rou
15:14	R/W		eth_mppll_pfd_gain
13	R/W		eth_mppll_dco_clk_sel
12	R/W		eth_mppll_dco_m_en
11:6	R/W		eth_mppll_lk_s
5:2	R/W		eth_mppll_lk_w
1:0	R/W		eth_mppll_lkw_sel

Table 13-40 ETH_PLL_CTL3 0x50

Bit(s)	R/W	Default	Description
31:1	R		reserved
0	R/W		eth_mppll_dco_sdm_en

Table 13-41 ETH_PLL_CTL4 0x54

Bit(s)	R/W	Default	Description
31:0	R/W		reserved
0	R/W	0	led_cfg_1

Table 13-42 ETH_PLL_CTL5 0x58

Bit(s)	R/W	Default	Description
31:16	R/W	0	ETH_PHY_RXADC0
15:3	R/W	0	ETH_PHY_CTLIO
2:0	R/W	0	reserved

Table 13-43 ETH_PLL_CTL6 0x5C

Bit(s)	R/W	Default	Description
31:16	R/W	0	reserved
15:0	R/W	0	ETH_PHY_RXSQLD

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Table 13-44 ETH_PLL_CTL7 0x60

Bit(s)	R/W	Default	Description
31:16	R/W	0	reserved
15:0	R/W	0	ETH_PHY_RXADC1

Table 13-45 ETH_PHY_CNTL0 0x80

Bit(s)	R/W	Default	Description
31:16	R/W	0	co_reg3_oui_in, SMI register 3 default value
15:0	R/W	0	co_reg2_oui_in, SMI register 2 default value

Table 13-46 ETH_PHY_CNTL1 0x84

Bit(s)	R/W	Default	Description
31:24	R/W	0	led_cfg {led_cfg_1,led_cfg[7:5]}: co_activity_led output select 0: link_led & (~activity) 1: link_led 2: link_led & activity 3: link_led | activity 4: activity 5: rx_led 6: tx_led 7: duplex_led 8: link_led | (~activity) led_cfg[4:2]: co_link_speed_led output select 0: speed100_led 1: activity & speed100_led 2: link_led & speed100_led 3: link_led & activity & speed100_led 4: speed10_led 5: activity & speed10_led 6: link_led & speed10_led 7: link_led & activity & speed10_led led_cfg[1]: invert co_link_speed_led when output to gpio led_cfg[0]: invert all led signal from phy
23	R/W	0	invert co_activity_led invert co_activity_led when output to gpio
22	R/W	0	co_pwruprst_byp
21	R/W	0	co_clk_ext
20	R/W	0	co_st_scan
19	R/W	0	co_rxclk_inv
18	R/W	0	co_phy_enb
17	R/W	0	co_clkfreq
16	R/W	0	eth_clk_enable
15:14	R/W	0	co_st_miimode[1:0]
13	R/W	0	co_smii_source_sync
12	R/W	0	co_st_pllbp
11	R/W	0	co_st_adcbp
10	R/W	0	co_st_fxmode
9	R/W	0	co_en_high
8	R/W	0	co_automdix_en
7:3	R/W	0	co_st_phyadd[4:0]
2:0	R/W	0	co_st_mode[2:0]

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Table 13-47 ETH_PHY_CNTL2 0x88

Bit(s)	R/W	Default	Description
31	R/W	0	reserved
30	R/W	0	eth_phy_clk25min_en: enable 125M clock in test/debug mode
29:28	R/W	0	reserved
27:24	R/W	0	debug output bus select
23:13	R/W	0	reserved
12	R/W	0	analog production test mode enable
11	R/W	0	mdi source select 0: normal 1: debug in
10	R/W	0	reserved
9	R/W	0	source select for rx_clk to mac 0: gpio 1: co_clkin from ephy
8	R/W	0	source select for tx_clk output to gpio 0: tx_clk from mac 1: co_tx_clk from ephy
7	R/W	0	rx_dv/col switch for mac
6	R/W	0	ephy smi source select 1: from mac
5	R/W	0	use internal phy
4	R/W	0	ephy smi source select 1: from debug in
3	R/W	0	co_clkin source select 1: from debug in
2	R/W	0	co_mdclk source select 1: from debug in
1	R/W	0	enable reset in test mode
0	R/W	0	ephy loopback mode enable, in/out through debug in/out gpio

Table 13-48 ETH_PHY_CNTL3 0x8C

Bit(s)	R/W	Default	Description
6	R/W	0	ETH_TXDA source select for analog phy 0: normal function, from digital phy 1: from eth_txda_test_data for AMP test
5:0	R/W	0	ETH_TXDA register control for AMP test

Table 13-49 ETH_PHY_STS0 0x94

Bit(s)	R/W	Default	Description
31:28	R		reserved
27:19	R		co_int_vec[8:0]
19	R		reserved
18:0	R		ETH_PLL_STS[18:0]

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Table 13-50 ETH_PHY_STS1 0x98

Bit(s)	R/W	Default	Description
31:0	R		eth_phy_dbg_prb

Table 13-51 ETH_PHY_STS2 0x9C

Bit(s)	R/W	Default	Description
31:26	R		eth_phy_rxda[5:0]
25	R		eth_phy_rxadcoflw
24	R		eth_phy_rxadcuflw
23	R		eth_phy_rxprepga
22:20	R		eth_phy_rxgain[2:0]
19:0	R		eth_test_status

Table 13-52 ETH_PHY_DBG_REG 0xA0

Bit(s)	R/W	Default	Description
31:16	R		eth_phy_dbg_reg
15:8			reserved
7:0	R/W	0	eth_phy_dbg_reg_mux

13.3 Inter-Integrated Circuit (I2C)

13.3.1 Overview

Inter-Integrated Circuit (IIC or I2C) is a multi-slave serial communication bus between ICs. The chip integrates the I2C interface and signals allowing communications with other I2C peripheral devices.

13.3.2 Features

The I2C Master Module has the following features:

- Support for 7-bit and 10-bit addressable devices
- Programmable bus speed including standard speed (100 KBits/s) and fast speed (400 KBits/s)
- Error transfer detection
- “Transfer complete” indication by polling or interrupt (Interrupts handled by the ISA module).
- Internal buffer holding up to 8 bytes for transfer (in either direction)
- Flexible architecture allowing the software to dictate the format of the I2C bit streams
- Manual setting of the I2C bus to accommodate a software only mode

13.3.3 Register Description

For I2C module in EE domain, each register final address = base address + offset * 4 for master mode, final address = base address + offset * 4 for slave mode.

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For I2C master registers the following lists describe the mapping between each I2C master register and its address.

I2C Master A

REGISTER_BASE_ADDR = 0xfe066000

I2C_M_A_CONTROL_REG 0xfe066000

I2C_M_A_SLAVE_ADDR 0xfe066004

I2C_M_A_TOKEN_LIST0 0xfe066008

I2C_M_A_TOKEN_LIST1 0xfe06600c

I2C_M_A_WDATA_REG0 0xfe066010

I2C_M_A_WDATA_REG1 0xfe066014

I2C_M_A_RDATA_REG0 0xfe066018

I2C_M_A_RDATA_REG1 0xfe06601c

I2C_M_A_TIMEOUT_TH 0xfe066020

I2C_M_A_CNTL_DELY1 0xfe066024

I2C_M_A_CNTL_DELY2 0xfe066028

I2C_M_A_LOW_DELY 0xfe06602c

I2C_M_A_HIGH_DELY 0xfe066030

I2C_M_A_FIFO_CTRL0 0xfe066034

I2C_M_A_FIFO_CTRL1 0xfe066038

I2C_M_A_FIFO_PENDING 0xfe06603c

I2C_M_A_FIFO_PENDING_MASK 0xfe066040

I2C_M_A_FIFO_ST0 0xfe066044

I2C Master B

REGISTER_BASE_ADDR = 0xfe068000

I2C_M_B_CONTROL_REG 0xfe068000

I2C_M_B_SLAVE_ADDR 0xfe068004

I2C_M_B_TOKEN_LIST0 0xfe068008

I2C_M_B_TOKEN_LIST1 0xfe06800c

I2C_M_B_WDATA_REG0 0xfe068010

I2C_M_B_WDATA_REG1 0xfe068014

I2C_M_B_RDATA_REG0 0xfe068018

I2C_M_B_RDATA_REG1 0xfe06801c

I2C_M_B_TIMEOUT_TH 0xfe068020

I2C_M_B_CNTL_DELY1 0xfe068024

I2C_M_B_CNTL_DELY2 0xfe068028

I2C_M_B_LOW_DELY 0xfe06802c

I2C_M_B_HIGH_DELY 0xfe068030

I2C_M_B_FIFO_CTRL0 0xfe068034

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I2C_M_B_FIFO_CTRL1 0xfe068038

I2C_M_B_FIFO_PENDING 0xfe06803c

I2C_M_B_FIFO_PENDING_MASK 0xfe068040

I2C_M_B_FIFO_ST0 0xfe068044

I2C Master C

REGISTER_BASE_ADDR = 0xfe06a000

I2C_M_C_CONTROL_REG 0xfe06a000

I2C_M_C_SLAVE_ADDR 0xfe06a004

I2C_M_C_TOKEN_LIST0 0xfe06a008

I2C_M_C_TOKEN_LIST1 0xfe06a00c

I2C_M_C_WDATA_REG0 0xfe06a010

I2C_M_C_WDATA_REG1 0xfe06a014

I2C_M_C_RDATA_REG0 0xfe06a018

I2C_M_C_RDATA_REG1 0xfe06a01c

I2C_M_C_TIMEOUT_TH 0xfe06a020

I2C_M_C_CNTL_DELY1 0xfe06a024

I2C_M_C_CNTL_DELY2 0xfe06a028

I2C_M_C_LOW_DELY 0xfe06a02c

I2C_M_C_HIGH_DELY 0xfe06a030

I2C_M_C_FIFO_CTRL0 0xfe06a034

I2C_M_C_FIFO_CTRL1 0xfe06a038

I2C_M_C_FIFO_PENDING 0xfe06a03c

I2C_M_C_FIFO_PENDING_MASK 0xfe06a040

I2C_M_C_FIFO_ST0 0xfe06a044

I2C Master D

REGISTER_BASE_ADDR = 0xfe06c000

I2C_M_D_CONTROL_REG 0xfe06c000

I2C_M_D_SLAVE_ADDR 0xfe06c004

I2C_M_D_TOKEN_LIST0 0xfe06c008

I2C_M_D_TOKEN_LIST1 0xfe06c00c

I2C_M_D_WDATA_REG0 0xfe06c010

I2C_M_D_WDATA_REG1 0xfe06c014

I2C_M_D_RDATA_REG0 0xfe06c018

I2C_M_D_RDATA_REG1 0xfe06c01c

I2C_M_D_TIMEOUT_TH 0xfe06c020

I2C_M_D_CNTL_DELY1 0xfe06c024

I2C_M_D_CNTL_DELY2 0xfe06c028

I2C_M_D_LOW_DELY 0xfe06c02c

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I2C_M_D_HIGH_DELY 0xfe06c030
I2C_M_D_FIFO_CTRL0 0xfe06c034
I2C_M_D_FIFO_CTRL1 0xfe06c038
I2C_M_D_FIFO_PENDING 0xfe06c03c
I2C_M_D_FIFO_PENDING_MASK 0xfe06c040
I2C_M_D_FIFO_ST0 0xfe06c044

I2C Master E

REGISTER_BASE_ADDR = 0xfe06e000
I2C_M_E_CONTROL_REG 0xfe06e000
I2C_M_E_SLAVE_ADDR 0xfe06e004
I2C_M_E_TOKEN_LIST0 0xfe06e008
I2C_M_E_TOKEN_LIST1 0xfe06e00c
I2C_M_E_WDATA_REG0 0xfe06e010
I2C_M_E_WDATA_REG1 0xfe06e014
I2C_M_E_RDATA_REG0 0xfe06e018
I2C_M_E_RDATA_REG1 0xfe06e01c
I2C_M_E_TIMEOUT_TH 0xfe06e020
I2C_M_E_CNTL_DELY1 0xfe06e024
I2C_M_E_CNTL_DELY2 0xfe06e028
I2C_M_E_LOW_DELY 0xfe06e02c
I2C_M_E_HIGH_DELY 0xfe06e030
I2C_M_E_FIFO_CTRL0 0xfe06e034
I2C_M_E_FIFO_CTRL1 0xfe06e038
I2C_M_E_FIFO_PENDING 0xfe06e03c
I2C_M_E_FIFO_PENDING_MASK 0xfe06e040
I2C_M_E_FIFO_ST0 0xfe06e044

I2C Master F

REGISTER_BASE_ADDR = 0xfe070000
I2C_M_F_CONTROL_REG 0xfe070000
I2C_M_F_SLAVE_ADDR 0xfe070004
I2C_M_F_TOKEN_LIST0 0xfe070008
I2C_M_F_TOKEN_LIST1 0xfe07000c
I2C_M_F_WDATA_REG0 0xfe070010
I2C_M_F_WDATA_REG1 0xfe070014
I2C_M_F_RDATA_REG0 0xfe070018
I2C_M_F_RDATA_REG1 0xfe07001c
I2C_M_F_TIMEOUT_TH 0xfe070020
I2C_M_F_CNTL_DELY1 0xfe070024

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I2C_M_F_CNTL_DELY2 0xfe070028

I2C_M_F_LOW_DELY 0xfe07002c

I2C_M_F_HIGH_DELY 0xfe070030

I2C_M_F_FIFO_CTRL_REG 0xfe070034

I2C_M_F_STATE_REG 0xfe070038

For I2C slave registers the following lists describe the mapping between each I2C slave register and its address.

I2C Slave A

REGISTER_BASE_ADDR = 0xfe064000

I2C_S_A_CONTROL_REG 0xfe064000

I2C_S_A_SEND_REG 0xfe064004

I2C_S_A_RECV_REG 0xfe064008

I2C_S_A_CNTL1_REG 0xfe06400c

B/C/D/E/F are the same design as A.

Table 13-53 I2C_M_A_CONTROL_REG

Bit(s)	R/W	Default	Description
31	R/W	0	CNTL_JIC: There is internal logic to dynamically enable the gated clocks. If this gated clock logic doesn't work, you can set this bit to always enable the clock. Setting this bit wastes power.
30	R/W	0	enhance mode,enhance mode enable timming adjust. =1,enable enhance mode =0, disable enhance mode
29-28	R/W	0	QTR_CLK_EXT: These two bits extend the clock divider to 12 bits: QTR_CLK = {[29:28],[21:12]}
26	R	0	Read back level of the SDA line
25	R	0	Read back level of the SCL line
24	R/W	0	Sets the level of the SDA line if manual mode is enabled. If this bit is '0', then the SDA line is pulled low. If this bit is '1' then the SDA line is tri-stated.
23	R/W	0	Sets the level of the SCL line if manual mode is enabled. If this bit is '0', then the SCL line is pulled low. If this bit is '1' then the SCL line is tri-stated.
22	R/W	0	This bit is used to enable manual mode. Manual I²C mode is controlled by bits 12,13,14 and 15 above.
21:12	R/W	0x142	**QTR_CLK_DLY**. This value corresponds to period of the SCL clock divided by 4 Quarter Clock Delay = * System Clock Frequency For example, if the system clock is 133Mhz, and the I²C clock period is 10uS (100khz), then Quarter Clock Delay = * 133 Mhz = 332
11:8	R	-	READ_DATA_COUNT: This value corresponds to the number of bytes READ over the I²C bus. If this value is zero, then no data has been read. If this value is 1, then bits [7:0] in TOKEN_RDATA_REG0 contains valid data. The software can read this register after an I²C transaction to get the number of bytes to read from the I²C device.
7:4	R	-	CURRENT_TOKEN: This value reflects the current token being processed. In the event of an error, the software can use this value to determine the error location.
3	R	-	ERROR: This read only bit is set if the I²C device generates a NACK during writing. This bit is cleared at on the clock cycle after the START bit is set to 1

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Bit(s)	R/W	Default	Description
			indicating the start of list processing. Errors can be ignored by setting the ACK_ IGNORE bit below. Errors will be generated on Writes to devices that return NACK instead of ACK. A NACK is returned by a device if it is unable to accept any more data (for example because it is processing some other real-time function). In the event of an ERROR, the I²C module will automatically generate a STOP condition on the bus.
2	R	-	STATUS: This bit reflects the status of the List processor: 0: IDLE 1: Running. The list processor will enter this state on the clock cycle after the START bit is set. The software can poll the status register to determine when processing is complete.
1	R/W	0	ACK_IGNORE: Set to 1 to disable I²C ACK detection. The I²C bus uses an ACK signal after every byte transfer to detect problems during the transfer. Current Software implementations of the I²C bus ignore this ACK. This bit is for compatibility with the current Amlogic software. This bit should be set to 0 to allow NACK operations to abort I²C bus transactions. If a NACK occurs, the ERROR bit above will be set.
0	R/W	0	START: Set to 1 to start list processing. Setting this bit to 0 while the list processor is operating causes the list processor to abort the current I²C operation and generate an I²C STOP command on the I²C bus. Normally this bit is set to 1 and left high until processing is complete. To re-start the list processor with a new list (after a previous list has been exhausted), simply set this bit to zero then to one.

Table 13-54 I2C_M_A_SLAVE ADDR

Bit(s)	R/W	Default	Description
31:29	R	0	Unused
28	R/W	0	USE_CNTL_SCL_LOW: If this bit is set to 1, then bits[27:16] control the SCL low time.
27:16	R/W	0	SCL Low delay. This is a new feature in M8baby. In the previous M8baby design, the SCL low time was controlled by bits[21:12] of the register above. In this design, the SCL delay is controlled independently by these bits.
15:14	R	0	Unused
13-11	R/W	0	SCL_FILTER: A filter was added in the SCL input path to allow for filtering of slow rise times. 0 = no filtering, 7 = max filtering
10:8	R/W	0	SDA FILTER: A filter was added in the SDA input path to allow for filtering of slow rise times. 0 = no filtering, 7 = max filtering
7:0	R/W	0x00	SLAVE_ADDRESS. This is a 7-bit value for a 7-bit I²C device, or (0xF0 | {A9,A8}) for a 10-bit I²C device. By convention, the slave address is typically stored in by first left shifting it so that it's MSB is D7 (The I²C bus assumes the 7-bit address is left shifted one). Additionally, since the SLAVE address is always an 7-bit value, D0 is always 0. NOTE: The I²C always transfers 8-bits even for address. The I²C hardware will use D0 to dictate the direction of the bus. Therefore, D0 should always be '0' when this register is set.

Table 13-55 I2C_M_A_TOKEN_LIST0

Bit(s)	R/W	Default	Description
31:28	R/W	0x00	8th token in the list to process
27:24	R/W	0x00	7th token in the list to process
23:20	R/W	0x00	6th token in the list to process

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Bit(s)	R/W	Default	Description
19:16	R/W	0x00	5th token in the list to process
15:12	R/W	0x00	4th token in the list to process
11:8	R/W	0x00	3rd token in the list to process
7:4	R/W	0x00	2nd token in the list to process
3:0	R/W	0x00	1st token in the list to process (See the table below for token definitions)

Table 13-56 Token Definitions

Command Token	Value	Data	Description
END	0x0	N/A	Used to tell the I²C module that this is the end of the Token list. This token is not associated with the I²C bus, but rather with the state-machine that drives the token list processor.
START	0x1	N/A	The START Token is used to tell an I²C device that this is the beginning of an I²C transfer
SLAVE_ ADDR-- WRITE	0x2	7-bits	This bit-sequence is used to address a device and tell the device it is being WRITTEN
SLAVE_ ADDR-- READ	0x3	7-bits	This bit sequence is used to address a device and tell the device it is being READ.
DATA	0x4	8-bits	This 8-bit byte sequence is a byte transfer (READ or WRITE). The DATA token corresponds to a WRITE if it follows a SLAVE_ADDR-WRITE token. The DA-TA token corresponds to a READ if it follows a SLAVE_ADDR-READ token.
DATA-LAST	0x5	8-bits	Used to indicate the last 8-bit byte transfer is a byte transfer of a READ.
STOP	0x6	N/A	This tells the I²C device it is no longer being addressed

Write data associated with the DATA token should be placed into the I2C_TOKEN_WDATA_REG0 or I2C_TOKEN_WDATA_REG1 registers. Read data associated with the DATA or DATA-LAST token can be read from the I2C_TOKEN_RDATA_REG0 or I2C_TOKEN_RDATA_REG1 registers.

Table 13-57 I2C_M_0_TOKEN_LIST1

Bit(s)	R/W	Default	Description
31:28	R/W	0x00	16th token in the list to process
27:24	R/W	0x00	15th token in the list to process
23:20	R/W	0x00	14th token in the list to process
19:16	R/W	0x00	13th token in the list to process
15:12	R/W	0x00	12th token in the list to process
11:8	R/W	0x00	11th token in the list to process
7:4	R/W	0x00	10th token in the list to process
3:0	R/W	0x00	9th token in the list to process

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Table 13-58 I2C_M_A_WDATA_REG0

Bit(s)	R/W	Default	Description
31:24	R/W	0x00	4th data byte written for a DATA (write) token.
23:16	R/W	0x00	3rd data byte written for a DATA (write) token.
15:8	R/W	0x00	2nd data byte written for a DATA (write) token.
7:0	R/W	0x00	1st data byte written for a DATA (write) token.

Table 13-59 I2C_M_A_WDATA_REG1

Bit(s)	R/W	Default	Description
31:24	R/W	0x00	8th data byte written for a DATA (write) token.
23:16	R/W	0x00	7th data byte written for a DATA (write) token.
15:8	R/W	0x00	6th data byte written for a DATA (write) token.
7:0	R/W	0x00	5th data byte written for a DATA (write) token.

Table 13-60 I2C_M_A_RDATA_REG0

Bit(s)	R/W	Default	Description
31:24	R/W	0x00	4th data byte read for a DATA or DATA-LAST (READ) token.
23:16	R/W	0x00	3rd data byte read for a DATA or DATA-LAST (READ) token.
15:8	R/W	0x00	2nd data byte read for a DATA or DATA-LAST (READ) token.
7:0	R/W	0x00	1st data byte read for a DATA or DATA-LAST (READ) token.

Table 13-61 I2C_M_A_RDATA_REG1

Bit(s)	R/W	Default	Description
31:24	R/W	0x00	8th data byte read for a DATA or DATA-LAST (READ) token.
23:16	R/W	0x00	7th data byte read for a DATA or DATA-LAST (READ) token.
15:8	R/W	0x00	6th data byte read for a DATA or DATA-LAST (READ) token.
7:0	R/W	0x00	5th data byte read for a DATA or DATA-LAST (READ) token.

Table 13-62 I2C_M_A_TIMEOUT_TH

Bit(s)	R/W	Default	Description
11:0	R/W	0x00	timeout irq th

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Table 13-63 I2C_M_A_CNTL_DELY1

Bit(s)	R/W	Default	Description
31:24	R/W	0	Reserved
23:12	R/W	0x14c	repeat start command control delay value,Used to repair timing. Valid in the enhance mode.
11:0	R/W	0x14c	start command control delay value,Used to repair timing. Valid in the enhance mode.

Table 13-64 I2C_M_A_CNTL_DELY2

Bit(s)	R/W	Default	Description
31:12	R/W	0	Reserved
11:0	R/W	0x14c	stop command control delay value,Used to repair timing. Valid in the enhance mode.

Table 13-65 I2C_M_A_LOW_DELY

Bit(s)	R/W	Default	Description
31:24	R/W	0	Reserved
23:12	R/W	0x14c	low2_delay data transfer second low level delay,Used to repair timing. Valid in the enhance mode.
11:0	R/W	0x14c	low1_delay data transfer first low level delay,Used to repair timing. Valid in the enhance mode.

Table 13-66 I2C_M_A_HIGH_DELY

Com-mand Token	Value	Data	Descriptiaon
31:24	R/W	0	Reserved
23:12	R/W	0xA6	high2_delay data transfer second high level delay,Used to repair timing. Valid in the enhance mode.
11:0	R/W	0xA6	high1_delay data transfer first high level delay,Used to repair timing. Valid in the enhance mode.

Table 13-67 I2C_M_A_FIFO_CTRL0

Bit(s)	R/W	Default	Description
30	R/W	0x00	reg_fifo_mode
24	R/W	0x00	reg_fifo_timeout_stop
23	R/W	0x00	reg_fifo_timeout_clr
22	R/W	0x00	reg_fifo_timeout_en
21	R/W	0x00	reg_fifo_irq_mode :0 pluse 1 level

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Bit(s)	R/W	Default	Description
20	R/W	0x00	reg_fifo_err_stop
18	R/W	0x00	reg_rd_fifo_rst
17	R/W	0x00	reg_wd_fifo_rst
16	R/W	0x00	reg_tk_fifo_rst

Table 13-68 I2C_M_A_FIFO_CTRL1

Bit(s)	R/W	Default	Description
31:16	R/W	0x00	reg_fifo_timeout_thd
11:8	R/W	0x00	reg_rd_fifo_thd
7:4	R/W	0x00	reg_wd_fifo_thd
2:0	R/W	0x00	reg_tk_fifo_thd

Table 13-69 I2C_M_A_FIFO_PENDING

Bit(s)	R/W	Default	Description
11	R/W	0x00	tk_fifo_underflow_pending,write 1 to clear pending
10	R/W	0x00	tk_fifo_overflow_pending,write 1 to clear pending
9	R/W	0x00	wd_fifo_underflow_pending,write 1 to clear pending
8	R/W	0x00	wd_fifo_overflow_pending,write 1 to clear pending
7	R/W	0x00	rd_fifo_underflow_pending,write 1 to clear pending
6	R/W	0x00	rd_fifo_overflow_pending,write 1 to clear pending
5	R/W	0x00	fifo_timeout_pending,write 1 to clear pending
4	R/W	0x00	rd_fifo_thd_irq_pending,write 1 to clear pending
3	R/W	0x00	wd_fifo_thd_irq_pending,write 1 to clear pending
2	R/W	0x00	tk_fifo_thd_irq_pending,write 1 to clear pending
1	R/W	0x00	error_pending,write 1 to clear pending
0	R/W	0x00	i2c_st_in_idle_pending,write 1 to clear pending

Table 13-70 I2C_M_A_FIFO_PENDING_MASK

Bit(s)	R/W	Default	Description
11:0	R/W	0x00	pending mask

Table 13-71 I2C_M_A_FIFO_ST0

Bit(s)	R/W	Default	Description
31:28	RO	0x00	wd_data_valid
26:24	RO	0x00	rd_data_valid

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Bit(s)	R/W	Default	Description
23:21	RO	0x00	rdata_din_valid
20:16	RO	0x00	tk_data_valid
14:12	RO	0x00	i2c_st
10:8	RO	0x00	token_count
7:4	RO	0x00	wdata_count
3:0	RO	0x00	rdata_count

Table 13-72 I2C_S_A_CONTROL_REG

Bit(s)	R/W	Default	Description
31-29	R	0	REG POINTER: There are 5 internal registers inside the I2C slave module. The I2C Master sets this value using the byte that follows the address byte in the I2C data stream. Register 4 (numbered 0,1,…4) is the status register.
28	R/W	0	SEND READY: This bit is set to '1' by the ARC to indicate to the slave machine that the I2C slave module is ready to send data. This bit is cleared by the I2C module when it has sent 4 bytes to the I2C master. This bit is also available in the status register that can be read by the I2C master. The I2C master can read the status register to see when the I2C slave module has data to send.
27	R/W	0	RECEIVE READY: This bit is set to '1' by the ARC to indicate to the slave machine that the I2C slave module is ready to receive data. This bit is cleared by the I2C module when it has received 4 bytes from the I2C master. This bit is also available in the status register that can be read by the I2C master. The I2C master can read the status register to see when the I2C slave module is ready to receive data.
26	R	0	BUSY: Read only status bit. '1' indicates that the I2C slave module is sending or receiving data.
25	R/W	0	IRQ_EN: If this bit is set, then an interrupt will be sent to the ARC whenever 4 bytes have been read or 4 bytes have been written to the I2C slave module.
24	R/W	0	ACK Always: Typically the ACK of a slave I2C device is dependent upon the availability of data (if reading) and room to store data (when we are being written). Our I2C module has a status register that can be read continuously. This bit can be set if the I2C master wants to continually read the status register.
23-16	R/W	0	Slave Address: Bits [7:1] are used to identify the device. Bit [0] is ignored since this corresponds to the R/W bit.
15-8	R/W	0x27	HOLD TIME: Data hold time after the falling edge of SCL. This hold time is computed as Hold time = (MPEG system clock period) * (value + 1).
7	R/W	0	Enable: A '1' enables the I2C slave state machine.
6-0	R/W	0x06	Sampling rate. Defined as MPEG system clock / (value + 1). The SDA and SCL inputs into the slave module are sampled as a way of filtering the inputs. A rising or falling edge is determined by when 3 successive samples are either high or low respectively.

Table 13-73 I2C_S_A_SEND_REG

Bit(s)	R/W	Default	Description
31-0	R/W	0	The I2C slave module can send up to 4 bytes of data starting with the byte located at bits [7:0]

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Table 13-74 I2C_S_A_RECV_REG

Bit(s)	R/W	Default	Description
31-0	R	0	This read only register corresponds to the 4 bytes of data written to the I2C slave module by an external I2C master. Bits [7:0] correspond to the first byte written by the I2C master.

Table 13-75 I2C_S_A_CNTL1_REG

Bit(s)	R/W	Default	Description
31-6	R	0	Unused
5-3	R/W	0	SCL_FILTER: A filter was added in the SCL input path to allow for filtering of slow rise times. 0 = no filtering, 7 = max filtering
2-0	R/W	0x00	SDA FILTER: A filter was added in the SDA input path to allow for filtering of slow rise times. 0 = no filtering, 7 = max filtering

13.4 Universal Asynchronous Receiver And Transmitter

13.4.1 Overview

There are a number of UARTs in the chip that offer 2-wire (RX/TX) and 4-wire (RX/TX, CTS/RTS) connections at the digital I/O pins. Each UART contains one transmit FIFO and a receive FIFO (see depths below). The FIFO's are filled by the CPU and read by the CPU.

Table 13-76 UART List

UART	RX/TX FIFO depths	Comment
UART_A	128 bytes	Located in the AO
UART_B	128 bytes	Located in the AO
UART_C	128 bytes	Located in the AO
UART_D	128 bytes	Located in the AO
UART_E	128 bytes	Located in the AO

13.4.2 Features

Input filters

The CTS (clear to send) and RX (receive) input paths have input filters to deal with slow rise times. The filters are configurable to use a 125ns or 1us sampling mechanism. There is an implied 3 system clock cycle delay (15ns for a typical system clock of 200MHz) that is used to synchronize and detect the rising/falling edge of the RXD signal. The RXD signal may be passed through an optional filter to deglitch the external signal in noisy conditions. The deglitch filter has two settings which add to the "detection delay" of the RXD signal by the internal logic:

- Filter setting 1 (125ns strobe): 375ns ~ 2.6us

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- Filter setting 2 (1us strobe): 3us ~ 21us

The filter is described in the register specification. If the filter is disabled, the shortest RXD low time and high time is 12 system clock cycles (60ns for a system clock of 200MHz).

Clear to Send

CTS is a signal sent from the receiver UART back to the transmitting UART to tell the transmitting UART to stop sending data. The CTS signal must be received before the next START symbol is sent. The transmitting UART is allowed to send one more byte after the CTS signal is recognized. The CTS signal coming into the chip goes through some synchronization and detection which adds an additional 5 system clocks (typically 25ns for a 200Mhz system clock). This setup time for CTS detection is called CTSstop. The CTS input also has an optional filter can be used to deglitch the incoming CTS signal. If the filter is disabled, the CTS signal must be de-asserted 5 system clock cycles before the start of the next BYTE transfer. If the CTS filter is enabled, then additional time must be added to the 25ns requirement. There are two programmable filter settings that effectively delay CTS being seen by the internal logic:

- Filter setting 1 (125ns strobe): 375ns ~ 2.6us
- Filter setting 2 (1us strobe): 3us ~ 21us

Interrupts

The UARTs can generate interrupts if the receive FIFO exceeds a pre-programmed threshold. An interrupt can also be generated if there is a frame or parity error.

Clock Independent Operation

Because the system clock can be altered to accommodate dynamic frequency scaling, the UARTs have an option in which they use the 24Mhz crystal clock as the source for the UART.

13.4.3 Functional Description

The UART requires that a Baud Rate be established. The UART supports rates as slow as 1Hz up to rates as high as 8M bits/s. Once the baud rate has been established, bytes are transmitted as they are written to the transmit-FIFO by the CPU. A large transmit-FIFO exists to allow the CPU to pre-load a transmit package because the CPU can often write faster than the UART can transmit the data.

Data this automatically received by the UART is placed into the receive FIFO one byte at a time. The receive-FIFO decouples the UART from the CPU allowing the CPU to read the UART byte data at a rate not dictated by the UART.

13.4.4 Register Description

The following register description is applied to all UART instantiations in the chip.

final address = base address + offset *4

B/C/D/E are the same design as A.

UART_A Registers

REGISTER_BASE_ADDR = 0xfe078000

UART_A_WFIFO 0xfe078000

UART_A_RFIFO 0xfe078004

UART_A_CONTROL 0xfe078008

UART_A_STATUS 0xfe07800c

UART_A_MISC 0xfe078010

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UART_A_REG5 0xfe078014

UART_B Registers

REGISTER_BASE_ADDR = 0xfe07a000

UART_B_WFIFO 0xfe07a000

UART_B_RFIFO 0xfe07a004

UART_B_CONTROL 0xfe07a008

UART_B_STATUS 0xfe07a00c

UART_B_MISC 0xfe07a010

UART_B_REG5 0xfe07a014

UART_C Registers

REGISTER_BASE_ADDR = 0xfe07c000

UART_C_WFIFO 0xfe07c000

UART_C_RFIFO 0xfe07c004

UART_C_CONTROL 0xfe07c008

UART_C_STATUS 0xfe07c00c

UART_C_MISC 0xfe07c010

UART_C_REG5 0xfe07c014

UART_D Registers

REGISTER_BASE_ADDR = 0xfe07e000

UART_D_WFIFO 0xfe07e000

UART_D_RFIFO 0xfe07e004

UART_D_CONTROL 0xfe07e008

UART_D_STATUS 0xfe07e00c

UART_D_MISC 0xfe07e010

UART_D_REG5 0xfe07e014

UART_E Registers

REGISTER_BASE_ADDR = 0xfe080000

UART_E_WFIFO 0xfe080000

UART_E_RFIFO 0xfe080004

UART_E_CONTROL 0xfe080008

UART_E_STATUS 0xfe08000c

UART_E_MISC 0xfe080010

UART_E_REG5 0xfe080014

Table 13-77 UART_A_WFIFO

Bit(s)	R/W	Default	Description
31-8	R	0	unused
7-0	R/W	-	Write FIFO data. The Write FIFO holds 128 or 64 bytes. The Write FIFO can be written as long as it is not full.

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Table 13-78 UART_A_RFIFO

Bit(s)	R/W	Default	Description
31-8	R	0	unused
7-0	R/W	-	Read FIFO data. The Read FIFO holds 128 or 64 bytes. The empty flag can be used to determine if data is available

Table 13-79 UART_A_CONTROL

Bit(s)	R/W	Default	Description
31	R/W	0	Invert the RTS signal
30	R/W	0	Mask Error: Set to 1 to mask errors
29	R/W	0	Invert the CTS signal
28	R/W	0	Transmit byte Interrupt: Set to 1 to enable the generation an interrupt whenever a byte is read from the transmit FIFO
27	R/W	0	Receive byte Interrupt: Set to 1 to enable the generation an interrupt whenever a byte is written to the receive FIFO
26	R/W	0	Set to 1 to invert the TX pin
25	R/W	0	Set to 1 to invert the RX pin
24	R/W	0	Clear Error
23	R/W	0	Reset the receive state machine
22	R/W	0	Reset the transmit state machine
21-20	R/W	0	Character length: 00 = 8 bits, 01 = 7 bits, 10 = 6 bits, 11 = 5 bits
19	R/W	1	Parity Enable: Set to 1 to enable parity
18	R/W	0	Parity type: 0 = even, 1 = odd
17-16	R/W	0	Stop bit length: 00 = 1 bit, 01 = 2 bits
15	R/W	0	Two Wire mode:
14	R/W	0	Unused
13	R/W	0	Receive Enable. Set to 1 to enable the UART receive function
12	R/W	0	Transmit Enable. Set to 1 to enable the UART transmit function
11-0	R/W	0x120	Old Baud rate:

Table 13-80 UART_A_STATUS

Bit(s)	R/W	Default	Description
31-27	R	0	Unused
26	R	0	UART_RECV_BUSY: This bit will be 1 if the uart receive state machine is busy
25	R	0	UART_XMIT_BUSY: This bit will be 1 if the uart transmit state machine is busy
24	R	0	RECV_FIFO_OVERFLOW:
23	R	0	CTS Level

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Bit(s)	R/W	Default	Description
22	R	0	Transmit FIFO Empty
21	R	0	Transmit FIFO Full
20	R	0	Receive FIFO empty
19	R	0	Receive FIFO full
18	R	0	This bit is set if the FIFO is written when it is full. To clear this bit, write bit 24 of register 0x2132
17	R	0	Frame error. To clear this bit, write bit 24 of register UART0_CONTROL
16	R	0	Parity error. To clear this bit, write bit 24 of register UART0_CONTROL
15	R	0	Unused
14-8	R	0	Transmit FIFO count. Number of bytes in the transmit FIFO
7	R	0	Unused
6-0	R	0	Receive FIFO count. Number of bytes in the receive FIFO

Table 13-81 UART_A_MISC

Bit(s)	R/W	Default	Description
31	R/W	0	Added a “just in case” bit that can be set to 1 to enable clocks always. The default is 0 meaning the auto-clock gating logic is enabled.
30	R/W	0	USE old Rx Baud: There was a bug in the RX baud rate generator. The Rx baud rate generator was re-designed to compute a baud rate correctly. If you want to use the old (stupid) logic, you can set this bit to 1.
29	R/W	0	ASYNC_FIFO_PURGE: This bit can be set to 1 after all UART bytes have been received in order to purge the data into the Async FIFO. This bit is needed because the UART receives 8-bit data, but the ASYNC FIFO can only be written with 16-bit data. In this case there might be a residual byte if the UART is not receiving an even number of bytes.
28	R/W	0	ASYNC_FIFO_EN: If this bit is set to 1, then the UART received data is automatically sent to the Async FIFO module which will in turn automatically send the data to DDR memory
27	R/W	0	CTS: Filter Timebase select: 1 = 1uS, 0 = 111nS timebase. A filter was added to the CTS input to allow for a little digital filtering. The amount of filtering is controlled by this timebase (longer = more filtering) and the value in bits FILTER_ SEL below.
26-24	R/W	0	CTS: FILTER_SEL: 0 = no filter, 7 = max filtering
23-20	R/W	0	Old BAUD_RATE_EXT: These 4 bits extend the baud rate divider to 16-bits: Baud Rate = {Reg4[23:20],Reg2[11:0]}
19	R/W	0	RX: Filter Timebase select: 1 = 1uS, 0 = 111nS timebase. A filter was added to the RX input to allow for a little digital filtering. The amount of filtering is controlled by this timebase (longer = more filtering) and the value in bits FILTER_ SEL below.
18-16	R/W	0	RX: FILTER_SEL: 0 = no filter, 7 = max filtering
15-8	R/W	32	XMIT_IRQ_CNT: The UART can be configured to generate an interrupt if the number of bytes in the transmit FIFO drops below this value.
7:0	R/W	15	RECV_IRQ_CNT: The UART can be configured to generate an interrupt after a certain number of bytes have been received by the UART.

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Table 13-82 UART_A_REG5

Bit(s)	R/W	Default	Description
31-28	R/W	0	unused
27	R/W	0	Xtal2_clk_sel: 0: see Xtal_clk_sel 1: xtal_div2(12M)
26	R/W	0	Xtal_clk_sel: 0: xtal_div3(8M); 1: xtal(24M);(need set xtal_tick_en =1 first);
24	R/W	0	USE_XTAL_CLK: If this bit is set, then the clock for generating the UART Baud rate comes from the crystal pad. This allows the UART to operate independent of clk81.
23	R/W	0	USE New Baud rate. Over the years, the baud rate has been extended by concatenating bits from different registers. To take advantage of the full 23-bit baud rate generate (extended to 23 bits to accommodate very low baud rates), you must set this bit. If this bit is set, then the baud rate is configured using bits [22:0] below
22:0	R/W	15	NEW_BAUD_RATE: If bit[23] = 1 above, then the baud rate for the UART is computed using these bits.

13.5 Infrared Remote

13.5.1 Overview

IR module includes 3 sub modules: IR demodulation, Legacy IR remote control and Multi-format IR remote control.

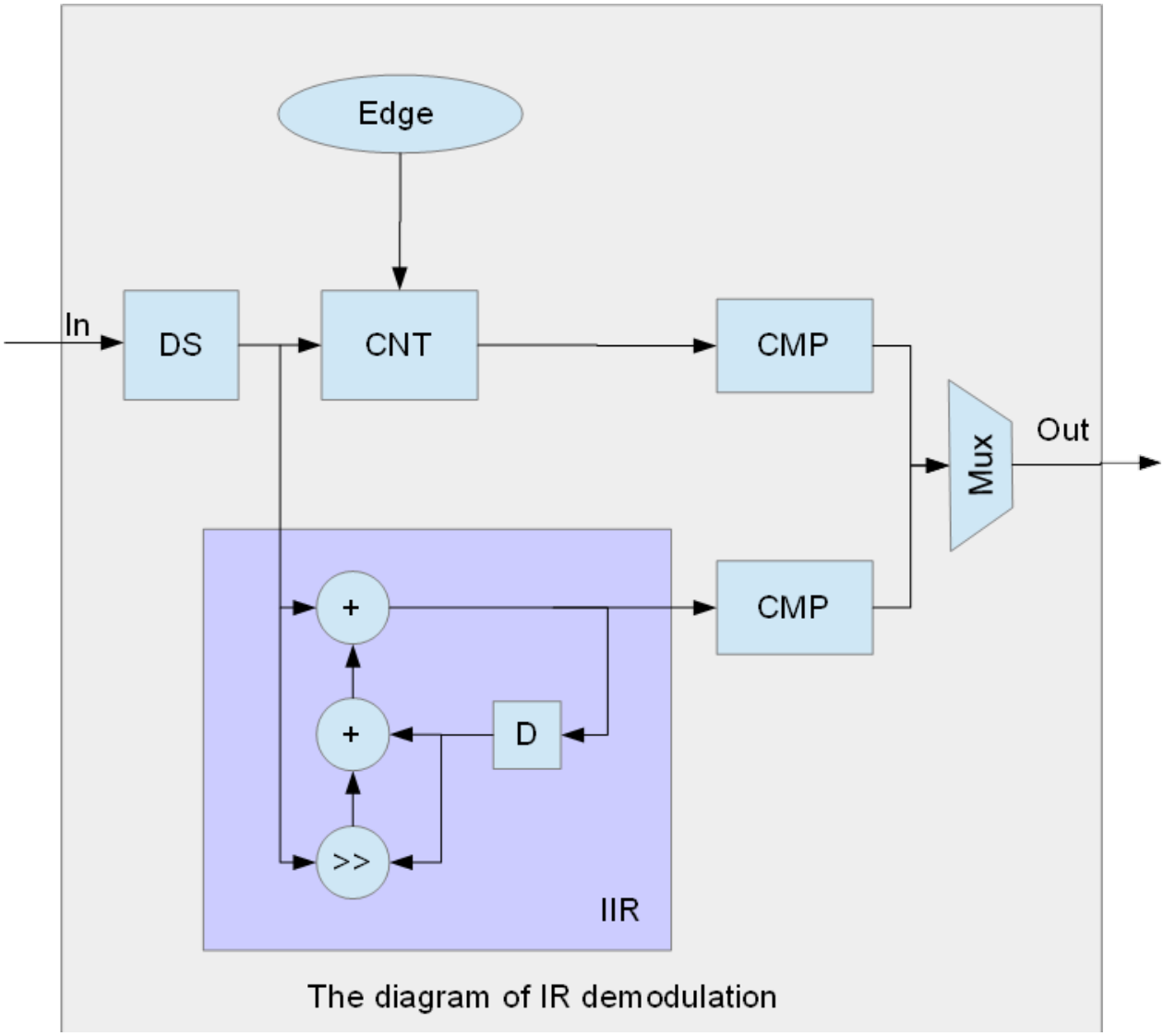
13.5.2 IR Demodulation

IR demolation module demodulate the modulate signal to get the envelop signal.

IR demulation diagram is shown below.

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Figure 13-1 IR Demulation



It implements two methods for demodulation. The input data is an one-bit stream.

The input data are down-sampled firstly. The rate of downsample are configured by register, ranges from 0 to 255.

One method is implemented in the upper path.

The CNT is used to counte the time for ‘0’ and ‘1’. It is cleared when input data changes (from 1 to 0 or from 0 to 1).

When (CNT>REG_IR_PROCT1 && in==1) , it outputs ‘1’. REG_IR_PROCT1 is used to canceled the glitch. Actually, the operation of downsample also have some utility to cancel the glitch.

When (CNT>REG_IR_DECT0 && in==0) , it outputs ‘0’. REG_IR_DECT0 is used to confirm the ‘0’. The value should be bigger than one carrier period.

The other method is implemented in the lower path.

It is a one tap IIR filter. The input data control the integrating factor and the factor can be configured from registers. When 1 inputs, the accumulator can grow quickly. When 0 input, the accumulator decays slowly, and when the number of 0 is bigger enough, it decays soon.

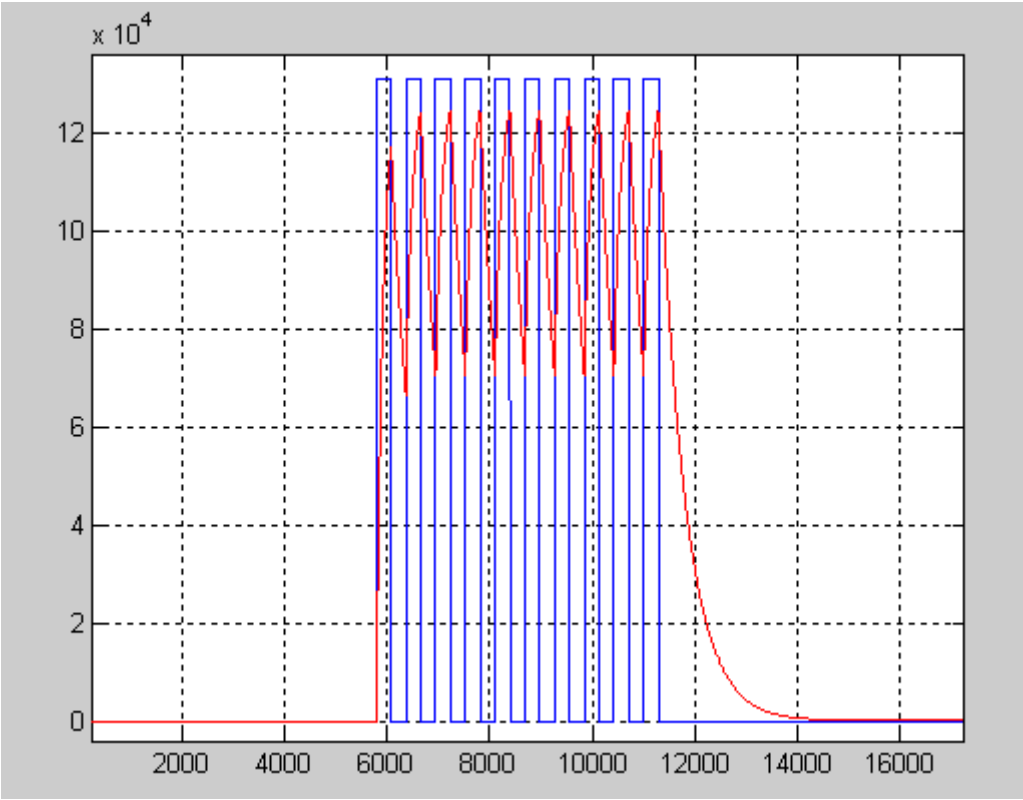
When (accum> REG_IR_IIR_THD1), it outputs ‘1’.

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When (accum< REG_IR_IIR_THD0), it outputs ‘0’.

The diagram shows the simple simulation result. The blue is the input data, the red is the filter out.

Figure 13-2 Simulation Result of IR Demulation

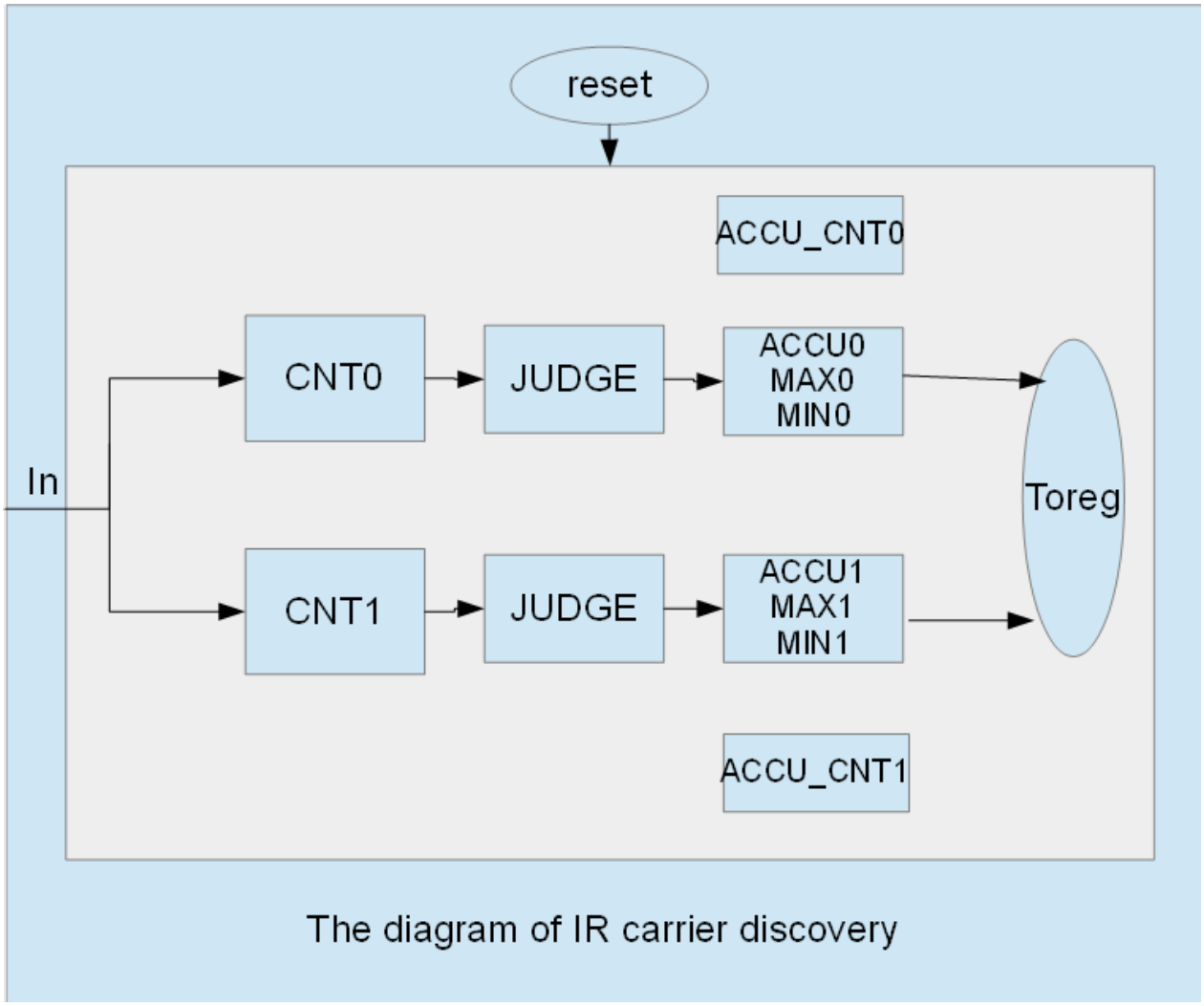


Because the input carrier signal is a rectangular wave signal, the carrier can be estimated easily by counting the wave period. For estimating precisely, the counter for the long “0” and start period and glitch should be removed.

The simple diagram is shown below:

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Figure 13-3 IR Carrier Discovery



CNT is the counter for time of “0” and “1”.

JUDGE is used to remove the long “0” and glitch.

ACC_CNT is the counter for number of accumulating. If ACC_CNT== REG_IR_ST_CNT_THD, then write the value to registers.

For example:

Set REG_IR_ST_CNT_THD to 256, then accumulates 256 times.

The carrier can be calculated:

Fc = Fsys/(RO_IR_SUM_CNT0 +RO_IR_SUM_CNT1)*256;

DUT = RO_IR_SUM_CNT1/(RO_IR_SUM_CNT0 +RO_IR_SUM_CNT1);

Where Fc is the carrier frequency, Fsys is the system clock frequency, DUT is the carrier duty ratio.

13.5.3 Legacy IR Control

The Lagacy IR Remote control module has two modes of operation:

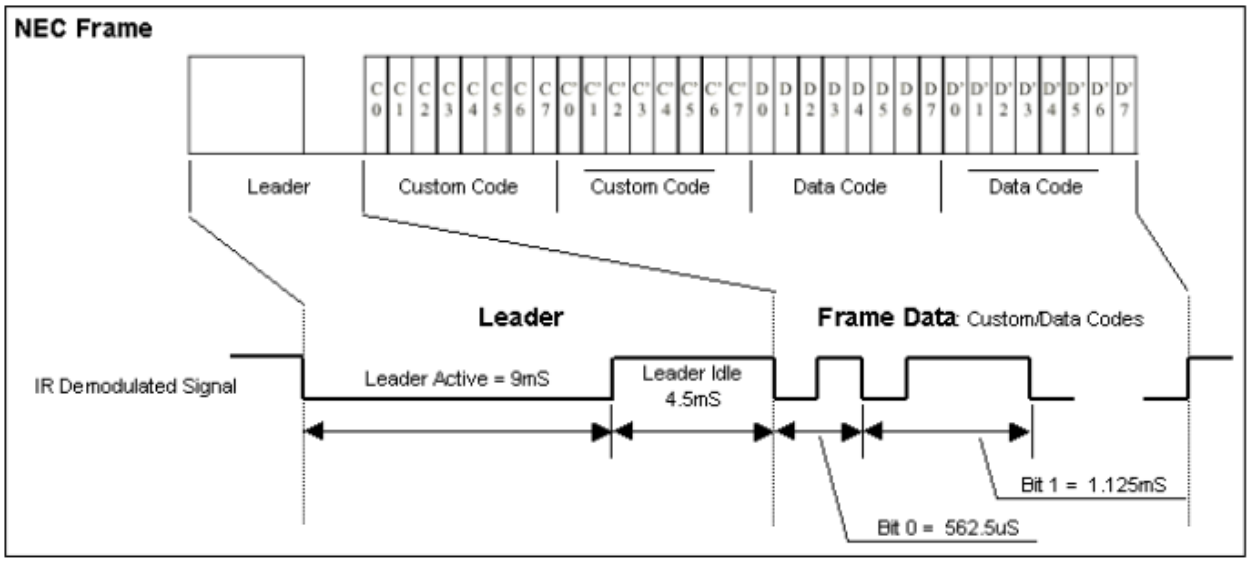
- NEC Frame decoder mode
- General Time Measurement mode

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Note

NEC Frame Decoder: The NEC Frame Decoder mode operates by analyzing the waveform of a TV remote.

Figure 13-4 NEC Frame Decoder



The waveform has a number of components, each of which must fit within a time window to be considered valid. If the entire waveform meets the specifications described by the registers below, then the TV remote codes are captured and an interrupt is generated.

Note

General Time Measurement: Some remotes don't follow the standard NEC format, so additional registers provide the ability to measure the time between rising and/or falling edges of the IR signal. Since the time measurement is done in hardware, the software only needs to read a "width" measurement from a register for every rising and/or falling edge event.

13.5.4 Multi Format IR Control

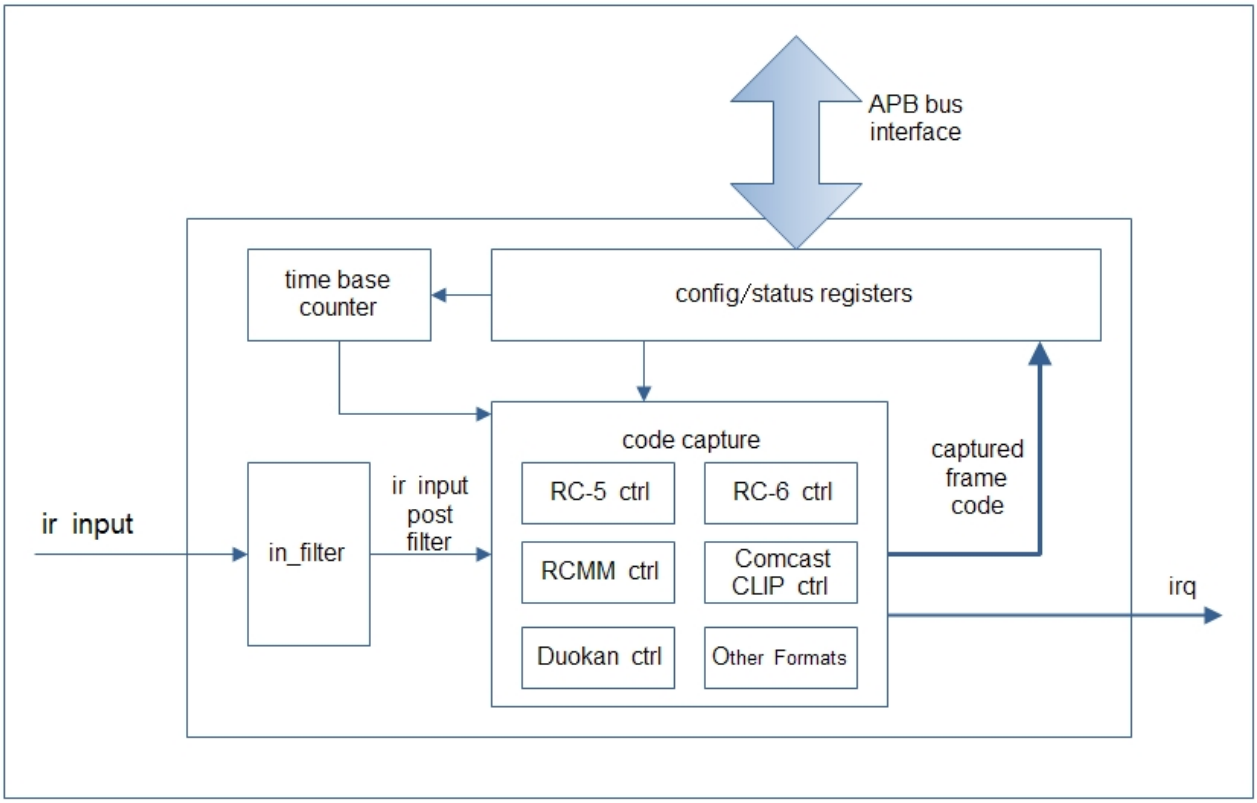
The decoder mainly consisted of two blocks:

- Decoder with input filter
- A set of registers including control & clock, data and tuning

The function diagram of IR decoder is illustrated in the figure below.

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Figure 13-5 IR Decoder Function Block



IR Decoder decodes the IR remote control input signal. 13 operation modes are supported:

- Hardware Decode IR transmission protocol compatible frame decoder mode (NEC MITSUBISHI Thomson Toshiba Sony SIRC RC5 RC6 RCMM Duokan Comcast Sanyo Modes)
- General programmable time measurement frame decoder mode (General Mode)

In Hardware Decode Mode, the Decoder uses signal pattern search mechanism to decode data frame. It can detect logical “0”, “1” , “00”, “01”, “10” and “11”, as well as data frame start and end. Whenever Decoder detects and decodes the data frame, the data are kept in data register.

In General Mode, the Decoder uses edge detection mechanism to decode data frame. It can detect each input signal edge and record the time between two edges. The time measurement result is kept in control register.

The user should set proper operation mode corresponding to the selection of remote controller.

There is a simple time-based signal Filter between the signal input and the Decoder. The Filter is programmable and helps to improve signal integrity.

13.5.5 Register Description

For the following registers:

Base_adr: 0xfe084000

Final_adr = base_adr + offset *4

The following lists describe the mapping between each IR RX/TX register and its address.

IRCTRL_IR_DEC_LDR_ACTIVE 0xfe084000

IRCTRL_IR_DEC_LDR_IDLE 0xfe084004

IRCTRL_IR_DEC_LDR_REPEAT 0xfe084008

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IRCTRL_IR_DEC_BIT_0 0xfe08400c
IRCTRL_IR_DEC_REG0 0xfe084010
IRCTRL_IR_DEC_FRAME 0xfe084014
IRCTRL_IR_DEC_STATUS 0xfe084018
IRCTRL_IR_DEC_REG1 0xfe08401c
IRCTRL_MF_IR_DEC_LDR_ACTIVE 0xfe084040
IRCTRL_MF_IR_DEC_LDR_IDLE 0xfe084044
IRCTRL_MF_IR_DEC_LDR_REPEAT 0xfe084048
IRCTRL_MF_IR_DEC_BIT_0 0xfe08404c
IRCTRL_MF_IR_DEC_REG0 0xfe084050
IRCTRL_MF_IR_DEC_FRAME 0xfe084054
IRCTRL_MF_IR_DEC_STATUS 0xfe084058
IRCTRL_MF_IR_DEC_REG1 0xfe08405c
IRCTRL_MF_IR_DEC_REG2 0xfe084060
IRCTRL_MF_IR_DEC_DURATN2 0xfe084064
IRCTRL_MF_IR_DEC_DURATN3 0xfe084068
IRCTRL_MF_IR_DEC_FRAME1 0xfe08406c
IRCTRL_MF_IR_DEC_STATUS1 0xfe084070
IRCTRL_MF_IR_DEC_STATUS2 0xfe084074
IRCTRL_MF_IR_DEC_REG3 0xfe084078
IRCTRL_MF_IR_DEC_FRAME_RSV0 0xfe08407c
IRCTRL_MF_IR_DEC_FRAME_RSV1 0xfe084080
IRCTRL_MF_IR_DEC_FILTE 0xfe084084
IRCTRL_MF_IR_DEC_IRQ_CTL 0xfe084088
IRCTRL_MF_IR_DEC_FIFO_CTL 0xfe08408c
IRCTRL_MF_IR_DEC_WIDTH_NEW 0xfe084090
IRCTRL_MF_IR_DEC_REPEAT_DET 0xfe084094
IRCTRL_IR_DEC_DEMOD_CNTL0 0xfe0840c0
IRCTRL_IR_DEC_DEMOD_CNTL1 0xfe0840c4
IRCTRL_IR_DEC_DEMOD_IIR_THD 0xfe0840c8
IRCTRL_IR_DEC_DEMOD_THD0 0xfe0840cc
IRCTRL_IR_DEC_DEMOD_THD1 0xfe0840d0
IRCTRL_IR_DEC_DEMOD_SUM_CNT0 0xfe0840d4
IRCTRL_IR_DEC_DEMOD_SUM_CNT1 0xfe0840d8
IRCTRL_IR_DEC_DEMOD_CNT0 0xfe0840dc
IRCTRL_IR_DEC_DEMOD_CNT1 0xfe0840e0
IRCTRL_IR_BLASTER_ADDR0 0xfe08410c
IRCTRL_IR_BLASTER_ADDR1 0xfe084110

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IRCTRL_IR_BLASTER_ADDR2 0xfe084114

IRCTRL_IR_BLASTER_ADDR3 0xfe084118

Table 13-83 IRCTRL_IR_BLASTER_ADDR0

Bit(s)	R/W	Default	Description
31-27	R	0	unused
26	R	-	BUSY: If this bit is 1, then the IR Blaster module is busy.
25	R	-	This output is 1 when the FIFO is Full
24	R	-	This output is 1 when the FIFO is Empty
23-16	R	-	FIFO Level
15-14	R/W	0	Unused
13-12	R/W	0	MODULATOR_TB: This input controls the clock used to create the modulator output. The modulator is typically run between 32khz and 56khz. The modulator output will equal a divided value of the following: 00: system clock “clk” 01: mpeg_xtal3_tick 10: mpeg_1uS_tick 11: mpeg_10uS_tick
11-4	R/W	0	SLOW_CLOCK_DIV: This is a divider value used to divide down the input “clk”. The divider is N+1 so a value of 0 equals divide by 1.
3	R/W	0	SLOW_CLOCK_MODE: Set this signal high to use a special mode in which the “clk” input is driven by a slow clock less than 1Mhz. This is used for low power cases where we want to run the IR Blaster between 32khz and 1Mhz
2	R/W	0	INIT_LOW: Setting this bit to 1 initializes the output to be high. Please set this bit back to 0 when done
1	R/W	0	INIT_LOW: Setting this bit to 1 initializes the output to be low. Please set this bit back to 0 when done
0	R/W	0	ENABLE: 1 = Enable. If this bit is set to 0, then the IR blaster module is reset and put into an IDLE state.

Table 13-84 IRCTRL_IR_BLASTER_ADDR1

Bit(s)	R/W	Default	Description
31-28	R/W	0	unused
27-16	R/W	0	This value is used with “modulator_tb[1:0]” above to create a low pulse. The time is computed as (mod_lo_count+1) x modulator_tb. The purpose for having a low/high count is the modulator output might not be 50% duty cycle. Hi/Lo counters allow us to modulate using a non-50% duty cycle waveform.
15-12	R/W	0	Unused
11-0	R/W	0	This value is used with “modulator_tb[1:0]” above to create a high pulse. The time is computed as (mod_hi_count+1) x modulator_tb

Table 13-85 IRCTRL_IR_BLASTER_ADDR2

Bit(s)	R/W	Default	Description
31-17	R	0	unused
16	W	0	Set this bit to 1 to write the data below to the FIFO

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Bit(s)	R/W	Default	Description
15-12	R	0	Unused
11-0	R/W	0	FIFO data to be written: Bit[12] output level (or modulation enable/disable: 1 = enable) Bit[11:10] Timebase: 00 = 1uS 01 = 10uS 10 = 100uS 11 = Modulator clock Bit[9:0] Count of timebase units to delay

Table 13-86 IRCTRL_IR_BLASTER_ADDR3

Bit(s)	R/W	Default	Description
31-17	R	0	unused
16	R	0	fifo thd pending
8	R/W	0	FIFO irq enable
7:0	R/W	0	FIFO irq threshold.

Table 13-87 IRCTRL_IR_DEC_DEMOD_CNTL0

Bits	R/W	Default	Description
31	R/W	0	Ir demodulor soft_reset:write 1 to reset ir_demodulor,will auto clr to 0
30	R/W	0	Reg_ir_fd_reset :It is used to reset the carrier detection module.write 1 to reset , will auto clr to 0
29	R/W	0	Reg_ir_demod_mode:It is uset to set the demod mode. 0 = count mode; 1 = iir mode.
28	R/W	0	Ir demodulor clk gate bypass:write 1 will bypass clk gate,default is 0
27:16	R/W	0x40	Reg_ir_st_cnt_thd:It is used to set the statistics number for carrier detection.
15:8	R/W	8	Reg_ir_ds_rate:It is uset to set the downsample rate.
7:4	R/W	7	Reg_ir_fsft_1:It is used to set the shift value for input data “1”.
3:0	R/W	9	Reg_ir_fsft_0:It is used to set the shift value for input data “0”.

Table 13-88 IRCTRL_IR_DEC_DEMOD_CNTL1

Bits	R/W	Default	Description
31	R/W	0	Reg_ir_demod_en:ir demod enable ,
30	R/W	0	Reg_ir_invt:ir input invert, invert input at 1.
29:16	R/W	0xa	Reg_ir_proctect1:It is used to set the protection threshold for 1. It is used to filter the glitch.
13:0	R/W	0x3e8	Reg_ir_detect0:It is used to set the detection threshold for signal “0”.

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Table 13-89 IRCTRL_IR_DEC_DEMOD_IIR_THD

Bits	R/W	Default	Description
31:16	R/W	0xdac	Reg_ir_iir_thd1:It is used to set the detection threshold for “1” in iir mode.
15:0	R/W	0xdac	Reg_ir_iir_thd0:It is used to set the detection threshold for “0” in iir mode.

Table 13-90 IRCTRL_IR_DEC_DEMOD_THD0

Bits	R/W	Default	Description
29:16	R/W	0x12c	Reg_ir_thd0_low:It is used to set the low threshold for “0” when statistics.
13:0	R/W	0x1770	Reg_ir_thd0_high:It is used to set the high threshold for “0” when statistics.

Table 13-91 IRCTRL_IR_DEC_DEMOD_THD1

Bits	R/W	Default	Description
29:16	R/W	0x12c	Reg_ir_thd1_low:It is used to set the low threshold for “1” when statistics.
13:0	R/W	0x1770	Reg_ir_thd1_high:It is used to set the high threshold for “1” when statistics.

Table 13-92 IRCTRL_IR_DEC_DEMOD_SUM_CNT0

Bits	R/W	Default	Description
25:0	R	0	Ro_ir_sum_cnt0:It is used to report the sum value for the statistics data “0”.

Table 13-93 IRCTRL_IR_DEC_DEMOD_SUM_CNT1

Bits	R/W	Default	Description
25:0	R	0	Ro_ir_sum_cnt1:It is used to report the sum value for the statistics data “1”

Table 13-94 IRCTRL_IR_DEC_DEMOD_CNT0

Bits	R/W	Default	Description
29:16	R	0	Ro_ir_max_cnt0:It is used to report the maximum value for the statistics data “0”.
13:0	R	0	Ro_ir_min_cnt0:It is used to report the minimum value for the statistics data “0”.

Table 13-95 IRCTRL_IR_DEC_DEMOD_CNT1

Bits	R/W	Default	Description
29:16	R	0	Ro_ir_max_cnt1:It is used to report the maximum value for the statistics data “1”.
13:0	R	0	Ro_ir_min_cnt1:It is used to report the minimum value for the statistics data “1”.

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Table 13-96 IRCTRL_IR_DEC_LDR_ACTIVE: Leader Active Time

Bit(s)	R/W	Default	Description
31-29	R	0	unused
28-16	R/W	0x 1d8	Max Leader ACTIVE time: 9.44mS assuming base rate = 20uS
15-13	R	0	unused
12-0	R/W	0x1ac	Min Leader ACTIVE time: 8.56mS assuming base rate = 20uS

This register controls the min/max leader active time window. For most TV remote controls, the leader active time is about 9mS. The values in this register correspond to counts of the base rate programmed by register 0x2124

Table 13-97 IRCTRL_IR_DEC_LDR_IDLE: Leader Idle Time

Bit(s)	R/W	Default	Description
31-26	R	0	unused
28-16	R/W	0xf8	Max Leader IDLE time: 4.96mS assuming base rate = 20uS
15-13	R	0	unused
12-0	R/W	0xca	Min Leader IDLE time: 4.04mS assuming base rate = 20uS

This register controls the min/max leader IDLE time window. For most TV remote controls, the leader idle time is about 4.5mS. The values in this register correspond to counts of the base rate programmed by register: 0x2124

Table 13-98 IRCTRL_IR_DEC_LDR_REPEAT: Repeat Leader Idle Time

Bit(s)	R/W	Default	Description
31-26	R	0	Unused
25-16	R/W	0x7a	Max REPEAT Leader IDLE time: 2.44mS assuming base rate = 20uS
15-10	R	0	unused
9-0	R/W	0x66	Min REPEAT Leader IDLE time: 2.04mS assuming base rate = 20uS

This register controls the repeat leader IDLE time window. The repeat key uses the standard leader active time (9ms) but a shorter leader idle time.

Table 13-99 IRCTRL_IR_DEC_BIT_0: BIT 0 Identification Time

Bit(s)	R/W	Default	Description
31-26	R	0	Unused
25-16	R/W	0x42	Max BIT 0 time: 1.32mS assuming base rate = 20uS
15-10	R	0	Unused
9-0	R/W	0x2e	Min BIT 0 time: 0.92mS assuming base rate = 20uS

This register controls the min/max BIT 0 time window. For most TV remote controls, the bit 0 time is about 1.125mS. The values in this register correspond to counts of the base rate programmed by register: 0x2124

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Table 13-100 IRCTRL_IR_DEC_REG0: Base Rate Generator

Bit(s)	R/W	Default	Description
31	R	0	Just in case bit. Normally this bit is set to 0 so that the auto-clock gating is enabled. If there is a problem related to the auto-clock gating, then this bit can be set to one to disable the auto-clock gating.
30-28	R/W	0	FILTER_COUNT: This is a new feature to Nike. The IR remote input now has a simple filter that accommodates slow rise times by providing a little hysteresis. The logic works as follows. If the input is low, then an input signal will only be considered HIGH if it remains high for (FILTER_COUNT * 111nS). Similarly, if the input is currently high, it will only be considered LOW if the input signal remains low for (FILTER_COUNT * 111nS).
27-25	R	0	Unused
24-12	R/w	0xFA0	Max Frame Time. 80mS assuming base rate = 20uS This value is used to determine if a code is a repeat code (e.g. leader followed by no data for this amount of time). This value can also be used to catch slow remote codes (i.e. code sequences that are longer than expected).
11-0	R/W	0x13	This value dictates the base rate time for all measurements associated with the IR decoder. In the past, the base rate was divided from the system clock. In the current design, the base rate is divided from a fixed 1uS timer. This 1uS timer is constant and doesn't change (even when the system clock does) Base rate = (count + 1) * 1uS

This register controls the master rate generator for all width measurements made by the IR decoder module.

Table 13-101 IRCTRL_IR_DEC_FRAME: Frame Data

Bit(s)	R/W	Default	Description
31-0	R	0	Frame Data. Format: {custom code, ~custom code, data, ~data}

Note

New keys will be ignored until this register is read if the hold first key bit is set in the decode control register. Reading this register resets an internal hold first flag.

Table 13-102 IRCTRL_IR_DEC_STATUS: Frame Status

Bit(s)	R/W	Default	Description
31	R/W	0	Sim faster: Reserved
30	R/W	0	BIT_1_MATCH_EN: Set this bit to 1 to enable qualification of bit 1 times. In the previous IR decoder module, frame detection only looked at the BIT 0 time to identify a zero bit. If a zero bit time wasn't found, then it was assumed that the bit was a 1. In the updated IR decoder module, the module will look at the BIT 0 time to find zero bits, and the BIT 1 time to find 1 bits. If the width of a pulse doesn't match the zero or the one bit width time, then the frame is considered invalid.
29-20	R/W	0x89	Max BIT 1 time: 2.74mS assuming base rate = 20uS
19-10	R/W	0x57	Min BIT 1 time: 1.74mS assuming base rate = 20uS
9	R	-	IRQ Status. 1 if there is an interrupt
8	R	-	IR Decoder input. This is the level of the digital signal coming into the IR module for decoding. This is the same as reading the I/O pad level.
7	R	-	BUSY. 1 if the decoder isbusy

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Bit(s)	R/W	Default	Description
6-4	R	0	Decoder Status: For debug only 000: OK 001: last frame timed out 010: leader time error (invalid IR signal) 011: repeat error (repeat leader, but other IR transitions found). 100: Invalid bit
3-0	R	0	Frame Status Bit 3: Frame data valid Bit 2: data code error (data != ~data in IR bit stream) Bit 1: custom code error (custom_code != ~custom_code in IR bit stream) Bit 0: 1 = repeat key, 0 = standard key

Table 13-103 IRCTRL_IR_DEC_REG1: Decode / Interrupt Control

Bit(s)	R/W	Default	Description
31	R	0	Unused
30	R/W	0	CNTL_1uS_EQ_CLK: This bit should be set to 1 if the clk81 (system clock) is less than 50 Mhz.
29	R/W	0	CNTL_111nS_EQ_CLK: This bit should be set to 1 if the clk81 (system clock) is less than 50 Mhz.
28-16	R	0	Time measurement since the last time the internal time counter was reset by the rising and/or falling edge of the IR signal. The selection of reset on rising and/or falling edge is determined by the selection of the IRQ (Bits 3-2 below)
15	R/W	1	ENABLE: If this bit is 1, then the state-machines are enabled. If this bit is zero, then the state-machines cleanup and immediately return to idle.
14	R/W	0	USE SYSTEM CLOCK: This is a new feature. 1 = use the system clock, 0 = use the 1uS timebase tick. During normal operation, the module is setup to create a 20uS tick from the 1uS internal timebase of the chip. If the chip is configured to operate using the 32khz RTC oscillator, the 1uS timebase is invalid and therefore the 20uS timebase is invalid. In order to measure time correctly, the IR remote circuit can use the system clock (which in this case is the 32khz oscillator clock) as the master timebase.
13-9	R/W	1f	Number of bits in the IR frame (N-1)
8-7	R/W	0	Decoder mode 00: NEC Frames: Decode Leader and 32 bits 01: Only accumulate bits (skip the leader) 10: Measure Mode: The internal width measuring counter is reset on the rising and/or falling edge of the IR remote signal based on the settings of IRQ Selection below. Just before being reset, the measured width is captured and stored so that it can be read in bits [28:16] of this register. 11: NEC Frames: Decode Leader and 32 bits
6	R/W	1	Hold First Key. If this bit is set true, then the frame data register (0x2125) will only be updated if hasn't already been updated. Once updated, the frame data register will not be updated again until it has been read. This bit can be used to guarantee the first TV remote code captured will not be overwritten by subsequent transmissions from a TV remote. NOTE: You must read the frame data register to clear an internal hold first flag if this bit is set.
5-4	R/W	11	Frame mask. These bits are used to qualify frames for capture. 00: Capture all frames good or bad 01: Capture only frames where data=~data. Ignore custom codes 10: Capture only frames where custom_code = ~custom_code. Ignore data codes 11: Capture only frames where (data=~data) and (custom_code = ~custom_ code)
3-2	R/W	0	IRQ Selection and width measurement reset:

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Bit(s)	R/W	Default	Description
			00: IR Decoder done 01: IR input rising or falling edge detected 10: IR input falling edge detected 11: IR rising edge detected
1	R/W	0	IR Polarity. Polarity of the input signal (VD[0])
0	R/W	0	Set to 1 to reset the IR decoder. This is useful because the IR remote state machine thinks in terms of milliseconds and may take tens of milliseconds to return to idle by itself.

Table 13-104 IRCTRL_MF_IR_DEC_LDR_ACTIVE

Bit(s)	R/W	Default	Description
28:16	R/W	0	Max duration of Leader's active part (The value is in unit of $\mathbf{T}_{RATE}$)
12:0	R/W	0	Min duration of Leader's active part (The value is in unit of $\mathbf{T}_{RATE}$)

Table 13-105 IRCTRL_MF_IR_DEC_LDR_IDLE: Leader Idle control

Bit(s)	R/W	Default	Description
28:16	R/W	0	Max duration of Leader's idle part
12:0	R/W	0	Min duration of Leader's idle part

Table 13-106 IRCTRL_MF_IR_DEC_LDR_REPEAT: Repeat Leader Idle Time

Bit(s)	R/W	Default	Description
25:16	R/W	0	Max duration of Repeat Code's Leader. In NECformat, it defines for the repeat leader's idle part. In Toshiba format, it defines for the repeat leader's second idle part (In Toshiba format, the repeat leader's first idle part has the same duration time as the normal leader idle part.)
9:0	R/W	0	Min duration of Repeat Code's Leader

Table 13-107 IRCTRL_MF_IR_DEC_BIT_0

Bit(s)	R/W	Default	Description
25:16	R/W	0	Max duration of Duration Setting Regiser 0. It defines max tining duration for: Logic"0" for NEC/Toshiba/Sony/Thomas format or Half trailer bit for RC6 format (RC6's half trailer bit typically 888.89us) or time of Duokan/RCMM/4ppm format's Logic "00"
9:0	R/W	0	Min duration of Duration Setting Regiser 0.

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Table 13-108 IRCTRL_MF_IR_DEC_REG0

Bit(s)	R/W	Default	Description
31	R/W	0	Clock gating control just in case. Set 1 can force clock gating disabled.
30:28	R/W	0	Filter ctrl. Set the monitor timing for input filter, bigger value means longer monitor time. Value 0 = no filtering.
27:25	R	0	Unused
24:12	R/W	0	Max frame time. Max duration of one whole frame.
11:0	R/W	0	Base time parameter. Used to generate the timing resolution. Resolution = (base_time_paramter + 1) * (1/ Freq_sys_clk). For example, if Frequency of sys_clk is 1Mhz, and base_time_parameter=19, Then resolution = (19+1)*(1uS) = 20uS.

Table 13-109 IRCTRL_MF_IR_DEC_FRAME

Bit(s)	R/W	Default	Description
31:0	R/W	0	32 bit Read-Only register stores frame body (LSB 32bit) captured from IR remote data flow, commonly includes custom/address code and data code.

Table 13-110 IRCTRL_MF_IR_DEC_STATUS

Bit(s)	R/W	Default	Description
31	R/W	0	Frame data valid 1. (This bit is set to 1 when a captured frame is updated/stored into “FrameBody_1” register. A read of “FrameBody_1” register will clear This bit. “FrameBody_1” register is used to store the over 32bit MSBs of the formats whose length is more than 32 bit)
30	R/W	0	bit_1_match_en. Set to 1 to enable the check of whether logic”1” bit matches timing configure during the frame input process.
29:20	R/W	0	Max Duration 1. Max duration of Duration Setting Regiser 1. It defines max duration for: Logic”1” for NEC/Toshiba/Sony format or Whole trailer bit for RC6 format (RC6’s whole trailer bit typically 1777.78us) or time of Duokan/RCMM/4ppm format’s Logic “01”
19:10	R/W	0	Min Duration 1. Min duration of Duration Setting Regiser 1.
9	R	0	irq_status. Appear as 1 if there is an interrupt.
8	R	0	ir_i_sync. IR remote serial input after synchronization. This is the level of the digital signal coming into the IR module for decoding. This is the same as reading the I/O pad level.
7	R	0	Busy. When =1, means state machine is active.

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Bit(s)	R/W	Default	Description
6:4	R	0	Decoder_status (for debug only). 000: OK 001: last frame timed out 010: leader time error (invalid IR signal) 011: repeat error (repeat leader, but other IR transitions found). 100: Invalid bit
3:0	R	0	Frame status. bit 3: Frame data valid (This bit is set to 1 when a captured frame is updated/stored into “FrameBody” register. A read of “FrameBody” register will clear This bit. If store and read occurs at the same time, This bit is set to 1 in common, But if “Hold first” is set to true and this valid Bit is already 1, a read clear takes precedance and This bit is clear to 0.) bit 2: data code error (data != ~data in IR bit stream) bit 1: custom code error (custom_code != ~custom_code in IR bit stream) bit 0: 1 = received frame is repeat key, 0 = received frame is normal key

Table 13-111 IRCTRL_MF_IR_DEC_REG1

Bit(s)	R/W	Default	Description
31	R/W	0	Set to 1 to use faster timebase. .
30	R/W	0	cntl_1us_eq_clk. Just use sys_clk to relace 1uS tick.
29	R/W	0	cntl_xtal3_eq_clk. Just use sys_clk to relace 111ns tick.
28:16	R	0	Pulse Width Counter. It stores the internal counter of pulse width duration. Commonly used as time measurement when decode_mode is set to measure width mode (software decode). Time measurement starts at the last time the internal time counter was reset by the rising and/or falling edge of the IR signal. The selection of reset on rising and/or falling edge is determined by the IRQ Selection field (Bits 3-2 below)
15	R/W	0	Enable. 1 = enable the state machine of IR decoder. 0 = disable the state machine of IR decoder.
14	R/W	0	cntl_use_sys_clk. Use sys_clk for the timebase. It’s useful when sys_clk at low frequency (such as 32Khz) and cannot create 1uS timebase tick. 1 = use the system clock as timebase. 0 = use the 1uS timebase tick as timebase.
13:8	R/W	0	bit_length minus 1. (N-1). Used to set the value of frame body’s bit length (frame body commonly includes address and data code part). If a format has 24 bit frame body, this value shall be set to 23.
7	R/W	0	Record_at_error. 1= record the frame body and status forcibly, even if data/custom code error check enabled by frame_mask and relative error occurs. 0 = if data/custom code error check enabled by frame_mask and relative error occurs, not record the frame body and status forcibly
6	R/W	0	Hold_first Used to hold the first captured frame data. If This bit is set to 1, then the “Frame-Body/FrameBody_1” register will only be updated if hasn’t already been updated. Once updated, the “FrameBody/FrameBody_1” register will not be updated again until it has been read. This bit can be used to guarantee the first TV remote code captured will not be overwritten by subsequent transmissions from a TV remote. NOTE: Read the”FrameBody” register can clear the internal “Frame data valid” flag, and read the “FrameBody_1” register can clear the “Frame data valid 1” flag.
5:4	R/W	0	Frame_mask.

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Bit(s)	R/W	Default	Description
			Some formats' body include bit-inversed data or custom/address code for error check. 00 = ignore error check from either data or custom/address code 01= check if data code matches its inverse values, ignore error check from custom/address code 10= check if custom/address code matches its inverse values, ignore error check from data code 11= check if data and custom codes match their inverse values
3:2	R/W	0	Irq_sel. IRQ Selection and width measurement reset: 00: IR Decoder done 01: IR input rising or falling edge detected 10: IR input falling edge detected 11: IR rising edge detected
1	R/W	0	IR input polarity selection. Used to adjust/invert the polarity of IR input waveform.
0	R/W	0	Decoder Reset. Set to 1 to reset the IR decoder. This is useful because the IR remote state machine thinks in terms of milliseconds and may take tens of milliseconds to return to idle by itself.

Table 13-112 IRCTRL_MF_IR_DEC_REG2

Bit(s)	R/W	Default	Description
26	R/W	0	Width_low_enable. Enable counter record of low pulse width duration. 0 = do not force enable of width low counter record 1 = force enable of width low counter record Some IR formats' decoding need to use internal width low counter record. By default, the width low counter record is enabled automatically for related formats. This bit is used for enable forcibly just in case. Besides, if "leader plus stop bit" method is enabled for repeat detection, this bit is also need to be enabled.
25	R/W	0	Width_high_enable. Enable counter record of high pulse width duration. 0 = do not force enable of width high counter record 1 = force enable of width high counter record Some IR formats' decoding need to use internal width high counter record. By default, the width high counter record is enabled automatically for related formats. This bit is used for enable forcibly just in case.
24	R/W	0	Enable "leader plus stop bit" method for repeat detection . 0 = "leader plus stop bit" method disabled 1 = "leader plus stop bit" method enabled Some IR formats use one normal frame's leader followed by a stop bit to represet repeat. There is no frame data in this kind repeat frame. To use this method, width_low_enable (bit[26] of 0x20 offset register) shall be set to 1, and max_duration_3 and min_duration_3 in 0x28 offset register shall be set to appropriate value for stop bit's timing duration.
21:16	R/W	0	Repeat_bit_index. These bits are used for compare bit method to set the index of the bit that is used as repeat flag. The index value can be 0 to 63. Compare bit method is one of the methods for repeat detection . Some IR formats use one bit in frame to represet whether the frame is repeat.
15	R/W	0	Running_count_tick_mode. This bit is only valid when use_clock_to_counter bit is 0. 0 = use 100uS as increasing time unit of frame-to-frame counter 1 = use 10uS as increasing time unit of frame-to-frame counter
14	R/W	0	Use_clock_to_counter. If this bit is set to 1, the running_count_tick_mode bit is ignored. 0 = do not use system clock as increasing time unit of frame-to-frame counter 1 = use system clock as increasing time unit of frame-to-frame counter

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Bit(s)	R/W	Default	Description
13	R/W	0	Enable frame-to-frame time counter (running-counter). 0 = frame-to-frame time counter disabled 1 = frame-to-frame time counter enabled If enabled, the frame-to-frame counter increases every 100uS or 10uS until it reaches its max value(all bits are 1) or it is reset. When it reaches its max value, it keeps the value until it is reset. When it is reset, it becomes zero and then begin increasing again. The counter can be reset even when it has not reached its max value. The increasing time unit can be 100uS or 10uS or system clock frequency which is set by running_count_tick_mode and use_clock_to_counter settings. When a frame's data are capured and stored into FrameBody/FrameBody_1 register, frame-to-frame counter is reset to zero. After reset to zero, the frame-to-frame counter will begin increasing again, until it reaches its max value or it is reset. For repeat frame detection, users can use hardware detection by enabling compare frame or compare bit method, or users can read frame-to-frame counter to let software to make the decision.
12	R/W	0	Enable repeat time check for repeat detection . This bit is valid only when compare frame method or compare bit method is enabled. 0 = repeat time check disabled 1 = repeat time check enabled When repeat frame detection is enabled by enabling compare frame or compare bit method, the frame time interval may need to be checked in order to decide whether the frames are repeat (key pressed without release) or not. You can configure the repeat_time_max value by setting 0x38 offset register. If frame interval is smaller than the "repeat time max", it may considered as repeat. If frame interval is bigger than the "repeat time max", it is considered as not repeat.
11	R/W	0	Enable compare frame method for repeat detection . 0 = compare frame method disabled 1 = compare frame method enabled Some IR formats transer the same data frame as repeat frame when the key is kept pressed without release. For repeat detection, compare frame method can be used. If a new frame and the old received frame are the same and the repeat time is under the limit(frame-to-frame time counter value is smaller than the repeat_time_max), the status register's frame_status[0] is set to 1 automatically as repeat detected flag. You can configure the repeat_time_max value by setting 0x38 offset register.
10	R/W	0	Enable compare bit method for repeat detection . 0 = compare bit method disabled 1 = compare bit method enabled Some IR formats use only one bit to represet whether the frame is repeat. You can compare only one bit instead of compare the whole frame for repeat detection. If compare frame method is enabled, then this bit is ignored.
9	R/W	0	Disable read-clear of FrameBody/FrameBody_1. 0 = read-clear enabled 1 = read-clear disabled FrameBody/FrameBody_1 registers are read-cleared in default. When these register are read, they are cleared to zero. This bit is used to disable this read-clear feature. (FrameBody/FrameBody_1 registers are used to store captured frame data).

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Bit(s)	R/W	Default	Description
8	R/W	0	input stream bit order. 0 = LSB first mode (first bit in input stream is considered as LSB) 1= MSB first mode (first bit in input stream is considered as MSB) Note: Commonly the following formats shall set 1 to enable MSB first mode (unless you insist on LSBfirst mode for your specified use): RC5, RC5 extend, RC6, RCMM, Duokan, Comcast
3:0	R/W	0	Decode_mode.(format selection) 0x0 =NEC 0x1= skip leader (just bits, without leader) 0x2=General time measurement (measure width, software decode) 0x3=MITSUBISHI or 50560 0x4=Thomson 0x5=Toshiba 0x6=Sony SIRC 0x7=RC5 0x8=Reserved 0x9=RC6 0xA=RCMM 0xB=Duokan 0xC=Reserved 0xD=Reserved 0xE=Comcast 0xF=Sanyo

Table 13-113 IRCTRL_MF_IR_DEC_DURATN2

Bit(s)	R/W	Default	Description
31:26	R	0	Unused
25:16	R/W	0	Max duration of Duration Setting Regiser 2. It defines max duration for: Half bit for RC5/6 format (RC5 typically 888.89us for half bit, RC6 typically 444.44us) or time of Duokan/RCMM/4ppm format's Logic "10" or time of Comcast/16ppm's base duration
15:10	R	0	Unused
9:0	R/W	0	Min duration of Duration Setting Regiser 2.

Table 13-114 IRCTRL_MF_IR_DEC_DURATN3

Bit(s)	R/W	Default	Description
31:26	R	0	Unused
25:16	R/W	0	Max duration of Duration Setting Regiser 3. It defines max duration for: Whole bit for RC5/6 format (RC5 typically 1777.78us for whole bit, RC6 typically 888.89us) or time of Duokan/RCMM/4ppm format's Logic "11" or time of Comcast/16ppm's offset duration
15:10	R	0	Unused
9:0	R/W	0	Min duration of Duration Setting Regiser 3.

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Table 13-115 IRCTRL_MF_IR_DEC_FRAME1: Frame Body 1 (Frame Data, MSB 32Bit)

Bit(s)	R/W	Default	Description
31:0	R	0	Stores frame body excess 32 bit range. (MSB 32 bit)

Note

New keys will be ignored until **FrameBody** register is read if the hold first key Bit is set in the decode control register. Reading this register resets an internal frame data valid flag.

Table 13-116 IRCTRL_MF_IR_DEC_STATUS_1

Bit(s)	R/W	Default	Description
31:20	R	0	Unused
19:0	R	0	Stores the last frame-to-frame counter value before the last counter reset caused by the last frame data record/update.

Table 13-117 IRCTRL_MF_IR_DEC_STATUS_2

Bit(s)	R/W	Default	Description
31:20	R	0	Unused
19:0	R	0	Stores the value of the frame-to-frame counter which is running currently.

Table 13-118 IRCTRL_MF_IR_DEC_REG3

Bit(s)	R/W	Default	Description
19:0	R/W	0	Repeat time max. Used to set the maximum time between two repeat frames for repeat frame detection. Time unit is 100uS or 10uS according to the running_count_tick_mode. When repeat frame detection is enabled by enabling compare frame or compare bit method, the frame time interval may need to be checked in order to decide whether the frames are repeat (key pressed without release) or not. If frame interval is smaller than the “repeat time max”, it may considered as repeat. If frame interval is bigger than the “repeat time max”, it is considered as not repeat.

Table 13-119 IRCTRL_MF_IR_DEC_FRAME_RSV0

Bit(s)	R/W	Default	Description
31:0	R/W	0	Frame Reserved register 0. Stores the LSB 32bit of the previous frame’s frame data while the “*Frame_Body*” register stores the LSB 32bit of the current frame’s frame data.

Table 13-120 IRCTRL_MF_IR_DEC_FRAME_RSV1

Bit(s)	R/W	Default	Description
31:0	R/W	0	Frame Reserved register 0. Stores the LSB 32bit of the previous frame’s frame data while the “*Frame_Body*” register stores the LSB 32bit of the current frame’s frame data.

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Table 13-121 IRCTRL_MF_IR_DEC_FILTE

Bit(s)	R/W	Default	Description
31	R/W	0	New filter ctrl enable: 1:new filter ctrl enable 0:old filter ctrl enable
12:0	R/W	0	New Filter ctrl Set the monitor timing for input filter, bigger value means longer monitor time. Value 0 = no filtering.

Table 13-122 IRCTRL_MF_IR_DEC_IRQ_CTL

Bit(s)	R/W	Default	Description
31	R/W	0	Interrupt enable 1:remote ir will generate irq 0:remote ir will not generate irq
30	R/W	0	Repeat idle mux 1:not check input single in NEC repeat idle state in the time of repeat_dely_time 0:check single
29	R/W	0	Release status Release pending bit ,write 1 to 0
28:16	R/W	0	Repeat_dely_time The time will not check input single after repeat leader
15:14	R/W	0	reversed
13	R/W	0	Release irq enable 1:release will generate irq 0:release will not generate irq
12:0	R/W	0	Release_det_time The time to judge release after irq

Table 13-123 IRCTRL_MF_IR_DEC_FIFO_CTL

Bit(s)	R/W	Default	Description
31	R/W	0	Fifo mode enable,only use in measure mode 1:fifo mode enable 2:use old measure mode
30	R/W	0	Fifo trigger pending,write 1 to 0 Fifo have received X dates.X configured by IR_DEC_FIFO_CTL[20:13]
29	R/W	0	Fifo in timeout pending,write 1 to 0 Fifo have not received data in X.X configured by IR_DEC_FIFO_CTL[12:0]
28	R/W	0	Fifo full
27	R/W	0	Fifo empty
26	R/W	0	Fifo initial
25:21	R/W	0	revered

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Bit(s)	R/W	Default	Description
20:13	R/W	0	Fifo trigger irq level Default is ‘h16
12:0	RIRCTR-L_MF_/W	0	Fifo in timeout Default is ‘d800

Table 13-124 IRCTRL_MF_IR_DEC_WIDTH_NEW

Bit(s)	R/W	Default	Description
12:0	R/W	0	Width new When use fifo mode,should read width from this register

Table 13-125 IRCTRL_MF_IR_DEC_REPEAT_DET

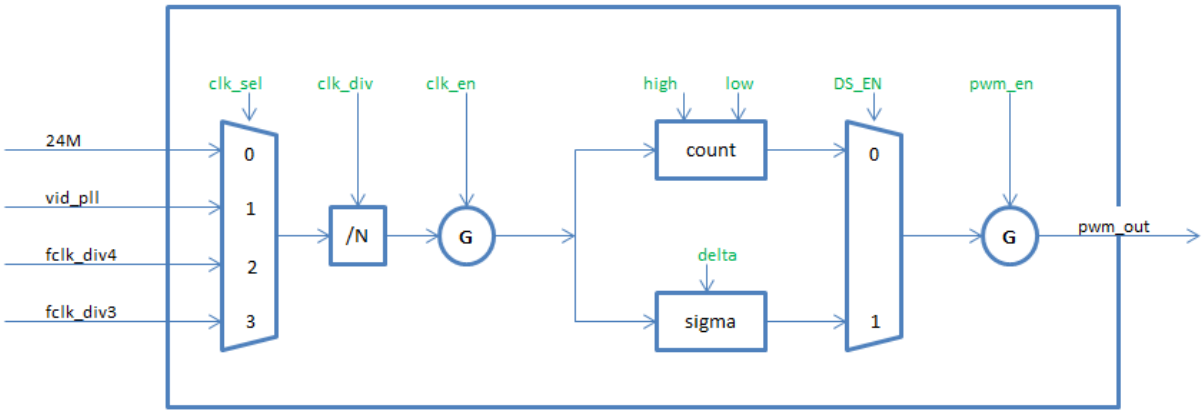
Bit(s)	R/W	Default	Description
31	R/W	0	Repeat detect mux enable
28:16	R/W	0	Max repeat idle time
12:0	R/W	0	Min repeat idle time

13.6 Pulse-Width Modulation

13.6.1 Overview

The chip has 6 PWM modules that can be connected to various digital I/O pins. Each PWM is driven by a programmable divider driven by a 4:1 clock selector. The PWM signal is generated using two 16-bit counters. One is the High and Low counter, which is individually programmable with values between 1 and 65535. Using a combination of the divided clock (divide by N) and the HIGH and LOW counters, a wide number of PWM configurations are possible. The other is delta-sigma counter, generate 18-bit sigma, the PWM-out is the highest sigma. The PWM outputs vs counters are also illustrate below.

Figure 13-6 PWM Block Diagram



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Figure 13-7 High/Low Counter

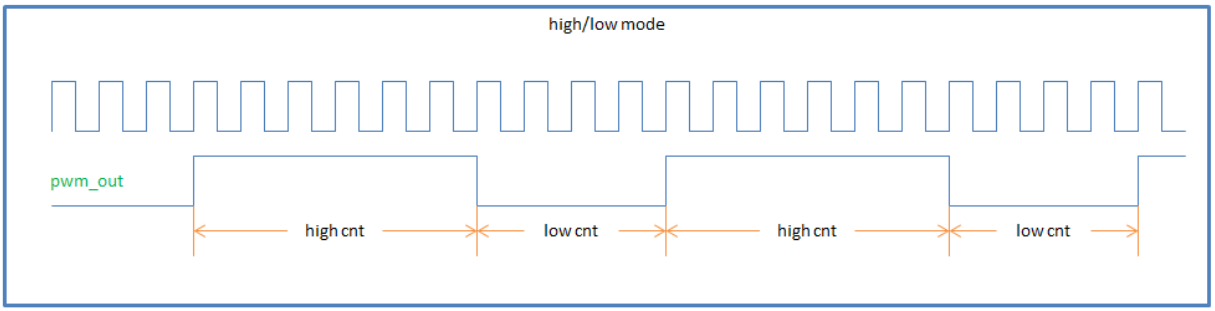
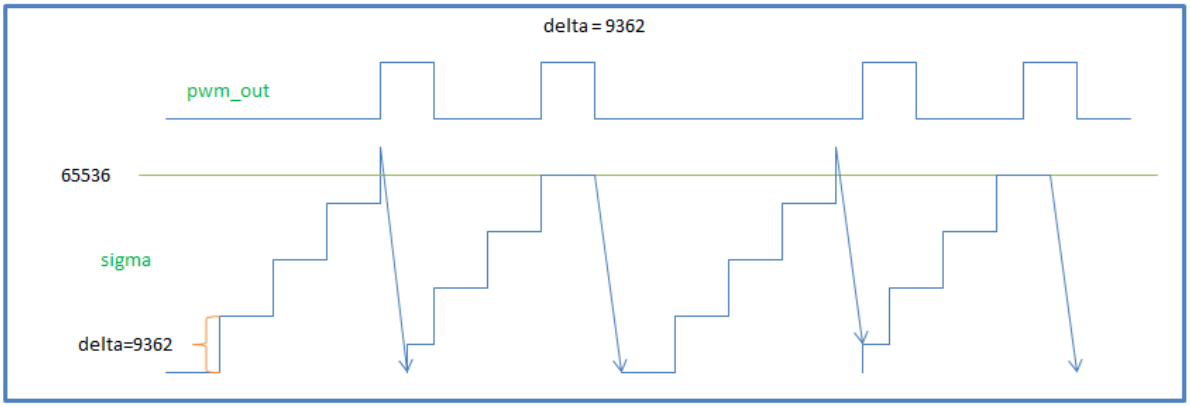
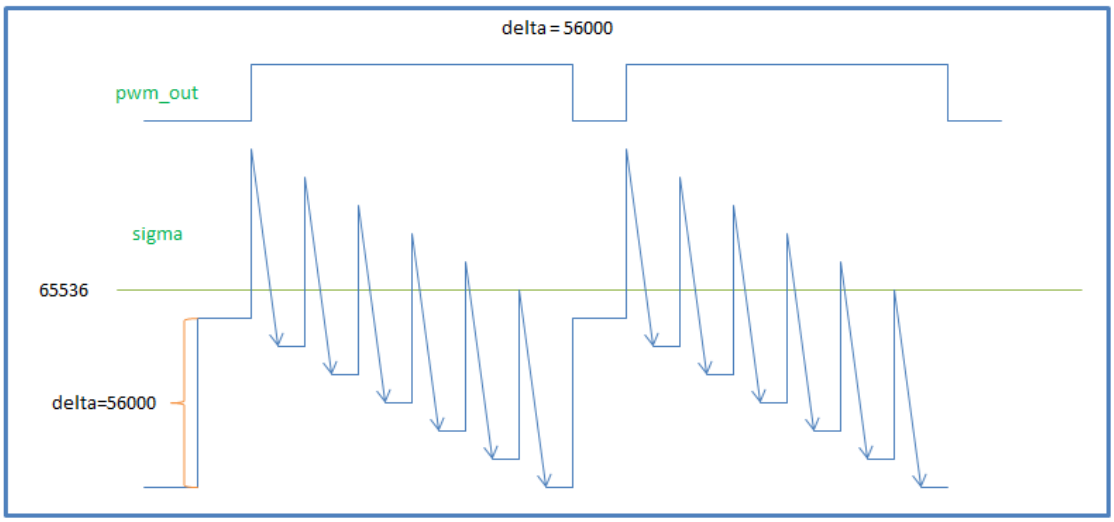


Figure 13-8 Delta-sigma Conter

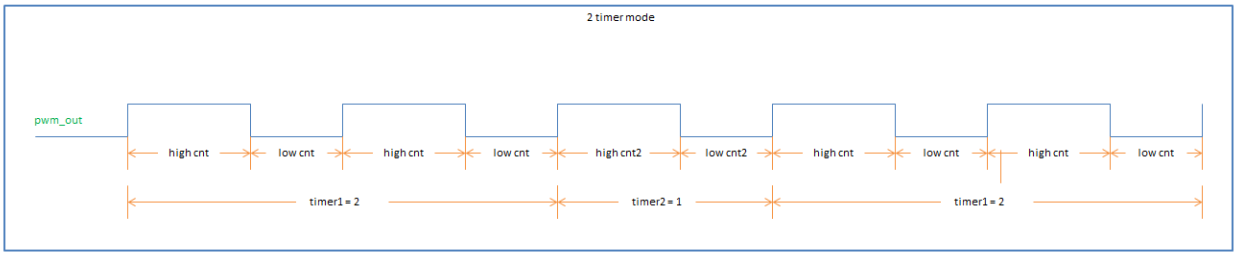




PWM 2 timer mode is illustrated as following:

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Figure 13-9 2 Timer Mode



13.6.2 Register Description

Each PWM module can generate 2 PWM. PWM_CD/EF/GH/IJ usage are the same as PWM_AB.

For the following registers:

Base_adr: 0xfe058000

Final_adr = base_adr + offset *4

The following lists describe the mapping between each PWM_AB register and its address.

PWMAB_PWM_A 0xfe058000

PWMAB_PWM_B 0xfe058004

PWMAB_MISC_REG_AB 0xfe058008

PWMAB_DELTA_SIGMA_AB 0xfe05800c

PWMAB_TIME_AB 0xfe058010

PWMAB_A2 0xfe058014

PWMAB_B2 0xfe058018

PWMAB_BLINK_AB 0xfe05801c

PWMAB_LOCK_AB 0xfe058020

Table 13-126 PWMAB_PWM_A

Bit(s)	R/W	Default	Description
31-15	R/W	134	PWM_A_HIGH: This sets the high time (in clock counts) for the PWM_A generator output
15-0	R/W	134	PWM_A_LOW: This sets the high time (in clock counts) for the PWM_A generator output

Table 13-127 PWMAB_PWM_B

Bit(s)	R/W	Default	Description
31-15	R/W	80	PWM_B_HIGH: This sets the high time (in clock counts) for the PWM_B generator output
15-0	R/W	8	PWM_B_LOW: This sets the high time (in clock counts) for the PWM_B generator output

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Table 13-128 PWMAB_MISC_REG_AB

Bit(s)	R/W	Default	Description
31	R/W	0	pwm_B_hiz when hiz mode, pwm_o will connect to pad_oe, then pad_o will equal this bit
30	R/W	0	pwm_A_hiz when hiz mode, pwm_o will connect to pad_oe, then pad_o will equal this bit
29	R/W	0	pwm_B_constant_en
28	R/W	0	pwm_A_constant_en
27	R/W	0	pwm_B_inv_en
26	R/W	0	pwm_A_inv_en
25	R/W	0	cntl_pwm_a2_en
24	R/W	0	cntl_pwm_b2_en
23	R/W	0	PWM_B_CLK_EN: Set this bit to 1 to enable PWM B clock
22-16	R/W	0	PWM_B_CLK_DIV: Selects the divider (N+1) for the PWM B clock. See the clock tress document
15	R/W	0	PWM_A_CLK_EN: Set this bit to 1 to enable PWM A clock
14-8	R/W	0	PWM_A_CLK_DIV: Selects the divider (N+1) for the PWM A clock. See the clock tress document
7-6	R/W	0	PWM_B_CLK_SEL: Select the clock for the PWM B. See the clock tress document
5-4	R/W	0	PWM_A_CLK_SEL: Select the clock for the PWM A. See the clock tress document
3	R/W	0	DS_B_EN: This bit is only valid if PWM_B_EN is 0: if this bit is set to 1, then the PWM_B output is configured to generate a delta sigma output based on the settings in the register below. If this bit is set to 0, then the PWM_B output is set low.
2	R/W	0	DS_A_EN: This bit is only valid if PWM_A_EN is 0: if this bit is set to 1, then the PWM_A output is configured to generate a delta sigma output based on the settings in the register below. If this bit is set to 0, then the PWM_A output is set low.
1	R/W	0	PWM_B_EN: If this bit is set to 1, then the PWM_B output is configured to generate a PWM output based on the register above. If this bit is 0, then the PWM_B output is controlled by DS_B_EN above.
0	R/W	0	PWM_A_EN: If this bit is set to 1, then the PWM_A output is configured to generate a PWM output based on the register above. If this bit is 0, then the PWM_A output is controlled by DS_A_EN above.

Table 13-129 PWMAB_DELTA_SIGMA_AB

Bit(s)	R/W	Default	Description
31-15	R/W	0x8000	DS_B_VAL: This value represents the delta sigma setting for channel B (PWM_B)
15-0	R/W	0x8000	DS_A_VAL: This value represents the delta sigma setting for channel A (PWM_A)

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Table 13-130 PWM_TIME_AB

Bit(s)	R/W	Default	Description
31-24	R/W	10	A_timer1
23:16	R/W	10	A_timer2
15:8	R/W	10	B_timer1
7:0	R/W	10	B_timer2

Table 13-131 PWMAB_A2

Bit(s)	R/W	Default	Description
31-15	R/W	134	PWM_A2_HIGH: This sets the high time (in clock counts) for the PWM_A2 generator output
15-0	R/W	134	PWM_A2_LOW: This sets the high time (in clock counts) for the PWM_A2 generator output

Table 13-132 PWMAB_B2

Bit(s)	R/W	Default	Description
31-15	R/W	80	PWM_B2_HIGH: This sets the high time (in clock counts) for the PWM_B2 generator output
15-0	R/W	8	PWM_B2_LOW: This sets the high time (in clock counts) for the PWM_B2 generator output

Table 13-133 PWMAB_LOCK_AB

Bit(s)	R/W	Default	Description
0	R/W	0	1: will lock all PWM register

13.7 SAR ADC

13.7.1 Overview

This SAR ADC is a general purpose ADC for measuring analog signals. The module can make RAW ADC measurements or average a number of measurements to introduce filtering. The SAR ADC is a single block so an analog mux is placed in front to allow multiple different measurements to be made sequentially. Timing of the samples, and delays between muxing are all programmable as is the averaging to be applied to the SAR ADC.

13.7.2 Register Description

For the following registers:

Base_adr: 0xfe026000

Final_adr = base_adr + offset *4

The following lists describe the mapping between each SAR_ADC register and its address.

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SAR_ADC_REG0 0xfe026000
SAR_ADC_CHAN_LIST 0xfe026004
SAR_ADC_AVG_CNTL 0xfe026008
SAR_ADC_REG3 0xfe02600c
SAR_ADC_DELAY 0xfe026010
SAR_ADC_LAST_RD 0xfe026014
SAR_ADC_FIFO_RD 0xfe026018
SAR_ADC_AUX_SW 0xfe02601c
SAR_ADC_CHAN_10_SW 0xfe026020
SAR_ADC_DETECT_IDLE_SW 0xfe026024
SAR_ADC_DELTA_10 0xfe026028
SAR_ADC_REG11 0xfe02602c
SAR_ADC_REG12 0xfe026030
SAR_ADC_REG13 0xfe026034
SAR_ADC_CHNL01 0xfe026038
SAR_ADC_CHNL23 0xfe02603c
SAR_ADC_CHNL45 0xfe026040
SAR_ADC_CHNL67 0xfe026044

Table 13-134 SAR_ADC_REG0: Control Register #0

Bit(s)	R/W	Default	Description
31	R	0	PANEL DETECT level.
30	R	0	DELTA_BUSY: If This bit is 1, then it indicates the delta processing engine is busy
29	R	0	AVG_BUSY: If This bit is 1, then it indicates the averaging engine is busy
28	R	0	SAMPLE_BUSY: If This bit is 1, then it indicates the sampling engine is busy
27	R	0	FIFO_FULL:
26	R	0	FIFO_EMPTY:
25-21	R/W	4	FIFO_COUNT: Current count of samples in the acquisition FIFO
20-19	R/W	0	ADC_BIAS_CTRL
18-16	R/W	0	CURR_CHAN_ID: These Bits represent the current channel (0..7) that is being sampled.
15	R	0	Unused
14	R/W	0	SAMPLING_STOP: This bit can be used to cleanly stop the sampling process in the event that continuous sampling is enabled. To stop sampling, simply set This bit and wait for all processing modules to no longer indicate that they are busy.
13-12	R/W	0	CHAN_DELTA_EN: There are two Bits corresponding to Channels 0 and 1. Channel 0 and channel 1 can be individually enabled to take advantage of the delta processing module.
11	R/W	0	Unused

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Bit(s)	R/W	Default	Description
10	R/W	0	DETECT_IRQ_POL: This bit sets the polarity of the detect signal. The detect signal is used during X/Y panel applications to detect if the panel is touched
9	R/W	0	DETECT_IRQ_EN: If This bit is set to 1, then an interrupt will be generated if the DETECT signal is low/high. The polarity is set in the bit above.
8-4	R/W	0	FIFO_CNT_IRQ: When the FIFO contains N samples, then generate an interrupt (if bit 3 is set below).
3	R/W	0	FIFO_IRQ_EN: Set This bit to 1 to enable an IRQ when the acquisition FIFO reaches a certain level.
2	W	0	SAMPLE_START: This bit should be written to 1 to start sampling.
1	R/W	0	CONTINUOUS_EN: If This bit is set to 1, then the channel list will be continually processed
0	R/W	0	SAMPLING_ENABLE: Setting This bit to '1' enables the touch panel controller sampling engine, averaging module, XY processing engine and the FIFO.

Table 13-135 SAR_ADC_CHAN_LIST:Channel List

Bit(s)	R/W	Default	Description
31-27	R/W	0	unused
26-24	R/W	2	Length of the list of channels to process. If this value is 2, then only channels in Bits [8:0] below are processed.
23-21	R/W	7	8th channel
20-18	R/W	6	7th channel
17-15	R/W	5	6th channel
14-12	R/W	4	5th channel
11-9	R/W	3	4th channel
8-6	R/W	2	3rd channel
5-3	R/W	1	2nd channel
2-0	R/W	0	First channel in the list of channels to process

Table 13-136 SAR_ADC_AVG_CNTL:Sampling/Averaging Modes

Bit(s)	R/W	Default	Description
31-30	R/W	0	Channel 7: Averaging mode: 0 = no averaging, 1 = simple averaging, 2 = median averaging.
29-28	R/W	0	Channel 6: Averaging mode: 0 = no averaging, 1 = simple averaging, 2 = median averaging.
27-26	R/W	0	Channel 5: Averaging mode: 0 = no averaging, 1 = simple averaging, 2 = median averaging.
25-24	R/W	0	Channel 4: Averaging mode: 0 = no averaging, 1 = simple averaging, 2 = median averaging.
23-22	R/W	0	Channel 3: Averaging mode: 0 = no averaging, 1 = simple averaging, 2 = median averaging.
21-20	R/W	0	Channel 2: Averaging mode: 0 = no averaging, 1 = simple averaging, 2 = median averaging.

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Bit(s)	R/W	Default	Description
19-18	R/W	0	Channel 1: Averaging mode: 0 = no averaging, 1 = simple averaging, 2 = median averaging.
17-16	R/W	0	Channel 0: Averaging mode: 0 = no averaging. 1 = simple averaging of the number of samples acquired (1,2,4 or 8). 2 = median averaging. NOTE: If these Bits are set to 2, then you must set the number of samples to acquire below to 8.
15-13	R/W	0	Channel 7: Number of samples to acquire 2N:
13-12	R/W	0	Channel 6: Number of samples to acquire 2N:
11-10	R/W	0	Channel 5: Number of samples to acquire 2N:
9-8	R/W	0	Channel 4: Number of samples to acquire 2N:
7-6	R/W	0	Channel 3: Number of samples to acquire 2N:
5-4	R/W	0	Channel 2: Number of samples to acquire 2N:
3-2	R/W	0	Channel 1: Number of samples to acquire 2N:
1-0	R/W	0	Channel 0: Number of samples to acquire 2N: 0 = 1, 1 = 2, 2 = 4, 4 = 8.

Each channel listed in the CHANNEL_LIST is given independent control of the number of samples to acquire and averaging mode.

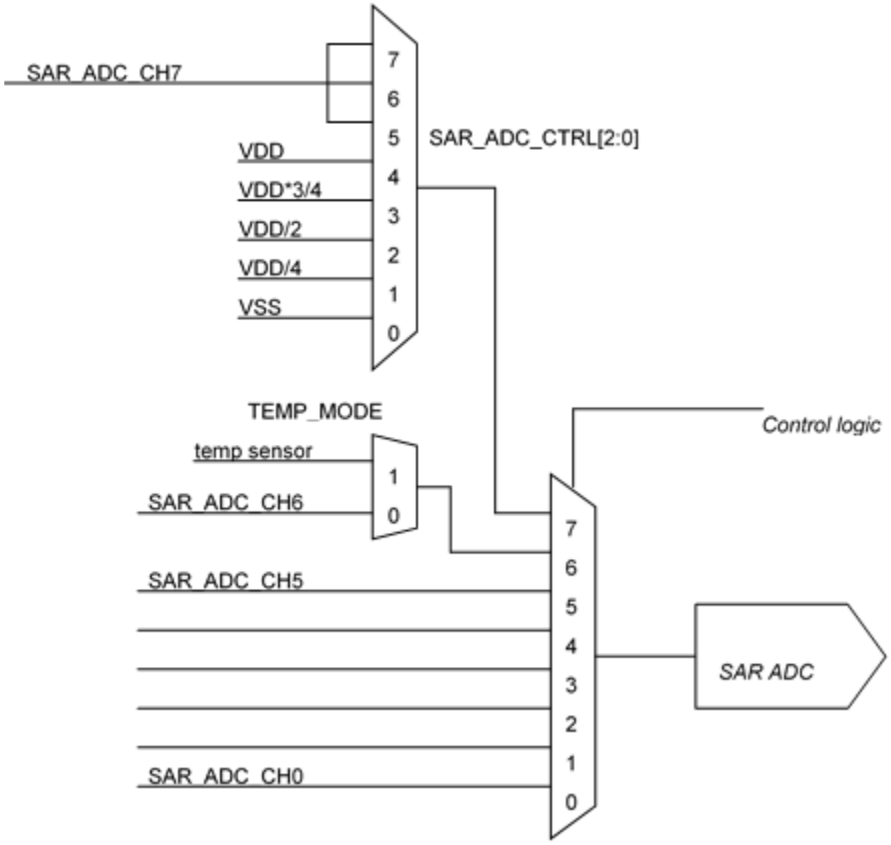
Table 13-137 SAR_ADC_REG3: Control Register #3

Bit(s)	R/W	Default	Description
31	R/W	0	CNTL_USE_SC_DLY: hold time delay was added to the start conversion clock. Unfortunately, it appears that the analog ADC design requires that we use the inverted clock so This bit is meaningless.
30	R/W	0	SAR ADC_CLK_EN: 1 = enable the SAR ADC clock
29	R/W	0	reserved
28	R/W	0	reserved
27	R/W	0	SARADC_CTRL[4]: is used to control the internal ring counter. 1 = enable the continuous ring counter. 0 = disable
26	R/W	0	SARADC_CTRL[3]: used to select the internal sampling clock phase
25~23	R/W	0	SARADC_CTRL[2:0]: 000 ssa 001 vdda/4 010 vdda/2 011 vdda*3/4 100 vdda 101, 110, 111 unused
22	R/W	0	DETECT_EN: This bit controls the analog switch that connects a 50k resistor to the X+ signal. Setting This bit to 1 closes the analog switch
21	R/W	0	ADC_EN: Set This bit to 1 to enable the ADC
20-18	R/W	2	PANEL_DETECT_COUNT: Increasing this value increases the filtering on the panel detect signal using the timebase settings in Bits [17:16] below.
17-16	R/W	0	PANEL_DETECT_FILTER_TB: 0 = count 1uS ticks, 1 = count 10uS ticks, 2 = count 100uS ticks. 3 = count 1mS ticks
15-10	R/W	20	ADC_CLK_DIV: The ADC clock is derived by dividing the 27Mhz crystal by N+1. This value divides the 27Mhz clock to generate an ADC clock. A value of 20 for example divides the 27Mhz clock by 21 to generate an equivalent 1.28Mhz clock.

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Bit(s)	R/W	Default	Description
9-8	R/W	1	BLOCK_DLY_SEL: 0 = count 1uS ticks, 1 = count 10uS ticks, 2 = count 100uS ticks. 3 = count 1mS ticks
7-0	R/W	10	BLOCK_DLY: After all channels in the CHANNEL_LIST have been processed, the sampling engine will delay for an amount of time before re-processing the CHANNEL_LIST again. Combined with Bits [9:8] above, this value is used to generate a delay between processing blocks of channels.

Figure 13-10 SAR_ADC_REG3



As the CHANNEL_LIST is process, the input switches are set according to the requirements of the channel. After setting the switches there is a programmable delay before sampling begins. Additionally, each channel specifies the number of samples for that particular channel. The sampling rate is programmed below.

Table 13-138 SAR_ADC_DELAY:INPUT / SAMPLING DELAY

Bit(s)	R/W	Default	Description
31-29	R	0	unused
28	R/W	0	CNTL_EOC_BY_CNT: ADC dout valid controlled by counter
27	R/W	0	CNTL_USE_LATCHED_DATA: ADC dout be latched first, then be sampled
26	R	0	unused
25-24	R/W	0	INPUT_DLY_SEL: 0 = 111nS ticks, 1 = count 1uS ticks, 2 = count 10uS ticks, 3 = count 100uS ticks

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Bit(s)	R/W	Default	Description
23-16	R/W	3	INPUT_DLY_CNY: For channels that acquire 2,4 or 8 samples, the delay between two samples is controlled by this count (N+1) combined with the delay selection in the two bits above.
15-10	R/W	14	CNTL_EOC_DLY_CNT: the delay between SC and ADC output data ready for latch/sample
9-8	R/W	0	SAMPLE_DLY_SEL: 0 = count 1uS ticks, 1 = count 10uS ticks, 2 = count 100uS ticks. 3 = count 1mS ticks
7-0	R/W	9	SAMPLE_DLY_CNY: For channels that acquire 2,4 or 8 samples, the delay between two samples is controlled by this count (N+1) combined with the delay selection in the two bits above.

For channel 0 and channel 1, (the special X/Y channels) the last sample pushed into the FIFO for each channel is saved in a register. This allows the software to see the last sample for channel 0 and channel 1 even when the FIFO overflows. For example, if we are sampling quickly and there is a gesture on the screen, we can use the contents of the FIFO to see the direction of the gesture and use the last sample values to see where the pen finally came to rest.

Table 13-139 SAR_ADC_LAST_RD: Last Sample

Bit(s)	R/W	Default	Description
31-28	R	0	unused
27-16	R	0	LAST_CHANNEL1
15-12	R	0	unused
11-0	R	0	LAST_CHANNEL0

Table 13-140 SAR_ADC_FIFO_RD: Control Register #6 (FIFO RD)

Bit(s)	R/W	Default	Description
31-28	R	0	Unused
27-16	R	0	RAW data
15	R	0	Unused
14-12	R	0	Channel ID. This value identifies the channel associated with the data in Bits [11:0] below
11-0	R	0	Sample value: 12-bit raw or averaged ADC sample written to the FIFO.

Channels 2 ~ 7 can program the ADC input mux to any selection between 0 and 7. This register allows the software to associate a mux selection with a particular channel. In addition to the ADC mux, there are a number of switches that can be set in any particular state. Channels 2 ~ 7 share a common switch setting. Channels 0 and 1 on the other hand have programmable switch settings (see other registers below).

Table 13-141 SAR_ADC_AUX_SW:Channel 2~7 ADC MUX, Switch Controls

Bit(s)	R/W	Default	Description
31	R	0	EOC
29	R/W	0	CNTL_MANUAL_SC
28	R/W	0	CNTL_MANUAL_CLK

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Bit(s)	R/W	Default	Description
27	R/W	0	CNTL_MANUAL_MODE
26	R	0	unused
25-23	R/W	7	Channel 7 ADC_MUX setting when channel 7 is being measured.
22-20	R/W	7	Channel 6 ADC_MUX setting when channel 6 is being measured.
19-17	R/W	7	Channel 5 ADC_MUX setting when channel 5 is being measured.
16-14	R/W	6	Channel 4 ADC_MUX setting when channel 4 is being measured.
13-11	R/W	0	Channel 3 ADC_MUX setting when channel 3 is being measured.
10-8	R/W	1	Channel 2 ADC_MUX setting when channel 2 is being measured.
7	R	0	unused
6	R/W	0	VREF_P_MUX setting when channel 2,3..7 is being measured
5	R/W	0	VREF_N_MUX setting when channel 2,3..7 is being measured
4	R/W	0	MODE_SEL setting when channel 2,3..7 is being measured
3	R/W	1	YP_DRIVE_SW setting when channel 2,3..7 is being measured
2	R/W	1	XP_DRIVE_SW setting when channel 2,3..7 is being measured
1	R/W	0	YM_DRIVE_SW setting when channel 2,3..7 is being measured
0	R/W	0	YM_DRIVE_SW setting when channel 2,3..7 is being measured

Channels 0 and 1 have independent programmable switch settings when either/both of these channels are being measured.

Table 13-142 SAR_ADC_CHAN_10_SW:Channel 0, 1 ADC MUX, Switch Controls

Bit(s)	R/W	Default	Description
31-26	R	0	unused
25-23	R/W	2	Channel 1 ADC MUX setting
22	R/W	0	Channel 1 VREF_P_MUX
21	R/W	0	Channel 1 VREF_N_MUX
20	R/W	0	Channel 1 MODE_SEL
19	R/W	1	Channel 1 YP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating
18	R/W	1	Channel 1 XP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating
17	R/W	0	Channel 1 YM_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND
16	R/W	0	Channel 1 YM_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND
15-10	R		unused
9-7	R/W	3	Channel 0 ADC MUX setting

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Bit(s)	R/W	Default	Description
6	R/W	0	Channel 0 VREF_P_MUX
5	R/W	0	Channel 0 VREF_N_MUX
4	R/W	0	Channel 0 MODE_SEL
3	R/W	1	Channel 0 YP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating
2	R/W	1	Channel 0 XP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating
1	R/W	0	Channel 0 YM_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND
0	R/W	0	Channel 0 YM_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND

IDLE MODE: When nothing is being measured, the switches should be put into a safe state. This safe state is accomplished using Bits [9:0] below.

DETECT MODE: When bit [26] is set, the input muxes / switches are configured according to the Bits below. Typically the software configures the switches below to correspond to the detect touch mode. That is, Y- internal MOSFET is closed so that the Y plane of the touch screen is connected to Ground. Additionally, the DETECT_EN bit (different register) set to 1 so that the 50k resistor to VDD is connected to X+. In this configuration, the detect comparator connected to the 50k resistor will be weakly pulled up to VDD through the 50k resistor. If the user touches the screen, the X and Y planes of the touch screen will contact causing the X+ signal to be pulled to ground.

Table 13-143 SAR_ADC_DETECT_IDLE_SW:DETECT / IDLE Mode switches

Bit(s)	R/W	Default	Description
31-27	R	0	unused
26	R/W	0	DETECT_SW_EN: If This bit is set, then Bits [25:16] below are applied to the analog muxes/switches of the touch panel controller.
25-23	R/W	5	DETECT MODE ADC MUX setting
22	R/W	0	DETECT MODE VREF_P_MUX setting
21	R/W	0	DETECT MODE VREF_N_MUX setting
20	R/W	0	DETECT MODE MODE_SEL setting
19	R/W	1	DETECT MODE YP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating
18	R/W	1	DETECT MODE XP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating
17	R/W	0	DETECT MODE YM_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND
16	R/W	0	DETECT MODE YM_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND

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Bit(s)	R/W	Default	Description
15-10	R		Unused
9-7	R/W	5	IDLE MODE ADC MUX setting
6	R/W	0	IDLE MODE VREF_P_MUX setting
5	R/W	0	IDLE MODE VREF_N_MUX setting
4	R/W	0	IDLE MODE MODE_SEL setting
3	R/W	1	IDLE MODE YP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating
2	R/W	1	IDLE MODE XP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating
1	R/W	0	IDLE MODE YN_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND
0	R/W	0	IDLE MODE XN_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND

Table 13-144 SAR_ADC_DELTA_10:Delta Mode Deltas

Bit(s)	R/W	Default	Description
31-28	R	0	unused
27-16	R/W	0	Channel 1 delta value when delta processing for channel 1 is enabled.
15-12	R/W		unused
11-0	R/W	0	Channel 0 delta value when delta processing for channel 0 is enabled.

Table 13-145 SAR_ADC_REG11

Bit(s)	R/W	Default	Description
31	R/W	0	fifo_disable: 1=dout don`t put into fifo
30	R/W	0	period_sample_en: 1=period_sample enable, dout register into chnl reg AO_ SAR_ADC_CHNL01/23/45/67
29-13	R/W	0	ts_cntl_int
12-0	R/W	0	sar_bg_cntl

Table 13-146 SAR_ADC_REG12

Bit(s)	R/W	Default	Description
31-0	R/W	0	reserved

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Table 13-147 SAR_ADC_REG13

Bit(s)	R/W	Default	Description
31-8	R	0	unused
15-8	R/W	0	SARADC_RSV2
7-0	R/W	0	reserved

Table 13-148 SAR_ADC_CHNL01

Bit(s)	R/W	Default	Description
31	R/W	0	dout_chnl1_valid
30-28	R/W	0	dout_chnl1_id
27-16	R/W	0	dout_chnl1
15	R/W	0	dout_chnl0_valid
14-12	R/W	0	dout_chnl0_id
11-0	R/W	0	dout_chnl0

Table 13-149 SAR_ADC_CHNL23

Bit(s)	R/W	Default	Description
31	R/W	0	dout_chnl3_valid
30-28	R/W	0	dout_chnl3_id
27-16	R/W	0	dout_chnl3
15	R/W	0	dout_chnl2_valid
14-12	R/W	0	dout_chnl2_id
11-0	R/W	0	dout_chnl2

Table 13-150 SAR_ADC_CHNL45

Bit(s)	R/W	Default	Description
31	R/W	0	dout_chnl5_valid
30-28	R/W	0	dout_chnl5_id
27-16	R/W	0	dout_chnl5
15	R/W	0	dout_chnl4_valid
14-12	R/W	0	dout_chnl4_id
11-0	R/W	0	dout_chnl4

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Table 13-151 SAR_ADC_CHNL67

Bit(s)	R/W	Default	Description
31	R/W	0	dout_chnl7_valid
30-28	R/W	0	dout_chnl7_id
27-16	R/W	0	dout_chnl7
15	R/W	0	dout_chnl6_valid
14-12	R/W	0	dout_chnl6_id
11-0	R/W	0	dout_chnl6

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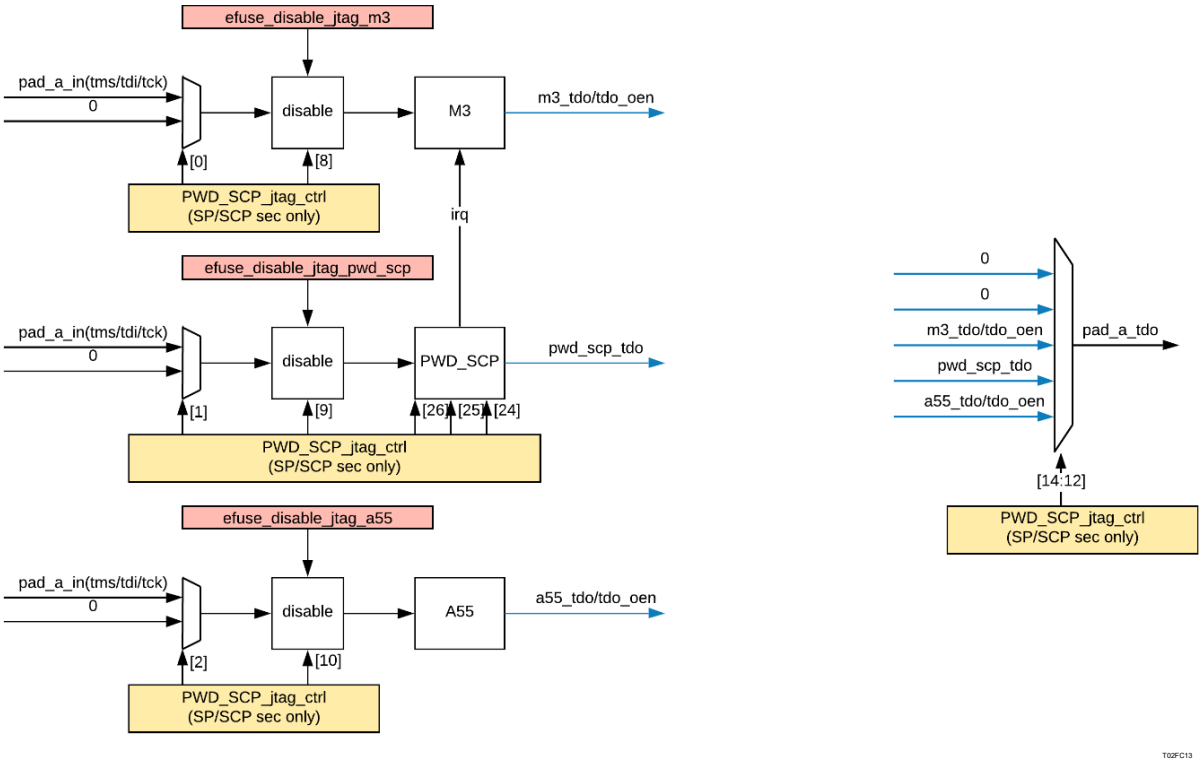
14 System Interface

14.1 JTAG

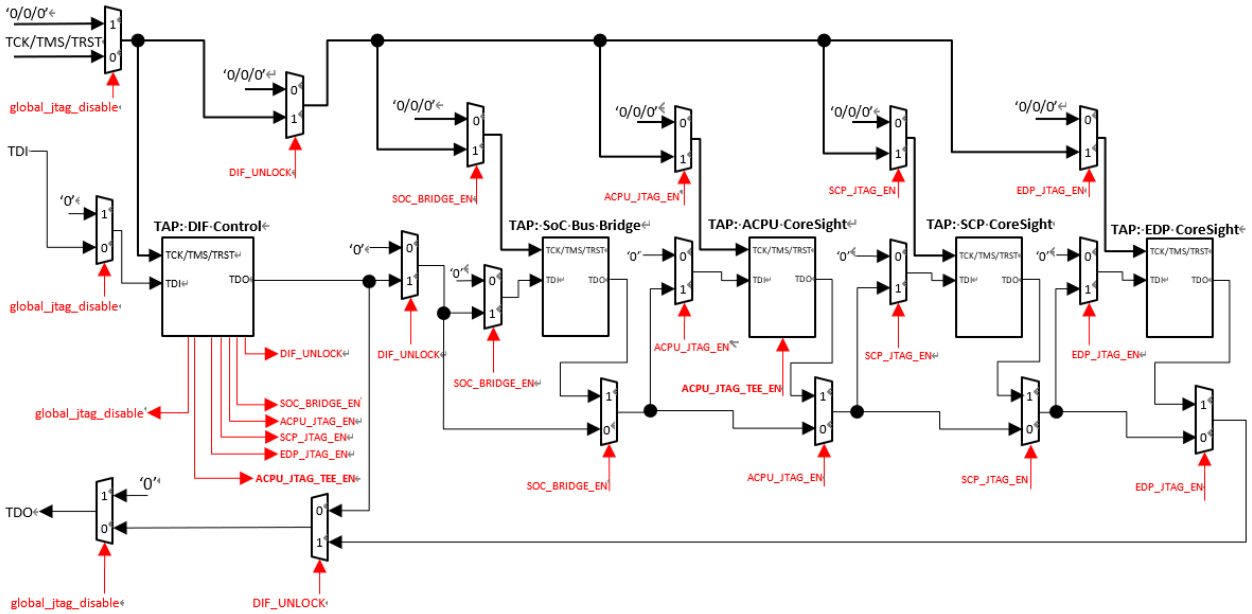
14.1.1 Overview

JTAG is an interface for internal test. The structure of SoC JTAG module is shown in the following diagram.

Figure 14-1 JTAG Structure



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14.1.2 Register Description

Base address: 0xFF800000

Register address: 0xFF800000 + offset * 4

Table 14-1 AO_SEC_JTAG_SP_CNTL 0xAC

Bit(s)	R/W	Default	Description
31	R	0	jrag_pwd_sp_data_valid; 1: finished write jtag_pwd_addr3;
30	R	0	jrag_pwd_sp_data_timeout; 1: jtag_pwd_sp_wd count greater threshold (time out);
26	R/W	0	jtag_pwd_sp_clr; 1: clear valid and irq status;
25	R/W	0	jtag_pwd_sp_wd_resetn; 0: reset pwd_sp_wd, then no irq;
24	R/W	0	jtag_pwd_sp_en; 0: disable jtag_pwd_sp in/out; 1: enable jtag_pwd_sp in/out;
9	R/W	0	jtag_disable_pwd_sp_in; 0: enable; 1: disable pwd_sp_jtag_in;
8	R/W	0	jtag_disable_m4_in; 0: enable; 1: disable m4_jtag_in;
4	R/W	0	jtag_sel_force_m4_tdo_en_low; 0: tdo_en = m4_jtag_tdo_en; 1: tdo_en = 1'b0 (always output);

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Bit(s)	R/W	Default	Description
1	R/W	0	jtag_sel_pwd_sp_in; 0: pad_a; 1: pad_b;
0	R/W	0	jtag_sel_m4_in; 0: pad_a; 1: pad_b;

Table 14-2 AO_SEC_JTAG_PWD_SP_0 0xAD

Bit(s)	R/W	Default	Description
31-0	R	0	jtag_pwd_sp received pwd[31:0]

Table 14-3 AO_SEC_JTAG_PWD_SP_1 0xAE

Bit(s)	R/W	Default	Description
31-0	R	0	jtag_pwd_sp received pwd[63:32]

Table 14-4 AO_SEC_JTAG_PWD_SP_2 0xAF

Bit(s)	R/W	Default	Description
31-0	R	0	jtag_pwd_sp received pwd[95:64]

Table 14-5 AO_SEC_JTAG_PWD_SP_3 0xB0

Bit(s)	R/W	Default	Description
31-0	R	0	jtag_pwd_sp received pwd[127:96]

Table 14-6 AO_SEC_JTAG_PWD_SP_CNTL 0xB1

Bit(s)	R/W	Default	Description
31:5	R/W	0	timeout threshold;
4	R/W	0	activity by tdo_en; 1: detect tdo activity and use it reset watchdog count;
3	R/W	0	activity by tck_en; 1: detect tck activity and use it reset watchdog count;
2	R/W	0	activity by tms_en; 1: detect tms activity and use it reset watchdog count;
1	R/W	0	activity by tdi_en; 1: detect tdi activity and use it reset watchdog count;
0	R/W	0	wd_timeout_en; 0: disable watchdog timeout; 1: enable watchdog timeout;

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Table 14-7 AO_SEC_JTAG_PWD_SP_ADDR0 0xB2

Bit(s)	R/W	Default	Description
31-0	R/W	0	addr0

Table 14-8 AO_SEC_JTAG_PWD_SP_ADDR1 0xB3

Bit(s)	R/W	Default	Description
31-0	R/W	0	addr1

Table 14-9 AO_SEC_JTAG_PWD_SP_ADDR2 0xB4

Bit(s)	R/W	Default	Description
31-0	R/W	0	addr2

Table 14-10 AO_SEC_JTAG_PWD_SP_ADDR3 0xB5

Bit(s)	R/W	Default	Description
31-0	R/W	0	addr3

Table 14-11 AO_SEC_JTAG_SCP_CNTL 0xB6

Bit(s)	R/W	Default	Description
31	R	0	jrag_pwd_scp_data_valid; 1: finished write jtag_pwd_addr3;
30	R	0	jrag_pwd_scp_data_timeout; 1: jtag_pwd_sp_wd count greater threshold (time out);
26	R/W	0	jtag_pwd_scp_clr; 1: clear valid and irq status;
25	R/W	0	jtag_pwd_scp_wd_resetn; 0: reset pwd_scp_wd, then no irq;
24	R/W	0	jtag_pwd_scp_en; 0: disable jtag_pwd_scp in/out; 1: enable jtag_pwd_scp in/out;
18:16	R/W	0	jtag_pad_b_out sel: 0: none; 1:m4; 2:jtag_pwd_sp; 3:m3; 4:jtag_pwd_scp; 5:A55
14:12	R/W	0	jtag_pad_a_out_sel: 0: none; 1:m4; 2:jtag_pwd_sp; 3:m3; 4:jtag_pwd_scp; 5:A55
10	R/W	0	jtag_disable_A55_in; 0: enable; 1: disable A55_jtag_in;

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Bit(s)	R/W	Default	Description
9	R/W	0	jtag_disable_pwd_scp_in; 0: enable; 1: disable pwd_scp_jtag_in;
8	R/W	0	jtag_disable_m3_in; 0: enable; 1: disable m3_jtag_in;
5	R/W	0	jtag_sel_force_A55_tdo_en_low; 0: tdo_en = A55_jtag_tdo_en; 1: tdo_en = 1'b0 (always output);
4	R/W	0	jtag_sel_force_m3_tdo_en_low; 0: tdo_en = m3_jtag_tdo_en; 1: tdo_en = 1'b0 (always output);
2	R/W	0	jtag_sel_A55_in; 0: pad_a; 1: pad_b;
1	R/W	0	jtag_sel_pwd_scp_in; 0: pad_a; 1: pad_b;
0	R/W	0	jtag_sel_m3_in; 0: pad_a; 1: pad_b;

Table 14-12 AO_SEC_JTAG_PWD_SCP_0 0xB7

Bit(s)	R/W	Default	Description
31-0	R	0	jtag_pwd_scp received pwd[31:0]

Table 14-13 AO_SEC_JTAG_PWD_SCP_1 0xB8

Bit(s)	R/W	Default	Description
31-0	R	0	jtag_pwd_scp received pwd[63:32]

Table 14-14 AO_SEC_JTAG_PWD_SCP_2 0xB9

Bit(s)	R/W	Default	Description
31-0	R	0	jtag_pwd_scp received pwd[95:64]

Table 14-15 AO_SEC_JTAG_PWD_SCP_3 0xBA

Bit(s)	R/W	Default	Description
31-0	R	0	jtag_pwd_scp received pwd[127:96]

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Table 14-16 AO_SEC_JTAG_PWD_SCP_CNTL 0xBB

Bit(s)	R/W	Default	Description
31:5	R/W	0	timeout threshold;
4	R/W	0	activity by tdo_en; 1: detect tdo activity and use it reset watchdog count;
3	R/W	0	activity by tck_en; 1: detect tck activity and use it reset watchdog count;
2	R/W	0	activity by tms_en; 1: detect tms activity and use it reset watchdog count;
1	R/W	0	activity by tdi_en; 1: detect tdi activity and use it reset watchdog count;
0	R/W	0	wd_timeout_en; 0: disable watchdog timeout; 1: enable watchdog timeout;

Table 14-17 AO_SEC_JTAG_PWD_SCP_ADDR0 0xBC

Bit(s)	R/W	Default	Description
31-0	R/W	0	addr0

Table 14-18 AO_SEC_JTAG_PWD_SCP_ADDR1 0xBD

Bit(s)	R/W	Default	Description
31-0	R/W	0	addr1

Table 14-19 AO_SEC_JTAG_PWD_SCP_ADDR2 0xBE

Bit(s)	R/W	Default	Description
31-0	R/W	0	addr2

Table 14-20 AO_SEC_JTAG_PWD_SCP_ADDR3 0xBF

Bit(s)	R/W	Default	Description
31-0	R/W	0	addr3

14.2 Temp Sensor

14.2.1 Overview

The SoC integrates 2 Temp Sensor, one is close to DDR, one is close to PLL (between CPU and GPU).

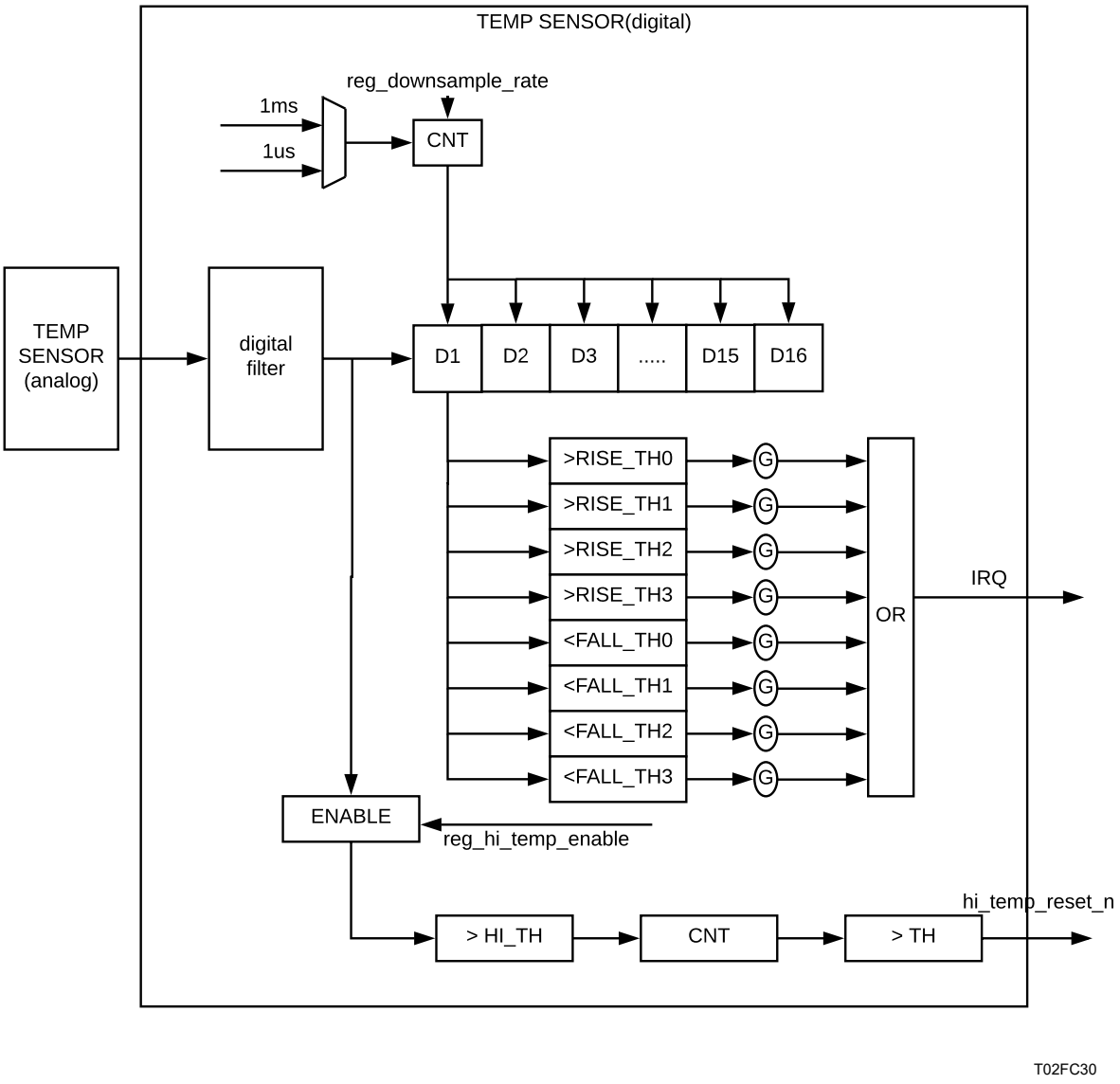
Each Temp Sensor are the same design.

- Capture temperature by programable tick;
- Store 16 temperature value;
- Can reset all chip if detect high temperature;

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- Can generate IRQ by 8 threshold;

Figure 14-2 Temp Sensor



14.2.2 Register Description

Temp Sensor PLL Registers

Base Address: FE020000

Each register final address = module base address+ address * 4

Temp Sensor DDR Registers

Base Address: FE022000

Each register final address = module base address+ address * 4

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Table 14-21 TS_CFG_REG1 0x001

Bits	R/W	Default	Description
31	R/W	0	fall_th3_irq_en
30	R/W	0	fall_th2_irq_en
29	R/W	0	fall_th1_irq_en
28	R/W	0	fall_th0_irq_en
27	R/W	0	rise_th3_irq_en
26	R/W	0	rise_th2_irq_en
25	R/W	0	rise_th1_irq_en
24	R/W	0	rise_th0_irq_en
23	R/W	0	fall_th3_irq_stat_clr
22	R/W	0	fall_th2_irq_stat_clr
21	R/W	0	fall_th1_irq_stat_clr
20	R/W	0	fall_th0_irq_stat_clr
19	R/W	0	rise_th3_irq_stat_clr
18	R/W	0	rise_th2_irq_stat_clr
17	R/W	0	rise_th1_irq_stat_clr
16	R/W	0	rise_th0_irq_stat_clr
15	R/W	0	1: enable IRQ related function.
14	R/W	0	fast_mode: 0 : downsample unit = 1ms; 1: downsample unit = 1us;
13	R/W	0	clr_hi_temp_stat
12	R/W	0	ts_ana_rset_vbg reset vbg(set 0, if have error place set it plus 01000..)
11	R/W	0	ts_ana_rst_sd reset adc(set 0, if have error place set it plus 01000..)
10	R/W	0	ts_ana_en_vcm enable vcm (disable:0; enable:1)
9	R/W	0	ts_ana_en_vbg enable vbg (disable:0; enable: 1)
8:7	R/W	0	filter hcic mode 0: downsample rate = 128; 1: downsample rate = 256; 2/3: downsample rate = 512;
6	R/W	0	filter ts_out_ctrl; 1: add more delay for filter lock;
5	R/W	0	filter en(disable:0; enable:1)
4	R/W	0	ts_ana_en_iptat, useless.

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Bits	R/W	Default	Description
3	R/W	0	Temp Sensor DEM enable. (disable:0; enable:1)
2:0	R/W	0	Bipolar bias current input control. recommend value : 3. ts_ana_ch_sel; 0: 8'b00000001; 1: 8'b00000011; 2: 8'b00000111; 3: 8'b00001111; 4: 8'b00011111; 5: 8'b00111111; 6: 8'b01111111; 7: 8'b11111111;

Table 14-22 TS_CFG_REG2 0x002

Bits	R/W	Default	Description
31	R/W	0	hi_temp_enable
30	R/W	0	reset_en, if = 0, will not reset all chip;
27:16	R/W	0	high temperature times, if continuous detect high temperature, then will reset all chip.
15:0	R/W	0	high temperature threshold, if temperature value > this th , mean detected once high temperature

Table 14-23 TS_CFG_REG3 0x03

Bits	R/W	Default	Description
31:16	R/W	0	
15:0	R/W	0	down_sample rate

Table 14-24 TS_CFG_REG4 0x04

Bits	R/W	Default	Description
23:12	R/W	0	rise_th0
11:0	R/W	0	rise_th1

Table 14-25 TS_CFG_REG5 0x05

Bits	R/W	Default	Description
23:12	R/W	0	rise_th2
11:0	R/W	0	rise_th3

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Table 14-26 TS_CFG_REG6 0x06

Bits	R/W	Default	Description
23:12	R/W	0	fall_th0
11:0	R/W	0	fall_th1

Table 14-27 TS_CFG_REG7 0x07

Bits	R/W	Default	Description
23:12	R/W	0	fall_th2
11:0	R/W	0	fall_th3

Table 14-28 TS_STAT0 0x10

Bits	R/W	Default	Description
31:18	R	0	detect_hi_temp_cnt
17	R	0	detected_hi_temp_stat
16	R	0	filter lock
15:0	R	0	filter out

Table 14-29 TS_STAT1 0x11

Bits	R/W	Default	Description
31:9	R	0	
8	R	0	hi_temp_stat
7	R	0	fall_th3_irq
6	R	0	fall_th2_irq
5	R	0	fall_th1_irq
4	R	0	fall_th0_irq
3	R	0	rise_th3_irq
2	R	0	rise_th2_irq
1	R	0	rise_th1_irq
0	R	0	rise_th0_irq

Table 14-30 TS_STAT2 0x12

Bits	R/W	Default	Description
31:16	R	0	temperature value D2
15:0	R	0	temperature value D1

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Table 14-31 TS_STAT3 0x13

Bits	R/W	Default	Description
31:16	R	0	temperature value D4
15:0	R	0	temperature value D3

Table 14-32 TS_STAT4 0x14

Bits	R/W	Default	Description
31:16	R	0	temperature value D6
15:0	R	0	temperature value D5

Table 14-33 TS_STAT5 0x15

Bits	R/W	Default	Description
31:16	R	0	temperature value D8
15:0	R	0	temperature value D7

Table 14-34 TS_STAT6 0x16

Bits	R/W	Default	Description
31:16	R	0	temperature value D10
15:0	R	0	temperature value D9

Table 14-35 TS_STAT7 0x17

Bits	R/W	Default	Description
31:16	R	0	temperature value D12
15:0	R	0	temperature value D11

Table 14-36 TS_STAT8 0x18

Bits	R/W	Default	Description
31:16	R	0	temperature value D14
15:0	R	0	temperature value D13

Table 14-37 TS_STAT9 0x19

Bits	R/W	Default	Description
31:16	R	0	temperature value D16
15:0	R	0	temperature value D15

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14.3 Appendix

14.3.1 Net Length

The following table describes the length of all nets on the SoC.

Table 14-38 Net Length

Signal Group	Net Name	Net Length(um)
AC	G0_AC0	4995.9532
	G0_AC1	6209.0714
	G0_AC2	8078.7084
	G0_AC3	8525.3769
	G0_AC4	8194.0647
	G0_AC5	8277.7676
	G0_AC6	5931.6871
	G0_AC7	6196.0923
	G1_AC0	6576.5281
	G1_AC1	5923.0226
	G1_AC2	6815.9275
	G1_AC3	5310.6382
	G1_AC4	4569.8335
	G1_AC5	5195.3102
	G1_AC6	4163.5963
	G1_AC7	7624.8996
	G1_AC8	5140.6955
	G1_AC9	5791.225
	G1_AC10	7473.9172
	G1_AC11	6780.1683
	G1_AC12	4957.405
	G1_AC13	7397.6613
	G1_AC14	5446.5526
	G1_AC15	5609.057
	G1_AC20	6254.1093
	G1_AC21	6210.2522
	G1_AC22	7347.3069
	G1_AC25	5051.5359
	G1_AC26	5266.4259
	G1_AC27	6553.2097

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Signal Group	Net Name	Net Length(um)
DDR Reset	DDR_RSTN	4631.5251
DDR lane 0	DDR_DQSN0	6617.1827
	DDR_DQSP0	6363.412
	DDR_DQM0	6273.4558
	DDR_DQ0	4392.8175
	DDR_DQ1	4976.0208
	DDR_DQ2	4806.5967
	DDR_DQ3	4907.0313
	DDR_DQ4	5662.6987
	DDR_DQ5	5887.6129
	DDR_DQ6	4854.7666
	DDR_DQ7	4313.0094
DDR lane 1	DDR_DQSN1	5753.0475
	DDR_DQSP1	5863.1398
	DDR_DQM1	4272.6971
	DDR_DQ8	7450.4514
	DDR_DQ9	7349.7742
	DDR_DQ10	7198.4092
	DDR_DQ11	5516.4657
	DDR_DQ12	4460.0285
	DDR_DQ13	5896.5808
	DDR_DQ14	5393.091
	DDR_DQ15	8219.9469
DDR lane 2	DDR_DQSN2	4988.8207
	DDR_DQSP2	5482.2507
	DDR_DQM2	5979.1351
	DDR_DQ16	4513.6578
	DDR_DQ17	5276.1367
	DDR_DQ18	5709.4256
	DDR_DQ19	4979.743
	DDR_DQ20	6955.2521
	DDR_DQ21	5797.6823
	DDR_DQ22	5695.1432
	DDR_DQ23	4360.2619
DDR lane 2	DDR_DQSN3	5667.7516

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Signal Group	Net Name	Net Length(um)
	DDR_DQSP3	6231.2075
	DDR_DQM3	6061.4321
	DDR_DQ24	4745.7244
	DDR_DQ25	4966.4934
	DDR_DQ26	4670.609
	DDR_DQ27	3610.3078
	DDR_DQ28	6532.384
	DDR_DQ29	5090.4958
	DDR_DQ30	4520.9821
	DDR_DQ31	4612.1269
Ethernet	ETH_RXN	3214.0684
	ETH_RXP	3517.7377
	ETH_TXN	2943.6746
	ETH_TXP	2893.254
HDMI	HDMITX_CKN	5906.6855
	HDMITX_CKP	6196.3401
	HDMITX_0N	6038.2514
	HDMITX_0P	6017.3422
	HDMITX_1N	4808.1346
	HDMITX_1P	5073.3619
	HDMITX_2N	5071.2759
	HDMITX_2P	5373.8334
USB	USBHOST_A_DM	5559.8027
	USBHOST_A_DP	5383.6651
	USBOTG_B_DM	5171.3445
	USBOTG_B_DP	5093.3638

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