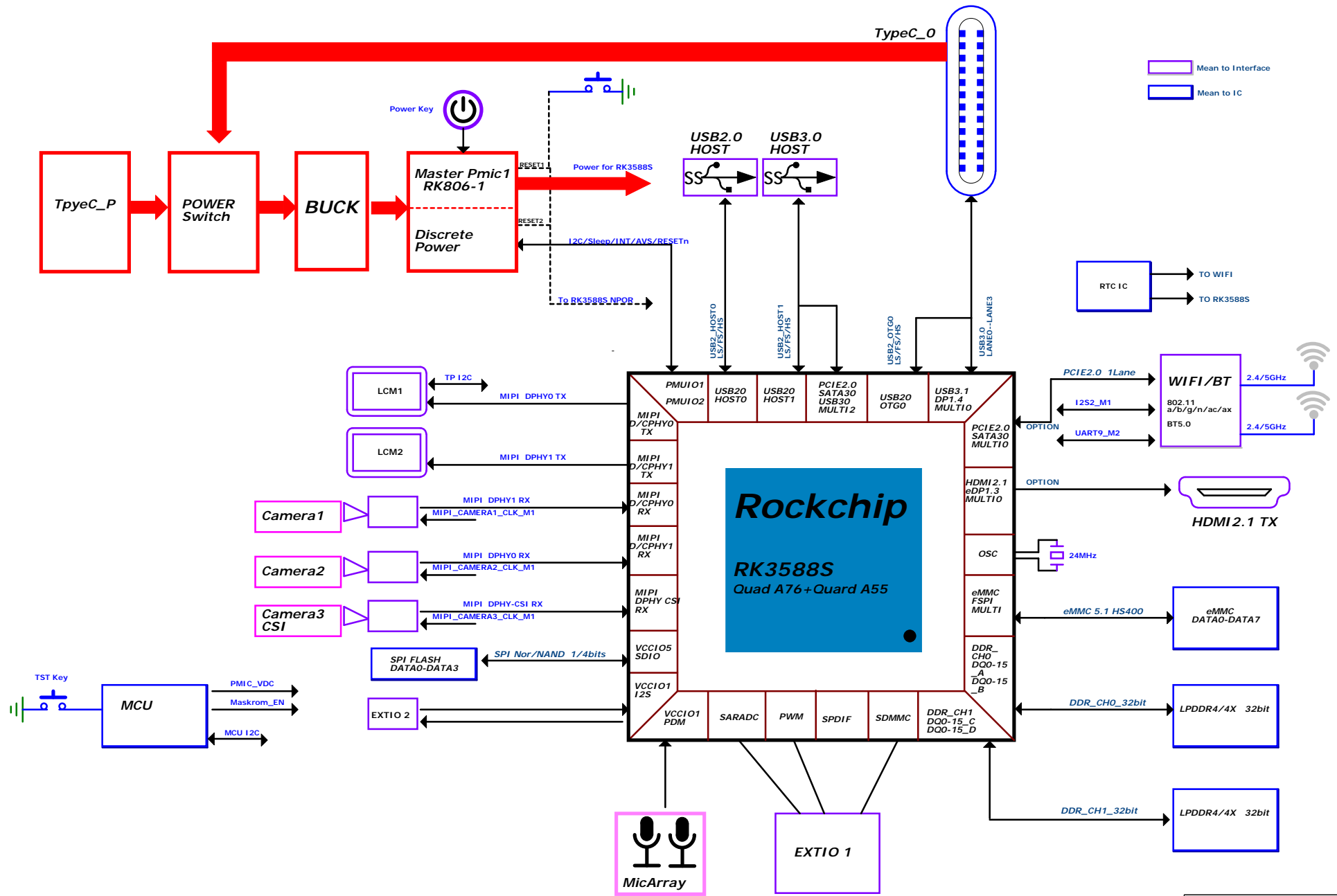




KHADASS

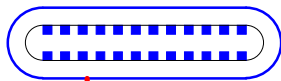
Something a little different.

Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	Khadass		
Date:	Thursday, November 17, 2022	Rev:	V12
Designed_by:	Totti	Sheet:	1



Mean to Interface
 Mean to IC

Shenzhen Wision Technology Co., Ltd.			
Project:	Edge2	Rev:	V12
File:	BLOCK	Draw:	2
Date:	Thursday, November 17, 2023	Draw:	
Design:by:	Tian	Draw:	



Power Switch
TypeC_P
16pin

BUCK
8000mA

BUCK
Seq:6
VCC_5V0

LDO
Seq:always ON
VCCA

VCC5V0_USB20_HOST
VCC5V0_USB30_HOST
VCC5V0_HDMI_TX0
VCC5V0_FAN

VCCA -> MCU_VCC -> RTC

VCC_SYSIN
Seq:0

RK806-1

VCC	Regulator	Current	Seq
VCC1	BUCK1	6.5A max	Seq:5
VCC2	BUCK2	5.0A max	Seq:3
VCC3	BUCK3	5.0A max	Seq:2
VCC4	BUCK4	5.0A max	Seq:5
VCC5	BUCK5	2.5A max	Seq:2
VCC6	BUCK6	2.5A max	Seq:4
VCC7	BUCK7	2.5A max	Seq:1
VCC8	BUCK8	2.5A max	Seq:6
VCC9	BUCK9	2.5A max	Seq:6
VCC10	BUCK10	2.5A max	Seq:3
VCC11	PLDO1	500mA max	Seq:3
VCC12	PLDO2	300mA max	Seq:3
VCC13	PLDO3	300mA max	Seq:4
VCC14	PLDO4	500mA max	Seq:6
VCC15	PLDO5	300mA max	Seq:6
VCCA	PLDO6	300mA max	Seq:3
VCC13	NLDO1	300mA max	Seq:2
VCC13	NLDO2	300mA max	Seq:2
VCC13	NLDO3	500mA max	Seq:2
VCC13	NLDO4	500mA max	Seq:2
VCC13	NLDO5	300mA max	Seq:2

VDD_GPU_S0 -> VDD_GPU / VDD_GPU_MEM
Max:6200mA

VDD_CPU_LIT_S0 -> VDD_CPU_LIT / VDD_CPU_LIT_MEM
Max:2800mA

VDD_LOGIC_S0 -> VDD_LOGIC
Max:1750mA

VDD_VDENC_S0 -> VDD_VDENC / VDD_VDENC_MEM
Max:1800mA

VDD_DDR_S0 -> VDD_DDR_S0

VDD2_DDR_S3 -> LPDDR4 VDDQ, LPDDR4/4x VDD2, DDR_CH0/1_VDDQ_CKE

VCC_2V0_PLDO_S3 -> VCC_2V0_PLDO_S3

VCC_3V3_S3 -> VCC_3V3_S3

VDDQ_DDR_S0 -> VDDQ_DDR_S0

VCC_1V8_S3 -> VCC_1V8_S3

VCC_1V8_S0 -> VCC_1V8_S0

VCCA_1V2_S0 -> MIPI_D/C_PHY0_VDD_1V2, MIPI_D/C_PHY1_VDD_1V2

VCCA_3V3_S0 -> VCCA_3V3_S0

VCCIO_SD_S0 -> VCCIO2

VCCA1V8_PLDO6 -> VCCA1V8_PLDO6

VDD_0V75_S3 -> VDD_0V75_S3

VDDA_DDR_PLL_S0 -> DDR_CH0_PLL_DVDD, DDR_CH1_PLL_DVDD

VDDA_0V75_S0 -> VDDA_0V75_S0

VDDA_0V85_S0 -> VDDA_0V85_S0

VDD_0V75_S0 -> VDD_0V75_S0

VDD_CPU_BIG0_S0 -> VDDCPU_BIG0 / VDDCPU_BIG0_MEM
Max:3500mA

VDD_CPU_BIG1_S0 -> VDDCPU_BIG1 / VDDCPU_BIG1_MEM
Max:3500mA

VDD_NPU_S0 -> VDD_NPU / VDD_NPU_MEM
Max:4000mA

VCC_1V1_NLDO_S3 -> VCC_1V1_NLDO_S3

EXT DC/DC_2A -> VCC_1V1_NLDO_S3

MCU_VCC -> RTC

VDD_GPU / VDD_GPU_MEM

VDD_CPU_LIT / VDD_CPU_LIT_MEM

VDD_LOGIC

VDD_VDENC / VDD_VDENC_MEM

VDD_DDR_S0

LPDDR4 VDDQ, LPDDR4/4x VDD2, DDR_CH0/1_VDDQ_CKE

VCC_2V0_PLDO_S3

VCC_3V3_S3

VDDQ_DDR_S0

VCC_1V8_S3

VCC_1V8_S0

MIPI_D/C_PHY0_VDD_1V2, MIPI_D/C_PHY1_VDD_1V2

VCCA_3V3_S0

VCCIO2

VCCA1V8_PLDO6

VDD_0V75_S3

DDR_CH0_PLL_DVDD, DDR_CH1_PLL_DVDD

VDDA_0V75_S0

VDDA_0V85_S0

VDD_0V75_S0

VDDCPU_BIG0 / VDDCPU_BIG0_MEM

VDDCPU_BIG1 / VDDCPU_BIG1_MEM

VDD_NPU / VDD_NPU_MEM

VCC_1V1_NLDO_S3

VCC_1V1_NLDO_S3

DDR_CH0_VDD, DDR_CH0_VDD_MIF, DDR_CH1_VDD, DDR_CH1_VDD_MIF

LPDDR4x, DDR_CH1_VDDQ_CK, DDR_CH1_VDDQ, DDR_CH0_VDDQ

MIPI_D/C_PHY0_VDD_1V2, MIPI_D/C_PHY1_VDD_1V2

CODEC_VCCA3V3, USB20_AVDD_3V3, LCD

DDR_CH0_PLL_DVDD, DDR_CH1_PLL_DVDD

VDDCPU_BIG0 / VDDCPU_BIG0_MEM

VDD_NPU / VDD_NPU_MEM

Load Switch, PMUIO2, Typec CC IC, WIFI BATT, Camera Input, TP, EXTIO 1, EXTIO 2

LPDDR4x, DDR_CH1_VDDQ_CK, DDR_CH1_VDDQ, DDR_CH0_VDDQ

OSC_1V8, PLL_AVDD1V8, MIPI_CSIO_AVCC1V8, SARADC_AVDD_1V8, DDR_CH0_PLL_AVDD1V8, DDR_CH1_PLL_AVDD1V8, TYPECO_DPO_VDDH_1V8, HDMI/EDP_TX0_VDD_IO_1V8, HDMI/EDP_TX0_VDD_CMN_1V8, PCIE20_SATA30_0_AVDD_1V8, PCIE20_SATA30_USB30_2_AVDD_1V8, MIPI_D/C_PHY0&1_VDD_1V8, AVCC_1V8_CODECC

TYPECO_DPO_VDD_0V85, TYPECO_DPO_VDDA_0V85, PCIE20_SATA30_0_AVDD_0V85, PCIE20_SATA30_USB30_2_AVDD_0V85

VDDCPU_BIG0 / VDDCPU_BIG0_MEM

VDD_NPU / VDD_NPU_MEM

VCC_3V3_S0 -> VCCIO6, eMMC VCC, EXTIO

VDD1_1V8_DDR, WIFI VDDIO, EMMCIO_1V8, eMMC VCCQ, PMUIO1_1V8, PMUIO2_1V8

VCCIO4_1V8, VCCIO5_1V8, VCCIO6_1V8, VCCIO4, VCCIO5, TP IO, DMIC, Sensor, LCD IO, USB20_AVDD_1V8

HDMI/EDP_TX0_VDD_0V75, HDMI/EDP_TX0_AVDD_0V75, MIPI_D/C_PHY0_VDD, MIPI_D/C_PHY1_VDD, MIPI_CSIO_AVCC0V75, OTP_VDDOTR_0V75, PLL_DVDD0V75, USB20_DVDD_0V75

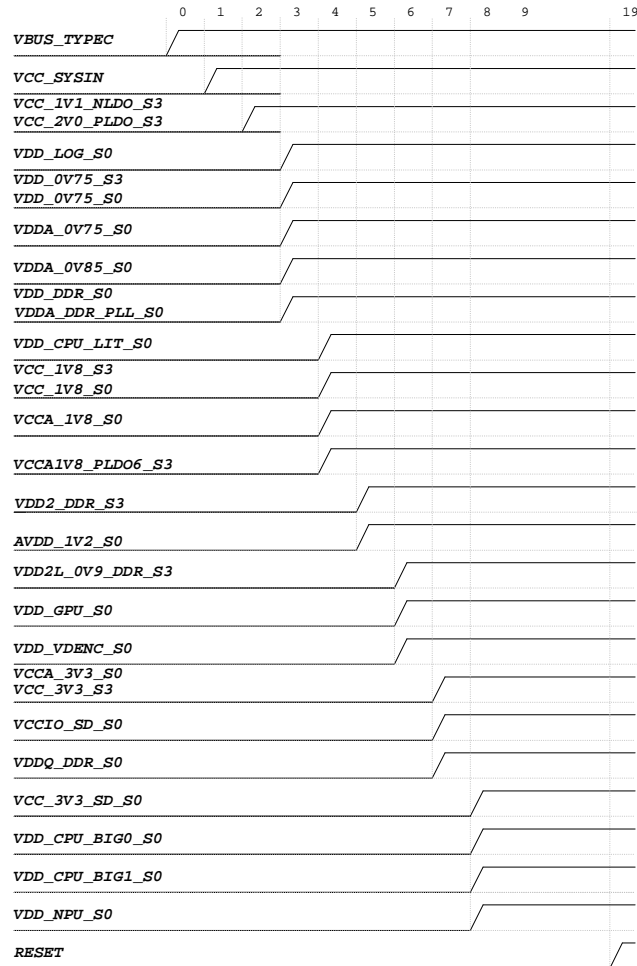
VDDA_0V75_S0

VDDCPU_BIG0 / VDDCPU_BIG0_MEM

VDD_NPU / VDD_NPU_MEM

Shenzhen Wision Technology Co., Ltd.			
Project:	Edge2	Rev:	V12
File:	POWER TREE	Draw:	3
Date:	Thursday, November 17, 2023	Rev:	V12
Designer: JY	Yan	Draw:	3

Power Sequence



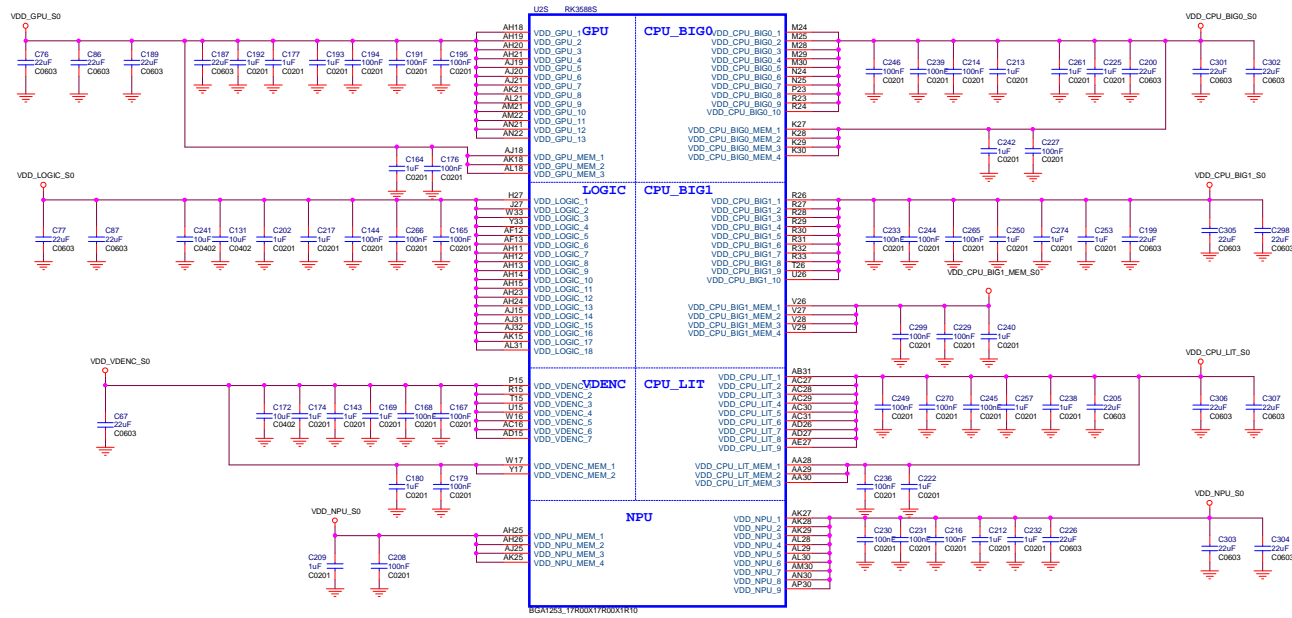
Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_SYSIN	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO_S3	RK806-1_PLDO1	0.5A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N36 N37	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin V37 Y37	1.8V or 3.3V	PMUIO2_1V8	VCC_1V8_S3	1.8V
	Pin V35 V36		PMUIO2	VCC_1V8_S3	1.8V
EMMCIO	Pin AC35	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
	Pin AC36				
VCCIO1	Pin H31	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AK11	1.8V or 3.3V	VCCIO2_1V8	VCC_1V8_S0	1.8V
	Pin AK10		VCCIO2	VCC_IO_SD	1.8V/3.3V
VCCIO4	Pin G27 G28	1.8V or 3.3V	VCCIO4_1V8	VCC_1V8_S0	1.8V
	Pin G31		VCCIO4	VCC_1V8_S0	1.8V
VCCIO5	Pin AF35 AF36	1.8V or 3.3V	VCCIO5_1V8	VCC_1V8_S0	1.8V
	Pin AC33 AC34		VCCIO5	VCC_1V8_S0	1.8V
VCCIO6	Pin AJ34	1.8V or 3.3V	VCCIO6_1V8	VCC_1V8_S0	1.8V
	Pin AL33 AM33		VCCIO6	VCC_3V3_S0	3.3V

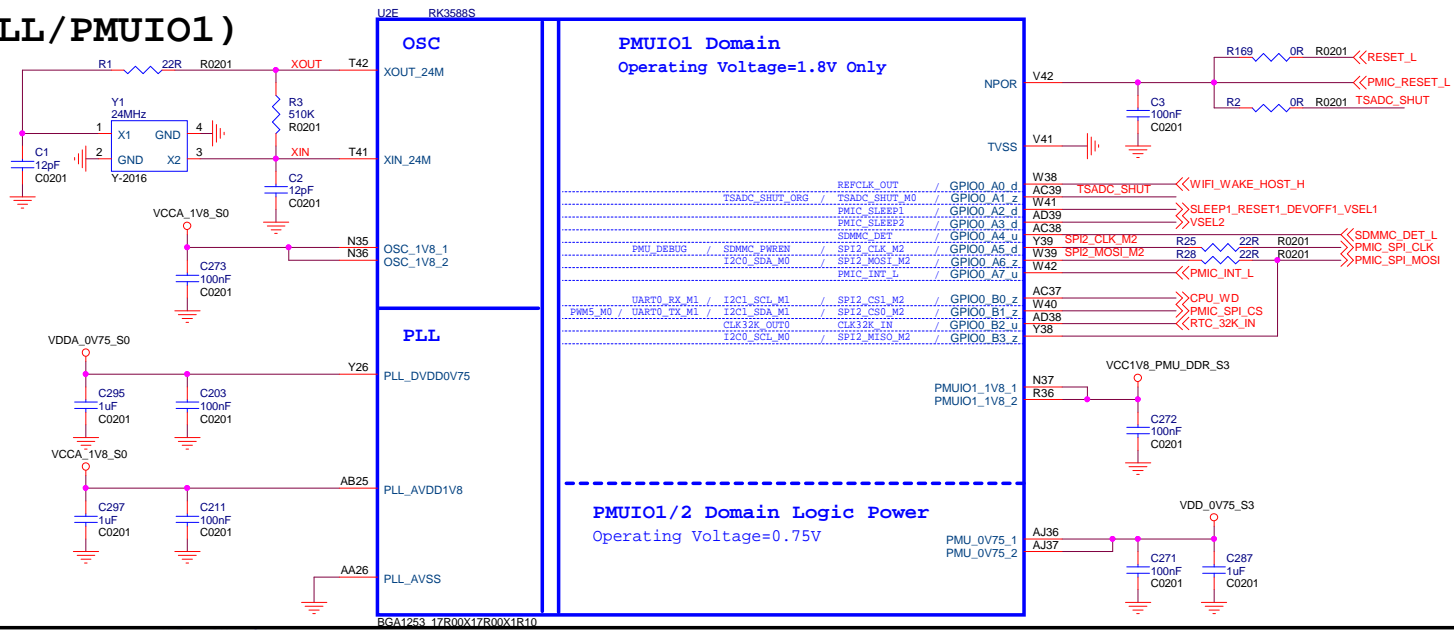
Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	System Power Sequence		
Date:	Thursday, November 17, 2022	Rev:	V12
Designed_by:	Toll	Sheet:	4

RK3588S (Power&Gnd)

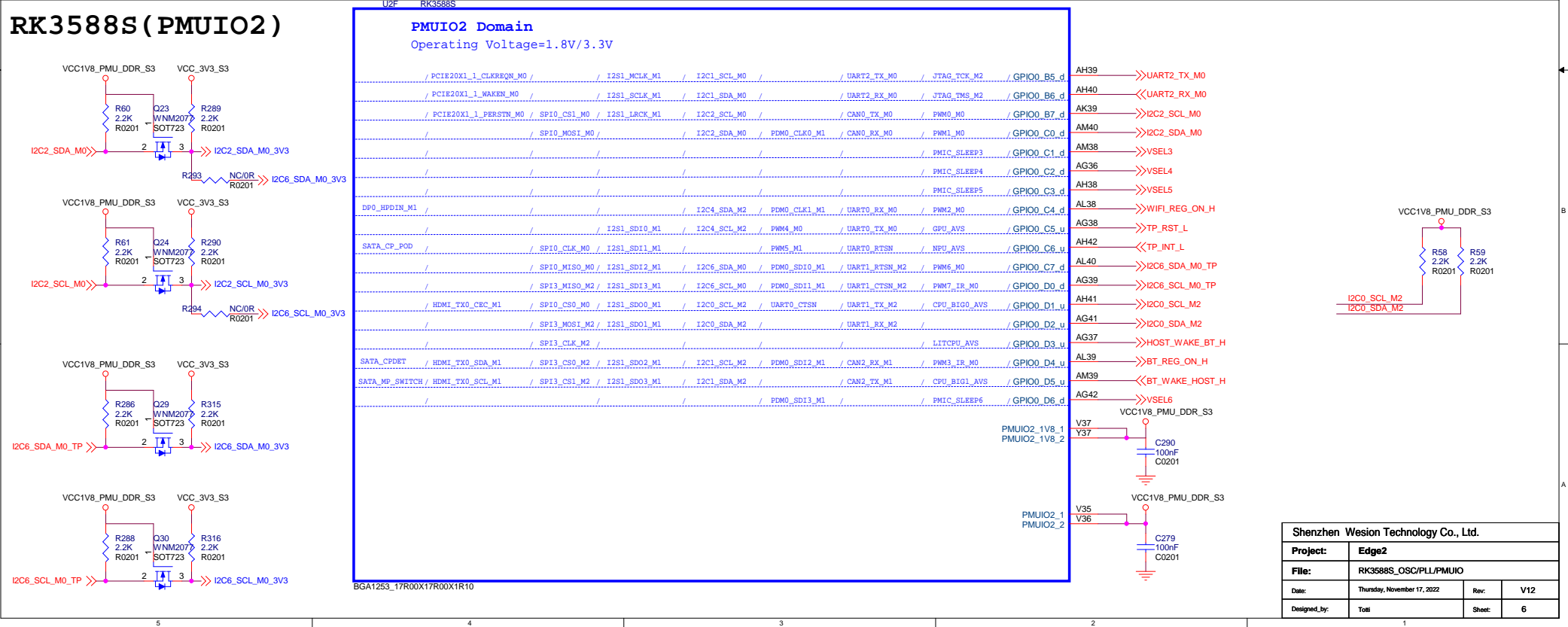


U21 RK3588S	G9 U21 RK3588S	U2V RK3588S	U41 U2V RK3588S	AA10 U2V RK3588S	AD11 U2V RK3588S	AF3 U2X RK3588S	AJ12 U2V RK3588S	U2Y RK3588S	U2Z RK3588S
A1 VSS_1	VSS_101	VSS_201	VSS_301	VSS_401	VSS_501	VSS_601	VSS_701	VSS_801	VSS_901
A2 VSS_2	VSS_102	VSS_202	VSS_302	VSS_402	VSS_502	VSS_602	VSS_702	VSS_802	VSS_902
A3 VSS_3	VSS_103	VSS_203	VSS_303	VSS_403	VSS_503	VSS_603	VSS_703	VSS_803	VSS_903
A4 VSS_4	VSS_104	VSS_204	VSS_304	VSS_404	VSS_504	VSS_604	VSS_704	VSS_804	VSS_904
A5 VSS_5	VSS_105	VSS_205	VSS_305	VSS_405	VSS_505	VSS_605	VSS_705	VSS_805	VSS_905
A6 VSS_6	VSS_106	VSS_206	VSS_306	VSS_406	VSS_506	VSS_606	VSS_706	VSS_806	VSS_906
A7 VSS_7	VSS_107	VSS_207	VSS_307	VSS_407	VSS_507	VSS_607	VSS_707	VSS_807	VSS_907
A8 VSS_8	VSS_108	VSS_208	VSS_308	VSS_408	VSS_508	VSS_608	VSS_708	VSS_808	VSS_908
A9 VSS_9	VSS_109	VSS_209	VSS_309	VSS_409	VSS_509	VSS_609	VSS_709	VSS_809	VSS_909
B10 VSS_10	VSS_110	VSS_210	VSS_310	VSS_410	VSS_510	VSS_610	VSS_710	VSS_810	VSS_910
B11 VSS_11	VSS_111	VSS_211	VSS_311	VSS_411	VSS_511	VSS_611	VSS_711	VSS_811	VSS_911
B12 VSS_12	VSS_112	VSS_212	VSS_312	VSS_412	VSS_512	VSS_612	VSS_712	VSS_812	VSS_912
B13 VSS_13	VSS_113	VSS_213	VSS_313	VSS_413	VSS_513	VSS_613	VSS_713	VSS_813	VSS_913
B14 VSS_14	VSS_114	VSS_214	VSS_314	VSS_414	VSS_514	VSS_614	VSS_714	VSS_814	VSS_914
B15 VSS_15	VSS_115	VSS_215	VSS_315	VSS_415	VSS_515	VSS_615	VSS_715	VSS_815	VSS_915
B16 VSS_16	VSS_116	VSS_216	VSS_316	VSS_416	VSS_516	VSS_616	VSS_716	VSS_816	VSS_916
B17 VSS_17	VSS_117	VSS_217	VSS_317	VSS_417	VSS_517	VSS_617	VSS_717	VSS_817	VSS_917
B18 VSS_18	VSS_118	VSS_218	VSS_318	VSS_418	VSS_518	VSS_618	VSS_718	VSS_818	VSS_918
B19 VSS_19	VSS_119	VSS_219	VSS_319	VSS_419	VSS_519	VSS_619	VSS_719	VSS_819	VSS_919
B20 VSS_20	VSS_120	VSS_220	VSS_320	VSS_420	VSS_520	VSS_620	VSS_720	VSS_820	VSS_920
B21 VSS_21	VSS_121	VSS_221	VSS_321	VSS_421	VSS_521	VSS_621	VSS_721	VSS_821	VSS_921
B22 VSS_22	VSS_122	VSS_222	VSS_322	VSS_422	VSS_522	VSS_622	VSS_722	VSS_822	VSS_922
B23 VSS_23	VSS_123	VSS_223	VSS_323	VSS_423	VSS_523	VSS_623	VSS_723	VSS_823	VSS_923
B24 VSS_24	VSS_124	VSS_224	VSS_324	VSS_424	VSS_524	VSS_624	VSS_724	VSS_824	VSS_924
B25 VSS_25	VSS_125	VSS_225	VSS_325	VSS_425	VSS_525	VSS_625	VSS_725	VSS_825	VSS_925
B26 VSS_26	VSS_126	VSS_226	VSS_326	VSS_426	VSS_526	VSS_626	VSS_726	VSS_826	VSS_926
B27 VSS_27	VSS_127	VSS_227	VSS_327	VSS_427	VSS_527	VSS_627	VSS_727	VSS_827	VSS_927
B28 VSS_28	VSS_128	VSS_228	VSS_328	VSS_428	VSS_528	VSS_628	VSS_728	VSS_828	VSS_928
B29 VSS_29	VSS_129	VSS_229	VSS_329	VSS_429	VSS_529	VSS_629	VSS_729	VSS_829	VSS_929
B30 VSS_30	VSS_130	VSS_230	VSS_330	VSS_430	VSS_530	VSS_630	VSS_730	VSS_830	VSS_930
B31 VSS_31	VSS_131	VSS_231	VSS_331	VSS_431	VSS_531	VSS_631	VSS_731	VSS_831	VSS_931
B32 VSS_32	VSS_132	VSS_232	VSS_332	VSS_432	VSS_532	VSS_632	VSS_732	VSS_832	VSS_932
B33 VSS_33	VSS_133	VSS_233	VSS_333	VSS_433	VSS_533	VSS_633	VSS_733	VSS_833	VSS_933
B34 VSS_34	VSS_134	VSS_234	VSS_334	VSS_434	VSS_534	VSS_634	VSS_734	VSS_834	VSS_934
B35 VSS_35	VSS_135	VSS_235	VSS_335	VSS_435	VSS_535	VSS_635	VSS_735	VSS_835	VSS_935
B36 VSS_36	VSS_136	VSS_236	VSS_336	VSS_436	VSS_536	VSS_636	VSS_736	VSS_836	VSS_936
B37 VSS_37	VSS_137	VSS_237	VSS_337	VSS_437	VSS_537	VSS_637	VSS_737	VSS_837	VSS_937
B38 VSS_38	VSS_138	VSS_238	VSS_338	VSS_438	VSS_538	VSS_638	VSS_738	VSS_838	VSS_938
B39 VSS_39	VSS_139	VSS_239	VSS_339	VSS_439	VSS_539	VSS_639	VSS_739	VSS_839	VSS_939
B40 VSS_40	VSS_140	VSS_240	VSS_340	VSS_440	VSS_540	VSS_640	VSS_740	VSS_840	VSS_940
B41 VSS_41	VSS_141	VSS_241	VSS_341	VSS_441	VSS_541	VSS_641	VSS_741	VSS_841	VSS_941
B42 VSS_42	VSS_142	VSS_242	VSS_342	VSS_442	VSS_542	VSS_642	VSS_742	VSS_842	VSS_942
B43 VSS_43	VSS_143	VSS_243	VSS_343	VSS_443	VSS_543	VSS_643	VSS_743	VSS_843	VSS_943
B44 VSS_44	VSS_144	VSS_244	VSS_344	VSS_444	VSS_544	VSS_644	VSS_744	VSS_844	VSS_944
B45 VSS_45	VSS_145	VSS_245	VSS_345	VSS_445	VSS_545	VSS_645	VSS_745	VSS_845	VSS_945
B46 VSS_46	VSS_146	VSS_246	VSS_346	VSS_446	VSS_546	VSS_646	VSS_746	VSS_846	VSS_946
B47 VSS_47	VSS_147	VSS_247	VSS_347	VSS_447	VSS_547	VSS_647	VSS_747	VSS_847	VSS_947
B48 VSS_48	VSS_148	VSS_248	VSS_348	VSS_448	VSS_548	VSS_648	VSS_748	VSS_848	VSS_948
B49 VSS_49	VSS_149	VSS_249	VSS_349	VSS_449	VSS_549	VSS_649	VSS_749	VSS_849	VSS_949
B50 VSS_50	VSS_150	VSS_250	VSS_350	VSS_450	VSS_550	VSS_650	VSS_750	VSS_850	VSS_950

RK3588S (OSC/PLL/PMUIO1)

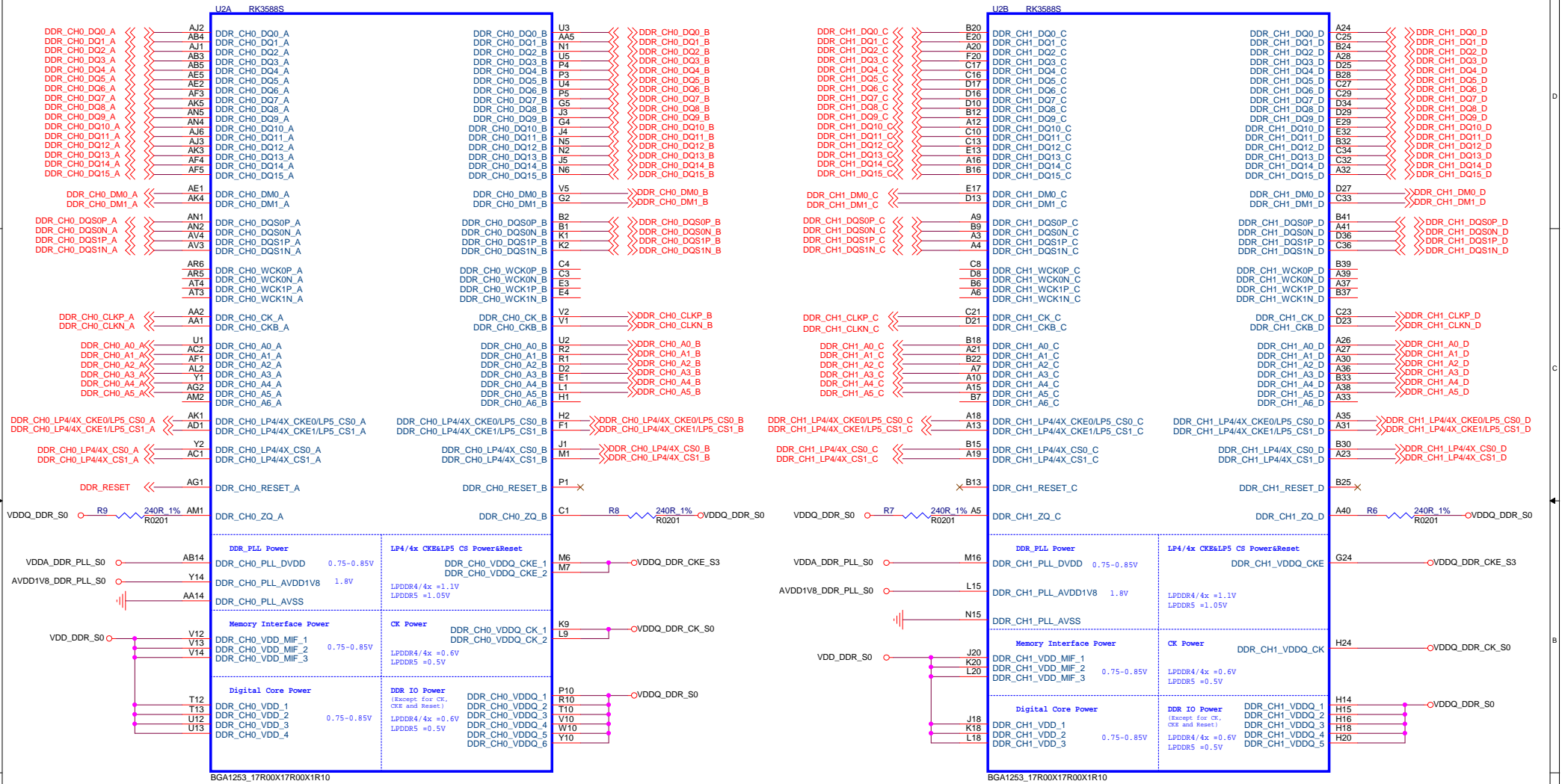


RK3588S (PMUIO2)

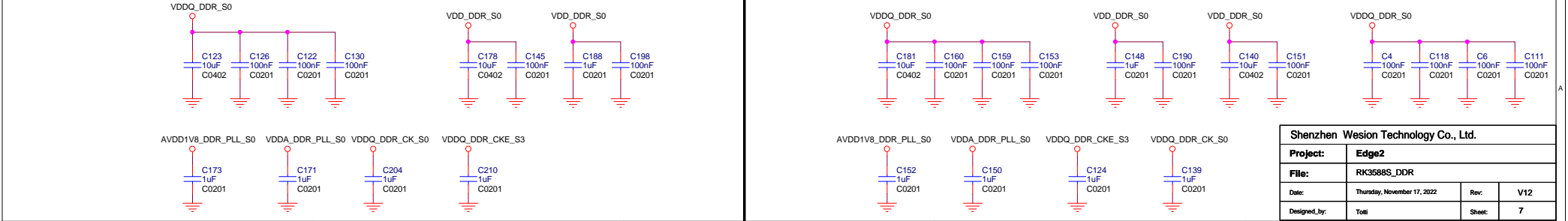


Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	RK3588S_OSC/PLL/PMUIO		
Date:	Thursday, November 17, 2022	Rev:	V12
Designed_by:	Toll	Sheet:	6

RK3588S (DDR PHY)



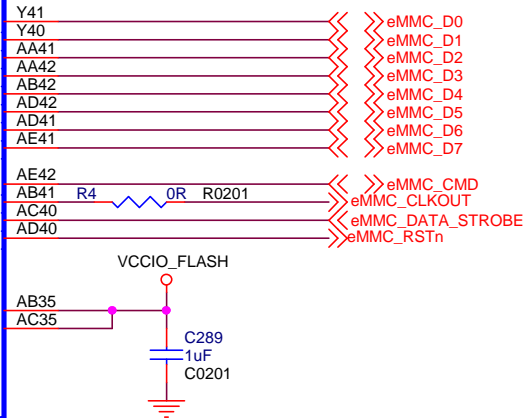
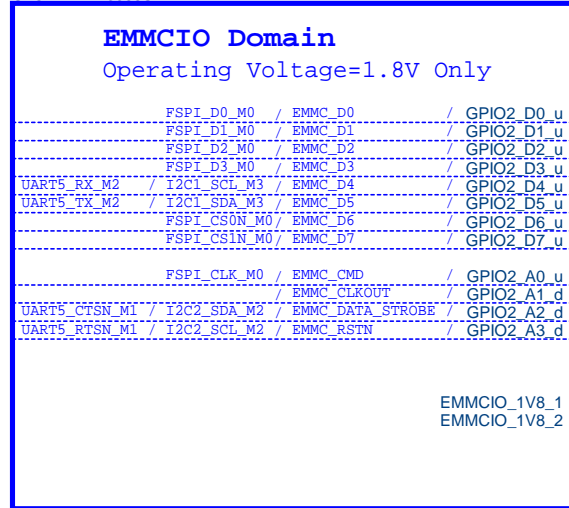
DDR FILTER



Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	RK3588S_DDR		
Date:	Thursday, November 17, 2022	Rev:	V12
Designed_by:	Toll	Sheet:	7

RK3588S (EMMCIO Domain)

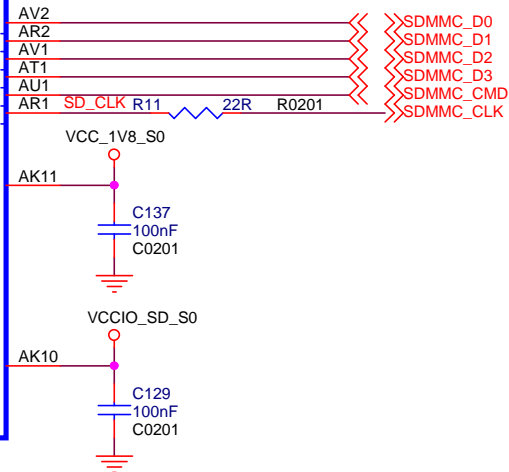
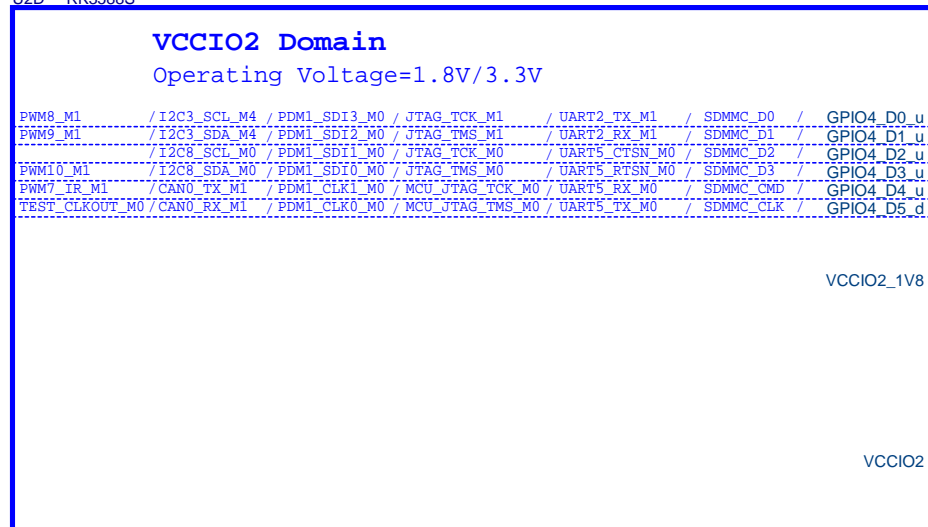
U2C RK3588S



BGA1253_17R00X17R00X1R10

RK3588S (VCCIO2 Domain)

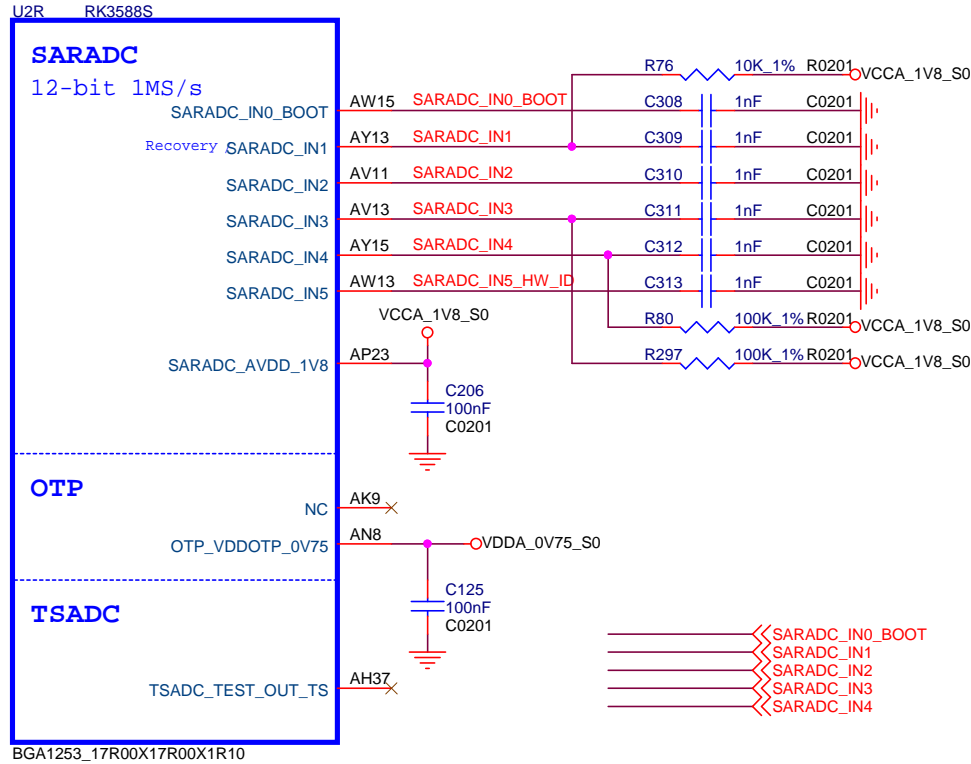
U2D RK3588S



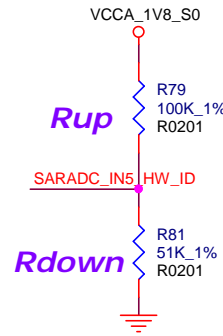
BGA1253_17R00X17R00X1R10

Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	RK3588S_Flash/SD		
Date:	Thursday, November 17, 2022	Rev:	V12
Designed_by:	Totti	Sheet:	8

RK3588S (SARADC/OTP/TSADC)

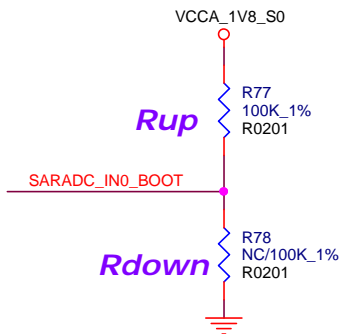


BOARD ID CONFIG



Item	Rup	Rdown	ADC	VERSION
LEVEL1	DNP	100K	0	V10
LEVEL2	100K	20K	682	V11
LEVEL3	100K	51K	1365	V12
LEVEL4	100K	100K	2047	V13
LEVEL5	100K	200K	2730	V14
LEVEL6	100K	499K	3412	V15
LEVEL7	100K	DNP	4095	V16

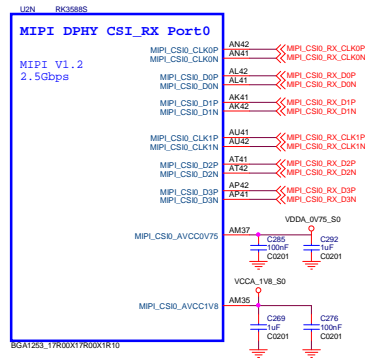
BOOT MODE CONFIG



Item	Rup	Rdown	ADC	BOOT MODE
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	RK3588S_SARADC		
Date:	Thursday, December 15, 2022	Rev:	V12
Designed_by:	Totti	Sheet:	9

RK3588S(MIPI_DPHY CSI0 RX)

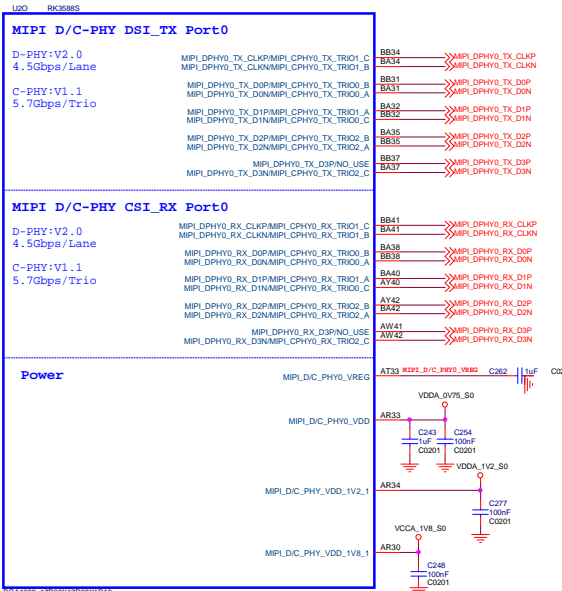


Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane	MIPI_CSI_RX_D0-1
	+ Sensor2 x2Lane	MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

BGA1253_17R00X17R00X1R10

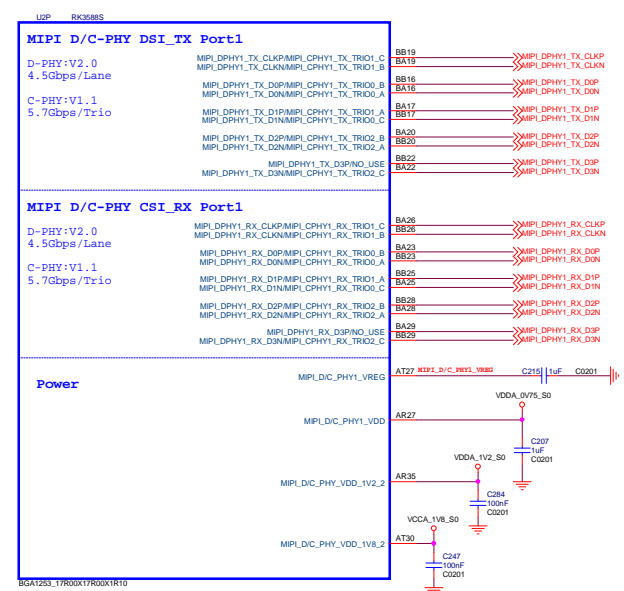
BGA1253_17R00X17R00X1R10

RK3588S(MIPI_D/C PHY0)



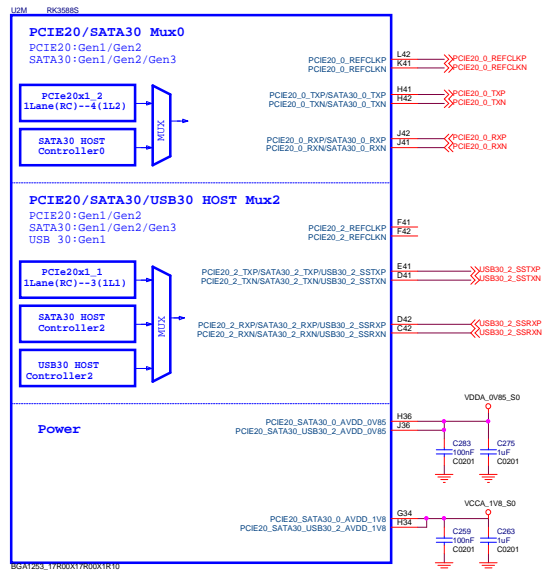
BGA1253_17R00X17R00X1R10

RK3588S(MIPI_D/C PHY1)



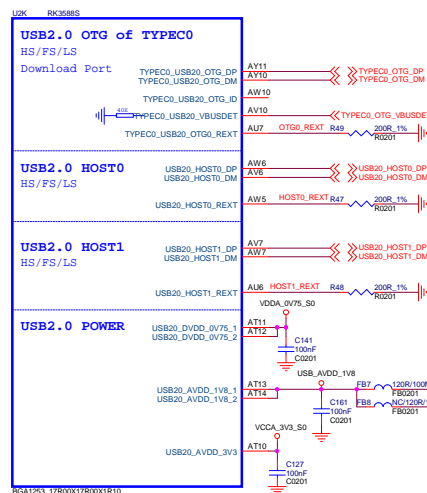
BGA1253_17R00X17R00X1R10

RK3588S(PCIE20/SATA30/USB30)



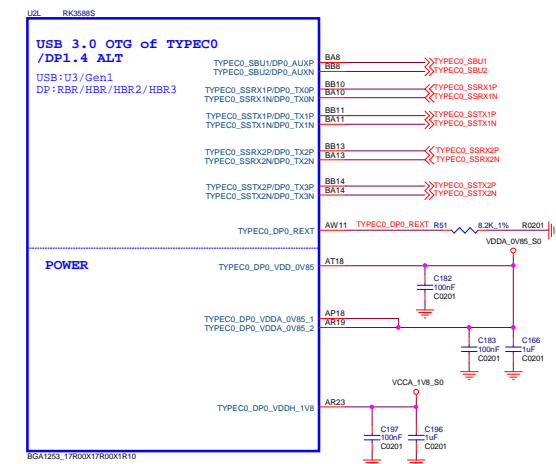
BGA1253_17R00X17R00X1R10

RK3588S(USB2.0)



BGA1253_17R00X17R00X1R10

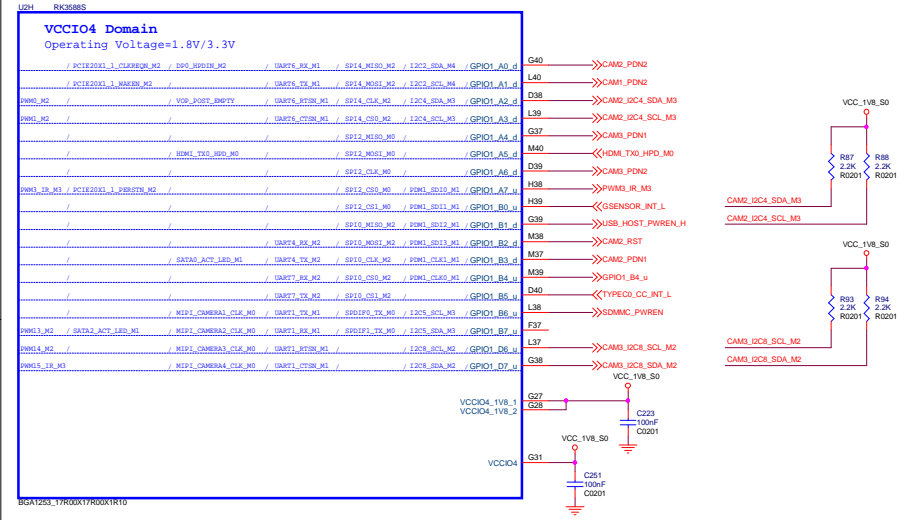
RK3588S(USB3.0/DP1.4)



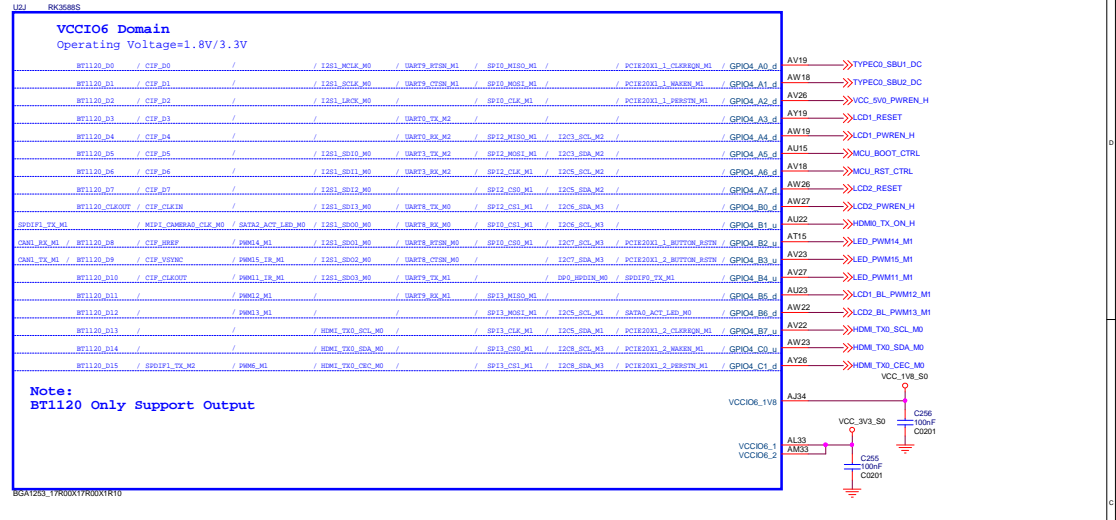
BGA1253_17R00X17R00X1R10

Shenzhen Wision Technology Co., Ltd.			
Project:	Edge2	Rev:	V12
File:	RK3588S_MIPUSBC/PCIE	Draw:	10
Date:	Thursday, November 17, 2022		
Designed by:	Yan		

RK3588S (VCCIO4 Domain)

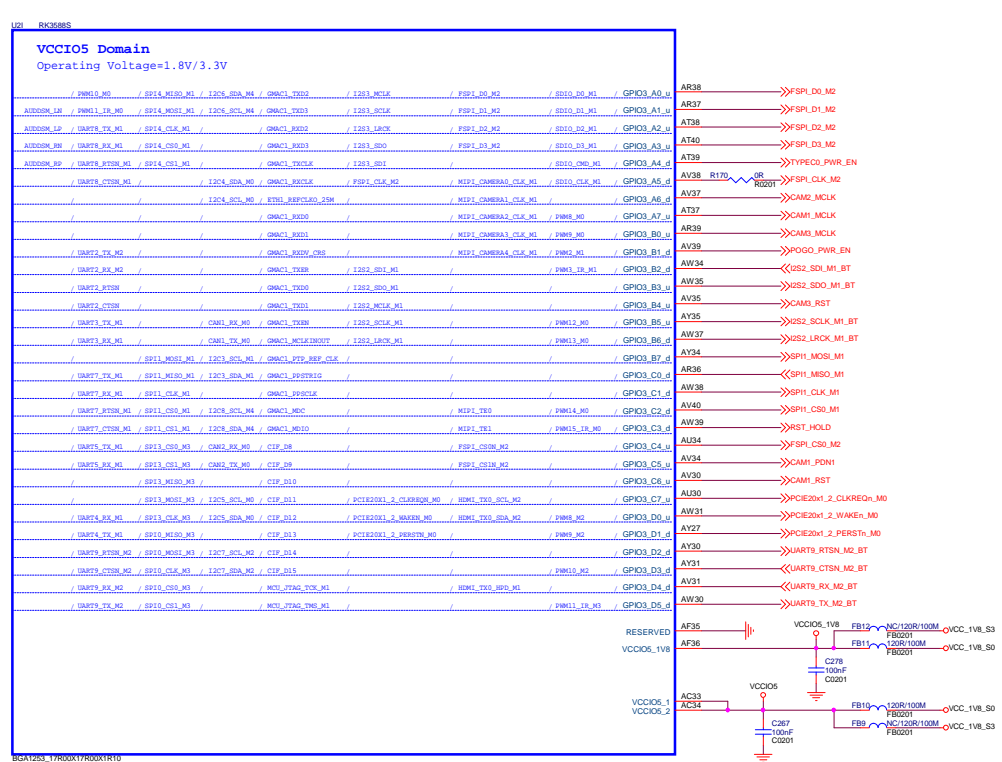


RK3588S (VCCIO6 Domain)

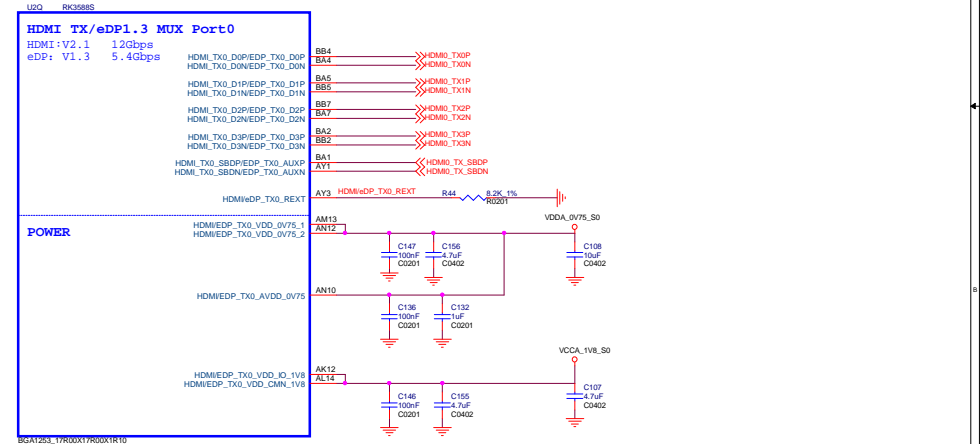


Note: BT1120 Only Support Output

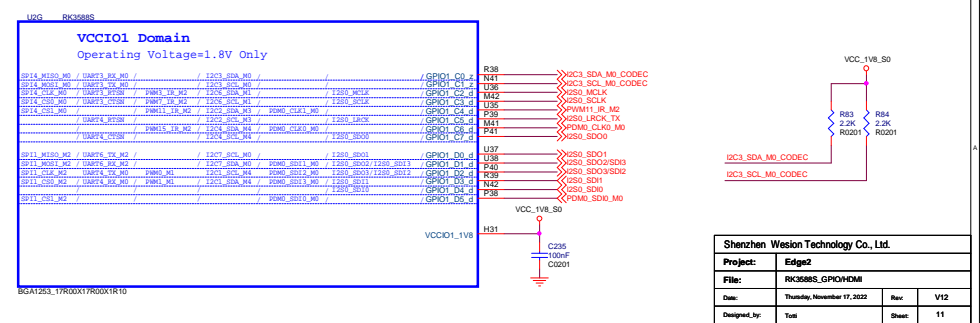
RK3588S (VCCIO5 Domain)



RK3588S (HDMI2.1 TX/eDP1.3 TX)

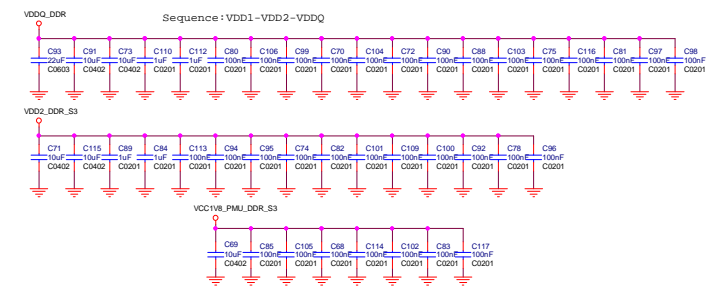
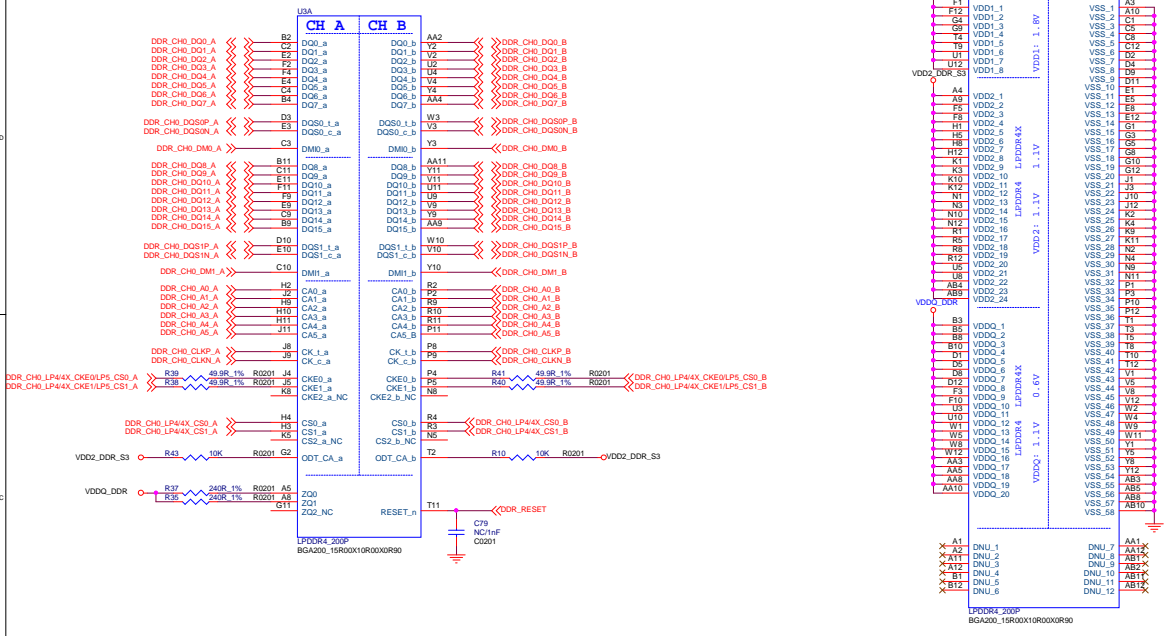


RK3588S (VCCIO1 Domain)

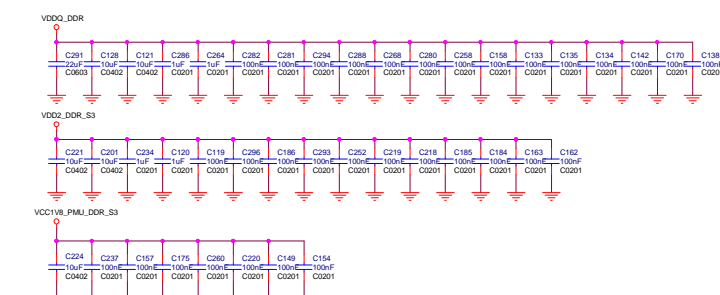
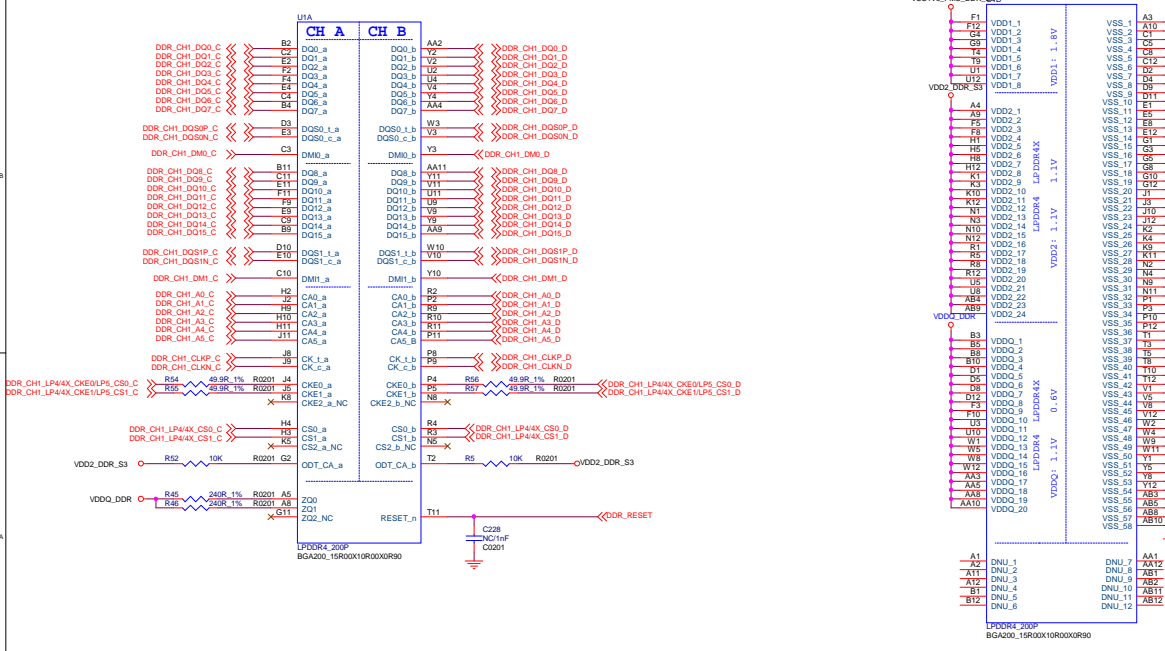
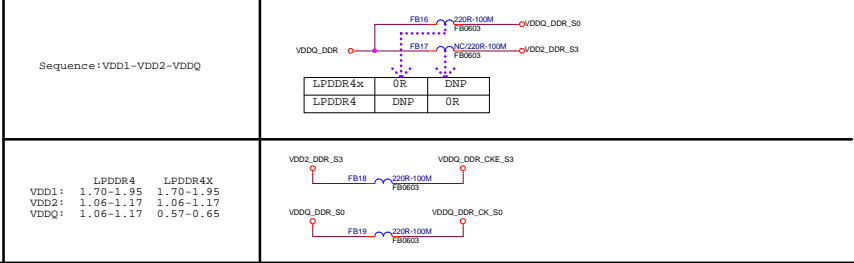


Shenzhen Wision Technology Co., Ltd.			
Project:	Edge2	Rev:	V12
File:	RK3588S_GPIOHDM	Rev:	
Date:	Thursday, November 17, 2022	Rev:	V12
Designed by:	Tao	Draw:	11

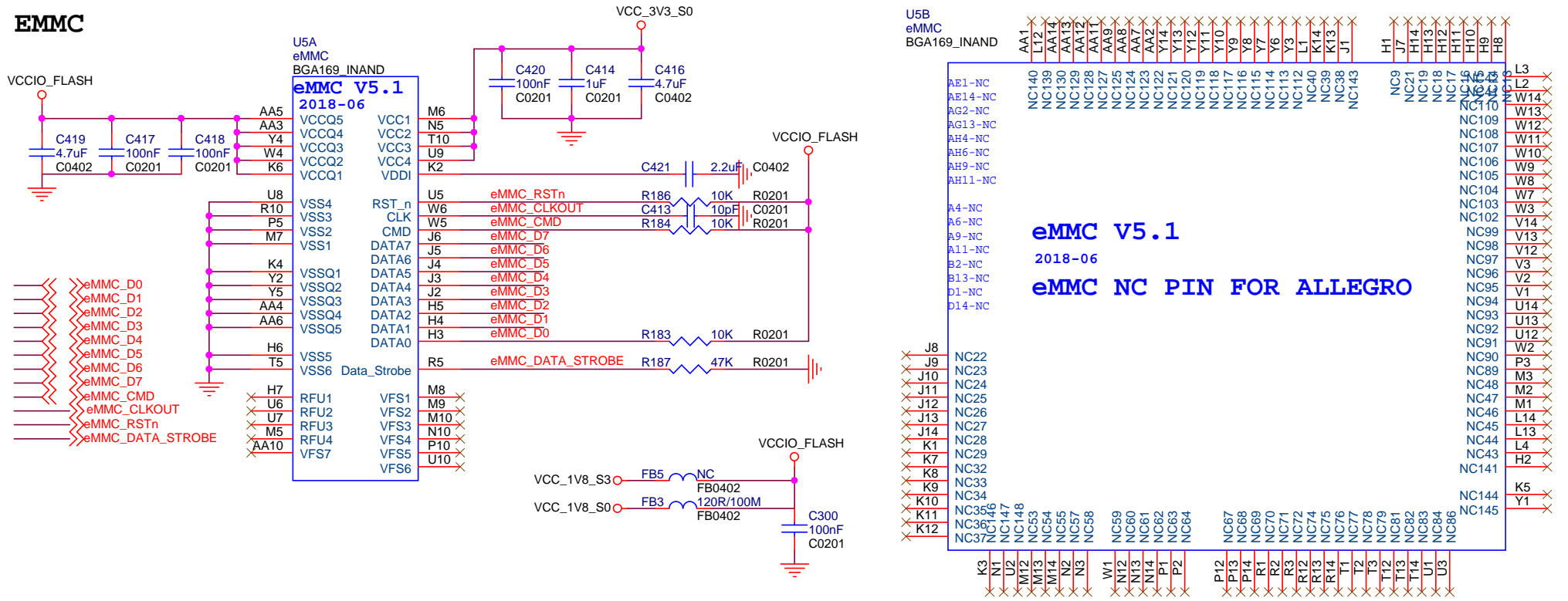
DRAM-LPDDR4/4x_2X32bit



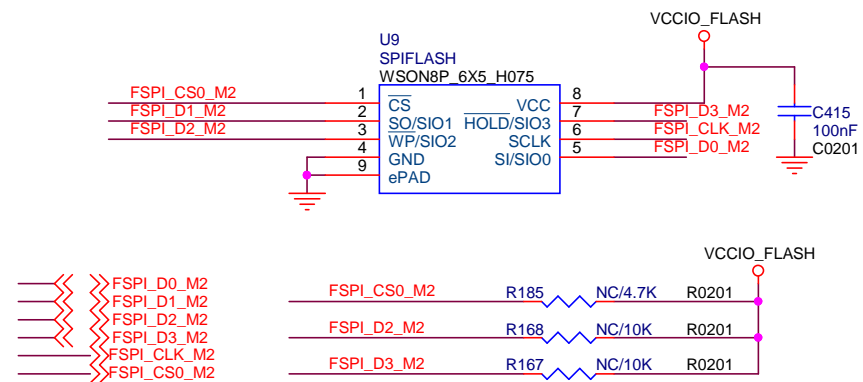
DRAM-LPDDR4/4x Power



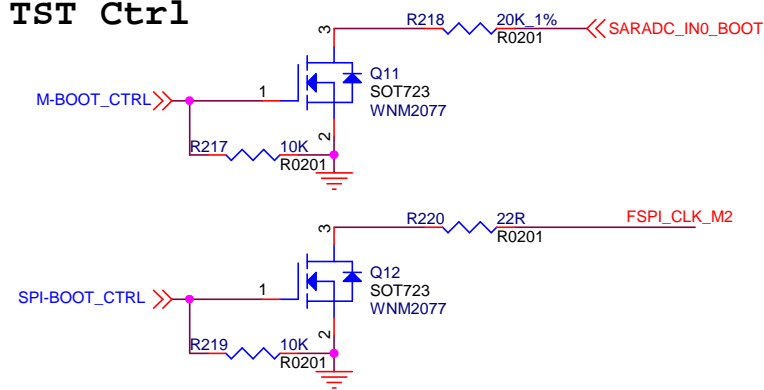
EMMC



SPI FLASH



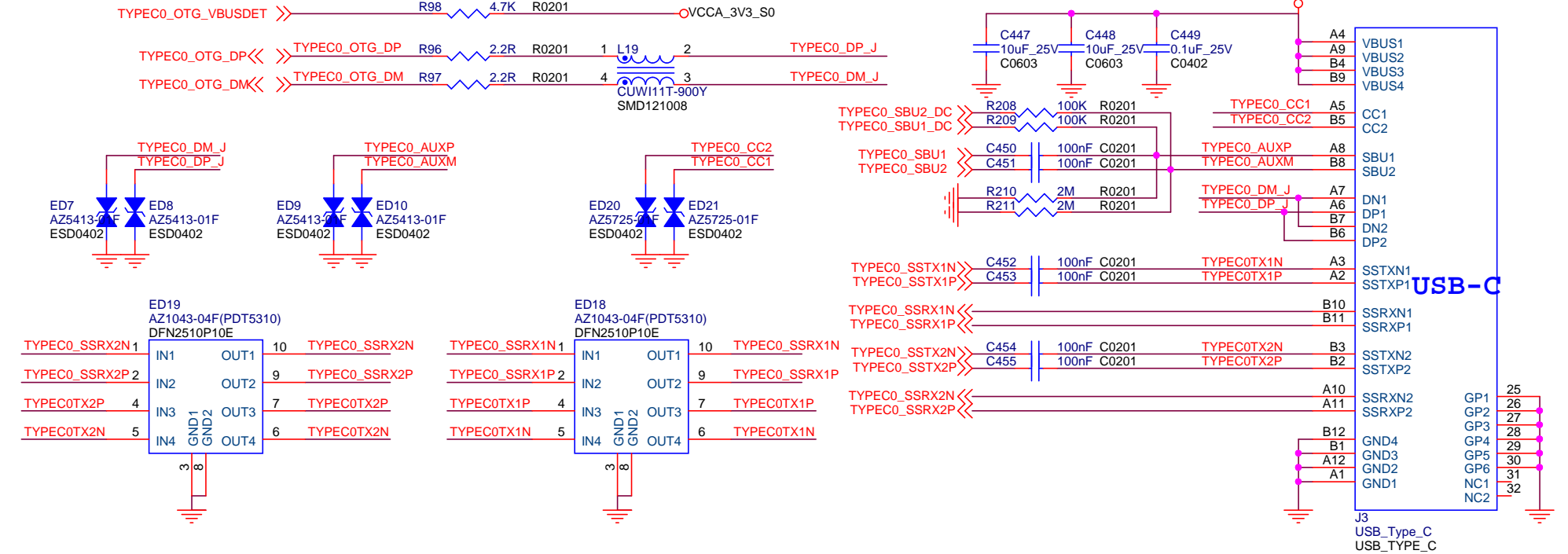
TST Ctrl



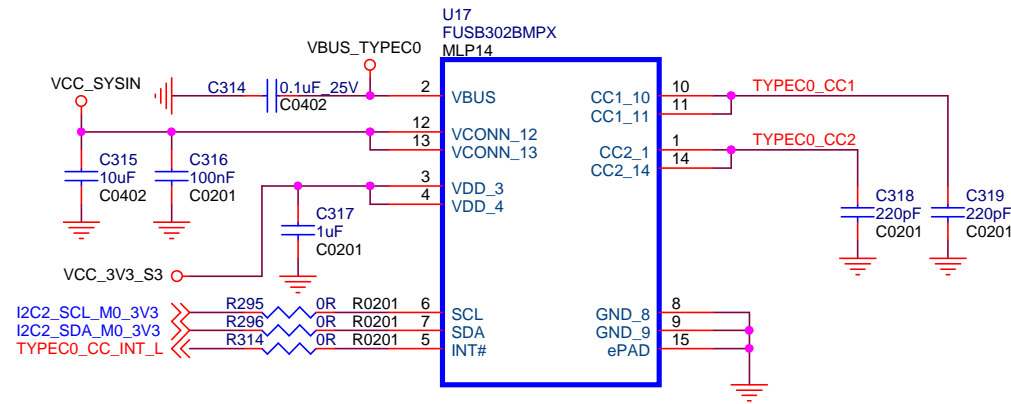
M-BOOT_CTRL	SPI-BOOT_CTRL	BOOT Priority
L	H	EMMC>USB
H	X	SD>USB
L	L	SPI>EMMC>USB default

Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	EMMC/SPI-FLASH		
Date:	Thursday, December 15, 2022	Rev:	V12
Designed_by:	Totit	Sheet:	13

TYPE-C0 Port



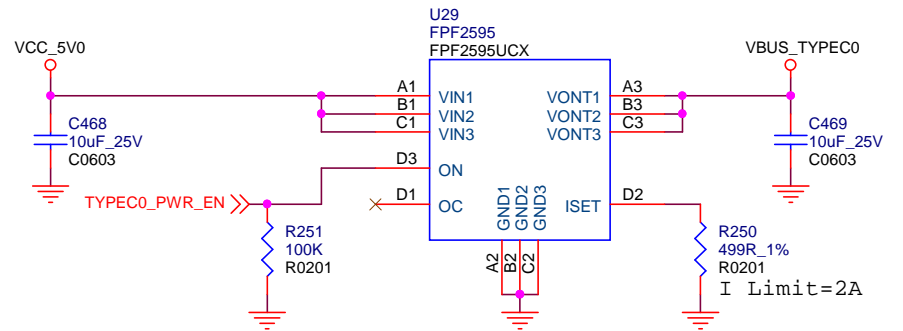
USB Type-C0 Controller(PD)



7bit address=0x22

VBUS of FUSB302BMPX: 4 to 21 TYP = 5V
 VDD of FUSB302BMPX: 3 to 5.5 TYP = 3.3V
 VCONN of FUSB302BMPX: 3 to 5.5

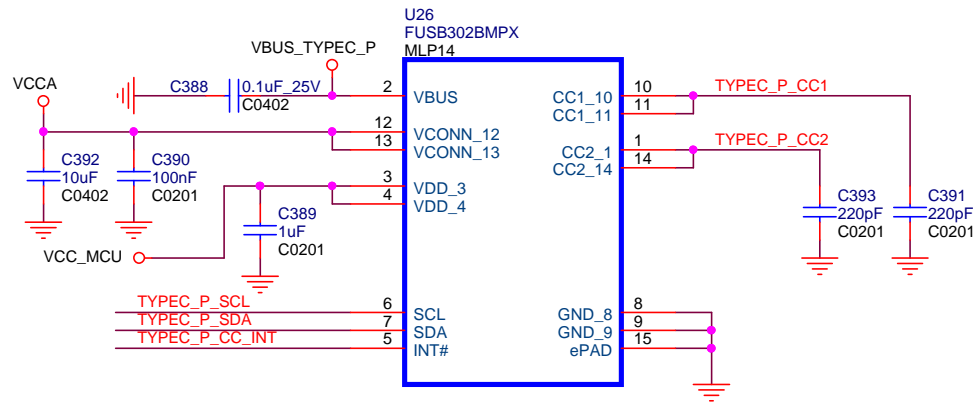
USB Type-C0 POWER



I Limit=2A

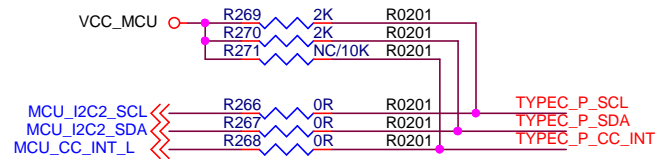
Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	Type-C0 Port		
Date:	Monday, November 21, 2022	Rev:	V12
Designed_by:	Totiti	Sheet:	14

USB Type-C_P Controller(PD)

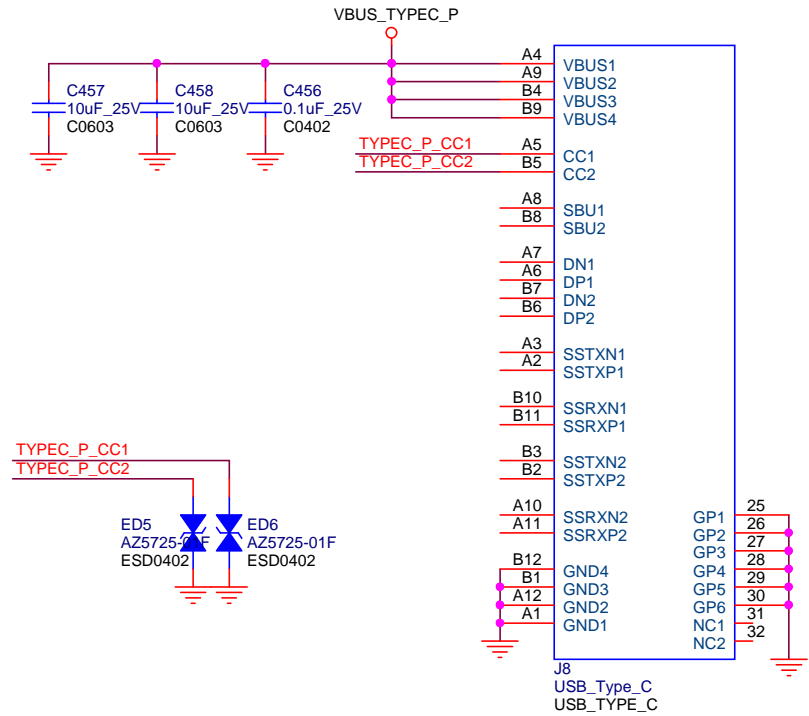


7bit address=0x22

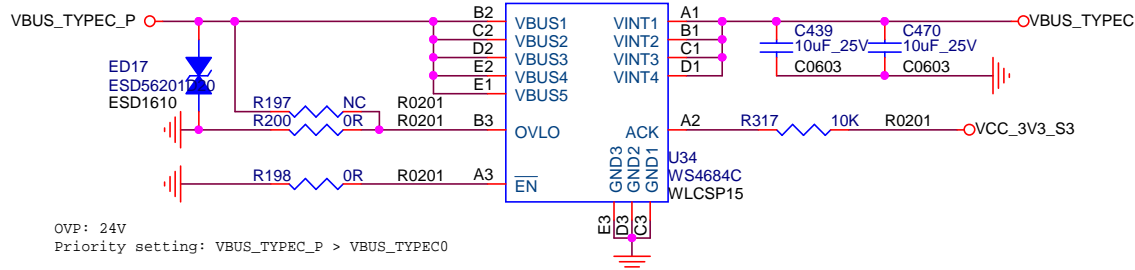
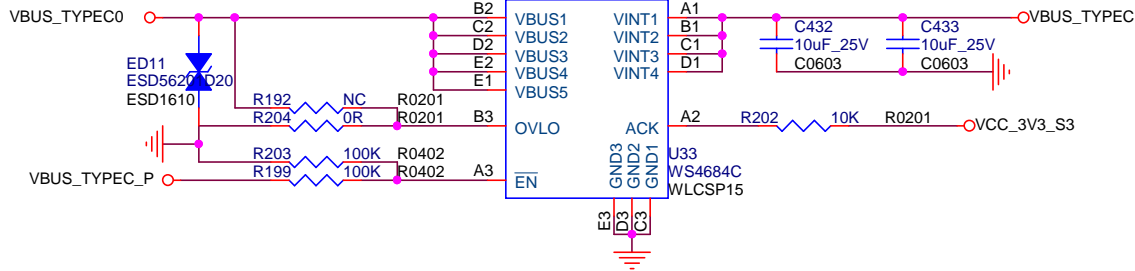
VBUS of FUSB302BMPX: 4 to 21 TYP = 5V
VDD of FUSB302BMPX: 3 to 5.5 TYP = 3.3V
VCONN of FUSB302BMPX: 3 to 5.5



TYPE-C POWER-Only Port



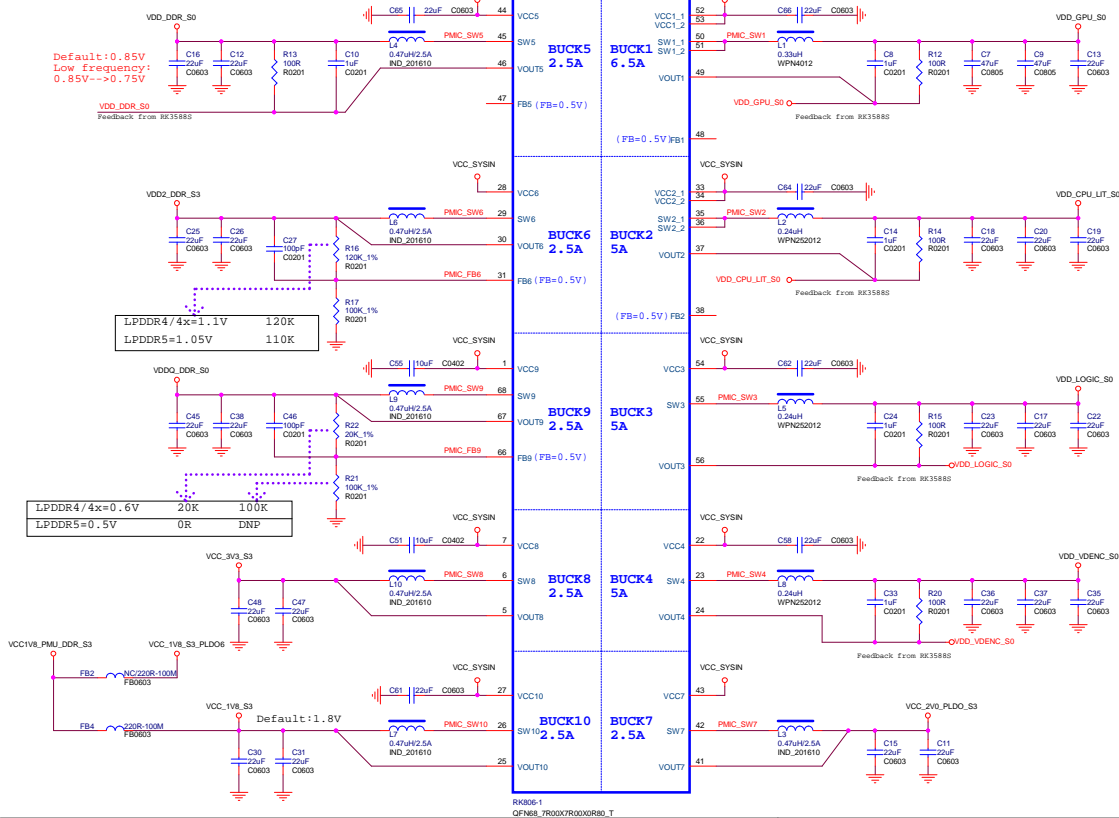
TYPE-C PWR PATH



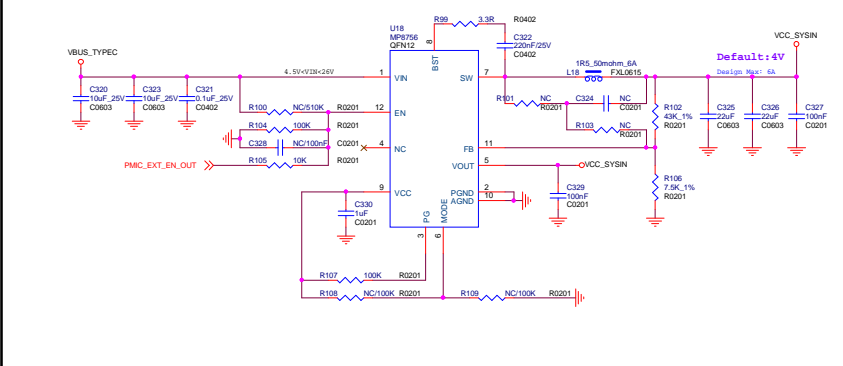
OVP: 24V
Priority setting: VBUS_TYPPEC_P > VBUS_TYPPEC0

Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	Type-C PWR Port		
Date:	Thursday, December 15, 2022	Rev:	V12
Designed_by:	Totit	Sheet:	15

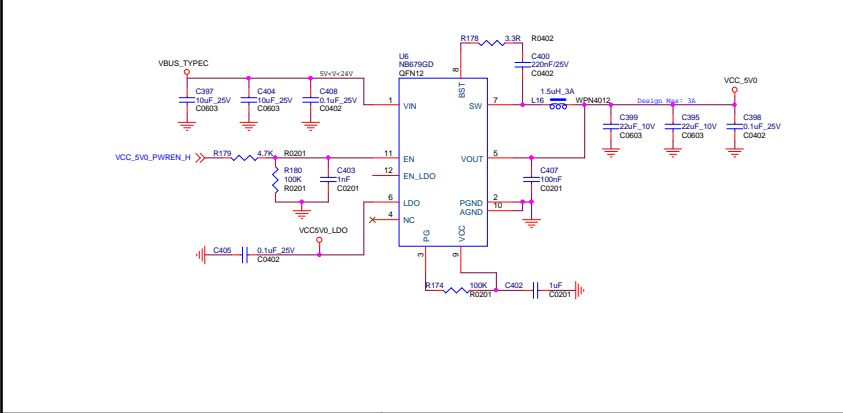
PMIC RK806-1 BUCK



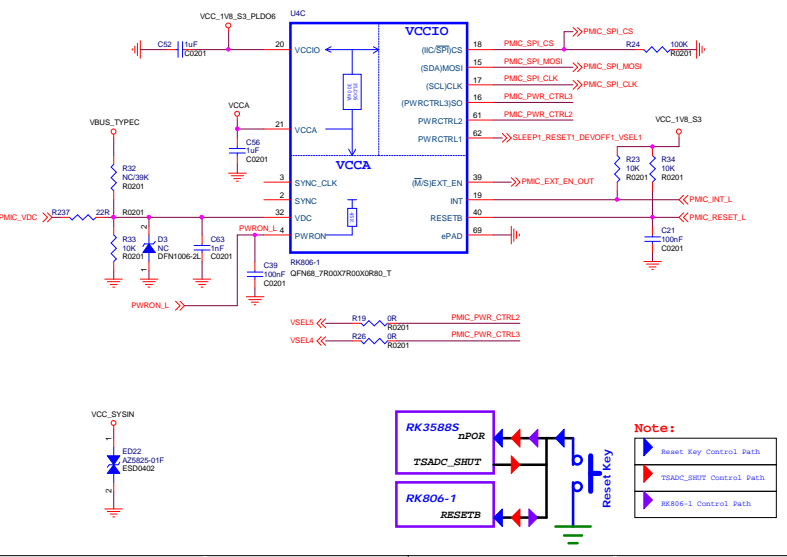
VCC_SYSIN



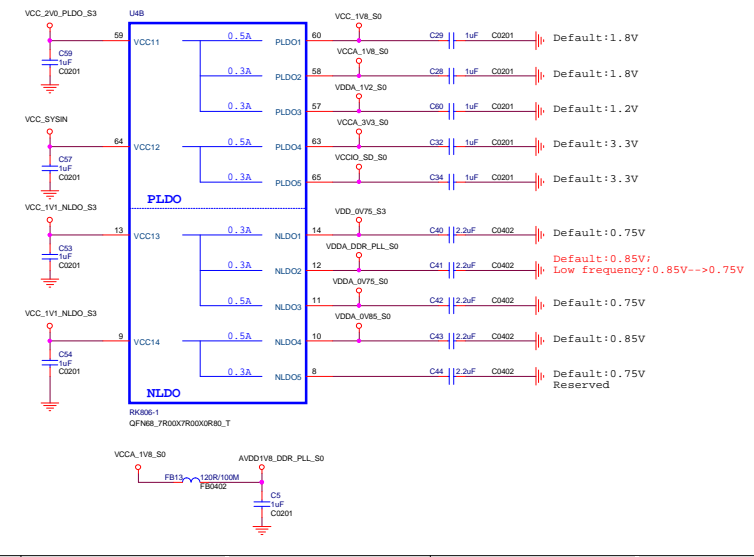
VCC5V



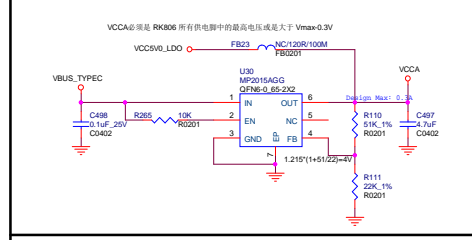
PMIC RK806-1 Management



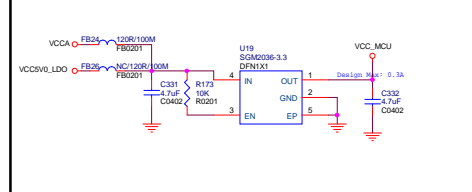
PMIC RK806-1 LDO



VCCA

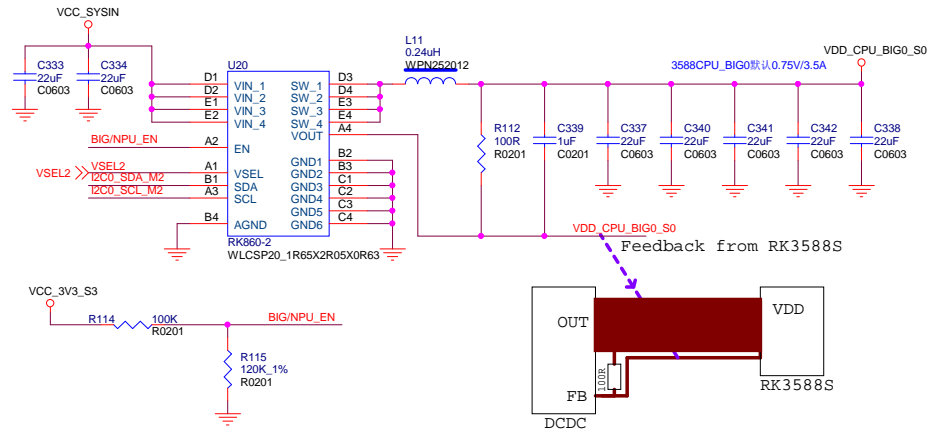


VCC_MCU

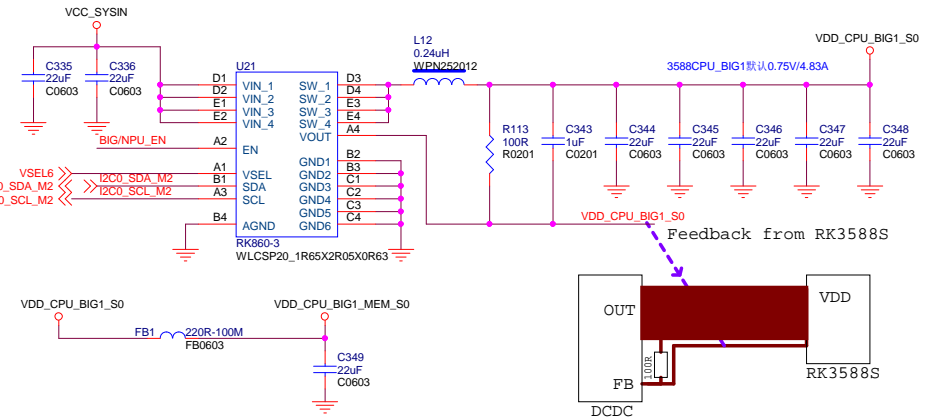


Shenzhen Wision Technology Co., Ltd.			
Project:	Edge2	Rev:	V12
File:	Power_RK806-1SYSINVCCSV	Draw:	16
Date:	Thursday, November 17, 2023		
Designed_by:	Yan		

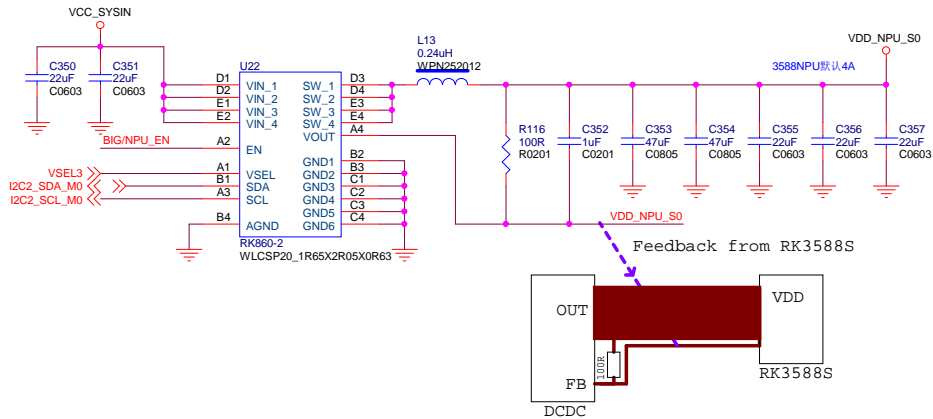
VDD_CPU_BIG0



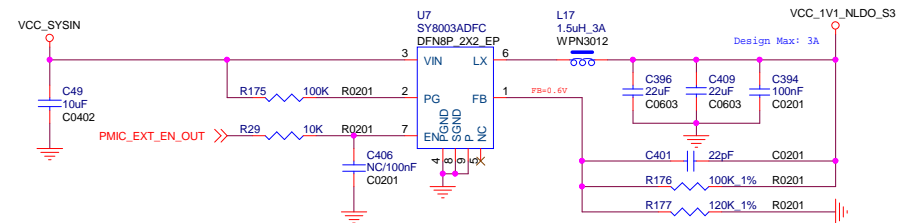
VDD_CPU_BIG1



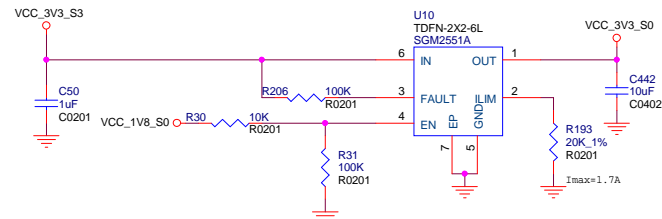
VDD_NPU



VCC_1V1_NLDO

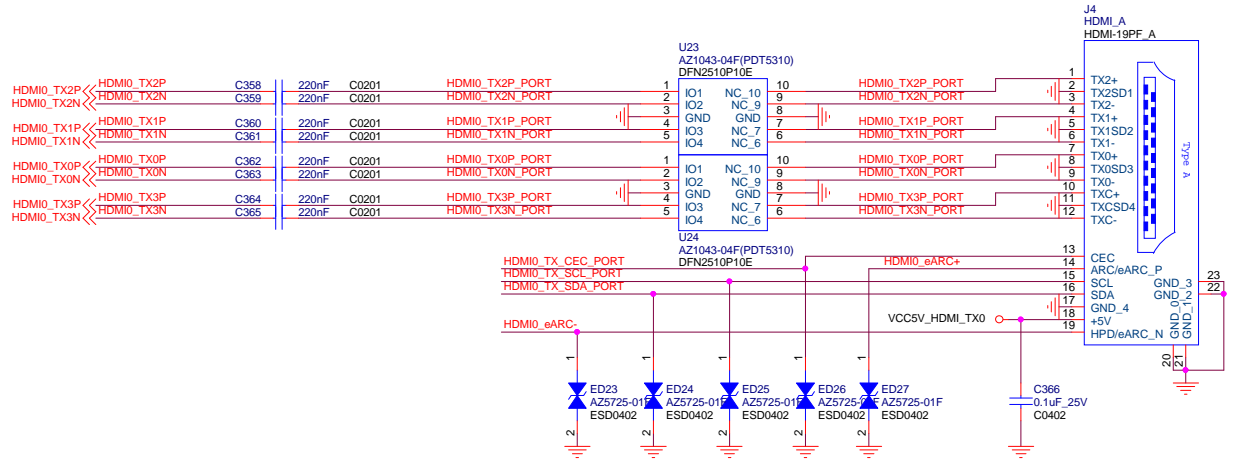


VCC_3V3_S0

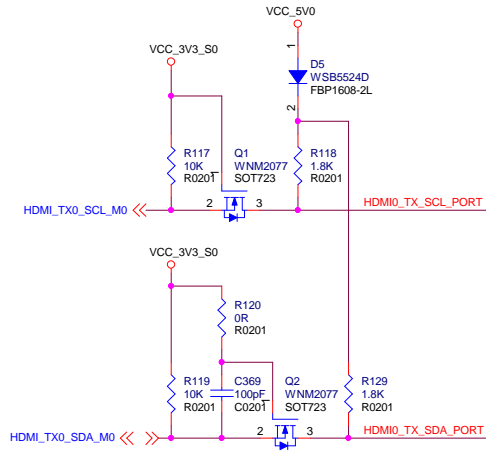


Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	Power_Ext_Discrete		
Date:	Thursday, November 17, 2022	Rev:	V12
Designed_by:	Toll	Sheet:	17

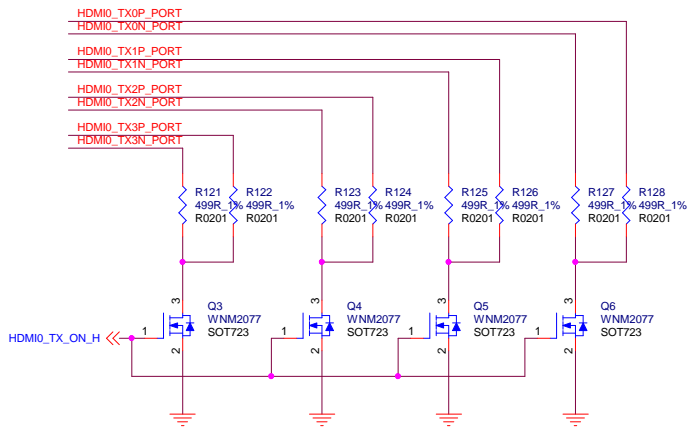
HDMI2.1 TX0



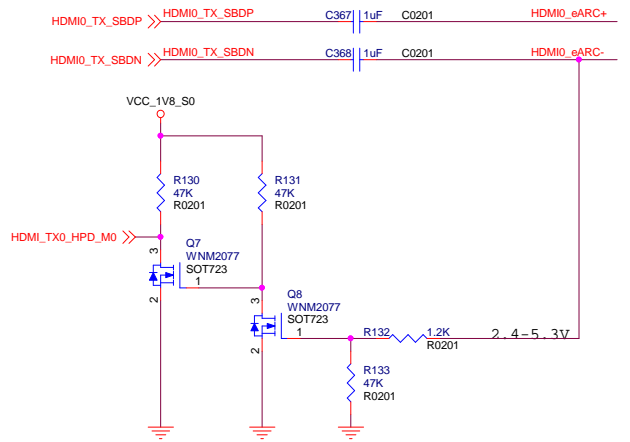
HDMI TX DDC



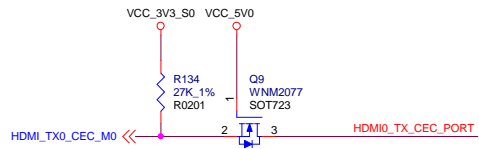
HDMI 2.0/2.1 SW



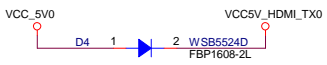
HDMI TX eARC



HDMI TX CEC

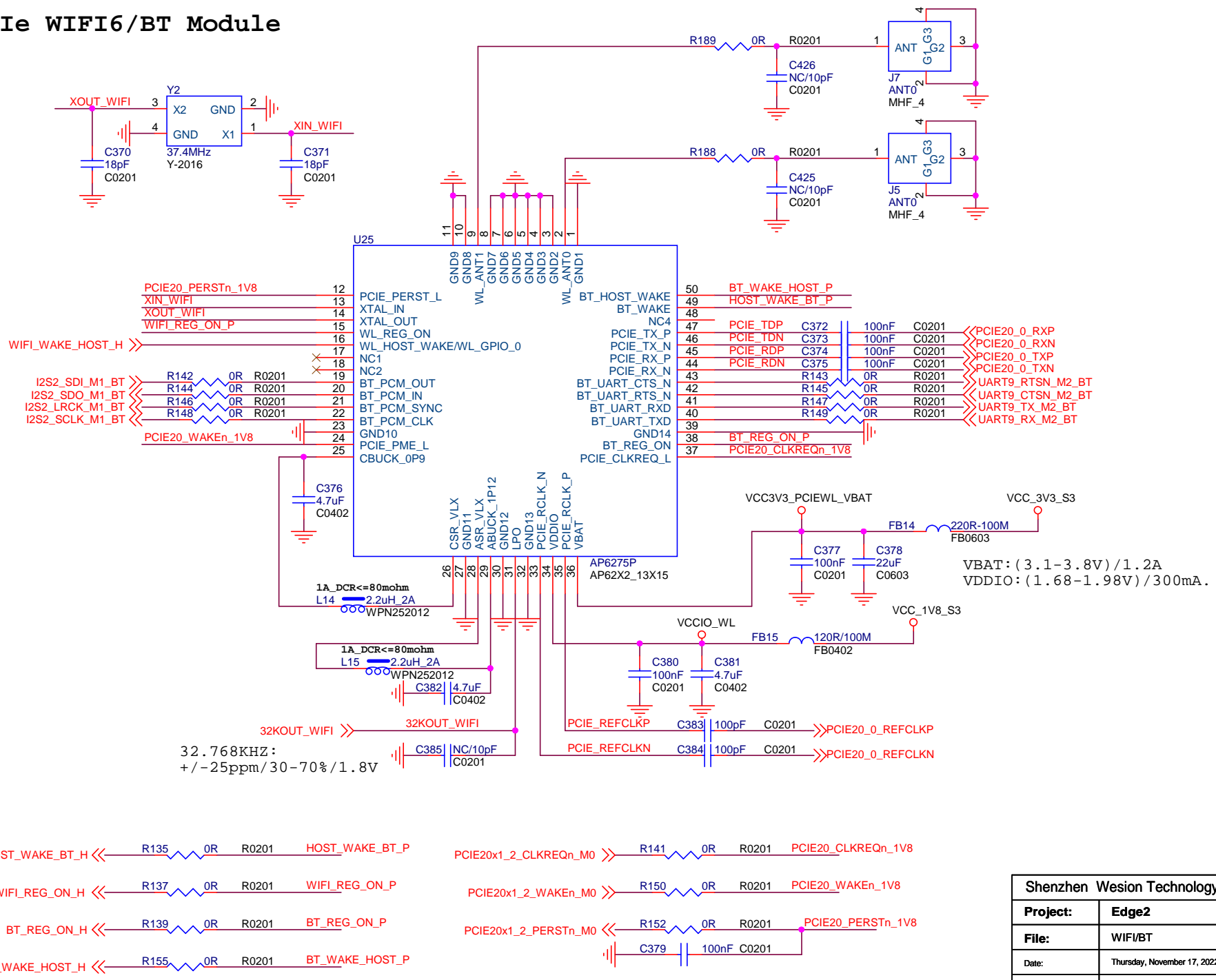


HDMI Power



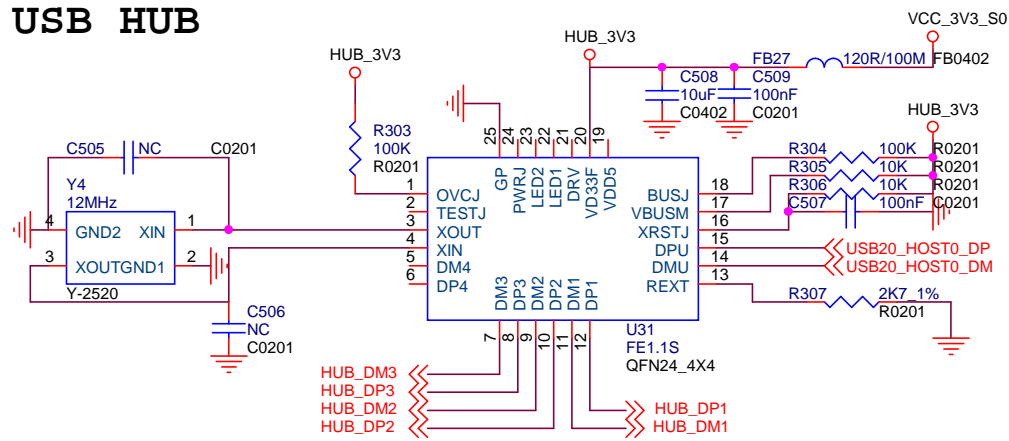
Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	HDMI OUT		
Date:	Thursday, November 17, 2022	Rev:	V12
Designed_by:	Toni	Sheet:	18

PCIe WIFI6/BT Module

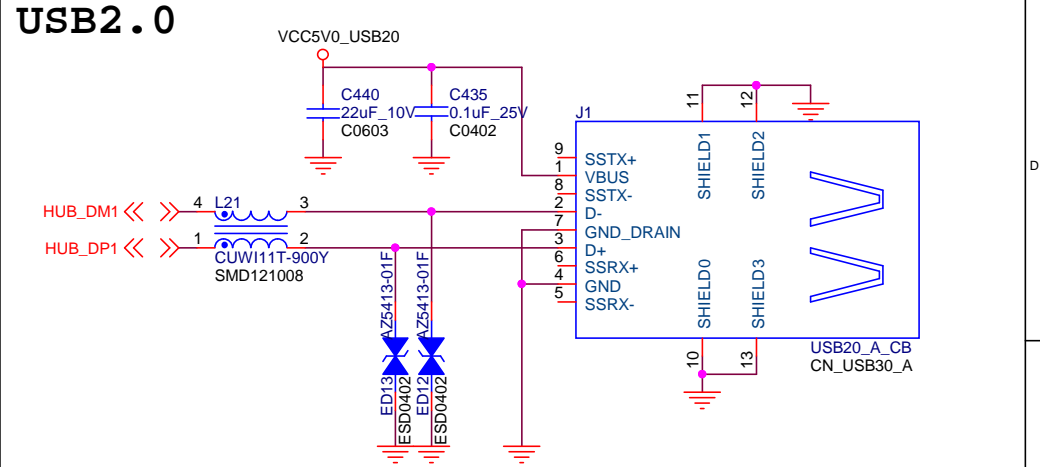


Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	WIFI/BT		
Date:	Thursday, November 17, 2022	Rev:	V12
Designed_by:	Totti	Sheet:	19

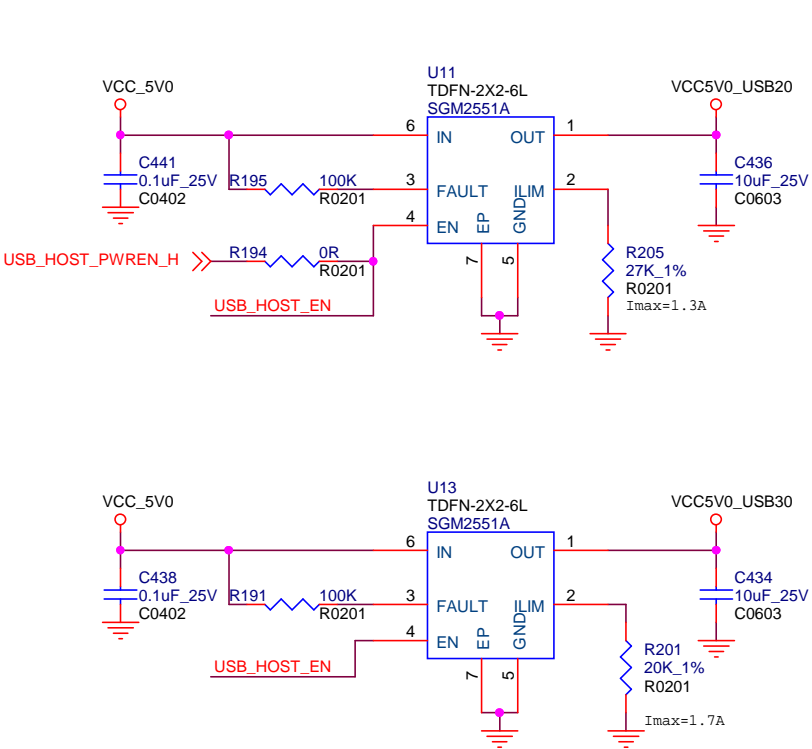
USB HUB



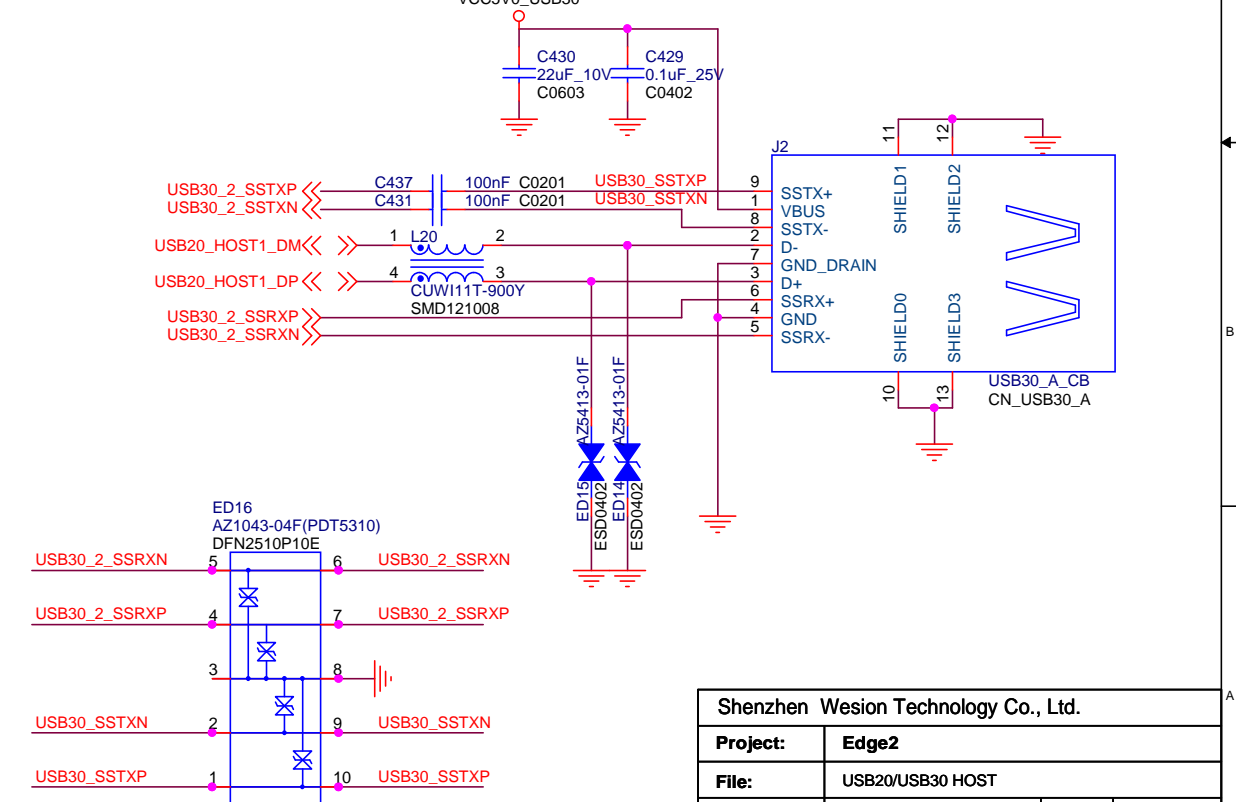
USB2.0



USB PWR SW

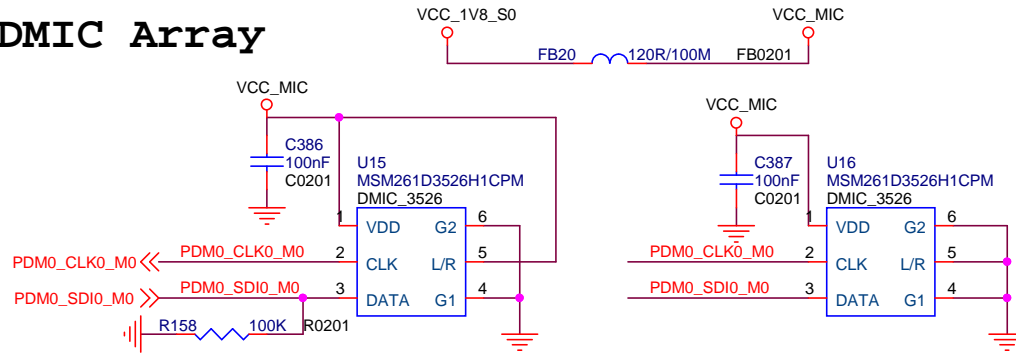


USB3.0

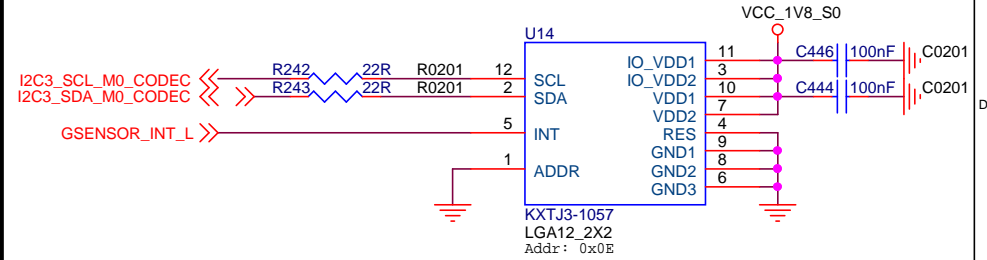


Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	USB20/USB30 HOST		
Date:	Thursday, November 17, 2022	Rev:	V12
Designed_by:	Totit	Sheet:	20

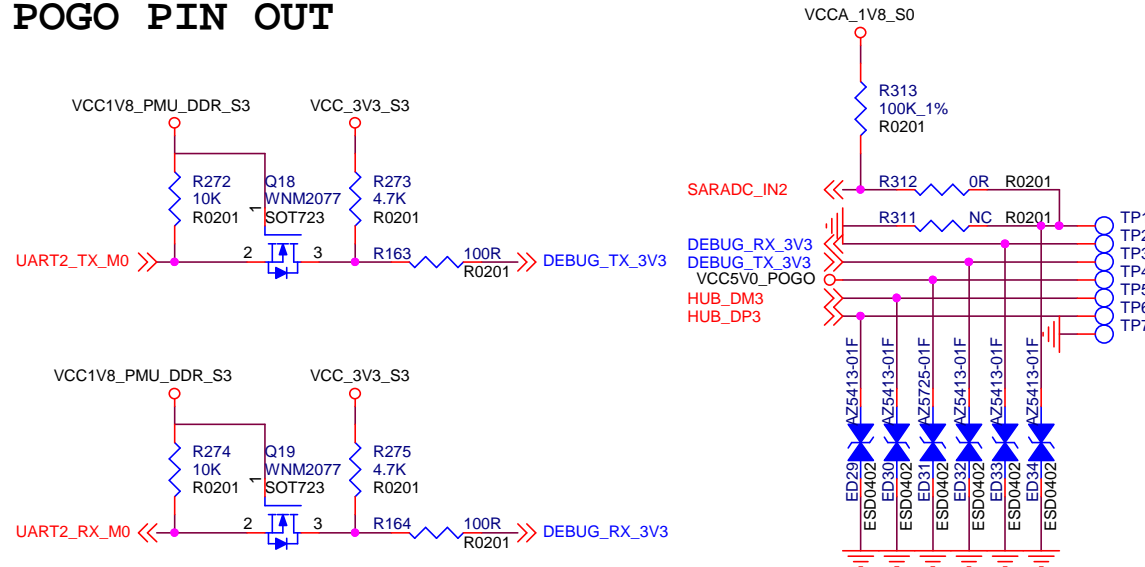
DMIC Array



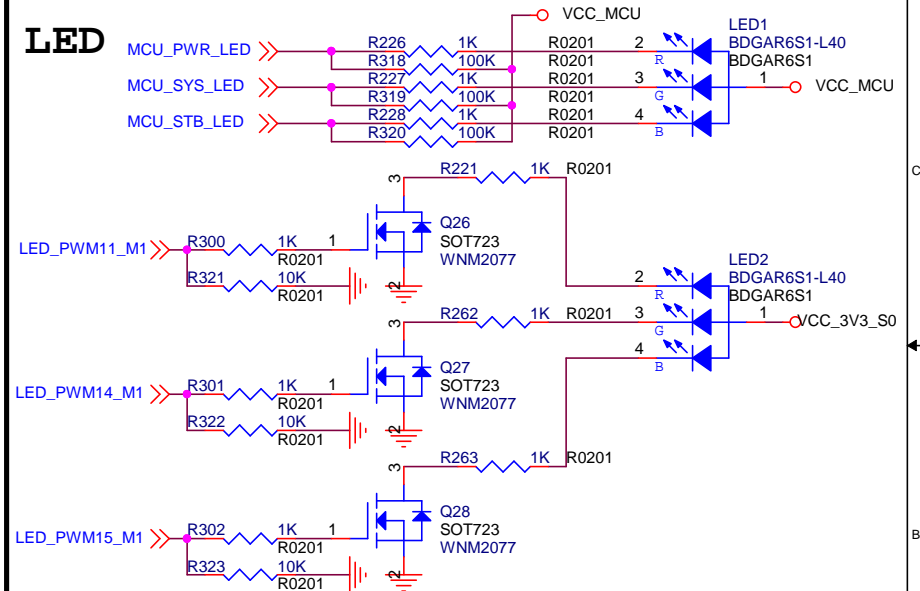
G-sensor



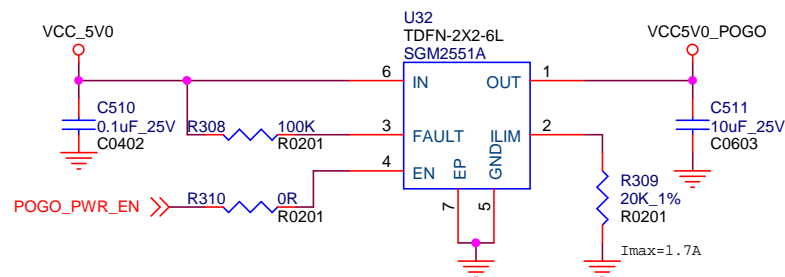
POGO PIN OUT



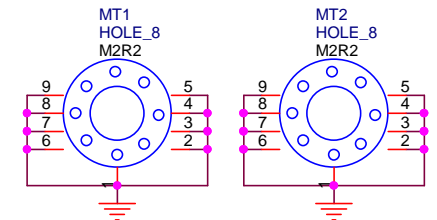
LED



POGO PIN PWR

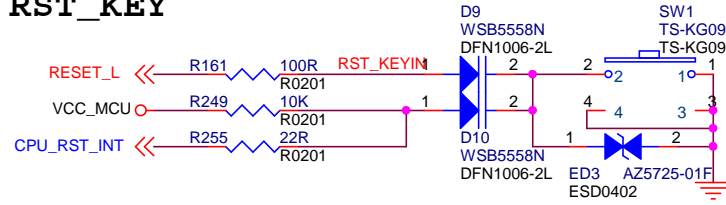


Mouting Holes

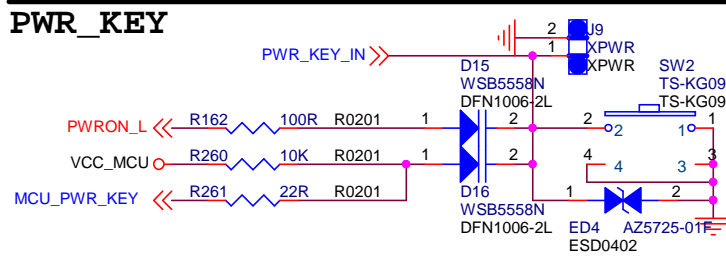


Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	DMIC/Sensor/DEBUG/LED		
Date:	Thursday, December 15, 2022	Rev:	V12
Designed_by:	Totti	Sheet:	21

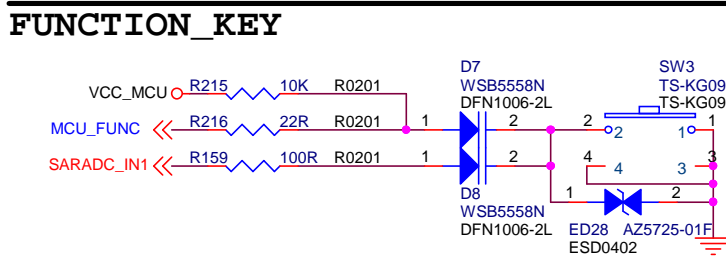
RST_KEY



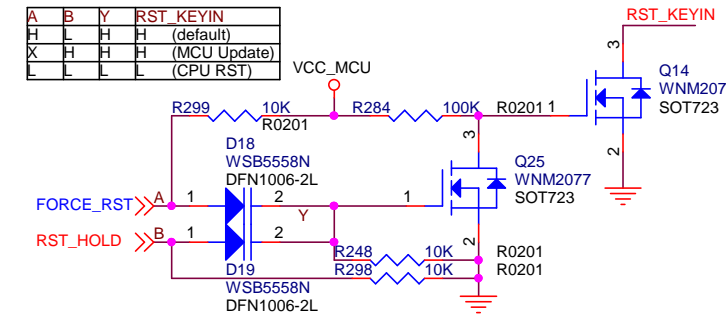
PWR_KEY



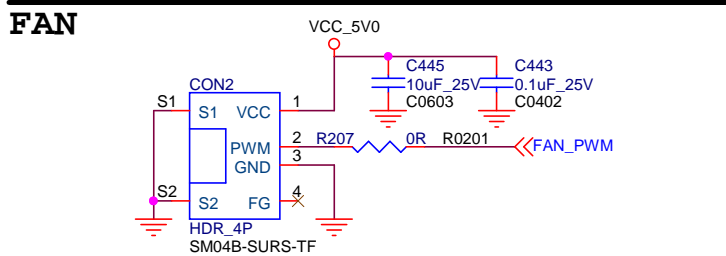
FUNCTION_KEY



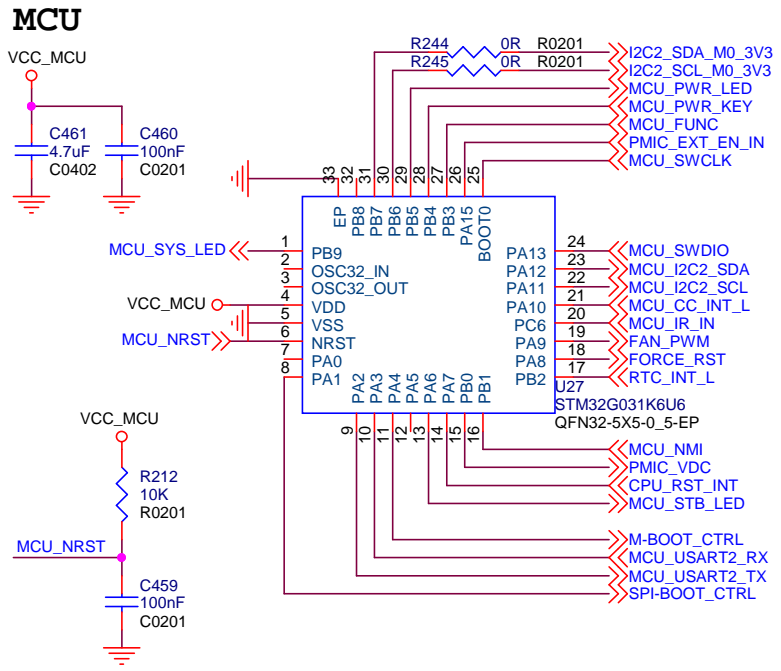
CPU_RST_CTRL



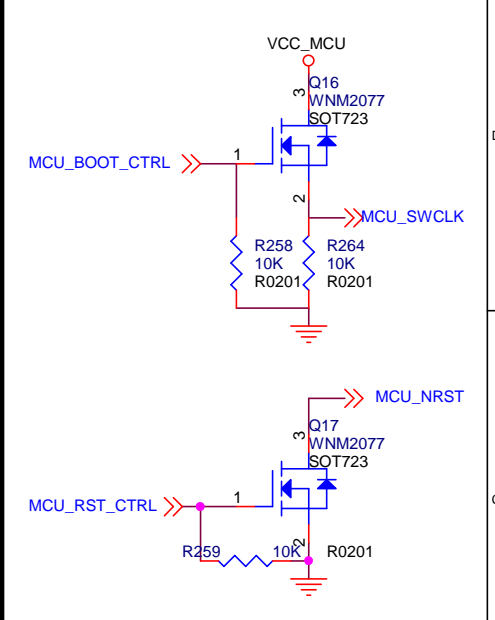
FAN



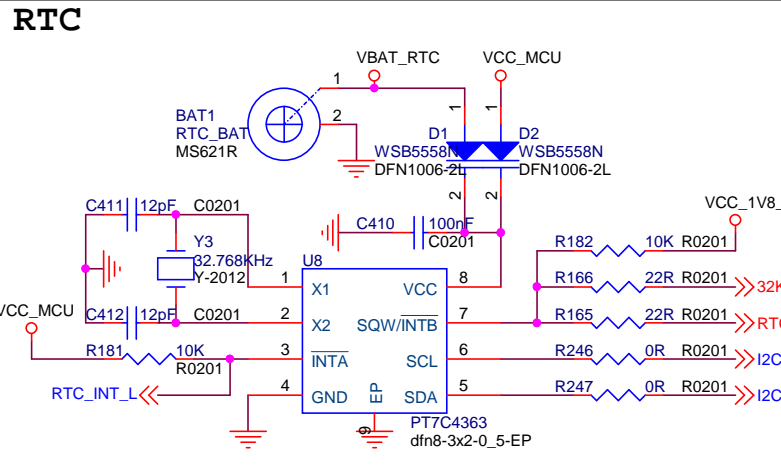
MCU



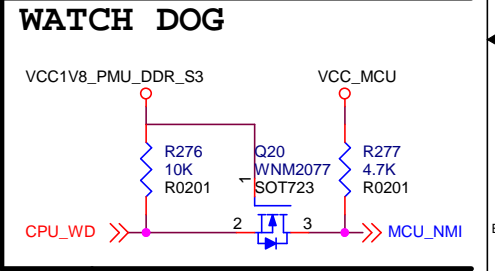
MCU BOOT CTRL



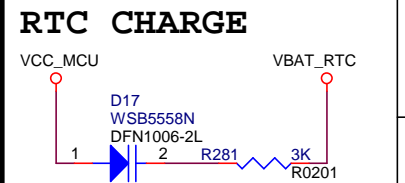
RTC



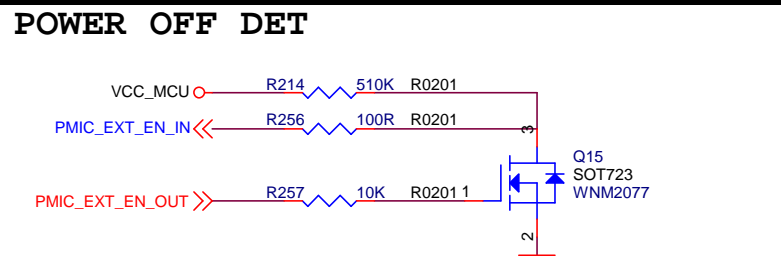
WATCH DOG



RTC CHARGE



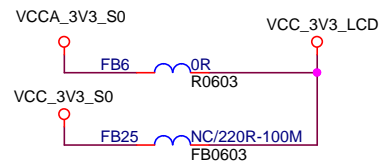
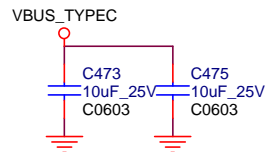
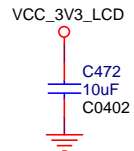
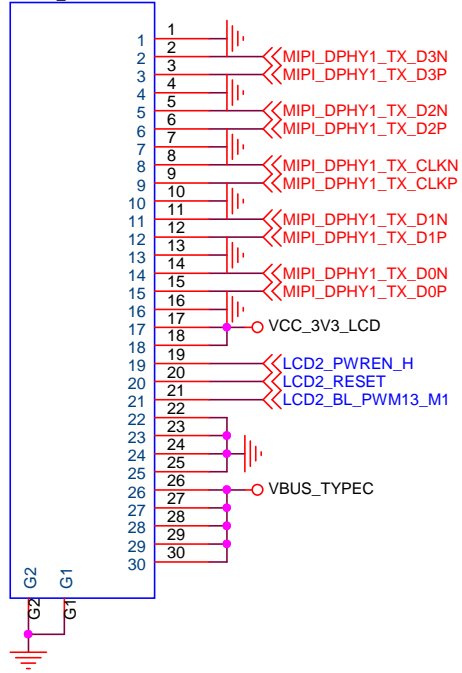
POWER OFF DET



Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	MCU/RTC/KEY/FAN		
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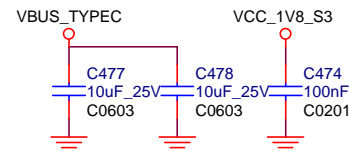
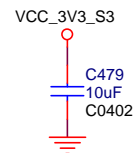
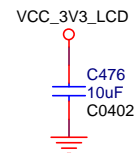
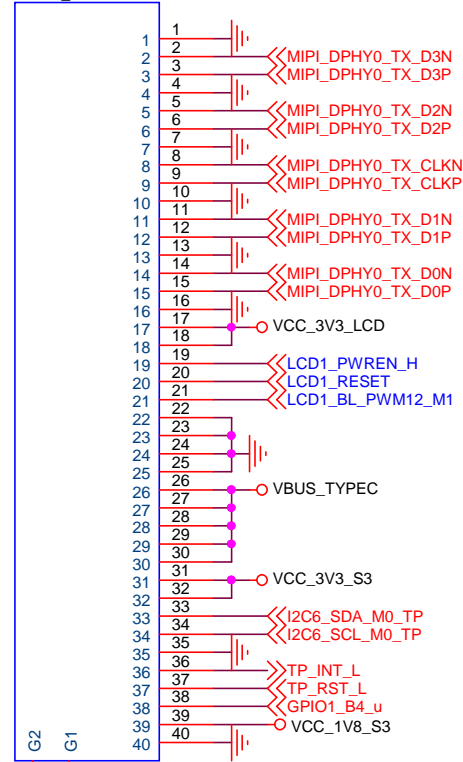
DSI 2

CON7
FH34SRJ-30S
FPC-0_5-30P



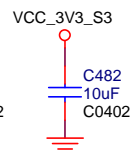
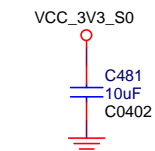
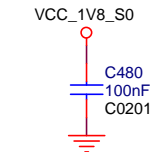
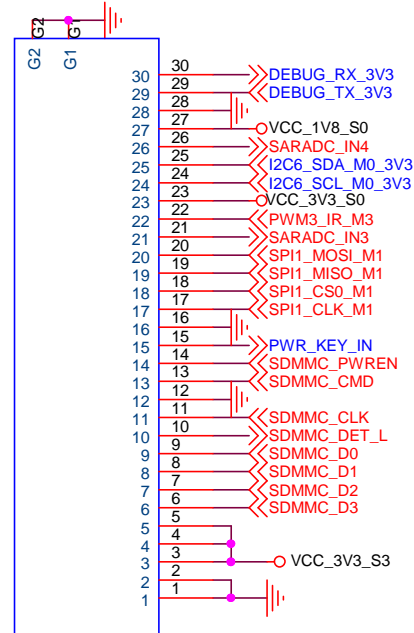
DSI 1

CON4
FH34SRJ-40S
FPC-0_5-40P



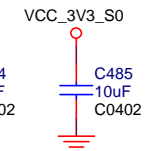
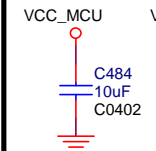
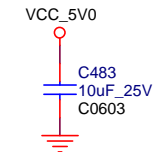
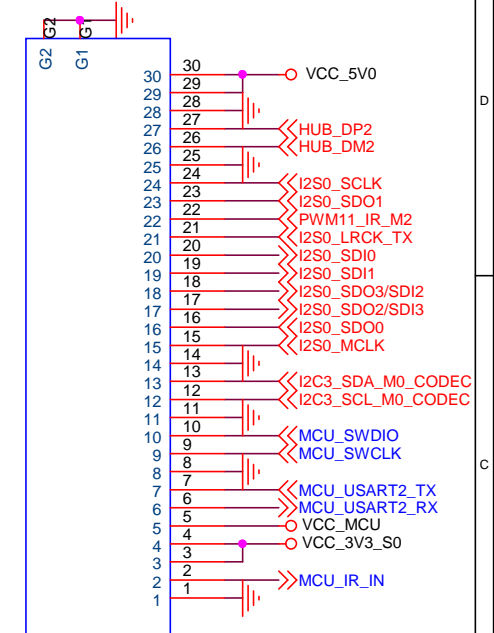
EXTIO 1

CON5
FH34SRJ-30S
FPC-0_5-30P



EXTIO 2

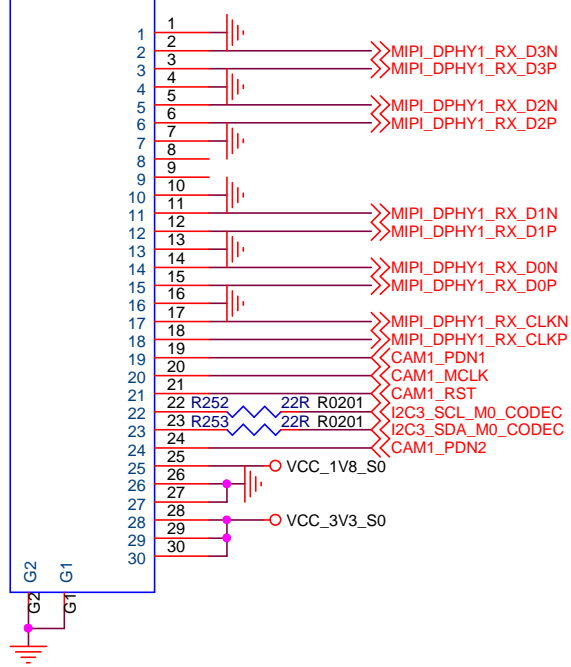
CON6
FH34SRJ-30S
FPC-0_5-30P



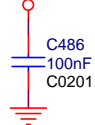
Shenzhen Wesion Technology Co., Ltd.			
Project:	Edge2		
File:	EXT IO/MIPI LCD		
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Camera1

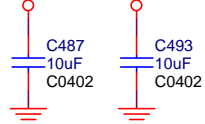
CON9
FH34SRJ-30S
FPC-0_5-30P



VCC_1V8_S0

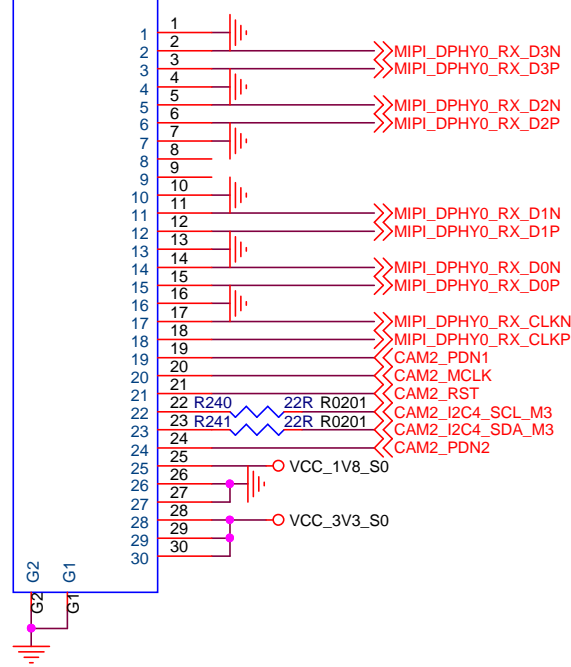


VCC_3V3_S0 VCC_3V3_S0

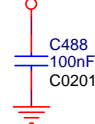


Camera2

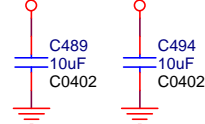
CON8
FH34SRJ-30S
FPC-0_5-30P



VCC_1V8_S0

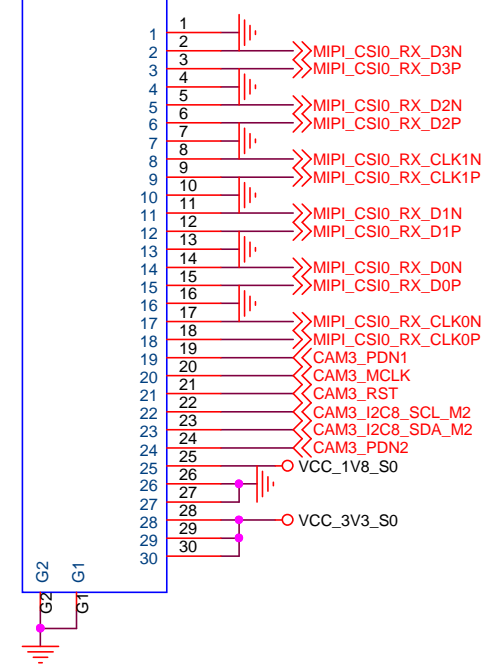


VCC_3V3_S0 VCC_3V3_S0

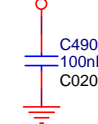


Camera3

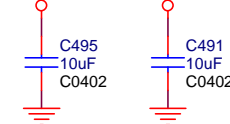
CON3
FH34SRJ-30S
FPC-0_5-30P



VCC_1V8_S0



VCC_3V3_S0 VCC_3V3_S0



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Project:	Edge2		
File:	CAMERA_Connector		
Date:	Thursday, November 17, 2022	Rev:	V12
Designed_by:	Totti	Sheet:	24