Rockchip
RK3576
Technical Reference Manual
(Part 2)

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Revision History

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2024-06-24	1.2	Reorganize the order of chapters; Update the following chapters: RGA, VOP, DPTX Controller, HDMI TX Controller, HDMI/Edp Combo PHY, UFS
2024-04-02	1.1	Update the PWM, VOP, RGA chapters
2024-03-18	1.0	Initial Release

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Chapter 1 JPEG

1.1 Overview

The JPEG codec provides a hardware-accelerated solution for processing JPEG-compressed images, including a decoder and an encoder. The capabilities of the codec are listed below:

- JPEG encoder
  - Supports Baseline(DCT sequential)
  - Supports JPEG file interchange format (JFIF) 1.02
  - Supports image size is from 16x16 to 65520x65520
  - Supports YUV400/YUV420/YUV422/YUV444
  - Supports low delay input and low delay output
  - Supports Ultra fast encoder
  - Supports enhance link mode
  - Supports ecs split
- JPEG decoder
  - Supports Baseline(DCT sequential)
  - Supports JPEG file interchange format (JFIF) 1.02
  - Supports image size is from 48x48 to 65520x65520
  - Supports YUV400/YUV420/YUV422/YUV440/YUV411/YUV444
  - Supports low delay input and low delay output
  - Supports Ultra fast decoder
  - Supports enhance link mode

1.2 Block Diagram

As shown in the figures below, the CPU can access the JPEC codec register bank via the AHB bus. Bit stream and other necessary data stored in DDR are fed into the codec via the AXI read channel, and when the coding processing is complete, the output is written to the designated DDR region via the AXI write channel.

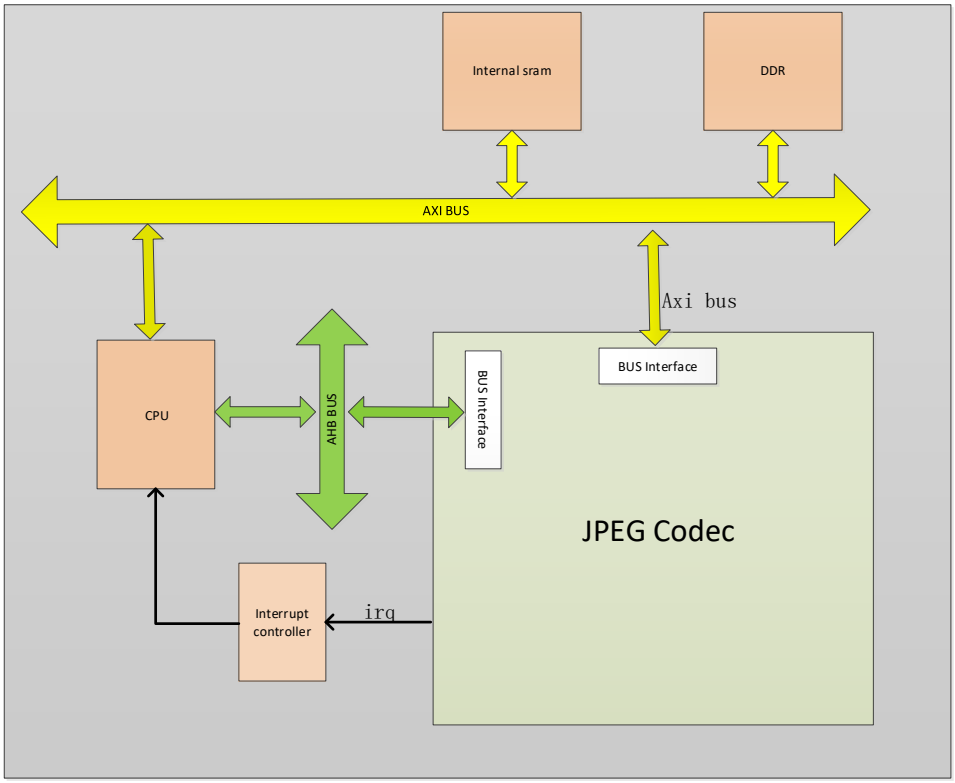


Fig. 1-1 JPEG codec Block Diagram

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1.3 Function Description

1.3.1 MMU

The MMU divides memory into 4KB pages, where each page can be individually configured. For each page the following parameters are specified:

- Address translation of virtual memory, this enables the processor to work using address that differ from the physical address in the memory system.
- The permitted types of accesses to that page. Each page can permit read, write, both, or none.

The MMU use 2-level page table structure:

1. The first level, the page directory consists of 1024 directory table entries (DTEs), each pointing to a page table.
2. The second level, the page table consists of 1024 page table entries (PTEs), each pointing to a page in memory.

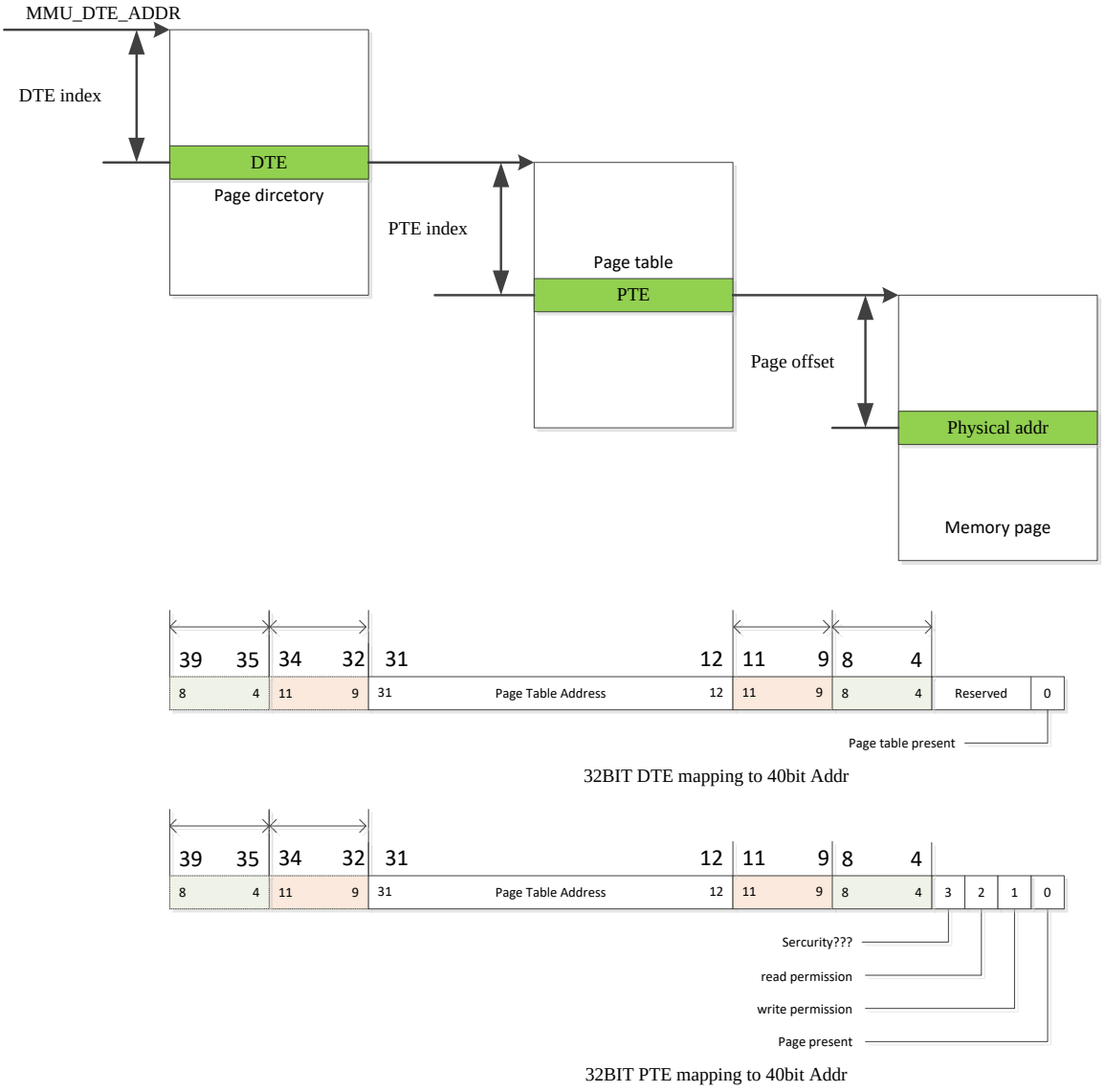


Fig. 1-2 structure of two-level page table

1.3.2 JPEG Decoder Feature

JPEG features supported by decoder are as shown in Table 1-1 JPEG features.

Table 1-1 JPEG features

Feature	Decoder support
Input data format	JFIF file format 1.02

Feature	Decoder support
	YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
Decoding scheme	frame by frame
Output data format	YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar, tile4x4
Supported image size	48x48 to 65520x65520 Step size 8 pixels
Maximum frame rate	Up to 240 million pixels pre second
Thumbnail decoding	JPEG compressed thumbnails supported
Restart marker frequency decoding	Supported
MJPEG	Supported
Error detection	Supported

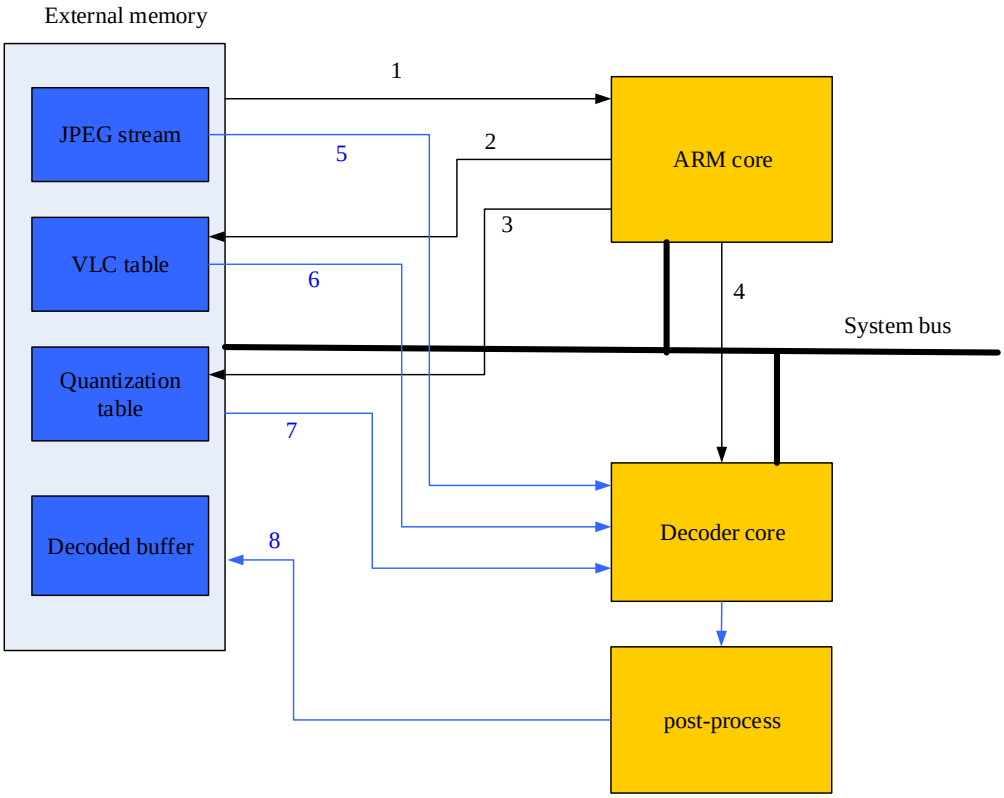


Fig. 1-3 The dataflow of JPEG decoder and post-processor

The data flow of JPEG decoder is as Fig. 1-8 shown. The decoder software starts decoding the picture by parsing the stream headers (1) and then writes the following items to external memory:
VLC tables (2)
Quantization tables (3)
Last step for the software is to write the hardware control registers and to enable the hardware (4). After starting hardware, SW waits interrupt from HW.
Hardware decodes the picture by reading stream (5), VLC (6) and QP (7) tables. Hardware writes the decoded output picture memory one macro block at a time (8). When the picture has been fully decoded, or the hardware has run out of stream data, it gives an interrupt with a proper status flag and provides stream end address for software to continue and returns to initial state.
The follow image post-processor only support combined mode.

The features supported by Post-processor are as show in Table 1-2 Post-processor features.

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Table 1-2 Post-processor features

Feature	Post-processor support
Input data format	Any format generated by the decoder in combined mode YCbCr 4:2:0 semi-planar YCbCr 4:2:0 planar YCbYCr 4:2:2 YCrYCb 4:2:2 CbYCrY 4:2:2 CrYCbY 4:2:2
Post-processor scheme	Frame by frame. Post-processor handles the image macroblock by macroblock.
Input image source	Internal source
Output data format	YCbCr 4:2:0 semi-planar YCbCr 4:2:2 YCrYCb 4:2:2 CbYCrY 4:2:2 CrYCbY 4:2:2
Input image size	48x48 to 65520x65520 Step size 8 pixels
Output image size	16x16 to 65520x65520 Horizontal step size 1 Vertical step size 1
Image down-scaling	Proprietary averaging filter Arbitrary, integer scaling ratio separately for both dimensions 0/2/4/8 down-scaling ratio
Output picture	support raster or tile mode picture out luma 4x4 block tile

In pipe-line mode, the post-processor works together with the multi-format decoder. The PP will take its input directly from the decoder. The dataflow is as Fig. 1-4 show.

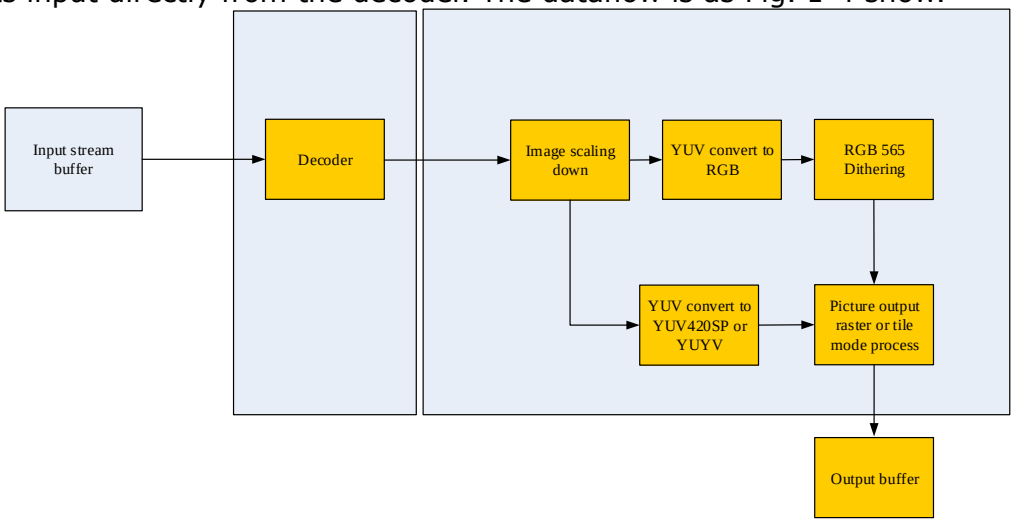


Fig. 1-4 Post-process Dataflow

1.3.3 JPEG Encoder Feature

The JPEG features supported by encoder are shown as follows.

Table 1-3 Video JPEG encoder feature

Feature	Encoder support
Input data format	YUV400 YUV420 planar

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Feature	Encoder support
	YUV420 semi-planar YUV422 YUV422 Interleaved YUYV422 UYVY422 YUV444 planar YUV444 semi-planar Tile4x4
Output data format	JFIF FILE format 1.02 YCbCr 4:0:0, 4:2:0, 4:2:2 and 4:4:4
Supported image size	16x16 to 65520x65520 Step size 8 pixels
Maximum Data rate	Up to 2.9 pixels per cycle

JPEG encoder supports 2 work modes: Register Configuration Mode and Link Table Mode.
In Register Configuration Mode, encoding a frame needs to be divided into three steps: Configure encoding parameters, start encoding, and then wait for encoding finish. Configuration register and interrupt response time will reduce the encoding speed, but software can adjust the configuration of the next frame in real time according to the encoding result of the previous frame.
In Link Table Mode, User can store several frames' configurations in DDR before encoding or add new frames to be encoded while VEPU is processing the previous one. This will save the time of interrupt response and register configuration and let VEPU and software process in parallel.

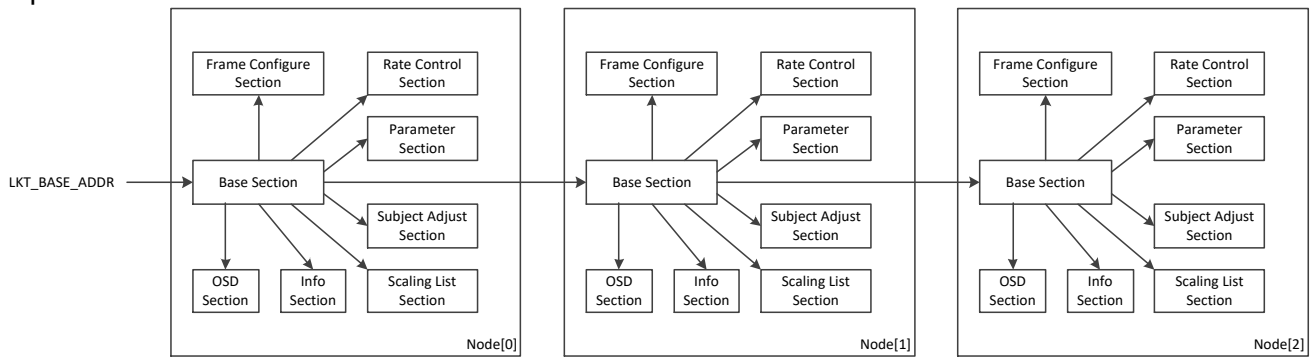


Fig. 1-2 VEPU Link Table Mode

All the configurations for each frame encoding are organized into a Node, and the configurations in each Node are classified into 6 sections:

- Base Section: Contains the information of other sections for current Node and Base Section of the next node, including whether it is valid and the starting address.
- Frame Configure Section: Contains the base frame configurations.
- Rate Control Section: Contains the configurations for Rate Control.
- Parameter Section: Contains the configurations of optional parameters.
- Subjective Adjust Section: Contains the configurations for subjective Quality Adjustment.
- Scaling List Section: Contains the configurations for User Defined HEVC/H.264 Scaling List and JPEG Quantization Table.
- Info Section: Contains the encoding information sent out by VEPU.

1.4 Register Description

1.4.1 Internal Address Mapping

The register address of JPEG codec is divided into three part:

- JPEG Decoder, whose offset is 0x0000
- JPEG Encoder, whose offset is 0x0800
- MMU, whose offset is 0x0F00

1.4.2 JPEG Decoder Registers Summary

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Name	Offset	Size	Reset Value	Description
rkdjpeg_swreg0_id	0x0000	W	0x00000000	ID register (read only)
rkdjpeg_swreg1_int	0x0004	W	0x00000000	interrupt and decoder enable register
rkdjpeg_swreg2_sys	0x0008	W	0x00000000	rk jpeg decoder system ctrl
rkdjpeg_swreg3_pic_size	0x000C	W	0x00000000	picture width and height size
rkdjpeg_swreg4_pic_format	0x0010	W	0x00000000	jpeg picture format configurate
rkdjpeg_swreg5_hor_virstride	0x0014	W	0x00000000	sw_y_hor_virstride and sw_uv_hor_virstride configurate
rkdjpeg_swreg6_y_virstride	0x0018	W	0x00000000	sw_y_virstride configurate
rkdjpeg_swreg7_table_len	0x001C	W	0x00000000	dequant table and huffman table length Description
rkdjpeg_swreg8_strm_len	0x0020	W	0x00000000	rk jpeg stream length and start byte info Description
rkdjpeg_swreg9_qtbl_base	0x0024	W	0x00000000	dequant table DDR base address Description
rkdjpeg_swreg10_htbl_mincode_base	0x0028	W	0x00000000	huffman mincode table DDR base address Description
rkdjpeg_swreg11_htbl_value_base	0x002C	W	0x00000000	huffman value table DDR base address Description
rkdjpeg_swreg12_strm_base	0x0030	W	0x00000000	stream data DDR base address Description
rkdjpeg_swreg13_dec_out_base	0x0034	W	0x00000000	rk jpeg recon decoder output data DDR address Description
rkdjpeg_swreg14_strm_error	0x0038	W	0x00000000	rk jpeg decoder stream error process
rkdjpeg_swreg15_strm_mask	0x003C	W	0x00000000	rk jpeg decoder special marker process
rkdjpeg_swreg16_clk_gate	0x0040	W	0x00000000	rk jpeg decoder clk gate enable
rkdjpeg_swreg21_low_delay_output	0x0044	W	0x00000000	rk JPEG decoder low delay threshold
rkdjpeg_swreg29_low_delay_output_status	0x0048	W	0x00000000	rk JPEG decoder low delay status
rkdjpeg_swreg30_perf_latency_ctrl0	0x0078	W	0x00000000	rk jpeg decoder axi performance ctrl0 Description
rkdjpeg_swreg31_perf_latency_ctrl1	0x007C	W	0x00000000	rk jpeg decoder axi performance ctrl1 Description
rkdjpeg_swreg32_dbg_mcu_pos	0x0080	W	0x00000000	rk jpeg debug register with mcu position Description
rkdjpeg_swreg33_dbg_error_info	0x0084	W	0x00000000	rk jpeg debug register with error info Description
rkdjpeg_swreg34_perf_rd_max_latency_num0	0x0088	W	0x00000000	rd_max_latency_num Description
rkdjpeg_swreg35_perf_rd_latency_samp_num	0x008C	W	0x00000000	rd_latency_thr_num Description
rkdjpeg_swreg36_perf_rd_latency_acc_sum	0x0090	W	0x00000000	rd_latency_acc_sum Description
rkdjpeg_swreg37_perf_rd_axi_total_byte	0x0094	W	0x00000000	perf_rd_axi_total_byte Description
rkdjpeg_swreg38_perf_wr_axi_total_byte	0x0098	W	0x00000000	perf_wr_axi_total_byte Description

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Name	Offset	Size	Reset Value	Description
rkdjpeg_swreg39_perf_working_cnt	0x009C	W	0x00000000	perf_working_cnt Description
rkdjpeg_swreg40_dbg_bus_sta	0x00A0	W	0x00000000	rk decoder bus status flag Description
rkdjpeg_swreg41_dbg_work_sta	0x00A4	W	0x00000000	rk decoder work status flag Description
rkdjpeg_swreg192_link_mode_irq	0x0300	W	0x00000000	interrupt in link mode
rkdjpeg_swreg193_cfg_start_addr	0x0304	W	0x00000000	the address of register data
rkdjpeg_swreg194_link_mode	0x0308	W	0x00000000	JPEG decoder link num gen mode
rkdjpeg_swreg195_config_done	0x030C	W	0x00000000	JPEG decoder link num cfg done cmd
rkdjpeg_swreg196_decodered_num	0x0310	W	0x00000000	the number of link completed by JPEG decoder
rkdjpeg_swreg197_dec_total_num	0x0314	W	0x00000000	the number of link cfg by JPEG decoder
rkdjpeg_swreg198_link_mode_en	0x0318	W	0x00000000	JPEG decoder link enable register
rkdjpeg_swreg200_link_num	0x0320	W	0x00000000	status of number in link mode
rkdjpeg_swreg201_link_info	0x0324	W	0x00000000	info of the current link cfg
rkdjpeg_swreg202_link_next_raddr	0x0328	W	0x00000000	next link cfg DDR base address
rkdjpeg_swreg203_link_wr_addr	0x032C	W	0x00000000	link status DDR base address Description

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

1.4.3 JPEG Decoder Detail Registers Description

rkdjpeg_swreg0_id

Address: Operational Base(0x27910000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	prod_num RKDJPEG version
15:9	RO	0x00	reserved
8	RO	0x0	bit_depth max bit_depth support 0: 8bits 1: 12bits
7:0	RO	0x00	minor_ver 0: default 1: 8k

rkdjpeg_swreg1_int

Address: Operational Base(0x27910000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	sw_lkt_data_error_sta when high, an error is found in link cfg data
22	RW	0x0	sw_lkt_error_stop_sta when high, an error is found and stop decoder in link mode

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Bit	Attr	Reset Value	Description
21	RW	0x0	sw_lkt_node_stop_sta when high, complete the response to force stop cmd in link mode
20	RW	0x0	sw_lkt_force_stop_sta when high, an task is finish and stop decoder in link mode
19	RW	0x0	sw_lkt_mode_int_sta when this bit is high, has decoded a link task with node_int enable
18	RW	0x0	sw_lkt_opertaion_error_sta when this bit is high, an error is found in link cmd opertaion
17	RW	0x0	sw_low_delay_out_sta when this bit is high, the output picture pixel line is big then sw_low_delay_output
16	RW	0x0	sw_care_strm_error_e use for sw_error_prc_mode=1 0:not care stream error,when sw_care_strm_error_e=0, sw_dec_error_sta will not valid, mmu will not be reset at frame end, link table mode will continue without care stream error, only active error info registers; 1:care stream error;
15	RW	0x0	sw_buf_empty_force_end_flag 0:invalid 1:valid buffer empty interrupt with stream real empty so should force hardware decoder current frame end
14	RW	0x0	sw_softreset_rdy when it is 1'b1, it says that softreset has been done
13	RW	0x0	sw_dec_buf_empty_sta buffer empty status, only when sw_buf_empty_e is 1'b1 , this bit is valid software should clean stream buffer empty state and set sw_buf_empty_reload_p enbale at the same time
12	RW	0x0	sw_dec_timeout_sta When high the decoder has been idling for too long. it will self reset the hardware.only when sw_dec_timeout_e is 1'b1, this bit is valid
11	RW	0x0	sw_dec_error_sta when high, an error is found in input data stream decoding.when sw_error_prc_mode is 1'b0, it will self reset the hardware, otherwise it will not
10	RW	0x0	sw_dec_bus_sta When this bit is high, there is error on the axi bus, it will self reset hardware
9	RW	0x0	sw_dec_rdy_sta when this bit is high, decoder has decoded a picture (the output module send out a frame rdy)
8	RW	0x0	sw_dec_irq when high, decoder requests an interrupt. sw_dec_irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0)
7	RW	0x0	sw_wait_reset_e the enable flag of wait software system to reset flag 0: hardware will auto reset when error occur 1: wait software process reset when error occur

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Bit	Attr	Reset Value	Description
6	RW	0x0	sw_dec_irq_raw the raw status of sw_dec_irq,SW should reset this bit after interrupt is handled
5	RW	0x0	sw_softrst_en_p softreset enable signal write 1 to soft reset, write 0 invalid puls register
4	RW	0x0	sw_buf_empty_reload_p buffer empty stream reload enable signal write 1 to reload stream data ready pulse register with hardware auto clean valid at next cycle before reload enable,strm_len register should be reset and start_of_type is zero sw_strm_base addr may be reset also. note:sw_error_prc_mode should be set to 1 when sw_buf_empty_e valid otherwise the hardware would be reset and not support buffer buffer empty reload
3	RW	0x0	sw_buf_empty_e buffer empty interrupt enable
2	RW	0x0	sw_dec_timeout_e If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture.
1	RW	0x0	sw_dec_irq_dis When hight, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt status
0	RW	0x0	sw_dec_e Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when the picture is decoded ready or bus error or time out interrupt is given for all decode format.

rkdjpeg_swreg2_sys

Address: Operational Base(0x27910000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:27	RW	0x0	sw_yuv_out_format jpeg decoder yuv output transmit format 000:yuv out without transmit format 001:reserved 010:reserved 011:yuv2yuv420sp(not support yuv400 transmit to yuv420sp) 100:yuv2yuyv(only support yuv422 or yuv444, yuv444 should uv scaledown)
26	RW	0x0	sw_dec_out_sequence recon data out format when afbc off 0:raster sequence out 1:tile sequence out
25	RW	0x0	sw_fill_right_e When JPEG picture width pixels is not a multiple of 16 pixels. 0: not fill picture width to multiple of 16 pixels. 1: fill picture width to multiple of 16 pixels. HW must fill one block of zero pixel data to the right border of the picture.
24	RW	0x0	sw_fill_down_e When JPEG picture height pixels is not a multiple of 16 pixels. 0: not fill picture height to multiple of 16 pixels. 1: fill picture height to multiple of 16 pixels. HW must fill one block row of zero pixel data for the last block row of picture.

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Bit	Attr	Reset Value	Description
23:22	RO	0x0	reserved
21	RW	0x0	sw_allow_16x8_cp_flag 0: not allow 1:allow the configurate value is depend on vop work mode
20	RW	0x0	sw_fbc_e 0:disable 1:fbc enable
19:18	RO	0x0	reserved
17	RW	0x0	sw_force_softreset_valid when sw_force_softreset_valid is 1'b1, sw_softrst_en will always be valid to the system no matter that whether the axi bus is idle; when sw_force_softreset_valid is 1'b0, sw_softrst_en will only be valid when the axi bus is idle.
16	RW	0x0	sw_timeout_mode timeout mode select 1'b0: TIMEOUT_CYCLES is {24{1'b1}}; 1'b1: TIMEOUT_CYCLES is {18{1'b1}};
15:14	RO	0x0	reserved
13:12	RW	0x0	sw_scaledown_mode jpeg decoder scaledown mode 00: not scaledown 01: 1/2 scaledown 10: 1/4 scaledown 11: 1/8 scaledown
11	RO	0x0	reserved
10	RW	0x0	sw_out_byte_swap may be used for 16 bits sequence output info 0 = no swapping of 8 bits data, 0x1234 1 = 8 bits data are swapped, 0x3412
9	RW	0x0	sw_out_cbcr_swap 1'b0: cb(u) is in the lower address, cr(v) is in the higher address 1'b1: cb(u) is in the higher address,cr(v) is in the lower address sw_in_cbcr_swap is the same with sw_out_cbcr_swap jpeg decoder only support for yuv4xxsp
8	RW	0x0	sw_out_swap64_e may be used for 128 bit environment 0 = no swapping of 64 bit words 1 = 64 bit data words are swapped
7	RW	0x0	sw_out_swap32_e may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
6	RW	0x0	sw_out_endian 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address
5	RW	0x0	sw_str_swap64_e may be used for 128 bit environment 0 = no swapping of 64 bit words 1 = 64 bit data words are swapped

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Bit	Attr	Reset Value	Description
4	RW	0x0	sw_str_swap32_e may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
3	RW	0x0	sw_str_endian 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address
2	RW	0x0	sw_in_swap64_e may be used for 128 bit environment 0 = no swapping of 64 bit words 1 = 64 bit data words are swapped
1	RW	0x0	sw_in_swap32_e may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
0	RW	0x0	sw_in_endian 0 = little endian 1 = big endian for little endian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address

rkdjpeg_swreg3_pic_size

Address: Operational Base(0x27910000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_pic_height_m1 Picture height in pixels unit minus1(should be mcu align by hardware)
15:0	RW	0x0000	sw_pic_width_m1 Picture width in pixels unit minus1(should be mcu align by hardware)

rkdjpeg_swreg4_pic_format

Address: Operational Base(0x27910000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dri_mcu_num_m1 Restart marker frequency. Tells the amount of coding units between restart markers Specifies the number of MCU in the restart. the number is minus1
15	RW	0x0	sw_dri_e define restart interval marker enable 0:restart interval marker disable 1:restart interval marker enable
14	RO	0x0	reserved
13:12	RW	0x0	sw_htables_sel Amount of Huffman tables in external memory: 0 = No Huffman tables. 1 = One Huffman table. Used when picture is single type 2 = Two Huffman tables. One for luminance and one for chominances 3 = Three Huffman tables. Each type (Lu, Cb, Cr) has own Huffman table
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	sw_qtables_sel Amount of Quantization tables in external memory: 0 = No quantization tables. 1 = One quantization table. Used when picture is single type 2 = Two quantization tables. One for luminance and one for chominances 3 = Three quantization tables. Each type (Lu, Cr, Cb) has own QP-table
7	RO	0x0	reserved
6:4	RW	0x0	sw_pixel_depth Picture luma pixel depth minus8. 0:8bits 4:12bits
3	RO	0x0	reserved
2:0	RW	0x0	sw_jpeg_mode Input picture sampling format: 0 = single type, MB 1 block (4:0:0) 1 = single type, MB 6 blocks (4:1:1) 2 = three types, MB 6 blocks (4:2:0) 3 = three types, MB 4 blocks (4:2:2) 4 = three types, MB 4 blocks (4:4:0) 5 = three types, MB 3 blocks (4:4:4)

rkdjpeg_swreg5_hor_virstride

Address: Operational Base(0x27910000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_uv_hor_virstride picture horizontal virtual stride (the unit is 128bit) the max is 65536x2/16 = 0x2000 suggest this register to configuration to even for advance DDR performance yuv444 tile mode ,uv_hor_virstride will use 16bits
15:0	RW	0x0000	sw_y_hor_virstride picture horizontal virtual stride (the unit is 128bit) the max is 65536x2/16 = 0x2000 suggest this register to configuration to even for advance DDR performance fbc mode: used for head virtual stride but rgb888 tile mode ,y_hor_virstride 16bits is not enough,will be use 17bits

rkdjpeg_swreg6_y_virstride

Address: Operational Base(0x27910000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_y_virstride Base address with 16 byte precision for decoder output luminance picture virtual stride
3:0	RO	0x0	reserved

rkdjpeg_swreg7_table_len

Address: Operational Base(0x27910000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24	RW	0x0	sw_y_hor_virstride_h picture horizontal virtual stride (the unit is 128bit) high bit when rgb888 tile mode use ,y_hor_virstride 16bits is not enought,will be use 17bits
23:22	RO	0x0	reserved
21:16	RW	0x00	sw_htbl_value_len Huffman value tables length(minus 1) with 16 byte align(128bits)
15:13	RO	0x0	reserved
12:8	RW	0x00	sw_htbl_mincode_len Huffman maxcode mincode and accaddr length(minus 1) with 16 byte align(128bits)
7:5	RO	0x0	reserved
4:0	RW	0x00	sw_qtbl_len quant table length(minus 1) with 16 byte align(128bits)

rkdjpeg_swreg8_strm_len

Address: Operational Base(0x27910000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_stream_len Amount of stream data 16 bytes(minus 1) in input buffer. If the given buffer size is not enough for finishing the picture the corresponding interrupt is given and new stream buffer base address and stream buffer size information should be given (assosiates with sw_strm_in_base).
3:0	RW	0x0	sw_strm_start_byte Input stream start byte offset: 0 = 0 type, of the base addr(16bytes) offset 1 = 1 type, of the base addr(16bytes) offset 2 = 2 type, of the base addr(16bytes) offset 3 = 3 type, of the base addr(16bytes) offset 4 = 4 type, of the base addr(16bytes) offset 5 = 5 type, of the base addr(16bytes) offset 6 = 6 type, of the base addr(16bytes) offset 7 = 7 type, of the base addr(16bytes) offset

rkdjpeg_swreg9_qtbl_base

Address: Operational Base(0x27910000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_qtbl_base Base address for standard dependent tables: AC,DC, QP tables64 byte align
5:0	RO	0x00	reserved

rkdjpeg_swreg10_htbl_mincode_base

Address: Operational Base(0x27910000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_htbl_mincode_base Base address for standard dependent tables: Huffman mincode and accaddr tables64 byte align
5:0	RO	0x00	reserved

rkdjpeg_swreg11_htbl_value_base

Address: Operational Base(0x27910000) + offset (0x002C)

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Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_htbl_value_base Base address for standard dependent tables: Huffman value tables64 byte align
5:0	RO	0x00	reserved

rkdjpeg_swreg12_strm_base

Address: Operational Base(0x27910000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_strm_in_base Stream start address with 16 byte precision. Actually, start byte number in stream_start_byte.
3:0	RO	0x0	reserved

rkdjpeg_swreg13_dec_out_base

Address: Operational Base(0x27910000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_dec_out_base Base address with 64 byte precision for decoder output luminance picture
5:0	RO	0x00	reserved

rkdjpeg_swreg14_strm_error

Address: Operational Base(0x27910000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	sw_hfm_force_stop 0: Huffman decoder error and continue. 1: Huffman decoder error force stop the decoder and wait soft reset. [12]: AXI stream buffer empty, and without detect EOI marker stop or not(0:support fill coefficient) [11]:Huffman get EOI marker without frame end stop or not(0:support fill coefficient) [10]:Huffman coefficient overflow detect and stop or not(0:support decode next coefficient) [9]:Huffman decode DRI stream stop or not, when MCU counter is not zero with DRI marker detect(0:support fill coefficient) [8]:Huffman decode DRI stream stop or not, when MCU counter is zero without DRI marker detect(0:support skip dummy stream)
15:10	RO	0x00	reserved
9	RW	0x0	sw_strm_dri_seq_err_mode 0:stream dri sequence error do not report error pos; 1:stream dri sequence error should be report error pos(if it's first error); note: error state should be report at all case
8:7	RW	0x0	sw_strm_other_mark_mode 00:stream detect other marker do skip process and not report error pos; 01: stream detect another marker stop the decoder and wait soft reset; 10:stream detect other marker do skip process 11:stream detect other marker do with normal stream note: error state should be report at all case

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Bit	Attr	Reset Value	Description
6:5	RW	0x0	sw_strm_ffff_err_mode 00:stream detect ffff marker do skip first 0xff process and not report error pos; 01: stream detect another marker stop the decoder and wait soft reset; 10:stream detect ffff marker do skip first 0xff process; 11:stream detect ffff marker do with normal stream at first 0xff; note: error state should be report at all case
4:3	RW	0x0	sw_strm_r1_err_mode stream detect second select marker process mode configuration 00: ignore second select marker. 01: force stop decoder when meet the second select marker 10: do skip process when meet the second select marker 11: do with normal stream when meet the second select marker
2:1	RW	0x0	sw_strm_r0_err_mode stream detect first select marker process mode configuration 00: ignore first select marker. 01: force stop decoder when meet the first select marker 10: do skip process when meet the first select marker 11: do with normal stream when meet the first select marker
0	RW	0x0	sw_error_prc_mode 1'b0: when there is any stream error, the hardware will stop the decoder and reset itself; 1'b1: when there is any stream error, the hardware will wait the end signal of recon and then reset request;

rkdjpeg_swreg15_strm_mask

Address: Operational Base(0x27910000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_strm_r1_mask mark the mask info 1:stream value[7-0] will mask and not care 0:stream value[7-0] shall match SW marker value
23:16	RW	0x00	sw_strm_r1_marker 0xffxx marker low 8bits value
15:8	RW	0x00	sw_strm_r0_mask mark the mask info 1:stream value[7-0] will mask and not care 0:stream value[7-0] shall match SW marker value
7:0	RW	0x00	sw_strm_r0_marker 0xffxx marker low 8bits value

rkdjpeg_swreg16_clk_gate

Address: Operational Base(0x27910000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	sw_dec_sram_gate_e 0 = Clock gate is not enable 1 = Clock gate is enable when busifd block is not working
6	RW	0x0	sw_post_prs_gate_e 0 = Clock gate is not enable 1 = Clock gate is enable when post process block is not working
5	RW	0x0	sw_busifd_gate_e 0 = Clock gate is not enable 1 = Clock gate is enable when busifd block is not working

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Bit	Attr	Reset Value	Description
4	RW	0x0	sw_dec_idct_gate_e 0 = Clock gate is not enable 1 = Clock gate is enable when IDCT block is not working
3	RW	0x0	sw_dec_izq_gate_e 0 = Clock gate is not enable 1 = Clock gate is enable when IZQ block is not working
2	RW	0x0	sw_dec_huffman_gate_e 0 = Clock gate is not enable 1 = Clock gate is enable when Huffman block is not working
1	RW	0x0	sw_dec_strm_gate_e 0 = Clock gate is not enable 1 = Clock gate is enable when stream block is not working
0	RW	0x0	sw_dec_clk_gate_e Decoder dynamic clock gating enable: 0 = Clock is running for all structures 1 = Clock is gated for decoder structures that are not used Note: Clock gating value can be changed only when decoder is disabled

rkdjpeg_swreg21_low_delay_output

Address: Operational Base(0x27910000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	sw_low_delay_output 0: disable low delay output other: ever sw_low_delay_output pixel line output , it will gen intr at swreg1_int.sw_low_delay_out_sta.

rkdjpeg_swreg29_low_delay_output_status

Address: Operational Base(0x27910000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	sw_low_delay_output_status output pixel line cnt

rkdjpeg_swreg30_perf_latency_ctrl0

Address: Operational Base(0x27910000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:8	RW	0x000	sw_rd_latency_thr rd channel latency threshold
7:4	RW	0x0	sw_rd_latency_id rd channel id for performance test
3	RW	0x0	sw_axi_cnt_type sw_axi_cnt_type 0:axi transfer num count 1:ddr align transfer num count
2	RW	0x0	sw_axi_perf_frm_type 1'b0: clear by frame end 1'b1: clear by software configuration
1	RW	0x0	sw_axi_perf_clr_e 1'b0: software clear disable 1'b1: software clear enalbe clear pulse

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Bit	Attr	Reset Value	Description
0	RW	0x0	sw_axi_perf_work_e 1'b0: disable 1'b1: enable

rkdjpeg_swreg31_perf_latency_ctrl1

Address: Operational Base(0x27910000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	sw_rd_total_bytes_mode 0:cal all id 1:cal sw_ar_count_id
11:8	RW	0x0	sw_aw_count_id sw_aw_count_id
7:4	RW	0x0	sw_ar_count_id sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type sw_aw_cnt_id_type 0:count all wr-channels 1:count sw_wr_cont_id wr-channel only
2	RW	0x0	sw_ar_cnt_id_type sw_ar_cnt_id_type 0:count all rd-channels 1:count sw_ar_cont_id rd-channel only
1:0	RW	0x0	sw_addr_align_type sw_addr_align_type 0:16 byte align 1:32byte align 2:64byte align 3:128byte align

rkdjpeg_swreg32_dbg_mcu_pos

Address: Operational Base(0x27910000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	mcu_pos_y Decoder mcu position at x coordinal with first error detect, only for read enable
15:0	RO	0x0000	mcu_pos_x Decoder mcu position at y coordinal with first error detect, only for read enable

rkdjpeg_swreg33_dbg_error_info

Address: Operational Base(0x27910000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	jpeg_first_error_idx jpeg decoder first error index 4'd0:stream_dri_seq_err_sta 4'd1:stream_r0_err_sta 4'd2:stream_r1_err_sta 4'd3:stream_ffff_err_sta 4'd4:stream_other_mark_err_sta 4'd8:huffman_mcu_cnt_l 4'd9:huffman_mcu_cnt_m 4'd10:huffman_eoi_without_end 4'd11:huffman_end_without_eoi

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Bit	Attr	Reset Value	Description
			4'd12:huffman_overflow 4'd13:huffman_buf_empty
15:14	RO	0x0	reserved
13	RW	0x0	huffman_buf_empty Decoder picture not complete, and not detect EOI with buffer empty 0:buffer not empty 1:buffer empty
12	RW	0x0	huffman_overflow Decoder Huffman coefficient overflow
11	RW	0x0	huffman_end_without_eoi Decoder Huffman frame end without get EOI marker
10	RW	0x0	huffman_eoi_without_end Decoder Huffman get EOI marker without frame end
9	RW	0x0	huffman_mcu_cnt_m Decoder dri stream mcu count more, mcu count 0 without restart mark
8	RW	0x0	huffman_mcu_cnt_l Decoder dri stream mcu count low, restart mark is coming without mcu count 0
7:5	RO	0x0	reserved
4	RW	0x0	stream_other_mark_err_sta Decoder stream other marker error detect flag, only for read enable 0:other marker not detect 1:other marker detect
3	RW	0x0	stream_ffff_err_sta Decoder stream ffff error detect flag, only for read enable 0:other marker not detect 1:other marker detect
2	RW	0x0	stream_r1_err_sta Decoder stream special marker1 error detect flag, only for read enable 0:special marker1 not detect 1:special marker1 detect
1	RW	0x0	stream_r0_err_sta Decoder stream special marker0 error detect flag, only for read enable 0:special marker0 not detect 1:special marker0 detect
0	RW	0x0	stream_dri_seq_err_sta 0:stream DRI at normal sequence 1:stream error with DRI not at normal sequence

rkdjpeg_swreg34_perf_rd_max_latency_num0

Address: Operational Base(0x27910000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	rd_max_latency_num_ch0 rd_max_latency_num_ch0

rkdjpeg_swreg35_perf_rd_latency_samp_num

Address: Operational Base(0x27910000) + offset (0x008C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_latency_thr_num_ch0 rd_latency_thr_num_ch0

rkdjpeg_swreg36_perf_rd_latency_acc_sum

Address: Operational Base(0x27910000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_latency_acc_sum rd_latency_acc_sum

rkdjpeg_swreg37_perf_rd_axi_total_byte

Address: Operational Base(0x27910000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_rd_axi_total_byte perf_rd_axi_total_byte

rkdjpeg_swreg38_perf_wr_axi_total_byte

Address: Operational Base(0x27910000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_wr_axi_total_byte perf_wr_axi_total_byte

rkdjpeg_swreg39_perf_working_cnt

Address: Operational Base(0x27910000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_working_cnt perf_working_cnt

rkdjpeg_swreg40_dbg_bus_sta

Address: Operational Base(0x27910000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RO	0x00000	bus_status_flag debug info of JPEG decoder bus channel

rkdjpeg_swreg41_dbg_work_sta

Address: Operational Base(0x27910000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	work_status_flag debug info or JPEG decoder inner

rkdjpeg_swreg192_link_mode_irq

Address: Operational Base(0x27910000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	sw_link_softreset_rdy when it is 1'b1, it says that softreset has been done
9	RW	0x0	rkvdec_irq_raw link interrupt status
8	RW	0x0	link_table_irq when high, decoder requests an interrupt. link table irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0)
7:3	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	sw_error_irq_dis 0: if there are any error ,not matter sw_dec_irq_dis ,it will give an interrupt . 1: if it will give interrept ,it only according to sw_dec_irq_dis
1:0	RO	0x0	reserved

rkdjpeg_swreg193_cfg_start_addr

Address: Operational Base(0x27910000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	reg_cfg_addr it should be align to 32 byte
3:0	RO	0x0	reserved

rkdjpeg_swreg194_link_mode

Address: Operational Base(0x27910000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31	RW	0x0	link_mode 0: normal mode,the first to start link mode 1: add extra ready frame to decoder
30	RO	0x0	reserved
29:0	RW	0x00000000	pre_frame_num 1: config 1 frame

rkdjpeg_swreg195_config_done

Address: Operational Base(0x27910000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	W1C	0x0	config_done 1: sw_ltb_link_mode eq 0,it start link; sw_ltb_link_mode wq 1 ,it add link frame 2: force stop 3: contiue link

rkdjpeg_swreg196_decodered_num

Address: Operational Base(0x27910000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31	RW	0x0	decoder_error_flag 0:no error 1:error,you will need to see swreg1 to check error type
30	RO	0x0	reserved
29:0	RO	0x00000000	decoder_num the number of link completed by JPEG

rkdjpeg_swreg197_dec_total_num

Address: Operational Base(0x27910000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	dec_total_num the number of link cfg by software

rkdjpeg_swreg198_link_mode_en

Address: Operational Base(0x27910000) + offset (0x0318)

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Bit	Attr	Reset Value	Description
31:29	RW	0x0	link_table_current_state the status of link fsm
28	RW	0x0	stop_calc_flag 0:no stop 1:stop status in link mode
27:15	RO	0x0000	reserved
14	RW	0x0	sw_lkt_node_int_en 0:node int disable 1:node int enable, When the lkt_node_in in lkt cfg equals 1, it will generate sw_lkt_node_int_sta
13	RW	0x0	sw_lkt_node_stop_en 0:node stop disable 1:node stop enable, When the lkt_stop_flag in lkt cfg equals 1, it will generate sw_lkt_node_stop_sta
12	RW	0x0	sw_lkt_error_stop_en 0:link error stop disable 1:link error stop enable, When an error in lkt cfg is found, it will generate sw_lkt_error_stop_sta
11:8	RW	0x0	sw_core_id when lkt_code_id not ea sw_core_id,the curr link will not be decoder
7:5	RO	0x0	reserved
4	RW	0x0	sw_link_softrst_en_p link mode software force hardware self reset enable signal write 1 to soft reset, write 0 invalid puls register
3:1	RO	0x0	reserved
0	RW	0x0	link_mode_en when error see by hw,it will auto reset to 0

rkdjpeg_swreg200_link_num

Address: Operational Base(0x27910000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	ltb_cfg_load_num the num of cfg load by JPEG decoder in link mode
23:16	RW	0x00	ltb_node_int_num the num of node int in link mode
15:8	RO	0x00	sw_ltb_deced_num the num of cfg completed by JPEG decoder in link mode
7:0	RO	0x00	sw_ltb_cfg_total_num the num of cfg generated by JPEG decoder in link mode

rkdjpeg_swreg201_link_info

Address: Operational Base(0x27910000) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:6	RW	0x000	lkt_task_id lkt_task_id from curr link cfg
5	RW	0x0	lkt_node_int lkt_node_int from curr link cfg
4	RW	0x0	lkt_stop_flag lkt_stop_flag from curr link cfg
3:0	RW	0x0	lkt_core_id curr link cfg core id

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rkdjpeg_swreg202_link_next_raddr

Address: Operational Base(0x27910000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	link_next_raddr next link cfg read addr

rkdjpeg_swreg203_link_wr_addr

Address: Operational Base(0x27910000) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	link_wr_addr curr frame end state write address

1.4.4 JPEG Encoder Registers Summary

Name	Offset	Size	Reset Value	Description
RKEJPEG_VERSION	0x0000	W	0x72010000	Version Register
RKEJPEG_ENC_STRT	0x0004	W	0x00000000	Start Command
RKEJPEG_INT_EN	0x0010	W	0x00000000	Interrupt Enable
RKEJPEG_INT_MSK	0x0014	W	0x00000000	Interrupt Mask
RKEJPEG_INT_CLR	0x0018	W	0x00000000	Interrupt Clear
RKEJPEG_INT_STATUS	0x001C	W	0x00000000	Interrupt State
RKEJPEG_CRU_CTRL	0x0020	W	0x00000000	CLOCK & RST CTRL
RKEJPEG_LKT_BASE_ADDR	0x0024	W	0x00000000	Link Table Base Address.
RKEJPEG_NODE_OCFG	0x0028	W	0x00000000	Link Table Node Operation Configuration
RKEJPEG_WDG_JPEG	0x002C	W	0x00000000	timetout threshold
RKEJPEG_LOW_DELAY_ECS_OCFG	0x0034	W	0x00000000	low delay ecs Operation Configuration
RKEJPEG_LOW_DELAY_PACKET_OCFG	0x0038	W	0x00000000	low delay packet Operation Configuration
RKEJPEG_ADR_QTBL_JPEG	0x0040	W	0x00000000	Address of JPEG TQBL Buffer
RKEJPEG_ADR_BSBT_JPEG	0x0044	W	0x00000000	Top Address of JPEG Bit Stream Buffer
RKEJPEG_ADR_BSBB_JPEG	0x0048	W	0x00000000	Bottom Address of JPEG Bit Stream Buffer
RKEJPEG_ADR_BSBR_JPEG	0x004C	W	0x00000000	Read Address of JPEG Bit Stream Buffer
RKEJPEG_ADR_BSBS_JPEG	0x0050	W	0x00000000	Start Address of JPEG Bit Stream Buffer
RKEJPEG_ADR_ECS_LEN	0x0054	W	0x00000000	Base address of the ECS len Buffer
RKEJPEG_ADR_SRC0_JPEG	0x0058	W	0x00000000	Base address of the 1st storage area for video source Buffer
RKEJPEG_ADR_SRC1_JPEG	0x005C	W	0x00000000	Base address of the 2nd storage area for video source Buffer
RKEJPEG_ADR_SRC2_JPEG	0x0060	W	0x00000000	Base address of the 3rd storage area for video source Buffer
RKEJPEG_AXI_PREF_CTRL0	0x0068	W	0x00000000	rk jpeg encoder axi performance ctrl0 Description
RKEJPEG_AXI_PERF_CTRL1	0x006C	W	0x00000000	rk jpeg encoder axi performance ctrl1 Description
RKEJPEG_ENC_RSL_JPEG	0x0074	W	0x00000000	pic size
RKEJPEG_SRC_FILL_JPEG	0x0078	W	0x00000000	JPEG source filling pixels for align.
RKEJPEG_SRC_FMT_JPEG	0x0080	W	0x00000000	JPEG source format

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Name	Offset	Size	Reset Value	Description
RKEJPEG_PIC_OFST_JPEG	0x0084	W	0x00000000	Encoding picture offset
RKEJPEG_SRC_STRD0_JPEG	0x0088	W	0x00000000	JPEG source stride0
RKEJPEG_SRC_STRD1_JPEG	0x008C	W	0x00000000	JPEG source stride1
RKEJPEG_JPEG_BASE_CFG	0x0090	W	0x00000000	jpeg common config
RKEJPEG_BSP_SIZE_JPEG	0x0094	W	0x00000000	low delay pack size config
RKEJPEG_UVC_CFG_JPEG	0x0098	W	0x00000000	bit stream ouput padding config
RKEJPEG_JPEG_Y_CFG	0x009C	W	0x00000000	Y Quantify rounding
RKEJPEG_JPEG_U_CFG	0x00A0	W	0x00000000	U Quantify rounding
RKEJPEG_JPEG_V_CFG	0x00A4	W	0x00000000	V Quantify rounding
RKEJPEG_DBUS_ENDN	0x00A8	W	0x00000000	Data Bus Endian
RKEJPEG_ST_BSL_L32_JPEG	0x00C0	W	0x00000000	Low 32bits of bit stream length for current frame.
RKEJPEG_ST_BSL_H32_JPEG	0x00C4	W	0x00000000	High 32bits of bit stream length for current frame.
RKEJPEG_ST_VSP_VALUE0	0x00C8	W	0x00000000	Y & U source range
RKEJPEG_ST_VSP_V_VALUE_AND_ECS_NUM	0x00CC	W	0x00000000	v source range and total_ecs_num_minus
RKEJPEG_ST_PERF_RD_MAX_LATENCY_NUM0	0x00D0	W	0x00000000	rd_max_latency_num Description
RKEJPEG_ST_PERF_RD_LATENCY_SAMP_NUM	0x00D4	W	0x00000000	rd_latency_thr_num Description
RKEJPEG_ST_PERF_RD_LATENCY_ACC_SUM_	0x00D8	W	0x00000000	rd_latency_acc_sum Description
RKEJPEG_ST_PERF_RD_AXI_TOTAL_BYTE	0x00DC	W	0x00000000	perf_rd_axi_total_byte Description
RKEJPEG_ST_PERF_WR_AXI_TOTAL_BYTE	0x00E0	W	0x00000000	perf_wr_axi_total_byte Description
RKEJPEG_ST_PERF_WROKING_CNT	0x00E4	W	0x00000000	perf_working_cnt Description
RKEJPEG_ST_WDG	0x00F0	W	0x00000000	VEPU watch dog status
RKEJPEG_ST_PPL_POS	0x00F4	W	0x00000000	Vsp mcu pos status
RKEJPEG_ST_CORE_POS	0x00F8	W	0x00000000	jpeg core mcu pos status
RKEJPEG_ST_BUS	0x00FC	W	0x00000000	bus status
RKEJPEG_DBG_PPL	0x0100	W	0x00000000	vsp dbg status
RKEJPEG_DBG_JPEG_CORE	0x0104	W	0x00000000	jpeg core dbg status
RKEJPEG_ST_ADR_JBSBW	0x010C	W	0x00000000	The bit stream write address status
RKEJPEG_ST_ADR_ECS_LEN	0x0110	W	0x00000000	Ecs len buffer write address status
RKEJPEG_ST_ADR_SRC0_JPEG	0x0114	W	0x00000000	the 1st storage area for video source Buffer read address status
RKEJPEG_ST_ADR_SRC1_JPEG	0x0118	W	0x00000000	the 2nd storage area for video source Buffer read address status
RKEJPEG_ST_ADR_SRC2_JPEG	0x011C	W	0x00000000	the 3rd storage area for video source Buffer read address status
RKEJPEG_ST_LOW_DELAY_PACKET_NUM	0x0120	W	0x00000000	low delay packet num status

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Name	Offset	Size	Reset Value	Description
RKEJPEG_ST_ECS_LEN_NUM	0x0124	W	0x00000000	low delay ecs_len num status
RKEJPEG_ST_ENC	0x0128	W	0x00000000	The jpeg common status
RKEJPEG_ST_LKT_NUM	0x012C	W	0x00000000	The lkt num
RKEJPEG_ST_LKT_INFO	0x0130	W	0x00000000	lkt cfg info
RKEJPEG_ST_LKT_NADR	0x0134	W	0x00000000	Next read addr for lkt_cfg
RKEJPEG_ST_LKT_WADDR	0x0138	W	0x00000000	The lkt state buff write addr

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

1.4.5 JPEG Encoder Detail Registers Description

RKEJPEG_VERSION

Address: Operational Base(0x27910800) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x72010000	RKEJPEG version verision

RKEJPEG_ENC_STRT

Address: Operational Base(0x27910800) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	WO	0x0	vepu_cmd VEPU command: 4'h0: N/A 4'h1: One-frame encoding by register configuration 4'h2: Multi-frame encoding start with link table mode 4'h3: Multi-frame encoding update (with link table mode) 4'h4: Link table encoding force pause 4'h5: contiue link table encoder when link table stop 4'h6: safe_clr 4'h7: force_clr
7:0	WO	0x00	lkt_num Number of new nodes added to Link Table.

RKEJPEG_INT_EN

Address: Operational Base(0x27910800) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	lkt_data_error_en link data error interrupt enable
11	RW	0x0	lkt_note_stp_en link table note stop interrupt enable
10	RW	0x0	lkt_fstp_en link cmd force pause interrupt enable
9	RW	0x0	lkt_estp_en link table encoding error stop interrupt enable.
8	RW	0x0	lkt_oerr_en link table opertaion error interrupt enable.
7	RW	0x0	wdg_en Watch dog(time out) interrupt enable.
6	RW	0x0	fenc_err_en bus error interrupt enable.
5	RW	0x0	vbsb_sct_en bit stream buffer write section interrupt enable.

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Bit	Attr	Reset Value	Description
4	RW	0x0	vbsb_oflw_en Bit stream buffer overflow enable.
3	RW	0x0	vslc_done_en One ecs of encoding finish interrupt enable.
2	RW	0x0	sclr_done_en safe reset interrupt enable.
1	RW	0x0	lkt_node_done_en link node done interrupt enable
0	RW	0x0	fenc_done_en One frame encoding finish interrupt enable.

RKEJPEG_INT_MSK

Address: Operational Base(0x27910800) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	lkt_data_error_msk link data error interrupt mask.
11	RW	0x0	lkt_note_stp_msk link table note stop interrupt mask
10	RW	0x0	lkt_fstp_msk link cmd force pause interrupt mask
9	RW	0x0	lkt_estp_msk link table encoding error stop interrupt mask.
8	RW	0x0	lkt_oerr_msk link table opertaion error interrupt mask.
7	RW	0x0	wdg_msk Watch dog(time out) interrupt mask.
6	RW	0x0	fenc_err_msk Frame encoding error interrupt mask.
5	RW	0x0	vbsb_sct_msk bit stream buffer write section interrupt mask.
4	RW	0x0	vbsb_oflw_msk Bit stream buffer overflow mask.
3	RW	0x0	vslc_done_msk One slice of video encoding finish interrupt mask.
2	RW	0x0	sclr_done_msk safe reset interrupt mask.
1	RW	0x0	lkt_node_done_msk link node done interrupt mask.
0	RW	0x0	fenc_done_msk One frame encoding finish interrupt mask.

RKEJPEG_INT_CLR

Address: Operational Base(0x27910800) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	lkt_data_error_clr link data error interrupt clear
11	WO	0x0	lkt_note_stp_clr link table note stop interrupt clear
10	WO	0x0	lkt_fstp_clr link cmd force pause interrupt clear
9	WO	0x0	lkt_estp_clr link table encoding error stop interrupt clear.

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Bit	Attr	Reset Value	Description
8	WO	0x0	lkt_oerr_clr link table opertaion error interrupt clear.
7	WO	0x0	Wdg_clr Watch dog(time out) interrupt clear.
6	WO	0x0	fenc_err_clr Frame encoding error interrupt clear.
5	WO	0x0	vbsb_sct_clr bit stream buffer write section interrupt clear.
4	WO	0x0	vbsb_oflw_clr Bit stream buffer overflow clear.
3	WO	0x0	vslc_done_clr One slice of video encoding finish interrupt clear.
2	WO	0x0	sclr_done_clr Safe clear finish interrupt clear.
1	WO	0x0	lkt_node_done_clr link table one node finish interrupt clear.
0	WO	0x0	fenc_done_clr One frame encoding finish interrupt clear.

RKEJPEG_INT_STATUS

Address: Operational Base(0x27910800) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	lkt_data_error_sta link data error interrupt status
11	RO	0x0	lkt_note_stp_sta link table note stop interrupt status
10	RO	0x0	lkt_fstp_sta link cmd force pause interrupt status
9	RO	0x0	lkt_estp_sta link table encoding error stop interrupt status.
8	RO	0x0	lkt_oerr_sta link table opertaion error interrupt status.
7	RO	0x0	Wdg_sta Watch dog(time out) interrupt status.
6	RO	0x0	fenc_err_sta Frame encoding error interrupt status.
5	RO	0x0	vbsb_sct_sta bit stream buffer write section interrupt status.
4	RO	0x0	vbsb_oflw_sta Bit stream buffer overflow status.
3	RO	0x0	vslc_done_sta One slice of video encoding finish interrupt status.
2	RO	0x0	sclr_done_sta Safe clear finish interrupt status.
1	RO	0x0	lkt_node_done_sta link table one node finish interrupt status.
0	RO	0x0	fenc_done_sta One frame encoding finish interrupt status.

RKEJPEG_CRU_CTRL

Address: Operational Base(0x27910800) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	cke auto clock gating enable.
1	RW	0x0	sram_ckg_en encoder sram auto clock gating enable.
0	RW	0x0	resetn_hw_en Encoder auto reset core clock domain when frame finished.

RKEJPEG_LKT_BASE_ADDR

Address: Operational Base(0x27910800) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	lkt_addr fst lkt cfg buffer addr 128byte align
6:0	RO	0x00	reserved

RKEJPEG_NODE_OCFG

Address: Operational Base(0x27910800) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x0	lktw_bus_edin Data swap for link table write channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
19:16	RW	0x0	lktr_bus_edin Data swap for link table read channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
15:6	RO	0x000	reserved
5	RW	0x0	lkt_node_stop_en the enable of lkt frame stop when the frame end
4	RW	0x0	lkt_err_stop_en the enable of lkt error stop next frame
3:0	RW	0x0	core_id Only the ejpeg with the same core ID can use this node.

RKEJPEG_WDG_JPEG

Address: Operational Base(0x27910800) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wdg_jpeg jpeg encoder timeout threshold. 32'h0: No time limit 32'hx: x*1 core clock cycles

RKEJPEG_LOW_DELAY_ECS_OCFG

Address: Operational Base(0x27910800) + offset (0x0034)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	WO	0x00000000	low_delay_ecs_ocfg read ecs num.

RKEJPEG_LOW_DELAY_PACKET_OCFG

Address: Operational Base(0x27910800) + offset (0x0038)

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Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	WO	0x00000000	low_delay_packet_ocfg read pack num.

RKEJPEG_ADR_QTBL_JPEG

Address: Operational Base(0x27910800) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	Qtbl_base_addr address of JPEG qtbl buffer,128byte align
6:0	RO	0x00	reserved

RKEJPEG_ADR_BSBT_JPEG

Address: Operational Base(0x27910800) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	bsbt_addr_jpeg High 25 bits top address of JPEG bit stream buffer.16byte align
3:0	RO	0x0	reserved

RKEJPEG_ADR_BSBB_JPEG

Address: Operational Base(0x27910800) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	bsbb_addr_jpeg bottom address of JPEG bit stream buffer.16byte align
3:0	RO	0x0	reserved

RKEJPEG_ADR_BSBR_JPEG

Address: Operational Base(0x27910800) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bsbr_addr_jpeg Read address of JPEG bit stream buffer

RKEJPEG_ADR_BSBS_JPEG

Address: Operational Base(0x27910800) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	adr_bsbs_jpeg Start address of JPEG bit stream buffer

RKEJPEG_ADR_ECS_LEN

Address: Operational Base(0x27910800) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	adr_ecs_len Start address of JPEG ecs len buffer .8byte align
2:0	RO	0x0	reserved

RKEJPEG_ADR_SRC0_JPEG

Address: Operational Base(0x27910800) + offset (0x0058)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	adr_src0_jpeg adr_src0_jpeg Base address of the 1st storage area for video source, based on byte. YUYV422 and UYUV422 have only one storage area, while adr_src0 is configured as the base address of video source frame buffer. YUV422/420 semi-planar have 2 storage area, while adr_src0 is configured as the base address of Y frame buffer. YUV422/420 planar have 3 storage area, while adr_src0 is configured as the base address of Y frame buffer. Note that if the video source is compressed by AFBC, adr_src0 is configured as the base address of header buffer, and it is 16-byte aligned.
3:0	RO	0x0	reserved

RKEJPEG_ADR_SRC1_JPEG

Address: Operational Base(0x27910800) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	adr_src1_jpeg Base address of the 2nd storage area for video source. YUYV422 and UYUV422 have only one storage area, while adr_src1 is reserved. YUV422/420 semi-planar have 2 storage area, while adr_src1 is configured as the base address of CHROMA frame buffer. YUV422/420 planar have 3 storage area, while adr_src1 is configured as the base address of U frame buffer. Note that if the video source is compressed by AFBC, adr_src1 is configured as the base address of body buffer.
3:0	RO	0x0	reserved

RKEJPEG_ADR_SRC2_JPEG

Address: Operational Base(0x27910800) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	adr_src2_jpeg Base address of V frame buffer when video source is uncompress and color format is YUV422/420 planar.
3:0	RO	0x0	reserved

RKEJPEG_AXI_PREF_CTRL0

Address: Operational Base(0x27910800) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:8	RW	0x000	sw_rd_latency_thr rd channel latency threshold
7:4	RW	0x0	sw_rd_latency_id rd channel id for performance test
3	RW	0x0	sw_axi_cnt_type sw_axi_cnt_type 0:axi transfer num count 1:ddr align transfer num count
2	RW	0x0	sw_axi_perf_frm_type 1'b0: clear by frame end 1'b1: clear by software configuration

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Bit	Attr	Reset Value	Description
1	RW	0x0	sw_axi_perf_clr_e 1'b0: software clear disable 1'b1: software clear enable clear pulse
0	RW	0x0	sw_axi_perf_work_e 1'b0: disable 1'b1: enable

RKEJPEG_AXI_PERF_CTRL1

Address: Operational Base(0x27910800) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	sw_rd_total_bytes_mode 0:cal all id 1:cal sw_ar_count_id
11:8	RW	0x0	sw_aw_count_id sw_aw_count_id
7:4	RW	0x0	sw_ar_count_id sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type sw_aw_cnt_id_type 0:count all wr-channels 1:count sw_wr_cont_id wr-channel only
2	RW	0x0	sw_ar_cnt_id_type sw_ar_cnt_id_type 0:count all rd-channels 1:count sw_ar_cont_id rd-channel only
1:0	RW	0x0	sw_addr_align_type sw_addr_align_type 0:16 byte align 1:32byte align 2:64byte align 3:128byte align

RKEJPEG_ENC_RSL_JPEG

Address: Operational Base(0x27910800) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	pic_hd8_m1_jpeg Ceil(encoding picture height/8) -1
15:13	RO	0x0	reserved
12:0	RW	0x0000	pic_wd8_m1_jpeg Ceil(encoding picture width/8) -1

RKEJPEG_SRC_FILL_JPEG

Address: Operational Base(0x27910800) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	pic_hfill_jpeg Filling pixels to keep (encoding) picture height is 16 pixels aligned
15:4	RO	0x000	reserved
3:0	RW	0x0	pic_wfill_jpeg Filling pixels to keep (encoding) picture width is 16 pixels aligned

RKEJPEG_SRC_FMT_JPEG

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Address: Operational Base(0x27910800) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_v_force_value when sw_chroma_force_en eq 1,then jpeg encoder v will force sw_v_force_value.
23:16	RW	0x00	sw_u_force_value when sw_chroma_force_en eq 1,then jpeg encoder u will force sw_u_force_value.
15	RW	0x0	src_mirr_jpeg 1-src mirror image
14:13	RO	0x0	reserved
12	RW	0x0	sw_chroma_force_en 1:the chroma for yuv422 or yuv420 will force to sw_u_force_value and sw_v_force_value.
11	RW	0x0	chroma_ds_mode_jpeg Downsampling mode of source chroma data.
10	RW	0x0	src_range_trns_sel_jpeg Source data scaling selection.
9	RW	0x0	src_range_trns_en_jpeg Source data scaling enable.
8	RO	0x0	reserved
7:6	RW	0x0	out_fmt_jpeg The color format of output from preprocess. 0-YUV400 1-YUV420 2-YUV422 3-YUV444
5:2	RW	0x0	src_cfmt_jpeg Video source color format. 4'h0: tile400 4'h1: tile420 4'h2: tile422 4'h3: tile444 4'h4: YUV422SP 4'h5: YUV422P 4'h6: YUV420SP 4'h7: YUV420P 4'h8: YUYV422 4'h9: UYVY422 4'ha: YUV400 4'hc: YUV444SP 4'hd: YUV444P Others: Reserved
1	RW	0x0	rbuv_swap_jpeg Swap the position of U and V for YUV422-SP, YUV420-SP, YUYV422 and UYUV422 format. 1'h0: YUYV or UYVY. 1'h1: YVYU or VYUY.
0	RO	0x0	reserved

RKEJPEG_PIC_OFST_JPEG

Address: Operational Base(0x27910800) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pic_ofst_y_jpeg Horizontal offset for encoding picture.

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	pic_ofst_x_jpeg Vertical offset for encoding picture.

RKEJPEG_SRC_STRD0_JPEG

Address: Operational Base(0x27910800) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	src_strd0_jpeg Video source stride0, based on pixel (byte). Note that if the video format is YUYV/UYVY, src_strd0 is the only one component stride, if the video format is YUV420P/YUV420SP/YUV422P/YUV422SP, src_strd0 is the LUMA component stride.

RKEJPEG_SRC_STRD1_JPEG

Address: Operational Base(0x27910800) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	src_strd1_jpeg CHROMA stride of video source, only for YUV format. Note that U and V stride must be the same when color format is YUV planar.

RKEJPEG_JPEG_BASE_CFG

Address: Operational Base(0x27910800) + offset (0x0090)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	jpeg_qtble_noload 0:load qtble cfg for the task encoder
29	RW	0x0	jpeg_pic_last_ecs 1:the task is the pic lastest task
28:26	RW	0x0	jpeg_start_rst_m the task first ecs rst_m
25	RW	0x0	jpeg_out_mode 1:Flush all the bit stream after each ecs finished.
24:16	RO	0x000	reserved
15:0	RW	0x0000	jpeg_ri JPEG syntax element.

RKEJPEG_BSP_SIZE_JPEG

Address: Operational Base(0x27910800) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bsp_size_jpeg Set the bit stream packet size of jpeg, 0 is disable.

RKEJPEG_UVC_CFG_JPEG

Address: Operational Base(0x27910800) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	uvc_skip_len_jpeg the number of partition filled with 00
23:12	RW	0x000	uvc_partition_len_jpeg not the first pariton length
11:0	RW	0x000	uvc_partition0_len_jpeg the first pariton length

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RKEJPEG_JPEG_Y_CFG

Address: Operational Base(0x27910800) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	jpeg_bias_y Y Quantify rounding

RKEJPEG_JPEG_U_CFG

Address: Operational Base(0x27910800) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	jpeg_bias_u U Quantify rounding

RKEJPEG_JPEG_V_CFG

Address: Operational Base(0x27910800) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	jpeg_bias_v V Quantify rounding

RKEJPEG_DBUS_ENDN

Address: Operational Base(0x27910800) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	sw_qtbl_edin Data swap for qtbl read channel [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
11:8	RW	0x0	ecs_len_edin Data swap for lkt state write channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
7:4	RW	0x0	vsl_bus_edin Data swap for video source loading channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
3:0	RW	0x0	jbsw_bus_edin Data swap for jpeg bit stream write channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits

RKEJPEG_ST_BSL_L32_JPEG

Address: Operational Base(0x27910800) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	jpeg_stream_byte_l32 Low 32 bits of JPEG stream length for byte.

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RKEJPEG_ST_BSL_H32_JPEG

Address: Operational Base(0x27910800) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	jpeg_stream_byte_h32 high 32 bits of JPEG stream length for byte

RKEJPEG_ST_VSP_VALUE0

Address: Operational Base(0x27910800) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	jpeg_y_min_value src luma min value
7:0	RO	0x00	jpeg_y_max_value src luma max value

RKEJPEG_ST_VSP_V_VALUE_AND_ECS_NUM

Address: Operational Base(0x27910800) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	jpeg_total_ecs_num_minus1 one task total ecs num minus 1
15:0	RO	0x0000	reserved

RKEJPEG_ST_PERF_RD_MAX_LATENCY_NUM0

Address: Operational Base(0x27910800) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	rd_max_latency_num_ch0 rd_max_latency_num_ch0

RKEJPEG_ST_PERF_RD_LATENCY_SAMP_NUM

Address: Operational Base(0x27910800) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_thr_num_ch0 rd_latency_thr_num_ch0

RKEJPEG_ST_PERF_RD_LATENCY_ACC_SUM

Address: Operational Base(0x27910800) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_acc_sum rd_latency_acc_sum

RKEJPEG_ST_PERF_RD_AXI_TOTAL_BYTE

Address: Operational Base(0x27910800) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	perf_rd_axi_total_byte perf_rd_axi_total_byte

RKEJPEG_ST_PERF_WR_AXI_TOTAL_BYTE

Address: Operational Base(0x27910800) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	perf_wr_axi_total_byte perf_wr_axi_total_byte

RKEJPEG_ST_PERF_WROKING_CNT

Address: Operational Base(0x27910800) + offset (0x00E4)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	perf_working_cnt perf_working_cnt

RKEJPEG_ST_WDG

Address: Operational Base(0x27910800) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	dma_work_flag 0: dma idle 1: dma work
2	RO	0x0	dma_wr_work_flag 0: dma write channel idle 1: dma write channel work
1	RO	0x0	jpeg_core_work_flag 0: JPEG_core idle 1: JPEG_core work
0	RO	0x0	vsp_work_flag 0: vsp idle 1: vsp work

RKEJPEG_ST_PPL_POS

Address: Operational Base(0x27910800) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_ppl_pos position of pp

RKEJPEG_ST_CORE_POS

Address: Operational Base(0x27910800) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_core_pos position of JPEG core

RKEJPEG_ST_BUS

Address: Operational Base(0x27910800) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	ejpeg_freeze_flag 1: JPEG encoder freeze,need continue cmd
29	RW	0x0	rkejpeg_wready wready of encoder axi channel
28	RW	0x0	rkejpeg_wvalid wvalid of encoder axi channel
27	RO	0x0	reserved
26	RW	0x0	rkejpeg_awvalid awvalid of encoder axi channel
25	RW	0x0	ejpeg_cfg_awready awready of encoder axi channel
24	RW	0x0	ejpeg_cfg_awvalid awvalid of encoder cfg axi channel
23	RW	0x0	ejpeg_strmd_wready wready of encoder stream axi channel
22	RW	0x0	ejpeg_strmd_wvalid wvalid of encoder stream axi channel
21	RW	0x0	ejpeg_strmd_awready awready of encoder stream axi channel

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Bit	Attr	Reset Value	Description
20	RW	0x0	ejpeg_strmd_awtype 0: stream axi channel 1: ecs length channel
19	RW	0x0	ejpeg_strmd_awvalid awvalid of encoder stream axi channel
18	RW	0x0	axi_wr_state_cs 0: encoder axi write channel idle 1: encoder axi write channel work
17	RW	0x0	rkejpeg_rready rready of encoder arb axi channel
16:15	RW	0x0	rkejpeg_rresp rresp of encoder arb axi channel
14:11	RW	0x0	rkejpeg_rid rid of encoder arb axi channel
10	RW	0x0	rkejpeg_ravlid ravlid of encoder arb axi channel
9	RW	0x0	rkejpeg_arready arready of encoder arb axi channel
8:7	RW	0x0	ejpeg_cfg_ar_cnt num of encoder axi arread but no receive data
6	RW	0x0	rkejpeg_arvalid arvalid of encoder arb axi channel
5	RW	0x0	ejpeg_vsp_arready arready of encoder vsp axi channel
4	RW	0x0	ejpeg_vsp_arvalid arvalid of encoder vsp axi channel
3	RW	0x0	ejpeg_cfg_arready arready of encoder cfg axi channel
2	RW	0x0	ejpeg_cfg_arvalid_type 1: qtbl 0: lkt
1	RW	0x0	ejpeg_cfg_arvalid arvalid of encoder cfg axi channel
0	RW	0x0	ejpeg_arready arready of encoder cfg axi channel

RKEJPEG_DBG_PPL

Address: Operational Base(0x27910800) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_debug_pp the debug info of pp

RKEJPEG_DBG_JPEG_CORE

Address: Operational Base(0x27910800) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_debug_core the debug info of core

RKEJPEG_ST_ADR_JBSBW

Address: Operational Base(0x27910800) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_adr_jbsbw bit stream buffer write address.

RKEJPEG_ST_ADR_ECS_LEN

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Address: Operational Base(0x27910800) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_adr_ecs_len ecs len buffer write address.

RKEJPEG_ST_ADR_SRC0_JPEG

Address: Operational Base(0x27910800) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_adr_src0_jpeg the 1st video source buffer read addr

RKEJPEG_ST_ADR_SRC1_JPEG

Address: Operational Base(0x27910800) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_adr_src1_jpeg the second video source buffer read addr

RKEJPEG_ST_ADR_SRC2_JPEG

Address: Operational Base(0x27910800) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_adr_src2_jpeg the third video source buffer read addr

RKEJPEG_ST_LOW_DELAY_PACKET_NUM

Address: Operational Base(0x27910800) + offset (0x0120)

Bit	Attr	Reset Value	Description
31	RO	0x0	bs_packet_lst The last bit stream packet of jpeg.
30:0	RO	0x00000000	bs_packet_num Number for slices has been encoded and not read out for JPEG(read num by write 0x38)

RKEJPEG_ST_ECS_LEN_NUM

Address: Operational Base(0x27910800) + offset (0x0124)

Bit	Attr	Reset Value	Description
31	RO	0x0	ecs_len_lst The last ecs len of jpeg
30:0	RO	0x00000000	ecs_len_num Num for the earlist encoded ecs which has not been read out for JPEG(read num by write 0x34)

RKEJPEG_ST_ENC

Address: Operational Base(0x27910800) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	st_bitstream_overflow_flag 1: bitsstream overflow
5	RO	0x0	lkt_mode_en 1: lkt mode

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Bit	Attr	Reset Value	Description
4:0	RO	0x00	jpeg_enc_state 0: idle 1: cru open 2: lkt cfg load 3: qtbl_cfg_load 4: enc 5: frame end 6: cru_close 7: lkt_error_stop 8: lkt_force_stop 9: lkt_node_stop

RKEJPEG_ST_LKT_NUM

Address: Operational Base(0x27910800) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lkt_cfg_load_num lkt cfg be loaded num
23:16	RO	0x00	lkt_int_num lkt mode gen node intr num
15:8	RO	0x00	lkt_done_num lkt encoder done num
7:0	RO	0x00	lkt_cfg_num drv config lkt cfg num

RKEJPEG_ST_LKT_INFO

Address: Operational Base(0x27910800) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:6	RO	0x000	lkt_task_id the task_id in curr lkt cfg
5	RO	0x0	lkt_node_int the node_int in curr lkt cfg
4	RO	0x0	lkt_stop_flag the stop flag in curr lkt cfg
3:0	RO	0x0	lkt_core_id the core id in curr lkt cfg

RKEJPEG_ST_LKT_NADR

Address: Operational Base(0x27910800) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lkt_cfg_next_addr next read addr for lkt_cfg

RKEJPEG_ST_LKT_WADDR

Address: Operational Base(0x27910800) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lkt_reg_wr_addr the lkt state buff write addr

1.4.6 JPEG MMU Registers Summary

Name	Offset	Size	Reset Value	Description
RKJPEG_MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table addressIt is only can be written when MMU state is disable or page fault or mmu enable stall state

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Name	Offset	Size	Reset Value	Description
RKJPEG_MMU_STATUS	0x0004	W	0x00000018	MMU status register
RKJPEG_MMU_COMMAND	0x0008	W	0x00000000	MMU command register
RKJPEG_MMU_PAGE_FAULT_ADDR	0x000C	W	0x00000000	MMU logical address of last page fault
RKJPEG_MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
RKJPEG_MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
RKJPEG_MMU_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
RKJPEG_MMU_INT_MASK	0x001C	W	0x00000000	MMU raw interrupt status register
RKJPEG_MMU_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register
RKJPEG_MMU_AUTO_GATING	0x0024	W	0x00000001	MMU auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

1.4.7 JPEG MMU Detail Registers Description

RKJPEG_MMU_DTE_ADDR

Address: Operational Base(0x27910F00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR mmu dte base addr , the address must be 4kb aligned

RKJPEG_MMU_STATUS

Address: Operational Base(0x27910F00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master reponsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 0 = Read 1 = Write
4	RO	0x1	REPLAY_BUFFER_EMPTY The MMU replay buffer is empty
3	RO	0x1	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled . The mode is enabled by command.
0	RO	0x0	PAGING_ENABLED Paging is enabled

RKJPEG_MMU_COMMAND

Address: Operational Base(0x27910F00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

RKJPEG_MMU_PAGE_FAULT_ADDR

Address: Operational Base(0x27910F00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR address of last page fault

RKJPEG_MMU_ZAP_ONE_LINE

Address: Operational Base(0x27910F00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE address to be invalidated from the page table cache

RKJPEG_MMU_INT_RAWSTAT

Address: Operational Base(0x27910F00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

RKJPEG_MMU_INT_CLEAR

Address: Operational Base(0x27910F00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	READ_BUS_ERROR read bus error
0	WO	0x0	PAGE_FAULT page fault

RKJPEG_MMU_INT_MASK

Address: Operational Base(0x27910F00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	READ_BUS_ERROR read bus error enable an interrupt source if the corresponding mask bit is set to 1
0	RW	0x0	PAGE_FAULT page fault enable an interrupt source if the corresponding mask bit is set to 1

RKJPEG_MMU_INT_STATUS

Address: Operational Base(0x27910F00) + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	READ_BUS_ERROR read bus error
0	RO	0x0	PAGE_FAULT page fault

RKJPEG_MMU_AUTO_GATING

Address: Operational Base(0x27910F00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	mmu_auto_gating when it is 1'b1, the mmu will auto gating it self

1.5 Application Notes

1.5.1 MMU Configuration Flow

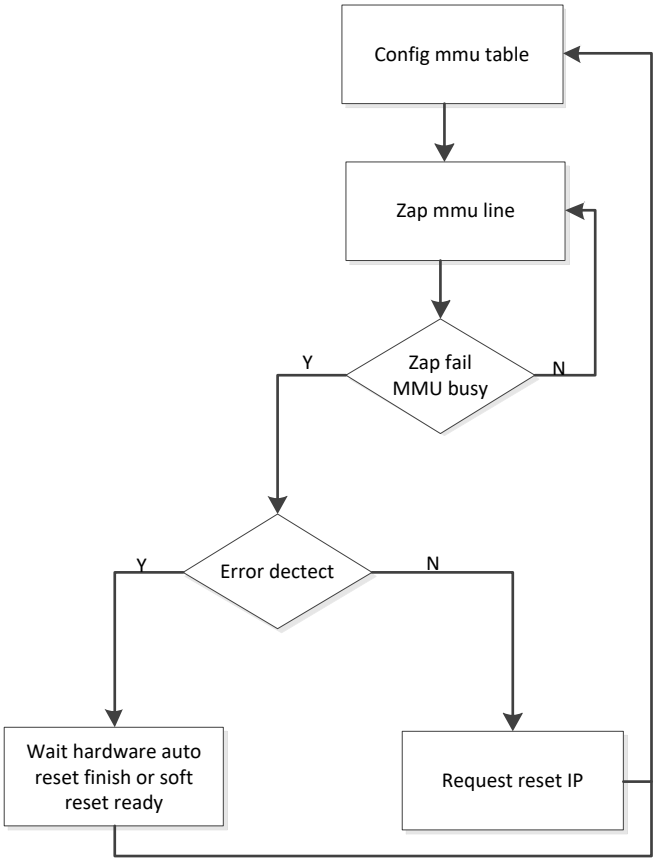


Fig. 1-5 MMU configure flow

1. Prepare MMU table to DDR and configure DTE address before begin to decoder.
2. If the MMU table have been changed, you will zap one MMU line.
3. If you zap success, you can continue to zap next line.
4. If you zap fail, maybe some error happened, then you should check if there any error happened when decoding.
5. If some error happened, you should wait reset finish, and then re-start MMU configure.
6. If don’t have any error find, it will still need to reset, and then re-start MMU configure.

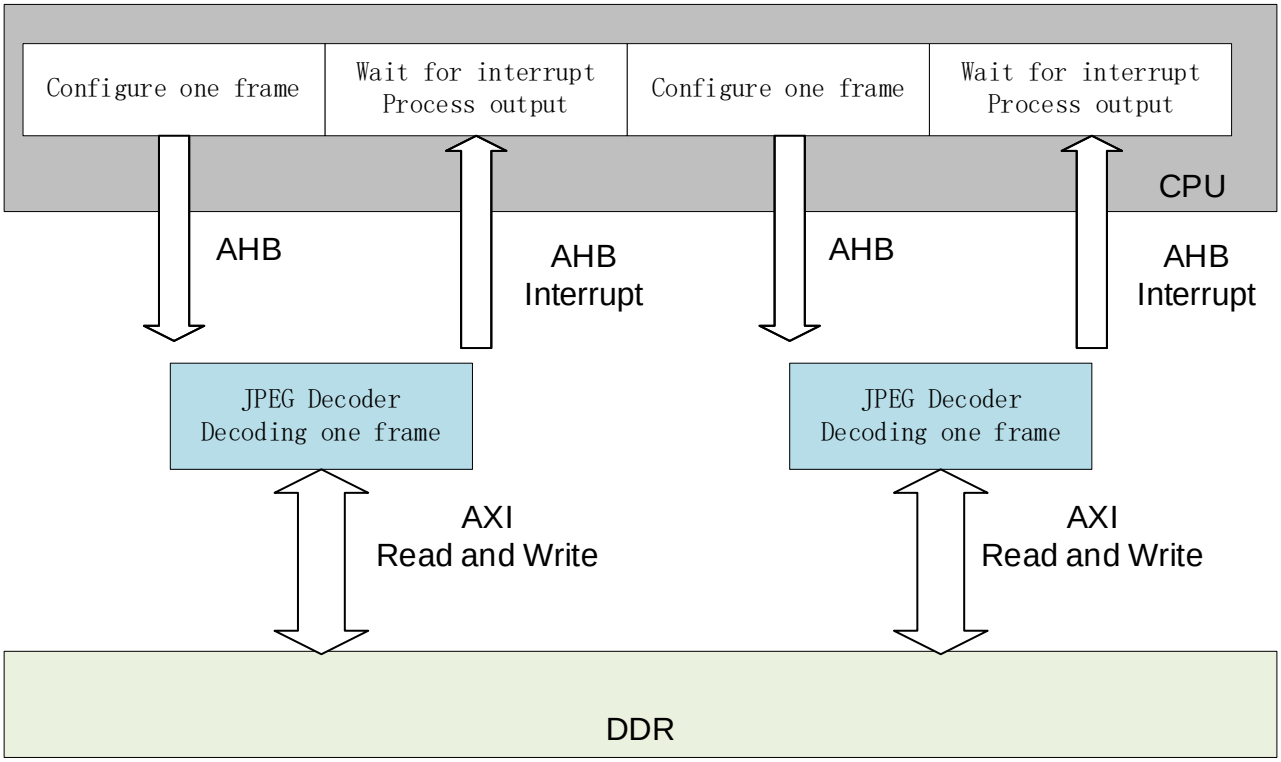
During MMU working, error might be happened, in such case, user must follow the MMU TRM to properly handle these errors.

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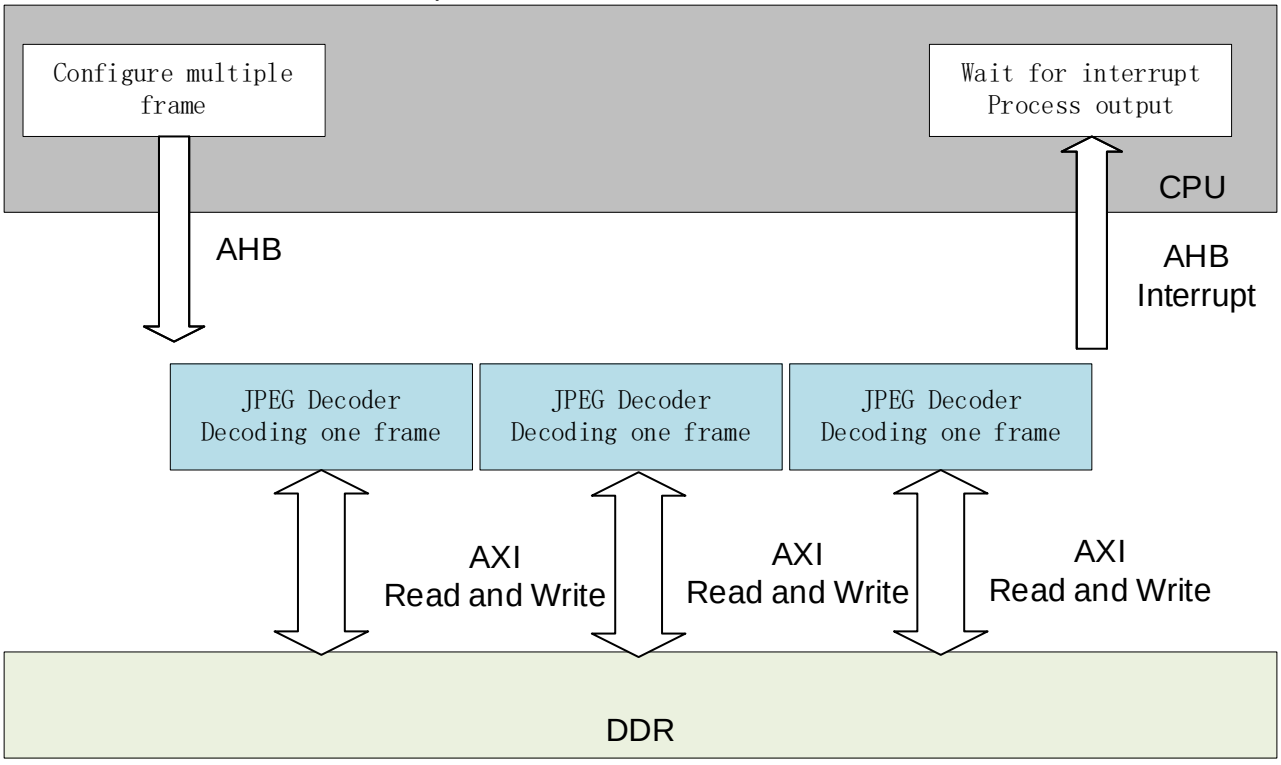
1.5.2 JPEG Codec Workflow

Both decoder and encoder support two workflows, the regular mode for frame by frame and the linked table mode for batch operation.

In regular mode, the coded is expected to work frame by frame, starting with register configuration, and ending with interrupting. Each frame is processed under the control of CPU.



In link table mode, user can prepare multiple frame configurations in DDR before coding, or append new frames while the codec is still processing the previous frame. This mode can saves waiting time, reduces interrupt handling and configuration operations, and allows the codec and software to work in parallel.



1.5.3 JPEG Decoder Regular Mode Configuration Flow

1. Prepare the decoder data in the DDR memory.
2. Configure all the registers will be used, except rkdjpeg_swreg1_int, which must be

configured at last.
3. Configure rkdjpeg_swreg1_int to start JPEG decoder.
4. Wait for the interrupt, and then check if the frame decoder ready interrupt is right or not, after that, you can get the processed results in the target DDR.
5. Clear all the interrupts, repeat step 2~4 to start a new frame decoder or encoder.

1.5.4 JPEG Decoder Linked Table Mode Configuration Flow

1. Prepare all the register configuration value into DDR.
2. Configure rkdjpeg_swreg194_link_mode and rkdjpeg_swreg198_link_mode_en
3. Configure rkdjpeg_swreg195_config_done to make the link table register configuration effective, hardware will begin to decoder frame by frame.
4. If you need to add more frame, append configuration to DDR, and set link table mode register, and enable the working flag by configure rkdjpeg_swreg194_link_mode and rkdjpeg_swreg195_config_done.
5. If all the frame be decoded, the hardware will hold the working status wait user to process.
6. When you get interrupt, at first, you should clear the interrupt, and then check if there have any error. If any error found by hardware, the hardware will disable link table mode and stop decoder until user restart next link table mode. And then you can get more information about error type from register.
9. When you get interrupt, if there doesn't have any error, you may be to check the frame number which have been decoded.
10. Please note that: when configure any link table register, rkdjpeg_swreg195_config_done must be set to make it effective.

Bit	Description
31:0	rkdjpeg_swreg1_int
63:32	rkdjpeg_swreg2_sys
95:64	rkdjpeg_swreg3_pic_size
127:96	rkdjpeg_swreg4_pic_format
159:128	rkdjpeg_swreg5_hor_virstride
191:160	rkdjpeg_swreg6_y_virstride
223:192	rkdjpeg_swreg7_table_len
255:224	rkdjpeg_swreg8_strm_len
287:256	rkdjpeg_swreg9_qtbl_base
319:288	rkdjpeg_swreg10_htbl_mincode_base
351:320	rkdjpeg_swreg11_htbl_value_base
383:352	rkdjpeg_swreg12_strm_base
415:384	rkdjpeg_swreg13_dec_out_base
447:416	rkdjpeg_swreg14_strm_error
479:448	rkdjpeg_swreg15_strm_mask
511:480	rkdjpeg_swreg16_clk_gate
543:512	reserved
575:544	reserved
607:576	reserved
639:608	reserved
671:640	rkdjpeg_swreg21_low_delay_output
703:672	reserved
735:704	reserved
767:736	reserved
799:768	reserved
831:800	reserved
863:832	reserved
895:864	reserved
927:896	rkdjpeg_swreg29_low_delay_output_status
959:928	rkdjpeg_swreg30_perf_latency_ctrl0

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991:960	rkdjpeg_swreg31_perf_latency_ctrl1
1023:992	reserved
1055:1024	reserved
1087:1056	reserved
1119:1088	reserved
1151:1120	reserved
1183:1152	reserved
1215:1184	reserved
1247:1216	reserved
1279:1248	reserved
1311:1280	reserved
1315:1312	core_id
1316	node_stop
1317	node_int
1329:1318	task_id
1343:1330	reserved
1375:1344	cfg_wr_addr
1407:1376	cfg_next_addr
1439:1408	reserved
1471:1440	reserved
1503:1472	reserved
1535:1504	reserved
1567:1536	lkt_mask

The register configuration need to be stored in DDR shall be organized as follow:

1.5.5 JPEG Encoder Regular Mode Configuration Flow

1. Prepare the decoder data in the DDR memory.
2. Configure all the registers will be used, except rkdjpeg_swreg1_int, which must be configured at last.
3. Configure RKEJPEG_ENC_STRT to start JPEG decoder.
4. Wait for the interrupt, and then check if the frame decoder ready interrupt is right or not, after that, you can get the processed results in the target DDR.
5. Clear all the interrupts, repeat step 2~4 to start a new frame decoder or encoder.

1.5.6 JPEG Encoder Linked Table Mode Configuration Flow

1. Prepare all the register configuration value into DDR.
2. Configure RKEJPEG_LKT_BASE_ADDR and RKEJPEG_NODE_OCFG.
3. Configure RKEJPEG_ENC_STRT to make the link table register configuration effective, hardware will begin to decoder frame by frame.
4. If you need to add more frame, append configuration to DDR, and configure RKEJPEG_ENC_STRT.
5. If all the frame be decoded, the hardware will hold the working status wait user to process.
6. When you get interrupt, at first, you should clear the interrupt, and then check if there have any error. If any error found by hardware, the hardware will disable link table mode and stop decoder until user restart next link table mode. And then you can get more information about error type from register.
9. When you get interrupt, if there doesn’t have any error, you may be to check the frame number which have been decoded.

The register configuration need to be stored in DDR shall be organized as follow:

Bit	Description
3:0	core_id
4	node_stop
5	node_int
17:6	task_id
57:18	cfg_wr_addr
97:58	cfg_next_addr

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Bit	Description
127:98	reserved
159:128	RKEJPEG_LKT_BASE_ADDR
191:160	RKEJPEG_NODE_OCFG
223:192	RKEJPEG_WDG_JPEG
255:224	RKEJPEG_LOW_DELAY_ECS_OCFG
287:256	RKEJPEG_LOW_DELAY_PACKET_OCFG
319:288	RKEJPEG_ADR_QTBL_JPEG
351:320	RKEJPEG_ADR_BSBT_JPEG
383:352	RKEJPEG_ADR_BSBB_JPEG
415:384	RKEJPEG_ADR_BSBR_JPEG
447:416	RKEJPEG_ADR_BSBS_JPEG
479:448	RKEJPEG_ADR_ECS_LEN
511:480	RKEJPEG_ADR_SRC0_JPEG
543:512	RKEJPEG_ADR_SRC1_JPEG
575:544	RKEJPEG_ADR_SRC2_JPEG
607:576	RKEJPEG_AXI_PREF_CTRL0
639:608	RKEJPEG_AXI_PERF_CTRL1
671:640	RKEJPEG_ENC_RSL_JPEG
703:672	RKEJPEG_SRC_FILL_JPEG
735:704	RKEJPEG_SRC_FMT_JPEG
767:736	RKEJPEG_PIC_OFST_JPEG
799:768	RKEJPEG_SRC_STRD0_JPEG
831:800	RKEJPEG_SRC_STRD1_JPEG
863:832	RKEJPEG_JPEG_BASE_CFG
895:864	RKEJPEG_BSP_SIZE_JPEG
927:896	RKEJPEG_UVC_CFG_JPEG
959:928	RKEJPEG_JPEG_Y_CFG
991:960	RKEJPEG_JPEG_U_CFG
1023:992	RKEJPEG_JPEG_V_CFG
1055:1024	RKEJPEG_DBUS_ENDN
1087:1056	lkt_mask

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Chapter 2 Video Display Post Processor (VDPP)

2.1 Overview

The Video Display Post Processor (VDPP) fetches data from system main memory and transmits data to system main memory by AXI bus. The main function is to enhance the picture quality.

VDPP is composed by DEI(De-interlace), VEP(Video Enhance Processor) and DCIHIST.

The features of DEI are as follows:

- **Image format**
  - Input data: YUV420/YUV422; Semi-planar/planar; UV swap
  - Output data: YUV420/YUV422; Semi-planar; UV swap; Tile mode
  - Max resolution for dynamic image up to 1920x1080
- **De-interlace**
  - **I5O2**: Input 5 Fields Output 2 frames mode
  - **I5O1T**: Input 5 Fields Output 1 Top frame mode
  - **I5O1B**: Input 5 Fields Output 1 Bottom frame mode
  - **I2O2**: Input 2 Fields Output 2 frames mode
  - **I1O1T**: Input 1 Field Output 1 Top frame mode
  - **I1O1B**: Input 1 Field Output 1 Bottom frame mode
  - **PULLDOWN_REC**: Pull-down Recovery mode
  - **DETECT_ONLY**: Detect Only mode
  - **FF DETECT**: Frame Field Detection
  - **FO DETECT**: Field Order Detection
  - **PD DETECT**: Pull Down Detection

The features of VEP are as follows:

- **Image format**
  - Input data: YUV420; Semi-planar; UV swap
  - Output data: YUV444; Semi-planar; UV swap;
  - YUV support up sampling conversion from 420 to 444 by ZME module
  - Input and output max resolution for dynamic image up to 1920x1080
- **DMSR**
  - De-Mosquito noise, De-Ringing effect and De-Shooting effect
  - Only process the Y 8bit component
- **ES（Edge Smoothing）**
  - Only process the Y 8bit component
  - The maximum supported image width: 1280;
- **ZME（Zoom Manage Engine）**
  - Video resize based Multi-phase Algorithm
  - Horizontal arbitrary non-integer scaling ratio, from 1/7 to 8
  - Vertical arbitrary non-integer scaling ratio, from 1/6 to 6
  - Dering
- **SHARP**
  - Support maximum width: 1920
  - Input and output image data format: YUV 10bit

The features of DCIHIST are as follows:

- **Image format**
  - RGB format: RGB888/ARGB8888/RGB101010
  - YUV Semi-Planer format：Y 8bit/10bit

The common features are as follows:

- **Interface**
  - 32bit AHB bus slave
  - 128bit AXI bus master
  - Combined interrupt output

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- Y and UV component independent resolution output
- QOS

2.2 Block Diagram

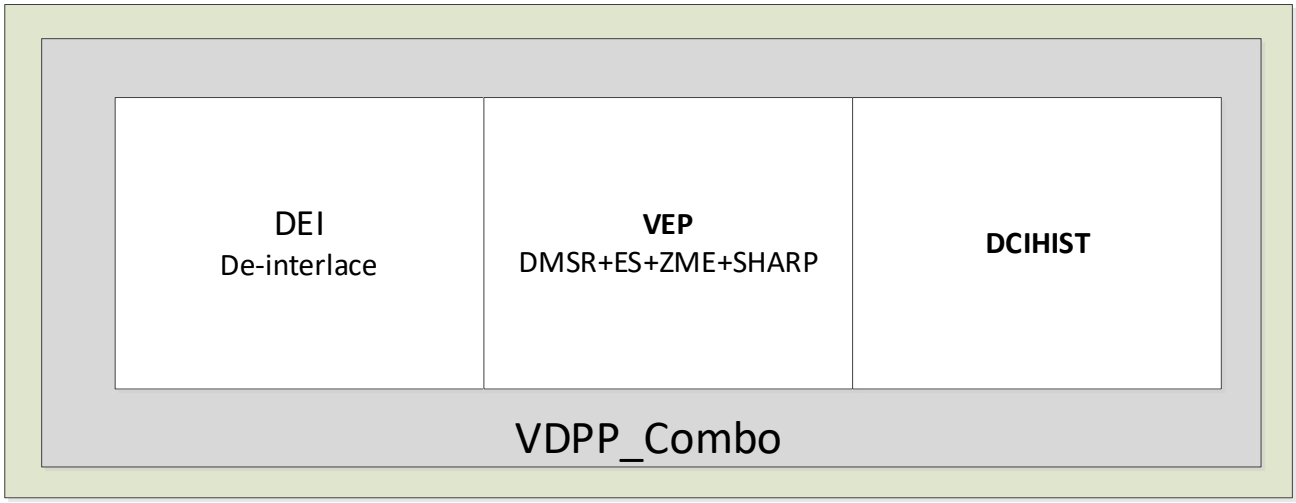


Fig. 2-1 Combo Block Diagram

As shown in the figures above, VDPP is composed by DEI(De-interlace), VEP(Video Enhance Processor) and DCIHIST.

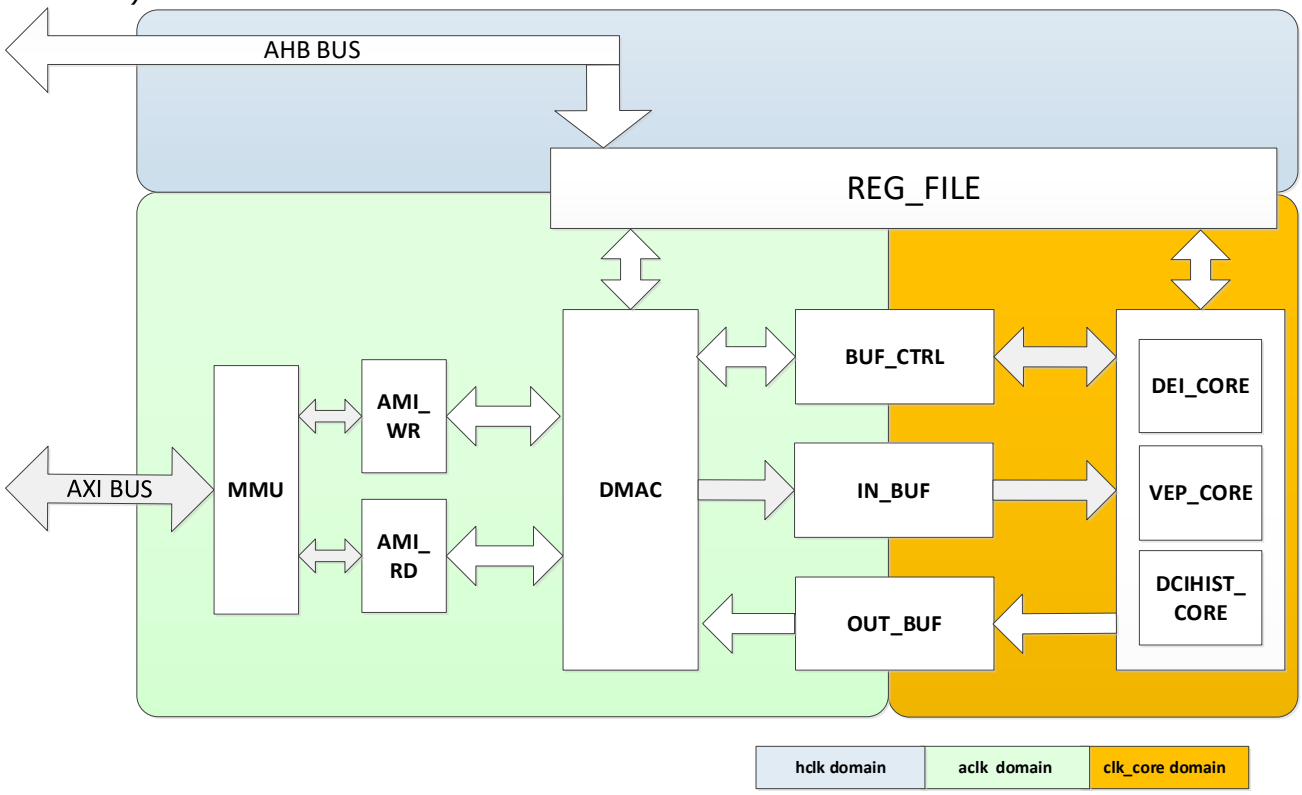


Fig. 2-2 VDPP block diagram

The data path in VDPP is in the previously diagram. The VDPP comprises with:

DEI_CORE
There are eight de-interlace modes (refer to feature description above) in the DIL_CORE block. Some important functions for deinterlace are in this module such as MD, ME, MC, EEDI.

VEP_CORE
DMSR

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DMSR stands for De-Mosquito noise, De-Ringing effect and De-Shooting effect.

ES
Smoothing edge sawtooth for small chip sources with a width of less than 1280 pixels.

ZME
ZME is used to resize the image with programmable poly-phase filter.

SHARP
Sharpen the Y component of the image

DCIHIST_CORE
DCIHIST_CORE module dynamically adjusts the brightness and contrast of the image to make it more transparent

DMA
DMA block responses for reading frame data from DDR and writing frame data to DDR.

REG FILE
All configurable signals will be configured in this block and send to other function modules for using.

2.3 Function Description

2.3.1 Deinterlace

There are eight deinterlace modes including I5O2, I5O1B, I5O1T, I2O2, I1O1B, I1O1T and detect only mode in the deinterlace block.

I5O2 mode
The I5O2 mode represents for 5 fields of input images and 2 frames of output images. This mode is the most frequently used. The input source images are stored as interlaced mode which means top field and bottom field are stored by the method that one top field line follows one bottom field or conversely. So, current, next and preview input frame address (SRC_ADDR_CURY, SRC_ADDR_NXTY and SRC_ADDR_PREY for Y channel) need to be configured. Top frame and bottom frame address (DST_ADDR_TOPY, DST_ADDR_BOTY for Y channel) need to be configured for output 2 frames.

I5O1B/T mode
The I5O1B and I5O1T mode have the same input images as the I5O2 mode, but only one frame output is generated which means only need configure one output frame address(top frame address for I5O1T mode and bottom frame address for I5O1B mode).

I2O2 mode
The I2O2 mode only need current input source frame, output is the same as I5O2 mode. This mode is the fastest and the most bandwidth saving.

I1O1B/T mode
The I1O1B and I1O1T mode just need read one filed. The output is same as I5O1B and I5O1T mode.

Bypass mode
If bypass mode is selected, there are not any deinterlace operations.

Pulldown Recovery mode
If the pulldown detection block detects the current source is pulldown interlace video. DEI supports pulldown recovery by setting this mode.

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Detect Only mode
This mode has no output frames for saving power and bandwidth. All of the detection results will be read back though AHB bus.

2.3.2 DMSR
After the image is compressed, the high-frequency information is lost due to compression quantization, which leads to the phenomenon of beating at the edge, which is called mosquito noise. DMSR stands for De-Mosquito noise, De-Ringing effect and De-Shooting effect.
The DMSR module only processes the Y component in image. By calculating the direction of each 8x8 block and the possibility of noise, the DMSR uses nonlinear low-pass filters to smooth the edges.

2.3.3 ES
The function of the Edge Smoothing module is to carry out low-pass filtering on the image along the edge before the small resolution image is magnified, so as to solve the sawtooth phenomenon generated when the small resolution image is magnified.

2.3.4 ZME
ZME is a image scaler based on polyphase filter that its characteristic is more approaching to ideal low pass filter. In addition, a new dering arithmetic is used to reduce the effect of ring.
The utilization of the hardware resource is mainly considered in the implementation of the entire module. The horizontal and vertical filter taps are 8 and 6, respectively.

2.3.5 SHARP
The main function of this system is to enhance image details and support configuring different strengths of gain for details of different scales and directions. The strength of detail enhancement can be controlled based on the image content, including local gradients, brightness, and variance information. Additionally, it supports controlling the strength of detail enhancement for different color channels of the input.

2.3.6 DCIHIST
The DCI module is mainly used to dynamically adjust the brightness and contrast of the picture according to the brightness distribution of the current picture to make the picture appear more transparent. The method used is mainly based on the histogram distribution of the current picture.

2.4 Register Description
The VDPP has some configuration segment.

2.4.1 Internal Address Mapping
Slave address can be divided into different length for different usage, which is shown as follows.

Table 2-1 VDPP Address Mapping

Base Address[15:12]	Device	Address Length	Offset Address Range
4'b0000	DEI	4096 BYTE	0x0000 ~ 0x0fff
4'b0001	VEP	4096 BYTE	0x1000 ~ 0x1fff
	DCIHIST	32 BYTE	0x10e0 ~ 0x10ff
	VEP_ES	128 BYTE	0x1100 ~ 0x117f
	VEP_SHARP	768 BYTE	0x1200 ~ 0x14ff
4'b0010	VEP_ZME	4096 BYTE	0x2000 ~ 0x2fff

2.4.2 Registers Summary

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2.4.2.1 DEI

Name	Offset	Size	Reset Value	Description
DEI_FRM_START	0x0000	W	0x00000000	Frame start and frame state register
DEI_CONFIG0	0x0004	W	0x00000303	DEI configuration register0
VDPP_WORKING_MODE	0x0008	W	0x00000000	Frame start and frame state register
DEI_QOS_CONFIG	0x000C	W	0x00000010	Frame start and frame state register
DEI_GATING_CTRL	0x0010	W	0x00000800	DEI auto gating register
DEI_STATUS	0x0014	W	0x00000000	DEI status
DEI_ARQOS_CONFIG	0x0018	W	0x00444141	AR qos config
DEI_AWQOS_CONFIG	0x001C	W	0x00004444	AW qos config
DEI_INT_EN	0x0020	W	0x00000011	DEI interrupt enable
DEI_INT_CLR	0x0024	W	0x00000000	DEI interrupt clear
DEI_INT_STS	0x0028	W	0x00000000	DEI interrupt status
DEI_INT_RAW_STS	0x002C	W	0x00000000	DEI interrupt raw status
DEI_VIR_SRC_IMG_WIDTH	0x0030	W	0x00000000	Source image virtual width
DEI_VIR_DST_IMG_WIDTH	0x0034	W	0x00000000	Destination image virtual width
DEI_SRC_IMG_SIZE	0x0038	W	0x00000000	Source image size
DEI_DIL_CONFIG0	0x0040	W	0x00029F01	Deinterlace configuration register0
DEI_DEI_TIMEOUT_CFG	0x0050	W	0x0065B9AA	Timeout configuration
DEI_DEI_VERSION_INFO	0x0054	W	0x20000000	DEI version information
DEI_DBG_FRM_CNT	0x0058	W	0x00000000	Frame counter
DEI_DBG_TIMEOUT_CNT	0x005C	W	0x00000000	Timeout counter
DEI_SRC_ADDR_CURY	0x0060	W	0x00000000	Start address of source current image(Y), frame address
DEI_SRC_ADDR_NXTY	0x0064	W	0x00000000	Start address of source next image(Y), frame address
DEI_SRC_ADDR_PREY	0x0068	W	0x00000000	Start address of source previous image(Y), frame address
DEI_SRC_ADDR_CURUV	0x006C	W	0x00000000	Start address of source current image(UV), SP mode UV frame or U P mode frame address
DEI_SRC_ADDR_CURV	0x0070	W	0x00000000	Start address of source current image(V), P mode V frame address
DEI_SRC_ADDR_NXTUV	0x0074	W	0x00000000	Start address of source next image(UV), SP mode UV frame or U P mode frame address
DEI_SRC_ADDR_NXTV	0x0078	W	0x00000000	Start address of source next image(V), P mode V frame address
DEI_SRC_ADDR_PREUV	0x007C	W	0x00000000	Start address of source previous image(UV), SP mode UV frame address or U P mode frame address
DEI_SRC_ADDR_PREV	0x0080	W	0x00000000	Start address of source previous image(V), P mode V frame address
DEI_SRC_ADDR_MD	0x0084	W	0x00000000	MD load address base register0

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Name	Offset	Size	Reset Value	Description
DEI_SRC_ADDR_MV	0x0088	W	0x00000000	MV load address base register0
DEI_ROI_ADDR	0x008C	W	0x00000000	ROI address register
DEI_DST_ADDR_TOPY	0x00B0	W	0x00000000	DST top frame luma address register
DEI_DST_ADDR_BOTY	0x00B4	W	0x00000000	DST bottom frame luma address register
DEI_DST_ADDR_TOPC	0x00B8	W	0x00000000	DST top frame chroma address register
DEI_DST_ADDR_BOTC	0x00BC	W	0x00000000	DST bottom frame chroma address register
DEI_DST_ADDR_MD	0x00C0	W	0x00000000	MD output base address register
DEI_DST_ADDR_MV	0x00C4	W	0x00000000	MV output base address register
DEI_MD_CONFIG0	0x00E0	W	0x00000044	Motion Detection configuration
DEI_DECT_CONFIG0	0x00E4	W	0x3C3C001E	Frame field detection, pulldown detection, OSD detection, combine detection
DEI_OSD_LIMIT_CONFIG	0x00F0	W	0x00000000	OSD limit area detection configuration
DEI_OSD_LIMIT_AREA0	0x00F4	W	0x00000000	OSD limit area 0
DEI_OSD_LIMIT_AREA1	0x00F8	W	0x00000000	OSD limit area 1
DEI_OSD_CONFIG0	0x00FC	W	0x00020032	OSD detection configuration
DEI_OSD_AREA_CONF0	0x0100	W	0x00000000	OSD area 0
DEI_OSD_AREA_CONF1	0x0104	W	0x00000000	OSD area 1
DEI_OSD_AREA_CONF2	0x0108	W	0x00000000	OSD area 2
DEI_OSD_AREA_CONF3	0x010C	W	0x00000000	OSD area 3
DEI_OSD_AREA_CONF4	0x0110	W	0x00000000	OSD area 4
DEI_OSD_AREA_CONF5	0x0114	W	0x00000000	OSD area 5
DEI_OSD_AREA_CONF6	0x0118	W	0x00000000	OSD area 6
DEI_OSD_AREA_CONF7	0x011C	W	0x00000000	OSD area 7
DEI_ME_CONFIG0	0x0120	W	0x001443A4	ME search configuration
DEI_ME_LIMIT_CONFIG	0x0124	W	0x00001B25	ME search limit
DEI_MV_TRU_LIST0	0x0128	W	0x00000000	MV trust list0~3
DEI_MV_TRU_LIST1	0x012C	W	0x00000000	MV trust list4~7
DEI_EEDI_CONFIG0	0x0130	W	0x0000000C	EEDI configuration register0
DEI_BLE_CONFIG0	0x0134	W	0x00000001	BLE configuration register0
DEI_COMB_CONFIG0	0x0138	W	0x001004FF	COMB DECT configuration register0
DEI_DIL_MTN_TAB0	0x0140	W	0x00000000	DIL_MTN_TAB0 table value
DEI_DIL_MTN_TAB1	0x0144	W	0x00000000	DIL_MTN_TAB1 table value
DEI_DIL_MTN_TAB2	0x0148	W	0x00000000	DIL_MTN_TAB2 table value
DEI_DIL_MTN_TAB3	0x014C	W	0x00000000	DIL_MTN_TAB3 table value
DEI_DIL_MTN_TAB4	0x0150	W	0x01010000	DIL_MTN_TAB4 table value
DEI_DIL_MTN_TAB5	0x0154	W	0x06050302	DIL_MTN_TAB5 table value
DEI_DIL_MTN_TAB6	0x0158	W	0x0F0D0A08	DIL_MTN_TAB6 table value
DEI_DIL_MTN_TAB7	0x015C	W	0x1C191512	DIL_MTN_TAB7 table value
DEI_DIL_MTN_TAB8	0x0160	W	0x2B282420	DIL_MTN_TAB8 table value
DEI_DIL_MTN_TAB9	0x0164	W	0x3634312E	DIL_MTN_TAB9 table value
DEI_DIL_MTN_TAB10	0x0168	W	0x3D3C3A38	DIL_MTN_TAB10 table value
DEI_DIL_MTN_TAB11	0x016C	W	0x40403F3E	DIL_MTN_TAB11 table value
DEI_DIL_MTN_TAB12	0x0170	W	0x40404040	DIL_MTN_TAB12 table value
DEI_DIL_MTN_TAB13	0x0174	W	0x40404040	DIL_MTN_TAB13 table value
DEI_DIL_MTN_TAB14	0x0178	W	0x40404040	DIL_MTN_TAB14 table value
DEI_DIL_MTN_TAB15	0x017C	W	0x40404040	DIL_MTN_TAB15 table value

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Name	Offset	Size	Reset Value	Description
DEI_RO_PD_TCNT	0x0400	W	0x00000000	Pulldown detection top field counter
DEI_RO_PD_BCNT	0x0404	W	0x00000000	Pulldown detection bottom field counter
DEI_RO_FF_CUR_TCNT	0x0408	W	0x00000000	Frame field detection current frame top field counter
DEI_RO_FF_CUR_BCNT	0x040C	W	0x00000000	Frame field detection current frame bottom field counter
DEI_RO_FF_NXT_TCNT	0x0410	W	0x00000000	Frame field detection next frame top field counter
DEI_RO_FF_NXT_BCNT	0x0414	W	0x00000000	Frame field detection next frame bottom field counter
DEI_RO_FF_BLE_TCNT	0x0418	W	0x00000000	Frame field detection current and next frame blend top field counter
DEI_RO_FF_BLE_BCNT	0x041C	W	0x00000000	Frame field detection current and next frame blend bottom field counter
DEI_RO_FF_COMB_NZ	0x0420	W	0x00000000	Frame field detection current frame combine detection none zero number
DEI_RO_FF_COMB_F	0x0424	W	0x00000000	Frame field detection current frame combine detection number
DEI_RO_OSD_NUM	0x0428	W	0x00000000	OSD area detection number
DEI_RO_OUT_COMB_CNT	0x042C	W	0x00000000	Deinterlace output combine detection
DEI_RO_FF_GRADT_TCNT	0x0430	W	0x00000000	Frame field detection, gradient top field counter
DEI_RO_FF_GRADT_BCNT	0x0434	W	0x00000000	Frame field detection, gradt bottom field counter
DEI_RO_MC_VLD_CNT	0x0438	W	0x00000000	MC valid counter
DEI_RO_OSD_AREA0_X	0x0440	W	0x00000000	OSD area detection area0 x
DEI_RO_OSD_AREA0_Y	0x0444	W	0x00000000	OSD area detection area0 y
DEI_RO_OSD_AREA1_X	0x0448	W	0x00000000	OSD area detection area1 x
DEI_RO_OSD_AREA1_Y	0x044C	W	0x00000000	OSD area detection area1 y
DEI_RO_OSD_AREA2_X	0x0450	W	0x00000000	OSD area detection area2 x
DEI_RO_OSD_AREA2_Y	0x0454	W	0x00000000	OSD area detection area2 y
DEI_RO_OSD_AREA3_X	0x0458	W	0x00000000	OSD area detection area3 x
DEI_RO_OSD_AREA3_Y	0x045C	W	0x00000000	OSD area detection area3 y
DEI_RO_OSD_AREA4_X	0x0460	W	0x00000000	OSD area detection area4 x
DEI_RO_OSD_AREA4_Y	0x0464	W	0x00000000	OSD area detection area4 y
DEI_RO_OSD_AREA5_X	0x0468	W	0x00000000	OSD area detection area5 x
DEI_RO_OSD_AREA5_Y	0x046C	W	0x00000000	OSD area detection area5 y
DEI_RO_OSD_AREA6_X	0x0470	W	0x00000000	OSD area detection area6 x
DEI_RO_OSD_AREA6_Y	0x0474	W	0x00000000	OSD area detection area6 y
DEI_RO_OSD_AREA7_X	0x0478	W	0x00000000	OSD area detection area7 x
DEI_RO_OSD_AREA7_Y	0x047C	W	0x00000000	OSD area detection area7 y
DEI_RO_MV_HIST_BIN0	0x0480	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN1	0x0484	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN2	0x0488	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN3	0x048C	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN4	0x0490	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN5	0x0494	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN6	0x0498	W	0x00000000	MV histogram

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Name	Offset	Size	Reset Value	Description
DEI_RO_MV_HIST_BIN7	0x049C	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN8	0x04A0	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN9	0x04A4	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN10	0x04A8	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN11	0x04AC	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN12	0x04B0	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN13	0x04B4	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN14	0x04B8	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN15	0x04BC	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN16	0x04C0	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN17	0x04C4	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN18	0x04C8	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN19	0x04CC	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN20	0x04D0	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN21	0x04D4	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN22	0x04D8	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN23	0x04DC	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN24	0x04E0	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN25	0x04E4	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN26	0x04E8	W	0x00000000	MV histogram
DEI_RO_MV_HIST_BIN27	0x04EC	W	0x00000000	MV histogram
DEI_PERF_LATENCY_CTRL0	0x0600	W	0x00000000	Only exist when this IP has axi_performance monitor feature
DEI_PERF_LATENCY_CTRL1	0x0604	W	0x00000000	Only exist when this IP has axi_performance monitor feature
DEI_PERF_RD_MAX_LATENCY_NUM	0x0608	W	0x00000000	Only exist when this IP has axi_performance monitor feature
DEI_PERF_RD_LATENCY_SAMP_NUM	0x060C	W	0x00000000	Only exist when this IP has axi_performance monitor feature
DEI_PERF_RD_LATENCY_ACC_SUM	0x0610	W	0x00000000	Only exist when this IP has axi_performance monitor feature
DEI_PERF_RD_AXI_TOTAL_BYTE	0x0614	W	0x00000000	Only exist when this IP has axi_performance monitor feature
DEI_PERF_WR_AXI_TOTAL_BYTE	0x0618	W	0x00000000	Only exist when this IP has axi_performance monitor feature
DEI_PERF_WORKING_CNT	0x061C	W	0x00000000	Only exist when this IP has axi_performance monitor feature
DEI_MMU_DTE_ADDR	0x0800	W	0x00000000	MMU DTE address
DEI_MMU_STATUS	0x0804	W	0x00000018	MMU status
DEI_MMU_CMD	0x0808	W	0x00000000	MMU command
DEI_MMU_PAGE_FAULT_ADDR	0x080C	W	0x00000000	Page fault address
DEI_MMU_ZAP_ONE_LINE	0x0810	W	0x00000000	MMU zap one line
DEI_MMU_INT_RAWSTAT	0x0814	W	0x00000000	MMU interruption raw status
DEI_MMU_INT_CLEAR	0x0818	W	0x00000000	MMU interruption clear
DEI_MMU_INT_MASK	0x081C	W	0x00000000	MMU interruption mask
DEI_MMU_INT_STATUS	0x0820	W	0x00000000	MMU interruption status
DEI_MMU_AUTO_GATING	0x0824	W	0x00000001	MMU auto gating configure
DEI_MMU_ID	0x0828	W	0x00000000	MMU ID

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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2.4.2.2 VEP

Name	Offset	Size	Reset Value	Description
VEP_FRM_START	0x0000	W	0x00000000	Frame start and frame state register
VEP_CONFIG0	0x0004	W	0x00000303	VEP configuration register0
VEP_WORKING_MODE	0x0008	W	0x00000000	Frame start and frame state register
VEP_QOS_CONFIG	0x000C	W	0x00000010	Frame start and frame state register
VEP_GATING_CTRL	0x0010	W	0x00000800	VEP auto gating register
VEP_STATUS	0x0014	W	0x00000000	VEP status
VEP_ARQOS_CONFIG	0x0018	W	0x00004141	AR qos config
VEP_AWQOS_CONFIG	0x001C	W	0x00004444	AW qos config
VEP_INT_EN	0x0020	W	0x00000051	VEP interrupt enable
VEP_INT_CLR	0x0024	W	0x00000000	VEP interrupt clear
VEP_INT_STS	0x0028	W	0x00000000	VEP interrupt status
VEP_INT_RAW_STS	0x002C	W	0x00000000	VEP interrupt raw status
VEP_VIR_SRC_IMG_WIDTH	0x0030	W	0x00000000	Source image virtual width
VEP_VIR_DST_IMG_WIDTH	0x0034	W	0x00000000	Destination image virtual width
VEP_SRC_IMG_SIZE	0x0038	W	0x00000000	Source image size
VEP_DST_IMG_SIZE	0x003C	W	0x00000000	Source image size
VEP_DST_IMG_SIZE_C	0x0040	W	0x00000000	Destination image uv component size
VEP_TIMEOUT_CFG	0x0050	W	0x0065B9AA	Timeout configuration
VEP_VERSION_INFO	0x0054	W	0x20000000	VEP version information
VEP_DBG_FRM_CNT	0x0058	W	0x00000000	Frame counter
VEP_SRC_ADDR_Y	0x0060	W	0x00000000	Start address of source image(Y), frame address
VEP_SRC_ADDR_UV	0x0064	W	0x00000000	Start address of source image(UV), frame address
VEP_DST_ADDR_Y	0x0068	W	0x00000000	Start address of destination image(Y), frame address
VEP_DST_ADDR_UV	0x006C	W	0x00000000	Start address of destination image(UV), frame address
VEP_DMSR_EDGE_THRE0	0x0080	W	0x00000000	Edge threshold
VEP_DMSR_EDGE_THRE1	0x0084	W	0x00000000	Edge threshold
VEP_DMSR_EDGE_THRE2	0x0088	W	0x00000000	Edge threshold
VEP_DMSR_EDGE_THRE3	0x008C	W	0x00000000	Edge threshold
VEP_DMSR_EDGE_THRE4	0x0090	W	0x00000000	Edge threshold
VEP_DMSR_EDGE_THRE5	0x0094	W	0x00000000	Edge threshold
VEP_DMSR_EDGE_THRE6	0x0098	W	0x00000000	Edge threshold
VEP_DMSR_EDGE_K0	0x009C	W	0x00000000	Edge mapping slope

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Name	Offset	Size	Reset Value	Description
VEP_DMSR_EDGE_K1	0x00A0	W	0x00000000	Edge mapping slope
VEP_DMSR_EDGE_K2	0x00A4	W	0x00000000	Edge mapping slope
VEP_DMSR_EDGE_K3	0x00A8	W	0x00000000	Edge mapping slope
VEP_DMSR_DIR_CONTRAST_CONF_X	0x00AC	W	0x00000000	DMSR direction contrast confidence mapping X
VEP_DMSR_DIR_CONTRAST_CONF_Y	0x00B0	W	0x00000000	DMSR direction contrast confidence mapping Y
VEP_DMSR_FLATNESS_THRE	0x00B4	W	0x00000000	DMSR flatness threshold
VEP_DMSR_DIFF_CORING_THRE	0x00B8	W	0x00000000	DMSR diff coring threshold
VEP_DMSR_DIFF_CORING_WEIGHT	0x00BC	W	0x00000000	DMSR diff coring weight
VEP_DMSR_DIFF_CORING_Y	0x00C0	W	0x00000000	DMSR diff coring threshold
VEP_DMSR_FILTER_PRIMARY_TAP_WEIGHT_GAIN	0x00C4	W	0x00000000	DMSR filter primary tap weight gain
VEP_DMSR_FILTER_SECONDARY_TAP_WEIGHT_GAIN	0x00C8	W	0x00000000	DMSR filter secondary tap weight gain
VEP_DMSR_FILTER_STRENGTH	0x00CC	W	0x00000000	DMSR filter strength and dumping
VEP_DMSR_DBG_MODE	0x00D0	W	0x00000000	DMSR debug coordinate
VEP_DCI_YRGB_ADDR	0x00E0	W	0x00000000	Start address of source image(Y), frame address
VEP_DCI_YRGB_VIR_STRIDE	0x00E4	W	0x00000000	DCI YRGB virtual strider
VEP_DCI_IMG_SIZE	0x00E8	W	0x00000000	DCI Source image size
VEP_DCI_CTRL	0x00EC	W	0x00000000	DCI config
VEP_DCI_HIST_ADDR	0x00F0	W	0x00000000	DCI HIST write address

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.2.3 ES

Name	Offset	Size	Reset Value	Description
ES_EN	0x0000	W	0x00000000	ES Enable Register
ES_DIR_TH	0x0004	W	0x00000000	ES Direction Threshold Register
ES_DIR_TAN	0x0008	W	0x00000000	Direction Tan Register
ES_DIR_CHK	0x000C	W	0x00000000	Direction Endpoint Check Enable & Mem Gating Enable Register
ES_FIL_DIFF0	0x0010	W	0x00000000	Confidence Map Parameter Register0
ES_FIL_DIFF1	0x0014	W	0x00000000	Confidence Map Parameter Register1
ES_FIL_LUT_X0	0x0018	W	0x00000000	Filter Lut X Register0

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Name	Offset	Size	Reset Value	Description
ES_FIL_LUT_X1	0x001C	W	0x00000000	Filter Lut X Register1
ES_FIL_LUT_X2	0x0020	W	0x00000000	Filter Lut X Register2
ES_FIL_LUT_X3	0x0024	W	0x00000000	Filter Lut X Register3
ES_FIL_LUT_Y0	0x0028	W	0x00000000	Filter Lut Y Register0
ES_FIL_LUT_Y1	0x002C	W	0x00000000	Filter Lut Y Register1
ES_FIL_LUT_Y2	0x0030	W	0x00000000	Filter Lut Y Register2
ES_FIL_LUT_K0	0x0034	W	0x00000000	Filter Lut K Register0
ES_FIL_LUT_K1	0x0038	W	0x00000000	Filter Lut K Register1
ES_FIL_WGT	0x003C	W	0x00000000	Filter Weight Resgister
ES_FIL_CONF	0x0040	W	0x00000000	Confidence Mean Map Parameter Register
ES_DBG_INL	0x0044	W	0x00000000	Bebug Ink Mode Contral Register
ES_DBG_INFO0	0x0070	W	0x00000000	Debug Information Register0
ES_DBG_INFO1	0x0074	W	0x00000000	Debug Information Register1
ES_DBG_INFO2	0x0078	W	0x00000000	Debug Information Register2
ES_DBG_INFO3	0x007C	W	0x00000000	Debug Information Register3

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.2.4 ZME

Name	Offset	Size	Reset Value	Description
ZME_YRGB_HOR_COE0_10	0x0000	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE0_32	0x0004	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE0_54	0x0008	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE0_76	0x000C	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE1_10	0x0010	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE1_32	0x0014	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE1_54	0x0018	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE1_76	0x001C	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE2_10	0x0020	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE2_32	0x0024	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE2_54	0x0028	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE2_76	0x002C	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE3_10	0x0030	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE3_32	0x0034	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE3_54	0x0038	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE3_76	0x003C	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE4_10	0x0040	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE4_32	0x0044	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE4_54	0x0048	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE4_76	0x004C	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE5_10	0x0050	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE5_32	0x0054	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE5_54	0x0058	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE5_76	0x005C	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE6_10	0x0060	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE6_32	0x0064	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE6_54	0x0068	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE6_76	0x006C	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE7_10	0x0070	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE7_32	0x0074	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE7_54	0x0078	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE7_76	0x007C	W	0x00000000	YRGB horizontal filter coefficient

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Name	Offset	Size	Reset Value	Description
ZME_YRGB_HOR_COE8_10	0x0080	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE8_32	0x0084	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE8_54	0x0088	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE8_76	0x008C	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE9_10	0x0090	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE9_32	0x0094	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE9_54	0x0098	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE9_76	0x009C	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE10_10	0x00A0	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE10_32	0x00A4	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE10_54	0x00A8	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE10_76	0x00AC	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE11_10	0x00B0	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE11_32	0x00B4	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE11_54	0x00B8	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE11_76	0x00BC	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE12_10	0x00C0	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE12_32	0x00C4	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE12_54	0x00C8	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE12_76	0x00CC	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE13_10	0x00D0	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE13_32	0x00D4	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE13_54	0x00D8	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE13_76	0x00DC	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE14_10	0x00E0	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE14_32	0x00E4	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE14_54	0x00E8	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE14_76	0x00EC	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE15_10	0x00F0	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE15_32	0x00F4	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE15_54	0x00F8	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE15_76	0x00FC	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE16_10	0x0100	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE16_32	0x0104	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE16_54	0x0108	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_HOR_COE16_76	0x010C	W	0x00000000	YRGB horizontal filter coefficient
ZME_YRGB_VER_COE0_10	0x0200	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE0_32	0x0204	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE0_54	0x0208	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE0_76	0x020C	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE1_10	0x0210	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE1_32	0x0214	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE1_54	0x0218	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE1_76	0x021C	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE2_10	0x0220	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE2_32	0x0224	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE2_54	0x0228	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE2_76	0x022C	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE3_10	0x0230	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE3_32	0x0234	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE3_54	0x0238	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE3_76	0x023C	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE4_10	0x0240	W	0x00000000	YRGB vertical filter coefficient

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Name	Offset	Size	Reset Value	Description
ZME_YRGB_VER_COE4_32	0x0244	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE4_54	0x0248	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE4_76	0x024C	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE5_10	0x0250	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE5_32	0x0254	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE5_54	0x0258	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE5_76	0x025C	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE6_10	0x0260	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE6_32	0x0264	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE6_54	0x0268	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE6_76	0x026C	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE7_10	0x0270	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE7_32	0x0274	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE7_54	0x0278	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE7_76	0x027C	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE8_10	0x0280	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE8_32	0x0284	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE8_54	0x0288	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE8_76	0x028C	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE9_10	0x0290	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE9_32	0x0294	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE9_54	0x0298	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE9_76	0x029C	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE10_10	0x02A0	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE10_32	0x02A4	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE10_54	0x02A8	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE10_76	0x02AC	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE11_10	0x02B0	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE11_32	0x02B4	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE11_54	0x02B8	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE11_76	0x02BC	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE12_10	0x02C0	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE12_32	0x02C4	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE12_54	0x02C8	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE12_76	0x02CC	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE13_10	0x02D0	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE13_32	0x02D4	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE13_54	0x02D8	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE13_76	0x02DC	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE14_10	0x02E0	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE14_32	0x02E4	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE14_54	0x02E8	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE14_76	0x02EC	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE15_10	0x02F0	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE15_32	0x02F4	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE15_54	0x02F8	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE15_76	0x02FC	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE16_10	0x0300	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE16_32	0x0304	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE16_54	0x0308	W	0x00000000	YRGB vertical filter coefficient
ZME_YRGB_VER_COE16_76	0x030C	W	0x00000000	YRGB vertical filter coefficient
ZME_CBCR_HOR_COE0_10	0x0400	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE0_32	0x0404	W	0x00000000	CBCR horizontal filter coefficient

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Name	Offset	Size	Reset Value	Description
ZME_CBCR_HOR_COE0_54	0x0408	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE0_76	0x040C	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE1_10	0x0410	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE1_32	0x0414	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE1_54	0x0418	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE1_76	0x041C	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE2_10	0x0420	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE2_32	0x0424	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE2_54	0x0428	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE2_76	0x042C	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE3_10	0x0430	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE3_32	0x0434	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE3_54	0x0438	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE3_76	0x043C	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE4_10	0x0440	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE4_32	0x0444	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE4_54	0x0448	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE4_76	0x044C	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE5_10	0x0450	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE5_32	0x0454	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE5_54	0x0458	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE5_76	0x045C	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE6_10	0x0460	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE6_32	0x0464	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE6_54	0x0468	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE6_76	0x046C	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE7_10	0x0470	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE7_32	0x0474	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE7_54	0x0478	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE7_76	0x047C	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE8_10	0x0480	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE8_32	0x0484	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE8_54	0x0488	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE8_76	0x048C	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE9_10	0x0490	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE9_32	0x0494	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE9_54	0x0498	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE9_76	0x049C	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE10_10	0x04A0	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE10_32	0x04A4	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE10_54	0x04A8	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE10_76	0x04AC	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE11_10	0x04B0	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE11_32	0x04B4	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE11_54	0x04B8	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE11_76	0x04BC	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE12_10	0x04C0	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE12_32	0x04C4	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE12_54	0x04C8	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE12_76	0x04CC	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE13_10	0x04D0	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE13_32	0x04D4	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE13_54	0x04D8	W	0x00000000	CBCR horizontal filter coefficient

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Name	Offset	Size	Reset Value	Description
ZME_CBCR_HOR_COE13_76	0x04DC	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE14_10	0x04E0	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE14_32	0x04E4	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE14_54	0x04E8	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE14_76	0x04EC	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE15_10	0x04F0	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE15_32	0x04F4	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE15_54	0x04F8	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE15_76	0x04FC	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE16_10	0x0500	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE16_32	0x0504	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE16_54	0x0508	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_HOR_COE16_76	0x050C	W	0x00000000	CBCR horizontal filter coefficient
ZME_CBCR_VER_COE0_10	0x0600	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE0_32	0x0604	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE0_54	0x0608	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE0_76	0x060C	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE1_10	0x0610	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE1_32	0x0614	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE1_54	0x0618	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE1_76	0x061C	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE2_10	0x0620	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE2_32	0x0624	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE2_54	0x0628	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE2_76	0x062C	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE3_10	0x0630	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE3_32	0x0634	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE3_54	0x0638	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE3_76	0x063C	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE4_10	0x0640	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE4_32	0x0644	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE4_54	0x0648	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE4_76	0x064C	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE5_10	0x0650	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE5_32	0x0654	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE5_54	0x0658	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE5_76	0x065C	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE6_10	0x0660	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE6_32	0x0664	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE6_54	0x0668	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE6_76	0x066C	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE7_10	0x0670	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE7_32	0x0674	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE7_54	0x0678	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE7_76	0x067C	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE8_10	0x0680	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE8_32	0x0684	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE8_54	0x0688	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE8_76	0x068C	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE9_10	0x0690	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE9_32	0x0694	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE9_54	0x0698	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE9_76	0x069C	W	0x00000000	CBCR vertical filter coefficient

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Name	Offset	Size	Reset Value	Description
ZME_CBCR_VER_COE10_10	0x06A0	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE10_32	0x06A4	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE10_54	0x06A8	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE10_76	0x06AC	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE11_10	0x06B0	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE11_32	0x06B4	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE11_54	0x06B8	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE11_76	0x06BC	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE12_10	0x06C0	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE12_32	0x06C4	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE12_54	0x06C8	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE12_76	0x06CC	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE13_10	0x06D0	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE13_32	0x06D4	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE13_54	0x06D8	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE13_76	0x06DC	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE14_10	0x06E0	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE14_32	0x06E4	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE14_54	0x06E8	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE14_76	0x06EC	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE15_10	0x06F0	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE15_32	0x06F4	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE15_54	0x06F8	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE15_76	0x06FC	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE16_10	0x0700	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE16_32	0x0704	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE16_54	0x0708	W	0x00000000	CBCR vertical filter coefficient
ZME_CBCR_VER_COE16_76	0x070C	W	0x00000000	CBCR vertical filter coefficient
ZME_ZME_CTRL	0x0800	W	0x00000000	ZME control
ZME_YRGB_SCL_CTRL	0x0810	W	0x00000000	YRGB scale control
ZME_YRGB_DERING_PARA	0x081C	W	0x00000000	YRGB dering control
ZME_YRGB_XSCL_FACTOR	0x0820	W	0x00000000	YRGB scale factor
ZME_YRGB_YSCL_FACTOR	0x0824	W	0x00000000	YRGB scale factor
ZME_CBCR_SCL_CTRL	0x0830	W	0x00000000	CBCR scale control
ZME_CBCR_DERING_PARA	0x083C	W	0x00000000	CBCR dering control
ZME_CBCR_XSCL_FACTOR	0x0840	W	0x00000000	CBCR scale factor
ZME_CBCR_YSCL_FACTOR	0x0844	W	0x00000000	CBCR scale factor

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.2.5 SHARP

Name	Offset	Size	Reset Value	Description
SHARP_CTRL	0x0000	W	0x00000000	Sharp function enable control.
SHARP_AUTO_GATING_IMD	0x0004	W	0x00000000	To control auto-gating.
SHARP_PEAKING_FILTER_COE0	0x0008	W	0x00000000	Sharp peaking filter coe0.
SHARP_PEAKING_FILTER_COE1	0x000C	W	0x00000000	Sharp peaking filter coe1.
SHARP_PEAKING_FILTER_COE2	0x0010	W	0x00000000	Sharp peaking filter coe2.
SHARP_PEAKING_FILTER_COE4	0x0018	W	0x00000000	Sharp peaking filter coe4.

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Name	Offset	Size	Reset Value	Description
SHARP_PEAKING_FILTER_COE6	0x0020	W	0x00000000	Sharp peaking filter coe6.
SHARP_PEAKING0_CTRL_COE0	0x0030	W	0x00000000	Sharp peaking0 control coe0.
SHARP_PEAKING0_CTRL_COE1	0x0034	W	0x00000000	Sharp peaking0 control coe1.
SHARP_PEAKING0_CTRL_COE2	0x0038	W	0x00000000	Sharp peaking0 control coe2.
SHARP_PEAKING0_CTRL_COE3	0x003C	W	0x00000000	Sharp peaking0 control coe3.
SHARP_PEAKING0_CTRL_COE4	0x0040	W	0x00000000	Sharp peaking0 control coe4.
SHARP_PEAKING0_CTRL_COE5	0x0044	W	0x00000000	Sharp peaking0 control coe5.
SHARP_PEAKING0_CTRL_COE6	0x0048	W	0x00000000	Sharp peaking0 control coe6.
SHARP_PEAKING0_CTRL_COE7	0x004C	W	0x00000000	Sharp peaking0 control coe7.
SHARP_PEAKING0_CTRL_COE8	0x0050	W	0x00000000	Sharp peaking0 control coe8.
SHARP_PEAKING0_CTRL_COE9	0x0054	W	0x00000000	Sharp peaking0 control coe9.
SHARP_PEAKING1_CTRL_COE0	0x005C	W	0x00000000	Sharp peaking1 control coe0.
SHARP_PEAKING1_CTRL_COE1	0x0060	W	0x00000000	Sharp peaking1 control coe1.
SHARP_PEAKING1_CTRL_COE2	0x0064	W	0x00000000	Sharp peaking1 control coe2.
SHARP_PEAKING1_CTRL_COE3	0x0068	W	0x00000000	Sharp peaking1 control coe3.
SHARP_PEAKING1_CTRL_COE4	0x006C	W	0x00000000	Sharp peaking1 control coe4.
SHARP_PEAKING1_CTRL_COE5	0x0070	W	0x00000000	Sharp peaking1 control coe5.
SHARP_PEAKING1_CTRL_COE6	0x0074	W	0x00000000	Sharp peaking1 control coe6.
SHARP_PEAKING1_CTRL_COE7	0x0078	W	0x00000000	Sharp peaking1 control coe7.
SHARP_PEAKING1_CTRL_COE8	0x007C	W	0x00000000	Sharp peaking1 control coe8.
SHARP_PEAKING1_CTRL_COE9	0x0080	W	0x00000000	Sharp peaking1 control coe9.
SHARP_PEAKING2_CTRL_COE0	0x0088	W	0x00000000	Sharp peaking2 control coe0.
SHARP_PEAKING2_CTRL_COE1	0x008C	W	0x00000000	Sharp peaking2 control coe1.
SHARP_PEAKING2_CTRL_COE2	0x0090	W	0x00000000	Sharp peaking2 control coe2.
SHARP_PEAKING2_CTRL_COE3	0x0094	W	0x00000000	Sharp peaking2 control coe3.
SHARP_PEAKING2_CTRL_COE4	0x0098	W	0x00000000	Sharp peaking2 control coe4.
SHARP_PEAKING2_CTRL_COE5	0x009C	W	0x00000000	Sharp peaking2 control coe5.

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Name	Offset	Size	Reset Value	Description
SHARP_PEAKING2_CTRL_COE6	0x00A0	W	0x00000000	Sharp peaking2 control coe6.
SHARP_PEAKING2_CTRL_COE7	0x00A4	W	0x00000000	Sharp peaking2 control coe7.
SHARP_PEAKING2_CTRL_COE8	0x00A8	W	0x00000000	Sharp peaking2 control coe8.
SHARP_PEAKING2_CTRL_COE9	0x00AC	W	0x00000000	Sharp peaking2 control coe9.
SHARP_PEAKING3_CTRL_COE0	0x00B4	W	0x00000000	Sharp peaking3 control coe0.
SHARP_PEAKING3_CTRL_COE1	0x00B8	W	0x00000000	Sharp peaking3 control coe1.
SHARP_PEAKING3_CTRL_COE2	0x00BC	W	0x00000000	Sharp peaking3 control coe2.
SHARP_PEAKING3_CTRL_COE3	0x00C0	W	0x00000000	Sharp peaking3 control coe3.
SHARP_PEAKING3_CTRL_COE4	0x00C4	W	0x00000000	Sharp peaking3 control coe4.
SHARP_PEAKING3_CTRL_COE5	0x00C8	W	0x00000000	Sharp peaking3 control coe5.
SHARP_PEAKING3_CTRL_COE6	0x00CC	W	0x00000000	Sharp peaking3 control coe6.
SHARP_PEAKING3_CTRL_COE7	0x00D0	W	0x00000000	Sharp peaking3 control coe7.
SHARP_PEAKING3_CTRL_COE8	0x00D4	W	0x00000000	Sharp peaking3 control coe8.
SHARP_PEAKING3_CTRL_COE9	0x00D8	W	0x00000000	Sharp peaking3 control coe9.
SHARP_PEAKING4_CTRL_COE0	0x00E0	W	0x00000000	Sharp peaking4 control coe0.
SHARP_PEAKING4_CTRL_COE1	0x00E4	W	0x00000000	Sharp peaking4 control coe1.
SHARP_PEAKING4_CTRL_COE2	0x00E8	W	0x00000000	Sharp peaking4 control coe2.
SHARP_PEAKING4_CTRL_COE3	0x00EC	W	0x00000000	Sharp peaking4 control coe3.
SHARP_PEAKING4_CTRL_COE4	0x00F0	W	0x00000000	Sharp peaking4 control coe4.
SHARP_PEAKING4_CTRL_COE5	0x00F4	W	0x00000000	Sharp peaking4 control coe5.
SHARP_PEAKING4_CTRL_COE6	0x00F8	W	0x00000000	Sharp peaking4 control coe6.
SHARP_PEAKING4_CTRL_COE7	0x00FC	W	0x00000000	Sharp peaking4 control coe7.
SHARP_PEAKING4_CTRL_COE8	0x0100	W	0x00000000	Sharp peaking4 control coe8.
SHARP_PEAKING4_CTRL_COE9	0x0104	W	0x00000000	Sharp peaking4 control coe9.
SHARP_PEAKING5_CTRL_COE0	0x010C	W	0x00000000	Sharp peaking5 control coe0.
SHARP_PEAKING5_CTRL_COE1	0x0110	W	0x00000000	Sharp peaking5 control coe1.
SHARP_PEAKING5_CTRL_COE2	0x0114	W	0x00000000	Sharp peaking5 control coe2.

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Name	Offset	Size	Reset Value	Description
SHARP_PEAKING5_CTRL_COE3	0x0118	W	0x00000000	Sharp peaking5 control coe3.
SHARP_PEAKING5_CTRL_COE4	0x011C	W	0x00000000	Sharp peaking5 control coe4.
SHARP_PEAKING5_CTRL_COE5	0x0120	W	0x00000000	Sharp peaking5 control coe5.
SHARP_PEAKING5_CTRL_COE6	0x0124	W	0x00000000	Sharp peaking5 control coe6.
SHARP_PEAKING5_CTRL_COE7	0x0128	W	0x00000000	Sharp peaking5 control coe7.
SHARP_PEAKING5_CTRL_COE8	0x012C	W	0x00000000	Sharp peaking5 control coe8.
SHARP_PEAKING5_CTRL_COE9	0x0130	W	0x00000000	Sharp peaking5 control coe9.
SHARP_PEAKING6_CTRL_COE0	0x0138	W	0x00000000	Sharp peaking6 control coe0.
SHARP_PEAKING6_CTRL_COE1	0x013C	W	0x00000000	Sharp peaking6 control coe1.
SHARP_PEAKING6_CTRL_COE2	0x0140	W	0x00000000	Sharp peaking6 control coe2.
SHARP_PEAKING6_CTRL_COE3	0x0144	W	0x00000000	Sharp peaking6 control coe3.
SHARP_PEAKING6_CTRL_COE4	0x0148	W	0x00000000	Sharp peaking6 control coe4.
SHARP_PEAKING6_CTRL_COE5	0x014C	W	0x00000000	Sharp peaking6 control coe5.
SHARP_PEAKING6_CTRL_COE6	0x0150	W	0x00000000	Sharp peaking6 control coe6.
SHARP_PEAKING6_CTRL_COE7	0x0154	W	0x00000000	Sharp peaking6 control coe7.
SHARP_PEAKING6_CTRL_COE8	0x0158	W	0x00000000	Sharp peaking6 control coe8.
SHARP_PEAKING6_CTRL_COE9	0x015C	W	0x00000000	Sharp peaking6 control coe9.
SHARP_PEAKING_CTRL0	0x0190	W	0x00000000	Sharp peaking control cfg0.
SHARP_PEAKING_CTRL1	0x0194	W	0x00000000	Sharp peaking control cfg1.
SHARP_PEAKING_CTRL2	0x0198	W	0x00000000	Sharp peaking control cfg2.
SHARP_PEAKING_CTRL3	0x019C	W	0x00000000	Sharp peaking control cfg3.
SHARP_PEAKING_CTRL4	0x01A0	W	0x00000000	Sharp peaking control cfg4.
SHARP_PEAKING_CTRL5	0x01A4	W	0x00000000	Sharp peaking control cfg5.
SHARP_PEAKING_CTRL6	0x01A8	W	0x00000000	Sharp peaking control cfg6.
SHARP_PEAKING_CTRL7	0x01AC	W	0x00000000	Sharp peaking control cfg7.
SHARP_PEAKING_CTRL8	0x01B0	W	0x00000000	Sharp peaking control cfg8.
SHARP_PEAKING_CTRL9	0x01B4	W	0x00000000	Sharp peaking control cfg9.
SHARP_SHOOT_CTRL0	0x01B8	W	0x00000000	Sharp shoot control cfg0.
SHARP_SHOOT_CTRL1	0x01BC	W	0x00000000	Sharp shoot control cfg1.
SHARP_GAIN_CTRL0	0x01C0	W	0x00000000	Sharp gain control cfg0.
SHARP_GAIN_CTRL1	0x01C4	W	0x00000000	Sharp gain control cfg1.
SHARP_GAIN_CTRL2	0x01C8	W	0x00000000	Sharp gain control cfg2.
SHARP_GAIN_CTRL3	0x01CC	W	0x00000000	Sharp gain control cfg3.
SHARP_GAIN_CTRL4	0x0200	W	0x00000000	Sharp gain control cfg4.
SHARP_GAIN_CTRL5	0x0204	W	0x00000000	Sharp gain control cfg5.
SHARP_GAIN_CTRL6	0x0208	W	0x00000000	Sharp gain control cfg6.

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Name	Offset	Size	Reset Value	Description
SHARP_GAIN_CTRL7	0x020C	W	0x00000000	Sharp gain control cfg7.
SHARP_GAIN_CTRL8	0x0210	W	0x00000000	Sharp gain control cfg8.
SHARP_GAIN_CTRL9	0x0214	W	0x00000000	Sharp gain control cfg9.
SHARP_GAIN_CTRL10	0x0218	W	0x00000000	Sharp gain control cfg10.
SHARP_GAIN_CTRL11	0x021C	W	0x00000000	Sharp gain control cfg11.
SHARP_GAIN_CTRL12	0x0220	W	0x00000000	Sharp gain control cfg12.
SHARP_GAIN_CTRL13	0x0224	W	0x00000000	Sharp gain control cfg13.
SHARP_GAIN_CTRL14	0x0228	W	0x00000000	Sharp gain control cfg14.
SHARP_GAIN_CTRL15	0x022C	W	0x00000000	Sharp gain control cfg15.
SHARP_COLORADJ_CTRL0	0x0230	W	0x00000000	Sharp color adjust control cfg0.
SHARP_COLORADJ_CTRL1	0x0234	W	0x00000000	Sharp color adjust control cfg1.
SHARP_COLORADJ_CTRL2	0x0238	W	0x00000000	Sharp color adjust control cfg2.
SHARP_COLORADJ_CTRL3	0x023C	W	0x00000000	Sharp color adjust control cfg3.
SHARP_COLORADJ_CTRL4	0x0240	W	0x00000000	Sharp color adjust control cfg4.
SHARP_COLORADJ_CTRL5	0x0244	W	0x00000000	Sharp color adjust control cfg5.
SHARP_COLORADJ_CTRL6	0x0248	W	0x00000000	Sharp color adjust control cfg6.
SHARP_COLORADJ_CTRL7	0x024C	W	0x00000000	Sharp color adjust control cfg7.
SHARP_COLORADJ_CTRL8	0x0250	W	0x00000000	Sharp color adjust control cfg8.
SHARP_COLORADJ_CTRL9	0x0254	W	0x00000000	Sharp color adjust control cfg9.
SHARP_COLORADJ_CTRL10	0x0258	W	0x00000000	Sharp color adjust control cfg10.
SHARP_COLORADJ_CTRL11	0x025C	W	0x00000000	Sharp color adjust control cfg11.
SHARP_COLORADJ_CTRL12	0x0260	W	0x00000000	Sharp color adjust control cfg12.
SHARP_COLORADJ_CTRL13	0x0264	W	0x00000000	Sharp color adjust control cfg13.
SHARP_COLORADJ_CTRL14	0x0268	W	0x00000000	Sharp color adjust control cfg14.
SHARP_COLORADJ_CTRL15	0x026C	W	0x00000000	Sharp color adjust control cfg15.
SHARP_TEXTURE_CTRL0	0x0270	W	0x00000000	Sharp texture control cfg0.
SHARP_TEXTURE_CTRL1	0x0274	W	0x00000000	Sharp texture control cfg1.
SHARP_TEXTURE_CTRL2	0x0278	W	0x00000000	Sharp texture control cfg2.
SHARP_TEXTURE_CTRL3	0x027C	W	0x00000000	Sharp texture control cfg3.
SHARP_TEXTURE_CTRL4	0x0280	W	0x00000000	Sharp texture control cfg4.
SHARP_TEXTURE_CTRL5	0x0284	W	0x00000000	Sharp texture control cfg5.
SHARP_LTI_CTRL0	0x0288	W	0x00000000	Sharp lti control cfg0.
SHARP_LTI_CTRL1	0x028C	W	0x00000000	Sharp lti control cfg1.
SHARP_LTI_CTRL2	0x0290	W	0x00000000	Sharp lti control cfg2.
SHARP_LTI_CTRL3	0x0294	W	0x00000000	Sharp lti control cfg3.
SHARP_CTI_CTRL0	0x0298	W	0x00000000	Sharp cti control cfg0.
SHARP_CTI_CTRL1	0x029C	W	0x00000000	Sharp cti control cfg1.
SHARP_DEBUG_CTRL0	0x02A8	W	0x00000000	Debug signals select.

2.4.3 Detail Registers Description

2.4.3.1 DEI

DEI_FRM_START

Address: Operational Base(0x27960000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_dei_frm_en Frame start, Write 1, frame work enable, frame end self clear

DEI_CONFIG0

Address: Operational Base(0x27960000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	sw_dei_init_dis 1'b1: Frame start not initial 1'b0: Frame start initial
21	W1C	0x0	sys_dei_sreset_p Write 1 to global reset dei, auto clear
20	RW	0x0	sw_dei_rst_protect_dis DMA bus error, default protect soft reset 1'b0: Protect reset 1'b1: Direct reset
19:17	RO	0x0	reserved
16	RW	0x0	sw_dei_debug_data_en If assert this bit, the debug signals will have data(just for power saving)
15:14	RO	0x0	reserved
13:12	RW	0x0	sw_dei_dst_yuv_swap 2'b00: SP UV 2'b01: SP VU 2'b10, 2'b11: Reserved
11:10	RO	0x0	reserved
9:8	RW	0x3	sw_dei_dst_fmt 2'b00, 2'b01: Reserved 2'b10: YUV422 2'b11: YUV420
7:6	RO	0x0	reserved
5:4	RW	0x0	sw_dei_src_yuv_swap 2'b00: SP UV 2'b01: SP VU 2'b10, 2'b11: P
3:2	RO	0x0	reserved
1:0	RW	0x3	sw_dei_src_fmt 2'b00,2'b01: Reserved 2'b10: YUV422 2'b11: YUV420

VDPP_WORKING_MODE

Address: Operational Base(0x27960000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	sw_vdpp_working_mode 2'd1: DEI working 2'd2: VEP working 2'd3: DCI working others: IDLE

DEI_QOS_CONFIG

Address: Operational Base(0x27960000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x1	sw_ar_mmu_qos3 QOS for some special channel(MMU and cross 4K ID).
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	sw_dei_awqos_en AW QOS enable bit
0	RW	0x0	sw_dei_arqos_en AR QOS enable bit

DEI_GATING_CTRL

Address: Operational Base(0x27960000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x1	sw_reg_clk_on Reg clk is auto gating, if write 1, clk always on,not gating, also control by sw_dei_clk_on.
10	RW	0x0	sw_dma_clk_on Aclk is auto gating, if write 1, clk always on,not gating, also control by sw_dei_clk_on.
9	RW	0x0	sw_ram_clk_on All ram clk always on 1'b0: Clk gating 1'b1: Clk always on
8	RW	0x0	sw_ctrl_clk_on CTRL clk is auto gating, if write 1, clk always on, not gating, also control by sw_dei_clk_on
7	RW	0x0	sw_out_clk_on OUT clk is auto gating, if write 1, clk always on, not gating, also control by sw_dei_clk_on
6	RW	0x0	sw_ble_clk_on BLE clk is auto gating, if write 1, clk always on, not gating, also control by sw_dei_clk_on
5	RW	0x0	sw_eedi_clk_on EEDI clk is auto gating, if write 1, clk always on, not gating, also control by sw_dei_clk_on
4	RW	0x0	sw_mc_clk_on MC clk is auto gating, if write 1, clk always on, not gating, also control by sw_dei_clk_on
3	RW	0x0	sw_me_clk_on ME clk is auto gating, if write 1, clk always on, not gating, also control by sw_dei_clk_on
2	RW	0x0	sw_dect_clk_on DECT clk is auto gating, if write 1, clk always on, not gating, also control by sw_dei_clk_on
1	RW	0x0	sw_md_clk_on MD clk is auto gating, if write 1, clk always on, not gating, also control by sw_dei_clk_on
0	RW	0x0	sw_dei_clk_on DEI clk is auto gating, if write 1, clk always on, not gating

DEI_STATUS

Address: Operational Base(0x27960000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	ro_arst_finish_done DEI protect safety reset success status, write 1 clear or frame start clear.

DEI_ARQOS_CONFIG

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Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x4	sw_ar_mv_qos ARQOS for MV and ROI
19:16	RW	0x4	sw_ar_md_qos ARQOS for MD
15:12	RW	0x4	sw_ar_uv_qos2 ARQOS for UV channel config when this channel is hurry.
11:8	RW	0x1	sw_ar_uv_qos1 ARQOS for UV channel config when this channel is not hurry.
7:4	RW	0x4	sw_ar_y_qos2 ARQOS for Y channel config when this channel is hurry.
3:0	RW	0x1	sw_ar_y_qos1 ARQOS for Y channel config when this channel is not hurry.

DEI_AWQOS_CONFIG

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x4	sw_aw_id10_qos AW QOS for ID10
11:8	RW	0x4	sw_aw_id9_qos AW QOS for ID9
7:4	RW	0x4	sw_aw_id8_qos AW QOS for ID8
3:0	RW	0x4	sw_aw_id7_qos AW QOS for ID7

DEI_INT_EN

Address: Operational Base(0x27960000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	sw_dei_timeout_int_en Timeout interruption enable
4	RW	0x1	sw_dei_bus_error_en Bus error interruption enable
3:2	RO	0x0	reserved
1	RW	0x0	sw_dei_osd_max_en Frame process OSD detection done interrupt 1'b0: Inactive 1'b1: Active
0	RW	0x1	sw_dei_frm_done_en Frame process done interrupt 1'b0: Inactive 1'b1: Active

DEI_INT_CLR

Address: Operational Base(0x27960000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	W1C	0x0	sw_dei_timeout_int_clr Time out interruption clear
4	W1C	0x0	sw_dei_bus_error_clr Bus error interruption clear
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	W1C	0x0	sw_dei_osd_max_clr OSD max interruption clear
0	W1C	0x0	sw_dei_frm_done_clr Frame process done interrupt clear

DEI_INT_STS

Address: Operational Base(0x27960000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	ro_timeout_sts Timeout error interruption status
4	RO	0x0	ro_bus_error_sts Bus error interruption status
3:2	RO	0x0	reserved
1	RO	0x0	ro_osd_max_sts Frame process OSD detection done interrupt status
0	RO	0x0	ro_frm_done_sts Frame process done interrupt status

DEI_INT_RAW_STS

Address: Operational Base(0x27960000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	ro_timeout_raw Timeout interruption raw status
4	RO	0x0	ro_bus_error_raw Bus error interruption raw status
3:2	RO	0x0	reserved
1	RO	0x0	ro_osd_max_raw OSD max interruption raw status
0	RO	0x0	ro_frm_done_raw Frame done interruption raw status

DEI_VIR_SRC_IMG_WIDTH

Address: Operational Base(0x27960000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dei_src_vir_uv_stride Source uv virtual image width(word align)
15:0	RW	0x0000	sw_dei_src_vir_y_stride Source y virtual image width(word align)

DEI_VIR_DST_IMG_WIDTH

Address: Operational Base(0x27960000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_dei_dst_vir_stride Destination virtual image width(word align)

DEI_SRC_IMG_SIZE

Address: Operational Base(0x27960000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:16	RW	0x000	sw_dei_src_pic_height Source and destination image height(pixel align and need minus 1, for example 1080 need configuration 1079)
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_dei_src_pic_width Source and destination image width(pixel align and need minus 1, for example 1920 need configuration 1919)

DEI_DIL_CONFIG0

Address: Operational Base(0x27960000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x1	sw_dil_mv_hist_en Deinterlace MV histogram enable. 1'b1: Deinterlace need MV histogram 1'b0: MV histogram not work
16	RW	0x0	sw_dil_roi_en Deinterlace ROI function enable bit 1'b1: Deinterlace use ROI mode 1'b0: ROI not work When ROI mode enable,each tile has 4bit for ROI mode 4'b0000: Normal mode 4'b0001: Bypass mode 4'b0010: EEDI only mode 4'b0011: MA only mode 4'b0100: MA MC mode(no cc) 4'b0101: MC EEDI mode 4'b0110:4'b0111:Reserved 4'b1xxx: MC only mode(MC's MV will be appointed by global MV based on ROI[2:0])
15	RW	0x1	sw_dil_comb_en Deinterlace output result combine detection, if is combine block back to original data, else select deinterlace result. 1'b1: Output data combine detection enable 1'b0: Output data not combine detection
14:13	RO	0x0	reserved
12	RW	0x1	sw_dil_memc_en Deinterlace use ME, MC result. 1'b1: ME, MC work enable 1'b0: ME, MC not work enable
11	RW	0x1	sw_dil_osd_en On screen display detection enable. 1'b1: OSD detection enable 1'b0: OSD not detection
10	RW	0x1	sw_dil_pd_en Pulldown detection enable. 1'b1: Pulldown detection enable 1'b0: Pulldown not detection
9	RW	0x1	sw_dil_ff_en Frame field detection work enable. 1'b1: Frame field detection enable 1'b0: Frame field not detection
8	RW	0x1	sw_dil_md_pre_en 1'b1: MD use previous frame data enable 1'b0: MD only use current frame data to calculate MD

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Bit	Attr	Reset Value	Description
7:6	RO	0x0	reserved
5	RW	0x0	sw_dil_field_order Field display order. 1'b0: TFF, top field display first 1'b1: BFF, bottom field display first
4	RW	0x0	sw_dil_out_mode Output deinterlace result to DDR, line mode or tile mode. 1'b0: LINE mode 1'b1: TILE mode
3:0	RW	0x1	sw_dil_mode 4'b0000: DIL disable 4'b0001: I5O2 mode 4'b0010: I5O1T mode 4'b0011: I5O1B mode 4'b0100: I2O2 mode 4'b0101: I1O1T mode 4'b0110: I1O1B mode 4'b0111: Pulldown recovery mode 4'b1000: Bypass mode 4'b1001: Dectect only mode Others: Reserved

DEI_TIMEOUT_CFG

Address: Operational Base(0x27960000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_dei_timeout_en DEI timeout enable
30:0	RW	0x0065b9aa	sw_dei_timeout_cnt When sw_dei_timeout_en ==1, timeout_cnt == sw_dei_timeout_cnt, DEI timeout

DEI_VERSION_INFO

Address: Operational Base(0x27960000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RO	0x2	major Used for IP structure version information
27:20	RO	0x00	minor Big feature change under same structure
19:0	RO	0x00000	svnbuild RTL current SVN number

DEI_DBG_FRM_CNT

Address: Operational Base(0x27960000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	W1C	0x0000	dbg_frm_cnt Self increase one after a frame operation is finished. Write arbitrary value to clear to zero

DEI_DBG_TIMEOUT_CNT

Address: Operational Base(0x27960000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30:0	RO	0x00000000	dbg_timeout_cnt When sw_dei_timeout_en==1, frame counter, frame start auto clear

DEI_SRC_ADDR_CURY

Address: Operational Base(0x27960000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_src_addr_cury Current frame luma address, frame address

DEI_SRC_ADDR_NXTY

Address: Operational Base(0x27960000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_src_addr_nxty Next frame luma addr, frame address

DEI_SRC_ADDR_PREY

Address: Operational Base(0x27960000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_src_addr_prey Start address of source previous image(Y), frame address

DEI_SRC_ADDR_CURUV

Address: Operational Base(0x27960000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_src_addr_curuv Start address of source current image(UV), SP mode UV frame address or U P mode frame address.

DEI_SRC_ADDR_CURV

Address: Operational Base(0x27960000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_src_addr_curv Start address of source current image(V), P mode V frame address

DEI_SRC_ADDR_NXTUV

Address: Operational Base(0x27960000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_src_addr_nxtuv Start address of source next image(UV), SP mode UV frame address or U P mode frame address

DEI_SRC_ADDR_NXTV

Address: Operational Base(0x27960000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_src_addr_nxtv Start address of source next image(V), P mode V frame address

DEI_SRC_ADDR_PREUV

Address: Operational Base(0x27960000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_src_addr_preuv Start address of source previous image(UV),SP mode UV frame address or U P mode frame address

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DEI_SRC_ADDR_PREV

Address: Operational Base(0x27960000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_src_addr_prev Start address of source previous image(V), P mode V frame address

DEI_SRC_ADDR_MD

Address: Operational Base(0x27960000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_src_addr_md Md address, save previous frame MD gradient

DEI_SRC_ADDR_MV

Address: Operational Base(0x27960000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_src_addr_mv Md addr, save previous frame MV

DEI_ROI_ADDR

Address: Operational Base(0x27960000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_addr_roi ROI address base

DEI_DST_ADDR_TOPY

Address: Operational Base(0x27960000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_dst_addr_topy DST top frame luma start address

DEI_DST_ADDR_BOTY

Address: Operational Base(0x27960000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_dst_addr_boty DST bottom frame luma start address

DEI_DST_ADDR_TOPC

Address: Operational Base(0x27960000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_dst_addr_topc DST top frame chroma start address, UV save together

DEI_DST_ADDR_BOTC

Address: Operational Base(0x27960000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_dst_addr_botc DST bottom frame chroma start addr, uv save together

DEI_DST_ADDR_MD

Address: Operational Base(0x27960000) + offset (0x00C0)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_dst_addr_md MD addr, save previous frame md gradt, and also save current frame md grad

DEI_DST_ADDR_MV

Address: Operational Base(0x27960000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dei_dst_addr_mv Output MV addr, save previous frame MV and also save current frame MV

DEI_MD_CONFIG0

Address: Operational Base(0x27960000) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	sw_md_theta GRADtc = CLIP(GRADtf -sw_md_theta, 0, 255);
7:4	RW	0x4	sw_md_r Gradtf *md_r*63/(gradtf*md_r*63 + gradv)
3:0	RW	0x4	sw_md_lambda Current grad * md_lambda/8 + pre grad*(8-md_lambda)/8, value range from 0~8

DEI_DECT_CONFIG0

Address: Operational Base(0x27960000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:24	RW	0x3c	sw_osd_gradv_thr Origial data grad compare with gradv thr, if more than gradv_thr, may be OSD area
23:16	RW	0x3c	sw_osd_gradh_thr Origial data grad compare with gradh thr, if more than gradh_thr, may be OSD area
15:12	RO	0x0	reserved
11:8	RW	0x0	sw_osd_area_num OSD area number, frame field dect, pulldown not detection this area, combine detection also use this value, 0~8
7:0	RW	0x1e	sw_dect_resi_thr For resi to bin, frame field, pulldown, OSD detection use this value

DEI_OSD_LIMIT_CONFIG

Address: Operational Base(0x27960000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	sw_osd_pos_limit_num OSD constrain area detection num, real value = OSD_pos_num+1
3:1	RO	0x0	reserved
0	RW	0x0	sw_osd_pos_limit_en OSD area constrain detection enable

DEI_OSD_LIMIT_AREA0

Address: Operational Base(0x27960000) + offset (0x00F4)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_osd_limit_area0 OSD constrain area 0 [6:0]: OSD constrain area0 x start, 16pixel number [13:7]: OSD constrain area0 x end, 16pixel number [22:14]: OSD constrain area0 y start, 4 pixel number [31:23]: OSD constrain area0 y end, 4 pixel number

DEI_OSD_LIMIT_AREA1

Address: Operational Base(0x27960000) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_osd_limit_area1 OSD limit area 1 [6:0]: OSD constrain area0 x start, 16pixel number [13:7]: OSD constrain area0 x end, 16pixel number [22:14]: OSD constrain area0 y start, 4 pixel number [31:23]: OSD constrain area0 y end, 4 pixel number

DEI_OSD_CONFIG0

Address: Operational Base(0x27960000) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x002	sw_osd_line_num Dect line num should more than OSD_line_num*4, this lines may be OSD area
15:11	RO	0x00	reserved
10:0	RW	0x032	sw_osd_pec_thr A line should more than OSD_per_thr, this line may be OSD area

DEI_OSD_AREA_CONF0

Address: Operational Base(0x27960000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end0 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta0 OSD area y start, 4 pixel number
13:7	RW	0x00	sw_osd_x_end0 OSD area x end, 16pixel number
6:0	RW	0x00	sw_osd_x_sta0 OSD area x start, 16pixel number

DEI_OSD_AREA_CONF1

Address: Operational Base(0x27960000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end1 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta1 OSD area y start, 4 pixel number
13:7	RW	0x00	sw_osd_x_end1 OSD area x end, 16pixel number
6:0	RW	0x00	sw_osd_x_sta1 OSD area x start, 16pixel number

DEI_OSD_AREA_CONF2

Address: Operational Base(0x27960000) + offset (0x0108)

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Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end2 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta2 OSD area y start, 4 pixel number
13:7	RW	0x00	sw_osd_x_end2 OSD area x end, 16pixel number
6:0	RW	0x00	sw_osd_x_sta2 OSD area x start, 16pixel number

DEI_OSD_AREA_CONF3

Address: Operational Base(0x27960000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end3 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta3 OSD area y start, 4 pixel number
13:7	RW	0x00	sw_osd_x_end3 OSD area x end, 16pixel number
6:0	RW	0x00	sw_osd_x_sta3 OSD area x start, 16pixel number

DEI_OSD_AREA_CONF4

Address: Operational Base(0x27960000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end4 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta4 OSD area y start, 4 pixel number
13:7	RW	0x00	sw_osd_x_end4 OSD area x end, 16pixel number
6:0	RW	0x00	sw_osd_x_sta4 OSD area x start, 16pixel number

DEI_OSD_AREA_CONF5

Address: Operational Base(0x27960000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end5 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta5 OSD area y start, 4 pixel number
13:7	RW	0x00	sw_osd_x_end5 OSD area x end, 16pixel number
6:0	RW	0x00	sw_osd_x_sta5 OSD area x start, 16pixel number

DEI_OSD_AREA_CONF6

Address: Operational Base(0x27960000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end6 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta6 OSD area y start, 4 pixel number
13:7	RW	0x00	sw_osd_x_end6 OSD area x end, 16pixel number

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Bit	Attr	Reset Value	Description
6:0	RW	0x00	sw_osd_x_sta6 OSD area x start, 16pixel number

DEI_OSD_AREA_CONF7

Address: Operational Base(0x27960000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end7 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta7 OSD area y start, 4 pixel number
13:7	RW	0x00	sw_osd_x_end7 OSD area x end, 16pixel number
6:0	RW	0x00	sw_osd_x_sta7 OSD area x start, 16pixel number

DEI_ME_CONFIG0

Address: Operational Base(0x27960000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x14	sw_me_thr_offset me_thr = me_thr(from md module) - sw_me_thr_offset . This signal is signed from(-128 ~127)
15:12	RW	0x4	sw_mv_similar_num_thr0 MV similar check result = MV_similar_invld_num < sw_mv_similar_num_thr0
11:8	RW	0x3	sw_mv_similar_thr Surround MV similar = |cur_MV - surround_MV| < sw_mv_similar_thr
7:4	RW	0xa	sw_mv_bonus MVc calc MV,the same MV range value
3:0	RW	0x4	sw_me_pena Balance resi and grad,grad*me_pena/8,me_pena value range from 0~8

DEI_ME_LIMIT_CONFIG

Address: Operational Base(0x27960000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x1b	sw_mv_right_limt MV right range limit, from 0~27, default 27
7:6	RO	0x0	reserved
5:0	RW	0x25	sw_mv_left_limt MV left range limit, from -27~0, default-27

DEI_MV_TRU_LIST0

Address: Operational Base(0x27960000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	sw_mv_tru_list3_mv MV trust list MV3
25	RO	0x0	reserved
24	RW	0x0	sw_mv_tru_list3_vld MV trust list MV3 valid
23:18	RW	0x00	sw_mv_tru_list2_mv MV trust list MV2
17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	sw_mv_tru_list2_vld MV trust list MV2 valid
15:10	RW	0x00	sw_mv_tru_list1_mv MV trust list MV1
9	RO	0x0	reserved
8	RW	0x0	sw_mv_tru_list1_vld MV trust list MV1 valid
7:2	RW	0x00	sw_mv_tru_list0_mv MV trust list MV0
1	RO	0x0	reserved
0	RW	0x0	sw_mv_tru_list0_vld MV trust list MV0 valid

DEI_MV_TRU_LIST1

Address: Operational Base(0x27960000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	sw_mv_tru_list7_mv MV trust list MV7
25	RO	0x0	reserved
24	RW	0x0	sw_mv_tru_list7_vld MV trust list MV7 valid
23:18	RW	0x00	sw_mv_tru_list6_mv MV trust list MV6
17	RO	0x0	reserved
16	RW	0x0	sw_mv_tru_list6_vld MV trust list MV6 valid
15:10	RW	0x00	sw_mv_tru_list5_mv MV trust list MV5
9	RO	0x0	reserved
8	RW	0x0	sw_mv_tru_list5_vld MV trust list MV5 valid
7:2	RW	0x00	sw_mv_tru_list4_mv MV trust list MV4
1	RO	0x0	reserved
0	RW	0x0	sw_mv_tru_list4_vld MV trust list MV4 valid

DEI_EEDI_CONFIG0

Address: Operational Base(0x27960000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0c	sw_eedi_thr0 EEDI thr0

DEI_BLE_CONFIG0

Address: Operational Base(0x27960000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x1	sw_ble_backtoma_num Left and right column of frame will back to MA, give up MC

DEI_COMB_CONFIG0

Address: Operational Base(0x27960000) + offset (0x0138)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	sw_comb_cnt_thr Top or bottom frame combine detection compare with original combine dect
23:22	RO	0x0	reserved
21:16	RW	0x10	sw_comb_feature_thr Top or bottom frame combine detection compare with original combine dect
15:8	RW	0x04	sw_comb_t_thr Different line compare use comb_t_thr
7:0	RW	0xff	sw_comb_osd_vld OSD area detection combine block back to original [0] area0,[1]area1....[7]area7 1'b1: Back to original 1'b0: Not back to original

DEI_DIL_MTN_TAB0

Address: Operational Base(0x27960000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab03 The MTN table member of number 03
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab02 The MTN table member of number 02
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab01 The MTN table member of number 01
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab00 The MTN table member of number 00

DEI_DIL_MTN_TAB1

Address: Operational Base(0x27960000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab07 The MTN table member of number 07
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab06 The MTN table member of number 06
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab05 The MTN table member of number 05
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab04 The MTN table member of number 04

DEI_DIL_MTN_TAB2

Address: Operational Base(0x27960000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab11 The MTN table member of number 11

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Bit	Attr	Reset Value	Description
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab10 The MTN table member of number 10
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab09 The MTN table member of number 09
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab08 The MTN table member of number 08

DEI_DIL_MTN_TAB3

Address: Operational Base(0x27960000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab15 The MTN table member of number 15
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab14 The MTN table member of number 14
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab13 The MTN table member of number 13
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab12 The MTN table member of number 12

DEI_DIL_MTN_TAB4

Address: Operational Base(0x27960000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x01	sw_mtn_sub_tab19 The MTN table member of number 19
23	RO	0x0	reserved
22:16	RW	0x01	sw_mtn_sub_tab18 The MTN table member of number 18
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab17 The MTN table member of number 17
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab16 The MTN table member of number 16

DEI_DIL_MTN_TAB5

Address: Operational Base(0x27960000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x06	sw_mtn_sub_tab23 The MTN table member of number 23
23	RO	0x0	reserved
22:16	RW	0x05	sw_mtn_sub_tab22 The MTN table member of number 22
15	RO	0x0	reserved
14:8	RW	0x03	sw_mtn_sub_tab21 The MTN table member of number 21

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Bit	Attr	Reset Value	Description
7	RO	0x0	reserved
6:0	RW	0x02	sw_mtn_sub_tab20 The MTN table member of number 20

DEI_DIL_MTN_TAB6

Address: Operational Base(0x27960000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x0f	sw_mtn_sub_tab27 The MTN table member of number 27
23	RO	0x0	reserved
22:16	RW	0x0d	sw_mtn_sub_tab26 The MTN table member of number 26
15	RO	0x0	reserved
14:8	RW	0x0a	sw_mtn_sub_tab25 The MTN table member of number 25
7	RO	0x0	reserved
6:0	RW	0x08	sw_mtn_sub_tab24 The MTN table member of number 24

DEI_DIL_MTN_TAB7

Address: Operational Base(0x27960000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x1c	sw_mtn_sub_tab31 The MTN table member of number 31
23	RO	0x0	reserved
22:16	RW	0x19	sw_mtn_sub_tab30 The MTN table member of number 30
15	RO	0x0	reserved
14:8	RW	0x15	sw_mtn_sub_tab29 The MTN table member of number 29
7	RO	0x0	reserved
6:0	RW	0x12	sw_mtn_sub_tab28 The MTN table member of number 28

DEI_DIL_MTN_TAB8

Address: Operational Base(0x27960000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x2b	sw_mtn_sub_tab35 The MTN table member of number 35
23	RO	0x0	reserved
22:16	RW	0x28	sw_mtn_sub_tab34 The MTN table member of number 34
15	RO	0x0	reserved
14:8	RW	0x24	sw_mtn_sub_tab33 The MTN table member of number 33
7	RO	0x0	reserved
6:0	RW	0x20	sw_mtn_sub_tab32 The MTN table member of number 32

DEI_DIL_MTN_TAB9

Address: Operational Base(0x27960000) + offset (0x0164)

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Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x36	sw_mtn_sub_tab39 The MTN table member of number 39
23	RO	0x0	reserved
22:16	RW	0x34	sw_mtn_sub_tab38 The MTN table member of number 38
15	RO	0x0	reserved
14:8	RW	0x31	sw_mtn_sub_tab37 The MTN table member of number 37
7	RO	0x0	reserved
6:0	RW	0x2e	sw_mtn_sub_tab36 The MTN table member of number 36

DEI_DIL_MTN_TAB10

Address: Operational Base(0x27960000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x3d	sw_mtn_sub_tab43 The MTN table member of number 43
23	RO	0x0	reserved
22:16	RW	0x3c	sw_mtn_sub_tab42 The MTN table member of number 42
15	RO	0x0	reserved
14:8	RW	0x3a	sw_mtn_sub_tab41 The MTN table member of number 41
7	RO	0x0	reserved
6:0	RW	0x38	sw_mtn_sub_tab40 The MTN table member of number 40

DEI_DIL_MTN_TAB11

Address: Operational Base(0x27960000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab47 The MTN table member of number 47
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab46 The MTN table member of number 46
15	RO	0x0	reserved
14:8	RW	0x3f	sw_mtn_sub_tab45 The MTN table member of number 45
7	RO	0x0	reserved
6:0	RW	0x3e	sw_mtn_sub_tab44 The MTN table member of number 44

DEI_DIL_MTN_TAB12

Address: Operational Base(0x27960000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab51 The MTN table member of number 51
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab50 The MTN table member of number 50

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Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab49 The MTN table member of number 49
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab48 The MTN table member of number 48

DEI_DIL_MTN_TAB13

Address: Operational Base(0x27960000) + offset (0x0174)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab55 The MTN table member of number 55
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab54 The MTN table member of number 54
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab53 The MTN table member of number 53
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab52 The MTN table member of number 52

DEI_DIL_MTN_TAB14

Address: Operational Base(0x27960000) + offset (0x0178)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab59 The MTN table member of number 59
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab58 The MTN table member of number 58
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab57 The MTN table member of number 57
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab56 The MTN table member of number 56

DEI_DIL_MTN_TAB15

Address: Operational Base(0x27960000) + offset (0x017C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab63 The MTN table member of number 63
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab62 The MTN table member of number 62
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab61 The MTN table member of number 61
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab60 The MTN table member of number 60

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DEI_RO_PD_TCNT

Address: Operational Base(0x27960000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	ro_dect_pd_tcnt Pulldown detection top field counter

DEI_RO_PD_BCNT

Address: Operational Base(0x27960000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	ro_dect_pd_bcnt Pulldown detection bottom field counter

DEI_RO_FF_CUR_TCNT

Address: Operational Base(0x27960000) + offset (0x0408)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_cur_tcnt Frame field detection current frame top field counter

DEI_RO_FF_CUR_BCNT

Address: Operational Base(0x27960000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_cur_bcnt Frame field detection current frame bottom field counter

DEI_RO_FF_NXT_TCNT

Address: Operational Base(0x27960000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_nxt_tcnt Frame field detection next frame top field counter

DEI_RO_FF_NXT_BCNT

Address: Operational Base(0x27960000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_nxt_bcnt Frame field detection next frame bottom field counter

DEI_RO_FF_BLE_TCNT

Address: Operational Base(0x27960000) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_ble_tcnt Frame field detection current and next frame blend top field counter

DEI_RO_FF_BLE_BCNT

Address: Operational Base(0x27960000) + offset (0x041C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_ble_bcnt Frame field detection current and next frame blend bottom field counter

DEI_RO_FF_COMB_NZ

Address: Operational Base(0x27960000) + offset (0x0420)

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Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RO	0x000000	ro_dect_ff_nz Frame field detection current frame none zero number

DEI_RO_FF_COMB_F

Address: Operational Base(0x27960000) + offset (0x0424)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RO	0x000000	ro_dect_ff_comb_f Frame field detection current frame combine detection number

DEI_RO_OSD_NUM

Address: Operational Base(0x27960000) + offset (0x0428)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	ro_dect_osd_cnt OSD area detection number

DEI_RO_OUT_COMB_CNT

Address: Operational Base(0x27960000) + offset (0x042C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_out_osd_comb_cnt Top frame and bottom frame OSD area combine number
15:0	RO	0x0000	ro_out_comb_cnt Top frame and bottom frame combine number

DEI_RO_FF_GRADT_TCNT

Address: Operational Base(0x27960000) + offset (0x0430)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_ff_gradt_tcnt Frame field detection,gradt top field counter

DEI_RO_FF_GRADT_BCNT

Address: Operational Base(0x27960000) + offset (0x0434)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_ff_gradt_bcnt Frame field detection,gradt bottom field counter

DEI_RO_MC_VLD_CNT

Address: Operational Base(0x27960000) + offset (0x0438)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RO	0x0000	ro_mc_vld_cnt OSD area detection number

DEI_RO_OSD_AREA0_X

Address: Operational Base(0x27960000) + offset (0x0440)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end0 1 pixel
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:0	RO	0x000	ro_x_sta0 1 pixel

DEI_RO_OSD_AREA0_Y

Address: Operational Base(0x27960000) + offset (0x0444)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end0 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta0 1 pixel

DEI_RO_OSD_AREA1_X

Address: Operational Base(0x27960000) + offset (0x0448)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end1 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta1 1 pixel

DEI_RO_OSD_AREA1_Y

Address: Operational Base(0x27960000) + offset (0x044C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end1 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta1 1 pixel

DEI_RO_OSD_AREA2_X

Address: Operational Base(0x27960000) + offset (0x0450)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end2 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta2 1 pixel

DEI_RO_OSD_AREA2_Y

Address: Operational Base(0x27960000) + offset (0x0454)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end2 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta2 1 pixel

DEI_RO_OSD_AREA3_X

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Address: Operational Base(0x27960000) + offset (0x0458)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end3 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta3 1 pixel

DEI_RO_OSD_AREA3_Y

Address: Operational Base(0x27960000) + offset (0x045C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end3 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta3 1 pixel

DEI_RO_OSD_AREA4_X

Address: Operational Base(0x27960000) + offset (0x0460)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end4 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta4 1 pixel

DEI_RO_OSD_AREA4_Y

Address: Operational Base(0x27960000) + offset (0x0464)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end4 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta4 1 pixel

DEI_RO_OSD_AREA5_X

Address: Operational Base(0x27960000) + offset (0x0468)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end5 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta5 1 pixel

DEI_RO_OSD_AREA5_Y

Address: Operational Base(0x27960000) + offset (0x046C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end5 1 pixel

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Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta5 1 pixel

DEI_RO_OSD_AREA6_X

Address: Operational Base(0x27960000) + offset (0x0470)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end6 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta6 1 pixel

DEI_RO_OSD_AREA6_Y

Address: Operational Base(0x27960000) + offset (0x0474)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end6 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta6 1 pixel

DEI_RO_OSD_AREA7_X

Address: Operational Base(0x27960000) + offset (0x0478)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end7 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta7 1 pixel

DEI_RO_OSD_AREA7_Y

Address: Operational Base(0x27960000) + offset (0x047C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end7 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta7 1 pixel

DEI_RO_MV_HIST_BIN0

Address: Operational Base(0x27960000) + offset (0x0480)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist01 Mv_histogram01
15:0	RO	0x0000	ro_mv_hist00 Mv_histogram00

DEI_RO_MV_HIST_BIN1

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Address: Operational Base(0x27960000) + offset (0x0484)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist03 Mv_histogram03
15:0	RO	0x0000	ro_mv_hist02 Mv_histogram02

DEI_RO_MV_HIST_BIN2

Address: Operational Base(0x27960000) + offset (0x0488)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist05 Mv_histogram05
15:0	RO	0x0000	ro_mv_hist04 Mv_histogram04

DEI_RO_MV_HIST_BIN3

Address: Operational Base(0x27960000) + offset (0x048C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist07 Mv_histogram07
15:0	RO	0x0000	ro_mv_hist06 Mv_histogram06

DEI_RO_MV_HIST_BIN4

Address: Operational Base(0x27960000) + offset (0x0490)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist09 Mv_histogram09
15:0	RO	0x0000	ro_mv_hist08 Mv_histogram08

DEI_RO_MV_HIST_BIN5

Address: Operational Base(0x27960000) + offset (0x0494)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist11 Mv_histogram11
15:0	RO	0x0000	ro_mv_hist10 Mv_histogram10

DEI_RO_MV_HIST_BIN6

Address: Operational Base(0x27960000) + offset (0x0498)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist13 Mv_histogram13
15:0	RO	0x0000	ro_mv_hist12 Mv_histogram12

DEI_RO_MV_HIST_BIN7

Address: Operational Base(0x27960000) + offset (0x049C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist15 Mv_histogram15
15:0	RO	0x0000	ro_mv_hist14 Mv_histogram14

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DEI_RO_MV_HIST_BIN8

Address: Operational Base(0x27960000) + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist17 Mv_histogram17
15:0	RO	0x0000	ro_mv_hist16 Mv_histogram16

DEI_RO_MV_HIST_BIN9

Address: Operational Base(0x27960000) + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist19 Mv_histogram19
15:0	RO	0x0000	ro_mv_hist18 Mv_histogram18

DEI_RO_MV_HIST_BIN10

Address: Operational Base(0x27960000) + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist21 Mv_histogram21
15:0	RO	0x0000	ro_mv_hist20 Mv_histogram20

DEI_RO_MV_HIST_BIN11

Address: Operational Base(0x27960000) + offset (0x04AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist23 Mv_histogram23
15:0	RO	0x0000	ro_mv_hist22 Mv_histogram22

DEI_RO_MV_HIST_BIN12

Address: Operational Base(0x27960000) + offset (0x04B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist25 Mv_histogram25
15:0	RO	0x0000	ro_mv_hist24 Mv_histogram24

DEI_RO_MV_HIST_BIN13

Address: Operational Base(0x27960000) + offset (0x04B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist27 Mv_histogram27
15:0	RO	0x0000	ro_mv_hist26 Mv_histogram26

DEI_RO_MV_HIST_BIN14

Address: Operational Base(0x27960000) + offset (0x04B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist29 Mv_histogram29

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	ro_mv_hist28 Mv_histogram28

DEI_RO_MV_HIST_BIN15

Address: Operational Base(0x27960000) + offset (0x04BC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist31 Mv_histogram31
15:0	RO	0x0000	ro_mv_hist30 Mv_histogram30

DEI_RO_MV_HIST_BIN16

Address: Operational Base(0x27960000) + offset (0x04C0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist33 Mv_histogram33
15:0	RO	0x0000	ro_mv_hist32 Mv_histogram32

DEI_RO_MV_HIST_BIN17

Address: Operational Base(0x27960000) + offset (0x04C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist35 Mv_histogram35
15:0	RO	0x0000	ro_mv_hist34 Mv_histogram34

DEI_RO_MV_HIST_BIN18

Address: Operational Base(0x27960000) + offset (0x04C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist37 Mv_histogram37
15:0	RO	0x0000	ro_mv_hist36 Mv_histogram36

DEI_RO_MV_HIST_BIN19

Address: Operational Base(0x27960000) + offset (0x04CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist39 Mv_histogram39
15:0	RO	0x0000	ro_mv_hist38 Mv_histogram38

DEI_RO_MV_HIST_BIN20

Address: Operational Base(0x27960000) + offset (0x04D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist41 Mv_histogram41
15:0	RO	0x0000	ro_mv_hist40 Mv_histogram40

DEI_RO_MV_HIST_BIN21

Address: Operational Base(0x27960000) + offset (0x04D4)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist43 Mv_histogram43
15:0	RO	0x0000	ro_mv_hist42 Mv_histogram42

DEI_RO_MV_HIST_BIN22

Address: Operational Base(0x27960000) + offset (0x04D8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist45 Mv_histogram45
15:0	RO	0x0000	ro_mv_hist44 Mv_histogram44

DEI_RO_MV_HIST_BIN23

Address: Operational Base(0x27960000) + offset (0x04DC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist47 Mv_histogram47
15:0	RO	0x0000	ro_mv_hist46 Mv_histogram46

DEI_RO_MV_HIST_BIN24

Address: Operational Base(0x27960000) + offset (0x04E0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist49 Mv_histogram49
15:0	RO	0x0000	ro_mv_hist48 Mv_histogram48

DEI_RO_MV_HIST_BIN25

Address: Operational Base(0x27960000) + offset (0x04E4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist51 Mv_histogram51
15:0	RO	0x0000	ro_mv_hist50 Mv_histogram50

DEI_RO_MV_HIST_BIN26

Address: Operational Base(0x27960000) + offset (0x04E8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist53 Mv_histogram54
15:0	RO	0x0000	ro_mv_hist52 Mv_histogram53

DEI_RO_MV_HIST_BIN27

Address: Operational Base(0x27960000) + offset (0x04EC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist55 Mv_histogram55
15:0	RO	0x0000	ro_mv_hist54 Mv_histogram54

DEI_PERF_LATENCY_CTRL0

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Address: Operational Base(0x27960000) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:8	RW	0x000	sw_rd_latency_thr Axi Read latency threshold
7:4	RW	0x0	sw_rd_latency_id Axi read channel id for latency AXI_PERF test
3	RW	0x0	sw_axi_cnt_type 1'b0: AXI transfer test 1'b1: DDR align transfer test
2	RW	0x0	sw_axi_perf_frm_type 1'b0: Clear by software configuration 1'b1: Clear by frame end or by software configuration
1	RW	0x0	sw_axi_perf_clr_e 1'b0: Software clear disable 1'b1: Software clear enalbe Note: user need write 1 to this bit and then write 0 to generate a clear pulse
0	RW	0x0	sw_axi_perf_work_e 1'b0: Disable 1'b1: Enable

DEI_PERF_LATENCY_CTRL1

Address: Operational Base(0x27960000) + offset (0x0604)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	sw_aw_count_id When sw_aw_cnt_id_type=1, only count the id designated by sw_aw_count_id
7:4	RW	0x0	sw_ar_count_id When sw_ar_cnt_id_type=1, only count the id designated by sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type 1'b0: Count all write channels 1'b1: Count sw_aw_count_id write channel only
2	RW	0x0	sw_ar_cnt_id_type 1'b0: Count all read channels 1'b1: Count sw_ar_count_id read channel only
1:0	RW	0x0	sw_addr_align_type 2'b00: 16-Byte align 2'b01: 32-Byte align 2'b10: 64-Byte align 2'b11: 128-Byte align

DEI_PERF_RD_MAX_LATENCY_NUM

Address: Operational Base(0x27960000) + offset (0x0608)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	rd_max_latency_num AXI max read latency(unit: cycles)

DEI_PERF_RD_LATENCY_SAMP_NUM

Address: Operational Base(0x27960000) + offset (0x060C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_thr_num AXI read latency total sample number

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DEI_PERF_RD_LATENCY_ACC_SUM

Address: Operational Base(0x27960000) + offset (0x0610)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_acc_sum AXI read latency (>sw_rd_latency_thr) total number

DEI_PERF_RD_AXI_TOTAL_BYTE

Address: Operational Base(0x27960000) + offset (0x0614)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	perf_rd_axi_total_byte AXI active total read bytes/DDR align read bytes

DEI_PERF_WR_AXI_TOTAL_BYTE

Address: Operational Base(0x27960000) + offset (0x0618)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	perf_wr_axi_total_byte AXI active total write bytes/ddr align write bytes

DEI_PERF_WORKING_CNT

Address: Operational Base(0x27960000) + offset (0x061C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	perf_working_cnt RKIP working counter

DEI_MMU_DTE_ADDR

Address: Operational Base(0x27960000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr MMU dte address

DEI_MMU_STATUS

Address: Operational Base(0x27960000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RW	0x00	mmu_page_fault_bus_id Index of master responsible for the last page fault
5	RW	0x0	mmu_page_fault_is_write The direction of access for last page fault. 1'b0: Read 1'b1: Write
4	RW	0x1	mmu_replay_buffer_empty The MMU replay buffer is empty
3	RW	0x1	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated access. The MMU_IDLE signal only reports idle when the MMU processor is idle and accesses are active on the external bus. Note: The MMU can be idle in page fault mode.
2	RW	0x0	mmu_stall_active MMU stall mode currently enabled. The mode is enabled by command
1	RW	0x0	mmu_page_fault_active MMU page fault mode currently enabled. The mode is enabled by command

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Bit	Attr	Reset Value	Description
0	RW	0x0	mmu_paging_enabled MMU page enable

DEI_MMU_CMD

Address: Operational Base(0x27960000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	mmu_cmd The MMU_ENABLE_STALL command can always be issued. Other commands are ignored unless the MMU is idle or stalled. 3'b000: Enable paging 3'b001: Disable paging 3'b010: Turn on stall mode 3'b011: Turn off stall mode 3'b100: Zap the entire page table cache 3'b101: Leave page fault mode 3'b110: Reset the MMU

DEI_MMU_PAGE_FAULT_ADDR

Address: Operational Base(0x27960000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_page_fault_addr mmu_page_fault_address

DEI_MMU_ZAP_ONE_LINE

Address: Operational Base(0x27960000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mmu_zap_one_line Address to be invalidated from the page table cache

DEI_MMU_INT_RAWSTAT

Address: Operational Base(0x27960000) + offset (0x0814)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error MMU read bus error
0	RW	0x0	page_fault Page fault

DEI_MMU_INT_CLEAR

Address: Operational Base(0x27960000) + offset (0x0818)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error_clear Read bus error interrupt clear. write 1 to this register can clear read bus error interrupt.
0	RW	0x0	page_fault_clear Page fault interrupt clear, write 1 to this register can clear page fault interrupt

DEI_MMU_INT_MASK

Address: Operational Base(0x27960000) + offset (0x081C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	read_bus_error_int_en MMU read bus error interruption enable
0	RW	0x0	page_fault_int_en PAGE fault interruption enable

DEI_MMU_INT_STATUS

Address: Operational Base(0x27960000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error MMU read bus error
0	RW	0x0	page_fault Page fault

DEI_MMU_AUTO_GATING

Address: Operational Base(0x27960000) + offset (0x0824)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	mmu_auto_gating When it is 1, the MMU will auto gating itself

DEI_MMU_ID

Address: Operational Base(0x27960000) + offset (0x0828)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	mmu_axi_id MMU ID configurable
3:1	RO	0x0	reserved
0	RW	0x0	reg_load_mmu_en Just for frame asynchronous using

2.4.3.2 VEP

VEP_FRM_START

Address: Operational Base(0x27961000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_vep_frm_en Frame start, Write 1, frame work enable, frame end self clear

VEP_CONFIG0

Address: Operational Base(0x27961000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	sw_dci_en DCI module enable bit
24	RW	0x0	sw_vep_dmsr_en DMSR module enable bit
23	RO	0x0	reserved
22	RW	0x0	sw_vep_init_dis 1'b0: Frame start initial 1'b1: Frame start not initial
21	W1C	0x0	sys_vep_sreset_p Write 1 to global reset vep, auto clear

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Bit	Attr	Reset Value	Description
20	RW	0x0	sw_vep_rst_protect_dis DMA bus error, default protect soft reset 1'b0: Protect reset 1'b1: Direct reset
19:17	RO	0x0	reserved
16	RW	0x0	sw_vep_debug_data_en If assert this bit, the debug signals will have data(just for power saving)
15:14	RO	0x0	reserved
13:12	RW	0x0	sw_vep_dst_yuv_swap 2'b00: SP UV (default NV12 [U0V0U1V1]) 2'b01: SP VU 2'b10, 2'b11: Reserved
11	RO	0x0	reserved
10	RW	0x0	sw_vep_yuvout_diff_en 1'b0: old mode, Y and UV output same resolution 1'b1: new mode, Y and UV output different resolution
9:8	RW	0x3	sw_vep_dst_fmt 2'b00: YUV444 2'b01,2'b10: Reserved 2'b11: YUV420
7:6	RO	0x0	reserved
5:4	RW	0x0	sw_vep_src_yuv_swap 2'b00: SP UV (default NV12 [U0V0U1V1]) 2'b01: SP VU 2'b10, 2'b11: Reserved
3:2	RO	0x0	reserved
1:0	RW	0x3	sw_vep_src_fmt 2'b00,2'b01,2'b10: Reserved 2'b11: YUV420

VDPP_WORKING_MODE

Address: Operational Base(0x27961000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	sw_vdpp_working_mode 2'd1: IEP2 working 2'd2: VEP working 2'd3: DCI working others: IDLE

VEP_QOS_CONFIG

Address: Operational Base(0x27961000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x1	sw_ar_mmu_qos3 QOS for some special channel(MMU and cross 4K ID).
3:2	RO	0x0	reserved
1	RW	0x0	sw_vep_awqos_en AW QOS enable bit
0	RW	0x0	sw_vep_arqos_en AR QOS enable bit

VEP_GATING_CTRL

Address: Operational Base(0x27961000) + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x1	sw_reg_clk_on Reg clk is auto gating, if write 1, clk always on,not gating, also control by sw_vep_clk_on.
10	RW	0x0	sw_dma_clk_on Aclk is auto gating, if write 1, clk always on,not gating, also control by sw_vep_clk_on.
9	RW	0x0	sw_ram_clk_on All ram clk always on 1'b0: Clk gating 1'b1: Clk always on
8	RW	0x0	sw_ctrl_clk_on CTRL clk is auto gating, if write 1, clk always on, not gating, also control by sw_vep_clk_on
7:1	RO	0x00	reserved
0	RW	0x0	sw_vep_clk_on VEP clk is auto gating, if write 1, clk always on, not gating

VEP_STATUS

Address: Operational Base(0x27961000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	ro_arst_finish_done VEP protect safety reset success status, write 1 clear or frame start clear.

VEP_ARQOS_CONFIG

Address: Operational Base(0x27961000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x4	sw_ar_uv_qos2 ARQOS for UV channel config when this channel is hurry.
11:8	RW	0x1	sw_ar_uv_qos1 ARQOS for UV channel config when this channel is not hurry.
7:4	RW	0x4	sw_ar_y_qos2 ARQOS for Y channel config when this channel is hurry.
3:0	RW	0x1	sw_ar_y_qos1 ARQOS for Y channel config when this channel is not hurry.

VEP_AWQOS_CONFIG

Address: Operational Base(0x27961000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x4	sw_aw_id10_qos AW QOS for ID10
11:8	RW	0x4	sw_aw_id9_qos AW QOS for ID9
7:4	RW	0x4	sw_aw_id8_qos AW QOS for ID8
3:0	RW	0x4	sw_aw_id7_qos AW QOS for ID7

VEP_INT_EN

Address: Operational Base(0x27961000) + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x1	sw_vep_config_error_en Timeout interruption enable
5	RW	0x0	sw_vep_timeout_int_en Timeout interruption enable
4	RW	0x1	sw_vep_bus_error_en Bus error interruption enable
3:2	RO	0x0	reserved
1	RW	0x0	sw_vep_osd_max_en Frame process OSD detection done interrupt 1'b0: Inactive 1'b1: Active
0	RW	0x1	sw_vep_frm_done_en Frame process done interrupt 1'b0: Inactive 1'b1: Active

VEP_INT_CLR

Address: Operational Base(0x27961000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	W1C	0x0	sw_vep_config_error_clr Bus error interruption clear
5	W1C	0x0	sw_vep_timeout_int_clr Time out interruption clear
4	W1C	0x0	sw_vep_bus_error_clr Bus error interruption clear
3:2	RO	0x0	reserved
1	W1C	0x0	sw_vep_osd_max_clr OSD max interruption clear
0	W1C	0x0	sw_vep_frm_done_clr Frame process done interrupt clear

VEP_INT_STS

Address: Operational Base(0x27961000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	ro_config_error_sts Bus error interruption status
5	RO	0x0	ro_timeout_sts Timeout error interruption status
4	RO	0x0	ro_bus_error_sts Bus error interruption status
3:2	RO	0x0	reserved
1	RO	0x0	ro_osd_max_sts Frame process OSD detection done interrupt status
0	RO	0x0	ro_frm_done_sts Frame process done interrupt status

VEP_INT_RAW_STS

Address: Operational Base(0x27961000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	ro_config_error_raw Bus error interruption raw status

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Bit	Attr	Reset Value	Description
5	RO	0x0	ro_timeout_raw Timeout interruption raw status
4	RO	0x0	ro_bus_error_raw Bus error interruption raw status
3:2	RO	0x0	reserved
1	RO	0x0	ro_osd_max_raw OSD max interruption raw status
0	RO	0x0	ro_frm_done_raw Frame done interruption raw status

VEP_VIR_SRC_IMG_WIDTH

Address: Operational Base(0x27961000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_vep_src_vir_y_stride Source y virtual image width(word align)

VEP_VIR_DST_IMG_WIDTH

Address: Operational Base(0x27961000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_vep_dst_vir_c_stride Destination UV channel virtual image width(word unit, only used when sw_vep_yuvout_diff_en open)
15:0	RW	0x0000	sw_vep_dst_vir_y_stride Destination virtual image width(word align)

VEP_SRC_IMG_SIZE

Address: Operational Base(0x27961000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	sw_vep_src_down_redundant This signal must even, biggist is 6. When this signal not equal to 0, the RTL will do copy the last line to redundant line.
27	RO	0x0	reserved
26:16	RW	0x000	sw_vep_src_pic_height Source image height(pixel align and need minus 1, for example 1080 need configuration 1079)
15:12	RW	0x0	sw_vep_src_right_redundant This signal must even, biggist is 14. When this signal not equal to 0, the RTL will do copy the last pixel to redundant pixel.
11	RO	0x0	reserved
10:0	RW	0x000	sw_vep_src_pic_width Source image width(pixel align and need minus 1, for example 1920 need configuration 1919)

VEP_DST_IMG_SIZE

Address: Operational Base(0x27961000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_vep_dst_pic_height Destination image height(pixel align and need minus 1, for example 1080 need configuration 1079)

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	sw_vep_dst_right_redundant This signal must even, biggist is 14. When this signal not equal to 0, the RTL will add 0 to redundant pixel.
11	RO	0x0	reserved
10:0	RW	0x000	sw_vep_dst_pic_width Destination image width(pixel align and need minus 1, for example 1920 need configuration 1919)

VEP_DST_IMG_SIZE_C

Address: Operational Base(0x27961000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_vep_dst_pic_height_c Destination image uv height(pixel align and need minus 1, for example 1080 need configuration 1079)(only used when sw_vep_yuvout_diff_en open)
15:12	RW	0x0	sw_vep_dst_right_redundant_c This signal must even, biggist is 14(only used when sw_vep_yuvout_diff_en open). When this signal not equal to 0, the RTL will add 0 to redundant pixel.
11	RO	0x0	reserved
10:0	RW	0x000	sw_vep_dst_pic_width_c Destination image uv width(pixel align and need minus 1, for example 1920 need configuration 1919) (only used when sw_vep_yuvout_diff_en open)

VEP_TIMEOUT_CFG

Address: Operational Base(0x27961000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_vep_timeout_en vep timeout enable
30:0	RW	0x0065b9aa	sw_vep_timeout_cnt When sw_vep_timeout_en ==1, timeout_cnt == sw_vep_timeout_cnt, vep timeout

VEP_VERSION_INFO

Address: Operational Base(0x27961000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RO	0x2	major Used for IP structure version information
27:20	RO	0x00	minor Big feature change under same structure
19:0	RO	0x00000	svnbuild RTL current SVN number

VEP_DBG_FRM_CNT

Address: Operational Base(0x27961000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	W1C	0x0000	dbg_frm_cnt Self increase one after a frame operation is finished. Write arbitrary value to clear to zero

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VEP_SRC_ADDR_Y

Address: Operational Base(0x27961000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_vep_src_addr_y Frame luma address, frame address

VEP_SRC_ADDR_UV

Address: Operational Base(0x27961000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_vep_src_addr_uv Frame UV address

VEP_DST_ADDR_Y

Address: Operational Base(0x27961000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_vep_dst_addr_y Frame luma address, frame address

VEP_DST_ADDR_UV

Address: Operational Base(0x27961000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_vep_dst_addr_uv Frame UV address

VEP_DMSR_EDGE_THRE0

Address: Operational Base(0x27961000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dmsr_edge_high_thre_0 High threshold for edgeness linear mapping 0
15:0	RW	0x0000	sw_dmsr_edge_low_thre_0 Low threshold for edgeness linear mapping 0

VEP_DMSR_EDGE_THRE1

Address: Operational Base(0x27961000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dmsr_edge_high_thre_1 High threshold for edgeness linear mapping 1
15:0	RW	0x0000	sw_dmsr_edge_low_thre_1 Low threshold for edgeness linear mapping 1

VEP_DMSR_EDGE_THRE2

Address: Operational Base(0x27961000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dmsr_edge_high_thre_2 High threshold for edgeness linear mapping 2
15:0	RW	0x0000	sw_dmsr_edge_low_thre_2 Low threshold for edgeness linear mapping 2

VEP_DMSR_EDGE_THRE3

Address: Operational Base(0x27961000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dmsr_edge_high_thre_3 High threshold for edgeness linear mapping 3
15:0	RW	0x0000	sw_dmsr_edge_low_thre_3 Low threshold for edgeness linear mapping 3

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VEP_DMSR_EDGE_THRE4

Address: Operational Base(0x27961000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dmsr_edge_high_thre_4 High threshold for edgeness linear mapping 4
15:0	RW	0x0000	sw_dmsr_edge_low_thre_4 Low threshold for edgeness linear mapping 4

VEP_DMSR_EDGE_THRE5

Address: Operational Base(0x27961000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dmsr_edge_high_thre_5 High threshold for edgeness linear mapping 5
15:0	RW	0x0000	sw_dmsr_edge_low_thre_5 Low threshold for edgeness linear mapping 5

VEP_DMSR_EDGE_THRE6

Address: Operational Base(0x27961000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dmsr_edge_high_thre_6 High threshold for edgeness linear mapping 6
15:0	RW	0x0000	sw_dmsr_edge_low_thre_6 Low threshold for edgeness linear mapping 6

VEP_DMSR_EDGE_K0

Address: Operational Base(0x27961000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dmsr_edge_k_1 High threshold for edgeness linear mapping 1
15:0	RW	0x0000	sw_dmsr_edge_k_0 Low threshold for edgeness linear mapping 0

VEP_DMSR_EDGE_K1

Address: Operational Base(0x27961000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dmsr_edge_k_3 High threshold for edgeness linear mapping 3
15:0	RW	0x0000	sw_dmsr_edge_k_2 Low threshold for edgeness linear mapping 2

VEP_DMSR_EDGE_K2

Address: Operational Base(0x27961000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dmsr_edge_k_5 High threshold for edgeness linear mapping 5
15:0	RW	0x0000	sw_dmsr_edge_k_4 Low threshold for edgeness linear mapping 4

VEP_DMSR_EDGE_K3

Address: Operational Base(0x27961000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dmsr_dir_contrast_conf_f DMSR direction contrast confidence mapping slope

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	sw_dmsr_edge_k_6 Low threshold for edgeness linear mapping 6

VEP_DMSR_DIR_CONTRAST_CONF_X

Address: Operational Base(0x27961000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dmsr_dir_contrast_conf_x1 DMSR direction contrast confidence mapping x1
15:0	RW	0x0000	sw_dmsr_dir_contrast_conf_x0 DMSR direction contrast confidence mapping x0

VEP_DMSR_DIR_CONTRAST_CONF_Y

Address: Operational Base(0x27961000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dmsr_dir_contrast_conf_y1 DMSR direction contrast confidence mapping y1
15:0	RW	0x0000	sw_dmsr_dir_contrast_conf_y0 DMSR direction contrast confidence mapping y0

VEP_DMSR_FLATNESS_THRE

Address: Operational Base(0x27961000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_dmsr_var_th DMSR flatness variance threshold

VEP_DMSR_DIFF_CORING_THRE

Address: Operational Base(0x27961000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	sw_dmsr_diff_coring_th1 DMSR diff coring threshold 1
7:0	RW	0x00	sw_dmsr_diff_coring_th0 DMSR diff coring threshold 0

VEP_DMSR_DIFF_CORING_WEIGHT

Address: Operational Base(0x27961000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	sw_dmsr_diff_coring_wgt2 DMSR diff coring weight 2
15:14	RO	0x0	reserved
13:8	RW	0x00	sw_dmsr_diff_coring_wgt1 DMSR diff coring weight 1
7:6	RO	0x0	reserved
5:0	RW	0x00	sw_dmsr_diff_coring_wgt0 DMSR diff coring weight 0

VEP_DMSR_DIFF_CORING_Y

Address: Operational Base(0x27961000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_dmsr_diff_coring_y1 DMSR diff coring y1

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Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_dmsr_diff_coring_y0 DMSR diff coring y0

VEP_DMSR_FILTER_PRIMARY_TAP_WEIGHT_GAIN

Address: Operational Base(0x27961000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_dmsr_wgt_pri_gain_2_even DMSR primary weight gain 2 even
23:22	RO	0x0	reserved
21:16	RW	0x00	sw_dmsr_wgt_pri_gain_2_odd DMSR primary weight gain 2 odd
15:14	RO	0x0	reserved
13:8	RW	0x00	sw_dmsr_wgt_pri_gain_1_even DMSR primary weight gain 1 even
7:6	RO	0x0	reserved
5:0	RW	0x00	sw_dmsr_wgt_pri_gain_1_odd DMSR primary weight gain 1 odd

VEP_DMSR_FILTER_SECONDARY_TAP_WEIGHT_GAIN

Address: Operational Base(0x27961000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x00	sw_dmsr_wgt_sec_gain_2 DMSR secondary weight gain 2
7:6	RO	0x0	reserved
5:0	RW	0x00	sw_dmsr_wgt_sec_gain_1 DMSR secondary weight gain 1

VEP_DMSR_FILTER_STRENGTH

Address: Operational Base(0x27961000) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	sw_dmsr_dump DMSR filter dumping
15:13	RO	0x0	reserved
12:8	RW	0x00	sw_dmsr_strength_sec DMSR filter secondary strength
7:5	RO	0x0	reserved
4:0	RW	0x00	sw_dmsr_strength_pri DMSR filter primary strength

VEP_DMSR_DBG_MODE

Address: Operational Base(0x27961000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	sw_dmsr_obv_mode 1'b0: OBV input data 1'b1: OBV output data
24	RW	0x0	sw_dmsr_obv_enable OBV enable bit
23:12	RW	0x000	sw_dmsr_obv_point_v OBV vertical coordinate

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	sw_dmsr_obv_point_h OBV horizon coordinate

VDPP_DCI_YRGB_ADDR

Address: Operational Base(0x27961000) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dci_yrgb_addr DCI image source data address

VDPP_DCI_YRGB_VIR_STRIDE

Address: Operational Base(0x27961000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_dci_yrgb_gather_en DCI AXI bus yrgb data gather transfer enable 1: Enable 0: Disable
19:16	RW	0x0	sw_dci_yrgb_gather_num DCI AXI bus yrgb data gather transfer number 4'b0000: Gather2 4'b0001: Gather4 4'b0010: Gather8 Others: Reserved
15:0	RW	0x0000	sw_dci_yrgb_vir_stride DCI Source y virtual image width(word align)

VDPP_DCI_IMG_SIZE

Address: Operational Base(0x27961000) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_vep_src_pic_height Source image height(pixel align and need minus 1, for example 1080 need configuration 1079)
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_vep_src_pic_width Source image width(pixel align and need minus 1, for example 1920 need configuration 1919)

VDPP_DCI_CTRL

Address: Operational Base(0x27961000) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_dci_blk_vsize DCI block vsize
23:16	RW	0x00	sw_dci_blk_hsize DCI block hsize
15:9	RO	0x00	reserved
8	RW	0x0	sw_dci_rb_swap Image souce R B swap 1: BGR 0: RGB
7	RW	0x0	sw_dci_alpha_swap Image souce ARGB swap 1: RGBA 0: ARGB

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Bit	Attr	Reset Value	Description
6	RW	0x0	sw_dci_hsd_mode DCI horizontal scale down mode select 1: x2 0: Disable
5:4	RW	0x0	sw_dci_vsd_mode DCI vertical scale down mode select 2: x4 1: x2 0: Disable
3	RW	0x0	sw_dci_csc_range 1: Full 0: Limit
2:0	RW	0x0	sw_dci_data_format DCI data format: 0:RGB888 1: ARGB8888 4: Y 8bit SP 5: Y 10bit SP

VDPP_DCI_HIST_ADDR

Address: Operational Base(0x27961000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dci_hist_addr DCI histogram data write address

2.4.3.3 ES

ES_EN

Address: Operational Base(0x27961100) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ES_ENABLE 1'b0:ES Disable 1'b1:ES Enable

ES_DIR_TH

Address: Operational Base(0x27961100) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	DIR_TH If the gradient is greater than the direction threshold, further determine the specific direction. If it is less than, it is determined as no direction (0).
7:0	RW	0x00	FLAT_TH If the gradient is less than the flatness threshold, it is judged as flat (1), therwise it is non flat (0).

ES_DIR_TAN

Address: Operational Base(0x27961100) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	TAN_LO_TH 23 angle range lower limit tan threshold.
15:9	RO	0x00	reserved
8:0	RW	0x000	TAN_HI_TH 23 angle range upper limit tan threshold.

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ES_DIR_CHK

Address: Operational Base(0x27961100) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	MEM_GAT_EN 1'b0:Memory Enable 1'b1:Memory Disable
7:1	RO	0x00	reserved
0	RW	0x0	EP_CHK_EN Pixel endpoint check enable. 1'b0:Enable 1'b1:Disable

ES_FIL_DIFF0

Address: Operational Base(0x27961100) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	DIFF_LIMIT Diff_base0/1 upper threahold.
15:0	RW	0x0000	DIFF_GAIN0 Diff base1 gain.

ES_FIL_DIFF1

Address: Operational Base(0x27961100) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	DIFF_GAIN1 Diff base2 gain.
15:0	RW	0x0000	LUT_X0 Diff2conf_lut_x[0]

ES_FIL_LUT_X0

Address: Operational Base(0x27961100) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LUT_X1 Diff2conf_lut_x[1]
15:0	RW	0x0000	LUT_X2 Diff2conf_lut_x[2]

ES_FIL_LUT_X1

Address: Operational Base(0x27961100) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LUT_X3 Diff2conf_lut_x[3]
15:0	RW	0x0000	LUT_X4 Diff2conf_lut_x[4]

ES_FIL_LUT_X2

Address: Operational Base(0x27961100) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LUT_X5 Diff2conf_lut_x[5]
15:0	RW	0x0000	LUT_X6 Diff2conf_lut_x[6]

ES_FIL_LUT_X3

Address: Operational Base(0x27961100) + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LUT_X7 Diff2conf_lut_x[7]
15:0	RW	0x0000	LUT_X8 Diff2conf_lut_x[8]

ES_FIL_LUT_Y0

Address: Operational Base(0x27961100) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	LUT_Y3 Diff2conf_lut_y[3]
23:16	RW	0x00	LUT_Y2 Diff2conf_lut_y[2]
15:8	RW	0x00	LUT_Y1 Diff2conf_lut_y[1]
7:0	RW	0x00	LUT_Y0 Diff2conf_lut_y[0]

ES_FIL_LUT_Y1

Address: Operational Base(0x27961100) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	LUT_Y7 Diff2conf_lut_y[7]
23:16	RW	0x00	LUT_Y6 Diff2conf_lut_y[6]
15:8	RW	0x00	LUT_Y5 Diff2conf_lut_y[5]
7:0	RW	0x00	LUT_Y4 Diff2conf_lut_y[4]

ES_FIL_LUT_Y2

Address: Operational Base(0x27961100) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	LUT_Y8 Diff2conf_lut_y[8]

ES_FIL_LUT_K0

Address: Operational Base(0x27961100) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	LUT_K3 Diff2conf_lut_k[3]
23:16	RW	0x00	LUT_K2 Diff2conf_lut_k[2]
15:8	RW	0x00	LUT_K1 Diff2conf_lut_k[1]
7:0	RW	0x00	LUT_K0 Diff2conf_lut_k[0]

ES_FIL_LUT_K1

Address: Operational Base(0x27961100) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	LUT_K7 Diff2conf_lut_k[7]

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	LUT_K6 Diff2conf_lut_k[6]
15:8	RW	0x00	LUT_K5 Diff2conf_lut_k[5]
7:0	RW	0x00	LUT_K4 Diff2conf_lut_k[4]

ES_FIL_WGT

Address: Operational Base(0x27961100) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	WGT_GAIN Filter weight gain.
7:0	RW	0x00	WGT_DECAY Filter weight decay factor.

ES_FIL_CONF

Address: Operational Base(0x27961100) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	LOW_CONF_TH Low confidence determine threshold.
23:16	RW	0x00	LOW_CONF_RATIO Low confidence mean scale factor.
15:12	RO	0x0	reserved
11:8	RW	0x0	CONF_CNT_TH Low confidence number determine threshold.
7:0	RW	0x00	CONF_MEAN_TH Confidence mean threshold.

ES_DBG_INL

Address: Operational Base(0x27961100) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	INK_MODE Debug ink mode slect.
3:1	RO	0x0	reserved
0	RW	0x0	INK_EN Debug ink enable bit.

ES_DBG_INFO0

Address: Operational Base(0x27961100) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	MEM_IN_LINE_CNT Memory input line count.
15:13	RO	0x0	reserved
12	RO	0x0	IN_VLD Dbmsr to es data valid signal
11:9	RO	0x0	reserved
8	RO	0x0	IN_HSYNC Es input horizontal synchronization
7:5	RO	0x0	reserved
4	RO	0x0	MEM_IN_VSYNC Es memory input vertical synchronization

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Bit	Attr	Reset Value	Description
3:1	RO	0x0	reserved
0	RO	0x0	IN_RDY Es to dbmsr ready signal

ES_DBG_INFO1

Address: Operational Base(0x27961100) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RO	0x0	IN_FLAT Dbmsr to es flatness data.
23:22	RO	0x0	reserved
21:16	RO	0x00	IN_DIR Dbmsr to es direction data.
15:0	RO	0x0000	IN_PIX Dbmsr to es pixel data.

ES_DBG_INFO2

Address: Operational Base(0x27961100) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	OUT_LINE_CNT Es filter output data line count.
15:13	RO	0x0	reserved
12	RO	0x0	OUT_VLD Es to zme data valid signal.
11:9	RO	0x0	reserved
8	RO	0x0	OUT_HSYNC Es filter output horizontal synchronization.
7:5	RO	0x0	reserved
4	RO	0x0	OUT_VSYNC Es filter output vertical synchronization.
3:1	RO	0x0	reserved
0	RO	0x0	OUT_RDY Zme to es ready signal.

ES_DBG_INFO3

Address: Operational Base(0x27961100) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	OUT_PIX Es to zme filter pixel data.

2.4.3.4 ZME

ZME_YRGB_HOR_COE0_10

Address: Operational Base(0x27962000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe0_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe0_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE0_32

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Address: Operational Base(0x27962000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe0_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe0_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE0_54

Address: Operational Base(0x27962000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe0_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe0_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE0_76

Address: Operational Base(0x27962000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe0_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe0_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE1_10

Address: Operational Base(0x27962000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe1_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe1_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE1_32

Address: Operational Base(0x27962000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe1_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe1_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE1_54

Address: Operational Base(0x27962000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	yrgb_hor_coe1_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe1_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE1_76

Address: Operational Base(0x27962000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe1_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe1_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE2_10

Address: Operational Base(0x27962000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe2_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe2_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE2_32

Address: Operational Base(0x27962000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe2_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe2_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE2_54

Address: Operational Base(0x27962000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe2_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe2_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE2_76

Address: Operational Base(0x27962000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe2_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	yrgb_hor_coe2_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE3_10

Address: Operational Base(0x27962000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe3_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe3_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE3_32

Address: Operational Base(0x27962000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe3_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe3_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE3_54

Address: Operational Base(0x27962000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe3_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe3_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE3_76

Address: Operational Base(0x27962000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe3_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe3_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE4_10

Address: Operational Base(0x27962000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe4_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe4_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE4_32

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Address: Operational Base(0x27962000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe4_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe4_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE4_54

Address: Operational Base(0x27962000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe4_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe4_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE4_76

Address: Operational Base(0x27962000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe4_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe4_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE5_10

Address: Operational Base(0x27962000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe5_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe5_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE5_32

Address: Operational Base(0x27962000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe5_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe5_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE5_54

Address: Operational Base(0x27962000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	yrgb_hor_coe5_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe5_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE5_76

Address: Operational Base(0x27962000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe5_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe5_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE6_10

Address: Operational Base(0x27962000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe6_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe6_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE6_32

Address: Operational Base(0x27962000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe6_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe6_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE6_54

Address: Operational Base(0x27962000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe6_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe6_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE6_76

Address: Operational Base(0x27962000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe6_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	yrgb_hor_coe6_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE7_10

Address: Operational Base(0x27962000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe7_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe7_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE7_32

Address: Operational Base(0x27962000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe7_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe7_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE7_54

Address: Operational Base(0x27962000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe7_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe7_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE7_76

Address: Operational Base(0x27962000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe7_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe7_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE8_10

Address: Operational Base(0x27962000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe8_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe8_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE8_32

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Address: Operational Base(0x27962000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe8_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe8_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE8_54

Address: Operational Base(0x27962000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe8_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe8_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE8_76

Address: Operational Base(0x27962000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe8_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe8_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE9_10

Address: Operational Base(0x27962000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe9_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe9_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE9_32

Address: Operational Base(0x27962000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe9_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe9_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE9_54

Address: Operational Base(0x27962000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	yrgb_hor_coe9_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe9_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE9_76

Address: Operational Base(0x27962000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe9_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe9_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE10_10

Address: Operational Base(0x27962000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe10_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe10_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE10_32

Address: Operational Base(0x27962000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe10_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe10_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE10_54

Address: Operational Base(0x27962000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe10_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe10_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE10_76

Address: Operational Base(0x27962000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe10_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	yrgb_hor_coe10_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE11_10

Address: Operational Base(0x27962000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe11_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe11_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE11_32

Address: Operational Base(0x27962000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe11_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe11_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE11_54

Address: Operational Base(0x27962000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe11_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe11_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE11_76

Address: Operational Base(0x27962000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe11_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe11_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE12_10

Address: Operational Base(0x27962000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe12_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe12_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE12_32

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Address: Operational Base(0x27962000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe12_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe12_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE12_54

Address: Operational Base(0x27962000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe12_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe12_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE12_76

Address: Operational Base(0x27962000) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe12_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe12_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE13_10

Address: Operational Base(0x27962000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe13_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe13_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE13_32

Address: Operational Base(0x27962000) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe13_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe13_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE13_54

Address: Operational Base(0x27962000) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	yrgb_hor_coe13_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe13_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE13_76

Address: Operational Base(0x27962000) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe13_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe13_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE14_10

Address: Operational Base(0x27962000) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe14_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe14_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE14_32

Address: Operational Base(0x27962000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe14_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe14_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE14_54

Address: Operational Base(0x27962000) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe14_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe14_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE14_76

Address: Operational Base(0x27962000) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe14_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	yrgb_hor_coe14_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE15_10

Address: Operational Base(0x27962000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe15_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe15_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE15_32

Address: Operational Base(0x27962000) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe15_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe15_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE15_54

Address: Operational Base(0x27962000) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe15_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe15_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE15_76

Address: Operational Base(0x27962000) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe15_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe15_6 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE16_10

Address: Operational Base(0x27962000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe16_1 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe16_0 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE16_32

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Address: Operational Base(0x27962000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe16_3 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe16_2 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE16_54

Address: Operational Base(0x27962000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe16_5 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe16_4 YRGB horizontal filter coefficient.

ZME_YRGB_HOR_COE16_76

Address: Operational Base(0x27962000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_hor_coe16_7 YRGB horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_hor_coe16_6 YRGB horizontal filter coefficient.

ZME_YRGB_VER_COE0_10

Address: Operational Base(0x27962000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe0_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe0_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE0_32

Address: Operational Base(0x27962000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe0_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe0_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE0_54

Address: Operational Base(0x27962000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	yrgb_ver_coe0_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe0_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE0_76

Address: Operational Base(0x27962000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe0_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe0_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE1_10

Address: Operational Base(0x27962000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe1_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe1_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE1_32

Address: Operational Base(0x27962000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe1_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe1_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE1_54

Address: Operational Base(0x27962000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe1_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe1_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE1_76

Address: Operational Base(0x27962000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe1_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	yrgb_ver_coe1_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE2_10

Address: Operational Base(0x27962000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe2_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe2_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE2_32

Address: Operational Base(0x27962000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe2_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe2_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE2_54

Address: Operational Base(0x27962000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe2_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe2_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE2_76

Address: Operational Base(0x27962000) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe2_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe2_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE3_10

Address: Operational Base(0x27962000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe3_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe3_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE3_32

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Address: Operational Base(0x27962000) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe3_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe3_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE3_54

Address: Operational Base(0x27962000) + offset (0x0238)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe3_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe3_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE3_76

Address: Operational Base(0x27962000) + offset (0x023C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe3_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe3_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE4_10

Address: Operational Base(0x27962000) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe4_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe4_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE4_32

Address: Operational Base(0x27962000) + offset (0x0244)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe4_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe4_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE4_54

Address: Operational Base(0x27962000) + offset (0x0248)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	yrgb_ver_coe4_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe4_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE4_76

Address: Operational Base(0x27962000) + offset (0x024C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe4_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe4_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE5_10

Address: Operational Base(0x27962000) + offset (0x0250)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe5_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe5_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE5_32

Address: Operational Base(0x27962000) + offset (0x0254)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe5_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe5_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE5_54

Address: Operational Base(0x27962000) + offset (0x0258)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe5_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe5_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE5_76

Address: Operational Base(0x27962000) + offset (0x025C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe5_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	yrgb_ver_coe5_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE6_10

Address: Operational Base(0x27962000) + offset (0x0260)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe6_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe6_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE6_32

Address: Operational Base(0x27962000) + offset (0x0264)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe6_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe6_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE6_54

Address: Operational Base(0x27962000) + offset (0x0268)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe6_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe6_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE6_76

Address: Operational Base(0x27962000) + offset (0x026C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe6_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe6_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE7_10

Address: Operational Base(0x27962000) + offset (0x0270)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe7_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe7_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE7_32

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Address: Operational Base(0x27962000) + offset (0x0274)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe7_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe7_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE7_54

Address: Operational Base(0x27962000) + offset (0x0278)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe7_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe7_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE7_76

Address: Operational Base(0x27962000) + offset (0x027C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe7_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe7_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE8_10

Address: Operational Base(0x27962000) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe8_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe8_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE8_32

Address: Operational Base(0x27962000) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe8_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe8_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE8_54

Address: Operational Base(0x27962000) + offset (0x0288)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	yrgb_ver_coe8_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe8_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE8_76

Address: Operational Base(0x27962000) + offset (0x028C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe8_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe8_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE9_10

Address: Operational Base(0x27962000) + offset (0x0290)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe9_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe9_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE9_32

Address: Operational Base(0x27962000) + offset (0x0294)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe9_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe9_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE9_54

Address: Operational Base(0x27962000) + offset (0x0298)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe9_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe9_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE9_76

Address: Operational Base(0x27962000) + offset (0x029C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe9_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	yrgb_ver_coe9_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE10_10

Address: Operational Base(0x27962000) + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe10_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe10_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE10_32

Address: Operational Base(0x27962000) + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe10_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe10_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE10_54

Address: Operational Base(0x27962000) + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe10_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe10_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE10_76

Address: Operational Base(0x27962000) + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe10_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe10_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE11_10

Address: Operational Base(0x27962000) + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe11_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe11_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE11_32

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Address: Operational Base(0x27962000) + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe11_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe11_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE11_54

Address: Operational Base(0x27962000) + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe11_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe11_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE11_76

Address: Operational Base(0x27962000) + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe11_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe11_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE12_10

Address: Operational Base(0x27962000) + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe12_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe12_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE12_32

Address: Operational Base(0x27962000) + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe12_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe12_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE12_54

Address: Operational Base(0x27962000) + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	yrgb_ver_coe12_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe12_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE12_76

Address: Operational Base(0x27962000) + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe12_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe12_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE13_10

Address: Operational Base(0x27962000) + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe13_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe13_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE13_32

Address: Operational Base(0x27962000) + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe13_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe13_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE13_54

Address: Operational Base(0x27962000) + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe13_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe13_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE13_76

Address: Operational Base(0x27962000) + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe13_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	yrgb_ver_coe13_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE14_10

Address: Operational Base(0x27962000) + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe14_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe14_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE14_32

Address: Operational Base(0x27962000) + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe14_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe14_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE14_54

Address: Operational Base(0x27962000) + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe14_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe14_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE14_76

Address: Operational Base(0x27962000) + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe14_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe14_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE15_10

Address: Operational Base(0x27962000) + offset (0x02F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe15_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe15_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE15_32

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Address: Operational Base(0x27962000) + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe15_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe15_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE15_54

Address: Operational Base(0x27962000) + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe15_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe15_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE15_76

Address: Operational Base(0x27962000) + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe15_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe15_6 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE16_10

Address: Operational Base(0x27962000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe16_1 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe16_0 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE16_32

Address: Operational Base(0x27962000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe16_3 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe16_2 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE16_54

Address: Operational Base(0x27962000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	yrgb_ver_coe16_5 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe16_4 YRGB vertical filter coefficient.

ZME_YRGB_VER_COE16_76

Address: Operational Base(0x27962000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	yrgb_ver_coe16_7 YRGB vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	yrgb_ver_coe16_6 YRGB vertical filter coefficient.

ZME_CBCR_HOR_COE0_10

Address: Operational Base(0x27962000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe0_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe0_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE0_32

Address: Operational Base(0x27962000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe0_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe0_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE0_54

Address: Operational Base(0x27962000) + offset (0x0408)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe0_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe0_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE0_76

Address: Operational Base(0x27962000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe0_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	cbcr_hor_coe0_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE1_10

Address: Operational Base(0x27962000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe1_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe1_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE1_32

Address: Operational Base(0x27962000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe1_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe1_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE1_54

Address: Operational Base(0x27962000) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe1_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe1_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE1_76

Address: Operational Base(0x27962000) + offset (0x041C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe1_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe1_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE2_10

Address: Operational Base(0x27962000) + offset (0x0420)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe2_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe2_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE2_32

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Address: Operational Base(0x27962000) + offset (0x0424)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe2_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe2_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE2_54

Address: Operational Base(0x27962000) + offset (0x0428)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe2_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe2_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE2_76

Address: Operational Base(0x27962000) + offset (0x042C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe2_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe2_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE3_10

Address: Operational Base(0x27962000) + offset (0x0430)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe3_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe3_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE3_32

Address: Operational Base(0x27962000) + offset (0x0434)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe3_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe3_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE3_54

Address: Operational Base(0x27962000) + offset (0x0438)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	cbcr_hor_coe3_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe3_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE3_76

Address: Operational Base(0x27962000) + offset (0x043C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe3_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe3_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE4_10

Address: Operational Base(0x27962000) + offset (0x0440)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe4_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe4_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE4_32

Address: Operational Base(0x27962000) + offset (0x0444)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe4_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe4_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE4_54

Address: Operational Base(0x27962000) + offset (0x0448)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe4_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe4_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE4_76

Address: Operational Base(0x27962000) + offset (0x044C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe4_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	cbcr_hor_coe4_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE5_10

Address: Operational Base(0x27962000) + offset (0x0450)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe5_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe5_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE5_32

Address: Operational Base(0x27962000) + offset (0x0454)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe5_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe5_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE5_54

Address: Operational Base(0x27962000) + offset (0x0458)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe5_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe5_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE5_76

Address: Operational Base(0x27962000) + offset (0x045C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe5_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe5_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE6_10

Address: Operational Base(0x27962000) + offset (0x0460)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe6_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe6_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE6_32

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Address: Operational Base(0x27962000) + offset (0x0464)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe6_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe6_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE6_54

Address: Operational Base(0x27962000) + offset (0x0468)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe6_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe6_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE6_76

Address: Operational Base(0x27962000) + offset (0x046C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe6_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe6_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE7_10

Address: Operational Base(0x27962000) + offset (0x0470)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe7_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe7_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE7_32

Address: Operational Base(0x27962000) + offset (0x0474)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe7_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe7_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE7_54

Address: Operational Base(0x27962000) + offset (0x0478)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	cbcr_hor_coe7_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe7_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE7_76

Address: Operational Base(0x27962000) + offset (0x047C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe7_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe7_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE8_10

Address: Operational Base(0x27962000) + offset (0x0480)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe8_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe8_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE8_32

Address: Operational Base(0x27962000) + offset (0x0484)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe8_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe8_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE8_54

Address: Operational Base(0x27962000) + offset (0x0488)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe8_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe8_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE8_76

Address: Operational Base(0x27962000) + offset (0x048C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe8_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	cbcr_hor_coe8_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE9_10

Address: Operational Base(0x27962000) + offset (0x0490)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe9_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe9_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE9_32

Address: Operational Base(0x27962000) + offset (0x0494)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe9_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe9_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE9_54

Address: Operational Base(0x27962000) + offset (0x0498)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe9_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe9_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE9_76

Address: Operational Base(0x27962000) + offset (0x049C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe9_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe9_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE10_10

Address: Operational Base(0x27962000) + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe10_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe10_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE10_32

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Address: Operational Base(0x27962000) + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe10_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe10_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE10_54

Address: Operational Base(0x27962000) + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe10_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe10_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE10_76

Address: Operational Base(0x27962000) + offset (0x04AC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe10_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe10_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE11_10

Address: Operational Base(0x27962000) + offset (0x04B0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe11_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe11_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE11_32

Address: Operational Base(0x27962000) + offset (0x04B4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe11_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe11_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE11_54

Address: Operational Base(0x27962000) + offset (0x04B8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	cbcr_hor_coe11_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe11_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE11_76

Address: Operational Base(0x27962000) + offset (0x04BC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe11_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe11_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE12_10

Address: Operational Base(0x27962000) + offset (0x04C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe12_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe12_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE12_32

Address: Operational Base(0x27962000) + offset (0x04C4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe12_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe12_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE12_54

Address: Operational Base(0x27962000) + offset (0x04C8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe12_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe12_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE12_76

Address: Operational Base(0x27962000) + offset (0x04CC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe12_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	cbcr_hor_coe12_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE13_10

Address: Operational Base(0x27962000) + offset (0x04D0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe13_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe13_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE13_32

Address: Operational Base(0x27962000) + offset (0x04D4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe13_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe13_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE13_54

Address: Operational Base(0x27962000) + offset (0x04D8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe13_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe13_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE13_76

Address: Operational Base(0x27962000) + offset (0x04DC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe13_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe13_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE14_10

Address: Operational Base(0x27962000) + offset (0x04E0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe14_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe14_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE14_32

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Address: Operational Base(0x27962000) + offset (0x04E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe14_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe14_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE14_54

Address: Operational Base(0x27962000) + offset (0x04E8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe14_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe14_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE14_76

Address: Operational Base(0x27962000) + offset (0x04EC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe14_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe14_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE15_10

Address: Operational Base(0x27962000) + offset (0x04F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe15_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe15_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE15_32

Address: Operational Base(0x27962000) + offset (0x04F4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe15_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe15_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE15_54

Address: Operational Base(0x27962000) + offset (0x04F8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	cbcr_hor_coe15_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe15_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE15_76

Address: Operational Base(0x27962000) + offset (0x04FC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe15_7 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe15_6 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE16_10

Address: Operational Base(0x27962000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe16_1 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe16_0 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE16_32

Address: Operational Base(0x27962000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe16_3 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe16_2 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE16_54

Address: Operational Base(0x27962000) + offset (0x0508)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe16_5 CBCR horizontal filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_hor_coe16_4 CBCR horizontal filter coefficient.

ZME_CBCR_HOR_COE16_76

Address: Operational Base(0x27962000) + offset (0x050C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_hor_coe16_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	cbcr_hor_coe16_6 CBCR horizontal filter coefficient.

ZME_CBCR_VER_COE0_10

Address: Operational Base(0x27962000) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe0_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe0_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE0_32

Address: Operational Base(0x27962000) + offset (0x0604)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe0_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe0_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE0_54

Address: Operational Base(0x27962000) + offset (0x0608)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe0_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe0_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE0_76

Address: Operational Base(0x27962000) + offset (0x060C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe0_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe0_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE1_10

Address: Operational Base(0x27962000) + offset (0x0610)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe1_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe1_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE1_32

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Address: Operational Base(0x27962000) + offset (0x0614)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe1_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe1_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE1_54

Address: Operational Base(0x27962000) + offset (0x0618)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe1_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe1_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE1_76

Address: Operational Base(0x27962000) + offset (0x061C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe1_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe1_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE2_10

Address: Operational Base(0x27962000) + offset (0x0620)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe2_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe2_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE2_32

Address: Operational Base(0x27962000) + offset (0x0624)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe2_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe2_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE2_54

Address: Operational Base(0x27962000) + offset (0x0628)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	cbcr_ver_coe2_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe2_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE2_76

Address: Operational Base(0x27962000) + offset (0x062C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe2_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe2_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE3_10

Address: Operational Base(0x27962000) + offset (0x0630)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe3_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe3_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE3_32

Address: Operational Base(0x27962000) + offset (0x0634)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe3_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe3_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE3_54

Address: Operational Base(0x27962000) + offset (0x0638)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe3_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe3_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE3_76

Address: Operational Base(0x27962000) + offset (0x063C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe3_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	cbcr_ver_coe3_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE4_10

Address: Operational Base(0x27962000) + offset (0x0640)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe4_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe4_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE4_32

Address: Operational Base(0x27962000) + offset (0x0644)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe4_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe4_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE4_54

Address: Operational Base(0x27962000) + offset (0x0648)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe4_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe4_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE4_76

Address: Operational Base(0x27962000) + offset (0x064C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe4_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe4_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE5_10

Address: Operational Base(0x27962000) + offset (0x0650)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe5_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe5_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE5_32

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Address: Operational Base(0x27962000) + offset (0x0654)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe5_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe5_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE5_54

Address: Operational Base(0x27962000) + offset (0x0658)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe5_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe5_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE5_76

Address: Operational Base(0x27962000) + offset (0x065C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe5_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe5_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE6_10

Address: Operational Base(0x27962000) + offset (0x0660)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe6_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe6_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE6_32

Address: Operational Base(0x27962000) + offset (0x0664)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe6_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe6_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE6_54

Address: Operational Base(0x27962000) + offset (0x0668)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	cbcr_ver_coe6_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe6_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE6_76

Address: Operational Base(0x27962000) + offset (0x066C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe6_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe6_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE7_10

Address: Operational Base(0x27962000) + offset (0x0670)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe7_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe7_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE7_32

Address: Operational Base(0x27962000) + offset (0x0674)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe7_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe7_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE7_54

Address: Operational Base(0x27962000) + offset (0x0678)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe7_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe7_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE7_76

Address: Operational Base(0x27962000) + offset (0x067C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe7_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	cbcr_ver_coe7_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE8_10

Address: Operational Base(0x27962000) + offset (0x0680)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe8_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe8_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE8_32

Address: Operational Base(0x27962000) + offset (0x0684)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe8_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe8_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE8_54

Address: Operational Base(0x27962000) + offset (0x0688)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe8_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe8_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE8_76

Address: Operational Base(0x27962000) + offset (0x068C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe8_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe8_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE9_10

Address: Operational Base(0x27962000) + offset (0x0690)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe9_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe9_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE9_32

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Address: Operational Base(0x27962000) + offset (0x0694)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe9_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe9_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE9_54

Address: Operational Base(0x27962000) + offset (0x0698)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe9_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe9_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE9_76

Address: Operational Base(0x27962000) + offset (0x069C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe9_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe9_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE10_10

Address: Operational Base(0x27962000) + offset (0x06A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe10_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe10_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE10_32

Address: Operational Base(0x27962000) + offset (0x06A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe10_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe10_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE10_54

Address: Operational Base(0x27962000) + offset (0x06A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	cbcr_ver_coe10_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe10_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE10_76

Address: Operational Base(0x27962000) + offset (0x06AC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe10_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe10_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE11_10

Address: Operational Base(0x27962000) + offset (0x06B0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe11_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe11_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE11_32

Address: Operational Base(0x27962000) + offset (0x06B4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe11_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe11_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE11_54

Address: Operational Base(0x27962000) + offset (0x06B8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe11_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe11_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE11_76

Address: Operational Base(0x27962000) + offset (0x06BC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe11_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	cbcr_ver_coe11_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE12_10

Address: Operational Base(0x27962000) + offset (0x06C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe12_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe12_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE12_32

Address: Operational Base(0x27962000) + offset (0x06C4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe12_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe12_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE12_54

Address: Operational Base(0x27962000) + offset (0x06C8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe12_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe12_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE12_76

Address: Operational Base(0x27962000) + offset (0x06CC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe12_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe12_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE13_10

Address: Operational Base(0x27962000) + offset (0x06D0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe13_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe13_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE13_32

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Address: Operational Base(0x27962000) + offset (0x06D4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe13_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe13_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE13_54

Address: Operational Base(0x27962000) + offset (0x06D8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe13_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe13_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE13_76

Address: Operational Base(0x27962000) + offset (0x06DC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe13_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe13_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE14_10

Address: Operational Base(0x27962000) + offset (0x06E0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe14_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe14_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE14_32

Address: Operational Base(0x27962000) + offset (0x06E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe14_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe14_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE14_54

Address: Operational Base(0x27962000) + offset (0x06E8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	cbcr_ver_coe14_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe14_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE14_76

Address: Operational Base(0x27962000) + offset (0x06EC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe14_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe14_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE15_10

Address: Operational Base(0x27962000) + offset (0x06F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe15_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe15_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE15_32

Address: Operational Base(0x27962000) + offset (0x06F4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe15_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe15_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE15_54

Address: Operational Base(0x27962000) + offset (0x06F8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe15_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe15_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE15_76

Address: Operational Base(0x27962000) + offset (0x06FC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe15_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	cbcr_ver_coe15_6 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE16_10

Address: Operational Base(0x27962000) + offset (0x0700)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe16_1 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe16_0 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE16_32

Address: Operational Base(0x27962000) + offset (0x0704)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe16_3 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe16_2 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE16_54

Address: Operational Base(0x27962000) + offset (0x0708)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe16_5 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe16_4 CBCR vertical filter coefficient.

ZME_CBCR_VER_COE16_76

Address: Operational Base(0x27962000) + offset (0x070C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	cbcr_ver_coe16_7 CBCR vertical filter coefficient.
15:10	RO	0x00	reserved
9:0	RW	0x000	cbcr_ver_coe16_6 CBCR vertical filter coefficient.

ZME_ZME_CTRL

Address: Operational Base(0x27962000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31	RW	0x0	auto_gating_en 1'b0: Disable 1'b1: Enable
30:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	format_out 4'b0000: FMT_ARGB8888 4'b0001: FMT_RGB888 4'b0100: FMT_YUV420 4'b0101: FMT_YUV422 4'b0110: FMT_YUV444 4'b0111: FMT_YUV400
7:4	RW	0x0	format_in 4'b0000: FMT_ARGB8888 4'b0001: FMT_RGB888 4'b0100: FMT_YUV420 4'b0101: FMT_YUV422 4'b0110: FMT_YUV444 4'b0111: FMT_YUV400
3:2	RO	0x0	reserved
1	RW	0x0	align_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	bypass_en 1'b0: Normal mode 1'b1: Bypass mode

ZME_YRGB_SCL_CTRL

Address: Operational Base(0x27962000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	yrgb_xsu_bypass 1'b0: Normal 1'b1: Bypass
17	RW	0x0	yrgb_ys_bypass 1'b0: Normal 1'b1: Bypass
16	RW	0x0	yrgb_xsd_bypass 1'b0: Normal 1'b1: Bypass
15:12	RO	0x0	reserved
11:10	RW	0x0	yrgb_gt_mode 2'b00: Drop 1 for every two line 2'b01: Drop 3 for every four line 2'b10: Drop 1 for every four line 2'b11: Auto
9	RW	0x0	yrgb_gt_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	yrgb_dering_en 1'b0: Disable 1'b1: Enable
7:6	RW	0x0	yrgb_yscl_mode This signal must config 2'b11(multi-phase).
5	RW	0x0	yrgb_ysu_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	yrgb_ysd_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	yrgb_xscl_mode This signal must config 2'b11(multi-phase).
1	RW	0x0	yrgb_xsu_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	yrgb_xsd_en 1'b0: Disable 1'b1: Enable

ZME_YRGB_DERING_PARA

Address: Operational Base(0x27962000) + offset (0x081C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	yrgb_dering_delta Deringing blending beta.
23:21	RO	0x0	reserved
20:16	RW	0x00	yrgb_dering_alpha Deringing blending alpha.
15:13	RO	0x0	reserved
12:8	RW	0x00	yrgb_dering_sen1 Deringing sensitivity1.
7:5	RO	0x0	reserved
4:0	RW	0x00	yrgb_dering_sen0 Deringing sensitivity0.

ZME_YRGB_XSCL_FACTOR

Address: Operational Base(0x27962000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	yrgb_xscl_offset YRGB horizontal scaler factor offset.
15:0	RW	0x0000	yrgb_xscl_factor Yrgb_xsd_en: (src_width-1)/(dst_width-1)*2^12 Yrgb_xsu_en: (src_width-1)/(dst_width-1)*2^16

ZME_YRGB_YSCL_FACTOR

Address: Operational Base(0x27962000) + offset (0x0824)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	yrgb_yscl_offset YRGB vertical scaler factor offset.
15:0	RW	0x0000	yrgb_yscl_factor Yrgb_ysd_en: (src_width-1)/(dst_width-1)*2^12 Yrgb_ysu_en: (src_width-1)/(dst_width-1)*2^16

ZME_CBCR_SCL_CTRL

Address: Operational Base(0x27962000) + offset (0x0830)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	cbcr_xsu_bypass 1'b0: Normal 1'b1: Bypass
17	RW	0x0	cbcr_ys_bypass 1'b0: Normal 1'b1: Bypass

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Bit	Attr	Reset Value	Description
16	RW	0x0	cbcr_xsd_bypass 1'b0: Normal 1'b1: Bypass
15:12	RO	0x0	reserved
11:10	RW	0x0	cbcr_gt_mode 2'b00: Drop 1 for every two line 2'b01: Drop 3 for every four line 2'b10: Drop 1 for every four line 2'b11: Auto
9	RW	0x0	cbcr_gt_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	cbcr_dering_en 1'b0: Disable 1'b1: Enable
7:6	RW	0x0	cbcr_yscl_mode This signal must config 2'b11(multi-phase).
5	RW	0x0	cbcr_ysu_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	cbcr_ysd_en 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	cbcr_xscl_mode This signal must config 2'b11(multi-phase).
1	RW	0x0	cbcr_xsu_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	cbcr_xsd_en 1'b0: Disable 1'b1: Enable

ZME_CBCR_DERING_PARA

Address: Operational Base(0x27962000) + offset (0x083C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	cbcr_dering_delta Deringing blending beta.
23:21	RO	0x0	reserved
20:16	RW	0x00	cbcr_dering_alpha Deringing blending alpha.
15:13	RO	0x0	reserved
12:8	RW	0x00	cbcr_dering_sen1 Deringing sensitivity1.
7:5	RO	0x0	reserved
4:0	RW	0x00	cbcr_dering_sen0 Deringing sensitivity0.

ZME_CBCR_XSCL_FACTOR

Address: Operational Base(0x27962000) + offset (0x0840)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cbcr_xscl_offset CBCR horizontal scaler factor offset.

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	cbcr_xscl_factor Cbcr_xsd_en: (src_width-1)/(dst_width-1)*2^12 Cbcr_xsu_en: (src_width-1)/(dst_width-1)*2^16

ZME_CBCR_YSCL_FACTOR

Address: Operational Base(0x27962000) + offset (0x0844)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cbcr_yscl_offset CBCR vertical scaler factor offset.
15:0	RW	0x0000	cbcr_yscl_factor Cbcr_ysd_en: (src_width-1)/(dst_width-1)*2^12 Cbcr_ysu_en: (src_width-1)/(dst_width-1)*2^16

2.4.3.5 SHARP

SHARP_CTRL

Address: Operational Base(0x27961200) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	sw_ink_enable Ink module enable bit 1'b1: Enable 1'b0: Disable
11	RW	0x0	sw_coloradj_bypass_en Bypass color_adj module enable bit, 1: bypass color_adj module
10	RW	0x0	sw_texture_adj_enable Texture_adj module enable bit, protect flat area. 1'b1: Enable 1'b0: Disable
9	RW	0x0	sw_color_adj_enable Color_adj module enable bit, adjust high frequency by chromaticity component. 1'b1: Enable 1'b0: Disable
8	RW	0x0	sw_gain_ctrl_enable Gain_ctrl module enable bit, adjust high frequency by luma, variance and gradient. 1'b1: Enable 1'b0: Disable
7	RW	0x0	sw_shoot_ctrl_enable ShootCtrl module enable bit, suppress overshoot and undershoot generate by sharp. 1'b1: Enable 1'b0: Disable
6	RW	0x0	sw_edge_proc_enable Peaking edge process module enable bit 1'b1: Enable 1'b0: Disable
5	RO	0x0	reserved
4	RW	0x0	sw_peaking_ctrl_enable Peaking ctrl process enable bit 1'b1: Enable 1'b0: Disable

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Bit	Attr	Reset Value	Description
3	RW	0x0	sw_peaking_enable Peaking module enable bit 1'b1: Enable 1'b0: Disable
2	RW	0x0	sw_cti_enable Cti module enable bit 1'b1: Enable 1'b0: Disable
1	RW	0x0	sw_lti_enable Lti module enable bit 1'b1: Enable 1'b0: Disable
0	RW	0x0	sw_sharp_enable Sharp module enable bit 1'b1: Enable 1'b0: Disable

SHARP_AUTO_GATING_IMD

Address: Operational Base(0x27961200) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	sw_texture_adj_gating_en 1'b1: Enable 1'b0: Disable
9	RW	0x0	sw_color_adj_gating_en 1'b1: Enable 1'b0: Disable
8	RW	0x0	sw_gain_ctrl_gating_en 1'b1: Enable 1'b0: Disable
7	RW	0x0	sw_shoot_ctrl_gating_en 1'b1: Enable 1'b0: Disable
6	RW	0x0	sw_edge_proc_gating_en 1'b1: Enable 1'b0: Disable
5	RO	0x0	reserved
4	RW	0x0	sw_peaking_ctrl_gating_en 1'b1: Enable 1'b0: Disable
3	RW	0x0	sw_peaking_gating_en 1'b1: Enable 1'b0: Disable
2	RW	0x0	sw_cti_gating_en 1'b1: Enable 1'b0: Disable
1	RW	0x0	sw_lti_gating_en 1'b1: Enable 1'b0: Disable
0	RW	0x0	sw_mem_gating_en 1'b1: Enable 1'b0: Disable

SHARP_PEAKING_FILTER_COE0

Address: Operational Base(0x27961200) + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x0	sw_peaking_v12 Peaking ver-direct filter1 coef2
19:16	RW	0x0	sw_peaking_v11 Peaking ver-direct filter1 coef1
15:12	RW	0x0	sw_peaking_v10 Peaking ver-direct filter1 coef0
11:8	RW	0x0	sw_peaking_v02 Peaking ver-direct filter0 coef2
7:4	RW	0x0	sw_peaking_v01 Peaking ver-direct filter0 coef1
3:0	RW	0x0	sw_peaking_v00 Peaking ver-direct filter0 coef0

SHARP_PEAKING_FILTER_COE1

Address: Operational Base(0x27961200) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	sw_diag_coef Peaking Diagonal filter core ctrl coef
23:20	RW	0x0	sw_peaking_usm2 Peaking non-direct filter coef2
19:16	RW	0x0	sw_peaking_usm1 Peaking non-direct filter coef1
15:12	RW	0x0	sw_peaking_usm0 Peaking non-direct filter coef0
11:8	RW	0x0	sw_peaking_v22 Peaking ver-direct filter2 coef2
7:4	RW	0x0	sw_peaking_v21 Peaking ver-direct filter2 coef1
3:0	RW	0x0	sw_peaking_v20 Peaking ver-direct filter2 coef0

SHARP_PEAKING_FILTER_COE2

Address: Operational Base(0x27961200) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	sw_peaking_h02 Peaking hor-direct filter0 coef2
15:14	RO	0x0	reserved
13:8	RW	0x00	sw_peaking_h01 Peaking hor-direct filter0 coef1
7:6	RO	0x0	reserved
5:0	RW	0x00	sw_peaking_h00 Peaking hor-direct filter0 coef0

SHARP_PEAKING_FILTER_COE4

Address: Operational Base(0x27961200) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	sw_peaking_h12 Peaking hor-direct filter1 coef2
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x00	sw_peaking_h11 Peaking hor-direct filter1 coef1
7:6	RO	0x0	reserved
5:0	RW	0x00	sw_peaking_h10 Peaking hor-direct filter1 coef0

SHARP_PEAKING_FILTER_COE6

Address: Operational Base(0x27961200) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	sw_peaking_h22 Peaking hor-direct filter2 coef2
15:14	RO	0x0	reserved
13:8	RW	0x00	sw_peaking_h21 Peaking hor-direct filter2 coef1
7:6	RO	0x0	reserved
5:0	RW	0x00	sw_peaking_h20 Peaking hor-direct filter2 coef0

SHARP_PEAKING0_CTRL_COE0

Address: Operational Base(0x27961200) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking0_idx_n1 Peaking_ctrl band0 negative half axis ctrl point index1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking0_idx_n0 Peaking_ctrl band0 negative half axis ctrl point index0

SHARP_PEAKING0_CTRL_COE1

Address: Operational Base(0x27961200) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking0_idx_n3 Peaking_ctrl band0 negative half axis ctrl point index3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking0_idx_n2 Peaking_ctrl band0 negative half axis ctrl point index2

SHARP_PEAKING0_CTRL_COE2

Address: Operational Base(0x27961200) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking0_idx_p1 Peaking_ctrl band0 positive half axis ctrl point index1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking0_idx_p0 Peaking_ctrl band0 positive half axis ctrl point index0

SHARP_PEAKING0_CTRL_COE3

Address: Operational Base(0x27961200) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24:16	RW	0x000	sw_peaking0_idx_p3 Peaking_ctrl band0 positive half axis ctrl point index3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking0_idx_p2 Peaking_ctrl band0 positive half axis ctrl point index2

SHARP_PEAKING0_CTRL_COE4

Address: Operational Base(0x27961200) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking0_value_n2 Peaking_ctrl band0 negative half axis ctrl point value2
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking0_value_n1 Peaking_ctrl band0 negative half axis ctrl point value1

SHARP_PEAKING0_CTRL_COE5

Address: Operational Base(0x27961200) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking0_value_p1 Peaking_ctrl band0 positive half axis ctrl point value1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking0_value_n3 Peaking_ctrl band0 negative half axis ctrl point value3

SHARP_PEAKING0_CTRL_COE6

Address: Operational Base(0x27961200) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking0_value_p3 Peaking_ctrl band0 positive half axis ctrl point value3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking0_value_p2 Peaking_ctrl band0 positive half axis ctrl point value2

SHARP_PEAKING0_CTRL_COE7

Address: Operational Base(0x27961200) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking0_ratio_n12 Peaking_ctrl band0 negative half axis slope12
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking0_ratio_n01 Peaking_ctrl band0 negative half axis slope01

SHARP_PEAKING0_CTRL_COE8

Address: Operational Base(0x27961200) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking0_ratio_p01 Peaking_ctrl band0 positive half axis slope01
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	sw_peaking0_ratio_n23 Peaking_ctrl band0 negative half axis slope23

SHARP_PEAKING0_CTRL_COE9

Address: Operational Base(0x27961200) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:12	RW	0x000	sw_peaking0_ratio_p23 Peaking_ctrl band0 positive half axis slope23
11:0	RW	0x000	sw_peaking0_ratio_p12 Peaking_ctrl band0 positive half axis slope12

SHARP_PEAKING1_CTRL_COE0

Address: Operational Base(0x27961200) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking1_idx_n1 Peaking_ctrl band1 negative half axis ctrl point index1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking1_idx_n0 Peaking_ctrl band1 negative half axis ctrl point index0

SHARP_PEAKING1_CTRL_COE1

Address: Operational Base(0x27961200) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking1_idx_n3 Peaking_ctrl band1 negative half axis ctrl point index3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking1_idx_n2 Peaking_ctrl band1 negative half axis ctrl point index2

SHARP_PEAKING1_CTRL_COE2

Address: Operational Base(0x27961200) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking1_idx_p1 Peaking_ctrl band1 positive half axis ctrl point index1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking1_idx_p0 Peaking_ctrl band1 positive half axis ctrl point index0

SHARP_PEAKING1_CTRL_COE3

Address: Operational Base(0x27961200) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking1_idx_p3 Peaking_ctrl band1 positive half axis ctrl point index3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking1_idx_p2 Peaking_ctrl band1 positive half axis ctrl point index2

SHARP_PEAKING1_CTRL_COE4

Address: Operational Base(0x27961200) + offset (0x006C)

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Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking1_value_n2 Peaking_ctrl band1 negative half axis ctrl point value2
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking1_value_n1 Peaking_ctrl band1 negative half axis ctrl point value1

SHARP_PEAKING1_CTRL_COE5

Address: Operational Base(0x27961200) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking1_value_p1 Peaking_ctrl band1 positive half axis ctrl point value1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking1_value_n3 Peaking_ctrl band1 negative half axis ctrl point value3

SHARP_PEAKING1_CTRL_COE6

Address: Operational Base(0x27961200) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking1_value_p3 Peaking_ctrl band1 positive half axis ctrl point value3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking1_value_p2 Peaking_ctrl band1 positive half axis ctrl point value2

SHARP_PEAKING1_CTRL_COE7

Address: Operational Base(0x27961200) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking1_ratio_n12 Peaking_ctrl band1 negative half axis slope12
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking1_ratio_n01 Peaking_ctrl band1 negative half axis slope01

SHARP_PEAKING1_CTRL_COE8

Address: Operational Base(0x27961200) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking1_ratio_p01 Peaking_ctrl band1 positive half axis slope01
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking1_ratio_n23 Peaking_ctrl band1 negative half axis slope23

SHARP_PEAKING1_CTRL_COE9

Address: Operational Base(0x27961200) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:12	RW	0x000	sw_peaking1_ratio_p23 Peaking_ctrl band1 positive half axis slope23

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	sw_peaking1_ratio_p12 Peaking_ctrl band1 positive half axis slope12

SHARP_PEAKING2_CTRL_COE0

Address: Operational Base(0x27961200) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking2_idx_n1 Peaking_ctrl band2 negative half axis ctrl point index1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking2_idx_n0 Peaking_ctrl band2 negative half axis ctrl point index0

SHARP_PEAKING2_CTRL_COE1

Address: Operational Base(0x27961200) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking2_idx_n3 Peaking_ctrl band2 negative half axis ctrl point index3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking2_idx_n2 Peaking_ctrl band2 negative half axis ctrl point index2

SHARP_PEAKING2_CTRL_COE2

Address: Operational Base(0x27961200) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking2_idx_p1 Peaking_ctrl band2 positive half axis ctrl point index1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking2_idx_p0 Peaking_ctrl band2 positive half axis ctrl point index0

SHARP_PEAKING2_CTRL_COE3

Address: Operational Base(0x27961200) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking2_idx_p3 Peaking_ctrl band2 positive half axis ctrl point index3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking2_idx_p2 Peaking_ctrl band2 positive half axis ctrl point index2

SHARP_PEAKING2_CTRL_COE4

Address: Operational Base(0x27961200) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking2_value_n2 Peaking_ctrl band2 negative half axis ctrl point value2
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking2_value_n1 Peaking_ctrl band2 negative half axis ctrl point value1

SHARP_PEAKING2_CTRL_COE5

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Address: Operational Base(0x27961200) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking2_value_p1 Peaking_ctrl band2 positive half axis ctrl point value1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking2_value_n3 Peaking_ctrl band2 negative half axis ctrl point value3

SHARP_PEAKING2_CTRL_COE6

Address: Operational Base(0x27961200) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking2_value_p3 Peaking_ctrl band2 positive half axis ctrl point value3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking2_value_p2 Peaking_ctrl band2 positive half axis ctrl point value2

SHARP_PEAKING2_CTRL_COE7

Address: Operational Base(0x27961200) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking2_ratio_n12 Peaking_ctrl band2 negative half axis slope12
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking2_ratio_n01 Peaking_ctrl band2 negative half axis slope01

SHARP_PEAKING2_CTRL_COE8

Address: Operational Base(0x27961200) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking2_ratio_p01 Peaking_ctrl band2 positive half axis slope01
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking2_ratio_n23 Peaking_ctrl band2 negative half axis slope23

SHARP_PEAKING2_CTRL_COE9

Address: Operational Base(0x27961200) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:12	RW	0x000	sw_peaking2_ratio_p23 Peaking_ctrl band2 positive half axis slope23
11:0	RW	0x000	sw_peaking2_ratio_p12 Peaking_ctrl band2 positive half axis slope12

SHARP_PEAKING3_CTRL_COE0

Address: Operational Base(0x27961200) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking3_idx_n1 Peaking_ctrl band3 negative half axis ctrl point index1
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8:0	RW	0x000	sw_peaking3_idx_n0 Peaking_ctrl band3 negative half axis ctrl point index0

SHARP_PEAKING3_CTRL_COE1

Address: Operational Base(0x27961200) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking3_idx_n3 Peaking_ctrl band3 negative half axis ctrl point index3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking3_idx_n2 Peaking_ctrl band3 negative half axis ctrl point index2

SHARP_PEAKING3_CTRL_COE2

Address: Operational Base(0x27961200) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking3_idx_p1 Peaking_ctrl band3 positive half axis ctrl point index1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking3_idx_p0 Peaking_ctrl band3 positive half axis ctrl point index0

SHARP_PEAKING3_CTRL_COE3

Address: Operational Base(0x27961200) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking3_idx_p3 Peaking_ctrl band3 positive half axis ctrl point index3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking3_idx_p2 Peaking_ctrl band3 positive half axis ctrl point index2

SHARP_PEAKING3_CTRL_COE4

Address: Operational Base(0x27961200) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking3_value_n2 Peaking_ctrl band3 negative half axis ctrl point value2
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking3_value_n1 Peaking_ctrl band3 negative half axis ctrl point value1

SHARP_PEAKING3_CTRL_COE5

Address: Operational Base(0x27961200) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking3_value_p1 Peaking_ctrl band3 positive half axis ctrl point value1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking3_value_n3 Peaking_ctrl band3 negative half axis ctrl point value3

SHARP_PEAKING3_CTRL_COE6

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Address: Operational Base(0x27961200) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking3_value_p3 Peaking_ctrl band3 positive half axis ctrl point value3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking3_value_p2 Peaking_ctrl band3 positive half axis ctrl point value2

SHARP_PEAKING3_CTRL_COE7

Address: Operational Base(0x27961200) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking3_ratio_n12 Peaking_ctrl band3 negative half axis slope12
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking3_ratio_n01 Peaking_ctrl band3 negative half axis slope01

SHARP_PEAKING3_CTRL_COE8

Address: Operational Base(0x27961200) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking3_ratio_p01 Peaking_ctrl band3 positive half axis slope01
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking3_ratio_n23 Peaking_ctrl band3 negative half axis slope23

SHARP_PEAKING3_CTRL_COE9

Address: Operational Base(0x27961200) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:12	RW	0x000	sw_peaking3_ratio_p23 Peaking_ctrl band3 positive half axis slope23
11:0	RW	0x000	sw_peaking3_ratio_p12 Peaking_ctrl band3 positive half axis slope12

SHARP_PEAKING4_CTRL_COE0

Address: Operational Base(0x27961200) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking4_idx_n1 Peaking_ctrl band4 negative half axis ctrl point index1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking4_idx_n0 Peaking_ctrl band4 negative half axis ctrl point index0

SHARP_PEAKING4_CTRL_COE1

Address: Operational Base(0x27961200) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking4_idx_n3 Peaking_ctrl band4 negative half axis ctrl point index3
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8:0	RW	0x000	sw_peaking4_idx_n2 Peaking_ctrl band4 negative half axis ctrl point index2

SHARP_PEAKING4_CTRL_COE2

Address: Operational Base(0x27961200) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking4_idx_p1 Peaking_ctrl band4 positive half axis ctrl point index1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking4_idx_p0 Peaking_ctrl band4 positive half axis ctrl point index0

SHARP_PEAKING4_CTRL_COE3

Address: Operational Base(0x27961200) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking4_idx_p3 Peaking_ctrl band4 positive half axis ctrl point index3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking4_idx_p2 Peaking_ctrl band4 positive half axis ctrl point index2

SHARP_PEAKING4_CTRL_COE4

Address: Operational Base(0x27961200) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking4_value_n2 Peaking_ctrl band4 negative half axis ctrl point value2
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking4_value_n1 Peaking_ctrl band4 negative half axis ctrl point value1

SHARP_PEAKING4_CTRL_COE5

Address: Operational Base(0x27961200) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking4_value_p1 Peaking_ctrl band4 positive half axis ctrl point value1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking4_value_n3 Peaking_ctrl band4 negative half axis ctrl point value3

SHARP_PEAKING4_CTRL_COE6

Address: Operational Base(0x27961200) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking4_value_p3 Peaking_ctrl band4 positive half axis ctrl point value3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking4_value_p2 Peaking_ctrl band4 positive half axis ctrl point value2

SHARP_PEAKING4_CTRL_COE7

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Address: Operational Base(0x27961200) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking4_ratio_n12 Peaking_ctrl band4 negative half axis slope12
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking4_ratio_n01 Peaking_ctrl band4 negative half axis slope01

SHARP_PEAKING4_CTRL_COE8

Address: Operational Base(0x27961200) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking4_ratio_p01 Peaking_ctrl band4 positive half axis slope01
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking4_ratio_n23 Peaking_ctrl band4 negative half axis slope23

SHARP_PEAKING4_CTRL_COE9

Address: Operational Base(0x27961200) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:12	RW	0x000	sw_peaking4_ratio_p23 Peaking_ctrl band4 positive half axis slope23
11:0	RW	0x000	sw_peaking4_ratio_p12 Peaking_ctrl band4 positive half axis slope12

SHARP_PEAKING5_CTRL_COE0

Address: Operational Base(0x27961200) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking5_idx_n1 Peaking_ctrl band5 negative half axis ctrl point index1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking5_idx_n0 Peaking_ctrl band5 negative half axis ctrl point index0

SHARP_PEAKING5_CTRL_COE1

Address: Operational Base(0x27961200) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking5_idx_n3 Peaking_ctrl band5 negative half axis ctrl point index3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking5_idx_n2 Peaking_ctrl band5 negative half axis ctrl point index2

SHARP_PEAKING5_CTRL_COE2

Address: Operational Base(0x27961200) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking5_idx_p1 Peaking_ctrl band5 positive half axis ctrl point index1
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8:0	RW	0x000	sw_peaking5_idx_p0 Peaking_ctrl band5 positive half axis ctrl point index0

SHARP_PEAKING5_CTRL_COE3

Address: Operational Base(0x27961200) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking5_idx_p3 Peaking_ctrl band5 positive half axis ctrl point index3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking5_idx_p2 Peaking_ctrl band5 positive half axis ctrl point index2

SHARP_PEAKING5_CTRL_COE4

Address: Operational Base(0x27961200) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking5_value_n2 Peaking_ctrl band5 negative half axis ctrl point value2
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking5_value_n1 Peaking_ctrl band5 negative half axis ctrl point value1

SHARP_PEAKING5_CTRL_COE5

Address: Operational Base(0x27961200) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking5_value_p1 Peaking_ctrl band5 positive half axis ctrl point value1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking5_value_n3 Peaking_ctrl band5 negative half axis ctrl point value3

SHARP_PEAKING5_CTRL_COE6

Address: Operational Base(0x27961200) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking5_value_p3 Peaking_ctrl band5 positive half axis ctrl point value3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking5_value_p2 Peaking_ctrl band5 positive half axis ctrl point value2

SHARP_PEAKING5_CTRL_COE7

Address: Operational Base(0x27961200) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking5_ratio_n12 Peaking_ctrl band5 negative half axis slope12
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking5_ratio_n01 Peaking_ctrl band5 negative half axis slope01

SHARP_PEAKING5_CTRL_COE8

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Address: Operational Base(0x27961200) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking5_ratio_p01 Peaking_ctrl band5 positive half axis slope01
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking5_ratio_n23 Peaking_ctrl band5 negative half axis slope23

SHARP_PEAKING5_CTRL_COE9

Address: Operational Base(0x27961200) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:12	RW	0x000	sw_peaking5_ratio_p23 Peaking_ctrl band5 positive half axis slope23
11:0	RW	0x000	sw_peaking5_ratio_p12 Peaking_ctrl band5 positive half axis slope12

SHARP_PEAKING6_CTRL_COE0

Address: Operational Base(0x27961200) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking6_idx_n1 Peaking_ctrl band6 negative half axis ctrl point index1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking6_idx_n0 Peaking_ctrl band6 negative half axis ctrl point index0

SHARP_PEAKING6_CTRL_COE1

Address: Operational Base(0x27961200) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking6_idx_n3 Peaking_ctrl band6 negative half axis ctrl point index3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking6_idx_n2 Peaking_ctrl band6 negative half axis ctrl point index2

SHARP_PEAKING6_CTRL_COE2

Address: Operational Base(0x27961200) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking6_idx_p1 Peaking_ctrl band6 positive half axis ctrl point index1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking6_idx_p0 Peaking_ctrl band6 positive half axis ctrl point index0

SHARP_PEAKING6_CTRL_COE3

Address: Operational Base(0x27961200) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking6_idx_p3 Peaking_ctrl band6 positive half axis ctrl point index3
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8:0	RW	0x000	sw_peaking6_idx_p2 Peaking_ctrl band6 positive half axis ctrl point index2

SHARP_PEAKING6_CTRL_COE4

Address: Operational Base(0x27961200) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking6_value_n2 Peaking_ctrl band6 negative half axis ctrl point value2
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking6_value_n1 Peaking_ctrl band6 negative half axis ctrl point value1

SHARP_PEAKING6_CTRL_COE5

Address: Operational Base(0x27961200) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking6_value_p1 Peaking_ctrl band6 positive half axis ctrl point value1
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking6_value_n3 Peaking_ctrl band6 negative half axis ctrl point value3

SHARP_PEAKING6_CTRL_COE6

Address: Operational Base(0x27961200) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking6_value_p3 Peaking_ctrl band6 positive half axis ctrl point value3
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_peaking6_value_p2 Peaking_ctrl band6 positive half axis ctrl point value2

SHARP_PEAKING6_CTRL_COE7

Address: Operational Base(0x27961200) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking6_ratio_n12 Peaking_ctrl band6 negative half axis slope12
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking6_ratio_n01 Peaking_ctrl band6 negative half axis slope01

SHARP_PEAKING6_CTRL_COE8

Address: Operational Base(0x27961200) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking6_ratio_p01 Peaking_ctrl band6 positive half axis slope01
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking6_ratio_n23 Peaking_ctrl band6 negative half axis slope23

SHARP_PEAKING6_CTRL_COE9

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Address: Operational Base(0x27961200) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:12	RW	0x000	sw_peaking6_ratio_p23 Peaking_ctrl band6 positive half axis slope23
11:0	RW	0x000	sw_peaking6_ratio_p12 Peaking_ctrl band6 positive half axis slope12

SHARP_PEAKING_CTRL0

Address: Operational Base(0x27961200) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	sw_nondir_wgt_ratio Ratio for non-direct weight
23:20	RW	0x0	sw_dir_cmp_ratio Ratio for direction judgment
19	RO	0x0	reserved
18:12	RW	0x00	sw_nondir_thr Peaking-edge proc non-dir threshold
11:10	RO	0x0	reserved
9:0	RW	0x000	sw_peaking_gain Peaking gain

SHARP_PEAKING_CTRL1

Address: Operational Base(0x27961200) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:20	RW	0x00	sw_diag_dir_thr Threshold of diagonal direction
19:16	RW	0x0	sw_dir_cnt_offset Offset of direction count
15	RO	0x0	reserved
14:12	RW	0x0	sw_dir_cnt_avg Setting average direction count
11:8	RW	0x0	sw_dir_cnt_thr Threshold of direction count
7:0	RW	0x00	sw_nondir_wgt_offset Offset for non-direct weight

SHARP_PEAKING_CTRL2

Address: Operational Base(0x27961200) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_diag_adjgain_tab7 Diagonal adjust gain table idx7
27:24	RW	0x0	sw_diag_adjgain_tab6 Diagonal adjust gain table idx6
23:20	RW	0x0	sw_diag_adjgain_tab5 Diagonal adjust gain table idx5
19:16	RW	0x0	sw_diag_adjgain_tab4 Diagonal adjust gain table idx4
15:12	RW	0x0	sw_diag_adjgain_tab3 Diagonal adjust gain table idx3
11:8	RW	0x0	sw_diag_adjgain_tab2 Diagonal adjust gain table idx2

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	sw_diag_adjgain_tab1 Diagonal adjust gain table idx1
3:0	RW	0x0	sw_diag_adjgain_tab0 Diagonal adjust gain table idx0

SHARP_PEAKING_CTRL3

Address: Operational Base(0x27961200) + offset (0x019C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_edge_alpha_under_unlimit_non Peaking-edge proc shootCtrl undershoot unlimit ctrl for non-direct area
23	RO	0x0	reserved
22:16	RW	0x00	sw_edge_alpha_over_unlimit_non Peaking-edge proc shootCtrl overshoot unlimit ctrl for non-direct area
15	RO	0x0	reserved
14:8	RW	0x00	sw_edge_alpha_under_non Peaking-edge proc shootCtrl undershoot ctrl for non-direct area
7	RO	0x0	reserved
6:0	RW	0x00	sw_edge_alpha_over_non Peaking-edge proc shootCtrl overshoot ctrl for non-direct area

SHARP_PEAKING_CTRL4

Address: Operational Base(0x27961200) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_edge_alpha_under_unlimit_v Peaking-edge proc shootCtrl undershoot unlimit ctrl for ver-direct area
23	RO	0x0	reserved
22:16	RW	0x00	sw_edge_alpha_over_unlimit_v Peaking-edge proc shootCtrl overshoot unlimit ctrl for ver-direct area
15	RO	0x0	reserved
14:8	RW	0x00	sw_edge_alpha_under_v Peaking-edge proc shootCtrl undershoot ctrl for ver-direct area
7	RO	0x0	reserved
6:0	RW	0x00	sw_edge_alpha_over_v Peaking-edge proc shootCtrl overshoot ctrl for ver-direct area

SHARP_PEAKING_CTRL5

Address: Operational Base(0x27961200) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_edge_alpha_under_unlimit_h Peaking-edge proc shootCtrl undershoot unlimit ctrl for hor-direct area
23	RO	0x0	reserved
22:16	RW	0x00	sw_edge_alpha_over_unlimit_h Peaking-edge proc shootCtrl overshoot unlimit ctrl for hor-direct area
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:8	RW	0x00	sw_edge_alpha_under_h Peaking-edge proc shootCtrl undershoot ctrl for hor-direct area
7	RO	0x0	reserved
6:0	RW	0x00	sw_edge_alpha_over_h Peaking-edge proc shootCtrl overshoot ctrl for hor-direct area

SHARP_PEAKING_CTRL6

Address: Operational Base(0x27961200) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_edge_alpha_under_unlimit_d0 Peaking-edge proc shootCtrl undershoot unlimit ctrl for diag0-direct area
23	RO	0x0	reserved
22:16	RW	0x00	sw_edge_alpha_over_unlimit_d0 Peaking-edge proc shootCtrl overshoot unlimit ctrl for diag0-direct area
15	RO	0x0	reserved
14:8	RW	0x00	sw_edge_alpha_under_d0 Peaking-edge proc shootCtrl undershoot ctrl for diag0-direct area
7	RO	0x0	reserved
6:0	RW	0x00	sw_edge_alpha_over_d0 Peaking-edge proc shootCtrl overshoot ctrl for diag0-direct area

SHARP_PEAKING_CTRL7

Address: Operational Base(0x27961200) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_edge_alpha_under_unlimit_d1 Peaking-edge proc shootCtrl undershoot unlimit ctrl for diag1-direct area
23	RO	0x0	reserved
22:16	RW	0x00	sw_edge_alpha_over_unlimit_d1 Peaking-edge proc shootCtrl overshoot unlimit ctrl for diag1-direct area
15	RO	0x0	reserved
14:8	RW	0x00	sw_edge_alpha_under_d1 Peaking-edge proc shootCtrl undershoot ctrl for diag1-direct area
7	RO	0x0	reserved
6:0	RW	0x00	sw_edge_alpha_over_d1 Peaking-edge proc shootCtrl overshoot ctrl for diag1-direct area

SHARP_PEAKING_CTRL8

Address: Operational Base(0x27961200) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	sw_edge_delta_offset_h Peaking-edge proc hor-direct shootCtrl delta offset
15:8	RW	0x00	sw_edge_delta_offset_v Peaking-edge proc ver-direct shootCtrl delta offset
7:0	RW	0x00	sw_edge_delta_offset_non Peaking-edge proc non-direct shootCtrl delta offset

SHARP_PEAKING_CTRL9

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Address: Operational Base(0x27961200) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	sw_edge_delta_offset_d1 Peaking-edge proc diag1-direct shootCtrl delta offset
7:0	RW	0x00	sw_edge_delta_offset_d0 Peaking-edge proc diag0-direct shootCtrl delta offset

SHARP_SHOOT_CTRL0

Address: Operational Base(0x27961200) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:20	RW	0x00	sw_shoot_alpha_under ShootCtrl undershoot ctrl
19	RO	0x0	reserved
18:12	RW	0x00	sw_shoot_alpha_over ShootCtrl overshoot ctrl
11:4	RW	0x00	sw_shoot_delta_offset ShootCtrl delta offset
3:1	RO	0x0	reserved
0	RW	0x0	sw_shoot_filt_radius ShootCtrl max/min filter radius

SHARP_SHOOT_CTRL1

Address: Operational Base(0x27961200) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x00	sw_shoot_alpha_under_unlimit ShootCtrl undershoot unlimit ctrl
7	RO	0x0	reserved
6:0	RW	0x00	sw_shoot_alpha_over_unlimit ShootCtrl overshoot unlimit ctrl

SHARP_GAIN_CTRL0

Address: Operational Base(0x27961200) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:20	RW	0x00	sw_adp_idx2 Ctrl index2 for sharpness strength ctrl by gradient
19:18	RO	0x0	reserved
17:10	RW	0x00	sw_adp_idx1 Ctrl index1 for sharpness strength ctrl by gradient
9:8	RO	0x0	reserved
7:0	RW	0x00	sw_adp_idx0 Ctrl index0 for sharpness strength ctrl by gradient

SHARP_GAIN_CTRL1

Address: Operational Base(0x27961200) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:20	RW	0x00	sw_adp_gain1 Ctrl gain1 for sharpness strength ctrl by gradient
19	RO	0x0	reserved
18:12	RW	0x00	sw_adp_gain0 Ctrl gain0 for sharpness strength ctrl by gradient

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Bit	Attr	Reset Value	Description
11:8	RO	0x0	reserved
7:0	RW	0x00	sw_adp_idx3 Ctrl index3 for sharpness strength ctrl by gradient

SHARP_GAIN_CTRL2

Address: Operational Base(0x27961200) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x00	sw_adp_gain4 Ctrl gain4 for sharpness strength ctrl by gradient
15	RO	0x0	reserved
14:8	RW	0x00	sw_adp_gain3 Ctrl gain3 for sharpness strength ctrl by gradient
7	RO	0x0	reserved
6:0	RW	0x00	sw_adp_gain2 Ctrl gain2 for sharpness strength ctrl by gradient

SHARP_GAIN_CTRL3

Address: Operational Base(0x27961200) + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:12	RW	0x000	sw_adp_slp12 Ctrl slope12 for sharpness strength ctrl by gradient
11	RO	0x0	reserved
10:0	RW	0x000	sw_adp_slp01 Ctrl slope01 for sharpness strength ctrl by gradient

SHARP_GAIN_CTRL4

Address: Operational Base(0x27961200) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:12	RW	0x000	sw_adp_slp34 Ctrl slope34 for sharpness strength ctrl by gradient
11	RO	0x0	reserved
10:0	RW	0x000	sw_adp_slp23 Ctrl slope23 for sharpness strength ctrl by gradient

SHARP_GAIN_CTRL5

Address: Operational Base(0x27961200) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:21	RW	0x00	sw_var_idx1 Ctrl index1 for sharpness strength ctrl by gradient
20:19	RO	0x0	reserved
18:11	RW	0x00	sw_var_idx0 Ctrl index0 for sharpness strength ctrl by gradient
10:0	RW	0x000	sw_adp_slp45 Ctrl slope45 for sharpness strength ctrl by gradient

SHARP_GAIN_CTRL6

Address: Operational Base(0x27961200) + offset (0x0208)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30:24	RW	0x00	sw_var_gain0 Ctrl gain0 for sharpness strength ctrl by gradient
23:20	RO	0x0	reserved
19:12	RW	0x00	sw_var_idx3 Ctrl index3 for sharpness strength ctrl by gradient
11:8	RO	0x0	reserved
7:0	RW	0x00	sw_var_idx2 Ctrl index2 for sharpness strength ctrl by gradient

SHARP_GAIN_CTRL7

Address: Operational Base(0x27961200) + offset (0x020C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_var_gain4 Ctrl gain4 for sharpness strength ctrl by gradient
23	RO	0x0	reserved
22:16	RW	0x00	sw_var_gain3 Ctrl gain3 for sharpness strength ctrl by gradient
15	RO	0x0	reserved
14:8	RW	0x00	sw_var_gain2 Ctrl gain2 for sharpness strength ctrl by gradient
7	RO	0x0	reserved
6:0	RW	0x00	sw_var_gain1 Ctrl gain1 for sharpness strength ctrl by gradient

SHARP_GAIN_CTRL8

Address: Operational Base(0x27961200) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:12	RW	0x000	sw_var_slp12 Ctrl slope12 for sharpness strength ctrl by gradient
11	RO	0x0	reserved
10:0	RW	0x000	sw_var_slp01 Ctrl slope01 for sharpness strength ctrl by gradient

SHARP_GAIN_CTRL9

Address: Operational Base(0x27961200) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:12	RW	0x000	sw_var_slp34 Ctrl slope34 for sharpness strength ctrl by gradient
11	RO	0x0	reserved
10:0	RW	0x000	sw_var_slp23 Ctrl slope23 for sharpness strength ctrl by gradient

SHARP_GAIN_CTRL10

Address: Operational Base(0x27961200) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:20	RW	0x00	sw_lum_idx0 Ctrl index0 for sharpness strength ctrl by luma
19:18	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
17:16	RW	0x0	sw_lum_select Luma mode select, 0-Yin, 1-mean3x3 filt result, 2-mean5x5 filt result
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_var_slp45 Ctrl slope45 for sharpness strength ctrl by gradient

SHARP_GAIN_CTRL11

Address: Operational Base(0x27961200) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:20	RW	0x00	sw_lum_idx3 Ctrl index3 for sharpness strength ctrl by luma
19:18	RO	0x0	reserved
17:10	RW	0x00	sw_lum_idx2 Ctrl index2 for sharpness strength ctrl by luma
9:8	RO	0x0	reserved
7:0	RW	0x00	sw_lum_idx1 Ctrl index1 for sharpness strength ctrl by luma

SHARP_GAIN_CTRL12

Address: Operational Base(0x27961200) + offset (0x0220)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_lum_gain3 Ctrl gain3 for sharpness strength ctrl by luma
23	RO	0x0	reserved
22:16	RW	0x00	sw_lum_gain2 Ctrl gain2 for sharpness strength ctrl by luma
15	RO	0x0	reserved
14:8	RW	0x00	sw_lum_gain1 Ctrl gain1 for sharpness strength ctrl by luma
7	RO	0x0	reserved
6:0	RW	0x00	sw_lum_gain0 Ctrl gain0 for sharpness strength ctrl by luma

SHARP_GAIN_CTRL13

Address: Operational Base(0x27961200) + offset (0x0224)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:20	RW	0x000	sw_lum_slp12 Ctrl slope12 for sharpness strength ctrl by luma
19	RO	0x0	reserved
18:8	RW	0x000	sw_lum_slp01 Ctrl slope01 for sharpness strength ctrl by luma
7	RO	0x0	reserved
6:0	RW	0x00	sw_lum_gain4 Ctrl gain4 for sharpness strength ctrl by luma

SHARP_GAIN_CTRL14

Address: Operational Base(0x27961200) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:12	RW	0x000	sw_lum_slp34 Ctrl slope34 for sharpness strength ctrl by luma
11	RO	0x0	reserved
10:0	RW	0x000	sw_lum_slp23 Ctrl slope23 for sharpness strength ctrl by luma

SHARP_GAIN_CTRL15

Address: Operational Base(0x27961200) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x000	sw_lum_slp45 Ctrl slope45 for sharpness strength ctrl by luma

SHARP_COLORADJ_CTRL0

Address: Operational Base(0x27961200) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	sw_adj_scaling_coef0 Color adjust point0, gain_curve scaleing coef
23:20	RO	0x0	reserved
19:12	RW	0x00	sw_adj_point_y0 Color adjust point0, v value
11:8	RO	0x0	reserved
7:0	RW	0x00	sw_adj_point_x0 Color adjust point0, u value

SHARP_COLORADJ_CTRL1

Address: Operational Base(0x27961200) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_coloradj_tab0_5 Color adjust point0, gain_curve_5
24:20	RW	0x00	sw_coloradj_tab0_4 Color adjust point0, gain_curve_4
19:15	RW	0x00	sw_coloradj_tab0_3 Color adjust point0, gain_curve_3
14:10	RW	0x00	sw_coloradj_tab0_2 Color adjust point0, gain_curve_2
9:5	RW	0x00	sw_coloradj_tab0_1 Color adjust point0, gain_curve_1
4:0	RW	0x00	sw_coloradj_tab0_0 Color adjust point0, gain_curve_0

SHARP_COLORADJ_CTRL2

Address: Operational Base(0x27961200) + offset (0x0238)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_coloradj_tab0_11 Color adjust point0, gain_curve_11
24:20	RW	0x00	sw_coloradj_tab0_10 Color adjust point0, gain_curve_10
19:15	RW	0x00	sw_coloradj_tab0_9 Color adjust point0, gain_curve_9

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Bit	Attr	Reset Value	Description
14:10	RW	0x00	sw_coloradj_tab0_8 Color adjust point0, gain_curve_8
9:5	RW	0x00	sw_coloradj_tab0_7 Color adjust point0, gain_curve_7
4:0	RW	0x00	sw_coloradj_tab0_6 Color adjust point0, gain_curve_6

SHARP_COLORADJ_CTRL3

Address: Operational Base(0x27961200) + offset (0x023C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x00	sw_coloradj_tab0_15 Color adjust point0, gain_curve_15
14:10	RW	0x00	sw_coloradj_tab0_14 Color adjust point0, gain_curve_14
9:5	RW	0x00	sw_coloradj_tab0_13 Color adjust point0, gain_curve_13
4:0	RW	0x00	sw_coloradj_tab0_12 Color adjust point0, gain_curve_12

SHARP_COLORADJ_CTRL4

Address: Operational Base(0x27961200) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	sw_adj_scaling_coef1 Color adjust point1, gain_curve scaleing coef
23:20	RO	0x0	reserved
19:12	RW	0x00	sw_adj_point_y1 Color adjust point1, v value
11:8	RO	0x0	reserved
7:0	RW	0x00	sw_adj_point_x1 Color adjust point1, u value

SHARP_COLORADJ_CTRL5

Address: Operational Base(0x27961200) + offset (0x0244)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_coloradj_tab1_5 Color adjust point1, gain_curve_5
24:20	RW	0x00	sw_coloradj_tab1_4 Color adjust point1, gain_curve_4
19:15	RW	0x00	sw_coloradj_tab1_3 Color adjust point1, gain_curve_3
14:10	RW	0x00	sw_coloradj_tab1_2 Color adjust point1, gain_curve_2
9:5	RW	0x00	sw_coloradj_tab1_1 Color adjust point1, gain_curve_1
4:0	RW	0x00	sw_coloradj_tab1_0 Color adjust point1, gain_curve_0

SHARP_COLORADJ_CTRL6

Address: Operational Base(0x27961200) + offset (0x0248)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:25	RW	0x00	sw_coloradj_tab1_11 Color adjust point1, gain_curve_11
24:20	RW	0x00	sw_coloradj_tab1_10 Color adjust point1, gain_curve_10
19:15	RW	0x00	sw_coloradj_tab1_9 Color adjust point1, gain_curve_9
14:10	RW	0x00	sw_coloradj_tab1_8 Color adjust point1, gain_curve_8
9:5	RW	0x00	sw_coloradj_tab1_7 Color adjust point1, gain_curve_7
4:0	RW	0x00	sw_coloradj_tab1_6 Color adjust point1, gain_curve_6

SHARP_COLORADJ_CTRL7

Address: Operational Base(0x27961200) + offset (0x024C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x00	sw_coloradj_tab1_15 Color adjust point1, gain_curve_15
14:10	RW	0x00	sw_coloradj_tab1_14 Color adjust point1, gain_curve_14
9:5	RW	0x00	sw_coloradj_tab1_13 Color adjust point1, gain_curve_13
4:0	RW	0x00	sw_coloradj_tab1_12 Color adjust point1, gain_curve_12

SHARP_COLORADJ_CTRL8

Address: Operational Base(0x27961200) + offset (0x0250)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	sw_adj_scaling_coef2 Color adjust point2, gain_curve scaleing coef
23:20	RO	0x0	reserved
19:12	RW	0x00	sw_adj_point_y2 Color adjust point2, v value
11:8	RO	0x0	reserved
7:0	RW	0x00	sw_adj_point_x2 Color adjust point2, u value

SHARP_COLORADJ_CTRL9

Address: Operational Base(0x27961200) + offset (0x0254)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_coloradj_tab2_5 Color adjust point2, gain_curve_5
24:20	RW	0x00	sw_coloradj_tab2_4 Color adjust point2, gain_curve_4
19:15	RW	0x00	sw_coloradj_tab2_3 Color adjust point2, gain_curve_3
14:10	RW	0x00	sw_coloradj_tab2_2 Color adjust point2, gain_curve_2
9:5	RW	0x00	sw_coloradj_tab2_1 Color adjust point2, gain_curve_1

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	sw_coloradj_tab2_0 Color adjust point2, gain_curve_0

SHARP_COLORADJ_CTRL10

Address: Operational Base(0x27961200) + offset (0x0258)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_coloradj_tab2_11 Color adjust point2, gain_curve_11
24:20	RW	0x00	sw_coloradj_tab2_10 Color adjust point2, gain_curve_10
19:15	RW	0x00	sw_coloradj_tab2_9 Color adjust point2, gain_curve_9
14:10	RW	0x00	sw_coloradj_tab2_8 Color adjust point2, gain_curve_8
9:5	RW	0x00	sw_coloradj_tab2_7 Color adjust point2, gain_curve_7
4:0	RW	0x00	sw_coloradj_tab2_6 Color adjust point2, gain_curve_6

SHARP_COLORADJ_CTRL11

Address: Operational Base(0x27961200) + offset (0x025C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x00	sw_coloradj_tab2_15 Color adjust point2, gain_curve_15
14:10	RW	0x00	sw_coloradj_tab2_14 Color adjust point2, gain_curve_14
9:5	RW	0x00	sw_coloradj_tab2_13 Color adjust point2, gain_curve_13
4:0	RW	0x00	sw_coloradj_tab2_12 Color adjust point2, gain_curve_12

SHARP_COLORADJ_CTRL12

Address: Operational Base(0x27961200) + offset (0x0260)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	sw_adj_scaling_coef3 Color adjust point3, gain_curve scaleing coef
23:20	RO	0x0	reserved
19:12	RW	0x00	sw_adj_point_y3 Color adjust point3, v value
11:8	RO	0x0	reserved
7:0	RW	0x00	sw_adj_point_x3 Color adjust point3, u value

SHARP_COLORADJ_CTRL13

Address: Operational Base(0x27961200) + offset (0x0264)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_coloradj_tab3_5 Color adjust point3, gain_curve_5
24:20	RW	0x00	sw_coloradj_tab3_4 Color adjust point3, gain_curve_4

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Bit	Attr	Reset Value	Description
19:15	RW	0x00	sw_coloradj_tab3_3 Color adjust point3, gain_curve_3
14:10	RW	0x00	sw_coloradj_tab3_2 Color adjust point3, gain_curve_2
9:5	RW	0x00	sw_coloradj_tab3_1 Color adjust point3, gain_curve_1
4:0	RW	0x00	sw_coloradj_tab3_0 Color adjust point3, gain_curve_0

SHARP_COLORADJ_CTRL14

Address: Operational Base(0x27961200) + offset (0x0268)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_coloradj_tab3_11 Color adjust point3, gain_curve_11
24:20	RW	0x00	sw_coloradj_tab3_10 Color adjust point3, gain_curve_10
19:15	RW	0x00	sw_coloradj_tab3_9 Color adjust point3, gain_curve_9
14:10	RW	0x00	sw_coloradj_tab3_8 Color adjust point3, gain_curve_8
9:5	RW	0x00	sw_coloradj_tab3_7 Color adjust point3, gain_curve_7
4:0	RW	0x00	sw_coloradj_tab3_6 Color adjust point3, gain_curve_6

SHARP_COLORADJ_CTRL15

Address: Operational Base(0x27961200) + offset (0x026C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x00	sw_coloradj_tab3_15 Color adjust point3, gain_curve_15
14:10	RW	0x00	sw_coloradj_tab3_14 Color adjust point3, gain_curve_14
9:5	RW	0x00	sw_coloradj_tab3_13 Color adjust point3, gain_curve_13
4:0	RW	0x00	sw_coloradj_tab3_12 Color adjust point3, gain_curve_12

SHARP_TEXTURE_CTRL0

Address: Operational Base(0x27961200) + offset (0x0270)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	sw_tex_idx1 Texture adjust index1
15:12	RO	0x0	reserved
11:4	RW	0x00	sw_tex_idx0 Texture adjust index0
3	RO	0x0	reserved
2:1	RW	0x0	sw_ymode_select Texture adjust result mode select, 0-sharp_result, 1-y_ori, 2-mean3x3 filt result, 3-mean5x5 filt result

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Bit	Attr	Reset Value	Description
0	RW	0x0	sw_idxmode_select Texture adjust idx mode select, 0: direct_wgt, 1: Y_high_freq

SHARP_TEXTURE_CTRL1

Address: Operational Base(0x27961200) + offset (0x0274)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_tex_gain0 Texture adjust gain0
23:20	RO	0x0	reserved
19:12	RW	0x00	sw_tex_idx3 Texture adjust index3
11:8	RO	0x0	reserved
7:0	RW	0x00	sw_tex_idx2 Texture adjust index2

SHARP_TEXTURE_CTRL2

Address: Operational Base(0x27961200) + offset (0x0278)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_tex_gain4 Texture adjust gain4
23	RO	0x0	reserved
22:16	RW	0x00	sw_tex_gain3 Texture adjust gain3
15	RO	0x0	reserved
14:8	RW	0x00	sw_tex_gain2 Texture adjust gain2
7	RO	0x0	reserved
6:0	RW	0x00	sw_tex_gain1 Texture adjust gain1

SHARP_TEXTURE_CTRL3

Address: Operational Base(0x27961200) + offset (0x027C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:12	RW	0x000	sw_tex_slp12 Texture adjust slope12
11	RO	0x0	reserved
10:0	RW	0x000	sw_tex_slp01 Texture adjust slope01

SHARP_TEXTURE_CTRL4

Address: Operational Base(0x27961200) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:12	RW	0x000	sw_tex_slp34 Texture adjust slope34
11	RO	0x0	reserved
10:0	RW	0x000	sw_tex_slp23 Texture adjust slope23

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SHARP_TEXTURE_CTRL5

Address: Operational Base(0x27961200) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x000	sw_tex_slp45 Texture adjust slope45

SHARP_LTI_CTRL0

Address: Operational Base(0x27961200) + offset (0x0288)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_ltih_thr1 Hor-direct Lti gain threshold
15:13	RO	0x0	reserved
12:4	RW	0x000	sw_ltih_slp1 Hor-direct Lti gain slope
3:1	RO	0x0	reserved
0	RW	0x0	sw_ltih_radius Hor-direct Lti max/min filter radius, 0: radius=3, 1: radius=5

SHARP_LTI_CTRL1

Address: Operational Base(0x27961200) + offset (0x028C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	sw_ltih_tigain Hor-direct Lti gain
23:22	RO	0x0	reserved
21:12	RW	0x000	sw_ltih_noisethrpos Hor-direct Lti positive noise threshold
11:10	RO	0x0	reserved
9:0	RW	0x000	sw_ltih_noisethrneg Hor-direct Lti negative noise threshold

SHARP_LTI_CTRL2

Address: Operational Base(0x27961200) + offset (0x0290)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_ltiv_thr1 Ver-direct Lti gain threshold
15:13	RO	0x0	reserved
12:4	RW	0x000	sw_ltiv_slp1 Ver-direct Lti gain slope
3:1	RO	0x0	reserved
0	RW	0x0	sw_ltiv_radius Ver-direct Lti max/min filter radius, 0: radius=3, 1: radius=5

SHARP_LTI_CTRL3

Address: Operational Base(0x27961200) + offset (0x0294)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	sw_ltiv_tigain Ver-direct Lti gain
23:22	RO	0x0	reserved
21:12	RW	0x000	sw_ltiv_noisethrpos Ver-direct Lti positive noise threshold

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Bit	Attr	Reset Value	Description
11:10	RO	0x0	reserved
9:0	RW	0x000	sw_ltiv_noisethrneg Ver-direct Lti negative noise threshold

SHARP_CTI_CTRL0

Address: Operational Base(0x27961200) + offset (0x0298)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_ctih_thr1 Hor-direct Cti gain threshold
15:13	RO	0x0	reserved
12:4	RW	0x000	sw_ctih_slp1 Hor-direct Cti gain slope
3:1	RO	0x0	reserved
0	RW	0x0	sw_ctih_radius Hor-direct Cti max/min filter radius, 0: radius=3, 1: radius=5

SHARP_CTI_CTRL1

Address: Operational Base(0x27961200) + offset (0x029C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	sw_ctih_tigain Hor-direct Cti gain
23:22	RO	0x0	reserved
21:12	RW	0x000	sw_ctih_noisethrpos Hor-direct Cti positive noise threshold
11:10	RO	0x0	reserved
9:0	RW	0x000	sw_ctih_noisethrneg Hor-direct Cti negative noise threshold

SHARP_DEBUG_CTRL0

Address: Operational Base(0x27961200) + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	sw_debug_mode Sharp ink mode

2.5 Application Notes

2.5.1 DEI Application Notes

Input source definition constraint

The input source definition(destination definition is same with source) must be 16x4 aligned, which means the image width 16 aligned and image height 4 aligned.

Normal configuration flow

- Set DEI related signals based on current video source information and deinterlace mode (must open frame done interruption by asserting the sw_dei_frm_done_en signal)
- Set sw_vdpp_working_mode = 1
- Set frame start by setting signal sw_dei_frm_en = 1
- Wait for DEI frame done interruption
- Read back many kinds of Detection data and MVHIST, analyze these data, get the global MV, OSD information etc

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- Configure the MV, OSD information back
- Set frame start for deinterlace loop

2.5.2 VEP Application Notes

Configuration constraint

- The input source definition must be 16x8 aligned, which means the image width 16 aligned and image height 8 aligned
- The output source definition must be 16x2 aligned
- The virtual stride of input and output must 16 byte align
- The smallest input and output definition is 64x16

Normal configuration flow

- Set VEP related signals based on current video source information
- Set sw_vdpp_working_mode = 2
- Set frame start by setting signal sw_vdpp_frm_en = 1
- Wait for VEP frame done interruption
- Set frame start for next loop

DEI+VEP configuration flow

- Start DEI configuration flow, set de-interlace related regs
- Set sw_vdpp_working_mode = 1，start deinterlace by setting signal sw_dei_frm_en = 1
- Wait for DEI frame done interruption
- Start VEP configuration flow, set VEP related regs
- Set sw_vdpp_working_mode = 2, start VEP by setting signal sw_vep_frm_en = 1
- Wait for VEP frame done interruption
- Next DEI+VEP loop

YUVDIFF mode

In Normal configuration flow, set sw_vep_yuvout_diff_en = 1(VEP_CONFIG, 0x0004), set destination image uv component output size(VEP_DST_IMG_SIZE_C, 0x0040).

2.5.3 DCIHIST Application Notes

Normal configuration flow

- Set VEP and DCI related signals based on current video source information
- Set sw_vdpp_working_mode = 3
- Set frame start by setting signal sw_vep_frm_en = 1
- Wait for VEP frame done interruption
- Set frame start for next loop

2.5.4 Some application scenarios

Scenario	Input	Operation
DEI only Case 1	Only i source input	Configure in DEI mode, use VDPP as DEI, refer to DEI for usage
DEI only Case 2	Only i source input	i source is first converted to p source by DEI, then the output p source is used as input, configure in VEP mode, equivalent to i source doing DEI+VEP

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VEP only	One or more small p source inputs	Each route does time division multiplexing, only configure in VEP mode
DCIHIST only	Independent source that needs to do DCI. The source may be ARGB, or it may be yuv4k 10bit source	Only do DCIHIST statistics, only output statistical results to DDR
DEI+VEP Case 1	One i source + one p source	i source is configured in DEI mode, p source is configured in VEP mode, each does its own thing, time division multiplexing, the base addresses and interrupts of the two configurations are different
DEI+VEP Case 2	One i source + one p source	i source: DEI+VEP, p source: VEP
DEI+DCI	One i source + one independent source that needs to do DCI	i source: DEI, DCI source: DCIHIST. In this case, it is generally for 4K source to do DCIHIST. At this time, the effects of other sources are not important, but i source must do DEI
DEI+VEP+DCI	One i source + one p source + one independent source that needs to do DCI	i source: DEI, p source: VEP, DCI source: DCIHIST. This is a three-way time division multiplexing, which is rarely used

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CHAPTER 3 Video Processing Sub-System (VPSS)

3.1 Introduction

3.1.1 Overview

The Video Processing Sub-System (VPSS) is an image and video stream processing unit with multi-channel output, including video mirror/flip, occlusion, cropping, scaling, rotation, and other functions.

All data is transmitted via the Memory Interface (MI) to an AXI bus system with master interface. Programming is done by register read/write transactions with an AHB slave interface.

VPSS supports the following features:

- Offline DMA input:
  - Line RGB888/ARGB888/RGB565/YUV422/YUV420 SP 8bits
  - Tile4x4 YUV422/YUV420 8bit (Rotate 90/180/270)
  - RKFBCD64x4 YUV444/YUV422/YUV420 8bits
- Online ISP input
- Both DMA and ISP input
- Maximum input: 4672x3504 (width no more than 4672)
- Minimum input: 32x32
- YUV422 processing
- MIRROR: Horizontal Mirror
- CMSC: Cover or Mosaic in 8 areas
- CROP: Cropping on 4 channels
- Channel0 output:
  - Scale: Polyphase filter
  - ASPT_RATIO: Aspective Ratio for image boundary extension
  - Either Line YUV422/YUV420 SP 8bit or Tile4x4 YUV422/YUV420 8bits
  - Flip: Vertical Flip
- Channel1 output:
  - Scale: Bilinear filter
  - ASPT_RATIO: Aspective Ratio for image boundary extension
  - Either Line RGB888/ARGB888/RGB565/YUV422/YUV420 SP 8bits or Tile4x4 YUV422/YUV420 8bit
  - Flip: Vertical Flip
- Channel2 output:
  - Scale: Bilinear filter (output width no more than 1920)
  - ASPT_RATIO: Aspective Ratio for image boundary extension
  - Line YUV422/YUV420 SP 8bit
  - Flip: Vertical Flip
- Channel3 output:
  - Scale: Bilinear filter (output width no more than 1920)
  - ASPT_RATIO: Aspective Ratio for image boundary extension
  - Line YUV422/YUV420 SP 8bits
  - Flip: Vertical Flip
- Either channel0 or channel1 Tile4x4 output
- BUS interface: 32 bit AHB slave; AXI-128 RW; MMU table
- Registers configuration: AHB or AXI-Read
- Low power, auto-gating for each block

3.1.2 Using constrains

1. The virtual stride of all read and write channels is byte unit. Read virtual stride must be configured. When the input is in Line mode, the read virtual stride should be aligned by at least 4, and the image width should be aligned by 2 pixels.

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2. When the input mode is Tile4x4, the width and height of the image need to be aligned by 4 pixels. If the Tile4x4 input is rotated, its output is in yuv420 format.
3. When the RKFBCD64x4 decoding format is yuv444, its output is yuv422.
4. Tile4x4 write channel does not support scaling in yuv420 format.
5. For the scaling module of Channel2 and Channel3, if the vertical scaling is bypass, the horizontal scaling output width is not limited by 1920.

3.2 Block Diagram

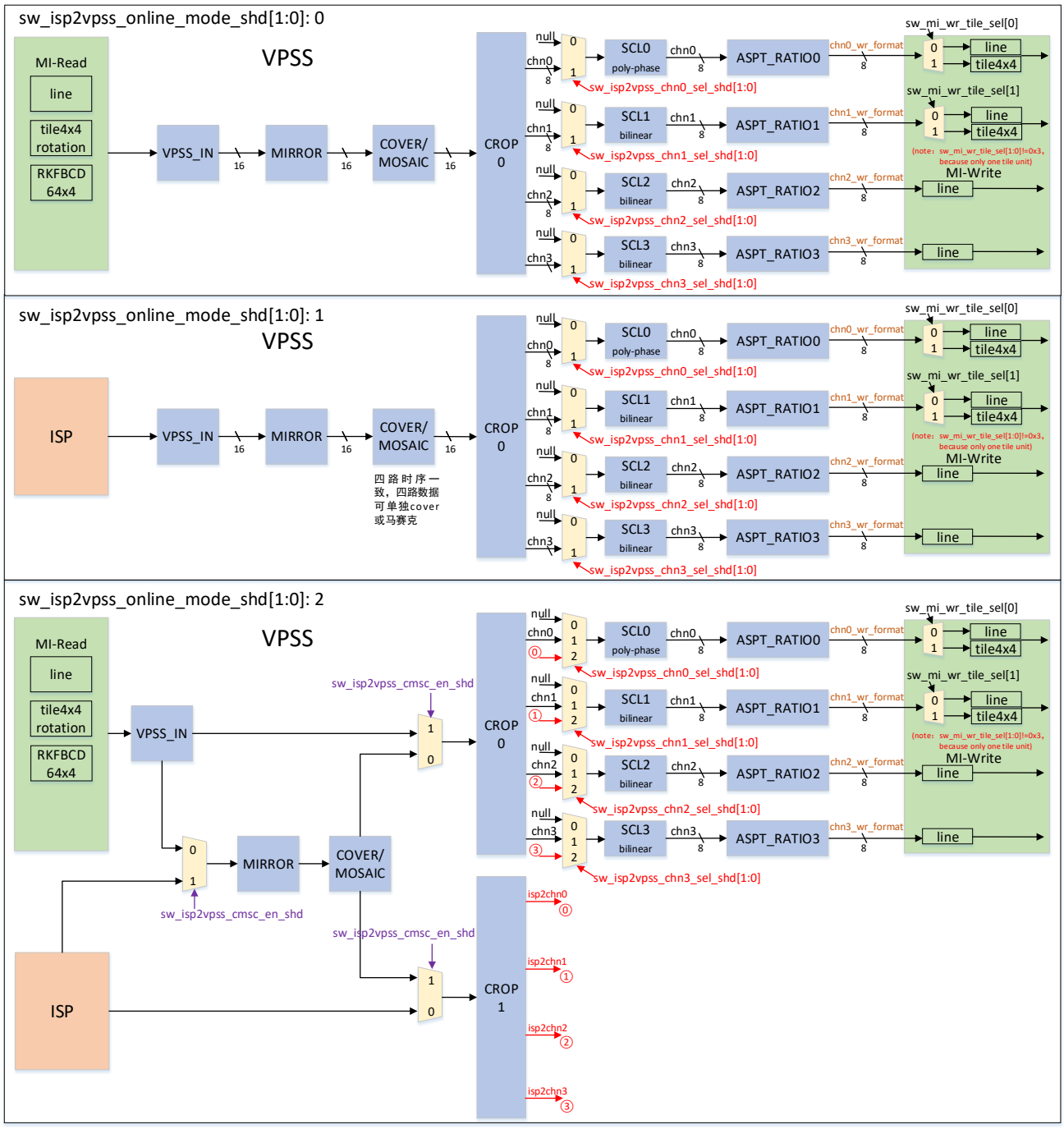


Fig. 3-1 VPSS Block Diagram

VPSS comprises with:

- ISP Direct Interface
- YUV422 Processing
- Memory Interface (MI)

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3.3 Function Description

3.3.1 Mirror

Horizontal mirror transformation of images in YUV processing.

3.3.2 CMSC

Cover or Mosaic (CMSC) implements the function of adding privacy occlusion to designated areas on the image, with the occlusion method being either specified color overlay or mosaic, and the area being any quadrilateral. The privacy occlusion can be added to four image output channels, which can be independently switched on or off.

3.3.3 Crop

VPSS has two cropping modules, where crop1 is only used by ISP in online mode2.Four output channels support cropping separately.

3.3.4 Scale

3.3.4.1 ZME

Zoom Manage Engine (ZME) is an image scaler based on polyphase filter that its characteristic is more approaching to ideal low pass filter. In addition, a new dering arithmetic is used to reduce the effect of ring.The horizontal and vertical filter taps are 8 and 6, respectively. ZME is used for channel0 scaling in VPSS.

Zoom ratio: Horizontal and vertical scaling are independent of each other. Horizontal arbitrary non-integer scaling ratio, from 1/7 to 8. Vertical arbitrary non-integer scaling ratio, from 1/6 to 6.

3.3.4.2 Bilinear

Bilinear filter is a common interpolation model, which performs Linear interpolation in the horizontal and vertical directions respectively to achieve the purpose of Image scaling. Bilinear interpolation is used for channel1~3 scaling in VPSS.

Zoom ratio: Horizontal and vertical scaling are independent of each other. Horizontal arbitrary non-integer scaling ratio, from 1/32 to 32. Vertical arbitrary non-integer scaling ratio, from 1/32 to 32.

3.3.5 Aspective Ratio

The screen aspect ratio module is used to expand image boundaries.

3.3.6 Memory Interface (MI)

The memory interface unit (MI) is responsible for reading/writing image data from/to the system memory(DDR). The MI has five main tasks, which can operate independently:

- Take image data from the DDR to VPSS
  - Line mode: Either in YCbCr or RGB format
  - Tile mode: YCbCr format
  - RKFBCD mode: YCbCr format
- Take image data from the channel0 to DDR
  - Line mode: YCbCr format
  - Tile mode: YCbCr format, either in channel0 or channel1
- Take image data from the channel1 to DDR
  - Line mode: either in YCbCr or RGB format
  - Tile mode: YCbCr format, either in channel0 or channel1
- Take image data from the channel2, YCbCr format of line mode, and write it into DDR.
- Take image data from the channel3, YCbCr format of line mode, and write it into DDR.

Memory Interface is as following:

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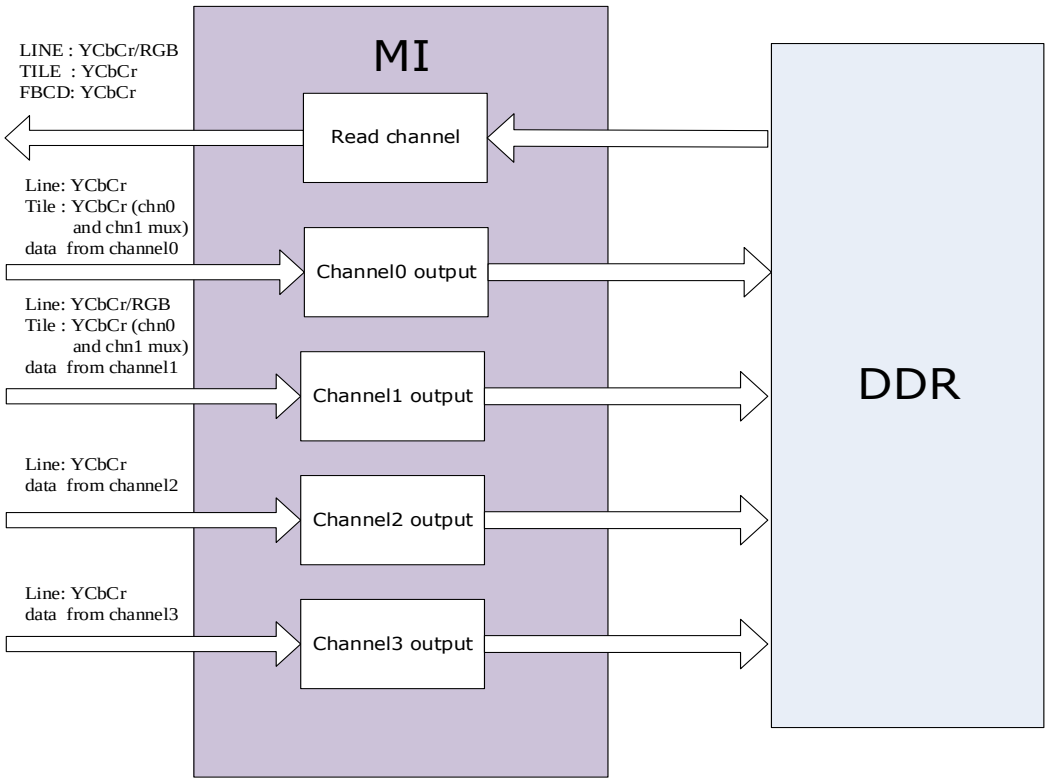


Fig. 3-2 Memory Interface

3.4 Register Description

VPSS adopts a distributed register configuration scheme, so there is no central unit containing all programming registers, but all sub-modules contain their own programming registers. An address space is reserved for each sub-module inside the total VPSS controller.

Table 3-1 VPSS module base address

Module	Description	Offset Address
VPSS_REG	Main control	0x0000
CMSC	Cover and Mosaic	0x0500
QUAD_CROP	VPSS crop	0x0700
	ISP crop	0x0800
SCALE	Chn0 scale, zoom manage engine, poly-phase filter	0x1000
	Chn1 sacle, bilinear	0x1c00
	Chn2 sacle, bilinear	0x2800
	Chn3 sacle, bilinear	0x2c00
ASPECT_RATIO	Chn0 aspective ratio	0x1900
	Chn1 aspective ratio	0x2500
	Chn2 aspective ratio	0x2900
	Chn3 aspective ratio	0x2d00
MI	Memory interface	0x3000
MMU	Memory management unit	0x3f00

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3.4.1 Registers Summary

3.4.1.1 VPSS_REG

Name	Offset	Size	Reset Value	Description
VPSS_REG_0000_VPSS_CTRL	0x0000	W	0x00000000	VPSS global control
VPSS_REG_0000_VPSS_ONLINE	0x0004	W	0x00000000	ISP to VPSS online mode
VPSS_REG_0000_VPSS_ONLINE2_SIZE	0x0008	W	0x00000000	ISP to VPSS online mode2 size
VPSS_REG_0000_VPSS_VERSION	0x000C	W	0x31002106	Revision identification register
VPSS_REG_0000_VPSS_UPDATE	0x0010	W	0x00000022	Shadow update register
VPSS_REG_0000_VPSS_CLK_EN	0x0014	W	0x00010FFF	Internal clock control register
VPSS_REG_0000_VPSS_CLK_GATE	0x0018	W	0x00000000	Internal clock control register
VPSS_REG_0000_VPSS_RESET	0x001C	W	0x00000000	Internal reset control register
VPSS_REG_0000_VPSS_SLICE_CTRL	0x0020	W	0x00000000	VPSS global control
VPSS_REG_0000_VPSS_IRQ_CFG	0x0050	W	0x00000000	Crop in irq configure register
VPSS_REG_0000_VPSS_IMSC	0x0070	W	0x00000000	Interrupt mask
VPSS_REG_0000_VPSS_RIS	0x0074	W	0x00000000	Raw interrupt status
VPSS_REG_0000_VPSS_MIS	0x0078	W	0x00000000	Masked interrupt status
VPSS_REG_0000_VPSS_ICR	0x007C	W	0x00000000	Interrupt clear register, high clear
VPSS_REG_0000_VPSS_ISR	0x0080	W	0x00000000	Interrupt set register, high set
VPSS_REG_0000_VPSS_CTRL_SHD	0x0090	W	0x00000000	VPSS global control, shadow register
VPSS_REG_0000_VPSS_ONLINE_SHD	0x0094	W	0x00000000	ISP to VPSS online mode, shadow register
VPSS_REG_0000_VPSS_ONLINE2_SIZE_SHD	0x0098	W	0x00000000	ISP to VPSS online mode2 size, shadow register
VPSS_REG_0000_VPSS_WORKING	0x00A0	W	0x00000000	VPSS working status
VPSS_REG_0000_VPSS_PIPE_ACK0	0x00B0	W	0x00000000	VPSS pipe ack group0
VPSS_REG_0000_VPSS_PIPE_ACK1	0x00B4	W	0x00000000	VPSS pipe ack group1
VPSS_REG_0000_VPSS_LINE_CNT0	0x00C0	W	0x00000000	VPSS line counter0
VPSS_REG_0000_VPSS_LINE_CNT1	0x00C4	W	0x00000000	VPSS line counter1
VPSS_REG_0000_VPSS_FRAME_CNT	0x00C8	W	0x00000000	VPSS frame counter
VPSS_REG_0000_VPSS2ENC_DEBUG	0x00CC	W	0x00000000	VPSS to Encoder debug register

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Name	Offset	Size	Reset Value	Description
VPSS_REG_0000_VPSS_Y2R_COE00	0x00D0	W	0x000004A8	YUV to RGB csc coefficient00
VPSS_REG_0000_VPSS_Y2R_COE01	0x00D4	W	0x00000000	YUV to RGB csc coefficient01
VPSS_REG_0000_VPSS_Y2R_COE02	0x00D8	W	0x0000072C	YUV to RGB csc coefficient02
VPSS_REG_0000_VPSS_Y2R_OFF0	0x00DC	W	0x001C1F80	YUV to RGB csc coefficient offset0
VPSS_REG_0000_VPSS_Y2R_COE10	0x00E0	W	0x000004A8	YUV to RGB csc coefficient10
VPSS_REG_0000_VPSS_Y2R_COE11	0x00E4	W	0x00001F26	YUV to RGB csc coefficient11
VPSS_REG_0000_VPSS_Y2R_COE12	0x00E8	W	0x00001DDE	YUV to RGB csc coefficient12
VPSS_REG_0000_VPSS_Y2R_OFF1	0x00EC	W	0x00013380	YUV to RGB csc coefficient offset1
VPSS_REG_0000_VPSS_Y2R_COE20	0x00F0	W	0x000004A8	YUV to RGB csc coefficient20
VPSS_REG_0000_VPSS_Y2R_COE21	0x00F4	W	0x00000873	YUV to RGB csc coefficient21
VPSS_REG_0000_VPSS_Y2R_COE22	0x00F8	W	0x00000000	YUV to RGB csc coefficient22
VPSS_REG_0000_VPSS_Y2R_OFF2	0x00FC	W	0x001B7C00	YUV to RGB csc coefficient offset2

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.4.1.2 CMSC

Name	Offset	Size	Reset Value	Description
VPSS_CMSC_0500_CMSC_CTRL	0x0000	W	0x00000000	CMSC main control
VPSS_CMSC_0500_CMSC_UPDATE	0x0004	W	0x00000020	CMSC configuration update control
VPSS_CMSC_0500_CMSC_INTSCT_CORR	0x0008	W	0x00000000	CMSC intersections correction
VPSS_CMSC_0500_CMSC_CHN0_WIN	0x0010	W	0x00000000	CMSC channel0 window control
VPSS_CMSC_0500_CMSC_CHN1_WIN	0x0014	W	0x00000000	CMSC channel1 window control
VPSS_CMSC_0500_CMSC_CHN2_WIN	0x0018	W	0x00000000	CMSC channel2 window control
VPSS_CMSC_0500_CMSC_CHN3_WIN	0x001C	W	0x00000000	CMSC channel3 window control
VPSS_CMSC_0500_CMSC_CHN0_MODE	0x0020	W	0x00000000	CMSC channel0 mode
VPSS_CMSC_0500_CMSC_CHN1_MODE	0x0024	W	0x00000000	CMSC channel1 mode
VPSS_CMSC_0500_CMSC_CHN2_MODE	0x0028	W	0x00000000	CMSC channel2 mode
VPSS_CMSC_0500_CMSC_CHN3_MODE	0x002C	W	0x00000000	CMSC channel3 mode

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Name	Offset	Size	Reset Value	Description
VPSS_CMSC_0500_CMSC_WIN0_PARA	0x0030	W	0x0F000000	CMSC window0 parameter
VPSS_CMSC_0500_CMSC_WIN1_PARA	0x0034	W	0x0F000000	CMSC window1 parameter
VPSS_CMSC_0500_CMSC_WIN2_PARA	0x0038	W	0x0F000000	CMSC window2 parameter
VPSS_CMSC_0500_CMSC_WIN3_PARA	0x003C	W	0x0F000000	CMSC window3 parameter
VPSS_CMSC_0500_CMSC_WIN4_PARA	0x0040	W	0x0F000000	CMSC window4 parameter
VPSS_CMSC_0500_CMSC_WIN5_PARA	0x0044	W	0x0F000000	CMSC window5 parameter
VPSS_CMSC_0500_CMSC_WIN6_PARA	0x0048	W	0x0F000000	CMSC window6 parameter
VPSS_CMSC_0500_CMSC_WIN7_PARA	0x004C	W	0x0F000000	CMSC window7 parameter
VPSS_CMSC_0500_CMSC_WIN0_L0_VTX	0x0050	W	0x00000000	CMSC window0 line0 vertex
VPSS_CMSC_0500_CMSC_WIN0_L0_SLP	0x0054	W	0x00000000	CMSC window0 line0 slope
VPSS_CMSC_0500_CMSC_WIN0_L1_VTX	0x0058	W	0x00000000	CMSC window0 line1 vertex
VPSS_CMSC_0500_CMSC_WIN0_L1_SLP	0x005C	W	0x00000000	CMSC window0 line0 slope
VPSS_CMSC_0500_CMSC_WIN0_L2_VTX	0x0060	W	0x00000000	CMSC window0 line2 vertex
VPSS_CMSC_0500_CMSC_WIN0_L2_SLP	0x0064	W	0x00000000	CMSC window0 line2 slope
VPSS_CMSC_0500_CMSC_WIN0_L3_VTX	0x0068	W	0x00000000	CMSC window0 line3 vertex
VPSS_CMSC_0500_CMSC_WIN0_L3_SLP	0x006C	W	0x00000000	CMSC window0 line3 slope
VPSS_CMSC_0500_CMSC_WIN1_L0_VTX	0x0070	W	0x00000000	CMSC window1 line0 vertex
VPSS_CMSC_0500_CMSC_WIN1_L0_SLP	0x0074	W	0x00000000	CMSC window1 line0 slope
VPSS_CMSC_0500_CMSC_WIN1_L1_VTX	0x0078	W	0x00000000	CMSC window1 line1 vertex
VPSS_CMSC_0500_CMSC_WIN1_L1_SLP	0x007C	W	0x00000000	CMSC window1 line1 slope
VPSS_CMSC_0500_CMSC_WIN1_L2_VTX	0x0080	W	0x00000000	CMSC window1 line2 vertex
VPSS_CMSC_0500_CMSC_WIN1_L2_SLP	0x0084	W	0x00000000	CMSC window1 line2 slope
VPSS_CMSC_0500_CMSC_WIN1_L3_VTX	0x0088	W	0x00000000	CMSC window1 line3 vertex
VPSS_CMSC_0500_CMSC_WIN1_L3_SLP	0x008C	W	0x00000000	CMSC window1 line3 slope
VPSS_CMSC_0500_CMSC_WIN2_L0_VTX	0x0090	W	0x00000000	CMSC window2 line0 vertex
VPSS_CMSC_0500_CMSC_WIN2_L0_SLP	0x0094	W	0x00000000	CMSC window2 line0 slope
VPSS_CMSC_0500_CMSC_WIN2_L1_VTX	0x0098	W	0x00000000	CMSC window2 line1 vertex

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Name	Offset	Size	Reset Value	Description
VPSS_CMSC_0500_CMSC_WIN2_L1_SLP	0x009C	W	0x00000000	CMSC window2 line1 slope
VPSS_CMSC_0500_CMSC_WIN2_L2_VTX	0x00A0	W	0x00000000	CMSC window2 line2 vertex
VPSS_CMSC_0500_CMSC_WIN2_L2_SLP	0x00A4	W	0x00000000	CMSC window2 line2 slope
VPSS_CMSC_0500_CMSC_WIN2_L3_VTX	0x00A8	W	0x00000000	CMSC window2 line3 vertex
VPSS_CMSC_0500_CMSC_WIN2_L3_SLP	0x00AC	W	0x00000000	CMSC window2 line3 slope
VPSS_CMSC_0500_CMSC_WIN3_L0_VTX	0x00B0	W	0x00000000	CMSC window3 line0 vertex
VPSS_CMSC_0500_CMSC_WIN3_L0_SLP	0x00B4	W	0x00000000	CMSC window3 line0 slope
VPSS_CMSC_0500_CMSC_WIN3_L1_VTX	0x00B8	W	0x00000000	CMSC window3 line1 vertex
VPSS_CMSC_0500_CMSC_WIN3_L1_SLP	0x00BC	W	0x00000000	CMSC window3 line1 slope
VPSS_CMSC_0500_CMSC_WIN3_L2_VTX	0x00C0	W	0x00000000	CMSC window3 line2 vertex
VPSS_CMSC_0500_CMSC_WIN3_L2_SLP	0x00C4	W	0x00000000	CMSC window3 line2 slope
VPSS_CMSC_0500_CMSC_WIN3_L3_VTX	0x00C8	W	0x00000000	CMSC window3 line3 vertex
VPSS_CMSC_0500_CMSC_WIN3_L3_SLP	0x00CC	W	0x00000000	CMSC window3 line3 slope
VPSS_CMSC_0500_CMSC_WIN4_L0_VTX	0x00D0	W	0x00000000	CMSC window4 line0 vertex
VPSS_CMSC_0500_CMSC_WIN4_L0_SLP	0x00D4	W	0x00000000	CMSC window4 line0 slope
VPSS_CMSC_0500_CMSC_WIN4_L1_VTX	0x00D8	W	0x00000000	CMSC window4 line1 vertex
VPSS_CMSC_0500_CMSC_WIN4_L1_SLP	0x00DC	W	0x00000000	CMSC window4 line1 slope
VPSS_CMSC_0500_CMSC_WIN4_L2_VTX	0x00E0	W	0x00000000	CMSC window4 line2 vertex
VPSS_CMSC_0500_CMSC_WIN4_L2_SLP	0x00E4	W	0x00000000	CMSC window4 line2 slope
VPSS_CMSC_0500_CMSC_WIN4_L3_VTX	0x00E8	W	0x00000000	CMSC window4 line3 vertex
VPSS_CMSC_0500_CMSC_WIN4_L3_SLP	0x00EC	W	0x00000000	CMSC window4 line3 slope
VPSS_CMSC_0500_CMSC_WIN5_L0_VTX	0x00F0	W	0x00000000	CMSC window5 line0 vertex
VPSS_CMSC_0500_CMSC_WIN5_L0_SLP	0x00F4	W	0x00000000	CMSC window5 line0 slope
VPSS_CMSC_0500_CMSC_WIN5_L1_VTX	0x00F8	W	0x00000000	CMSC window5 line1 vertex
VPSS_CMSC_0500_CMSC_WIN5_L1_SLP	0x00FC	W	0x00000000	CMSC window5 line1 slope
VPSS_CMSC_0500_CMSC_WIN5_L2_VTX	0x0100	W	0x00000000	CMSC window5 line2 vertex
VPSS_CMSC_0500_CMSC_WIN5_L2_SLP	0x0104	W	0x00000000	CMSC window5 line2 slope

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Name	Offset	Size	Reset Value	Description
VPSS_CMSC_0500_CMSC_WIN5_L3_VTX	0x0108	W	0x00000000	CMSC window5 line3 vertex
VPSS_CMSC_0500_CMSC_WIN5_L3_SLP	0x010C	W	0x00000000	CMSC window5 line3 slope
VPSS_CMSC_0500_CMSC_WIN6_L0_VTX	0x0110	W	0x00000000	CMSC window6 line0 vertex
VPSS_CMSC_0500_CMSC_WIN6_L0_SLP	0x0114	W	0x00000000	CMSC window6 line0 slope
VPSS_CMSC_0500_CMSC_WIN6_L1_VTX	0x0118	W	0x00000000	CMSC window6 line1 vertex
VPSS_CMSC_0500_CMSC_WIN6_L1_SLP	0x011C	W	0x00000000	CMSC window6 line1 slope
VPSS_CMSC_0500_CMSC_WIN6_L2_VTX	0x0120	W	0x00000000	CMSC window6 line2 vertex
VPSS_CMSC_0500_CMSC_WIN6_L2_SLP	0x0124	W	0x00000000	CMSC window6 line2 slope
VPSS_CMSC_0500_CMSC_WIN6_L3_VTX	0x0128	W	0x00000000	CMSC window6 line3 vertex
VPSS_CMSC_0500_CMSC_WIN6_L3_SLP	0x012C	W	0x00000000	CMSC window6 line3 slope
VPSS_CMSC_0500_CMSC_WIN7_L0_VTX	0x0130	W	0x00000000	CMSC window7 line0 vertex
VPSS_CMSC_0500_CMSC_WIN7_L0_SLP	0x0134	W	0x00000000	CMSC window7 line0 slope
VPSS_CMSC_0500_CMSC_WIN7_L1_VTX	0x0138	W	0x00000000	CMSC window7 line1 vertex
VPSS_CMSC_0500_CMSC_WIN7_L1_SLP	0x013C	W	0x00000000	CMSC window7 line1 slope
VPSS_CMSC_0500_CMSC_WIN7_L2_VTX	0x0140	W	0x00000000	CMSC window7 line2 vertex
VPSS_CMSC_0500_CMSC_WIN7_L2_SLP	0x0144	W	0x00000000	CMSC window7 line2 slope
VPSS_CMSC_0500_CMSC_WIN7_L3_VTX	0x0148	W	0x00000000	CMSC window7 line3 vertex
VPSS_CMSC_0500_CMSC_WIN7_L3_SLP	0x014C	W	0x00000000	CMSC window7 line3 slope

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.4.1.3 Crop

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
VPSS	0x27C30700
ISP	0x27C30800

Name	Offset	Size	Reset Value	Description
QUAD_CROP_0700_0800_CROP_CTRL	0x0000	W	0x00000000	Global control register
QUAD_CROP_0700_0800_CROP_UPDATE	0x0004	W	0x00000020	Global control register

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Name	Offset	Size	Reset Value	Description
QUAD_CROP_0700_0800_CROP_0_H_OFFS	0x0010	W	0x00000000	Channel0 h offset
QUAD_CROP_0700_0800_CROP_0_V_OFFS	0x0014	W	0x00000000	Channel0 v offset
QUAD_CROP_0700_0800_CROP_0_H_SIZE	0x0018	W	0x00000000	Channel0 h size
QUAD_CROP_0700_0800_CROP_0_V_SIZE	0x001C	W	0x00000000	Channel0 v size
QUAD_CROP_0700_0800_CROP_1_H_OFFS	0x0020	W	0x00000000	Channel1 h offset
QUAD_CROP_0700_0800_CROP_1_V_OFFS	0x0024	W	0x00000000	Channel1 v offset
QUAD_CROP_0700_0800_CROP_1_H_SIZE	0x0028	W	0x00000000	Channel1 h size
QUAD_CROP_0700_0800_CROP_1_V_SIZE	0x002C	W	0x00000000	Channel1 v size
QUAD_CROP_0700_0800_CROP_2_H_OFFS	0x0030	W	0x00000000	Channel2 h offset
QUAD_CROP_0700_0800_CROP_2_V_OFFS	0x0034	W	0x00000000	Channel2 v offset
QUAD_CROP_0700_0800_CROP_2_H_SIZE	0x0038	W	0x00000000	Channel2 h size
QUAD_CROP_0700_0800_CROP_2_V_SIZE	0x003C	W	0x00000000	Channel2 v size
QUAD_CROP_0700_0800_CROP_3_H_OFFS	0x0040	W	0x00000000	Channel3 h offset
QUAD_CROP_0700_0800_CROP_3_V_OFFS	0x0044	W	0x00000000	Channel3 v offset
QUAD_CROP_0700_0800_CROP_3_H_SIZE	0x0048	W	0x00000000	Channel3 h size
QUAD_CROP_0700_0800_CROP_3_V_SIZE	0x004C	W	0x00000000	Channel3 v size
QUAD_CROP_0700_0800_CROP_CTRL_SHD	0x0060	W	0x00000000	Global control shadow register
QUAD_CROP_0700_0800_CROP_0_H_OFFS_SHD	0x0070	W	0x00000000	Channel0 h offset shadow signal
QUAD_CROP_0700_0800_CROP_0_V_OFFS_SHD	0x0074	W	0x00000000	Channel0 v offset shadow signal
QUAD_CROP_0700_0800_CROP_0_H_SIZE_SHD	0x0078	W	0x00000000	Channel0 h size shadow signal
QUAD_CROP_0700_0800_CROP_0_V_SIZE_SHD	0x007C	W	0x00000000	Channel0 v size shadow signal
QUAD_CROP_0700_0800_CROP_1_H_OFFS_SHD	0x0080	W	0x00000000	Channel1 h offset shadow signal
QUAD_CROP_0700_0800_CROP_1_V_OFFS_SHD	0x0084	W	0x00000000	Channel1 v offset shadow signal
QUAD_CROP_0700_0800_CROP_1_H_SIZE_SHD	0x0088	W	0x00000000	Channel1 h size shadow signal
QUAD_CROP_0700_0800_CROP_1_V_SIZE_SHD	0x008C	W	0x00000000	Channel1 v size shadow signal
QUAD_CROP_0700_0800_CROP_2_H_OFFS_SHD	0x0090	W	0x00000000	Channel2 h offset shadow signal
QUAD_CROP_0700_0800_CROP_2_V_OFFS_SHD	0x0094	W	0x00000000	Channel2 v offset shadow signal

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Name	Offset	Size	Reset Value	Description
QUAD_CROP_0700_0800_CROP_2_H_SIZE_SHD	0x0098	W	0x00000000	Channel2 h size shadow signal
QUAD_CROP_0700_0800_CROP_2_V_SIZE_SHD	0x009C	W	0x00000000	Channel2 v size shadow signal
QUAD_CROP_0700_0800_CROP_3_H_OFFS_SHD	0x00A0	W	0x00000000	Channel3 h offset shadow signal
QUAD_CROP_0700_0800_CROP_3_V_OFFS_SHD	0x00A4	W	0x00000000	Channel3 v offset shadow signal
QUAD_CROP_0700_0800_CROP_3_H_SIZE_SHD	0x00A8	W	0x00000000	Channel3 h size shadow signal
QUAD_CROP_0700_0800_CROP_3_V_SIZE_SHD	0x00AC	W	0x00000000	Channel3 v size shadow signal

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.4.1.4 ZME

Name	Offset	Size	Reset Value	Description
VPSS_ZME_1000_Y_HOR_COE0_10	0x0000	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE0_32	0x0004	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE0_54	0x0008	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE0_76	0x000C	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE1_10	0x0010	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE1_32	0x0014	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE1_54	0x0018	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE1_76	0x001C	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE2_10	0x0020	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE2_32	0x0024	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE2_54	0x0028	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE2_76	0x002C	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE3_10	0x0030	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE3_32	0x0034	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE3_54	0x0038	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE3_76	0x003C	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE4_10	0x0040	W	0x00000000	Component y horizontal filter coefficient

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Name	Offset	Size	Reset Value	Description
VPSS_ZME_1000_Y_HOR_COE4_32	0x0044	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE4_54	0x0048	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE4_76	0x004C	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE5_10	0x0050	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE5_32	0x0054	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE5_54	0x0058	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE5_76	0x005C	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE6_10	0x0060	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE6_32	0x0064	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE6_54	0x0068	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE6_76	0x006C	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE7_10	0x0070	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE7_32	0x0074	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE7_54	0x0078	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE7_76	0x007C	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE8_10	0x0080	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE8_32	0x0084	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE8_54	0x0088	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE8_76	0x008C	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE9_10	0x0090	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE9_32	0x0094	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE9_54	0x0098	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE9_76	0x009C	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE10_10	0x00A0	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE10_32	0x00A4	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE10_54	0x00A8	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE10_76	0x00AC	W	0x00000000	Component y horizontal filter coefficient

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Name	Offset	Size	Reset Value	Description
VPSS_ZME_1000_Y_HOR_COE11_10	0x00B0	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE11_32	0x00B4	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE11_54	0x00B8	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE11_76	0x00BC	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE12_10	0x00C0	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE12_32	0x00C4	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE12_54	0x00C8	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE12_76	0x00CC	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE13_10	0x00D0	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE13_32	0x00D4	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE13_54	0x00D8	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE13_76	0x00DC	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE14_10	0x00E0	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE14_32	0x00E4	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE14_54	0x00E8	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE14_76	0x00EC	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE15_10	0x00F0	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE15_32	0x00F4	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE15_54	0x00F8	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE15_76	0x00FC	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE16_10	0x0100	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE16_32	0x0104	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE16_54	0x0108	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_HOR_COE16_76	0x010C	W	0x00000000	Component y horizontal filter coefficient
VPSS_ZME_1000_Y_VER_COE0_10	0x0200	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE0_32	0x0204	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE0_54	0x0208	W	0x00000000	Component y vertical filter coefficient

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Name	Offset	Size	Reset Value	Description
VPSS_ZME_1000_Y_VER_COE0_76	0x020C	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE1_10	0x0210	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE1_32	0x0214	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE1_54	0x0218	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE1_76	0x021C	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE2_10	0x0220	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE2_32	0x0224	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE2_54	0x0228	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE2_76	0x022C	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE3_10	0x0230	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE3_32	0x0234	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE3_54	0x0238	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE3_76	0x023C	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE4_10	0x0240	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE4_32	0x0244	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE4_54	0x0248	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE4_76	0x024C	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE5_10	0x0250	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE5_32	0x0254	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE5_54	0x0258	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE5_76	0x025C	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE6_10	0x0260	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE6_32	0x0264	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE6_54	0x0268	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE6_76	0x026C	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE7_10	0x0270	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE7_32	0x0274	W	0x00000000	Component y vertical filter coefficient

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Name	Offset	Size	Reset Value	Description
VPSS_ZME_1000_Y_VER_COE7_54	0x0278	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE7_76	0x027C	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE8_10	0x0280	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE8_32	0x0284	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE8_54	0x0288	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE8_76	0x028C	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE9_10	0x0290	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE9_32	0x0294	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE9_54	0x0298	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE9_76	0x029C	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE10_10	0x02A0	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE10_32	0x02A4	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE10_54	0x02A8	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE10_76	0x02AC	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE11_10	0x02B0	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE11_32	0x02B4	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE11_54	0x02B8	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE11_76	0x02BC	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE12_10	0x02C0	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE12_32	0x02C4	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE12_54	0x02C8	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE12_76	0x02CC	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE13_10	0x02D0	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE13_32	0x02D4	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE13_54	0x02D8	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE13_76	0x02DC	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE14_10	0x02E0	W	0x00000000	Component y vertical filter coefficient

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Name	Offset	Size	Reset Value	Description
VPSS_ZME_1000_Y_VER_COE14_32	0x02E4	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE14_54	0x02E8	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE14_76	0x02EC	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE15_10	0x02F0	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE15_32	0x02F4	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE15_54	0x02F8	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE15_76	0x02FC	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE16_10	0x0300	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE16_32	0x0304	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE16_54	0x0308	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_Y_VER_COE16_76	0x030C	W	0x00000000	Component y vertical filter coefficient
VPSS_ZME_1000_UV_HOR_COE0_10	0x0400	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE0_32	0x0404	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE0_54	0x0408	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE0_76	0x040C	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE1_10	0x0410	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE1_32	0x0414	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE1_54	0x0418	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE1_76	0x041C	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE2_10	0x0420	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE2_32	0x0424	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE2_54	0x0428	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE2_76	0x042C	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE3_10	0x0430	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE3_32	0x0434	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE3_54	0x0438	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE3_76	0x043C	W	0x00000000	Component uv horizontal filter coefficient

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Name	Offset	Size	Reset Value	Description
VPSS_ZME_1000_UV_HOR_COE4_10	0x0440	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE4_32	0x0444	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE4_54	0x0448	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE4_76	0x044C	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE5_10	0x0450	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE5_32	0x0454	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE5_54	0x0458	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE5_76	0x045C	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE6_10	0x0460	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE6_32	0x0464	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE6_54	0x0468	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE6_76	0x046C	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE7_10	0x0470	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE7_32	0x0474	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE7_54	0x0478	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE7_76	0x047C	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE8_10	0x0480	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE8_32	0x0484	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE8_54	0x0488	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE8_76	0x048C	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE9_10	0x0490	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE9_32	0x0494	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE9_54	0x0498	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE9_76	0x049C	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE10_10	0x04A0	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE10_32	0x04A4	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE10_54	0x04A8	W	0x00000000	Component uv horizontal filter coefficient

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Name	Offset	Size	Reset Value	Description
VPSS_ZME_1000_UV_HOR_COE10_76	0x04AC	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE11_10	0x04B0	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE11_32	0x04B4	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE11_54	0x04B8	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE11_76	0x04BC	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE12_10	0x04C0	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE12_32	0x04C4	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE12_54	0x04C8	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE12_76	0x04CC	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE13_10	0x04D0	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE13_32	0x04D4	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE13_54	0x04D8	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE13_76	0x04DC	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE14_10	0x04E0	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE14_32	0x04E4	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE14_54	0x04E8	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE14_76	0x04EC	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE15_10	0x04F0	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE15_32	0x04F4	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE15_54	0x04F8	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE15_76	0x04FC	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE16_10	0x0500	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE16_32	0x0504	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE16_54	0x0508	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_HOR_COE16_76	0x050C	W	0x00000000	Component uv horizontal filter coefficient
VPSS_ZME_1000_UV_VER_COE0_10	0x0600	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE0_32	0x0604	W	0x00000000	Component uv vertical filter coefficient

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Name	Offset	Size	Reset Value	Description
VPSS_ZME_1000_UV_VER_COE0_54	0x0608	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE0_76	0x060C	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE1_10	0x0610	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE1_32	0x0614	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE1_54	0x0618	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE1_76	0x061C	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE2_10	0x0620	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE2_32	0x0624	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE2_54	0x0628	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE2_76	0x062C	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE3_10	0x0630	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE3_32	0x0634	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE3_54	0x0638	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE3_76	0x063C	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE4_10	0x0640	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE4_32	0x0644	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE4_54	0x0648	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE4_76	0x064C	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE5_10	0x0650	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE5_32	0x0654	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE5_54	0x0658	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE5_76	0x065C	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE6_10	0x0660	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE6_32	0x0664	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE6_54	0x0668	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE6_76	0x066C	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE7_10	0x0670	W	0x00000000	Component uv vertical filter coefficient

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Name	Offset	Size	Reset Value	Description
VPSS_ZME_1000_UV_VER_COE7_32	0x0674	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE7_54	0x0678	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE7_76	0x067C	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE8_10	0x0680	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE8_32	0x0684	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE8_54	0x0688	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE8_76	0x068C	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE9_10	0x0690	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE9_32	0x0694	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE9_54	0x0698	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE9_76	0x069C	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE10_10	0x06A0	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE10_32	0x06A4	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE10_54	0x06A8	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE10_76	0x06AC	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE11_10	0x06B0	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE11_32	0x06B4	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE11_54	0x06B8	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE11_76	0x06BC	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE12_10	0x06C0	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE12_32	0x06C4	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE12_54	0x06C8	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE12_76	0x06CC	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE13_10	0x06D0	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE13_32	0x06D4	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE13_54	0x06D8	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE13_76	0x06DC	W	0x00000000	Component uv vertical filter coefficient

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Name	Offset	Size	Reset Value	Description
VPSS_ZME_1000_UV_VER_COE14_10	0x06E0	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE14_32	0x06E4	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE14_54	0x06E8	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE14_76	0x06EC	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE15_10	0x06F0	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE15_32	0x06F4	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE15_54	0x06F8	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE15_76	0x06FC	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE16_10	0x0700	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE16_32	0x0704	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE16_54	0x0708	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_UV_VER_COE16_76	0x070C	W	0x00000000	Component uv vertical filter coefficient
VPSS_ZME_1000_ZME_CTRL	0x0800	W	0x00000001	Global control register
VPSS_ZME_1000_ZME_UPDATE	0x0804	W	0x00000020	Shadow update register
VPSS_ZME_1000_ZME_H_SIZE	0x0808	W	0x00000000	Scale out size, used for 8K
VPSS_ZME_1000_ZME_H_OFFS	0x080C	W	0x00000000	Use for 8K
VPSS_ZME_1000_Y_SCL_CTRL	0x0810	W	0x000000CC	Component y scale control
VPSS_ZME_1000_Y_SRC_SIZE	0x0814	W	0x00000000	Component y scale size of source (input)
VPSS_ZME_1000_Y_DST_SIZE	0x0818	W	0x00000000	Component y scale size of destination (output)
VPSS_ZME_1000_Y_DERING_PARA	0x081C	W	0x0D100410	Component y scale dering parameters
VPSS_ZME_1000_Y_XSCL_FACTOR	0x0820	W	0x00000000	Component y horizontal luminance scale factor register
VPSS_ZME_1000_Y_YSCL_FACTOR	0x0824	W	0x00000000	Component y vertical luminance scale factor register
VPSS_ZME_1000_UV_SCL_CTRL	0x0830	W	0x000000CC	Component uv scale control
VPSS_ZME_1000_UV_SRC_SIZE	0x0834	W	0x00000000	Component uv scale size of source (input)
VPSS_ZME_1000_UV_DST_SIZE	0x0838	W	0x00000000	Component uv scale size of destination (output)
VPSS_ZME_1000_UV_DERING_PARA	0x083C	W	0x0D100410	Component uv scale dering parameters
VPSS_ZME_1000_UV_XSCL_FACTOR	0x0840	W	0x00000000	Component uv horizontal luminance scale factor register

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Name	Offset	Size	Reset Value	Description
VPSS_ZME_1000_UV_YSCL_FACTOR	0x0844	W	0x00000000	Component uv vertical luminance scale factor register
VPSS_ZME_1000_SCL_CTRL_SHD	0x084C	W	0x00000000	Scale control shadow register
VPSS_ZME_1000_Y_SRC_SIZE_SHD	0x0850	W	0x00000000	Component y scale size of source (input), shadow register
VPSS_ZME_1000_Y_DST_SIZE_SHD	0x0854	W	0x00000000	Component y scale size of destination (output), shadow register
VPSS_ZME_1000_Y_XSCL_FACTOR_SHD	0x0858	W	0x00000000	Component y horizontal luminance scale factor register, shadow register
VPSS_ZME_1000_Y_YSCL_FACTOR_SHD	0x085C	W	0x00000000	Component y vertical luminance scale factor register, shadow register
VPSS_ZME_1000_UV_SRC_SIZE_SHD	0x0860	W	0x00000000	Component uv scale size of source (input), shadow register
VPSS_ZME_1000_UV_DST_SIZE_SHD	0x0864	W	0x00000000	Component uv scale size of destination (output), shadow register
VPSS_ZME_1000_UV_XSCL_FACTOR_SHD	0x0868	W	0x00000000	Component uv horizontal luminance scale factor register, shadow register
VPSS_ZME_1000_UV_YSCL_FACTOR_SHD	0x086C	W	0x00000000	Component uv vertical luminance scale factor register, shadow register
VPSS_ZME_1000_ZME_H_SIZE_SHD	0x0870	W	0x00000000	Scale out size, used for 8K, shadow registers
VPSS_ZME_1000_ZME_H_OFFS_SHD	0x0874	W	0x00000000	Use for 8K, shadow registers

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.4.1.5 Bilinear Scale

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
CHN1	0x27C31C00
CHN2	0x27C32800
CHN3	0x27C32C00

Name	Offset	Size	Reset Value	Description
VPSS_SCALE_1C00_2800_2C00_SCALE_CTRL	0x0000	W	0x00000000	Global control register
VPSS_SCALE_1C00_2800_2C00_SCALE_UPDATE	0x0004	W	0x00000020	Shadow update register
VPSS_SCALE_1C00_2800_2C00_SCALE_SRC_SIZE	0x0008	W	0x00000000	Scale size of source (input)
VPSS_SCALE_1C00_2800_2C00_SCALE_DST_SIZE	0x000C	W	0x00000000	Scale size of destination (output)

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Name	Offset	Size	Reset Value	Description
VPSS_SCALE_1C00_2800_2C00_SCALE_HY_FAC	0x0010	W	0x00000000	Horizontal luminance scale factor register
VPSS_SCALE_1C00_2800_2C00_SCALE_HC_FAC	0x0014	W	0x00000000	Horizontal chrominance scale factor register
VPSS_SCALE_1C00_2800_2C00_SCALE_VY_FAC	0x0018	W	0x00000000	Vertical luminance scale factor register
VPSS_SCALE_1C00_2800_2C00_SCALE_VC_FAC	0x001C	W	0x00000000	Vertical chrominance scale factor register
VPSS_SCALE_1C00_2800_2C00_SCALE_HY_OFFS	0x0020	W	0x00000000	Horizontal luminance scale coordinate offset register for bilinear
VPSS_SCALE_1C00_2800_2C00_SCALE_HC_OFFS	0x0024	W	0x00000000	Horizontal chrominance scale coordinate offset register for bilinear
VPSS_SCALE_1C00_2800_2C00_SCALE_VY_OFFS	0x0028	W	0x00000000	Vertical luminance scale coordinate offset register for bilinear
VPSS_SCALE_1C00_2800_2C00_SCALE_VC_OFFS	0x002C	W	0x00000000	Vertical chrominance scale coordinate offset register for bilinear
VPSS_SCALE_1C00_2800_2C00_SCALE_HY_SIZE	0x0040	W	0x00000000	Scale out Y size
VPSS_SCALE_1C00_2800_2C00_SCALE_HC_SIZE	0x0044	W	0x00000000	Scale out UV size for average
VPSS_SCALE_1C00_2800_2C00_SCALE_HY_OFFS_MI	0x0048	W	0x00000000	DDR data width is 128bit but Y data width is 8bit. This register configure the offset of first Y pixel in 128bit, which range from 0~15.
VPSS_SCALE_1C00_2800_2C00_SCALE_HC_OFFS_MI	0x004C	W	0x00000000	DDR data width is 128bit but UV data width is 8bit. This register configure the offset of first UV pixel in 128bit, which range from 0~15.
VPSS_SCALE_1C00_2800_2C00_SCALE_IN_CROP_OFFSET	0x0050	W	0x00000000	Scale in data cut first some pixels if needed.
VPSS_SCALE_1C00_2800_2C00_SCALE_CTRL_SHD	0x0080	W	0x00000000	Global control shadow register
VPSS_SCALE_1C00_2800_2C00_SCALE_SRC_SIZE_SHD	0x0088	W	0x00000000	Scale size of source (input), shadow register
VPSS_SCALE_1C00_2800_2C00_SCALE_DST_SIZE_SHD	0x008C	W	0x00000000	Scale size of destination (output), shadow register
VPSS_SCALE_1C00_2800_2C00_SCALE_HY_FAC_SHD	0x0090	W	0x00000000	Horizontal luminance scale factor shadow register
VPSS_SCALE_1C00_2800_2C00_SCALE_HC_FAC_SHD	0x0094	W	0x00000000	Horizontal chrominance scale factor shadow register
VPSS_SCALE_1C00_2800_2C00_SCALE_VY_FAC_SHD	0x0098	W	0x00000000	Vertical luminance scale factor shadow register

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Name	Offset	Size	Reset Value	Description
VPSS_SCALE_1C00_2800_2C00_SCALE_VC_FAC_SHD	0x009C	W	0x00000000	Vertical chrominance scale factor shadow register
VPSS_SCALE_1C00_2800_2C00_SCALE_HY_OFFS_SHD	0x00A0	W	0x00000000	Horizontal luminance scale coordinate offset shadow register for bilinear
VPSS_SCALE_1C00_2800_2C00_SCALE_HC_OFFS_SHD	0x00A4	W	0x00000000	Horizontal chrominance scale coordinate offset shadow register for bilinear
VPSS_SCALE_1C00_2800_2C00_SCALE_VY_OFFS_SHD	0x00A8	W	0x00000000	Vertical luminance scale coordinate offset shadow register for bilinear
VPSS_SCALE_1C00_2800_2C00_SCALE_VC_OFFS_SHD	0x00AC	W	0x00000000	Vertical chrominance scale coordinate offset shadow register for bilinear
VPSS_SCALE_1C00_2800_2C00_SCALE_HY_SIZE_SHD	0x00C0	W	0x00000000	Scale out Y size shadow signal
VPSS_SCALE_1C00_2800_2C00_SCALE_HC_SIZE_SHD	0x00C4	W	0x00000000	Scale out UV size shadow signal
VPSS_SCALE_1C00_2800_2C00_SCALE_HY_OFFS_MI_SHD	0x00C8	W	0x00000000	Shadow signal of sw_scl_hy_offs_mi
VPSS_SCALE_1C00_2800_2C00_SCALE_HC_OFFS_MI_SHD	0x00CC	W	0x00000000	Shadow signal of sw_scl_hc_offs_mi
VPSS_SCALE_1C00_2800_2C00_SCALE_IN_CROP_OFFSET_SHD	0x00D0	W	0x00000000	Scale in data cut first some pixels if needed, shadow register.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.4.1.6 Aspective Ratio

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
CHN0	0x27C31900
CHN1	0x27C32500
CHN2	0x27C32900
CHN3	0x27C32D00

Name	Offset	Size	Reset Value	Description
ASPT_RATIO_1900_2500_2900_2D00_RATIO_CTRL	0x0000	W	0x00000000	Global control register
ASPT_RATIO_1900_2500_2900_2D00_RATIO_UPDATE	0x0004	W	0x00000020	Shadow update register
ASPT_RATIO_1900_2500_2900_2D00_RATIO_ACT_SIZE	0x0010	W	0x00000000	Actual image size (input)

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Name	Offset	Size	Reset Value	Description
ASPT_RATIO_1900_2500_2900_2D00_RATIO_VIR_SIZE	0x0014	W	0x00000000	Virtual image size (output)
ASPT_RATIO_1900_2500_2900_2D00_RATIO_OFFS	0x0018	W	0x00000000	Actual image offset
ASPT_RATIO_1900_2500_2900_2D00_RATIO_COLOR	0x001C	W	0x80800000	Background color for image filling.
ASPT_RATIO_1900_2500_2900_2D00_RATIO_ACT_SIZE_SHD	0x0030	W	0x00000000	Actual image size (input), shadow register
ASPT_RATIO_1900_2500_2900_2D00_RATIO_VIR_SIZE_SHD	0x0034	W	0x00000000	Virtual image size (output), shadow register
ASPT_RATIO_1900_2500_2900_2D00_RATIO_OFFS_SHD	0x0038	W	0x00000000	Actual image offset, shadow register
ASPT_RATIO_1900_2500_2900_2D00_RATIO_COLOR_SHD	0x003C	W	0x00000000	Background color for image filling, shadow register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.4.1.7 MI

Name	Offset	Size	Reset Value	Description
VPSS_MI_3000_MI_WR_CTRL	0x0000	W	0x00A20010	Global write control register
VPSS_MI_3000_MI_WR_INIT	0x0004	W	0x00000000	Control register for address initialization and skip function
VPSS_MI_3000_MI_WR_WRAP_CTRL	0x0010	W	0x0000000F	MI write wrap control
VPSS_MI_3000_MI_WR_VFLIP_CTRL	0x0014	W	0x00000000	MI write wrap control
VPSS_MI_3000_MI_HURRY_CTRL	0x0040	W	0x00000000	VPSS interconnect hurry control
VPSS_MI_3000_MI_ARQOS_CTRL	0x0044	W	0x00000030	AXI read qos to interconnect control
VPSS_MI_3000_MI_AWQOS_CTRL	0x0048	W	0x00000000	AXI write qos to interconnect control
VPSS_MI_3000_MI_IMSC	0x0050	W	0x00000000	Interrupt mask
VPSS_MI_3000_MI_RIS	0x0054	W	0x00000000	Raw interrupt status
VPSS_MI_3000_MI_MIS	0x0058	W	0x00000000	Masked interrupt status
VPSS_MI_3000_MI_ICR	0x005C	W	0x00000000	Interrupt clear register, high clear
VPSS_MI_3000_MI_ISR	0x0060	W	0x00000000	Interrupt set register, high set
VPSS_MI_3000_MI_STATUS	0x0070	W	0x00000000	MI Status Register
VPSS_MI_3000_MI_STATUS_CLR	0x0074	W	0x00000000	MI Status Clear Register
VPSS_MI_3000_MI_RD_CTRL	0x0100	W	0x00200002	DMA read control register
VPSS_MI_3000_MI_RD_INIT	0x0104	W	0x00000000	DMA start register

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Name	Offset	Size	Reset Value	Description
VPSS_MI_3000_MI_RD_START	0x0108	W	0x00000000	DMA start register
VPSS_MI_3000_MI_RD_Y_BASE	0x0110	W	0x00000000	Y component image start address
VPSS_MI_3000_MI_RD_Y_WIDTH	0x0114	W	0x00000000	Y component image width
VPSS_MI_3000_MI_RD_Y_HEIGHT	0x0118	W	0x00000000	Y component image height
VPSS_MI_3000_MI_RD_Y_STRIDE	0x011C	W	0x00000000	Y component original line stride
VPSS_MI_3000_MI_RD_C_BASE	0x0120	W	0x00000000	UV component image start address
VPSS_MI_3000_MI_RD_Y_BASE_SHD	0x0130	W	0x00000000	Y component image start address, shadow register
VPSS_MI_3000_MI_RD_C_BASE_SHD	0x0134	W	0x00000000	UV component image start address, shadow register
VPSS_MI_3000_MI_RD_Y_WIDTH_SHD	0x0138	W	0x00000000	Y component image width, shadow register
VPSS_MI_3000_MI_RD_Y_HEIGHT_SHD	0x013C	W	0x00000000	Y component image height, shadow register
VPSS_MI_3000_AXI_CFG_RD_CTRL	0x0160	W	0x80000010	AXI configure read control for module registers, except MMU.
VPSS_MI_3000_AXI_CFG_RD_BASE	0x0164	W	0x00000000	Base address for axi configure read
VPSS_MI_3000_AXI_CFG_RD_H_WSIZE	0x0168	W	0x00000000	AXI configure read word size of horizontal direction
VPSS_MI_3000_AXI_CFG_RD_V_SIZE	0x016C	W	0x00000001	AXI configure read word size of horizontal direction
VPSS_MI_3000_MI_RD_R2Y_COE00	0x0180	W	0x00000001	Read RGB to YUV csc coefficient00
VPSS_MI_3000_MI_RD_R2Y_COE01	0x0184	W	0x00000001	Read RGB to YUV csc coefficient01
VPSS_MI_3000_MI_RD_R2Y_COE02	0x0188	W	0x00000001	Read RGB to YUV csc coefficient02
VPSS_MI_3000_MI_RD_R2Y_OFF0	0x018C	W	0x00000001	Read RGB to YUV csc coefficient00
VPSS_MI_3000_MI_RD_R2Y_COE10	0x0190	W	0x00000001	Read RGB to YUV csc coefficient10
VPSS_MI_3000_MI_RD_R2Y_COE11	0x0194	W	0x00000001	Read RGB to YUV csc coefficient11
VPSS_MI_3000_MI_RD_R2Y_COE12	0x0198	W	0x00000001	Read RGB to YUV csc coefficient12
VPSS_MI_3000_MI_RD_R2Y_OFF1	0x019C	W	0x00000001	Read RGB to YUV csc coefficient offset1
VPSS_MI_3000_MI_RD_R2Y_COE20	0x01A0	W	0x00000001	Read RGB to YUV csc coefficient20
VPSS_MI_3000_MI_RD_R2Y_COE21	0x01A4	W	0x00000001	Read RGB to YUV csc coefficient21
VPSS_MI_3000_MI_RD_R2Y_COE22	0x01A8	W	0x00000001	Read RGB to YUV csc coefficient22
VPSS_MI_3000_MI_RD_R2Y_OFF2	0x01AC	W	0x00000001	Read RGB to YUV csc coefficient offset2
VPSS_MI_3000_MI_CHN0_WR_CTRL	0x0200	W	0x00000212	Chn0 write control register

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Name	Offset	Size	Reset Value	Description
VPSS_MI_3000_MI_CHN0_WR_Y_BASE	0x0210	W	0x00000000	Base address for chn0 picture Y component
VPSS_MI_3000_MI_CHN0_WR_Y_SIZE	0x0214	W	0x00000000	Size of chn0 picture Y component
VPSS_MI_3000_MI_CHN0_WR_Y_OFFS_CNT	0x0218	W	0x00000000	Offset counter initial value for chn0 picture Y
VPSS_MI_3000_MI_CHN0_WR_Y_OFFS_CNT_START	0x021C	W	0x00000000	Offset counter start value for chn0 picture Y
VPSS_MI_3000_MI_CHN0_WR_CB_BASE	0x0220	W	0x00000000	Base address for chn0 picture uv component ring buffer
VPSS_MI_3000_MI_CHN0_WR_CB_SIZE	0x0224	W	0x00000000	Size of chn0 picture uv component ring buffer
VPSS_MI_3000_MI_CHN0_WR_CB_OFFS_CNT	0x0228	W	0x00000000	Offset counter initial value for chn0 picture uv component ring buffer
VPSS_MI_3000_MI_CHN0_WR_CB_OFFS_CNT_START	0x022C	W	0x00000000	Offset counter start value for chn0 picture uv component ring buffer
VPSS_MI_3000_MI_CHN0_WR_Y_STRIDE	0x0230	W	0x00000000	Line stride of chn0 picture Y component
VPSS_MI_3000_MI_CHN0_WR_Y_PIC_WIDTH	0x0234	W	0x00000000	Y component image width for chn0 picture
VPSS_MI_3000_MI_CHN0_WR_Y_PIC_SIZE	0x023C	W	0x00000000	Y component image size
VPSS_MI_3000_MI_CHN0_WR_CTRL_SHD	0x0250	W	0x00000210	Chn0 write control shadow register
VPSS_MI_3000_MI_CHN0_WR_Y_BASE_SHD	0x0260	W	0x00000000	Base address shadow register for chn0 picture Y component
VPSS_MI_3000_MI_CHN0_WR_Y_SIZE_SHD	0x0264	W	0x00000000	Size shadow register of chn0 picture Y component
VPSS_MI_3000_MI_CHN0_WR_Y_OFFS_CNT_SHD	0x0268	W	0x00000000	Current offset counter of chn0 picture Y component
VPSS_MI_3000_MI_CHN0_WR_CB_BASE_SHD	0x0270	W	0x00000000	Base address shadow register for chn0 picture uv component ring buffer
VPSS_MI_3000_MI_CHN0_WR_CB_SIZE_SHD	0x0274	W	0x00000000	Size shadow register of chn0 picture uv component ring buffer
VPSS_MI_3000_MI_CHN0_WR_CB_OFFS_CNT_SHD	0x0278	W	0x00000000	Current offset counter of chn0 picture uv component ring buffer
VPSS_MI_3000_MI_CHN0_WR_Y_END_ADDR	0x0280	W	0x00000000	Channel0 y frame end address
VPSS_MI_3000_MI_CHN0_WR_CB_END_ADDR	0x0284	W	0x00000000	Channel0 uv frame end address
VPSS_MI_3000_MI_CHN0_WR_LINE_CNT	0x0288	W	0x00000000	MI channel0 write line counter
VPSS_MI_3000_MI_CHN1_WR_CTRL	0x0300	W	0x10000212	Chn1 write control register
VPSS_MI_3000_MI_CHN1_WR_Y_BASE	0x0310	W	0x00000000	Base address for chn1 picture Y component
VPSS_MI_3000_MI_CHN1_WR_Y_SIZE	0x0314	W	0x00000000	Size of chn1 picture Y component
VPSS_MI_3000_MI_CHN1_WR_Y_OFFS_CNT	0x0318	W	0x00000000	Offset counter initial value for chn1 picture Y

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Name	Offset	Size	Reset Value	Description
VPSS_MI_3000_MI_CHN1_WR_Y_OFFS_CNT_START	0x031C	W	0x00000000	Offset counter start value for chn1 picture Y
VPSS_MI_3000_MI_CHN1_WR_CB_BASE	0x0320	W	0x00000000	Base address for chn1 picture uv component ring buffer
VPSS_MI_3000_MI_CHN1_WR_CB_SIZE	0x0324	W	0x00000000	Size of chn1 picture uv component ring buffer
VPSS_MI_3000_MI_CHN1_WR_CB_OFFS_CNT	0x0328	W	0x00000000	Offset counter initial value for chn1 picture uv component ring buffer
VPSS_MI_3000_MI_CHN1_WR_CB_OFFS_CNT_START	0x032C	W	0x00000000	Offset counter start value for chn1 picture uv component ring buffer
VPSS_MI_3000_MI_CHN1_WR_Y_STRIDE	0x0330	W	0x00000000	Line stride of chn1 picture Y component
VPSS_MI_3000_MI_CHN1_WR_Y_PIC_WIDTH	0x0334	W	0x00000000	Y component image width for chn1 picture
VPSS_MI_3000_MI_CHN1_WR_Y_PIC_SIZE	0x033C	W	0x00000000	Y component image size
VPSS_MI_3000_MI_CHN1_WR_CTRL_SHD	0x0350	W	0x00000210	Chn1 write control shadow register
VPSS_MI_3000_MI_CHN1_WR_Y_BASE_SHD	0x0360	W	0x00000000	Base address shadow register for chn1 picture Y component
VPSS_MI_3000_MI_CHN1_WR_Y_SIZE_SHD	0x0364	W	0x00000000	Size shadow register of chn1 picture Y component
VPSS_MI_3000_MI_CHN1_WR_Y_OFFS_CNT_SHD	0x0368	W	0x00000000	Current offset counter of chn1 picture Y component
VPSS_MI_3000_MI_CHN1_WR_CB_BASE_SHD	0x0370	W	0x00000000	Base address shadow register for chn1 picture uv component ring buffer
VPSS_MI_3000_MI_CHN1_WR_CB_SIZE_SHD	0x0374	W	0x00000000	Size shadow register of chn1 picture uv component ring buffer
VPSS_MI_3000_MI_CHN1_WR_CB_OFFS_CNT_SHD	0x0378	W	0x00000000	Current offset counter of chn1 picture uv component ring buffer
VPSS_MI_3000_MI_CHN1_WR_Y_END_ADDR	0x0380	W	0x00000000	Channel1 y frame end address
VPSS_MI_3000_MI_CHN1_WR_CB_END_ADDR	0x0384	W	0x00000000	Channel1 uv frame end address
VPSS_MI_3000_MI_CHN1_WR_LINE_CNT	0x0388	W	0x00000000	MI channel1 write line counter
VPSS_MI_3000_MI_CHN1_WR_Y2R_COE00	0x03A0	W	0x000004A8	Channel1 YUV to RGB csc coefficient00
VPSS_MI_3000_MI_CHN1_WR_Y2R_COE01	0x03A4	W	0x00000000	Channel1 YUV to RGB csc coefficient01
VPSS_MI_3000_MI_CHN1_WR_Y2R_COE02	0x03A8	W	0x0000072C	Channel1 YUV to RGB csc coefficient02
VPSS_MI_3000_MI_CHN1_WR_Y2R_OFF0	0x03AC	W	0x001C1F80	Channel1 YUV to RGB csc coefficient offset0
VPSS_MI_3000_MI_CHN1_WR_Y2R_COE10	0x03B0	W	0x000004A8	Channel1 YUV to RGB csc coefficient10
VPSS_MI_3000_MI_CHN1_WR_Y2R_COE11	0x03B4	W	0x00001F26	Channel1 YUV to RGB csc coefficient11
VPSS_MI_3000_MI_CHN1_WR_Y2R_COE12	0x03B8	W	0x00001DDE	Channel1 YUV to RGB csc coefficient12

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Name	Offset	Size	Reset Value	Description
VPSS_MI_3000_MI_CHN1_WR_Y2R_OFF1	0x03BC	W	0x00013380	Channel1 YUV to RGB csc coefficient offset1
VPSS_MI_3000_MI_CHN1_WR_Y2R_COE20	0x03C0	W	0x000004A8	Channel1 YUV to RGB csc coefficient20
VPSS_MI_3000_MI_CHN1_WR_Y2R_COE21	0x03C4	W	0x00000873	Channel1 YUV to RGB csc coefficient21
VPSS_MI_3000_MI_CHN1_WR_Y2R_COE32	0x03C8	W	0x00000000	Channel1 YUV to RGB csc coefficient22
VPSS_MI_3000_MI_CHN1_WR_Y2R_OFF2	0x03CC	W	0x001B7C00	Channel1 YUV to RGB csc coefficient offset2
VPSS_MI_3000_MI_CHN2_WR_CTRL	0x0400	W	0x00000212	Chn2 write control register
VPSS_MI_3000_MI_CHN2_WR_Y_BASE	0x0410	W	0x00000000	Base address for chn2 picture Y component
VPSS_MI_3000_MI_CHN2_WR_Y_SIZE	0x0414	W	0x00000000	Size of chn2 picture Y component
VPSS_MI_3000_MI_CHN2_WR_Y_OFFS_CNT	0x0418	W	0x00000000	Offset counter initial value for chn2 picture Y
VPSS_MI_3000_MI_CHN2_WR_Y_OFFS_CNT_START	0x041C	W	0x00000000	Offset counter start value for chn2 picture Y
VPSS_MI_3000_MI_CHN2_WR_CB_BASE	0x0420	W	0x00000000	Base address for chn2 picture uv component ring buffer
VPSS_MI_3000_MI_CHN2_WR_CB_SIZE	0x0424	W	0x00000000	Size of chn2 picture uv component ring buffer
VPSS_MI_3000_MI_CHN2_WR_CB_OFFS_CNT	0x0428	W	0x00000000	Offset counter initial value for chn2 picture uv component ring buffer
VPSS_MI_3000_MI_CHN2_WR_CB_OFFS_CNT_START	0x042C	W	0x00000000	Offset counter start value for chn2 picture uv component ring buffer
VPSS_MI_3000_MI_CHN2_WR_Y_STRIDE	0x0430	W	0x00000000	Line stride of chn2 picture Y component
VPSS_MI_3000_MI_CHN2_WR_Y_PIC_WIDTH	0x0434	W	0x00000000	Y component image width for chn2 picture
VPSS_MI_3000_MI_CHN2_WR_Y_PIC_SIZE	0x043C	W	0x00000000	Y component image size
VPSS_MI_3000_MI_CHN2_WR_CTRL_SHD	0x0450	W	0x00000210	Chn2 write control shadow register
VPSS_MI_3000_MI_CHN2_WR_Y_BASE_SHD	0x0460	W	0x00000000	Base address shadow register for chn2 picture Y component
VPSS_MI_3000_MI_CHN2_WR_Y_SIZE_SHD	0x0464	W	0x00000000	Size shadow register of chn2 picture Y component
VPSS_MI_3000_MI_CHN2_WR_Y_OFFS_CNT_SHD	0x0468	W	0x00000000	Current offset counter of chn2 picture Y component
VPSS_MI_3000_MI_CHN2_WR_CB_BASE_SHD	0x0470	W	0x00000000	Base address shadow register for chn2 picture uv component ring buffer
VPSS_MI_3000_MI_CHN2_WR_CB_SIZE_SHD	0x0474	W	0x00000000	Size shadow register of chn2 picture uv component ring buffer
VPSS_MI_3000_MI_CHN2_WR_CB_OFFS_CNT_SHD	0x0478	W	0x00000000	Current offset counter of chn2 picture uv component ring buffer
VPSS_MI_3000_MI_CHN2_WR_Y_END_ADDR	0x0480	W	0x00000000	Channel2 y frame end address

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Name	Offset	Size	Reset Value	Description
VPSS_MI_3000_MI_CHN2_WR_CB_END_ADDR	0x0484	W	0x00000000	Channel2 uv frame end address
VPSS_MI_3000_MI_CHN2_WR_LINE_CNT	0x0488	W	0x00000000	MI channel2 write line counter
VPSS_MI_3000_MI_CHN3_WR_CTRL	0x0500	W	0x00000212	Chn3 write control register
VPSS_MI_3000_MI_CHN3_WR_Y_BASE	0x0510	W	0x00000000	Base address for chn3 picture Y component
VPSS_MI_3000_MI_CHN3_WR_Y_SIZE	0x0514	W	0x00000000	Size of chn3 picture Y component
VPSS_MI_3000_MI_CHN3_WR_Y_OFFS_CNT	0x0518	W	0x00000000	Offset counter initial value for chn3 picture Y
VPSS_MI_3000_MI_CHN3_WR_Y_OFFS_CNT_START	0x051C	W	0x00000000	Offset counter start value for chn3 picture Y
VPSS_MI_3000_MI_CHN3_WR_CB_BASE	0x0520	W	0x00000000	Base address for chn3 picture uv component ring buffer
VPSS_MI_3000_MI_CHN3_WR_CB_SIZE	0x0524	W	0x00000000	Size of chn3 picture uv component ring buffer
VPSS_MI_3000_MI_CHN3_WR_CB_OFFS_CNT	0x0528	W	0x00000000	Offset counter initial value for chn3 picture uv component ring buffer
VPSS_MI_3000_MI_CHN3_WR_CB_OFFS_CNT_START	0x052C	W	0x00000000	Offset counter start value for chn3 picture uv component ring buffer
VPSS_MI_3000_MI_CHN3_WR_Y_STRIDE	0x0530	W	0x00000000	Line stride of chn3 picture Y component
VPSS_MI_3000_MI_CHN3_WR_Y_PIC_WIDTH	0x0534	W	0x00000000	Y component image width for chn3 picture
VPSS_MI_3000_MI_CHN3_WR_Y_PIC_SIZE	0x053C	W	0x00000000	Y component image size
VPSS_MI_3000_MI_CHN3_WR_CTRL_SHD	0x0550	W	0x00000210	Chn3 write control shadow register
VPSS_MI_3000_MI_CHN3_WR_Y_BASE_SHD	0x0560	W	0x00000000	Base address shadow register for chn3 picture Y component
VPSS_MI_3000_MI_CHN3_WR_Y_SIZE_SHD	0x0564	W	0x00000000	Size shadow register of chn3 picture Y component
VPSS_MI_3000_MI_CHN3_WR_Y_OFFS_CNT_SHD	0x0568	W	0x00000000	Current offset counter of chn3 picture Y component
VPSS_MI_3000_MI_CHN3_WR_CB_BASE_SHD	0x0570	W	0x00000000	Base address shadow register for chn3 picture uv component ring buffer
VPSS_MI_3000_MI_CHN3_WR_CB_SIZE_SHD	0x0574	W	0x00000000	Size shadow register of chn3 picture uv component ring buffer
VPSS_MI_3000_MI_CHN3_WR_CB_OFFS_CNT_SHD	0x0578	W	0x00000000	Current offset counter of chn3 picture uv component ring buffer
VPSS_MI_3000_MI_CHN3_WR_Y_END_ADDR	0x0580	W	0x00000000	Channel3 y frame end address
VPSS_MI_3000_MI_CHN3_WR_CB_END_ADDR	0x0584	W	0x00000000	Channel3 uv frame end address
VPSS_MI_3000_MI_CHN3_WR_LINE_CNT	0x0588	W	0x00000000	MI channel3 write line counter

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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3.4.1.8 MMU

Name	Offset	Size	Reset Value	Description
MMU_3F00_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address
MMU_3F00_STATUS	0x0004	W	0x00000000	MMU status register
MMU_3F00_COMMAND	0x0008	W	0x00000000	MMU command register
MMU_3F00_PAGE_FAULT_ADDR	0x000C	W	0x00000000	MMU logical address of last page fault
MMU_3F00_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
MMU_3F00_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
MMU_3F00_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
MMU_3F00_INT_MASK	0x001C	W	0x00000000	MMU raw interrupt status register
MMU_3F00_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register
MMU_3F00_AUTO_GATING	0x0024	W	0x00000000	mmu auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.4.2 Detail Registers Description

3.4.2.1 VPSS_REG

VPSS_REG_0000_VPSS_CTRL

Address: Operational Base(0x27C30000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_vpss_all_clk_dis VPSS all clock disable
30	RW	0x0	sw_vpss_chn_judge_dis VPSS channel enable judge disable for MI all frame end generation, backdoor
29	RW	0x0	sw_ack_frm_pro_dis Vblank optimize disable
28	RW	0x0	sw_noc_idle_dis VPSS NOC idle disable for cru not clock gating
27:26	RO	0x0	reserved
25	RW	0x0	sw_sub_frm_st_en Sub-module frame start enable, backdoor
24	RW	0x0	sw_vpss_frm_end_mode VPSS frame end use mode 1'b0: use mi all frame end 1'b1: use crop input frame end
23:11	RO	0x0000	reserved
10	RW	0x0	sw_vpss2enc_cnt_sel VPSS to Encoder line counter selection. 1'b0: Line counter from channel0 scale out 1'b1: Line counter from channel1 scale out
9	RW	0x0	sw_vpss2enc_pipe_en Pipeline enable from VPSS to Encoder 1'b0: VPSS can not be holded by Encoder 1'b1: VPSS can be holded by Encoder
8	RW	0x0	sw_vi2enc_sel Online interface selection for encoder 1'b0: From ISP 1'b1: From VPSS

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Bit	Attr	Reset Value	Description
7:5	RO	0x0	reserved
4	RW	0x0	sw_mir_en Mirror enable 1'b0: disable 1'b1: enable
3:0	RO	0x0	reserved

VPSS_REG_0000_VPSS_ONLINE

Address: Operational Base(0x27C30000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	sw_isp2vpss_cmsc_en ISP to VPSS mirror and cover mosaic enable for online mode2 1'b0: disable 2'b1: enable
17:16	RW	0x0	sw_isp2vpss_online_mode ISP to VPSS online mode 2'b00: only VPSS offline(DMA) mode 2'b01: only ISP to VPSS online mode 2'b10: VPSS offline and ISP reuse VPSS channels online mode 2'b11: reserved
15:8	RO	0x00	reserved
7:6	RW	0x0	sw_isp2vpss_chn3_sel ISP to VPSS channel select 2'b00: channel3 disable 2'b01: VPSS channel3 enable 2'b10: ISP channel3 enable for online mode2 2'b11: reserved
5:4	RW	0x0	sw_isp2vpss_chn2_sel ISP to VPSS channel select 2'b00: channel2 disable 2'b01: VPSS channel2 enable 2'b10: ISP channel2 enable for online mode2 2'b11: reserved
3:2	RW	0x0	sw_isp2vpss_chn1_sel ISP to VPSS channel select 2'b00: channel1 disable 2'b01: VPSS channel1 enable 2'b10: ISP channel1 enable for online mode2 2'b11: reserved
1:0	RW	0x0	sw_isp2vpss_chn0_sel ISP to VPSS channel select 2'b00: channel0 disable 2'b01: VPSS channel0 enable 2'b10: ISP channel0 enable for online mode2 2'b11: reserved

VPSS_REG_0000_VPSS_ONLINE2_SIZE

Address: Operational Base(0x27C30000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_isp2vpss_mir_height Mirror height, only online mode2 used
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_isp2vpss_mir_width Mirror width, only online mode2 used

VPSS_REG_0000_VPSS_VERSION

Address: Operational Base(0x27C30000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:28	RO	0x3	ro_vpss_version_major Major version
27:24	RO	0x1	ro_vpss_version_minor Minor version
23:0	RO	0x002106	ro_vpss_version_date Year, Month, Day

VPSS_REG_0000_VPSS_UPDATE

Address: Operational Base(0x27C30000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	W1C	0x0	sys_isp_chn_force_upd ISP channel enable shadow register force update for online mode2 1'b0: Nothing happens 1'b1: Update shadow registers Note: sys_isp_chn_force_upd is not valid during any chn working period.
8	W1C	0x0	sys_vpss_chn_force_upd VPSS channel enable shadow register force update 1'b0: Nothing happens 1'b1: Update shadow registers Note: sys_vpss_chn0_force_upd is not valid during any chn working period.
7:6	RO	0x0	reserved
5	RW	0x1	sys_mir_gen_upd Mirror automatic register update 1'b1: Automatic register update at frame end enabled 1'b0: Automatic register update at frame end disabled
4	W1C	0x0	sys_mir_force_upd Mirror shadow registers force update 1'b0: Nothing happens 1'b1: Update shadow registers
3:2	RO	0x0	reserved
1	RW	0x1	sys_cfg_gen_upd VPSS main control automatic register update 1'b1: Automatic register update at frame end enabled 1'b0: Automatic register update at frame end disabled
0	W1C	0x0	sys_cfg_force_upd VPSS main control shadow registers force update 1'b0: Nothing happens 1'b1: Update shadow registers

VPSS_REG_0000_VPSS_CLK_EN

Address: Operational Base(0x27C30000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x1	sw_vpss_mi_clk_en Memory interface clock enable 1'b1: Processing mode 1'b0: Power safe
15:12	RO	0x0	reserved
11	RW	0x1	sw_vpss_ratio3_clk_en Ratio3 processing clock enable 1'b1: Processing mode 1'b0: Power safe
10	RW	0x1	sw_vpss_ratio2_clk_en Ratio2 processing clock enable 1'b1: Processing mode 1'b0: Power safe
9	RW	0x1	sw_vpss_ratio1_clk_en Ratio1 processing clock enable 1'b1: Processing mode 1'b0: Power safe
8	RW	0x1	sw_vpss_ratio0_clk_en Ratio0 processing clock enable 1'b1: Processing mode 1'b0: Power safe
7	RW	0x1	sw_vpss_scl3_clk_en Scale3 processing clock enable 1'b1: Processing mode 1'b0: Power safe
6	RW	0x1	sw_vpss_scl2_clk_en Scale2 processing clock enable 1'b1: Processing mode 1'b0: Power safe
5	RW	0x1	sw_vpss_scl1_clk_en Scale1 processing clock enable 1'b1: Processing mode 1'b0: Power safe
4	RW	0x1	sw_vpss_scl0_clk_en Scale0 processing clock enable 1'b1: Processing mode 1'b0: Power safe
3	RW	0x1	sw_vpss_cr1_clk_en ISP quad-crop processing clock enable 1'b1: Processing mode 1'b0: Power safe
2	RW	0x1	sw_vpss_cr_clk_en VPSS quad-crop processing clock enable 1'b1: Processing mode 1'b0: Power safe
1	RW	0x1	sw_vpss_cmsc_clk_en Cover and mosaic processing clock enable 1'b1: Processing mode 1'b0: Power safe
0	RW	0x1	sw_vpss_mir_clk_en Mirror processing clock enable 1'b1: Processing mode 1'b0: Power safe

VPSS_REG_0000_VPSS_CLK_GATE

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Address: Operational Base(0x27C30000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	sw_mi_rd_ckg_dis MI read clock control 1'b1: Clock always on 1'b0: Clock auto-gate
23:20	RO	0x0	reserved
19	RW	0x0	sw_mi_chn3_ckg_dis MI channel3 clock control 1'b1: Clock always on 1'b0: Clock auto-gate
18	RW	0x0	sw_mi_chn2_ckg_dis MI channel2 clock control 1'b1: Clock always on 1'b0: Clock auto-gate
17	RW	0x0	sw_mi_chn1_ckg_dis MI channel1 clock control 1'b1: Clock always on 1'b0: Clock auto-gate
16	RW	0x0	sw_mi_chn0_ckg_dis MI channel0 clock control 1'b1: Clock always on 1'b0: Clock auto-gate
15:12	RO	0x0	reserved
11	RW	0x0	sw_vpss_ratio3_ckg_dis Ratio3 module clock control 1'b1: Clock always on 1'b0: Clock auto-gate
10	RW	0x0	sw_vpss_ratio2_ckg_dis Ratio2 module clock control 1'b1: Clock always on 1'b0: Clock auto-gate
9	RW	0x0	sw_vpss_ratio1_ckg_dis Ratio1 module clock control 1'b1: Clock always on 1'b0: Clock auto-gate
8	RW	0x0	sw_vpss_ratio0_ckg_dis Ratio0 module clock control 1'b1: Clock always on 1'b0: Clock auto-gate
7	RW	0x0	sw_vpss_scl3_ckg_dis Scale0 module clock control 1'b1: Clock always on 1'b0: Clock auto-gate
6	RW	0x0	sw_vpss_scl2_ckg_dis Scale2 module clock control 1'b1: Clock always on 1'b0: Clock auto-gate
5	RW	0x0	sw_vpss_scl1_ckg_dis Scale1 module clock control 1'b1: Clock always on 1'b0: Clock auto-gate

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Bit	Attr	Reset Value	Description
4	RW	0x0	sw_vpss_scl0_ckg_dis Scale0 module clock control 1'b1: Clock always on 1'b0: Clock auto-gate
3:2	RO	0x0	reserved
1	RW	0x0	sw_vpss_cmsc_ckg_dis Cover and mosaic module clock control 1'b1: Clock always on 1'b0: Clock auto-gate
0	RW	0x0	sw_vpss_mir_ckg_dis Mirror module clock control 1'b1: Clock always on 1'b0: Clock auto-gate

VPSS_REG_0000_VPSS_RESET

Address: Operational Base(0x27C30000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_safety_done_clr Safety reset vpss done status clear. Note: This register readback is safety reset vpss done status.
30	RW	0x0	sw_rst_protect_dis Safety protect reset disable
29:1	RO	0x00000000	reserved
0	W1C	0x0	sys_glb_soft_rst Hardware reset of entire vpss, global reset when high valid 1'b0: Processing mode 1'b1: Reset state

VPSS_REG_0000_VPSS_SLICE_CTRL

Address: Operational Base(0x27C30000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	sw_vpss_slice_en VPSS slice enable
0	RW	0x0	sys_vpss_slice_st VPSS slice start. It is used to continue VPSS when vpss_slice_done is pulled up. Slice line number in VPSS_IRQ_CFG.

VPSS_REG_0000_VPSS_IRQ_CFG

Address: Operational Base(0x27C30000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_crop_in_irq_line Quad-crop in irq line configuration for interrupt of image height. Note: VPSS slice reused.

VPSS_REG_0000_VPSS_IMSC

Address: Operational Base(0x27C30000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	ratio3_in_frm_end_p Mask ratio3 end of frame interrupt
14	RW	0x0	ratio2_in_frm_end_p Mask ratio2 end of frame interrupt

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Bit	Attr	Reset Value	Description
13	RW	0x0	ratio1_in_frm_end_p Mask ratio1 end of frame interrupt
12	RW	0x0	ratio0_in_frm_end_p Mask ratio0 end of frame interrupt
11	RW	0x0	scl3_in_frm_end_p Mask scl3 end of frame interrupt
10	RW	0x0	scl2_in_frm_end_p Mask scl2 end of frame interrupt
9	RW	0x0	scl1_in_frm_end_p Mask scl1 end of frame interrupt
8	RW	0x0	scl0_in_frm_end_p Mask scl0 end of frame interrupt
7	RW	0x0	isp_all_frame_end_p Mask ISP all end of frame interrupt for online mode2 Note: If ISP all channels closed, that is ISP quad-crop input end of frame.
6	RW	0x0	crop1_in_cfg_irq Mask isp quad-crop in irq line configuration interrupt for online mode2
5	RW	0x0	crop1_in_frm_end_p Mask ISP quad-crop input end of frame interrupt for online mode2
4	RW	0x0	mir_frm_end_p Mask mirror end of frame interrupt
3	RW	0x0	vpss_all_frame_end_p Mask VPSS all end of frame interrupt Note: If VPSS all channels closed, that is VPSS quad-crop input end of frame.
2	RW	0x0	crop_in_cfg_irq Mask VPSS quad-crop in irq line configuration interrupt
1	RW	0x0	crop_in_frm_end_p Mask VPSS quad-crop input end of frame interrupt
0	RW	0x0	crop_in_frm_st Mask VPSS quad-crop input frame start interrupt

VPSS_REG_0000_VPSS_RIS

Address: Operational Base(0x27C30000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	ratio3_in_frm_end_p Raw status of ratio3 end of frame interrupt
14	RO	0x0	ratio2_in_frm_end_p Raw status of ratio2 end of frame interrupt
13	RO	0x0	ratio1_in_frm_end_p Raw status of ratio1 end of frame interrupt
12	RO	0x0	ratio0_in_frm_end_p Raw status of ratio0 end of frame interrupt
11	RO	0x0	scl3_in_frm_end_p Raw status of scl3 end of frame interrupt
10	RO	0x0	scl2_in_frm_end_p Raw status of scl2 end of frame interrupt
9	RO	0x0	scl1_in_frm_end_p Raw status of scl1 end of frame interrupt
8	RO	0x0	scl0_in_frm_end_p Raw status of scl0 end of frame interrupt

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Bit	Attr	Reset Value	Description
7	RO	0x0	isp_all_frame_end_p Raw status of ISP all end of frame interrupt for online mode2 Note: If ISP all channels closed, that is ISP quad-crop input end of frame.
6	RO	0x0	crop1_in_cfg_irq Raw status of ISP quad-crop in irq line configuration interrupt for online mode2
5	RO	0x0	crop1_in_frm_end_p Raw status of ISP quad-crop input end of frame interrupt for online mode2
4	RO	0x0	mir_frm_end_p Raw status of mirror end of frame interrupt
3	RO	0x0	vpss_all_frame_end_p Raw status of VPSS all end of frame interrupt Note: If VPSS all channels closed, that is VPSS quad-crop input end of frame.
2	RO	0x0	crop_in_cfg_irq Raw status of VPSS quad-crop in irq line configuration interrupt
1	RO	0x0	crop_in_frm_end_p Raw status of VPSS quad-crop input end of frame interrupt
0	RO	0x0	crop_in_frm_st Raw status of VPSS quad-crop input frame start interrupt

VPSS_REG_0000_VPSS_MIS

Address: Operational Base(0x27C30000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	ratio3_in_frm_end_p Masked status of ratio3 end of frame interrupt
14	RO	0x0	ratio2_in_frm_end_p Masked status of ratio2 end of frame interrupt
13	RO	0x0	ratio1_in_frm_end_p Masked status of ratio1 end of frame interrupt
12	RO	0x0	ratio0_in_frm_end_p Masked status of ratio0 end of frame interrupt
11	RO	0x0	scl3_in_frm_end_p Masked status of scl3 end of frame interrupt
10	RO	0x0	scl2_in_frm_end_p Masked status of scl2 end of frame interrupt
9	RO	0x0	scl1_in_frm_end_p Masked status of scl1 end of frame interrupt
8	RO	0x0	scl0_in_frm_end_p Masked status of scl0 end of frame interrupt
7	RO	0x0	isp_all_frame_end_p Masked status of ISP all end of frame interrupt for online mode2 Note: If ISP all channels closed, that is ISP quad-crop input end of frame.
6	RO	0x0	crop1_in_cfg_irq Masked status of ISP quad-crop in irq line configuration interrupt for online mode2
5	RO	0x0	crop1_in_frm_end_p Masked status of ISP quad-crop input end of frame interrupt for online mode2
4	RO	0x0	mir_frm_end_p Masked status of mirror end of frame interrupt

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Bit	Attr	Reset Value	Description
3	RO	0x0	vpss_all_frame_end_p Masked status of VPSS all end of frame interrupt Note: If VPSS all channels closed, that is VPSS quad-crop input end of frame.
2	RO	0x0	crop_in_cfg_irq Masked status of VPSS quad-crop in irq line configuration interrupt
1	RO	0x0	crop_in_frm_end_p Masked status of VPSS quad-crop input end of frame interrupt
0	RO	0x0	crop_in_frm_st Masked status of VPSS quad-crop input frame start interrupt

VPSS_REG_0000_VPSS_ICR

Address: Operational Base(0x27C30000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	W1C	0x0	ratio3_in_frm_end_p Clear ratio3 end of frame interrupt
14	W1C	0x0	ratio2_in_frm_end_p Clear ratio2 end of frame interrupt
13	W1C	0x0	ratio1_in_frm_end_p Clear ratio1 end of frame interrupt
12	W1C	0x0	ratio0_in_frm_end_p Clear ratio0 end of frame interrupt
11	W1C	0x0	scl3_in_frm_end_p Clear scl3 end of frame interrupt
10	W1C	0x0	scl2_in_frm_end_p Clear scl2 end of frame interrupt
9	W1C	0x0	scl1_in_frm_end_p Clear scl1 end of frame interrupt
8	W1C	0x0	scl0_in_frm_end_p Clear scl0 end of frame interrupt
7	W1C	0x0	isp_all_frame_end_p Clear ISP all end of frame interrupt for online mode2 Note: If ISP all channels closed, that is ISP quad-crop input end of frame.
6	W1C	0x0	crop1_in_cfg_irq Clear ISP quad-crop in irq line configuration interrupt for online mode2
5	W1C	0x0	crop1_in_frm_end_p Clear ISP quad-crop input end of frame interrupt for online mode2
4	W1C	0x0	mir_frm_end_p Clear mirror end of frame interrupt
3	W1C	0x0	vpss_all_frame_end_p Clear VPSS all end of frame interrupt Note: If VPSS all channels closed, that is VPSS quad-crop input end of frame.
2	W1C	0x0	crop_in_cfg_irq Clear VPSS quad-crop in irq line configuration interrupt
1	W1C	0x0	crop_in_frm_end_p Clear VPSS quad-crop input end of frame interrupt
0	W1C	0x0	crop_in_frm_st Clear VPSS quad-crop input frame start interrupt

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VPSS_REG_0000_VPSS_ISR

Address: Operational Base(0x27C30000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	W1C	0x0	ratio3_in_frm_end_p Set ratio3 end of frame interrupt
14	W1C	0x0	ratio2_in_frm_end_p Set ratio2 end of frame interrupt
13	W1C	0x0	ratio1_in_frm_end_p Set ratio1 end of frame interrupt
12	W1C	0x0	ratio0_in_frm_end_p Set ratio0 end of frame interrupt
11	W1C	0x0	scl3_in_frm_end_p Set scl3 end of frame interrupt
10	W1C	0x0	scl2_in_frm_end_p Set scl2 end of frame interrupt
9	W1C	0x0	scl1_in_frm_end_p Set scl1 end of frame interrupt
8	W1C	0x0	scl0_in_frm_end_p Set scl0 end of frame interrupt
7	W1C	0x0	isp_all_frame_end_p Set ISP all end of frame interrupt for online mode2 Note: If ISP all channels closed, that is ISP quad-crop input end of frame.
6	W1C	0x0	crop1_in_cfg_irq Set ISP quad-crop in irq line configuration interrupt for online mode2
5	W1C	0x0	crop1_in_frm_end_p Set ISP quad-crop input end of frame interrupt for online mode2
4	W1C	0x0	mir_frm_end_p Set mirror end of frame interrupt
3	W1C	0x0	vpss_all_frame_end_p Set VPSS all end of frame interrupt Note: If VPSS all channels closed, that is VPSS quad-crop input end of frame.
2	W1C	0x0	crop_in_cfg_irq Set VPSS quad-crop in irq line configuration interrupt
1	W1C	0x0	crop_in_frm_end_p Set VPSS quad-crop input end of frame interrupt
0	W1C	0x0	crop_in_frm_st Set VPSS quad-crop input frame start interrupt

VPSS_REG_0000_VPSS_CTRL_SHD

Address: Operational Base(0x27C30000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	sw_mir_en_shd Mirror enable 1'b0: disable 1'b1: enable
3:0	RO	0x0	reserved

VPSS_REG_0000_VPSS_ONLINE_SHD

Address: Operational Base(0x27C30000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
18	RO	0x0	sw_isp2vpss_cmsc_en_shd ISP to VPSS mirror and cover mosaic enable for online mode2, shadow register 1'b0: disable 2'b1: enable
17	RO	0x0	sw_isp2vpss_online2_en_shd ISP to VPSS online mode2 enable, shadow register
16	RO	0x0	sw_isp2vpss_online1_en_shd ISP to VPSS online mode1 enable, shadow register
15:8	RO	0x00	reserved
7	RO	0x0	sw_isp_chn3_en_shd ISP channel3 enable for online mode2, shadow register
6	RO	0x0	sw_vpss_chn3_en_shd VPSS channel0 enable, shadow register
5	RO	0x0	sw_isp_chn2_en_shd ISP channel2 enable for online mode2, shadow register
4	RO	0x0	sw_vpss_chn2_en_shd VPSS channel2 enable, shadow register
3	RO	0x0	sw_isp_chn1_en_shd ISP channel1 enable for online mode2, shadow register
2	RO	0x0	sw_vpss_chn1_en_shd VPSS channel1 enable, shadow register
1	RO	0x0	sw_isp_chn0_en_shd ISP channel0 enable for online mode2, shadow register
0	RO	0x0	sw_vpss_chn0_en_shd VPSS channel0 enable, shadow register

VPSS_REG_0000_VPSS_ONLINE2_SIZE_SHD

Address: Operational Base(0x27C30000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_isp2vpss_mir_height_shd Mirror height, only online mode2 used
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_isp2vpss_mir_width_shd Mirror width, only online mode2 used

VPSS_REG_0000_VPSS_WORKING

Address: Operational Base(0x27C30000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31	RO	0x0	vpss_offline_working VPSS offline mode working
30	RO	0x0	isp2vpss_working ISP to VPSS working
29	RO	0x0	vpss_working VPSS working, all online mode available
28	RO	0x0	isp_working ISP working, online mode2 available
27:12	RO	0x0000	reserved
11	RO	0x0	ratio3_working Ratio3 working
10	RO	0x0	ratio2_working Ratio2 working
9	RO	0x0	ratio1_working Ratio1 working

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Bit	Attr	Reset Value	Description
8	RO	0x0	ratio0_working Ratio0 working
7	RO	0x0	scl3_working Scale3 working
6	RO	0x0	scl2_working Scale2 working
5	RO	0x0	scl1_working Scale1 working
4	RO	0x0	scl0_working Scale0 working
3:2	RO	0x0	reserved
1	RO	0x0	cmsc_working Cover mosaic working
0	RO	0x0	mir_working Mirror working

VPSS_REG_0000_VPSS_PIPE_ACK0

Address: Operational Base(0x27C30000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_vpss_pipe_ack0 [4'b0, quad2chn3_c_val, quad2chn3_c_ack, quad2chn3_y_val, quad2chn3_y_ack, quad2chn2_c_val, quad2chn2_c_ack, quad2chn2_y_val, quad2chn2_y_ack, quad2chn1_c_val, quad2chn1_c_ack, quad2chn1_y_val, quad2chn1_y_ack, quad2chn0_c_val, quad2chn0_c_ack, quad2chn0_y_val, quad2chn0_y_ack, cmsc_val , cmsc_ack , mir_val , mir_ack , 2'b0 , isp2chn_ack , isp2chn_val , isp2vpss_val , isp2vpss_ack , vpss_in_val , vpss_in_ack];

VPSS_REG_0000_VPSS_PIPE_ACK1

Address: Operational Base(0x27C30000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_vpss_pipe_ack1 [chn32mi_c_val, chn32mi_c_ack, chn32mi_y_val, chn32mi_y_ack, chn22mi_c_val, chn22mi_c_ack, chn22mi_y_val, chn22mi_y_ack, chn12mi_c_val, chn12mi_c_ack, chn12mi_y_val, chn12mi_y_ack, chn02mi_c_val, chn02mi_c_ack, chn02mi_y_val, chn02mi_y_ack, ratio3_c_val, ratio3_c_ack, ratio3_y_val, ratio3_y_ack, ratio2_c_val, ratio2_c_ack, ratio2_y_val, ratio2_y_ack, ratio1_c_val, ratio1_c_ack, ratio1_y_val, ratio1_y_ack, ratio0_c_val, ratio0_c_ack, ratio0_y_val, ratio0_y_ack];

VPSS_REG_0000_VPSS_LINE_CNT0

Address: Operational Base(0x27C30000) + offset (0x00C0)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_chn0_in_line_cnt MI channel0 input line counter
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_crop_in_line_cnt VPSS quad-crop input line counter

VPSS_REG_0000_VPSS_LINE_CNT1

Address: Operational Base(0x27C30000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	ro_crop1_in_line_cnt ISP quad-crop input line counter

VPSS_REG_0000_VPSS_FRAME_CNT

Address: Operational Base(0x27C30000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	ro_isp_frame_cnt ISP frame counter of online mode2, debug register
15:10	RO	0x00	reserved
9:0	RO	0x000	ro_vpss_frame_cnt VPSS frame counter, debug register

VPSS_REG_0000_VPSS2ENC_DEBUG

Address: Operational Base(0x27C30000) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31	RW	0x0	vpss2enc_hold VPSS to Encoder hold flag
30:24	RO	0x00	reserved
23:16	RO	0x00	ro_vpss2enc_frm_cnt VPSS to Encoder frame counter
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_vpss2enc_line_cnt VPSS to Encoder line counter

VPSS_REG_0000_VPSS_Y2R_COE00

Address: Operational Base(0x27C30000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_vpss_y2r_en Global YUV to RGB csc enable
30	RW	0x0	sw_vpss_y2r_rb_swap Enable rb swap of RGB format
29:13	RO	0x00000	reserved
12:0	RW	0x04a8	sw_vpss_y2r_coe_00 1bit signed+2bit integer+10bit float factor R: sw_vpss_y2r_coe_00*Y + sw_vpss_coe_01*U + sw_vpss_coe_02*V + sw_vpss_y2r_coe_off0 Note: initial value is bt709-limit

VPSS_REG_0000_VPSS_Y2R_COE01

Address: Operational Base(0x27C30000) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	sw_vpss_y2r_coe_01 1bit signed+2bit integer+10bit float factor R: sw_vpss_y2r_coe_00*Y + sw_vpss_coe_01*U + sw_vpss_coe_02*V + sw_vpss_y2r_coe_off0 Note: initial value is bt709-limit

VPSS_REG_0000_VPSS_Y2R_COE02

Address: Operational Base(0x27C30000) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x072c	sw_vpss_y2r_coe_02 1bit signed+2bit integer+10bit float factor R: sw_vpss_y2r_coe_00*Y + sw_vpss_coe_01*U + sw_vpss_coe_02*V + sw_vpss_y2r_coe_off0 Note: initial value is bt709-limit

VPSS_REG_0000_VPSS_Y2R_OFF0

Address: Operational Base(0x27C30000) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x1c1f80	sw_vpss_y2r_coe_off0 1bit signed+10bit integer+10bit float factor R: sw_vpss_y2r_coe_00*Y + sw_vpss_coe_01*U + sw_vpss_coe_02*V + sw_vpss_y2r_coe_off0 Note: initial value is bt709-limit

VPSS_REG_0000_VPSS_Y2R_COE10

Address: Operational Base(0x27C30000) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x04a8	sw_vpss_y2r_coe_10 1bit signed+2bit integer+10bit float factor G: sw_vpss_y2r_coe_10*Y + sw_vpss_coe_11*U + sw_vpss_coe_12*V + sw_vpss_y2r_coe_off1 Note: initial value is bt709-limit

VPSS_REG_0000_VPSS_Y2R_COE11

Address: Operational Base(0x27C30000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x1f26	sw_vpss_y2r_coe_11 1bit signed+2bit integer+10bit float factor G: sw_vpss_y2r_coe_10*Y + sw_vpss_coe_11*U + sw_vpss_coe_12*V + sw_vpss_y2r_coe_off1 Note: initial value is bt709-limit

VPSS_REG_0000_VPSS_Y2R_COE12

Address: Operational Base(0x27C30000) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x1dde	sw_vpss_y2r_coe_12 1bit signed+2bit integer+10bit float factor G: sw_vpss_y2r_coe_10*Y + sw_vpss_coe_11*U + sw_vpss_coe_12*V + sw_vpss_y2r_coe_off1 Note: initial value is bt709-limit

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VPSS_REG_0000_VPSS_Y2R_OFF1

Address: Operational Base(0x27C30000) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x013380	sw_vpss_y2r_coe_off1 1bit signed+10bit integer+10bit float factor G: sw_vpss_y2r_coe_10*Y + sw_vpss_coe_11*U + sw_vpss_coe_12*V + sw_vpss_y2r_coe_off1 Note: initial value is bt709-limit

VPSS_REG_0000_VPSS_Y2R_COE20

Address: Operational Base(0x27C30000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x04a8	sw_vpss_y2r_coe_20 1bit signed+2bit integer+10bit float factor B: sw_vpss_y2r_coe_20*Y + sw_vpss_coe_21*U + sw_vpss_coe_22*V + sw_vpss_y2r_coe_off2 Note: initial value is bt709-limit

VPSS_REG_0000_VPSS_Y2R_COE21

Address: Operational Base(0x27C30000) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0873	sw_vpss_y2r_coe_21 1bit signed+2bit integer+10bit float factor B: sw_vpss_y2r_coe_20*Y + sw_vpss_coe_21*U + sw_vpss_coe_22*V + sw_vpss_y2r_coe_off2 Note: initial value is bt709-limit

VPSS_REG_0000_VPSS_Y2R_COE22

Address: Operational Base(0x27C30000) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_vpss_y2r_coe_22 1bit signed+2bit integer+10bit float factor B: sw_vpss_y2r_coe_20*Y + sw_vpss_coe_21*U + sw_vpss_coe_22*V + sw_vpss_y2r_coe_off2 Note: initial value is bt709-limit

VPSS_REG_0000_VPSS_Y2R_OFF2

Address: Operational Base(0x27C30000) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x1b7c00	sw_vpss_y2r_coe_off2 1bit signed+10bit integer+10bit float factor B: sw_vpss_y2r_coe_20*Y + sw_vpss_coe_21*U + sw_vpss_coe_22*V + sw_vpss_y2r_coe_off2 Note: initial value is bt709-limit

3.4.2.2 CMSC

VPSS_CMSC_0500_CMSC_CTRL

Address: Operational Base(0x27C30500) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	cmsc_working CMSC working signal 1'b0: CMSC no working 1'b1: CMSC working
30:26	RO	0x00	reserved
25:24	RO	0x0	sw_cmsc_blk_size_shd CMSC block size of mosaic mode, shadowed
23	RO	0x0	sw_cmsc_chn3_en_shd CMSC channel3 enable, shadowed
22	RO	0x0	sw_cmsc_chn2_en_shd CMSC channel2 enable, shadowed
21	RO	0x0	sw_cmsc_chn1_en_shd CMSC channel1 enable, shadowed
20	RO	0x0	sw_cmsc_chn0_en_shd CMSC channel0 enable, shadowed
19:17	RO	0x0	reserved
16	RO	0x0	sw_cmsc_en_shd CMSC enable, shadowed
15:10	RO	0x00	reserved
9:8	RW	0x0	sw_cmsc_blk_size CMSC block size of mosaic mode 2'd0: 8x8 2'd1: 16x16 2'd2: 32x32 3'd3: 64x64
7	RW	0x0	sw_cmsc_chn3_en CMSC channel3 enable 1'b0: Disabled 1'b1: Enabled
6	RW	0x0	sw_cmsc_chn2_en CMSC channel2 enable 1'b0: Disabled 1'b1: Enabled
5	RW	0x0	sw_cmsc_chn1_en CMSC channel1 enable 1'b0: Disabled 1'b1: Enabled
4	RW	0x0	sw_cmsc_chn0_en CMSC channel0 enable 1'b0: Disabled 1'b1: Enabled
3:1	RO	0x0	reserved
0	RW	0x0	sw_cmsc_en CMSC enable 1'b0: Disabled 1'b1: Enabled

VPSS_CMSC_0500_CMSC_UPDATE

Address: Operational Base(0x27C30500) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x1	sys_cfg_gen_upd CMSC configuration update at frame end
4	W1C	0x0	sys_itself_force_upd CMSC configuration update immediately, auto clear.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	reserved

VPSS_CMSC_0500_CMSC_INTSCT_CORR

Address: Operational Base(0x27C30500) + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_cmsc_win7_intsct_pty_corr_dis CMSC window7 intersection parity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
30	RW	0x0	sw_cmsc_win6_intsct_pty_corr_dis CMSC window6 intersection parity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
29	RW	0x0	sw_cmsc_win5_intsct_pty_corr_dis CMSC window5 intersection parity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
28	RW	0x0	sw_cmsc_win4_intsct_pty_corr_dis CMSC window4 intersection parity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
27	RW	0x0	sw_cmsc_win3_intsct_pty_corr_dis CMSC window3 intersection parity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
26	RW	0x0	sw_cmsc_win2_intsct_pty_corr_dis CMSC window2 intersection parity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
25	RW	0x0	sw_cmsc_win1_intsct_pty_corr_dis CMSC window1 intersection parity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
24	RW	0x0	sw_cmsc_win0_intsct_pty_corr_dis CMSC window0 intersection parity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
23	RW	0x0	sw_cmsc_win7_intsct_conti_corr_dis CMSC window7 intersection continuity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
22	RW	0x0	sw_cmsc_win6_intsct_conti_corr_dis CMSC window6 intersection continuity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable

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Bit	Attr	Reset Value	Description
21	RW	0x0	sw_cmsc_win5_intsct_conti_corr_dis CMSC window5 intersection continuity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
20	RW	0x0	sw_cmsc_win4_intsct_conti_corr_dis CMSC window4 intersection continuity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
19	RW	0x0	sw_cmsc_win3_intsct_conti_corr_dis CMSC window3 intersection continuity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
18	RW	0x0	sw_cmsc_win2_intsct_conti_corr_dis CMSC window2 intersection continuity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
17	RW	0x0	sw_cmsc_win1_intsct_conti_corr_dis CMSC window1 intersection continuity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
16	RW	0x0	sw_cmsc_win0_intsct_conti_corr_dis CMSC window0 intersection continuity correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
15	RW	0x0	sw_cmsc_win7_intsct_exist_corr_dis CMSC window7 intersection existence correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
14	RW	0x0	sw_cmsc_win6_intsct_exist_corr_dis CMSC window6 intersection existence correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
13	RW	0x0	sw_cmsc_win5_intsct_exist_corr_dis CMSC window5 intersection existence correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
12	RW	0x0	sw_cmsc_win4_intsct_exist_corr_dis CMSC window4 intersection existence correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
11	RW	0x0	sw_cmsc_win3_intsct_exist_corr_dis CMSC window3 intersection existence correction disable, read back is shadow 1'b0: Enable 1'b1: Disable

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Bit	Attr	Reset Value	Description
10	RW	0x0	sw_cmsc_win2_intsct_exist_corr_dis CMSC window2 intersection existence correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
9	RW	0x0	sw_cmsc_win1_intsct_exist_corr_dis CMSC window1 intersection existence correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
8	RW	0x0	sw_cmsc_win0_intsct_exist_corr_dis CMSC window0 intersection existence correction disable, read back is shadow 1'b0: Enable 1'b1: Disable
7	RW	0x0	sw_cmsc_win7_intsct_exist_corr CMSC window7 intersection existence correction 1'b0: min = max 1'b1: max = min
6	RW	0x0	sw_cmsc_win6_intsct_exist_corr CMSC window6 intersection existence correction 1'b0: min = max 1'b1: max = min
5	RW	0x0	sw_cmsc_win5_intsct_exist_corr CMSC window5 intersection existence correction 1'b0: min = max 1'b1: max = min
4	RW	0x0	sw_cmsc_win4_intsct_exist_corr CMSC window4 intersection existence correction 1'b0: min = max 1'b1: max = min
3	RW	0x0	sw_cmsc_win3_intsct_exist_corr CMSC window3 intersection existence correction 1'b0: min = max 1'b1: max = min
2	RW	0x0	sw_cmsc_win2_intsct_exist_corr CMSC window2 intersection existence correction 1'b0: min = max 1'b1: max = min
1	RW	0x0	sw_cmsc_win1_intsct_exist_corr CMSC window1 intersection existence correction 1'b0: min = max 1'b1: max = min
0	RW	0x0	sw_cmsc_win0_intsct_exist_corr CMSC window0 intersection existence correction 1'b0: min = max 1'b1: max = min

VPSS_CMSC_0500_CMSC_CHN0_WIN

Address: Operational Base(0x27C30500) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	sw_cmsc_chn0_win_en_shd CMSC channel0 window0~window7 enable, shadowed
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	sw_cmsc_chn0_win_en CMSC channel0 window0~window7 enable 1'b0: Disabled 1'b1: Enabled

VPSS_CMSC_0500_CMSC_CHN1_WIN

Address: Operational Base(0x27C30500) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	sw_cmsc_chn0_win_en_shd CMSC channel1 window0~window7 enable, shadowed
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_cmsc_chn0_win_en CMSC channel1 window0~window7 enable 1'b0: Disabled 1'b1: Enabled

VPSS_CMSC_0500_CMSC_CHN2_WIN

Address: Operational Base(0x27C30500) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	sw_cmsc_chn0_win_en_shd CMSC channel2 window0~window7 enable, shadowed
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_cmsc_chn0_win_en CMSC channel2 window0~window7 enable 1'b0: Disabled 1'b1: Enabled

VPSS_CMSC_0500_CMSC_CHN3_WIN

Address: Operational Base(0x27C30500) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	sw_cmsc_chn0_win_en_shd CMSC channel3 window0~window7 enable, shadowed
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_cmsc_chn0_win_en CMSC channel3 window0~window7 enable 1'b0: Disabled 1'b1: Enabled

VPSS_CMSC_0500_CMSC_CHN0_MODE

Address: Operational Base(0x27C30500) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	sw_cmsc_chn0_mode_shd CMSC channel0 window0~window7 mode, shadowed
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_cmsc_chn0_mode CMSC channel0 window0~window7 mode 1'b0: Cover 1'b1: Mosaic

VPSS_CMSC_0500_CMSC_CHN1_MODE

Address: Operational Base(0x27C30500) + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	sw_cmsc_chn1_mode_shd CMSC channel1 window0~window7 mode, shadowed
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_cmsc_chn1_mode CMSC channel1 window0~window7 mode 1'b0: Cover 1'b1: Mosaic

VPSS_CMSC_0500_CMSC_CHN2_MODE

Address: Operational Base(0x27C30500) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	sw_cmsc_chn2_mode_shd CMSC channel2 window0~window7 mode, shadowed
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_cmsc_chn2_mode CMSC channel2 window0~window7 mode 1'b0: Cover 1'b1: Mosaic

VPSS_CMSC_0500_CMSC_CHN3_MODE

Address: Operational Base(0x27C30500) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	sw_cmsc_chn3_mode_shd CMSC channel3 window0~window7 mode, shadowed
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_cmsc_chn3_mode CMSC channel3 window0~window7 mode 1'b0: Cover 1'b1: Mosaic

VPSS_CMSC_0500_CMSC_WIN0_PARA

Address: Operational Base(0x27C30500) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	sw_cmsc_win0_intsct_pty_corr CMSC window0 intersection parity correction direction 2'd0: <| |> 2'd1: <| | 2'd2: >| |> 2'd3: >| |<
27:24	RW	0xf	sw_cmsc_win0_alpha CMSC window0 cover alpha, range [0, 15]
23:0	RW	0x000000	sw_cmsc_win0_yuv CMSC window0 YUV value, consist of {V8, U8, Y8}

VPSS_CMSC_0500_CMSC_WIN1_PARA

Address: Operational Base(0x27C30500) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:28	RW	0x0	sw_cmsc_win1_intsct_pty_corr CMSC window1 intersection parity correction direction 2'd0: <| |> 2'd1: <| |< 2'd2: >| |> 2'd3: >| |<
27:24	RW	0xf	sw_cmsc_win1_alpha CMSC window1 cover alpha, range [0, 15]
23:0	RW	0x000000	sw_cmsc_win1_yuv CMSC window1 YUV value, consist of {V8, U8, Y8}

VPSS_CMSC_0500_CMSC_WIN2_PARA

Address: Operational Base(0x27C30500) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	sw_cmsc_win2_intsct_pty_corr CMSC window2 intersection parity correction direction 2'd0: <| |> 2'd1: <| |< 2'd2: >| |> 2'd3: >| |<
27:24	RW	0xf	sw_cmsc_win2_alpha CMSC window2 cover alpha, range [0, 15]
23:0	RW	0x000000	sw_cmsc_win2_yuv CMSC window2 YUV value, consist of {V8, U8, Y8}

VPSS_CMSC_0500_CMSC_WIN3_PARA

Address: Operational Base(0x27C30500) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	sw_cmsc_win3_intsct_pty_corr CMSC window3 intersection parity correction direction 2'd0: <| |> 2'd1: <| |< 2'd2: >| |> 2'd3: >| |<
27:24	RW	0xf	sw_cmsc_win3_alpha CMSC window3 cover alpha, range [0, 15]
23:0	RW	0x000000	sw_cmsc_win3_yuv CMSC window3 YUV value, consist of {V8, U8, Y8}

VPSS_CMSC_0500_CMSC_WIN4_PARA

Address: Operational Base(0x27C30500) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	sw_cmsc_win4_intsct_pty_corr CMSC window4 intersection parity correction direction 2'd0: <| |> 2'd1: <| |< 2'd2: >| |> 2'd3: >| |<
27:24	RW	0xf	sw_cmsc_win4_alpha CMSC window4 cover alpha, range [0, 15]
23:0	RW	0x000000	sw_cmsc_win4_yuv CMSC window4 YUV value, consist of {V8, U8, Y8}

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VPSS_CMSC_0500_CMSC_WIN5_PARA

Address: Operational Base(0x27C30500) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	sw_cmsc_win5_intsct_pty_corr CMSC window5 intersection parity correction direction 2'd0: <| |> 2'd1: <| |< 2'd2: >| |> 2'd3: >| |<
27:24	RW	0xf	sw_cmsc_win5_alpha CMSC window5 cover alpha, range [0, 15]
23:0	RW	0x000000	sw_cmsc_win5_yuv CMSC window5 YUV value, consist of {V8, U8, Y8}

VPSS_CMSC_0500_CMSC_WIN6_PARA

Address: Operational Base(0x27C30500) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	sw_cmsc_win6_intsct_pty_corr CMSC window6 intersection parity correction direction 2'd0: <| |> 2'd1: <| |< 2'd2: >| |> 2'd3: >| |<
27:24	RW	0xf	sw_cmsc_win6_alpha CMSC window6 cover alpha, range [0, 15]
23:0	RW	0x000000	sw_cmsc_win6_yuv CMSC window6 YUV value, consist of {V8, U8, Y8}

VPSS_CMSC_0500_CMSC_WIN7_PARA

Address: Operational Base(0x27C30500) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	sw_cmsc_win7_intsct_pty_corr CMSC window7 intersection parity correction direction 2'd0: <| |> 2'd1: <| |< 2'd2: >| |> 2'd3: >| |<
27:24	RW	0xf	sw_cmsc_win7_alpha CMSC window7 cover alpha, range [0, 15]
23:0	RW	0x000000	sw_cmsc_win7_yuv CMSC window7 YUV value, consist of {V8, U8, Y8}

VPSS_CMSC_0500_CMSC_WIN0_L0_VTX

Address: Operational Base(0x27C30500) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win0_y0 CMSC window0 vertex0 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win0_x0 CMSC window0 vertex0 abscissa

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VPSS_CMSC_0500_CMSC_WIN0_L0_SLP

Address: Operational Base(0x27C30500) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win0_hor0 CMSC window0 line0 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win0_k0 CMSC window0 line0 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN0_L1_VTX

Address: Operational Base(0x27C30500) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win0_y1 CMSC window0 vertex1 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win0_x1 CMSC window0 vertex1 abscissa

VPSS_CMSC_0500_CMSC_WIN0_L1_SLP

Address: Operational Base(0x27C30500) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win0_hor1 CMSC window0 line1 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win0_k1 CMSC window0 line1 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN0_L2_VTX

Address: Operational Base(0x27C30500) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win0_y2 CMSC window0 vertex2 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win0_x2 CMSC window0 vertex2 abscissa

VPSS_CMSC_0500_CMSC_WIN0_L2_SLP

Address: Operational Base(0x27C30500) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win0_hor2 CMSC window0 line2 horizon flag 1'b0: Not horizontal 1'b1: Horizontal

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Bit	Attr	Reset Value	Description
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win0_k2 CMSC window0 line2 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN0_L3_VTX

Address: Operational Base(0x27C30500) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win0_y3 CMSC window0 vertex3 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win0_x3 CMSC window0 vertex3 abscissa

VPSS_CMSC_0500_CMSC_WIN0_L3_SLP

Address: Operational Base(0x27C30500) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_cmsc_win0_k3 CMSC window0 line3 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN1_L0_VTX

Address: Operational Base(0x27C30500) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win1_y0 CMSC window1 vertex0 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win1_x0 CMSC window1 vertex0 abscissa

VPSS_CMSC_0500_CMSC_WIN1_L0_SLP

Address: Operational Base(0x27C30500) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win1_hor0 CMSC window1 line0 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win1_k0 CMSC window1 line0 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN1_L1_VTX

Address: Operational Base(0x27C30500) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RW	0x0000	sw_cmsc_win1_y1 CMSC window1 vertex1 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win1_x1 CMSC window1 vertex1 abscissa

VPSS_CMSC_0500_CMSC_WIN1_L1_SLP

Address: Operational Base(0x27C30500) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win1_hor0 CMSC window1 line0 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win1_k0 CMSC window1 line0 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN1_L2_VTX

Address: Operational Base(0x27C30500) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win1_y2 CMSC window1 vertex2 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win1_x2 CMSC window1 vertex2 abscissa

VPSS_CMSC_0500_CMSC_WIN1_L2_SLP

Address: Operational Base(0x27C30500) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win1_hor2 CMSC window1 line2 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win1_k2 CMSC window1 line2 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN1_L3_VTX

Address: Operational Base(0x27C30500) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win1_y3 CMSC window1 vertex3 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win1_x3 CMSC window1 vertex3 abscissa

VPSS_CMSC_0500_CMSC_WIN1_L3_SLP

Address: Operational Base(0x27C30500) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_cmsc_win1_k3 CMSC window1 line3 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN2_L0_VTX

Address: Operational Base(0x27C30500) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win2_y0 CMSC window2 vertex0 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win2_x0 CMSC window2 vertex0 abscissa

VPSS_CMSC_0500_CMSC_WIN2_L0_SLP

Address: Operational Base(0x27C30500) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win2_hor0 CMSC window2 line0 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win2_k0 CMSC window2 line0 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN2_L1_VTX

Address: Operational Base(0x27C30500) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win2_y1 CMSC window2 vertex1 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win2_x1 CMSC window2 vertex1 abscissa

VPSS_CMSC_0500_CMSC_WIN2_L1_SLP

Address: Operational Base(0x27C30500) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win2_hor1 CMSC window2 line1 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win2_k1 CMSC window2 line1 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

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VPSS_CMSC_0500_CMSC_WIN2_L2_VTX

Address: Operational Base(0x27C30500) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win2_y2 CMSC window2 vertex2 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win2_x2 CMSC window2 vertex2 abscissa

VPSS_CMSC_0500_CMSC_WIN2_L2_SLP

Address: Operational Base(0x27C30500) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win2_hor2 CMSC window2 line2 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win2_k2 CMSC window2 line2 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN2_L3_VTX

Address: Operational Base(0x27C30500) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win2_y3 CMSC window2 vertex3 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win2_x3 CMSC window2 vertex3 abscissa

VPSS_CMSC_0500_CMSC_WIN2_L3_SLP

Address: Operational Base(0x27C30500) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_cmsc_win2_k3 CMSC window2 line3 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN3_L0_VTX

Address: Operational Base(0x27C30500) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win3_y0 CMSC window3 vertex0 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win3_x0 CMSC window3 vertex0 abscissa

VPSS_CMSC_0500_CMSC_WIN3_L0_SLP

Address: Operational Base(0x27C30500) + offset (0x00B4)

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Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win3_hor0 CMSC window3 line0 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win3_k0 CMSC window3 line0 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN3_L1_VTX

Address: Operational Base(0x27C30500) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win3_y1 CMSC window3 vertex1 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win3_x1 CMSC window3 vertex1 abscissa

VPSS_CMSC_0500_CMSC_WIN3_L1_SLP

Address: Operational Base(0x27C30500) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win3_hor1 CMSC window3 line1 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win3_k1 CMSC window3 line1 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN3_L2_VTX

Address: Operational Base(0x27C30500) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win3_y2 CMSC window3 vertex2 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win3_x2 CMSC window3 vertex2 abscissa

VPSS_CMSC_0500_CMSC_WIN3_L2_SLP

Address: Operational Base(0x27C30500) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win3_hor2 CMSC window3 line2 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
17:0	RW	0x00000	sw_cmsc_win3_k2 CMSC window3 line2 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN3_L3_VTX

Address: Operational Base(0x27C30500) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win3_y3 CMSC window3 vertex3 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win3_x3 CMSC window3 vertex3 abscissa

VPSS_CMSC_0500_CMSC_WIN3_L3_SLP

Address: Operational Base(0x27C30500) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_cmsc_win3_k3 CMSC window3 line3 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN4_L0_VTX

Address: Operational Base(0x27C30500) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win4_y0 CMSC window4 vertex0 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win4_x0 CMSC window4 vertex0 abscissa

VPSS_CMSC_0500_CMSC_WIN4_L0_SLP

Address: Operational Base(0x27C30500) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win4_hor0 CMSC window4 line0 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win4_k0 CMSC window4 line0 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN4_L1_VTX

Address: Operational Base(0x27C30500) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win4_y1 CMSC window4 vertex1 ordinate

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Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win4_x1 CMSC window4 vertex1 abscissa

VPSS_CMSC_0500_CMSC_WIN4_L1_SLP

Address: Operational Base(0x27C30500) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win4_hor1 CMSC window4 line1 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win4_k1 CMSC window4 line1 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN4_L2_VTX

Address: Operational Base(0x27C30500) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win4_y2 CMSC window4 vertex2 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win4_x2 CMSC window4 vertex2 abscissa

VPSS_CMSC_0500_CMSC_WIN4_L2_SLP

Address: Operational Base(0x27C30500) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win4_hor2 CMSC window4 line2 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win4_k2 CMSC window4 line2 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN4_L3_VTX

Address: Operational Base(0x27C30500) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win4_y3 CMSC window4 vertex3 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win4_x3 CMSC window4 vertex3 abscissa

VPSS_CMSC_0500_CMSC_WIN4_L3_SLP

Address: Operational Base(0x27C30500) + offset (0x00EC)

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Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_cmsc_win4_k3 CMSC window4 line3 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN5_L0_VTX

Address: Operational Base(0x27C30500) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win5_y0 CMSC window5 vertex0 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win5_x0 CMSC window5 vertex0 abscissa

VPSS_CMSC_0500_CMSC_WIN5_L0_SLP

Address: Operational Base(0x27C30500) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win5_hor0 CMSC window5 line0 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win5_k0 CMSC window5 line0 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN5_L1_VTX

Address: Operational Base(0x27C30500) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win5_y1 CMSC window5 vertex1 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win5_x1 CMSC window5 vertex1 abscissa

VPSS_CMSC_0500_CMSC_WIN5_L1_SLP

Address: Operational Base(0x27C30500) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win5_hor1 CMSC window5 line1 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win5_k1 CMSC window5 line1 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN5_L2_VTX

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Address: Operational Base(0x27C30500) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win5_y2 CMSC window5 vertex2 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win5_x2 CMSC window5 vertex2 abscissa

VPSS_CMSC_0500_CMSC_WIN5_L2_SLP

Address: Operational Base(0x27C30500) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win5_hor2 CMSC window5 line2 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win5_k2 CMSC window5 line2 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN5_L3_VTX

Address: Operational Base(0x27C30500) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win5_y3 CMSC window5 vertex3 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win5_x3 CMSC window5 vertex3 abscissa

VPSS_CMSC_0500_CMSC_WIN5_L3_SLP

Address: Operational Base(0x27C30500) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_cmsc_win5_k3 CMSC window5 line3 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN6_L0_VTX

Address: Operational Base(0x27C30500) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win6_y0 CMSC window6 vertex0 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win6_x0 CMSC window6 vertex0 abscissa

VPSS_CMSC_0500_CMSC_WIN6_L0_SLP

Address: Operational Base(0x27C30500) + offset (0x0114)

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Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win6_hor0 CMSC window6 line0 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win6_k0 CMSC window6 line0 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN6_L1_VTX

Address: Operational Base(0x27C30500) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win6_y1 CMSC window6 vertex1 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win6_x1 CMSC window6 vertex1 abscissa

VPSS_CMSC_0500_CMSC_WIN6_L1_SLP

Address: Operational Base(0x27C30500) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win6_hor1 CMSC window6 line1 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win6_k1 CMSC window6 line1 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN6_L2_VTX

Address: Operational Base(0x27C30500) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win6_y2 CMSC window6 vertex2 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win6_x2 CMSC window6 vertex2 abscissa

VPSS_CMSC_0500_CMSC_WIN6_L2_SLP

Address: Operational Base(0x27C30500) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win6_hor2 CMSC window6 line2 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
17:0	RW	0x00000	sw_cmsc_win6_k2 CMSC window6 line2 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN6_L3_VTX

Address: Operational Base(0x27C30500) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win6_y3 CMSC window6 vertex3 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win6_x3 CMSC window6 vertex3 abscissa

VPSS_CMSC_0500_CMSC_WIN6_L3_SLP

Address: Operational Base(0x27C30500) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_cmsc_win6_k3 CMSC window6 line3 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN7_L0_VTX

Address: Operational Base(0x27C30500) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win7_y0 CMSC window7 vertex0 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win7_x0 CMSC window7 vertex0 abscissa

VPSS_CMSC_0500_CMSC_WIN7_L0_SLP

Address: Operational Base(0x27C30500) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win7_hor0 CMSC window7 line0 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win7_k0 CMSC window7 line0 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN7_L1_VTX

Address: Operational Base(0x27C30500) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win7_y1 CMSC window7 vertex1 ordinate

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Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win7_x1 CMSC window7 vertex1 abscissa

VPSS_CMSC_0500_CMSC_WIN7_L1_SLP

Address: Operational Base(0x27C30500) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win7_hor1 CMSC window7 line1 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win7_k1 CMSC window7 line1 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN7_L2_VTX

Address: Operational Base(0x27C30500) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win7_y2 CMSC window7 vertex2 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win7_x2 CMSC window7 vertex2 abscissa

VPSS_CMSC_0500_CMSC_WIN7_L2_SLP

Address: Operational Base(0x27C30500) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_cmsc_win7_hor2 CMSC window7 line2 horizon flag 1'b0: Not horizontal 1'b1: Horizontal
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_cmsc_win7_k2 CMSC window7 line2 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

VPSS_CMSC_0500_CMSC_WIN7_L3_VTX

Address: Operational Base(0x27C30500) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_cmsc_win7_y3 CMSC window7 vertex3 ordinate
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_cmsc_win7_x3 CMSC window7 vertex3 abscissa

VPSS_CMSC_0500_CMSC_WIN7_L3_SLP

Address: Operational Base(0x27C30500) + offset (0x014C)

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Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_cmsc_win7_k3 CMSC window7 line3 slope 1bit for sign, 4bit for power, 13bit for digit, the order is {sign, power, digit}

3.4.2.3 Crop

QUAD_CROP_0700_0800_CROP_CTRL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	in_upd_dis Input frame end update shadow registers disable 1'b0: update shadow with input frame end 1'b1: update shadow with output frame end Note: Since the input size is larger than the output size, the shadow registers should be updated with the input frame end.
30:4	RO	0x0000000	reserved
3	RW	0x0	sw_crop3_en Channel3 crop enable
2	RW	0x0	sw_crop2_en Channel2 crop enable
1	RW	0x0	sw_crop1_en Channel1 crop enable
0	RW	0x0	sw_crop0_en Channel0 crop enable

QUAD_CROP_0700_0800_CROP_UPDATE

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	W1C	0x0	sys_crop3_force_upd Force update of configuration registers for channel3 crop
10	W1C	0x0	sys_crop2_force_upd Force update of configuration registers for channel2 crop
9	W1C	0x0	sys_crop1_force_upd Force update of configuration registers for channel1 crop
8	W1C	0x0	sys_crop0_force_upd Force update of configuration registers for channel0 crop
7:6	RO	0x0	reserved
5	RW	0x1	sys_cfg_gen_upd 1'b1: Automatic register update at frame end enabled 1'b0: Automatic register update at frame end disabled
4	W1C	0x0	sys_cfg_force_upd 1'b1: Immediately configure (update) shadow registers, write only
3:0	RO	0x0	reserved

QUAD_CROP_0700_0800_CROP_0_H_OFFS

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_0_h_offs Channel0 h offset

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QUAD_CROP_0700_0800_CROP_0_V_OFFS

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_0_v_offs Channel0 v offset

QUAD_CROP_0700_0800_CROP_0_H_SIZE

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_0_h_size Channel0 h size

QUAD_CROP_0700_0800_CROP_0_V_SIZE

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_0_v_size Channel0 v size

QUAD_CROP_0700_0800_CROP_1_H_OFFS

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_1_h_offs Channel1 h offset

QUAD_CROP_0700_0800_CROP_1_V_OFFS

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_1_v_offs Channel1 v offset

QUAD_CROP_0700_0800_CROP_1_H_SIZE

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_1_h_size Channel1 h size

QUAD_CROP_0700_0800_CROP_1_V_SIZE

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_1_v_size Channel1 v size

QUAD_CROP_0700_0800_CROP_2_H_OFFS

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_2_h_offs Channel2 h offset

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QUAD_CROP_0700_0800_CROP_2_V_OFFS

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_2_v_offs Channel2 v offset

QUAD_CROP_0700_0800_CROP_2_H_SIZE

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_2_h_size Channel2 h size

QUAD_CROP_0700_0800_CROP_2_V_SIZE

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_2_v_size Channel2 v size

QUAD_CROP_0700_0800_CROP_3_H_OFFS

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_3_h_offs Channel3 h offset

QUAD_CROP_0700_0800_CROP_3_V_OFFS

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_3_v_offs Channel3 v offset

QUAD_CROP_0700_0800_CROP_3_H_SIZE

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_3_h_size Channel3 h size

QUAD_CROP_0700_0800_CROP_3_V_SIZE

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_3_v_size Channel3 v size

QUAD_CROP_0700_0800_CROP_CTRL_SHD

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3	RO	0x0	sw_crop3_en_shd Channel3 crop enable shadow
2	RO	0x0	sw_crop2_en_shd Channel2 crop enable shadow
1	RO	0x0	sw_crop1_en_shd Channel1 crop enable shadow
0	RO	0x0	sw_crop0_en_shd Channel0 crop enable shadow

QUAD_CROP_0700_0800_CROP_0_H_OFFS_SHD

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_0_h_offs_shd Channel0 h offset shadow signal

QUAD_CROP_0700_0800_CROP_0_V_OFFS_SHD

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_0_v_offs_shd Channel0 v offset shadow signal

QUAD_CROP_0700_0800_CROP_0_H_SIZE_SHD

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_0_h_size_shd Channel0 h size shadow signal

QUAD_CROP_0700_0800_CROP_0_V_SIZE_SHD

Address: **Operational Base** + offset (0x007C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_0_v_size_shd Channel0 v size shadow signal

QUAD_CROP_0700_0800_CROP_1_H_OFFS_SHD

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_1_h_offs_shd Channel1 h offset shadow signal

QUAD_CROP_0700_0800_CROP_1_V_OFFS_SHD

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_1_v_offs_shd Channel1 v offset shadow signal

QUAD_CROP_0700_0800_CROP_1_H_SIZE_SHD

Address: **Operational Base** + offset (0x0088)

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Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_1_h_size_shd Channel1 h size shadow signal

QUAD_CROP_0700_0800_CROP_1_V_SIZE_SHD

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_1_v_size_shd Channel1 v size shadow signal

QUAD_CROP_0700_0800_CROP_2_H_OFFS_SHD

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	R/WSC	0x0000	sw_2_h_offs_shd Channel2 h offset shadow signal

QUAD_CROP_0700_0800_CROP_2_V_OFFS_SHD

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_2_v_offs_shd Channel2 v offset shadow signal

QUAD_CROP_0700_0800_CROP_2_H_SIZE_SHD

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_2_h_size_shd Channel2 h size shadow signal

QUAD_CROP_0700_0800_CROP_2_V_SIZE_SHD

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_2_v_size_shd Channel2 v size shadow signal

QUAD_CROP_0700_0800_CROP_3_H_OFFS_SHD

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_3_h_offs_shd Channel3 h offset shadow signal

QUAD_CROP_0700_0800_CROP_3_V_OFFS_SHD

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_3_v_offs_shd Channel3 v offset shadow signal

QUAD_CROP_0700_0800_CROP_3_H_SIZE_SHD

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Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_3_h_size_shd Channel3 h size shadow signal

QUAD_CROP_0700_0800_CROP_3_V_SIZE_SHD

Address: **Operational Base** + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_3_v_size_shd Channel3 v size shadow signal

3.4.2.4 ZME

VPSS_ZME_1000_Y_HOR_COE0_10

Address: Operational Base(0x27C31000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe0_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe0_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE0_32

Address: Operational Base(0x27C31000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe0_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe0_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE0_54

Address: Operational Base(0x27C31000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe0_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe0_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE0_76

Address: Operational Base(0x27C31000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe0_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe0_6 Y horizontal filter coefficient

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VPSS_ZME_1000_Y_HOR_COE1_10

Address: Operational Base(0x27C31000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe1_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe1_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE1_32

Address: Operational Base(0x27C31000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe1_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe1_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE1_54

Address: Operational Base(0x27C31000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe1_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe1_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE1_76

Address: Operational Base(0x27C31000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe1_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe1_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE2_10

Address: Operational Base(0x27C31000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe2_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe2_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE2_32

Address: Operational Base(0x27C31000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	sw_yy_tap8_coe2_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe2_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE2_54

Address: Operational Base(0x27C31000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe2_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe2_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE2_76

Address: Operational Base(0x27C31000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe2_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe2_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE3_10

Address: Operational Base(0x27C31000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe3_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe3_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE3_32

Address: Operational Base(0x27C31000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe3_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe3_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE3_54

Address: Operational Base(0x27C31000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe3_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_yy_tap8_coe3_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE3_76

Address: Operational Base(0x27C31000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe3_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe3_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE4_10

Address: Operational Base(0x27C31000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe4_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe4_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE4_32

Address: Operational Base(0x27C31000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe4_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe4_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE4_54

Address: Operational Base(0x27C31000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe4_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe4_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE4_76

Address: Operational Base(0x27C31000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe4_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe4_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE5_10

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Address: Operational Base(0x27C31000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe5_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe5_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE5_32

Address: Operational Base(0x27C31000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe5_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe5_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE5_54

Address: Operational Base(0x27C31000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe5_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe5_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE5_76

Address: Operational Base(0x27C31000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe5_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe5_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE6_10

Address: Operational Base(0x27C31000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe6_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe6_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE6_32

Address: Operational Base(0x27C31000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe6_3 Y horizontal filter coefficient

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Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe6_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE6_54

Address: Operational Base(0x27C31000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe6_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe6_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE6_76

Address: Operational Base(0x27C31000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe6_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe6_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE7_10

Address: Operational Base(0x27C31000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe7_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe7_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE7_32

Address: Operational Base(0x27C31000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe7_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe7_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE7_54

Address: Operational Base(0x27C31000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe7_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe7_4 Y horizontal filter coefficient

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VPSS_ZME_1000_Y_HOR_COE7_76

Address: Operational Base(0x27C31000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe7_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe7_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE8_10

Address: Operational Base(0x27C31000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe8_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe8_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE8_32

Address: Operational Base(0x27C31000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe8_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe8_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE8_54

Address: Operational Base(0x27C31000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe8_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe8_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE8_76

Address: Operational Base(0x27C31000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe8_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe8_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE9_10

Address: Operational Base(0x27C31000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	sw_yy_tap8_coe9_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe9_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE9_32

Address: Operational Base(0x27C31000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe9_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe9_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE9_54

Address: Operational Base(0x27C31000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe9_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe9_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE9_76

Address: Operational Base(0x27C31000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe9_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe9_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE10_10

Address: Operational Base(0x27C31000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe10_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe10_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE10_32

Address: Operational Base(0x27C31000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe10_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_yy_tap8_coe10_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE10_54

Address: Operational Base(0x27C31000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe10_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe10_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE10_76

Address: Operational Base(0x27C31000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe10_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe10_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE11_10

Address: Operational Base(0x27C31000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe11_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe11_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE11_32

Address: Operational Base(0x27C31000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe11_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe11_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE11_54

Address: Operational Base(0x27C31000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe11_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe11_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE11_76

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Address: Operational Base(0x27C31000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe11_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe11_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE12_10

Address: Operational Base(0x27C31000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe12_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe12_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE12_32

Address: Operational Base(0x27C31000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe12_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe12_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE12_54

Address: Operational Base(0x27C31000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe12_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe12_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE12_76

Address: Operational Base(0x27C31000) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe12_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe12_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE13_10

Address: Operational Base(0x27C31000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe13_1 Y horizontal filter coefficient

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Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe13_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE13_32

Address: Operational Base(0x27C31000) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe13_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe13_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE13_54

Address: Operational Base(0x27C31000) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe13_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe13_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE13_76

Address: Operational Base(0x27C31000) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe13_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe13_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE14_10

Address: Operational Base(0x27C31000) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe14_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe14_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE14_32

Address: Operational Base(0x27C31000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe14_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe14_2 Y horizontal filter coefficient

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VPSS_ZME_1000_Y_HOR_COE14_54

Address: Operational Base(0x27C31000) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe14_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe14_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE14_76

Address: Operational Base(0x27C31000) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe14_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe14_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE15_10

Address: Operational Base(0x27C31000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe15_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe15_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE15_32

Address: Operational Base(0x27C31000) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe15_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe15_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE15_54

Address: Operational Base(0x27C31000) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe15_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe15_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE15_76

Address: Operational Base(0x27C31000) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	sw_yy_tap8_coe15_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe15_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE16_10

Address: Operational Base(0x27C31000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe16_1 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe16_0 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE16_32

Address: Operational Base(0x27C31000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe16_3 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe16_2 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE16_54

Address: Operational Base(0x27C31000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe16_5 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe16_4 Y horizontal filter coefficient

VPSS_ZME_1000_Y_HOR_COE16_76

Address: Operational Base(0x27C31000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap8_coe16_7 Y horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap8_coe16_6 Y horizontal filter coefficient

VPSS_ZME_1000_Y_VER_COE0_10

Address: Operational Base(0x27C31000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe0_1 Y vertical filter coefficient
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_yy_tap6_coe0_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE0_32

Address: Operational Base(0x27C31000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe0_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe0_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE0_54

Address: Operational Base(0x27C31000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe0_5 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe0_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE0_76

Address: Operational Base(0x27C31000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe0_7 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe0_6 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE1_10

Address: Operational Base(0x27C31000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe1_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe1_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE1_32

Address: Operational Base(0x27C31000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe1_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe1_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE1_54

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Address: Operational Base(0x27C31000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe1_5 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe1_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE1_76

Address: Operational Base(0x27C31000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe1_7 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe1_6 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE2_10

Address: Operational Base(0x27C31000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe2_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe2_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE2_32

Address: Operational Base(0x27C31000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe2_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe2_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE2_54

Address: Operational Base(0x27C31000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe2_5 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe2_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE2_76

Address: Operational Base(0x27C31000) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe2_7 Y vertical filter coefficient

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Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe2_6 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE3_10

Address: Operational Base(0x27C31000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe3_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe3_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE3_32

Address: Operational Base(0x27C31000) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe3_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe3_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE3_54

Address: Operational Base(0x27C31000) + offset (0x0238)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe3_5 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe3_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE3_76

Address: Operational Base(0x27C31000) + offset (0x023C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe3_7 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe3_6 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE4_10

Address: Operational Base(0x27C31000) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe4_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe4_0 Y vertical filter coefficient

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VPSS_ZME_1000_Y_VER_COE4_32

Address: Operational Base(0x27C31000) + offset (0x0244)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe4_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe4_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE4_54

Address: Operational Base(0x27C31000) + offset (0x0248)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe4_5 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe4_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE4_76

Address: Operational Base(0x27C31000) + offset (0x024C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe4_7 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe4_6 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE5_10

Address: Operational Base(0x27C31000) + offset (0x0250)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe5_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe5_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE5_32

Address: Operational Base(0x27C31000) + offset (0x0254)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe5_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe5_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE5_54

Address: Operational Base(0x27C31000) + offset (0x0258)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	sw_yy_tap6_coe5_5 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe5_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE5_76

Address: Operational Base(0x27C31000) + offset (0x025C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe5_7 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe5_6 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE6_10

Address: Operational Base(0x27C31000) + offset (0x0260)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe6_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe6_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE6_32

Address: Operational Base(0x27C31000) + offset (0x0264)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe6_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe6_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE6_54

Address: Operational Base(0x27C31000) + offset (0x0268)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe6_5 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe6_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE6_76

Address: Operational Base(0x27C31000) + offset (0x026C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe6_7 Y vertical filter coefficient
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_yy_tap6_coe6_6 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE7_10

Address: Operational Base(0x27C31000) + offset (0x0270)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe7_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe7_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE7_32

Address: Operational Base(0x27C31000) + offset (0x0274)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe7_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe7_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE7_54

Address: Operational Base(0x27C31000) + offset (0x0278)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe7_5 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe7_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE7_76

Address: Operational Base(0x27C31000) + offset (0x027C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe7_7 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe7_6 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE8_10

Address: Operational Base(0x27C31000) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe8_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe8_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE8_32

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Address: Operational Base(0x27C31000) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe8_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe8_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE8_54

Address: Operational Base(0x27C31000) + offset (0x0288)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe8_5 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe8_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE8_76

Address: Operational Base(0x27C31000) + offset (0x028C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe8_7 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe8_6 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE9_10

Address: Operational Base(0x27C31000) + offset (0x0290)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe9_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe9_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE9_32

Address: Operational Base(0x27C31000) + offset (0x0294)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe9_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe9_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE9_54

Address: Operational Base(0x27C31000) + offset (0x0298)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe9_5 Y vertical filter coefficient

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Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe9_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE9_76

Address: Operational Base(0x27C31000) + offset (0x029C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe9_7 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe9_6 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE10_10

Address: Operational Base(0x27C31000) + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe10_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe10_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE10_32

Address: Operational Base(0x27C31000) + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe10_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe10_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE10_54

Address: Operational Base(0x27C31000) + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe10_5 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe10_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE10_76

Address: Operational Base(0x27C31000) + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe10_7 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe10_6 Y vertical filter coefficient

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VPSS_ZME_1000_Y_VER_COE11_10

Address: Operational Base(0x27C31000) + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe11_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe11_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE11_32

Address: Operational Base(0x27C31000) + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe11_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe11_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE11_54

Address: Operational Base(0x27C31000) + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe11_5 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe11_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE11_76

Address: Operational Base(0x27C31000) + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe11_7 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe11_6 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE12_10

Address: Operational Base(0x27C31000) + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe12_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe12_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE12_32

Address: Operational Base(0x27C31000) + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	sw_yy_tap6_coe12_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe12_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE12_54

Address: Operational Base(0x27C31000) + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe12_5 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe12_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE12_76

Address: Operational Base(0x27C31000) + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe12_7 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe12_6 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE13_10

Address: Operational Base(0x27C31000) + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe13_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe13_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE13_32

Address: Operational Base(0x27C31000) + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe13_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe13_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE13_54

Address: Operational Base(0x27C31000) + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe13_5 Y vertical filter coefficient
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_yy_tap6_coe13_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE13_76

Address: Operational Base(0x27C31000) + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe13_7 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe13_6 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE14_10

Address: Operational Base(0x27C31000) + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe14_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe14_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE14_32

Address: Operational Base(0x27C31000) + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe14_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe14_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE14_54

Address: Operational Base(0x27C31000) + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe14_5 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe14_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE14_76

Address: Operational Base(0x27C31000) + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe14_7 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe14_6 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE15_10

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Address: Operational Base(0x27C31000) + offset (0x02F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe15_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe15_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE15_32

Address: Operational Base(0x27C31000) + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe15_3 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe15_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE15_54

Address: Operational Base(0x27C31000) + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe15_5 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe15_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE15_76

Address: Operational Base(0x27C31000) + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe15_7 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe15_6 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE16_10

Address: Operational Base(0x27C31000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe16_1 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe16_0 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE16_32

Address: Operational Base(0x27C31000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe16_3 Y vertical filter coefficient

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Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe16_2 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE16_54

Address: Operational Base(0x27C31000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe16_5 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe16_4 Y vertical filter coefficient

VPSS_ZME_1000_Y_VER_COE16_76

Address: Operational Base(0x27C31000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_yy_tap6_coe16_7 Y vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_yy_tap6_coe16_6 Y vertical filter coefficient

VPSS_ZME_1000_UV_HOR_COE0_10

Address: Operational Base(0x27C31000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe0_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe0_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE0_32

Address: Operational Base(0x27C31000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe0_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe0_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE0_54

Address: Operational Base(0x27C31000) + offset (0x0408)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe0_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe0_4 UV horizontal filter coefficient

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VPSS_ZME_1000_UV_HOR_COE0_76

Address: Operational Base(0x27C31000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe0_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe0_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE1_10

Address: Operational Base(0x27C31000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe1_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe1_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE1_32

Address: Operational Base(0x27C31000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe1_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe1_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE1_54

Address: Operational Base(0x27C31000) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe1_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe1_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE1_76

Address: Operational Base(0x27C31000) + offset (0x041C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe1_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe1_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE2_10

Address: Operational Base(0x27C31000) + offset (0x0420)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	sw_uv_tap8_coe2_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe2_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE2_32

Address: Operational Base(0x27C31000) + offset (0x0424)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe2_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe2_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE2_54

Address: Operational Base(0x27C31000) + offset (0x0428)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe2_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe2_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE2_76

Address: Operational Base(0x27C31000) + offset (0x042C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe2_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe2_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE3_10

Address: Operational Base(0x27C31000) + offset (0x0430)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe3_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe3_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE3_32

Address: Operational Base(0x27C31000) + offset (0x0434)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe3_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_uv_tap8_coe3_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE3_54

Address: Operational Base(0x27C31000) + offset (0x0438)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe3_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe3_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE3_76

Address: Operational Base(0x27C31000) + offset (0x043C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe3_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe3_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE4_10

Address: Operational Base(0x27C31000) + offset (0x0440)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe4_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe4_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE4_32

Address: Operational Base(0x27C31000) + offset (0x0444)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe4_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe4_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE4_54

Address: Operational Base(0x27C31000) + offset (0x0448)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe4_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe4_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE4_76

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Address: Operational Base(0x27C31000) + offset (0x044C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe4_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe4_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE5_10

Address: Operational Base(0x27C31000) + offset (0x0450)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe5_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe5_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE5_32

Address: Operational Base(0x27C31000) + offset (0x0454)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe5_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe5_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE5_54

Address: Operational Base(0x27C31000) + offset (0x0458)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe5_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe5_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE5_76

Address: Operational Base(0x27C31000) + offset (0x045C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe5_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe5_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE6_10

Address: Operational Base(0x27C31000) + offset (0x0460)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe6_1 UV horizontal filter coefficient

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Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe6_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE6_32

Address: Operational Base(0x27C31000) + offset (0x0464)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe6_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe6_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE6_54

Address: Operational Base(0x27C31000) + offset (0x0468)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe6_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe6_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE6_76

Address: Operational Base(0x27C31000) + offset (0x046C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe6_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe6_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE7_10

Address: Operational Base(0x27C31000) + offset (0x0470)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe7_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe7_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE7_32

Address: Operational Base(0x27C31000) + offset (0x0474)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe7_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe7_2 UV horizontal filter coefficient

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VPSS_ZME_1000_UV_HOR_COE7_54

Address: Operational Base(0x27C31000) + offset (0x0478)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe7_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe7_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE7_76

Address: Operational Base(0x27C31000) + offset (0x047C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe7_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe7_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE8_10

Address: Operational Base(0x27C31000) + offset (0x0480)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe8_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe8_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE8_32

Address: Operational Base(0x27C31000) + offset (0x0484)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe8_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe8_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE8_54

Address: Operational Base(0x27C31000) + offset (0x0488)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe8_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe8_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE8_76

Address: Operational Base(0x27C31000) + offset (0x048C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	sw_uv_tap8_coe8_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe8_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE9_10

Address: Operational Base(0x27C31000) + offset (0x0490)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe9_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe9_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE9_32

Address: Operational Base(0x27C31000) + offset (0x0494)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe9_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe9_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE9_54

Address: Operational Base(0x27C31000) + offset (0x0498)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe9_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe9_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE9_76

Address: Operational Base(0x27C31000) + offset (0x049C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe9_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe9_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE10_10

Address: Operational Base(0x27C31000) + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe10_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_uv_tap8_coe10_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE10_32

Address: Operational Base(0x27C31000) + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe10_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe10_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE10_54

Address: Operational Base(0x27C31000) + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe10_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe10_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE10_76

Address: Operational Base(0x27C31000) + offset (0x04AC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe10_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe10_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE11_10

Address: Operational Base(0x27C31000) + offset (0x04B0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe11_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe11_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE11_32

Address: Operational Base(0x27C31000) + offset (0x04B4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe11_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe11_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE11_54

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Address: Operational Base(0x27C31000) + offset (0x04B8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe11_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe11_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE11_76

Address: Operational Base(0x27C31000) + offset (0x04BC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe11_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe11_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE12_10

Address: Operational Base(0x27C31000) + offset (0x04C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe12_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe12_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE12_32

Address: Operational Base(0x27C31000) + offset (0x04C4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe12_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe12_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE12_54

Address: Operational Base(0x27C31000) + offset (0x04C8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe12_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe12_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE12_76

Address: Operational Base(0x27C31000) + offset (0x04CC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe12_7 UV horizontal filter coefficient

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Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe12_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE13_10

Address: Operational Base(0x27C31000) + offset (0x04D0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe13_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe13_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE13_32

Address: Operational Base(0x27C31000) + offset (0x04D4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe13_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe13_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE13_54

Address: Operational Base(0x27C31000) + offset (0x04D8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe13_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe13_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE13_76

Address: Operational Base(0x27C31000) + offset (0x04DC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe13_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe13_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE14_10

Address: Operational Base(0x27C31000) + offset (0x04E0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe14_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe14_0 UV horizontal filter coefficient

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VPSS_ZME_1000_UV_HOR_COE14_32

Address: Operational Base(0x27C31000) + offset (0x04E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe14_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe14_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE14_54

Address: Operational Base(0x27C31000) + offset (0x04E8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe14_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe14_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE14_76

Address: Operational Base(0x27C31000) + offset (0x04EC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe14_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe14_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE15_10

Address: Operational Base(0x27C31000) + offset (0x04F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe15_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe15_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE15_32

Address: Operational Base(0x27C31000) + offset (0x04F4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe15_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe15_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE15_54

Address: Operational Base(0x27C31000) + offset (0x04F8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	sw_uv_tap8_coe15_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe15_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE15_76

Address: Operational Base(0x27C31000) + offset (0x04FC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe15_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe15_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE16_10

Address: Operational Base(0x27C31000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe16_1 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe16_0 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE16_32

Address: Operational Base(0x27C31000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe16_3 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe16_2 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE16_54

Address: Operational Base(0x27C31000) + offset (0x0508)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe16_5 UV horizontal filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap8_coe16_4 UV horizontal filter coefficient

VPSS_ZME_1000_UV_HOR_COE16_76

Address: Operational Base(0x27C31000) + offset (0x050C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap8_coe16_7 UV horizontal filter coefficient
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_uv_tap8_coe16_6 UV horizontal filter coefficient

VPSS_ZME_1000_UV_VER_COE0_10

Address: Operational Base(0x27C31000) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe0_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe0_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE0_32

Address: Operational Base(0x27C31000) + offset (0x0604)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe0_3 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe0_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE0_54

Address: Operational Base(0x27C31000) + offset (0x0608)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe0_5 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe0_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE0_76

Address: Operational Base(0x27C31000) + offset (0x060C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe0_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe0_6 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE1_10

Address: Operational Base(0x27C31000) + offset (0x0610)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe1_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe1_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE1_32

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Address: Operational Base(0x27C31000) + offset (0x0614)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe1_3 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe1_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE1_54

Address: Operational Base(0x27C31000) + offset (0x0618)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe1_5 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe1_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE1_76

Address: Operational Base(0x27C31000) + offset (0x061C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe1_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe1_6 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE2_10

Address: Operational Base(0x27C31000) + offset (0x0620)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe2_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe2_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE2_32

Address: Operational Base(0x27C31000) + offset (0x0624)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe2_3 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe2_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE2_54

Address: Operational Base(0x27C31000) + offset (0x0628)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe2_5 UV vertical filter coefficient

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Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe2_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE2_76

Address: Operational Base(0x27C31000) + offset (0x062C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe2_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe2_6 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE3_10

Address: Operational Base(0x27C31000) + offset (0x0630)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe3_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe3_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE3_32

Address: Operational Base(0x27C31000) + offset (0x0634)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe3_3 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe3_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE3_54

Address: Operational Base(0x27C31000) + offset (0x0638)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe3_5 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe3_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE3_76

Address: Operational Base(0x27C31000) + offset (0x063C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe3_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe3_6 UV vertical filter coefficient

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VPSS_ZME_1000_UV_VER_COE4_10

Address: Operational Base(0x27C31000) + offset (0x0640)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe4_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe4_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE4_32

Address: Operational Base(0x27C31000) + offset (0x0644)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe4_3 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe4_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE4_54

Address: Operational Base(0x27C31000) + offset (0x0648)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe4_5 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe4_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE4_76

Address: Operational Base(0x27C31000) + offset (0x064C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe4_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe4_6 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE5_10

Address: Operational Base(0x27C31000) + offset (0x0650)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe5_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe5_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE5_32

Address: Operational Base(0x27C31000) + offset (0x0654)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	sw_uv_tap6_coe5_3 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe5_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE5_54

Address: Operational Base(0x27C31000) + offset (0x0658)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe5_5 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe5_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE5_76

Address: Operational Base(0x27C31000) + offset (0x065C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe5_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe5_6 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE6_10

Address: Operational Base(0x27C31000) + offset (0x0660)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe6_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe6_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE6_32

Address: Operational Base(0x27C31000) + offset (0x0664)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe6_3 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe6_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE6_54

Address: Operational Base(0x27C31000) + offset (0x0668)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe6_5 UV vertical filter coefficient
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_uv_tap6_coe6_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE6_76

Address: Operational Base(0x27C31000) + offset (0x066C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe6_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe6_6 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE7_10

Address: Operational Base(0x27C31000) + offset (0x0670)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe7_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe7_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE7_32

Address: Operational Base(0x27C31000) + offset (0x0674)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe7_3 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe7_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE7_54

Address: Operational Base(0x27C31000) + offset (0x0678)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe7_5 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe7_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE7_76

Address: Operational Base(0x27C31000) + offset (0x067C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe7_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe7_6 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE8_10

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Address: Operational Base(0x27C31000) + offset (0x0680)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe8_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe8_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE8_32

Address: Operational Base(0x27C31000) + offset (0x0684)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe8_3 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe8_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE8_54

Address: Operational Base(0x27C31000) + offset (0x0688)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe8_5 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe8_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE8_76

Address: Operational Base(0x27C31000) + offset (0x068C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe8_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe8_6 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE9_10

Address: Operational Base(0x27C31000) + offset (0x0690)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe9_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe9_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE9_32

Address: Operational Base(0x27C31000) + offset (0x0694)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe9_3 UV vertical filter coefficient

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Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe9_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE9_54

Address: Operational Base(0x27C31000) + offset (0x0698)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe9_5 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe9_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE9_76

Address: Operational Base(0x27C31000) + offset (0x069C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe9_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe9_6 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE10_10

Address: Operational Base(0x27C31000) + offset (0x06A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe10_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe10_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE10_32

Address: Operational Base(0x27C31000) + offset (0x06A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe10_3 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe10_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE10_54

Address: Operational Base(0x27C31000) + offset (0x06A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe10_5 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe10_4 UV vertical filter coefficient

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VPSS_ZME_1000_UV_VER_COE10_76

Address: Operational Base(0x27C31000) + offset (0x06AC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe10_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe10_6 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE11_10

Address: Operational Base(0x27C31000) + offset (0x06B0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe11_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe11_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE11_32

Address: Operational Base(0x27C31000) + offset (0x06B4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe11_3 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe11_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE11_54

Address: Operational Base(0x27C31000) + offset (0x06B8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe11_5 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe11_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE11_76

Address: Operational Base(0x27C31000) + offset (0x06BC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe11_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe11_6 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE12_10

Address: Operational Base(0x27C31000) + offset (0x06C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	sw_uv_tap6_coe12_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe12_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE12_32

Address: Operational Base(0x27C31000) + offset (0x06C4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe12_3 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe12_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE12_54

Address: Operational Base(0x27C31000) + offset (0x06C8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe12_5 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe12_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE12_76

Address: Operational Base(0x27C31000) + offset (0x06CC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe12_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe12_6 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE13_10

Address: Operational Base(0x27C31000) + offset (0x06D0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe13_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe13_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE13_32

Address: Operational Base(0x27C31000) + offset (0x06D4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe13_3 UV vertical filter coefficient
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_uv_tap6_coe13_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE13_54

Address: Operational Base(0x27C31000) + offset (0x06D8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe13_5 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe13_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE13_76

Address: Operational Base(0x27C31000) + offset (0x06DC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe13_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe13_6 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE14_10

Address: Operational Base(0x27C31000) + offset (0x06E0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe14_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe14_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE14_32

Address: Operational Base(0x27C31000) + offset (0x06E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe14_3 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe14_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE14_54

Address: Operational Base(0x27C31000) + offset (0x06E8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe14_5 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe14_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE14_76

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Address: Operational Base(0x27C31000) + offset (0x06EC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe14_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe14_6 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE15_10

Address: Operational Base(0x27C31000) + offset (0x06F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe15_1 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe15_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE15_32

Address: Operational Base(0x27C31000) + offset (0x06F4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe15_3 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe15_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE15_54

Address: Operational Base(0x27C31000) + offset (0x06F8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe15_5 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe15_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE15_76

Address: Operational Base(0x27C31000) + offset (0x06FC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe15_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe15_6 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE16_10

Address: Operational Base(0x27C31000) + offset (0x0700)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe16_1 UV vertical filter coefficient

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Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe16_0 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE16_32

Address: Operational Base(0x27C31000) + offset (0x0704)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe16_3 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe16_2 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE16_54

Address: Operational Base(0x27C31000) + offset (0x0708)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe16_5 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe16_4 UV vertical filter coefficient

VPSS_ZME_1000_UV_VER_COE16_76

Address: Operational Base(0x27C31000) + offset (0x070C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_uv_tap6_coe16_7 UV vertical filter coefficient
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_uv_tap6_coe16_6 UV vertical filter coefficient

VPSS_ZME_1000_ZME_CTRL

Address: Operational Base(0x27C31000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_scl_yuv420_real_en Scale input real yuv420 enable.
30	RW	0x0	sw_422to420_en Scale from yuv422 to yuv420 enable.
29:16	RO	0x0000	reserved
15	RW	0x0	sw_8k_en Use for 8K 1'b0: Disable 8K 1'b1: Enable 8K
14	RW	0x0	sw_in_clip_en Use for 8K 1'b0: Disable scale in clip 1'b1: Enable scale in clip
13	RW	0x0	sw_clip_en Use for 8K 1'b0: Disable scale out clip 1'b1: Enable scale out clip

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Bit	Attr	Reset Value	Description
12:1	RO	0x000	reserved
0	RW	0x1	sw_gating_en Module auto gating enable.

VPSS_ZME_1000_ZME_UPDATE

Address: Operational Base(0x27C31000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x1	sys_cfg_gen_upd 1'b1: Automatic register update at frame end enabled 1'b0: Automatic register update at frame end disabled
4	W1C	0x0	sys_cfg_force_upd 1'b0: Nothing happens 1'b1: Update shadow registers
3:0	RO	0x0	reserved

VPSS_ZME_1000_ZME_H_SIZE

Address: Operational Base(0x27C31000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_hc_size Scale out horizontal UV size, only works when sw_scl_clip_en equal to 1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_hy_size Scale out horizontal Y size, only works when sw_scl_clip_en equal to 1.

VPSS_ZME_1000_ZME_H_OFFS

Address: Operational Base(0x27C31000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x0	sw_hc_st_coord Horizontal starting coordinates of the uv component of the poly-phase filter for 8K. Configure sw_hy_st_coord = 3
19:16	RW	0x0	sw_hy_st_coord Horizontal starting coordinates of the y component of the poly-phase filter for 8K. Configure sw_hy_st_coord = 3
15:12	RW	0x0	sw_in_hc_offs Scale in UV data cut some pixels if needed, only works when sw_scl_in_clip_en is effect.
11:8	RW	0x0	sw_in_hy_offs Scale in Y data cut some pixels if needed, only works when sw_in_clip_en is effect.
7:4	RW	0x0	sw_hc_offs_mi DDR data width is 128bit but UV data width is 8bit. This register configure the offset of first UV pixel in 128bit, which range from 0~15.
3:0	RW	0x0	sw_hy_offs_mi DDR data width is 128bit but Y data width is 8bit. This register configure the offset of first Y pixel in 128bit, which range from 0~15.

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VPSS_ZME_1000_Y_SCL_CTRL

Address: Operational Base(0x27C31000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:13	RW	0x0	sw_yy_xgt_mode Horizontal drop line mode 2'b00: drop 1 pixel for every 2 pixel 2'b01: generate 1 average pixel for every 2 pixel 2'b10: drop 3 pixel for every 4 pixel 2'b11: generate 1 average pixel for every 4 pixel
12	RW	0x0	sw_yy_xgt_en Horizontal drop line enable for scale down over 8times
11:10	RW	0x0	sw_yy_gt_mode Vertical drop line mode 2'b00: drop 1 for every two line 2'b01: drop 3 for every four line 2'b10: drop 1 for every four line 2'b11: drop auto
9	RW	0x0	sw_yy_gt_en Vertical drop line enable for scale down over 6times
8	RW	0x0	sw_yy_dering_en Scale deringing enable
7:6	RW	0x3	sw_yy_yscl_mode Vertical scale mode 2'b11: multi-phase others: reserved
5	RW	0x0	sw_yy_ysu_en Vertical scale up enable
4	RW	0x0	sw_yy_ysd_en Vertical scale down enable
3:2	RW	0x3	sw_yy_xscl_mode Horizontal scale mode 2'b11: multi-phase others: reserved
1	RW	0x0	sw_yy_xsu_en Horizontal scale up enable
0	RW	0x0	sw_yy_xsd_en Horizontal scale down enable

VPSS_ZME_1000_Y_SRC_SIZE

Address: Operational Base(0x27C31000) + offset (0x0814)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_yy_src_height Scale height of source (input), real-1
15:0	RW	0x0000	sw_yy_src_width Scale width of source (input), real-1

VPSS_ZME_1000_Y_DST_SIZE

Address: Operational Base(0x27C31000) + offset (0x0818)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_yy_dst_height Scale height of destination (output), real-1
15:0	RW	0x0000	sw_yy_dst_width Scale width of destination (output), real-1

VPSS_ZME_1000_Y_DERING_PARA

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Address: Operational Base(0x27C31000) + offset (0x081C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x0d	sw_yy_dering_delta Deringing blending beta
23:21	RO	0x0	reserved
20:16	RW	0x10	sw_yy_dering_alpha Deringing blending alpha
15:13	RO	0x0	reserved
12:8	RW	0x04	sw_yy_dering_sen1 Deringing sensitivity1
7:5	RO	0x0	reserved
4:0	RW	0x10	sw_yy_dering_sen0 Deringing sensitivity0

VPSS_ZME_1000_Y_XSCL_FACTOR

Address: Operational Base(0x27C31000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_yy_xscl_offset Horizontal scaler factor offset
15:0	RW	0x0000	sw_yy_xscl_factor Horizontal scale down: (src_width-1)/(dst_width-1)*2^12 Horizontal sacle up: (src_width-1)/(dst_width-1)*2^16

VPSS_ZME_1000_Y_YSCL_FACTOR

Address: Operational Base(0x27C31000) + offset (0x0824)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_yy_yscl_offset Vertical scaler factor offset
15:0	RW	0x0000	sw_yy_yscl_factor Vertical scale down: (src_height-1)/(dst_height-1)*2^12 Vertical sacle up: (src_height-1)/(dst_height-1)*2^16

VPSS_ZME_1000_UV_SCL_CTRL

Address: Operational Base(0x27C31000) + offset (0x0830)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:13	RW	0x0	sw_uv_xgt_mode Horizontal drop line mode 2'b00: drop 1 pixel for every 2 pixel 2'b01: generate 1 average pixel for every 2 pixel 2'b10: drop 3 pixel for every 4 pixel 2'b11: generate 1 average pixel for every 4 pixel
12	RW	0x0	sw_uv_xgt_en Horizontal drop line enable for scale down over 8times
11:10	RW	0x0	sw_uv_gt_mode Vertical drop line mode 2'b00: drop 1 for every two line 2'b01: drop 3 for every four line 2'b10: drop 1 for every four line 2'b11: drop auto
9	RW	0x0	sw_uv_gt_en Vertical drop line enable for scale down over 6times
8	RW	0x0	sw_uv_dering_en Scale deringing enable

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Bit	Attr	Reset Value	Description
7:6	RW	0x3	sw_uv_yscl_mode Vertical scale mode 2'b11: multi-phase others: reserved
5	RW	0x0	sw_uv_ysu_en Vertical scale up enable
4	RW	0x0	sw_uv_ysd_en Vertical scale down enable
3:2	RW	0x3	sw_uv_xscl_mode Horizontal scale mode 2'b11: multi-phase others: reserved
1	RW	0x0	sw_uv_xsu_en Horizontal scale up enable
0	RW	0x0	sw_uv_xsd_en Horizontal scale down enable

VPSS_ZME_1000_UV_SRC_SIZE

Address: Operational Base(0x27C31000) + offset (0x0834)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_uv_src_height Scale height of source (input), real-1
15:0	RW	0x0000	sw_uv_src_width Scale width of source (input), real-1

VPSS_ZME_1000_UV_DST_SIZE

Address: Operational Base(0x27C31000) + offset (0x0838)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_uv_dst_height Scale height of destination (output), real-1
15:0	RW	0x0000	sw_uv_dst_width Scale width of destination (output), real-1

VPSS_ZME_1000_UV_DERING_PARA

Address: Operational Base(0x27C31000) + offset (0x083C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x0d	sw_uv_dering_delta Deringing blending beta
23:21	RO	0x0	reserved
20:16	RW	0x10	sw_uv_dering_alpha Deringing blending alpha
15:13	RO	0x0	reserved
12:8	RW	0x04	sw_uv_dering_sen1 Deringing sensitivity1
7:5	RO	0x0	reserved
4:0	RW	0x10	sw_uv_dering_sen0 Deringing sensitivity0

VPSS_ZME_1000_UV_XSCL_FACTOR

Address: Operational Base(0x27C31000) + offset (0x0840)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_uv_xscl_offset Horizontal scaler factor offset

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	sw_uv_xscl_factor Horizontal scale down: (src_width/2-1)/(dst_width/2-1)*2^12 Horizontal sacle up: (src_width/2-1)/(dst_width/2-1)*2^16

VPSS_ZME_1000_UV_YSCL_FACTOR

Address: Operational Base(0x27C31000) + offset (0x0844)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_uv_yscl_offset Vertical scaler factor offset
15:0	RW	0x0000	sw_uv_yscl_factor If sw_scl_yuv420_real_en = 1, Vertical scale down: (src_height/2 - 1)/(dst_height/2 - 1)*2^12 Vertical sacle up: (src_height/2 - 1)/(dst_height/2 - 1)*2^16 elseif sw_scl_422to420_en = 1, Vertical scale down: (src_height - 1)/(dst_height/2 - 1)*2^12 Vertical sacle up: (src_height - 1)/(dst_height/2 - 1)*2^16 Else Vertical scale down: (src_height - 1)/(dst_height - 1)*2^12 Vertical sacle up: (src_height - 1)/(dst_height - 1)*2^16

VPSS_ZME_1000_SCL_CTRL_SHD

Address: Operational Base(0x27C31000) + offset (0x084C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RO	0x0	sw_8k_en_shd Scale 8K enable
13	RO	0x0	sw_in_clip_en_shd Scale in clip enable
12	RO	0x0	sw_clip_en_shd Scale out clip enable
11:10	RO	0x0	reserved
9	RO	0x0	sw_uv_dering_en_shd Scale deringing enable
8	RO	0x0	sw_yy_dering_en_shd Scale deringing enable
7	RO	0x0	sw_uv_ysu_en_shd Vertical scale up enable
6	RO	0x0	sw_uv_ysd_en_shd Vertical scale down enable
5	RO	0x0	sw_uv_xsu_en_shd Horizontal scale up enable
4	RO	0x0	sw_uv_xsd_en_shd Horizontal scale down enable
3	RO	0x0	sw_yy_ysu_en_shd Vertical scale up enable
2	RO	0x0	sw_yy_ysd_en_shd Vertical scale down enable
1	RO	0x0	sw_yy_xsu_en_shd Horizontal scale up enable
0	RO	0x0	sw_yy_xsd_en_shd Horizontal scale down enable

VPSS_ZME_1000_Y_SRC_SIZE_SHD

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Address: Operational Base(0x27C31000) + offset (0x0850)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	sw_y_src_height_shd Scale height of source (input), real-1
15:0	RO	0x0000	sw_y_src_width_shd Scale width of source (input), real-1

VPSS_ZME_1000_Y_DST_SIZE_SHD

Address: Operational Base(0x27C31000) + offset (0x0854)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	sw_yy_dst_height_shd Scale height of destination (output), real-1
15:0	RO	0x0000	sw_yy_dst_width_shd Scale width of destination (output), real-1

VPSS_ZME_1000_Y_XSCL_FACTOR_SHD

Address: Operational Base(0x27C31000) + offset (0x0858)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	sw_yy_xscl_offset_shd Horizontal scaler factor offset
15:0	RO	0x0000	sw_yy_xscl_factor_shd Horizontal scale down: (src_width-1)/(dst_width-1)*2^12 Horizontal sacle up: (src_width-1)/(dst_width-1)*2^16

VPSS_ZME_1000_Y_YSCL_FACTOR_SHD

Address: Operational Base(0x27C31000) + offset (0x085C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	sw_yy_yscl_offset_shd Vertical scaler factor offset
15:0	RO	0x0000	sw_yy_yscl_factor_shd Vertical scale down: (src_height-1)/(dst_height-1)*2^12 Vertical sacle up: (src_height-1)/(dst_height-1)*2^16

VPSS_ZME_1000_UV_SRC_SIZE_SHD

Address: Operational Base(0x27C31000) + offset (0x0860)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	sw_uv_src_height_shd Scale height of source (input), real-1
15:0	RO	0x0000	sw_uv_src_width_shd Scale width of source (input), real-1

VPSS_ZME_1000_UV_DST_SIZE_SHD

Address: Operational Base(0x27C31000) + offset (0x0864)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	sw_uv_dst_height_shd Scale height of destination (output), real-1
15:0	RO	0x0000	sw_uv_dst_width_shd Scale width of destination (output), real-1

VPSS_ZME_1000_UV_XSCL_FACTOR_SHD

Address: Operational Base(0x27C31000) + offset (0x0868)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	sw_uv_xscl_offset_shd Horizontal scaler factor offset

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	sw_uv_xscl_factor_shd Horizontal scale down: (src_width/2-1)/(dst_width/2-1)*2^12 Horizontal sacle up: (src_width/2-1)/(dst_width/2-1)*2^16

VPSS_ZME_1000_UV_YSCL_FACTOR_SHD

Address: Operational Base(0x27C31000) + offset (0x086C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	sw_uv_yscl_offset_shd Vertical scaler factor offset
15:0	RO	0x0000	sw_uv_yscl_factor_shd If sw_scl_yuv420_real_en = 1, Vertical scale down: (src_height/2 - 1)/(dst_height/2 - 1)*2^12 Vertical sacle up: (src_height/2 - 1)/(dst_height/2 - 1)*2^16 elseif sw_scl_422to420_en = 1, Vertical scale down: (src_height - 1)/(dst_height/2 - 1)*2^12 Vertical sacle up: (src_height - 1)/(dst_height/2 - 1)*2^16 Else Vertical scale down: (src_height - 1)/(dst_height - 1)*2^12 Vertical sacle up: (src_height - 1)/(dst_height - 1)*2^16

VPSS_ZME_1000_ZME_H_SIZE_SHD

Address: Operational Base(0x27C31000) + offset (0x0870)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_hc_size_shd Scale out horizontal UV size
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_hy_size_shd Scale out horizontal Y size

VPSS_ZME_1000_ZME_H_OFFS_SHD

Address: Operational Base(0x27C31000) + offset (0x0874)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x0	sw_hc_st_coord_shd Horizontal starting coordinates of the uv component of the poly-phase filter for 8K. Configure sw_hy_st_coord = 3
19:16	RW	0x0	sw_hy_st_coord_shd Horizontal starting coordinates of the y component of the poly-phase filter for 8K. Configure sw_hy_st_coord = 3
15:12	RW	0x0	sw_in_hc_offs_shd Scale in UV data cut some pixels if needed, only works when sw_scl_in_clip_en is effect.
11:8	RW	0x0	sw_in_hy_offs_shd Scale in Y data cut some pixels if needed, only works when sw_in_clip_en is effect.
7:4	RW	0x0	sw_hc_offs_mi_shd DDR data width is 128bit but UV data width is 8bit. This register configure the offset of first UV pixel in 128bit, which range from 0~15.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	sw_hy_offs_mi_shd DDR data width is 128bit but Y data width is 8bit. This register configure the offset of first Y pixel in 128bit, which range from 0~15.

3.4.2.5 Bilinear Scale

VPSS_SCALE_1C00_2800_2C00_SCALE_CTRL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_scl_yuv420_real_en Scale input real yuv420 enable.
30	RW	0x0	sw_scl_422to420_en Scale from yuv422 to yuv420 enable.
29:15	RO	0x0000	reserved
14	RW	0x0	sw_scl_in_clip_en Use for 8K 1'b0: Disable scale in clip 1'b1: Enable scale in clip
13	RW	0x0	sw_scl_clip_en Use for 8K 1'b0: Disable scale out clip 1'b1: Enable scale out clip
12:4	RO	0x000	reserved
3	RW	0x0	sw_scale_vc_en 1'b0: Bypass vertical chrominance scaling unit 1'b1: Enable vertical chrominance scaling unit
2	RW	0x0	sw_scale_vy_en 1'b0: Bypass vertical luminance scaling unit 1'b1: Enable vertical luminance scaling unit
1	RW	0x0	sw_scale_hc_en 1'b0: Bypass horizontal chrominance scaling unit 1'b1: Enable horizontal chrominance scaling unit
0	RW	0x0	sw_scale_hy_en 1'b0: Bypass horizontal luminance scaling unit 1'b1: Enable horizontal luminance scaling unit

VPSS_SCALE_1C00_2800_2C00_SCALE_UPDATE

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x1	sys_cfg_gen_upd 1'b1: Automatic register update at frame end enabled 1'b0: Automatic register update at frame end disabled
4	W1C	0x0	sys_cfg_force_upd 1'b0: Nothing happens 1'b1: Update shadow registers
3:0	RO	0x0	reserved

VPSS_SCALE_1C00_2800_2C00_SCALE_SRC_SIZE

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_scale_src_height Scale height of source (input)

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Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_scale_src_width Scale width of source (input)

VPSS_SCALE_1C00_2800_2C00_SCALE_DST_SIZE

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_scale_dst_height Scale height of destination (output)
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_scale_dst_width Scale width of destination (output)

VPSS_SCALE_1C00_2800_2C00_SCALE_HY_FAC

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_scale_hy_fac This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: (src_width - 1) / (dst_width - 1)) = scale The value of the sw_scale_hy_fac register then has to be int(scale * 2^12).

VPSS_SCALE_1C00_2800_2C00_SCALE_HC_FAC

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_scale_hc_fac This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: ((src_width / 2) - 1) / ((dst_width / 2) - 1)) = scale The value of the sw_scale_hc_fac register then has to be int(scale * 2^12).

VPSS_SCALE_1C00_2800_2C00_SCALE_VY_FAC

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_scale_vy_fac This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: (src_height - 1) / (dst_height - 1)) = scale The value of the sw_scale_vy_fac register then has to be int(scale * 2^12).

VPSS_SCALE_1C00_2800_2C00_SCALE_VC_FAC

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17:0	RW	0x00000	sw_scale_vc_fac This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: If sw_scl_yuv420_real_en = 1, ((src_height / 2) - 1) / ((dst_height / 2) - 1)) = scale elseif sw_scl_422to420_en = 1, (src_height - 1) / ((dst_height / 2) - 1)) = scale Else (src_height - 1) / (dst_height - 1)) = scale The value of the sw_scale_vc_fac register then has to be int(scale * 2^12).

VPSS_SCALE_1C00_2800_2C00_SCALE_HY_OFFS

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_scale_hy_offs This register is set to the horizontal luminance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

VPSS_SCALE_1C00_2800_2C00_SCALE_HC_OFFS

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_scale_hc_offs This register is set to the horizontal chrominance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

VPSS_SCALE_1C00_2800_2C00_SCALE_VY_OFFS

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_scale_vy_offs This register is set to the vertical luminance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

VPSS_SCALE_1C00_2800_2C00_SCALE_VC_OFFS

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_scale_vc_offs This register is set to the vertical chrominance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

VPSS_SCALE_1C00_2800_2C00_SCALE_HY_SIZE

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_scl_hy_size Scale out Y size, only works when sw_scl_clip_en equal to 1.

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VPSS_SCALE_1C00_2800_2C00_SCALE_HC_SIZE

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_scl_hc_size Scale out UV size, only works when sw_scl_clip_en equal to 1.

VPSS_SCALE_1C00_2800_2C00_SCALE_HY_OFFS_MI

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	sw_scl_hy_offs_mi The offset of first Y pixel in 128bit, which range from 0~15.

VPSS_SCALE_1C00_2800_2C00_SCALE_HC_OFFS_MI

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	sw_scl_hc_offs_mi The offset of first UV pixel in 128bit, which range from 0~15.

VPSS_SCALE_1C00_2800_2C00_SCALE_IN_CROP_OFFSET

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	sw_scl_in_hc_offs Scale in UV data cut some pixels if needed, only works when sw_scl_in_clip_en is effect.
3:0	RW	0x0	sw_scl_in_hy_offs Scale in Y data cut some pixels if needed, only works when sw_scl_in_clip_en is effect.

VPSS_SCALE_1C00_2800_2C00_SCALE_CTRL_SHD

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RO	0x0	sw_scl_in_clip_en_shd Use for 8K 1'b0: Disable scale in clip 1'b1: Enable scale in clip
13	RO	0x0	sw_scl_clip_en_shd Use for 8K 1'b0: Disable scale out clip 1'b1: Enable scale out clip
12:4	RO	0x000	reserved
3	RO	0x0	sw_scale_vc_en_shd 1'b0: Bypass vertical chrominance scaling unit 1'b1: Enable vertical chrominance scaling unit
2	RO	0x0	sw_scale_vy_en_shd 1'b0: Bypass vertical luminance scaling unit 1'b1: Enable vertical luminance scaling unit
1	RO	0x0	sw_scale_hc_en_shd 1'b0: Bypass horizontal chrominance scaling unit 1'b1: Enable horizontal chrominance scaling unit

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Bit	Attr	Reset Value	Description
0	RO	0x0	sw_scale_hy_en_shd 1'b0: Bypass horizontal luminance scaling unit 1'b1: Enable horizontal luminance scaling unit

VPSS_SCALE_1C00_2800_2C00_SCALE_SRC_SIZE_SHD

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	sw_scale_src_height_shd Scale height of source (input)
15:14	RO	0x0	reserved
13:0	RO	0x0000	sw_scale_src_width_shd Scale width of source (input)

VPSS_SCALE_1C00_2800_2C00_SCALE_DST_SIZE_SHD

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	sw_scale_dst_height_shd Scale height of destination(output)
15:14	RO	0x0	reserved
13:0	RO	0x0000	sw_scale_dst_width_shd Scale width of destination (output)

VPSS_SCALE_1C00_2800_2C00_SCALE_HY_FAC_SHD

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	sw_scale_hy_fac_shd This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: (width_in - 1) / (width_out - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^12).

VPSS_SCALE_1C00_2800_2C00_SCALE_HC_FAC_SHD

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	sw_scale_hc_fac_shd This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: ((width_in / 2) - 1) / ((width_out / 2) - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^12).

VPSS_SCALE_1C00_2800_2C00_SCALE_VY_FAC_SHD

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17:0	RO	0x00000	sw_scale_vy_fac_shd This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: (height_in - 1) / (height_out - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^12).

VPSS_SCALE_1C00_2800_2C00_SCALE_VC_FAC_SHD

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	sw_scale_vc_fac_shd This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: If sw_scl_yuv420_real_en = 1, ((src_height / 2) - 1) / ((dst_height / 2) - 1)) = scale elseif sw_scl_422to420_en = 1, (src_height - 1) / ((dst_height / 2) - 1)) = scale Else (src_height - 1) / (dst_height - 1)) = scale The value of the sw_scale_vc_fac register then has to be int(scale * 2^12).

VPSS_SCALE_1C00_2800_2C00_SCALE_HY_OFFS_SHD

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	sw_scale_hy_offs_shd This register is set to the horizontal luminance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

VPSS_SCALE_1C00_2800_2C00_SCALE_HC_OFFS_SHD

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	sw_scale_hc_offs_shd This register is set to the horizontal chrominance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

VPSS_SCALE_1C00_2800_2C00_SCALE_VY_OFFS_SHD

Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	sw_scale_vy_offs_shd This register is set to the vertical luminance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

VPSS_SCALE_1C00_2800_2C00_SCALE_VC_OFFS_SHD

Address: **Operational Base** + offset (0x00AC)

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Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	sw_scale_vc_offs_shd This register is set to the vertical chrominance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

VPSS_SCALE_1C00_2800_2C00_SCALE_HY_SIZE_SHD

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_scl_hy_size_shd Scale out Y size shadow signal

VPSS_SCALE_1C00_2800_2C00_SCALE_HC_SIZE_SHD

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_scl_hc_size_shd Scale out UV size, only works when sw_scl_clip_en equal to 1.

VPSS_SCALE_1C00_2800_2C00_SCALE_HY_OFFS_MI_SHD

Address: **Operational Base** + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	sw_scl_hy_offs_mi_shd Shadow signal of sw_scl_hy_offs_mi

VPSS_SCALE_1C00_2800_2C00_SCALE_HC_OFFS_MI_SHD

Address: **Operational Base** + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	sw_scl_hc_offs_mi_shd Shadow signal of sw_scl_hy_offs_mi

VPSS_SCALE_1C00_2800_2C00_SCALE_IN_CROP_OFFSET_SHD

Address: **Operational Base** + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RO	0x0	sw_scl_in_hc_offs_shd Scale in UV data cut some pixels if needed, only works when sw_scl_in_clip_en is effect.
3:0	RO	0x0	sw_scl_in_hy_offs_shd Scale in Y data cut some pixels if needed, only works when sw_scl_in_clip_en is effect.

3.4.2.6 Aspective Ratio

ASPT_RATIO_1900_2500_2900_2D00_RATIO_CTRL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_aspect_ratio_en_shd Shadow register
30:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_aspect_ratio_en Aspective ratio enable for image edge filling. 1'b0: Bypass ratio unit 1'b1: Enable ratio unit

ASPT_RATIO_1900_2500_2900_2D00_RATIO_UPDATE

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x1	sys_cfg_gen_upd 1'b1: Automatic register update at frame end enabled 1'b0: Automatic register update at frame end disabled
4	W1C	0x0	sys_cfg_force_upd 1'b0: Nothing happens 1'b1: Update shadow registers
3:0	RO	0x0	reserved

ASPT_RATIO_1900_2500_2900_2D00_RATIO_ACT_SIZE

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_act_height Actual image height (input)
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_act_width Actual image width (input)

ASPT_RATIO_1900_2500_2900_2D00_RATIO_VIR_SIZE

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_act_height Virtual image height (output)
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_act_width Virtual image width (output)

ASPT_RATIO_1900_2500_2900_2D00_RATIO_OFFS

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_v_offs This register is set to the vertical offset (0~1) for actual image.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_h_offs This register is set to the horizontal offset (0~1) for actual image.

ASPT_RATIO_1900_2500_2900_2D00_RATIO_COLOR

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	sw_v_color Component v background color.
23:16	RW	0x80	sw_u_color Component u background color.

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_y_color Component y background color.

ASPT_RATIO_1900_2500_2900_2D00_RATIO_ACT_SIZE_SHD

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	W1C	0x0000	sw_act_height_shd Actual image height (input)
15:14	RO	0x0	reserved
13:0	W1C	0x0000	sw_act_width_shd Actual image width (input)

ASPT_RATIO_1900_2500_2900_2D00_RATIO_VIR_SIZE_SHD

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	sw_act_height_shd Virtual image height (output)
15:14	RO	0x0	reserved
13:0	RO	0x0000	sw_act_width_shd Virtual image width (output)

ASPT_RATIO_1900_2500_2900_2D00_RATIO_OFFS_SHD

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	sw_v_offs_shd This register is set to the vertical offset (0~1) for actual image.
15:14	RO	0x0	reserved
13:0	RO	0x0000	sw_h_offs_shd This register is set to the horizontal offset (0~1) for actual image.

ASPT_RATIO_1900_2500_2900_2D00_RATIO_COLOR_SHD

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	sw_v_color_shd Component v background color.
23:16	RO	0x00	sw_u_color_shd Component u background color.
15:8	RO	0x00	reserved
7:0	RO	0x00	sw_y_color_shd Component y background color.

3.4.2.7 MI

VPSS_MI_3000_MI_WR_CTRL

Address: Operational Base(0x27C33000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mi_new_wr_burst_dis 1'b0: Self-adaption enable 1'b1: Self-adaption disable

Bit	Attr	Reset Value	Description
30	RW	0x0	sw_path_sel_fix_dis MI path select fix disable 1'b0: enable 1'b1: disable If sw_path_sel_fix_dis is 1, maybe MI path enable input shadow update fail when When auto-update and self-update are used together.
29	RW	0x0	sw_mi_wr_align_dis 1'b0: channel burst align 1'b1: Disable channel write burst align
28	RW	0x0	sw_mi_wr_group_fix Fix group mode, backdoor
27	RW	0x0	sw_mi_wr_id_poll_dis MI write axi-id polling disable, backdoor
26	W1C	0x0	sys_mi_wr_id_poll_clr MI write axi-id polling clear counter
25	RW	0x0	sw_mi_wr_glb_en_dis 1'b0: Gloal channel enable used, for mi write 1'b0: MI channel enable used, for mi write
24	RW	0x0	sw_mi_wr_isp_prior_dis Disable raising ISP write channel priority for online mode2
23:22	RW	0x2	sw_mi_wr_burst_len_chrom_org Burst length for Cb or Cr data affecting write port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: Reserved Ignored if 8- or 16-beat bursts are not supported. If rotation is active, then only 4-beat bursts will be generated in self path, regardless of the setting here.
21:20	RW	0x2	sw_mi_wr_burst_len_lum_org Burst length for Y data affecting write port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: Reserved Ignored if 8- or 16-beat bursts are not supported.
19:18	RO	0x0	reserved
17:16	RW	0x2	sw_mi_wr_group_mode Group mode for yuv data affecting DMA write port. 2'b00: BurstN*4 2'b01: BurstN*3 2'b10: BurstN*2 2'b11: BurstN*1
15	RW	0x0	sw_mi_wr_stride_cfg_dis MI write virtual stride adapt-configure disable 1'b0: virtual stride byte unit 1'b1: virtual stride pixel unit
14:12	RO	0x0	reserved
11:10	RW	0x0	sw_mi_wr_tile_sel_shd MI write tile channel select shadow register. 2'b00: no tile write 2'b01: chn0 tile write 2'b10: chn1 tile write 2'b11: reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	sw_mi_wr_tile_sel MI write tile channel select. 2'b00: no tile write 2'b01: chn0 tile write 2'b10: chn1 tile write 2'b11: reserved
7:6	RO	0x0	reserved
5	RW	0x0	sw_mi_wr_uv_swap Enable uv swap function YVYU mode: 1'b0: YVYU (U,LSB) 1'b1: YUYV (V,LSB) YUV-SP mode: 1'b0: VU (U,LSB) 1'b1: UV (V,LSB)
4	RW	0x1	sw_mi_wr_init_base_en Enables updating of the base address and buffer size shadow registers to the programmed register initial values.
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_WR_INIT

Address: Operational Base(0x27C33000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sw_itself_force_pro_dis Itself force update protection disable
30:8	RO	0x000000	reserved
7	W1C	0x0	sys_chn3self_force_upd Force update of configuration registers for chn3 DMA write. Note: If sw_itself_force_pro_dis = 0, sys_chn3self_force_upd is not valid during chn3 working period.
6	W1C	0x0	sys_chn2self_force_upd Force update of configuration registers for chn2 DMA write. Note: If sw_itself_force_pro_dis = 0, sys_chn2self_force_upd is not valid during chn2 working period.
5	W1C	0x0	sys_chn1self_force_upd Force update of configuration registers for chn1 DMA write. Note: If sw_itself_force_pro_dis = 0, sys_chn1self_force_upd is not valid during chn1 working period.
4	W1C	0x0	sys_chn0self_force_upd Force update of configuration registers for chn0 DMA write. Note: If sw_itself_force_pro_dis = 0, sys_chn0self_force_upd is not valid during chn0 working period.
3:2	RO	0x0	reserved
1	RW	0x0	sw_mi_update_mode 1'b0: Old mode 1'b1: New mode, all path will update when frame_end In new mode, all path registers of MI will be updated at right time. Note: default 0.
0	W1C	0x0	sys_mi_force_update Forced configuration update. Leads to an immediate update of the shadow registers. Depending on the two initial enable bits in the MI_CTRL register (init_offset_en and init_base_en) the offset counter, base address and buffer size shadow registers are also updated

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VPSS_MI_3000_MI_WR_WRAP_CTRL

Address: Operational Base(0x27C33000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	sw_chn3_wr_frmend_upd_dis Frame end address shadow update disable of chn3
26	RW	0x0	sw_chn2_wr_frmend_upd_dis Frame end address shadow update disable of chn2
25	RW	0x0	sw_chn1_wr_frmend_upd_dis Frame end address shadow update disable of chn1
24	RW	0x0	sw_chn0_wr_frmend_upd_dis Frame end address shadow update disable of chn0
23:12	RO	0x000	reserved
11	RW	0x0	sw_chn3_dynamic_upd_addr Wrap dynamic address update enable of chn3
10	RW	0x0	sw_chn2_dynamic_upd_addr Wrap dynamic address update enable of chn2
9	RW	0x0	sw_chn1_dynamic_upd_addr Wrap dynamic address update enable of chn1
8	RW	0x0	sw_chn0_dynamic_upd_addr Wrap dynamic address update enable of chn0
7:4	RO	0x0	reserved
3	RW	0x1	sw_chn3_wr_init_offset_en Enables updating of the offset counters shadow registers for chn3 to the programmed register initial values.
2	RW	0x1	sw_chn2_wr_init_offset_en Enables updating of the offset counters shadow registers for chn2 to the programmed register initial values.
1	RW	0x1	sw_chn1_wr_init_offset_en Enables updating of the offset counters shadow registers for chn1 to the programmed register initial values.
0	RW	0x1	sw_chn0_wr_init_offset_en Enables updating of the offset counters shadow registers for chn0 to the programmed register initial values.

VPSS_MI_3000_MI_WR_VFLIP_CTRL

Address: Operational Base(0x27C33000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RO	0x0	sw_chn3_wr_v_flip_shd Vertical flipping of bypass picture. For Y component the line length in 4:2:x planar mode must be a multiple of 16. 1'b1: Enabled 1'b0: Disabled Note: - Readback is shadow register. - If sw_chn3_wr_v_flip = 1, need to configure sw_chn3_wr_y_pic_size

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Bit	Attr	Reset Value	Description
18	RO	0x0	sw_chn2_wr_v_flip_shd Vertical flipping of bypass picture. For Y component the line length in 4:2:x planar mode must be a multiple of 16. 1'b1: Enabled 1'b0: Disabled Note: - Readback is shadow register. - If sw_chn2_wr_v_flip = 1, need to configure sw_chn2_wr_y_pic_size
17	RO	0x0	sw_chn1_wr_v_flip_shd Vertical flipping of mainchn1 picture. For Y component the line length in 4:2:x planar mode must be a multiple of 16. 1'b1: Enabled 1'b0: Disabled Note: - Readback is shadow register. - If sw_chn1_wr_v_flip = 1, need to configure sw_chn1_wr_y_pic_size
16	RO	0x0	sw_chn0_wr_v_flip_shd Vertical flipping of chn0 picture. For Y component the line length in 4:2:x planar mode must be a multiple of 16. 1'b1: Enabled 1'b0: Disabled Note: - Readback is shadow register. - If sw_chn0_wr_v_flip = 1, need to configure sw_chn0_wr_y_pic_size
15:4	RO	0x000	reserved
3	RW	0x0	sw_chn3_wr_v_flip Vertical flipping of bypass picture. For Y component the line length in 4:2:x planar mode must be a multiple of 16. 1'b1: Enabled 1'b0: Disabled Note: - Readback is shadow register. - If sw_chn3_wr_v_flip = 1, need to configure sw_chn3_wr_y_pic_size
2	RW	0x0	sw_chn2_wr_v_flip Vertical flipping of bypass picture. For Y component the line length in 4:2:x planar mode must be a multiple of 16. 1'b1: Enabled 1'b0: Disabled Note: - Readback is shadow register. - If sw_chn2_wr_v_flip = 1, need to configure sw_chn2_wr_y_pic_size

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Bit	Attr	Reset Value	Description
1	RW	0x0	sw_chn1_wr_v_flip Vertical flipping of mainchn1 picture. For Y component the line length in 4:2:x planar mode must be a multiple of 16. 1'b1: Enabled 1'b0: Disabled Note: - Readback is shadow register. - If sw_chn1_wr_v_flip = 1, need to configure sw_chn1_wr_y_pic_size
0	RW	0x0	sw_chn0_wr_v_flip Vertical flipping of chn0 picture. For Y component the line length in 4:2:x planar mode must be a multiple of 16. 1'b1: Enabled 1'b0: Disabled Note: - Readback is shadow register. - If sw_chn0_wr_v_flip = 1, need to configure sw_chn0_wr_y_pic_size

VPSS_MI_3000_MI_HURRY_CTRL

Address: Operational Base(0x27C33000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	sw_noc_hurry_value 3'b000: The Low priority to interconnect ..... 3'b111: The first High priority to interconnect

VPSS_MI_3000_MI_ARQOS_CTRL

Address: Operational Base(0x27C33000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:12	RW	0x0	sw_ar_yuv_qos1 Register of yuv read qos to interconnect, configure 0 to 7, default 0
11	RO	0x0	reserved
10:8	RW	0x0	sw_ar_yuv_qos2 Register of yuv read qos to interconnect, configure 0 to 7, default 0
7	RO	0x0	reserved
6:4	RW	0x3	sw_ar_mmu_qos3 MMU write qos to interconnect, configure 0 to 7, default 3
3:1	RO	0x0	reserved
0	RW	0x0	sw_ar_qos_en All bus channel AXI read qos to interconnect, enable

VPSS_MI_3000_MI_AWQOS_CTRL

Address: Operational Base(0x27C33000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:12	RW	0x0	sw_aw_yuv_qos1 Register of yuv write qos to interconnect, configure 0 to 7, default 0

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Bit	Attr	Reset Value	Description
11	RO	0x0	reserved
10:8	RW	0x0	sw_aw_yuv_qos2 Register of yuv write qos to interconnect, configure 0 to 7, default 0
7:1	RO	0x00	reserved
0	W1C	0x0	sw_aw_qos_en All bus channel AXI read qos to interconnect, enable

VPSS_MI_3000_MI_IMSC

Address: Operational Base(0x27C33000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31	RW	0x0	stat_all_frame_end Mask all picture end of frame interrupt
30	RW	0x0	isp2chn_frame_end Mask isp all picture end of frame interrupt for online mode2
29	RO	0x0	reserved
28	RW	0x0	vpss_bus_err Mask bit for axi bus error interrupt
27:16	RO	0x000	reserved
15	RW	0x0	stat_wrap_chn3_cb Mask bit for chn3 picture Cb address wrap interrupt
14	RW	0x0	stat_wrap_chn3_y Mask bit for chn3 picture Y address wrap interrupt
13	RW	0x0	stat_wrap_chn2_cb Mask bit for chn2 picture Cb address wrap interrupt
12	RW	0x0	stat_wrap_chn2_y Mask bit for chn2 picture Y address wrap interrupt
11	RW	0x0	stat_wrap_chn1_cb Mask bit for chn1 picture Cb address wrap interrupt
10	RW	0x0	stat_wrap_chn1_y Mask bit for chn1 picture Y address wrap interrupt
9	RW	0x0	stat_wrap_chn0_cb Mask bit for chn0 picture Cb address wrap interrupt
8	RW	0x0	stat_wrap_chn0_y Mask bit for chn0 picture Y address wrap interrupt
7:5	RO	0x0	reserved
4	RW	0x0	stat_read_frame_end Mask dma read picture end of frame interrupt
3	RW	0x0	stat_chn3_frame_end Mask chn3 picture end of frame interrupt
2	RW	0x0	stat_chn2_frame_end Mask chn2 write end of frame interrupt
1	RW	0x0	stat_chn1_frame_end Mask chn1 picture end of frame interrupt
0	RW	0x0	stat_chn0_frame_end Mask chn0 picture end of frame interrupt

VPSS_MI_3000_MI_RIS

Address: Operational Base(0x27C33000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31	RO	0x0	stat_all_frame_end Raw status of all picture end of frame interrupt
30	RO	0x0	isp2chn_frame_end Raw status of isp all picture end of frame interrupt for online mode2

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Bit	Attr	Reset Value	Description
29	RO	0x0	reserved
28	RO	0x0	vpss_bus_err Raw status of axi bus error interrupt
27:16	RO	0x000	reserved
15	RO	0x0	stat_wrap_chn3_cb Raw status of chn3 picture Cb address wrap interrupt
14	RO	0x0	stat_wrap_chn3_y Raw status of chn3 picture Y address wrap interrupt
13	RO	0x0	stat_wrap_chn2_cb Raw status of chn2 picture Cb address wrap interrupt
12	RO	0x0	stat_wrap_chn2_y Raw status of chn2 picture Y address wrap interrupt
11	RO	0x0	stat_wrap_chn1_cb Raw status of chn1 picture Cb address wrap interrupt
10	RO	0x0	stat_wrap_chn1_y Raw status of chn1 picture Y address wrap interrupt
9	RO	0x0	stat_wrap_chn0_cb Raw status of chn0 picture Cb address wrap interrupt
8	RO	0x0	stat_wrap_chn0_y Raw status of chn0 picture Y address wrap interrupt
7:5	RO	0x0	reserved
4	RO	0x0	stat_read_frame_end Raw status of dma read picture end of frame interrupt
3	RO	0x0	stat_chn3_frame_end Raw status of chn3 picture end of frame interrupt
2	RO	0x0	stat_chn2_frame_end Raw status of chn2 write end of frame interrupt
1	RO	0x0	stat_chn1_frame_end Raw status of chn1 picture end of frame interrupt
0	RO	0x0	stat_chn0_frame_end Raw status of chn0 picture end of frame interrupt

VPSS_MI_3000_MI_MIS

Address: Operational Base(0x27C33000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31	RO	0x0	stat_all_frame_end Masked status of all picture end of frame interrupt
30	RO	0x0	isp2chn_frame_end Masked status of isp all picture end of frame interrupt for online mode2
29	RO	0x0	reserved
28	RO	0x0	vpss_bus_err Masked status of axi bus error interrupt
27:16	RO	0x000	reserved
15	RO	0x0	stat_wrap_chn3_cb Masked status of chn3 picture Cb address wrap interrupt
14	RO	0x0	stat_wrap_chn3_y Masked status of chn3 picture Y address wrap interrupt
13	RO	0x0	stat_wrap_chn2_cb Masked status of chn2 picture Cb address wrap interrupt
12	RO	0x0	stat_wrap_chn2_y Masked status of chn2 picture Y address wrap interrupt
11	RO	0x0	stat_wrap_chn1_cb Masked status of chn1 picture Cb address wrap interrupt

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Bit	Attr	Reset Value	Description
10	RO	0x0	stat_wrap_chn1_y Masked status of chn1 picture Y address wrap interrupt
9	RO	0x0	stat_wrap_chn0_cb Masked status of chn0 picture Cb address wrap interrupt
8	RO	0x0	stat_wrap_chn0_y Masked status of chn0 picture Y address wrap interrupt
7:5	RO	0x0	reserved
4	RO	0x0	stat_read_frame_end Masked status of dma read picture end of frame interrupt
3	RO	0x0	stat_chn3_frame_end Masked status of chn3 picture end of frame interrupt
2	RO	0x0	stat_chn2_frame_end Masked status of chn2 write end of frame interrupt
1	RO	0x0	stat_chn1_frame_end Masked status of chn1 picture end of frame interrupt
0	RO	0x0	stat_chn0_frame_end Masked status of chn0 picture end of frame interrupt

VPSS_MI_3000_MI_ICR

Address: Operational Base(0x27C33000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31	W1C	0x0	stat_all_frame_end Clear all picture end of frame interrupt
30	W1C	0x0	isp2chn_frame_end Clear isp all picture end of frame interrupt for online mode2
29	RO	0x0	reserved
28	W1C	0x0	vpss_bus_err Clear axi bus error interrupt
27:16	RO	0x000	reserved
15	W1C	0x0	stat_wrap_chn3_cb Clear chn3 picture Cb address wrap interrupt
14	W1C	0x0	stat_wrap_chn3_y Clear chn3 picture Y address wrap interrupt
13	W1C	0x0	stat_wrap_chn2_cb Clear chn2 picture Cb address wrap interrupt
12	W1C	0x0	stat_wrap_chn2_y Clear chn2 picture Y address wrap interrupt
11	W1C	0x0	stat_wrap_chn1_cb Clear chn1 picture Cb address wrap interrupt
10	W1C	0x0	stat_wrap_chn1_y Clear chn1 picture Y address wrap interrupt
9	W1C	0x0	stat_wrap_chn0_cb Clear chn0 picture Cb address wrap interrupt
8	W1C	0x0	stat_wrap_chn0_y Clear chn0 picture Y address wrap interrupt
7:5	RO	0x0	reserved
4	W1C	0x0	stat_read_frame_end Clear dma read picture end of frame interrupt
3	W1C	0x0	stat_chn3_frame_end Clear chn3 picture end of frame interrupt
2	W1C	0x0	stat_chn2_frame_end Clear chn2 write end of frame interrupt
1	W1C	0x0	stat_chn1_frame_end Clear chn1 picture end of frame interrupt

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Bit	Attr	Reset Value	Description
0	W1 C	0x0	stat_chn0_frame_end Clear chn0 picture end of frame interrupt

VPSS_MI_3000_MI_ISR

Address: Operational Base(0x27C33000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31	W1 C	0x0	stat_all_frame_end Set all picture end of frame interrupt
30	W1 C	0x0	isp2chn_frame_end Set isp all picture end of frame interrupt for online mode2
29	RO	0x0	reserved
28	W1 C	0x0	vpss_bus_err Set axi bus error interrupt
27:16	RO	0x000	reserved
15	W1 C	0x0	stat_wrap_chn3_cb Set chn3 picture Cb address wrap interrupt
14	W1 C	0x0	stat_wrap_chn3_y Set chn3 picture Y address wrap interrupt
13	W1 C	0x0	stat_wrap_chn2_cb Set chn2 picture Cb address wrap interrupt
12	W1 C	0x0	stat_wrap_chn2_y Set chn2 picture Y address wrap interrupt
11	W1 C	0x0	stat_wrap_chn1_cb Set chn1 picture Cb address wrap interrupt
10	W1 C	0x0	stat_wrap_chn1_y Set chn1 picture Y address wrap interrupt
9	W1 C	0x0	stat_wrap_chn0_cb Set chn0 picture Cb address wrap interrupt
8	W1 C	0x0	stat_wrap_chn0_y Set chn0 picture Y address wrap interrupt
7:5	RO	0x0	reserved
4	W1 C	0x0	stat_read_frame_end Set dma read picture end of frame interrupt
3	W1 C	0x0	stat_chn3_frame_end Set chn3 picture end of frame interrupt
2	W1 C	0x0	stat_chn2_frame_end Set chn2 write end of frame interrupt
1	W1 C	0x0	stat_chn1_frame_end Set chn1 picture end of frame interrupt
0	W1 C	0x0	stat_chn0_frame_end Set chn0 picture end of frame interrupt

VPSS_MI_3000_MI_STATUS

Address: Operational Base(0x27C33000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	stat_chn3_cb_fifo_full FIFO full flag of Cb FIFO in chn3 asserted since last clear
6	RO	0x0	stat_chn3_y_fifo_full FIFO full flag of Y FIFO in chn3 asserted since last clear
5	RO	0x0	stat_chn2_cb_fifo_full FIFO full flag of Cb FIFO in bypass path asserted since last clear
4	RO	0x0	stat_chn2_y_fifo_full FIFO full flag of Y FIFO in bypass path asserted since last clear

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Bit	Attr	Reset Value	Description
3	RO	0x0	stat_chn1_cb_fifo_full FIFO full flag of Cb FIFO in self path asserted since last clear
2	RO	0x0	stat_chn1_y_fifo_full FIFO full flag of Y FIFO in self path asserted since last clear
1	RO	0x0	stat_chn0_cb_fifo_full FIFO full flag of Cb FIFO in chn0 asserted since last clear
0	RO	0x0	stat_chn0_y_fifo_full FIFO full flag of Y FIFO in chn0 asserted since last clear

VPSS_MI_3000_MI_STATUS_CLR

Address: Operational Base(0x27C33000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	WO	0x0	stat_chn3_cb_fifo_full Clear status of Cb FIFO full flag in bypass path
6	WO	0x0	stat_chn3_y_fifo_full Clear status of Y FIFO full flag in bypass path
5	WO	0x0	stat_chn2_cb_fifo_full Clear status of Cb FIFO full flag in bypass path
4	WO	0x0	stat_chn2_y_fifo_full Clear status of Y FIFO full flag in bypass path
3	WO	0x0	stat_chn1_cb_fifo_full Clear status of Cb FIFO full flag in self path
2	WO	0x0	stat_chn1_y_fifo_full Clear status of Y FIFO full flag in self path
1	WO	0x0	stat_chn0_cb_fifo_full Clear status of Cb FIFO full flag in chn0
0	WO	0x0	stat_chn0_y_fifo_full Clear status of Y FIFO full flag in chn0

VPSS_MI_3000_MI_RD_CTRL

Address: Operational Base(0x27C33000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mi_new_rd_burst_dis 1'b0: Self-adaption enable 1'b1: Self-adaption disable
30	RW	0x0	sw_mi_rd_old Old-mi read. 1'b0: mi read effect burst length 1'b1: mi read waste bandwidth
29	RO	0x0	reserved
28	RW	0x0	sw_mi_rd_r2y_bypass VPSS read rgb bypass enable (no csc)
27	RW	0x0	sw_mi_rd_fbcd_opt_dis RKFBCD64x4 payload burst DDR align optimization disable
26	RW	0x0	sw_mi_rd_fbcd_yuv444_en RKFBCD64x4 yuv444 enable. Input yuv444, output yuv422. Note: If sw_mi_rd_fbcd_yuv444_en = 1, must config sw_mi_rd_input_format = 2 (yuv422)
25:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:20	RW	0x2	sw_mi_rd_burst_len Burst length for Y data affecting DMA read port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: Reserved Ignored if 8- or 16-beat bursts are not supported
19:18	RO	0x0	reserved
17:16	RW	0x0	sw_mi_rd_group_mode Group mode for yuv data affecting DMA read port in line mode. 2'b00: BurstN*4 2'b01: BurstN*3 2'b10: BurstN*2 2'b11: BurstN*1
15:14	RW	0x0	sw_mi_rd_act_yoff DMA read verticaloffset for tile4x4 2'b00: no offset 2'b01: reserved 2'b10: vertical 2pixel offset 2'b11:reserved Note: Only support tile4x4 read.
13:12	RW	0x0	sw_mi_rd_act_xoff DMA read horizontal offset for tile4x4 2'b00: no offset 2'b01: reserved 2'b10: horizontal 2pixel offset 2'b11:reserved Note: Only support tile4x4 read.
11:10	RW	0x0	sw_mi_rd_rot_mode DMA read rotation mode for tile4x4 2'b00: normal mode 2'b01: rotation 90 2'b10: rotation 180 2'b11: rotation 270 Note: Only support tile4x4 read rotation. Constraint: If read yuv422 tile4x4, rotate to yuv420 (yuv422 in, yuv420 out for rotation).
9:8	RW	0x0	sw_mi_rd_mode DMA read mode 2'b00: line mode 2'b01: tile4x4 mode 2'b10: rkfbcd64x4 mode 2'b11: reserved Note: If sw_mi_rd_act_xoff = 0, sw_mi_rd_y_width need 4pixel align in tile4x4 mode. If sw_mi_rd_act_yoff = 0, sw_mi_rd_y_height need 4pixel align in tile4x4 mode.
7	RW	0x0	sw_mi_rd_r2y_uv_sel UV selection for yuv444 to yuv422 1'b0: even used 1'b1: odd used
6	RW	0x0	sw_mi_rd_alpha_swap Enable alpha swap function
5	RW	0x0	sw_mi_rd_rb_swap Enable rb swap function
4	RW	0x0	sw_mi_rd_uv_swap Enable uv swap function

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Bit	Attr	Reset Value	Description
3	RO	0x0	reserved
2:0	RW	0x2	sw_mi_rd_input_format Defines how YCbCr or RGB picture data is read from memory. 3'b000: Reserved 3'b001: Semi planar, for YCbCr 4:2:0 3'b010: Semi planar, for YCbCr 4:2:2 3'b100: BGR565 3'b110: ABGR888 3'b111: BGR888 others: Reserved Note: R is LSB in BGR.

VPSS_MI_3000_MI_RD_INIT

Address: Operational Base(0x27C33000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	W1C	0x0	sys_mi_rd_force_upd 1'b0: Nothing happens 1'b1: Update shadow registers
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_RD_START

Address: Operational Base(0x27C33000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	sys_mi_rd_start_pre Enables DMA access.

VPSS_MI_3000_MI_RD_Y_BASE

Address: Operational Base(0x27C33000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mi_rd_y_base Image start address of the y component, 16byte align

VPSS_MI_3000_MI_RD_Y_WIDTH

Address: Operational Base(0x27C33000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_mi_rd_y_width Image width of the Y component in pixel. Note: If semi planar yuv format, the hardware automatically calculate the uv width. Online mode0 and mode1 reuse this width.

VPSS_MI_3000_MI_RD_Y_HEIGHT

Address: Operational Base(0x27C33000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mi_rd_y_height Image height of the Y component in pixel. Note: If semi planar yuv format, the hardware automatically calculate the uv height. Online mode0 and mode1 reuse this height.

VPSS_MI_3000_MI_RD_Y_STRIDE

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Address: Operational Base(0x27C33000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_mi_rd_y_stride Line stride of the Y component of the original image in memory For an uncropped image, where lines follow each other without offset (no line stride), line length must match image width.

VPSS_MI_3000_MI_RD_C_BASE

Address: Operational Base(0x27C33000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mi_rd_c_base Image start address of the UV component , 16byte align

VPSS_MI_3000_MI_RD_Y_BASE_SHD

Address: Operational Base(0x27C33000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mi_rd_y_base_shd Image start address of the y component, 16byte align

VPSS_MI_3000_MI_RD_C_BASE_SHD

Address: Operational Base(0x27C33000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mi_rd_c_base_shd Image start address of the UV component, 16byte align

VPSS_MI_3000_MI_RD_Y_WIDTH_SHD

Address: Operational Base(0x27C33000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_mi_rd_y_width_shd Image width of the Y component in pixel. Note: If semi planar yuv format, the hardware automatically calculate the uv width. Online mode0 and mode1 reuse this width.

VPSS_MI_3000_MI_RD_Y_HEIGHT_SHD

Address: Operational Base(0x27C33000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mi_rd_y_height_shd Image height of the Y component in pixel. Note: If semi planar yuv format, the hardware automatically calculate the uv height. Online mode0 and mode1 reuse this height.

VPSS_MI_3000_AXI_CFG_RD_CTRL

Address: Operational Base(0x27C33000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31	RO	0x1	axi_cfg_rd_status AXI configure read status. 1'b1: axi configure done. 1'b0: auto-start axi configure at mi all_frame_end or vpss input frame end

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Bit	Attr	Reset Value	Description
30	RO	0x0	ro_axi_cfg_might_fail AXI configure might fail. 1'b1: ISP2VPSS online is valid in the period of axi configure, maybe configure fail.
29:8	RO	0x000000	reserved
7	RW	0x0	sw_axi_cfg_rd_dis AXI configure read disable.
6:5	RO	0x0	reserved
4	W1C	0x1	sys_axi_cfg_rd_clear AXI configure read clear to pull down axi_cfg_rd_status for next frame auto axi configure.
3:2	RO	0x0	reserved
1	RW	0x0	sw_axi_cfg_rd_st_mode AXI configure read start mode. 1'b0: aoto-start axi configure at mi all_frame_end when axi_cfg_rd_status is 0. 1'b1: start axi configure at sys_axi_fg_rd_st is 1.
0	W1C	0x0	sys_axi_cfg_rd_st AXI configure read start.

VPSS_MI_3000_AXI_CFG_RD_BASE

Address: Operational Base(0x27C33000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:4	W1C	0x0000000	sw_axi_cfg_rd_base Base address of axi configure read data ring buffer.
3:0	RO	0x0	reserved

VPSS_MI_3000_AXI_CFG_RD_H_WSIZE

Address: Operational Base(0x27C33000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	W1C	0x0000	sw_axi_cfg_wsize sw_axi_conf_wsize

VPSS_MI_3000_AXI_CFG_RD_V_SIZE

Address: Operational Base(0x27C33000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	W1C	0x0001	sw_axi_cfg_vsize AXI configure size of vertical direction

VPSS_MI_3000_MI_RD_R2Y_COE00

Address: Operational Base(0x27C33000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0001	sw_mi_rd_r2y_coe_00 1bit signed+2bit integer+10bit float factor Y: sw_mi_rd_r2y_coe_00*R + sw_mi_rd_r2y_coe_01*G + sw_mi_rd_r2y_coe_02*B + sw_mi_rd_r2y_coe_off0 Note: initial value is bt709-limit

VPSS_MI_3000_MI_RD_R2Y_COE01

Address: Operational Base(0x27C33000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0001	sw_mi_rd_r2y_coe_01 1bit signed+2bit integer+10bit float factor Y: sw_mi_rd_r2y_coe_00*R + sw_mi_rd_r2y_coe_01*G + sw_mi_rd_r2y_coe_02*B + sw_mi_rd_r2y_coe_off0 Note: initial value is bt709-limit

VPSS_MI_3000_MI_RD_R2Y_COE02

Address: Operational Base(0x27C33000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0001	sw_mi_rd_r2y_coe_02 1bit signed+2bit integer+10bit float factor Y: sw_mi_rd_r2y_coe_00*R + sw_mi_rd_r2y_coe_01*G + sw_mi_rd_r2y_coe_02*B + sw_mi_rd_r2y_coe_off0 Note: initial value is bt709-limit

VPSS_MI_3000_MI_RD_R2Y_OFF0

Address: Operational Base(0x27C33000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0001	sw_mi_rd_r2y_coe_off0 1bit signed+10bit integer+10bit float factor Y: sw_mi_rd_r2y_coe_00*R + sw_mi_rd_r2y_coe_01*G + sw_mi_rd_r2y_coe_02*B + sw_mi_rd_r2y_coe_off0 Note: initial value is bt709-limit

VPSS_MI_3000_MI_RD_R2Y_COE10

Address: Operational Base(0x27C33000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0001	sw_mi_rd_r2y_coe_10 1bit signed+2bit integer+10bit float factor U: sw_mi_rd_r2y_coe_10*R + sw_mi_rd_r2y_coe_11*G + sw_mi_rd_r2y_coe_12*B + sw_mi_rd_r2y_coe_off1 Note: initial value is bt709-limit

VPSS_MI_3000_MI_RD_R2Y_COE11

Address: Operational Base(0x27C33000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0001	sw_mi_rd_r2y_coe_11 1bit signed+2bit integer+10bit float factor U: sw_mi_rd_r2y_coe_10*R + sw_mi_rd_r2y_coe_11*G + sw_mi_rd_r2y_coe_12*B + sw_mi_rd_r2y_coe_off1 Note: initial value is bt709-limit

VPSS_MI_3000_MI_RD_R2Y_COE12

Address: Operational Base(0x27C33000) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0001	sw_mi_rd_r2y_coe_12 1bit signed+2bit integer+10bit float factor U: sw_mi_rd_r2y_coe_10*R + sw_mi_rd_r2y_coe_11*G + sw_mi_rd_r2y_coe_12*B + sw_mi_rd_r2y_coe_off1 Note: initial value is bt709-limit

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VPSS_MI_3000_MI_RD_R2Y_OFF1

Address: Operational Base(0x27C33000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0001	sw_mi_rd_r2y_coe_off1 1bit signed+10bit integer+10bit float factor U: sw_mi_rd_r2y_coe_10*R + sw_mi_rd_r2y_coe_11*G + sw_mi_rd_r2y_coe_12*B + sw_mi_rd_r2y_coe_off1 Note: initial value is bt709-limit

VPSS_MI_3000_MI_RD_R2Y_COE20

Address: Operational Base(0x27C33000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0001	sw_mi_rd_r2y_coe_20 1bit signed+2bit integer+10bit float factor V: sw_mi_rd_r2y_coe_20*R + sw_mi_rd_r2y_coe_21*G + sw_mi_rd_r2y_coe_22*B + sw_mi_rd_r2y_coe_off2 Note: initial value is bt709-limit

VPSS_MI_3000_MI_RD_R2Y_COE21

Address: Operational Base(0x27C33000) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0001	sw_mi_rd_r2y_coe_21 1bit signed+2bit integer+10bit float factor V: sw_mi_rd_r2y_coe_20*R + sw_mi_rd_r2y_coe_21*G + sw_mi_rd_r2y_coe_22*B + sw_mi_rd_r2y_coe_off2 Note: initial value is bt709-limit

VPSS_MI_3000_MI_RD_R2Y_COE22

Address: Operational Base(0x27C33000) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0001	sw_mi_rd_r2y_coe_22 1bit signed+2bit integer+10bit float factor V: sw_mi_rd_r2y_coe_20*R + sw_mi_rd_r2y_coe_21*G + sw_mi_rd_r2y_coe_22*B + sw_mi_rd_r2y_coe_off2 Note: initial value is bt709-limit

VPSS_MI_3000_MI_RD_R2Y_OFF2

Address: Operational Base(0x27C33000) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0001	sw_mi_rd_r2y_coe_off2 1bit signed+10bit integer+10bit float factor V: sw_mi_rd_r2y_coe_20*R + sw_mi_rd_r2y_coe_21*G + sw_mi_rd_r2y_coe_22*B + sw_mi_rd_r2y_coe_off2 Note: initial value is bt709-limit

VPSS_MI_3000_MI_CHN0_WR_CTRL

Address: Operational Base(0x27C33000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31	RO	0x0	mi_chn0_working MI channel0 working

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Bit	Attr	Reset Value	Description
30:11	RO	0x00000	reserved
10:8	RW	0x2	sw_chn0_wr_output_format Selects output format of chn0 picture. 3'b111: RGB 888 3'b110: ARGB 888 3'b100: RGB 565 3'b010: YCbCr 4:2:2 3'b001: YCbCr 4:2:0 3'b000: YCbCr 4:0:0 Note: - If sw_chn1_wr_v_flip = 1 and yuv420 format, need to configure sw_chn1_wr_output_format = 1 - If sw_mi_rd_r2y_bypass = 1 or sw_vpss_y2r_en = 1, MI output format need to be configured in RGB.
7:6	RO	0x0	reserved
5:4	RW	0x1	sw_chn0_wr_format Defines how YCbCr chn0 picture data is written to memory. 2'b00: Reserved 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved
3:2	RO	0x0	reserved
1	RW	0x1	sw_chn0_wr_auto_update Automatic update of configuration registers for chn0 at frame end. 1'b1: Enabled 1'b0: Disabled
0	RW	0x0	sw_chn0_wr_enable Channel0 write enable

VPSS_MI_3000_MI_CHN0_WR_Y_BASE

Address: Operational Base(0x27C33000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_chn0_wr_y_base Base address of chn0 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN0_WR_Y_SIZE

Address: Operational Base(0x27C33000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_chn0_wr_y_size Size of chn0 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN0_WR_Y_OFFS_CNT

Address: Operational Base(0x27C33000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_chn0_wr_y_offs_cnt Offset counter initial value of chn0 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN0_WR_Y_OFFS_CNT_START

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Address: Operational Base(0x27C33000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_chn0_wr_y_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (chn0 picture Y component)
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN0_WR_CB_BASE

Address: Operational Base(0x27C33000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_chn0_wr_cb_base Base address of chn0 picture uv component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN0_WR_CB_SIZE

Address: Operational Base(0x27C33000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_chn0_wr_cb_size Size of chn0 picture uv component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN0_WR_CB_OFFS_CNT

Address: Operational Base(0x27C33000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_chn0_wr_cb_offs_cnt Offset counter initial value of chn0 picture uv component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN0_WR_CB_OFFS_CNT_START

Address: Operational Base(0x27C33000) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_chn0_wr_cb_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (chn0 picture uv component)
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN0_WR_Y_STRIDE

Address: Operational Base(0x27C33000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_chn0_wr_y_stride Line stride of chn0 picture Y component in pixel, also known as line stride, 16byte align. If no line stride is used, line stride must match image width. If tile4x4 write, byte unit; else, pixel unit

VPSS_MI_3000_MI_CHN0_WR_Y_PIC_WIDTH

Address: Operational Base(0x27C33000) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
14:0	RW	0x0000	sw_chn0_wr_y_pic_width Image width of the main picture Y component or RGB picture in pixel. If no line stride is used but flipping required, the image width must be configured

VPSS_MI_3000_MI_CHN0_WR_Y_PIC_SIZE

Address: Operational Base(0x27C33000) + offset (0x023C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	sw_chn0_wr_y_pic_size Image size of the Y component in pixel which has to be the Y line length multiplied by the Y image height (chn0_y_llength * chn0_y_pic_height), used for flipping

VPSS_MI_3000_MI_CHN0_WR_CTRL_SHD

Address: Operational Base(0x27C33000) + offset (0x0250)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RO	0x2	sw_chn0_wr_output_format_shd Selects output format of chn0 picture. 3'b000: YCbCr 4:0:0 3'b001: YCbCr 4:2:0 3'b010: YCbCr 4:2:2 Others: Reserved Note: - If sw_chn0_wr_v_flip = 1 and yuv420 format, need to configure sw_chn0_wr_output_format = 1
7:6	RO	0x0	reserved
5:4	RO	0x1	sw_chn0_wr_format_shd Defines how YCbCr chn0 picture data is written to memory. 2'b00: Reserved 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved
3:1	RO	0x0	reserved
0	RO	0x0	stat_chn0_wr_enable_shd Channel0 write enable

VPSS_MI_3000_MI_CHN0_WR_Y_BASE_SHD

Address: Operational Base(0x27C33000) + offset (0x0260)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_chn0_wr_y_base_shd Base address of chn0 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN0_WR_Y_SIZE_SHD

Address: Operational Base(0x27C33000) + offset (0x0264)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_chn0_wr_y_size_shd Size of chn0 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN0_WR_Y_OFFS_CNT_SHD

Address: Operational Base(0x27C33000) + offset (0x0268)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_chn0_wr_y_offs_cnt_shd Current offset counter of chn0 picture Y component
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN0_WR_CB_BASE_SHD

Address: Operational Base(0x27C33000) + offset (0x0270)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_chn0_wr_cb_base_shd Base address of chn0 picture uv component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN0_WR_CB_SIZE_SHD

Address: Operational Base(0x27C33000) + offset (0x0274)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_chn0_wr_cb_size_shd Size of chn0 picture Cb component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN0_WR_CB_OFFS_CNT_SHD

Address: Operational Base(0x27C33000) + offset (0x0278)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_chn0_wr_cb_offs_cnt_shd Current offset counter of chn0 picture uv component ring buffer for address generation
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN0_WR_Y_END_ADDR

Address: Operational Base(0x27C33000) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_chn0_wr_y_end_addr Channel0 y frame end address readback, used for channel0 wrap debug

VPSS_MI_3000_MI_CHN0_WR_CB_END_ADDR

Address: Operational Base(0x27C33000) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_chn0_wr_cb_end_addr Channel0 uv frame end address readback, used for channel0 wrap debug

VPSS_MI_3000_MI_CHN0_WR_LINE_CNT

Address: Operational Base(0x27C33000) + offset (0x0288)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_chn0_wr_line_cnt Channel0 write line counter of of y component

VPSS_MI_3000_MI_CHN1_WR_CTRL

Address: Operational Base(0x27C33000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31	RO	0x0	mi_chn1_working MI channel1 working

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Bit	Attr	Reset Value	Description
30:29	RO	0x0	reserved
28	RW	0x1	sw_chn1_wr_y2r_bypass Channel1 YUV to RGB csc bypass. Note: If global y2r used (sw_mi_rd_r2y_bypass = 1 or sw_vpss_y2r_en = 1), sw_chn1_wr_y2r_bypass needs to be set 1.
27:11	RO	0x00000	reserved
10:8	RW	0x2	sw_chn1_wr_output_format Selects output format of chn1 picture. 3'b111: RGB 888 3'b110: ARGB 888 3'b100: RGB 565 3'b010: YCbCr 4:2:2 3'b001: YCbCr 4:2:0 3'b000: YCbCr 4:0:0 Note: -For ARGB888 format, Alpha is configurable. - If sw_chn1_wr_v_flip = 1 and yuv420 format, need to configure sw_chn1_wr_output_format = 1
7:6	RO	0x0	reserved
5:4	RW	0x1	sw_chn1_wr_format Defines how YCbCr chn1 picture data is written to memory. 2'b00: Reserved 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved
3	RO	0x0	reserved
2	RW	0x0	sw_chn1_wr_rb_swap Swap for rgb format
1	RW	0x1	sw_chn1_wr_auto_update Automatic update of configuration registers for chn1 at frame end. 1'b1: Enabled 1'b0: Disabled
0	RW	0x0	sw_chn1_wr_enable Channel1 write enable

VPSS_MI_3000_MI_CHN1_WR_Y_BASE

Address: Operational Base(0x27C33000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_chn1_wr_y_base Base address of chn1 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN1_WR_Y_SIZE

Address: Operational Base(0x27C33000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_chn1_wr_y_size Size of chn1 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN1_WR_Y_OFFS_CNT

Address: Operational Base(0x27C33000) + offset (0x0318)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_chn1_wr_y_offs_cnt Offset counter initial value of chn1 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN1_WR_Y_OFFS_CNT_START

Address: Operational Base(0x27C33000) + offset (0x031C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_chn1_wr_y_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (chn1 picture Y component)
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN1_WR_CB_BASE

Address: Operational Base(0x27C33000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_chn1_wr_cb_base Base address of chn1 picture uv component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN1_WR_CB_SIZE

Address: Operational Base(0x27C33000) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_chn1_wr_cb_size Size of chn1 picture uv component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN1_WR_CB_OFFS_CNT

Address: Operational Base(0x27C33000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_chn1_wr_cb_offs_cnt Offset counter initial value of chn1 picture uv component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN1_WR_CB_OFFS_CNT_START

Address: Operational Base(0x27C33000) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_chn1_wr_cb_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (chn1 picture uv component)
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN1_WR_Y_STRIDE

Address: Operational Base(0x27C33000) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
14:0	RW	0x0000	sw_chn1_wr_y_stride Line stride of chn1 picture Y component in pixel, also known as line stride, 16byte align. If no line stride is used, line stride must match image width. If tile4x4 write, byte unit; else, pixel unit

VPSS_MI_3000_MI_CHN1_WR_Y_PIC_WIDTH

Address: Operational Base(0x27C33000) + offset (0x0334)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_chn1_wr_y_pic_width Image width of the main picture Y component or RGB picture in pixel. If no line stride is used but flipping required, the image width must be configured

VPSS_MI_3000_MI_CHN1_WR_Y_PIC_SIZE

Address: Operational Base(0x27C33000) + offset (0x033C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	sw_chn1_wr_y_pic_size Image size of the Y component in pixel which has to be the Y line length multiplied by the Y image height (chn1_y_llength * chn1_y_pic_height), used for flipping

VPSS_MI_3000_MI_CHN1_WR_CTRL_SHD

Address: Operational Base(0x27C33000) + offset (0x0350)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RO	0x2	sw_chn1_wr_output_format_shd Selects output format of chn0 picture. 3'b000: YCbCr 4:0:0 3'b001: YCbCr 4:2:0 3'b010: YCbCr 4:2:2 Others: Reserved Note: - If sw_chn1_wr_v_flip = 1 and yuv420 format, need to configure sw_chn0_wr_output_format = 1
7:6	RO	0x0	reserved
5:4	RO	0x1	sw_chn1_wr_format_shd Defines how YCbCr chn1 picture data is written to memory. 2'b00: Reserved 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved
3:1	RO	0x0	reserved
0	RO	0x0	stat_chn1_wr_enable_shd Channel1 write enable

VPSS_MI_3000_MI_CHN1_WR_Y_BASE_SHD

Address: Operational Base(0x27C33000) + offset (0x0360)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_chn1_wr_y_base_shd Base address of chn1 picture Y component ring buffer
3:0	RO	0x0	reserved

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VPSS_MI_3000_MI_CHN1_WR_Y_SIZE_SHD

Address: Operational Base(0x27C33000) + offset (0x0364)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_chn1_wr_y_size_shd Size of chn1 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN1_WR_Y_OFFS_CNT_SHD

Address: Operational Base(0x27C33000) + offset (0x0368)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_chn1_wr_y_offs_cnt_shd Current offset counter of chn1 picture Y component
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN1_WR_CB_BASE_SHD

Address: Operational Base(0x27C33000) + offset (0x0370)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_chn1_wr_cb_base_shd Base address of chn1 picture uv component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN1_WR_CB_SIZE_SHD

Address: Operational Base(0x27C33000) + offset (0x0374)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_chn1_wr_cb_size_shd Size of chn1 picture Cb component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN1_WR_CB_OFFS_CNT_SHD

Address: Operational Base(0x27C33000) + offset (0x0378)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_chn1_wr_cb_offs_cnt_shd Current offset counter of chn1 picture uv component ring buffer for address generation
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN1_WR_Y_END_ADDR

Address: Operational Base(0x27C33000) + offset (0x0380)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_chn1_wr_y_end_addr Channel1 y frame end address readback, used for channel1 wrap debug

VPSS_MI_3000_MI_CHN1_WR_CB_END_ADDR

Address: Operational Base(0x27C33000) + offset (0x0384)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_chn1_wr_cb_end_addr Channel1 uv frame end address readback, used for channel1 wrap debug

VPSS_MI_3000_MI_CHN1_WR_LINE_CNT

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Address: Operational Base(0x27C33000) + offset (0x0388)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_chn1_wr_line_cnt Channel1 write line counter of of y component

VPSS_MI_3000_MI_CHN1_WR_Y2R_COE00

Address: Operational Base(0x27C33000) + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x04a8	sw_chn1_wr_y2r_coe_00 1bit signed+2bit integer+10bit float factor R: sw_chn1_wr_y2r_coe_00*Y + sw_chn1_wr_y2r_coe_01*U + sw_chn1_wr_y2r_coe_02*V + sw_chn1_wr_y2r_coe_off0 Note: initial value is bt709-limit

VPSS_MI_3000_MI_CHN1_WR_Y2R_COE01

Address: Operational Base(0x27C33000) + offset (0x03A4)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_chn1_wr_y2r_coe_01 1bit signed+2bit integer+10bit float factor R: sw_chn1_wr_y2r_coe_00*Y + sw_chn1_wr_y2r_coe_01*U + sw_chn1_wr_y2r_coe_02*V + sw_chn1_wr_y2r_coe_off0 Note: initial value is bt709-limit

VPSS_MI_3000_MI_CHN1_WR_Y2R_COE02

Address: Operational Base(0x27C33000) + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x072c	sw_chn1_wr_y2r_coe_02 1bit signed+2bit integer+10bit float factor R: sw_chn1_wr_y2r_coe_00*Y + sw_chn1_wr_y2r_coe_01*U + sw_chn1_wr_y2r_coe_02*V + sw_chn1_wr_y2r_coe_off0 Note: initial value is bt709-limit

VPSS_MI_3000_MI_CHN1_WR_Y2R_OFF0

Address: Operational Base(0x27C33000) + offset (0x03AC)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x1c1f80	sw_chn1_wr_y2r_coe_off0 1bit signed+10bit integer+10bit float factor R: sw_chn1_wr_y2r_coe_00*Y + sw_chn1_wr_y2r_coe_01*U + sw_chn1_wr_y2r_coe_02*V + sw_chn1_wr_y2r_coe_off0 Note: initial value is bt709-limit

VPSS_MI_3000_MI_CHN1_WR_Y2R_COE10

Address: Operational Base(0x27C33000) + offset (0x03B0)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x04a8	sw_chn1_wr_y2r_coe_10 1bit signed+2bit integer+10bit float factor G: sw_chn1_wr_y2r_coe_10*Y + sw_chn1_wr_y2r_coe_11*U + sw_chn1_wr_y2r_coe_12*V + sw_chn1_wr_y2r_coe_off1 Note: initial value is bt709-limit

VPSS_MI_3000_MI_CHN1_WR_Y2R_COE11

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Address: Operational Base(0x27C33000) + offset (0x03B4)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x1f26	sw_chn1_wr_y2r_coe_11 1bit signed+2bit integer+10bit float factor G: sw_chn1_wr_y2r_coe_10*Y + sw_chn1_wr_y2r_coe_11*U + sw_chn1_wr_y2r_coe_12*V + sw_chn1_wr_y2r_coe_off1 Note: initial value is bt709-limit

VPSS_MI_3000_MI_CHN1_WR_Y2R_COE12

Address: Operational Base(0x27C33000) + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x1dde	sw_chn1_wr_y2r_coe_12 1bit signed+2bit integer+10bit float factor G: sw_chn1_wr_y2r_coe_10*Y + sw_chn1_wr_y2r_coe_11*U + sw_chn1_wr_y2r_coe_12*V + sw_chn1_wr_y2r_coe_off1 Note: initial value is bt709-limit

VPSS_MI_3000_MI_CHN1_WR_Y2R_OFF1

Address: Operational Base(0x27C33000) + offset (0x03BC)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x013380	sw_chn1_wr_y2r_coe_off1 1bit signed+10bit integer+10bit float factor G: sw_chn1_wr_y2r_coe_10*Y + sw_chn1_wr_y2r_coe_11*U + sw_chn1_wr_y2r_coe_12*V + sw_chn1_wr_y2r_coe_off1 Note: initial value is bt709-limit

VPSS_MI_3000_MI_CHN1_WR_Y2R_COE20

Address: Operational Base(0x27C33000) + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x04a8	sw_chn1_wr_y2r_coe_20 1bit signed+2bit integer+10bit float factor B: sw_chn1_wr_y2r_coe_20*Y + sw_chn1_wr_y2r_coe_21*U + sw_chn1_wr_y2r_coe_22*V + sw_chn1_wr_y2r_coe_off2 Note: initial value is bt709-limit

VPSS_MI_3000_MI_CHN1_WR_Y2R_COE21

Address: Operational Base(0x27C33000) + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0873	sw_chn1_wr_y2r_coe_21 1bit signed+2bit integer+10bit float factor B: sw_chn1_wr_y2r_coe_20*Y + sw_chn1_wr_y2r_coe_21*U + sw_chn1_wr_y2r_coe_22*V + sw_chn1_wr_y2r_coe_off2 Note: initial value is bt709-limit

VPSS_MI_3000_MI_CHN1_WR_Y2R_COE32

Address: Operational Base(0x27C33000) + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	sw_chn1_wr_y2r_coe_22 1bit signed+2bit integer+10bit float factor B: sw_chn1_wr_y2r_coe_20*Y + sw_chn1_wr_y2r_coe_21*U + sw_chn1_wr_y2r_coe_22*V + sw_chn1_wr_y2r_coe_off2 Note: initial value is bt709-limit

VPSS_MI_3000_MI_CHN1_WR_Y2R_OFF2

Address: Operational Base(0x27C33000) + offset (0x03CC)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x1b7c00	sw_chn1_wr_y2r_coe_off2 1bit signed+10bit integer+10bit float factor B: sw_chn1_wr_y2r_coe_20*Y + sw_chn1_wr_y2r_coe_21*U + sw_chn1_wr_y2r_coe_22*V + sw_chn1_wr_y2r_coe_off2 Note: initial value is bt709-limit

VPSS_MI_3000_MI_CHN2_WR_CTRL

Address: Operational Base(0x27C33000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31	RO	0x0	mi_chn2_working MI channel2 working
30:11	RO	0x00000	reserved
10:8	RW	0x2	sw_chn2_wr_output_format Selects output format of chn2 picture. 3'b111: RGB 888 3'b110: ARGB 888 3'b100: RGB 565 3'b010: YCbCr 4:2:2 3'b001: YCbCr 4:2:0 3'b000: YCbCr 4:0:0 Note: - If sw_chn2_wr_v_flip = 1 and yuv420 format, need to configure sw_chn2_wr_output_format = 1 - If sw_mi_rd_r2y_bypass = 1 or sw_vpss_y2r_en = 1, MI output format need to be configured in RGB.
7:6	RO	0x0	reserved
5:4	RW	0x1	sw_chn2_wr_format Defines how YCbCr chn2 picture data is written to memory. 2'b00: Reserved 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved
3:2	RO	0x0	reserved
1	RW	0x1	sw_chn2_wr_auto_update Automatic update of configuration registers for chn2 at frame end. 1'b1: Enabled 1'b0: Disabled
0	RW	0x0	sw_chn2_wr_enable Channel2 write enable

VPSS_MI_3000_MI_CHN2_WR_Y_BASE

Address: Operational Base(0x27C33000) + offset (0x0410)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_chn2_wr_y_base Base address of chn2 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN2_WR_Y_SIZE

Address: Operational Base(0x27C33000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_chn2_wr_y_size Size of chn2 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN2_WR_Y_OFFS_CNT

Address: Operational Base(0x27C33000) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_chn2_wr_y_offs_cnt Offset counter initial value of chn2 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN2_WR_Y_OFFS_CNT_START

Address: Operational Base(0x27C33000) + offset (0x041C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_chn2_wr_y_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (chn2 picture Y component)
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN2_WR_CB_BASE

Address: Operational Base(0x27C33000) + offset (0x0420)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_chn2_wr_cb_base Base address of chn2 picture uv component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN2_WR_CB_SIZE

Address: Operational Base(0x27C33000) + offset (0x0424)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_chn2_wr_cb_size Size of chn2 picture uv component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN2_WR_CB_OFFS_CNT

Address: Operational Base(0x27C33000) + offset (0x0428)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_chn2_wr_cb_offs_cnt Offset counter initial value of chn2 picture uv component ring buffer
3:0	RO	0x0	reserved

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VPSS_MI_3000_MI_CHN2_WR_CB_OFFS_CNT_START

Address: Operational Base(0x27C33000) + offset (0x042C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_chn2_wr_cb_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (chn2 picture uv component)
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN2_WR_Y_STRIDE

Address: Operational Base(0x27C33000) + offset (0x0430)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_chn2_wr_y_stride Line stride of chn2 picture Y component in pixel, also known as line stride, 16byte align. If no line stride is used, line stride must match image width. If tile4x4 write, byte unit; else, pixel unit

VPSS_MI_3000_MI_CHN2_WR_Y_PIC_WIDTH

Address: Operational Base(0x27C33000) + offset (0x0434)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_chn2_wr_y_pic_width Image width of the main picture Y component or RGB picture in pixel. If no line stride is used but flipping required, the image width must be configured

VPSS_MI_3000_MI_CHN2_WR_Y_PIC_SIZE

Address: Operational Base(0x27C33000) + offset (0x043C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	sw_chn2_wr_y_pic_size Image size of the Y component in pixel which has to be the Y line length multiplied by the Y image height (chn2_y_llength * chn2_y_pic_height), used for flipping

VPSS_MI_3000_MI_CHN2_WR_CTRL_SHD

Address: Operational Base(0x27C33000) + offset (0x0450)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RO	0x2	sw_chn2_wr_output_format_shd Selects output format of chn2 picture. 3'b000: YCbCr 4:0:0 3'b001: YCbCr 4:2:0 3'b010: YCbCr 4:2:2 Others: Reserved Note: - If sw_chn0_wr_v_flip = 1 and yuv420 format, need to configure sw_chn0_wr_output_format = 1
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:4	RO	0x1	sw_chn2_wr_format_shd Defines how YCbCr chn2 picture data is written to memory. 2'b00: Reserved 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved
3:1	RO	0x0	reserved
0	RO	0x0	stat_chn2_wr_enable_shd Channel2 write enable

VPSS_MI_3000_MI_CHN2_WR_Y_BASE_SHD

Address: Operational Base(0x27C33000) + offset (0x0460)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_chn2_wr_y_base_shd Base address of chn2 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN2_WR_Y_SIZE_SHD

Address: Operational Base(0x27C33000) + offset (0x0464)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_chn2_wr_y_size_shd Size of chn2 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN2_WR_Y_OFFS_CNT_SHD

Address: Operational Base(0x27C33000) + offset (0x0468)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_chn2_wr_y_offs_cnt_shd Current offset counter of chn2 picture Y component
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN2_WR_CB_BASE_SHD

Address: Operational Base(0x27C33000) + offset (0x0470)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_chn2_wr_cb_base_shd Base address of chn2 picture uv component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN2_WR_CB_SIZE_SHD

Address: Operational Base(0x27C33000) + offset (0x0474)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_chn2_wr_cb_size_shd Size of chn2 picture Cb component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN2_WR_CB_OFFS_CNT_SHD

Address: Operational Base(0x27C33000) + offset (0x0478)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:4	RO	0x000000	sw_chn2_wr_cb_offs_cnt_shd Current offset counter of chn2 picture uv component ring buffer for address generation
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN2_WR_Y_END_ADDR

Address: Operational Base(0x27C33000) + offset (0x0480)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_chn2_wr_y_end_addr Channel2 y frame end address readback, used for channel2 wrap debug

VPSS_MI_3000_MI_CHN2_WR_CB_END_ADDR

Address: Operational Base(0x27C33000) + offset (0x0484)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_chn2_wr_cb_end_addr Channel2 uv frame end address readback, used for channel2 wrap debug

VPSS_MI_3000_MI_CHN2_WR_LINE_CNT

Address: Operational Base(0x27C33000) + offset (0x0488)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_chn2_wr_line_cnt Channel2 write line counter of of y component

VPSS_MI_3000_MI_CHN3_WR_CTRL

Address: Operational Base(0x27C33000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31	RO	0x0	mi_chn3_working MI channel3 working
30:11	RO	0x00000	reserved
10:8	RW	0x2	sw_chn3_wr_output_format Selects output format of chn3 picture. 3'b111: RGB 888 3'b110: ARGB 888 3'b100: RGB 565 3'b010: YCbCr 4:2:2 3'b001: YCbCr 4:2:0 3'b000: YCbCr 4:0:0 Note: - If sw_chn3_wr_v_flip = 1 and yuv420 format, need to configure sw_chn3_wr_output_format = 1 - If sw_mi_rd_r2y_bypass = 1 or sw_vpss_y2r_en = 1, MI output format need to be configured in RGB.
7:6	RO	0x0	reserved
5:4	RW	0x1	sw_chn3_wr_format Defines how YCbCr chn3 picture data is written to memory. 2'b00: Reserved 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x1	sw_chn3_wr_auto_update Automatic update of configuration registers for chn3 at frame end. 1'b1: Enabled 1'b0: Disabled
0	RW	0x0	sw_chn3_wr_enable Channel3 write enable

VPSS_MI_3000_MI_CHN3_WR_Y_BASE

Address: Operational Base(0x27C33000) + offset (0x0510)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_chn3_wr_y_base Base address of chn3 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN3_WR_Y_SIZE

Address: Operational Base(0x27C33000) + offset (0x0514)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_chn3_wr_y_size Size of chn3 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN3_WR_Y_OFFS_CNT

Address: Operational Base(0x27C33000) + offset (0x0518)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_chn3_wr_y_offs_cnt Offset counter initial value of chn3 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN3_WR_Y_OFFS_CNT_START

Address: Operational Base(0x27C33000) + offset (0x051C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_chn3_wr_y_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (chn3 picture Y component)
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN3_WR_CB_BASE

Address: Operational Base(0x27C33000) + offset (0x0520)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_chn3_wr_cb_base Base address of chn3 picture uv component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN3_WR_CB_SIZE

Address: Operational Base(0x27C33000) + offset (0x0524)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_chn3_wr_cb_size Size of chn3 picture uv component ring buffer

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN3_WR_CB_OFFS_CNT

Address: Operational Base(0x27C33000) + offset (0x0528)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_chn3_wr_cb_offs_cnt Offset counter initial value of chn3 picture uv component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN3_WR_CB_OFFS_CNT_START

Address: Operational Base(0x27C33000) + offset (0x052C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_chn3_wr_cb_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (chn3 picture uv component)
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN3_WR_Y_STRIDE

Address: Operational Base(0x27C33000) + offset (0x0530)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_chn3_wr_y_stride Line stride of chn3 picture Y component in pixel, also known as line stride, 16byte align. If no line stride is used, line stride must match image width. If tile4x4 write, byte unit; else, pixel unit

VPSS_MI_3000_MI_CHN3_WR_Y_PIC_WIDTH

Address: Operational Base(0x27C33000) + offset (0x0534)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_chn3_wr_y_pic_width Image width of the main picture Y component or RGB picture in pixel. If no line stride is used but flipping required, the image width must be configured

VPSS_MI_3000_MI_CHN3_WR_Y_PIC_SIZE

Address: Operational Base(0x27C33000) + offset (0x053C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	sw_chn3_wr_y_pic_size Image size of the Y component in pixel which has to be the Y line length multiplied by the Y image height (chn3_y_llength * chn3_y_pic_height), used for flipping

VPSS_MI_3000_MI_CHN3_WR_CTRL_SHD

Address: Operational Base(0x27C33000) + offset (0x0550)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
10:8	RO	0x2	sw_chn3_wr_output_format_shd Selects output format of chn3 picture. 3'b000: YCbCr 4:0:0 3'b001: YCbCr 4:2:0 3'b010: YCbCr 4:2:2 Others: Reserved Note: - If sw_chn0_wr_v_flip = 1 and yuv420 format, need to configure sw_chn0_wr_output_format = 1
7:6	RO	0x0	reserved
5:4	RO	0x1	sw_chn3_wr_format_shd Defines how YCbCr chn3 picture data is written to memory. 2'b00: Reserved 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved
3:1	RO	0x0	reserved
0	RO	0x0	stat_chn3_wr_enable_shd Channel3 write enable

VPSS_MI_3000_MI_CHN3_WR_Y_BASE_SHD

Address: Operational Base(0x27C33000) + offset (0x0560)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_chn3_wr_y_base_shd Base address of chn3 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN3_WR_Y_SIZE_SHD

Address: Operational Base(0x27C33000) + offset (0x0564)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_chn3_wr_y_size_shd Size of chn3 picture Y component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN3_WR_Y_OFFS_CNT_SHD

Address: Operational Base(0x27C33000) + offset (0x0568)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_chn3_wr_y_offs_cnt_shd Current offset counter of chn3 picture Y component
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN3_WR_CB_BASE_SHD

Address: Operational Base(0x27C33000) + offset (0x0570)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_chn3_wr_cb_base_shd Base address of chn3 picture uv component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN3_WR_CB_SIZE_SHD

Address: Operational Base(0x27C33000) + offset (0x0574)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:4	RO	0x000000	sw_chn3_wr_cb_size_shd Size of chn3 picture Cb component ring buffer
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN3_WR_CB_OFFS_CNT_SHD

Address: Operational Base(0x27C33000) + offset (0x0578)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_chn3_wr_cb_offs_cnt_shd Current offset counter of chn3 picture uv component ring buffer for address generation
3:0	RO	0x0	reserved

VPSS_MI_3000_MI_CHN3_WR_Y_END_ADDR

Address: Operational Base(0x27C33000) + offset (0x0580)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_chn3_wr_y_end_addr Channel3 y frame end address readback, used for channel3 wrap debug

VPSS_MI_3000_MI_CHN3_WR_CB_END_ADDR

Address: Operational Base(0x27C33000) + offset (0x0584)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_chn3_wr_cb_end_addr Channel3 uv frame end address readback, used for channel3 wrap debug

VPSS_MI_3000_MI_CHN3_WR_LINE_CNT

Address: Operational Base(0x27C33000) + offset (0x0588)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_chn3_wr_line_cnt Channel3 write line counter of of y component

3.4.2.8 MMU

MMU_3F00_DTE_ADDR

Address: Operational Base(0x27C33F00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU current page Table address

MMU_3F00_STATUS

Address: Operational Base(0x27C33F00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master reponsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 1'b0: Read 1'b1: Write
4	RO	0x0	REPLAY_BUFFER_EMPTY The MMU replay buffer is empty

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Bit	Attr	Reset Value	Description
3	RO	0x0	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled . The mode is enabled by command
0	RO	0x0	PAGING_ENABLED Paging is enabled

MMU_3F00_COMMAND

Address: Operational Base(0x27C33F00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE 3'b110: MMU_FORCE_RESET

MMU_3F00_PAGE_FAULT_ADDR

Address: Operational Base(0x27C33F00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR address of last page fault

MMU_3F00_ZAP_ONE_LINE

Address: Operational Base(0x27C33F00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE address to be invalidated from the page table cache

MMU_3F00_INT_RAWSTAT

Address: Operational Base(0x27C33F00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

MMU_3F00_INT_CLEAR

Address: Operational Base(0x27C33F00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	READ_BUS_ERROR read bus error
0	WO	0x0	PAGE_FAULT page fault

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MMU_3F00_INT_MASK

Address: Operational Base(0x27C33F00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

MMU_3F00_INT_STATUS

Address: Operational Base(0x27C33F00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	READ_BUS_ERROR read bus error
0	RO	0x0	PAGE_FAULT page fault

MMU_3F00_AUTO_GATING

Address: Operational Base(0x27C33F00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mmu_auto_gating when it is 1'b1, the mmu will auto gating it self

3.5 Application Notes

3.5.1 Mirror

1) Set 0x0000[4] sw_mir_en = 1
2) Set 0x0010[4] sys_mir_force_upd = 1, to update the shadow register

3.5.2 CMSC

1) Set 0x0500[0] sw_cmsc_en = 1
2) The four output channels can independently control the CMSC window switches and modes, but share the window vertex, mosaic block size, and cover color configurations
3) Set 0x0504[4] sys_itself_force_upd = 1, to update shadow registers

3.5.3 Crop

The cropping module supports one channel input and four channels output, taking Channel0 as an example:

1) Set 0x0700[1] sw_crop0_en = 1
2) Set 0x0710[13:0] sw_0_h_offs
3) Set 0x0714[13:0] sw_0_v_offs
4) Set 0x0718[13:0] sw_0_h_size
5) Set 0x071c[13:0] sw_0_v_size
6) Set 0x0704[4] sys_cfg_force_upd = 1, to update shadow registers

3.5.4 Scale

3.5.4.1 ZME

ZME is used for CHN0 scaling. The tap coefficients of polyphase filtering need to be selected based on different scaling ratios.

1) Configure Y (0x1810) and UV (0x1830) scaling enable based on the specific scaling case
2) Configure 0x1814[15:0] and 0x1834[15:0] to be equal to scale *input_width* minus 1
3) Configure 0x1814[31:16] and 0x1834[31:16] to be equal to scale *input_height* minus 1
4) Configure 0x1818[15:0] and 0x1838[15:0] to be equal to scale *output_width* minus 1
5) Configure 0x1818[31:16] and 0x1838[31:16] to be equal to scale *output_height* minus

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1
6) Configure horizontal and vertical scaling factors
7) Configure tab coefficients
8) Set 0x1804[4] sys_cfg_force_upd = 1, to update shadow registers

3.5.4.2 Bilinear

Channel1~channel3 all use bilinear scaling, taking CHN1 as an example:
1) Configure Y and UV (0x1c00) scaling enable based on the specific scaling case
2) Configure the input resolution of scale 0x1c08[13:0] and 0x1c08[29:16]
3) Configure the output resolution of scale 0x1c0c[13:0] and 0x1c0c[29:16]
4) Configure the horizontal scaling factor of the Y-component 0x1c10[17:0]
5) Configure the horizontal scaling factor of the UV-component 0x1c14[17:0]
6) Configure the vertical scaling factor of the Y-component 0x1c18[17:0]
7) Configure the vertical scaling factor of the UV-component 0x1c1c[17:0]
8) Set 0x1c04[4] sys_cfg_force_upd = 1, to update shadow registers

3.5.5 Aspective Ratio

Channel0~channel3 all support the screen aspect ratio, taking CHN0 as an example:
1) Configure Ratio input width 0x1910[13:0] and height 0x1910[29:16]
2) Configure output width 0x1914[13:0] and height 0x1914[29:16] after boundary filling
3) Configure the offsets of Ratio input-image in output-image ox1918[13:0] and 0x1918[29:16]
4) Set 0x1904[4] sys_cfg_force_upd = 1, to update shadow registers

3.5.6 MI

3.5.6.1 MI Read

VPSS dma-read supports three modes: LINE, TILE, and RKFBCD.
1) According to the read mode, configure 0x3100[9:8] sw_mi_rd_mode
2) If tile rotation mode is used, configure 0x3100[11:10] sw_mi_rd_rot_mode
3) Configure the input image width 0x3114
4) Configure the input image height 0x3118
5) Configure the read start address 0x3110 for Y-component
6) Configure the read start address 0x3120 for UV-component
7) Configure the image virtual stride 0x311c
8) When all MI registers are configured, then set 0x3004[4] = 1, to update shadow registers

3.5.6.2 MI Write

VPSS has four write channels, one of which supports TILE writing for CHN0 and CHN1, and CHN1 can support RGB output. Taking CHN1 as an example:
1) Set channel1 writing enable 0x3300 = 1
2) Configure output image format 0x3300[10:8]
3) Configure the write start address 0x3310 for Y-component
4) Configure image size 0x3314 for Y-component
5) Configure the write start address 0x3320 for UV-component
6) Configure image size 0x3324 for UV-component
7) When all MI registers are configured, then set 0x3004[4] = 1, to update shadow registers

3.5.7 Registers Readback

All registers of VPSS (except MMU) can be configured in AXI readback mode. During registers AXI readback, AHB configuration is also supported, and AHB has a high priority. AXI register configuration is composed of head (address offset + mode + counter) + data, which is shown as below:

	[31:18]	[17:16]	[15:0]
head	addr[15:2]	mode	counter
data	data(32bit)		

Fig. 3-3 AXI register configuration

mode 2'b00 is increased mode, mode 2'b11 is fixed mode, counter is the number of the register configuration, which must be consistent with data number. When data is 32'hffffffff,

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registers readback is finished. Here is an example of registers readback:

	[31:18]	[17:16]	[15:0]		
head	0x3c00>>2	00	5		
data	data_0			0x1c00	mode=2'b00, address increment
	data_1			0x1c04	
	data_2			0x1c08	
	data_3			0x1c0c	
	data_4			0x1c10	
head	0x2600>>2	11	6		
data	data_0			0x1000	mode=2'b11, address fixed
	data_1			0x1000	
	data_2			0x1000	
	data_3			0x1000	
	data_4			0x1000	
	data_5			0x1000	
	32'hffff_ffff			结束	

Fig. 3-4 an example of registers readback

The step of registers readback:

1) Calculate the word number of configuration, configure sw_axi_cfg_wsize (0x3168) and sw_axi_cfg_vsize (0x316c). The total word number of configuration is sw_axi_cfg_wsize * sw_axi_cfg_vsize (this product results must be greater than or equal to 64). When sw_axi_cfg_wsize is no more than 8192, set sw_axi_cfg_vsize = 1, otherwise when sw_axi_cfg_wsize is no more than 8192 * 2, set sw_axi_cfg_vsize = 2, and so on.

2) Configure sw_axi_cfg_rd_base (0x3164), where has loaded the AXI register configuration list.

3) Set sys_axi_cfg_rd_st (0x3160[0]) = 1, to start registers readback. There are two modes of registers readback. When sys_axi_cfg_rd_st_mode (0x3160[1]) is configured to 1, registers readback start by configuring sys_axi_cfg_rd_st to 1 in each frame. When sys_axi_cfg_rd_st_mode is 0, registers readback start by sys_axi_cfg_rd_st in first frame, then will start by frame end signal automatically, and on this condition axi_cfg_rd_status (address offset 0x3160[31]) must be cleared by configuring axi_cfg_rd_clear (0x3160[4]) to 1 during current frame.

3.5.8 Online mode

VPSS has three working modes: Mode 0, offline mode; Mode 1, online mode with direct connection to ISP; Mode 2, offline and ISP online coexistence mode shared with VPSS channels.

1) Set 0x0004[17:16] sw_isp2vpss_online_mode = 0, VPSS is in offline working mode, and the image data comes from DDR; Set sw_isp2vpss_online_mode = 1, VPSS receives direct data flow from ISP and is in online working mode; Set sw_isp2vpss_online_mode = 2, VPSS itself is in offline working mode and can receive online data flow from ISP.

2) When sw_isp2vpss_online_mode = 2, if ISP needs to use Mirror and CMSC of VPSS, set 0x0004[18] sw_isp2vpss_cmsc_en = 1, and ISP resolution register 0x0008 is configured; Configure the channel that ISP needs to use, for example, if ISP needs to use channel0, set 0x0004[1:0] sw_isp2vpss_chn0_sel = 2.

3) Set 0x0010[0] = 1, to update shadow registers

3.5.9 IRQ

There are two important interrupt registers in VPSS, VPSS_MIS (0x0078) and MI_MIS (0x3058).

The following chart shows the interrupt sequence between several interrupts:

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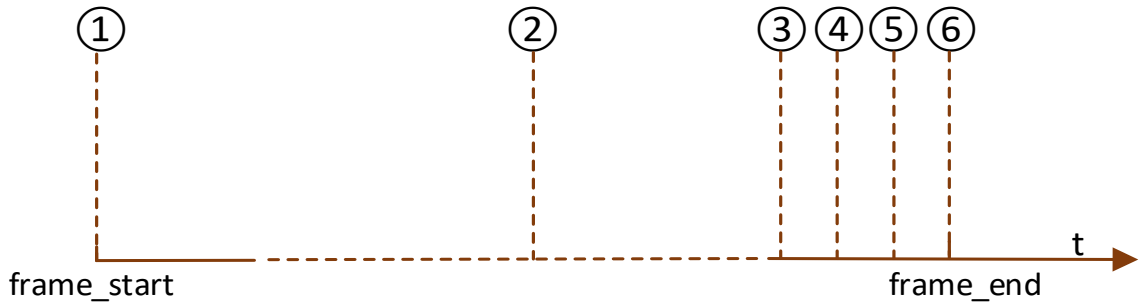


Fig. 3-5 Interrupt Sequence

The meaning of the above numerical symbols are as follows:

Table 3-2 Meaning of IRQ

No.	Interrupt name	Register name	Meaning
1	crop_in_frm_st	VPSS_MIS	Start edge, pull up time is the same as first pixel valid in VPSS
2	crop_in_cfg_irq	VPSS_MIS	The line counter of VPSS has reached the configured number of lines
3	crop_in_frm_end_p	VPSS_MIS	VPSS input frame end
4	scl0_in_frm_end_p	VPSS_MIS	Channel0 scale frame end
5	ratio0_in_frm_end_p	VPSS_MIS	Channel0 aspective_ratio frame end
6	stat_all_frame_end	MI_MIS	MI all channels frame end

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Chapter 4 Raster Graphic Acceleration (RGA2.5)

4.1 Overview

RGA2.5 is a separate 2D raster graphic accelerator, use to accelerate basic 2D graphics operations, including: image scaling, rotation, BitBLT, alpha blending.

4.1.1 Features

- **Data format**
  - SRC0 Input data format:
    - ARGB8888/RGBA8888/RGBA4444/RGBA5551
    - RGB888P/RGB565
    - YUV422-P/YUV422-SP-8bit/10bit(clip to 8bit after input)
    - YUV420-P/YUV420-SP-8bit/10bit(clip to 8bit after input)
    - YUV444I/YUV444SP-8bit
    - YVYU422-8bit
    - YUV400-8bit
    - RFBC YUV420/422/444-8bit
    - RFBC YUV420/422/444-10bit(clip to 8bit after input)
    - AFBC32X8(split mode only) ARGB8888/RGB888P
    - AFBC64X4 ARGB8888/RGB888P/RGB565
    - TILE4X4 YUV420/422/444-8bit
    - TILE4X4 YUV420/422/444-10bit(clip to 8bit after input)
    - BPP1/2/4/8
  - SRC1 Input data format:
    - ARGB8888/RGBA8888/RGBA4444/RGBA5551/A8
    - RGB888P/RGB565
  - Output data format(all YUV format is 8bit):
    - ARGB8888/RGBA8888/ARGB4444/RGBA4444/ARGB5551/RGBA5551
    - RGB888/RGB565
    - YUV420/YUV422 P/SP
    - YUV400/Y4
    - TILE4x4 YUV420/422
    - YUV444SP/444I
  - Pixel Format conversion, BT.601/BT.709
  - Dither operation
  - Max resolution: 8192x8192 source, 4096x4096 destination
- **Scaling**
  - Down-scaling: Average/Bilinear filter
  - Up-scaling: Bi-cubic filter(source>1992 would use Bi-linear)
  - Arbitrary non-integer scaling ratio, from 1/16 to 16
- **Rotation**
  - 0, 90, 180, 270 degree rotation
  - x-mirror, y-mirror operation
  - Mirroring and rotation co-operation
- **BitBLT**
  - Block transfer
  - Color palette/Color fill, support with alpha
  - Transparency mode (color keying/stencil test, specified value/value range)
  - Two source BitBLT
  - A+B=B only BitBLT, A support rotate & scale when B fixed
  - A+B=C second source (B) has same attribute with (C) plus rotation function
- **Alpha Blending**
  - Comprehensive per-pixel alpha(color/alpha channel separately)
  - Fading
  - Support SRC1(R2Y)+SRC0(YUV) -> DST(YUV)
  - Support DST Full CSC convert for YUV2YUV

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- **OSD Automatic Inversion**
  - Supports OSD sources in ARGB8888/ARGB1555/ARGB444/ARGB2BPP format
  - Support SRC0 and OSD overlay
- **Others**
  - Support square mosaic patterns to cover rectangular mosaic areas
  - Support MMU and MMU table pre-fetch

4.1.2 The Constraints

- YUV420/422-8bit virtual stride need 8byte align, xoff/yoff need 2byte align
- YUV420/422-10bit virtual stride need 16byte align, not support xoff/yoff
- Horizontal Bi-cubic scale up && Vertical scale up Bi-cubic src0 width<=1928
- Horizontal Bi-cubic scale up && Vertical scale up Bilinear src0 width<=3856
- Horizontal Bi-cubic scale up && Vertical scale down or bypass src0 width<=4096

4.2 Block Diagram

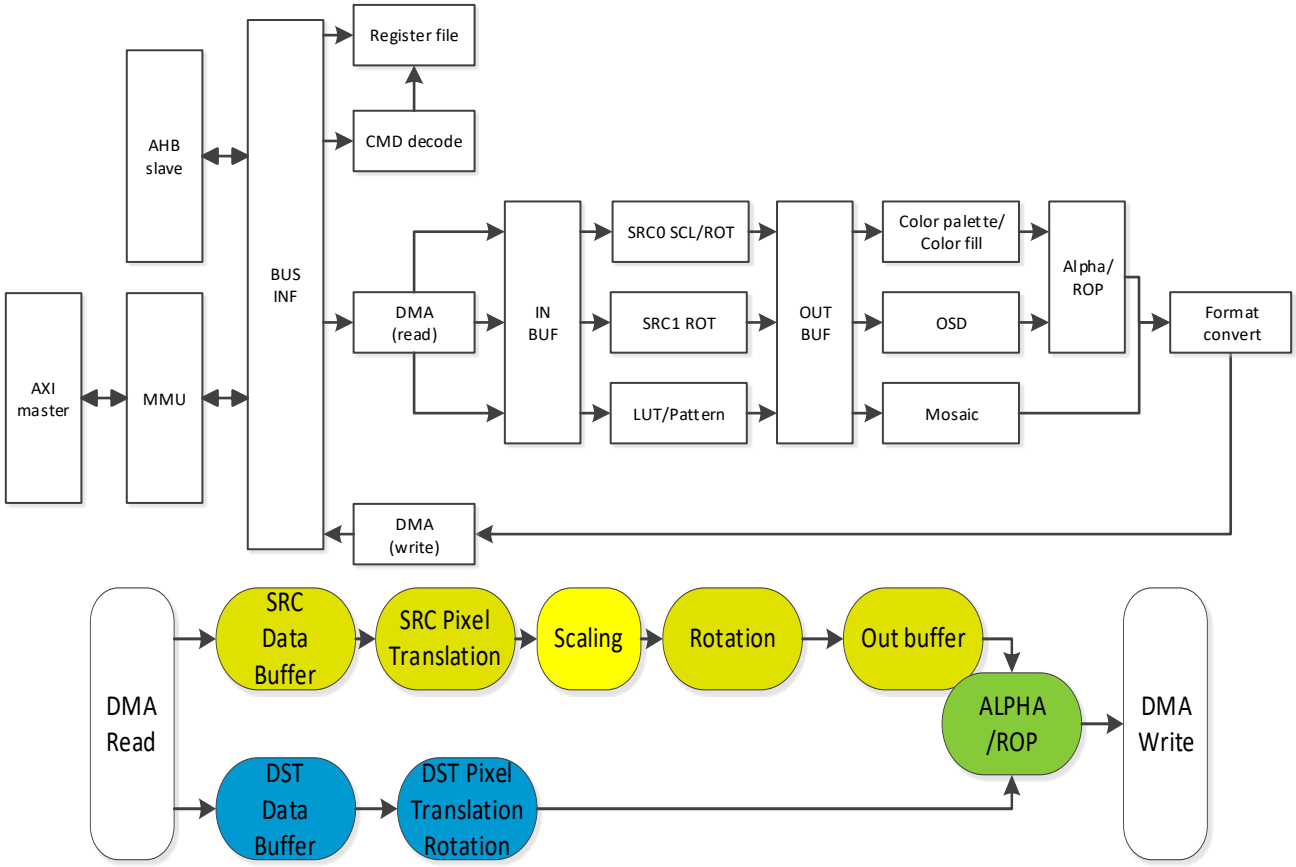


Fig. 4-1 RGA Block Diagram

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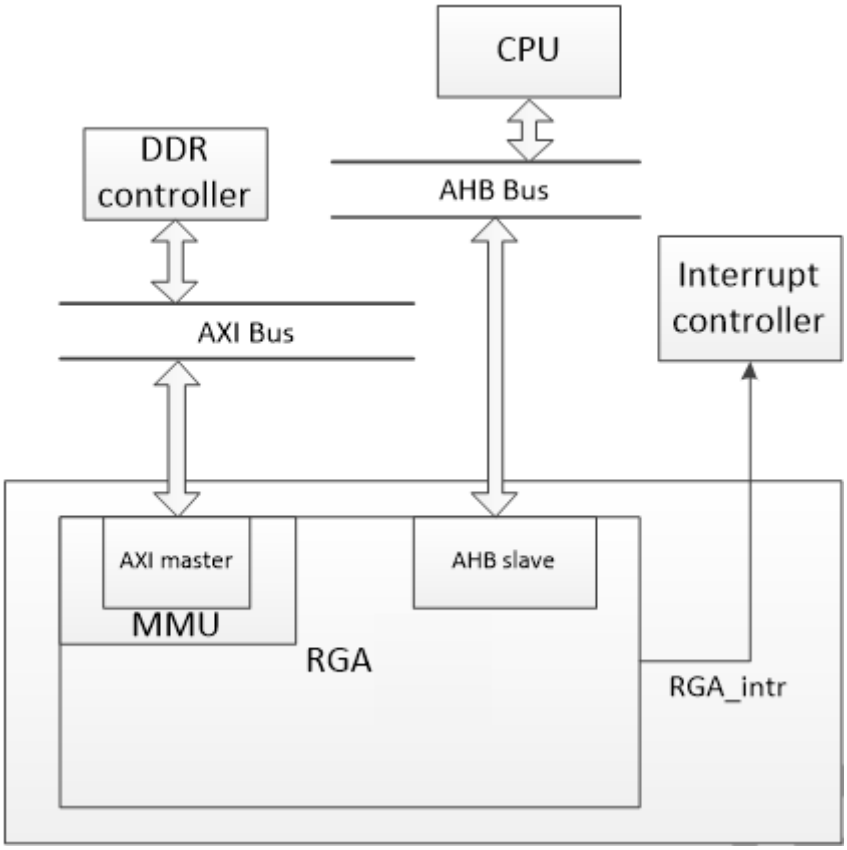


Fig. 4-2 RGA in SOC

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4.3 Function Description

4.3.1 Data Format

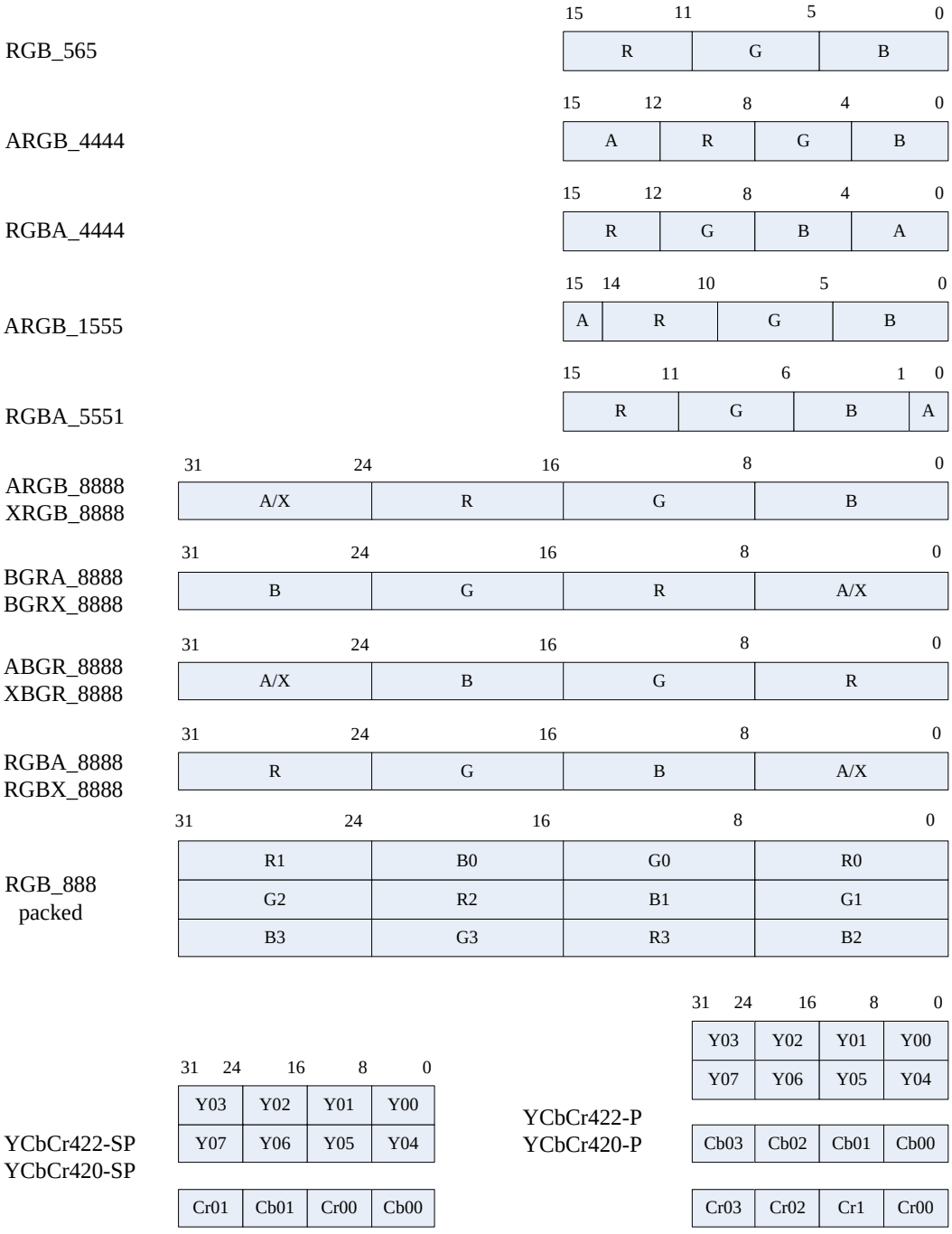


Fig. 4-3 RGA Input Data Format

All input data (defined by SRC_IN_FMT/DST_IN_FMT) are converted to ABGR8888/AUYV8888. The results are converted to the output data format (defined by DST_OUT_FMT).

4.3.2 Dithering

There could have dithering operation for source image when the source image format is not RGB565 and the destination format is RGB565.

The down-dithering is done using Dither Allegro.

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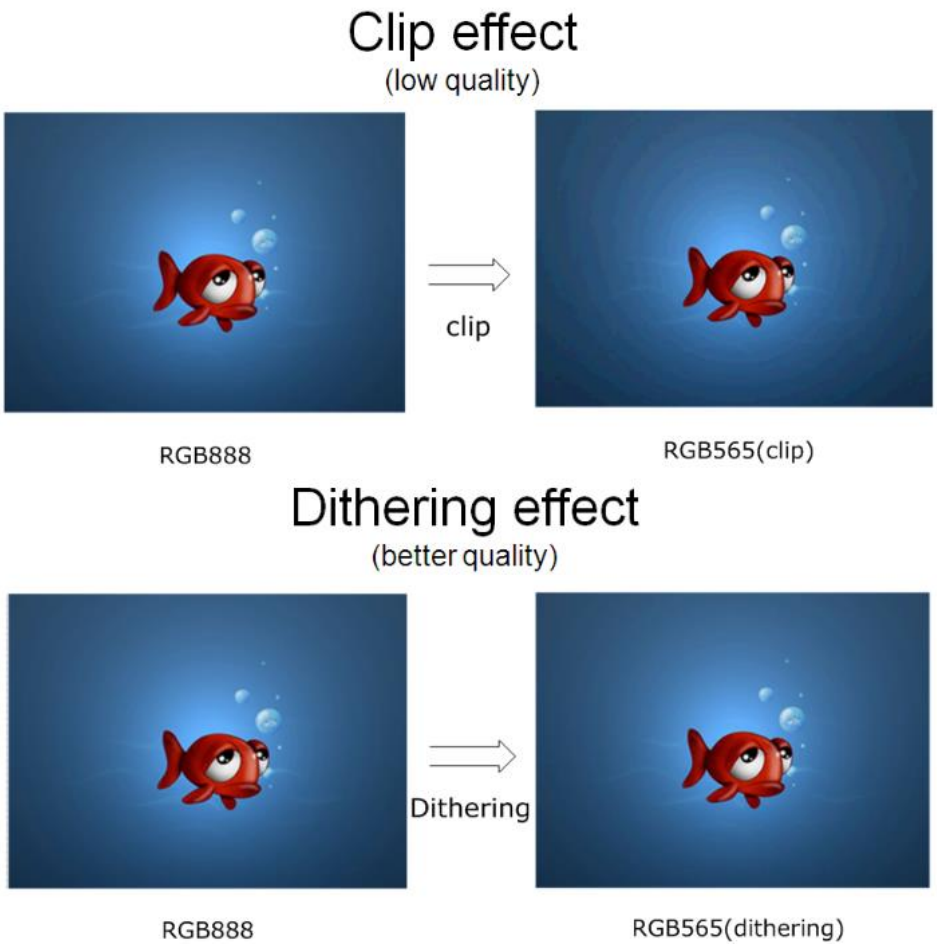
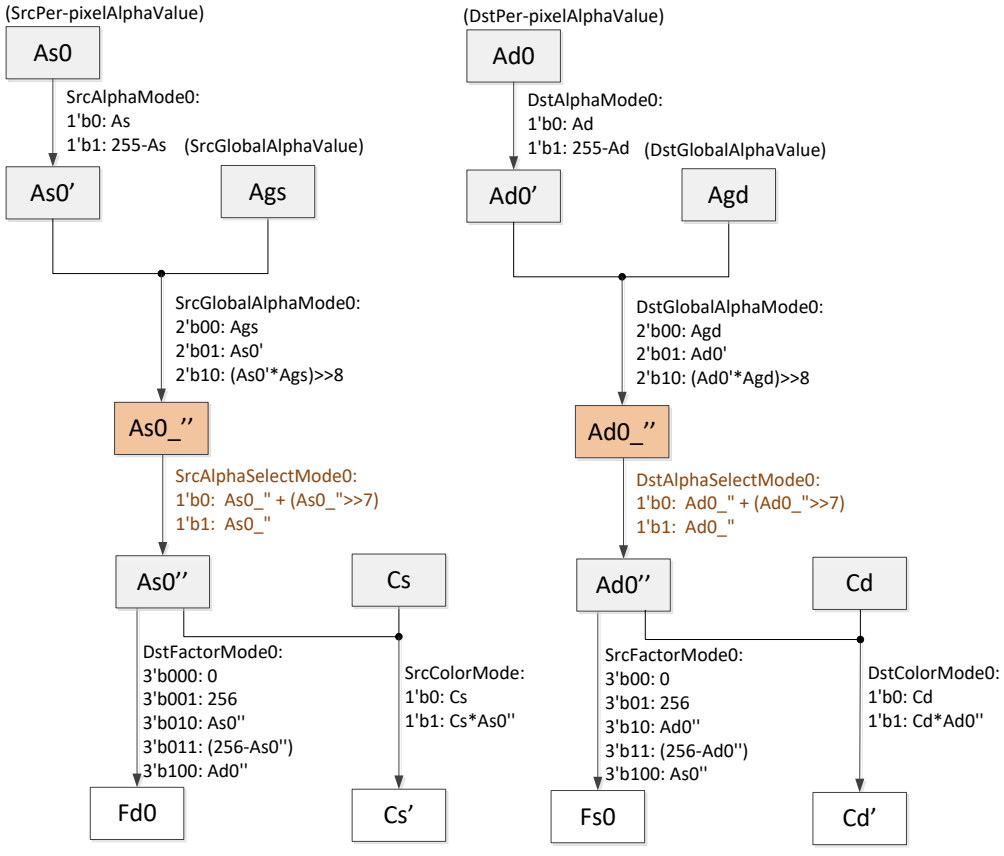


Fig. 4-4 RGA Dither effect

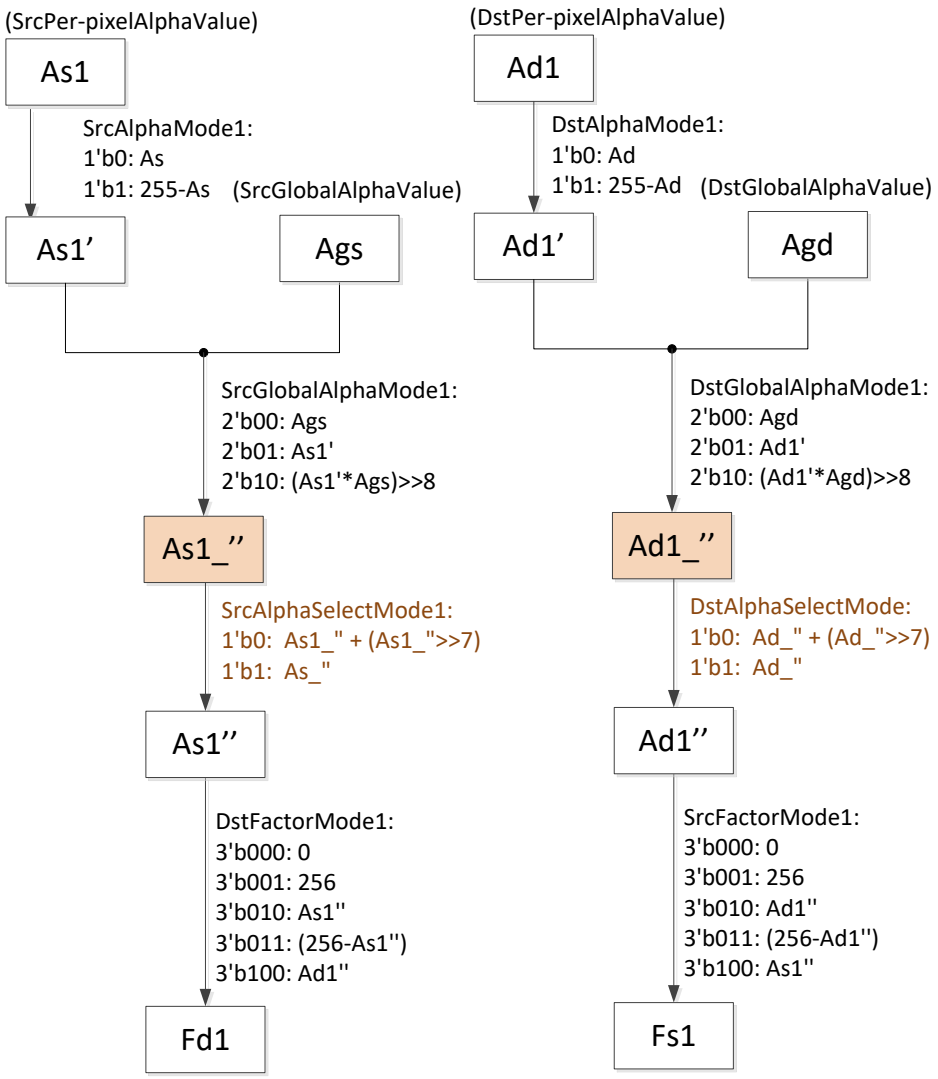
4.3.3 Alpha Mode



$$Cd = Fs0 * Cs' + Fd0 * Cd' \quad (1)$$

(Cd – dst color, Fs0 – color src factor0, Cs' – src color', Fd0 – color dst factor0, Cd' – dst color')

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$$Ad = Fs1 * As1'' + Fd1 * Ad1'' \quad (2)$$

(Ad – dst alpha, Fs1 – alpha src factor1, As1'' – src alpha'', Fd1 – alpha dst factor1, Ad1' – dst alpha'')

Fig. 4-5 alpha mode configure description

4.3.4 Color Fill

Two modes of color fill can be done by RGA: solid fill and gradient fill.

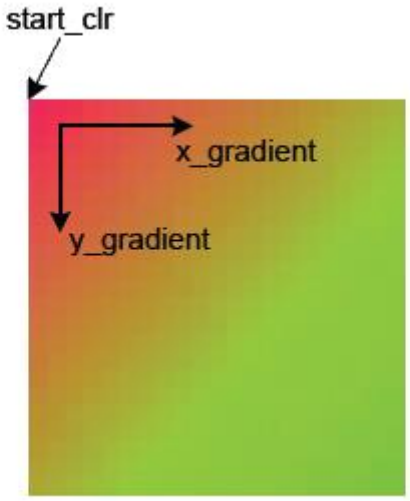


Fig. 4-6 RGA Gradient Fill

Gradient fill using following equations for ARGB calculation of every pixel in different coordinate.

A_cur = (A_start + x*x_A_gradient) +y*y_A_gradient;
R_cur = (R_start + x*x_R_gradient) +y*y_R_gradient;
G_cur = (G_start + x*x_G_gradient) +y*y_G_gradient;
B_cur = (B_start + x*x_B_gradient) +y*y_B_gradient;

A_start, R_start, G_start, B_start is the ARGB value of start point. There are four pairs of values for horizontal and vertical gradient. Saturation operation could be enabled or disabled if the color overflows 255 or underflows 0.

4.3.5 Scaling

The scaling operation is the image reshaping processing of source image. Scaling is done base on ARGB8888 format.
There are three sampling modes: scale down (Average); scale up(Bi-cubic), scale up(Bi-linear).

4.3.6 OSD Automatic Inversion

Supports unidirectional (vertical or horizontal) OSD bars. Support OSD automatic color inversion and regional brightness statistics. The command of statistics and automatic color inversion can be operated at the same time or separately.
The width of each OSD block supports fixed mode and variable mode. The threshold for whether the OSD inverts color can be configured. The brightness statistics or the inverse color flags of OSD blocks can be read by AHB.This function can be used in dash cams, monitors, players, etc.



Fig. 4-7 RGA OSD Figure

4.3.7 Cover Mosaic

The Mosaic function realizes the coverage of the image area, which blurs the specific area.



Fig. 4-8 RGA Mosaic Figure

4.4 Register Description

4.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
RGA0	0x27920000
RGA1	0x27930000

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4.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RGA_SYS_CTRL	0x0000	W	0x00000044	RGA system control register
RGA_CMD_CTRL	0x0004	W	0x000FC000	RGA command control register
RGA_CMD_BASE	0x0008	W	0x00000000	RGA command codes base address register
RGA_STATUS1	0x000C	W	0x00000000	RGA status register
RGA_INT	0x0010	W	0x00000000	RGA interrupt register
RGA_MMU_CTRL0	0x0014	W	0x00000000	RGA MMU control 0 register
RGA_STATUS2	0x001C	W	0x00000000	RGA status register
RGA_WORK_CNT	0x0020	W	0x00000000	RGA work counter
RGA_VERSION_INFO	0x0028	W	0x00000000	RTL version and FPGA version information
RGA_READ_LINE_CNT_TH	0x0030	W	0x00001FFF	RGA read interrupt line count threshold.
RGA_WRITE_LINE_CNT_TH	0x0034	W	0x00001FFF	RGA write interrupt line threshold start and step.
RGA_INT_LINE_CNT	0x0038	W	0x00000000	Read and write line count for interrupt.
RGA_DST_CSC_00	0x0060	W	0x000000BC	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA_DST_CSC_01	0x0064	W	0x00000274	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA_DST_CSC_02	0x0068	W	0x00000040	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA_DST_CSC_OFF0	0x006C	W	0x00004200	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA_DST_CSC_10	0x0070	W	0x00000798	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA_DST_CSC_11	0x0074	W	0x000006A4	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA_DST_CSC_12	0x0078	W	0x000001C0	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA_DST_CSC_OFF1	0x007C	W	0x00020200	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA_DST_CSC_20	0x0080	W	0x000001C0	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA_DST_CSC_21	0x0084	W	0x00000668	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA_DST_CSC_22	0x0088	W	0x000007D8	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA_DST_CSC_OFF2	0x008C	W	0x00020200	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA_MODE_CTRL	0x0100	W	0x00000000	RGA mode control register
RGA_SRC_INFO	0x0104	W	0x00000000	RGA source information register
RGA_SRC_BASE0	0x0108	W	0x00000000	RGA source image Y/RGB base address register
RGA_FBCIN_HEAD_BASE	0x0108	W	0x00000000	RGA FBC source image head base address register
RGA_SRC_BASE1	0x010C	W	0x00000000	RGA source image Cb/Cbr base address register
RGA_FBCIN_PAYL_BASE	0x010C	W	0x00000000	RGA FBC source image payload base address register

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Name	Offset	Size	Reset Value	Description
RGA_SRC_BASE2	0x0110	W	0x00000000	RGA source image Cr base address register
RGA_FBCIN_ACT_OFF	0x0110	W	0x00000000	
RGA_SRC_BASE3	0x0114	W	0x00000000	RGA source image 1 base address register
RGA_SRC_VIR_INFO	0x0118	W	0x00000000	RGA source image virtual stride / RGA source image tile number register
RGA_SRC_ACT_INFO	0x011C	W	0x00000000	RGA source image active width/height register
RGA_SRC_X_FACTOR	0x0120	W	0x00000000	RGA source image horizontal scaling factor
RGA_OSD_CTRL0	0x0120	W	0x00000000	RGA OSD control register
RGA_SRC_Y_FACTOR	0x0124	W	0x00000000	RGA source image vertical scaling factor
RGA_OSD_CTRL1	0x0124	W	0x00000000	RGA OSD control register
RGA_SRC_BG_COLOR	0x0128	W	0x00000000	RGA source image background color
RGA_OSD_COLOR0	0x0128	W	0x00000000	OSD color0
RGA_SRC_FG_COLOR	0x012C	W	0x00000000	RGA source image foreground color
RGA_OSD_COLOR1	0x012C	W	0x00000000	OSD color1
RGA_MOSAIC_MODE	0x0130	W	0x00000000	RGA mosaic function mode select.
RGA_SRC_TR_COLOR0	0x0130	W	0x00000000	RGA source image transparency color min value
RGA_CP_GR_A	0x0130	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA_OSD_LAST_FLAGS0	0x0130	W	0x00000000	Flags for cur OSD auto inversion using
RGA_SRC_TR_COLOR1	0x0134	W	0x00000000	RGA source image transparency color max value
RGA_CP_GR_B	0x0134	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA_OSD_LAST_FLAGS1	0x0134	W	0x00000000	Flags for cur OSD auto inversion using
RGA_DST_INFO	0x0138	W	0x00000000	RGA destination format register
RGA_DST_BASE0	0x013C	W	0x00000000	RGA destination image base address 0 register
RGA_DST_BASE1	0x0140	W	0x00000000	RGA destination image base address 1 register
RGA_DST_BASE2	0x0144	W	0x00000000	RGA destination image base address 2 register
RGA_DST_VIR_INFO	0x0148	W	0x00000000	RGA destination image virtual width/height register
RGA_DST_ACT_INFO	0x014C	W	0x00000000	RGA destination image active width/height register
RGA_ALPHA_CTRL0	0x0150	W	0x00000000	Alpha control register 0
RGA_ALPHA_CTRL1	0x0154	W	0x00000000	Register0000 Description
RGA_FADING_CTRL	0x0158	W	0x00000000	Fading control register
RGA_PAT_CON	0x015C	W	0x00000000	Pattern size/offset register
RGA_NN_QUANTIZE_SCALE	0x0160	W	0x00000000	Quantize scale of RGB (2bit integer+8bit fraction, 0~3.99)
RGA_ROP_CON0	0x0160	W	0x00000000	ROP code 0 control register

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Name	Offset	Size	Reset Value	Description
RGA_CP_GR_G	0x0160	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA_DST_Y4MAP_LUT0	0x0160	W	0x76543210	Y4MAP LUT REGS from lut0 to lut7
RGA_OSD_INVERTSION_CAL0	0x0160	W	0x00000000	Used for OSD inversion calculation clip
RGA_NN_QUANTIZE_OFFSET	0x0164	W	0x00000000	Quantize offset of RGB (1bit signed + 8bit integer)
RGA_CP_GR_R	0x0164	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA_DST_Y4MAP_LUT1	0x0164	W	0xFEDCBA98	Y4MAP LUT REGS from lut8 to lut15
RGA_ROP_CON1	0x0164	W	0x00000000	ROP code 1 control register
RGA_OSD_INVERTSION_CAL1	0x0164	W	0x00000000	Used for OSD inversion calculation clip
RGA_MASK_BASE	0x0168	W	0x00000000	RGA mask base address register
RGA_SRC_SCL_OFFSET	0x016C	W	0x00000000	RGA mask base address register
RGA_PREFETCH_ADDR_TH	0x0170	W	0x00000000	The threshold of IOMMU pre-fetch address
RGA_OSD_ST_LUMA0	0x0400	W	0x00000000	Luminance statistics for the OSD block 0-3
RGA_OSD_ST_LUMA1	0x0404	W	0x00000000	Luminance statistics for the OSD block 4-7
RGA_OSD_ST_LUMA2	0x0408	W	0x00000000	Luminance statistics for the OSD block 8-11
RGA_OSD_ST_LUMA3	0x040C	W	0x00000000	Luminance statistics for the OSD block 12-15
RGA_OSD_ST_LUMA4	0x0410	W	0x00000000	Luminance statistics for the OSD block 16-19
RGA_OSD_ST_LUMA5	0x0414	W	0x00000000	Luminance statistics for the OSD block 20-23
RGA_OSD_ST_LUMA6	0x0418	W	0x00000000	Luminance statistics for the OSD block 24-27
RGA_OSD_ST_LUMA7	0x041C	W	0x00000000	Luminance statistics for the OSD block 28-31
RGA_OSD_ST_LUMA8	0x0420	W	0x00000000	Luminance statistics for the OSD block 32-35
RGA_OSD_ST_LUMA9	0x0424	W	0x00000000	Luminance statistics for the OSD block 36-39
RGA_OSD_ST_LUMA10	0x0428	W	0x00000000	Luminance statistics for the OSD block 40-43
RGA_OSD_ST_LUMA11	0x042C	W	0x00000000	Luminance statistics for the OSD block 44-47
RGA_OSD_ST_LUMA12	0x0430	W	0x00000000	Luminance statistics for the OSD block 48-51
RGA_OSD_ST_LUMA13	0x0434	W	0x00000000	Luminance statistics for the OSD block 52-55
RGA_OSD_ST_LUMA14	0x0438	W	0x00000000	Luminance statistics for the OSD block 56-59
RGA_OSD_ST_LUMA15	0x043C	W	0x00000000	Luminance statistics for the OSD block 60-63
RGA_DTE_ADDR	0x0F00	W	0x00000000	MMU current page Table address
RGA_STATUS	0x0F04	W	0x00000000	MMU status register
RGA_COMMAND	0x0F08	W	0x00000000	MMU command register

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Name	Offset	Size	Reset Value	Description
RGA_PAGE_FAULT_ADDR	0x0F0C	W	0x00000000	MMU logical address of last page fault
RGA_ZAP_ONE_LINE	0x0F10	W	0x00000000	MMU Zap cache line register
RGA_INT_RAWSTAT	0x0F14	W	0x00000000	MMU raw interrupt status register
RGA_INT_CLEAR	0x0F18	W	0x00000000	MMU raw interrupt status register
RGA_INT_MASK	0x0F1C	W	0x00000000	MMU raw interrupt status register
RGA_INT_STATUS	0x0F20	W	0x00000000	MMU raw interrupt status register
RGA_AUTO_GATING	0x0F24	W	0x80000000	mmu auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

4.4.3 Detail Registers Description

RGA_SYS_CTRL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	sw_src1_rgb888_fix_dis SRC1 RGB888 format 4K un-align optimization disable bit.
12	RW	0x0	sw_src0yuv420sp_rd_opt_dis SRC0 YUV420SP format read optimization disable bit.
11	RW	0x0	sw_dst_wr_opt_dis AXI write optimization disable bit(If this bit equal to 0, the write data will continuously in one whole burst)
10	W1C	0x0	sys_cmd_continue_p RGA read continue pulse, and read commands will continue to be sent.
9	RW	0x0	sw_rd_hold_mode_en RGA read hold mode enable bit, the read command will be holden when RGA raising read line count interrupt.
8	RO	0x0	reserved
7	RW	0x0	sys_rst_handsave_p It would save protect-rstn into initial status if long time dead in protect-rstn status(auto clear into '0').
6	RW	0x1	sw_rst_protect_e Protect-rstn mode enable. It would be ensure all AXI write/read operation into completion status when sw_cclk_sreset_p or sw_aclk_sreset_p valid.
5	RW	0x0	sw_auto_rst It would auto-resetn after one frame finish. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sys_cclk_sreset_p RGA core clk domain Soft reset, write '1' to this would reset the RGA engine except config registers.
3	WO	0x0	sys_aclk_sreset_p RGA aclk domain Soft reset, write '1' to this would reset the RGA engine except config registers.
2	WO	0x1	sw_auto_ckg RGA auto clock gating enable bit 1'b0: Disable 1'b1: Enable
1	WO	0x0	sw_cmd_mode RGA command mode 1'b0: Slave mode 1'b1: Master mode

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Bit	Attr	Reset Value	Description
0	W1C	0x0	sys_cmd_op_st_p Only used in passive (slave) control mode

RGA_CMD_CTRL

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:14	RW	0x3f	sw_max_rd_outstanding
13	RW	0x0	sw_outstanding_cfg_dis
12:3	RW	0x000	sw_cmd_incr_num RGA command increment number
2	WO	0x0	sw_cmd_stop_mode RGA command stop mode Command execution would stop after the current graphic operation finish if set this bit to 1.
1	WO	0x0	sys_cmd_incr_valid_p RGA command increment valid (Auto cleared) When setting this bit, 1. The total command number would increase by the RGA_INCR_CMD_NUM. 2. RGA would continue running if idle.
0	RW	0x0	sys_cmd_line_st_p RGA command line fetch start (command line reset) (Auto cleared) When fetch start, the total command number would reset to RGA_INCR_CMD_NUM.

RGA_CMD_BASE

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_cmd_base RGA command codes base address

RGA_STATUS1

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	sw_cmd_total_num RGA command total number
19:8	RO	0x000	sw_cmd_cur_num RGA command current number
7:1	RO	0x00	reserved
0	RO	0x0	sw_rga_sta RGA engine status 1'b0: Idle 1'b1: Working

RGA_INT

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	W1C	0x0	sys_intr_fbcin_dec_err_clr FBCIN DEC error interrupt clear

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Bit	Attr	Reset Value	Description
23	RW	0x0	sw_intr_fbcin_dec_err_e FBCIN DEC error interrupt enable
22	RW	0x0	ro_intr_fbcin_dec_err FBCIN DEC error interrupt
21	RO	0x0	ro_prefetch_th_intr Interruption without configuring the threshold of IOMMU prefetch.
20	W1C	0x0	sys_intr_pre_th_clr Clear interruption without configuring the threshold of IOMMU prefetch.
19	W1C	0x0	sys_intr_scl_err_clr SCL error interrupt clear
18	RW	0x0	sw_intr_scl_err_e SCL error interrupt enable
17	RO	0x0	ro_scl_error_intr SCL error interrupt flag
16	W1C	0x0	sys_intr_line_wr_clr RGA write line count interrupt clear pulse.
15	W1C	0x0	sys_intr_line_rd_clr RGA read line count interrupt clear pulse.
14	RW	0x0	sw_intr_line_wr_en RGA write line count and interrupt enable bit.
13	RW	0x0	sw_intr_line_rd_en RGA read line count and interrupt enable bit.
12	RO	0x0	ro_write_cnt_intr RGA write data line count reach threshold interrupt flag.
11	RO	0x0	ro_read_cnt_intr RGA read data line count reach threshold interrupt flag.
10	RW	0x0	sw_intr_af_e All command finished interrupt enable
9	RW	0x0	sw_intr_rpp_err_e RPP error interrupt enable
8	RW	0x0	sw_intr_bus_err_e Bus error interrupt enable
7	W1C	0x0	sys_intr_cf_clr Current command finished interrupt clear
6	W1C	0x0	sys_intr_af_clr All command finished interrupt clear
5	W1C	0x0	sys_intr_rpp_err_clr RPP error interrupt clear
4	W1C	0x0	sys_intr_bus_err_clr Bus error interrupt clear
3	RO	0x0	ro_cmd_cur_finish_intr Current command finished interrupt flag
2	RO	0x0	ro_cmd_all_finish_intr All command finished interrupt flag
1	RO	0x0	ro_rpp_error_intr RPP error interrupt flag
0	RO	0x0	ro_bus_error_intr Bus error interrupt flag

RGA_MMU_CTRL0

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17:15	RW	0x0	sw_mmu_qos_num2 RGA DATA QOS number2.
14:12	RW	0x0	sw_mmu_qos_num3 RGA MMU/CMD QOS number3.
11	RW	0x0	sw_qos_en RGA QOS enable bit.
10:9	RW	0x0	sw_els_ch_priority The priority of this channel
8:7	RW	0x0	sw_dst_ch_priority The priority of this channel
6:5	RW	0x0	sw_src1_ch_priority The priority of this channel
4:3	RW	0x0	sw_src_ch_priority The priority of this channel
2:0	RO	0x0	reserved

RGA_STATUS2

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:11	RO	0x0	rpp_mkram_rready Rpp mkram rready
10:6	RO	0x00	dstrpp_outbuf_rready Dstrpp outbuf rready
5:2	RO	0x0	srcrpp_outbuf_rready Srcrpp outbuf rready
1	RO	0x0	bus_error Bus error status
0	RO	0x0	rpp_error RPP error status

RGA_WORK_CNT

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RO	0x0000000	sw_work_cnt RGA total working counter

RGA_VERSION_INFO

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	major Used for IP structure version information
23:20	RW	0x0	minor Big feature change under same structure
19:0	RW	0x00000	svnbuild RTL current SVN number

RGA_READ_LINE_CNT_TH

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x1fff	sw_intr_line_rd_th RGA read interrupt line count threshold.

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RGA_WRITE_LINE_CNT_TH

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_intr_line_wr_step The threshold step size for RGA, and the interrupt raising when write count reach very threshold(start + N * step).
15:13	RO	0x0	reserved
12:0	RW	0x1fff	sw_intr_line_wr_start RGA write interrupt line count threshold start value.

RGA_INT_LINE_CNT

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x0000	ro_write_line_cnt RGA write interrupt line count. (Read Only)
15:14	RO	0x0	reserved
13	RO	0x0	ro_dma_cmd_hold RGA raising the dma hold when read interrupt.
12:0	RO	0x0000	ro_read_line_cnt RGA read interrupt line count. (Read Only)

RGA_DST_CSC_00

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_dst_csc_y_min Dst csc Y channel clip min value
23:16	RW	0x00	sw_dst_csc_y_max Dst csc Y channel clip max value.
15:11	RO	0x00	reserved
10:0	RW	0x0bc	sw_dst_coe_00 1bit signed+2bit integer+8bit float factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA_DST_CSC_01

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_dst_csc_uv_min Dst csc UV channel clip min value.
23:16	RW	0x00	sw_dst_csc_uv_max Dst csc UV channel clip max value.
15:11	RO	0x00	reserved
10:0	RW	0x274	sw_dst_coe_01 1bit signed+2bit integer+8bit float factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA_DST_CSC_02

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x040	sw_dst_coe_02 1bit signed+2bit integer+8bit float factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA_DST_CSC_OFF0

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x004200	sw_dst_coe_off0 1bit signed+10bit integer+10bit float factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA_DST_CSC_10

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x798	sw_dst_coe_10 1bit signed+2bit integer+8bit float factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA_DST_CSC_11

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x6a4	sw_dst_coe_11 1bit signed+2bit integer+8bit float factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA_DST_CSC_12

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x1c0	sw_dst_coe_12 1bit signed+2bit integer+8bit float factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA_DST_CSC_OFF1

Address: **Operational Base** + offset (0x007C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x020200	sw_dst_coe_off1 1bit signed+10bit integer+10bit float factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA_DST_CSC_20

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x1c0	sw_dst_coe_20 1bit signed+2bit integer+8bit float factor V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA_DST_CSC_21

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x668	sw_dst_coe_21 1bit signed+2bit integer+8bit float factor V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA_DST_CSC_22

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x7d8	sw_dst_coe_22 1bit signed+2bit integer+8bit float factor V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA_DST_CSC_OFF2

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x020200	sw_dst_coe_off2 1bit signed+10bit integer+10bit float factor V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA_MODE_CTRL

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	sw_hsp_left_copy_dis RGA HSP bicubic copy leftmost pixel as the first pixel disable bit.
20	RW	0x0	sw_axi_wr128_dis RGA AXI write size 128bit disable bit, and only support raster data as output.
19	RW	0x0	sw_table_pre_fetch_dis RGA table pre-fetch function optimization disable bit.
18	RW	0x0	sw_fbcin_bsp_dis
17	RO	0x0	reserved
16	RW	0x0	sw_fbcin_en RGA FBC input enable bit.
15:14	RW	0x0	sw_table_pre_fetch_mode RGA table pre-fetch function optimization mode. 2'b00: pre-fetch before 128KB table size 2'b01: pre-fetch before 192KB table size 2'b10: pre-fetch before 64KB table size

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Bit	Attr	Reset Value	Description
13	RW	0x0	sw_tile4x4_out_en This bit valid when RGA support TILE4X4 YUV picture as output. 1'b0: TILE4X4 output disable 1'b1: TILE4X4 output enable
12	RW	0x0	sw_tile4x4_in_en This bit valid when RGA support TILE4X4 YUV picture as input. 1'b0: TILE4X4 input disable 1'b1: TILE4X4 input enable
11	RO	0x0	reserved
10	RW	0x0	sw_yin_yout_mode RGA Y in Y out mode enable bit.
9	RW	0x0	sw_mosaic_en RGA Mosaic function enable bit.
8	RW	0x0	sw_osd_en RGA OSD function enable bit.
7	RW	0x0	sw_intr_cf_e Current command finished interrupt enable
6	RW	0x0	sw_gradient_sat Gradient saturation calculation mode 1'b0:Clip 1'b1:Not-clip
5	RW	0x0	sw_alpha_zero_key ARGB888 alpha zero key mode 0x000000 would be changed to 0x000100(RGB888)/0x0020(RGB565)for ARGB888 to RGBX/RGB565 color key. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_cf_rop4_pat Color fill/ROP4 pattern 1'b0: Solid color 1'b1: Pattern color
3	RW	0x0	sw_bb_mode Bitblt mode 1'b0: SRC + DST => DST 1'b1: SRC + SRC1 => DST
2:0	RW	0x0	sw_render_mode RGA 2D render mode 3'b000: Bitblt 3'b001: Color palette 3'b010: Rectangle fill 3'b011: Update palette LUT/pattern ram

RGA_SRC_INFO

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_hsd_mode 1'b0:Average 1'b1:Bi-linear
30	RW	0x0	sw_hsp_mode 1'b0:Bicubic 1'b1:Bi-linear

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Bit	Attr	Reset Value	Description
29	RW	0x0	sw_vsd_mode 1'b0:Average 1'b1:Bi-linear
28	RW	0x0	sw_src_yuv10_round_dis RGA round disable bit when YUV 10bit picture as input. 1'b0: YUV 10bit to 8bit round enable (default) 1'b1: YUV 10bit to 8bit round disable
27	RW	0x0	sw_src_yuv10_e This bit valid when RGA/2L support YUV 10bit picture input. 1'b0: YUV 10bit disable 1'b1: YUV 10bit enable
26	RW	0x0	sw_vsp_mode 1'b0:By-cubic 1'b1:Bi-linear
25:24	RW	0x0	sw_bic_coe_sel SRC BI-cubic scaling coefficient select 2'b00: CATROM 2'b01: MITCHELL 2'b10: HERMITE 2'b11: B-SPLINE
23	RW	0x0	sw_src_dither_up SRC dither up enable 1'b0: Disable 1'b1: Enable
22:19	RW	0x0	sw_src_trans_e Source transparency enable bits [3]: A value stencil test enable bit [2]: B value stencil test enable bit [1]: G value stencil test enable bit [0]: R value stencil test enable bit
18	RW	0x0	sw_src_trans_mode Source transparency mode 1'b0: Normal stencil test (color key) 1'b1: Inverted stencil test
17:16	RW	0x0	sw_src_vscl_mode SRC vertical scaling mode 2'b00No scaling 2'b01: Down-scaling 2'b10: Up-scaling
15:14	RW	0x0	sw_src_hscl_mode SRC horizontal scaling mode 2'b00No scaling 2'b01: Down-scaling 2'b10: Up-scaling
13:12	RW	0x0	sw_src_mir_mode SRC mirror mode 2'b00: No mirror 2'b01: X mirror 2'b10: Y mirror 2'b11: X mirror + y mirror
11:10	RW	0x0	sw_src_rot_mode SRC rotation mode 2'b00: 0 degree 2'b01: 90 degree 2'b10: 180 degree 2'b11: 270 degree

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	sw_src_csc_mode Source bitmap YUV2RGB conversion mode 2'b00: Bypass 2'b01: BT.601-range0(limit range) 2'b10: BT.601-range1(full range) 2'b11: BT.709-range0(limit range)
7	RW	0x0	sw_cp_endian Source Color palette endian swap 1'b0: Big endian 1'b1: Little endian
6	RW	0x0	sw_src_uvswap Source Cb-Cr swap 1'b0: CrCb 1'b1: CbCr For YVYU422 mode, UV swap 1'b0: YVYU422(U LSB) 1'b1: YUYV422(V LSB)
5	RW	0x0	sw_src_alpha_swap Source bitmap data alpha swap 1'b0: ABGR 1'b1: BGRA
4	RW	0x0	sw_src_rbswap Source bitmap data RB swap 1'b0: BGR 1'b1: RGB For YVYU422 mode, YC swap 1'b0: YVYU422(U LSB) 1'b1: VYUY422(Y LSB)
3:0	RW	0x0	sw_src_fmt Source bitmap data format 4'b0000: ABGR888 4'b0001: XBGR888 4'b0010: BGR packed 4'b0011: YUV444SP 4'b0100: RGB565 4'b0101: ARGB1555 4'b0110: ARGB4444 4'b0111: YVYU422(U LSB) 4'b1000: YUV422SP 4'b1001: YUV422P 4'b1010: YUV420SP 4'b1011: YUV420P 4'b1100: 1BPP (color palette) 4'b1101: 2BPP (color palette) 4'b1110: 4BPP (color palette) 4'b1111: 8BPP (color palette)

RGA_SRC_BASE0

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base0 Source image Y/RGB base address

RGA_FBCIN_HEAD_BASE

Address: **Operational Base** + offset (0x0108)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_fbcin_head_base FBC source image head base address

RGA_SRC_BASE1

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base1 Source image Cb base address (YUV422/420-P) Source image Cb/Cr base address (YU,V422/420-SP)

RGA_FBCIN_PAYL_BASE

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_fbcin_payl_base FBC source image payload base address

RGA_SRC_BASE2

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base2 Source image Cr base address (YUV422/420-P)

RGA_FBCIN_ACT_OFF

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_fbcin_act_yoff The distance in Y axis between operating pixels in FBC mode and the left side of the input source.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_fbcin_act_xoff The distance in X axis between operating pixels in FBC mode and the left side of the input source.

RGA_SRC_BASE3

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base3 Source image 1 RGB base address(source bitblt mode1)

RGA_SRC_VIR_INFO

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_mask_vir_stride Mask image virtual stride (words)
15:0	RW	0x0000	sw_src_vir_stride SRC image virtual stride (words)(also effective in FBC or tile4x4 mode)

RGA_SRC_ACT_INFO

Address: **Operational Base** + offset (0x011C)

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Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_tile4x4_in_yoff The Y offset of the first point of the input act area from the first point of TILE4X4 block.
29	RO	0x0	reserved
28:16	RW	0x0000	sw_src_act_height Source image active height(also effective in FBC or tile4x4 mode)
15:14	RW	0x0	sw_tile4x4_in_xoff The X offset of the first point of the input act area from the first point of TILE4X4 block.
13	RO	0x0	reserved
12:0	RW	0x0000	sw_src_act_width Source image active width(also effective in FBC or tile4x4 mode)

RGA_SRC_X_FACTOR

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_hsp_factor Source image horizontal up-scaling factor =((SRC_ACT_WIDTH-1)/(DST_ACT_WIDTH-1)) * 65536
15:0	RW	0x0000	sw_src_hsd_factor Source image horizontal down-scaling factor =(DST_ACT_WIDTH/(SRC_ACT_WIDTH) * 65536 + 1

RGA_OSD_CTRL0

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	sw_osd_2bpp_mode OSD 2bpp(1bit alpha, 1bit color) format.
29:20	RW	0x000	sw_osd_fix_width If sw_osd_width_mode is fix mode, use this signal. Each real OSD width = (sw_osd_fix_width+1)*2
19:10	RW	0x000	sw_osd_flags_index Cur OSD flags ID
9:4	RW	0x00	sw_osd_blk_num OSD block number
3	RW	0x0	sw_osd_width_mode OSD width mode 1'b0: Each OSD width is fix(use sw_osd_fix_width) 1'b1: Each OSD width is different (use LUT mode to load each OSD width)
2	RW	0x0	sw_osd_ver_mode OSD shape mode 1'b0: OSD is horizontal 1'b1: OSD is vertical
1:0	RW	0x0	sw_osd_mode OSD calculate mode 2'b00: OSD static disable and OSD auto inversion disable 2'b01: OSD static only mode 2'b10: OSD auto inversion only mode 2'b11: OSD static enable and OSD auto inversion enable

RGA_SRC_Y_FACTOR

Address: **Operational Base** + offset (0x0124)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_vsp_factor Source image vertical up-scaling factor =((SRC_ACT_ HEIGHT -1)/(DST_ACT_ HEIGHT -1)) * 65536
15:0	RW	0x0000	sw_src_vsd_factor Source image vertical down-scaling factor =(DST_ACT_ HEIGHT /(SRC_ACT_ HEIGHT) * 65536 + 1

RGA_OSD_CTRL1

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	sw_osd_unfix_index Cur OSD unfix width configuration ID
15	RO	0x0	reserved
14	RW	0x0	sw_osd_invert_c_dis OSD auto inversion C/RB channel disable bit
13	RW	0x0	sw_osd_invert_y_dis OSD auto inversion Y/G channel disable bit
12	RW	0x0	sw_osd_invert_a_en OSD auto inversion alpha channel enable bit
11:4	RW	0x00	sw_osd_thresh If cur OSD average luminance > sw_osd_thresh, cur osd flag=1.
3	RW	0x0	sw_osd_auto_invert_mode OSD auto inversion mode 1'b0: OSD auto inversion use (sw_osd_max - DATA) 1'b1: OSD auto inversion use swap (If YUV overlay, UV swap; If RGB overlay, RB swap)
2	RW	0x0	sw_osd_default_color OSD default color mode 1'b0: OSD default color is bright, OSD content will invert when background is bright 1'b1: OSD default color is dark, OSD content will invert when background is dark
1	RW	0x0	sw_osd_flag_sel OSD overlay use flags mode 1'b0: OSD overlay use internal data 1'b1: OSD overlay use external data(sw_osd_last_result)
0	RW	0x0	sw_osd_color_sel 1'b0: Select SRC1 data for OSD overlay content 1'b1: Select config data for OSD overlay content

RGA_SRC_BG_COLOR

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_bg_color Source image background color ("0" bit color for mono expansion.)

RGA_OSD_COLOR0

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_osd2bpp_alpha0 Substitute value for alpha to be 0 when in OSD ARGB2BPP format.

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Bit	Attr	Reset Value	Description
23:0	RW	0x000000	sw_osd_color0 This color will be used when sw_osd_color_sel is 1.

RGA_SRC_FG_COLOR

Address: **Operational Base** + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_fg_color Source image foreground color ("1" bit color for mono expansion.) Color fill color, Pan color

RGA_OSD_COLOR1

Address: **Operational Base** + offset (0x012C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_osd2bpp_alpha1 Substitute value for alpha to be 0 when in OSD ARGB2BPP format.
23:0	RW	0x000000	sw_osd_color1 This color will be used when sw_osd_color_sel is 1.

RGA_MOSAIC_MODE

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	sw_mosaic_mode RGA mosaic function mode select. 3'b000: 8 * 8 pixel 3'b001: 16 * 16 pixel 3'b010: 32 * 32 pixel 3'b011: 64 * 64 pixel 3b100: 128 * 128 pixel Others: Reserved

RGA_SRC_TR_COLOR0

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amin Source image transparency color A min value
23:16	RW	0x00	sw_src_trans_bmin Source image transparency color B min value
15:8	RW	0x00	sw_src_trans_gmin Source image transparency color G min value
7:0	RW	0x00	sw_src_trans_rmin Source image transparency color R min value

RGA_CP_GR_A

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_a Y gradient value of Alpha (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_a X gradient value of Alpha (signed 8.8)

RGA_OSD_LAST_FLAGS0

Address: **Operational Base** + offset (0x0130)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_osd_last_flags0 This signal means sw_osd_last_result[31:0]

RGA_SRC_TR_COLOR1

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amax Source image transparency color A max value
23:16	RW	0x00	sw_src_trans_bmax Source image transparency color B max value
15:8	RW	0x00	sw_src_trans_gmax Source image transparency color G max value
7:0	RW	0x00	sw_src_trans_rmax Source image transparency color R max value

RGA_CP_GR_B

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_b Y gradient value of Blue (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_b X gradient value of Blue (signed 8.8)

RGA_OSD_LAST_FLAGS1

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_osd_last_flags1 This signal means sw_osd_last_result[63:32]

RGA_DST_INFO

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	sw_src1_a1555_aconfig_en SRC1 ARGB1555 alpha 1bit config enable bit. 0 is bg_color[31:24], 1 is fg_color[31:24] .
27	RW	0x0	sw_dst_uvvds_mode Destination Cb-Cr down-sampling vertical optimization (valid for YUV420 P/SP format) 1'b0: Optimization enable 1'b1: Optimization disable
26	RW	0x0	sw_dst_nn_quantize_en Destination output RGB quantize calculate 1'b0: Quantize calculate disable 1'b1: Quantize calculate enable
25	RW	0x0	sw_dst_fmt_y4_en Destination output Y channel 4bit and UV 0bit 1'b0: Y4 out disable 1'b1: Y4 out enable
24	RW	0x0	sw_dst_fmt_yuv400_en Destination Cb-Cr output disable (valid for YUV420/2 P/SP format) 1'b0: CbCr output normal 1'b1: CbCr output disable

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Bit	Attr	Reset Value	Description
23	RW	0x0	sw_dst_uvhds_mode Destination Cb-Cr down-sampling horizontal optimization (valid for YUV420/2 P/SP format) 1'b0: Optimization enable 1'b1: Optimization disable
22	RW	0x0	sw_src1_csc_clip Src1 read BGR2YUV Clip mode(RGB from 0~255 clip to 16~235) 1'b0: Clip disable 1'b1: Clip enable
21:20	RW	0x0	sw_src1_csc_mode SRC1 read bitmap RGB2YUV conversion mode 2'b00: Bypass 2'b01: BT.601-range0,BT601_l, Y{00,255}, UV{00,255} 2'b10: BT.601-range1,BT601_f, Y{16,235}, UV{16,240} 2'b11: BT.709,Y{16,235},UV{16,240}
19	RW	0x0	sw_dst_csc_mode_2 sw_dst_csc_mode[2]+sw_dst_csc_mode[1:0]; DST read bitmap CSC(r2y/y2y) conversion mode under sw_dst_csc_mode[2]=1'b0: 3'b1xx: Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0 U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1 V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2 without clip
18	RW	0x0	sw_dst_csc_clip Dst write RGB2YUV Clip mode(RGB from 0~255 clip to 16~235) 1'b1: Clip enable 1'b0: Clip disable
17:16	RW	0x0	sw_dst_csc_mode_01 sw_dst_csc_mode[1:0] under sw_dst_csc_mode[2]=1'b0: DST read bitmap RGB2YUV conversion mode 3'b000: Bypass 3'b001: BT.601-range0,BT601_l,Y{00,255},UV{00,255} 3'b010: BT.601-range1,BT601_f,Y{16,235},UV{16,240} 3'b011: BT.709,Y{16,235},UV{16,240}
15:14	RW	0x0	sw_dither_mode DST RGB dither down bit mode 2'b00: 888 to 666 2'b01: 888 to 565 2'b10: 888 to 555 2'b11: 888 to 444 DST YUV dither down bit mode 2'b00: Y8 to Y4 2'b01:Y8 to Y1 others:Y8&0xf0
13	RW	0x0	sw_dither_down DST dither down enable 1'b0: Disable 1'b1: Enable
12	RW	0x0	sw_src1_dither_up DST/SRC1 dither up enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
11	RW	0x0	sw_src1_alpha_swap Source 1 bitmap data alpha swap 1'b0: ABGR 1'b1: BGRA
10	RW	0x0	sw_src1_rbswap Source 1 bitmap data RB swap 1'b0: BGR 1'b1: RGB
9:7	RW	0x0	sw_src1_fmt Source 1 bitmap data format 3'b000: ABGR888 3'b001: XBGR888 3'b010: BGR packed 3'b011: Alpha only 3'b100: RGB565 3'b101: ARGB1555 3'b110: ARGB4444 3'b111: Alpha only and AXI data select according to address disable
6	RW	0x0	sw_dst_uvswap Destination Cb-Cr swap 1'b0: CrCb 1'b1: CbCr
5	RW	0x0	sw_dst_alpha_swap Destination bitmap data alpha swap 1'b0: ABGR 1'b1: BGRA
4	RW	0x0	sw_dst_rbswap Destination bitmap data RB swap 1'b0: BGR 1'b1: RGB
3:0	RW	0x0	sw_dst_fmt Destination bitmap data format 4'b0000: ABGR888 4'b0001: XBGR888 4'b0010: BGR packed 4'b0011: YUV444SP 4'b0100: RGB565 4'b0101: ARGB1555 4'b0110: ARGB4444 when sw_dst_fmt_yuv400_en=1, YUV420/2 P/SP format will change to YUV400: 4'b1000: YUV422SP 4'b1001: YUV422P 4'b1010: YUV420SP 4'b1011: YUV420P only RGA has yuyv output format feature: 4'b1100: YVYU422(U, LSB) 4'b1101: YVYU420(U, LSB) 4'b1110: VYUY422(Y, LSB) 4'b1111: VYUY420(Y, LSB)

RGA_DST_BASE0

Address: **Operational Base** + offset (0x013C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base0 Destination image Y/RGB base address

RGA_DST_BASE1

Address: **Operational Base** + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base1 Destination image Cb/CbCr base address

RGA_DST_BASE2

Address: **Operational Base** + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base2 Destination image Cr base address

RGA_DST_VIR_INFO

Address: **Operational Base** + offset (0x0148)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_src1_vir_stride Source image 1 virtual stride (words)
15:0	RW	0x0000	sw_dst_vir_stride Destination image virtual stride(words)

RGA_DST_ACT_INFO

Address: **Operational Base** + offset (0x014C)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_tile4x4_out_yoff The Y offset of the first point of the output act area from the first point of TILE4X4 block.
29:28	RO	0x0	reserved
27:16	RW	0x000	sw_dst_act_height Destination image active height
15:14	RW	0x0	sw_tile4x4_out_xoff The X offset of the first point of the output act area from the first point of TILE4X4 block.
13:12	RO	0x0	reserved
11:0	RW	0x000	sw_dst_act_width Destination image active width

RGA_ALPHA_CTRL0

Address: **Operational Base** + offset (0x0150)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_mask_endian ROP4 mask endian swap 1'b0: Big endian 1'b1: Little endian
19:12	RW	0x00	sw_dst_global_alpha Global alpha value of DST(Agd)
11:4	RW	0x00	sw_src_global_alpha Global alpha value of SRC(Ags) Fading value in fading mod

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	sw_rop_mode ROP mode select 2'b00: ROP 2 2'b01: ROP 3 2'b10: ROP 4
1	RW	0x0	sw_alpha_rop_sel Alpha or ROP select 1'b0: Alpha 1'b1: ROP
0	RW	0x0	sw_alpha_rop_e Alpha or ROP enable 1'b0: Disable 1'b1: Enable

RGA_ALPHA_CTRL1

Address: **Operational Base** + offset (0x0154)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved Reserved
29	RW	0x0	sw_src_alpha_m1 SRC Transparent/opaque of alpha channel (As1) 1'b0: As 1'b1: 255-As
28	RW	0x0	sw_dst_alpha_m1 DST Transparent/opaque of alpha channel (Ad1) 1'b0: Ad 1'b1: 255-Ad
27:26	RW	0x0	sw_src_blend_m1 Alpha SRC blend mode select of alpha channel (As1_) 2'b00: Ags 2'b01: As1 2'b10: (As1*Ags)>>8 2'b11: reserved
25:24	RW	0x0	sw_dst_blend_m1 Alpha DST blend mode select of alpha channel(Ad1_) 2'b00: Agd 2'b01: Ad1 2'b10: (Ad1*Agd)>>8 2'b11: reserved
23	RW	0x0	sw_src_alpha_cal_m1 Alpha SRC calculate mode of alpha channel(As1) 1'b0: As1= As1_ + (As1_ >>7) 1'b1: As1= As1 _
22	RW	0x0	sw_dst_alpha_cal_m1 Alpha DST calculate mode of alpha channel(Ad1) 1'b0: Ad1= Ad1_ + (Ad1_ >>7) 1'b1: Ad1= Ad1_
21:19	RW	0x0	w_src_factor_m1 SRC factor mode of alpha channel(Fs1) 3'b000: 0 3'b001: 256 3'b010: Ad1 3'b011: 256-Ad1 3'b100: As1

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Bit	Attr	Reset Value	Description
18:16	RW	0x0	sw_dst_factor_m1 DST factor mode of alpha channel(Fd1) 3'b000: 0 3'b001: 256 3'b010: As1 3'b011: 256-As1 3'b100: Ad1
15	RW	0x0	sw_src_alpha_m0 Src Transparent/opaque of color channel (As0) 1'b0: As 1'b1: 255-As
14	RW	0x0	sw_dst_alpha_m0 DST Transparent/opaque of color channel (Ad0) 1'b0: Ad 1'b1: 255-Ad
13:12	RW	0x0	sw_src_blend_m0 Alpha SRC blend mode select of color channel (As0_) 2'b00: Ags 2'b01: As0 2'b10: (As0*Ags)>>8 2'b11: Reserved
11:10	RW	0x0	sw_dst_blend_m0 Alpha DST blend mode select of color channel(Ad0_) 2'b00: Agd 2'b01: Ad0 2'b10: (Ad0*Agd)>>8 2'b11: Reserved
9	RW	0x0	sw_src_alpha_cal_m0 Alpha SRC calculate mode of color channel(As0) 1'b0: As0= As0_ + (As0_ >>7) 1'b1: As0= As0 _
8	RW	0x0	sw_dst_alpha_cal_m0 Alpha DST calculate mode of color channel(Ad0) 1'b0: Ad0= Ad0_ + (Ad0_ >>7) 1'b1: Ad0= Ad0_
7:5	RW	0x0	sw_src_factor_m0 SRC factor mode of color channel(Fs0) 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0
4:2	RW	0x0	sw_dst_factor_m0 Dst factor mode of color channel(Fd0) 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0
1	RW	0x0	sw_src_color_m0 SRC color select(Cs) 1'b0: Cs 1'b1: Cs * As0

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Bit	Attr	Reset Value	Description
0	RW	0x0	sw_dst_color_m0 SRC color select(Cd) 1'b0: Cd 1'b1: Cd * Ad0

RGA_FADING_CTRL

Address: **Operational Base** + offset (0x0158)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	sw_fading_en Fading enable
23:16	RW	0x00	sw_fading_offset_b Fading offset B value
15:8	RW	0x00	sw_fading_offset_g Fading offset G value (Pattern total number when pattern loading)
7:0	RW	0x00	sw_fading_offset_r Fading offset R value (Start point of pattern ram in pattern mode)

RGA_PAT_CON

Address: **Operational Base** + offset (0x015C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pat_offset_y Pattern y offset
23:16	RW	0x00	sw_pat_offset_x Pattern x offset
15:8	RW	0x00	sw_pat_height Pattern height
7:0	RW	0x00	sw_pat_width Pattern width

RGA_NN_QUANTIZE_SCALE

Address: **Operational Base** + offset (0x0160)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_nn_quantize_scale_b Quantize scale of Blue (2bit integer+8bit fraction, 0--3.99)
19:10	RW	0x000	sw_nn_quantize_scale_g Quantize scale of Green (2bit integer+8bit fraction, 0--3.99)
9:0	RW	0x000	sw_nn_quantize_scale_r Quantize scale of Red (2bit integer+8bit fraction, 0--3.99)

RGA_ROP_CON0

Address: **Operational Base** + offset (0x0160)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:0	RW	0x0000000	sw_rop3_code0 Rop3 code 0 control bits

RGA_CP_GR_G

Address: **Operational Base** + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_g Y gradient value of Green (signed 8.8)

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	sw_gradient_x_g X gradient value of Green (signed 8.8)

RGA_DST_Y4MAP_LUT0

Address: **Operational Base** + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RW	0x76543210	sw_dst_y4map_lut0 Y4 lut from lut0 to lut7

RGA_OSD_INVERTSION_CAL0

Address: **Operational Base** + offset (0x0160)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_osd_maxc Used for OSD inversion calculation C/RB channel clip
23:16	RW	0x00	sw_osd_minc Used for OSD inversion calculation C/RB channel clip
15:8	RW	0x00	sw_osd_maxy Used for OSD inversion calculation Y/G channel clip
7:0	RW	0x00	sw_osd_miny Used for OSD inversion calculation Y/G channel clip

RGA_NN_QUANTIZE_OFFSET

Address: **Operational Base** + offset (0x0164)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:20	RW	0x000	sw_nn_quantize_offset_b Quantize offset of Blue(1bit signed + 8bit integer)
19	RO	0x0	reserved
18:10	RW	0x000	sw_nn_quantize_offset_g Quantize offset of Green (1bit signed + 8bit integer)
9	RO	0x0	reserved
8:0	RW	0x000	sw_nn_quantize_offset_r Quantize offset of Red(1bit signed + 8bit integer)

RGA_CP_GR_R

Address: **Operational Base** + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_r Y gradient value of Red(signed 8.8)
15:0	RW	0x0000	sw_gradient_x_r X gradient value of Red(signed 8.8)

RGA_DST_Y4MAP_LUT1

Address: **Operational Base** + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RW	0xfedcba98	sw_dst_y4map_lut1 Y4 lut from lut8 to lut15

RGA_ROP_CON1

Address: **Operational Base** + offset (0x0164)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:0	RW	0x0000000	sw_rop3_code1 Rop3 code 1 control bits

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RGA_OSD_INVERTSION_CAL1

Address: **Operational Base** + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	sw_osd_maxa Used for OSD inversion calculation A channel clip
7:0	RW	0x00	sw_osd_mina Used for OSD inversion calculation A channel clip

RGA_MASK_BASE

Address: **Operational Base** + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mask_base Mask base address in ROP4 mode LUT/ pattern load base address

RGA_SRC_SCL_OFFSET

Address: **Operational Base** + offset (0x016C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_src_v_factor_offset Used for bil config scl offset
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_src_h_factor_offset Used for bil config scl offset

RGA_PREFETCH_ADDR_TH

Address: **Operational Base** + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_prefetch_addr_th_uv The threshold of UV channel address for IOMMU pre-fetch.
15:0	RW	0x0000	sw_prefetch_addr_th_y The threshold of Y/RGB channel address for IOMMU pre-fetch.

RGA_OSD_ST_LUMA0

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma3 Luminance statistics for the OSD block 3
23:16	RO	0x00	ro_osd_st_luma2 Luminance statistics for the OSD block 2
15:8	RO	0x00	ro_osd_st_luma1 Luminance statistics for the OSD block 1
7:0	RO	0x00	ro_osd_st_luma0 Luminance statistics for the OSD block 0

RGA_OSD_ST_LUMA1

Address: **Operational Base** + offset (0x0404)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma7 Luminance statistics for the OSD block 7
23:16	RO	0x00	ro_osd_st_luma6 Luminance statistics for the OSD block 6

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	ro_osd_st_luma5 Luminance statistics for the OSD block 5
7:0	RO	0x00	ro_osd_st_luma4 Luminance statistics for the OSD block 4

RGA_OSD_ST_LUMA2

Address: **Operational Base** + offset (0x0408)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma11 Luminance statistics for the OSD block 11
23:16	RO	0x00	ro_osd_st_luma10 Luminance statistics for the OSD block 10
15:8	RO	0x00	ro_osd_st_luma9 Luminance statistics for the OSD block 9
7:0	RO	0x00	ro_osd_st_luma8 Luminance statistics for the OSD block 8

RGA_OSD_ST_LUMA3

Address: **Operational Base** + offset (0x040C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma15 Luminance statistics for the OSD block 15
23:16	RO	0x00	ro_osd_st_luma14 Luminance statistics for the OSD block 14
15:8	RO	0x00	ro_osd_st_luma13 Luminance statistics for the OSD block 13
7:0	RO	0x00	ro_osd_st_luma12 Luminance statistics for the OSD block 12

RGA_OSD_ST_LUMA4

Address: **Operational Base** + offset (0x0410)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma19 Luminance statistics for the OSD block 19
23:16	RO	0x00	ro_osd_st_luma18 Luminance statistics for the OSD block 18
15:8	RO	0x00	ro_osd_st_luma17 Luminance statistics for the OSD block 17
7:0	RO	0x00	ro_osd_st_luma16 Luminance statistics for the OSD block 16

RGA_OSD_ST_LUMA5

Address: **Operational Base** + offset (0x0414)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma23 Luminance statistics for the OSD block 23
23:16	RO	0x00	ro_osd_st_luma22 Luminance statistics for the OSD block 22
15:8	RO	0x00	ro_osd_st_luma21 Luminance statistics for the OSD block 21
7:0	RO	0x00	ro_osd_st_luma20 Luminance statistics for the OSD block 20

RGA_OSD_ST_LUMA6

Address: **Operational Base** + offset (0x0418)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma27 Luminance statistics for the OSD block 27
23:16	RO	0x00	ro_osd_st_luma26 Luminance statistics for the OSD block 26
15:8	RO	0x00	ro_osd_st_luma25 Luminance statistics for the OSD block 25
7:0	RO	0x00	ro_osd_st_luma24 Luminance statistics for the OSD block 24

RGA_OSD_ST_LUMA7

Address: **Operational Base** + offset (0x041C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma31 Luminance statistics for the OSD block 31
23:16	RO	0x00	ro_osd_st_luma30 Luminance statistics for the OSD block 30
15:8	RO	0x00	ro_osd_st_luma29 Luminance statistics for the OSD block 29
7:0	RO	0x00	ro_osd_st_luma28 Luminance statistics for the OSD block 28

RGA_OSD_ST_LUMA8

Address: **Operational Base** + offset (0x0420)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma35 Luminance statistics for the OSD block 35
23:16	RO	0x00	ro_osd_st_luma34 Luminance statistics for the OSD block 34
15:8	RO	0x00	ro_osd_st_luma33 Luminance statistics for the OSD block 33
7:0	RO	0x00	ro_osd_st_luma32 Luminance statistics for the OSD block 32

RGA_OSD_ST_LUMA9

Address: **Operational Base** + offset (0x0424)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma39 Luminance statistics for the OSD block 39
23:16	RO	0x00	ro_osd_st_luma38 Luminance statistics for the OSD block 38
15:8	RO	0x00	ro_osd_st_luma37 Luminance statistics for the OSD block 37
7:0	RO	0x00	ro_osd_st_luma36 Luminance statistics for the OSD block 36

RGA_OSD_ST_LUMA10

Address: **Operational Base** + offset (0x0428)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma43 Luminance statistics for the OSD block 43
23:16	RO	0x00	ro_osd_st_luma42 Luminance statistics for the OSD block 42
15:8	RO	0x00	ro_osd_st_luma41 Luminance statistics for the OSD block 41

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	ro_osd_st_luma40 Luminance statistics for the OSD block 40

RGA_OSD_ST_LUMA11

Address: **Operational Base** + offset (0x042C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma47 Luminance statistics for the OSD block 47
23:16	RO	0x00	ro_osd_st_luma46 Luminance statistics for the OSD block 46
15:8	RO	0x00	ro_osd_st_luma45 Luminance statistics for the OSD block 45
7:0	RO	0x00	ro_osd_st_luma44 Luminance statistics for the OSD block 44

RGA_OSD_ST_LUMA12

Address: **Operational Base** + offset (0x0430)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma51 Luminance statistics for the OSD block 51
23:16	RO	0x00	ro_osd_st_luma50 Luminance statistics for the OSD block 50
15:8	RO	0x00	ro_osd_st_luma49 Luminance statistics for the OSD block 49
7:0	RO	0x00	ro_osd_st_luma48 Luminance statistics for the OSD block 48

RGA_OSD_ST_LUMA13

Address: **Operational Base** + offset (0x0434)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma55 Luminance statistics for the OSD block 55
23:16	RO	0x00	ro_osd_st_luma54 Luminance statistics for the OSD block 54
15:8	RO	0x00	ro_osd_st_luma53 Luminance statistics for the OSD block 53
7:0	RO	0x00	ro_osd_st_luma52 Luminance statistics for the OSD block 52

RGA_OSD_ST_LUMA14

Address: **Operational Base** + offset (0x0438)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma59 Luminance statistics for the OSD block 59
23:16	RO	0x00	ro_osd_st_luma58 Luminance statistics for the OSD block 58
15:8	RO	0x00	ro_osd_st_luma57 Luminance statistics for the OSD block 57
7:0	RO	0x00	ro_osd_st_luma56 Luminance statistics for the OSD block 56

RGA_OSD_ST_LUMA15

Address: **Operational Base** + offset (0x043C)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	ro_osd_st_luma63 Luminance statistics for the OSD block 63
23:16	RO	0x00	ro_osd_st_luma62 Luminance statistics for the OSD block 62
15:8	RO	0x00	ro_osd_st_luma61 Luminance statistics for the OSD block 61
7:0	RO	0x00	ro_osd_st_luma60 Luminance statistics for the OSD block 60

RGA_DTE_ADDR

Address: **Operational Base** + offset (0x0F00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr MMU current page Table address

RGA_STATUS

Address: **Operational Base** + offset (0x0F04)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	page_fault_bus_id Index of master reponsible for last page fault.
5	RO	0x0	page_fault_is_write The direction of access for last page fault 1'b0: Read 1'b1: Write
4	RO	0x0	replay_buffer_empty The MMU replay buffer is empty
3	RO	0x0	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated accesses
2	RO	0x0	stail_active MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	page_fault_active MMU page fault mode currently enabled . The mode is enabled by command
0	RO	0x0	paging_enabled Paging is enabled

RGA_COMMAND

Address: **Operational Base** + offset (0x0F08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	WO	0x0	mmu_cmd MMU_CMD. This can be 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE 3'b110: MMU_FORCE_RESET

RGA_PAGE_FAULT_ADDR

Address: **Operational Base** + offset (0x0F0C)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	page_fault_addr Address of last page fault.

RGA_ZAP_ONE_LINE

Address: **Operational Base** + offset (0x0F10)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	mmu_zap_one_line Address to be invalidated from the page table cache.

RGA_INT_RAWSTAT

Address: **Operational Base** + offset (0x0F14)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error
0	RW	0x0	page_fault Page fault

RGA_INT_CLEAR

Address: **Operational Base** + offset (0x0F18)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	read_bus_error Read bus error
0	WO	0x0	page_fault Page fault

RGA_INT_MASK

Address: **Operational Base** + offset (0x0F1C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error
0	RW	0x0	page_fault Page fault

RGA_INT_STATUS

Address: **Operational Base** + offset (0x0F20)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	read_bus_error Read bus error
0	RO	0x0	page_fault Page fault

RGA_AUTO_GATING

Address: **Operational Base** + offset (0x0F24)

Bit	Attr	Reset Value	Description
31	RW	0x1	sw_mmu_old_en mmu old version enable, need set 1.
30:1	RO	0x00000000	reserved
0	RW	0x0	mmu_auto_gating When it is 1'b1, the mmu will auto gating it self.

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4.5 Application Notes

4.5.1 Register Partition

There are two types of register in RGA. The first part registers (0x0 - 0xFC) are general registers for system configuration including command mode, command parameter, RGA status, general interrupts. The other registers (from 0x100) are command registers for command codes.

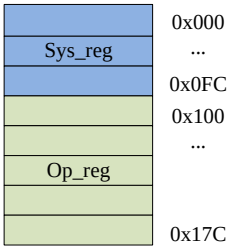


Fig. 4-9 RGA software main register-region

4.5.2 Command Modes

RGA has two command modes: slave mode and master mode. In salve mode (RGA_SYS_CTRL[1] = 1'b0), 2D graphic command only could be run one by one. CPU set all the command registers in RGA and then start RGA running by setting RGA_SYS_CTRL[0] to 1. In master mode (RGA_SYS_CTRL[1] = 1'b1), 2D graphic commands could be run sequentially. After setting command's number to RGA_CMD_CTRL[12:3], writing 1 to RGA_CMD_CTRL[0] will start the command fetch, then Internal command DMA fetch commands from external command line.

Command line is a collection of several command codes with continuous address. At the first start, the command start address (RGA_CMD_ADDR) and command number (RGA_CMD_CTRL[12:3]) should be set, then write 1 to cmd_line_st (RGA_CMD_CTRL[0]) to start the command line fetch. Incremental command is supported by setting cmd_incr_num (RGA_CMD_CTRL[12:3]) and cmd_incr_valid (RGA_CMD_CTRL[1]=1'b1).

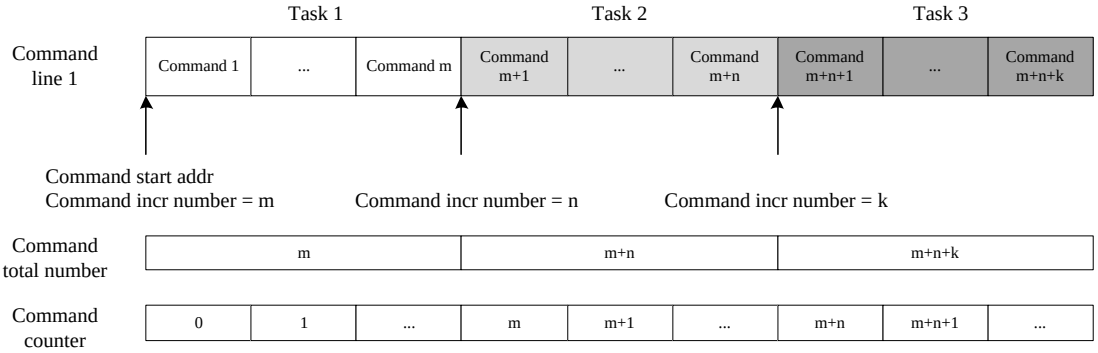


Fig. 4-10 RGA command line and command counter

4.5.3 Command Sync

In slave command mode, command sync is controlled by CPU.
In master command mode, user can enable the current_cmd_int (sw_intr_cf), command by command to generate a interrupt at the end point of target command operation.

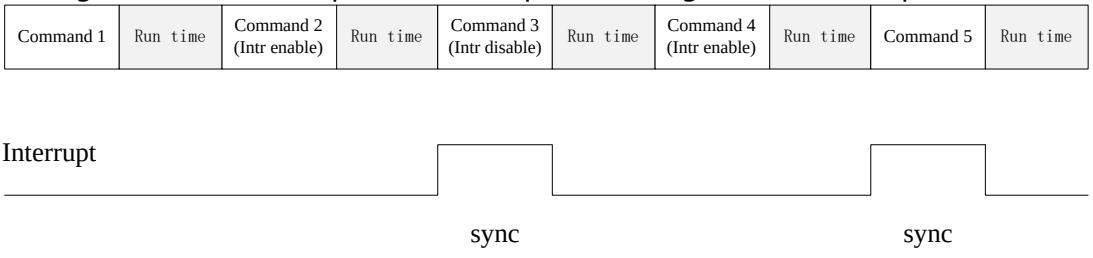


Fig. 4-11 RGA command sync generation

4.5.4 Color Palette Application Notes

1. Palette/LUT Load into special RAM in ELS_BUF_CTRL.
2. Color Palette/Pattern interval operations no need to initial LUT/pattern ram if LUT/pattern content no update.

4.5.5 OSD Automatic Inversion Application Notes

1. In horizontal mode, the width must be greater than or equal to the height, and vice versa.
2. Supports up to 64 OSD blocks, and the width of each OSD ranges from 8 to 2048, so that the size of the OSD area supports up to 4096.
3. The format of SRC0 and the format of DST need to be equal.
4. SRC0 sources format support in YUV422 P/SP,YUV420 P/SP.
5. In OSD width variable mode, the maximum supported width is 512.
6. OSD inverse flags can be configured externally or read from internal storage, and the internal storage supports a maximum of 1024 flags.
7. OSD sources in ARGB2BPP format virtual stride need 32pixel(64bits) align.
8. At least one of the sw_auto_rst or sw_auto_ckg register needs to be closed when using OSD unfix width function.

4.5.6 Some Special Application Constraints

1. The algorithm of vertical scale up: must select BI-cubic algorithm when source picture is smaller or equal to 2k and must select BI-linear when bigger than 2k.

2. The effects that The output’s definition is near 2k or 4k may not very well when at the scenario that the vertical side is scale up and the horizontal is scale down within range of 2%(such as:2048x32, 2008x64).

3. At the scenario A+B->C(A means SRC0, B means DST, C means SRC1), the size among the A B C has some constraints:
A’s size after scale must be equal to C. C’s size must equal to B when A+C is no rotation.
C’s rotation (90degree)size must equal to B1 when A+C is rotation 90 degree.

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Chapter 5 DECOM

5.1 Overview

DECOM can decompress compressed files in GZIP, DEFALTE and ZLIB formats. DECOM controller supports the following features:

- Support for decompressing GZIP files
- Support for decompressing data in DEFLATE format
- Support for decompressing data in ZLIB format
- Not support for decompressing LZ4 files
- There is a 32bit APB slave interface for configuring decompression parameters and querying register status
- There is a 128-bit AXI master interface for reading compressed data and outputting decompressed data. The AXI master interface supports burst 4/8/16 and single transmissions
- Support one internal 128-bit wide and 64-location deep FIFO(RX_FIFO) for caching source compressed data
- Support one internal 24-bit wide and 64-location deep FIFO(HF_FIFO) for caching intermediate data during decompression
- Built-in a 8KB two-port RAM for storing decompressed data
- Support complete interrupt and error interrupt output
- Support the limit_size function of the decompressed data to prevent the memory from being maliciously destroyed during the decompression process
- Support software to stop the decompression process

5.2 Block Diagram

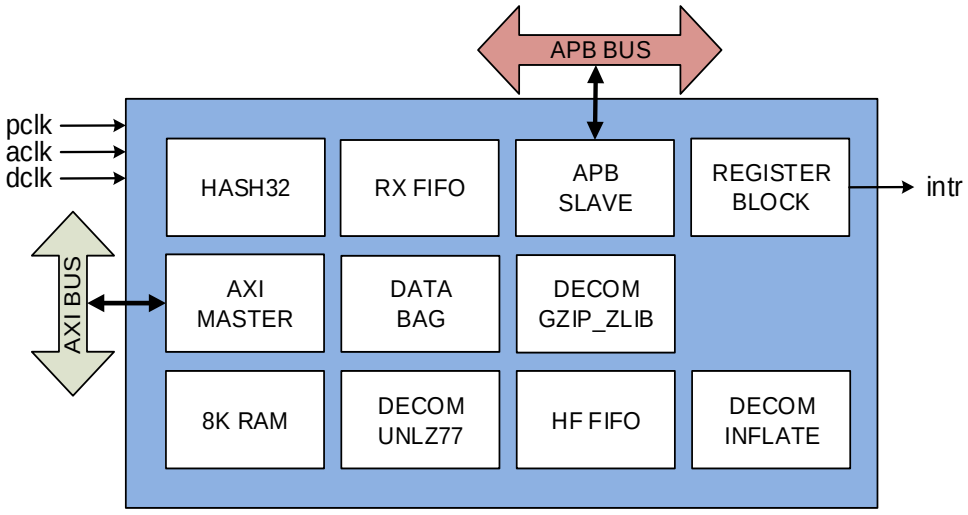


Fig. 5-1 DECOM Block Diagram

5.3 Function Description

5.3.1 Module Introduction

5.3.1.1 APB INTERFACE

The APB slave interface is used for registers configuration, decompression file parameter reading and interrupt status query, etc.

5.3.1.2 AXI MASTER INTERFACE

The AXI master interface is used to read compressed file data from external storage into the RX_FIFO and output the decompressed data to external storage.

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5.3.1.3 RX_FIFO

The RX_FIFO is used to buffer the source compressed file data read back through the AXI master interface. The RX_FIFO is an asynchronous FIFO, the write interface uses aclk, and the read interface uses dclk.

5.3.1.4 Data Bag

The Data Bag reads and bites the data in the RX_FIFO, and extracts the corresponding number of bits according to the needs of the decompression module.

5.3.1.5 GZIP_ZLIB

The GZIP_ZLIB module is used to perform file header and file end parsing for compressed files in GZIP format and compressed data in ZLIB format, and the compressed data portion is decompressed by the INFLATE module. The GZIP or ZLIB decompression mode can be configured by configuring the CTRL register.

5.3.1.6 INFLATE Module

INFLATE Module is used to decompress compressed files in DEFLATE format, implement static/dynamic huffman decoding, decompress compressed data in DEFLATE format into LZ77 format (match length-match distance) data pairs or character data, and store them in HF_FIFO.

5.3.1.7 HF_FIFO

The HF_FIFO is used to buffer the LZ77 format (match length-match distance) data pair or character data decompressed by the INFLATE module, and wait for the UNLZ77 module to further decompress the intermediate data. The HF_FIFO is an asynchronous FIFO, the write interface uses dclk, and the read interface uses aclk.

5.3.1.8 UNLZ77 Module

UNLZ77 is used to implement LZ77 decoding and store the decompressed data in 8K RAM. When the matching distance is less than 8k byte, matching replication is performed in 8K RAM. When the matching distance is greater than 8k byte, the AXI master interface is controlled to perform matching replication in the external storage.

5.3.1.9 8K-RAM

The 8K RAM is used to buffer the decompressed data. During the decompression process, the UNLZ77 module also performs read access to the RAM to complete the data matching.

5.3.1.10 Interface and Clock

The 32-bit APB Slave interface in DECOM is used for register configuration and interrupt status query interface, using pclk as the interface clock.

DECOM uses 128bit AXI master interface to realize the functions of reading the data to be compressed, decompressing the data output and reading external matching data; it should be noted that the AXI master interface supports Single and Burst transmission, which only supports incr4, incr8 and Incr16 three transmission types, does not support Wrap transmission. DECOM automatically configures the burst type according to the length of the transmitted data and the starting address. The software configuration is not supported to select the burst type.

DECOM has three sets of clock and reset inputs, pclk and presetn, dclk and drstn, aclk and aresetn. Among them pclk and aclk are APB and AXI bus clocks respectively, and dclk is decompression clock.

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5.3.2 Data Flow

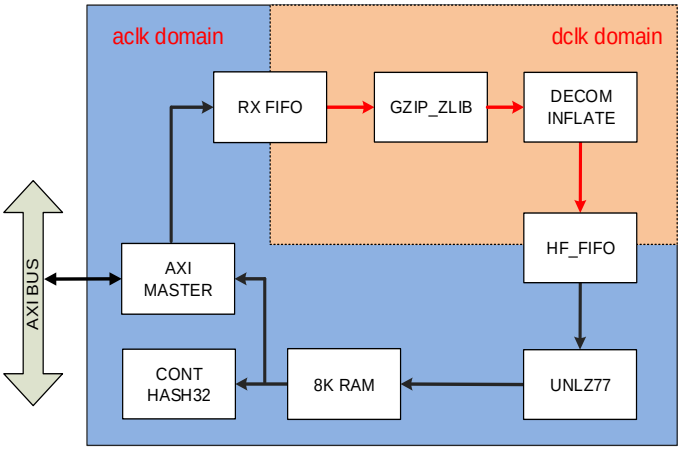


Fig. 5-2 DECOM Data Flow

5.4 Register Description

5.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

5.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DECOM_CTRL	0x0000	W	0x00000000	Control Register
DECOM_ENR	0x0004	W	0x00000000	Enable Register
DECOM_RADDR	0x0008	W	0x00000000	Read Address
DECOM_WADDR	0x000C	W	0x00000000	Write Address
DECOM_UDDSL	0x0010	W	0xFFFFFFFF	Undecompressed Data Size
DECOM_UDDSH	0x0014	W	0xFFFFFFFF	Undecompressed Data Size
DECOM_TXTHR	0x0018	W	0x00000100	Transmit Threshold Level
DECOM_SLEN	0x0020	W	0x00000000	INFLATE Store Length
DECOM_STAT	0x0024	W	0x00000000	DECOM Status Register
DECOM_ISR	0x0028	W	0x00000000	Interrupt Status Register
DECOM_IEN	0x002C	W	0x00000000	Interrupt Enable Register
DECOM_AXI_STAT	0x0030	W	0x00000010	AXI Master Interface State
DECOM_TSIZEL	0x0034	W	0x00000000	Decompressed Data Total Size Lower 32bit
DECOM_TSIZEH	0x0038	W	0x00000000	Decompressed Data Total Size Upper 32bit
DECOM_MGNUM	0x003C	W	0x00000000	LZ4 File Magic Number
DECOM_FRAME	0x0040	W	0x00000000	LZ4 File Frame Descriptor
DECOM_DICTID	0x0044	W	0x00000000	Dictionary ID
DECOM_CSL	0x0048	W	0x00000000	LZ4 Content Size(CS) Lower 32-bits
DECOM_CSH	0x004C	W	0x00000000	LZ4 Content Size(CS) Upper 32-bits
DECOM_LMTSL	0x0050	W	0xFFFFFFFF	Limit Size of Decompressed Data
DECOM_LMTSH	0x0054	W	0xFFFFFFFF	Limit Size of Decompressed Data
DECOM_GZFHD	0x0058	W	0x00000000	GZIP/ZLIB File Header Information
DECOM_VERSION	0x00F0	W	0x20211216	DECOM Version Number

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-*

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Double WORD (64 bits) access

5.4.3 Detail Registers Description

DECOM_CTRL

Address: Operational Base (0x2AC30000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ZLIBM ZLIB mode. 1'b0: Disable 1'b1: Enable When decompressing ZLIB compressed data, ZLIBM must be enabled and DEM should be set to 1.
4	RW	0x0	GZIPM GZIP mode. 1'b0: Disable 1'b1: Enable When decompressing GZIP files, GZIPM must be enabled and DEM should be set to 1.
3	RW	0x0	CCEN LZ4 content checksum check enable. 1'b0: Disable 1'b1: Enable In LZ4 files, a 32-bits content checksum will be appended at the end of the file. When CCEN is enabled, DECOM will verify the content checksum to check if the decompressed data is correct. Only valid when decompressing LZ4 files.
2	RW	0x0	BCEN LZ4 block checksum check enable. Not used. 1'b0: Disable 1'b1: Enable In LZ4 files, each data block will be followed by a 4-bytes checksum, calculated by using the xxHash-32 algorithm on the compressed data block. The intention is to detect data corruption(storage or transmission errors) immediately, before decoding. When BCEN is enabled, DECOM will check the block checksum to determine if the block to be decompressed is correct. Only valid when decompressing LZ4 files.
1	RW	0x0	HCEN LZ4 header checksum check enable. Not used. 1'b0: Disable 1'b1: Enable The LZ4 header contains a 1-byte xxh32 checksum value(HC). When HCEN is enabled, DECOM will check the HC to check if the header is correct. Only valid when decompressing LZ4 files.
0	RW	0x0	DEM DECOM mode select. 1'b0: UNLZ4 mode. Decompress the file in LZ4 format. 1'b1: INFLATE mode. Decompress the file in INFLATE format. If GZIPM=1'b1 or GZLIBM=1'b1, DEM must be set 1.

DECOM_ENR

Address: Operational Base (0x2AC30000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	R/WSC	0x0	ENR Enables and disables all decompress operations. 1'b0: Disable decompressor 1'b1: Enable decompressor to work All FIFO buffers and aclk/dclk domain work registers are cleared when the device is disabled. Self clear when decompression is complete. The ENR should be enabled after the other registers are configured.

DECOM_RADDR

Address: Operational Base (0x2AC30000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	RADDR Read address. This register is used to configure the starting address of the file to be decompressed.

DECOM_WADDR

Address: Operational Base (0x2AC30000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	WADDR Write address. This register is used to configure the starting address of the location where the decompressed data is written. Note: WADDR[31:0] must be configured with a 128bit aligned address (WADDR[3:0]==4'b0).

DECOM_UDDSL

Address: Operational Base (0x2AC30000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	UDDSL Undecompressed data size lower 32bits. (Unit:byte) UDDS[63:0] is the total size of undecompressed file. DECOM will read the compressed file data according to the value of UDDS[63:0], but the configuration of this register is optional. If this register is not configured, DECOM will use the default value of 64'hffff_ffff_ffff_ffff, and DECOM will keep reading data until the current decompression process ends.

DECOM_UDDSH

Address: Operational Base (0x2AC30000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	UDDSH Undecompressed data size higher 32bits.

DECOM_TXTHR

Address: Operational Base (0x2AC30000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000100	TXTHR When the number of 8K_MEM entries is greater than or equal to this value, the DECOM will automatically transfer the data in the 8K_MEM to the external via the AXI Master interface. The value ranges is 0~7680.(Unit:byte)

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DECOM_SLEN

Address: Operational Base (0x2AC30000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	SLEN INFLATE store block size. (Unit:byte) Indicate the block size when decompressing the store block of INFALTE file. For debugging SLC_ERR.

DECOM_STAT

Address: Operational Base (0x2AC30000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	LAST Used to indicate whether the currently processed compressed data block is the last one. 1'b0: Not last block 1'b1: Last block
0	RO	0x0	COMPLETE DECOM complete flag. 1'b0: Not complete 1'b1: Decompress is complete with no error Only decompress total complete with no error, this flag is set to 1.

DECOM_ISR

Address: Operational Base (0x2AC30000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	W1C	0x0	DSOLI Decompressed data size over limit_size interrupt. 1'b0: Interrupt is not active 1'b1: Interrupt is active
18	W1C	0x0	ZDICTEI ZLIB dictionary error interrupt. 1'b0: Interrupt is not active 1'b1: Interrupt is active
17	W1C	0x0	GCMEI GZIP/ZLIB compression method check error interrupt. 1'b0: Interrupt is not active 1'b1: Interrupt is active
16	W1C	0x0	GIDEI GZIP ID error interrupt. 1'b0: Interrupt is not active 1'b1: Interrupt is active
15	W1C	0x0	CCCEI UNLZ4 content checksum check error interrupt. 1'b0: ccc_err interrupt is not active 1'b1: ccc_err interrupt is active
14	W1C	0x0	BCCEI UNLZ4 block checksum check error interrupt. 1'b0: bcc_err interrupt is not active 1'b1: bcc_err interrupt is active
13	W1C	0x0	HCCEI UNLZ4 header checksum check error interrupt. 1'b0: hcc_err interrupt is not active 1'b1: hcc_err interrupt is active

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Bit	Attr	Reset Value	Description
12	W1C	0x0	CSEI UNLZ4 content size (or GZIP isize) error interrupt. 1'b0: cs_err interrupt is not active 1'b1: cs_err interrupt is active
11	W1C	0x0	DICTEI UNLZ4 dictionary error interrupt. 1'b0: Interrupt is not active 1'b1: Interrupt is active
10	W1C	0x0	VNEI UNLZ4 version number error interrupt. 1'b0: vn_err interrupt is not active 1'b1: vn_err interrupt is active
9	W1C	0x0	MNEI UNLZ4 magic number error interrupt. 1'b0: mn_err interrupt is not active 1'b1: mn_err interrupt is active
8	W1C	0x0	RDCEI AXI read channel error interrupt. 1'b0: INFLATE AXI RDC_ERR interrupt is not active 1'b1: INFLATE AXI RDC_ERR interrupt is active
7	W1C	0x0	WRCEI AXI write channel error interrupt. 1'b0: INFLATE AXI WRC_ERR interrupt is not active 1'b1: INFLATE AXI WRC_ERR interrupt is active
6	W1C	0x0	DISEI INFLATE huffman distance error interrupt. 1'b0: INFLATE HFDIS_ERR interrupt is not active 1'b1: INFLATE HFDIS_ERR interrupt is active
5	W1C	0x0	LENEI INFLATE huffman length error interrupt. 1'b0: INFLATE HFLEN_ERR interrupt is not active 1'b1: INFLATE HFLEN_ERR interrupt is active
4	W1C	0x0	LITEI INFLATE huffman literal error interrupt. 1'b0: INFLATE HFLIT_ERR interrupt is not active 1'b1: INFLATE HFLIT_ERR interrupt is active
3	W1C	0x0	SQMEI INFLATE SQ match error interrupt. 1'b0: INFLATE SQM_ERR interrupt is not active 1'b1: INFLATE SQM_ERR interrupt is active
2	W1C	0x0	SLCEI INFLATE store block length check error interrupt. 1'b0: INFLATE SLC_ERR interrupt is not active 1'b1: INFLATE SLC_ERR interrupt is active
1	W1C	0x0	HDEI INFLATE file header error interrupt. 1'b0: INFLATE header error interrupt is not active 1'b1: INFLATE header error interrupt is active
0	W1C	0x0	DSI DECOM stop interrupt. 1'b0: Decompression stop interrupt is not active 1'b1: Decompression stop interrupt is active This interrupt indicates that DECOM has stopped working. Including decompression completion or decompression encountered an error.

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DECOM_IEN

Address: Operational Base (0x2AC30000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	DSOLIEN Decompressed data size over limit_size interrupt enable. 1'b0: Disable 1'b1: Enable
18	RW	0x0	ZDICTEIEN ZLIB dictionary error interrupt enable. 1'b0: Disable 1'b1: Enable
17	RW	0x0	GCMEIEN GZIP/ZLIB compression method error interrupt enable. 1'b0: Disable 1'b1: Enable
16	RW	0x0	GIDEIEN GZIP ID error interrupt enable. 1'b0: Disable 1'b1: Enable
15	RW	0x0	CCCEIEN UNLZ4 content checksum check error interrupt enable. 1'b0: Disable 1'b1: Enable
14	RW	0x0	BCCEIEN UNLZ4 block checksum check error interrupt enable. 1'b0: Disable 1'b1: Enable
13	RW	0x0	HCCEIEN UNLZ4 header checksum check error interrupt enable. 1'b0: Disable 1'b1: Enable
12	RW	0x0	CSEIEN UNLZ4 content size (or GZIP isize) error interrupt enable. 1'b0: Disable 1'b1: Enable
11	RW	0x0	DICTEIEN UNLZ4 dictionary error interrupt enable. 1'b0: Disable 1'b1: Enable
10	RW	0x0	VNEIEN UNLZ4 version number error interrupt enable. 1'b0: Disable 1'b1: Enable
9	RW	0x0	WNEIEN UNLZ4 magic number error interrupt enable. 1'b0: Disable 1'b1: Enable
8	RW	0x0	RDCEIEN AXI read channel error interrupt enable. 1'b0: Disable 1'b1: Enable
7	RW	0x0	WRCEIEN AXI write channel error interrupt enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
6	RW	0x0	DISEIEN INFLATE huffman distance error interrupt enable. 1'b0: Disable 1'b1: Enable
5	RW	0x0	LENEIEN INFLATE huffman length error interrupt enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	LITEIEN INFLATE huffman literal error interrupt enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	SQMEIEN INFLATE SQ match error interrupt enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	SLCIEN INFLATE store block length check error interrupt enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	HDEIEN INFLATE file header error interrupt enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	DSIEN DECOM stop interrupt enable. 1'b0: Disable 1'b1: Enable

DECOM_AXI_STAT

Address: Operational Base (0x2AC30000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x1	AXI_IDLE AXI master idle state register. 1'b0: AXI master is busy 1'b1: AXI master is idle When the decompression is aborted, DECOM will wait for AXI master's current read/write transfer to complete, that is, wait for AXI_IDLE=1, then reset DECOM, otherwise the uncompleted AXI transmission will cause AXI bus exception. It should be noted that after the decompression is abnormal, the AXI master's unfinished write operation will continue, but the output value of wstrb[15:0] will become 16'b0.
3:2	RO	0x0	RRESP AXI read channel response state.
1:0	RO	0x0	BRESP AXI write channel response state.

DECOM_TSIZEL

Address: Operational Base (0x2AC30000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TSIZEL The total size of the data after decompression. TSIZE[63:0]. (Unit:byte)

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DECOM_TSIZEH

Address: Operational Base (0x2AC30000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TSIZEH The total size of the data after decompression.

DECOM_MGNUM

Address: Operational Base (0x2AC30000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	MGNUM Magic number of LZ4 is 0x184D2204. If the MGNUM is not 0x184D2204, a magic number error(mn_err) will be generated. And DECOM will stop decompressing.

DECOM_FRAME

Address: Operational Base (0x2AC30000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	HCC Header checksum byte. One-byte checksum of combined descriptor fields, including optional ones. The value is the second byte of xxh32() using zero as a see, and the full frame descriptor as an input (including optional fields when they are present). A wrong checksum indicates an error in the descriptor. Header checksum is informational and can be skipped. The header checksum check function can be enabled by controlling the HCEN enable signal in the CTRL register. After being turned on, DECOM calculates the hash32 check value based on the data of the frame descriptor part of the LZ4 compressed file, and performs the header checksum byte in the file. In contrast, if they are not equal, an HCC error will be generated and an interrupt will be generated.
15:8	RO	0x00	BD BD byte. Including Block Maximum Size information. This information is useful to help the decoder allocate memory. Size here refers to the original(uncompressed) data size.
7:6	RO	0x0	VN_NUM Version number. 2-bits field, must be set to 2'b01. Any other value cannot be decoded by this version of the specification. If the version number is error, Version number error(VNE) will be generated.
5	RO	0x0	BCC_FLG Block checksum flag. If this flag is set, each data block will be followed by a 4-bytes checksum, calculated by using the xxHash-32 algorithm on the raw (compressed) data block. The intention is to detect data corruption (storage or transmission errors) immediately, before decoding. Block checksum usage is optional.

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Bit	Attr	Reset Value	Description
4	RO	0x0	BIND_FLG Block independence flag. If this flag is set to "1", blocks are independent. If this flag is set to "0", each block depends on previous ones (up to LZ4 window size, which is 64 KB). In such case, it's necessary to decode all blocks in sequence. Block dependency improves compression ratio, especially for small blocks. On the other hand, it makes random access or multi-threaded decoding impossible. For debugging.
3	RO	0x0	CS_FLG Content size flag. If this flag is set, the uncompressed size of data included within the frame will be present as an 8 bytes unsigned little endian value, after the flags. Content size usage is optional.
2	RO	0x0	CCC_FLG Content checksum flag. If this flag is set, a 32-bits content checksum will be appended after the EndMark.
1	RO	0x0	reserved
0	RO	0x0	DICT_FLG Dictionary ID flag. If this flag is set, a 4-bytes Dict-ID field will be present, after the descriptor flags and the Content Size. If this flag is set, Dictionary ID error will be generated. DECOM will stop decompressing.

DECOM_DICTID

Address: Operational Base (0x2AC30000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DICTID Dictionary ID in the compressed file header. Dictionary ID is only present if the DID_FLG is set. It works as a kind of "known prefix" which is used by both the compressor and the decompressor to "warm-up" reference tables.

DECOM_CSL

Address: Operational Base (0x2AC30000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CSL Content size(CS) lower 32-bits. (Unit:byte) CS[63:0] is the original(uncompressed) size. This information is optional in LZ4 file header, and only present if CS_FLG is set. CS[63:0]={CSH, CSL};

DECOM_CSH

Address: Operational Base (0x2AC30000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	CSH Content size(CS) upper 32-bits.

DECOM_LMTSL

Address: Operational Base (0x2AC30000) + offset (0x0050)

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Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	LMTSL Limit size of decompressed data lower 32bits. (Unit:byte) When the amount of decompressed data is greater than the LMTS, DSOLI interrupt is generated and the decompression process is stopped.

DECOM_LMTSH

Address: Operational Base (0x2AC30000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	LMTSH Limit size of decompressed data higher 32bits.

DECOM_GZFHD

Address: Operational Base (0x2AC30000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	GZFHD GZIP/ZLIB file header information. When GZIPM = 1, GZFHD is GZIP file header information. When ZLIBM = 1, GZFHD is ZLIB file header information.

DECOM_VERSION

Address: Operational Base (0x2AC30000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000926	VERSION Version number = 32'h2021_1216.

5.5 Application Notes

- After configuring the decompression mode and other decompression parameters, configure the decompression enable register ENR
- When the decompression is not completed, setting ENR from 1 to 0 will force the decompression process to stop and DECOM will return to the IDLE state. Need to reconfigure and enable DECOM to start the next decompression
- When an error is encountered in the decompression, DECOM will immediately stop the decompression process, set the relevant status register, and generate the corresponding interrupt
- After the decompression process is stopped, ENR will automatically change to 0
- After the decompression process is stopped, DSI will be set to 1. If DSIEN is 1, an interrupt will be generated; if DSIEN is 0, no interrupt will be generated
- After the decompression process is stopped, COMPLETE (DECOM_STAT[0]) is not set to 1 if there is an error in the decompression process; COMPLETE is set to 1 only when the decompression is complete and there are no errors

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Chapter 6 Video Capture (VICAP)

6.1 Overview

The Video Capture, receives the data from Camera via MIPI or DVP, and transfers the data into system main memory by AXI bus or transfers the data into ISP.

- Support BT.601 RAW8/10/12 YCbCr 422 8-bit input
- Support BT.656 YCbCr 422 8-bit progressive/interlaced input
- Support 16-pins BT.1120 YCbCr 422 8-bit progressive/interlaced input
- Support 2/4 mixed BT.656/BT.1120 YCbCr 422 input
- Support dual-edge sampling for BT.656/BT.1120
- Support receiving five groups of MIPI CSI interfaces, up to four IDs for each group
- Support VC/DT configurable for each ID
- Support ten MIPI CSI data formats: RAW8/10/12/14/16, RGB888, YUV422 8bit, YUV422 8bit interlaced, YUV420 8bit, Legacy YUV420 8bit
- Support three modes of MIPI CSI HDR: virtual channel mode, identification code mode, line counter mode
- Support window cropping
- Support 8/16/32 times down-sampling for RAW data
- Support RAW 2x2 binning
- Support pixel extraction from 2x2 pattern
- Support UV mean down-sampling for YUV422
- Support reducing frame rate
- Support compact/non-compact output format for RAW data
- Support NV16/NV12/YUV400/YUYV output format for YUV data
- Support virtual stride when write to DDR
- Support DMA burst gather 2/4/8
- Support MMU
- Support QOS(hurry/press)
- Support sending RAW data directly to ISP
- Support soft reset, auto-reset when DMA error
- Support debug mode

6.2 Block Diagram

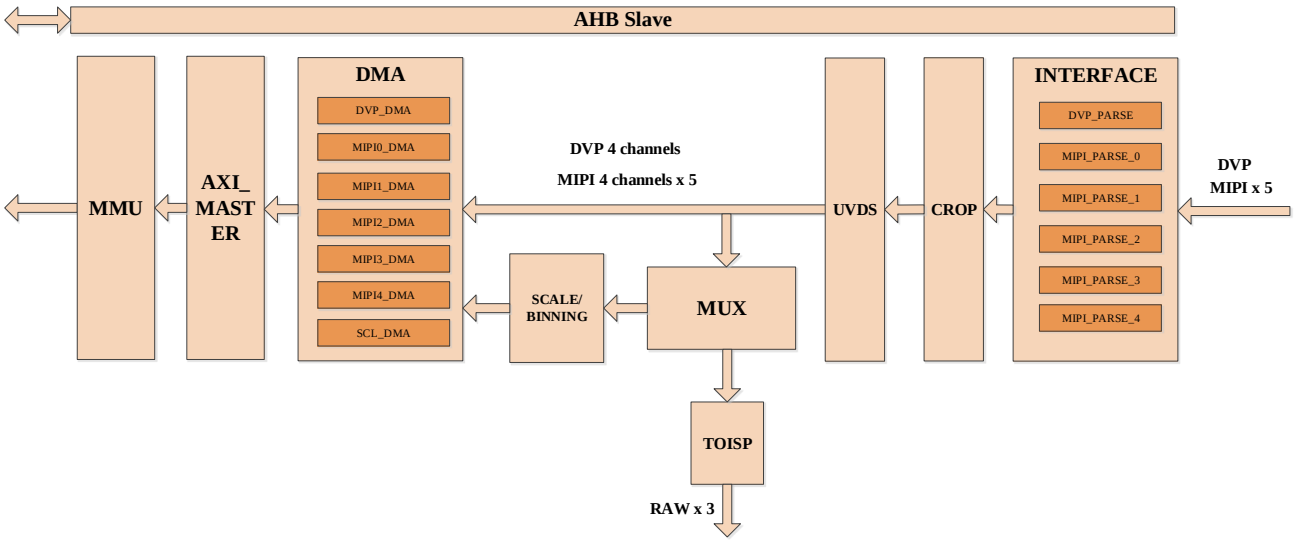


Fig. 6-1 VICAP Block Diagram

VICAP comprises with:

- AHB Slave
- AXI Master
- MMU
- INTERFACE
- CROP

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- UVDS
- SCALE/BINNING
- TOISP
- DMA

6.3 Function Description

6.3.1 Interface

Translate the input video data into the requisite data format

- DVP BT.656/BT.1120 format

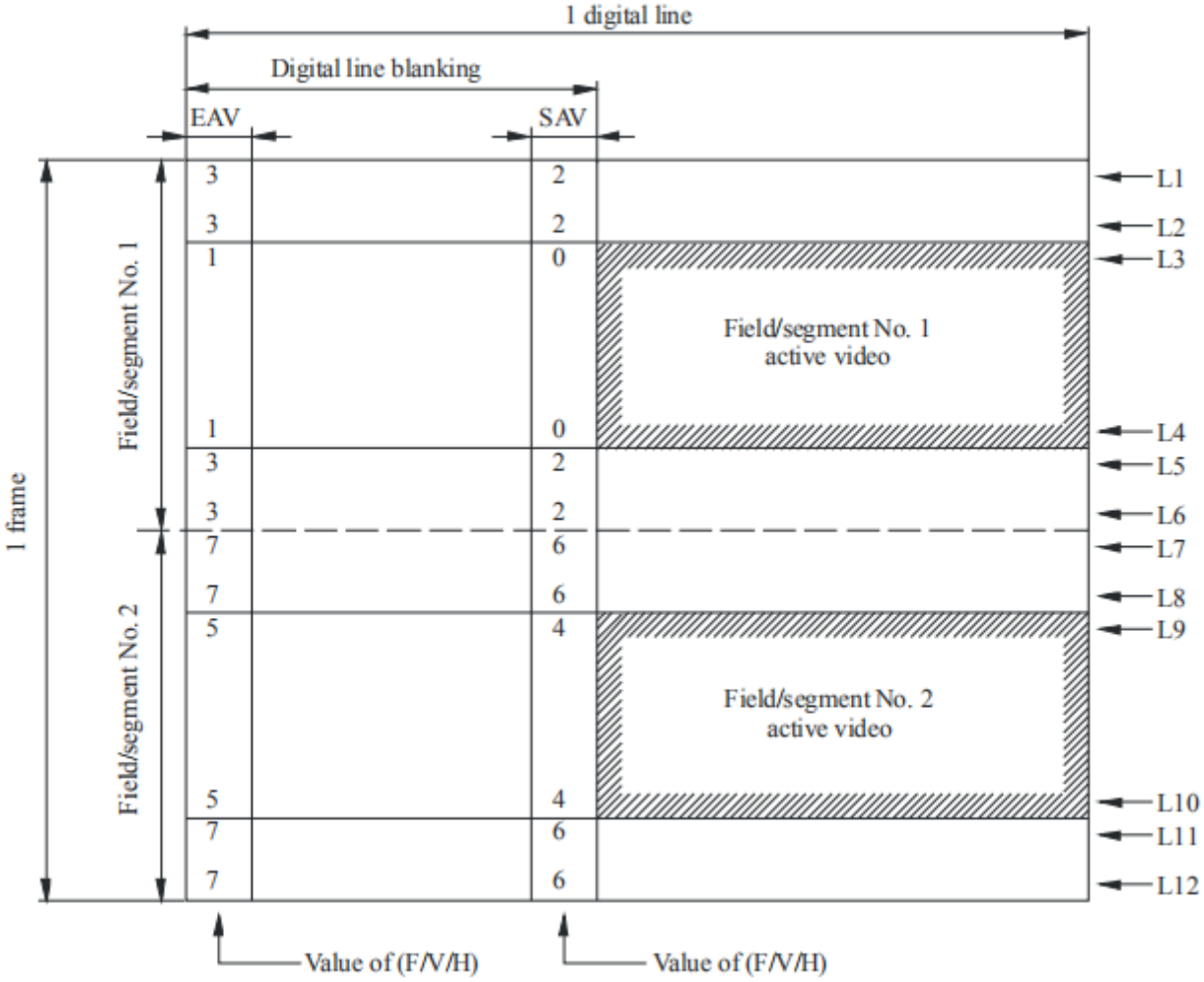


Fig. 6-2 BT656/BT1120 interlace timing relationship

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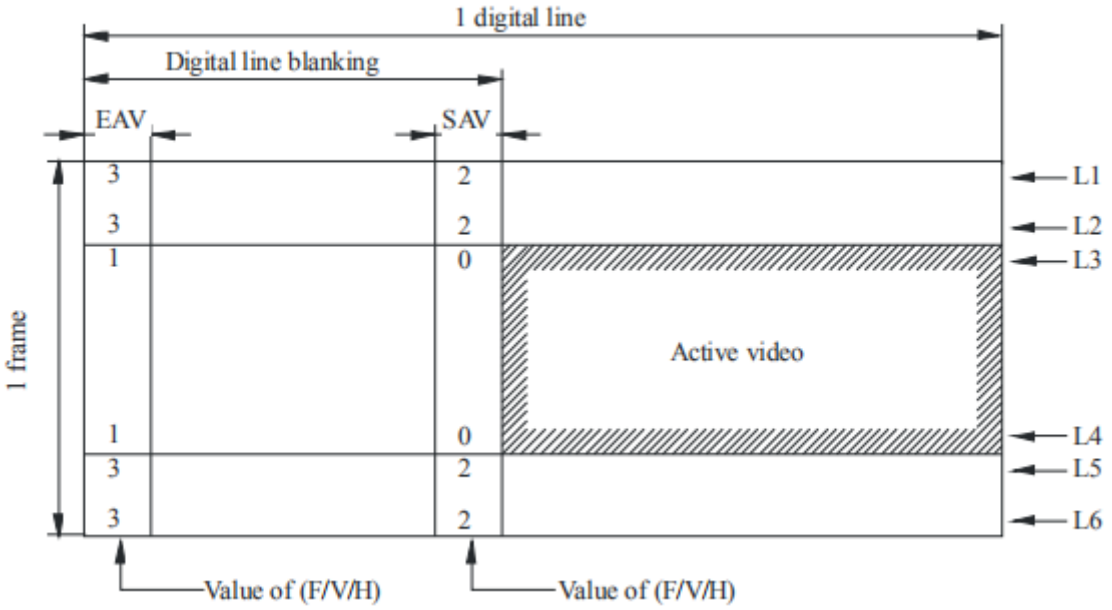


Fig. 6-3 BT656/BT1120 progressive timing relationship

- DVP 2/4 channels mixed BT.656/BT.1120 format

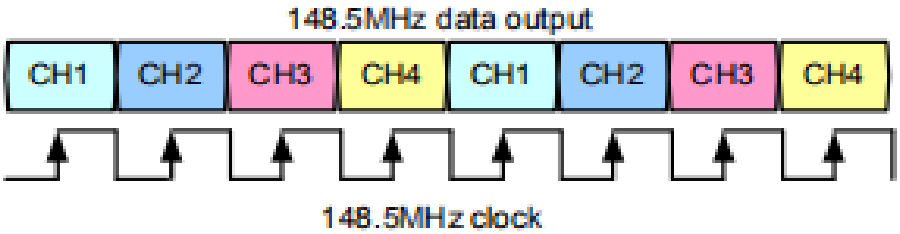


Fig. 6-4 4 channels mixed BT656/BT1120

- DVP BT.601 format

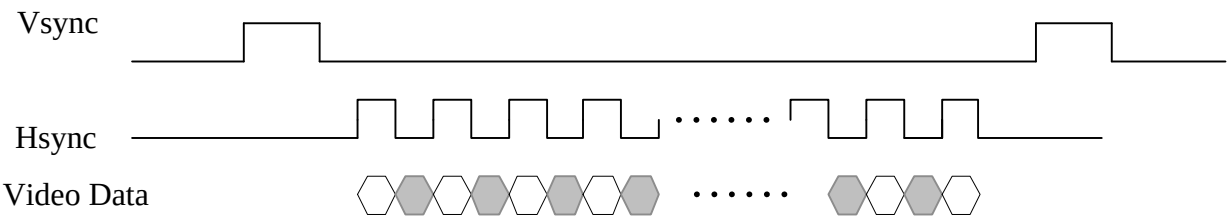


Fig. 6-5 BT656/BT1120 timing relationship

- MIPI CSI RAW8 format

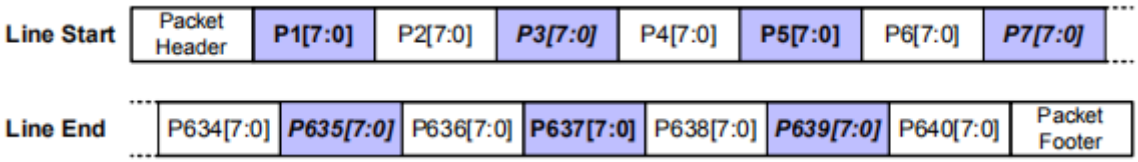
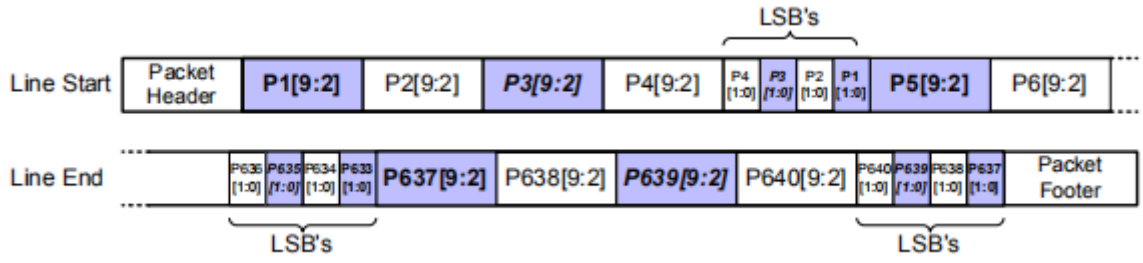


Fig. 6-6 MIPI CSI RAW8 format

- MIPI CSI RAW10 format



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Fig. 6-7 MIPI CSI RAW10 format

- MIPI CSI RAW12 format

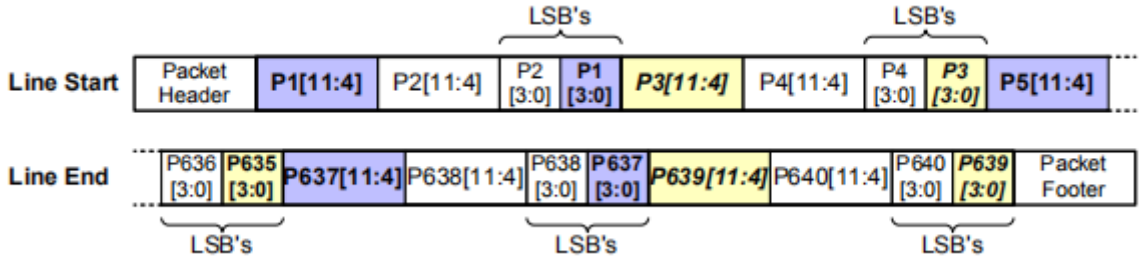


Fig. 6-8 MIPI CSI RAW12 format

- MIPI CSI RAW14 format

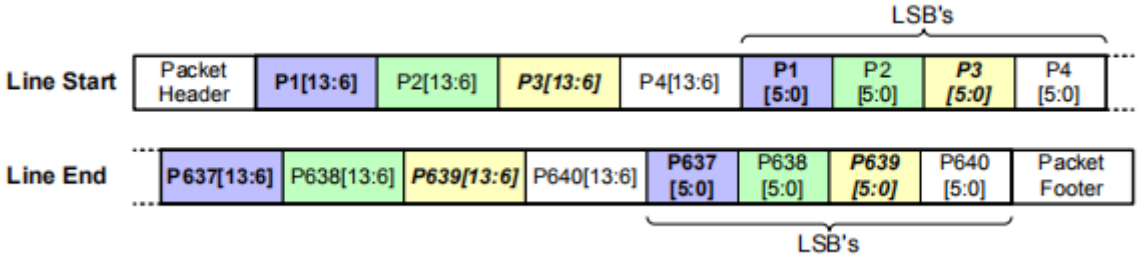


Fig. 6-9 MIPI CSI RAW14 format

- MIPI CSI RAW16 format

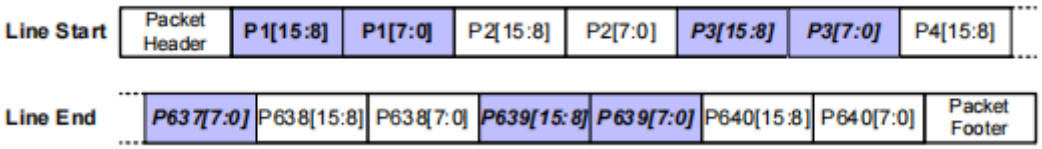


Fig. 6-10 MIPI CSI RAW16 format

- RGB888 format

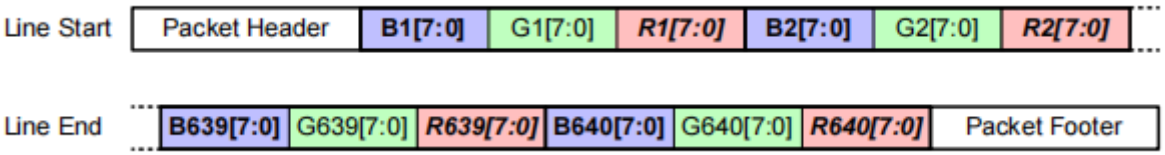


Fig. 6-11 RGB888 format

- MIPI CSI YUV422 format

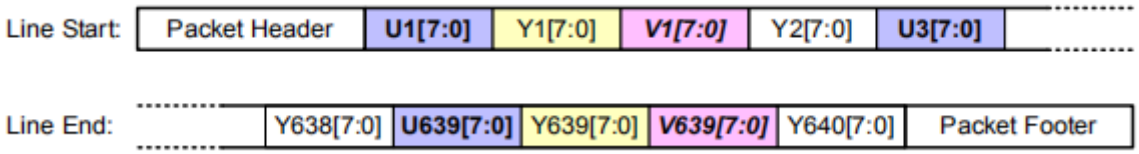


Fig. 6-12 MIPI CSI YUV422 format

- MIPI CSI YUV420 format

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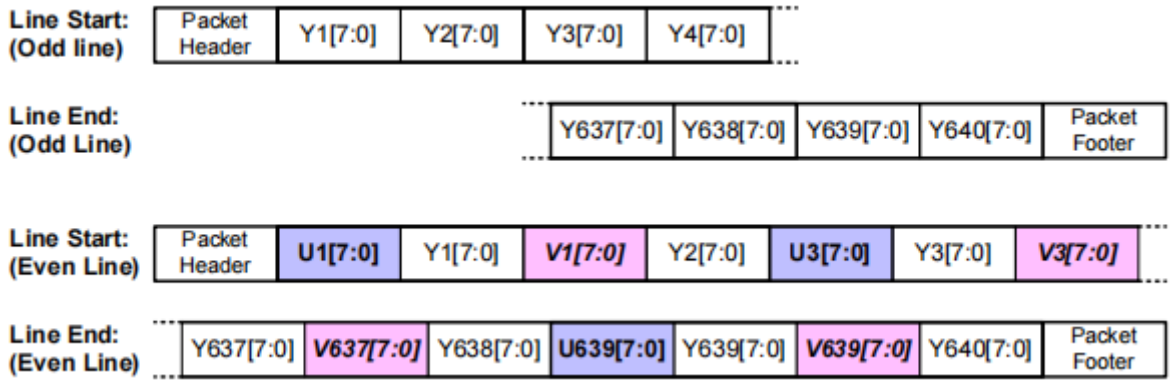


Fig. 6-13 MIPI CSI YUV420 format

- MIPI CSI Legacy YUV420 format

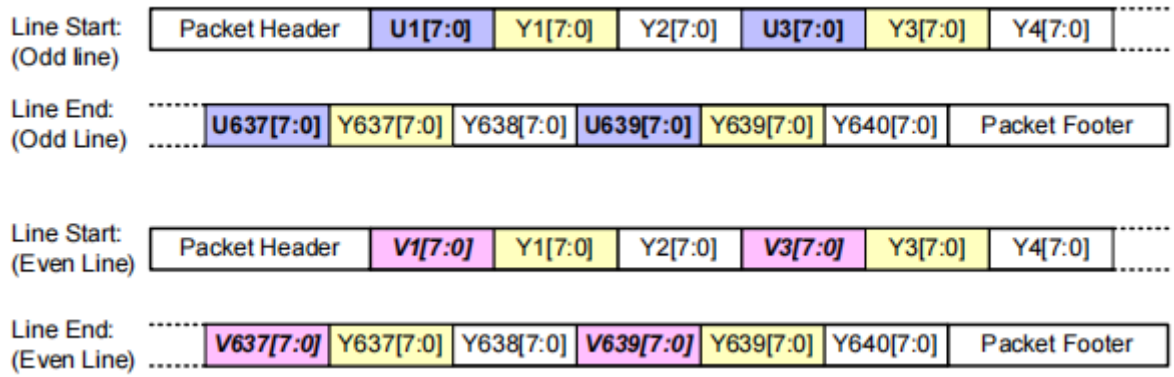


Fig. 6-14 MIPI CSI Legacy YUV420 format

6.3.2 Crop

Bypass or crop the source video data to a smaller size destination.

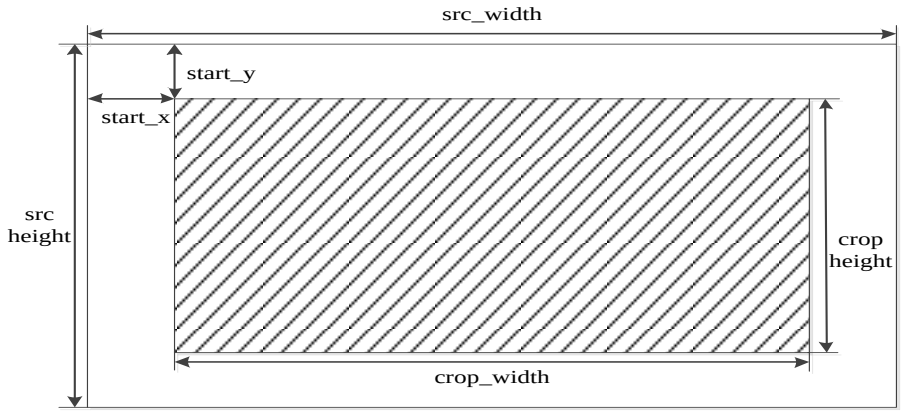


Fig. 6-15 Crop

6.3.3 Scale

Scale down for RAW data:

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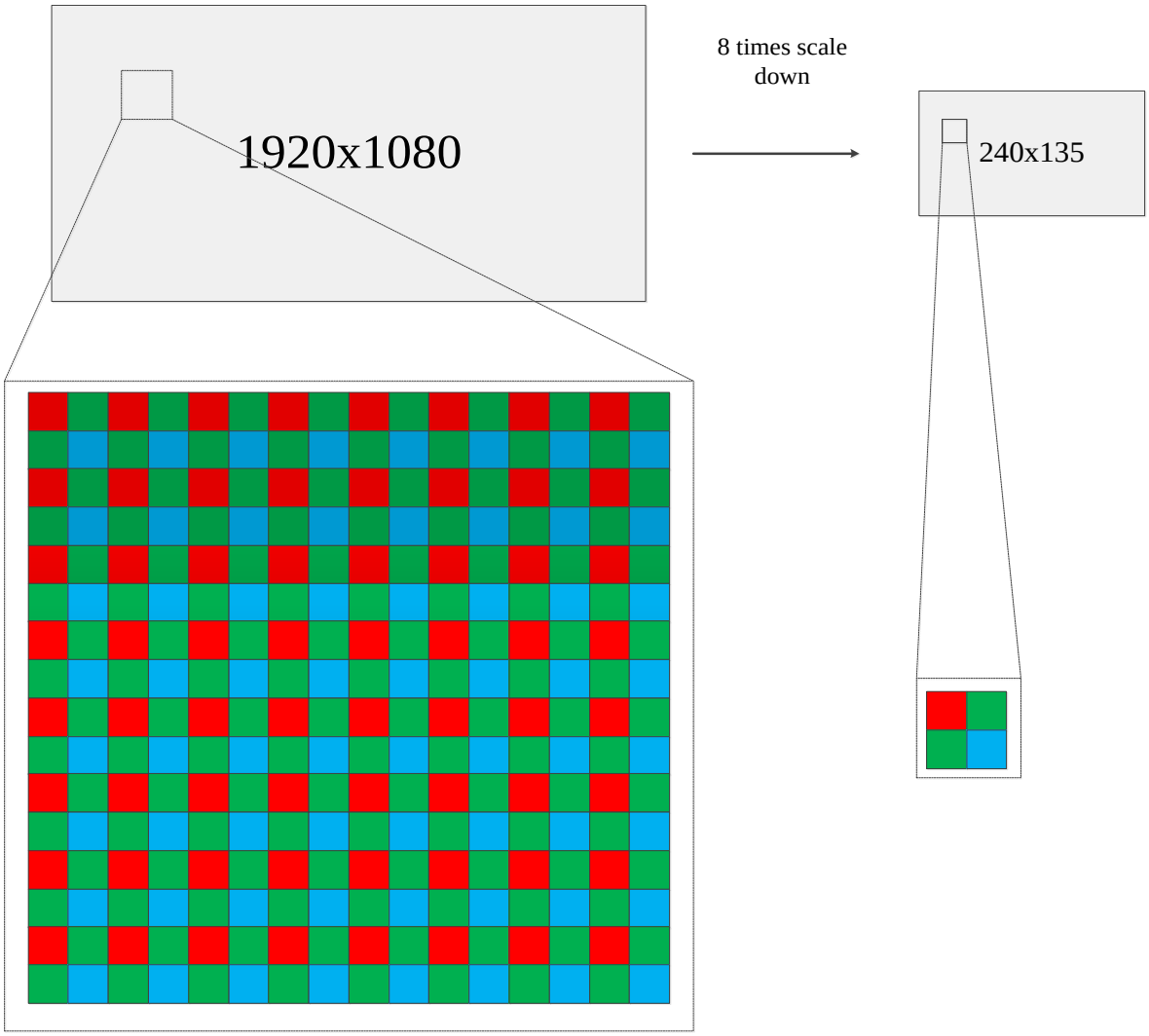


Fig. 6-16 8 times Scale down

RAW data 2x2 binning:

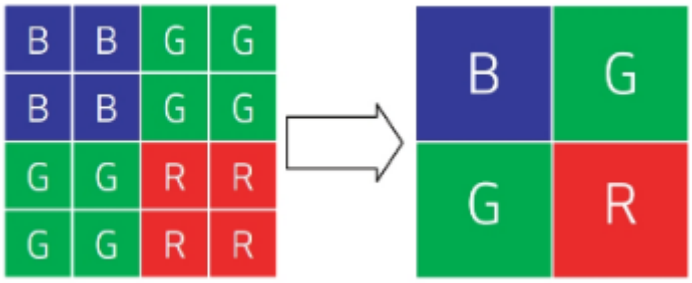


Fig. 6-17 RAW 2x2 binning

6.3.4 UVDS

UV mean downsampling for YUV422:

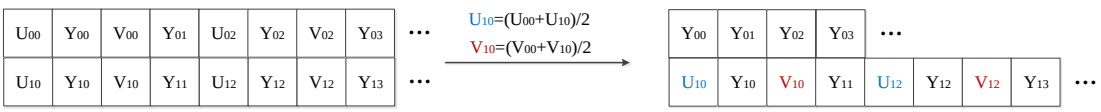


Fig. 6-18 convert yuv422 to yuv420 by UVDS

6.3.5 Toisp

The parsed video data can go straight to ISP for real-time processing.

6.3.6 DMA

The DMA is used to transfer the data from crop module to the AXI master block which will

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send the data to the AXI bus.

- NV16

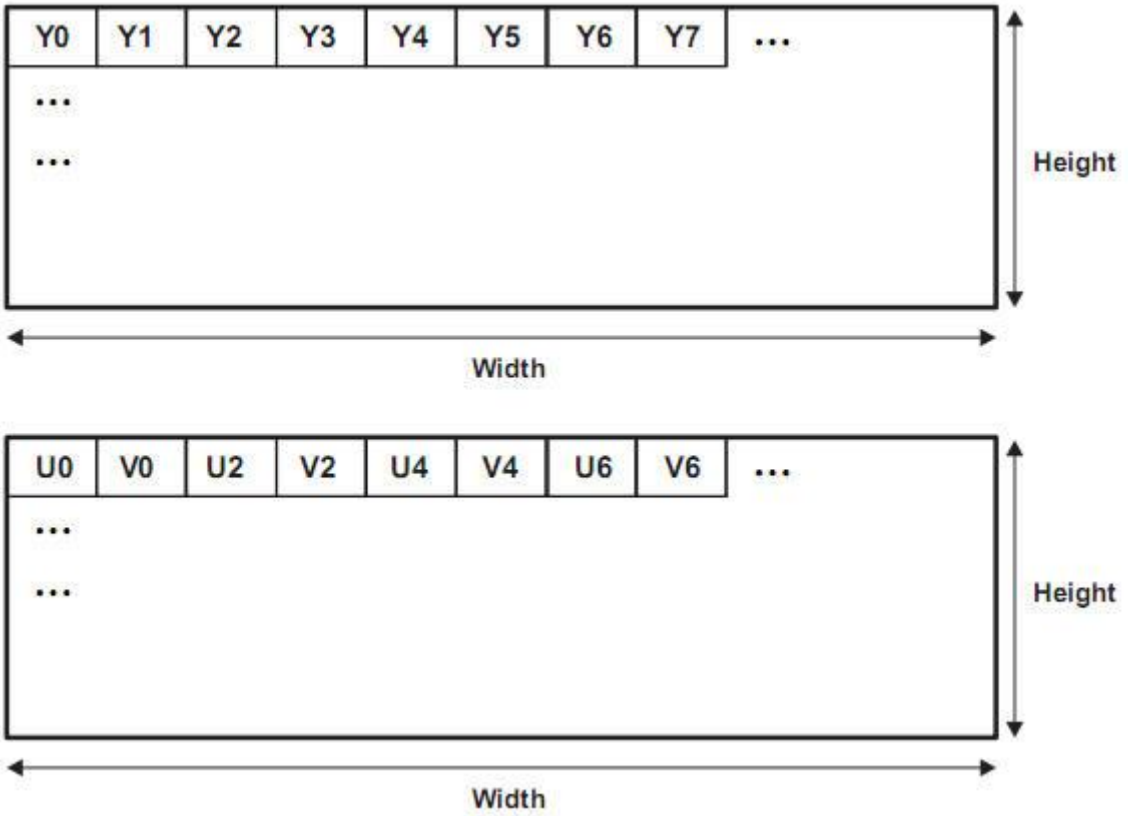


Fig. 6-19 NV16

- NV12

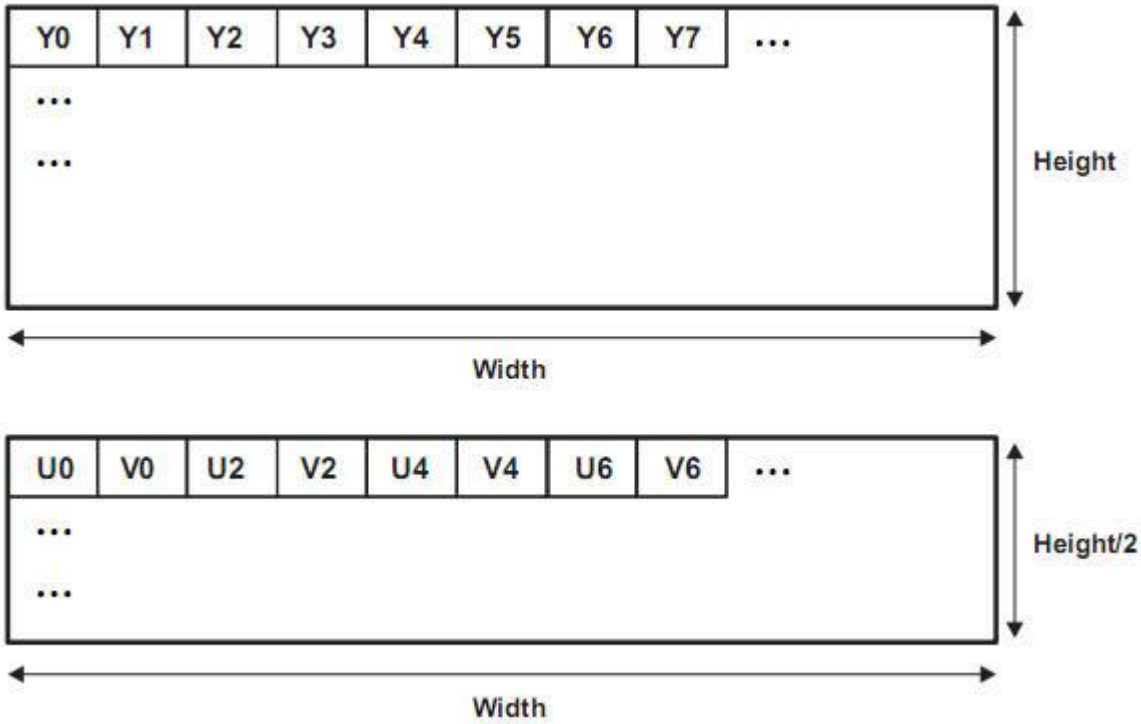


Fig. 6-20 NV12

- YUV400

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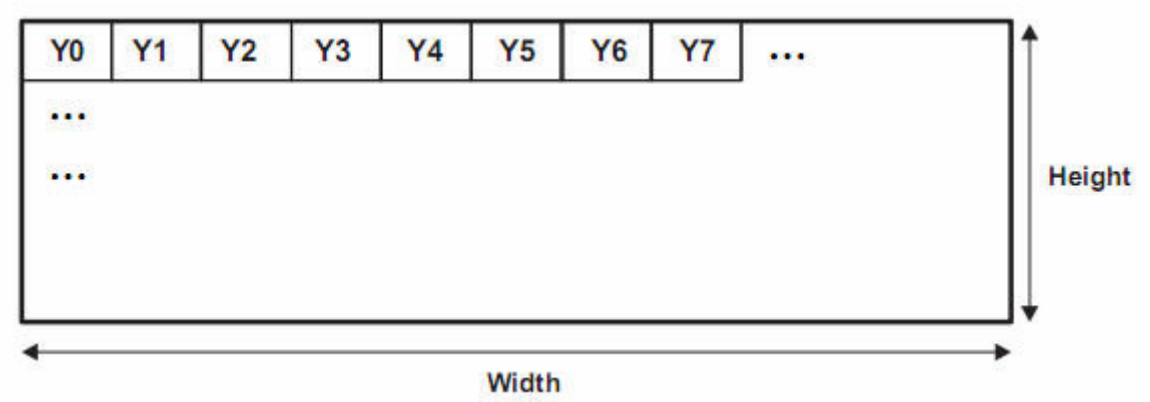


Fig. 6-21 YUV400

- YUYV

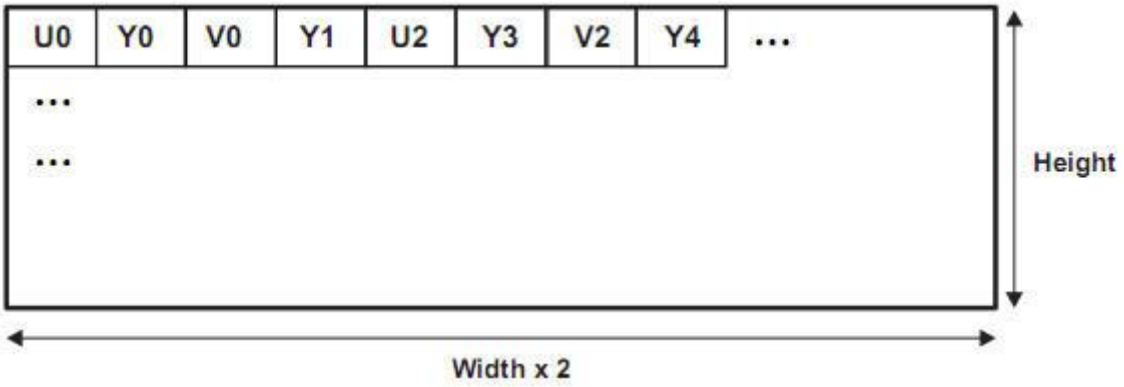


Fig. 6-22 YUYV

- Compact RAW

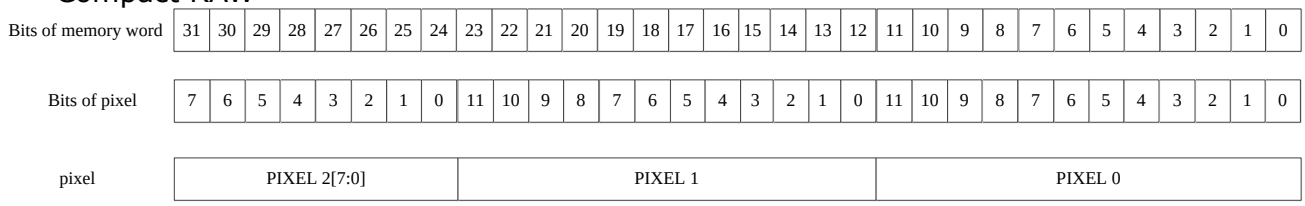


Fig. 6-23 Compact RAW12

- Noncompact RAW

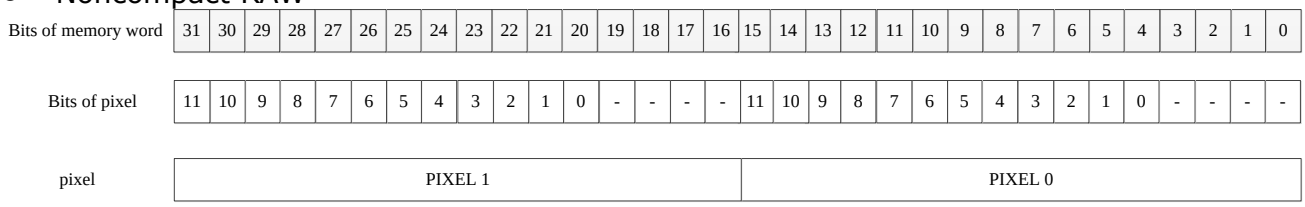


Fig. 6-24 noncompact RAW12(high align)

6.3.7 AXI Master

Transmit the data to chip memory via the AXI Master.

6.3.8 MMU

Map the virtual address to physical address.

6.3.9 AHB Slave

Host configure the registers via the AHB Slave.

6.4 Register Description

6.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 6-1 VICAP Address Mapping

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Base Address[11:8]	Device	Address Length	Offset Address Range
4'b0000	Global/DVP	256 BYTE	0x0000 ~ 0x00ff
4'b0001	MIPI0	512 BYTE	0x0100 ~ 0x01ff
4'b0011	MIPI1	512 BYTE	0x0300 ~ 0x03ff
4'b0100	MIPI2	512 BYTE	0x0400 ~ 0x04ff
4'b0101	MIPI3	512 BYTE	0x0500 ~ 0x05ff
4'b0110	MIPI4	512 BYTE	0x0600 ~ 0x06ff
4'b0111	Scale/TOISP	256 BYTE	0x0700 ~ 0x07ff
4'b1000	MMU	256 BYTE	0x0800 ~ 0x08ff

6.5 Registers Summary

Name	Offset	Size	Reset Value	Description
VICAP_GLB_CTRL	0x0000	W	0x8001FE61	VICAP global control
VICAP_GLB_INTEN	0x0004	W	0x00000000	VICAP global interrupt enable.
VICAP_GLB_INTST	0x0008	W	0x00000000	VICAP global interrupt status.
VICAP_GLB_TOLE	0x000C	W	0x00000000	Enable/Status for ddr freq int
VICAP_DVP_CTRL	0x0010	W	0x00000000	DVP path control
VICAP_DVP_INTEN	0x0014	W	0x00000000	DVP path interrupt status
VICAP_DVP_INTSTAT	0x0018	W	0x00000000	DVP path interrupt status
VICAP_DVP_FORMAT	0x001C	W	0x00000000	DVP path format
VICAP_DVP_MULTI_ID	0x0020	W	0x00000000	Channel ID for multi-ID mode
VICAP_DVP_SAV_EAV	0x0024	W	0xFEDCBA98	SAV/EAV for ACT/BLK
VICAP_DVP_CROP_SIZE	0x0028	W	0x00000000	The expected width and height of received image
VICAP_DVP_CROP_START	0x002C	W	0x00000000	The start point of DVP path cropping
VICAP_DVP_FRM0_ADDR_Y_ID0	0x0030	W	0x00000000	DVP path frame0 y address
VICAP_DVP_FRM0_ADDR_UV_ID0	0x0034	W	0x00000000	DVP path frame0 uv address
VICAP_DVP_FRM1_ADDR_Y_ID0	0x0038	W	0x00000000	DVP path frame1 y address
VICAP_DVP_FRM1_ADDR_UV_ID0	0x003C	W	0x00000000	DVP path frame1 uv address
VICAP_DVP_FRM0_ADDR_Y_ID1	0x0040	W	0x00000000	DVP path frame0 y address for ID1
VICAP_DVP_FRM0_ADDR_UV_ID1	0x0044	W	0x00000000	DVP path frame0 uv address for id1
VICAP_DVP_FRM1_ADDR_Y_ID1	0x0048	W	0x00000000	DVP path frame1 y address for id1
VICAP_DVP_FRM1_ADDR_UV_ID1	0x004C	W	0x00000000	DVP path frame1 uv address for id1
VICAP_DVP_FRM0_ADDR_Y_ID2	0x0050	W	0x00000000	DVP path frame0 y address for id2
VICAP_DVP_FRM0_ADDR_UV_ID2	0x0054	W	0x00000000	DVP path frame0 uv address for id2
VICAP_DVP_FRM1_ADDR_Y_ID2	0x0058	W	0x00000000	DVP path frame1 y address for id2
VICAP_DVP_FRM1_ADDR_UV_ID2	0x005C	W	0x00000000	DVP path frame1 uv address for id2
VICAP_DVP_FRM0_ADDR_Y_ID3	0x0060	W	0x00000000	DVP path frame0 y address for id3

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Name	Offset	Size	Reset Value	Description
VICAP_DVP_FRM0_ADDR_UV_ID3	0x0064	W	0x00000000	DVP path frame0 uv address for id3
VICAP_DVP_FRM1_ADDR_Y_ID3	0x0068	W	0x00000000	DVP path frame1 y address for id3
VICAP_DVP_FRM1_ADDR_UV_ID3	0x006C	W	0x00000000	DVP path frame1 uv address for id3
VICAP_DVP_VIR_LINE_WIDTH	0x0070	W	0x00000000	DVP path virtual line width
VICAP_DVP_LINE_INT_NUM_ID0_1	0x0074	W	0x00000000	DVP path id0/1 line interrupt number
VICAP_DVP_LINE_INT_NUM_ID2_3	0x0078	W	0x00000000	DVP path id2/3 line interrupt number
VICAP_DVP_LINE_CNT_ID0_1	0x007C	W	0x00000000	DVP path id0/1 line count
VICAP_DVP_LINE_CNT_ID2_3	0x0080	W	0x00000000	DVP path id2/3 line count
VICAP_DVP_SIZE_NUM_ID0	0x0084	W	0x00000000	DVP path ID0 SIZE NUMBER
VICAP_DVP_SIZE_NUM_ID1	0x0088	W	0x00000000	DVP path ID1 SIZE NUMBER
VICAP_DVP_SIZE_NUM_ID2	0x008C	W	0x00000000	DVP path ID2 SIZE NUMBER
VICAP_DVP_SIZE_NUM_ID3	0x0090	W	0x00000000	DVP path ID3 SIZE NUMBER
VICAP_DVP_SYNC_HEADER	0x00A4	W	0x00000000	DVP SYNC HEADER FOR BT656/BT1120
VICAP_MIPI0_ID0_CTRL0	0x0100	W	0x00000000	MIPI0 path id0 control0
VICAP_MIPI0_ID0_CTRL1	0x0104	W	0x00000000	MIPI0 path id0 control1
VICAP_MIPI0_ID1_CTRL0	0x0108	W	0x00000000	MIPI0 path id1 control0
VICAP_MIPI0_ID1_CTRL1	0x010C	W	0x00000000	MIPI0 path id1 control1
VICAP_MIPI0_ID2_CTRL0	0x0110	W	0x00000000	MIPI0 path id2 control0
VICAP_MIPI0_ID2_CTRL1	0x0114	W	0x00000000	MIPI0 path id2 control1
VICAP_MIPI0_ID3_CTRL0	0x0118	W	0x00000000	MIPI0 path id3 control0
VICAP_MIPI0_ID3_CTRL1	0x011C	W	0x00000000	MIPI0 path id3 control1
VICAP_MIPI0_CTRL	0x0120	W	0x00001200	MIPI0 path control
VICAP_MIPI0_FRAME0_ADDR_Y_ID0	0x0124	W	0x00000000	First address of even frame for ID0 Y/RAW/RGB path
VICAP_MIPI0_FRAME1_ADDR_Y_ID0	0x0128	W	0x00000000	First address of odd frame for ID0 Y path
VICAP_MIPI0_FRAME0_ADDR_UV_ID0	0x012C	W	0x00000000	First address of even frame for ID0 UV path
VICAP_MIPI0_FRAME1_ADDR_UV_ID0	0x0130	W	0x00000000	First address of odd frame for ID0 UV path
VICAP_MIPI0_VLW_ID0	0x0134	W	0x00000000	Virtual line width for ID0
VICAP_MIPI0_FRAME0_ADDR_Y_ID1	0x0138	W	0x00000000	First address of even frame for ID1 Y/RAW/RGB path
VICAP_MIPI0_FRAME1_ADDR_Y_ID1	0x013C	W	0x00000000	First address of odd frame for ID1 Y/RAW/RGB path
VICAP_MIPI0_FRAME0_ADDR_UV_ID1	0x0140	W	0x00000000	First address of even frame for ID1 UV path
VICAP_MIPI0_FRAME1_ADDR_UV_ID1	0x0144	W	0x00000000	First address of odd frame for ID1 UV path
VICAP_MIPI0_VLW_ID1	0x0148	W	0x00000000	Virtual line width for ID1 path

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Name	Offset	Size	Reset Value	Description
VICAP_MIPI0_FRAME0_ADDR_Y_ID2	0x014C	W	0x00000000	First address of even frame for ID2 Y/RAW/RGB path
VICAP_MIPI0_FRAME1_ADDR_Y_ID2	0x0150	W	0x00000000	First address of odd frame for ID2 Y/RAW/RGB path
VICAP_MIPI0_FRAME0_ADDR_UV_ID2	0x0154	W	0x00000000	First address of even frame for ID2 UV path
VICAP_MIPI0_FRAME1_ADDR_UV_ID2	0x0158	W	0x00000000	First address of odd frame for ID2 UV path
VICAP_MIPI0_VLW_ID2	0x015C	W	0x00000000	Virtual line width for ID2 path
VICAP_MIPI0_FRAME0_ADDR_Y_ID3	0x0160	W	0x00000000	First address of even frame for ID3 Y/RAW/RGB path
VICAP_MIPI0_FRAME1_ADDR_Y_ID3	0x0164	W	0x00000000	First address of odd frame for ID3 Y/RAW/RGB path
VICAP_MIPI0_FRAME0_ADDR_UV_ID3	0x0168	W	0x00000000	First address of even frame for ID3 UV path
VICAP_MIPI0_FRAME1_ADDR_UV_ID3	0x016C	W	0x00000000	First address of odd frame for ID3 UV path
VICAP_MIPI0_VLW_ID3	0x0170	W	0x00000000	Virtual line width for ID3 path
VICAP_MIPI0_INTEN	0x0174	W	0x00000000	MIPI0 path interrupt enable
VICAP_MIPI0_INTSTAT	0x0178	W	0x00000000	MIPI0 path interrupt status
VICAP_MIPI0_ON_PAD_VALUE	0x017C	W	0x00000000	The ON padding value of MIPI0
VICAP_MIPI0_ID0_EFFECT_CODE	0x0180	W	0x00000000	The effect code of MIPI0 ID0
VICAP_MIPI0_ID1_EFFECT_CODE	0x0184	W	0x00000000	The effect code of MIPI0 ID1
VICAP_MIPI0_ID2_EFFECT_CODE	0x0188	W	0x00000000	The effect code of MIPI0 ID2
VICAP_MIPI0_ID3_EFFECT_CODE	0x018C	W	0x00000000	The effect code of MIPI0 ID3
VICAP_MIPI0_ID0_CROP_START	0x0190	W	0x00000000	The start point of MIPI0 ID0 cropping
VICAP_MIPI0_ID1_CROP_START	0x0194	W	0x00000000	The start point of MIPI0 ID1 cropping
VICAP_MIPI0_ID2_CROP_START	0x0198	W	0x00000000	The start point of MIPI0 ID2 cropping
VICAP_MIPI0_ID3_CROP_START	0x019C	W	0x00000000	The start point of MIPI0 ID3 cropping
VICAP_MIPI0_ID0_SET_SIZE	0x01A0	W	0x00000000	The size of MIPI0 ID0
VICAP_MIPI0_ID1_SET_SIZE	0x01A4	W	0x00000000	The size of MIPI0 ID1
VICAP_MIPI0_ID2_SET_SIZE	0x01A8	W	0x00000000	The size of MIPI0 ID2
VICAP_MIPI0_ID3_SET_SIZE	0x01AC	W	0x00000000	The size of MIPI0 ID3
VICAP_MIPI0_LINE_INT_NUM_ID0_1	0x01B0	W	0x00400040	Line number of the MIPI0 path ID0/1 line interrupt
VICAP_MIPI0_LINE_INT_NUM_ID2_3	0x01B4	W	0x00400040	Line number of the MIPI0 path ID2/3 line interrupt
VICAP_MIPI0_LINE_CNT_ID0_1	0x01B8	W	0x00000000	Line count of the MIPI0 path ID0/1
VICAP_MIPI0_LINE_CNT_ID2_3	0x01BC	W	0x00000000	Line count of the MIPI0 path ID2/3

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Name	Offset	Size	Reset Value	Description
VICAP_MIPI0_SIZE_NUM_ID0	0x01C0	W	0x00000000	MIPI0 path ID0 SIZE NUMBER
VICAP_MIPI0_SIZE_NUM_ID1	0x01C4	W	0x00000000	MIPI0 path ID1 SIZE NUMBER
VICAP_MIPI0_SIZE_NUM_ID2	0x01C8	W	0x00000000	MIPI0 path ID2 SIZE NUMBER
VICAP_MIPI0_SIZE_NUM_ID3	0x01CC	W	0x00000000	MIPI0 path ID3 SIZE NUMBER
VICAP_MIPI0_FRAME_NUM_VC0	0x01D0	W	0x00000000	The frame number of virtual channel 0
VICAP_MIPI0_FRAME_NUM_VC1	0x01D4	W	0x00000000	The frame number of virtual channel 1
VICAP_MIPI0_FRAME_NUM_VC2	0x01D8	W	0x00000000	The frame number of virtual channel 2
VICAP_MIPI0_FRAME_NUM_VC3	0x01DC	W	0x00000000	The frame number of virtual channel 3
VICAP_MIPI1_ID0_CTRL0	0x0300	W	0x00000000	MIPI1 path id0 control0
VICAP_MIPI1_ID0_CTRL1	0x0304	W	0x00000000	MIPI1 path id0 control1
VICAP_MIPI1_ID1_CTRL0	0x0308	W	0x00000000	MIPI1 path id1 control0
VICAP_MIPI1_ID1_CTRL1	0x030C	W	0x00000000	MIPI1 path id1 control1
VICAP_MIPI1_ID2_CTRL0	0x0310	W	0x00000000	MIPI1 path id2 control0
VICAP_MIPI1_ID2_CTRL1	0x0314	W	0x00000000	MIPI1 path id2 control1
VICAP_MIPI1_ID3_CTRL0	0x0318	W	0x00000000	MIPI1 path id3 control0
VICAP_MIPI1_ID3_CTRL1	0x031C	W	0x00000000	MIPI1 path id3 control1
VICAP_MIPI1_CTRL	0x0320	W	0x00000000	MIPI1 path control
VICAP_MIPI1_FRAME0_ADDR_Y_ID0	0x0324	W	0x00000000	First address of even frame for ID0 Y/RAW/RGB path
VICAP_MIPI1_FRAME1_ADDR_Y_ID0	0x0328	W	0x00000000	First address of odd frame for ID0 Y path
VICAP_MIPI1_FRAME0_ADDR_UV_ID0	0x032C	W	0x00000000	First address of even frame for ID0 UV path
VICAP_MIPI1_FRAME1_ADDR_UV_ID0	0x0330	W	0x00000000	First address of odd frame for ID0 UV path
VICAP_MIPI1_VLW_ID0	0x0334	W	0x00000000	Virtual line width for ID0
VICAP_MIPI1_FRAME0_ADDR_Y_ID1	0x0338	W	0x00000000	First address of even frame for ID1 Y/RAW/RGB path
VICAP_MIPI1_FRAME1_ADDR_Y_ID1	0x033C	W	0x00000000	First address of odd frame for ID1 Y/RAW/RGB path
VICAP_MIPI1_FRAME0_ADDR_UV_ID1	0x0340	W	0x00000000	First address of even frame for ID1 UV path
VICAP_MIPI1_FRAME1_ADDR_UV_ID1	0x0344	W	0x00000000	First address of odd frame for ID1 UV path
VICAP_MIPI1_VLW_ID1	0x0348	W	0x00000000	Virtual line width for ID1 path
VICAP_MIPI1_FRAME0_ADDR_Y_ID2	0x034C	W	0x00000000	First address of even frame for ID2 Y/RAW/RGB path
VICAP_MIPI1_FRAME1_ADDR_Y_ID2	0x0350	W	0x00000000	First address of odd frame for ID2 Y/RAW/RGB path
VICAP_MIPI1_FRAME0_ADDR_UV_ID2	0x0354	W	0x00000000	First address of even frame for ID2 UV path
VICAP_MIPI1_FRAME1_ADDR_UV_ID2	0x0358	W	0x00000000	First address of odd frame for ID2 UV path
VICAP_MIPI1_VLW_ID2	0x035C	W	0x00000000	Virtual line width for ID2 path

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Name	Offset	Size	Reset Value	Description
VICAP_MIPI1_FRAME0_ADDR_Y_ID3	0x0360	W	0x00000000	First address of even frame for ID3 Y/RAW/RGB path
VICAP_MIPI1_FRAME1_ADDR_Y_ID3	0x0364	W	0x00000000	First address of odd frame for ID3 Y/RAW/RGB path
VICAP_MIPI1_FRAME0_ADDR_UV_ID3	0x0368	W	0x00000000	First address of even frame for ID3 UV path
VICAP_MIPI1_FRAME1_ADDR_UV_ID3	0x036C	W	0x00000000	First address of odd frame for ID3 UV path
VICAP_MIPI1_VLW_ID3	0x0370	W	0x00000000	Virtual line width for ID3 path
VICAP_MIPI1_INTEN	0x0374	W	0x00000000	MIPI1 path interrupt enable
VICAP_MIPI1_INTSTAT	0x0378	W	0x00000000	MIPI1 path interrupt status
VICAP_MIPI1_ON_PAD_VALUE	0x037C	W	0x00000000	The ON padding value of MIPI1
VICAP_MIPI1_ID0_EFFECT_CODE	0x0380	W	0x00000000	The effect code of MIPI1 ID0
VICAP_MIPI1_ID1_EFFECT_CODE	0x0384	W	0x00000000	The effect code of MIPI1 ID1
VICAP_MIPI1_ID2_EFFECT_CODE	0x0388	W	0x00000000	The effect code of MIPI1 ID2
VICAP_MIPI1_ID3_EFFECT_CODE	0x038C	W	0x00000000	The effect code of MIPI1 ID3
VICAP_MIPI1_ID0_CROP_START	0x0390	W	0x00000000	The start point of MIPI1 ID0 cropping
VICAP_MIPI1_ID1_CROP_START	0x0394	W	0x00000000	The start point of MIPI1 ID1 cropping
VICAP_MIPI1_ID2_CROP_START	0x0398	W	0x00000000	The start point of MIPI1 ID2 cropping
VICAP_MIPI1_ID3_CROP_START	0x039C	W	0x00000000	The start point of MIPI1 ID3 cropping
VICAP_MIPI1_ID0_SET_SIZE	0x03A0	W	0x00000000	The size of MIPI1 ID0
VICAP_MIPI1_ID1_SET_SIZE	0x03A4	W	0x00000000	The size of MIPI1 ID1
VICAP_MIPI1_ID2_SET_SIZE	0x03A8	W	0x00000000	The size of MIPI1 ID2
VICAP_MIPI1_ID3_SET_SIZE	0x03AC	W	0x00000000	The size of MIPI1 ID3
VICAP_MIPI1_LINE_INT_NUM_ID0_1	0x03B0	W	0x00400040	Line number of the MIPI1 path ID0/1 line interrupt
VICAP_MIPI1_LINE_INT_NUM_ID2_3	0x03B4	W	0x00400040	Line number of the MIPI1 path ID2/3 line interrupt
VICAP_MIPI1_LINE_CNT_ID0_1	0x03B8	W	0x00000000	Line count of the MIPI1 path ID0/1
VICAP_MIPI1_LINE_CNT_ID2_3	0x03BC	W	0x00000000	Line count of the MIPI1 path ID2/3
VICAP_MIPI1_SIZE_NUM_ID0	0x03C0	W	0x00000000	MIPI1 path ID0 SIZE NUMBER
VICAP_MIPI1_SIZE_NUM_ID1	0x03C4	W	0x00000000	MIPI1 path ID1 SIZE NUMBER
VICAP_MIPI1_SIZE_NUM_ID2	0x03C8	W	0x00000000	MIPI1 path ID2 SIZE NUMBER
VICAP_MIPI1_SIZE_NUM_ID3	0x03CC	W	0x00000000	MIPI1 path ID3 SIZE NUMBER

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Name	Offset	Size	Reset Value	Description
VICAP_MIPI1_FRAME_NUM_VC0	0x03D0	W	0x00000000	The frame number of virtual channel 0
VICAP_MIPI1_FRAME_NUM_VC1	0x03D4	W	0x00000000	The frame number of virtual channel 1
VICAP_MIPI1_FRAME_NUM_VC2	0x03D8	W	0x00000000	The frame number of virtual channel 2
VICAP_MIPI1_FRAME_NUM_VC3	0x03DC	W	0x00000000	The frame number of virtual channel 3
VICAP_MIPI2_ID0_CTRL0	0x0400	W	0x00000000	MIPI2 path id0 control0
VICAP_MIPI2_ID0_CTRL1	0x0404	W	0x00000000	MIPI2 path id0 control1
VICAP_MIPI2_ID1_CTRL0	0x0408	W	0x00000000	MIPI2 path id1 control0
VICAP_MIPI2_ID1_CTRL1	0x040C	W	0x00000000	MIPI2 path id1 control1
VICAP_MIPI2_ID2_CTRL0	0x0410	W	0x00000000	MIPI2 path id2 control0
VICAP_MIPI2_ID2_CTRL1	0x0414	W	0x00000000	MIPI2 path id2 control1
VICAP_MIPI2_ID3_CTRL0	0x0418	W	0x00000000	MIPI2 path id3 control0
VICAP_MIPI2_ID3_CTRL1	0x041C	W	0x00000000	MIPI2 path id3 control1
VICAP_MIPI2_CTRL	0x0420	W	0x00000000	MIPI2 path control
VICAP_MIPI2_FRAME0_ADDR_Y_ID0	0x0424	W	0x00000000	First address of even frame for ID0 Y/RAW/RGB path
VICAP_MIPI2_FRAME1_ADDR_Y_ID0	0x0428	W	0x00000000	First address of odd frame for ID0 Y path
VICAP_MIPI2_FRAME0_ADDR_UV_ID0	0x042C	W	0x00000000	First address of even frame for ID0 UV path
VICAP_MIPI2_FRAME1_ADDR_UV_ID0	0x0430	W	0x00000000	First address of odd frame for ID0 UV path
VICAP_MIPI2_VLW_ID0	0x0434	W	0x00000000	Virtual line width for ID0
VICAP_MIPI2_FRAME0_ADDR_Y_ID1	0x0438	W	0x00000000	First address of even frame for ID1 Y/RAW/RGB path
VICAP_MIPI2_FRAME1_ADDR_Y_ID1	0x043C	W	0x00000000	First address of odd frame for ID1 Y/RAW/RGB path
VICAP_MIPI2_FRAME0_ADDR_UV_ID1	0x0440	W	0x00000000	First address of even frame for ID1 UV path
VICAP_MIPI2_FRAME1_ADDR_UV_ID1	0x0444	W	0x00000000	First address of odd frame for ID1 UV path
VICAP_MIPI2_VLW_ID1	0x0448	W	0x00000000	Virtual line width for ID1 path
VICAP_MIPI2_FRAME0_ADDR_Y_ID2	0x044C	W	0x00000000	First address of even frame for ID2 Y/RAW/RGB path
VICAP_MIPI2_FRAME1_ADDR_Y_ID2	0x0450	W	0x00000000	First address of odd frame for ID2 Y/RAW/RGB path
VICAP_MIPI2_FRAME0_ADDR_UV_ID2	0x0454	W	0x00000000	First address of even frame for ID2 UV path
VICAP_MIPI2_FRAME1_ADDR_UV_ID2	0x0458	W	0x00000000	First address of odd frame for ID2 UV path
VICAP_MIPI2_VLW_ID2	0x045C	W	0x00000000	Virtual line width for ID2 path
VICAP_MIPI2_FRAME0_ADDR_Y_ID3	0x0460	W	0x00000000	First address of even frame for ID3 Y/RAW/RGB path
VICAP_MIPI2_FRAME1_ADDR_Y_ID3	0x0464	W	0x00000000	First address of odd frame for ID3 Y/RAW/RGB path
VICAP_MIPI2_FRAME0_ADDR_UV_ID3	0x0468	W	0x00000000	First address of even frame for ID3 UV path
VICAP_MIPI2_FRAME1_ADDR_UV_ID3	0x046C	W	0x00000000	First address of odd frame for ID3 UV path
VICAP_MIPI2_VLW_ID3	0x0470	W	0x00000000	Virtual line width for ID3 path

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Name	Offset	Size	Reset Value	Description
VICAP_MIPI2_INTEN	0x0474	W	0x00000000	MIPI2 path interrupt enable
VICAP_MIPI2_INTSTAT	0x0478	W	0x00000000	MIPI2 path interrupt status
VICAP_MIPI2_ON_PAD_VALUE	0x047C	W	0x00000000	The ON padding value of MIPI2
VICAP_MIPI2_ID0_EFFECT_CODE	0x0480	W	0x00000000	The effect code of MIPI2 ID0
VICAP_MIPI2_ID1_EFFECT_CODE	0x0484	W	0x00000000	The effect code of MIPI2 ID1
VICAP_MIPI2_ID2_EFFECT_CODE	0x0488	W	0x00000000	The effect code of MIPI2 ID2
VICAP_MIPI2_ID3_EFFECT_CODE	0x048C	W	0x00000000	The effect code of MIPI2 ID3
VICAP_MIPI2_ID0_CROP_START	0x0490	W	0x00000000	The start point of MIPI2 ID0 cropping
VICAP_MIPI2_ID1_CROP_START	0x0494	W	0x00000000	The start point of MIPI2 ID1 cropping
VICAP_MIPI2_ID2_CROP_START	0x0498	W	0x00000000	The start point of MIPI2 ID2 cropping
VICAP_MIPI2_ID3_CROP_START	0x049C	W	0x00000000	The start point of MIPI2 ID3 cropping
VICAP_MIPI2_ID0_SET_SIZE	0x04A0	W	0x00000000	The size of MIPI2 ID0
VICAP_MIPI2_ID1_SET_SIZE	0x04A4	W	0x00000000	The size of MIPI2 ID1
VICAP_MIPI2_ID2_SET_SIZE	0x04A8	W	0x00000000	The size of MIPI2 ID2
VICAP_MIPI2_ID3_SET_SIZE	0x04AC	W	0x00000000	The size of MIPI2 ID3
VICAP_MIPI2_LINE_INT_NUM_ID0_1	0x04B0	W	0x00400040	Line number of the MIPI2 path ID0/1 line interrupt
VICAP_MIPI2_LINE_INT_NUM_ID2_3	0x04B4	W	0x00400040	Line number of the MIPI2 path ID2/3 line interrupt
VICAP_MIPI2_LINE_CNT_ID0_1	0x04B8	W	0x00000000	Line count of the MIPI2 path ID0/1
VICAP_MIPI2_LINE_CNT_ID2_3	0x04BC	W	0x00000000	Line count of the MIPI2 path ID2/3
VICAP_MIPI2_SIZE_NUM_ID0	0x04C0	W	0x00000000	MIPI2 path ID0 SIZE NUMBER
VICAP_MIPI2_SIZE_NUM_ID1	0x04C4	W	0x00000000	MIPI2 path ID1 SIZE NUMBER
VICAP_MIPI2_SIZE_NUM_ID2	0x04C8	W	0x00000000	MIPI2 path ID2 SIZE NUMBER
VICAP_MIPI2_SIZE_NUM_ID3	0x04CC	W	0x00000000	MIPI2 path ID3 SIZE NUMBER
VICAP_MIPI2_FRAME_NUM_VC0	0x04D0	W	0x00000000	The frame number of virtual channel 0
VICAP_MIPI2_FRAME_NUM_VC1	0x04D4	W	0x00000000	The frame number of virtual channel 1
VICAP_MIPI2_FRAME_NUM_VC2	0x04D8	W	0x00000000	The frame number of virtual channel 2
VICAP_MIPI2_FRAME_NUM_VC3	0x04DC	W	0x00000000	The frame number of virtual channel 3
VICAP_MIPI3_ID0_CTRL0	0x0500	W	0x00000000	MIPI3 path id0 control0
VICAP_MIPI3_ID0_CTRL1	0x0504	W	0x00000000	MIPI3 path id0 control1

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Name	Offset	Size	Reset Value	Description
VICAP_MIPI3_ID1_CTRL0	0x0508	W	0x00000000	MIPI3 path id1 control0
VICAP_MIPI3_ID1_CTRL1	0x050C	W	0x00000000	MIPI3 path id1 control1
VICAP_MIPI3_ID2_CTRL0	0x0510	W	0x00000000	MIPI3 path id2 control0
VICAP_MIPI3_ID2_CTRL1	0x0514	W	0x00000000	MIPI3 path id2 control1
VICAP_MIPI3_ID3_CTRL0	0x0518	W	0x00000000	MIPI3 path id3 control0
VICAP_MIPI3_ID3_CTRL1	0x051C	W	0x00000000	MIPI3 path id3 control1
VICAP_MIPI3_CTRL	0x0520	W	0x00000000	MIPI3 path control
VICAP_MIPI3_FRAME0_ADDR_Y_ID0	0x0524	W	0x00000000	First address of even frame for ID0 Y/RAW/RGB path
VICAP_MIPI3_FRAME1_ADDR_Y_ID0	0x0528	W	0x00000000	First address of odd frame for ID0 Y path
VICAP_MIPI3_FRAME0_ADDR_UV_ID0	0x052C	W	0x00000000	First address of even frame for ID0 UV path
VICAP_MIPI3_FRAME1_ADDR_UV_ID0	0x0530	W	0x00000000	First address of odd frame for ID0 UV path
VICAP_MIPI3_VLW_ID0	0x0534	W	0x00000000	Virtual line width for ID0
VICAP_MIPI3_FRAME0_ADDR_Y_ID1	0x0538	W	0x00000000	First address of even frame for ID1 Y/RAW/RGB path
VICAP_MIPI3_FRAME1_ADDR_Y_ID1	0x053C	W	0x00000000	First address of odd frame for ID1 Y/RAW/RGB path
VICAP_MIPI3_FRAME0_ADDR_UV_ID1	0x0540	W	0x00000000	First address of even frame for ID1 UV path
VICAP_MIPI3_FRAME1_ADDR_UV_ID1	0x0544	W	0x00000000	First address of odd frame for ID1 UV path
VICAP_MIPI3_VLW_ID1	0x0548	W	0x00000000	Virtual line width for ID1 path
VICAP_MIPI3_FRAME0_ADDR_Y_ID2	0x054C	W	0x00000000	First address of even frame for ID2 Y/RAW/RGB path
VICAP_MIPI3_FRAME1_ADDR_Y_ID2	0x0550	W	0x00000000	First address of odd frame for ID2 Y/RAW/RGB path
VICAP_MIPI3_FRAME0_ADDR_UV_ID2	0x0554	W	0x00000000	First address of even frame for ID2 UV path
VICAP_MIPI3_FRAME1_ADDR_UV_ID2	0x0558	W	0x00000000	First address of odd frame for ID2 UV path
VICAP_MIPI3_VLW_ID2	0x055C	W	0x00000000	Virtual line width for ID2 path
VICAP_MIPI3_FRAME0_ADDR_Y_ID3	0x0560	W	0x00000000	First address of even frame for ID3 Y/RAW/RGB path
VICAP_MIPI3_FRAME1_ADDR_Y_ID3	0x0564	W	0x00000000	First address of odd frame for ID3 Y/RAW/RGB path
VICAP_MIPI3_FRAME0_ADDR_UV_ID3	0x0568	W	0x00000000	First address of even frame for ID3 UV path
VICAP_MIPI3_FRAME1_ADDR_UV_ID3	0x056C	W	0x00000000	First address of odd frame for ID3 UV path
VICAP_MIPI3_VLW_ID3	0x0570	W	0x00000000	Virtual line width for ID3 path
VICAP_MIPI3_INTEN	0x0574	W	0x00000000	MIPI3 path interrupt enable
VICAP_MIPI3_INTSTAT	0x0578	W	0x00000000	MIPI3 path interrupt status
VICAP_MIPI3_ON_PAD_VALUE	0x057C	W	0x00000000	The ON padding value of MIPI3
VICAP_MIPI3_ID0_EFFECT_CODE	0x0580	W	0x00000000	The effect code of MIPI3 ID0
VICAP_MIPI3_ID1_EFFECT_CODE	0x0584	W	0x00000000	The effect code of MIPI3 ID1
VICAP_MIPI3_ID2_EFFECT_CODE	0x0588	W	0x00000000	The effect code of MIPI3 ID2

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Name	Offset	Size	Reset Value	Description
VICAP_MIPI3_ID3_EFFECT_CODE	0x058C	W	0x00000000	The effect code of MIPI3 ID3
VICAP_MIPI3_ID0_CROP_START	0x0590	W	0x00000000	The start point of MIPI3 ID0 cropping
VICAP_MIPI3_ID1_CROP_START	0x0594	W	0x00000000	The start point of MIPI3 ID1 cropping
VICAP_MIPI3_ID2_CROP_START	0x0598	W	0x00000000	The start point of MIPI3 ID2 cropping
VICAP_MIPI3_ID3_CROP_START	0x059C	W	0x00000000	The start point of MIPI3 ID3 cropping
VICAP_MIPI3_ID0_SET_SIZE	0x05A0	W	0x00000000	The size of MIPI3 ID0
VICAP_MIPI3_ID1_SET_SIZE	0x05A4	W	0x00000000	The size of MIPI3 ID1
VICAP_MIPI3_ID2_SET_SIZE	0x05A8	W	0x00000000	The size of MIPI3 ID2
VICAP_MIPI3_ID3_SET_SIZE	0x05AC	W	0x00000000	The size of MIPI3 ID3
VICAP_MIPI3_LINE_INT_NUM_ID0_1	0x05B0	W	0x00400040	Line number of the MIPI3 path ID0/1 line interrupt
VICAP_MIPI3_LINE_INT_NUM_ID2_3	0x05B4	W	0x00400040	Line number of the MIPI3 path ID2/3 line interrupt
VICAP_MIPI3_LINE_CNT_ID0_1	0x05B8	W	0x00000000	Line count of the MIPI3 path ID0/1
VICAP_MIPI3_LINE_CNT_ID2_3	0x05BC	W	0x00000000	Line count of the MIPI3 path ID2/3
VICAP_MIPI3_SIZE_NUM_ID0	0x05C0	W	0x00000000	MIPI3 path ID0 SIZE NUMBER
VICAP_MIPI3_SIZE_NUM_ID1	0x05C4	W	0x00000000	MIPI3 path ID1 SIZE NUMBER
VICAP_MIPI3_SIZE_NUM_ID2	0x05C8	W	0x00000000	MIPI3 path ID2 SIZE NUMBER
VICAP_MIPI3_SIZE_NUM_ID3	0x05CC	W	0x00000000	MIPI3 path ID3 SIZE NUMBER
VICAP_MIPI3_FRAME_NUM_VC0	0x05D0	W	0x00000000	The frame number of virtual channel 0
VICAP_MIPI3_FRAME_NUM_VC1	0x05D4	W	0x00000000	The frame number of virtual channel 1
VICAP_MIPI3_FRAME_NUM_VC2	0x05D8	W	0x00000000	The frame number of virtual channel 2
VICAP_MIPI3_FRAME_NUM_VC3	0x05DC	W	0x00000000	The frame number of virtual channel 3
VICAP_MIPI4_ID0_CTRL0	0x0600	W	0x00000000	MIPI4 path id0 control0
VICAP_MIPI4_ID0_CTRL1	0x0604	W	0x00000000	MIPI4 path id0 control1
VICAP_MIPI4_ID1_CTRL0	0x0608	W	0x00000000	MIPI4 path id1 control0
VICAP_MIPI4_ID1_CTRL1	0x060C	W	0x00000000	MIPI4 path id1 control1
VICAP_MIPI4_ID2_CTRL0	0x0610	W	0x00000000	MIPI4 path id2 control0
VICAP_MIPI4_ID2_CTRL1	0x0614	W	0x00000000	MIPI4 path id2 control1
VICAP_MIPI4_ID3_CTRL0	0x0618	W	0x00000000	MIPI4 path id3 control0
VICAP_MIPI4_ID3_CTRL1	0x061C	W	0x00000000	MIPI4 path id3 control1
VICAP_MIPI4_CTRL	0x0620	W	0x00000000	MIPI4 path control
VICAP_MIPI4_FRAME0_ADDR_Y_ID0	0x0624	W	0x00000000	First address of even frame for ID0 Y/RAW/RGB path

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Name	Offset	Size	Reset Value	Description
VICAP_MIPI4_FRAME1_ADDR_Y_ID0	0x0628	W	0x00000000	First address of odd frame for ID0 Y path
VICAP_MIPI4_FRAME0_ADDR_UV_ID0	0x062C	W	0x00000000	First address of even frame for ID0 UV path
VICAP_MIPI4_FRAME1_ADDR_UV_ID0	0x0630	W	0x00000000	First address of odd frame for ID0 UV path
VICAP_MIPI4_VLW_ID0	0x0634	W	0x00000000	Virtual line width for ID0
VICAP_MIPI4_FRAME0_ADDR_Y_ID1	0x0638	W	0x00000000	First address of even frame for ID1 Y/RAW/RGB path
VICAP_MIPI4_FRAME1_ADDR_Y_ID1	0x063C	W	0x00000000	First address of odd frame for ID1 Y/RAW/RGB path
VICAP_MIPI4_FRAME0_ADDR_UV_ID1	0x0640	W	0x00000000	First address of even frame for ID1 UV path
VICAP_MIPI4_FRAME1_ADDR_UV_ID1	0x0644	W	0x00000000	First address of odd frame for ID1 UV path
VICAP_MIPI4_VLW_ID1	0x0648	W	0x00000000	Virtual line width for ID1 path
VICAP_MIPI4_FRAME0_ADDR_Y_ID2	0x064C	W	0x00000000	First address of even frame for ID2 Y/RAW/RGB path
VICAP_MIPI4_FRAME1_ADDR_Y_ID2	0x0650	W	0x00000000	First address of odd frame for ID2 Y/RAW/RGB path
VICAP_MIPI4_FRAME0_ADDR_UV_ID2	0x0654	W	0x00000000	First address of even frame for ID2 UV path
VICAP_MIPI4_FRAME1_ADDR_UV_ID2	0x0658	W	0x00000000	First address of odd frame for ID2 UV path
VICAP_MIPI4_VLW_ID2	0x065C	W	0x00000000	Virtual line width for ID2 path
VICAP_MIPI4_FRAME0_ADDR_Y_ID3	0x0660	W	0x00000000	First address of even frame for ID3 Y/RAW/RGB path
VICAP_MIPI4_FRAME1_ADDR_Y_ID3	0x0664	W	0x00000000	First address of odd frame for ID3 Y/RAW/RGB path
VICAP_MIPI4_FRAME0_ADDR_UV_ID3	0x0668	W	0x00000000	First address of even frame for ID3 UV path
VICAP_MIPI4_FRAME1_ADDR_UV_ID3	0x066C	W	0x00000000	First address of odd frame for ID3 UV path
VICAP_MIPI4_VLW_ID3	0x0670	W	0x00000000	Virtual line width for ID3 path
VICAP_MIPI4_INTEN	0x0674	W	0x00000000	MIPI4 path interrupt enable
VICAP_MIPI4_INTSTAT	0x0678	W	0x00000000	MIPI4 path interrupt status
VICAP_MIPI4_ON_PAD_VALUE	0x067C	W	0x00000000	The ON padding value of MIPI4
VICAP_MIPI4_ID0_EFFECT_CODE	0x0680	W	0x00000000	The effect code of MIPI4 ID0
VICAP_MIPI4_ID1_EFFECT_CODE	0x0684	W	0x00000000	The effect code of MIPI4 ID1
VICAP_MIPI4_ID2_EFFECT_CODE	0x0688	W	0x00000000	The effect code of MIPI4 ID2
VICAP_MIPI4_ID3_EFFECT_CODE	0x068C	W	0x00000000	The effect code of MIPI4 ID3
VICAP_MIPI4_ID0_CROP_START	0x0690	W	0x00000000	The start point of MIPI4 ID0 cropping
VICAP_MIPI4_ID1_CROP_START	0x0694	W	0x00000000	The start point of MIPI4 ID1 cropping
VICAP_MIPI4_ID2_CROP_START	0x0698	W	0x00000000	The start point of MIPI4 ID2 cropping
VICAP_MIPI4_ID3_CROP_START	0x069C	W	0x00000000	The start point of MIPI4 ID3 cropping

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Name	Offset	Size	Reset Value	Description
VICAP_MIPI4_ID0_SET_SIZE	0x06A0	W	0x00000000	The size of MIPI4 ID0
VICAP_MIPI4_ID1_SET_SIZE	0x06A4	W	0x00000000	The size of MIPI4 ID1
VICAP_MIPI4_ID2_SET_SIZE	0x06A8	W	0x00000000	The size of MIPI4 ID2
VICAP_MIPI4_ID3_SET_SIZE	0x06AC	W	0x00000000	The size of MIPI4 ID3
VICAP_MIPI4_LINE_INT_NUM_ID0_1	0x06B0	W	0x00400040	Line number of the MIPI4 path ID0/1 line interrupt
VICAP_MIPI4_LINE_INT_NUM_ID2_3	0x06B4	W	0x00400040	Line number of the MIPI4 path ID2/3 line interrupt
VICAP_MIPI4_LINE_CNT_ID0_1	0x06B8	W	0x00000000	Line count of the MIPI4 path ID0/1
VICAP_MIPI4_LINE_CNT_ID2_3	0x06BC	W	0x00000000	Line count of the MIPI4 path ID2/3
VICAP_MIPI4_SIZE_NUM_ID0	0x06C0	W	0x00000000	MIPI4 path ID0 SIZE NUMBER
VICAP_MIPI4_SIZE_NUM_ID1	0x06C4	W	0x00000000	MIPI4 path ID1 SIZE NUMBER
VICAP_MIPI4_SIZE_NUM_ID2	0x06C8	W	0x00000000	MIPI4 path ID2 SIZE NUMBER
VICAP_MIPI4_SIZE_NUM_ID3	0x06CC	W	0x00000000	MIPI4 path ID3 SIZE NUMBER
VICAP_MIPI4_FRAME_NUM_VC0	0x06D0	W	0x00000000	The frame number of virtual channel 0
VICAP_MIPI4_FRAME_NUM_VC1	0x06D4	W	0x00000000	The frame number of virtual channel 1
VICAP_MIPI4_FRAME_NUM_VC2	0x06D8	W	0x00000000	The frame number of virtual channel 2
VICAP_MIPI4_FRAME_NUM_VC3	0x06DC	W	0x00000000	The frame number of virtual channel 3
VICAP_SCL_CH_CTRL	0x0700	W	0x00000000	Scale channel0 path control
VICAP_SCL_CTRL	0x0704	W	0x00000000	Scale path control
VICAP_SCL_FRAME0_ADDR_CH0	0x0708	W	0x00000000	First address of even frame for CH0 path
VICAP_SCL_FRAME1_ADDR_CH0	0x070C	W	0x00000000	First address of odd frame for CH0 path
VICAP_SCL_VLW_CH0	0x0710	W	0x00000000	Virtual line width for CH0
VICAP_SCL_CH0_BLACK_LEVEL	0x0738	W	0x00000000	Scale channel0 black level
VICAP_TOISP0_CH_CTRL	0x0780	W	0x00000000	TOISP0 path control
VICAP_TOISP0_CROP_SIZE	0x0784	W	0x00000000	The expected width and height of received image
VICAP_TOISP0_CROP_START	0x0788	W	0x00000000	The start point of toisp0 path cropping
VICAP_SPACE_DDR_FREQ	0x07F4	W	0x00000000	Space for ddr frequency conversion.
VICAP_VBLANK_LIMIT_CYCLE_NUM	0x07F8	W	0x00000000	Dclk cycle number for vblank limit.
VICAP_DDR_FREQ_CYCLE_NUM	0x07FC	W	0x00000000	Dclk cycle number for ddr frequency conversion.
VICAP_MMU0_DTE_ADDR	0x0800	W	0x00000000	MMU0 current page table address
VICAP_MMU0_STATUS	0x0804	W	0x00000000	MMU0 status register

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Name	Offset	Size	Reset Value	Description
VICAP_MMU0_COMMAND	0x0808	W	0x00000000	MMU0 command register
VICAP_MMU0_PAGE_FAULT_ADDR	0x080C	W	0x00000000	MMU0 logical address of last page fault
VICAP_MMU0_ZAP_ONE_LINE	0x0810	W	0x00000000	MMU0 Zap cache line register
VICAP_MMU0_INT_RAWSTAT	0x0814	W	0x00000000	MMU0 raw interrupt status register
VICAP_MMU0_INT_CLEAR	0x0818	W	0x00000000	MMU0 interrupt status clear
VICAP_MMU0_INT_MASK	0x081C	W	0x00000000	MMU0 interrupt mask
VICAP_MMU0_INT_STATUS	0x0820	W	0x00000000	MMU0 interrupt status
VICAP_MMU0_AUTO_GATING	0x0824	W	0x00000000	MMU0 auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

6.5.1 Detail Registers Description

VICAP_GLB_CTRL

Address: Operational Base(0x27C10000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x1	ro_axi_idle 1'b0: AXI is working 1'b1: AXI is idle.
30:27	RO	0x0	reserved
26	RW	0x0	sw_dphy2_2x2lane_en 1'b0: DPHY 4lane mode 1'b1: DPHY 2x2lane mode.
25	RW	0x0	sw_dphy1_2x2lane_en 1'b0: DPHY 4lane mode 1'b1: DPHY 2x2lane mode.
24:20	RO	0x00	reserved
19	RW	0x0	sw_acs_isp_c_dis 1'b0: Enable isp coreclk acs signal out 1'b1: Disable isp coreclk acs signal out.
18	RW	0x0	sw_acs_a_dis 1'b0: Enable aclk acs signal out 1'b1: Disable aclk acs signal out.
17	RW	0x0	sw_int_mode 1'b0: sw_intst=sw_inten&sw_intst_raw 1'b1: sw_intst=sw_intst_raw.
16	RW	0x1	sw_dma_adapt_en 1'b0: Disable dma self-adapt(dma will transport data according the configured height) 1'b1: Enable dma self-adapt(dma will transport data according the actual height).
15:13	RW	0x7	sw_press_value Press value.
12	RW	0x1	sw_press_en 1'b0: Disable press 1'b1: Enable press
11:9	RW	0x7	sw_hurry_value Hurry value.
8	RW	0x0	sw_hurry_en 1'b0: Disable hurry 1'b1: Enable hurry

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Bit	Attr	Reset Value	Description
7:6	RW	0x1	sw_dma_group_mode 2'b00: Group 2 (2 bursts gather) 2'b01: Group 4 (4 bursts gather) 2'b10: Group 8 (8 bursts gather) 2'b11: Group 8 (8 bursts gather) This register is valid when sw_dma_group_en=1.
5	RW	0x1	sw_dma_group_en 1'b0: Disable dma burst group 1'b1: Enable dma burst group.
4	RW	0x0	sw_clk_gating_dis 1'b0: Enable the auto clk gating 1'b1: Disable the auto clk gating
3:2	RW	0x0	sw_soft_rst_mode 2'b00: Soft reset and protect toisp path frame integrity; 2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically; 2'b10: Soft reset directly; 2'b11: Reserved.
1	RW	0x0	sw_soft_rst 1'b0: Not reset 1'b1: Reset the VICAP(except MMU/AXI MASTER/REG FILE)
0	RW	0x1	sw_cap_en 1'b0: Disable all interface capture 1'b1: Enable capture(still depends on sw_xxx_cap_en).

VICAP_GLB_INTEN

Address: Operational Base(0x27C10000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	ddr_freq_inten Enable the interrupt of ddr frequency conversion. 1'b0: Disable 1'b1: Enable
30:11	RO	0x00000	reserved
10	RW	0x0	toisp0_fifo_overflow_inten Enable the interrupt of fifo overflow of TOISP0 path. 1'b0: Disable 1'b1: Enable
9	RW	0x0	frame_end_toisp0_ch2_inten Enable the interrupt of frame end for TOISP0 channel2. 1'b0: Disable 1'b1: Enable
8	RW	0x0	frame_end_toisp0_ch1_inten Enable the interrupt of frame end for TOISP0 channel1. 1'b0: Disable 1'b1: Enable
7	RW	0x0	frame_end_toisp0_ch0_inten Enable the interrupt of frame end for TOISP0 channel0. 1'b0: Disable 1'b1: Enable
6	RW	0x0	frame_start_toisp0_ch2_inten Enable the interrupt of frame start for TOISP0 channel2. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	frame_start_toisp0_ch1_inten Enable the interrupt of frame start for TOISP0 channel1. 1'b0: Disable 1'b1: Enable
4	RW	0x0	frame_start_toisp0_ch0_inten Enable the interrupt of frame start for TOISP0 channel0. 1'b0: Disable 1'b1: Enable
3	RW	0x0	dma_fifo_overflow_scl_ch0_inten Enable the interrupt of dma fifo overflow of scale path CH0. 1'b0: Disable 1'b1: Enable
2	RW	0x0	frame1_dma_end_scl_ch0_inten Enable the interrupt of end of odd frame for scale CH0. 1'b0: Disable 1'b1: Enable
1	RW	0x0	frame0_dma_end_scl_ch0_inten Enable the interrupt of end of even frame for scale CH0. 1'b0: Disable 1'b1: Enable
0	RW	0x0	axi0_bus_err_inten Enable the interrupt of axi0 bus error. 1'b0: Disable 1'b1: Enable

VICAP_GLB_INTST

Address: Operational Base(0x27C10000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31	W1C	0x0	ddr_freq_intst 1'b0: No interrupt 1'b1: Interrupt
30:11	RO	0x00000	reserved
10	W1C	0x0	toisp0_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
9	W1C	0x0	frame_end_toisp0_ch2_intst 1'b0: No interrupt 1'b1: Interrupt
8	W1C	0x0	frame_end_toisp0_ch1_intst 1'b0: No interrupt 1'b1: Interrupt
7	W1C	0x0	frame_end_toisp0_ch0_intst 1'b0: No interrupt 1'b1: Interrupt
6	W1C	0x0	frame_start_toisp0_ch2_intst 1'b0: No interrupt 1'b1: Interrupt
5	W1C	0x0	frame_start_toisp0_ch1_intst 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	frame_start_toisp0_ch0_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
3	W1C	0x0	dma_fifo_overflow_scl_ch0_intst 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	frame1_dma_end_scl_ch0_intst 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	frame0_dma_end_scl_ch0_intst 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	axi0_bus_err_intst 1'b0: No interrupt 1'b1: Interrupt

VICAP_GLB_TOLE

Address: Operational Base(0x27C10000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RO	0x0	ro_mipi4_buffer_stat MIPI4 path buffer flag.
26	RO	0x0	ro_mipi4_vblank_stat MIPI4 path vblank flag.
25	RO	0x0	ro_mipi3_buffer_stat MIPI3 path buffer flag.
24	RO	0x0	ro_mipi3_vblank_stat MIPI3 path vblank flag.
23	RO	0x0	ro_mipi2_buffer_stat MIPI3 path buffer flag.
22	RO	0x0	ro_mipi2_vblank_stat MIPI3 path vblank flag.
21	RO	0x0	ro_mipi1_buffer_stat MIPI1 path buffer flag.
20	RO	0x0	ro_mipi1_vblank_stat MIPI1 path vblank flag.
19	RO	0x0	ro_mipi0_buffer_stat MIPI0 path buffer flag.
18	RO	0x0	ro_mipi0_vblank_stat MIPI0 path vblank flag.
17	RO	0x0	ro_dvp_buffer_stat DVP path buffer flag.
16	RO	0x0	ro_dvp_vblank_stat DVP path vblank flag.
15:12	RO	0x0	reserved
11	RW	0x0	sw_mipi4_buffer_en Enable mipi4 path buffer flag.
10	RW	0x0	sw_mipi4_vblank_en Enable mipi4 path vblank flag.
9	RW	0x0	sw_mipi3_buffer_en Enable mipi3 path buffer flag.
8	RW	0x0	sw_mipi3_vblank_en Enable mipi3 path vblank flag.
7	RW	0x0	sw_mipi2_buffer_en Enable mipi2 path buffer flag.
6	RW	0x0	sw_mipi2_vblank_en Enable mipi2 path vblank flag.

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Bit	Attr	Reset Value	Description
5	RW	0x0	sw_mipi1_buffer_en Enable mipi1 path buffer flag.
4	RW	0x0	sw_mipi1_vblank_en Enable mipi1 path vblank flag.
3	RW	0x0	sw_mipi0_buffer_en Enable mipi0 path buffer flag.
2	RW	0x0	sw_mipi0_vblank_en Enable mipi0 path vblank flag.
1	RW	0x0	sw_dvp_buffer_en Enable dvp path buffer flag.
0	RW	0x0	sw_dvp_vblank_en Enable dvp path vblank flag.

VICAP_DVP_CTRL

Address: Operational Base(0x27C10000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_debug_en 1'b0: Normal mode 1'b1: Debug mode.
30:22	RO	0x000	reserved
21:20	RW	0x0	sw_water_line 2'b00: 75% 2'b01: 50% 2'b10: 25% 2'b11: 0%
19:18	RW	0x0	sw_soft_rst_mode 2'b00: Soft reset and protect toisp path frame integrity; 2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically; 2'b10: Soft reset directly; 2'b11: Reserved.
17	RW	0x0	sw_soft_rst 1'b0: Not reset 1'b1: Reset the VICAP DVP path(except MMU/AXI MASTER/REG FILE)
16	RW	0x0	sw_dma_rst Write 1 will reset VICAP DVP path dma. When this bit change to 0,dma is reseted completely.
15:12	RO	0x0	reserved
11	RW	0x0	sw_dma_en_id3 1'b0: Disable 1'b1: Enable
10	RW	0x0	sw_dma_en_id2 1'b0: Disable 1'b1: Enable
9	RW	0x0	sw_dma_en_id1 1'b0: Disable 1'b1: Enable
8	RW	0x0	sw_dma_en_id0 1'b0: Disable 1'b1: Enable
7	RW	0x0	sw_cap_en_id3 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
6	RW	0x0	sw_cap_en_id2 1'b0: Disable 1'b1: Enable
5	RW	0x0	sw_cap_en_id1 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_cap_en_id0 1'b0: Disable 1'b1: Enable
3:1	RO	0x0	reserved
0	RW	0x0	sw_cap_en 1'b0: Disable 1'b1: Enable

VICAP_DVP_INTEN

Address: Operational Base(0x27C10000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	size_err_id3_inten 1'b0: Disable 1'b1: Enable
24	RW	0x0	size_err_id2_inten 1'b0: Disable 1'b1: Enable
23	RW	0x0	size_err_id1_inten 1'b0: Disable 1'b1: Enable
22	RW	0x0	size_err_id0_inten 1'b0: Disable 1'b1: Enable
21	RW	0x0	line_id3_inten 1'b0: Disable 1'b1: Enable
20	RW	0x0	line_id2_inten 1'b0: Disable 1'b1: Enable
19	RW	0x0	line_id1_inten 1'b0: Disable 1'b1: Enable
18	RW	0x0	line_id0_inten 1'b0: Disable 1'b1: Enable
17	RW	0x0	bandwidth_lack_inten Enable the interrupt of bandwidth lack. 1'b0: Disable 1'b1: Enable
16	RW	0x0	dma_fifo_overflow_inten Enable the interrupt of dma fifo overflow . 1'b0: Disable 1'b1: Enable
15	RW	0x0	frame1_dma_end_id3_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
14	RW	0x0	frame0_dma_end_id3_inten Enable the interrupt of end of even frame for ID3. 1'b0: Disable 1'b1: Enable
13	RW	0x0	frame1_dma_end_id2_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
12	RW	0x0	frame0_dma_end_id2_inten Enable the interrupt of end of even frame for ID2. 1'b0: Disable 1'b1: Enable
11	RW	0x0	frame1_dma_end_id1_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
10	RW	0x0	frame0_dma_end_id1_inten Enable the interrupt of end of even frame for ID1. 1'b0: Disable 1'b1: Enable
9	RW	0x0	frame1_dma_end_id0_inten Enable the interrupt of end of odd frame for ID0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	frame0_dma_end_id0_inten Enable the interrupt of end of even frame for ID0. 1'b0: Disable 1'b1: Enable
7	RW	0x0	frame_inf_end_id3_inten Enable the interrupt of interface frame end for ID3. 1'b0: Disable 1'b1: Enable
6	RW	0x0	frame_inf_end_id2_inten Enable the interrupt of interface frame end for ID2. 1'b0: Disable 1'b1: Enable
5	RW	0x0	frame_inf_end_id1_inten Enable the interrupt of interface frame end for ID1. 1'b0: Disable 1'b1: Enable
4	RW	0x0	frame_inf_end_id0_inten Enable the interrupt of interface frame end for ID0. 1'b0: Disable 1'b1: Enable
3	RW	0x0	frame_inf_start_id3_inten Enable the interrupt of interface frame start for ID3. 1'b0: Disable 1'b1: Enable
2	RW	0x0	frame_inf_start_id2_inten Enable the interrupt of interface frame start for ID2. 1'b0: Disable 1'b1: Enable
1	RW	0x0	frame_inf_start_id1_inten Enable the interrupt of interface frame start for ID1. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	frame_inf_start_id0_inten Enable the interrupt of interface frame start for ID0. 1'b0: Disable 1'b1: Enable

VICAP_DVP_INTSTAT

Address: Operational Base(0x27C10000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	W1C	0x0	size_err_id3_intst 1'b0: No interrupt 1'b1: Interrupt
24	W1C	0x0	size_err_id2_intst 1'b0: No interrupt 1'b1: Interrupt
23	W1C	0x0	size_err_id1_intst 1'b0: No interrupt 1'b1: Interrupt
22	W1C	0x0	size_err_id0_intst 1'b0: No interrupt 1'b1: Interrupt
21	W1C	0x0	line_id3_intst 1'b0: No interrupt 1'b1: Interrupt
20	W1C	0x0	line_id2_intst 1'b0: No interrupt 1'b1: Interrupt
19	W1C	0x0	line_id1_intst 1'b0: No interrupt 1'b1: Interrupt
18	W1C	0x0	line_id0_intst 1'b0: No interrupt 1'b1: Interrupt
17	W1C	0x0	bandwidth_lack_intst 1'b0: No interrupt 1'b1: Interrupt
16	W1C	0x0	dma_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
15	W1C	0x0	frame1_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
14	W1C	0x0	frame0_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
13	W1C	0x0	frame1_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
12	W1C	0x0	frame0_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
11	W1C	0x0	frame1_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
10	W1C	0x0	frame0_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
9	W1C	0x0	frame1_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
8	W1C	0x0	frame0_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
7	W1C	0x0	frame_inf_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
6	W1C	0x0	frame_inf_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
5	W1C	0x0	frame_inf_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	frame_inf_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	frame_inf_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	frame_inf_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	frame_inf_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	frame_inf_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt

VICAP_DVP_FORMAT

Address: Operational Base(0x27C10000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_multi_id_mode 2'd0: 1to1 (ID0 will work) 2'd1: 1to2 (ID0/ID1 will work) 2'd2: 1to4 (ID0/ID1/ID2/ID3 will work) 2'd3: Reserved
29	RW	0x0	sw_multi_id_sel Only for BT1120. 1'b0: Parse the id by data[11:8] 1'b1: Parse the id by data[3:0]
28	RW	0x0	sw_multi_id_en 1'b0: Disable multi-ID bt656/bt1120 received 1'b1: Enable multi-ID bt656/bt1120 received
27:24	RO	0x0	reserved
23	RW	0x0	sw_align 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.

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Bit	Attr	Reset Value	Description
22:20	RW	0x0	sw_wrddr_type 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
19:18	RW	0x0	sw_yuv_out_order 2'b00: UYVY 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
17:16	RW	0x0	sw_yuv_in_order 2'b00: UYVY 2'b01: VYUY 2'b10: YUYV 2'b11: YVYU
15	RO	0x0	reserved
14	RW	0x0	sw_uvds_en Enable to uv down-sample id0. 1'b0: Disable 1'b1: Enable
13:12	RW	0x0	sw_raw_width 2'b00: 8bit raw data 2'b01: 10bit raw data 2'b10: 12bit raw data 2'b11: Reserved
11	RO	0x0	reserved
10	RW	0x0	sw_yc_swap 1'b0: No swap for y and c 1'b1: Swap for y and c Only for BT1120 mode.
9	RW	0x0	sw_field_order 1'b0: Odd field first 1'b1: Even field first.
8	RW	0x0	sw_interlace_en 1'b0: Progress 1'b1: Interlace
7	RO	0x0	reserved
6:4	RW	0x0	sw_input_mode 3'b000: BT601 YUV422 3'b001: BT601 RAW 3'b010: BT656 YUV422 3'b011: BT1120 YUV422 3'b100: SONY RAW Others: Reserved
3	RW	0x0	sw_dualedge_en 1'b0: Only use single edge of clock 1'b1: Use double edges of clock Only for BT1120 mode.
2	RW	0x0	sw_low_align_en 1'b0: High alignment 1'b1: Low alignment

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Bit	Attr	Reset Value	Description
1	RW	0x0	sw_href_pol 1'b0: High active 1'b1: Low active
0	RW	0x0	sw_vsync_pol 1'b0: Low active 1'b1: High active

VICAP_DVP_MULTI_ID

Address: Operational Base(0x27C10000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_chid_bit_en_id3 Bit enable for chid_id3. Eg: chid_id3 = 4'b1111 and chid_bit_en_id3 = 4'b0011.Then the data[3:0] = 4'bxx11 will be detected.
27:24	RW	0x0	sw_chid_id3 The channel id for id3.
23:20	RW	0x0	sw_chid_bit_en_id2 Bit enable for chid_id2. Eg: chid_id2 = 4'b1111 and chid_bit_en_id2 = 4'b0011.Then the data[3:0] = 4'bxx11 will be detected.
19:16	RW	0x0	sw_chid_id2 The channel id for id2.
15:12	RW	0x0	sw_chid_bit_en_id1 Bit enable for chid_id1. Eg: chid_id1 = 4'b1111 and chid_bit_en_id1 = 4'b0011.Then the data[3:0] = 4'bxx11 will be detected.
11:8	RW	0x0	sw_chid_id1 The channel id for id1.
7:4	RW	0x0	sw_chid_bit_en_id0 Bit enable for chid_id0. Eg: chid_id0 = 4'b1111 and chid_bit_en_id0 = 4'b0011.Then the data[3:0] = 4'bxx11 will be detected.
3:0	RW	0x0	sw_chid_id0 The channel id for id0.

VICAP_DVP_SAV_EAV

Address: Operational Base(0x27C10000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RW	0xf	sw_eav_blk1 EAV for even field blank.
27:24	RW	0xe	sw_sav_blk1 SAV for even field blank.
23:20	RW	0xd	sw_eav_act1 EAV for even field active.
19:16	RW	0xc	sw_sav_act1 SAV for even field active.
15:12	RW	0xb	sw_eav_blk0 EAV for odd field blank.
11:8	RW	0xa	sw_sav_blk0 SAV for odd field blank.
7:4	RW	0x9	sw_eav_act0 EAV for odd field active.
3:0	RW	0x8	sw_sav_act0 SAV for odd field active.

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VICAP_DVP_CROP_SIZE

Address: Operational Base(0x27C10000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_height The expected height of received image.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_width The expected width of received image.

VICAP_DVP_CROP_START

Address: Operational Base(0x27C10000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_start_y The vertical ordinate of the start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_start_x The horizontal ordinate of the start point.

VICAP_DVP_FRM0_ADDR_Y_ID0

Address: Operational Base(0x27C10000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id0 DVP path frame0 y address.

VICAP_DVP_FRM0_ADDR_UV_ID0

Address: Operational Base(0x27C10000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id0 DVP path frame0 uv address.

VICAP_DVP_FRM1_ADDR_Y_ID0

Address: Operational Base(0x27C10000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id1 DVP path frame1 y address.

VICAP_DVP_FRM1_ADDR_UV_ID0

Address: Operational Base(0x27C10000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 DVP path frame1 uv address.

VICAP_DVP_FRM0_ADDR_Y_ID1

Address: Operational Base(0x27C10000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id1 DVP path frame0 y address for id1.

VICAP_DVP_FRM0_ADDR_UV_ID1

Address: Operational Base(0x27C10000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id1 DVP path frame0 uv address for id1.

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VICAP_DVP_FRM1_ADDR_Y_ID1

Address: Operational Base(0x27C10000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id1 DVP path frame1 y address for id1.

VICAP_DVP_FRM1_ADDR_UV_ID1

Address: Operational Base(0x27C10000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id1 DVP path frame1 uv address for id1.

VICAP_DVP_FRM0_ADDR_Y_ID2

Address: Operational Base(0x27C10000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id2 DVP path frame0 y address for id2.

VICAP_DVP_FRM0_ADDR_UV_ID2

Address: Operational Base(0x27C10000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id2 DVP path frame0 uv address for id2.

VICAP_DVP_FRM1_ADDR_Y_ID2

Address: Operational Base(0x27C10000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id2 DVP path frame1 y address for id2.

VICAP_DVP_FRM1_ADDR_UV_ID2

Address: Operational Base(0x27C10000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id2 DVP path frame1 uv address for id2.

VICAP_DVP_FRM0_ADDR_Y_ID3

Address: Operational Base(0x27C10000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id3 DVP path frame0 y address for id3.

VICAP_DVP_FRM0_ADDR_UV_ID3

Address: Operational Base(0x27C10000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id3 DVP path frame0 uv address for id3.

VICAP_DVP_FRM1_ADDR_Y_ID3

Address: Operational Base(0x27C10000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id3 DVP path frame1 y address for id3.

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VICAP_DVP_FRM1_ADDR_UV_ID3

Address: Operational Base(0x27C10000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id3 DVP path frame1 uv address for id3.

VICAP_DVP_VIR_LINE_WIDTH

Address: Operational Base(0x27C10000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id3 Address force update for id3. Self clear.
30	R/W SC	0x0	sw_addr_force_update_id2 Address force update for id2. Self clear.
29	R/W SC	0x0	sw_addr_force_update_id1 Address force update for id1. Self clear.
28	R/W SC	0x0	sw_addr_force_update_id0 Address force update for id0. Self clear.
27:20	RO	0x00	reserved
19:0	RW	0x00000	sw_vir_line_width DVP path virtual line width.

VICAP_DVP_LINE_INT_NUM_ID0_1

Address: Operational Base(0x27C10000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id1 1'b0: One-time mode 1'b1: Circular mode
30:29	RO	0x0	reserved
28:16	RW	0x0000	sw_line_int_num_id1 For one-time mode, if line_int_num_id1=100, then channel 1 receive 100th line,the line_id1_intst will be 1. For circular mode, if line_int_num_id1=100, then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1.
15	RW	0x0	line_int_mode_id0 1'b0: One-time mode 1'b1: Circular mode
14:13	RO	0x0	reserved
12:0	RW	0x0000	sw_line_int_num_id0 For one-time mode, if line_int_num_id0=100, then channel 0 receive 100th line, the line_id0_intst will be 1. For circular mode, if line_int_num_id0=100, then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1.

VICAP_DVP_LINE_INT_NUM_ID2_3

Address: Operational Base(0x27C10000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id3 1'b0: One-time mode 1'b1: Circular mode
30:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:16	RW	0x0000	sw_line_int_num_id3 For one-time mode, if line_int_num_id3=100, then channel 3 receive 100th line,the line_id3_intst will be 1. For circular mode, if line_int_num_id3=100, then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1.
15	RW	0x0	line_int_mode_id2 1'b0: One-time mode 1'b1: Circular mode
14:13	RO	0x0	reserved
12:0	RW	0x0000	sw_line_int_num_id2 For one-time mode, if line_int_num_id2=100,then channel 2 receive 100th line, the line_id2_intst will be 1. For circular mode, if line_int_num_id2=100, then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1.

VICAP_DVP_LINE_CNT_ID0_1

Address: Operational Base(0x27C10000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id1 Current line count.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id0 Current line count.

VICAP_DVP_LINE_CNT_ID2_3

Address: Operational Base(0x27C10000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id3 Current line count.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id2 Current line count.

VICAP_DVP_SIZE_NUM_ID0

Address: Operational Base(0x27C10000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id0 The id0 UV pixel number in one line.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id0 The id0 pixel number in one line.

VICAP_DVP_SIZE_NUM_ID1

Address: Operational Base(0x27C10000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id1 The id1 line number in one frame.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RO	0x0000	ro_pix_num_id1 The id1 pix number in one line.

VICAP_DVP_SIZE_NUM_ID2

Address: Operational Base(0x27C10000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id2 The id2 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id2 The id2 pixel number in one line.

VICAP_DVP_SIZE_NUM_ID3

Address: Operational Base(0x27C10000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id3 The id3 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id3 The id3 pix number in one line.

VICAP_DVP_SYNC_HEADER

Address: Operational Base(0x27C10000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	ro_sync_header_7 Sync header 7.
27:24	RO	0x0	ro_sync_header_6 Sync header 6.
23:20	RO	0x0	ro_sync_header_5 Sync header 5.
19:16	RO	0x0	ro_sync_header_4 Sync header 4.
15:12	RO	0x0	ro_sync_header_3 Sync header 3.
11:8	RO	0x0	ro_sync_header_2 Sync header 2.
7:4	RO	0x0	ro_sync_header_1 Sync header 1.
3:0	RO	0x0	ro_sync_header_0 Sync header 0. Header 0 is the latest, and header 7 is the earliest.

VICAP_MIPI0_ID0_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id0 1'b0: Odd field first 1'b1: Even field first.

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Bit	Attr	Reset Value	Description
16	RW	0x0	sw_uvds_en_id0 Enable to uv down-sample id0. 1'b0: Disable 1'b1: Enable Note: This bit is valid only when sw_parse_type_id0=4'b1000 && sw_wrddr_type_id0=3'b101.
15:14	RW	0x0	sw_yuyv_out_order_id0 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id0 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id0 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id0 The write ddr type of id0. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
7:4	RW	0x0	sw_parse_type_id0 The parse type of id0. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id0 Enable dma transport id0. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id0 1'b0: Disable drop id0 frame 1'b1: Enable drop id0 frame.
1	RW	0x0	sw_crop_en_id0 Enable to crop for id0. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	sw_cap_en_id0 Enable to capture id0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI0_ID0_CTRL1

Address: Operational Base(0x27C10000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id0 Select command mode for id0. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id0 If sw_mipi0_on_hdr_mode_id0=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id0=1, id0 channel will capture the line which line count value equal to 1.
11:10	RW	0x0	sw_on_hdr_mode_id0 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id0 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id0 Data type for id0.
1:0	RW	0x0	sw_vc_id0 Virtual channel for id0.

VICAP_MIPI0_ID1_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id1 1'b0: Odd field first 1'b1: Even field first.
16	RO	0x0	reserved
15:14	RW	0x0	sw_yuyv_out_order_id1 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id1 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id1 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	sw_wrddr_type_id1 The write ddr type of id0. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
7:4	RW	0x0	sw_parse_type_id1 The parse type of id1. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id1 Enable dma transport id1. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id1 1'b0: Disable drop id1 frame 1'b1: Enable drop id1 frame.
1	RW	0x0	sw_crop_en_id1 Enable to crop for id1. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id1 Enable to capture id1. 1'b0: Disable 1'b1: Enable

VICAP_MIPI0_ID1_CTRL1

Address: Operational Base(0x27C10000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id1 Select command mode for id1. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id1 If sw_mipi0_on_hdr_mode_id1=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id1=1, id1 channel will capture the line which line count value equal to 1.

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Bit	Attr	Reset Value	Description
11:10	RW	0x0	sw_on_hdr_mode_id1 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id1 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id1 Data type for id1.
1:0	RW	0x0	sw_vc_id1 Virtual channel for id1.

VICAP_MIPI0_ID2_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id2 1'b0: Odd field first 1'b1: Even field first.
16	RO	0x0	reserved
15:14	RW	0x0	sw_yuyv_out_order_id2 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id2 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id2 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id2 The write ddr type of id2. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	sw_parse_type_id2 The parse type of id2. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id2 Enable dma transport id2. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id2 1'b0: Disable drop id2 frame 1'b1: Enable drop id2 frame.
1	RW	0x0	sw_crop_en_id2 Enable to crop for id2. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id2 Enable to capture id2. 1'b0: Disable 1'b1: Enable

VICAP_MIPI0_ID2_CTRL1

Address: Operational Base(0x27C10000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id2 Select command mode for id2. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id2 If sw_mipi0_on_hdr_mode_id2=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id2=1, id2 channel will capture the line which line count value equal to 1.
11:10	RW	0x0	sw_on_hdr_mode_id2 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id2 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id2 Data type for id2.

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	sw_vc_id2 Virtual channel for id2.

VICAP_MIPI0_ID3_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id3 1'b0: Odd field first 1'b1: Even field first.
16	RO	0x0	reserved
15:14	RW	0x0	sw_yuyv_out_order_id3 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id3 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id3 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id3 The write ddr type of id3. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
7:4	RW	0x0	sw_parse_type_id3 The parse type of id3. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id3 Enable dma transport id3. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id3 1'b0: Disable drop id3 frame 1'b1: Enable drop id3 frame.

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Bit	Attr	Reset Value	Description
1	RW	0x0	sw_crop_en_id3 Enable to crop for id3. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id3 Enable to capture id3. 1'b0: Disable 1'b1: Enable

VICAP_MIPI0_ID3_CTRL1

Address: Operational Base(0x27C10000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id3 Select command mode for id3. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id3 If sw_mipi0_on_hdr_mode_id3=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id3=1, id3 channel will capture the line which line count value equal to 1.
11:10	RW	0x0	sw_on_hdr_mode_id3 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id3 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id3 Data type for id3.
1:0	RW	0x0	sw_vc_id3 Virtual channel for id3.

VICAP_MIPI0_CTRL

Address: Operational Base(0x27C10000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_debug_en 1'b0: Normal mode 1'b1: Debug mode.
30:22	RO	0x000	reserved
21:20	RW	0x0	sw_water_line 2'b00: 75% 2'b01: 50% 2'b10: 25% 2'b11: 0%
19:18	RW	0x0	sw_soft_rst_mode 2'b00: Soft reset and protect toisp path frame integrity; 2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically; 2'b10: Soft reset directly; 2'b11: Reserved.

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Bit	Attr	Reset Value	Description
17	RW	0x0	sw_soft_rst 1'b0: Not reset 1'b1: Reset the VICAP MIPI0 path(except MMU/AXI MASTER/REG FILE)
16	RW	0x0	sw_dma_rst Write 1 will reset VICAP MIPI0 path dma. When this bit change to 0,dma is reseted completely.
15:14	RW	0x0	sw_drop_frame_main_id The id that is the last coming in HDR mode.
13:12	RW	0x1	sw_drop_frame_m Receive m frames,and drop n frames.(m>0,n>0)
11:9	RW	0x1	sw_drop_frame_n Receive m frames,and drop n frames.(m>0,n>0)
8	RW	0x0	sw_drop_frame_en 1'b0: Disable drop all id frame 1'b1: Enable drop all id frame.
7	RO	0x0	reserved
6:5	RW	0x0	sw_vc_hdr_main_id The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
4	RW	0x0	sw_vc_hdr_protect_en 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
3:1	RO	0x0	reserved
0	RW	0x0	sw_cap_en 1'b0: Disable capture all id 1'b1: Enable capture all id.

VICAP_MIPI0_FRAME0_ADDR_Y_ID0

Address: Operational Base(0x27C10000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id0 First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_Y_ID0

Address: Operational Base(0x27C10000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id0 First address of odd frame for ID0 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME0_ADDR_UV_ID0

Address: Operational Base(0x27C10000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id0 First address of even frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_UV_ID0

Address: Operational Base(0x27C10000) + offset (0x0130)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI0_VLW_ID0

Address: Operational Base(0x27C10000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id0 Address force update for id0. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id0 Virtual line width of even frame for ID0 path(must be aligned to double word).

VICAP_MIPI0_FRAME0_ADDR_Y_ID1

Address: Operational Base(0x27C10000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id1 First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_Y_ID1

Address: Operational Base(0x27C10000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id1 First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME0_ADDR_UV_ID1

Address: Operational Base(0x27C10000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id1 First address of even frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_UV_ID1

Address: Operational Base(0x27C10000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id1 First address of odd frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI0_VLW_ID1

Address: Operational Base(0x27C10000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id1 Address force update for id1. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id1 Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME0_ADDR_Y_ID2

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Address: Operational Base(0x27C10000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id2 First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_Y_ID2

Address: Operational Base(0x27C10000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id2 First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME0_ADDR_UV_ID2

Address: Operational Base(0x27C10000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id2 First address of even frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_UV_ID2

Address: Operational Base(0x27C10000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI0_VLW_ID2

Address: Operational Base(0x27C10000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id2 Address force update for id2. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id2 Virtual line width of even frame for ID2 path(must be aligned to double word).

VICAP_MIPI0_FRAME0_ADDR_Y_ID3

Address: Operational Base(0x27C10000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id3 First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_Y_ID3

Address: Operational Base(0x27C10000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id3 First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI0_FRAME0_ADDR_UV_ID3

Address: Operational Base(0x27C10000) + offset (0x0168)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id3 First address of even frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI0_FRAME1_ADDR_UV_ID3

Address: Operational Base(0x27C10000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id3 First address of odd frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI0_VLW_ID3

Address: Operational Base(0x27C10000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id3 Address force update for id3. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id3 Virtual line width of even frame for ID3 path(must be aligned to double word).

VICAP_MIPI0_INTEN

Address: Operational Base(0x27C10000) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	size_err_id3_inten 1'b0: Disable 1'b1: Enable
26	RW	0x0	size_err_id2_inten 1'b0: Disable 1'b1: Enable
25	RW	0x0	size_err_id1_inten 1'b0: Disable 1'b1: Enable
24	RW	0x0	size_err_id0_inten 1'b0: Disable 1'b1: Enable
23	RW	0x0	line_id3_inten 1'b0: Disable 1'b1: Enable
22	RW	0x0	line_id2_inten 1'b0: Disable 1'b1: Enable
21	RW	0x0	line_id1_inten 1'b0: Disable 1'b1: Enable
20	RW	0x0	line_id0_inten 1'b0: Disable 1'b1: Enable
19	RW	0x0	csi2rx_fifo_overflow_inten 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
18	RW	0x0	bandwidth_lack_inten 1'b0: Disable 1'b1: Enable
17	RW	0x0	dma_uv_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path. 1'b0: Disable 1'b1: Enable
16	RW	0x0	dma_y_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path. 1'b0: Disable 1'b1: Enable
15	RW	0x0	frame1_dma_end_id3_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
14	RW	0x0	frame0_dma_end_id3_inten Enable the interrupt of end of even frame for ID3. 1'b0: Disable 1'b1: Enable
13	RW	0x0	frame1_dma_end_id2_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
12	RW	0x0	frame0_dma_end_id2_inten Enable the interrupt of end of even frame for ID2. 1'b0: Disable 1'b1: Enable
11	RW	0x0	frame1_dma_end_id1_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
10	RW	0x0	frame0_dma_end_id1_inten Enable the interrupt of end of even frame for ID1. 1'b0: Disable 1'b1: Enable
9	RW	0x0	frame1_dma_end_id0_inten Enable the interrupt of end of odd frame for ID0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	frame0_dma_end_id0_inten Enable the interrupt of end of even frame for ID0. 1'b0: Disable 1'b1: Enable
7	RW	0x0	frame_inf_end_id3_inten Enable the interrupt of interface frame end for ID3. 1'b0: Disable 1'b1: Enable
6	RW	0x0	frame_inf_end_id2_inten Enable the interrupt of interface frame end for ID2. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	frame_inf_end_id1_inten Enable the interrupt of interface frame end for ID1. 1'b0: Disable 1'b1: Enable
4	RW	0x0	frame_inf_end_id0_inten Enable the interrupt of interface frame end for ID0. 1'b0: Disable 1'b1: Enable
3	RW	0x0	frame_inf_start_id3_inten Enable the interrupt of interface frame start for ID3. 1'b0: Disable 1'b1: Enable
2	RW	0x0	frame_inf_start_id2_inten Enable the interrupt of interface frame start for ID2. 1'b0: Disable 1'b1: Enable
1	RW	0x0	frame_inf_start_id1_inten Enable the interrupt of interface frame start for ID1. 1'b0: Disable 1'b1: Enable
0	RW	0x0	frame_inf_start_id0_inten Enable the interrupt of interface frame start for ID0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI0_INTSTAT

Address: Operational Base(0x27C10000) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	W1C	0x0	size_err_id3_intst 1'b0: No interrupt 1'b1: Interrupt
26	W1C	0x0	size_err_id2_intst 1'b0: No interrupt 1'b1: Interrupt
25	W1C	0x0	size_err_id1_intst 1'b0: No interrupt 1'b1: Interrupt
24	W1C	0x0	size_err_id0_intst 1'b0: No interrupt 1'b1: Interrupt
23	W1C	0x0	line_id3_intst 1'b0: No interrupt 1'b1: Interrupt
22	W1C	0x0	line_id2_intst 1'b0: No interrupt 1'b1: Interrupt
21	W1C	0x0	line_id1_intst 1'b0: No interrupt 1'b1: Interrupt
20	W1C	0x0	line_id0_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
19	W1C	0x0	csi2rx_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
18	W1C	0x0	bandwidth_lack_intst 1'b0: No interrupt 1'b1: Interrupt
17	W1C	0x0	dma_uv_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
16	W1C	0x0	dma_y_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
15	W1C	0x0	frame1_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
14	W1C	0x0	frame0_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
13	W1C	0x0	frame1_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
12	W1C	0x0	frame0_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
11	W1C	0x0	frame1_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
10	W1C	0x0	frame0_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
9	W1C	0x0	frame1_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
8	W1C	0x0	frame0_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
7	W1C	0x0	frame_inf_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
6	W1C	0x0	frame_inf_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
5	W1C	0x0	frame_inf_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	frame_inf_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	frame_inf_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	frame_inf_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
1	W1C	0x0	frame_inf_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	frame_inf_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt

VICAP_MIPI0_ON_PAD_VALUE

Address: Operational Base(0x27C10000) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_on_pad_value Padding value for ON sensor.

VICAP_MIPI0_ID0_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id0 Effect code of id0 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id0 Effect code of id0 for sony sensor.

VICAP_MIPI0_ID1_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id1 Effect code of id1 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id1 Effect code of id1 for sony sensor.

VICAP_MIPI0_ID2_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id2 Effect code of id2 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id2 Effect code of id2 for sony sensor.

VICAP_MIPI0_ID3_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id3 Effect code of id3 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id3 Effect code of id3 for sony sensor.

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VICAP_MIPI0_ID0_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id0 The start y coordinate for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id0 The start x coordinate for id0. The start x value must be 4 aligned.

VICAP_MIPI0_ID1_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id1 The start y coordinate for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id1 The start x coordinate for id1. The start x value must be 4 aligned.

VICAP_MIPI0_ID2_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id2 The start y coordinate for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id2 The start x coordinate for id2. The start x value must be 4 aligned.

VICAP_MIPI0_ID3_CROP_START

Address: Operational Base(0x27C10000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id3 The start y coordinate for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id3 The start x coordinate for id3. The start x value must be 4 aligned.

VICAP_MIPI0_ID0_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id0 Height for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id0 Width for id0. The width value must be 4 aligned.

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VICAP_MIPI0_ID1_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id1 Height for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id1 Width for id1. The width value must be 4 aligned.

VICAP_MIPI0_ID2_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id2 Height for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id2 Width for id2. The width value must be 4 aligned.

VICAP_MIPI0_ID3_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id3 Height for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id3 Width for id3. The width value must be 4 aligned.

VICAP_MIPI0_LINE_INT_NUM_ID0_1

Address: Operational Base(0x27C10000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id1 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id1 For one-time mode,if line_int_num_id1=100,then channel 1 receive 100th line,the line_id1_intst will be 1. For circular mode ,if line_int_num_id1=100,then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1.
15	RW	0x0	line_int_mode_id0 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id0 For one-time mode,if line_int_num_id0=100,then channel 0 receive 100th line,the line_id0_intst will be 1. For circular mode ,if line_int_num_id0=100,then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1.

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VICAP_MIPI0_LINE_INT_NUM_ID2_3

Address: Operational Base(0x27C10000) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id3 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id3 For one-time mode,if line_int_num_id3=100,then channel 3 receive 100th line,the line_id3_intst will be 1. For circular mode ,if line_int_num_id3=100,then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1.
15	RW	0x0	line_int_mode_id2 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id2 For one-time mode,if line_int_num_id2=100,then channel 2 receive 100th line,the line_id2_intst will be 1. For circular mode ,if line_int_num_id2=100,then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1.

VICAP_MIPI0_LINE_CNT_ID0_1

Address: Operational Base(0x27C10000) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id1 Current line count for id1.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id0 Current line count for id0.

VICAP_MIPI0_LINE_CNT_ID2_3

Address: Operational Base(0x27C10000) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id3 Current line count for id3.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id2 Current line count for id2.

VICAP_MIPI0_SIZE_NUM_ID0

Address: Operational Base(0x27C10000) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id0 The id0 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id0 The id0 pixel number in one line.

VICAP_MIPI0_SIZE_NUM_ID1

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Address: Operational Base(0x27C10000) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id1 The id1 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id1 The id1 pixel number in one line.

VICAP_MIPI0_SIZE_NUM_ID2

Address: Operational Base(0x27C10000) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id2 The id2 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id2 The id2 pixel number in one line.

VICAP_MIPI0_SIZE_NUM_ID3

Address: Operational Base(0x27C10000) + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id3 The id3 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id3 The id3 pixel number in one line.

VICAP_MIPI0_FRAME_NUM_VC0

Address: Operational Base(0x27C10000) + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc0 The frame number of frame end of virtual channel 0.
15:0	RO	0x0000	ro_frame_num_start_vc0 The frame number of frame start of virtual channel 0.

VICAP_MIPI0_FRAME_NUM_VC1

Address: Operational Base(0x27C10000) + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc1 The frame number of frame end of virtual channel 1.
15:0	RO	0x0000	ro_frame_num_start_vc1 The frame number of frame start of virtual channel 1.

VICAP_MIPI0_FRAME_NUM_VC2

Address: Operational Base(0x27C10000) + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc2 The frame number of frame end of virtual channel 2.
15:0	RO	0x0000	ro_frame_num_start_vc2 The frame number of frame start of virtual channel 2.

VICAP_MIPI0_FRAME_NUM_VC3

Address: Operational Base(0x27C10000) + offset (0x01DC)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc3 The frame number of frame end of virtual channel 3.
15:0	RO	0x0000	ro_frame_num_start_vc3 The frame number of frame start of virtual channel 3.

VICAP_MIPI1_ID0_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id0 1'b0: Odd field first 1'b1: Even field first.
16	RW	0x0	sw_uvds_en_id0 Enable to uv down-sample id0. 1'b0: Disable 1'b1: Enable Note: This bit is valid only when sw_parse_type_id0=4'b1000 && sw_wrddr_type_id0=3'b101.
15:14	RW	0x0	sw_yuyv_out_order_id0 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id0 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id0 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id0 The write ddr type of id0. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
7:4	RW	0x0	sw_parse_type_id0 The parse type of id0. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.

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Bit	Attr	Reset Value	Description
3	RW	0x0	sw_dma_en_id0 Enable dma transport id0. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id0 1'b0: Disable drop id0 frame 1'b1: Enable drop id0 frame.
1	RW	0x0	sw_crop_en_id0 Enable to crop for id0. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id0 Enable to capture id0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI1_ID0_CTRL1

Address: Operational Base(0x27C10000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id0 Select command mode for id0. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id0 If sw_mipi0_on_hdr_mode_id0=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id0=1, id0 channel will capture the line which line count value equal to 1.
11:10	RW	0x0	sw_on_hdr_mode_id0 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id0 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id0 Data type for id0.
1:0	RW	0x0	sw_vc_id0 Virtual channel for id0.

VICAP_MIPI1_ID1_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id1 1'b0: Odd field first 1'b1: Even field first.
16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	sw_yuyv_out_order_id1 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id1 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id1 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id1 The write ddr type of id0. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
7:4	RW	0x0	sw_parse_type_id1 The parse type of id1. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id1 Enable dma transport id1. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id1 1'b0: Disable drop id1 frame 1'b1: Enable drop id1 frame.
1	RW	0x0	sw_crop_en_id1 Enable to crop for id1. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id1 Enable to capture id1. 1'b0: Disable 1'b1: Enable

VICAP_MIPI1_ID1_CTRL1

Address: Operational Base(0x27C10000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id1 Select command mode for id1. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id1 If sw_mipi0_on_hdr_mode_id1=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id1=1, id1 channel will capture the line which line count value equal to 1.
11:10	RW	0x0	sw_on_hdr_mode_id1 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id1 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id1 Data type for id1.
1:0	RW	0x0	sw_vc_id1 Virtual channel for id1.

VICAP_MIPI1_ID2_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id2 1'b0: Odd field first 1'b1: Even field first.
16	RO	0x0	reserved
15:14	RW	0x0	sw_yuyv_out_order_id2 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id2 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id2 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	sw_wrddr_type_id2 The write ddr type of id2. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
7:4	RW	0x0	sw_parse_type_id2 The parse type of id2. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id2 Enable dma transport id2. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id2 1'b0: Disable drop id2 frame 1'b1: Enable drop id2 frame.
1	RW	0x0	sw_crop_en_id2 Enable to crop for id2. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id2 Enable to capture id2. 1'b0: Disable 1'b1: Enable

VICAP_MIPI1_ID2_CTRL1

Address: Operational Base(0x27C10000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id2 Select command mode for id2. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id2 If sw_mipi0_on_hdr_mode_id2=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id2=1, id2 channel will capture the line which line count value equal to 1.

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Bit	Attr	Reset Value	Description
11:10	RW	0x0	sw_on_hdr_mode_id2 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id2 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id2 Data type for id2.
1:0	RW	0x0	sw_vc_id2 Virtual channel for id2.

VICAP_MIPI1_ID3_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id3 1'b0: Odd field first 1'b1: Even field first.
16	RO	0x0	reserved
15:14	RW	0x0	sw_yuyv_out_order_id3 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id3 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id3 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id3 The write ddr type of id3. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	sw_parse_type_id3 The parse type of id3. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id3 Enable dma transport id3. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id3 1'b0: Disable drop id3 frame 1'b1: Enable drop id3 frame.
1	RW	0x0	sw_crop_en_id3 Enable to crop for id3. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id3 Enable to capture id3. 1'b0: Disable 1'b1: Enable

VICAP_MIPI1_ID3_CTRL1

Address: Operational Base(0x27C10000) + offset (0x031C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id3 Select command mode for id3. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id3 If sw_mipi0_on_hdr_mode_id3=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id3=1, id3 channel will capture the line which line count value equal to 1.
11:10	RW	0x0	sw_on_hdr_mode_id3 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id3 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id3 Data type for id3.

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	sw_vc_id3 Virtual channel for id3.

VICAP_MIPI1_CTRL

Address: Operational Base(0x27C10000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_debug_en 1'b0: Normal mode 1'b1: Debug mode.
30:22	RO	0x000	reserved
21:20	RW	0x0	sw_water_line 2'b00: 75% 2'b01: 50% 2'b10: 25% 2'b11: 0%
19:18	RW	0x0	sw_soft_rst_mode 2'b00: Soft reset and protect toisp path frame integrity; 2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically; 2'b10: Soft reset directly; 2'b11: Reserved.
17	RW	0x0	sw_soft_rst 1'b0: Not reset 1'b1: Reset the VICAP MIPI1 path(except MMU/AXI MASTER/REG FILE)
16	RW	0x0	sw_dma_rst Write 1 will reset VICAP MIPI1 path dma. When this bit change to 0,dma is reseted completely.
15:14	RW	0x0	sw_drop_frame_main_id The id that is the last coming in HDR mode.
13:12	RW	0x0	sw_drop_frame_m Receive m frames,and drop n frames.(m>0,n>0)
11:9	RW	0x0	sw_drop_frame_n Receive m frames,and drop n frames.(m>0,n>0)
8	RW	0x0	sw_drop_frame_en 1'b0: Disable drop all id frame 1'b1: Enable drop all id frame.
7	RO	0x0	reserved
6:5	RW	0x0	sw_vc_hdr_main_id The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
4	RW	0x0	sw_vc_hdr_protect_en 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
3:1	RO	0x0	reserved
0	RW	0x0	sw_cap_en 1'b0: Disable capture all id 1'b1: Enable capture all id.

VICAP_MIPI1_FRAME0_ADDR_Y_ID0

Address: Operational Base(0x27C10000) + offset (0x0324)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id0 First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_Y_ID0

Address: Operational Base(0x27C10000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id0 First address of odd frame for ID0 Y path(must be aligned to double word).

VICAP_MIPI1_FRAME0_ADDR_UV_ID0

Address: Operational Base(0x27C10000) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id0 First address of even frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_UV_ID0

Address: Operational Base(0x27C10000) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI1_VLW_ID0

Address: Operational Base(0x27C10000) + offset (0x0334)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id0 Address force update for id0. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id0 Virtual line width of even frame for ID0 path(must be aligned to double word).

VICAP_MIPI1_FRAME0_ADDR_Y_ID1

Address: Operational Base(0x27C10000) + offset (0x0338)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id1 First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_Y_ID1

Address: Operational Base(0x27C10000) + offset (0x033C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id1 First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME0_ADDR_UV_ID1

Address: Operational Base(0x27C10000) + offset (0x0340)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id1 First address of even frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_UV_ID1

Address: Operational Base(0x27C10000) + offset (0x0344)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id1 First address of odd frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI1_VLW_ID1

Address: Operational Base(0x27C10000) + offset (0x0348)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id1 Address force update for id1. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id1 Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME0_ADDR_Y_ID2

Address: Operational Base(0x27C10000) + offset (0x034C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id2 First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_Y_ID2

Address: Operational Base(0x27C10000) + offset (0x0350)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id2 First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME0_ADDR_UV_ID2

Address: Operational Base(0x27C10000) + offset (0x0354)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id2 First address of even frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_UV_ID2

Address: Operational Base(0x27C10000) + offset (0x0358)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI1_VLW_ID2

Address: Operational Base(0x27C10000) + offset (0x035C)

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Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id2 Address force update for id2. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id2 Virtual line width of even frame for ID2 path(must be aligned to double word).

VICAP_MIPI1_FRAME0_ADDR_Y_ID3

Address: Operational Base(0x27C10000) + offset (0x0360)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id3 First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_Y_ID3

Address: Operational Base(0x27C10000) + offset (0x0364)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id3 First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI1_FRAME0_ADDR_UV_ID3

Address: Operational Base(0x27C10000) + offset (0x0368)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id3 First address of even frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI1_FRAME1_ADDR_UV_ID3

Address: Operational Base(0x27C10000) + offset (0x036C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id3 First address of odd frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI1_VLW_ID3

Address: Operational Base(0x27C10000) + offset (0x0370)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id3 Address force update for id3. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id3 Virtual line width of even frame for ID3 path(must be aligned to double word).

VICAP_MIPI1_INTEN

Address: Operational Base(0x27C10000) + offset (0x0374)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	size_err_id3_inten 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
26	RW	0x0	size_err_id2_inten 1'b0: Disable 1'b1: Enable
25	RW	0x0	size_err_id1_inten 1'b0: Disable 1'b1: Enable
24	RW	0x0	size_err_id0_inten 1'b0: Disable 1'b1: Enable
23	RW	0x0	line_id3_inten 1'b0: Disable 1'b1: Enable
22	RW	0x0	line_id2_inten 1'b0: Disable 1'b1: Enable
21	RW	0x0	line_id1_inten 1'b0: Disable 1'b1: Enable
20	RW	0x0	line_id0_inten 1'b0: Disable 1'b1: Enable
19	RW	0x0	csi2rx_fifo_overflow_inten 1'b0: Disable 1'b1: Enable
18	RW	0x0	bandwidth_lack_inten 1'b0: Disable 1'b1: Enable
17	RW	0x0	dma_uv_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path. 1'b0: Disable 1'b1: Enable
16	RW	0x0	dma_y_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path. 1'b0: Disable 1'b1: Enable
15	RW	0x0	frame1_dma_end_id3_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
14	RW	0x0	frame0_dma_end_id3_inten Enable the interrupt of end of even frame for ID3. 1'b0: Disable 1'b1: Enable
13	RW	0x0	frame1_dma_end_id2_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
12	RW	0x0	frame0_dma_end_id2_inten Enable the interrupt of end of even frame for ID2. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
11	RW	0x0	frame1_dma_end_id1_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
10	RW	0x0	frame0_dma_end_id1_inten Enable the interrupt of end of even frame for ID1. 1'b0: Disable 1'b1: Enable
9	RW	0x0	frame1_dma_end_id0_inten Enable the interrupt of end of odd frame for ID0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	frame0_dma_end_id0_inten Enable the interrupt of end of even frame for ID0. 1'b0: Disable 1'b1: Enable
7	RW	0x0	frame_inf_end_id3_inten Enable the interrupt of interface frame end for ID3. 1'b0: Disable 1'b1: Enable
6	RW	0x0	frame_inf_end_id2_inten Enable the interrupt of interface frame end for ID2. 1'b0: Disable 1'b1: Enable
5	RW	0x0	frame_inf_end_id1_inten Enable the interrupt of interface frame end for ID1. 1'b0: Disable 1'b1: Enable
4	RW	0x0	frame_inf_end_id0_inten Enable the interrupt of interface frame end for ID0. 1'b0: Disable 1'b1: Enable
3	RW	0x0	frame_inf_start_id3_inten Enable the interrupt of interface frame start for ID3. 1'b0: Disable 1'b1: Enable
2	RW	0x0	frame_inf_start_id2_inten Enable the interrupt of interface frame start for ID2. 1'b0: Disable 1'b1: Enable
1	RW	0x0	frame_inf_start_id1_inten Enable the interrupt of interface frame start for ID1. 1'b0: Disable 1'b1: Enable
0	RW	0x0	frame_inf_start_id0_inten Enable the interrupt of interface frame start for ID0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI1_INTSTAT

Address: Operational Base(0x27C10000) + offset (0x0378)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27	W1C	0x0	size_err_id3_intst 1'b0: No interrupt 1'b1: Interrupt
26	W1C	0x0	size_err_id2_intst 1'b0: No interrupt 1'b1: Interrupt
25	W1C	0x0	size_err_id1_intst 1'b0: No interrupt 1'b1: Interrupt
24	W1C	0x0	size_err_id0_intst 1'b0: No interrupt 1'b1: Interrupt
23	W1C	0x0	line_id3_intst 1'b0: No interrupt 1'b1: Interrupt
22	W1C	0x0	line_id2_intst 1'b0: No interrupt 1'b1: Interrupt
21	W1C	0x0	line_id1_intst 1'b0: No interrupt 1'b1: Interrupt
20	W1C	0x0	line_id0_intst 1'b0: No interrupt 1'b1: Interrupt
19	W1C	0x0	csi2rx_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
18	W1C	0x0	bandwidth_lack_intst 1'b0: No interrupt 1'b1: Interrupt
17	W1C	0x0	dma_uv_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
16	W1C	0x0	dma_y_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
15	W1C	0x0	frame1_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
14	W1C	0x0	frame0_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
13	W1C	0x0	frame1_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
12	W1C	0x0	frame0_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
11	W1C	0x0	frame1_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
10	W1C	0x0	frame0_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
9	W1C	0x0	frame1_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
8	W1C	0x0	frame0_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
7	W1C	0x0	frame_inf_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
6	W1C	0x0	frame_inf_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
5	W1C	0x0	frame_inf_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	frame_inf_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	frame_inf_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	frame_inf_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	frame_inf_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	frame_inf_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt

VICAP_MIPI1_ON_PAD_VALUE

Address: Operational Base(0x27C10000) + offset (0x037C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_on_pad_value Padding value for ON sensor.

VICAP_MIPI1_ID0_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x0380)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id0 Effect code of id0 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id0 Effect code of id0 for sony sensor.

VICAP_MIPI1_ID1_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x0384)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id1 Effect code of id1 for sony sensor.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_sony_effect_code0_id1 Effect code of id1 for sony sensor.

VICAP_MIPI1_ID2_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x0388)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id2 Effect code of id2 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id2 Effect code of id2 for sony sensor.

VICAP_MIPI1_ID3_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x038C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id3 Effect code of id3 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id3 Effect code of id3 for sony sensor.

VICAP_MIPI1_ID0_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0390)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id0 The start y coordinate for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id0 The start x coordinate for id0. The start x value must be 4 aligned.

VICAP_MIPI1_ID1_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0394)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id1 The start y coordinate for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id1 The start x coordinate for id1. The start x value must be 4 aligned.

VICAP_MIPI1_ID2_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0398)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id2 The start y coordinate for id2.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_start_x_id2 The start x coordinate for id2. The start x value must be 4 aligned.

VICAP_MIPI1_ID3_CROP_START

Address: Operational Base(0x27C10000) + offset (0x039C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id3 The start y coordinate for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id3 The start x coordinate for id3. The start x value must be 4 aligned.

VICAP_MIPI1_ID0_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id0 Height for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id0 Width for id0. The width value must be 4 aligned.

VICAP_MIPI1_ID1_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x03A4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id1 Height for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id1 Width for id1. The width value must be 4 aligned.

VICAP_MIPI1_ID2_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id2 Height for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id2 Width for id2. The width value must be 4 aligned.

VICAP_MIPI1_ID3_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x03AC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id3 Height for id3.

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Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id3 Width for id3. The width value must be 4 aligned.

VICAP_MIPI1_LINE_INT_NUM_ID0_1

Address: Operational Base(0x27C10000) + offset (0x03B0)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id1 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id1 For one-time mode,if line_int_num_id1=100,then channel 1 receive 100th line,the line_id1_intst will be 1. For circular mode ,if line_int_num_id1=100,then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1.
15	RW	0x0	line_int_mode_id0 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id0 For one-time mode,if line_int_num_id0=100,then channel 0 receive 100th line,the line_id0_intst will be 1. For circular mode ,if line_int_num_id0=100,then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1.

VICAP_MIPI1_LINE_INT_NUM_ID2_3

Address: Operational Base(0x27C10000) + offset (0x03B4)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id3 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id3 For one-time mode,if line_int_num_id3=100,then channel 3 receive 100th line,the line_id3_intst will be 1. For circular mode ,if line_int_num_id3=100,then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1.
15	RW	0x0	line_int_mode_id2 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id2 For one-time mode,if line_int_num_id2=100,then channel 2 receive 100th line,the line_id2_intst will be 1. For circular mode ,if line_int_num_id2=100,then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1.

VICAP_MIPI1_LINE_CNT_ID0_1

Address: Operational Base(0x27C10000) + offset (0x03B8)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id1 Current line count for id1.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id0 Current line count for id0.

VICAP_MIPI1_LINE_CNT_ID2_3

Address: Operational Base(0x27C10000) + offset (0x03BC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id3 Current line count for id3.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id2 Current line count for id2.

VICAP_MIPI1_SIZE_NUM_ID0

Address: Operational Base(0x27C10000) + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id0 The id0 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id0 The id0 pixel number in one line.

VICAP_MIPI1_SIZE_NUM_ID1

Address: Operational Base(0x27C10000) + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id1 The id1 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id1 The id1 pixel number in one line.

VICAP_MIPI1_SIZE_NUM_ID2

Address: Operational Base(0x27C10000) + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id2 The id2 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id2 The id2 pixel number in one line.

VICAP_MIPI1_SIZE_NUM_ID3

Address: Operational Base(0x27C10000) + offset (0x03CC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id3 The id3 line number in one frame.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RO	0x0000	ro_pix_num_id3 The id3 pixel number in one line.

VICAP_MIPI1_FRAME_NUM_VC0

Address: Operational Base(0x27C10000) + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc0 The frame number of frame end of virtual channel 0.
15:0	RO	0x0000	ro_frame_num_start_vc0 The frame number of frame start of virtual channel 0.

VICAP_MIPI1_FRAME_NUM_VC1

Address: Operational Base(0x27C10000) + offset (0x03D4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc1 The frame number of frame end of virtual channel 1.
15:0	RO	0x0000	ro_frame_num_start_vc1 The frame number of frame start of virtual channel 1.

VICAP_MIPI1_FRAME_NUM_VC2

Address: Operational Base(0x27C10000) + offset (0x03D8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc2 The frame number of frame end of virtual channel 2.
15:0	RO	0x0000	ro_frame_num_start_vc2 The frame number of frame start of virtual channel 2.

VICAP_MIPI1_FRAME_NUM_VC3

Address: Operational Base(0x27C10000) + offset (0x03DC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc3 The frame number of frame end of virtual channel 3.
15:0	RO	0x0000	ro_frame_num_start_vc3 The frame number of frame start of virtual channel 3.

VICAP_MIPI2_ID0_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id0 1'b0: Odd field first 1'b1: Even field first.
16	RW	0x0	sw_uvds_en_id0 Enable to uv down-sample id0. 1'b0: Disable 1'b1: Enable Note: This bit is valid only when sw_parse_type_id0=4'b1000 && sw_wrddr_type_id0=3'b101.
15:14	RW	0x0	sw_yuyv_out_order_id0 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	sw_yuyv_in_order_id0 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id0 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id0 The write ddr type of id0. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
7:4	RW	0x0	sw_parse_type_id0 The parse type of id0. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id0 Enable dma transport id0. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id0 1'b0: Disable drop id0 frame 1'b1: Enable drop id0 frame.
1	RW	0x0	sw_crop_en_id0 Enable to crop for id0. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id0 Enable to capture id0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI2_ID0_CTRL1

Address: Operational Base(0x27C10000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id0 Select command mode for id0. 1'b0: Not command mode 1'b1: Command mode

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	sw_on_hdr_line_cnt_id0 If sw_mipi2_on_hdr_mode_id0=1(2),the line count value will circulate between 0~1(2).And if sw_mipi2_on_hdr_line_cnt_id0=1, id0 channel will capture the line which line count value equal to 1.
11:10	RW	0x0	sw_on_hdr_mode_id0 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id0 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id0 Data type for id0.
1:0	RW	0x0	sw_vc_id0 Virtual channel for id0.

VICAP_MIPI2_ID1_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0408)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id1 1'b0: Odd field first 1'b1: Even field first.
16	RO	0x0	reserved
15:14	RW	0x0	sw_yuyv_out_order_id1 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id1 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id1 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id1 The write ddr type of id0. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	sw_parse_type_id1 The parse type of id1. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id1 Enable dma transport id1. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id1 1'b0: Disable drop id1 frame 1'b1: Enable drop id1 frame.
1	RW	0x0	sw_crop_en_id1 Enable to crop for id1. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id1 Enable to capture id1. 1'b0: Disable 1'b1: Enable

VICAP_MIPI2_ID1_CTRL1

Address: Operational Base(0x27C10000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id1 Select command mode for id1. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id1 If sw_mipi0_on_hdr_mode_id1=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id1=1, id1 channel will capture the line which line count value equal to 1.
11:10	RW	0x0	sw_on_hdr_mode_id1 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id1 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id1 Data type for id1.

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	sw_vc_id1 Virtual channel for id1.

VICAP_MIPI2_ID2_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id2 1'b0: Odd field first 1'b1: Even field first.
16	RO	0x0	reserved
15:14	RW	0x0	sw_yuyv_out_order_id2 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id2 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id2 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id2 The write ddr type of id2. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
7:4	RW	0x0	sw_parse_type_id2 The parse type of id2. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id2 Enable dma transport id2. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id2 1'b0: Disable drop id2 frame 1'b1: Enable drop id2 frame.

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Bit	Attr	Reset Value	Description
1	RW	0x0	sw_crop_en_id2 Enable to crop for id2. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id2 Enable to capture id2. 1'b0: Disable 1'b1: Enable

VICAP_MIPI2_ID2_CTRL1

Address: Operational Base(0x27C10000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id2 Select command mode for id2. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id2 If sw_mipi0_on_hdr_mode_id2=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id2=1, id2 channel will capture the line which line count value equal to 1.
11:10	RW	0x0	sw_on_hdr_mode_id2 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id2 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id2 Data type for id2.
1:0	RW	0x0	sw_vc_id2 Virtual channel for id2.

VICAP_MIPI2_ID3_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id3 1'b0: Odd field first 1'b1: Even field first.
16	RO	0x0	reserved
15:14	RW	0x0	sw_yuyv_out_order_id3 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id3 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU

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Bit	Attr	Reset Value	Description
11	RW	0x0	sw_align_id3 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id3 The write ddr type of id3. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
7:4	RW	0x0	sw_parse_type_id3 The parse type of id3. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id3 Enable dma transport id3. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id3 1'b0: Disable drop id3 frame 1'b1: Enable drop id3 frame.
1	RW	0x0	sw_crop_en_id3 Enable to crop for id3. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id3 Enable to capture id3. 1'b0: Disable 1'b1: Enable

VICAP_MIPI2_ID3_CTRL1

Address: Operational Base(0x27C10000) + offset (0x041C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id3 Select command mode for id3. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id3 If sw_mipi0_on_hdr_mode_id3=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id3=1, id3 channel will capture the line which line count value equal to 1.

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Bit	Attr	Reset Value	Description
11:10	RW	0x0	sw_on_hdr_mode_id3 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id3 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id3 Data type for id3.
1:0	RW	0x0	sw_vc_id3 Virtual channel for id3.

VICAP_MIPI2_CTRL

Address: Operational Base(0x27C10000) + offset (0x0420)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_debug_en 1'b0: Normal mode 1'b1: Debug mode.
30:22	RO	0x000	reserved
21:20	RW	0x0	sw_water_line 2'b00: 75% 2'b01: 50% 2'b10: 25% 2'b11: 0%
19:18	RW	0x0	sw_soft_rst_mode 2'b00: Soft reset and protect toisp path frame integrity; 2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically; 2'b10: Soft reset directly; 2'b11: Reserved.
17	RW	0x0	sw_soft_rst 1'b0: Not reset 1'b1: Reset the VICAP MIPI2 path(except MMU/AXI MASTER/REG FILE)
16	RW	0x0	sw_dma_rst Write 1 will reset VICAP MIPI2 path dma. When this bit change to 0,dma is reseted completely.
15:14	RW	0x0	sw_drop_frame_main_id The id that is the last coming in HDR mode.
13:12	RW	0x0	sw_drop_frame_m Receive m frames,and drop n frames.(m>0,n>0)
11:9	RW	0x0	sw_drop_frame_n Receive m frames,and drop n frames.(m>0,n>0)
8	RW	0x0	sw_drop_frame_en 1'b0: Disable drop all id frame 1'b1: Enable drop all id frame.
7	RO	0x0	reserved
6:5	RW	0x0	sw_vc_hdr_main_id The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.

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Bit	Attr	Reset Value	Description
4	RW	0x0	sw_vc_hdr_protect_en 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
3:1	RO	0x0	reserved
0	RW	0x0	sw_cap_en 1'b0: Disable capture all id 1'b1: Enable capture all id.

VICAP_MIPI2_FRAME0_ADDR_Y_ID0

Address: Operational Base(0x27C10000) + offset (0x0424)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id0 First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_Y_ID0

Address: Operational Base(0x27C10000) + offset (0x0428)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id0 First address of odd frame for ID0 Y path(must be aligned to double word).

VICAP_MIPI2_FRAME0_ADDR_UV_ID0

Address: Operational Base(0x27C10000) + offset (0x042C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id0 First address of even frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_UV_ID0

Address: Operational Base(0x27C10000) + offset (0x0430)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI2_VLW_ID0

Address: Operational Base(0x27C10000) + offset (0x0434)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id0 Address force update for id0. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id0 Virtual line width of even frame for ID0 path(must be aligned to double word).

VICAP_MIPI2_FRAME0_ADDR_Y_ID1

Address: Operational Base(0x27C10000) + offset (0x0438)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id1 First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_Y_ID1

Address: Operational Base(0x27C10000) + offset (0x043C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id1 First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME0_ADDR_UV_ID1

Address: Operational Base(0x27C10000) + offset (0x0440)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id1 First address of even frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_UV_ID1

Address: Operational Base(0x27C10000) + offset (0x0444)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id1 First address of odd frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI2_VLW_ID1

Address: Operational Base(0x27C10000) + offset (0x0448)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id1 Address force update for id1. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id1 Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME0_ADDR_Y_ID2

Address: Operational Base(0x27C10000) + offset (0x044C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id2 First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_Y_ID2

Address: Operational Base(0x27C10000) + offset (0x0450)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id2 First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME0_ADDR_UV_ID2

Address: Operational Base(0x27C10000) + offset (0x0454)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id2 First address of even frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_UV_ID2

Address: Operational Base(0x27C10000) + offset (0x0458)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI2_VLW_ID2

Address: Operational Base(0x27C10000) + offset (0x045C)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id2 Address force update for id2. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id2 Virtual line width of even frame for ID2 path(must be aligned to double word).

VICAP_MIPI2_FRAME0_ADDR_Y_ID3

Address: Operational Base(0x27C10000) + offset (0x0460)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id3 First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_Y_ID3

Address: Operational Base(0x27C10000) + offset (0x0464)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id3 First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI2_FRAME0_ADDR_UV_ID3

Address: Operational Base(0x27C10000) + offset (0x0468)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id3 First address of even frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI2_FRAME1_ADDR_UV_ID3

Address: Operational Base(0x27C10000) + offset (0x046C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id3 First address of odd frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI2_VLW_ID3

Address: Operational Base(0x27C10000) + offset (0x0470)

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Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id3 Address force update for id3. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id3 Virtual line width of even frame for ID3 path(must be aligned to double word).

VICAP_MIPI2_INTEN

Address: Operational Base(0x27C10000) + offset (0x0474)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	size_err_id3_inten 1'b0: Disable 1'b1: Enable
26	RW	0x0	size_err_id2_inten 1'b0: Disable 1'b1: Enable
25	RW	0x0	size_err_id1_inten 1'b0: Disable 1'b1: Enable
24	RW	0x0	size_err_id0_inten 1'b0: Disable 1'b1: Enable
23	RW	0x0	line_id3_inten 1'b0: Disable 1'b1: Enable
22	RW	0x0	line_id2_inten 1'b0: Disable 1'b1: Enable
21	RW	0x0	line_id1_inten 1'b0: Disable 1'b1: Enable
20	RW	0x0	line_id0_inten 1'b0: Disable 1'b1: Enable
19	RW	0x0	csi2rx_fifo_overflow_inten 1'b0: Disable 1'b1: Enable
18	RW	0x0	bandwidth_lack_inten 1'b0: Disable 1'b1: Enable
17	RW	0x0	dma_uv_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path. 1'b0: Disable 1'b1: Enable
16	RW	0x0	dma_y_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
15	RW	0x0	frame1_dma_end_id3_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
14	RW	0x0	frame0_dma_end_id3_inten Enable the interrupt of end of even frame for ID3. 1'b0: Disable 1'b1: Enable
13	RW	0x0	frame1_dma_end_id2_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
12	RW	0x0	frame0_dma_end_id2_inten Enable the interrupt of end of even frame for ID2. 1'b0: Disable 1'b1: Enable
11	RW	0x0	frame1_dma_end_id1_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
10	RW	0x0	frame0_dma_end_id1_inten Enable the interrupt of end of even frame for ID1. 1'b0: Disable 1'b1: Enable
9	RW	0x0	frame1_dma_end_id0_inten Enable the interrupt of end of odd frame for ID0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	frame0_dma_end_id0_inten Enable the interrupt of end of even frame for ID0. 1'b0: Disable 1'b1: Enable
7	RW	0x0	frame_inf_end_id3_inten Enable the interrupt of interface frame end for ID3. 1'b0: Disable 1'b1: Enable
6	RW	0x0	frame_inf_end_id2_inten Enable the interrupt of interface frame end for ID2. 1'b0: Disable 1'b1: Enable
5	RW	0x0	frame_inf_end_id1_inten Enable the interrupt of interface frame end for ID1. 1'b0: Disable 1'b1: Enable
4	RW	0x0	frame_inf_end_id0_inten Enable the interrupt of interface frame end for ID0. 1'b0: Disable 1'b1: Enable
3	RW	0x0	frame_inf_start_id3_inten Enable the interrupt of interface frame start for ID3. 1'b0: Disable 1'b1: Enable
2	RW	0x0	frame_inf_start_id2_inten Enable the interrupt of interface frame start for ID2. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	frame_inf_start_id1_inten Enable the interrupt of interface frame start for ID1. 1'b0: Disable 1'b1: Enable
0	RW	0x0	frame_inf_start_id0_inten Enable the interrupt of interface frame start for ID0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI2_INTSTAT

Address: Operational Base(0x27C10000) + offset (0x0478)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	W1C	0x0	size_err_id3_intst 1'b0: No interrupt 1'b1: Interrupt
26	W1C	0x0	size_err_id2_intst 1'b0: No interrupt 1'b1: Interrupt
25	W1C	0x0	size_err_id1_intst 1'b0: No interrupt 1'b1: Interrupt
24	W1C	0x0	size_err_id0_intst 1'b0: No interrupt 1'b1: Interrupt
23	W1C	0x0	line_id3_intst 1'b0: No interrupt 1'b1: Interrupt
22	W1C	0x0	line_id2_intst 1'b0: No interrupt 1'b1: Interrupt
21	W1C	0x0	line_id1_intst 1'b0: No interrupt 1'b1: Interrupt
20	W1C	0x0	line_id0_intst 1'b0: No interrupt 1'b1: Interrupt
19	W1C	0x0	csi2rx_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
18	W1C	0x0	bandwidth_lack_intst 1'b0: No interrupt 1'b1: Interrupt
17	W1C	0x0	dma_uv_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
16	W1C	0x0	dma_y_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
15	W1C	0x0	frame1_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
14	W1C	0x0	frame0_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
13	W1C	0x0	frame1_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
12	W1C	0x0	frame0_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
11	W1C	0x0	frame1_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
10	W1C	0x0	frame0_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
9	W1C	0x0	frame1_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
8	W1C	0x0	frame0_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
7	W1C	0x0	frame_inf_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
6	W1C	0x0	frame_inf_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
5	W1C	0x0	frame_inf_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	frame_inf_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	frame_inf_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	frame_inf_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	frame_inf_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	frame_inf_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt

VICAP_MIPI2_ON_PAD_VALUE

Address: Operational Base(0x27C10000) + offset (0x047C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_on_pad_value Padding value for ON sensor.

VICAP_MIPI2_ID0_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x0480)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RW	0x0000	sw_sony_effect_code1_id0 Effect code of id0 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id0 Effect code of id0 for sony sensor.

VICAP_MIPI2_ID1_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x0484)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id1 Effect code of id1 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id1 Effect code of id1 for sony sensor.

VICAP_MIPI2_ID2_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x0488)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id2 Effect code of id2 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id2 Effect code of id2 for sony sensor.

VICAP_MIPI2_ID3_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x048C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id3 Effect code of id3 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id3 Effect code of id3 for sony sensor.

VICAP_MIPI2_ID0_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0490)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id0 The start y coordinate for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id0 The start x coordinate for id0. The start x value must be 4 aligned.

VICAP_MIPI2_ID1_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0494)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id1 The start y coordinate for id1.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_start_x_id1 The start x coordinate for id1. The start x value must be 4 aligned.

VICAP_MIPI2_ID2_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0498)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id2 The start y coordinate for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id2 The start x coordinate for id2. The start x value must be 4 aligned.

VICAP_MIPI2_ID3_CROP_START

Address: Operational Base(0x27C10000) + offset (0x049C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id3 The start y coordinate for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id3 The start x coordinate for id3. The start x value must be 4 aligned.

VICAP_MIPI2_ID0_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id0 Height for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id0 Width for id0. The width value must be 4 aligned.

VICAP_MIPI2_ID1_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id1 Height for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id1 Width for id1. The width value must be 4 aligned.

VICAP_MIPI2_ID2_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id2 Height for id2.

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Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id2 Width for id2. The width value must be 4 aligned.

VICAP_MIPI2_ID3_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x04AC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id3 Height for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id3 Width for id3. The width value must be 4 aligned.

VICAP_MIPI2_LINE_INT_NUM_ID0_1

Address: Operational Base(0x27C10000) + offset (0x04B0)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id1 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id1 For one-time mode,if line_int_num_id1=100,then channel 1 receive 100th line,the line_id1_intst will be 1. For circular mode ,if line_int_num_id1=100,then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1.
15	RW	0x0	line_int_mode_id0 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id0 For one-time mode,if line_int_num_id0=100,then channel 0 receive 100th line,the line_id0_intst will be 1. For circular mode ,if line_int_num_id0=100,then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1.

VICAP_MIPI2_LINE_INT_NUM_ID2_3

Address: Operational Base(0x27C10000) + offset (0x04B4)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id3 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id3 For one-time mode,if line_int_num_id3=100,then channel 3 receive 100th line,the line_id3_intst will be 1. For circular mode ,if line_int_num_id3=100,then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1.

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Bit	Attr	Reset Value	Description
15	RW	0x0	line_int_mode_id2 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id2 For one-time mode,if line_int_num_id2=100,then channel 2 receive 100th line,the line_id2_intst will be 1. For circular mode ,if line_int_num_id2=100,then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1.

VICAP_MIPI2_LINE_CNT_ID0_1

Address: Operational Base(0x27C10000) + offset (0x04B8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id1 Current line count for id1.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id0 Current line count for id0.

VICAP_MIPI2_LINE_CNT_ID2_3

Address: Operational Base(0x27C10000) + offset (0x04BC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id3 Current line count for id3.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id2 Current line count for id2.

VICAP_MIPI2_SIZE_NUM_ID0

Address: Operational Base(0x27C10000) + offset (0x04C0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id0 The id0 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id0 The id0 pixel number in one line.

VICAP_MIPI2_SIZE_NUM_ID1

Address: Operational Base(0x27C10000) + offset (0x04C4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id1 The id1 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id1 The id1 pixel number in one line.

VICAP_MIPI2_SIZE_NUM_ID2

Address: Operational Base(0x27C10000) + offset (0x04C8)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id2 The id2 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id2 The id2 pixel number in one line.

VICAP_MIPI2_SIZE_NUM_ID3

Address: Operational Base(0x27C10000) + offset (0x04CC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id3 The id3 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id3 The id3 pixel number in one line.

VICAP_MIPI2_FRAME_NUM_VC0

Address: Operational Base(0x27C10000) + offset (0x04D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc0 The frame number of frame end of virtual channel 0.
15:0	RO	0x0000	ro_frame_num_start_vc0 The frame number of frame start of virtual channel 0.

VICAP_MIPI2_FRAME_NUM_VC1

Address: Operational Base(0x27C10000) + offset (0x04D4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc1 The frame number of frame end of virtual channel 1.
15:0	RO	0x0000	ro_frame_num_start_vc1 The frame number of frame start of virtual channel 1.

VICAP_MIPI2_FRAME_NUM_VC2

Address: Operational Base(0x27C10000) + offset (0x04D8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc2 The frame number of frame end of virtual channel 2.
15:0	RO	0x0000	ro_frame_num_start_vc2 The frame number of frame start of virtual channel 2.

VICAP_MIPI2_FRAME_NUM_VC3

Address: Operational Base(0x27C10000) + offset (0x04DC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc3 The frame number of frame end of virtual channel 3.
15:0	RO	0x0000	ro_frame_num_start_vc3 The frame number of frame start of virtual channel 3.

VICAP_MIPI3_ID0_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17	RW	0x0	sw_field_order_id0 1'b0: Odd field first 1'b1: Even field first.
16	RW	0x0	sw_uvds_en_id0 Enable to uv down-sample id0. 1'b0: Disable 1'b1: Enable Note: This bit is valid only when sw_parse_type_id0=4'b1000 && sw_wrddr_type_id0=3'b101.
15:14	RW	0x0	sw_yuyv_out_order_id0 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id0 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id0 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id0 The write ddr type of id0. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
7:4	RW	0x0	sw_parse_type_id0 The parse type of id0. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id0 Enable dma transport id0. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id0 1'b0: Disable drop id0 frame 1'b1: Enable drop id0 frame.

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Bit	Attr	Reset Value	Description
1	RW	0x0	sw_crop_en_id0 Enable to crop for id0. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id0 Enable to capture id0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI3_ID0_CTRL1

Address: Operational Base(0x27C10000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id0 Select command mode for id0. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id0 If sw_mipi2_on_hdr_mode_id0=1(2),the line count value will circulate between 0~1(2).And if sw_mipi2_on_hdr_line_cnt_id0=1, id0 channel will capture the line which line count value equal to 1.
11:10	RW	0x0	sw_on_hdr_mode_id0 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id0 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id0 Data type for id0.
1:0	RW	0x0	sw_vc_id0 Virtual channel for id0.

VICAP_MIPI3_ID1_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0508)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id1 1'b0: Odd field first 1'b1: Even field first.
16	RO	0x0	reserved
15:14	RW	0x0	sw_yuyv_out_order_id1 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id1 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU

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Bit	Attr	Reset Value	Description
11	RW	0x0	sw_align_id1 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id1 The write ddr type of id0. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
7:4	RW	0x0	sw_parse_type_id1 The parse type of id1. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id1 Enable dma transport id1. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id1 1'b0: Disable drop id1 frame 1'b1: Enable drop id1 frame.
1	RW	0x0	sw_crop_en_id1 Enable to crop for id1. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id1 Enable to capture id1. 1'b0: Disable 1'b1: Enable

VICAP_MIPI3_ID1_CTRL1

Address: Operational Base(0x27C10000) + offset (0x050C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id1 Select command mode for id1. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id1 If sw_mipi0_on_hdr_mode_id1=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id1=1, id1 channel will capture the line which line count value equal to 1.

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Bit	Attr	Reset Value	Description
11:10	RW	0x0	sw_on_hdr_mode_id1 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id1 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id1 Data type for id1.
1:0	RW	0x0	sw_vc_id1 Virtual channel for id1.

VICAP_MIPI3_ID2_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0510)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id2 1'b0: Odd field first 1'b1: Even field first.
16	RO	0x0	reserved
15:14	RW	0x0	sw_yuyv_out_order_id2 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id2 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id2 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id2 The write ddr type of id2. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	sw_parse_type_id2 The parse type of id2. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id2 Enable dma transport id2. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id2 1'b0: Disable drop id2 frame 1'b1: Enable drop id2 frame.
1	RW	0x0	sw_crop_en_id2 Enable to crop for id2. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id2 Enable to capture id2. 1'b0: Disable 1'b1: Enable

VICAP_MIPI3_ID2_CTRL1

Address: Operational Base(0x27C10000) + offset (0x0514)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id2 Select command mode for id2. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id2 If sw_mipi0_on_hdr_mode_id2=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id2=1, id2 channel will capture the line which line count value equal to 1.
11:10	RW	0x0	sw_on_hdr_mode_id2 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id2 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id2 Data type for id2.

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	sw_vc_id2 Virtual channel for id2.

VICAP_MIPI3_ID3_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0518)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id3 1'b0: Odd field first 1'b1: Even field first.
16	RO	0x0	reserved
15:14	RW	0x0	sw_yuyv_out_order_id3 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id3 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id3 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id3 The write ddr type of id3. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
7:4	RW	0x0	sw_parse_type_id3 The parse type of id3. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id3 Enable dma transport id3. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id3 1'b0: Disable drop id3 frame 1'b1: Enable drop id3 frame.

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Bit	Attr	Reset Value	Description
1	RW	0x0	sw_crop_en_id3 Enable to crop for id3. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id3 Enable to capture id3. 1'b0: Disable 1'b1: Enable

VICAP_MIPI3_ID3_CTRL1

Address: Operational Base(0x27C10000) + offset (0x051C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id3 Select command mode for id3. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id3 If sw_mipi0_on_hdr_mode_id3=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id3=1, id3 channel will capture the line which line count value equal to 1.
11:10	RW	0x0	sw_on_hdr_mode_id3 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id3 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id3 Data type for id3.
1:0	RW	0x0	sw_vc_id3 Virtual channel for id3.

VICAP_MIPI3_CTRL

Address: Operational Base(0x27C10000) + offset (0x0520)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_debug_en 1'b0: Normal mode 1'b1: Debug mode.
30:22	RO	0x000	reserved
21:20	RW	0x0	sw_water_line 2'b00: 75% 2'b01: 50% 2'b10: 25% 2'b11: 0%
19:18	RW	0x0	sw_soft_rst_mode 2'b00: Soft reset and protect toisp path frame integrity; 2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically; 2'b10: Soft reset directly; 2'b11: Reserved.

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Bit	Attr	Reset Value	Description
17	RW	0x0	sw_soft_rst 1'b0: Not reset 1'b1: Reset the VICAP MIPI3 path(except MMU/AXI MASTER/REG FILE)
16	RW	0x0	sw_dma_rst Write 1 will reset VICAP MIPI3 path dma. When this bit change to 0,dma is reseted completely.
15:14	RW	0x0	sw_drop_frame_main_id The id that is the last coming in HDR mode.
13:12	RW	0x0	sw_drop_frame_m Receive m frames,and drop n frames.(m>0,n>0)
11:9	RW	0x0	sw_drop_frame_n Receive m frames,and drop n frames.(m>0,n>0)
8	RW	0x0	sw_drop_frame_en 1'b0: Disable drop all id frame 1'b1: Enable drop all id frame.
7	RO	0x0	reserved
6:5	RW	0x0	sw_vc_hdr_main_id The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
4	RW	0x0	sw_vc_hdr_protect_en 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
3:1	RO	0x0	reserved
0	RW	0x0	sw_cap_en 1'b0: Disable capture all id 1'b1: Enable capture all id.

VICAP_MIPI3_FRAME0_ADDR_Y_ID0

Address: Operational Base(0x27C10000) + offset (0x0524)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id0 First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_Y_ID0

Address: Operational Base(0x27C10000) + offset (0x0528)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id0 First address of odd frame for ID0 Y path(must be aligned to double word).

VICAP_MIPI3_FRAME0_ADDR_UV_ID0

Address: Operational Base(0x27C10000) + offset (0x052C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id0 First address of even frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_UV_ID0

Address: Operational Base(0x27C10000) + offset (0x0530)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI3_VLW_ID0

Address: Operational Base(0x27C10000) + offset (0x0534)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id0 Address force update for id0. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id0 Virtual line width of even frame for ID0 path(must be aligned to double word).

VICAP_MIPI3_FRAME0_ADDR_Y_ID1

Address: Operational Base(0x27C10000) + offset (0x0538)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id1 First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_Y_ID1

Address: Operational Base(0x27C10000) + offset (0x053C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id1 First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME0_ADDR_UV_ID1

Address: Operational Base(0x27C10000) + offset (0x0540)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id1 First address of even frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_UV_ID1

Address: Operational Base(0x27C10000) + offset (0x0544)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id1 First address of odd frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI3_VLW_ID1

Address: Operational Base(0x27C10000) + offset (0x0548)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id1 Address force update for id1. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id1 Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME0_ADDR_Y_ID2

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Address: Operational Base(0x27C10000) + offset (0x054C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id2 First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_Y_ID2

Address: Operational Base(0x27C10000) + offset (0x0550)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id2 First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME0_ADDR_UV_ID2

Address: Operational Base(0x27C10000) + offset (0x0554)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id2 First address of even frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_UV_ID2

Address: Operational Base(0x27C10000) + offset (0x0558)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI3_VLW_ID2

Address: Operational Base(0x27C10000) + offset (0x055C)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id2 Address force update for id2. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id2 Virtual line width of even frame for ID2 path(must be aligned to double word).

VICAP_MIPI3_FRAME0_ADDR_Y_ID3

Address: Operational Base(0x27C10000) + offset (0x0560)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id3 First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_Y_ID3

Address: Operational Base(0x27C10000) + offset (0x0564)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id3 First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI3_FRAME0_ADDR_UV_ID3

Address: Operational Base(0x27C10000) + offset (0x0568)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id3 First address of even frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI3_FRAME1_ADDR_UV_ID3

Address: Operational Base(0x27C10000) + offset (0x056C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id3 First address of odd frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI3_VLW_ID3

Address: Operational Base(0x27C10000) + offset (0x0570)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id3 Address force update for id3. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id3 Virtual line width of even frame for ID3 path(must be aligned to double word).

VICAP_MIPI3_INTEN

Address: Operational Base(0x27C10000) + offset (0x0574)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	size_err_id3_inten 1'b0: Disable 1'b1: Enable
26	RW	0x0	size_err_id2_inten 1'b0: Disable 1'b1: Enable
25	RW	0x0	size_err_id1_inten 1'b0: Disable 1'b1: Enable
24	RW	0x0	size_err_id0_inten 1'b0: Disable 1'b1: Enable
23	RW	0x0	line_id3_inten 1'b0: Disable 1'b1: Enable
22	RW	0x0	line_id2_inten 1'b0: Disable 1'b1: Enable
21	RW	0x0	line_id1_inten 1'b0: Disable 1'b1: Enable
20	RW	0x0	line_id0_inten 1'b0: Disable 1'b1: Enable
19	RW	0x0	csi2rx_fifo_overflow_inten 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
18	RW	0x0	bandwidth_lack_inten 1'b0: Disable 1'b1: Enable
17	RW	0x0	dma_uv_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path. 1'b0: Disable 1'b1: Enable
16	RW	0x0	dma_y_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path. 1'b0: Disable 1'b1: Enable
15	RW	0x0	frame1_dma_end_id3_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
14	RW	0x0	frame0_dma_end_id3_inten Enable the interrupt of end of even frame for ID3. 1'b0: Disable 1'b1: Enable
13	RW	0x0	frame1_dma_end_id2_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
12	RW	0x0	frame0_dma_end_id2_inten Enable the interrupt of end of even frame for ID2. 1'b0: Disable 1'b1: Enable
11	RW	0x0	frame1_dma_end_id1_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
10	RW	0x0	frame0_dma_end_id1_inten Enable the interrupt of end of even frame for ID1. 1'b0: Disable 1'b1: Enable
9	RW	0x0	frame1_dma_end_id0_inten Enable the interrupt of end of odd frame for ID0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	frame0_dma_end_id0_inten Enable the interrupt of end of even frame for ID0. 1'b0: Disable 1'b1: Enable
7	RW	0x0	frame_inf_end_id3_inten Enable the interrupt of interface frame end for ID3. 1'b0: Disable 1'b1: Enable
6	RW	0x0	frame_inf_end_id2_inten Enable the interrupt of interface frame end for ID2. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	frame_inf_end_id1_inten Enable the interrupt of interface frame end for ID1. 1'b0: Disable 1'b1: Enable
4	RW	0x0	frame_inf_end_id0_inten Enable the interrupt of interface frame end for ID0. 1'b0: Disable 1'b1: Enable
3	RW	0x0	frame_inf_start_id3_inten Enable the interrupt of interface frame start for ID3. 1'b0: Disable 1'b1: Enable
2	RW	0x0	frame_inf_start_id2_inten Enable the interrupt of interface frame start for ID2. 1'b0: Disable 1'b1: Enable
1	RW	0x0	frame_inf_start_id1_inten Enable the interrupt of interface frame start for ID1. 1'b0: Disable 1'b1: Enable
0	RW	0x0	frame_inf_start_id0_inten Enable the interrupt of interface frame start for ID0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI3_INTSTAT

Address: Operational Base(0x27C10000) + offset (0x0578)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	W1C	0x0	size_err_id3_intst 1'b0: No interrupt 1'b1: Interrupt
26	W1C	0x0	size_err_id2_intst 1'b0: No interrupt 1'b1: Interrupt
25	W1C	0x0	size_err_id1_intst 1'b0: No interrupt 1'b1: Interrupt
24	W1C	0x0	size_err_id0_intst 1'b0: No interrupt 1'b1: Interrupt
23	W1C	0x0	line_id3_intst 1'b0: No interrupt 1'b1: Interrupt
22	W1C	0x0	line_id2_intst 1'b0: No interrupt 1'b1: Interrupt
21	W1C	0x0	line_id1_intst 1'b0: No interrupt 1'b1: Interrupt
20	W1C	0x0	line_id0_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
19	W1C	0x0	csi2rx_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
18	W1C	0x0	bandwidth_lack_intst 1'b0: No interrupt 1'b1: Interrupt
17	W1C	0x0	dma_uv_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
16	W1C	0x0	dma_y_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
15	W1C	0x0	frame1_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
14	W1C	0x0	frame0_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
13	W1C	0x0	frame1_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
12	W1C	0x0	frame0_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
11	W1C	0x0	frame1_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
10	W1C	0x0	frame0_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
9	W1C	0x0	frame1_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
8	W1C	0x0	frame0_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
7	W1C	0x0	frame_inf_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
6	W1C	0x0	frame_inf_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
5	W1C	0x0	frame_inf_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	frame_inf_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	frame_inf_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	frame_inf_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
1	W1C	0x0	frame_inf_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	frame_inf_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt

VICAP_MIPI3_ON_PAD_VALUE

Address: Operational Base(0x27C10000) + offset (0x057C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_on_pad_value Padding value for ON sensor.

VICAP_MIPI3_ID0_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x0580)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id0 Effect code of id0 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id0 Effect code of id0 for sony sensor.

VICAP_MIPI3_ID1_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x0584)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id1 Effect code of id1 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id1 Effect code of id1 for sony sensor.

VICAP_MIPI3_ID2_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x0588)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id2 Effect code of id2 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id2 Effect code of id2 for sony sensor.

VICAP_MIPI3_ID3_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x058C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id3 Effect code of id3 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id3 Effect code of id3 for sony sensor.

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VICAP_MIPI3_ID0_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0590)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id0 The start y coordinate for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id0 The start x coordinate for id0. The start x value must be 4 aligned.

VICAP_MIPI3_ID1_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0594)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id1 The start y coordinate for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id1 The start x coordinate for id1. The start x value must be 4 aligned.

VICAP_MIPI3_ID2_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0598)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id2 The start y coordinate for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id2 The start x coordinate for id2. The start x value must be 4 aligned.

VICAP_MIPI3_ID3_CROP_START

Address: Operational Base(0x27C10000) + offset (0x059C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id3 The start y coordinate for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id3 The start x coordinate for id3. The start x value must be 4 aligned.

VICAP_MIPI3_ID0_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x05A0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id0 Height for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id0 Width for id0. The width value must be 4 aligned.

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VICAP_MIPI3_ID1_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x05A4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id1 Height for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id1 Width for id1. The width value must be 4 aligned.

VICAP_MIPI3_ID2_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x05A8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id2 Height for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id2 Width for id2. The width value must be 4 aligned.

VICAP_MIPI3_ID3_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x05AC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id3 Height for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id3 Width for id3. The width value must be 4 aligned.

VICAP_MIPI3_LINE_INT_NUM_ID0_1

Address: Operational Base(0x27C10000) + offset (0x05B0)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id1 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id1 For one-time mode,if line_int_num_id1=100,then channel 1 receive 100th line,the line_id1_intst will be 1. For circular mode ,if line_int_num_id1=100,then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1.
15	RW	0x0	line_int_mode_id0 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id0 For one-time mode,if line_int_num_id0=100,then channel 0 receive 100th line,the line_id0_intst will be 1. For circular mode ,if line_int_num_id0=100,then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1.

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VICAP_MIPI3_LINE_INT_NUM_ID2_3

Address: Operational Base(0x27C10000) + offset (0x05B4)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id3 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id3 For one-time mode,if line_int_num_id3=100,then channel 3 receive 100th line,the line_id3_intst will be 1. For circular mode ,if line_int_num_id3=100,then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1.
15	RW	0x0	line_int_mode_id2 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id2 For one-time mode,if line_int_num_id2=100,then channel 2 receive 100th line,the line_id2_intst will be 1. For circular mode ,if line_int_num_id2=100,then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1.

VICAP_MIPI3_LINE_CNT_ID0_1

Address: Operational Base(0x27C10000) + offset (0x05B8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id1 Current line count for id1.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id0 Current line count for id0.

VICAP_MIPI3_LINE_CNT_ID2_3

Address: Operational Base(0x27C10000) + offset (0x05BC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id3 Current line count for id3.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id2 Current line count for id2.

VICAP_MIPI3_SIZE_NUM_ID0

Address: Operational Base(0x27C10000) + offset (0x05C0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id0 The id0 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id0 The id0 pixel number in one line.

VICAP_MIPI3_SIZE_NUM_ID1

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Address: Operational Base(0x27C10000) + offset (0x05C4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id1 The id1 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id1 The id1 pixel number in one line.

VICAP_MIPI3_SIZE_NUM_ID2

Address: Operational Base(0x27C10000) + offset (0x05C8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id2 The id2 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id2 The id2 pixel number in one line.

VICAP_MIPI3_SIZE_NUM_ID3

Address: Operational Base(0x27C10000) + offset (0x05CC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id3 The id3 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id3 The id3 pixel number in one line.

VICAP_MIPI3_FRAME_NUM_VC0

Address: Operational Base(0x27C10000) + offset (0x05D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc0 The frame number of frame end of virtual channel 0.
15:0	RO	0x0000	ro_frame_num_start_vc0 The frame number of frame start of virtual channel 0.

VICAP_MIPI3_FRAME_NUM_VC1

Address: Operational Base(0x27C10000) + offset (0x05D4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc1 The frame number of frame end of virtual channel 1.
15:0	RO	0x0000	ro_frame_num_start_vc1 The frame number of frame start of virtual channel 1.

VICAP_MIPI3_FRAME_NUM_VC2

Address: Operational Base(0x27C10000) + offset (0x05D8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc2 The frame number of frame end of virtual channel 2.
15:0	RO	0x0000	ro_frame_num_start_vc2 The frame number of frame start of virtual channel 2.

VICAP_MIPI3_FRAME_NUM_VC3

Address: Operational Base(0x27C10000) + offset (0x05DC)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc3 The frame number of frame end of virtual channel 3.
15:0	RO	0x0000	ro_frame_num_start_vc3 The frame number of frame start of virtual channel 3.

VICAP_MIPI4_ID0_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id0 1'b0: Odd field first 1'b1: Even field first.
16	RW	0x0	sw_uvds_en_id0 Enable to uv down-sample id0. 1'b0: Disable 1'b1: Enable Note: This bit is valid only when sw_parse_type_id0=4'b1000 && sw_wrddr_type_id0=3'b101.
15:14	RW	0x0	sw_yuyv_out_order_id0 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id0 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id0 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id0 The write ddr type of id0. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
7:4	RW	0x0	sw_parse_type_id0 The parse type of id0. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.

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Bit	Attr	Reset Value	Description
3	RW	0x0	sw_dma_en_id0 Enable dma transport id0. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id0 1'b0: Disable drop id0 frame 1'b1: Enable drop id0 frame.
1	RW	0x0	sw_crop_en_id0 Enable to crop for id0. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id0 Enable to capture id0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI4_ID0_CTRL1

Address: Operational Base(0x27C10000) + offset (0x0604)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id0 Select command mode for id0. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id0 If sw_mipi2_on_hdr_mode_id0=1(2),the line count value will circulate between 0~1(2).And if sw_mipi2_on_hdr_line_cnt_id0=1, id0 channel will capture the line which line count value equal to 1.
11:10	RW	0x0	sw_on_hdr_mode_id0 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id0 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id0 Data type for id0.
1:0	RW	0x0	sw_vc_id0 Virtual channel for id0.

VICAP_MIPI4_ID1_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0608)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id1 1'b0: Odd field first 1'b1: Even field first.
16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	sw_yuyv_out_order_id1 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id1 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id1 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id1 The write ddr type of id0. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
7:4	RW	0x0	sw_parse_type_id1 The parse type of id1. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id1 Enable dma transport id1. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id1 1'b0: Disable drop id1 frame 1'b1: Enable drop id1 frame.
1	RW	0x0	sw_crop_en_id1 Enable to crop for id1. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id1 Enable to capture id1. 1'b0: Disable 1'b1: Enable

VICAP_MIPI4_ID1_CTRL1

Address: Operational Base(0x27C10000) + offset (0x060C)

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Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id1 Select command mode for id1. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id1 If sw_mipi0_on_hdr_mode_id1=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id1=1, id1 channel will capture the line which line count value equal to 1.
11:10	RW	0x0	sw_on_hdr_mode_id1 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id1 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id1 Data type for id1.
1:0	RW	0x0	sw_vc_id1 Virtual channel for id1.

VICAP_MIPI4_ID2_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0610)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id2 1'b0: Odd field first 1'b1: Even field first.
16	RO	0x0	reserved
15:14	RW	0x0	sw_yuyv_out_order_id2 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id2 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id2 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	sw_wrddr_type_id2 The write ddr type of id2. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved
7:4	RW	0x0	sw_parse_type_id2 The parse type of id2. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id2 Enable dma transport id2. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id2 1'b0: Disable drop id2 frame 1'b1: Enable drop id2 frame.
1	RW	0x0	sw_crop_en_id2 Enable to crop for id2. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id2 Enable to capture id2. 1'b0: Disable 1'b1: Enable

VICAP_MIPI4_ID2_CTRL1

Address: Operational Base(0x27C10000) + offset (0x0614)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id2 Select command mode for id2. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id2 If sw_mipi0_on_hdr_mode_id2=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id2=1, id2 channel will capture the line which line count value equal to 1.

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Bit	Attr	Reset Value	Description
11:10	RW	0x0	sw_on_hdr_mode_id2 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id2 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id2 Data type for id2.
1:0	RW	0x0	sw_vc_id2 Virtual channel for id2.

VICAP_MIPI4_ID3_CTRL0

Address: Operational Base(0x27C10000) + offset (0x0618)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	sw_field_order_id3 1'b0: Odd field first 1'b1: Even field first.
16	RO	0x0	reserved
15:14	RW	0x0	sw_yuyv_out_order_id3 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
13:12	RW	0x0	sw_yuyv_in_order_id3 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
11	RW	0x0	sw_align_id3 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
10:8	RW	0x0	sw_wrddr_type_id3 The write ddr type of id3. 3'b000: Raw-compact 3'b001: Raw-uncompact 3'b010: YUV packet 3'b011: YUV 400 3'b100: YUV 422sp 3'b101: YUV 420sp Others: Reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	sw_parse_type_id3 The parse type of id3. 4'b0000: For raw8 4'b0001: For raw10 4'b0010: For raw12 4'b0011: For raw14 4'b0100: For raw16 4'b0111: For rgb888 4'b1000: For yuv422 8bit progress 4'b1001: For yuv422 8bit interlace 4'b1010: For yuv420 8bit 4'b1011: For yuv420 8bit legacy Others: Reserved Note: raw14 will be rounded to raw12.
3	RW	0x0	sw_dma_en_id3 Enable dma transport id3. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_drop_frame_en_id3 1'b0: Disable drop id3 frame 1'b1: Enable drop id3 frame.
1	RW	0x0	sw_crop_en_id3 Enable to crop for id3. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_id3 Enable to capture id3. 1'b0: Disable 1'b1: Enable

VICAP_MIPI4_ID3_CTRL1

Address: Operational Base(0x27C10000) + offset (0x061C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_command_mode_en_id3 Select command mode for id3. 1'b0: Not command mode 1'b1: Command mode
13:12	RW	0x0	sw_on_hdr_line_cnt_id3 If sw_mipi0_on_hdr_mode_id3=1(2),the line count value will circulate between 0~1(2).And if sw_mipi0_on_hdr_line_cnt_id3=1, id3 channel will capture the line which line count value equal to 1.
11:10	RW	0x0	sw_on_hdr_mode_id3 2'b00: Normal mode(no HDR) 2'b01: 2 frames HDR 2'b10: 3 frames HDR 2'b11: Reserved
9:8	RW	0x0	sw_hdr_mode_id3 2'b00: HDR distinguished by virtual channel 2'b01: HDR distinguished by line number(ON HDR mode) 2'b10: HDR distinguished by first 4pixel(SONY HDR mode) 2'b11: Reserved
7:2	RW	0x00	sw_dt_id3 Data type for id3.

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	sw_vc_id3 Virtual channel for id3.

VICAP_MIPI4_CTRL

Address: Operational Base(0x27C10000) + offset (0x0620)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_debug_en 1'b0: Normal mode 1'b1: Debug mode.
30:22	RO	0x000	reserved
21:20	RW	0x0	sw_water_line 2'b00: 75% 2'b01: 50% 2'b10: 25% 2'b11: 0%
19:18	RW	0x0	sw_soft_rst_mode 2'b00: Soft reset and protect toisp path frame integrity; 2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically; 2'b10: Soft reset directly; 2'b11: Reserved.
17	RW	0x0	sw_soft_rst 1'b0: Not reset 1'b1: Reset the VICAP MIPI4 path(except MMU/AXI MASTER/REG FILE)
16	RW	0x0	sw_dma_rst Write 1 will reset VICAP MIPI4 path dma. When this bit change to 0,dma is reseted completely.
15:14	RW	0x0	sw_drop_frame_main_id The id that is the last coming in HDR mode.
13:12	RW	0x0	sw_drop_frame_m Receive m frames,and drop n frames.(m>0,n>0)
11:9	RW	0x0	sw_drop_frame_n Receive m frames,and drop n frames.(m>0,n>0)
8	RW	0x0	sw_drop_frame_en 1'b0: Disable drop all id frame 1'b1: Enable drop all id frame.
7	RO	0x0	reserved
6:5	RW	0x0	sw_vc_hdr_main_id The id that is the first coming. Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1.
4	RW	0x0	sw_vc_hdr_protect_en 1'b0: Not ensure hdr long exposure frame is captured firstly; 1'b1: Ensure hdr long exposure frame is captured firstly. Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id).
3:1	RO	0x0	reserved
0	RW	0x0	sw_cap_en 1'b0: Disable capture all id 1'b1: Enable capture all id.

VICAP_MIPI4_FRAME0_ADDR_Y_ID0

Address: Operational Base(0x27C10000) + offset (0x0624)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id0 First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI4_FRAME1_ADDR_Y_ID0

Address: Operational Base(0x27C10000) + offset (0x0628)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id0 First address of odd frame for ID0 Y path(must be aligned to double word).

VICAP_MIPI4_FRAME0_ADDR_UV_ID0

Address: Operational Base(0x27C10000) + offset (0x062C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id0 First address of even frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI4_FRAME1_ADDR_UV_ID0

Address: Operational Base(0x27C10000) + offset (0x0630)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI4_VLW_ID0

Address: Operational Base(0x27C10000) + offset (0x0634)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id0 Address force update for id0. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id0 Virtual line width of even frame for ID0 path(must be aligned to double word).

VICAP_MIPI4_FRAME0_ADDR_Y_ID1

Address: Operational Base(0x27C10000) + offset (0x0638)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id1 First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI4_FRAME1_ADDR_Y_ID1

Address: Operational Base(0x27C10000) + offset (0x063C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id1 First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI4_FRAME0_ADDR_UV_ID1

Address: Operational Base(0x27C10000) + offset (0x0640)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id1 First address of even frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI4_FRAME1_ADDR_UV_ID1

Address: Operational Base(0x27C10000) + offset (0x0644)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id1 First address of odd frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI4_VLW_ID1

Address: Operational Base(0x27C10000) + offset (0x0648)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_id1 Address force update for id1. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id1 Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI4_FRAME0_ADDR_Y_ID2

Address: Operational Base(0x27C10000) + offset (0x064C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id2 First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI4_FRAME1_ADDR_Y_ID2

Address: Operational Base(0x27C10000) + offset (0x0650)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id2 First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI4_FRAME0_ADDR_UV_ID2

Address: Operational Base(0x27C10000) + offset (0x0654)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id2 First address of even frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI4_FRAME1_ADDR_UV_ID2

Address: Operational Base(0x27C10000) + offset (0x0658)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI4_VLW_ID2

Address: Operational Base(0x27C10000) + offset (0x065C)

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Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id2 Address force update for id2. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id2 Virtual line width of even frame for ID2 path(must be aligned to double word).

VICAP_MIPI4_FRAME0_ADDR_Y_ID3

Address: Operational Base(0x27C10000) + offset (0x0660)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id3 First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI4_FRAME1_ADDR_Y_ID3

Address: Operational Base(0x27C10000) + offset (0x0664)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id3 First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI4_FRAME0_ADDR_UV_ID3

Address: Operational Base(0x27C10000) + offset (0x0668)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id3 First address of even frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI4_FRAME1_ADDR_UV_ID3

Address: Operational Base(0x27C10000) + offset (0x066C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id3 First address of odd frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI4_VLW_ID3

Address: Operational Base(0x27C10000) + offset (0x0670)

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	sw_addr_force_update_id3 Address force update for id3. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_id3 Virtual line width of even frame for ID3 path(must be aligned to double word).

VICAP_MIPI4_INTEN

Address: Operational Base(0x27C10000) + offset (0x0674)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	size_err_id3_inten 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
26	RW	0x0	size_err_id2_inten 1'b0: Disable 1'b1: Enable
25	RW	0x0	size_err_id1_inten 1'b0: Disable 1'b1: Enable
24	RW	0x0	size_err_id0_inten 1'b0: Disable 1'b1: Enable
23	RW	0x0	line_id3_inten 1'b0: Disable 1'b1: Enable
22	RW	0x0	line_id2_inten 1'b0: Disable 1'b1: Enable
21	RW	0x0	line_id1_inten 1'b0: Disable 1'b1: Enable
20	RW	0x0	line_id0_inten 1'b0: Disable 1'b1: Enable
19	RW	0x0	csi2rx_fifo_overflow_inten 1'b0: Disable 1'b1: Enable
18	RW	0x0	bandwidth_lack_inten 1'b0: Disable 1'b1: Enable
17	RW	0x0	dma_uv_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path. 1'b0: Disable 1'b1: Enable
16	RW	0x0	dma_y_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path. 1'b0: Disable 1'b1: Enable
15	RW	0x0	frame1_dma_end_id3_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
14	RW	0x0	frame0_dma_end_id3_inten Enable the interrupt of end of even frame for ID3. 1'b0: Disable 1'b1: Enable
13	RW	0x0	frame1_dma_end_id2_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
12	RW	0x0	frame0_dma_end_id2_inten Enable the interrupt of end of even frame for ID2. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
11	RW	0x0	frame1_dma_end_id1_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
10	RW	0x0	frame0_dma_end_id1_inten Enable the interrupt of end of even frame for ID1. 1'b0: Disable 1'b1: Enable
9	RW	0x0	frame1_dma_end_id0_inten Enable the interrupt of end of odd frame for ID0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	frame0_dma_end_id0_inten Enable the interrupt of end of even frame for ID0. 1'b0: Disable 1'b1: Enable
7	RW	0x0	frame_inf_end_id3_inten Enable the interrupt of interface frame end for ID3. 1'b0: Disable 1'b1: Enable
6	RW	0x0	frame_inf_end_id2_inten Enable the interrupt of interface frame end for ID2. 1'b0: Disable 1'b1: Enable
5	RW	0x0	frame_inf_end_id1_inten Enable the interrupt of interface frame end for ID1. 1'b0: Disable 1'b1: Enable
4	RW	0x0	frame_inf_end_id0_inten Enable the interrupt of interface frame end for ID0. 1'b0: Disable 1'b1: Enable
3	RW	0x0	frame_inf_start_id3_inten Enable the interrupt of interface frame start for ID3. 1'b0: Disable 1'b1: Enable
2	RW	0x0	frame_inf_start_id2_inten Enable the interrupt of interface frame start for ID2. 1'b0: Disable 1'b1: Enable
1	RW	0x0	frame_inf_start_id1_inten Enable the interrupt of interface frame start for ID1. 1'b0: Disable 1'b1: Enable
0	RW	0x0	frame_inf_start_id0_inten Enable the interrupt of interface frame start for ID0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI4_INTSTAT

Address: Operational Base(0x27C10000) + offset (0x0678)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27	W1C	0x0	size_err_id3_intst 1'b0: No interrupt 1'b1: Interrupt
26	W1C	0x0	size_err_id2_intst 1'b0: No interrupt 1'b1: Interrupt
25	W1C	0x0	size_err_id1_intst 1'b0: No interrupt 1'b1: Interrupt
24	W1C	0x0	size_err_id0_intst 1'b0: No interrupt 1'b1: Interrupt
23	W1C	0x0	line_id3_intst 1'b0: No interrupt 1'b1: Interrupt
22	W1C	0x0	line_id2_intst 1'b0: No interrupt 1'b1: Interrupt
21	W1C	0x0	line_id1_intst 1'b0: No interrupt 1'b1: Interrupt
20	W1C	0x0	line_id0_intst 1'b0: No interrupt 1'b1: Interrupt
19	W1C	0x0	csi2rx_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
18	W1C	0x0	bandwidth_lack_intst 1'b0: No interrupt 1'b1: Interrupt
17	W1C	0x0	dma_uv_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
16	W1C	0x0	dma_y_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
15	W1C	0x0	frame1_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
14	W1C	0x0	frame0_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
13	W1C	0x0	frame1_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
12	W1C	0x0	frame0_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
11	W1C	0x0	frame1_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
10	W1C	0x0	frame0_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
9	W1C	0x0	frame1_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
8	W1C	0x0	frame0_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
7	W1C	0x0	frame_inf_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
6	W1C	0x0	frame_inf_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
5	W1C	0x0	frame_inf_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	frame_inf_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	frame_inf_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	frame_inf_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	frame_inf_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	frame_inf_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt

VICAP_MIPI4_ON_PAD_VALUE

Address: Operational Base(0x27C10000) + offset (0x067C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_on_pad_value Padding value for ON sensor.

VICAP_MIPI4_ID0_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x0680)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id0 Effect code of id0 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id0 Effect code of id0 for sony sensor.

VICAP_MIPI4_ID1_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x0684)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id1 Effect code of id1 for sony sensor.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_sony_effect_code0_id1 Effect code of id1 for sony sensor.

VICAP_MIPI4_ID2_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x0688)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id2 Effect code of id2 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id2 Effect code of id2 for sony sensor.

VICAP_MIPI4_ID3_EFFECT_CODE

Address: Operational Base(0x27C10000) + offset (0x068C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_sony_effect_code1_id3 Effect code of id3 for sony sensor.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_sony_effect_code0_id3 Effect code of id3 for sony sensor.

VICAP_MIPI4_ID0_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0690)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id0 The start y coordinate for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id0 The start x coordinate for id0. The start x value must be 4 aligned.

VICAP_MIPI4_ID1_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0694)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id1 The start y coordinate for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id1 The start x coordinate for id1. The start x value must be 4 aligned.

VICAP_MIPI4_ID2_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0698)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id2 The start y coordinate for id2.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_start_x_id2 The start x coordinate for id2. The start x value must be 4 aligned.

VICAP_MIPI4_ID3_CROP_START

Address: Operational Base(0x27C10000) + offset (0x069C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id3 The start y coordinate for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id3 The start x coordinate for id3. The start x value must be 4 aligned.

VICAP_MIPI4_ID0_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x06A0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id0 Height for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id0 Width for id0. The width value must be 4 aligned.

VICAP_MIPI4_ID1_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x06A4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id1 Height for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id1 Width for id1. The width value must be 4 aligned.

VICAP_MIPI4_ID2_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x06A8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id2 Height for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id2 Width for id2. The width value must be 4 aligned.

VICAP_MIPI4_ID3_SET_SIZE

Address: Operational Base(0x27C10000) + offset (0x06AC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id3 Height for id3.

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Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id3 Width for id3. The width value must be 4 aligned.

VICAP_MIPI4_LINE_INT_NUM_ID0_1

Address: Operational Base(0x27C10000) + offset (0x06B0)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id1 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id1 For one-time mode,if line_int_num_id1=100,then channel 1 receive 100th line,the line_id1_intst will be 1. For circular mode ,if line_int_num_id1=100,then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1.
15	RW	0x0	line_int_mode_id0 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id0 For one-time mode,if line_int_num_id0=100,then channel 0 receive 100th line,the line_id0_intst will be 1. For circular mode ,if line_int_num_id0=100,then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1.

VICAP_MIPI4_LINE_INT_NUM_ID2_3

Address: Operational Base(0x27C10000) + offset (0x06B4)

Bit	Attr	Reset Value	Description
31	RW	0x0	line_int_mode_id3 1'b0: One-time mode 1'b1: Circular mode
30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id3 For one-time mode,if line_int_num_id3=100,then channel 3 receive 100th line,the line_id3_intst will be 1. For circular mode ,if line_int_num_id3=100,then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1.
15	RW	0x0	line_int_mode_id2 1'b0: One-time mode 1'b1: Circular mode
14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id2 For one-time mode,if line_int_num_id2=100,then channel 2 receive 100th line,the line_id2_intst will be 1. For circular mode ,if line_int_num_id2=100,then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1.

VICAP_MIPI4_LINE_CNT_ID0_1

Address: Operational Base(0x27C10000) + offset (0x06B8)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id1 Current line count for id1.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id0 Current line count for id0.

VICAP_MIPI4_LINE_CNT_ID2_3

Address: Operational Base(0x27C10000) + offset (0x06BC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_cnt_id3 Current line count for id3.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_line_cnt_id2 Current line count for id2.

VICAP_MIPI4_SIZE_NUM_ID0

Address: Operational Base(0x27C10000) + offset (0x06C0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id0 The id0 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id0 The id0 pixel number in one line.

VICAP_MIPI4_SIZE_NUM_ID1

Address: Operational Base(0x27C10000) + offset (0x06C4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id1 The id1 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id1 The id1 pixel number in one line.

VICAP_MIPI4_SIZE_NUM_ID2

Address: Operational Base(0x27C10000) + offset (0x06C8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id2 The id2 line number in one frame.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_pix_num_id2 The id2 pixel number in one line.

VICAP_MIPI4_SIZE_NUM_ID3

Address: Operational Base(0x27C10000) + offset (0x06CC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_line_num_id3 The id3 line number in one frame.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RO	0x0000	ro_pix_num_id3 The id3 pixel number in one line.

VICAP_MIPI4_FRAME_NUM_VC0

Address: Operational Base(0x27C10000) + offset (0x06D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc0 The frame number of frame end of virtual channel 0.
15:0	RO	0x0000	ro_frame_num_start_vc0 The frame number of frame start of virtual channel 0.

VICAP_MIPI4_FRAME_NUM_VC1

Address: Operational Base(0x27C10000) + offset (0x06D4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc1 The frame number of frame end of virtual channel 1.
15:0	RO	0x0000	ro_frame_num_start_vc1 The frame number of frame start of virtual channel 1.

VICAP_MIPI4_FRAME_NUM_VC2

Address: Operational Base(0x27C10000) + offset (0x06D8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc2 The frame number of frame end of virtual channel 2.
15:0	RO	0x0000	ro_frame_num_start_vc2 The frame number of frame start of virtual channel 2.

VICAP_MIPI4_FRAME_NUM_VC3

Address: Operational Base(0x27C10000) + offset (0x06DC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc3 The frame number of frame end of virtual channel 3.
15:0	RO	0x0000	ro_frame_num_start_vc3 The frame number of frame start of virtual channel 3.

VICAP_SCL_CH_CTRL

Address: Operational Base(0x27C10000) + offset (0x0700)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	sw_scl_dma_en_ch0 Enable dma transport scale channel0. 1'b0: Disable 1'b1: Enable
15:13	RO	0x0	reserved
12	RW	0x0	sw_scl_wrddr_type_ch0 1'b0: RAW-compacted 1'b1: RAW-uncompacted Note: This register is valid only when sw_scl_mode_ch0>2'b00.
11:10	RW	0x0	sw_scl_site_ch0 2'b00: Upper left corner in 2x2 pixel block 2'b01: Upper right corner in 2x2 pixel block 2'b10: Bottom left corner in 2x2 pixel block 2'b11: Bottom right corner in 2x2 pixel block Note: This register is valid only when sw_scl_mode_ch0=2'b10.

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	sw_scl_times_ch0 2'b00: 8 times scale 2'b01: 16 times scale 2'b10: 32 times scale 2'b11: Reserved Note: This register is valid only when sw_scl_mode_ch0=2'b00.
7:3	RW	0x00	sw_scl_mux_ch0 5'd0: Select MIPI0 ID0 5'd1: Select MIPI0 ID1 5'd2: Select MIPI0 ID2 5'd3: Select MIPI0 ID3 5'd4: Select MIPI1 ID0 5'd5: Select MIPI1 ID1 5'd6: Select MIPI1 ID2 5'd7: Select MIPI1 ID3 5'd8: Select MIPI2 ID0 5'd9: Select MIPI2 ID1 5'd10: Select MIPI2 ID2 5'd11: Select MIPI2 ID3 5'd12: Select MIPI3 ID0 5'd13: Select MIPI3 ID1 5'd14: Select MIPI3 ID2 5'd15: Select MIPI3 ID3 5'd16: Select MIPI4 ID0 5'd17: Select MIPI4 ID1 5'd18: Select MIPI4 ID2 5'd19: Select MIPI4 ID3 5'd24: Select DVP Others: Reserved
2:1	RW	0x0	sw_scl_mode_ch0 Scale mode for channel 0. 2'b00: Raw scale 2'b01: 2x2 binning 2'b10: 2x2 pixel extraction 2'b11: Reserved Others: Reserved
0	RW	0x0	sw_scl_en_ch0 Enable scale channel0. 1'b0: Disable 1'b1: Enable

VICAP_SCL_CTRL

Address: Operational Base(0x27C10000) + offset (0x0704)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:17	RW	0x0	sw_soft_rst_mode_ch0 2'b00: Soft reset and protect toisp path frame integrity; 2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically; 2'b10: Soft reset directly; 2'b11: Reserved.
16	RW	0x0	sw_soft_rst_ch0 Write 1 will reset VICAP SCALE channel 0 path. When this bit change to 0,scale is reseted completely.
15:3	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
2:1	RW	0x0	sw_water_line 2'b00: 75% 2'b01: 50% 2'b10: 25% 2'b11: 0%
0	RO	0x0	reserved

VICAP_SCL_FRAME0_ADDR_CH0

Address: Operational Base(0x27C10000) + offset (0x0708)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_ch0 First address of even frame for CH0 path(must be aligned to double word).

VICAP_SCL_FRAME1_ADDR_CH0

Address: Operational Base(0x27C10000) + offset (0x070C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_ch0 First address of odd frame for CH0 path(must be aligned to double word).

VICAP_SCL_VLW_CH0

Address: Operational Base(0x27C10000) + offset (0x0710)

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	sw_addr_force_update_ch0 Address force update for ch0. Self clear.
30:20	RO	0x000	reserved
19:0	RW	0x00000	sw_vlw_ch0 Virtual line width of even frame for CH0 path(must be aligned to double word).

VICAP_SCL_CH0_BLACK_LEVEL

Address: Operational Base(0x27C10000) + offset (0x0738)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_scl_ch0_black_11 The black level for scale channel0 bayer pattern 11 position.
23:16	RW	0x00	sw_scl_ch0_black_10 The black level for scale channel0 bayer pattern 10 position.
15:8	RW	0x00	sw_scl_ch0_black_01 The black level for scale channel0 bayer pattern 01 position.
7:0	RW	0x00	sw_scl_ch0_black_00 The black level for scale channel0 bayer pattern 00 position.

VICAP_TOISP0_CH_CTRL

Address: Operational Base(0x27C10000) + offset (0x0780)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	sw_toisp0_en Enable toisp0. 1'b0: Disable 1'b1: Enable
27:24	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
23:19	RW	0x00	sw_toisp0_mux_ch2 5'd0: Select MIPI0 ID0 5'd1: Select MIPI0 ID1 5'd2: Select MIPI0 ID2 5'd3: Select MIPI0 ID3 5'd4: Select MIPI1 ID0 5'd5: Select MIPI1 ID1 5'd6: Select MIPI1 ID2 5'd7: Select MIPI1 ID3 5'd8: Select MIPI2 ID0 5'd9: Select MIPI2 ID1 5'd10: Select MIPI2 ID2 5'd11: Select MIPI2 ID3 5'd12: Select MIPI3 ID0 5'd13: Select MIPI3 ID1 5'd14: Select MIPI3 ID2 5'd15: Select MIPI3 ID3 5'd16: Select MIPI4 ID0 5'd17: Select MIPI4 ID1 5'd18: Select MIPI4 ID2 5'd19: Select MIPI4 ID3 Others: Reserved
18:17	RO	0x0	reserved
16	RW	0x0	sw_toisp0_en_ch2 Enable toisp0 channel2. 1'b0: Disable 1'b1: Enable
15:11	RW	0x00	sw_toisp0_mux_ch1 5'd0: Select MIPI0 ID0 5'd1: Select MIPI0 ID1 5'd2: Select MIPI0 ID2 5'd3: Select MIPI0 ID3 5'd4: Select MIPI1 ID0 5'd5: Select MIPI1 ID1 5'd6: Select MIPI1 ID2 5'd7: Select MIPI1 ID3 5'd8: Select MIPI2 ID0 5'd9: Select MIPI2 ID1 5'd10: Select MIPI2 ID2 5'd11: Select MIPI2 ID3 5'd12: Select MIPI3 ID0 5'd13: Select MIPI3 ID1 5'd14: Select MIPI3 ID2 5'd15: Select MIPI3 ID3 5'd16: Select MIPI4 ID0 5'd17: Select MIPI4 ID1 5'd18: Select MIPI4 ID2 5'd19: Select MIPI4 ID3 Others: Reserved
10:9	RO	0x0	reserved
8	RW	0x0	sw_toisp0_en_ch1 Enable toisp0 channel1. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
7:3	RW	0x00	sw_toisp0_mux_ch0 5'd0: Select MIPI0 ID0 5'd1: Select MIPI0 ID1 5'd2: Select MIPI0 ID2 5'd3: Select MIPI0 ID3 5'd4: Select MIPI1 ID0 5'd5: Select MIPI1 ID1 5'd6: Select MIPI1 ID2 5'd7: Select MIPI1 ID3 5'd8: Select MIPI2 ID0 5'd9: Select MIPI2 ID1 5'd10: Select MIPI2 ID2 5'd11: Select MIPI2 ID3 5'd12: Select MIPI3 ID0 5'd13: Select MIPI3 ID1 5'd14: Select MIPI3 ID2 5'd15: Select MIPI3 ID3 5'd16: Select MIPI4 ID0 5'd17: Select MIPI4 ID1 5'd18: Select MIPI4 ID2 5'd19: Select MIPI4 ID3 5'd24: Select DVP 5'd29: Select SCL Others: Reserved
2:1	RO	0x0	reserved
0	RW	0x0	sw_toisp0_en_ch0 Enable toisp0 channel0. 1'b0: Disable 1'b1: Enable

VICAP_TOISP0_CROP_SIZE

Address: Operational Base(0x27C10000) + offset (0x0784)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height The expected height of received image.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width The expected width of received image.

VICAP_TOISP0_CROP_START

Address: Operational Base(0x27C10000) + offset (0x0788)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y The vertical ordinate of the start point.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x The horizontal ordinate of the start point.

VICAP_SPACE_DDR_FREQ

Address: Operational Base(0x27C10000) + offset (0x07F4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24	RO	0x0	ro_space_ddr_freq_less_buffer 1'b0: Space for ddr frequency conversion is more than the buffer depth 1'b1: Space for ddr frequency conversion is less than the buffer depth
23:18	RO	0x00	reserved
17:0	RO	0x00000	ro_space_ddr_freq Space for ddr frequency conversion.

VICAP_VBLANK_LIMIT_CYCLE_NUM

Address: Operational Base(0x27C10000) + offset (0x07F8)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	sw_sensor_sel 3'b000: DVP 3'b001: MIPI0 3'b010: MIPI1 3'b011: MIPI2 3'b100: MIPI3 3'b101: MIPI4 others: Reserve
27:0	RO	0x0000000	ro_vblank_limit_cycle_num Dclk cycle number for vblank limit.

VICAP_DDR_FREQ_CYCLE_NUM

Address: Operational Base(0x27C10000) + offset (0x07FC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_ddr_freq_cycle_num Dclk cycle number for ddr frequency conversion.

VICAP_MMU0_DTE_ADDR

Address: Operational Base(0x27C10000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr MMU current page table address.

VICAP_MMU0_STATUS

Address: Operational Base(0x27C10000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RW	0x00	page_fault_bus_id Index of master reponsible for last page fault.
5	RW	0x0	page_fault_is_write The direction of access for last page fault: 1'b0: Read 1'b1: Write
4	RW	0x0	replay_buffer_empty The MMU replay buffer is empty.
3	RW	0x0	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RW	0x0	stail_active MMU stall mode currently enabled. The mode is enabled by command.

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Bit	Attr	Reset Value	Description
1	RW	0x0	page_fault_active MMU page fault mode currently enabled . The mode is enabled by command.
0	RW	0x0	paging_enabled Paging is enabled.

VICAP_MMU0_COMMAND

Address: Operational Base(0x27C10000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	mmu_cmd MMU_CMD. This can be: 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE

VICAP_MMU0_PAGE_FAULT_ADDR

Address: Operational Base(0x27C10000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	page_fault_addr Address of last page fault.

VICAP_MMU0_ZAP_ONE_LINE

Address: Operational Base(0x27C10000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zap_one_line Address to be invalidated from the page table cache.

VICAP_MMU0_INT_RAWSTAT

Address: Operational Base(0x27C10000) + offset (0x0814)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error.
0	RW	0x0	page_fault Page fault.

VICAP_MMU0_INT_CLEAR

Address: Operational Base(0x27C10000) + offset (0x0818)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error.
0	RW	0x0	page_fault Page fault.

VICAP_MMU0_INT_MASK

Address: Operational Base(0x27C10000) + offset (0x081C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error

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Bit	Attr	Reset Value	Description
0	RW	0x0	page_fault Page fault

VICAP_MMU0_INT_STATUS

Address: Operational Base(0x27C10000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error.
0	RW	0x0	page_fault Page fault.

VICAP_MMU0_AUTO_GATING

Address: Operational Base(0x27C10000) + offset (0x0824)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mmu_auto_gating When it is 1'b1, the mmu will auto gating it self

6.6 Interface Description

Table 6-2 VICAP Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
vicap_clkout	O	VI_CIF_CLKO/ETH1_PPSCLK_M0/ETH0_RXCTL_M1/SAI3_SDO_M2/SPDIF_RX1_M1/UART3_CTSN_M0/SPI3_MISO_M0/CAN1_TX_M3/MIPI_TE_M1/GPIO3_A2_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[11:8]==4'h1
vicap_clkin	I	VI_CIF_CLKI/ETH1_PTP_REFCLK_M0/ETH0_RXD1_M1/SAI3_SDI_M2/SPDIF_TX1_M1/UART3_RTSN_M0/SPI3_CSN0_M0/CAN1_RX_M3/GPIO3_A3_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[15:12]==4'h1
vicap_href	I	VI_CIF_HREF/ETH0_MDIO_M1/SAI3_SCLK_M2/UART3_TX_M0/SPI3_CLK_M0/I2C7_SCL_M1/GPIO3_A0_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[3:0]==4'h1
vicap_vsync	I	VI_CIF_VSYNC/ETH1_PPSTRIG_M0/ETH0_MDC_M1/SAI3_LRCK_M2/UART3_RX_M0/SPI3_MOSI_M0/I2C7_SDA_M1/GPIO3_A1_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[7:4]==4'h1
vicap_data0	I	VI_CIF_D0/ETH1_TXCLK_M0/SAI2_SDI_M1/PDM1_CLK0_M0/UART11_RX_M1/SPI1_CLK_M1/PWM1_CH4_M2/GPIO2_C5_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[7:4]==4'h1
vicap_data1	I	VI_CIF_D1/ETH1_TXD3_M0/SAI2_SDO_M1/PDM1_SDI0_M0/UART11_TX_M1/SPI1_CSN0_M1/PWM1_CH3_M2/GPIO2_C4_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[3:0]==4'h1
vicap_data2	I	VI_CIF_D2/ETH1_TXD2_M0/SAI2_LRCK_M1/PDM1_SDI3_M0/UART11_RTSN_M1/SPI1_MISO_M1/PWM0_CH0_M2/GPIO2_C3_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[15:12]==4'h1
vicap_data3	I	VI_CIF_D3/ETH1_RXCLK_M0/ETH0_PPSTRIG_M1/SAI2_SCLK_M1/PDM1_SDI2_M0/UART11_CTSN_M1/SPI1_MOSI_M1/PWM1_CH2_M2/GPIO2_C2_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[11:8]==4'h1
vicap_data4	I	VI_CIF_D4/ETH1_RXD3_M0/ETH0_PPSCLK_M1/SAI2_MCLK_M1/PDM1_CLK1_M0/UART9_TX_M0/SPI1_CSN1_M1/PWM1_CH1_M2/GPIO2_C1_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[7:4]==4'h1
vicap_data5	I	VI_CIF_D5/ETH1_RXD2_M0/ETH0_PTP_REFCLK_M1/PDM1_SDI1_M0/UART9_RX_M0/PWM1_CH0_M2/GPIO2_C0_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[3:0]==4'h1
vicap_data6	I	VI_CIF_D6/ETH0_RXD2_M1/SAI0_LRCK_M0/UART7_RX_M0/UART8_CTSN_M1/I2C8_SDA_M2/GPIO2_B7_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[15:12]==4'h1
vicap_data7	I	VI_CIF_D7/ETH1_PTP_REFCLK_M1/ETH0_RXD3_M1/SAI0_SCLK_M0/UART7_TX_M0/UART8_RTSN_M1/I2C8_SCL_M2/GPIO2_B6_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[11:8]==4'h1
vicap_data8	I	VI_CIF_D8/SDMMC1_DETN_M1/ETH0_RXCLK_M1/S	TOP_IOC_GPIO2B_IOMUX_

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Module Pin	Dir	Pad Name	IOMUX Setting
		AI0_MCLK_M0/PDM0_CLK0_M3/UART7_RTSN_M0/SPI4_MISO_M3/SATA1_ACTLED_M0/GPIO2_B5_d	SEL_H[7:4]==4'h1
vicap_data9	I	VI_CIF_D9/SDMMC1_PWREN_M1/ETH0_TXD2_M1/SAI0_SDI3_M0/PDM0_SDI0_M3/UART7_CTSN_M0/SPI4_MOSI_M3/SATA0_ACTLED_M0/GPIO2_B4_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[3:0]==4'h1
vicap_data10	I	VI_CIF_D10/SDMMC1_CLK_M1/ETH0_TXCLK_M1/SAI0_SDO2_M0/PDM0_CLK1_M3/UART1_RTSN_M1/SPI4_CLK_M3/PCIE1_CLKREQN_M0/GPIO2_B3_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[15:12]==4'h1
vicap_data11	I	VI_CIF_D11/SDMMC1_CMD_M1/ETH0_TXD3_M1/SAI0_SDI2_M0/PDM0_SDI1_M3/UART1_CTSN_M1/SPI4_CSN0_M3/PCIE0_CLKREQN_M0/GPIO2_B2_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[11:8]==4'h1
vicap_data12	I	VI_CIF_D12/SDMMC1_D3_M1/ETH0_TXD0_M1/SAI0_SDI1_M0/PDM0_SDI2_M3/UART1_RX_M1/GPIO2_B1_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[7:4]==4'h1
vicap_data13	I	VI_CIF_D13/SDMMC1_D2_M1/ETH0_TXD1_M1/SAI0_SDI0_M0/PDM0_SDI3_M3/UART1_TX_M1/GPIO2_B0_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[3:0]==4'h1
vicap_data14	I	VI_CIF_D14/SDMMC1_D1_M1/ETH0_TXCTL_M1/SAI0_SDO1_M0/UART8_RX_M1/I2C4_SDA_M2/GPIO2_A7_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[15:12]==4'h1
vicap_data15	I	VI_CIF_D15/SDMMC1_D0_M1/ETH0_RXD0_M1/SAI0_SDO0_M0/UART8_TX_M1/SPI4_CSN1_M3/I2C4_SCL_M2/GPIO2_A6_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[11:8]==4'h1

Notes: I=input, O=output, I/O=input/output, bidirectional

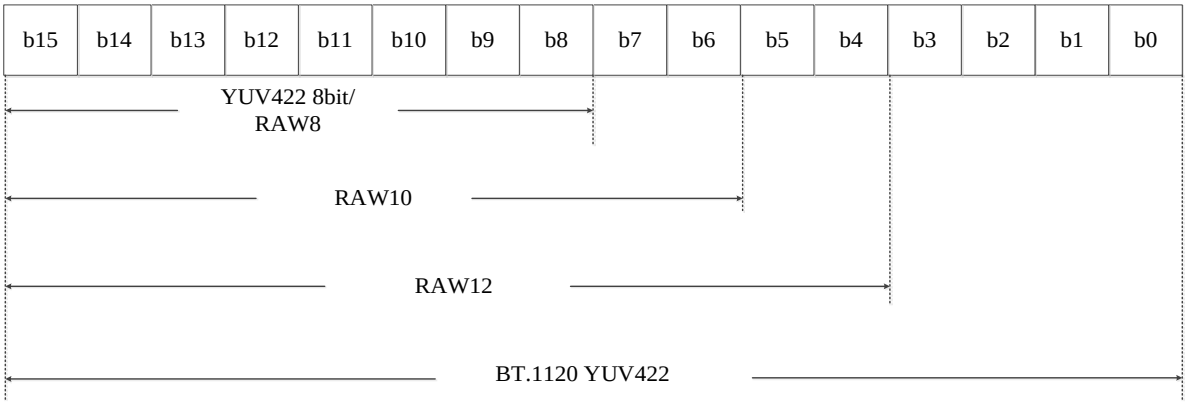
Furthermore, different IOs are selected and connected to different flash interface, which is shown as follows.

6.7 Application Notes

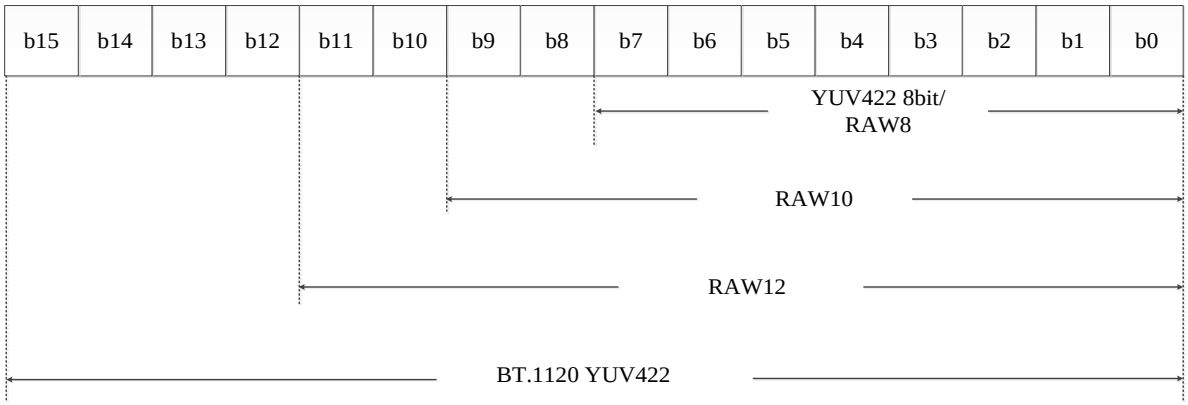
6.7.1 DVP Interface

- The MSB 4 bits of SAV/EAV of BT.656/BT.1120 are configurable, and the default values of SAV/EAV abide by the agreement.
- User can read the register of ro_sync_header_0~ro_sync_header_7 to obtain the recent 8 SAV/EAV.
- The register sw_yuyv_in_order should be configured correctly. In the BT.1120 case 2'h0/2'h2 are the same for UV sequence and 2'h1/2'h3 are the same for VU sequence.
- In the dual-edge sampling case, the VCCIO_IOC_MISC_CON1[9] must be set to 1, and the register sw_dualedge_en must be set to 1. The clock phase could be adjusted by setting the VCCIO_IOC_MISC_CON1[6:0].
- User could invert the DVP interface clk by the register VCCIO_IOC_MISC_CON1[8].
- The default data arrangement is high alignment, and user could change to low alignment by the register sw_low_align_en.

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high alignment



low alignment

6.7.2 MIPI Interface

- The register sw_crop_en is suggested to be set to 1. The register sw_width/sw_start_x should be aligned to 4.
- In the sony identification code hdr mode, the register sw_sony_effect_code0/1 should be configured correctly according to the camera manual.
- In the line counter hdr mode, the register sw_on_pad_value should be configured correctly according to the camera manual.
- In the VC hdr mode, the register sw_vc_hdr_protect is suggested to be set to 1, and the register sw_vc_hdr_id_main should be configured as the first coming id that is the long exposure frame id.
- The register sw_cap_en_idx is recommended for static configuration, and the register sw_cap_en is recommended for dynamic configuration.
- The MIPI interface can receive DSI data, but there are following restrictions on DSI TX: (1) one row of data could not be split into multiple long packets; (2) multiple packets could not be concatenated within a single HS transmission.

6.7.3 UV Mean Down Sampling

- Only ID0 support UV mean down sampling for all interfaces.
- The register sw_uvds_en is valid only when the register sw_wrddr_type=0x5.
- Support 4K(DVP)+4K(MIPI0)+4K(MIPI1/MIPI2)+4K(MIPI3/MIPI4) or 4K(DVP)+4K(MIPI0)+2K(MIPI1)+2K(MIPI2)+2K(MIPI3)+2K(MIPI4)
- UV mean down sampling for DVP interface and scale down function(raw scale/binning) are mutually exclusive.

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6.7.4 Scale down

- 2x2 raw binning function could convert the 4 cell pattern to normal bayer pattern. And the resolution is a quarter of what it was before.
- 2x2 pixel extraction function could extract one pixel from 2x2 bayer pattern. User needs to configure sw_scl_site correctly.
- The register sw_scl_chx_black_00/01/10/11 is the black level value for bayer pattern 00/01/10/11 position.
- The bit width of scale down output data is 16. When the max bit width of the scale down output data exceed 16, output data will be clipped. For example, 8 times scale down for RAW12, the bit width is 18, then the result will be clipped to 16 bits.
- When the width is not a multiple of double scale down times,then the result will be rounded up to an integer. For example, the image width is 4656 and 32 times scaling down is performed, the result width equals to ceil(4656/64)*2.
- When the height is not a multiple of double scale down times, then the result will be rounded down to an integer. For example, the image height is 1080 and 8 times scaling down is performed, the result height equals to floor(1080/16)*2.
- The registers sw_scl_en/sw_scl_mode/sw_scl_mux/sw_scl_times/sw_scl_site could be changed in the middle of the frame.

6.7.5 TOISP

- The register sw_width/sw_start_x should be aligned to 4.
- Only channel 0 need be enabled for linear case.
- Channel 0/1 need be enabled for HDR2 case, and channel 0 must be short exposure frame.
- Channel 0/1/2 need be enabled for HDR3 case, and channel 0 must be short exposure frame, channel 1 must be medium exposure frame, channel 2 must be long exposure frame.
- The register sw_toisp0_en_chx could be switched in the middle of the frame.

6.7.6 DMA

- The start address/virtual stride should be aligned to 8 at least. And being aligned to 64 is good for DDR.
- User could shut down DMA transferring by setting the register sw_dma_en to 0.
- User could set sw_hurry_en/sw_press_en to 1 for dynamic adjusting the priority of VICAP. And the register sw_water_line is the triggering condition of pulling up hurry/press signal.
- The register sw_yuyv_out_order is effective when the register sw_wrddr_type is NV16/NV12/YUYV. And in the NV16/NV12 case, 2'h0/2'h2 are the same for UV sequence and 2'h1/2'h3 are the same for VU sequence.
- There are two modes for line counter interrupt.In one-time mode, if line_int_num =100, the line_intst will be 1 when receive 100th line. In circular mode, if line_int_num =100, the line_intst will be 1 when receive 100th line200th line300th line.....
- The DMA has two transfer strategies :1. transfer image according to the actual height of reception. 2. transfer image according to the configured height. Which strategy you choose depends the register sw_dma_adapt_en.
- If DPHY1 work in the 2x2lane mode, the register sw_dphy1_2x2lane_en must be configured to 1.
- If DPHY2 work in the 2x2lane mode, the register sw_dphy2_2x2lane_en must be configured to 1.
- The following table lists the write ddr types supported for each MIPI parse type.

parse_type wrddr_type	RAW-compact	RAW-uncompact	YUV packet	YUV400	NV16	NV12
RAW8	***Y***	***Y***	**--**	**--**	**--**	**--**

RAW10	***Y***	***Y***	***--***	***--***	***--***	***--***
RAW12	***Y***	***Y***	***--***	***--***	***--***	***--***
RAW14	***Y***	***Y***	***--***	***--***	***--***	***--***
RAW16	***Y***	***Y***	***--***	***--***	***--***	***--***
RGB888	***Y***	***--***	***--***	***--***	***--***	***--***
YUV422-8bit progress	***--***	***--***	***Y***	***Y***	***Y***	***Y***
YUV422-8bit interlace	***--***	***--***	***Y***	***Y***	***Y***	***Y***
YUV420-8bit	***--***	***--***	***--***	***Y***	***--***	***Y***
YUV420-8bit leagcy	***--***	***--***	***--***	***Y***	***--***	***Y***

- The following table lists the write ddr types supported for each DVP input mode.

input_mode wrddr_type	RAW-compact	RAW-uncompact	YUV packet	YUV400	NV16	NV12
BT.601 YUV422	***--***	***--***	***Y***	***Y***	***Y***	***Y***
BT.601 RAW	***Y***	***Y***	***--***	***--***	***--***	***--***
BT.656 YUV422	***--***	***--***	***Y***	***Y***	***Y***	***Y***
BT.1120 YUV422	***--***	***--***	***Y***	***Y***	***Y***	***Y***
SONY DVP RAW	***Y***	***Y***	***--***	***--***	***--***	***--***

6.7.7 Reset

- DMA will be auto-reset when DMA goes wrong, for example FIFO overflow. And DMA will transfer data from the next frame.
- DMA also could be soft-reset by the register sw_dma_rst.
- User could reset the entire data path (interface/dma) by setting the register sw_soft_rst to 1. And the scale/toisp module will be reset if the sw_scl_mux/sw_toisp_mux is setted to choose the path.

6.7.8 DDR Frequency Interrupt

- User needs to config the register sw_ddr_freq_cycle_num, which is dclk cycle number for ddr frequency conversion.
- User needs to config the register sw_xxx_vblank_en/sw_xxx_buffer_en to 1, if the xxx interface is working.(‘xxx’ represent DVP/MIPI0/MIPI1/MIPI2/MIPI3/MIPI4)

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6.7.9 Debug Mode

- All interfaces support debug mode. Users can configure the register sw_debug_en to make the corresponding module enter debug mode. And the CSI2HOST also need enter debug mode, if the module is MIPI.
- The register sw_dma_adapt_en must be configured to 0.
- The path ID0 is used for debug mode.
- The register sw_dualedge_en/sw_input_mode must be configured correctly in DVP debug mode.
- The register sw_wrddr_type must be configured to 0 in debug mode.
- The space of a frame is equal to sw_vlw*sw_height, so the register sw_vlw/sw_height needs to be configured.
- In DVP debug mode, one debug data occupies 16 bits, the data arrangement is shown in the figure below.

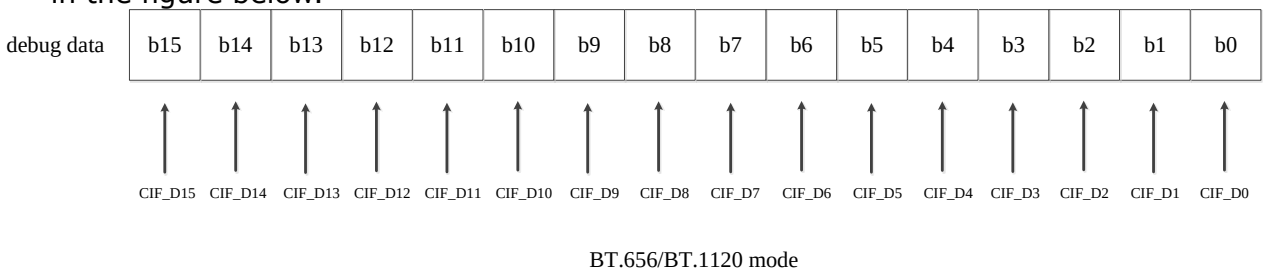


Fig. 6-25 DVP debug mode data arrangement

- In MIPI1/MIPI2/MIPI3/MIPI4 debug mode, one debug data occupies 48 bits, the data arrangement is shown in the figure below.

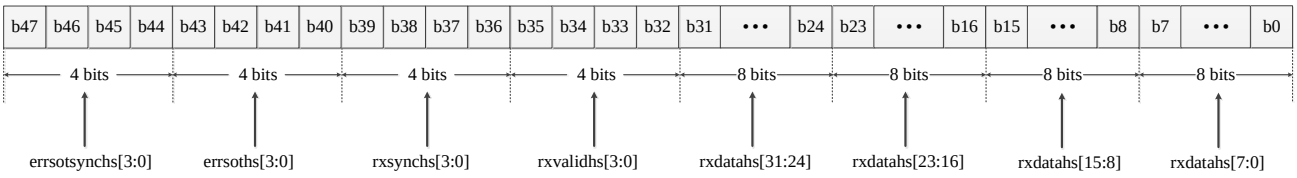


Fig. 6-26 MIPI1/2/3/4 debug mode data arrangement

- In MIPI0 debug mode, one debug data occupies 96 bits, the data arrangement is shown in the figure below.

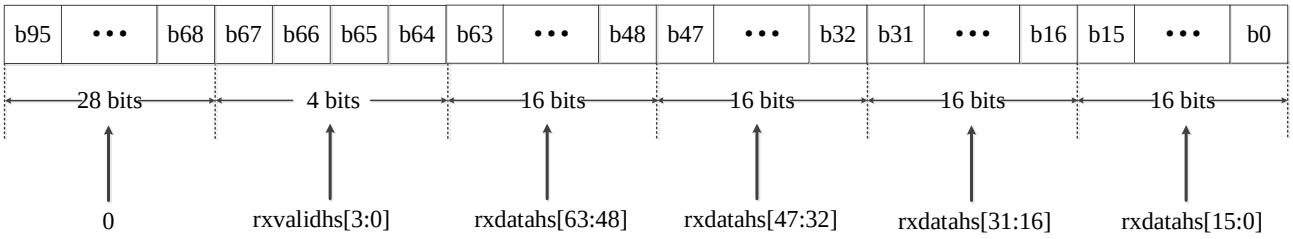


Fig. 6-27 MIPI0 debug mode data arrangement

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Chapter 7 Dynamic Memory Interface (DMC)

7.1 Overview

The DMC includes LPDDR4/4X/5 controller (DDRCTL), DDRPHY, DDR monitor and DFI scramble, which are a complete memory interface solution for DDR memory subsystems. The DDRCTL SoC application bus interface supports AXI interface, with flexible address mapper logic allow application-specific mapping of row, column, bank, bank group and rank bits to achieve industry leading high-efficiency, low-latency and high-performance from memory interface.
The DDRPHY provides control features to ease the customer implementation of digitally controlled features of the PHY such as DQS clean, read training, write training, dvfs training, periodic training and programmable configuration controls.
The DMC supports the following features:

- Support LPDDR4/4X/5
- Support LPDDR4 protocol up to LPDDR4-4266 speed grade and LPDDR5 protocol up to LPDDR5-4800
- Support up to 2-channel interleaving with a maximum of 16GB capacity in total, 2 ranks for each channel
- Support scalable and software-controlled 1:2:2(LPDDR4/4X) or 1:1:2/1:1:4 (LPDDR5) frequency ratio
- Support 5 AXI ports which communicate between the SoC interconnect and DDRCTL
- Support 32-bit DDR data bus width for 2-channel interleaving
- Support up to 10 kinds of address mapping
- Support burst16 for LPDDR4/4X/5
- Support different CL/WL latency
- Support 16 bank mode and BG mode for LPDDR5
- Support open, close, intelligent pre-charge paging policy
- Support advance refresh control
- Support LPDDR4/4X/5 software controlled frequency change
- Support DFI PHY master interface
- Support MC-initiated requests and PHY-initiated requests interface
- Support DFI data low power and ctrl low power interface
- Support auto power-down or auto self-refresh power down when DDRCTL is idle for a period of time. The DDRCTL's core clock, DDRCTL's AXI clock and interconnect's AXI clock can be gated
- Support auto or SW issue entry or exit clock stop/power-down/self-refresh/deep sleep mode
- Software programmable Quality-of-Service (QoS) support
  - Three traffic classes on read commands—high priority reads, variable priority reads, and low priority reads
  - Two traffic classes on write commands—normal priority writes and variable priority writes
  - Port urgent and port throttling control
- Dynamic scheduling inside DDRCTL to optimize bandwidth and latency
- Support PMU controlled DDRPHY entry or exit IO retention mode
- Support scrambling and descrambling of data written to or read from DDR SDRAM
- Support DDR monitor for following features
  - AMBA 32-bit APB slave interface
  - Each DDR channel embedded with one DDR monitor module
  - Support to monitor DDR read or write address within 8GB address range for each channel
  - Support to observe whether DDR access address within a specified range
  - Support to do the following statistics during a programmed number of time through hardware mode or software mode
    - Statistics about DDR idle cycles
    - Statistics about SR/PD/CKSTOP/SRPD/DFI data low power/DFI ctrl low power

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for LPDDR4/4X
- Statistics about SR/PD/CKSTOP/SRPD/DFIDLP/DFICLP/DSM for LPDDR5
- Statistics about number of activate, read and write cycles for a designated rank or bank
- Statistics about number of activate, read and write cycles for all banks and ranks in one DDR channel
- Statistics about read to read, read to write, write to write and write to read page hit or page miss for a designated rank or bank

- Support monitor interrupt

7.2 Block Diagram

Following is the 2-channel interleaving DMC block diagram. The two DDR channels are the same.

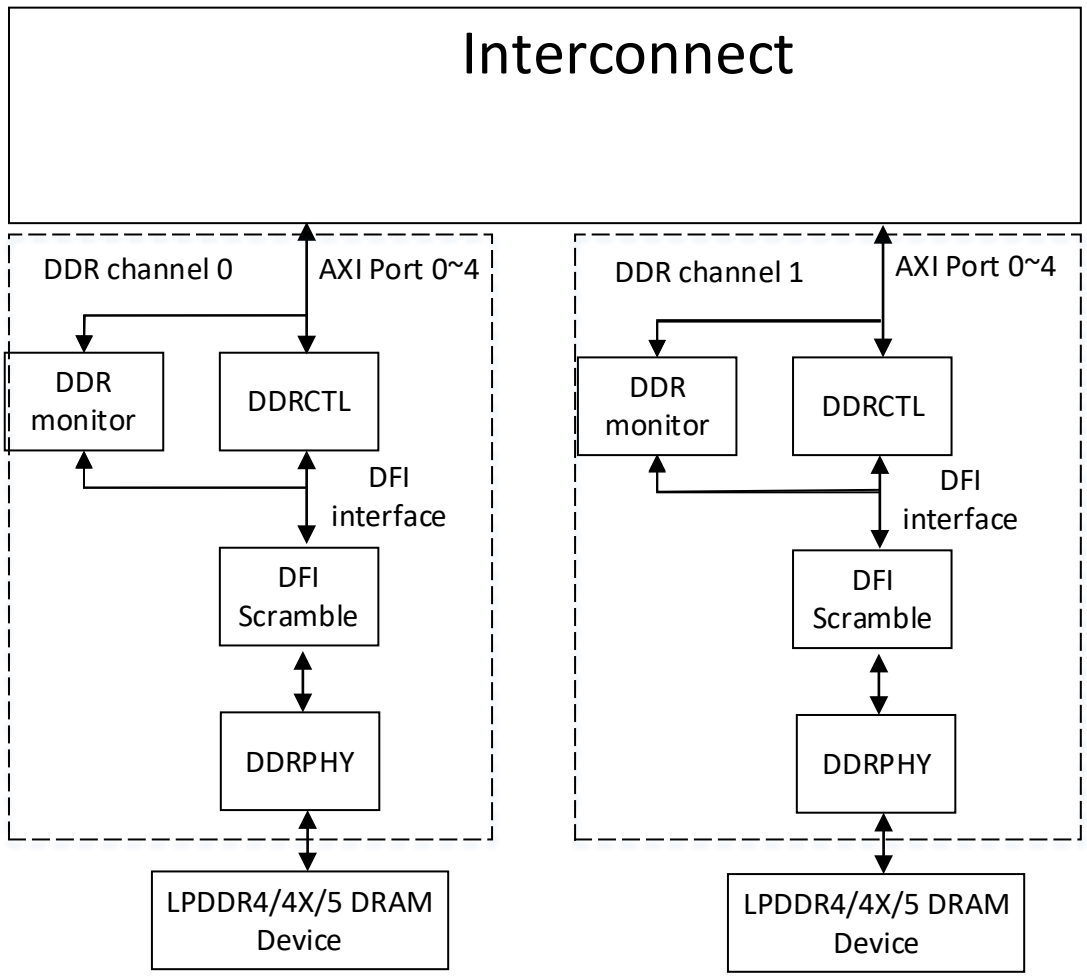


Fig. 7-1 DMC Block Diagram

Please refer to the other chapter for more information about interconnect.

7.3 Function Description

7.3.1 DDRCTL

DDRCTL supports 5 AXI Ports, it receives AXI transactions from interconnect directly. These transactions are queued internally and scheduled to the SDRAM while satisfying SDRAM protocol timing requirements. It in turn receives read data on the DFI interface from the DDRPHY block.

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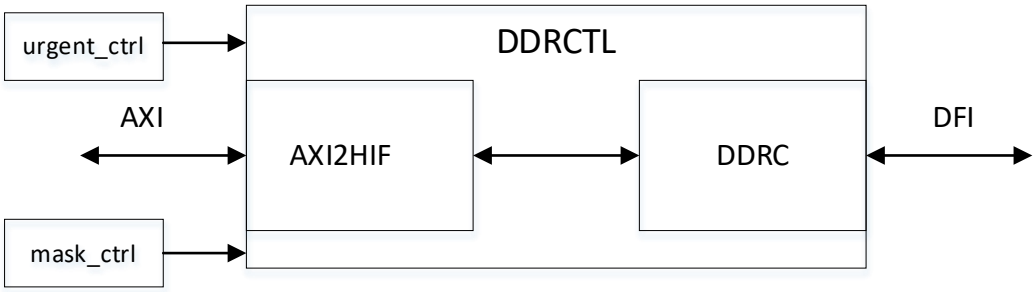


Fig. 7-2 DDRCTL Block Diagram

DDRCTL contains the following main components.

- AXI2HIF block: This block provides the AXI interfaces to system level and HIF interface to DDRC block. It provides bus protocol handling, data buffering, data bus size conversion and memory burst alignment. Read is stored in a read re-order buffer and return to the AXI Port.
- DDRC block: This block issues the read/write commands, carries out the DRAM page management, issues DRAM maintenance commands, and implement the DFI interface. Write data is stored in an SRAM until its associated command is issued to the PHY. Read data is handled by the response engine in the DDRC and is returned on the HIF.

To improve DDR performance in different scenarios, there are two modules named urgent_ctrl module and mask_ctrl module outside the DDRCTL.

7.3.1.1 urgent_ctrl

The function of urgent_ctrl module is to control the DDRCTL's awurgent_n/arurgent_n(n=0~4) per port according to the press_n or awqos_n/arqos_n(n=0~4) signals from interconnect module, as well as status signals such as raq_pop_n/waq_pop_n(n=0~4) from DDRCTL.

For a given AXI port, there is an embedded queue for each port inside urgent_ctrl module to store arqos or awqos respectively. The queue depth is 12. The arqos or awqos queue becomes urgent if there are commands in the queue and not popped for DDR_GRF_CHA/B_CON16.press_queue_wait_limit*4 cycles. The arqos_out and awqos_out is popped at the same time as DDRCTL internal AR FIFO and AW FIFO. The value of arqos_out, awqos_out and press signals are compared to select the maximum one as the QoS of a given AXI port. Then a port priority comparison module compares the QoS of 5 AXI ports and selects the port which has the largest QoS.

The arurgent is generated based on the following conditions.

- The port is selected by port priority comparison module.
- The arqos queue becomes urgent, arqos_out is largest of awqos_out, press and DDR_GRF_CHA/B_CON14.press_ar_th. If not, press should be larger than DDR_GRF_CHA/B_CON14.press_ar_th when arvalid is high and arready is low.
- When write is blocked by read (the awqos queue becomes urgent inside urgent_ctrl module but read port is granted by PA(Port Arbiter) inside DDRCTL and DDR_GRF_CHA/B_CON16.press_rdwr_order is set 1'b1).

The awurgent is generated based on the following conditions.

- The port is selected by port priority comparison module.
- The awqos queue becomes urgent, awqos_out is largest of arqos_out, press and DDR_GRF_CHA/B_CON14.press_aw_th. If not, press should be larger than DDR_GRF_CHA/B_CON14.press_aw_th when awvalid is high and awready is low.
- When read is blocked by write (the arqos queue becomes urgent inside urgent_ctrl module but write port is granted by PA inside DDRCTL and DDR_GRF_CHA/B_CON16.press_rdwr_order is set 1'b1).

7.3.1.2 mask_ctrl

This module is instantiated outside each DDRCTL to control the arurgent_0/arurgent_1/ arurgent_2, awurgent_0/awurgent_1/ awurgent_2 of DDRCTL. It also generates signals to mask read port and write port of PA to be not granted. Following is the block diagram of mask_ctrl module.

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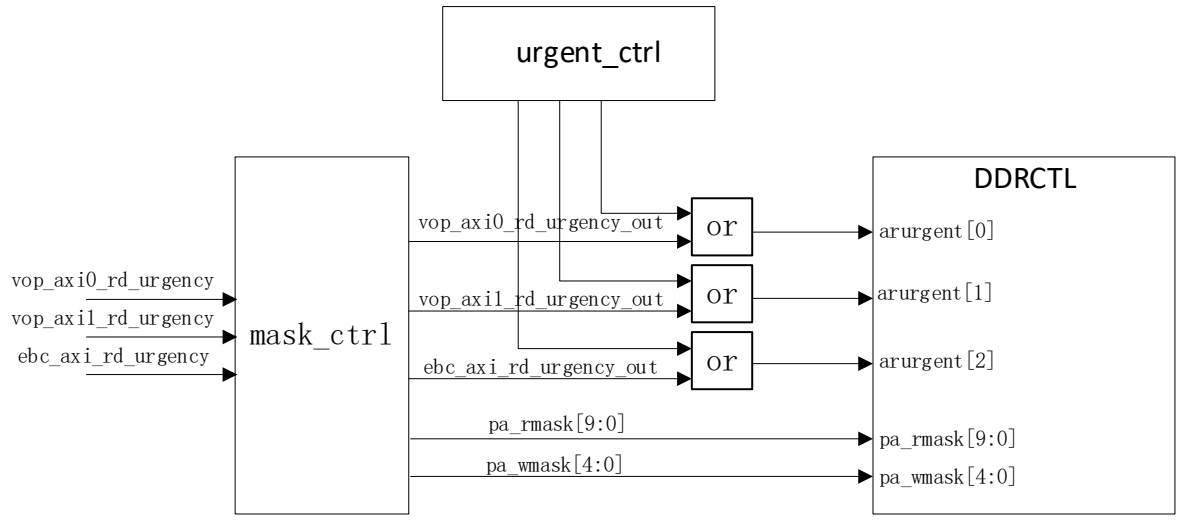


Fig. 7-3 Mask_ctrl Block Diagram

The input of mask_ctrl module is from VOP and EBC. Vop_axi0_rd_urgency means AXI read port0 of VOP becoming urgent, vop_axi1_rd_urgency means AXI read port1 of VOP becoming urgent and ebc_axi_rd_urgency means AXI read port of EBC becoming urgent. The output signals vop_axi0_rd_urgency_out, vop_axi1_rd_urgency_out and ebc_axi_rd_urgency_out are synchronize to the DDRCTL's core_ddrc_core_clk. If any of these three read urgency signals are pulled high, the mask_ctrl module will mask all the other AXI read ports and mask all the AXI write ports except the one that read port is urgent (If read/write ordered is enabled, the AXI write port can't be masked when the corresponding read port is urgent). For example, if vop_axi0_rd_urgency is high, the other two are low. Then write port of AXI port 1/2/3/4 are masked (Whether can be masked is controlled by DDR_GRF_CHA/CHB_CON18[4:1]), read port of AXI port 1/2/3/4 are masked(Whether can be masked is controlled by DDR_GRF_CHA/CHB_CON17[9:2]). Whether the write port of AXI port 0 can be masked depends on the DDR_GRF_CHA/CHB_CON18[0] and DDR_GRF_CHA/CHB_CON19[0].

7.3.2 DDRPHY

DDRPHY supports LPDDR4/4X/5 SDRAM and provides physical interface solutions for DDRCTL requiring access to JEDEC compatible SDRAM devices. It is optimized for low power and high speed (up to 4266Mbps for LPDDR4/4X and up to 4800Mbps for LPDDR5) applications with robust timing and small silicon area. The DDRPHY has fully digital DLL for 90° phase shift of strobe signal. DQS clean, read training, write training, dvfs training and periodic training are supported.

In order to support DDR fast frequency change, there are 2 PLLs in each DDR channel. D0APLL and D0BPLL are used to provide operation clock for DDRPHY channel 0, while D1APLL and D1BPLL are used for DDRPHY channel 1. The output clock of 2 PLLs in each channel are connected to the input of a multiplexer, the output of the multiplexer drives the DDRPHY source clock clk_phy2x. During DDR frequency change period, it just needs to switch to the other PLL that has locked before without waiting for PLL lock.

7.3.3 DFI Scramble

The function of DFI scramble module is to scramble data written to DDR SDRAM and descramble data read from DDR SDRAM. This module is by default bypassed. If it is enabled, it receives data from DDRCTL through DFI interface, scramble written data and then send it to the DDRPHY. It also descrambles date received from DDRPHY and send it back to DDRCTL through DFI interface.

7.3.4 DDR Monitor

The DDR Monitor Module has four functions. The first function is used when debug, it will monitor the DDR read or write address within a specified range. The second function is used to do the statistics about DDR bandwidth and utilization. The third function is used to statistic special pattern for a designated bank or for all banks. The fourth function is used to statistic low power such as self-refresh, power down, self-refresh power down, clock stop and so on.

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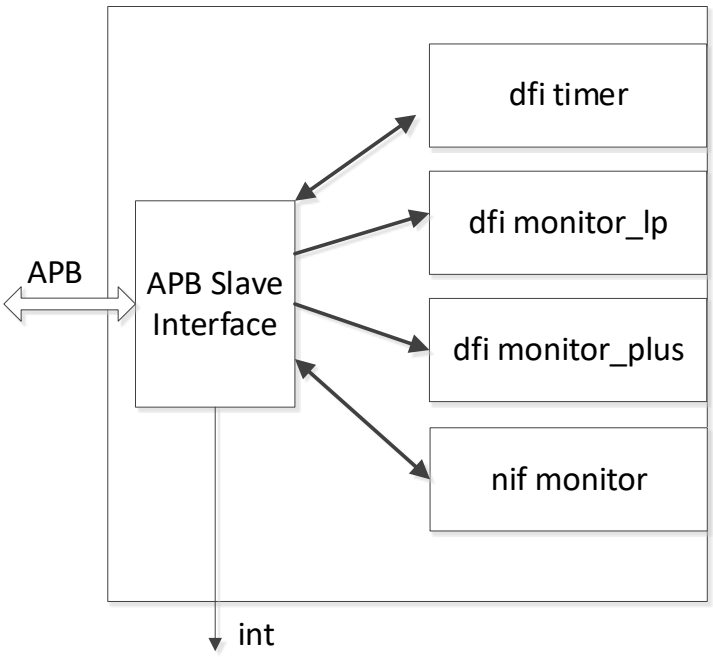


Fig. 7-4 DDR Monitor Block Diagram

The 5 AXI ports signals such as arready_n, arvalid_n, araddr_n[33:0], arid_n[7:0] and awready_n, awvalid_n, awaddr_n[33:0], awid_n[7:0](where n is 0~4) are input to the DDR Monitor. The host processor gets access to DDR Monitor Register Block through the APB slave interface, and the DDR Monitor can assert an active-high level interrupt to the host processor.

DDR Monitor does the monitor and statistics by dfi monitor_plus module, nif monitor module and dfi monitor_lp module. The dfi monitor_plus module is used to statistic DDR bandwidth, utilization and special pattern for a designated bank or for all banks. The nif monitor module is used to monitor DDR read or write address within a specified range. The dfi monitor_lp module is used to statistics low power.

7.4 Register Description

7.4.1 Internal Address Mapping For DDRCTL

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
DDRCTL0	0x28000000
DDRCTL1	0x29000000

7.4.2 Registers Summary For DDRCTL

Name	Offset	Size	Reset Value	Description
DDRCTL_DRAMSET1TMG0_FREQ0	0x0000	W	0x0F101B0F	SDRAM Timing Register 0 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG1_FREQ0	0x0004	W	0x00080414	SDRAM Timing Register 1 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG2_FREQ0	0x0008	W	0x0305060D	SDRAM Timing Register 2 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG3_FREQ0	0x000C	W	0x00040404	SDRAM Timing Register 3 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG4_FREQ0	0x0010	W	0x05040405	SDRAM Timing Register 4 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG5_FREQ0	0x0014	W	0x05050403	SDRAM Timing Register 5 belonging to Timing Set 1

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Name	Offset	Size	Reset Value	Description
DDRCTL_DRAMSET1TMG6_FREQ0	0x0018	W	0x00000005	SDRAM Timing Register 6 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG7_FREQ0	0x001C	W	0x00000000	SDRAM Timing Register 7 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG8_FREQ0	0x0020	W	0x00004405	SDRAM Timing Register 8 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG9_FREQ0	0x0024	W	0x0004040D	SDRAM Timing Register 9 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG12_FREQ0	0x0030	W	0x00020000	SDRAM Timing Register 12 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG13_FREQ0	0x0034	W	0x1C200004	SDRAM Timing Register 13 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG14_FREQ0	0x0038	W	0x000800A0	SDRAM Timing Register 14 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG23_FREQ0	0x005C	W	0x00000000	SDRAM Timing Register 23 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG24_FREQ0	0x0060	W	0x000F0F0F	SDRAM Timing Register 24 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG25_FREQ0	0x0064	W	0x00000000	SDRAM Timing Register 25 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG30_FREQ0	0x0078	W	0x00000000	SDRAM Timing Register 30 belonging to Timing Set 1
DDRCTL_INITMR0_FREQ0	0x0500	W	0x00000510	SDRAM Initialization MR Setting Register 0
DDRCTL_INITMR1_FREQ0	0x0504	W	0x00000000	SDRAM Initialization MR Setting Register 1
DDRCTL_INITMR2_FREQ0	0x0508	W	0x00000000	SDRAM Initialization MR Setting Register 2
DDRCTL_INITMR3_FREQ0	0x050C	W	0x00000000	SDRAM Initialization MR Setting Register 3
DDRCTL_DFITMG0_FREQ0	0x0580	W	0x07020002	DFI Timing Register 0
DDRCTL_DFITMG1_FREQ0	0x0584	W	0x00000404	DFI Timing Register 1
DDRCTL_DFITMG2_FREQ0	0x0588	W	0x00000202	DFI Timing Register 2
DDRCTL_DFITMG4_FREQ0	0x0590	W	0x00000000	DFI Timing Register 4
DDRCTL_DFITMG5_FREQ0	0x0594	W	0x00000000	DFI Timing Register 5
DDRCTL_DFILPTMG0_FREQ0	0x05A0	W	0x00000000	DFI Low Power Timing Register 0
DDRCTL_DFILPTMG1_FREQ0	0x05A4	W	0x00000700	DFI Low Power Timing Register 1
DDRCTL_DFIUPDTMG0_FREQ0	0x05A8	W	0x00400003	DFI Update Timing Register 0
DDRCTL_DFIUPDTMG1_FREQ0	0x05AC	W	0x00010001	DFI Update Timing Register 1
DDRCTL_DFIMSGTMG0_FREQ0	0x05B0	W	0x00000004	DFI MC-PHY Message Timing Register 0
DDRCTL_RFSHSET1TMG0_FREQ0	0x0600	W	0x02100062	Refresh Timing Register 0 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG1_FREQ0	0x0604	W	0x0000008C	Refresh Timing Register 1 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG2_FREQ0	0x0608	W	0x8C8C0000	Refresh Timing Register 2 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG4_FREQ0	0x0610	W	0x00000000	Refresh Timing Register 4 belonging to Timing Set 1

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Name	Offset	Size	Reset Value	Description
DDRCTL_ZQSET1TMG0_FREQ0	0x0800	W	0x00400200	ZQ Timing Register 0 belonging to DRAM ZQ timing set 1
DDRCTL_ZQSET1TMG1_FREQ0	0x0804	W	0x02000100	ZQ Timing Register 1 belonging to DRAM ZQ timing set 1
DDRCTL_DQSOSCCTL0_FREQ0	0x0A80	W	0x00000070	DQS/WCK Oscillator Control Register 0
DDRCTL_DERATEINT_FREQ0	0x0B00	W	0x00800000	Temperature Derate Interval Register
DDRCTL_DERATEVAL0_FREQ0	0x0B04	W	0x050F0504	Temperature Derate Timing Register 0
DDRCTL_DERATEVAL1_FREQ0	0x0B08	W	0x00000014	Temperature Derate Timing Register 1
DDRCTL_HWLPTMG0_FREQ0	0x0B80	W	0x00000000	Hardware Low Power Control Register
DDRCTL_SCHEDTMG0_FREQ0	0x0C00	W	0x00000000	Scheduler Control Register
DDRCTL_PERFHPR1_FREQ0	0x0C80	W	0x0F000001	High Priority Read CAM Register 1
DDRCTL_PERFLPR1_FREQ0	0x0C84	W	0x0F00007F	Low Priority Read CAM Register 1
DDRCTL_PERFWR1_FREQ0	0x0C88	W	0x0F00007F	Write CAM Register 1
DDRCTL_TMGCFG_FREQ0	0x0D00	W	0x00000000	Timing Configuration Register
DDRCTL_RANKTMG0_FREQ0	0x0D04	W	0x00000606	Rank Control Timing 0
DDRCTL_RANKTMG1_FREQ0	0x0D08	W	0x00000F0F	Rank Timing Register 1
DDRCTL_PWRTMG_FREQ0	0x0D0C	W	0x00400010	Low Power Timing Register
DDRCTL_MSTR0	0x10000	W	0x03040000	Master Register0
DDRCTL_MSTR2	0x10008	W	0x00000000	Master Register2
DDRCTL_MSTR4	0x10010	W	0x00000000	Master Register4
DDRCTL_STAT	0x10014	W	0x00000000	Operating Mode Status Register
DDRCTL_MRCTRL0	0x10080	W	0x00000030	Mode Register Read/Write Control Register 0.
DDRCTL_MRCTRL1	0x10084	W	0x00000000	Mode Register Read/Write Control Register 1
DDRCTL_MRSTAT	0x10090	W	0x00000000	Mode Register Read/Write Status Register
DDRCTL_MRRDATA0	0x10094	W	0x00000000	Mode Register Read Data 0
DDRCTL_MRRDATA1	0x10098	W	0x00000000	Mode Register Read Data 1
DDRCTL_DERATECTL0	0x10100	W	0x00000018	Temperature Derate Control Register 0
DDRCTL_DERATECTL1	0x10104	W	0x00000000	Temperature Derate Control Register 1
DDRCTL_DERATECTL2	0x10108	W	0x00000000	Temperature Derate Control Register 2
DDRCTL_DERATECTL5	0x10114	W	0x00000001	Temperature Derate Control Register 5
DDRCTL_DERATECTL6	0x10118	W	0x00000000	Temperature Derate Control Register 6
DDRCTL_DERATESTAT0	0x1011C	W	0x00000000	Temperature Derate Status Register 0
DDRCTL_DERATEDBGCTL	0x10124	W	0x00000000	Temperature Derate Debug Contrl Register

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Name	Offset	Size	Reset Value	Description
DDRCTL_DERATEDBGSTAT	0x10128	W	0x00000000	Temperature Derate Debug Status Register
DDRCTL_PWRCTL	0x10180	W	0x00000000	Low Power Control Register
DDRCTL_HWLPCTL	0x10184	W	0x00000003	Hardware Low Power Control Register
DDRCTL_CLKGATECTL	0x1018C	W	0x0000003F	clock gate control
DDRCTL_RFSHMOD0	0x10200	W	0x00000000	Refresh Mode Register 0
DDRCTL_RFSHCTL0	0x10208	W	0x00000000	Refresh Control Register 0
DDRCTL_ZQCTL0	0x10280	W	0x00000000	ZQ Control Register 0
DDRCTL_ZQCTL1	0x10284	W	0x00000000	ZQ Control Register 1
DDRCTL_ZQCTL2	0x10288	W	0x00000000	ZQ Control Register 2
DDRCTL_ZQSTAT	0x1028C	W	0x00000000	ZQ Status Register
DDRCTL_DQSOSCRUNTIME	0x10300	W	0x00400040	DQS/WCK Oscillator Runtime Register
DDRCTL_DQSOSCSTAT0	0x10304	W	0x00000000	DQS/WCK Oscillator Status Register 0
DDRCTL_DQSOSCCFG0	0x10308	W	0x00000000	DQSOSC ConfigureRegister 0
DDRCTL_SCHED0	0x10380	W	0x8001201C	Scheduler Control Register 0
DDRCTL_SCHED1	0x10384	W	0x00002000	Scheduler Control Register 1
DDRCTL_SCHED3	0x1038C	W	0x04040208	Scheduler Control Register 3
DDRCTL_SCHED4	0x10390	W	0x08400810	Scheduler Control Register 4
DDRCTL_DFILPCFG0	0x10500	W	0x00100000	DFI Low Power Configuration Register 0
DDRCTL_DFIUPD0	0x10508	W	0x00008000	DFI Update Register 0
DDRCTL_DFIMISC	0x10510	W	0x00000001	DFI Miscellaneous Control Register
DDRCTL_DFISTAT	0x10514	W	0x00000000	DFI Status Register
DDRCTL_DFIPHYMSTR	0x10518	W	0x80000001	DFI PHY Master
DDRCTL_DFI0MSGCTL0	0x10520	W	0x00000000	DFI0 Message Control Register 0.
DDRCTL_DFI0MSGSTAT0	0x10524	W	0x00000000	DFI0 Message Status Register 0
DDRCTL_POISONCFG	0x10580	W	0x00110011	AXI Poison Configuration Register. Common for all AXI ports
DDRCTL_POISONSTAT	0x10584	W	0x00000000	AXI Poison Status Register
DDRCTL_OPCTRL0	0x10B80	W	0x00000000	Operation Control Register 0
DDRCTL_OPCTRL1	0x10B84	W	0x00000000	Operation Control Register 1
DDRCTL_OPCTRLCAM	0x10B88	W	0x00000000	CAM Operation Control Register
DDRCTL_OPCTRLCMD	0x10B8C	W	0x00000000	Command Operation Control Register
DDRCTL_OPCTRLSTAT	0x10B90	W	0x00000000	Status Operation Control Register
DDRCTL_OPREFCTRL0	0x10B98	W	0x00000000	Refresh Operation Control Register 0
DDRCTL_OPREFSTAT0	0x10BA0	W	0x00000000	Refresh Operation Status Register 0
DDRCTL_SWCTL	0x10C80	W	0x00000001	Software Register Programming Control Enable
DDRCTL_SWSTAT	0x10C84	W	0x00000001	Software Register Programming Control Status
DDRCTL_RANKCTL	0x10C90	W	0x0000000F	Rank Control Register
DDRCTL_DBICTL	0x10C94	W	0x00000001	DM/DBI Control Register
DDRCTL_ODTMAP	0x10C9C	W	0x00002211	ODT/Rank Map Register
DDRCTL_DATACTL0	0x10CA0	W	0x00000000	Data Control register 0
DDRCTL_SWCTLSTATIC	0x10CA4	W	0x00000000	Static Registers Write Enable

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Name	Offset	Size	Reset Value	Description
DDRCTL_INITTMG0	0x10D00	W	0x0002004E	SDRAM Initialization Timing Register 0
DDRCTL_INITTMG1	0x10D04	W	0x00000000	SDRAM Initialization Timing Register 1
DDRCTL_DDRCTL_VER_NUMBER	0x10FF8	W	0x3130312A	DDRCTL Version Number Register
DDRCTL_DDRCTL_VER_TYPE	0x10FFC	W	0x6C633031	DDRCTL Version Type Register
DDRCTL_PCCFG_PORT0	0x20000	W	0x00000000	Port Common Configuration Register.
DDRCTL_PCFGR_PORT0	0x20004	W	0x0000501F	Configuration Read Register
DDRCTL_PCFGW_PORT0	0x20008	W	0x0000501F	Configuration Write Register
DDRCTL_PCTRL_PORT0	0x20090	W	0x00000000	Port Control Register
DDRCTL_PCFGQOS0_PORT0	0x20094	W	0x00000000	Port n Read QoS Configuration Register 0
DDRCTL_PCFGQOS1_PORT0	0x20098	W	0x00000000	Port n Read QoS Configuration Register 1
DDRCTL_PCFGWQOS0_PORT0	0x2009C	W	0x00000E00	Port n Write QoS Configuration Register 0
DDRCTL_PCFGWQOS1_PORT0	0x200A0	W	0x00000000	Port n Write QoS Configuration Register 1
DDRCTL_PSTAT_PORT0	0x20114	W	0x00000000	Port Status Register
DDRCTL_PCFGR_PORT1	0x21004	W	0x0000501F	Configuration Read Register
DDRCTL_PCFGW_PORT1	0x21008	W	0x0000501F	Configuration Write Register
DDRCTL_PCTRL_PORT1	0x21090	W	0x00000000	Port Control Register
DDRCTL_PCFGQOS0_PORT1	0x21094	W	0x00000000	Port n Read QoS Configuration Register 0
DDRCTL_PCFGQOS1_PORT1	0x21098	W	0x00000000	Port n Read QoS Configuration Register 1
DDRCTL_PCFGWQOS0_PORT1	0x2109C	W	0x00000E00	Port n Write QoS Configuration Register 0
DDRCTL_PCFGWQOS1_PORT1	0x210A0	W	0x00000000	Port n Write QoS Configuration Register 1
DDRCTL_PCFGR_PORT2	0x22004	W	0x0000501F	Configuration Read Register
DDRCTL_PCFGW_PORT2	0x22008	W	0x0000501F	Configuration Write Register
DDRCTL_PCTRL_PORT2	0x22090	W	0x00000000	Port Control Register
DDRCTL_PCFGQOS0_PORT2	0x22094	W	0x00000000	Port n Read QoS Configuration Register 0
DDRCTL_PCFGQOS1_PORT2	0x22098	W	0x00000000	Port n Read QoS Configuration Register 1
DDRCTL_PCFGWQOS0_PORT2	0x2209C	W	0x00000E00	Port n Write QoS Configuration Register 0
DDRCTL_PCFGWQOS1_PORT2	0x220A0	W	0x00000000	Port n Write QoS Configuration Register 1
DDRCTL_PCFGR_PORT3	0x23004	W	0x0000501F	Configuration Read Register
DDRCTL_PCFGW_PORT3	0x23008	W	0x0000501F	Configuration Write Register
DDRCTL_PCTRL_PORT3	0x23090	W	0x00000000	Port Control Register
DDRCTL_PCFGQOS0_PORT3	0x23094	W	0x00000000	Port n Read QoS Configuration Register 0
DDRCTL_PCFGQOS1_PORT3	0x23098	W	0x00000000	Port n Read QoS Configuration Register 1
DDRCTL_PCFGWQOS0_PORT3	0x2309C	W	0x00000E00	Port n Write QoS Configuration Register 0

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Name	Offset	Size	Reset Value	Description
DDRCTL_PCFGWQOS1_PORT3	0x230A0	W	0x00000000	Port n Write QoS Configuration Register 1
DDRCTL_PCFGR_PORT4	0x24004	W	0x0000501F	Configuration Read Register
DDRCTL_PCFGW_PORT4	0x24008	W	0x0000501F	Configuration Write Register
DDRCTL_PCTRL_PORT4	0x24090	W	0x00000000	Port Control Register
DDRCTL_PCFGQOS0_PORT4	0x24094	W	0x00000000	Port n Read QoS Configuration Register 0
DDRCTL_PCFGQOS1_PORT4	0x24098	W	0x00000000	Port n Read QoS Configuration Register 1
DDRCTL_PCFGWQOS0_PORT4	0x2409C	W	0x00000E00	Port n Write QoS Configuration Register 0
DDRCTL_PCFGWQOS1_PORT4	0x240A0	W	0x00000000	Port n Write QoS Configuration Register 1
DDRCTL_ADDRMAP1	0x30004	W	0x00000000	Address Map Register 1
DDRCTL_ADDRMAP3	0x3000C	W	0x00000000	Address Map Register 3
DDRCTL_ADDRMAP4	0x30010	W	0x00000000	Address Map Register 4
DDRCTL_ADDRMAP5	0x30014	W	0x00000000	Address Map Register 5
DDRCTL_ADDRMAP6	0x30018	W	0x00000000	Address Map Register 6
DDRCTL_ADDRMAP7	0x3001C	W	0x00000000	Address Map Register 7
DDRCTL_ADDRMAP8	0x30020	W	0x00000000	Address Map Register 8
DDRCTL_ADDRMAP9	0x30024	W	0x00000000	Address Map Register 9
DDRCTL_ADDRMAP10	0x30028	W	0x00000000	Address Map Register 10
DDRCTL_ADDRMAP11	0x3002C	W	0x00000000	Address Map Register 11
DDRCTL_ADDRMAP12	0x30030	W	0x00000000	Address Map Register 12
DDRCTL_DRAMSET1TMG0_FREQ1	0x100000	W	0x0F101B0F	SDRAM Timing Register 0 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG1_FREQ1	0x100004	W	0x00080414	SDRAM Timing Register 1 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG2_FREQ1	0x100008	W	0x0305060D	SDRAM Timing Register 2 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG3_FREQ1	0x10000C	W	0x00040404	SDRAM Timing Register 3 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG4_FREQ1	0x100010	W	0x05040405	SDRAM Timing Register 4 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG5_FREQ1	0x100014	W	0x05050403	SDRAM Timing Register 5 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG6_FREQ1	0x100018	W	0x00000005	SDRAM Timing Register 6 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG7_FREQ1	0x10001C	W	0x00000000	SDRAM Timing Register 7 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG8_FREQ1	0x100020	W	0x00004405	SDRAM Timing Register 8 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG9_FREQ1	0x100024	W	0x0004040D	SDRAM Timing Register 9 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG12_FREQ1	0x100030	W	0x00020000	SDRAM Timing Register 12 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG13_FREQ1	0x100034	W	0x1C200004	SDRAM Timing Register 13 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG14_FREQ1	0x100038	W	0x000800A0	SDRAM Timing Register 14 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG23_FREQ1	0x10005C	W	0x00000000	SDRAM Timing Register 23 belonging to Timing Set 1

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Name	Offset	Size	Reset Value	Description
DDRCTL_DRAMSET1TMG24_FREQ1	0x100060	W	0x000F0F0F	SDRAM Timing Register 24 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG25_FREQ1	0x100064	W	0x00000000	SDRAM Timing Register 25 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG30_FREQ1	0x100078	W	0x00000000	SDRAM Timing Register 30 belonging to Timing Set 1
DDRCTL_INITMR0_FREQ1	0x100500	W	0x00000510	SDRAM Initialization MR Setting Register 0
DDRCTL_INITMR1_FREQ1	0x100504	W	0x00000000	SDRAM Initialization MR Setting Register 1
DDRCTL_INITMR2_FREQ1	0x100508	W	0x00000000	SDRAM Initialization MR Setting Register 2
DDRCTL_INITMR3_FREQ1	0x10050C	W	0x00000000	SDRAM Initialization MR Setting Register 3
DDRCTL_DFITMG0_FREQ1	0x100580	W	0x07020002	DFI Timing Register 0
DDRCTL_DFITMG1_FREQ1	0x100584	W	0x00000404	DFI Timing Register 1
DDRCTL_DFITMG2_FREQ1	0x100588	W	0x00000202	DFI Timing Register 2
DDRCTL_DFITMG4_FREQ1	0x100590	W	0x00000000	DFI Timing Register 4
DDRCTL_DFITMG5_FREQ1	0x100594	W	0x00000000	DFI Timing Register 5
DDRCTL_DFIUPDTMG1_FREQ1	0x1005AC	W	0x00010001	DFI Update Timing Register 1
DDRCTL_RFSHSET1TMG0_FREQ1	0x100600	W	0x02100062	Refresh Timing Register 0 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG1_FREQ1	0x100604	W	0x0000008C	Refresh Timing Register 1 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG2_FREQ1	0x100608	W	0x8C8C0000	Refresh Timing Register 2 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG4_FREQ1	0x100610	W	0x00000000	Refresh Timing Register 4 belonging to Timing Set 1
DDRCTL_ZQSET1TMG0_FREQ1	0x100800	W	0x00400200	ZQ Timing Register 0 belonging to DRAM ZQ timing set 1
DDRCTL_ZQSET1TMG1_FREQ1	0x100804	W	0x02000100	ZQ Timing Register 1 belonging to DRAM ZQ timing set 1
DDRCTL_DQSOSCCTL0_FREQ1	0x100A80	W	0x00000070	DQS/WCK Oscillator Control Register 0
DDRCTL_DERATEINT_FREQ1	0x100B00	W	0x00800000	Temperature Derate Interval Register
DDRCTL_DERATEVAL0_FREQ1	0x100B04	W	0x050F0504	Temperature Derate Timing Register 0
DDRCTL_DERATEVAL1_FREQ1	0x100B08	W	0x00000014	Temperature Derate Timing Register 1
DDRCTL_HWLPTMG0_FREQ1	0x100B80	W	0x00000000	Hardware Low Power Control Register
DDRCTL_SCHEDTMG0_FREQ1	0x100C00	W	0x00000000	Scheduler Control Register
DDRCTL_PERFHPR1_FREQ1	0x100C80	W	0x0F000001	High Priority Read CAM Register 1
DDRCTL_PERFLPR1_FREQ1	0x100C84	W	0x0F00007F	Low Priority Read CAM Register 1
DDRCTL_PERFWR1_FREQ1	0x100C88	W	0x0F00007F	Write CAM Register 1
DDRCTL_TMGCFG_FREQ1	0x100D00	W	0x00000000	Timing Configuration Register
DDRCTL_RANKTMG0_FREQ1	0x100D04	W	0x00000606	Rank Control Timing 0

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Name	Offset	Size	Reset Value	Description
DDRCTL_RANKTMG1_FREQ1	0x100D08	W	0x00000F0F	Rank Timing Register 1
DDRCTL_PWRTMG_FREQ1	0x100D0C	W	0x00400010	Low Power Timing Register
DDRCTL_DRAMSET1TMG0_FREQ2	0x200000	W	0x0F101B0F	SDRAM Timing Register 0 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG1_FREQ2	0x200004	W	0x00080414	SDRAM Timing Register 1 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG2_FREQ2	0x200008	W	0x0305060D	SDRAM Timing Register 2 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG3_FREQ2	0x20000C	W	0x00040404	SDRAM Timing Register 3 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG4_FREQ2	0x200010	W	0x05040405	SDRAM Timing Register 4 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG5_FREQ2	0x200014	W	0x05050403	SDRAM Timing Register 5 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG6_FREQ2	0x200018	W	0x00000005	SDRAM Timing Register 6 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG7_FREQ2	0x20001C	W	0x00000000	SDRAM Timing Register 7 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG8_FREQ2	0x200020	W	0x00004405	SDRAM Timing Register 8 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG9_FREQ2	0x200024	W	0x0004040D	SDRAM Timing Register 9 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG12_FREQ2	0x200030	W	0x00020000	SDRAM Timing Register 12 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG13_FREQ2	0x200034	W	0x1C200004	SDRAM Timing Register 13 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG14_FREQ2	0x200038	W	0x000800A0	SDRAM Timing Register 14 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG23_FREQ2	0x20005C	W	0x00000000	SDRAM Timing Register 23 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG24_FREQ2	0x200060	W	0x000F0F0F	SDRAM Timing Register 24 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG25_FREQ2	0x200064	W	0x00000000	SDRAM Timing Register 25 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG30_FREQ2	0x200078	W	0x00000000	SDRAM Timing Register 30 belonging to Timing Set 1
DDRCTL_INITMR0_FREQ2	0x200500	W	0x00000510	SDRAM Initialization MR Setting Register 0
DDRCTL_INITMR1_FREQ2	0x200504	W	0x00000000	SDRAM Initialization MR Setting Register 1
DDRCTL_INITMR2_FREQ2	0x200508	W	0x00000000	SDRAM Initialization MR Setting Register 2
DDRCTL_INITMR3_FREQ2	0x20050C	W	0x00000000	SDRAM Initialization MR Setting Register 3
DDRCTL_DFITMG0_FREQ2	0x200580	W	0x07020002	DFI Timing Register 0
DDRCTL_DFITMG1_FREQ2	0x200584	W	0x00000404	DFI Timing Register 1
DDRCTL_DFITMG2_FREQ2	0x200588	W	0x00000202	DFI Timing Register 2
DDRCTL_DFITMG4_FREQ2	0x200590	W	0x00000000	DFI Timing Register 4
DDRCTL_DFITMG5_FREQ2	0x200594	W	0x00000000	DFI Timing Register 5
DDRCTL_DFIUPDTMG1_FREQ2	0x2005AC	W	0x00010001	DFI Update Timing Register 1
DDRCTL_RFSHSET1TMG0_FREQ2	0x200600	W	0x02100062	Refresh Timing Register 0 belonging to Timing Set 1

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Name	Offset	Size	Reset Value	Description
DDRCTL_RFSHSET1TMG1_FREQ2	0x200604	W	0x0000008C	Refresh Timing Register 1 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG2_FREQ2	0x200608	W	0x8C8C0000	Refresh Timing Register 2 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG4_FREQ2	0x200610	W	0x00000000	Refresh Timing Register 4 belonging to Timing Set 1
DDRCTL_ZQSET1TMG0_FREQ2	0x200800	W	0x00400200	ZQ Timing Register 0 belonging to DRAM ZQ timing set 1
DDRCTL_ZQSET1TMG1_FREQ2	0x200804	W	0x02000100	ZQ Timing Register 1 belonging to DRAM ZQ timing set 1
DDRCTL_DQSOSCCTL0_FREQ2	0x200A80	W	0x00000070	DQS/WCK Oscillator Control Register 0
DDRCTL_DERATEINT_FREQ2	0x200B00	W	0x00800000	Temperature Derate Interval Register
DDRCTL_DERATEVAL0_FREQ2	0x200B04	W	0x050F0504	Temperature Derate Timing Register 0
DDRCTL_DERATEVAL1_FREQ2	0x200B08	W	0x00000014	Temperature Derate Timing Register 1
DDRCTL_HWLPTMG0_FREQ2	0x200B80	W	0x00000000	Hardware Low Power Control Register
DDRCTL_SCHEDTMG0_FREQ2	0x200C00	W	0x00000000	Scheduler Control Register
DDRCTL_PERFHPR1_FREQ2	0x200C80	W	0x0F000001	High Priority Read CAM Register 1
DDRCTL_PERFLPR1_FREQ2	0x200C84	W	0x0F00007F	Low Priority Read CAM Register 1
DDRCTL_PERFWR1_FREQ2	0x200C88	W	0x0F00007F	Write CAM Register 1
DDRCTL_TMGCFG_FREQ2	0x200D00	W	0x00000000	Timing Configuration Register
DDRCTL_RANKTMG0_FREQ2	0x200D04	W	0x00000606	Rank Control Timing 0
DDRCTL_RANKTMG1_FREQ2	0x200D08	W	0x00000F0F	Rank Timing Register 1
DDRCTL_PWRTMG_FREQ2	0x200D0C	W	0x00400010	Low Power Timing Register
DDRCTL_DRAMSET1TMG0_FREQ3	0x300000	W	0x0F101B0F	SDRAM Timing Register 0 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG1_FREQ3	0x300004	W	0x00080414	SDRAM Timing Register 1 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG2_FREQ3	0x300008	W	0x0305060D	SDRAM Timing Register 2 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG3_FREQ3	0x30000C	W	0x00040404	SDRAM Timing Register 3 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG4_FREQ3	0x300010	W	0x05040405	SDRAM Timing Register 4 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG5_FREQ3	0x300014	W	0x05050403	SDRAM Timing Register 5 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG6_FREQ3	0x300018	W	0x00000005	SDRAM Timing Register 6 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG7_FREQ3	0x30001C	W	0x00000000	SDRAM Timing Register 7 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG8_FREQ3	0x300020	W	0x00004405	SDRAM Timing Register 8 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG9_FREQ3	0x300024	W	0x0004040D	SDRAM Timing Register 9 belonging to Timing Set 1

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Name	Offset	Size	Reset Value	Description
DDRCTL_DRAMSET1TMG12_FREQ3	0x300030	W	0x00020000	SDRAM Timing Register 12 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG13_FREQ3	0x300034	W	0x1C200004	SDRAM Timing Register 13 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG14_FREQ3	0x300038	W	0x000800A0	SDRAM Timing Register 14 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG23_FREQ3	0x30005C	W	0x00000000	SDRAM Timing Register 23 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG24_FREQ3	0x300060	W	0x000F0F0F	SDRAM Timing Register 24 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG25_FREQ3	0x300064	W	0x00000000	SDRAM Timing Register 25 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG30_FREQ3	0x300078	W	0x00000000	SDRAM Timing Register 30 belonging to Timing Set 1
DDRCTL_INITMR0_FREQ3	0x300500	W	0x00000510	SDRAM Initialization MR Setting Register 0
DDRCTL_INITMR1_FREQ3	0x300504	W	0x00000000	SDRAM Initialization MR Setting Register 1
DDRCTL_INITMR2_FREQ3	0x300508	W	0x00000000	SDRAM Initialization MR Setting Register 2
DDRCTL_INITMR3_FREQ3	0x30050C	W	0x00000000	SDRAM Initialization MR Setting Register 3
DDRCTL_DFITMG0_FREQ3	0x300580	W	0x07020002	DFI Timing Register 0
DDRCTL_DFITMG1_FREQ3	0x300584	W	0x00000404	DFI Timing Register 1
DDRCTL_DFITMG2_FREQ3	0x300588	W	0x00000202	DFI Timing Register 2
DDRCTL_DFITMG4_FREQ3	0x300590	W	0x00000000	DFI Timing Register 4
DDRCTL_DFITMG5_FREQ3	0x300594	W	0x00000000	DFI Timing Register 5
DDRCTL_DFIUPDTMG1_FREQ3	0x3005AC	W	0x00010001	DFI Update Timing Register 1
DDRCTL_RFSHSET1TMG0_FREQ3	0x300600	W	0x02100062	Refresh Timing Register 0 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG1_FREQ3	0x300604	W	0x0000008C	Refresh Timing Register 1 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG2_FREQ3	0x300608	W	0x8C8C0000	Refresh Timing Register 2 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG4_FREQ3	0x300610	W	0x00000000	Refresh Timing Register 4 belonging to Timing Set 1
DDRCTL_ZQSET1TMG0_FREQ3	0x300800	W	0x00400200	ZQ Timing Register 0 belonging to DRAM ZQ timing set 1
DDRCTL_ZQSET1TMG1_FREQ3	0x300804	W	0x02000100	ZQ Timing Register 1 belonging to DRAM ZQ timing set 1
DDRCTL_DQSOSCCTL0_FREQ3	0x300A80	W	0x00000070	DQS/WCK Oscillator Control Register 0
DDRCTL_DERATEINT_FREQ3	0x300B00	W	0x00800000	Temperature Derate Interval Register
DDRCTL_DERATEVAL0_FREQ3	0x300B04	W	0x050F0504	Temperature Derate Timing Register 0
DDRCTL_DERATEVAL1_FREQ3	0x300B08	W	0x00000014	Temperature Derate Timing Register 1
DDRCTL_HWLPTMG0_FREQ3	0x300B80	W	0x00000000	Hardware Low Power Control Register
DDRCTL_SCHEDTMG0_FREQ3	0x300C00	W	0x00000000	Scheduler Control Register

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Name	Offset	Size	Reset Value	Description
DDRCTL_PERFHPR1_FREQ3	0x300C80	W	0x0F000001	High Priority Read CAM Register 1
DDRCTL_PERFLPR1_FREQ3	0x300C84	W	0x0F00007F	Low Priority Read CAM Register 1
DDRCTL_PERFWR1_FREQ3	0x300C88	W	0x0F00007F	Write CAM Register 1
DDRCTL_TMGCFG_FREQ3	0x300D00	W	0x00000000	Timing Configuration Register
DDRCTL_RANKTMG0_FREQ3	0x300D04	W	0x00000606	Rank Control Timing 0
DDRCTL_RANKTMG1_FREQ3	0x300D08	W	0x00000F0F	Rank Timing Register 1
DDRCTL_PWRTMG_FREQ3	0x300D0C	W	0x00400010	Low Power Timing Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.3 Detail Registers Description For DDRCTL

Some register fields might use the following optional attributes.
Volatile: If true, indicates in the case of a write followed by read, or in the case of two consecutive reads, there is no guarantee as to what is returned by the read on the second transaction or that this return value is consistent with the write or read of the first transaction. The element implies there is some additional mechanism by which this field can acquire new values other than by reads/writes/resets. For example, when the controller updates the register field contents.
Testable: Possible values are unconstrained, untestable, readOnly, writeAsRead, restore. Untestable means that this field is untestable by a simple automated register test. For example, the read-write access of the register is controlled by a pin or another register. Read only means that you should not write to this register; only read from it. This might apply for a register that modifies the contents of another register.
The Programming Mode Field: The "Programming Mode" field in the description column of the register tables specifies the type of register. The DDRCTL registers belong to one of the following types.

- Static: Can be written only when the controller is in reset.
- Dynamic: Can be written at any time during operation.
- Quasi Dynamic: Can be written when the controller is in reset and some specific conditions outside reset. Please refer to the application notes for detailed information.

DDRCTL_DRAMSET1TMG0_FREQ0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	wr2pre Minimum time between write and precharge to same bank. Specifications: WL + BL/2 + tWR where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present. tWR = Write recovery time. This comes directly from the SDRAM specification. Add one extra cycle for LPDDR4/5 for this parameter. Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

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Bit	Attr	Reset Value	Description
23:16	RW	0x10	t_faw tFAW: At most 4 banks must be activated in a rolling window of tFAW cycles. Unit: DRAM clock cycles. Value After Reset: 0x10 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:8	RW	0x1b	t_ras_max tRAS(max): Maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open t_ras_max must be set to RoundDown(tRAS(max)/tCK/1024). Unit: 1024 DRAM clock cycles. Value After Reset: 0x1b Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:0	RW	0x0f	t_ras_min tRAS(min): Minimum time between activate and precharge to the same bank. Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG1_FREQ0

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x08	t_xp tXP: Minimum time after power-down exit to any operation. LPDDR4 (tCKELPD is defined in spec): larger of tXP and tCKELPD instead. LPDDR4 (tCKELPD is not defined in spec): tXP. LPDDR5: tXP + tCSH Unit: DRAM clock cycles. Value After Reset: 0x8 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:8	RW	0x04	rd2pre tRTP: Minimum time from read to precharge of same bank. LPDDR4 - BL/2 + max(RoundUp(tRTP/tCK),8) - 8 LPDDR5(BG mode): BL/n_min + RU(tRBTP/tCK) LPDDR5(16B mode): BL/n + RU(tRBTP/tCK) Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x14	t_rc tRC: Minimum time between activates to same bank. Unit: DRAM clock cycles. Value After Reset: 0x14 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG2_FREQ0

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Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x03	write_latency Set to WL Time from write command to write data on SDRAM interface. This must be set to WL. For all protocols, in addition to programming this register field, it is necessary to program DDRCTL_DFITMG0_FREQ0 and DDRCTL_DFITMG1_FREQ0 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset: 0x3 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
23	RO	0x0	reserved
22:16	RW	0x05	read_latency Set to RL Time from read command to read data on SDRAM interface. This must be set to RL. In addition to programming this register field, it is necessary to program DDRCTL_DFITMG0_FREQ0 and DDRCTL_DFITMG1_FREQ0 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x06	rd2wr LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled) : RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (BG mode && DQ ODT is Disabled): RL + BL/n_max + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (BG mode && DQ ODT is Enabled) : RL + BL/n_max + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (16B mode && DQ ODT is Disabled): RL + BL/n + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (16B mode && DQ ODT is Enabled) : RL + BL/n + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 Minimum time from read command to write command. Include time for bus turnaround and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM RL = read latency = CAS latency WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). RD_POSTAMBLE = 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation.

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Bit	Attr	Reset Value	Description
			For LPDDR4, if derating is enabled (DDRCTL_DERATECTL0_FREQ0.derate_enable=1), derated tDQSCKmax must be used. Unit: DRAM clock cycles. Value After Reset: 0x6 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x0d	wr2rd LPDDR4: WL + BL/2 + tWTR + 1 LPDDR5(BG mode): WL + BL/n_max + RU(tWTR_L/tCK) LPDDR5(16B mode): WL + BL/n + RU(tWTR/tCK) Minimum time from write command to read command. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: CWL = CAS write latency WL = Write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_L = internal write to read command delay for same bank group. This comes directly from the SDRAM specification. tWTR = internal write to read command delay. This comes directly from the SDRAM specification. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Add one extra cycle for LPDDR4 operation. Unit: DRAM clock cycles. Value After Reset: 0xd Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG3_FREQ0

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x04	t_mr Time from MRW/MRS to valid command LPDDR4: Set this to the larger of tMRR, tMRW, tMRWCKEL and tMRD. LPDDR5: Set this to the larger of tMRR, tMRW, tMRWPD and tMRD. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

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Bit	Attr	Reset Value	Description
15:8	RW	0x04	rd2mr Time from Read to MRW/MRR command. LPDDR4: RL + BL/2 + RU(tDQSCKmax/tCK) + RD(tRPST) + max(RU(7.5ns/tCK),8nCK) + nRTP - 8 LPDDR5: RL + RU(tWCKDQO(max)/tCK)) + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nRBTP Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:0	RW	0x04	wr2mr Time from Write to MRW/MRR command. LPDDR4: WL + 1 + BL/2 + max(RU(7.5ns/tCK),8nCK) + nWR LPDDR5: WL + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nWR Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG4_FREQ0

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	t_rcd tRCD - tAL: Minimum time from activate to read or write command to same bank. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
23:22	RO	0x0	reserved
21:16	RW	0x04	t_ccd This is the minimum time between two reads or two writes. LPDDR4: tCCD LPDDR5: BL/n Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:14	RO	0x0	reserved
13:8	RW	0x04	t_rrd For LPDDR5(BG mode): Minimum time between activates from bank "a" to bank "b" for same bank group. For LPDDR4/LPDDR5(16B mode): Minimum time between activates from bank "a" to bank "b". LPDDR4: RU(tRRD/tCK) LPDDR5(BG mode): RU(tRRD_L/tCK) LPDDR5(16B mode): RU(tRRD/tCK) Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:0	RW	0x05	t_rp tRP: Minimum time from single-bank precharge to activate of same bank. t_rp must be set to RoundUp(tRP/tCK). Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG5_FREQ0

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x05	t_cksrx This is the time before Self Refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: LPDDR4: tCKCKEH LPDDR5: tCKCSH Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
23	RO	0x0	reserved
22:16	RW	0x05	t_cksre This is the time after Self Refresh Down Entry/Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE/PDE. Recommended settings: LPDDR4: tCKELCK LPDDR5: tCSLCK Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15	RO	0x0	reserved
14:8	RW	0x04	t_ckesr Minimum CKE low width for Self refresh or Self refresh power down entry to exit timing in memory clock cycles. Recommended settings: LPDDR4: Max(tCKE, tSR) LPDDR5: tSR Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:6	RO	0x0	reserved
5:0	RW	0x03	t_cke Delay time between PDE and PDX. LPDDR4: tCKE LPDDR5: tCSPD Unit: DRAM clock cycles. Value After Reset: 0x3 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

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DDRCTL_DRAMSET1TMG6_FREQ0

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x05	t_ckcsx This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit. Recommended settings: LPDDR4/5: tXP + 2 This is only present for designs supporting LPDDR devices. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG7_FREQ0

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	t_csh CS High Pulse width at PDX LPDDR5: tCSH Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG8_FREQ0

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	reserved
14:8	RW	0x44	t_xs_dll_x32 tXSDLL: Exit Self Refresh to commands requiring a locked DLL. Note: Not used for LPDDR4/LPDDR5 SDRAMs.
7	RO	0x0	reserved
6:0	RW	0x05	t_xs_x32 tXS: Exit Self Refresh to commands not requiring a locked DLL. Note: Not used for LPDDR4/5 SDRAMs.

DDRCTL_DRAMSET1TMG9_FREQ0

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x04	t_ccd_s tCCD_S: This is the minimum time between two reads or two writes for different bank group. For bank switching (from bank "a" to bank "b"), the minimum time is this value + 1. Note: This register field is only applicable for designs supporting LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

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Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:8	RW	0x04	t_rrd_s tRRD_S: Minimum time between activates from bank "a" to bank "b" for different bank group. Note: This register field is only applicable for designs supporting LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:0	RW	0x0d	wr2rd_s Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Applicable only in designs configured to support LPDDR5 SDRAM memories. LPDDR5 designs: WL + BL/n_min +RU(tWTR_S/tCK) Where: WL = Write Latency BL/n_min = Effective Burst Length tWTR_S = internal write to read command delay for different bank group. Unit: DRAM clock cycles. Value After Reset: 0xd Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG12_FREQ0

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x2	t_cmdcke tCMDCKE: Delay from valid command to PDE LPDDR4: Max(tESCKE, tCMDCKE) LPDDR5: Max(tESPD, tCMDPD) Unit: DRAM clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:0	RO	0x0000	reserved

DDRCTL_DRAMSET1TMG13_FREQ0

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x1c	odtloff LPDDR4: ODTLoff: This is the latency from CAS-2 command to ODToff reference. Note: This register field is only applicable for designs supporting LPDDR4 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x1c Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
23	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
22:16	RW	0x20	t_ccd_mw This is the minimum time from write or masked write to masked write command for same bank. LPDDR4: tCCDMW LPDDR5(BG mode): 4*BL/n_max LPDDR5(16B mode): 4*BL/n Note: This register field is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x20 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:4	RO	0x000	reserved
3:0	RW	0x4	t_ppd LPDDR4/5: tPPD: This is the minimum time from precharge to precharge command. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG14_FREQ0

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x008	t_osco tosco: Minimum time from DQS Oscillator stop to Mode register readout. LPDDR4 : max(40ns,8nck) LPDDR5A: tOSCODQI=tOSCODQO=max(40ns,8nck) Unit: DRAM clock cycles. Value After Reset: 0x8 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:12	RO	0x0	reserved
11:0	RW	0x0a0	t_xsr tXSR: Exit Self Refresh to any command. The value 0xfff is illegal for this register field. Unit: DRAM clock cycles. Value After Reset: 0xa0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG23_FREQ0

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	t_xsr_dsm_x1024 Delay from Deep Sleep Mode Exit to SRX. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	t_pdn Minimum interval between Deep Sleep Mode Entry and Exit. Unit: DRAM clock cycles. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related

DDRCTL_DRAMSET1TMG24_FREQ0

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RW	0x0	bank_org Select Bank/ Bank group organization: 2'b00: 4 Banks/ 4 Bank groups 2'b01: 8 Banks 2'b10: 16 Banks 2'b11: Reserved Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
23:16	RW	0x0f	rd2wr_s Minimum time from read command to write command for different bank group. Includes time for bus turnaround, recovery times and all per-bank, per-rank and global constraints. LPDDR5(DQ ODT is disabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) - WL LPDDR5(DQ ODT is enabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x0f	max_rd_sync Minimum time from read command to WCK2CK sync OFF. RL + BL/n_max + RU(tRPST/tCK) Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x0f	max_wr_sync Minimum time from write command to WCK2CK sync OFF. WL + BL/n_max Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG25_FREQ0

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
18:16	RW	0x0	lpddr4_diff_bank_rwa2pre Set the timing constraint between different bank RD/WR/MWR/ACT and PRE in LPDDR4. LPDDR4 JESD209-4A requires 4 cycles LPDDR4 JESD209-4B requires 2 cycles Value of 1, 3, 5, 6, and 7 are illegal. Don't care for LPDDR5. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x00	wra2pre Time between write with AP and precharge to same bank. LPDDR4: WL + BL/2 + nWR + 1 LPDDR5: WL + BL/n_min + nWR + 1 Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x00	rda2pre Time between read with AP and precharge to same bank. LPDDR4: nRTP LPDDR5: BL/n_min + nRBTP Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG30_FREQ0

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mrr2mrw MRR to MRW delay Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:8	RW	0x00	mrr2wr MRR to WR delay Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:0	RW	0x00	mrr2rd MRR to RD delay Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR0_FREQ0

Address: **Operational Base** + offset (0x0500)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr LPDDR4: Value to write to MR1 register Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:0	RW	0x0510	emr LPDDR4: Value to write to MR2 register Value After Reset: 0x510 Volatile: True Programming Mode: Quasi-dynamic Group 4

DDRCTL_INITMR1_FREQ0

Address: **Operational Base** + offset (0x0504)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	emr2 LPDDR4: Value to write to MR3 register Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4
15:0	RW	0x0000	emr3 LPDDR4: Value to write to MR13 register Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR2_FREQ0

Address: **Operational Base** + offset (0x0508)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr4 LPDDR4: Value to be loaded into SDRAM MR11 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	mr5 LPDDR4: Value to be loaded into SDRAM MR12 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4

DDRCTL_INITMR3_FREQ0

Address: **Operational Base** + offset (0x050C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr22 LPDDR4 Value to be loaded into SDRAM MR22 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	mr6 LPDDR4 Value to be loaded into SDRAM MR14 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4

DDRCTL_DFITMG0_FREQ0

Address: **Operational Base** + offset (0x0580)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x07	dfi_t_ctrl_delay Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DRAM clock and the memory clock are not phase-aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x7 Volatile: True Programming Mode: Quasi-dynamic Group 4
23	RO	0x0	reserved
22:16	RW	0x02	dfi_t_rddata_en Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:14	RO	0x0	reserved
13:8	RW	0x00	dfi_tphy_wrdata Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. Refer to PHY specification for correct value. Note, max supported value is 8. Unit: DRAM data clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4
7:6	RO	0x0	reserved
5:0	RW	0x02	dfi_tphy_wrlat Write latency Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value. For LPDDR4, dfi_tphy_wrlat>60 is not supported. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

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DDRCTL_DFITMG1_FREQ0

Address: **Operational Base** + offset (0x0584)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	dfi_t_wrdata_delay Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. For LPDDR5, this should be set to "twck_delay + BL/n_max - BL/n_min" instead of twrdata_delay. twck_delay specifies the time from dfi_wck_en deassertion to when WCK transfer completes on the DRAM bus and is defined by the PHY Refer to PHY specification for correct value. When DDRCTL_TMGCFG_FREQ0.frequency_ratio is set to 0(1:2 Mode), divided the value by 2 and round it up to the next integer value. When DDRCTL_TMGCFG_FREQ0.frequency_ratio is set to 1(1:4 Mode), divided the value by 4 and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4
15:13	RO	0x0	reserved
12:8	RW	0x04	dfi_t_dram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 4
7:5	RO	0x0	reserved
4:0	RW	0x04	dfi_t_dram_clk_enable Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 4

DDRCTL_DFITMG2_FREQ0

Address: **Operational Base** + offset (0x0588)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

Bit	Attr	Reset Value	Description
21:16	RW	0x00	dfi_twck_delay Number of DFI PHY clock cycles from dfi_wck_en is de-asserted to when the WCK transfer completes on the DRAM bus. Refer to PHY specification for correct value. Unit: DFI PHY clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15	RO	0x0	reserved
14:8	RW	0x02	dfi_tphy_rdcslat Number of DFI PHY clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:6	RO	0x0	reserved
5:0	RW	0x02	dfi_tphy_wrcslat Number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DFITMG4_FREQ0

Address: **Operational Base** + offset (0x0590)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_en_rd WCK Enable Read Timing. Defines the timing from the CAS-WS_RD command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_en_wr WCK Enable Read Timing. Defines the timing from the CAS-WS_WR command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_en_fs WCK Enable Fast Sync Timing. Defines the timing from the CAS-WS_FS command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset: 0x0 Programming Mode: Quasi-dynamic Group 1, Group 4

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	dfi_twck_dis WCK Off Timing. Defines the timing from the last command opportunity to the deassertion of dfi_wck_en and dfi_wck_toggle_en assuming that no command is being sent. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4

DDRCTL_DFITMG5_FREQ0

Address: **Operational Base** + offset (0x0594)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_fast_toggle Defines the number of clock cycles between the dfi_wck_signal being driven to TOGGLE to when the dfi_wck_signal is driven to FAST_TOGGLE. This timing is only applicable when the WCK transitions from the slow to fast toggle. Otherwise, this timing parameter must be set to 0x0. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_toggle WCK Toggle Enable Timing. Defines the timing from dfi_wck_en assertion to dfi_wck_toggle_en assertion. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_toggle_cs Defines the number of clock cycles between a read or write command to when the dfi_wck_cs signal must be stable. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
7:0	RW	0x00	dfi_twck_toggle_post Defines the number of clock cycles after a read or write command data burst completion during which the WCK must remain in the current toggle state. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4

DDRCTL_DFILPTMG0_FREQ0

Address: **Operational Base** + offset (0x05A0)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved

Bit	Attr	Reset Value	Description
20:16	RW	0x00	dfi_lp_wakeup_dsm Indicates the value in DFI clock cycles to drive on dfi_lp_ctrl_wakeup and dfi_lp_data_wakeup signals when Deep Sleep Mode is entered. Determines the DFI's tlp_wakeup time: 5'h0: 1 cycle 5'h1: 2 cycles 5'h2: 4 cycles 5'h3: 8 cycles 5'h4: 16 cycles 5'h5: 32 cycles 5'h6: 64 cycles 5'h7: 128 cycles 5'h8: 256 cycles 5'h9: 512 cycles 5'ha: 1024 cycles 5'hb: 2048 cycles 5'hc: 4096 cycles 5'hd: 8192 cycles 5'he: 16384 cycles 5'hf: 32768 cycles 5'h10: 65536 cycles 5'h11: 131072 cycles 5'h12: 262144 cycles 5'h13: Unlimited This is only present for designs supporting LPDDR5 devices. Unit: DFI clock cycles. Value After Reset: 0x0 Programming Mode: Static
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	dfi_lp_wakeup_sr Indicates the value in DFI clock cycles to drive on dfi_lp_ctrl_wakeup and dfi_lp_data_wakeup signals when Self Refresh mode is entered. Determines the DFI's tlp_wakeup time: 5'h0: 1 cycle 5'h1: 2 cycles 5'h2: 4 cycles 5'h3: 8 cycles 5'h4: 16 cycles 5'h5: 32 cycles 5'h6: 64 cycles 5'h7: 128 cycles 5'h8: 256 cycles 5'h9: 512 cycles 5'ha: 1024 cycles 5'hb: 2048 cycles 5'hc: 4096 cycles 5'hd: 8192 cycles 5'he: 16384 cycles 5'hf: 32768 cycles 5'h10: 65536 cycles 5'h11: 131072 cycles 5'h12: 262144 cycles 5'h13: Unlimited Unit: DFI clock cycles. Value After Reset: 0x0 Programming Mode: Static
7:5	RO	0x0	reserved
4:0	RW	0x00	dfi_lp_wakeup_pd Indicates the value in DFI clock cycles to drive on dfi_lp_ctrl_wakeup and dfi_lp_data_wakeup signals when Power Down mode is entered. Determines the DFI's tlp_wakeup time: 5'h0: 1 cycle 5'h1: 2 cycles 5'h2: 4 cycles 5'h3: 8 cycles 5'h4: 16 cycles 5'h5: 32 cycles 5'h6: 64 cycles 5'h7: 128 cycles 5'h8: 256 cycles 5'h9: 512 cycles 5'ha: 1024 cycles 5'hb: 2048 cycles 5'hc: 4096 cycles 5'hd: 8192 cycles 5'he: 16384 cycles 5'hf: 32768 cycles 5'h10: 65536 cycles 5'h11: 131072 cycles 5'h12: 262144 cycles 5'h13: Unlimited Unit: DFI clock cycles. Value After Reset: 0x0

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Bit	Attr	Reset Value	Description
			Programming Mode: Static

DDRCTL_DFILPTMG1_FREQ0

Address: **Operational Base** + offset (0x05A4)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x07	dfi_tlp_resp Setting in DFI clock cycles for DFI's tlp_resp time. Same value is used for both Power Down, Self Refresh, Deep Sleep Mode and Maximum Power Saving modes. Refer to PHY databook for recommended values Unit: DFI clock cycles. Value After Reset: 0x7 Programming Mode: Static
7:5	RO	0x0	reserved
4:0	RW	0x00	dfi_lp_wakeup_data Indicates the value in DFI clock cycles to drive on dfi_lp_data_wakeup signal when data bus is idle. Determines the DFI's tlp_wakeup time: 5'h0: 1 cycle 5'h1: 2 cycles 5'h2: 4 cycles 5'h3: 8 cycles 5'h4: 16 cycles 5'h5: 32 cycles 5'h6: 64 cycles 5'h7: 128 cycles 5'h8: 256 cycles 5'h9: 512 cycles 5'ha: 1024 cycles 5'hb: 2048 cycles 5'hc: 4096 cycles 5'hd: 8192 cycles 5'he: 16384 cycles 5'hf: 32768 cycles 5'h10: 65536 cycles 5'h11: 131072 cycles 5'h12: 262144 cycles 5'h13: Unlimited Unit: DFI clock cycles. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_DFIUPDTMG0_FREQ0

Address: **Operational Base** + offset (0x05A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x040	dfi_t_ctrlup_max Specifies the maximum number of DFI clock cycles that the dfi_ctrlupd_req signal can assert. Lowest value to assign to this variable is 0x40. Unit: DFI clock cycles. Value After Reset: 0x40 Programming Mode: Static
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x003	dfi_t_ctrlup_min Specifies the minimum number of DFI clock cycles that the dfi_ctrlupd_req signal must be asserted. The DDRCTL expects the PHY to respond within this time. If the PHY does not respond, the DDRCTL will de-assert dfi_ctrlupd_req after dfi_t_ctrlup_min + 2 cycles. Lowest value to assign to this variable is 0x1. Unit: DFI clock cycles. Value After Reset: 0x3 Programming Mode: Static

DDRCTL_DFIUPDTMG1_FREQ0

Address: **Operational Base** + offset (0x05AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x01	dfi_t_ctrlupd_interval_min_x1024 This is the minimum amount of time between DDRCTL initiated DFI update requests (which is executed whenever the DDRCTL is idle). Set this number higher to reduce the frequency of update requests, which can have a small impact on the latency of the first read request when the DDRCTL is idle. Minimum allowed value for this field is 1. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x01 Programming Mode: Static
15:8	RO	0x00	reserved
7:0	RW	0x01	dfi_t_ctrlupd_interval_max_x1024 This is the maximum amount of time between DDRCTL initiated DFI update requests. This timer resets with each update request; when the timer expires dfi_ctrlupd_req is sent and traffic is blocked until the dfi_ctrlupd_ackx is received. PHY can use this idle time to recalibrate the delay lines to the DLLs. The DFI controller update is also used to reset PHY FIFO pointers in case of data capture errors. Updates are required to maintain calibration over PVT, but frequent updates may impact performance. Minimum allowed value for this field is 1. Note: Value programmed for dfi_t_ctrlupd_interval_max_x1024 must be greater than dfi_t_ctrlupd_interval_min_x1024. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x01 Programming Mode: Static

DDRCTL_DFIMSGTMG0_FREQ0

Address: **Operational Base** + offset (0x05B0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x04	dfi_t_ctrlmsg_resp This is the maximum amount in DFI clock cycles between the assertion of the dfi{0/1}_ctrlmsg_req signal to the assertion of the dfi{0/1}_ctrlmsg_ack signal. If the PHY does not acknowledge the request within dfi_t_ctrlmsg_resp cycles, the PHY must not acknowledge the request at all. In this case, the controller should de-assert the corresponding dfi{0/1}_ctrlmsg_req signal. The timing values might vary based on the frequency ratio and user must reprogram if there is any change in the frequency ratio. Refer to PHY databook for recommended values Unit: DFI clock cycles. Value After Reset: 0x4 Programming Mode: Static

DDRCTL_RFSHSET1TMG0_FREQ0

Address: **Operational Base** + offset (0x0600)

Bit	Attr	Reset Value	Description
31	RW	0x0	t_refi_x1_sel Specifies whether DDRCTL_RFSHSET1TMG0_FREQ0.t_refi_x1_x32 and DDRCTL_RFSHSET1TMG0_FREQ0.refresh_to_x1_x32 register values are x1 or x32. 1'b0: x32 register values are used. 1'b1: Register values are used. This applies only when per-bank refresh is enabled (DDRCTL_RFSHMOD0.per_bank_refresh=1). If per-bank refresh is not enabled, the x32 register values are used and this register field is ignored. This register field does not exist for configurations which do not support LPDDR4/5. For such configurations, the value of this register field can be assumed to be 0, so that DDRCTL_RFSHSET1TMG0_FREQ0.t_refi_x1_x32 and DDRCTL_RFSHSET1TMG0_FREQ0.refresh_to_x1_x32 are interpreted as x32 register fields Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related
30:28	RO	0x0	reserved
27:24	RW	0x2	refresh_margin Threshold value in number of DRAM clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_refi/32. Note that internally used t_refi is equal to DDRCTL_RFSHSET1TMG0_FREQ0.t_refi_x1_x32 * 32 if DDRCTL_RFSHSET1TMG0_FREQ0.t_refi_x1_sel = 0. If DDRCTL_RFSHSET1TMG0_FREQ0.t_refi_x1_sel = 1, internally used t_refi is equal to DDRCTL_RFSHSET1TMG0_FREQ0.t_refi_x1_x32. Note that, internally used t_refi may be divided by four if derating or TCR is enabled. Unit: Multiples of 32 DRAM clock cycles. Value After Reset: 0x2 Programming Mode: Dynamic - Refresh Related
23:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:16	RW	0x10	refresh_to_x1_x32 If the refresh timer has expired at least once (i.e. >tREFI period elapses, and there are postponed refreshes), then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful. When there are no transactions pending in the CAM for a period of time determined by this DDRCTL_RFSHSET1TMG0_FREQ0.refresh_to_x1_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the DDRCTL. This is also used for non speculative refresh when LPDDR per-bank refresh (REFpb) is enabled. The controller observes the period of time determined by this for each bank, and a priority of bank address is determined. This should be programmed to tREFI based value in controller's current refresh mode. The controller calculates this according to current refresh mode. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on DDRCTL_RFSHSET1TMG0_FREQ0.t_refi_x1_sel. Value After Reset: 0x10 Programming Mode: Dynamic - Refresh Related
15:12	RO	0x0	reserved
11:0	RW	0x062	t_refi_x1_x32 Average time interval between refreshes per rank (See JEDEC specification for LPDDR4). Set this register to RoundDown(tREFI/tCK). If DDRCTL_RFSHSET1TMG0_FREQ0.t_refi_x1_sel = 0, divide the above result by 32 and round down. For LPDDR controller: If using all-bank refreshes (DDRCTL_RFSHMOD0.per_bank_refresh = 0), use tREFIab in the above calculations. If using per-bank refreshes (DDRCTL_RFSHMOD0.per_bank_refresh = 1), use tREFIpb in the above calculations. Note that: DDRCTL_RFSHSET1TMG0_FREQ0.t_refi_x1_x32 must be greater than 0x1. If DDRCTL_RFSHSET1TMG0_FREQ0.t_refi_x1_sel == 1, DDRCTL_RFSHSET1TMG0_FREQ0.t_refi_x1_x32 must be greater than DDRCTL_RFSHSET1TMG1_FREQ0.t_rfc_min If DDRCTL_RFSHSET1TMG0_FREQ0.t_refi_x1_sel == 0, DDRCTL_RFSHSET1TMG0_FREQ0.t_refi_x1_x32 * 32 must be greater than DDRCTL_RFSHSET1TMG1_FREQ0.t_rfc_min DDRCTL_RFSHSET1TMG0_FREQ0.t_refi_x1_x32 must be less than or equal to 0xFFE. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on DDRCTL_RFSHSET1TMG0_FREQ0.t_refi_x1_sel. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to

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Bit	Attr	Reset Value	Description
			program this register field. Value After Reset: 0x62 Programming Mode: Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG1_FREQ0

Address: **Operational Base** + offset (0x0604)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x08c	t_rfc_min tRFC (min): Minimum time from refresh to refresh or activate. t_rfc_min must be set to RoundUp(tRFCmin/tCK). In LPDDR controller, if using all-bank refreshes, the tRFCmin value in the above equations is equal to tRFCab. If using per-bank refreshes, the tRFCmin value in the above equations is equal to tRFCpb. Unit: DRAM clock cycles. Value After Reset: 0x8c Programming Mode: Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG2_FREQ0

Address: **Operational Base** + offset (0x0608)

Bit	Attr	Reset Value	Description
31:24	RW	0x8c	t_pbr2act Time from REFpb to activate command to different bank than REFpb. LPDDR5: tpbr2act Value After Reset: 0x8c Programming Mode: Dynamic - Refresh Related
23:16	RW	0x8c	t_pbr2pbr LPDDR4: tpbR2pbR Per-bank Refresh to Per-bank refresh different bank Time. Program this to RoundUp(tpbR2pbR/tCK). The tpbR2pbR value in the above equations is different depending on the device density. The user must program the appropriate value from the spec. Register is valid only in LPDDR4 per-bank refresh mode (DDRCTL_RFSHMOD0.per_bank_refresh == 1). Value After Reset: 0x8c Programming Mode: Dynamic - Refresh Related
15:0	RO	0x0000	reserved

DDRCTL_RFSHSET1TMG4_FREQ0

Address: **Operational Base** + offset (0x0610)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x000	refresh_timer1_start_value_x32 Refresh timer start for rank 1 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related
15:12	RO	0x0	reserved
11:0	RW	0x000	refresh_timer0_start_value_x32 Refresh timer start for rank 0 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related

DDRCTL_ZQSET1TMG0_FREQ0

Address: **Operational Base** + offset (0x0800)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x040	t_zq_short_nop tZQLAT for LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset: 0x40 Programming Mode: Static
15:14	RO	0x0	reserved
13:0	RW	0x0200	t_zq_long_nop tZQCAL for LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM. If using LPDDR5, this register needs to be programmed to tZQCAL + 10 cycles. Unit: DRAM clock cycles. Value After Reset: 0x200 Programming Mode: Static

DDRCTL_ZQSET1TMG1_FREQ0

Address: **Operational Base** + offset (0x0804)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:20	RW	0x020	t_zq_reset_nop tZQReset: Number of DRAM clock cycles of NOP required after a ZQReset (ZQ calibration Reset) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset: 0x20 Programming Mode: Static
19:0	RW	0x00100	t_zq_short_interval_x1024 Average interval to wait between automatically issuing ZQCS (ZQ calibration short)/MPC(ZQ calibration) commands to LPDDR4 devices. Meaningless, if DDRCTL_ZQCTL0.dis_auto_zq=1. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x100 Programming Mode: Static

DDRCTL_DQSOSCCTL0_FREQ0

Address: **Operational Base** + offset (0x0A80)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RW	0x007	dqsosc_interval DQS Oscillator interval, specifies the time between two DQS oscillator sequences. Minimum programmable value is 1. The value can be changed while DQSOSCCTL0.dqsosc_enable=0 Unit: DFI clock cycles Value After Reset: 0x7 Programming Mode: Dynamic
3	RO	0x0	reserved
2	RW	0x0	dqsosc_interval_unit DQS/WCK Oscillator Interval unit. Specifies the unit for counting DQS oscillator interval. The value can be changed while DQSOSCCTL0.dqsosc_enable=0 1'b1: x2K DFI clock cycles 1'b0: x32K DFI clock cycles Value After Reset: 0x0 Programming Mode: Dynamic
1	RO	0x0	reserved
0	RW	0x0	dqsosc_enable DQS/WCK Oscillator Enable 1'b1: Enable DQS Oscillator 1'b0: Disable DQS Oscillator Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_DERATEINT_FREQ0

Address: **Operational Base** + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00800000	mr4_read_interval Interval between two MR4 reads, used to derate the timing parameters. This register must not be set to zero. Unit: DRAM clock cycles. Value After Reset: 0x800000 Volatile: True

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Bit	Attr	Reset Value	Description
			Programming Mode: Static

DDRCTL_DERATEVAL0_FREQ0

Address: **Operational Base** + offset (0x0B04)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	derated_t_rcd Derated value for tRCD. For LPDDR4, the required period with derating is tRCD + 1.875ns For LPDDR5, the required period with derating is tRCD + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
23:16	RW	0x0f	derated_t_ras_min Derated value for tRAS. For LPDDR4, the required period with derating is tRAS + 1.875ns For LPDDR5, the required period with derating is tRAS + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15	RO	0x0	reserved
14:8	RW	0x05	derated_t_rp Derated value for tRP. For LPDDR4, the required period with derating is tRP + 1.875ns For LPDDR5, the required period with derating is tRP + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:6	RO	0x0	reserved
5:0	RW	0x04	derated_t_rrd Derated value for tRRD. For LPDDR4, the required period with derating is tRRD + 1.875ns For LPDDR5, the required period with derating is tRRD + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DERATEVAL1_FREQ0

Address: **Operational Base** + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x14	derated_t_rc Derated value for tRC. For LPDDR4, the required period with derating is tRC + 3.75ns For LPDDR5, the required period with derating is tRC + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x14 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_HWLPTMG0_FREQ0

Address: **Operational Base** + offset (0x0B80)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_lp_idle_x32 Hardware idle period. The cactive_ddrc output is driven low if the DDRC command channel is idle for hw_lp_idle * 32 cycles if not in INIT or DPD/MPSM operating_mode. The DDRC command channel is considered idle when there are no HIF commands outstanding. The hardware idle function is disabled when hw_lp_idle_x32=0. hw_lp_idle_x32=1 is an illegal value when the controller is in 1:2 mode. hw_lp_idle_x32=1/2/3 are illegal values when the controller is in 1:4 mode. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Volatile: True Programming Mode: Static
15:0	RO	0x0000	reserved

DDRCTL_SCHEDTMG0_FREQ0

Address: **Operational Base** + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x00	rdwr_idle_gap When the preferred transaction store is empty for these many clock cycles, switch to the alternate transaction store if it is non-empty. The read transaction store (both high and low priority) is the default preferred transaction store and the write transaction store is the alternative store. When prefer write over read is set this is reversed. 0x0 is a legal value for this register. When set to 0x0, the transaction store switching will happen immediately when the switching conditions become true. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x0 Programming Mode: Static

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	pageclose_timer This field works in conjunction with DDRCTL_SCHED0.pageclose. It only has meaning if DDRCTL_SCHED0.pageclose==1. If DDRCTL_SCHED0.pageclose==1 and pageclose_timer==0, then an auto-precharge may be scheduled for last read or write command in the CAM with a bank and page hit. Note, sometimes an explicit precharge is scheduled instead of the auto-precharge. See DDRCTL_SCHED0.pageclose for details of when this may happen. If DDRCTL_SCHED0.pageclose==1 and pageclose_timer>0, then an auto-precharge is not scheduled for last read or write command in the CAM with a bank and page hit. Instead, a timer is started, with pageclose_timer as the initial value. There is a timer on a per bank basis. The timer decrements unless the next read or write in the CAM to a bank is a page hit. It gets reset to pageclose_timer value if the next read or write in the CAM to a bank is a page hit. Once the timer has reached zero, an explcit precharge will be attempted to be scheduled. Unit: DRAM clock cycles. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_PERFHPR1_FREQ0

Address: **Operational Base** + offset (0x0C80)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	hpr_xact_run_length Number of transactions that are serviced once the HPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available Unit: Transaction FOR PERFORMANCE ONLY. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x00	reserved
15:0	RW	0x0001	hpr_max_starve Number of DRAM clocks that the HPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x1 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PERFLPR1_FREQ0

Address: **Operational Base** + offset (0x0C84)

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Bit	Attr	Reset Value	Description
31:24	RW	0x0f	lpr_xact_run_length Number of transactions that are serviced once the LPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available Unit: Transaction FOR PERFORMANCE ONLY. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x00	reserved
15:0	RW	0x007f	lpr_max_starve Number of DRAM clocks that the LPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x7f Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PERFWR1_FREQ0

Address: **Operational Base** + offset (0x0C88)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	w_xact_run_length Number of transactions that are serviced once the WR queue goes critical is the smaller of: (a) This number (b) Number of transactions available Unit: Transaction FOR PERFORMANCE ONLY. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x00	reserved
15:0	RW	0x007f	w_max_starve Number of DRAM clocks that the WR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x7f Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_TMGCFG_FREQ0

Address: **Operational Base** + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	dfi_freq_fsp This register value propergates to dfi_freq_fsp pin directly. Value After Reset: 0x0 Programming Mode: Dynamic
7:1	RO	0x00	reserved
0	RW	0x0	frequency_ratio Selects the Frequency Ratio For LPDDR4: 1'b0: 1:2 Mode 1'b1: 1:4 Mode For LPDDR5: 1'b0: 1:1:2 Mode 1'b1: 1:1:4 Mode Value After Reset: 0x0 Programming Mode: Quasi-dynamic Group 2

DDRCTL_RANKTMG0_FREQ0

Address: **Operational Base** + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x06	diff_rank_wr_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_wrcsgap (see PHY databook for value of tphy_wrcsgap) If CRC feature is enabled, must be increased by 1. Write preamble is always set to 2tCK for LPDDR4, refer to PHY databook to see if this is already factored into tphy_wrcsgap value or if it needs to be increased by 1. If write postamble is set to 1.5tCK(LPDDR4 only), must be increased by 1. ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, with DQ ODT enabled, diff_rank_wr_gap must be a minimum of ODTLoff - ODTLon - BL/2 + 1 For other cases, diff_rank_wr_gap must be a minimum of ODTCFG.wr_odt_hold - BL/2. Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay". Please see PHY databook for the value of tphy_wckcsgap. Unit: DRAM clock cycles. Value After Reset: 0x6 Volatile: True Programming Mode: Quasi-dynamic Group 2

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Bit	Attr	Reset Value	Description
7:0	RW	0x06	diff_rank_rd_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_rdcsgap (see PHY databook for value of tphy_rdcsgap) ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads: Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay". Please see PHY databook for the value of tphy_wckcsgap. Unit: DRAM clock cycles. Value After Reset: 0x6 Volatile: True Programming Mode: Quasi-dynamic Group 2

DDRCTL_RANKTMG1_FREQ0

Address: **Operational Base** + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x0f	rd2wr_dr Minimum time from read command to write command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. The value must be larger than or equal to the value of DRAMSET1TMG2.rd2wr. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay". Please see PHY databook for the value of tphy_wckcsgap. Unit: DRAM clock cycles Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x0f	wr2rd_dr Minimum time from write command to read command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay". Please see PHY databook for the value of tphy_wckcsgap. Unit: DRAM clock cycles Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_PWRTMG_FREQ0

Address: **Operational Base** + offset (0x0D0C)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x040	selfref_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into Self Refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x40 Volatile: True Programming Mode: Quasi-dynamic Group 4
15:7	RO	0x000	reserved
6:0	RW	0x10	powerdown_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into power-down. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x10 Volatile: True Programming Mode: Quasi-dynamic Group 4

DDRCTL_MSTR0

Address: **Operational Base** + offset (0x10000)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RW	0x3	active_ranks Only present for multi-rank configurations. Each bit represents one rank. For two-rank configurations, only bits[25:24] are present. 1'b1: Populated 1'b0: Unpopulated LSB is the lowest rank number. For 2 ranks following combinations are legal: 2'b01: One rank 2'b11: Two ranks Others: Reserved. For 4 ranks following combinations are legal: 4'b0001: One rank 4'b0011: Two ranks 4'b1111: Four ranks Others: Reserved Note: the four rank populated Configure4'b0101 can only be supported with heterogenous rank support enable. Value After Reset: 0x3 Programming Mode: Static
23:21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20:16	RW	0x04	burst_rdwr SDRAM burst length used: 5'b00100: Burst length of 8 5'b01000: Burst length of 16 All other values are reserved. This controls the burst size used to access the SDRAM. This must match the burst length mode register setting in the SDRAM. For LPDDR4/LPDDR5, this must be set to 0x01000 (BL16). Value After Reset: 0x4 Programming Mode: Static
15:14	RO	0x0	reserved
13:12	RW	0x0	data_bus_width Selects proportion of DQ bus width that is used by the SDRAM. 2'b00: Full DQ bus width to SDRAM 2'b01: Half DQ bus width to SDRAM 2'b10: Quarter DQ bus width to SDRAM 2'b11: Reserved Note that half bus width mode is only supported when the SDRAM bus width is a multiple of 16, and quarter bus width mode is only supported when the SDRAM bus width is a multiple of 32 and the configuration parameter MEMC_QBUS_SUPPORT is set. Bus width refers to DQ bus width (excluding any ECC width). Value After Reset: 0x0 Programming Mode: Static
11:4	RO	0x00	reserved
3	RW	0x0	lpddr5 Select LPDDR5 SDRAM 1'b1: LPDDR5 SDRAM device in use. 1'b0: Non-LPDDR5 device in use. Present only in designs configured to support LPDDR5 SDRAM memories. Value After Reset: 0x0 Programming Mode: Static
2	RO	0x0	reserved
1	RW	0x0	lpddr4 Select LPDDR4 SDRAM 1'b1: LPDDR4 SDRAM device in use. 1'b0: Non-LPDDR4 device in use. Present only in designs configured to support LPDDR4 SDRAM memories. Value After Reset: 0x0 Programming Mode: Static
0	RO	0x0	reserved

DDRCTL_MSTR2

Address: **Operational Base** + offset (0x10008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	target_frequency This field specifies the target frequency. 2'b00: Frequency 0/Normal 2'b01: Frequency 1/FREQ1 2'b10: Frequency 2/FREQ2 2'b11: Frequency 3/FREQ3 All other values are reserved. Note: If the target frequency can be changed through Hardware Low Power Interface only, this field is not needed. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2

DDRCTL_MSTR4

Address: **Operational Base** + offset (0x10010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	wck_on WCK always on mode 1'b0: WCK always on mode disabled 1'b1: WCK always on mode enabled In case of multi-rank system, the controller issues CAS-WS_FS to all ranks to sets DRAM in sync state simultaneously. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2

DDRCTL_STAT

Address: **Operational Base** + offset (0x10014)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	selfref_cam_not_empty Self refresh with CAMs not empty. Set to 1 when Self Refresh is entered but CAMs are not drained. Cleared after exiting Self Refresh. Value After Reset: 0x0 Programming Mode: Static
15	RO	0x0	reserved
14:12	RO	0x0	selfref_state Self refresh state. This indicates self refresh or self refresh power down state or Deep Sleep Mode (LPDDR5 only). This register is used for frequency change and MRR/MRW access during self refresh. 3'b000: SDRAM is not in Self Refresh. 3'b001: Self refresh 1 3'b010: Self refresh power down 3'b011: Self refresh 2 3'b100: Deep Sleep Mode (LPDDR5 only) Value After Reset: 0x0 Programming Mode: Static
11:6	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
5:4	RO	0x0	selfref_type Flags if Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5) is entered and if it was under Automatic Self Refresh control only or not. 2'b00: SDRAM is not in Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5). 2'b11: SDRAM is in Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5), which was caused by Automatic Self Refresh only. If retry is enabled, this guarantees SRE command is executed correctly without parity error. 2'b10: SDRAM is in Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5), which was not caused solely under Automatic Self Refresh control. It could have been caused by Hardware Low Power Interface and/or Software (DDRCTL_PWRCTL.selfref_sw). If retry is enabled, this guarantees SRE command is executed correctly without parity error. 2'b01: SDRAM is in Self Refresh, which was caused by PHY Master Request. For LPDDR54, only bit[5:4] are used. Bit[5:4]: Rank 0 selfref_type Bit[7:6]: Rank 1 selfref_type Bit[9:8]: Rank 2 selfref_type Bit[11:10]: Rank 3 selfref_type Value After Reset: 0x0 Programming Mode: Static
3	RO	0x0	reserved
2:0	RO	0x0	operating_mode Operating mode LPDDR4/LPDDR5designs: 3'b000: Init 3'b001: Normal 3'b010: Power-down 3'b011: Self refresh/Self refresh power-down Value After Reset: 0x0 Programming Mode: Static

DDRCTL_MRCTRL0

Address: **Operational Base** + offset (0x10080)

Bit	Attr	Reset Value	Description
31	RW	0x0	mr_wr Setting this register bit to 1 triggers a mode register read or write operation. When the MR operation is complete, the DDRCTL automatically clears this bit. The other register fields of this register must be written in a separate APB transaction, before setting this mr_wr bit. It is recommended NOT to set this signal if in Init, Deep power-down or MPSM operating modes. Value After Reset: 0x0 Testable: Read only Programming Mode: Dynamic
30:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24	RW	0x0	mrr_done_clr If this bit is set, mrr_done will be cleared by the controller. Value After Reset: 0x0 Testable: Read only Programming Mode: Dynamic
23:16	RO	0x00	reserved
15:12	RW	0x0	mr_addr Address of the mode register that is to be written to. 4'b0000: MR0 4'b0001: MR1 4'b0010: MR2 4'b0011: MR3 4'b0100: MR4 4'b0101: MR5 4'b0110: MR6 4'b0111: MR7 Don't Care for LPDDR4/5 (see DDRCTL_MRCTRL1.mr_data for mode register addressing in LPDDR4/5). Value After Reset: 0x0 Programming Mode: Dynamic
11:6	RO	0x00	reserved
5:4	RW	0x3	mr_rank Controls which rank is accessed by MRCTRL0.mr_wr. Normally, it is desired to access all ranks, so all bits must be set to 1. Examples (assume DDRCTL is configured for 4 ranks): 4'h1: select rank 0 only 4'h2: select rank 1 only 4'h5: select ranks 0 and 2 4'hA: select ranks 1 and 3 4'hF: select ranks 0, 1, 2 and 3 Value After Reset: 0x3 Programming Mode: Dynamic
3	RW	0x0	sw_init_int Indicates whether Software intervention is allowed via DDRCTL_MRCTRL0/MRCTRL1 before automatic SDRAM initialization routine or not. For LPDDR4/5, this bit can be used to program additional mode registers before automatic SDRAM initialization if necessary. In LPDDR4 dual channel mode, note that this must be programmed to both channels beforehand. Note that this must be cleared to 0 after completing Software operation. Otherwise, SDRAM initialization routine will not re-start. 1'b0: Software intervention is not allowed. 1'b1: Software intervention is allowed. Value After Reset: 0x0 Programming Mode: Dynamic
2:1	RO	0x0	reserved
0	RW	0x0	mr_type Indicates whether the mode register operation is read or write. 1'b0: Write 1'b1: Read Only used for LPDDR4/LPDDR5. Value After Reset: 0x0 Programming Mode: Dynamic

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DDRCTL_MRCTRL1

Address: **Operational Base** + offset (0x10084)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	mr_data For LPDDR4/5, MRCTRL1[15:0] are interpreted as [15:8] MR Address [7:0] MR data for writes, don't care for read. This is 16-bits for the LPDDR5/4 controller. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_MRSTAT

Address: **Operational Base** + offset (0x10090)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	mrr_done This signal goes high when the controller received MRR data which is triggered by DDRCTL_MRCTRL0.mr_wr. This signal is cleared by mrr_done_clr Value After Reset: 0x0 Programming Mode: Dynamic
15:1	RO	0x0000	reserved
0	RO	0x0	mr_wr_busy The SoC core may initiate a MR write operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the MRW/MRR request. It goes low when the MRW/MRR command is issued to the SDRAM. It is recommended not to perform MRW/MRR commands when 'MRSTAT.mr_wr_busy' is high. 1'b0: Indicates that the SoC core can initiate a mode register write operation. 1'b1: Indicates that mode register write operation is in progress. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_MRRDATA0

Address: **Operational Base** + offset (0x10094)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data_lwr MRR data for DQ[31:0] This register is updated when the controller issued MRR command triggered by DDRCTL_MRCTRL register. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_MRRDATA1

Address: **Operational Base** + offset (0x10098)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data_upr MRR data for DQ[63:32] This register is updated when the controller issued MRR command triggered by DDRCTL_MRCTRL register. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_DERATECTL0

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Address: **Operational Base** + offset (0x10100)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x1	dis_trefi_x0125 Disables 0.125 x tREFI refresh rate for derating. When this register filed is set to 1, controller behaves like 0.25 x tREFI refresh rate mode although in 0.125 x tREFI refresh rate mode. And controller asserts interrupt signal "derate_temp_limit_intr" when receives MR4 OP[4:0] = 01110 or 01111. 1'b0: Enable 0.125 x tREFI refresh rate 1'b1: Disable 0.125 x tREFI refresh rate Note: This register field is only applicable for designs supporting LPDDR5 SDRAM. This register bit is required to set 1 if per-bank refresh "DDRCTL_RFSHMOD0.per_bank_refresh=1" and derating "DDRCTL_DERATECTL0.derate_enable=1" are enabled. Value After Reset: 0x1 Programming Mode: Static
3	RW	0x1	dis_trefi_x6x8 Disables 8x tREFI and 6x tREFI refresh rate for derating.When this register filed is set to 1, controller behaves like 4x tREFI refresh rate mode even though in 8x tREFI and 6x tREFI mode. 1'b0: Enable 6x tREFI and 8x tREFI refresh rate 1'b1: Disable 6x tREFI and 8x tREFI refresh rate Note: This register field is only applicable for designs supporting LPDDR5 SDRAM. This register bit is required to set 1 if LPDDR5 is used. Value After Reset: 0x1 Programming Mode: Dynamic - Refresh Related
2	RW	0x0	derate_mr4_pause_fc Pauses automatic MRR to MR4. For more details, see description of DDRCTL_DERATECTL0.derate_enable. Value After Reset: 0x0 Programming Mode: Dynamic
1	RW	0x0	lpddr4_refresh_mode Selects the LPDDR4 refresh mode 1'b0: Legacy refresh mode 1'b1: Modified refresh mode (Unsupported) Value After Reset: 0x0 Programming Mode: Static
0	RW	0x0	derate_enable Enables derating 1'b0: Timing parameter derating is disabled. 1'b1: Timing parameter derating is enabled using MR4 read value. Note that, once DDRCTL_DERATECTL0.derate_enable is set to 1, it has to keep 1. Otherwise, the refresh rate and other timing parameters revert to their nominal values. To stop automatic MRR to MR4 temporarily after setting DDRCTL_DERATECTL0.derate_enable =1, DDRCTL_DERATECTL0.derate_mr4_pause_fc needs to be set to 1 without changing DDRCTL_DERATECTL0.derate_enable. Setting DDRCTL_DERATECTL0.derate_mr4_pause_fc=0 without changing DDRCTL_DERATECTL0.derate_enable restarts automatic MRR to MR4. Value After Reset: 0x0 Programming Mode: Dynamic

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DDRCTL_DERATECTL1

Address: **Operational Base** + offset (0x10104)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	active_derate_byte_rank0 Indicates which byte of the MRR data is used for derating in rank0. The each bit corresponds each byte. If the multiple register bits are enabled, controller compares refresh rate of the corresponding devices and chooses the worst refresh rate among them This register only supports LPDDR4 and LPDDR5. For LPDDR4 and LPDDR5: Valid width is MEMC_DRAM_DATA_WIDTH/8. This bit[n]=1 means that DQ[8*n+:8] is valid MRR data. All "0"s is invalid, if DDRCTL_DERATECTL0.derate_enable=1. Device DQ width is based on DDRCTL_MSTR0.device_Configureregister value. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_DERATECTL2

Address: **Operational Base** + offset (0x10108)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	active_derate_byte_rank1 Indicates which byte of the MRR data is used for derating in rank1. The each bit corresponds each byte. If the multiple register bits are enabled, controller compares refresh rate of the corresponding devices and chooses the worst refresh rate among them. This register only supports LPDDR4, LPDDR5. For LPDDR4 and LPDDR5: Valid width is MEMC_DRAM_DATA_WIDTH/8. This bit[n]=1 means that DQ[8*n+:8] is valid MRR data. All "0"s is invalid, if DDRCTL_DERATECTL0.derate_enable=1. Device DQ width is based on DDRCTL_MSTR0.device_Configureregister value. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_DERATECTL5

Address: **Operational Base** + offset (0x10114)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	derate_temp_limit_intr_force Interrupt force bit for derate_temp_limit_intr. Setting this register to 1 will cause the derate_temp_limit_intr output pin to be asserted. At the end of the interrupt force operation, the DDRCTL automatically clears this bit. Value After Reset: 0x0 Testable: Read only Programming Mode: Dynamic

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Bit	Attr	Reset Value	Description
1	RW	0x0	derate_temp_limit_intr_clr Interrupt clear bit for derate_temp_limit_intr. At the end of the interrupt clear operation, the DDRCTL automatically clears this bit. Value After Reset: 0x0 Testable: Read only Programming Mode: Dynamic
0	RW	0x1	derate_temp_limit_intr_en Interrupt enable bit for derate_temp_limit_intr output pin. 1'b1: Enabled 1'b0: Disabled Value After Reset: 0x1 Programming Mode: Dynamic

DDRCTL_DERATECTL6

Address: **Operational Base** + offset (0x10118)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	derate_mr4_tuf_dis Disable use of MR4 TUF flag (MR4[7]) bit. 1'b0: Use MR4 TUF flag (MR4[7]) 1'b1: Do not use MR4 TUF Flag (MR4[7]) It is recommended to set this register to 1. This affects both the periodic refresh rate update and asserting interrupt signal derate_temp_limit_intr. (i.e. In derate_mr4_tuf_dis==1, the contoller can update the refresh rate, and assert the derate_temp_limit_intr if it exceeds the thresholds irrespective of tha value of TUF flag.) Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DERATESTAT0

Address: **Operational Base** + offset (0x1011C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	derate_temp_limit_intr Derate temperature interrupt indicating SDRAM temperature operating limit is exceeded. In LPDDR4, this register field is set to 1 when the value read from MR4[2:0] is 3'b000 or 3'b111. In LPDDR5, this register field is set to 1 when the value read from MR4[4:0] is 5'b00000 or 5'b11111 or invalid value. Cleared by register DDRCTL_DERATECTL1.derate_temp_limit_intr_clr. Value After Reset: 0x0 Testable: Read only Programming Mode: Static

DDRCTL_DERATEDBGCTL

Address: **Operational Base** + offset (0x10124)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	dbg_mr4_rank_sel MR4 rank select in case of multi ranks Value After Reset: 0x0 Programming Mode: Static
3	RO	0x0	reserved
2:0	RW	0x0	dbg_mr4_grp_sel MR4 data group select based on 4 device MRR read data Value After Reset: 0x0 Programming Mode: Static

DDRCTL_DERATEDBGSTAT

Address: **Operational Base** + offset (0x10128)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	dbg_mr4_byte3 Byte 3 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5, it is occurred only if derating is enabled (DDRCTL_DERATECTL0.derate_enable=1). Value After Reset: 0x0 Programming Mode: Dynamic
23:16	RO	0x00	dbg_mr4_byte2 Byte 2 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5, it is occurred only if derating is enabled (DDRCTL_DERATECTL0.derate_enable=1). Value After Reset: 0x0 Programming Mode: Dynamic
15:8	RO	0x00	dbg_mr4_byte1 Byte 1 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5, it is occurred only if derating is enabled (DDRCTL_DERATECTL0.derate_enable=1). Value After Reset: 0x0 Programming Mode: Dynamic
7:0	RO	0x00	dbg_mr4_byte0 Byte 0 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5, it is occurred only if derating is enabled (DDRCTL_DERATECTL0.derate_enable=1). Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_PWRCTL

Address: **Operational Base** + offset (0x10180)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
18	RW	0x0	dsm_en A value of 1 to this register causes system to move to Deep Sleep Mode state immediately. 1'b1: Entry to Deep Sleep Mode 1'b0: Exit from Deep Sleep Mode Value After Reset: 0x0 Programming Mode: Dynamic
17	RW	0x0	lpddr4_sr_allowed Indicates whether transition from SR-PD to SR and back to SR-PD is allowed. This register field cannot be modified while DDRCTL_PWRCTL.selfref_sw==1. 1'b0: SR-PD -> SR -> SR-PD not allowed 1'b1: SR-PD -> SR -> SR-PD allowed Value After Reset: 0x0 Programming Mode: Dynamic
16	RW	0x0	dis_cam_drain_selfref Indicates whether skipping CAM draining is allowed when entering Self-Refresh. This register field cannot be modified while PWRCTL.selfref_sw==1. 1'b0: CAMs must be empty before entering SR 1'b1: CAMs are not emptied before entering SR (unsupported) Note, DDRCTL_PWRCTL.dis_cam_drain_selfref=1 is unsupported in this release. DDRCTL_PWRCTL.dis_cam_drain_selfref=0 is required. Value After Reset: 0x0 Programming Mode: Dynamic
15	RW	0x0	stay_in_selfref Self refresh state is an intermediate state to enter to Self refresh power down state or exit Self refresh power down state for LPDDR4/5. This register controls transition from the Self refresh state. 1'b1: Prohibit transition from Self refresh state 1'b0: Allow transition from Self refresh state Value After Reset: 0x0 Programming Mode: Dynamic
14:12	RO	0x0	reserved
11	RW	0x0	selfref_sw A value of 1 to this register causes system to move to Self Refresh state immediately, as long as it is not in INIT or DPD/MPSM operating mode. This is referred to as Software Entry/Exit to Self Refresh. 1'b1: Software Entry to Self Refresh 1'b0: Software Exit from Self Refresh Value After Reset: 0x0 Programming Mode: Dynamic
10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	en_dfi_dram_clk_disable Enable the assertion of dfi_dram_clk_disable whenever a clock is not required by the SDRAM. If set to 0, dfi_dram_clk_disable is never asserted. Assertion of dfi_dram_clk_disable is as follows. In LPDDR4, can be asserted (1)In Self Refresh Power Down (2)In Power Down (3)During Normal operation (Clock Stop) Value After Reset: 0x0 Programming Mode: Dynamic
8:5	RO	0x0	reserved
4	RW	0x0	powerdown_en If true then the DDRCTL goes into power-down after a programmable number of cycles "maximum idle clocks before power down" (DDRCTL_PWRTMG_FREQn.powerdown_to_x32,n=0, 1, 2 and 3). This register bit may be re-programmed during the course of normal operation. For LPDDR4/5, only bit[4] is used. Bit[4]: Rank 0 powerdown_en Bit[5]: Rank 1 powerdown_en Bit[6]: Rank 2 powerdown_en Bit[7]: Rank 3 powerdown_en Value After Reset: 0x0 Programming Mode: Dynamic
3:1	RO	0x0	reserved
0	RW	0x0	selfref_en If true then the DDRCTL puts the SDRAM per rank into Self Refresh after a programmable number of cycles "maximum idle clocks before Self Refresh (DDRCTL_PWRTMG_FREQn.selfref_to_x32,n=0, 1, 2 and 3)". This register bit may be re-programmed during the course of normal operation. For LPDDR4/5, only bit[0] is used. Bit[0]: Rank 0 selfref_en Bit[1]: Rank 1 selfref_en Bit[2]: Rank 2 selfref_en Bit[3]: Rank 3 selfref_en Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_HWLPCTL

Address: **Operational Base** + offset (0x10184)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x1	hw_lp_exit_idle_en When this bit is programmed to 1 the cactive_in_ddrc pin of the DDRC can be used to exit from the automatic clock stop, automatic power down or automatic self-refresh modes. Note, it will not cause exit of Self-Refresh that was caused by Hardware Low Power Interface and/or Software (DDRCTL_PWRCTL.selfref_sw). Value After Reset: 0x1 Testable: Read only Programming Mode: Static

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Bit	Attr	Reset Value	Description
0	RW	0x1	hw_lp_en Enable for Hardware Low Power Interface. Value After Reset: 0x1 Volatile: True Programming Mode: Quasi-dynamic Group 2

DDRCTL_CLKGATECTL

Address: **Operational Base** + offset (0x1018C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x3f	bsm_clk_on Indicates whether the output signal bsm_clk_en [MEMC_NUM_RANKS-1:0] become 0 for each corresponding DDRCTL internal state: 1'b0: bsm_clk_en become 0 in case where DDRCTL is in corresponding state described below. 1'b1: bsm_clk_en remain 1 in case where DDRCTL is in corresponding state. The bsm_clk_en [MEMC_NUM_RANKS-1:0] indicates that clock can be removed when corresponding rank of this signal is 0. Each corresponding DDRCTL internal state is as follows: [0] Unpopulated rank control [1] Controller initialization state (until dfi0_init_start/dfi0_init_complete handshake is done) [2] Self Refresh mode [3] Self Refresh Powerdown mode [4] Powerdown mode [5] Deep Sleep Mode (LPDDR5 Only) Bit[5:1] indicates behavior of the bsm_clk_en for each corresponding DDRCTL internal state. For example, if this field is set to 6'b00_0100, bsm_clk_en becomes 1 when it is in self refresh mode. This implies that bsm_clk is not removed while it is in self refresh mode, but the bsm_clk is removed by external clock gating logic in other modes above. If bit 0 (Unpopulated rank control) is set to 1, behavior of the bsm_clk_en is determined by other fields in this register irrespective of MSTR.active_ranks. If the bsm_clk_en[1]=0 is needed in case of single rank (MSTR.active_ranks=1), bit 0 has to be set to 0. To maximize power-saving, this field needs to be set to 6'b00_0000. Value After Reset: 0x3f Programming Mode: Static

DDRCTL_RFSHMOD0

Address: **Operational Base** + offset (0x10200)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	per_bank_refresh 1'b1: Per bank refresh 1'b0: All bank refresh Per bank refresh allows traffic to flow to other banks. Value After Reset: 0x0 Programming Mode: Static
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x00	refresh_burst The programmed value + 1 is the number of refresh timeouts that is allowed to accumulate before traffic is blocked and the refreshes are forced to execute. Closing pages to perform a refresh is a one-time penalty that must be paid for each group of refreshes. Therefore, performing refreshes in a burst reduces the per-refresh penalty of these page closings. Higher numbers for RFSHCTL.refresh_burst slightly increases utilization; lower numbers decreases the worst-case latency associated with refreshes. 6'h0: Single refresh 6'h1: Burst-of-2 refresh 6'h7: Burst-of-8 refresh In per-bank refresh mode of LPDDR4/5 (DDRCTL_RFSHMOD0.per_bank_refresh = 1), 64 refreshes can be postponed. If using PHY-initiated updates, care must be taken in the setting of DDRCTL_RFSHMOD0.refresh_burst, to ensure that tRFCmax is not violated due to a PHY-initiated update occurring shortly before a refresh burst was due. In this situation, the refresh burst will be delayed until the PHY-initiated update is complete. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related

DDRCTL_RFSHCTL0

Address: **Operational Base** + offset (0x10208)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	refresh_update_level Toggle this signal (either from 0 to 1 or from 1 to 0) to indicate that the refresh register(s) have been updated. refresh_update_level must not be toggled when the DDRC is in reset (core_ddrc_rstn = 0). The refresh register(s) are automatically updated when exiting reset. Value After Reset: 0x0 Programming Mode: Dynamic
3:1	RO	0x0	reserved
0	RW	0x0	dis_auto_refresh When '1', disable auto-refresh generated by the DDRCTL. When auto-refresh is disabled, the SoC core must generate refreshes using the registers DDRCTL_OPREFCTRL*.rankn_refresh. When dis_auto_refresh transitions from 0 to 1, any pending refreshes are immediately scheduled by the DDRCTL. This register field is changeable on the fly. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related

DDRCTL_ZQCTL0

Address: **Operational Base** + offset (0x10280)

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Bit	Attr	Reset Value	Description
31	RW	0x0	dis_auto_zq 1'b1: Disable DDRCTL generation of ZQCS/MPC(ZQ calibration) command. Register DDRCTL_OPCTRLCMD.zq_calib_short can be used instead to issue ZQ calibration request from APB module. 1'b0: Internally generate ZQCS/MPC(ZQ calibration) commands based on DDRCTL_ZQSET1TMG1_FREQn.t_zq_short_interval_x1024(n=0, 1, 2 and 3). This register field only applys to LPDDR4 and LPDDR5. Value After Reset: 0x0 Programming Mode: Dynamic
30	RO	0x0	reserved
29	RW	0x0	zq_resistor_shared 1'b1: Denotes that ZQ resistor is shared between ranks. Means ZQinit/ZQCL/ZQCS/MPC(ZQ calibration) commands are sent to one rank at a time with tZQinit/tZQCL/tZQCS/tZQCAL/tZQLAT timing met between commands so that commands to different ranks do not overlap. 1'b0: ZQ resistor is not shared. If LPDDR5 is used, this register needs to be set to "0". Value After Reset: 0x0 Programming Mode: Static
28:0	RO	0x00000000	reserved

DDRCTL_ZQCTL1

Address: **Operational Base** + offset (0x10284)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	zq_reset Setting this register bit to 1 triggers a ZQ Reset operation. When the ZQ Reset operation is complete, the DDRCTL automatically clears this bit. It is recommended NOT to set this register bit if in Init, in SR-Powerdown or Deep Sleep Modes. For SR-Powerdown it will be scheduled after SRPD has been exited. For Deep Sleep Mode, it will be scheduled after DSM and/or SRPD has been exited. Value After Reset: 0x0 Testable: Read only Programming Mode: Dynamic

DDRCTL_ZQCTL2

Address: **Operational Base** + offset (0x10288)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dis_srx_zqcl 1'b1: Disable issuing of ZQCL/MPC(ZQ calibration) command at Self-Refresh/SR-Powerdown exit. 1'b0: Enable issuing of ZQCL/MPC(ZQ calibration) command at Self-Refresh/SR-Powerdown exit. This is only present for designs supporting LPDDR4 or LPDDR5 devices. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

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DDRCTL_ZQSTAT

Address: **Operational Base** + offset (0x1028C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	zq_reset_busy SoC core may initiate a ZQ Reset operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the ZQ Reset request. It goes low when the ZQ Reset command is issued to the SDRAM and the associated NOP period is over. It is recommended not to perform ZQ Reset commands when this signal is high. 1'b0: Indicates that the SoC core can initiate a ZQ Reset operation. 1'b1: Indicates that ZQ Reset operation is in progress. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_DQSOSCRUNTIME

Address: **Operational Base** + offset (0x10300)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x40	wck2dqo_runtime WCK2DQO interval timer run time setting as programmed in MR40 for LPDDR5.This field must be non zero. 8'h0: Interval timer stop via MPC command (not supported). 8'h1: Interval timer stops automatically at 16th clocks after timer start. 8'h2: Interval timer stops automatically at 32nd clocks after timer start. 8'h3: Interval timer stops automatically at 48th clocks after timer start. 8'h4: Interval timer stops automatically at 64th clocks after timer start. ..... 8'h3F: Interval timer stops automatically at (63x16)th clocks after timer start. 8'h40 to 8'h7F: Interval timer stops automatically at 2048th clocks after timer start. 8'h80 to 8'hBF: Interval timer stops automatically at 4096th clocks after timer start. 8'hC0 to 8'hFF: Interval timer stops automatically at 8192nd clocks after timer start. This register field is only applicable for designs supporting LPDDR5 SDRAM memories. It is don't care for LPDDR4 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x40 Volatile: True Programming Mode: Quasi-dynamic Group 2
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x40	dqsosc_runtime DQS interval timer run time setting as programmed in MR23 for LPDDR4. WCK2DQI interval timer run time setting as programmed in MR37 for LPDDR5. This field must be non zero. 8'h0: Interval timer stop via MPC command (not supported). 8'h1: Interval timer stops automatically at 16th clocks after timer start. 8'h2: Interval timer stops automatically at 32nd clocks after timer start. 8'h3: Interval timer stops automatically at 48th clocks after timer start. 8'h4: Interval timer stops automatically at 64th clocks after timer start. ..... 8'h3F: Interval timer stops automatically at (63x16)th clocks after timer start. 8'h40 to 8'h7F: Interval timer stops automatically at 2048th clocks after timer start. 8'h80 to 8'hBF: Interval timer stops automatically at 4096th clocks after timer start. 8'hC0 to 8'hFF: Interval timer stops automatically at 8192nd clocks after timer start. Unit: DRAM clock cycles. Value After Reset: 0x40 Volatile: True Programming Mode: Quasi-dynamic Group 2

DDRCTL_DQSOSCSTAT0

Address: **Operational Base** + offset (0x10304)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RO	0x0	dqsosc_per_rank_stat DQS/WCK Oscillator per rank status. This bit is set to 0 when DDRCTL_DQSOSCCTL0_FREQn.dqsosc_enable (n=0, 1, 2 and 3) is set to 1, and set to 1 when the DQS Oscillator command sequence is started for the corresponding active rank. Value After Reset: 0x0 Programming Mode: Static
3	RO	0x0	reserved
2:0	RO	0x0	dqsosc_state DQS/WCK Oscillator Control State Status. 3'b000: DQSOSC_IDLE 3'b001: DQSOSC_START: Sending MPC 3'b010: DQSOSC_RUNTIME: Waiting for runtime passed 3'b011: DQSOSC_GET_RESULT1: Sending first MRR 3'b100: DQSOSC_WAIT1: Waiting for tMRR for sending next MRR 3'b101: DQSOSC_GET_RESULT2: Sending second MRR 3'b110: DQSOSC_WAIT2: Waiting for tMRR or rank gap Others: Reserved Value After Reset: 0x0 Programming Mode: Static

DDRCTL_DQSOSCCFG0

Address: **Operational Base** + offset (0x10308)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dis_dqsosc_srx 1'b1: Disable issuing of DQSOSC command sequences at Self-Refresh/SR-Powerdown exit. 1'b0: Enable issuing of DQSOSC command sequences at Self-Refresh/SR-Powerdown exit. This is only present for designs supporting LPDDR4 or LPDDR5 devices. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2

DDRCTL_SCHED0

Address: **Operational Base** + offset (0x10380)

Bit	Attr	Reset Value	Description
31	RW	0x1	opt_vprw_sch Optimize exVPR/exVPW scheduling. 1'b0: When any exVPR/exVPW are pending on CAM, read/write command of all other traffic class are masked to be scheduled 1'b1: When any exVPR/exVPW are pending as page-hit, read/write command of all other traffic class are masked to be scheduled Program to 1 can improve utilization as other traffic class can utilize bandwidth while pages for exVPR/exVPW are being prepared or ranks/banks for exVPR/exVPW are being refreshed, but it can delay execution of exVPR/exVPW due to delay of Activate by read/write command of other traffic class. Value After Reset: 0x1 Volatile: True Programming Mode: Static
30	RW	0x0	dis_speculative_act Disable speculative Activate. In enhanced read write switching mode, activate commands can be issued to the other direction speculatively. This may have side-effect that the page opened for RD/WR proactively may be required to be closed to serve WR/RD respectively and it can have negative impact on performance due to command bus congestion. This register can limit such a speculative activate for the other direction. 1'b0: Allow speculative activates (default) 1'b1: Limit the speculative activates This register is effective for LPDDR4 and LPDDR5. In this version, the value 1 is not fully verified hence this register must be set to 0. Value After Reset: 0x0 Volatile: True Programming Mode: Static
29:17	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x1	lpddr5_opt_act_timing Optimized ACT timing control for LPDDR5. This register is to be used for debug purpose. In LPDDR5, ACTIVATE command is composed of two commands, ACT-1 and ACT-2. When this register is set, ACT-1 can be issued "tRRD-2" cycle after previous ACT-2. If ACT-1 is issued at this timing, the controller does not issue ACT-2 at next cycle due to tRRD. 1'b0: Disable (only for debug purpose) 1'b0: Enable (Default) This register is ignored when MSTR0.lpddr5==0. This register field is only applicable for LPDDR5 mode. Value After Reset: 0x1 Volatile: True Programming Mode: Static
15	RW	0x0	lpddr4_opt_act_timing Optimized ACT timing control for LPDDR4. In LPDDR4, RD/WR/ACT takes 4 cycle. To stream Read/Write, there are only 4 cycle space between Reads/Writes. If ACT is scheduled-out after RD/WR with 1, 2 or 3 cycle gap, next RD/WR may be pushed by 1, 2 or 3 cycle and create a gap on DQ. When this register is set, ACT is not scheduled-out with the gap = 1, 2 and 3 cycle. If enabled, there could be performance impact especially for random traffic(Latency/Utilization). 1'b1: Enable this feature 1'b0: Disable this feature This register is ignored when MSTR0.lpddr4==0. This register field is only applicable for LPDDR4 mode. Value After Reset: 0x0 Volatile: True Programming Mode: Static
14	RO	0x0	reserved
13:8	RW	0x20	lpr_num_entries Number of entries in the low priority transaction store is this value + 1. (MEMC_NO_OF_ENTRY - (SCHED.lpr_num_entries + 1)) is the number of entries available for the high priority transaction store. Setting this to maximum value allocates all entries to low priority transaction store. Setting this to 0 allocates 1 entry to low priority transaction store and the rest to high priority transaction store. Note: In ECC configurations, the numbers of write and low priority read credits issued is one less than in the non-ECC case. One entry each is in the write and low-priority read CAMs for storing the RMW requests arising out of single bit error correction RMW operation. Value After Reset: 0x20 Volatile: True Programming Mode: Static
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	dis_opt_ntt_by_pre Disable optimized NTT update by Precharge command. This register is debug purpose only. For normal operation, This register must be set to 0. 1'b1: Disabled 1'b0: Enabled Value After Reset: 0x0 Volatile: True Programming Mode: Static
5	RW	0x0	dis_opt_ntt_by_act Disable optimized NTT update by Activate command. This register is debug purpose only. For normal operation, This register must be set to 0. 1'b1: Disabled 1'b0: Enabled Value After Reset: 0x0 Volatile: True Programming Mode: Static
4	RW	0x1	opt_wrcam_fill_level Enable the feature of optimized write CAM fill level by switching to write when write CAM reaches certain fill level set in DDRCTL_SCHED3.wrcam_highthresh. 1'b1: Enabled 1'b0: Disabled If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. It is recommended that w_max_starve is programmed as >0 value when opt_wrcam_fill_level=1 to avoid starving extremely. Value After Reset: 0x1 Volatile: True Programming Mode: Static
3	RW	0x1	rdwr_switch_policy_sel Select read write switching policy. 1'b1: Select "enhanced" read write switching policy. 1'b0: Select "original" read write switching policy. Value After Reset: 0x1 Volatile: True Programming Mode: Static
2	RW	0x1	pageclose If true, bank is kept open only while there are page hit transactions available in the CAM to that bank. The last read or write command in the CAM with a bank and page hit will be executed with auto-precharge if DDRCTL_SCHEDTMG0_FREQn.pageclose_timer=0(n=0, 1, 2 and 3). Even if this register set to 1 and DDRCTL_SCHEDTMG0_FREQn.pageclose_timer is set to 0, explicit precharge (and not auto-precharge) may be issued in some cases where there is a mode switch between Write and Read or between LPR and HPR. The Read and Write commands that are executed as part of the ECC scrub requests are also executed without auto-precharge. If false, the bank remains open until there is a need to close it (to open a different page, or for page timeout or refresh timeout) - also known as open page policy. The open page policy can be overridden by setting the per-command-autopre bit on the HIF interface (hif_cmd_autopre).

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Bit	Attr	Reset Value	Description
			The pageclose feature provids a midway between Open and Close page policies. FOR PERFORMANCE ONLY. Value After Reset: 0x1 Volatile: True Programming Mode: Quasi-dynamic Group 3
1	RW	0x0	prefer_write If set then the bank selector prefers writes over reads. FOR DEBUG ONLY. Value After Reset: 0x0 Programming Mode: Static
0	RO	0x0	reserved

DDRCTL_SCHED1

Address: **Operational Base** + offset (0x10384)

Bit	Attr	Reset Value	Description
31	RW	0x0	opt_hit_gt_hpr Optimize the priority between Page-hit LPR and Page-miss HPR 1'b0: Page-miss HPR has priority (default) 1'b1: Page-hit LPR has priority This is to choose trade-off between HPR latency and total utilization. If set to 0, HPR latency can be better than 1 because HPR has priority over LPR. If set to 1, DRAM utilization can be better than 0 because number of ACT-PRE is reduced. When this register is set to 1, recommend to enable page-hit limiter so that once page-hit limiter is expired, HPR can have priority. Value After Reset: 0x0 Programming Mode: Static
30:28	RW	0x0	page_hit_limit_rd Page-Hit limiter for read. When certain number of read commands are scheduled out without ACT for a bank (schedule page-hit commands), all entries belonging to the bank priority are increased equal to page-hit entry even if these are page-miss so that oldest entry belonging to the bank can be served regardless of page-hit/page-miss. The priority is reset once any ACT/PRE/AP is served to the bank. 3'h0: Disable this feature 3'h1: 4 commands 3'h2: 8 commands 3'h3: 16 commands 3'h4: 32 commands Others: Reserved Value After Reset: 0x0 Volatile: True Programming Mode: Static
27	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
26:24	RW	0x0	page_hit_limit_wr Page-Hit limiter for write. When certain number of write commands are scheduled out without ACT for a bank (schedule page-hit commands), all entries belonging to the bank priority are increased equal to page-hit entry even if these are page-miss so that oldest entry belonging to the bank can be served regardless of page-hit/page-miss. The priority is reset once any ACT/PRE/AP is served to the bank. 3'h0: Disable this feature 3'h1: 4 commands 3'h2: 8 commands 3'h3: 16 commands 3'h4: 32 commands Others: Reserved Value After Reset: 0x0 Volatile: True Programming Mode: Static
23	RO	0x0	reserved
22:20	RW	0x0	visible_window_limit_rd Visible window limiter for read. This is to prevent extreme starvation against other entries within a CAM. Each read CAM entry has a counter, it is set to the value programmed in this register when command is pushed and is counted-down when newer read CAM entry is scheduled-out. The counter represent starvation within RD CAM in terms of number of commands to be over taken. When the counter reaches to 0, the entry becomes expired-VPR to eliminate more starvation. 3'h0: Disable this feature 3'h1: 31 commands 3'h2: 63 commands 3'h3: 127 commands 3'h4: 255 commands Others: Reserved Value After Reset: 0x0 Volatile: True Programming Mode: Static
19	RO	0x0	reserved
18:16	RW	0x0	visible_window_limit_wr Visible window limiter for write. This is to prevent extreme starvation against other entries within a CAM. Each write CAM entry has a counter, it is set to the value programmed in this register when command is pushed and is counted-down when newer write CAM entry is scheduled-out. The counter represent starvation within WR CAM in terms of number of commands to be over taken. When the counter reaches to 0, the entry becomes expired-VPW to eliminate more starvation. 3'h0: Disable this feature 3'h1: 31 commands 3'h2: 63 commands 3'h3: 127 commands 3'h4: 255 commands Others: Reserved

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Bit	Attr	Reset Value	Description
			Value After Reset: 0x0 Volatile: True Programming Mode: Static
15:12	RW	0x2	delay_switch_write delay_switch_write indicates number of cycles to delay switching read to write mode when write page-hit request is there and no read page-hit request is there. Setting higher value may reduce number of read to write switching but increase read to write turn-around time. The register indicates the number of cycles: 4'h0: no delay 4'h1: 2 cycles delay 4'h2: 4 cycles delay 4'h3: 6 cycles delay 4'h4: 8 cycles delay ..... 4'hf: 30 cycles delay If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. Value After Reset: 0x2 Volatile: True Programming Mode: Static
11:0	RO	0x000	reserved

DDRCTL_SCHED3

Address: **Operational Base** + offset (0x1038C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x04	rd_pghit_num_thresh Switch to read mode once number of read page-hit request exceeds the threshold set in the register during waiting tW2R. Set to 0 will disable the feature. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 3
23:22	RO	0x0	reserved
21:16	RW	0x04	wr_pghit_num_thresh Switch to write mode once number of write page-hit request exceeds threshold set in this register during waiting delay_switch_write timeout. Set to 0 will disable the feature. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x02	wrcam_highthresh The high threshold used in optimized write CAM fill level. When (MEMC_NO_OF_ENTRY - (number of loaded entries) < wrcam_highthresh), switch to write mode and prepare banks for write direction if no Exp-VPR or read collision is there. wrcam_highthresh must be set to a smaller value than wrcam_lowthresh. Note: In Sideband ECC configuration, the number of write entries is (MEMC_NO_OF_ENTRY-1) - except if MEMC_INLINE_ECC=1 is also set, where number of entries is MEMC_NO_OF_ENTRY for Inline ECC mode, otherwise, (MEMC_NO_OF_ENTRY-1). This feature is enabled when opt_wrcam_fill_level is 1. Value After Reset: 0x2 Volatile: True Programming Mode: Static
7:6	RO	0x0	reserved
5:0	RW	0x08	wrcam_lowthresh The low threshold used in optimized write CAM fill level. When (MEMC_NO_OF_ENTRY - (number of loaded entries) < wrcam_lowthresh), keep to write mode and stop to prepare banks for read direction if no Exp-VPR or read collision is there. Note: In Sideband ECC configuration, the number of write entries is (MEMC_NO_OF_ENTRY-1) - except if MEMC_INLINE_ECC=1 is also set, where number of entries is MEMC_NO_OF_ENTRY for Inline ECC mode, otherwise, (MEMC_NO_OF_ENTRY-1). This feature is enabled when opt_wrcam_fill_level is 1. Value After Reset: 0x8 Volatile: True Programming Mode: Static

DDRCTL_SCHED4

Address: **Operational Base** + offset (0x10390)

Bit	Attr	Reset Value	Description
31:24	RW	0x08	wr_page_exp_cycles wr_page_exp_cycles indicates number of cycles to keep the bank opened for write direction in read mode when both directions has request to the bank. The register indicates the number of cycle. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. Value After Reset: 0x8 Volatile: True Programming Mode: Quasi-dynamic Group 3
23:16	RW	0x40	rd_page_exp_cycles rd_page_exp_cycles indicates number of cycles to keep the bank opened for read direction in write mode when both directions has request to the bank. The register indicates the number of cycle. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. Value After Reset: 0x40 Volatile: True Programming Mode: Quasi-dynamic Group 3

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Bit	Attr	Reset Value	Description
15:8	RW	0x08	wr_act_idle_gap wr_act_idle_gap indicates number of cycles when write direction has no request to start preparing bank for read direction. The register indicates the number of cycle. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. Value After Reset: 0x8 Volatile: True Programming Mode: Quasi-dynamic Group 3
7:0	RW	0x10	rd_act_idle_gap rd_act_idle_gap indicates number of cycles when read direction has no request to start preparing bank for write direction. The register indicates the number of cycle. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. Value After Reset: 0x10 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_DFILPCFG0

Address: **Operational Base** + offset (0x10500)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x1	dfi_lp_data_req_en Enables DFI Data Low Power interface. 1'b0: Disabled. dfi_lp_data_req is not asserted. 1'b1: Enabled Value After Reset: 0x1 Programming Mode: Static
19:17	RO	0x0	reserved
16	RW	0x0	dfi_lp_en_data Enables DFI Data Low Power interface handshaking during data bus idle. 1'b0: Disabled 1'b1: Enabled Value After Reset: 0x0 Programming Mode: Static
15:9	RO	0x00	reserved
8	RW	0x0	dfi_lp_en_dsm Enables DFI Low Power interface handshaking during Deep Sleep Mode Entry/Exit. 1'b0: Disabled 1'b1: Enabled This is only present for designs supporting LPDDR5 devices. Value After Reset: 0x0 Programming Mode: Static
7:5	RO	0x0	reserved
4	RW	0x0	dfi_lp_en_sr Enables DFI Low Power interface handshaking during Self Refresh Entry/Exit. 1'b0: Disabled 1'b1: Enabled Value After Reset: 0x0 Programming Mode: Static
3:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	dfi_lp_en_pd Enables DFI Low Power interface handshaking during Power Down Entry/Exit. 1'b0: Disabled 1'b1: Enabled Value After Reset: 0x0 Programming Mode: Static

DDRCTL_DFIUPD0

Address: **Operational Base** + offset (0x10508)

Bit	Attr	Reset Value	Description
31	RW	0x0	dis_auto_ctrlupd 1'b0: DDRCTL issues dfi_ctrlupd_req periodically. 1'b1: Disable the automatic dfi_ctrlupd_req generation by the DDRCTL. The core must issue the dfi_ctrlupd_req signal using register DDRCTL_OPCTRLCMD.ctrlupd. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
30	RW	0x0	dis_auto_ctrlupd_srx 1'b0: DDRCTL issues a dfi_ctrlupd_req before or after exiting self-refresh, depending on DDRCTL_DFIUPD0.ctrlupd_pre_srx. 1'b1: Disable the automatic dfi_ctrlupd_req generation by the DDRCTL at self-refresh exit. Value After Reset: 0x0 Volatile: True Programming Mode: Static
29	RW	0x0	ctrlupd_pre_srx Selects dfi_ctrlupd_req requirements at SRX. 1'b0: Send ctrlupd after SRX 1'b1: Send ctrlupd before SRX If DDRCTL_DFIUPD0.dis_auto_ctrlupd_srx=1, this register has no impact, because no dfi_ctrlupd_req will be issued when SRX. Value After Reset: 0x0 Programming Mode: Static
28:16	RO	0x0000	reserved
15	RW	0x1	dfi_phyupd_en Enables the support for acknowledging PHY-initiated updates. 1'b0: Disabled 1'b1: Enabled Value After Reset: 0x1 Programming Mode: Static
14:0	RO	0x0000	reserved

DDRCTL_DFIMISC

Address: **Operational Base** + offset (0x10510)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	dfi_channel_mode This field controls how internal DFI data is connected to dfi0_*data* and dfi1_*data*. This must be set to 2'b00. Value After Reset: 0x0 Programming Mode: Static
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	dfi_frequency Indicates the operating frequency of the system. The number of supported frequencies and the mapping of signal values to clock frequencies are defined by the PHY. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1
7	RW	0x0	lp_optimized_write If this bit is 1, LPDDR4 write DQ is set to 8'hF8 if masked write with enabling DBI. Otherwise, that value is set to 8'hFF Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
6	RO	0x0	reserved
5	RW	0x0	dfi_init_start PHY init start request signal. When asserted it triggers the PHY init start request Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
4:3	RO	0x0	reserved
2	RW	0x0	dfi_data_cs_polarity Defines polarity of dfi_wrdata_cs and dfi_rddata_cs signals. 1'b0: Signals are active low. 1'b1: Signals are active high. Value After Reset: 0x0 Programming Mode: Static
1	RW	0x0	phy_dbi_mode DBI implemented in DDRC or PHY. 1'b0: DDRC implements DBI functionality. 1'b1: PHY implements DBI functionality. Present only in designs configured to support LPDDR4. Value After Reset: 0x0 Programming Mode: Static
0	RW	0x1	dfi_init_complete_en PHY initialization complete enable signal. When asserted the dfi_init_complete signal can be used to trigger SDRAM initialisation. Value After Reset: 0x1 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_DFISTAT

Address: **Operational Base** + offset (0x10514)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	dfi_lp_data_ack_stat Stores the value of the dfi_lp_data_ack input to the controller. Value After Reset: 0x0 Programming Mode: Dynamic
1	RO	0x0	dfi_lp_ctrl_ack_stat Stores the value of the dfi_lp_ctrl_ack input to the controller. Value After Reset: 0x0 Programming Mode: Dynamic

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Bit	Attr	Reset Value	Description
0	RO	0x0	dfi_init_complete The status flag register which announces when the DFI initialization has been completed. The DFI INIT triggered by dfi_init_start signal and then the dfi_init_complete flag is polled to know when the initialization is done. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_DFIPHYMSTR

Address: **Operational Base** + offset (0x10518)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	dfi_phymstr_blk_ref_x32 The programmed value x32 is the maximum number of DFI clock cycles that allows to send pending refreshes before starting self-refresh entry process. 8'h00: 0 DFI clock cycles, no delay 8'h01: 32 DFI clock cycles ..... 8'hFF: 8160 DFI clock cycles Unit: Multiples of 32 DFI clock cycles. Note: Use as default value (0x80). Value After Reset: 0x80 Programming Mode: Static
23:1	RO	0x000000	reserved
0	RW	0x1	dfi_phymstr_en Enables the PHY Master Interface 1'b0: Disabled 1'b1: Enabled Value After Reset: 0x1 Programming Mode: Static

DDRCTL_DFI0MSGCTL0

Address: **Operational Base** + offset (0x10520)

Bit	Attr	Reset Value	Description
31	RW	0x0	dfi0_ctrlmsg_req Setting this register bit to 1 triggers a DFI controller message transmission operation. DDRCTL automatically clear this bit when the DFI controller message request (dfi0_ctrlmsg_req) is asserted at the DFI MC to PHY Message port interface. This bit must be programmed separately after programming other register fields appropriately of this register. Note: DFI controller message request can be issued only if DDRCTL_DFIPHYMSTR.dfi_phymstr_en = 1. DFI controller message request must not be set during DFI LP mode due to software controlled low power entry. Value After Reset: 0x0 Testable: Read only Programming Mode: Dynamic
30:25	RO	0x00	reserved
24	RW	0x0	dfi0_ctrlmsg_tout_clr If this bit is set, DDRCTL_DFI0MSGSTAT0.dfi0_ctrlmsg_resp_tout is cleared by the controller. Value After Reset: 0x0 Testable: Read only Programming Mode: Dynamic

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	dfi0_ctrlmsg_cmd DFI0 controller message command. Value After Reset: 0x0 Programming Mode: Dynamic
15:0	RW	0x0000	dfi0_ctrlmsg_data DFI0 controller message data. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_DFI0MSGSTAT0

Address: **Operational Base** + offset (0x10524)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	dfi0_ctrlmsg_resp_tout This bit is set if dfi0_ctrlmsg_ack is not asserted by PHY within dfi_t_ctrlmsg_resp after asserting dfi0_ctrlmsg_req. Value After Reset: 0x0 Programming Mode: Dynamic
15:1	RO	0x0000	reserved
0	RO	0x0	dfi0_ctrlmsg_req_busy The SoC must trigger DFI controller message request only if this signal is low. This signal goes high in the clock after the DDRCTL accepts software triggered DFI controller message request by writing into DDRCTL_DFI0MSGCTRL0.dfi0_ctrlmsg_req. It goes low when PHY de-asserts dfi0_ctrlmsg_ack or dfi0_ctrlmsg_resp_tout event has triggered. 1'b0: Indicates that the SoC core can initiate a DFI controller message request operation. 1'b1: Indicates that DFI controller message request operation is in progress. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_POISONCFG

Address: **Operational Base** + offset (0x10580)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	rd_poison_intr_clr Interrupt clear for read transaction poisoning. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. DDRCTL automatically clears this bit. Value After Reset: 0x0 Testable: Read only Programming Mode: Dynamic
23:21	RO	0x0	reserved
20	RW	0x1	rd_poison_intr_en If set to 1, enables interrupts for read transaction poisoning. Value After Reset: 0x1 Programming Mode: Dynamic
19:17	RO	0x0	reserved
16	RW	0x1	rd_poison_slverr_en If set to 1, enables SLVERR response for read transaction poisoning. Value After Reset: 0x1 Programming Mode: Dynamic

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Bit	Attr	Reset Value	Description
15:9	RO	0x00	reserved
8	RW	0x0	wr_poison_intr_clr Interrupt clear for write transaction poisoning. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. DDRCTL automatically clears this bit. Value After Reset: 0x0 Testable: Read only Programming Mode: Dynamic
7:5	RO	0x0	reserved
4	RW	0x1	wr_poison_intr_en If set to 1, enables interrupts for write transaction poisoning. Value After Reset: 0x1 Programming Mode: Dynamic
3:1	RO	0x0	reserved
0	RW	0x1	wr_poison_slverr_en If set to 1, enables SLVERR response for write transaction poisoning. Value After Reset: 0x1 Programming Mode: Dynamic

DDRCTL_POISONSTAT

Address: **Operational Base** + offset (0x10584)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RO	0x0	rd_poison_intr_4 Read transaction poisoning error interrupt for port 4. This register is an APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. Value After Reset: 0x0 Programming Mode: Dynamic
19	RO	0x0	rd_poison_intr_3 Read transaction poisoning error interrupt for port 3. This register is an APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. Value After Reset: 0x0 Programming Mode: Dynamic
18	RO	0x0	rd_poison_intr_2 Read transaction poisoning error interrupt for port 2. This register is an APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. Value After Reset: 0x0 Programming Mode: Dynamic

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Bit	Attr	Reset Value	Description
17	RO	0x0	rd_poison_intr_1 Read transaction poisoning error interrupt for port 1. This register is an APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. Value After Reset: 0x0 Programming Mode: Dynamic
16	RO	0x0	rd_poison_intr_0 Read transaction poisoning error interrupt for port 0. This register is an APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. Value After Reset: 0x0 Programming Mode: Dynamic
15:5	RO	0x000	reserved
4	RO	0x0	wr_poison_intr_4 Write transaction poisoning error interrupt for port 4. This register is an APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. Value After Reset: 0x0 Programming Mode: Dynamic
3	RO	0x0	wr_poison_intr_3 Write transaction poisoning error interrupt for port 3. This register is an APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. Value After Reset: 0x0 Programming Mode: Dynamic
2	RO	0x0	wr_poison_intr_2 Write transaction poisoning error interrupt for port 2. This register is an APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. Value After Reset: 0x0 Programming Mode: Dynamic
1	RO	0x0	wr_poison_intr_1 Write transaction poisoning error interrupt for port 1. This register is an APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. Value After Reset: 0x0 Programming Mode: Dynamic

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Bit	Attr	Reset Value	Description
0	RO	0x0	wr_poison_intr_0 Write transaction poisoning error interrupt for port 0. This register is an APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_OPCTRL0

Address: **Operational Base** + offset (0x10B80)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	dis_max_rank_wr_opt Disable optimized max_rank_wr and max_logical_rank_wr feature. This register is debug purpose only. For normal operation, this register must be set to 0. Value After Reset: 0x0 Volatile: True Programming Mode: Static
6	RW	0x0	dis_max_rank_rd_opt Disable optimized max_rank_rd and max_logical_rank_rd feature. This register is debug purpose only. For normal operation, this register must be set to 0. Value After Reset: 0x0 Volatile: True Programming Mode: Static
5	RO	0x0	reserved
4	RW	0x0	dis_collision_page_opt When this is set to '0', auto-precharge is disabled for the flushed command in a collision case. Collision cases are write followed by read to same address, read followed by write to same address, or write followed by write to same address with DDRCTL_OPCTRL0.dis_wc bit = 1 (where same address comparisons exclude the two address bits representing critical word). FOR DEBUG ONLY. CAN ONLY BE SET TO 1. Value After Reset: 0x0 Programming Mode: Static
3:1	RO	0x0	reserved
0	RW	0x0	dis_wc When 1, disable write combine. FOR DEBUG ONLY Value After Reset: 0x0 Programming Mode: Static

DDRCTL_OPCTRL1

Address: **Operational Base** + offset (0x10B84)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	dis_hif When 1, DDRCTL asserts the HIF command signal hif_cmd_stall. DDRCTL will ignore the hif_cmd_valid and all other associated request signals. This bit is intended to be switched on-the-fly. Value After Reset: 0x0 Programming Mode: Dynamic
0	RW	0x0	dis_dq When 1, DDRCTL will not de-queue any transactions from the CAM. Bypass is also disabled. All transactions are queued in the CAM. No reads or writes are issued to SDRAM as long as this is asserted. This bit may be used to prevent reads or writes being issued by the DDRCTL, which makes it safe to modify certain register fields associated with reads and writes (see Programming Chapter for details). After setting this bit, it is strongly recommended to poll DDRCTL_OPCTRLCAM.wr_data_pipeline_empty and DDRCTL_OPCTRLCAM.rd_data_pipeline_empty, before making changes to any registers which affect reads and writes. This will ensure that the relevant logic in the DDRC is idle. This bit is intended to be switched on-the-fly. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_OPCTRLCAM

Address: **Operational Base** + offset (0x10B88)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RO	0x0	wr_data_pipeline_empty This bit indicates that the write data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting DDRCTL_OPCTRL1.dis_dq, to ensure that all remaining commands/data have completed. Value After Reset: 0x0 Reset Mask: 0x0 Volatile: True Programming Mode: Dynamic
28	RO	0x0	rd_data_pipeline_empty This bit indicates that the read data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting DDRCTL_OPCTRL1.dis_dq, to ensure that all remaining commands/data have completed. Value After Reset: 0x0 Reset Mask: 0x0 Volatile: True Programming Mode: Dynamic
27	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
26	RO	0x0	dbg_wr_q_empty When 1, all the Write command queues and Write data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When Controller enters Self-Refresh using the Low-Power entry sequence, Controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register must be 1 at that time. Value After Reset: 0x0 Reset Mask: 0x0 Volatile: True Programming Mode: Dynamic
25	RO	0x0	dbg_rd_q_empty When 1, all the Read command queues and Read data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When Controller enters Self-Refresh using the Low-Power entry sequence, Controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register must be 1 at that time. Value After Reset: 0x0 Reset Mask: 0x0 Volatile: True Programming Mode: Dynamic
24	RO	0x0	dbg_stall Stall FOR DEBUG ONLY Value After Reset: 0x0 Programming Mode: Dynamic
23	RO	0x0	reserved
22:16	RO	0x00	dbg_w_q_depth Write queue depth The last entry of WR queue is for ECC SCRUB operation. This entry is not included in the calculation of the queue depth. Value After Reset: 0x0 Programming Mode: Dynamic
15	RO	0x0	reserved
14:8	RO	0x00	dbg_lpr_q_depth Low priority read queue depth The last entry of Lpr queue is for ECC SCRUB operation. This entry is not included in the calculation of the queue depth. Value After Reset: 0x0 Programming Mode: Dynamic
7	RO	0x0	reserved
6:0	RO	0x00	dbg_hpr_q_depth High priority read queue depth Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_OPCTRLCMD

Address: **Operational Base** + offset (0x10B8C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
17	RW	0x0	ctrlupd Setting this register bit to 1 indicates to the DDRCTL to issue a dfi_ctrlupd_req to the PHY. When this request is stored in the DDRCTL, the bit is automatically cleared. This operation must only be performed when DDRCTL_DFIUPD0.dis_auto_ctrlupd=1. Value After Reset: 0x0 Testable: Read only Programming Mode: Dynamic
16	RW	0x0	zq_calib_short Setting this register bit to 1 indicates to the DDRCTL to issue a ZQCS (ZQ calibration short)/MPC(ZQ calibration) command to the SDRAM. When this request is stored in the DDRCTL, the bit is automatically cleared. This operation can be performed only when DDRCTL_ZQCTL0.dis_auto_zq=1. It is recommended NOT to set this register bit if in Init, in Self-Refresh(except LPDDR4/5) or SR-Powerdown(LPDDR4/5) or Deep Sleep Mode or Maximum Power Saving Mode. For Self-Refresh(except LPDDR4/5) or SR-Powerdown(LPDDR4/5) it will be scheduled after SR(except LPDDR4/5) or SRPD(LPDDR4/5) has been exited. For Deep Sleep Mode, it will be scheduled after DSM and/or SRPD has been exited. For Maximum Power Saving Mode, it will not be scheduled, although DDRCTL_OPCTRLSTAT.zq_calib_short_busy will be de-asserted. Value After Reset: 0x0 Testable: Read only Programming Mode: Dynamic
15:0	RO	0x0000	reserved

DDRCTL_OPCTRLSTAT

Address: **Operational Base** + offset (0x10B90)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	ctrlupd_busy SoC core may initiate a ctrlupd operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the ctrlupd request. It goes low when the ctrlupd operation is initiated in the DDRCTL. It is recommended not to perform ctrlupd operations when this signal is high. 1'b0: Indicates that the SoC core can initiate a ctrlupd operation. 1'b1: Indicates that ctrlupd operation has not been initiated yet in the DDRCTL. Value After Reset: 0x0 Programming Mode: Dynamic

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Bit	Attr	Reset Value	Description
16	RO	0x0	zq_calib_short_busy SoC core may initiate a ZQCS (ZQ calibration short) operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the ZQCS request. It goes low when the ZQCS operation is initiated in the DDRCTL. It is recommended not to perform ZQCS operations when this signal is high. 1'b0: Indicates that the SoC core can initiate a ZQCS operation. 1'b1: Indicates that ZQCS operation has not been initiated yet in the DDRCTL. Value After Reset: 0x0 Programming Mode: Dynamic
15:0	RO	0x0000	reserved

DDRCTL_OPREFCTRL0

Address: **Operational Base** + offset (0x10B98)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rank1_refresh Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 1. Writing to this bit causes DDRCTL_OPREFSTAT0.rank1_refresh_busy to be set. When DDRCTL_OPREFSTAT0.rank1_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 1. This operation can be performed only when DDRCTL_RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. Value After Reset: 0x0 Testable: Read only Programming Mode: Dynamic
0	RW	0x0	rank0_refresh Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 0. Writing to this bit causes DDRCTL_OPREFSTAT0.rank0_refresh_busy to be set. When DDRCTL_OPREFSTAT0.rank0_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 0. This operation can be performed only when DDRCTL_RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. Value After Reset: 0x0 Testable: Read only Programming Mode: Dynamic

DDRCTL_OPREFSTAT0

Address: **Operational Base** + offset (0x10BA0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1	RO	0x0	rank1_refresh_busy SoC core may initiate a rank1_refresh operation (refresh operation to rank 1) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank1_refresh is set to one. It goes low when the rank1_refresh operation is stored in the DDRCTL. It is recommended not to perform rank1_refresh operations when this signal is high. 1'b0: Indicates that the SoC core can initiate a rank1_refresh operation. 1'b1: Indicates that rank1_refresh operation has not been stored yet in the DDRCTL. Value After Reset: 0x0 Programming Mode: Dynamic
0	RO	0x0	rank0_refresh_busy SoC core may initiate a rank0_refresh operation (refresh operation to rank 0) only if this signal is low. This signal goes high in the clock after DDRCTL_OPREFCTRL0.rank0_refresh is set to one. It goes low when the rank0_refresh operation is stored in the DDRCTL. It is recommended not to perform rank0_refresh operations when this signal is high. 1'b0: Indicates that the SoC core can initiate a rank0_refresh operation. 1'b1: Indicates that rank0_refresh operation has not been stored yet in the DDRCTL. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_SWCTL

Address: **Operational Base** + offset (0x10C80)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	sw_done Enable quasi-dynamic register programming outside reset. Program register to 0 to enable quasi-dynamic programming. Set back register to 1 once programming is done. Value After Reset: 0x1 Programming Mode: Dynamic

DDRCTL_SWSTAT

Address: **Operational Base** + offset (0x10C84)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	sw_done_ack Register programming done. This register is the echo of DDRCTL_SWCTL.sw_done. Wait for sw_done value 1 to propagate to sw_done_ack at the end of the programming sequence to ensure that the correct registers values are propagated to the destination clock domains. Value After Reset: 0x1 Programming Mode: Static

DDRCTL_RANKCTL

Address: **Operational Base** + offset (0x10C90)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	max_rank_wr Only present for multi-rank configurations. Background: Writes to the same rank can be performed back-to-back. Writes to different ranks require additional gap dictated by the register DDRCTL_RANKCTL.diff_rank_wr_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The DDRCTL arbitrates for bus access on a cycle-by-cycle basis; therefore after a write is scheduled, there are few clock cycles (determined by the value on DDRCTL_RANKCTL.diff_rank_wr_gap register) in which only writes from the same rank are eligible to be scheduled. This prevents writes from other ranks from having fair access to the data bus. This parameter represents the maximum number of writes that can be scheduled consecutively to the same rank. After this number is reached, a delay equal to DDRCTL_RANKCTL.diff_rank_wr_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. FOR PERFORMANCE ONLY. Value After Reset: 0x0 Programming Mode: Static
11:4	RO	0x00	reserved
3:0	RW	0xf	max_rank_rd Only present for multi-rank configurations. Background: Reads to the same rank can be performed back-to-back. Reads to different ranks require additional gap dictated by the register DDRCTL_RANKCTL.diff_rank_rd_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The DDRCTL arbitrates for bus access on a cycle-by-cycle basis; therefore after a read is scheduled, there are few clock cycles (determined by the value on DDRCTL_RANKCTL.diff_rank_rd_gap register) in which only reads from the same rank are eligible to be scheduled. This prevents reads from other ranks from having fair access to the data bus. This parameter represents the maximum number of reads that can be scheduled consecutively to the same rank. After this number is reached, a delay equal to DDRCTL_RANKCTL.diff_rank_rd_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. FOR PERFORMANCE ONLY. Value After Reset: 0xf Programming Mode: Static

DDRCTL_DBICTL

Address: **Operational Base** + offset (0x10C94)

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Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	rd_dbi_en Read DBI enable signal in DDRC. 1'b0: Read DBI is disabled. 1'b1: Read DBI is enabled. This signal must be set the same value as DRAM's mode register. LPDDR4/LPDDR5: MR3[6]. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1
1	RW	0x0	wr_dbi_en Write DBI enable signal in DDRC. 1'b0: Write DBI is disabled. 1'b1: Write DBI is enabled. This signal must be set the same value as DRAM's mode register. LPDDR4/LPDDR5: MR3[7]. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1
0	RW	0x1	dm_en DM enable signal in DDRC. 1'b0: DM is disabled. 1'b1: DM is enabled. This signal must be set the same logical value as DRAM's mode register. LPDDR4/LPDDR5: Set this to inverted value of MR13[5] which is opposite polarity from this signal. Value After Reset: 0x1 Volatile: True Programming Mode: Static

DDRCTL_ODTMAP

Address: **Operational Base** + offset (0x10C9C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x2	rank1_rd_odt Indicates which remote ODTs must be turned on during a read from rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 2 or more ranks Value After Reset: 0x2 Programming Mode: Static
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x2	rank1_wr_odt Indicates which remote ODTs must be turned on during a write to rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 2 or more ranks Value After Reset: 0x2 Programming Mode: Static
7:6	RO	0x0	reserved
5:4	RW	0x1	rank0_rd_odt Indicates which remote ODTs must be turned on during a read from rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Value After Reset: 0x1 Programming Mode: Static
3:2	RO	0x0	reserved
1:0	RW	0x1	rank0_wr_odt Indicates which remote ODTs must be turned on during a write to rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Value After Reset: 0x1 Programming Mode: Static

DDRCTL_DATACTL0

Address: **Operational Base** + offset (0x10CA0)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	wr_data_x_en Write Data X 1'b1: Enable Write X 1'b0: Write X This feature is not supported at present. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2
17	RW	0x0	wr_data_copy_en Write Data Copy 1'b1: Enable Write Data Copy X 1'b0: Disable Write Data Copy X This feature is not supported at present. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2

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Bit	Attr	Reset Value	Description
16	RW	0x0	rd_data_copy_en Read Data Copy 1'b1: Enable Read Data Copy X 1'b0: Disable Read Data Copy X This feature is not supported at present. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2
15:0	RO	0x0000	reserved

DDRCTL_SWCTLSTATIC

Address: **Operational Base** + offset (0x10CA4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_static_unlock Enables static register programming outside reset. Program this register to 1 to enable static register programming. Set register back to 0 once programming is done. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_INITTMG0

Address: **Operational Base** + offset (0x10D00)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	skip_dram_init If lower bit is enabled the SDRAM initialization routine is skipped. The upper bit decides what state the controller starts up in when reset is removed. 2'b00: SDRAM Initialization routine is run after power-up 2'b01: SDRAM Initialization routine is skipped after power-up. Controller starts up in Normal Mode 2'b11: SDRAM Initialization routine is skipped after power-up. Controller starts up in Self-refresh Mode. 2'b10: Reserved Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2
29:26	RO	0x0	reserved
25:16	RW	0x002	post_cke_x1024 Cycles to wait after driving CKE (CS in LPDDR5) high to start the SDRAM initialization sequence. LPDDR4 typically requires this to be programmed for a delay of 2 us. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x2 Programming Mode: Static
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x004e	pre_cke_x1024 Cycles to wait after reset before driving CKE (CS in LPDDR5) high to start the SDRAM initialization sequence. LPDDR4: tINIT3 of 2 ms (min) Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x4e Programming Mode: Static

DDRCTL_INITTMG1

Address: **Operational Base** + offset (0x10D04)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	dram_rstn_x1024 Number of cycles to assert SDRAM reset signal during init sequence. For use with a Synopsys DDR PHY, this must be set to a minimum of 1. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Programming Mode: Static
15:0	RO	0x0000	reserved

DDRCTL_DDRCTL_VER_NUMBER

Address: **Operational Base** + offset (0x10FF8)

Bit	Attr	Reset Value	Description
31:0	RO	0x3130312a	ver_number Indicates the Device Version Number value. This is in ASCII format, with each byte corresponding to a character of the version number Value After Reset: 0x3130312a Programming Mode: Static

DDRCTL_DDRCTL_VER_TYPE

Address: **Operational Base** + offset (0x10FFC)

Bit	Attr	Reset Value	Description
31:0	RO	0x6c633031	ver_type Indicates the Device Version Type value. This is in ASCII format, with each byte corresponding to a character of the version type Value After Reset: 0x6c633031 Programming Mode: Static

DDRCTL_PCCFG_PORT0

Address: **Operational Base** + offset (0x20000)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	pagematch_limit Page match four limit. If set to 1, limits the number of consecutive same page DDRC transactions that can be granted by the Port Arbiter to four when Page Match feature is enabled. If set to 0, there is no limit imposed on number of consecutive same page DDRC transactions. Value After Reset: 0x0 Programming Mode: Static
3:1	RO	0x0	reserved
0	RW	0x0	go2critical_en If set to 1 (enabled), sets co_gs_go2critical_wr and co_gs_go2critical_lpr/co_gs_go2critical_hpr signals going to DDRC based on urgent input (awurgent, arurgent) coming from AXI master. If set to 0 (disabled), co_gs_go2critical_wr and co_gs_go2critical_lpr/co_gs_go2critical_hpr signals at DDRC are driven to 1b'0. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_PCFGR_PORT0

Address: **Operational Base** + offset (0x20004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	rdwr_ordered_en Enable ordered read/writes. If set to 1, preserves the ordering between read transaction and write transaction issued to the same address, on a given port. In other words, the controller ensures that all same address read and write commands from the application port interface are transported to the DFI interface in the order of acceptance. This feature is useful in cases where software coherency is desired for masters issuing back-to-back read/write transactions without waiting for write/read responses. Note that this register has an effect only if necessary logic is instantiated via the UMCTL2_RDWR_ORDERED_n parameter. Value After Reset: 0x0 Volatile: True Programming Mode: Static
15	RO	0x0	reserved
14	RW	0x1	rd_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related DDRCTL_PCCFG_PORT0.pagematch_limit register. Value After Reset: 0x1 Programming Mode: Static

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Bit	Attr	Reset Value	Description
13	RW	0x0	rd_port_urgent_en If set to 1, enables the AXI urgent sideband signal (arurgent). When enabled and arurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_lpr/co_gs_go2critical_hpr signal to DDRC is asserted if enabled in DDRCTL_PCCFG_PORT0.go2critical_en register. Note that arurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Value After Reset: 0x0 Programming Mode: Static
12	RW	0x1	rd_port_aging_en If set to 1, enables aging function for the read channel of the port. Value After Reset: 0x1 Programming Mode: Static
11:10	RO	0x0	reserved
9:0	RW	0x01f	rd_port_priority Determines the initial load value of read aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the read aging counter sets the priority of the read channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level (timeout condition - Priority0). For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (arqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. In this case, external dynamic priority input, arqos (for reads only) can still be used to set the DDRC read priority(2 priority levels: low priority read - LPR, high priority read - HPR) on a command by command basis. Note: The two LSBs of this register field are tied internally to 2'b00. Value After Reset: 0x1f Programming Mode: Static

DDRCTL_PCFGW_PORT0

Address: **Operational Base** + offset (0x20008)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x1	wr_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related DDRCTL_PCCFG_PORT0.pagematch_limit register. Value After Reset: 0x1 Programming Mode: Static

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Bit	Attr	Reset Value	Description
13	RW	0x0	wr_port_urgent_en If set to 1, enables the AXI urgent sideband signal (awurgent). When enabled and awurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_wr signal to DDRC is asserted if enabled in DDRCTL_PCCFG_PORT0.go2critical_en register. Note that awurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Value After Reset: 0x0 Programming Mode: Static
12	RW	0x1	wr_port_aging_en If set to 1, enables aging function for the write channel of the port. Value After Reset: 0x1 Programming Mode: Static
11:10	RO	0x0	reserved
9:0	RW	0x01f	wr_port_priority Determines the initial load value of write aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the write aging counter sets the initial priority of the write channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level. For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (awqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. Note: The two LSBs of this register field are tied internally to 2'b00. Value After Reset: 0x1f Programming Mode: Static

DDRCTL_PCTRL_PORT0

Address: **Operational Base** + offset (0x20090)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	port_en Enables AXI port n. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_PCFGQOS0_PORT0

Address: **Operational Base** + offset (0x20094)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:20	RW	0x0	rqos_map_region1 This bitfield indicates the traffic class of region 1. Valid values are: 2'b00: LPR 2'b01: VPR 2'b10: HPR For dual address queue configurations, region1 maps to the blue address queue. In this case, valid values are 2'b0: LPR 2'b1: VPR only When VPR support is disabled (UMCTL2_VPR_EN = 0) and traffic class of region 1 is set to 1 (VPR), VPR traffic is aliased to LPR traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
19:18	RO	0x0	reserved
17:16	RW	0x0	rqos_map_region0 This bitfield indicates the traffic class of region 0. Valid values are: 2'b00: LPR 2'b01: VPR 2'b10: HPR For dual address queue configurations, region 0 maps to the blue address queue. In this case, valid values are: 2'b0: LPR 2'b1: VPR only When VPR support is disabled (UMCTL2_VPR_EN = 0) and traffic class of region0 is set to 1 (VPR), VPR traffic is aliased to LPR traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:4	RO	0x000	reserved
3:0	RW	0x0	rqos_map_level1 Separation level1 indicating the end of region0 mapping; start of region0 is 0. Possible values for level1 are 0 to 13 (for dual RAQ) or 0 to 14 (for single RAQ) which corresponds to arqos. Note that for PA, arqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGQOS1_PORT0

Address: **Operational Base** + offset (0x20098)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26:16	RW	0x000	rqos_map_timeoutr Specifies the timeout value for transactions mapped to the red address queue. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:11	RO	0x00	reserved
10:0	RW	0x000	rqos_map_timeoutb Specifies the timeout value for transactions mapped to the blue address queue. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGWQOS0_PORT0

Address: **Operational Base** + offset (0x2009C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RW	0x0	wqos_map_region2 This bitfield indicates the traffic class of region 2. Valid values are: 2'b00: NPW 2'b01: VPW When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 2 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
23:22	RO	0x0	reserved
21:20	RW	0x0	wqos_map_region1 This bitfield indicates the traffic class of region 1. Valid values are: 2'b00: NPW 2'b01: VPW When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 1 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
19:18	RO	0x0	reserved
17:16	RW	0x0	wqos_map_region0 This bitfield indicates the traffic class of region 0. Valid values are: 2'b00: NPW 2'b01: VPW When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 0 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0xe	wqos_map_level2 Separation level2 indicating the end of region1 mapping; start of region1 is (level1 + 1). Possible values for level2 are (level1 + 1) to 14 which corresponds to awqos. Region2 starts from (level2 + 1) up to 15. Note that for PA, awqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset: 0xe Volatile: True Programming Mode: Quasi-dynamic Group 3
7:4	RO	0x0	reserved
3:0	RW	0x0	wqos_map_level1 Separation level indicating the end of region0 mapping; start of region0 is 0. Possible values for level1 are 0 to 13 which corresponds to awqos. Note that for PA, awqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGWQOS1_PORT0

Address: **Operational Base** + offset (0x200A0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	wqos_map_timeout2 Specifies the timeout value for write transactions in region 2. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:11	RO	0x00	reserved
10:0	RW	0x000	wqos_map_timeout1 Specifies the timeout value for write transactions in region 0 and 1. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PSTAT_PORT0

Address: **Operational Base** + offset (0x20114)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RO	0x0	wr_port_busy_4 Indicates if there are outstanding writes for AXI/CHI port 4. Value After Reset: 0x0 Programming Mode: Dynamic
19	RO	0x0	wr_port_busy_3 Indicates if there are outstanding writes for AXI/CHI port 3. Value After Reset: 0x0 Programming Mode: Dynamic

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Bit	Attr	Reset Value	Description
18	RO	0x0	wr_port_busy_2 Indicates if there are outstanding writes for AXI/CHI port 2. Value After Reset: 0x0 Programming Mode: Dynamic
17	RO	0x0	wr_port_busy_1 Indicates if there are outstanding writes for AXI/CHI port 1. Value After Reset: 0x0 Programming Mode: Dynamic
16	RO	0x0	wr_port_busy_0 Indicates if there are outstanding writes for AXI/CHI port 0. Value After Reset: 0x0 Programming Mode: Dynamic
15:5	RO	0x000	reserved
4	RO	0x0	rd_port_busy_4 Indicates if there are outstanding reads for AXI/CHI port 4. Value After Reset: 0x0 Programming Mode: Dynamic
3	RO	0x0	rd_port_busy_3 Indicates if there are outstanding reads for AXI/CHI port 3. Value After Reset: 0x0 Programming Mode: Dynamic
2	RO	0x0	rd_port_busy_2 Indicates if there are outstanding reads for AXI/CHI port 2. Value After Reset: 0x0 Programming Mode: Dynamic
1	RO	0x0	rd_port_busy_1 Indicates if there are outstanding reads for AXI/CHI port 1. Value After Reset: 0x0 Programming Mode: Dynamic
0	RO	0x0	rd_port_busy_0 Indicates if there are outstanding reads for AXI/CHI port 0. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_PCFGR_PORT1

Address: **Operational Base** + offset (0x21004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	rdwr_ordered_en Enable ordered read/writes. If set to 1, preserves the ordering between read transaction and write transaction issued to the same address, on a given port. In other words, the controller ensures that all same address read and write commands from the application port interface are transported to the DFI interface in the order of acceptance. This feature is useful in cases where software coherency is desired for masters issuing back-to-back read/write transactions without waiting for write/read responses. Note that this register has an effect only if necessary logic is instantiated via the UMCTL2_RDWR_ORDERED_n parameter. Value After Reset: 0x0 Volatile: True Programming Mode: Static
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x1	rd_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related DDRCTL_PCCFG_PORT0.pagematch_limit register. Value After Reset: 0x1 Programming Mode: Static
13	RW	0x0	rd_port_urgent_en If set to 1, enables the AXI urgent sideband signal (arurgent). When enabled and arurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_lpr/co_gs_go2critical_hpr signal to DDRC is asserted if enabled in DDRCTL_PCCFG_PORT0.go2critical_en register. Note that arurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Value After Reset: 0x0 Programming Mode: Static
12	RW	0x1	rd_port_aging_en If set to 1, enables aging function for the read channel of the port. Value After Reset: 0x1 Programming Mode: Static
11:10	RO	0x0	reserved
9:0	RW	0x01f	rd_port_priority Determines the initial load value of read aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the read aging counter sets the priority of the read channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level (timeout condition - Priority0). For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (arqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. In this case, external dynamic priority input, arqos (for reads only) can still be used to set the DDRC read priority(2 priority levels: low priority read - LPR, high priority read - HPR) on a command by command basis. Note: The two LSBs of this register field are tied internally to 2'b00. Value After Reset: 0x1f Programming Mode: Static

DDRCTL_PCFGW_PORT1

Address: **Operational Base** + offset (0x21008)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
14	RW	0x1	wr_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related DDRCTL_PCCFG_PORT0.pagematch_limit register. Value After Reset: 0x1 Programming Mode: Static
13	RW	0x0	wr_port_urgent_en If set to 1, enables the AXI urgent sideband signal (awurgent). When enabled and awurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_wr signal to DDRC is asserted if enabled in DDRCTL_PCCFG_PORT0.go2critical_en register. Note that awurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Value After Reset: 0x0 Programming Mode: Static
12	RW	0x1	wr_port_aging_en If set to 1, enables aging function for the write channel of the port. Value After Reset: 0x1 Programming Mode: Static
11:10	RO	0x0	reserved
9:0	RW	0x01f	wr_port_priority Determines the initial load value of write aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the write aging counter sets the initial priority of the write channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level. For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (awqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. Note: The two LSBs of this register field are tied internally to 2'b00. Value After Reset: 0x1f Programming Mode: Static

DDRCTL_PCTRL_PORT1

Address: **Operational Base** + offset (0x21090)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	port_en Enables AXI port n. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_PCFGQOS0_PORT1

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Address: **Operational Base** + offset (0x21094)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:20	RW	0x0	rqos_map_region1 This bitfield indicates the traffic class of region 1. Valid values are: 2'b00: LPR 2'b01: VPR 2'b10: HPR For dual address queue configurations, region1 maps to the blue address queue. In this case, valid values are 2'b0: LPR 2'b1: VPR only When VPR support is disabled (UMCTL2_VPR_EN = 0) and traffic class of region 1 is set to 1 (VPR), VPR traffic is aliased to LPR traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
19:18	RO	0x0	reserved
17:16	RW	0x0	rqos_map_region0 This bitfield indicates the traffic class of region 0. Valid values are: 2'b00: LPR 2'b01: VPR 2'b10: HPR For dual address queue configurations, region 0 maps to the blue address queue. In this case, valid values are: 2'b0: LPR 2'b1: VPR only When VPR support is disabled (UMCTL2_VPR_EN = 0) and traffic class of region0 is set to 1 (VPR), VPR traffic is aliased to LPR traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:4	RO	0x000	reserved
3:0	RW	0x0	rqos_map_level1 Separation level1 indicating the end of region0 mapping; start of region0 is 0. Possible values for level1 are 0 to 13 (for dual RAQ) or 0 to 14 (for single RAQ) which corresponds to arqos. Note that for PA, arqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGQOS1_PORT1

Address: **Operational Base** + offset (0x21098)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:16	RW	0x000	rqos_map_timeoutr Specifies the timeout value for transactions mapped to the red address queue. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:11	RO	0x00	reserved
10:0	RW	0x000	rqos_map_timeoutb Specifies the timeout value for transactions mapped to the blue address queue. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGWQOS0_PORT1

Address: **Operational Base** + offset (0x2109C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RW	0x0	wqos_map_region2 This bitfield indicates the traffic class of region 2. Valid values are: 2'b00: NPW 2'b01: VPW When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 2 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
23:22	RO	0x0	reserved
21:20	RW	0x0	wqos_map_region1 This bitfield indicates the traffic class of region 1. Valid values are: 2'b00: NPW 2'b01: VPW When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 1 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
19:18	RO	0x0	reserved
17:16	RW	0x0	wqos_map_region0 This bitfield indicates the traffic class of region 0. Valid values are: 2'b00: NPW 2'b01: VPW When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 0 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0xe	wqos_map_level2 Separation level2 indicating the end of region1 mapping; start of region1 is (level1 + 1). Possible values for level2 are (level1 + 1) to 14 which corresponds to awqos. Region2 starts from (level2 + 1) up to 15. Note that for PA, awqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset: 0xe Volatile: True Programming Mode: Quasi-dynamic Group 3
7:4	RO	0x0	reserved
3:0	RW	0x0	wqos_map_level1 Separation level indicating the end of region0 mapping; start of region0 is 0. Possible values for level1 are 0 to 13 which corresponds to awqos. Note that for PA, awqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGWQOS1_PORT1

Address: **Operational Base** + offset (0x210A0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	wqos_map_timeout2 Specifies the timeout value for write transactions in region 2. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:11	RO	0x00	reserved
10:0	RW	0x000	wqos_map_timeout1 Specifies the timeout value for write transactions in region 0 and 1. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGR_PORT2

Address: **Operational Base** + offset (0x22004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	rdwr_ordered_en Enable ordered read/writes. If set to 1, preserves the ordering between read transaction and write transaction issued to the same address, on a given port. In other words, the controller ensures that all same address read and write commands from the application port interface are transported to the DFI interface in the order of acceptance. This feature is useful in cases where software coherency is desired for masters issuing back-to-back read/write transactions without waiting for write/read responses. Note that this register has an effect only if necessary logic is instantiated via the UMCTL2_RDWR_ORDERED_n parameter. Value After Reset: 0x0 Volatile: True Programming Mode: Static
15	RO	0x0	reserved
14	RW	0x1	rd_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related DDRCTL_PCCFG_PORT0.pagematch_limit register. Value After Reset: 0x1 Programming Mode: Static
13	RW	0x0	rd_port_urgent_en If set to 1, enables the AXI urgent sideband signal (arurgent). When enabled and arurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_lpr/co_gs_go2critical_hpr signal to DDRC is asserted if enabled in DDRCTL_PCCFG_PORT0.go2critical_en register. Note that arurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Value After Reset: 0x0 Programming Mode: Static
12	RW	0x1	rd_port_aging_en If set to 1, enables aging function for the read channel of the port. Value After Reset: 0x1 Programming Mode: Static
11:10	RO	0x0	reserved
9:0	RW	0x01f	rd_port_priority Determines the initial load value of read aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the read aging counter sets the priority of the read channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level (timeout condition - Priority0). For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (arqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. In this case, external dynamic priority input, arqos (for

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Bit	Attr	Reset Value	Description
			reads only) can still be used to set the DDRC read priority(2 priority levels: low priority read - LPR, high priority read - HPR) on a command by command basis. Note: The two LSBs of this register field are tied internally to 2'b00. Value After Reset: 0x1f Programming Mode: Static

DDRCTL_PCFGW_PORT2

Address: **Operational Base** + offset (0x22008)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x1	wr_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related DDRCTL_PCCFG_PORT0.pagematch_limit register. Value After Reset: 0x1 Programming Mode: Static
13	RW	0x0	wr_port_urgent_en If set to 1, enables the AXI urgent sideband signal (awurgent). When enabled and awurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_wr signal to DDRC is asserted if enabled in DDRCTL_PCCFG_PORT0.go2critical_en register. Note that awurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Value After Reset: 0x0 Programming Mode: Static
12	RW	0x1	wr_port_aging_en If set to 1, enables aging function for the write channel of the port. Value After Reset: 0x1 Programming Mode: Static
11:10	RO	0x0	reserved
9:0	RW	0x01f	wr_port_priority Determines the initial load value of write aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the write aging counter sets the initial priority of the write channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level. For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (awqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. Note: The two LSBs of this register field are tied internally to 2'b00. Value After Reset: 0x1f

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Bit	Attr	Reset Value	Description
			Programming Mode: Static

DDRCTL_PCTRL_PORT2

Address: **Operational Base** + offset (0x22090)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	port_en Enables AXI port n. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_PCFGQOS0_PORT2

Address: **Operational Base** + offset (0x22094)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:20	RW	0x0	rqos_map_region1 This bitfield indicates the traffic class of region 1. Valid values are: 2'b00: LPR 2'b01: VPR 2'b10: HPR For dual address queue configurations, region1 maps to the blue address queue. In this case, valid values are 2'b0: LPR 2'b1: VPR only When VPR support is disabled (UMCTL2_VPR_EN = 0) and traffic class of region 1 is set to 1 (VPR), VPR traffic is aliased to LPR traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
19:18	RO	0x0	reserved
17:16	RW	0x0	rqos_map_region0 This bitfield indicates the traffic class of region 0. Valid values are: 2'b00: LPR 2'b01: VPR 2'b10: HPR For dual address queue configurations, region 0 maps to the blue address queue. In this case, valid values are: 2'b0: LPR 2'b1: VPR only When VPR support is disabled (UMCTL2_VPR_EN = 0) and traffic class of region0 is set to 1 (VPR), VPR traffic is aliased to LPR traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:4	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	rqos_map_level1 Separation level1 indicating the end of region0 mapping; start of region0 is 0. Possible values for level1 are 0 to 13 (for dual RAQ) or 0 to 14 (for single RAQ) which corresponds to arqos. Note that for PA, arqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGQOS1_PORT2

Address: **Operational Base** + offset (0x22098)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	rqos_map_timeoutr Specifies the timeout value for transactions mapped to the red address queue. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:11	RO	0x00	reserved
10:0	RW	0x000	rqos_map_timeoutb Specifies the timeout value for transactions mapped to the blue address queue. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGWQOS0_PORT2

Address: **Operational Base** + offset (0x2209C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RW	0x0	wqos_map_region2 This bitfield indicates the traffic class of region 2. Valid values are: 2'b00: NPW 2'b01: VPW When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 2 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
23:22	RO	0x0	reserved
21:20	RW	0x0	wqos_map_region1 This bitfield indicates the traffic class of region 1. Valid values are: 2'b00: NPW 2'b01: VPW When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 1 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

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Bit	Attr	Reset Value	Description
19:18	RO	0x0	reserved
17:16	RW	0x0	wqos_map_region0 This bitfield indicates the traffic class of region 0. Valid values are: 2'b00: NPW 2'b01: VPW When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 0 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:12	RO	0x0	reserved
11:8	RW	0xe	wqos_map_level2 Separation level2 indicating the end of region1 mapping; start of region1 is (level1 + 1). Possible values for level2 are (level1 + 1) to 14 which corresponds to awqos. Region2 starts from (level2 + 1) up to 15. Note that for PA, awqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset: 0xe Volatile: True Programming Mode: Quasi-dynamic Group 3
7:4	RO	0x0	reserved
3:0	RW	0x0	wqos_map_level1 Separation level indicating the end of region0 mapping; start of region0 is 0. Possible values for level1 are 0 to 13 which corresponds to awqos. Note that for PA, awqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGWQOS1_PORT2

Address: **Operational Base** + offset (0x220A0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	wqos_map_timeout2 Specifies the timeout value for write transactions in region 2. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:11	RO	0x00	reserved
10:0	RW	0x000	wqos_map_timeout1 Specifies the timeout value for write transactions in region 0 and 1. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGR_PORT3

Address: **Operational Base** + offset (0x23004)

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Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	rdwr_ordered_en Enable ordered read/writes. If set to 1, preserves the ordering between read transaction and write transaction issued to the same address, on a given port. In other words, the controller ensures that all same address read and write commands from the application port interface are transported to the DFI interface in the order of acceptance. This feature is useful in cases where software coherency is desired for masters issuing back-to-back read/write transactions without waiting for write/read responses. Note that this register has an effect only if necessary logic is instantiated via the UMCTL2_RDWR_ORDERED_n parameter. Value After Reset: 0x0 Volatile: True Programming Mode: Static
15	RO	0x0	reserved
14	RW	0x1	rd_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related DDRCTL_PCCFG_PORT0.pagematch_limit register. Value After Reset: 0x1 Programming Mode: Static
13	RW	0x0	rd_port_urgent_en If set to 1, enables the AXI urgent sideband signal (arurgent). When enabled and arurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_lpr/co_gs_go2critical_hpr signal to DDRC is asserted if enabled in DDRCTL_PCCFG_PORT0.go2critical_en register. Note that arurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Value After Reset: 0x0 Programming Mode: Static
12	RW	0x1	rd_port_aging_en If set to 1, enables aging function for the read channel of the port. Value After Reset: 0x1 Programming Mode: Static
11:10	RO	0x0	reserved
9:0	RW	0x01f	rd_port_priority Determines the initial load value of read aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the read aging counter sets the priority of the read channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level (timeout condition - Priority0). For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (arqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction

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Bit	Attr	Reset Value	Description
			switching. In this case, external dynamic priority input, arqos (for reads only) can still be used to set the DDRC read priority(2 priority levels: low priority read - LPR, high priority read - HPR) on a command by command basis. Note: The two LSBs of this register field are tied internally to 2'b00. Value After Reset: 0x1f Programming Mode: Static

DDRCTL_PCFGW_PORT3

Address: **Operational Base** + offset (0x23008)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x1	wr_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related DDRCTL_PCCFG_PORT0.pagematch_limit register. Value After Reset: 0x1 Programming Mode: Static
13	RW	0x0	wr_port_urgent_en If set to 1, enables the AXI urgent sideband signal (awurgent). When enabled and awurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_wr signal to DDRC is asserted if enabled in DDRCTL_PCCFG_PORT0.go2critical_en register. Note that awurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Value After Reset: 0x0 Programming Mode: Static
12	RW	0x1	wr_port_aging_en If set to 1, enables aging function for the write channel of the port. Value After Reset: 0x1 Programming Mode: Static
11:10	RO	0x0	reserved
9:0	RW	0x01f	wr_port_priority Determines the initial load value of write aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the write aging counter sets the initial priority of the write channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level. For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (awqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. Note: The two LSBs of this register field are tied internally to 2'b00.

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Bit	Attr	Reset Value	Description
			Value After Reset: 0x1f Programming Mode: Static

DDRCTL_PCTRL_PORT3

Address: **Operational Base** + offset (0x23090)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	port_en Enables AXI port n. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_PCFGQOS0_PORT3

Address: **Operational Base** + offset (0x23094)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:20	RW	0x0	rqos_map_region1 This bitfield indicates the traffic class of region 1. Valid values are: 2'b00: LPR 2'b01: VPR 2'b10: HPR For dual address queue configurations, region1 maps to the blue address queue. In this case, valid values are 2'b0: LPR 2'b1: VPR only When VPR support is disabled (UMCTL2_VPR_EN = 0) and traffic class of region 1 is set to 1 (VPR), VPR traffic is aliased to LPR traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
19:18	RO	0x0	reserved
17:16	RW	0x0	rqos_map_region0 This bitfield indicates the traffic class of region 0. Valid values are: 2'b00: LPR 2'b01: VPR 2'b10: HPR For dual address queue configurations, region 0 maps to the blue address queue. In this case, valid values are: 2'b0: LPR 2'b1: VPR only When VPR support is disabled (UMCTL2_VPR_EN = 0) and traffic class of region0 is set to 1 (VPR), VPR traffic is aliased to LPR traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:4	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	rqos_map_level1 Separation level1 indicating the end of region0 mapping; start of region0 is 0. Possible values for level1 are 0 to 13 (for dual RAQ) or 0 to 14 (for single RAQ) which corresponds to arqos. Note that for PA, arqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGQOS1_PORT3

Address: **Operational Base** + offset (0x23098)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	rqos_map_timeoutr Specifies the timeout value for transactions mapped to the red address queue. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:11	RO	0x00	reserved
10:0	RW	0x000	rqos_map_timeoutb Specifies the timeout value for transactions mapped to the blue address queue. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGWQOS0_PORT3

Address: **Operational Base** + offset (0x2309C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RW	0x0	wqos_map_region2 This bitfield indicates the traffic class of region 2. Valid values are: 2'b00: NPW 2'b01: VPW When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 2 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
23:22	RO	0x0	reserved
21:20	RW	0x0	wqos_map_region1 This bitfield indicates the traffic class of region 1. Valid values are: 2'b00: NPW 2'b01: VPW When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 1 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

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Bit	Attr	Reset Value	Description
19:18	RO	0x0	reserved
17:16	RW	0x0	wqos_map_region0 This bitfield indicates the traffic class of region 0. Valid values are: 2'b00: NPW 2'b01: VPW When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 0 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:12	RO	0x0	reserved
11:8	RW	0xe	wqos_map_level2 Separation level2 indicating the end of region1 mapping; start of region1 is (level1 + 1). Possible values for level2 are (level1 + 1) to 14 which corresponds to awqos. Region2 starts from (level2 + 1) up to 15. Note that for PA, awqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset: 0xe Volatile: True Programming Mode: Quasi-dynamic Group 3
7:4	RO	0x0	reserved
3:0	RW	0x0	wqos_map_level1 Separation level indicating the end of region0 mapping; start of region0 is 0. Possible values for level1 are 0 to 13 which corresponds to awqos. Note that for PA, awqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGWQOS1_PORT3

Address: **Operational Base** + offset (0x230A0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	wqos_map_timeout2 Specifies the timeout value for write transactions in region 2. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:11	RO	0x00	reserved
10:0	RW	0x000	wqos_map_timeout1 Specifies the timeout value for write transactions in region 0 and 1. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGR_PORT4

Address: **Operational Base** + offset (0x24004)

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Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	rdwr_ordered_en Enable ordered read/writes. If set to 1, preserves the ordering between read transaction and write transaction issued to the same address, on a given port. In other words, the controller ensures that all same address read and write commands from the application port interface are transported to the DFI interface in the order of acceptance. This feature is useful in cases where software coherency is desired for masters issuing back-to-back read/write transactions without waiting for write/read responses. Note that this register has an effect only if necessary logic is instantiated via the UMCTL2_RDWR_ORDERED_n parameter. Value After Reset: 0x0 Volatile: True Programming Mode: Static
15	RO	0x0	reserved
14	RW	0x1	rd_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related DDRCTL_PCCFG_PORT0.pagematch_limit register. Value After Reset: 0x1 Programming Mode: Static
13	RW	0x0	rd_port_urgent_en If set to 1, enables the AXI urgent sideband signal (arurgent). When enabled and arurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_lpr/co_gs_go2critical_hpr signal to DDRC is asserted if enabled in DDRCTL_PCCFG_PORT0.go2critical_en register. Note that arurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Value After Reset: 0x0 Programming Mode: Static
12	RW	0x1	rd_port_aging_en If set to 1, enables aging function for the read channel of the port. Value After Reset: 0x1 Programming Mode: Static
11:10	RO	0x0	reserved
9:0	RW	0x01f	rd_port_priority Determines the initial load value of read aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the read aging counter sets the priority of the read channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level (timeout condition - Priority0). For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (arqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction

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Bit	Attr	Reset Value	Description
			switching. In this case, external dynamic priority input, arqos (for reads only) can still be used to set the DDRC read priority(2 priority levels: low priority read - LPR, high priority read - HPR) on a command by command basis. Note: The two LSBs of this register field are tied internally to 2'b00. Value After Reset: 0x1f Programming Mode: Static

DDRCTL_PCFGW_PORT4

Address: **Operational Base** + offset (0x24008)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x1	wr_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related DDRCTL_PCCFG_PORT0.pagematch_limit register. Value After Reset: 0x1 Programming Mode: Static
13	RW	0x0	wr_port_urgent_en If set to 1, enables the AXI urgent sideband signal (awurgent). When enabled and awurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_wr signal to DDRC is asserted if enabled in DDRCTL_PCCFG_PORT0.go2critical_en register. Note that awurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Value After Reset: 0x0 Programming Mode: Static
12	RW	0x1	wr_port_aging_en If set to 1, enables aging function for the write channel of the port. Value After Reset: 0x1 Programming Mode: Static
11:10	RO	0x0	reserved
9:0	RW	0x01f	wr_port_priority Determines the initial load value of write aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the write aging counter sets the initial priority of the write channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level. For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (awqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. Note: The two LSBs of this register field are tied internally to 2'b00.

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Bit	Attr	Reset Value	Description
			Value After Reset: 0x1f Programming Mode: Static

DDRCTL_PCTRL_PORT4

Address: **Operational Base** + offset (0x24090)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	port_en Enables AXI port n. Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_PCFGQOS0_PORT4

Address: **Operational Base** + offset (0x24094)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:20	RW	0x0	rqos_map_region1 This bitfield indicates the traffic class of region 1. Valid values are: 2'b00: LPR 2'b01: VPR 2'b10: HPR For dual address queue configurations, region1 maps to the blue address queue. In this case, valid values are 2'b0: LPR 2'b1: VPR only When VPR support is disabled (UMCTL2_VPR_EN = 0) and traffic class of region 1 is set to 1 (VPR), VPR traffic is aliased to LPR traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
19:18	RO	0x0	reserved
17:16	RW	0x0	rqos_map_region0 This bitfield indicates the traffic class of region 0. Valid values are: 2'b00: LPR 2'b01: VPR 2'b10: HPR For dual address queue configurations, region 0 maps to the blue address queue. In this case, valid values are: 2'b0: LPR 2'b1: VPR only When VPR support is disabled (UMCTL2_VPR_EN = 0) and traffic class of region0 is set to 1 (VPR), VPR traffic is aliased to LPR traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:4	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	rqos_map_level1 Separation level1 indicating the end of region0 mapping; start of region0 is 0. Possible values for level1 are 0 to 13 (for dual RAQ) or 0 to 14 (for single RAQ) which corresponds to arqos. Note that for PA, arqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGQOS1_PORT4

Address: **Operational Base** + offset (0x24098)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	rqos_map_timeoutr Specifies the timeout value for transactions mapped to the red address queue. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:11	RO	0x00	reserved
10:0	RW	0x000	rqos_map_timeoutb Specifies the timeout value for transactions mapped to the blue address queue. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGWQOS0_PORT4

Address: **Operational Base** + offset (0x2409C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RW	0x0	wqos_map_region2 This bitfield indicates the traffic class of region 2. Valid values are: 2'b00: NPW 2'b01: VPW When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 2 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
23:22	RO	0x0	reserved
21:20	RW	0x0	wqos_map_region1 This bitfield indicates the traffic class of region 1. Valid values are: 2'b00: NPW 2'b01: VPW When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 1 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

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Bit	Attr	Reset Value	Description
19:18	RO	0x0	reserved
17:16	RW	0x0	wqos_map_region0 This bitfield indicates the traffic class of region 0. Valid values are: 2'b00: NPW 2'b01: VPW When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 0 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:12	RO	0x0	reserved
11:8	RW	0xe	wqos_map_level2 Separation level2 indicating the end of region1 mapping; start of region1 is (level1 + 1). Possible values for level2 are (level1 + 1) to 14 which corresponds to awqos. Region2 starts from (level2 + 1) up to 15. Note that for PA, awqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset: 0xe Volatile: True Programming Mode: Quasi-dynamic Group 3
7:4	RO	0x0	reserved
3:0	RW	0x0	wqos_map_level1 Separation level indicating the end of region0 mapping; start of region0 is 0. Possible values for level1 are 0 to 13 which corresponds to awqos. Note that for PA, awqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PCFGWQOS1_PORT4

Address: **Operational Base** + offset (0x240A0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	wqos_map_timeout2 Specifies the timeout value for write transactions in region 2. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3
15:11	RO	0x00	reserved
10:0	RW	0x000	wqos_map_timeout1 Specifies the timeout value for write transactions in region 0 and 1. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_ADDRMAP1

Address: **Operational Base** + offset (0x30004)

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Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	addrmap_cs_bit0 Selects the HIF address bit used as rank address bit 0. Valid Range: 0 to 33, and 63 Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then rank address bit 0 is set to 0. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_ADDRMAP3

Address: **Operational Base** + offset (0x3000C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	addrmap_bank_b2 Selects the HIF address bit used as bank address bit 2. Valid Range: 0 to 34, and 63 Internal Base: 5 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 2 is set to 0. Value After Reset: 0x0 Programming Mode: Static
15:14	RO	0x0	reserved
13:8	RW	0x00	addrmap_bank_b1 Selects the HIF address bits used as bank address bit 1. Valid Range: 0 to 35, and 63 Internal Base: 4 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 1 is set to 0. Value After Reset: 0x0 Programming Mode: Static
7:6	RO	0x0	reserved
5:0	RW	0x00	addrmap_bank_b0 Selects the HIF address bits used as bank address bit 0. Valid Range: 0 to 36, and 63 Internal Base: 3 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_ADDRMAP4

Address: **Operational Base** + offset (0x30010)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x00	addrmap_bg_b1 Selects the HIF address bits used as bank group address bit 1. Valid Range: 0 to 35, and 63 Internal Base: 4 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 1 is set to 0. Value After Reset: 0x0 Programming Mode: Static
7:6	RO	0x0	reserved
5:0	RW	0x00	addrmap_bg_b0 Selects the HIF address bits used as bank group address bit 0. Valid Range: 0 to 36, and 63 Internal Base: 3 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 0 is set to 0. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_ADDRMAP5

Address: **Operational Base** + offset (0x30014)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	addrmap_col_b10 Selects the HIF address bit used as column address bit 10. Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 10 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 10 is the highest column address bit, it must map to the highest valid HIF address bit. (x = the highest valid HIF address bit - internal base) If column bit 10 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base). If column bit 10 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base). If unused, set to 31 and then this column address bit is set to 0. Value After Reset: 0x0 Programming Mode: Static
23:21	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
20:16	RW	0x00	addrmap_col_b9 Selects the HIF address bit used as column address bit 9. Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 9 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 9 is the highest column address bit, it must map to the highest valid HIF address bit. (x = the highest valid HIF address bit - internal base) If column bit 9 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base). If column bit 9 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base). If unused, set to 31 and then this column address bit is set to 0. Value After Reset: 0x0 Programming Mode: Static
15:13	RO	0x0	reserved
12:8	RW	0x00	addrmap_col_b8 Selects the HIF address bit used as column address bit 8. Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 8 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 8 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base). If column bit 8 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base). If unused, set to 31 and then this column address bit is set to 0. Value After Reset: 0x0 Programming Mode: Static
7:5	RO	0x0	reserved
4:0	RW	0x00	addrmap_col_b7 Selects the HIF address bit used as column address bit 7. Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 7 The selected HIF address bit is determined by adding the internal base to the value of this field. In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 7 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base).

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Bit	Attr	Reset Value	Description
			If unused, set to 31 and then this column address bit is set to 0. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_ADDRMAP6

Address: **Operational Base** + offset (0x30018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	addrmap_col_b6 Selects the HIF address bit used as column address bit 6. Valid Range: 0 to 7, x and 15. x indicates a valid value in the inline ECC configuration. Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Value After Reset: 0x0 Programming Mode: Static
23:20	RO	0x0	reserved
19:16	RW	0x0	addrmap_col_b5 Selects the HIF address bit used as column address bit 5. Valid Range: 0 to 7, and 15 Internal Base: 5 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Value After Reset: 0x0 Programming Mode: Static
15:12	RO	0x0	reserved
11:8	RW	0x0	addrmap_col_b4 Full bus width mode: Selects the HIF address bit used as column address bit 4. Half bus width mode: Selects the HIF address bit used as column address bit 5. Quarter bus width mode: Selects the HIF address bit used as column address bit 6. Valid Range: 0 to 7, and 15 Internal Base: 4 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Value After Reset: 0x0 Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_col_b3 Selects the HIF address bit used as column address bit 3. Valid Range: 0 to 7. Internal Base: 3 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: In LPDDR4/5, it is required to program this to 0. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_ADDRMAP7

Address: **Operational Base** + offset (0x3001C)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	addrmap_row_b17 Selects the HIF address bit used as row address bit 17. Valid Range: 0 to 16, and 31 Internal Base: 23 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 17 is set to 0. Value After Reset: 0x0 Programming Mode: Static
23:21	RO	0x0	reserved
20:16	RW	0x00	addrmap_row_b16 Selects the HIF address bit used as row address bit 16. Valid Range: 0 to 16, and 31 Internal Base: 22 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 16 is set to 0. Value After Reset: 0x0 Programming Mode: Static
15:13	RO	0x0	reserved
12:8	RW	0x00	addrmap_row_b15 Selects the HIF address bit used as row address bit 15. Valid Range: 0 to 16, and 31 Internal Base: 21 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 15 is set to 0. Value After Reset: 0x0 Programming Mode: Static
7:5	RO	0x0	reserved
4:0	RW	0x00	addrmap_row_b14 Selects the HIF address bit used as row address bit 14. Valid Range: 0 to 16, and 31 Internal Base: 20 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 14 is set to 0. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_ADDRMAP8

Address: **Operational Base** + offset (0x30020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	addrmap_row_b13 Selects the HIF address bit used as row address bit 13. Valid Range: 0 to 16, and 31 Internal Base: 19 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 13 is set to 0. Value After Reset: 0x0 Programming Mode: Static
23:21	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
20:16	RW	0x00	addrmap_row_b12 Selects the HIF address bit used as row address bit 12. Valid Range: 0 to 16, and 31 Internal Base: 18 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 12 is set to 0. Value After Reset: 0x0 Programming Mode: Static
15:13	RO	0x0	reserved
12:8	RW	0x00	addrmap_row_b11 Selects the HIF address bit used as row address bit 11. Valid Range: 0 to 16 Internal Base: 17 The selected HIF address bit is determined by adding the internal base to the value of this field. Value After Reset: 0x0 Programming Mode: Static
7:5	RO	0x0	reserved
4:0	RW	0x00	addrmap_row_b10 Selects the HIF address bits used as row address bit 10. Valid Range: 0 to 16 Internal Base: 16 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_ADDRMAP9

Address: **Operational Base** + offset (0x30024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	addrmap_row_b9 Selects the HIF address bits used as row address bit 9. Valid Range: 0 to 16 Internal Base: 15 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset: 0x0 Programming Mode: Static
23:21	RO	0x0	reserved
20:16	RW	0x00	addrmap_row_b8 Selects the HIF address bits used as row address bit 8. Valid Range: 0 to 16 Internal Base: 14 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset: 0x0 Programming Mode: Static
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	addrmap_row_b7 Selects the HIF address bits used as row address bit 7. Valid Range: 0 to 16 Internal Base: 13 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset: 0x0 Programming Mode: Static
7:5	RO	0x0	reserved
4:0	RW	0x00	addrmap_row_b6 Selects the HIF address bits used as row address bit 6. Valid Range: 0 to 16 Internal Base: 12 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_ADDRMAP10

Address: **Operational Base** + offset (0x30028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	addrmap_row_b5 Selects the HIF address bits used as row address bit 5. Valid Range: 0 to 16 Internal Base: 11 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset: 0x0 Programming Mode: Static
23:21	RO	0x0	reserved
20:16	RW	0x00	addrmap_row_b4 Selects the HIF address bits used as row address bit 4. Valid Range: 0 to 16 Internal Base: 10 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset: 0x0 Programming Mode: Static
15:13	RO	0x0	reserved
12:8	RW	0x00	addrmap_row_b3 Selects the HIF address bits used as row address bit 3. Valid Range: 0 to 16 Internal Base: 9 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset: 0x0 Programming Mode: Static
7:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	addrmap_row_b2 Selects the HIF address bits used as row address bit 2. Valid Range: 0 to 16 Internal Base: 8 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_ADDRMAP11

Address: **Operational Base** + offset (0x3002C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	addrmap_row_b1 Selects the HIF address bits used as row address bit 1. Valid Range: 0 to 16 Internal Base: 7 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset: 0x0 Programming Mode: Static
7:5	RO	0x0	reserved
4:0	RW	0x00	addrmap_row_b0 Selects the HIF address bits used as row address bit 0. Valid Range: 0 to 16 Internal Base: 6 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_ADDRMAP12

Address: **Operational Base** + offset (0x30030)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	nonbinary_device_density Indicates what type of SDRAM device is in use. 3'b000: All addresses are valid. 3'b001: Every address having row[13:12]==2'b11 is considered as invalid. 3'b010: Every address having row[14:13]==2'b11 is considered as invalid. 3'b011: Every address having row[15:14]==2'b11 is considered as invalid. 3'b100: Every address having row[16:15]==2'b11 is considered as invalid. 3'b101: Every address having row[17:16]==2'b11 is considered as invalid. Value After Reset: 0xf0 Programming Mode: Static

DDRCTL_DRAMSET1TMG0_FREQ1

Address: **Operational Base** + offset (0x100000)

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Bit	Attr	Reset Value	Description
31:24	RW	0x0f	wr2pre Minimum time between write and precharge to same bank. Specifications: WL + BL/2 + tWR where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present. tWR = Write recovery time. This comes directly from the SDRAM specification. Add one extra cycle for LPDDR4/5 for this parameter. Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
23:16	RW	0x10	t_faw tFAW: At most 4 banks must be activated in a rolling window of tFAW cycles. Unit: DRAM clock cycles. Value After Reset: 0x10 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:8	RW	0x1b	t_ras_max tRAS(max): Maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open t_ras_max must be set to RoundDown(tRAS(max)/tCK/1024). Unit: 1024 DRAM clock cycles. Value After Reset: 0x1b Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:0	RW	0x0f	t_ras_min tRAS(min): Minimum time between activate and precharge to the same bank. Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG1_FREQ1

Address: **Operational Base** + offset (0x100004)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x08	t_xp tXP: Minimum time after power-down exit to any operation. LPDDR4 (tCKELPD is defined in spec): larger of tXP and tCKELPD instead. LPDDR4 (tCKELPD is not defined in spec): tXP. LPDDR5: tXP + tCSH Unit: DRAM clock cycles. Value After Reset: 0x8 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

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Bit	Attr	Reset Value	Description
15:8	RW	0x04	rd2pre tRTP: Minimum time from read to precharge of same bank. LPDDR4 - BL/2 + max(RoundUp(tRTP/tCK),8) - 8 LPDDR5(BG mode): BL/n_min + RU(tRBTP/tCK) LPDDR5(16B mode): BL/n + RU(tRBTP/tCK) Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x14	t_rc tRC: Minimum time between activates to same bank. Unit: DRAM clock cycles. Value After Reset: 0x14 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG2_FREQ1

Address: **Operational Base** + offset (0x100008)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x03	write_latency Set to WL Time from write command to write data on SDRAM interface. This must be set to WL. For all protocols, in addition to programming this register field, it is necessary to program DDRCTL_DFITMG0_FREQ1 and DDRCTL_DFITMG1_FREQ1 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset: 0x3 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
23	RO	0x0	reserved
22:16	RW	0x05	read_latency Set to RL Time from read command to read data on SDRAM interface. This must be set to RL. In addition to programming this register field, it is necessary to program DDRCTL_DFITMG0_FREQ1 and DDRCTL_DFITMG1_FREQ1 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x06	rd2wr LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled) : RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (BG mode && DQ ODT is Disabled): RL + BL/n_max + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (BG mode && DQ ODT is Enabled) : RL + BL/n_max + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (16B mode && DQ ODT is Disabled): RL + BL/n + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (16B mode && DQ ODT is Enabled) : RL + BL/n +

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Bit	Attr	Reset Value	Description
			RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 Minimum time from read command to write command. Include time for bus turnaround and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM RL = read latency = CAS latency WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). RD_POSTAMBLE = 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR4, if derating is enabled (DDRCTL_DERATECTL0_FREQ1.derate_enable=1), derated tDQSCKmax must be used. Unit: DRAM clock cycles. Value After Reset: 0x6 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x0d	wr2rd LPDDR4: WL + BL/2 + tWTR + 1 LPDDR5(BG mode): WL + BL/n_max + RU(tWTR_L/tCK) LPDDR5(16B mode): WL + BL/n + RU(tWTR/tCK) Minimum time from write command to read command. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: CWL = CAS write latency WL = Write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_L = internal write to read command delay for same bank group. This comes directly from the SDRAM specification. tWTR = internal write to read command delay. This comes directly from the SDRAM specification. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Add one extra cycle for LPDDR4 operation. Unit: DRAM clock cycles. Value After Reset: 0xd Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG3_FREQ1

Address: **Operational Base** + offset (0x10000C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:16	RW	0x04	t_mr Time from MRW/MRS to valid command LPDDR4: Set this to the larger of tMRR, tMRW, tMRWCKEL and tMRD. LPDDR5: Set this to the larger of tMRR, tMRW, tMRWPD and tMRD. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:8	RW	0x04	rd2mr Time from Read to MRW/MRR command. LPDDR4: RL + BL/2 + RU(tDQSCKmax/tCK) + RD(tRPST) + max(RU(7.5ns/tCK),8nCK) + nRTP - 8 LPDDR5: RL + RU(tWCKDQO(max)/tCK)) + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nRBTP Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:0	RW	0x04	wr2mr Time from Write to MRW/MRR command. LPDDR4: WL + 1 + BL/2 + max(RU(7.5ns/tCK),8nCK) + nWR LPDDR5: WL + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nWR Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG4_FREQ1

Address: **Operational Base** + offset (0x100010)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	t_rcd tRCD - tAL: Minimum time from activate to read or write command to same bank. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
23:22	RO	0x0	reserved
21:16	RW	0x04	t_ccd This is the minimum time between two reads or two writes. LPDDR4: tCCD LPDDR5: BL/n Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x04	t_rrd For LPDDR5(BG mode): Minimum time between activates from bank "a" to bank "b" for same bank group. For LPDDR4/LPDDR5(16B mode): Minimum time between activates from bank "a" to bank "b". LPDDR4: RU(tRRD/tCK) LPDDR5(BG mode): RU(tRRD_L/tCK) LPDDR5(16B mode): RU(tRRD/tCK) Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7	RO	0x0	reserved
6:0	RW	0x05	t_rp tRP: Minimum time from single-bank precharge to activate of same bank. t_rp must be set to RoundUp(tRP/tCK). Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG5_FREQ1

Address: **Operational Base** + offset (0x100014)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x05	t_cksrx This is the time before Self Refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: LPDDR4: tCKCKEH LPDDR5: tCKCSH Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
23	RO	0x0	reserved
22:16	RW	0x05	t_cksre This is the time after Self Refresh Down Entry/Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE/PDE. Recommended settings: LPDDR4: tCKELCK LPDDR5: tCSLCK Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:8	RW	0x04	t_ckesr Minimum CKE low width for Self refresh or Self refresh power down entry to exit timing in memory clock cycles. Recommended settings: LPDDR4: Max(tCKE, tSR) LPDDR5: tSR Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:6	RO	0x0	reserved
5:0	RW	0x03	t_cke Delay time between PDE and PDX. LPDDR4: tCKE LPDDR5: tCSPD Unit: DRAM clock cycles. Value After Reset: 0x3 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG6_FREQ1

Address: **Operational Base** + offset (0x100018)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x05	t_ckcsx This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit. Recommended settings: LPDDR4/5: tXP + 2 This is only present for designs supporting LPDDR devices. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG7_FREQ1

Address: **Operational Base** + offset (0x10001C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	t_csh CS High Pulse width at PDX LPDDR5: tCSH Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG8_FREQ1

Address: **Operational Base** + offset (0x100020)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x44	t_xs_dll_x32 tXSDLL: Exit Self Refresh to commands requiring a locked DLL. Note: Not used for LPDDR4/LPDDR5 SDRAMs.

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Bit	Attr	Reset Value	Description
7	RO	0x0	reserved
6:0	RW	0x05	t_xs_x32 tXS: Exit Self Refresh to commands not requiring a locked DLL. Note: Not used for LPDDR4/5 SDRAMs.

DDRCTL_DRAMSET1TMG9_FREQ1

Address: **Operational Base** + offset (0x100024)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x04	t_ccd_s tCCD_S: This is the minimum time between two reads or two writes for different bank group. For bank switching (from bank "a" to bank "b"), the minimum time is this value + 1. Note: This register field is only applicable for designs supporting LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:14	RO	0x0	reserved
13:8	RW	0x04	t_rrd_s tRRD_S: Minimum time between activates from bank "a" to bank "b" for different bank group. Note: This register field is only applicable for designs supporting LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:0	RW	0x0d	wr2rd_s Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Applicable only in designs configured to support LPDDR5 SDRAM memories. LPDDR5 designs: WL + BL/n_min +RU(tWTR_S/tCK) Where: WL = Write Latency BL/n_min = Effective Burst Length tWTR_S = internal write to read command delay for different bank group. Unit: DRAM clock cycles. Value After Reset: 0xd Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG12_FREQ1

Address: **Operational Base** + offset (0x100030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
19:16	RW	0x2	t_cmdcke tCMDCKE: Delay from valid command to PDE LPDDR4: Max(tESCKE, tCMDCKE) LPDDR5: Max(tESPD, tCMDPD) Unit: DRAM clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:0	RO	0x0000	reserved

DDRCTL_DRAMSET1TMG13_FREQ1

Address: **Operational Base** + offset (0x100034)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x1c	odtloff LPDDR4: ODTLoff: This is the latency from CAS-2 command to ODToff reference. Note: This register field is only applicable for designs supporting LPDDR4 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x1c Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
23	RO	0x0	reserved
22:16	RW	0x20	t_ccd_mw This is the minimum time from write or masked write to masked write command for same bank. LPDDR4: tCCDMW LPDDR5(BG mode): 4*BL/n_max LPDDR5(16B mode): 4*BL/n Note: This register field is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x20 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:4	RO	0x000	reserved
3:0	RW	0x4	t_ppd LPDDR4/5: tPPD: This is the minimum time from precharge to precharge command. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG14_FREQ1

Address: **Operational Base** + offset (0x100038)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24:16	RW	0x008	t_osco tosco: Minimum time from DQS Oscillator stop to Mode register readout. LPDDR4 : max(40ns,8nck) LPDDR5A: tOSCODQI=tOSCODQO=max(40ns,8nck) Unit: DRAM clock cycles. Value After Reset: 0x8 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:12	RO	0x0	reserved
11:0	RW	0x0a0	t_xsr tXSR: Exit Self Refresh to any command. The value 0xfff is illegal for this register field. Unit: DRAM clock cycles. Value After Reset: 0xa0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG23_FREQ1

Address: **Operational Base** + offset (0x10005C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	t_xsr_dsm_x1024 Delay from Deep Sleep Mode Exit to SRX. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related
15:12	RO	0x0	reserved
11:0	RW	0x000	t_pdn Minimum interval between Deep Sleep Mode Entry and Exit. Unit: DRAM clock cycles. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related

DDRCTL_DRAMSET1TMG24_FREQ1

Address: **Operational Base** + offset (0x100060)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RW	0x0	bank_org Select Bank/ Bank group organization: 2'b00: 4 Banks/ 4 Bank groups 2'b01: 8 Banks 2'b10: 16 Banks 2'b11: Reserved Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

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Bit	Attr	Reset Value	Description
23:16	RW	0x0f	rd2wr_s Minimum time from read command to write command for different bank group. Includes time for bus turnaround, recovery times and all per-bank, per-rank and global constraints. LPDDR5(DQ ODT is disabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) - WL LPDDR5(DQ ODT is enabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x0f	max_rd_sync Minimum time from read command to WCK2CK sync OFF. RL + BL/n_max + RU(tRPST/tCK) Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x0f	max_wr_sync Minimum time from write command to WCK2CK sync OFF. WL + BL/n_max Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG25_FREQ1

Address: **Operational Base** + offset (0x100064)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:16	RW	0x0	lpddr4_diff_bank_rwa2pre Set the timing constraint between different bank RD/WR/MWR/ACT and PRE in LPDDR4. LPDDR4 JESD209-4A requires 4 cycles LPDDR4 JESD209-4B requires 2 cycles Value of 1, 3, 5, 6, and 7 are illegal. Don't care for LPDDR5. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x00	wra2pre Time between write with AP and precharge to same bank. LPDDR4: WL + BL/2 + nWR + 1 LPDDR5: WL + BL/n_min + nWR + 1 Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	rda2pre Time between read with AP and precharge to same bank. LPDDR4: nRTP LPDDR5: BL/n_min + nRBTP Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG30_FREQ1

Address: **Operational Base** + offset (0x100078)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mrr2mrw MRR to MRW delay Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:8	RW	0x00	mrr2wr MRR to WR delay Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:0	RW	0x00	mrr2rd MRR to RD delay Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR0_FREQ1

Address: **Operational Base** + offset (0x100500)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr LPDDR4: Value to write to MR1 register Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:0	RW	0x0510	emr LPDDR4: Value to write to MR2 register Value After Reset: 0x510 Volatile: True Programming Mode: Quasi-dynamic Group 4

DDRCTL_INITMR1_FREQ1

Address: **Operational Base** + offset (0x100504)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	emr2 LPDDR4: Value to write to MR3 register Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	emr3 LPDDR4: Value to write to MR13 register Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR2_FREQ1

Address: **Operational Base** + offset (0x100508)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr4 LPDDR4: Value to be loaded into SDRAM MR11 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	mr5 LPDDR4: Value to be loaded into SDRAM MR12 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4

DDRCTL_INITMR3_FREQ1

Address: **Operational Base** + offset (0x10050C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr22 LPDDR4 Value to be loaded into SDRAM MR22 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4
15:0	RW	0x0000	mr6 LPDDR4 Value to be loaded into SDRAM MR14 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4

DDRCTL_DFITMG0_FREQ1

Address: **Operational Base** + offset (0x100580)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x07	dfi_t_ctrl_delay Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DRAM clock and the memory clock are not phase-aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x7 Volatile: True Programming Mode: Quasi-dynamic Group 4

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Bit	Attr	Reset Value	Description
23	RO	0x0	reserved
22:16	RW	0x02	dfi_t_rddata_en Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:14	RO	0x0	reserved
13:8	RW	0x00	dfi_tphy_wrdata Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. Refer to PHY specification for correct value. Note, max supported value is 8. Unit: DRAM data clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4
7:6	RO	0x0	reserved
5:0	RW	0x02	dfi_tphy_wrlat Write latency Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value. For LPDDR4, dfi_tphy_wrlat>60 is not supported. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DFITMG1_FREQ1

Address: **Operational Base** + offset (0x100584)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	dfi_t_wrdata_delay Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. For LPDDR5, this should be set to "twck_delay + BL/n_max - BL/n_min" instead of twrdata_delay. twck_delay specifies the time from dfi_wck_en deassertion to when WCK transfer completes on the DRAM bus and is defined by the PHY Refer to PHY specification for correct value. When DDRCTL_TMGCFG_FREQ1.frequency_ratio is set to 0(1:2 Mode), divided the value by 2 and round it up to the next integer value. When DDRCTL_TMGCFG_FREQ1.frequency_ratio is set to 1(1:4 Mode), divided the value by 4 and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x0

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Bit	Attr	Reset Value	Description
			Volatile: True Programming Mode: Quasi-dynamic Group 4
15:13	RO	0x0	reserved
12:8	RW	0x04	dfi_t_dram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 4
7:5	RO	0x0	reserved
4:0	RW	0x04	dfi_t_dram_clk_enable Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 4

DDRCTL_DFITMG2_FREQ1

Address: **Operational Base** + offset (0x100588)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	dfi_twck_delay Number of DFI PHY clock cycles from dfi_wck_en is de-asserted to when the WCK transfer completes on the DRAM bus. Refer to PHY specification for correct value. Unit: DFI PHY clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15	RO	0x0	reserved
14:8	RW	0x02	dfi_tphy_rdcslat Number of DFI PHY clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x02	dfi_tphy_wrcslat Number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DFITMG4_FREQ1

Address: **Operational Base** + offset (0x100590)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_en_rd WCK Enable Read Timing. Defines the timing from the CAS-WS_RD command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_en_wr WCK Enable Read Timing. Defines the timing from the CAS-WS_WR command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_en_fs WCK Enable Fast Sync Timing. Defines the timing from the CAS-WS_FS command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset: 0x0 Programming Mode: Quasi-dynamic Group 1, Group 4
7:0	RW	0x00	dfi_twck_dis WCK Off Timing. Defines the timing from the last command opportunity to the deassertion of dfi_wck_en and dfi_wck_toggle_en assuming that no command is being sent. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4

DDRCTL_DFITMG5_FREQ1

Address: **Operational Base** + offset (0x100594)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_fast_toggle Defines the number of clock cycles between the dfi_wck_signal being driven to TOGGLE to when the dfi_wck_signal is driven to FAST_TOGGLE. This timing is only applicable when the WCK transitions from the slow to fast toggle. Otherwise, this timing parameter must be set to 0x0. Unit: WCK cycles Value After Reset: 0x0

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Bit	Attr	Reset Value	Description
			Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_toggle WCK Toggle Enable Timing. Defines the timing from dfi_wck_en assertion to dfi_wck_toggle_en assertion. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_toggle_cs Defines the number of clock cycles between a read or write command to when the dfi_wck_cs signal must be stable. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
7:0	RW	0x00	dfi_twck_toggle_post Defines the number of clock cycles after a read or write command data burst completion during which the WCK must remain in the current toggle state. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4

DDRCTL_DFIUPDTMG1_FREQ1

Address: **Operational Base** + offset (0x1005AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x01	dfi_t_ctrlupd_interval_min_x1024 This is the minimum amount of time between DDRCTL initiated DFI update requests (which is executed whenever the DDRCTL is idle). Set this number higher to reduce the frequency of update requests, which can have a small impact on the latency of the first read request when the DDRCTL is idle. Minimum allowed value for this field is 1. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x01 Programming Mode: Static
15:8	RO	0x00	reserved
7:0	RW	0x01	dfi_t_ctrlupd_interval_max_x1024 This is the maximum amount of time between DDRCTL initiated DFI update requests. This timer resets with each update request; when the timer expires dfi_ctrlupd_req is sent and traffic is blocked until the dfi_ctrlupd_ackx is received. PHY can use this idle time to recalibrate the delay lines to the DLLs. The DFI controller update is also used to reset PHY FIFO pointers in case of data capture errors. Updates are required to maintain calibration over PVT, but frequent updates may impact performance. Minimum allowed value for this field is 1. Note: Value programmed for dfi_t_ctrlupd_interval_max_x1024 must be greater than dfi_t_ctrlupd_interval_min_x1024. Unit: Multiples of 1024 DFI clock cycles.

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Bit	Attr	Reset Value	Description
			Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x01 Programming Mode: Static

DDRCTL_RFSHSET1TMG0_FREQ1

Address: **Operational Base** + offset (0x100600)

Bit	Attr	Reset Value	Description
31	RW	0x0	t_refi_x1_sel Specifies whether DDRCTL_RFSHSET1TMG0_FREQ1.t_refi_x1_x32 and DDRCTL_RFSHSET1TMG0_FREQ1.refresh_to_x1_x32 register values are x1 or x32. 1'b0: x32 register values are used. 1'b1: Register values are used. This applies only when per-bank refresh is enabled (DDRCTL_RFSHMOD0.per_bank_refresh=1). If per-bank refresh is not enabled, the x32 register values are used and this register field is ignored. This register field does not exist for configurations which do not support LPDDR4/5. For such configurations, the value of this register field can be assumed to be 0, so that DDRCTL_RFSHSET1TMG0_FREQ1.t_refi_x1_x32 and DDRCTL_RFSHSET1TMG0_FREQ1.refresh_to_x1_x32 are interpreted as x32 register fields Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related
30:28	RO	0x0	reserved
27:24	RW	0x2	refresh_margin Threshold value in number of DRAM clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_refi/32. Note that internally used t_refi is equal to DDRCTL_RFSHSET1TMG0_FREQ1.t_refi_x1_x32 * 32 if DDRCTL_RFSHSET1TMG0_FREQ1.t_refi_x1_sel = 0. If DDRCTL_RFSHSET1TMG0_FREQ1.t_refi_x1_sel = 1, internally used t_refi is equal to DDRCTL_RFSHSET1TMG0_FREQ1.t_refi_x1_x32. Note that, internally used t_refi may be divided by four if derating or TCR is enabled. Unit: Multiples of 32 DRAM clock cycles. Value After Reset: 0x2 Programming Mode: Dynamic - Refresh Related
23:22	RO	0x0	reserved
21:16	RW	0x10	refresh_to_x1_x32 If the refresh timer has expired at least once (i.e. >tREFI period elapses, and there are postponed refreshes), then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful. When there are no transactions pending in the CAM for a period of time determined by this DDRCTL_RFSHSET1TMG0_FREQ1.refresh_to_x1_x32 and the refresh timer has expired at least once since the last refresh,

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Bit	Attr	Reset Value	Description
			then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the DDRCTL. This is also used for non speculative refresh when LPDDR per-bank refresh (REFpb) is enabled. The controller observes the period of time determined by this for each bank, and a priority of bank address is determined. This should be programmed to tREFI based value in controller's current refresh mode. The controller calculates this according to current refresh mode. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on DDRCTL_RFSHSET1TMG0_FREQ1.t_refi_x1_sel. Value After Reset: 0x10 Programming Mode: Dynamic - Refresh Related
15:12	RO	0x0	reserved
11:0	RW	0x062	t_refi_x1_x32 Average time interval between refreshes per rank (See JEDEC specification for LPDDR4). Set this register to RoundDown(tREFI/tCK). If DDRCTL_RFSHSET1TMG0_FREQ1.t_refi_x1_sel = 0, divide the above result by 32 and round down. For LPDDR controller: If using all-bank refreshes (DDRCTL_RFSHMOD0.per_bank_refresh = 0), use tREFIab in the above calculations. If using per-bank refreshes (DDRCTL_RFSHMOD0.per_bank_refresh = 1), use tREFIpb in the above calculations. Note that: DDRCTL_RFSHSET1TMG0_FREQ1.t_refi_x1_x32 must be greater than 0x1. If DDRCTL_RFSHSET1TMG0_FREQ1.t_refi_x1_sel == 1, DDRCTL_RFSHSET1TMG0_FREQ1.t_refi_x1_x32 must be greater than DDRCTL_RFSHSET1TMG1_FREQ1.t_rfc_min If DDRCTL_RFSHSET1TMG0_FREQ1.t_refi_x1_sel == 0, DDRCTL_RFSHSET1TMG0_FREQ1.t_refi_x1_x32 * 32 must be greater than DDRCTL_RFSHSET1TMG1_FREQ1.t_rfc_min DDRCTL_RFSHSET1TMG0_FREQ1.t_refi_x1_x32 must be less than or equal to 0xFFE. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on DDRCTL_RFSHSET1TMG0_FREQ1.t_refi_x1_sel. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x62 Programming Mode: Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG1_FREQ1

Address: **Operational Base** + offset (0x100604)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x08c	t_rfc_min tRFC (min): Minimum time from refresh to refresh or activate. t_rfc_min must be set to RoundUp(tRFCmin/tCK). In LPDDR controller, if using all-bank refreshes, the tRFCmin value in the above equations is equal to tRFCab. If using per-bank refreshes, the tRFCmin value in the above equations is equal to tRFCpb. Unit: DRAM clock cycles. Value After Reset: 0x8c Programming Mode: Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG2_FREQ1

Address: **Operational Base** + offset (0x100608)

Bit	Attr	Reset Value	Description
31:24	RW	0x8c	t_pbr2act Time from REFpb to activate command to different bank than REFpb. LPDDR5: tpbr2act Value After Reset: 0x8c Programming Mode: Dynamic - Refresh Related
23:16	RW	0x8c	t_pbr2pbr LPDDR4: tpbR2pbR Per-bank Refresh to Per-bank refresh different bank Time. Program this to RoundUp(tpbR2pbR/tCK). The tpbR2pbR value in the above equations is different depending on the device density. The user must program the appropriate value from the spec. Register is valid only in LPDDR4 per-bank refresh mode (DDRCTL_RFSHMOD0.per_bank_refresh == 1). Value After Reset: 0x8c Programming Mode: Dynamic - Refresh Related
15:0	RO	0x0000	reserved

DDRCTL_RFSHSET1TMG4_FREQ1

Address: **Operational Base** + offset (0x100610)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	refresh_timer1_start_value_x32 Refresh timer start for rank 1 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	refresh_timer0_start_value_x32 Refresh timer start for rank 0 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related

DDRCTL_ZQSET1TMG0_FREQ1

Address: **Operational Base** + offset (0x100800)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x040	t_zq_short_nop tZQLAT for LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset: 0x40 Programming Mode: Static
15:14	RO	0x0	reserved
13:0	RW	0x0200	t_zq_long_nop tZQCAL for LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM. If using LPDDR5, this register needs to be programmed to tZQCAL + 10 cycles. Unit: DRAM clock cycles. Value After Reset: 0x200 Programming Mode: Static

DDRCTL_ZQSET1TMG1_FREQ1

Address: **Operational Base** + offset (0x100804)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x020	t_zq_reset_nop tZQReset: Number of DRAM clock cycles of NOP required after a ZQReset (ZQ calibration Reset) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset: 0x20 Programming Mode: Static
19:0	RW	0x00100	t_zq_short_interval_x1024 Average interval to wait between automatically issuing ZQCS (ZQ calibration short)/MPC(ZQ calibration) commands to LPDDR4 devices. Meaningless, if DDRCTL_ZQCTL0.dis_auto_zq=1. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x100 Programming Mode: Static

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DDRCTL_DQSOSCCTL0_FREQ1

Address: **Operational Base** + offset (0x100A80)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RW	0x007	dqsosc_interval DQS Oscillator interval, specifies the time between two DQS oscillator sequences. Minimum programmable value is 1. The value can be changed while DQSOSCCTL0.dqsosc_enable=0 Unit: DFI clock cycles Value After Reset: 0x7 Programming Mode: Dynamic
3	RO	0x0	reserved
2	RW	0x0	dqsosc_interval_unit DQS/WCK Oscillator Interval unit. Specifies the unit for counting DQS oscillator interval. The value can be changed while DQSOSCCTL0.dqsosc_enable=0 1'b1: x2K DFI clock cycles 1'b0: x32K DFI clock cycles Value After Reset: 0x0 Programming Mode: Dynamic
1	RO	0x0	reserved
0	RW	0x0	dqsosc_enable DQS/WCK Oscillator Enable 1'b1: Enable DQS Oscillator 1'b0: Disable DQS Oscillator Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_DERATEINT_FREQ1

Address: **Operational Base** + offset (0x100B00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00800000	mr4_read_interval Interval between two MR4 reads, used to derate the timing parameters. This register must not be set to zero. Unit: DRAM clock cycles. Value After Reset: 0x800000 Volatile: True Programming Mode: Static

DDRCTL_DERATEVAL0_FREQ1

Address: **Operational Base** + offset (0x100B04)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	derated_t_rcd Derated value for tRCD. For LPDDR4, the required period with derating is tRCD + 1.875ns For LPDDR5, the required period with derating is tRCD + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

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Bit	Attr	Reset Value	Description
23:16	RW	0x0f	derated_t_ras_min Derated value for tRAS. For LPDDR4, the required period with derating is tRAS + 1.875ns For LPDDR5, the required period with derating is tRAS + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15	RO	0x0	reserved
14:8	RW	0x05	derated_t_rp Derated value for tRP. For LPDDR4, the required period with derating is tRP + 1.875ns For LPDDR5, the required period with derating is tRP + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:6	RO	0x0	reserved
5:0	RW	0x04	derated_t_rrd Derated value for tRRD. For LPDDR4, the required period with derating is tRRD + 1.875ns For LPDDR5, the required period with derating is tRRD + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DERATEVAL1_FREQ1

Address: **Operational Base** + offset (0x100B08)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x14	derated_t_rc Derated value for tRC. For LPDDR4, the required period with derating is tRC + 3.75ns For LPDDR5, the required period with derating is tRC + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x14 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_HWLPTMG0_FREQ1

Address: **Operational Base** + offset (0x100B80)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x000	hw_lp_idle_x32 Hardware idle period. The cactive_ddrc output is driven low if the DDRC command channel is idle for hw_lp_idle * 32 cycles if not in INIT or DPD/MPSM operating_mode. The DDRC command channel is considered idle when there are no HIF commands outstanding. The hardware idle function is disabled when hw_lp_idle_x32=0. hw_lp_idle_x32=1 is an illegal value when the controller is in 1:2 mode. hw_lp_idle_x32=1/2/3 are illegal values when the controller is in 1:4 mode. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Volatile: True Programming Mode: Static
15:0	RO	0x0000	reserved

DDRCTL_SCHEDTMG0_FREQ1

Address: **Operational Base** + offset (0x100C00)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x00	rdwr_idle_gap When the preferred transaction store is empty for these many clock cycles, switch to the alternate transaction store if it is non-empty. The read transaction store (both high and low priority) is the default preferred transaction store and the write transaction store is the alternative store. When prefer write over read is set this is reversed. 0x0 is a legal value for this register. When set to 0x0, the transaction store switching will happen immediately when the switching conditions become true. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x0 Programming Mode: Static
7:0	RW	0x00	pageclose_timer This field works in conjunction with DDRCTL_SCHED0.pageclose. It only has meaning if DDRCTL_SCHED0.pageclose==1. If DDRCTL_SCHED0.pageclose==1 and pageclose_timer==0, then an auto-precharge may be scheduled for last read or write command in the CAM with a bank and page hit. Note, sometimes an explicit precharge is scheduled instead of the auto-precharge. See DDRCTL_SCHED0.pageclose for details of when this may happen. If DDRCTL_SCHED0.pageclose==1 and pageclose_timer>0, then an auto-precharge is not scheduled for last read or write command in the CAM with a bank and page hit. Instead, a timer is started, with pageclose_timer as the initial value. There is a timer on a per bank basis. The timer decrements unless the next read or write in the CAM to a bank is a page hit. It gets reset to pageclose_timer value if the next read or write in the CAM to a bank is a page hit. Once the timer has reached

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Bit	Attr	Reset Value	Description
			zero, an explcit precharge will be attempted to be scheduled. Unit: DRAM clock cycles. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_PERFHPR1_FREQ1

Address: **Operational Base** + offset (0x100C80)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	hpr_xact_run_length Number of transactions that are serviced once the HPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available Unit: Transaction FOR PERFORMANCE ONLY. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x00	reserved
15:0	RW	0x0001	hpr_max_starve Number of DRAM clocks that the HPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x1 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PERFLPR1_FREQ1

Address: **Operational Base** + offset (0x100C84)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	lpr_xact_run_length Number of transactions that are serviced once the LPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available Unit: Transaction FOR PERFORMANCE ONLY. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x00	reserved
15:0	RW	0x007f	lpr_max_starve Number of DRAM clocks that the LPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x7f Volatile: True Programming Mode: Quasi-dynamic Group 3

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DDRCTL_PERFWR1_FREQ1

Address: **Operational Base** + offset (0x100C88)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	w_xact_run_length Number of transactions that are serviced once the WR queue goes critical is the smaller of: (a) This number (b) Number of transactions available Unit: Transaction FOR PERFORMANCE ONLY. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x00	reserved
15:0	RW	0x007f	w_max_starve Number of DRAM clocks that the WR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x7f Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_TMGCFG_FREQ1

Address: **Operational Base** + offset (0x100D00)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	dfi_freq_fsp This register value propergates to dfi_freq_fsp pin directly. Value After Reset: 0x0 Programming Mode: Dynamic
7:1	RO	0x00	reserved
0	RW	0x0	frequency_ratio Selects the Frequency Ratio For LPDDR4: 1'b0: 1:2 Mode 1'b1: 1:4 Mode For LPDDR5: 1'b0: 1:1:2 Mode 1'b1: 1:1:4 Mode Value After Reset: 0x0 Programming Mode: Quasi-dynamic Group 2

DDRCTL_RANKTMG0_FREQ1

Address: **Operational Base** + offset (0x100D04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:8	RW	0x06	diff_rank_wr_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_wrcsgap (see PHY databook for value of tphy_wrcsgap) If CRC feature is enabled, must be increased by 1. Write preamble is always set to 2tCK for LPDDR4, refer to PHY databook to see if this is already factored into tphy_wrcsgap value or if it needs to be increased by 1. If write postamble is set to 1.5tCK(LPDDR4 only), must be increased by 1. ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, with DQ ODT enabled, diff_rank_wr_gap must be a minimum of ODTLoff - ODTLon - BL/2 + 1 For other cases, diff_rank_wr_gap must be a minimum of ODTCFG.wr_odt_hold - BL/2. Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay". Please see PHY databook for the value of tphy_wckcsgap. Unit: DRAM clock cycles. Value After Reset: 0x6 Volatile: True Programming Mode: Quasi-dynamic Group 2
7:0	RW	0x06	diff_rank_rd_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_rdcsgap (see PHY databook for value of tphy_rdcsgap) ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads: Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay". Please see PHY databook for the value of tphy_wckcsgap. Unit: DRAM clock cycles. Value After Reset: 0x6

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Bit	Attr	Reset Value	Description
			Volatile: True Programming Mode: Quasi-dynamic Group 2

DDRCTL_RANKTMG1_FREQ1

Address: **Operational Base** + offset (0x100D08)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x0f	rd2wr_dr Minimum time from read command to write command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. The value must be larger than or equal to the value of DRAMSET1TMG2.rd2wr. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay". Please see PHY databook for the value of tphy_wckcsgap. Unit: DRAM clock cycles Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x0f	wr2rd_dr Minimum time from write command to read command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay". Please see PHY databook for the value of tphy_wckcsgap. Unit: DRAM clock cycles Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_PWRTMG_FREQ1

Address: **Operational Base** + offset (0x100D0C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x040	selfref_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into Self Refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x40 Volatile: True Programming Mode: Quasi-dynamic Group 4
15:7	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
6:0	RW	0x10	powerdown_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into power-down. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x10 Volatile: True Programming Mode: Quasi-dynamic Group 4

DDRCTL_DRAMSET1TMG0_FREQ2

Address: **Operational Base** + offset (0x200000)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	wr2pre Minimum time between write and precharge to same bank. Specifications: WL + BL/2 + tWR where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present. tWR = Write recovery time. This comes directly from the SDRAM specification. Add one extra cycle for LPDDR4/5 for this parameter. Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
23:16	RW	0x10	t_faw tFAW: At most 4 banks must be activated in a rolling window of tFAW cycles. Unit: DRAM clock cycles. Value After Reset: 0x10 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:8	RW	0x1b	t_ras_max tRAS(max): Maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open t_ras_max must be set to RoundDown(tRAS(max)/tCK/1024). Unit: 1024 DRAM clock cycles. Value After Reset: 0x1b Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

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Bit	Attr	Reset Value	Description
7:0	RW	0x0f	t_ras_min tRAS(min): Minimum time between activate and precharge to the same bank. Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG1_FREQ2

Address: **Operational Base** + offset (0x200004)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x08	t_xp tXP: Minimum time after power-down exit to any operation. LPDDR4 (tCKELPD is defined in spec): larger of tXP and tCKELPD instead. LPDDR4 (tCKELPD is not defined in spec): tXP. LPDDR5: tXP + tCSH Unit: DRAM clock cycles. Value After Reset: 0x8 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:8	RW	0x04	rd2pre tRTP: Minimum time from read to precharge of same bank. LPDDR4 - BL/2 + max(RoundUp(tRTP/tCK),8) - 8 LPDDR5(BG mode): BL/n_min + RU(tRBTP/tCK) LPDDR5(16B mode): BL/n + RU(tRBTP/tCK) Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x14	t_rc tRC: Minimum time between activates to same bank. Unit: DRAM clock cycles. Value After Reset: 0x14 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG2_FREQ2

Address: **Operational Base** + offset (0x200008)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x03	write_latency Set to WL Time from write command to write data on SDRAM interface. This must be set to WL. For all protocols, in addition to programming this register field, it is necessary to program DDRCTL_DFITMG0_FREQ2 and DDRCTL_DFITMG1_FREQ2 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset: 0x3 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
23	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
22:16	RW	0x05	read_latency Set to RL Time from read command to read data on SDRAM interface. This must be set to RL. In addition to programming this register field, it is necessary to program DDRCTL_DFITMG0_FREQ2 and DDRCTL_DFITMG1_FREQ2 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x06	rd2wr LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled) : RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (BG mode && DQ ODT is Disabled): RL + BL/n_max + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (BG mode && DQ ODT is Enabled) : RL + BL/n_max + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (16B mode && DQ ODT is Disabled): RL + BL/n + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (16B mode && DQ ODT is Enabled) : RL + BL/n + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 Minimum time from read command to write command. Include time for bus turnaround and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM RL = read latency = CAS latency WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). RD_POSTAMBLE = 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR4, if derating is enabled (DDRCTL_DERATECTL0_FREQ2.derate_enable=1), derated tDQSCKmax must be used. Unit: DRAM clock cycles. Value After Reset: 0x6 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

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Bit	Attr	Reset Value	Description
7:0	RW	0x0d	wr2rd LPDDR4: WL + BL/2 + tWTR + 1 LPDDR5(BG mode): WL + BL/n_max + RU(tWTR_L/tCK) LPDDR5(16B mode): WL + BL/n + RU(tWTR/tCK) Minimum time from write command to read command. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: CWL = CAS write latency WL = Write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_L = internal write to read command delay for same bank group. This comes directly from the SDRAM specification. tWTR = internal write to read command delay. This comes directly from the SDRAM specification. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Add one extra cycle for LPDDR4 operation. Unit: DRAM clock cycles. Value After Reset: 0xd Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG3_FREQ2

Address: **Operational Base** + offset (0x20000C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x04	t_mr Time from MRW/MRS to valid command LPDDR4: Set this to the larger of tMRR, tMRW, tMRWCKEL and tMRD. LPDDR5: Set this to the larger of tMRR, tMRW, tMRWPD and tMRD. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:8	RW	0x04	rd2mr Time from Read to MRW/MRR command. LPDDR4: RL + BL/2 + RU(tDQSCKmax/tCK) + RD(tRPST) + max(RU(7.5ns/tCK),8nCK) + nRTP - 8 LPDDR5: RL + RU(tWCKDQO(max)/tCK)) + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nRBTP Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

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Bit	Attr	Reset Value	Description
7:0	RW	0x04	wr2mr Time from Write to MRW/MRR command. LPDDR4: WL + 1 + BL/2 + max(RU(7.5ns/tCK),8nCK) + nWR LPDDR5: WL + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nWR Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG4_FREQ2

Address: **Operational Base** + offset (0x200010)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	t_rcd tRCD - tAL: Minimum time from activate to read or write command to same bank. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
23:22	RO	0x0	reserved
21:16	RW	0x04	t_ccd This is the minimum time between two reads or two writes. LPDDR4: tCCD LPDDR5: BL/n Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:14	RO	0x0	reserved
13:8	RW	0x04	t_rrd For LPDDR5(BG mode): Minimum time between activates from bank "a" to bank "b" for same bank group. For LPDDR4/LPDDR5(16B mode): Minimum time between activates from bank "a" to bank "b". LPDDR4: RU(tRRD/tCK) LPDDR5(BG mode): RU(tRRD_L/tCK) LPDDR5(16B mode): RU(tRRD/tCK) Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7	RO	0x0	reserved
6:0	RW	0x05	t_rp tRP: Minimum time from single-bank precharge to activate of same bank. t_rp must be set to RoundUp(tRP/tCK). Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG5_FREQ2

Address: **Operational Base** + offset (0x200014)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:24	RW	0x05	t_cksrx This is the time before Self Refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: LPDDR4: tCKCKEH LPDDR5: tCKCSH Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
23	RO	0x0	reserved
22:16	RW	0x05	t_cksre This is the time after Self Refresh Down Entry/Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE/PDE. Recommended settings: LPDDR4: tCKELCK LPDDR5: tCSLCK Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15	RO	0x0	reserved
14:8	RW	0x04	t_ckesr Minimum CKE low width for Self refresh or Self refresh power down entry to exit timing in memory clock cycles. Recommended settings: LPDDR4: Max(tCKE, tSR) LPDDR5: tSR Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:6	RO	0x0	reserved
5:0	RW	0x03	t_cke Delay time between PDE and PDX. LPDDR4: tCKE LPDDR5: tCSPD Unit: DRAM clock cycles. Value After Reset: 0x3 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG6_FREQ2

Address: **Operational Base** + offset (0x200018)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x05	t_ckcsx This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit. Recommended settings: LPDDR4/5: tXP + 2 This is only present for designs supporting LPDDR devices. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG7_FREQ2

Address: **Operational Base** + offset (0x20001C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	t_csh CS High Pulse width at PDX LPDDR5: tCSH Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG8_FREQ2

Address: **Operational Base** + offset (0x200020)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x44	t_xs_dll_x32 tXSDLL: Exit Self Refresh to commands requiring a locked DLL. Note: Not used for LPDDR4/LPDDR5 SDRAMs.
7	RO	0x0	reserved
6:0	RW	0x05	t_xs_x32 tXS: Exit Self Refresh to commands not requiring a locked DLL. Note: Not used for LPDDR4/5 SDRAMs.

DDRCTL_DRAMSET1TMG9_FREQ2

Address: **Operational Base** + offset (0x200024)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x04	t_ccd_s tCCD_S: This is the minimum time between two reads or two writes for different bank group. For bank switching (from bank "a" to bank "b"), the minimum time is this value + 1. Note: This register field is only applicable for designs supporting LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x04	t_rrd_s tRRD_S: Minimum time between activates from bank "a" to bank "b" for different bank group. Note: This register field is only applicable for designs supporting LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:0	RW	0x0d	wr2rd_s Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Applicable only in designs configured to support LPDDR5 SDRAM memories. LPDDR5 designs: WL + BL/n_min +RU(tWTR_S/tCK) Where: WL = Write Latency BL/n_min = Effective Burst Length tWTR_S = internal write to read command delay for different bank group. Unit: DRAM clock cycles. Value After Reset: 0xd Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG12_FREQ2

Address: **Operational Base** + offset (0x200030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x2	t_cmdcke tCMDCKE: Delay from valid command to PDE LPDDR4: Max(tESCKE, tCMDCKE) LPDDR5: Max(tESPD, tCMDPD) Unit: DRAM clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:0	RO	0x0000	reserved

DDRCTL_DRAMSET1TMG13_FREQ2

Address: **Operational Base** + offset (0x200034)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x1c	odtloff LPDDR4: ODTLoff: This is the latency from CAS-2 command to ODToff reference. Note: This register field is only applicable for designs supporting LPDDR4 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x1c Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
23	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
22:16	RW	0x20	t_ccd_mw This is the minimum time from write or masked write to masked write command for same bank. LPDDR4: tCCDMW LPDDR5(BG mode): 4*BL/n_max LPDDR5(16B mode): 4*BL/n Note: This register field is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x20 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:4	RO	0x000	reserved
3:0	RW	0x4	t_ppd LPDDR4/5: tPPD: This is the minimum time from precharge to precharge command. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG14_FREQ2

Address: **Operational Base** + offset (0x200038)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x008	t_osco tosco: Minimum time from DQS Oscillator stop to Mode register readout. LPDDR4 : max(40ns,8nck) LPDDR5A: tOSCODQI=tOSCODQO=max(40ns,8nck) Unit: DRAM clock cycles. Value After Reset: 0x8 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:12	RO	0x0	reserved
11:0	RW	0x0a0	t_xsr tXSR: Exit Self Refresh to any command. The value 0xfff is illegal for this register field. Unit: DRAM clock cycles. Value After Reset: 0xa0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG23_FREQ2

Address: **Operational Base** + offset (0x20005C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	t_xsr_dsm_x1024 Delay from Deep Sleep Mode Exit to SRX. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	t_pdn Minimum interval between Deep Sleep Mode Entry and Exit. Unit: DRAM clock cycles. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related

DDRCTL_DRAMSET1TMG24_FREQ2

Address: **Operational Base** + offset (0x200060)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RW	0x0	bank_org Select Bank/ Bank group organization: 2'b00: 4 Banks/ 4 Bank groups 2'b01: 8 Banks 2'b10: 16 Banks 2'b11: Reserved Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
23:16	RW	0x0f	rd2wr_s Minimum time from read command to write command for different bank group. Includes time for bus turnaround, recovery times and all per-bank, per-rank and global constraints. LPDDR5(DQ ODT is disabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) - WL LPDDR5(DQ ODT is enabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x0f	max_rd_sync Minimum time from read command to WCK2CK sync OFF. RL + BL/n_max + RU(tRPST/tCK) Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x0f	max_wr_sync Minimum time from write command to WCK2CK sync OFF. WL + BL/n_max Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG25_FREQ2

Address: **Operational Base** + offset (0x200064)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
18:16	RW	0x0	lpddr4_diff_bank_rwa2pre Set the timing constraint between different bank RD/WR/MWR/ACT and PRE in LPDDR4. LPDDR4 JESD209-4A requires 4 cycles LPDDR4 JESD209-4B requires 2 cycles Value of 1, 3, 5, 6, and 7 are illegal. Don't care for LPDDR5. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x00	wra2pre Time between write with AP and precharge to same bank. LPDDR4: WL + BL/2 + nWR + 1 LPDDR5: WL + BL/n_min + nWR + 1 Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x00	rda2pre Time between read with AP and precharge to same bank. LPDDR4: nRTP LPDDR5: BL/n_min + nRBTP Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG30_FREQ2

Address: **Operational Base** + offset (0x200078)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mrr2mrw MRR to MRW delay Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:8	RW	0x00	mrr2wr MRR to WR delay Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:0	RW	0x00	mrr2rd MRR to RD delay Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR0_FREQ2

Address: **Operational Base** + offset (0x200500)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr LPDDR4: Value to write to MR1 register Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:0	RW	0x0510	emr LPDDR4: Value to write to MR2 register Value After Reset: 0x510 Volatile: True Programming Mode: Quasi-dynamic Group 4

DDRCTL_INITMR1_FREQ2

Address: **Operational Base** + offset (0x200504)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	emr2 LPDDR4: Value to write to MR3 register Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4
15:0	RW	0x0000	emr3 LPDDR4: Value to write to MR13 register Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR2_FREQ2

Address: **Operational Base** + offset (0x200508)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr4 LPDDR4: Value to be loaded into SDRAM MR11 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	mr5 LPDDR4: Value to be loaded into SDRAM MR12 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4

DDRCTL_INITMR3_FREQ2

Address: **Operational Base** + offset (0x20050C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr22 LPDDR4 Value to be loaded into SDRAM MR22 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	mr6 LPDDR4 Value to be loaded into SDRAM MR14 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4

DDRCTL_DFITMG0_FREQ2

Address: **Operational Base** + offset (0x200580)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x07	dfi_t_ctrl_delay Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DRAM clock and the memory clock are not phase-aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x7 Volatile: True Programming Mode: Quasi-dynamic Group 4
23	RO	0x0	reserved
22:16	RW	0x02	dfi_t_rddata_en Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:14	RO	0x0	reserved
13:8	RW	0x00	dfi_tphy_wrdata Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. Refer to PHY specification for correct value. Note, max supported value is 8. Unit: DRAM data clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4
7:6	RO	0x0	reserved
5:0	RW	0x02	dfi_tphy_wrlat Write latency Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value. For LPDDR4, dfi_tphy_wrlat>60 is not supported. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

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DDRCTL_DFITMG1_FREQ2

Address: **Operational Base** + offset (0x200584)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	dfi_t_wrdata_delay Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. For LPDDR5, this should be set to "twck_delay + BL/n_max - BL/n_min" instead of twrdata_delay. twck_delay specifies the time from dfi_wck_en deassertion to when WCK transfer completes on the DRAM bus and is defined by the PHY Refer to PHY specification for correct value. When DDRCTL_TMGCFG_FREQ2.frequency_ratio is set to 0(1:2 Mode), divided the value by 2 and round it up to the next integer value. When DDRCTL_TMGCFG_FREQ2.frequency_ratio is set to 1(1:4 Mode), divided the value by 4 and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4
15:13	RO	0x0	reserved
12:8	RW	0x04	dfi_t_dram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 4
7:5	RO	0x0	reserved
4:0	RW	0x04	dfi_t_dram_clk_enable Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 4

DDRCTL_DFITMG2_FREQ2

Address: **Operational Base** + offset (0x200588)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

Bit	Attr	Reset Value	Description
21:16	RW	0x00	dfi_twck_delay Number of DFI PHY clock cycles from dfi_wck_en is de-asserted to when the WCK transfer completes on the DRAM bus. Refer to PHY specification for correct value. Unit: DFI PHY clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15	RO	0x0	reserved
14:8	RW	0x02	dfi_tphy_rdcslat Number of DFI PHY clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:6	RO	0x0	reserved
5:0	RW	0x02	dfi_tphy_wrcslat Number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DFITMG4_FREQ2

Address: **Operational Base** + offset (0x200590)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_en_rd WCK Enable Read Timing. Defines the timing from the CAS-WS_RD command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_en_wr WCK Enable Read Timing. Defines the timing from the CAS-WS_WR command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_en_fs WCK Enable Fast Sync Timing. Defines the timing from the CAS-WS_FS command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset: 0x0 Programming Mode: Quasi-dynamic Group 1, Group 4

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	dfi_twck_dis WCK Off Timing. Defines the timing from the last command opportunity to the deassertion of dfi_wck_en and dfi_wck_toggle_en assuming that no command is being sent. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4

DDRCTL_DFITMG5_FREQ2

Address: **Operational Base** + offset (0x200594)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_fast_toggle Defines the number of clock cycles between the dfi_wck_signal being driven to TOGGLE to when the dfi_wck_signal is driven to FAST_TOGGLE. This timing is only applicable when the WCK transitions from the slow to fast toggle. Otherwise, this timing parameter must be set to 0x0. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_toggle WCK Toggle Enable Timing. Defines the timing from dfi_wck_en assertion to dfi_wck_toggle_en assertion. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_toggle_cs Defines the number of clock cycles between a read or write command to when the dfi_wck_cs signal must be stable. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
7:0	RW	0x00	dfi_twck_toggle_post Defines the number of clock cycles after a read or write command data burst completion during which the WCK must remain in the current toggle state. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4

DDRCTL_DFIUPDTMG1_FREQ2

Address: **Operational Base** + offset (0x2005AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x01	dfi_t_ctrlupd_interval_min_x1024 This is the minimum amount of time between DDRCTL initiated DFI update requests (which is executed whenever the DDRCTL is idle). Set this number higher to reduce the frequency of update requests, which can have a small impact on the latency of the first read request when the DDRCTL is idle. Minimum allowed value for this field is 1. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x01 Programming Mode: Static
15:8	RO	0x00	reserved
7:0	RW	0x01	dfi_t_ctrlupd_interval_max_x1024 This is the maximum amount of time between DDRCTL initiated DFI update requests. This timer resets with each update request; when the timer expires dfi_ctrlupd_req is sent and traffic is blocked until the dfi_ctrlupd_ackx is received. PHY can use this idle time to recalibrate the delay lines to the DLLs. The DFI controller update is also used to reset PHY FIFO pointers in case of data capture errors. Updates are required to maintain calibration over PVT, but frequent updates may impact performance. Minimum allowed value for this field is 1. Note: Value programmed for dfi_t_ctrlupd_interval_max_x1024 must be greater than dfi_t_ctrlupd_interval_min_x1024. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x01 Programming Mode: Static

DDRCTL_RFSHSET1TMG0_FREQ2

Address: **Operational Base** + offset (0x200600)

Bit	Attr	Reset Value	Description
31	RW	0x0	t_refi_x1_sel Specifies whether DDRCTL_RFSHSET1TMG0_FREQ2.t_refi_x1_x32 and DDRCTL_RFSHSET1TMG0_FREQ2.refresh_to_x1_x32 register values are x1 or x32. 1'b0: x32 register values are used. 1'b1: Register values are used. This applies only when per-bank refresh is enabled (DDRCTL_RFSHMOD0.per_bank_refresh=1). If per-bank refresh is not enabled, the x32 register values are used and this register field is ignored. This register field does not exist for configurations which do not support LPDDR4/5. For such configurations, the value of this register field can be assumed to be 0, so that DDRCTL_RFSHSET1TMG0_FREQ2.t_refi_x1_x32 and DDRCTL_RFSHSET1TMG0_FREQ2.refresh_to_x1_x32 are interpreted as x32 register fields Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related
30:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:24	RW	0x2	refresh_margin Threshold value in number of DRAM clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_refi/32. Note that internally used t_refi is equal to DDRCTL_RFSHSET1TMG0_FREQ2.t_refi_x1_x32 * 32 if DDRCTL_RFSHSET1TMG0_FREQ2.t_refi_x1_sel = 0. If DDRCTL_RFSHSET1TMG0_FREQ2.t_refi_x1_sel = 1, internally used t_refi is equal to DDRCTL_RFSHSET1TMG0_FREQ2.t_refi_x1_x32. Note that, internally used t_refi may be divided by four if derating or TCR is enabled. Unit: Multiples of 32 DRAM clock cycles. Value After Reset: 0x2 Programming Mode: Dynamic - Refresh Related
23:22	RO	0x0	reserved
21:16	RW	0x10	refresh_to_x1_x32 If the refresh timer has expired at least once (i.e. >tREFI period elapses, and there are postponed refreshes), then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful. When there are no transactions pending in the CAM for a period of time determined by this DDRCTL_RFSHSET1TMG0_FREQ2.refresh_to_x1_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the DDRCTL. This is also used for non speculative refresh when LPDDR per-bank refresh (REFpb) is enabled. The controller observes the period of time determined by this for each bank, and a priority of bank address is determined. This should be programmed to tREFI based value in controller's current refresh mode. The controller calculates this according to current refresh mode. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on DDRCTL_RFSHSET1TMG0_FREQ2.t_refi_x1_sel. Value After Reset: 0x10 Programming Mode: Dynamic - Refresh Related
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x062	t_refi_x1_x32 Average time interval between refreshes per rank (See JEDEC specification for LPDDR4). Set this register to RoundDown(tREFI/tCK). If DDRCTL_RFSHSET1TMG0_FREQ2.t_refi_x1_sel = 0, divide the above result by 32 and round down. For LPDDR controller: If using all-bank refreshes (DDRCTL_RFSHMOD0.per_bank_refresh = 0), use tREFIab in the above calculations. If using per-bank refreshes (DDRCTL_RFSHMOD0.per_bank_refresh = 1), use tREFIpb in the above calculations. Note that: DDRCTL_RFSHSET1TMG0_FREQ2.t_refi_x1_x32 must be greater than 0x1. If DDRCTL_RFSHSET1TMG0_FREQ2.t_refi_x1_sel == 1, DDRCTL_RFSHSET1TMG0_FREQ2.t_refi_x1_x32 must be greater than DDRCTL_RFSHSET1TMG1_FREQ2.t_rfc_min If DDRCTL_RFSHSET1TMG0_FREQ2.t_refi_x1_sel == 0, DDRCTL_RFSHSET1TMG0_FREQ2.t_refi_x1_x32 * 32 must be greater than DDRCTL_RFSHSET1TMG1_FREQ2.t_rfc_min DDRCTL_RFSHSET1TMG0_FREQ2.t_refi_x1_x32 must be less than or equal to 0xFFE. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on DDRCTL_RFSHSET1TMG0_FREQ2.t_refi_x1_sel. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x62 Programming Mode: Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG1_FREQ2

Address: **Operational Base** + offset (0x200604)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x08c	t_rfc_min tRFC (min): Minimum time from refresh to refresh or activate. t_rfc_min must be set to RoundUp(tRFCmin/tCK). In LPDDR controller, if using all-bank refreshes, the tRFCmin value in the above equations is equal to tRFCab. If using per-bank refreshes, the tRFCmin value in the above equations is equal to tRFCpb. Unit: DRAM clock cycles. Value After Reset: 0x8c Programming Mode: Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG2_FREQ2

Address: **Operational Base** + offset (0x200608)

Bit	Attr	Reset Value	Description
31:24	RW	0x8c	t_pbr2act Time from REFpb to activate command to different bank than REFpb. LPDDR5: tpbr2act Value After Reset: 0x8c Programming Mode: Dynamic - Refresh Related

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Bit	Attr	Reset Value	Description
23:16	RW	0x8c	t_pbr2pbr LPDDR4: tpbR2pbR Per-bank Refresh to Per-bank refresh different bank Time. Program this to RoundUp(tpbR2pbR/tCK). The tpbR2pbR value in the above equations is different depending on the device density. The user must program the appropriate value from the spec. Register is valid only in LPDDR4 per-bank refresh mode (DDRCTL_RFSHMOD0.per_bank_refresh == 1). Value After Reset: 0x8c Programming Mode: Dynamic - Refresh Related
15:0	RO	0x0000	reserved

DDRCTL_RFSHSET1TMG4_FREQ2

Address: **Operational Base** + offset (0x200610)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	refresh_timer1_start_value_x32 Refresh timer start for rank 1 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related
15:12	RO	0x0	reserved
11:0	RW	0x000	refresh_timer0_start_value_x32 Refresh timer start for rank 0 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related

DDRCTL_ZQSET1TMG0_FREQ2

Address: **Operational Base** + offset (0x200800)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x040	t_zq_short_nop tZQLAT for LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset: 0x40 Programming Mode: Static
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0200	t_zq_long_nop tZQCAL for LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM. If using LPDDR5, this register needs to be programmed to tZQCAL + 10 cycles. Unit: DRAM clock cycles. Value After Reset: 0x200 Programming Mode: Static

DDRCTL_ZQSET1TMG1_FREQ2

Address: **Operational Base** + offset (0x200804)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x020	t_zq_reset_nop tZQReset: Number of DRAM clock cycles of NOP required after a ZQReset (ZQ calibration Reset) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset: 0x20 Programming Mode: Static
19:0	RW	0x00100	t_zq_short_interval_x1024 Average interval to wait between automatically issuing ZQCS (ZQ calibration short)/MPC(ZQ calibration) commands to LPDDR4 devices. Meaningless, if DDRCTL_ZQCTL0.dis_auto_zq=1. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x100 Programming Mode: Static

DDRCTL_DQSOSCCTL0_FREQ2

Address: **Operational Base** + offset (0x200A80)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RW	0x007	dqsosc_interval DQS Oscillator interval, specifies the time between two DQS oscillator sequences. Minimum programmable value is 1. The value can be changed while DQSOSCCTL0.dqsosc_enable=0 Unit: DFI clock cycles Value After Reset: 0x7 Programming Mode: Dynamic
3	RO	0x0	reserved
2	RW	0x0	dqsosc_interval_unit DQS/WCK Oscillator Interval unit. Specifies the unit for counting DQS oscillator interval. The value can be changed while DQSOSCCTL0.dqsosc_enable=0 1'b1: x2K DFI clock cycles 1'b0: x32K DFI clock cycles Value After Reset: 0x0 Programming Mode: Dynamic
1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	dqsosc_enable DQS/WCK Oscillator Enable 1'b1: Enable DQS Oscillator 1'b0: Disable DQS Oscillator Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_DERATEINT_FREQ2

Address: **Operational Base** + offset (0x200B00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00800000	mr4_read_interval Interval between two MR4 reads, used to derate the timing parameters. This register must not be set to zero. Unit: DRAM clock cycles. Value After Reset: 0x800000 Volatile: True Programming Mode: Static

DDRCTL_DERATEVAL0_FREQ2

Address: **Operational Base** + offset (0x200B04)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	derated_t_rcd Derated value for tRCD. For LPDDR4, the required period with derating is tRCD + 1.875ns For LPDDR5, the required period with derating is tRCD + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
23:16	RW	0x0f	derated_t_ras_min Derated value for tRAS. For LPDDR4, the required period with derating is tRAS + 1.875ns For LPDDR5, the required period with derating is tRAS + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15	RO	0x0	reserved
14:8	RW	0x05	derated_t_rp Derated value for tRP. For LPDDR4, the required period with derating is tRP + 1.875ns For LPDDR5, the required period with derating is tRP + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x04	derated_t_rrd Derated value for tRRD. For LPDDR4, the required period with derating is tRRD + 1.875ns For LPDDR5, the required period with derating is tRRD + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DERATEVAL1_FREQ2

Address: **Operational Base** + offset (0x200B08)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x14	derated_t_rc Derated value for tRC. For LPDDR4, the required period with derating is tRC + 3.75ns For LPDDR5, the required period with derating is tRC + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x14 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_HWLPTMG0_FREQ2

Address: **Operational Base** + offset (0x200B80)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_lp_idle_x32 Hardware idle period. The cactive_ddrc output is driven low if the DDRC command channel is idle for hw_lp_idle * 32 cycles if not in INIT or DPD/MPSM operating_mode. The DDRC command channel is considered idle when there are no HIF commands outstanding. The hardware idle function is disabled when hw_lp_idle_x32=0. hw_lp_idle_x32=1 is an illegal value when the controller is in 1:2 mode. hw_lp_idle_x32=1/2/3 are illegal values when the controller is in 1:4 mode. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Volatile: True Programming Mode: Static
15:0	RO	0x0000	reserved

DDRCTL_SCHEDTMG0_FREQ2

Address: **Operational Base** + offset (0x200C00)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
14:8	RW	0x00	rdwr_idle_gap When the preferred transaction store is empty for these many clock cycles, switch to the alternate transaction store if it is non-empty. The read transaction store (both high and low priority) is the default preferred transaction store and the write transaction store is the alternative store. When prefer write over read is set this is reversed. 0x0 is a legal value for this register. When set to 0x0, the transaction store switching will happen immediately when the switching conditions become true. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x0 Programming Mode: Static
7:0	RW	0x00	pageclose_timer This field works in conjunction with DDRCTL_SCHED0.pageclose. It only has meaning if DDRCTL_SCHED0.pageclose==1. If DDRCTL_SCHED0.pageclose==1 and pageclose_timer==0, then an auto-precharge may be scheduled for last read or write command in the CAM with a bank and page hit. Note, sometimes an explicit precharge is scheduled instead of the auto-precharge. See DDRCTL_SCHED0.pageclose for details of when this may happen. If DDRCTL_SCHED0.pageclose==1 and pageclose_timer>0, then an auto-precharge is not scheduled for last read or write command in the CAM with a bank and page hit. Instead, a timer is started, with pageclose_timer as the initial value. There is a timer on a per bank basis. The timer decrements unless the next read or write in the CAM to a bank is a page hit. It gets reset to pageclose_timer value if the next read or write in the CAM to a bank is a page hit. Once the timer has reached zero, an explcit precharge will be attempted to be scheduled. Unit: DRAM clock cycles. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_PERFHPR1_FREQ2

Address: **Operational Base** + offset (0x200C80)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	hpr_xact_run_length Number of transactions that are serviced once the HPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available Unit: Transaction FOR PERFORMANCE ONLY. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0001	hpr_max_starve Number of DRAM clocks that the HPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x1 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PERFLPR1_FREQ2

Address: **Operational Base** + offset (0x200C84)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	lpr_xact_run_length Number of transactions that are serviced once the LPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available Unit: Transaction FOR PERFORMANCE ONLY. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x00	reserved
15:0	RW	0x007f	lpr_max_starve Number of DRAM clocks that the LPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x7f Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PERFWR1_FREQ2

Address: **Operational Base** + offset (0x200C88)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	w_xact_run_length Number of transactions that are serviced once the WR queue goes critical is the smaller of: (a) This number (b) Number of transactions available Unit: Transaction FOR PERFORMANCE ONLY. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x007f	w_max_starve Number of DRAM clocks that the WR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x7f Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_TMGCFG_FREQ2

Address: **Operational Base** + offset (0x200D00)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	dfi_freq_fsp This register value propergates to dfi_freq_fsp pin directly. Value After Reset: 0x0 Programming Mode: Dynamic
7:1	RO	0x00	reserved
0	RW	0x0	frequency_ratio Selects the Frequency Ratio For LPDDR4: 1'b0: 1:2 Mode 1'b1: 1:4 Mode For LPDDR5: 1'b0: 1:1:2 Mode 1'b1: 1:1:4 Mode Value After Reset: 0x0 Programming Mode: Quasi-dynamic Group 2

DDRCTL_RANKTMG0_FREQ2

Address: **Operational Base** + offset (0x200D04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x06	diff_rank_wr_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_wrcsgap (see PHY databook for value of tphy_wrcsgap) If CRC feature is enabled, must be increased by 1. Write preamble is always set to 2tCK for LPDDR4, refer to PHY databook to see if this is already factored into tphy_wrcsgap value or if it needs to be increased by 1. If write postamble is set to 1.5tCK(LPDDR4 only), must be increased by 1. ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, with DQ ODT enabled, diff_rank_wr_gap must be a

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Bit	Attr	Reset Value	Description
			minimum of ODTLoff - ODTLon - BL/2 + 1 For other cases, diff_rank_wr_gap must be a minimum of ODTCFG.wr_odt_hold - BL/2. Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay". Please see PHY databook for the value of tphy_wckcsgap. Unit: DRAM clock cycles. Value After Reset: 0x6 Volatile: True Programming Mode: Quasi-dynamic Group 2
7:0	RW	0x06	diff_rank_rd_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_rdcsgap (see PHY databook for value of tphy_rdcsgap) ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads: Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay". Please see PHY databook for the value of tphy_wckcsgap. Unit: DRAM clock cycles. Value After Reset: 0x6 Volatile: True Programming Mode: Quasi-dynamic Group 2

DDRCTL_RANKTMG1_FREQ2

Address: **Operational Base** + offset (0x200D08)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x0f	rd2wr_dr Minimum time from read command to write command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. The value must be larger than or equal to the value of DRAMSET1TMG2.rd2wr. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

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Bit	Attr	Reset Value	Description
7:0	RW	0x0f	wr2rd_dr Minimum time from write command to read command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_PWRTMG_FREQ2

Address: **Operational Base** + offset (0x200D0C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x040	selfref_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into Self Refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x40 Volatile: True Programming Mode: Quasi-dynamic Group 4
15:7	RO	0x000	reserved
6:0	RW	0x10	powerdown_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into power-down. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x10 Volatile: True Programming Mode: Quasi-dynamic Group 4

DDRCTL_DRAMSET1TMG0_FREQ3

Address: **Operational Base** + offset (0x300000)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	wr2pre Minimum time between write and precharge to same bank. Specifications: WL + BL/2 + tWR where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate)

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Bit	Attr	Reset Value	Description
			is not supported at present. tWR = Write recovery time. This comes directly from the SDRAM specification. Add one extra cycle for LPDDR4/5 for this parameter. Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
23:16	RW	0x10	t_faw tFAW: At most 4 banks must be activated in a rolling window of tFAW cycles. Unit: DRAM clock cycles. Value After Reset: 0x10 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:8	RW	0x1b	t_ras_max tRAS(max): Maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open t_ras_max must be set to RoundDown(tRAS(max)/tCK/1024). Unit: 1024 DRAM clock cycles. Value After Reset: 0x1b Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:0	RW	0x0f	t_ras_min tRAS(min): Minimum time between activate and precharge to the same bank. Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG1_FREQ3

Address: **Operational Base** + offset (0x300004)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x08	t_xp tXP: Minimum time after power-down exit to any operation. LPDDR4 (tCKELPD is defined in spec): larger of tXP and tCKELPD instead. LPDDR4 (tCKELPD is not defined in spec): tXP. LPDDR5: tXP + tCSH Unit: DRAM clock cycles. Value After Reset: 0x8 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:8	RW	0x04	rd2pre tRTP: Minimum time from read to precharge of same bank. LPDDR4 - BL/2 + max(RoundUp(tRTP/tCK),8) - 8 LPDDR5(BG mode): BL/n_min + RU(tRBTP/tCK) LPDDR5(16B mode): BL/n + RU(tRBTP/tCK) Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

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Bit	Attr	Reset Value	Description
7:0	RW	0x14	t_rc tRC: Minimum time between activates to same bank. Unit: DRAM clock cycles. Value After Reset: 0x14 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG2_FREQ3

Address: **Operational Base** + offset (0x300008)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x03	write_latency Set to WL Time from write command to write data on SDRAM interface. This must be set to WL. For all protocols, in addition to programming this register field, it is necessary to program DDRCTL_DFITMG0_FREQ3 and DDRCTL_DFITMG1_FREQ3 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset: 0x3 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
23	RO	0x0	reserved
22:16	RW	0x05	read_latency Set to RL Time from read command to read data on SDRAM interface. This must be set to RL. In addition to programming this register field, it is necessary to program DDRCTL_DFITMG0_FREQ3 and DDRCTL_DFITMG1_FREQ3 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x06	rd2wr LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled) : RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (BG mode && DQ ODT is Disabled): RL + BL/n_max + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (BG mode && DQ ODT is Enabled) : RL + BL/n_max + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (16B mode && DQ ODT is Disabled): RL + BL/n + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (16B mode && DQ ODT is Enabled) : RL + BL/n + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 Minimum time from read command to write command. Include time for bus turnaround and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: WL = write latency

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Bit	Attr	Reset Value	Description
			BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM RL = read latency = CAS latency WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). RD_POSTAMBLE = 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR4, if derating is enabled (DDRCTL_DERATECTL0_FREQ3.derate_enable=1), derated tDQSCKmax must be used. Unit: DRAM clock cycles. Value After Reset: 0x6 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x0d	wr2rd LPDDR4: WL + BL/2 + tWTR + 1 LPDDR5(BG mode): WL + BL/n_max + RU(tWTR_L/tCK) LPDDR5(16B mode): WL + BL/n + RU(tWTR/tCK) Minimum time from write command to read command. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: CWL = CAS write latency WL = Write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_L = internal write to read command delay for same bank group. This comes directly from the SDRAM specification. tWTR = internal write to read command delay. This comes directly from the SDRAM specification. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Add one extra cycle for LPDDR4 operation. Unit: DRAM clock cycles. Value After Reset: 0xd Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG3_FREQ3

Address: **Operational Base** + offset (0x30000C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x04	t_mr Time from MRW/MRS to valid command LPDDR4: Set this to the larger of tMRR, tMRW, tMRWCKEL and tMRD. LPDDR5: Set this to the larger of tMRR, tMRW, tMRWPD and tMRD. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True

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Bit	Attr	Reset Value	Description
			Programming Mode: Quasi-dynamic Group 2, Group 4
15:8	RW	0x04	rd2mr Time from Read to MRW/MRR command. LPDDR4: RL + BL/2 + RU(tDQSCKmax/tCK) + RD(tRPST) + max(RU(7.5ns/tCK),8nCK) + nRTP - 8 LPDDR5: RL + RU(tWCKDQO(max)/tCK)) + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nRBTP Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:0	RW	0x04	wr2mr Time from Write to MRW/MRR command. LPDDR4: WL + 1 + BL/2 + max(RU(7.5ns/tCK),8nCK) + nWR LPDDR5: WL + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nWR Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG4_FREQ3

Address: **Operational Base** + offset (0x300010)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	t_rcd tRCD - tAL: Minimum time from activate to read or write command to same bank. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
23:22	RO	0x0	reserved
21:16	RW	0x04	t_ccd This is the minimum time between two reads or two writes. LPDDR4: tCCD LPDDR5: BL/n Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:14	RO	0x0	reserved
13:8	RW	0x04	t_rrd For LPDDR5(BG mode): Minimum time between activates from bank "a" to bank "b" for same bank group. For LPDDR4/LPDDR5(16B mode): Minimum time between activates from bank "a" to bank "b". LPDDR4: RU(tRRD/tCK) LPDDR5(BG mode): RU(tRRD_L/tCK) LPDDR5(16B mode): RU(tRRD/tCK) Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:0	RW	0x05	t_rp tRP: Minimum time from single-bank precharge to activate of same bank. t_rp must be set to RoundUp(tRP/tCK). Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG5_FREQ3

Address: **Operational Base** + offset (0x300014)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x05	t_cksrx This is the time before Self Refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: LPDDR4: tCKCKEH LPDDR5: tCKCSH Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
23	RO	0x0	reserved
22:16	RW	0x05	t_cksre This is the time after Self Refresh Down Entry/Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE/PDE. Recommended settings: LPDDR4: tCKELCK LPDDR5: tCSLCK Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15	RO	0x0	reserved
14:8	RW	0x04	t_ckesr Minimum CKE low width for Self refresh or Self refresh power down entry to exit timing in memory clock cycles. Recommended settings: LPDDR4: Max(tCKE, tSR) LPDDR5: tSR Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:6	RO	0x0	reserved
5:0	RW	0x03	t_cke Delay time between PDE and PDX. LPDDR4: tCKE LPDDR5: tCSPD Unit: DRAM clock cycles. Value After Reset: 0x3 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

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DDRCTL_DRAMSET1TMG6_FREQ3

Address: **Operational Base** + offset (0x300018)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x05	t_ckcsx This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit. Recommended settings: LPDDR4/5: tXP + 2 This is only present for designs supporting LPDDR devices. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG7_FREQ3

Address: **Operational Base** + offset (0x30001C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	t_csh CS High Pulse width at PDX LPDDR5: tCSH Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG8_FREQ3

Address: **Operational Base** + offset (0x300020)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x44	t_xs_dll_x32 tXSDLL: Exit Self Refresh to commands requiring a locked DLL. Note: Not used for LPDDR4/LPDDR5 SDRAMs.
7	RO	0x0	reserved
6:0	RW	0x05	t_xs_x32 tXS: Exit Self Refresh to commands not requiring a locked DLL. Note: Not used for LPDDR4/5 SDRAMs.

DDRCTL_DRAMSET1TMG9_FREQ3

Address: **Operational Base** + offset (0x300024)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x04	t_ccd_s tCCD_S: This is the minimum time between two reads or two writes for different bank group. For bank switching (from bank "a" to bank "b"), the minimum time is this value + 1. Note: This register field is only applicable for designs supporting LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x04	t_rrd_s tRRD_S: Minimum time between activates from bank "a" to bank "b" for different bank group. Note: This register field is only applicable for designs supporting LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:0	RW	0x0d	wr2rd_s Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Applicable only in designs configured to support LPDDR5 SDRAM memories. LPDDR5 designs: WL + BL/n_min +RU(tWTR_S/tCK) Where: WL = Write Latency BL/n_min = Effective Burst Length tWTR_S = internal write to read command delay for different bank group. Unit: DRAM clock cycles. Value After Reset: 0xd Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG12_FREQ3

Address: **Operational Base** + offset (0x300030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x2	t_cmdcke tCMDCKE: Delay from valid command to PDE LPDDR4: Max(tESCKE, tCMDCKE) LPDDR5: Max(tESPD, tCMDPD) Unit: DRAM clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:0	RO	0x0000	reserved

DDRCTL_DRAMSET1TMG13_FREQ3

Address: **Operational Base** + offset (0x300034)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x1c	odtloff LPDDR4: ODTLoff: This is the latency from CAS-2 command to ODToff reference. Note: This register field is only applicable for designs supporting LPDDR4 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x1c Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
23	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
22:16	RW	0x20	t_ccd_mw This is the minimum time from write or masked write to masked write command for same bank. LPDDR4: tCCDMW LPDDR5(BG mode): 4*BL/n_max LPDDR5(16B mode): 4*BL/n Note: This register field is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset: 0x20 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:4	RO	0x000	reserved
3:0	RW	0x4	t_ppd LPDDR4/5: tPPD: This is the minimum time from precharge to precharge command. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG14_FREQ3

Address: **Operational Base** + offset (0x300038)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x008	t_osco tosco: Minimum time from DQS Oscillator stop to Mode register readout. LPDDR4 : max(40ns,8nck) LPDDR5A: tOSCODQI=tOSCODQO=max(40ns,8nck) Unit: DRAM clock cycles. Value After Reset: 0x8 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:12	RO	0x0	reserved
11:0	RW	0x0a0	t_xsr tXSR: Exit Self Refresh to any command. The value 0xfff is illegal for this register field. Unit: DRAM clock cycles. Value After Reset: 0xa0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG23_FREQ3

Address: **Operational Base** + offset (0x30005C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	t_xsr_dsm_x1024 Delay from Deep Sleep Mode Exit to SRX. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	t_pdn Minimum interval between Deep Sleep Mode Entry and Exit. Unit: DRAM clock cycles. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related

DDRCTL_DRAMSET1TMG24_FREQ3

Address: **Operational Base** + offset (0x300060)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RW	0x0	bank_org Select Bank/ Bank group organization: 2'b00: 4 Banks/ 4 Bank groups 2'b01: 8 Banks 2'b10: 16 Banks 2'b11: Reserved Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
23:16	RW	0x0f	rd2wr_s Minimum time from read command to write command for different bank group. Includes time for bus turnaround, recovery times and all per-bank, per-rank and global constraints. LPDDR5(DQ ODT is disabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) - WL LPDDR5(DQ ODT is enabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x0f	max_rd_sync Minimum time from read command to WCK2CK sync OFF. RL + BL/n_max + RU(tRPST/tCK) Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x0f	max_wr_sync Minimum time from write command to WCK2CK sync OFF. WL + BL/n_max Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG25_FREQ3

Address: **Operational Base** + offset (0x300064)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
18:16	RW	0x0	lpddr4_diff_bank_rwa2pre Set the timing constraint between different bank RD/WR/MWR/ACT and PRE in LPDDR4. LPDDR4 JESD209-4A requires 4 cycles LPDDR4 JESD209-4B requires 2 cycles Value of 1, 3, 5, 6, and 7 are illegal. Don't care for LPDDR5. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x00	wra2pre Time between write with AP and precharge to same bank. LPDDR4: WL + BL/2 + nWR + 1 LPDDR5: WL + BL/n_min + nWR + 1 Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x00	rda2pre Time between read with AP and precharge to same bank. LPDDR4: nRTP LPDDR5: BL/n_min + nRBTP Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG30_FREQ3

Address: **Operational Base** + offset (0x300078)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mrr2mrw MRR to MRW delay Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:8	RW	0x00	mrr2wr MRR to WR delay Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:0	RW	0x00	mrr2rd MRR to RD delay Unit: DRAM clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR0_FREQ3

Address: **Operational Base** + offset (0x300500)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr LPDDR4: Value to write to MR1 register Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:0	RW	0x0510	emr LPDDR4: Value to write to MR2 register Value After Reset: 0x510 Volatile: True Programming Mode: Quasi-dynamic Group 4

DDRCTL_INITMR1_FREQ3

Address: **Operational Base** + offset (0x300504)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	emr2 LPDDR4: Value to write to MR3 register Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4
15:0	RW	0x0000	emr3 LPDDR4: Value to write to MR13 register Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR2_FREQ3

Address: **Operational Base** + offset (0x300508)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr4 LPDDR4: Value to be loaded into SDRAM MR11 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	mr5 LPDDR4: Value to be loaded into SDRAM MR12 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4

DDRCTL_INITMR3_FREQ3

Address: **Operational Base** + offset (0x30050C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr22 LPDDR4 Value to be loaded into SDRAM MR22 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	mr6 LPDDR4 Value to be loaded into SDRAM MR14 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4

DDRCTL_DFITMG0_FREQ3

Address: **Operational Base** + offset (0x300580)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x07	dfi_t_ctrl_delay Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DRAM clock and the memory clock are not phase-aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x7 Volatile: True Programming Mode: Quasi-dynamic Group 4
23	RO	0x0	reserved
22:16	RW	0x02	dfi_t_rddata_en Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:14	RO	0x0	reserved
13:8	RW	0x00	dfi_tphy_wrdata Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. Refer to PHY specification for correct value. Note, max supported value is 8. Unit: DRAM data clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4
7:6	RO	0x0	reserved
5:0	RW	0x02	dfi_tphy_wrlat Write latency Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value. For LPDDR4, dfi_tphy_wrlat>60 is not supported. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

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DDRCTL_DFITMG1_FREQ3

Address: **Operational Base** + offset (0x300584)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	dfi_t_wrdata_delay Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. For LPDDR5, this should be set to "twck_delay + BL/n_max - BL/n_min" instead of twrdata_delay. twck_delay specifies the time from dfi_wck_en deassertion to when WCK transfer completes on the DRAM bus and is defined by the PHY Refer to PHY specification for correct value. When DDRCTL_TMGCFG_FREQ3.frequency_ratio is set to 0(1:2 Mode), divided the value by 2 and round it up to the next integer value. When DDRCTL_TMGCFG_FREQ3.frequency_ratio is set to 1(1:4 Mode), divided the value by 4 and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 4
15:13	RO	0x0	reserved
12:8	RW	0x04	dfi_t_dram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 4
7:5	RO	0x0	reserved
4:0	RW	0x04	dfi_t_dram_clk_enable Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 4

DDRCTL_DFITMG2_FREQ3

Address: **Operational Base** + offset (0x300588)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

Bit	Attr	Reset Value	Description
21:16	RW	0x00	dfi_twck_delay Number of DFI PHY clock cycles from dfi_wck_en is de-asserted to when the WCK transfer completes on the DRAM bus. Refer to PHY specification for correct value. Unit: DFI PHY clock cycles. Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15	RO	0x0	reserved
14:8	RW	0x02	dfi_tphy_rdcslat Number of DFI PHY clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:6	RO	0x0	reserved
5:0	RW	0x02	dfi_tphy_wrcslat Number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset: 0x2 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DFITMG4_FREQ3

Address: **Operational Base** + offset (0x300590)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_en_rd WCK Enable Read Timing. Defines the timing from the CAS-WS_RD command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_en_wr WCK Enable Read Timing. Defines the timing from the CAS-WS_WR command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_en_fs WCK Enable Fast Sync Timing. Defines the timing from the CAS-WS_FS command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset: 0x0 Programming Mode: Quasi-dynamic Group 1, Group 4

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	dfi_twck_dis WCK Off Timing. Defines the timing from the last command opportunity to the deassertion of dfi_wck_en and dfi_wck_toggle_en assuming that no command is being sent. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4

DDRCTL_DFITMG5_FREQ3

Address: **Operational Base** + offset (0x300594)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_fast_toggle Defines the number of clock cycles between the dfi_wck_signal being driven to TOGGLE to when the dfi_wck_signal is driven to FAST_TOGGLE. This timing is only applicable when the WCK transitions from the slow to fast toggle. Otherwise, this timing parameter must be set to 0x0. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_toggle WCK Toggle Enable Timing. Defines the timing from dfi_wck_en assertion to dfi_wck_toggle_en assertion. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_toggle_cs Defines the number of clock cycles between a read or write command to when the dfi_wck_cs signal must be stable. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4
7:0	RW	0x00	dfi_twck_toggle_post Defines the number of clock cycles after a read or write command data burst completion during which the WCK must remain in the current toggle state. Unit: WCK cycles Value After Reset: 0x0 Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 4

DDRCTL_DFIUPDTMG1_FREQ3

Address: **Operational Base** + offset (0x3005AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x01	dfi_t_ctrlupd_interval_min_x1024 This is the minimum amount of time between DDRCTL initiated DFI update requests (which is executed whenever the DDRCTL is idle). Set this number higher to reduce the frequency of update requests, which can have a small impact on the latency of the first read request when the DDRCTL is idle. Minimum allowed value for this field is 1. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x01 Programming Mode: Static
15:8	RO	0x00	reserved
7:0	RW	0x01	dfi_t_ctrlupd_interval_max_x1024 This is the maximum amount of time between DDRCTL initiated DFI update requests. This timer resets with each update request; when the timer expires dfi_ctrlupd_req is sent and traffic is blocked until the dfi_ctrlupd_ackx is received. PHY can use this idle time to recalibrate the delay lines to the DLLs. The DFI controller update is also used to reset PHY FIFO pointers in case of data capture errors. Updates are required to maintain calibration over PVT, but frequent updates may impact performance. Minimum allowed value for this field is 1. Note: Value programmed for dfi_t_ctrlupd_interval_max_x1024 must be greater than dfi_t_ctrlupd_interval_min_x1024. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x01 Programming Mode: Static

DDRCTL_RFSHSET1TMG0_FREQ3

Address: **Operational Base** + offset (0x300600)

Bit	Attr	Reset Value	Description
31	RW	0x0	t_refi_x1_sel Specifies whether DDRCTL_RFSHSET1TMG0_FREQ3.t_refi_x1_x32 and DDRCTL_RFSHSET1TMG0_FREQ3.refresh_to_x1_x32 register values are x1 or x32. 1'b0: x32 register values are used. 1'b1: Register values are used. This applies only when per-bank refresh is enabled (DDRCTL_RFSHMOD0.per_bank_refresh=1). If per-bank refresh is not enabled, the x32 register values are used and this register field is ignored. This register field does not exist for configurations which do not support LPDDR4/5. For such configurations, the value of this register field can be assumed to be 0, so that DDRCTL_RFSHSET1TMG0_FREQ3.t_refi_x1_x32 and DDRCTL_RFSHSET1TMG0_FREQ3.refresh_to_x1_x32 are interpreted as x32 register fields Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related
30:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:24	RW	0x2	refresh_margin Threshold value in number of DRAM clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_refi/32. Note that internally used t_refi is equal to DDRCTL_RFSHSET1TMG0_FREQ3.t_refi_x1_x32 * 32 if DDRCTL_RFSHSET1TMG0_FREQ3.t_refi_x1_sel = 0. If DDRCTL_RFSHSET1TMG0_FREQ3.t_refi_x1_sel = 1, internally used t_refi is equal to DDRCTL_RFSHSET1TMG0_FREQ3.t_refi_x1_x32. Note that, internally used t_refi may be divided by four if derating or TCR is enabled. Unit: Multiples of 32 DRAM clock cycles. Value After Reset: 0x2 Programming Mode: Dynamic - Refresh Related
23:22	RO	0x0	reserved
21:16	RW	0x10	refresh_to_x1_x32 If the refresh timer has expired at least once (i.e. >tREFI period elapses, and there are postponed refreshes), then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful. When there are no transactions pending in the CAM for a period of time determined by this DDRCTL_RFSHSET1TMG0_FREQ3.refresh_to_x1_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the DDRCTL. This is also used for non speculative refresh when LPDDR per-bank refresh (REFpb) is enabled. The controller observes the period of time determined by this for each bank, and a priority of bank address is determined. This should be programmed to tREFI based value in controller's current refresh mode. The controller calculates this according to current refresh mode. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on DDRCTL_RFSHSET1TMG0_FREQ3.t_refi_x1_sel. Value After Reset: 0x10 Programming Mode: Dynamic - Refresh Related
15:12	RO	0x0	reserved
11:0	RW	0x062	t_refi_x1_x32 Average time interval between refreshes per rank (See JEDEC specification for LPDDR4). Set this register to RoundDown(tREFI/tCK). If DDRCTL_RFSHSET1TMG0_FREQ3.t_refi_x1_sel = 0, divide the above result by 32 and round down. For LPDDR controller: If using all-bank refreshes (DDRCTL_RFSHMOD0.per_bank_refresh = 0), use tREFIab in the above calculations.

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Bit	Attr	Reset Value	Description
			If using per-bank refreshes (DDRCTL_RFSHMOD0.per_bank_refresh = 1), use tREFIpb in the above calculations. Note that: DDRCTL_RFSHSET1TMG0_FREQ3.t_refi_x1_x32 must be greater than 0x1. If DDRCTL_RFSHSET1TMG0_FREQ3.t_refi_x1_sel == 1, DDRCTL_RFSHSET1TMG0_FREQ3.t_refi_x1_x32 must be greater than DDRCTL_RFSHSET1TMG1_FREQ3.t_rfc_min If DDRCTL_RFSHSET1TMG0_FREQ3.t_refi_x1_sel == 0, DDRCTL_RFSHSET1TMG0_FREQ3.t_refi_x1_x32 * 32 must be greater than DDRCTL_RFSHSET1TMG1_FREQ3.t_rfc_min DDRCTL_RFSHSET1TMG0_FREQ3.t_refi_x1_x32 must be less than or equal to 0xFFE. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on DDRCTL_RFSHSET1TMG0_FREQ3.t_refi_x1_sel. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x62 Programming Mode: Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG1_FREQ3

Address: **Operational Base** + offset (0x300604)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x08c	t_rfc_min tRFC (min): Minimum time from refresh to refresh or activate. t_rfc_min must be set to RoundUp(tRFCmin/tCK). In LPDDR controller, if using all-bank refreshes, the tRFCmin value in the above equations is equal to tRFCab. If using per-bank refreshes, the tRFCmin value in the above equations is equal to tRFCpb. Unit: DRAM clock cycles. Value After Reset: 0x8c Programming Mode: Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG2_FREQ3

Address: **Operational Base** + offset (0x300608)

Bit	Attr	Reset Value	Description
31:24	RW	0x8c	t_pbr2act Time from REFpb to activate command to different bank than REFpb. LPDDR5: tpbr2act Value After Reset: 0x8c Programming Mode: Dynamic - Refresh Related

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Bit	Attr	Reset Value	Description
23:16	RW	0x8c	t_pbr2pbr LPDDR4: tpbR2pbR Per-bank Refresh to Per-bank refresh different bank Time. Program this to RoundUp(tpbR2pbR/tCK). The tpbR2pbR value in the above equations is different depending on the device density. The user must program the appropriate value from the spec. Register is valid only in LPDDR4 per-bank refresh mode (DDRCTL_RFSHMOD0.per_bank_refresh == 1). Value After Reset: 0x8c Programming Mode: Dynamic - Refresh Related
15:0	RO	0x0000	reserved

DDRCTL_RFSHSET1TMG4_FREQ3

Address: **Operational Base** + offset (0x300610)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	refresh_timer1_start_value_x32 Refresh timer start for rank 1 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related
15:12	RO	0x0	reserved
11:0	RW	0x000	refresh_timer0_start_value_x32 Refresh timer start for rank 0 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Programming Mode: Dynamic - Refresh Related

DDRCTL_ZQSET1TMG0_FREQ3

Address: **Operational Base** + offset (0x300800)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x040	t_zq_short_nop tZQLAT for LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset: 0x40 Programming Mode: Static
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0200	t_zq_long_nop tZQCAL for LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM. If using LPDDR5, this register needs to be programmed to tZQCAL + 10 cycles. Unit: DRAM clock cycles. Value After Reset: 0x200 Programming Mode: Static

DDRCTL_ZQSET1TMG1_FREQ3

Address: **Operational Base** + offset (0x300804)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x020	t_zq_reset_nop tZQReset: Number of DRAM clock cycles of NOP required after a ZQReset (ZQ calibration Reset) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset: 0x20 Programming Mode: Static
19:0	RW	0x00100	t_zq_short_interval_x1024 Average interval to wait between automatically issuing ZQCS (ZQ calibration short)/MPC(ZQ calibration) commands to LPDDR4 devices. Meaningless, if DDRCTL_ZQCTL0.dis_auto_zq=1. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x100 Programming Mode: Static

DDRCTL_DQSOSCCTL0_FREQ3

Address: **Operational Base** + offset (0x300A80)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RW	0x007	dqsosc_interval DQS Oscillator interval, specifies the time between two DQS oscillator sequences. Minimum programmable value is 1. The value can be changed while DQSOSCCTL0.dqsosc_enable=0 Unit: DFI clock cycles Value After Reset: 0x7 Programming Mode: Dynamic
3	RO	0x0	reserved
2	RW	0x0	dqsosc_interval_unit DQS/WCK Oscillator Interval unit. Specifies the unit for counting DQS oscillator interval. The value can be changed while DQSOSCCTL0.dqsosc_enable=0 1'b1: x2K DFI clock cycles 1'b0: x32K DFI clock cycles Value After Reset: 0x0 Programming Mode: Dynamic
1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	dqsosc_enable DQS/WCK Oscillator Enable 1'b1: Enable DQS Oscillator 1'b0: Disable DQS Oscillator Value After Reset: 0x0 Programming Mode: Dynamic

DDRCTL_DERATEINT_FREQ3

Address: **Operational Base** + offset (0x300B00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00800000	mr4_read_interval Interval between two MR4 reads, used to derate the timing parameters. This register must not be set to zero. Unit: DRAM clock cycles. Value After Reset: 0x800000 Volatile: True Programming Mode: Static

DDRCTL_DERATEVAL0_FREQ3

Address: **Operational Base** + offset (0x300B04)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	derated_t_rcd Derated value for tRCD. For LPDDR4, the required period with derating is tRCD + 1.875ns For LPDDR5, the required period with derating is tRCD + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
23:16	RW	0x0f	derated_t_ras_min Derated value for tRAS. For LPDDR4, the required period with derating is tRAS + 1.875ns For LPDDR5, the required period with derating is tRAS + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
15	RO	0x0	reserved
14:8	RW	0x05	derated_t_rp Derated value for tRP. For LPDDR4, the required period with derating is tRP + 1.875ns For LPDDR5, the required period with derating is tRP + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x5 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x04	derated_t_rrd Derated value for tRRD. For LPDDR4, the required period with derating is tRRD + 1.875ns For LPDDR5, the required period with derating is tRRD + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x4 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_DERATEVAL1_FREQ3

Address: **Operational Base** + offset (0x300B08)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x14	derated_t_rc Derated value for tRC. For LPDDR4, the required period with derating is tRC + 3.75ns For LPDDR5, the required period with derating is tRC + TBD ns This timing parameter must be rounded up to the next integer value. Unit: DRAM clock cycles. Value After Reset: 0x14 Volatile: True Programming Mode: Quasi-dynamic Group 2, Group 4

DDRCTL_HWLPTMG0_FREQ3

Address: **Operational Base** + offset (0x300B80)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_lp_idle_x32 Hardware idle period. The cactive_ddrc output is driven low if the DDRC command channel is idle for hw_lp_idle * 32 cycles if not in INIT or DPD/MPSM operating_mode. The DDRC command channel is considered idle when there are no HIF commands outstanding. The hardware idle function is disabled when hw_lp_idle_x32=0. hw_lp_idle_x32=1 is an illegal value when the controller is in 1:2 mode. hw_lp_idle_x32=1/2/3 are illegal values when the controller is in 1:4 mode. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x0 Volatile: True Programming Mode: Static
15:0	RO	0x0000	reserved

DDRCTL_SCHEDTMG0_FREQ3

Address: **Operational Base** + offset (0x300C00)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
14:8	RW	0x00	rdwr_idle_gap When the preferred transaction store is empty for these many clock cycles, switch to the alternate transaction store if it is non-empty. The read transaction store (both high and low priority) is the default preferred transaction store and the write transaction store is the alternative store. When prefer write over read is set this is reversed. 0x0 is a legal value for this register. When set to 0x0, the transaction store switching will happen immediately when the switching conditions become true. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x0 Programming Mode: Static
7:0	RW	0x00	pageclose_timer This field works in conjunction with DDRCTL_SCHED0.pageclose. It only has meaning if DDRCTL_SCHED0.pageclose==1. If DDRCTL_SCHED0.pageclose==1 and pageclose_timer==0, then an auto-precharge may be scheduled for last read or write command in the CAM with a bank and page hit. Note, sometimes an explicit precharge is scheduled instead of the auto-precharge. See DDRCTL_SCHED0.pageclose for details of when this may happen. If DDRCTL_SCHED0.pageclose==1 and pageclose_timer>0, then an auto-precharge is not scheduled for last read or write command in the CAM with a bank and page hit. Instead, a timer is started, with pageclose_timer as the initial value. There is a timer on a per bank basis. The timer decrements unless the next read or write in the CAM to a bank is a page hit. It gets reset to pageclose_timer value if the next read or write in the CAM to a bank is a page hit. Once the timer has reached zero, an explcit precharge will be attempted to be scheduled. Unit: DRAM clock cycles. Value After Reset: 0x0 Programming Mode: Static

DDRCTL_PERFHPR1_FREQ3

Address: **Operational Base** + offset (0x300C80)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	hpr_xact_run_length Number of transactions that are serviced once the HPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available Unit: Transaction FOR PERFORMANCE ONLY. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0001	hpr_max_starve Number of DRAM clocks that the HPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x1 Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PERFLPR1_FREQ3

Address: **Operational Base** + offset (0x300C84)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	lpr_xact_run_length Number of transactions that are serviced once the LPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available Unit: Transaction FOR PERFORMANCE ONLY. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x00	reserved
15:0	RW	0x007f	lpr_max_starve Number of DRAM clocks that the LPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x7f Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_PERFWR1_FREQ3

Address: **Operational Base** + offset (0x300C88)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	w_xact_run_length Number of transactions that are serviced once the WR queue goes critical is the smaller of: (a) This number (b) Number of transactions available Unit: Transaction FOR PERFORMANCE ONLY. Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x007f	w_max_starve Number of DRAM clocks that the WR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset: 0x7f Volatile: True Programming Mode: Quasi-dynamic Group 3

DDRCTL_TMGCFG_FREQ3

Address: **Operational Base** + offset (0x300D00)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	dfi_freq_fsp This register value propergates to dfi_freq_fsp pin directly. Value After Reset: 0x0 Programming Mode: Dynamic
7:1	RO	0x00	reserved
0	RW	0x0	frequency_ratio Selects the Frequency Ratio For LPDDR4: 1'b0: 1:2 Mode 1'b1: 1:4 Mode For LPDDR5: 1'b0: 1:1:2 Mode 1'b1: 1:1:4 Mode Value After Reset: 0x0 Programming Mode: Quasi-dynamic Group 2

DDRCTL_RANKTMG0_FREQ3

Address: **Operational Base** + offset (0x300D04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x06	diff_rank_wr_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_wrcsgap (see PHY databook for value of tphy_wrcsgap) If CRC feature is enabled, must be increased by 1. Write preamble is always set to 2tCK for LPDDR4, refer to PHY databook to see if this is already factored into tphy_wrcsgap value or if it needs to be increased by 1. If write postamble is set to 1.5tCK(LPDDR4 only), must be increased by 1. ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, with DQ ODT enabled, diff_rank_wr_gap must be a

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Bit	Attr	Reset Value	Description
			minimum of ODTLoff - ODTLon - BL/2 + 1 For other cases, diff_rank_wr_gap must be a minimum of ODTCFG.wr_odt_hold - BL/2. Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay". Please see PHY databook for the value of tphy_wckcsgap. Unit: DRAM clock cycles. Value After Reset: 0x6 Volatile: True Programming Mode: Quasi-dynamic Group 2
7:0	RW	0x06	diff_rank_rd_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_rdcsgap (see PHY databook for value of tphy_rdcsgap) ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads: Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay". Please see PHY databook for the value of tphy_wckcsgap. Unit: DRAM clock cycles. Value After Reset: 0x6 Volatile: True Programming Mode: Quasi-dynamic Group 2

DDRCTL_RANKTMG1_FREQ3

Address: **Operational Base** + offset (0x300D08)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x0f	rd2wr_dr Minimum time from read command to write command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. The value must be larger than or equal to the value of DRAMSET1TMG2.rd2wr. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay". Please see PHY databook for the value of tphy_wckcsgap. Unit: DRAM clock cycles Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

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Bit	Attr	Reset Value	Description
7:0	RW	0x0f	wr2rd_dr Minimum time from write command to read command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay". Please see PHY databook for the value of tphy_wckcsgap. Unit: DRAM clock cycles Value After Reset: 0xf Volatile: True Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_PWRTMG_FREQ3

Address: **Operational Base** + offset (0x300D0C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x040	selfref_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into Self Refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x40 Volatile: True Programming Mode: Quasi-dynamic Group 4
15:7	RO	0x000	reserved
6:0	RW	0x10	powerdown_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into power-down. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset: 0x10 Volatile: True Programming Mode: Quasi-dynamic Group 4

7.4.4 Internal Address Mapping For DDRPHY

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
DDRPHY0	0x2A020000
DDRPHY1	0x2A030000

7.4.5 Registers Summary For DDRPHY

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Name	Offset	Size	Reset Value	Description
DDRPHY_GNR_CON0	0x0000	W	0x44005011	General Control Register 0
DDRPHY_CAL_CON0	0x0004	W	0x789606C0	Calibration Control Register 0
DDRPHY_CAL_CON1	0x0008	W	0x20142001	Calibration Control Register 1
DDRPHY_CAL_CON2	0x000C	W	0x42001300	Calibration Control Register 2
DDRPHY_CAL_CON3	0x0010	W	0xFC7F9000	Calibration Control Register 3
DDRPHY_CAL_CON4	0x0014	W	0x0083806F	Calibration Control Register 4
DDRPHY_LP_CON0	0x0018	W	0x000C4403	Low Power Control Register 0
DDRPHY_GATE_CON0	0x001C	W	0x03003003	Gate Control Register 0
DDRPHY_OFFSETR_CON0	0x0020	W	0x00000000	Read DQS Code Offset Control Register 0
DDRPHY_OFFSETW_CON0	0x0030	W	0x00000000	Write DQ Code Offset Control Register 0
DDRPHY_OFFSET_DQ_CON0	0x003C	W	0x00000000	Read DQ Code Offset Control Register 0
DDRPHY_OFFSETC_CON0	0x0040	W	0x00000000	Gate Code Offset Control Register 0
DDRPHY_SHIFTC_CON0	0x004C	W	0x00000000	Gate Code Shift Control Register 0
DDRPHY_OFFSETD_CON0	0x0050	W	0x00000000	CMD Code Offset Control Register
DDRPHY_OFFSETO_CON0	0x0058	W	0x00000000	DQ/DM OEN Code Offset Control Register 0
DDRPHY_WR_LVL_CON0	0x006C	W	0x00000000	Write Levelling Control Register 0
DDRPHY_WR_LVL_CON1	0x0070	W	0x01E80473	Write Levelling Control Register 1
DDRPHY_WR_LVL_CON2	0x0074	W	0x40465580	Write Levelling Control Register 2
DDRPHY_WR_LVL_CON3	0x0078	W	0x00000B00	Write Levelling Control Register 3
DDRPHY_CA_DESKEW_CON0	0x007C	W	0x00000000	CA De-skew Control Register 0
DDRPHY_CA_DESKEW_CON1	0x0080	W	0x00000000	CA De-skew Control Register 1
DDRPHY_CA_DESKEW_CON2	0x0084	W	0x00000000	CA De-skew Control Register 2
DDRPHY_CA_DESKEW_CON3	0x0088	W	0x00000000	CA De-skew Control Register 3
DDRPHY_CA_DESKEW_CON4	0x008C	W	0x00000000	CA De-skew Control Register 4
DDRPHY_CA_DESKEW_CON5	0x0090	W	0x00000000	CA De-skew Control Register 5
DDRPHY_CA_DESKEW_CON6	0x0094	W	0x00000000	CA De-skew Control Register 6
DDRPHY_CAL_WR_PATTERN_CON0	0x0098	W	0x00FF00FF	Write Calibration Pattern Register 0
DDRPHY_CAL_WR_PATTERN_CON1	0x009C	W	0x00FF00FF	Write Calibration Pattern Register 1
DDRPHY_CAL_WR_PATTERN_CON2	0x00A0	W	0x00FF00FF	Write Calibration Pattern Register 2
DDRPHY_CAL_WR_PATTERN_CON3	0x00A4	W	0x00FF00FF	Write Calibration Pattern Register 3
DDRPHY_CAL_WR_PATTERN_CON4	0x00A8	W	0x00005555	Write Calibration Pattern Register 4
DDRPHY_CAL_RD_PATTERN_CON0	0x00AC	W	0x55555A3C	Read Calibration Pattern Register 0
DDRPHY_MDLL_CON0	0x00B0	W	0x2000017E	MDLL Control Register 0
DDRPHY_MDLL_CON1	0x00B4	W	0x00200100	MDLL Control Register 1
DDRPHY_DVFS_CON	0x00B8	W	0x00002640	DVFS Control Register

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Name	Offset	Size	Reset Value	Description
DDRPHY_DVFS0_CON0	0x00BC	W	0x64080C06	DVFS0 Control Register 0
DDRPHY_DVFS1_CON0	0x00C0	W	0x64080C06	DVFS1 Control Register 0
DDRPHY_DVFS0_CON1	0x00C4	W	0x30800000	DVFS0 Control Register 1
DDRPHY_DVFS1_CON1	0x00C8	W	0x30800000	DVFS1 Control Register 1
DDRPHY_DVFS0_CON2	0x00CC	W	0x60062001	DVFS0 Control Register 2
DDRPHY_DVFS1_CON2	0x00D0	W	0x60062001	DVFS1 Control Register 2
DDRPHY_DVFS0_CON3	0x00D4	W	0x0003FFFF	DVFS0 Control Register 3
DDRPHY_DVFS1_CON3	0x00D8	W	0x0003FFFF	DVFS1 Control Register 3
DDRPHY_DVFS0_CON4	0x00DC	W	0x00243F3F	DVFS0 Control Register 4
DDRPHY_DVFS1_CON4	0x00E0	W	0x00243F3F	DVFS1 Control Register 4
DDRPHY_CAL_WRLVL_STAT	0x00E4	W	0x00000000	Write Levelling Status Register
DDRPHY_CAL_FAIL_STAT0	0x00E8	W	0x00000000	Calibration Fail Status Register 0
DDRPHY_CAL_FAIL_STAT1	0x00EC	W	0x00000000	Calibration Fail Status Register 1
DDRPHY_CAL_GT_CS0_VWMC0	0x00F0	W	0x00000000	Gate Training Center Code CS0 Register 0
DDRPHY_CAL_GT_CS0_CYC	0x00FC	W	0x00000000	Gate Training CS0 Cycle Register
DDRPHY_CAL_RD_VWMC0	0x0100	W	0x00000000	Read Calibration Center Code 0
DDRPHY_CAL_RD_VWML0	0x0110	W	0x00000000	Read Calibration Left Code 0
DDRPHY_CAL_RD_VWMR0	0x0120	W	0x00000000	Read Calibration Right Code 0
DDRPHY_CAL_WR_VWMC0	0x0130	W	0x00000000	Write Calibration Center Code 0
DDRPHY_CAL_WR_VWML0	0x0140	W	0x00000000	Write Calibration Left Code 0
DDRPHY_CAL_WR_VWMR0	0x0150	W	0x00000000	Write Calibration Right Code 0
DDRPHY_CAL_CON5	0x0160	W	0x00000000	Calibration Control Register 5
DDRPHY_DVFS_UPD_CON0	0x0164	W	0x003F3F3F	DVFS Update Control Register 0
DDRPHY_DVFS_UPD_CON1	0x0168	W	0x003F3F3F	DVFS Update Control Register 1
DDRPHY_RD_DESKEW_CENTER_CS0_CON_DM	0x018C	W	0x00000000	Read DM De-skew CS0 Center Code Control Register
DDRPHY_RD_DESKEW_CENTER_CS0_CON0	0x0190	W	0x00000000	Read DQ De-skew CS0 Center Code Control Register 0
DDRPHY_RD_DESKEW_CENTER_CS0_CON1	0x019C	W	0x00000000	Read DQ De-skew CS0 Center Code Control Register 1
DDRPHY_RD_DESKEW_CENTER_CS0_CON2	0x01A8	W	0x00000000	Read DQ De-skew CS0 Center Code Control Register 2
DDRPHY_RD_DESKEW_CENTER_CS0_CON3	0x01B4	W	0x00000000	Read DQ De-skew CS0 Center Code Control Register 3
DDRPHY_RD_DESKEW_CENTER_CS0_CON4	0x01C0	W	0x00000000	Read DQ De-skew CS0 Center Code Control Register 4
DDRPHY_RD_DESKEW_CENTER_CS0_CON5	0x01CC	W	0x00000000	Read DQ De-skew CS0 Center Code Control Register 5
DDRPHY_RD_DESKEW_CENTER_CS0_CON6	0x01D8	W	0x00000000	Read DQ De-skew CS0 Center Code Control Register 6
DDRPHY_RD_DESKEW_CENTER_CS0_CON7	0x01E4	W	0x00000000	Read DQ De-skew CS0 Center Code Control Register 7
DDRPHY_WR_DESKEWC_CS0_CON0	0x01F0	W	0x00000000	Write DQ De-skew CS0 Center Code Control Register 0

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Name	Offset	Size	Reset Value	Description
DDRPHY_WR_DESKEWC_CS0_CON1	0x01FC	W	0x00000000	Write DQ De-skew CS0 Center Code Control Register 1
DDRPHY_WR_DESKEWC_CS0_CON2	0x0208	W	0x00000000	Write DQ De-skew CS0 Center Code Control Register 2
DDRPHY_WR_DESKEWC_CS0_CON3	0x0214	W	0x00000000	Write DQ De-skew CS0 Center Code Control Register 3
DDRPHY_WR_DESKEWC_CS0_CON4	0x0220	W	0x00000000	Write DQ De-skew CS0 Center Code Control Register 4
DDRPHY_WR_DESKEWC_CS0_CON5	0x022C	W	0x00000000	Write DQ De-skew CS0 Center Code Control Register 5
DDRPHY_WR_DESKEWC_CS0_CON6	0x0238	W	0x00000000	Write DQ De-skew CS0 Center Code Control Register 6
DDRPHY_WR_DESKEWC_CS0_CON7	0x0244	W	0x00000000	Write DQ De-skew CS0 Center Code Control Register 7
DDRPHY_DM_DESKEWC_CS0_CON0	0x0250	W	0x00000000	Write DM De-skew CS0 Center Code Control Register 0
DDRPHY_VWMC_STAT0	0x025C	W	0x00000000	VWMC Status 0
DDRPHY_VWMC_STAT3	0x0268	W	0x00000000	VWMC Status 3
DDRPHY_VWMC_STAT6	0x0274	W	0x00000000	VWMC Status 6
DDRPHY_VWMC_STAT9	0x0280	W	0x00000000	VWMC Status 9
DDRPHY_VWMC_STAT12	0x028C	W	0x00000000	VWMC Status 12
DDRPHY_VWMC_STAT15	0x0298	W	0x00000000	VWMC Status 15
DDRPHY_VWMC_STAT18	0x02A4	W	0x00000000	VWMC Status 18
DDRPHY_VWMC_STAT21	0x02B0	W	0x00000000	VWMC Status 21
DDRPHY_DM_VWMC_STAT0	0x02BC	W	0x00000000	DM VWMC Status 0
DDRPHY_VWML_STAT0	0x02C8	W	0x00000000	VWML Status 0
DDRPHY_VWML_STAT3	0x02D4	W	0x00000000	VWML Status 3
DDRPHY_VWML_STAT6	0x02E0	W	0x00000000	VWML Status 6
DDRPHY_VWML_STAT9	0x02EC	W	0x00000000	VWML Status 9
DDRPHY_VWML_STAT12	0x02F8	W	0x00000000	VWML Status 12
DDRPHY_VWML_STAT15	0x0304	W	0x00000000	VWML Status 15
DDRPHY_VWML_STAT18	0x0310	W	0x00000000	VWML Status 18
DDRPHY_VWML_STAT21	0x031C	W	0x00000000	VWML Status 21
DDRPHY_DM_VWML_STAT0	0x0328	W	0x00000000	DM VWML Status 0
DDRPHY_VWMR_STAT0	0x0334	W	0x00000000	VWMR Status 0
DDRPHY_VWMR_STAT3	0x0340	W	0x00000000	VWMR Status 3
DDRPHY_VWMR_STAT6	0x034C	W	0x00000000	VWMR Status 6
DDRPHY_VWMR_STAT9	0x0358	W	0x00000000	VWMR Status 9
DDRPHY_VWMR_STAT12	0x0364	W	0x00000000	VWMR Status 12
DDRPHY_VWMR_STAT15	0x0370	W	0x00000000	VWMR Status 15
DDRPHY_VWMR_STAT18	0x037C	W	0x00000000	VWMR Status 18
DDRPHY_VWMR_STAT21	0x0388	W	0x00000000	VWMR Status 21
DDRPHY_DM_VWMR_STAT0	0x0394	W	0x00000000	DM VWMR Status 0
DDRPHY_DQ_IO_RDATA0	0x03A0	W	0x00000000	DQ I/O Read Data Status 0
DDRPHY_VERSION_INFO_STAT0	0x03AC	W	0x09080005	Version Information
DDRPHY_ZQ_CON0	0x03C8	W	0xFF807404	ZQ Control Register 0
DDRPHY_ZQ_CON1	0x03CC	W	0x00140000	ZQ Control Register 1
DDRPHY_ZQ_CON2	0x03D0	W	0x001E0002	ZQ Control Register 2
DDRPHY_ZQ_CON3	0x03D4	W	0x003F3F3F	ZQ Control Register 3

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Name	Offset	Size	Reset Value	Description
DDRPHY_ZQ_CON5	0x03DC	W	0x073F0000	ZQ Control Register 5
DDRPHY_ZQ_CON6	0x03E0	W	0x00002121	ZQ Control Register 6
DDRPHY_ZQ_CON9	0x03EC	W	0x00001414	ZQ Control Register 9
DDRPHY_ZQ_CON12	0x03F8	W	0x00000707	ZQ Control Register 12
DDRPHY_TESTIRCV_CON0	0x0400	W	0x00080000	ZQ And Test Control Register
DDRPHY_WR_DESKEWC_CS1_CON0	0x0410	W	0x00000000	Write DQ De-skew CS1 Center Code Control Register 0
DDRPHY_WR_DESKEWC_CS1_CON1	0x041C	W	0x00000000	Write DQ De-skew CS1 Center Code Control Register 1
DDRPHY_WR_DESKEWC_CS1_CON2	0x0428	W	0x00000000	Write DQ De-skew CS1 Center Code Control Register 2
DDRPHY_WR_DESKEWC_CS1_CON3	0x0434	W	0x00000000	Write DQ De-skew CS1 Center Code Control Register 3
DDRPHY_WR_DESKEWC_CS1_CON4	0x0440	W	0x00000000	Write DQ De-skew CS1 Center Code Control Register 4
DDRPHY_WR_DESKEWC_CS1_CON5	0x044C	W	0x00000000	Write DQ De-skew CS1 Center Code Control Register 5
DDRPHY_WR_DESKEWC_CS1_CON6	0x0458	W	0x00000000	Write DQ De-skew CS1 Center Code Control Register 6
DDRPHY_WR_DESKEWC_CS1_CON7	0x0464	W	0x00000000	Write DQ De-skew CS1 Center Code Control Register 7
DDRPHY_DM_DESKEWC_CS1_CON0	0x0470	W	0x00000000	Write DM De-skew CS1 Center Code Control Register 0
DDRPHY_WR_DESKEWL_CS0_CON0	0x0490	W	0x00000000	Write DQ De-skew CS0 Left Code Control Register 0
DDRPHY_WR_DESKEWL_CS0_CON1	0x049C	W	0x00000000	Write DQ De-skew CS0 Left Code Control Register 1
DDRPHY_WR_DESKEWL_CS0_CON2	0x04A8	W	0x00000000	Write DQ De-skew CS0 Left Code Control Register 2
DDRPHY_WR_DESKEWL_CS0_CON3	0x04B4	W	0x00000000	Write DQ De-skew CS0 Left Code Control Register 3
DDRPHY_WR_DESKEWL_CS0_CON4	0x04C0	W	0x00000000	Write DQ De-skew CS0 Left Code Control Register 4
DDRPHY_WR_DESKEWL_CS0_CON5	0x04CC	W	0x00000000	Write DQ De-skew CS0 Left Code Control Register 5
DDRPHY_WR_DESKEWL_CS0_CON6	0x04D8	W	0x00000000	Write DQ De-skew CS0 Left Code Control Register 6
DDRPHY_WR_DESKEWL_CS0_CON7	0x04E4	W	0x00000000	Write DQ De-skew CS0 Left Code Control Register 7
DDRPHY_DM_DESKEWL_CS0_CON0	0x04F0	W	0x00000000	Write DM De-skew CS0 Left Code Control Register 0
DDRPHY_WR_DESKEWL_CS1_CON0	0x0500	W	0x00000000	Write DQ De-skew CS1 Left Code Control Register 0
DDRPHY_WR_DESKEWL_CS1_CON1	0x050C	W	0x00000000	Write DQ De-skew CS1 Left Code Control Register 1
DDRPHY_WR_DESKEWL_CS1_CON2	0x0518	W	0x00000000	Write DQ De-skew CS1 Left Code Control Register 2
DDRPHY_WR_DESKEWL_CS1_CON3	0x0524	W	0x00000000	Write DQ De-skew CS1 Left Code Control Register 3
DDRPHY_WR_DESKEWL_CS1_CON4	0x0530	W	0x00000000	Write DQ De-skew CS1 Left Code Control Register 4
DDRPHY_WR_DESKEWL_CS1_CON5	0x053C	W	0x00000000	Write DQ De-skew CS1 Left Code Control Register 5

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Name	Offset	Size	Reset Value	Description
DDRPHY_WR_DESKEWL_CS1_CON6	0x0548	W	0x00000000	Write DQ De-skew CS1 Left Code Control Register 6
DDRPHY_WR_DESKEWL_CS1_CON7	0x0554	W	0x00000000	Write DQ De-skew CS1 Left Code Control Register 7
DDRPHY_DM_DESKEWL_CS1_CON0	0x0560	W	0x00000000	Write DM De-skew CS1 Left Code Control Register 0
DDRPHY_RD_DQS_VWML_CS0_CON0	0x0574	W	0x00000000	Read DQS CS0 Left Code Control Register 0
DDRPHY_RD_DQS_VWMC_CS0_CON0	0x0580	W	0x00000000	Read DQS CS0 Center Code Control Register 0
DDRPHY_GT_STATUS_CON0	0x058C	W	0x00000000	Gate Status Register 0
DDRPHY_GT_STATUS_CON1	0x0590	W	0x00000000	Gate Status Register 1
DDRPHY_GT_FSM_STATUS_CON1	0x0594	W	0x00000000	Gate FSM Status register 1
DDRPHY_CAL_GT_CS1_VWMC0	0x05E4	W	0x00000000	Gate Training CS1 Center Code
DDRPHY_CAL_GT_CS1_CYC	0x05F0	W	0x00000000	Gate Training CS1 Cycle
DDRPHY_CBT_CON5	0x05F4	W	0x000D3400	Command Bus Training Control Register 5
DDRPHY_CBT_CMD	0x05FC	W	0x0000043F	Command Bus Training CMD Register
DDRPHY_CBT_CON0	0x0600	W	0x0000004D	Command Bus Training Control Register 0
DDRPHY_CBT_CON2	0x0608	W	0x00006300	Command Bus Training Control Register 2
DDRPHY_CBT_CON3	0x060C	W	0x00C80000	Command Bus Training Control Register 3
DDRPHY_RD_DESKEW_LEFT_CS0_CON_DM	0x0610	W	0x00000000	Read DM De-skew CS0 Left Code Control Register
DDRPHY_RD_DESKEW_LEFT_CS0_CON0	0x0614	W	0x00000000	Read DQ De-skew CS0 Left Code Control Register 0
DDRPHY_RD_DESKEW_LEFT_CS0_CON1	0x0620	W	0x00000000	Read DQ De-skew CS0 Left Code Control Register 1
DDRPHY_RD_DESKEW_LEFT_CS0_CON2	0x062C	W	0x00000000	Read DQ De-skew CS0 Left Code Control Register 2
DDRPHY_RD_DESKEW_LEFT_CS0_CON3	0x0638	W	0x00000000	Read DQ De-skew CS0 Left Code Control Register 3
DDRPHY_RD_DESKEW_LEFT_CS0_CON4	0x0644	W	0x00000000	Read DQ De-skew CS0 Left Code Control Register 4
DDRPHY_RD_DESKEW_LEFT_CS0_CON5	0x0650	W	0x00000000	Read DQ De-skew CS0 Left Code Control Register 5
DDRPHY_RD_DESKEW_LEFT_CS0_CON6	0x065C	W	0x00000000	Read DQ De-skew CS0 Left Code Control Register 6
DDRPHY_RD_DESKEW_LEFT_CS0_CON7	0x0668	W	0x00000000	Read DQ De-skew CS0 Left Code Control Register 7
DDRPHY_FREQ_OFFSET_CON	0x0680	W	0x00000000	Frequency Offset Configure Register
DDRPHY_PRBS_CON0	0x0684	W	0x00050000	PRBS Control Register 0
DDRPHY_PRBS_CON1	0x0688	W	0x0542010C	PRBS Control Register 1
DDRPHY_PRBS_CON2	0x068C	W	0x00000000	PRBS Control Register 2
DDRPHY_PRBS_CON3	0x0690	W	0x00000000	PRBS Control Register 3

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Name	Offset	Size	Reset Value	Description
DDRPHY_PRBS_CON4	0x0694	W	0x00000000	PRBS Control Register 4
DDRPHY_PRBS_CON5	0x0698	W	0x00000000	PRBS Control Register 5
DDRPHY_PRBS_CON6	0x069C	W	0x00000000	PRBS Control Register 6
DDRPHY_PRBS_CON7	0x06A0	W	0x00000000	PRBS Control Register 7
DDRPHY_PRBS_CON8	0x06A4	W	0x800B0000	PRBS Control Register 8
DDRPHY_PRBS_CON9	0x06A8	W	0x00FF00FF	PRBS Control Register 9
DDRPHY_PRBS_CON10	0x06AC	W	0x0F0F0F0F	PRBS Control Register 10
DDRPHY_PRBS_CON11	0x06B0	W	0x5A5A5A5A	PRBS Control Register 11
DDRPHY_PRBS_CON12	0x06B4	W	0xFF00FF00	PRBS Control Register 12
DDRPHY_PRBS_CON13	0x06B8	W	0x00000055	PRBS Control Register 13
DDRPHY_DUTY_CAL0	0x06BC	W	0x00000000	Duty Calibration Register 0
DDRPHY_MON_CON0	0x0700	W	0x00020000	Debug Mode Register 0
DDRPHY_MON_CON1	0x0704	W	0x00000000	Debug Mode Register 1
DDRPHY_MON_CON2	0x0708	W	0x00000000	Debug Mode Register 2
DDRPHY_MON_CON3	0x070C	W	0x00000000	Debug Mode Register 3
DDRPHY_MON_CON4	0x0710	W	0x00000000	Debug Mode Register 4
DDRPHY_MON_CON5	0x0714	W	0x00000000	Debug Mode Register 5
DDRPHY_MON_CON6	0x0718	W	0x00000000	Debug Mode Register 6
DDRPHY_MON_CON7	0x071C	W	0x00000000	Debug Mode Register 7
DDRPHY_WR_TRAIN_MON0	0x0720	W	0x00000000	Write Training Monitor Register 0
DDRPHY_LOCK_VAL0	0x0728	W	0x001FFC01	DVFS0 Master DLL Status Register 0
DDRPHY_LOCK_VAL1	0x072C	W	0x001FFC01	DVFS1 Master DLL Status Register 1
DDRPHY_LOCK_VAL2	0x0730	W	0x001FFC01	Master DLL Status Register 2
DDRPHY_WR_CHECK_CON0	0x0750	W	0x00000000	FIFO Status Register 0
DDRPHY_WR_CHECK_CON1	0x0754	W	0x00000000	FIFO Status Register 1
DDRPHY_WR_CHECK_CON2	0x0760	W	0x00000000	FIFO Status Register 2
DDRPHY_RD_DQS_VWML_CS1_CON0	0x0764	W	0x00000000	Read DQS CS1 Left Code Control Register 0
DDRPHY_RD_DQS_VWMC_CS1_CON0	0x0768	W	0x00000000	Read DQS CS1 Center Code Control Register 0
DDRPHY_RD_DESKEW_CENTER_CS1_CON_DM	0x076C	W	0x00000000	Read DM De-skew CS1 Center Code Control Register
DDRPHY_RD_DESKEW_CENTER_CS1_CON0	0x0770	W	0x00000000	Read DQ De-skew CS1 Center Code Control Register 0
DDRPHY_RD_DESKEW_CENTER_CS1_CON1	0x0774	W	0x00000000	Read DQ De-skew CS1 Center Code Control Register 1
DDRPHY_RD_DESKEW_CENTER_CS1_CON2	0x0778	W	0x00000000	Read DQ De-skew CS1 Center Code Control Register 2
DDRPHY_RD_DESKEW_CENTER_CS1_CON3	0x077C	W	0x00000000	Read DQ De-skew CS1 Center Code Control Register 3
DDRPHY_RD_DESKEW_CENTER_CS1_CON4	0x0780	W	0x00000000	Read DQ De-skew CS1 Center Code Control Register 4
DDRPHY_RD_DESKEW_CENTER_CS1_CON5	0x0784	W	0x00000000	Read DQ De-skew CS1 Center Code Control Register 5
DDRPHY_RD_DESKEW_CENTER_CS1_CON6	0x0788	W	0x00000000	Read DQ De-skew CS1 Center Code Control Register 6

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Name	Offset	Size	Reset Value	Description
DDRPHY_RD_DESKEW_CENTER_CS1_CON7	0x078C	W	0x00000000	Read DQ De-skew CS1 Center Code Control Register 7
DDRPHY_RD_DESKEW_LEFT_CS1_CON_DM	0x0790	W	0x00000000	Read DM De-skew CS1 Left Code Control Register
DDRPHY_RD_DESKEW_LEFT_CS1_CON0	0x0794	W	0x00000000	Read DQ De-skew CS1 Left Code Control Register 0
DDRPHY_RD_DESKEW_LEFT_CS1_CON1	0x0798	W	0x00000000	Read DQ De-skew CS1 Left Code Control Register 1
DDRPHY_RD_DESKEW_LEFT_CS1_CON2	0x079C	W	0x00000000	Read DQ De-skew CS1 Left Code Control Register 2
DDRPHY_RD_DESKEW_LEFT_CS1_CON3	0x07A0	W	0x00000000	Read DQ De-skew CS1 Left Code Control Register 3
DDRPHY_RD_DESKEW_LEFT_CS1_CON4	0x07A4	W	0x00000000	Read DQ De-skew CS1 Left Code Control Register 4
DDRPHY_RD_DESKEW_LEFT_CS1_CON5	0x07A8	W	0x00000000	Read DQ De-skew CS1 Left Code Control Register 5
DDRPHY_RD_DESKEW_LEFT_CS1_CON6	0x07AC	W	0x00000000	Read DQ De-skew CS1 Left Code Control Register 6
DDRPHY_RD_DESKEW_LEFT_CS1_CON7	0x07B0	W	0x00000000	Read DQ De-skew CS1 Left Code Control Register 7
DDRPHY_SW_RD_DQS_VWML_CS0_CON0	0x07C0	W	0x00000000	SW Read DQS CS0 Left Code Control Register 0
DDRPHY_SW_RD_DQS_VWMC_CS0_CON0	0x07C4	W	0x00000000	SW Read DQS CS0 Center Code Control Register 0
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON_DM	0x07C8	W	0x00000000	SW Read DM De-skew CS0 Center Code Control Register
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON0	0x07CC	W	0x00000000	SW Read DQ De-skew CS0 Center Code Control Register 0
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON1	0x07D0	W	0x00000000	SW Read DQ De-skew CS0 Center Code Control Register 1
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON2	0x07D4	W	0x00000000	SW Read DQ De-skew CS0 Center Code Control Register 2
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON3	0x07D8	W	0x00000000	SW Read DQ De-skew CS0 Center Code Control Register 3
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON4	0x07DC	W	0x00000000	SW Read DQ De-skew CS0 Center Code Control Register 4
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON5	0x07E0	W	0x00000000	SW Read DQ De-skew CS0 Center Code Control Register 5
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON6	0x07E4	W	0x00000000	SW Read DQ De-skew CS0 Center Code Control Register 6
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON7	0x07E8	W	0x00000000	SW Read DQ De-skew CS0 Center Code Control Register 7
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON_DM	0x07F0	W	0x00000000	SW Read DM De-skew CS0 Left Code Control Register
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON0	0x07F4	W	0x00000000	SW Read DQ De-skew CS0 Left Code Control Register 0
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON1	0x07F8	W	0x00000000	SW Read DQ De-skew CS0 Left Code Control Register 1
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON2	0x07FC	W	0x00000000	SW Read DQ De-skew CS0 Left Code Control Register 2
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON3	0x0800	W	0x00000000	SW Read DQ De-skew CS0 Left Code Control Register 3

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Name	Offset	Size	Reset Value	Description
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON4	0x0804	W	0x00000000	SW Read DQ De-skew CS0 Left Code Control Register 4
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON5	0x0808	W	0x00000000	SW Read DQ De-skew CS0 Left Code Control Register 5
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON6	0x080C	W	0x00000000	SW Read DQ De-skew CS0 Left Code Control Register 6
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON7	0x0810	W	0x00000000	SW Read DQ De-skew CS0 Left Code Control Register 7
DDRPHY_SW_RD_DQS_VWML_CS1_CON0	0x0814	W	0x00000000	SW Read DQS CS1 Left Code Control Register 0
DDRPHY_SW_RD_DQS_VWMC_CS1_CON0	0x0818	W	0x00000000	SW Read DQS CS1 Center Code Control Register 0
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON_DM	0x0820	W	0x00000000	SW Read DM De-skew CS1 Center Code Control Register
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON0	0x0824	W	0x00000000	SW Read DQ De-skew CS1 Center Code Control Register 0
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON1	0x0828	W	0x00000000	SW Read DQ De-skew CS1 Center Code Control Register 1
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON2	0x082C	W	0x00000000	SW Read DQ De-skew CS1 Center Code Control Register 2
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON3	0x0830	W	0x00000000	SW Read DQ De-skew CS1 Center Code Control Register 3
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON4	0x0834	W	0x00000000	SW Read DQ De-skew CS1 Center Code Control Register 4
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON5	0x0838	W	0x00000000	SW Read DQ De-skew CS1 Center Code Control Register 5
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON6	0x083C	W	0x00000000	SW Read DQ De-skew CS1 Center Code Control Register 6
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON7	0x0840	W	0x00000000	SW Read DQ De-skew CS1 Center Code Control Register 7
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON_DM	0x0850	W	0x00000000	SW Read DM De-skew CS1 Left Code Control Register
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON0	0x0854	W	0x00000000	SW Read DQ De-skew CS1 Left Code Control Register 0
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON1	0x0858	W	0x00000000	SW Read DQ De-skew CS1 Left Code Control Register 1
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON2	0x085C	W	0x00000000	SW Read DQ De-skew CS1 Left Code Control Register 2
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON3	0x0860	W	0x00000000	SW Read DQ De-skew CS1 Left Code Control Register 3
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON4	0x0864	W	0x00000000	SW Read DQ De-skew CS1 Left Code Control Register 4
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON5	0x0868	W	0x00000000	SW Read DQ De-skew CS1 Left Code Control Register 5
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON6	0x086C	W	0x00000000	SW Read DQ De-skew CS1 Left Code Control Register 6
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON7	0x0870	W	0x00000000	SW Read DQ De-skew CS1 Left Code Control Register 7
DDRPHY_SW_WR_DESKEWC_CS0_CON0	0x0880	W	0x00000000	SW Write DQ De-skew CS0 Center Code Control Register 0
DDRPHY_SW_WR_DESKEWC_CS0_CON1	0x0884	W	0x00000000	SW Write DQ De-skew CS0 Center Code Control Register 1

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Name	Offset	Size	Reset Value	Description
DDRPHY_SW_WR_DESKEWC_CS0_CON2	0x0888	W	0x00000000	SW Write DQ De-skew CS0 Center Code Control Register 2
DDRPHY_SW_WR_DESKEWC_CS0_CON3	0x088C	W	0x00000000	SW Write DQ De-skew CS0 Center Code Control Register 3
DDRPHY_SW_WR_DESKEWC_CS0_CON4	0x0890	W	0x00000000	SW Write DQ De-skew CS0 Center Code Control Register 4
DDRPHY_SW_WR_DESKEWC_CS0_CON5	0x0894	W	0x00000000	SW Write DQ De-skew CS0 Center Code Control Register 5
DDRPHY_SW_WR_DESKEWC_CS0_CON6	0x0898	W	0x00000000	SW Write DQ De-skew CS0 Center Code Control Register 6
DDRPHY_SW_WR_DESKEWC_CS0_CON7	0x089C	W	0x00000000	SW Write DQ De-skew CS0 Center Code Control Register 7
DDRPHY_SW_DM_DESKEWC_CS0_CON0	0x08A0	W	0x00000000	SW Write DM De-skew CS0 Center Code Control Register 0
DDRPHY_SW_WR_DESKEWL_CS0_CON0	0x08B0	W	0x00000000	SW Write DQ De-skew CS0 Left Code Control Register 0
DDRPHY_SW_WR_DESKEWL_CS0_CON1	0x08B4	W	0x00000000	SW Write DQ De-skew CS0 Left Code Control Register 1
DDRPHY_SW_WR_DESKEWL_CS0_CON2	0x08B8	W	0x00000000	SW Write DQ De-skew CS0 Left Code Control Register 2
DDRPHY_SW_WR_DESKEWL_CS0_CON3	0x08BC	W	0x00000000	SW Write DQ De-skew CS0 Left Code Control Register 3
DDRPHY_SW_WR_DESKEWL_CS0_CON4	0x08C0	W	0x00000000	SW Write DQ De-skew CS0 Left Code Control Register 4
DDRPHY_SW_WR_DESKEWL_CS0_CON5	0x08C4	W	0x00000000	SW Write DQ De-skew CS0 Left Code Control Register 5
DDRPHY_SW_WR_DESKEWL_CS0_CON6	0x08C8	W	0x00000000	SW Write DQ De-skew CS0 Left Code Control Register 6
DDRPHY_SW_WR_DESKEWL_CS0_CON7	0x08CC	W	0x00000000	SW Write DQ De-skew CS0 Left Code Control Register 7
DDRPHY_SW_WR_DM_DESKEWL_CS0_CON0	0x08D0	W	0x00000000	SW Write DM De-skew CS0 Left Code Control Register 0
DDRPHY_SW_WR_DESKEWC_CS1_CON0	0x08E0	W	0x00000000	SW Write DQ De-skew CS1 Center Code Control Register 0
DDRPHY_SW_WR_DESKEWC_CS1_CON1	0x08E4	W	0x00000000	SW Write DQ De-skew CS1 Center Code Control Register 1
DDRPHY_SW_WR_DESKEWC_CS1_CON2	0x08E8	W	0x00000000	SW Write DQ De-skew CS1 Center Code Control Register 2
DDRPHY_SW_WR_DESKEWC_CS1_CON3	0x08EC	W	0x00000000	SW Write DQ De-skew CS1 Center Code Control Register 3
DDRPHY_SW_WR_DESKEWC_CS1_CON4	0x08F0	W	0x00000000	SW Write DQ De-skew CS1 Center Code Control Register 4
DDRPHY_SW_WR_DESKEWC_CS1_CON5	0x08F4	W	0x00000000	SW Write DQ De-skew CS1 Center Code Control Register 5
DDRPHY_SW_WR_DESKEWC_CS1_CON6	0x08F8	W	0x00000000	SW Write DQ De-skew CS1 Center Code Control Register 6
DDRPHY_SW_WR_DESKEWC_CS1_CON7	0x08FC	W	0x00000000	SW Write DQ De-skew CS1 Center Code Control Register 7
DDRPHY_SW_WR_DM_DESKEWC_CS1_CON0	0x0900	W	0x00000000	SW Write DM De-skew CS1 Center Code Control Register 0
DDRPHY_SW_WR_DESKEWL_CS1_CON0	0x0910	W	0x00000000	SW Write DQ De-skew CS1 Left Code Control Register 0
DDRPHY_SW_WR_DESKEWL_CS1_CON1	0x0914	W	0x00000000	SW Write DQ De-skew CS1 Left Code Control Register 1

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Name	Offset	Size	Reset Value	Description
DDRPHY_SW_WR_DESKEWL_CS1_CON2	0x0918	W	0x00000000	SW Write DQ De-skew CS1 Left Code Control Register 2
DDRPHY_SW_WR_DESKEWL_CS1_CON3	0x091C	W	0x00000000	SW Write DQ De-skew CS1 Left Code Control Register 3
DDRPHY_SW_WR_DESKEWL_CS1_CON4	0x0920	W	0x00000000	SW Write DQ De-skew CS1 Left Code Control Register 4
DDRPHY_SW_WR_DESKEWL_CS1_CON5	0x0924	W	0x00000000	SW Write DQ De-skew CS1 Left Code Control Register 5
DDRPHY_SW_WR_DESKEWL_CS1_CON6	0x0928	W	0x00000000	SW Write DQ De-skew CS1 Left Code Control Register 6
DDRPHY_SW_WR_DESKEWL_CS1_CON7	0x092C	W	0x00000000	SW Write DQ De-skew CS1 Left Code Control Register 7
DDRPHY_SW_DM_DESKEWL_CS1_CON0	0x0930	W	0x00000000	SW Write DM De-skew CS1 Left Code Control Register 0
DDRPHY_DVFS0_CON5	0x0934	W	0x00000040	DVFS0 Control Register 5
DDRPHY_DVFS1_CON5	0x0938	W	0x00000040	DVFS1 Control Register 5
DDRPHY_CAL_WR_PATTERN_CON5	0x093C	W	0x00FF00FF	Write Calibration Pattern Register 5
DDRPHY_CAL_WR_PATTERN_CON6	0x0940	W	0x00FF00FF	Write Calibration Pattern Register 6
DDRPHY_CAL_WR_PATTERN_CON7	0x0944	W	0x00FF00FF	Write Calibration Pattern Register 7
DDRPHY_CAL_WR_PATTERN_CON8	0x0948	W	0x00FF00FF	Write Calibration Pattern Register 8
DDRPHY_CAL_WR_PATTERN_CON9	0x094C	W	0x00FF00FF	Write Calibration Pattern Register 9
DDRPHY_CAL_WR_PATTERN_CON10	0x0950	W	0x00FF00FF	Write Calibration Pattern Register 10
DDRPHY_CAL_WR_PATTERN_CON11	0x0954	W	0x00FF00FF	Write Calibration Pattern Register 11
DDRPHY_CAL_WR_PATTERN_CON12	0x0958	W	0x00FF00FF	Write Calibration Pattern Register 12
DDRPHY_CAL_WR_PATTERN_CON13	0x095C	W	0x00FF00FF	Write Calibration Pattern Register 13
DDRPHY_CAL_WR_PATTERN_CON14	0x0960	W	0x00FF00FF	Write Calibration Pattern Register 14
DDRPHY_CAL_WR_PATTERN_CON15	0x0964	W	0x00FF00FF	Write Calibration Pattern Register 15
DDRPHY_CAL_WR_PATTERN_CON16	0x0968	W	0x00FF00FF	Write Calibration Pattern Register 16
DDRPHY_CAL_WR_PATTERN_CON17	0x096C	W	0x00005555	Write Calibration Pattern Register 17
DDRPHY_CAL_WR_PATTERN_CON18	0x0970	W	0x00005555	Write Calibration Pattern Register 18
DDRPHY_CAL_WR_PATTERN_CON19	0x0974	W	0x00005555	Write Calibration Pattern Register 19
DDRPHY_READ_DQ_OFFSET_CTRL0	0x0978	W	0x37373737	Read DQ Offset Control Register 0 For Rank0
DDRPHY_READ_DQ_OFFSET_CTRL1	0x097C	W	0x37373737	Read DQ Offset Control Register 1 For Rank0
DDRPHY_READ_DQ_OFFSET_CTRL2	0x0980	W	0x00000037	Read DQ Offset Control Register 2 For Rank0
DDRPHY_READ_DQ_OFFSET_CTRL3	0x0984	W	0x37373737	Read DQ Offset Control Register 3 For Rank0

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Name	Offset	Size	Reset Value	Description
DDRPHY_READ_DQ_OFFSET_CTRL4	0x0988	W	0x37373737	Read DQ Offset Control Register 4 For Rank0
DDRPHY_READ_DQ_OFFSET_CTRL5	0x098C	W	0x00000037	Read DQ Offset Control Register 5 For Rank0
DDRPHY_READ_DQ_OFFSET_CTRL0_CS1	0x0990	W	0x37373737	Read DQ Offset Control Register 0 For Rank1
DDRPHY_READ_DQ_OFFSET_CTRL1_CS1	0x0994	W	0x37373737	Read DQ Offset Control Register 1 For Rank1
DDRPHY_READ_DQ_OFFSET_CTRL2_CS1	0x0998	W	0x00000037	Read DQ Offset Control Register 2 For Rank1
DDRPHY_READ_DQ_OFFSET_CTRL3_CS1	0x099C	W	0x37373737	Read DQ Offset Control Register 3 For Rank1
DDRPHY_READ_DQ_OFFSET_CTRL4_CS1	0x09A0	W	0x37373737	Read DQ Offset Control Register 4 For Rank1
DDRPHY_READ_DQ_OFFSET_CTRL5_CS1	0x09A4	W	0x00000037	Read DQ Offset Control Register 5 For Rank1
DDRPHY_WRITE_DQ_DLINE_DUTY_CTRL0	0x09A8	W	0x00000000	Write DQ Duty Control Register 0
DDRPHY_WRITE_DQ_DLINE_DUTY_CTRL1	0x09AC	W	0x00000000	Write DQ Duty Control Register 1
DDRPHY_READ_DQ_DLINE_DUTY_CTRL0	0x09B0	W	0x00000000	Read DQ Duty Control Register 0
DDRPHY_READ_DQ_DLINE_DUTY_CTRL1	0x09B4	W	0x00000000	Read DQ Duty Control Register 1
DDRPHY_READ_DQ_DLINE_DUTY_CTRL2	0x09B8	W	0x00000000	Read DQ Duty Control Register 2
DDRPHY_READ_DQ_DLINE_DUTY_CTRL3	0x09BC	W	0x00000000	Read DQ Duty Control Register 3
DDRPHY_WRITE_DQS_DLINE_DUTY_CTRL0	0x09C0	W	0x00000000	Write DQS Duty Control Register 0
DDRPHY_DQ_SEL_CTRL0	0x09C4	W	0x02492492	DQ DLL Select Control Register 0
DDRPHY_DQ_SEL_CTRL1	0x09C8	W	0x02492492	DQ DLL Select Control Register 1
DDRPHY_DQ_SEL_CTRL2	0x09CC	W	0x02492492	DQ DLL Select Control Register 2
DDRPHY_DQ_SEL_CTRL3	0x09D0	W	0x02492492	DQ DLL Select Control Register 3
DDRPHY_DQ_SEL_CTRL4	0x09D4	W	0x02492492	DQ DLL Select Control Register 4
DDRPHY_DQ_SEL_CTRL5	0x09D8	W	0x02492492	DQ DLL Select Control Register 5
DDRPHY_DQ_SEL_CTRL6	0x09DC	W	0x02492492	DQ DLL Select Control Register 6
DDRPHY_DQ_SEL_CTRL7	0x09E0	W	0x02492492	DQ DLL Select Control Register 7
DDRPHY_CK_DLINE_DUTY_CTRL0	0x09E4	W	0x00000000	CK Duty Control Register 0
DDRPHY_IO_DUTY_CTRL0	0x09E8	W	0x2DB6DB6D	IO Duty Control Register 0
DDRPHY_IO_DUTY_CTRL1	0x09EC	W	0x2DB6DB6D	IO Duty Control Register 1
DDRPHY_IO_DUTY_CTRL2	0x09F0	W	0x1B6DB6DB	IO Duty Control Register 2
DDRPHY_IO_DUTY_CTRL3	0x09F4	W	0x1B6DB6DB	IO Duty Control Register 3
DDRPHY_IO_DUTY_CTRL4	0x09F8	W	0x00000000	IO Duty Control Register 4
DDRPHY_IO_DUTY_CTRL5	0x09FC	W	0x0000001D	IO Duty Control Register 5
DDRPHY_DVFS0_CON6	0x0A00	W	0x003F0000	DVFS0 Control Register 6
DDRPHY_DVFS1_CON6	0x0A04	W	0x003F0000	DVFS1 Control Register 6

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Name	Offset	Size	Reset Value	Description
DDRPHY_DQOENDESKEWCODE0	0x0A08	W	0x00000000	DQ Output Enable De-skew Code Register 0
DDRPHY_DQOENDESKEWCODE1	0x0A0C	W	0x00000000	DQ Output Enable De-skew Code Register 1
DDRPHY_DQSOENDESKEWCODE	0x0A10	W	0x00000000	DQS Output Enable De-skew Code Register
DDRPHY_DTB	0x0A14	W	0x00000000	DTB Control Register
DDRPHY_GTCC_CON0	0x0A18	W	0x00000000	Gate Center Control Register 0
DDRPHY_RANK1_CON0	0x0A1C	W	0x00020820	Rank1 RL Control Register 0
DDRPHY_SCHD_CON0	0x0A20	W	0x00000040	Scheduler Control Register 0
DDRPHY_SCHD_TRAIN_CON0	0x0A24	W	0x00000000	Scheduler Training Control Register 0
DDRPHY_SCHD_TRAIN_CON1	0x0A28	W	0x000403F5	Scheduler Training Control Register 1
DDRPHY_SCHD_TIME_CON0	0x0A2C	W	0x005A01D2	Scheduler CMD Timing Control Register 0
DDRPHY_SCHD_TIME_CON1	0x0A30	W	0x640D1008	Scheduler CMD Timing Control Register 1
DDRPHY_SCHD_TIME_CON2	0x0A34	W	0x03C74780	Scheduler CMD Timing Control Register 2
DDRPHY_SCHD_TIME_CON3	0x0A38	W	0x00000080	Scheduler CMD Timing Control Register 3
DDRPHY_DVFS0_SCHD_TIME_CON0	0x0A3C	W	0x005A01D2	DVFS0 Scheduler CMD Timing Control Register 0
DDRPHY_DVFS0_SCHD_TIME_CON1	0x0A40	W	0x640D1008	DVFS0 Scheduler CMD Timing Control Register 1
DDRPHY_DVFS0_SCHD_TIME_CON2	0x0A44	W	0x03C74780	DVFS0 Scheduler CMD Timing Control Register 2
DDRPHY_DVFS0_SCHD_TIME_CON3	0x0A48	W	0x04000001	DVFS0 Scheduler CMD Timing Control Register 3
DDRPHY_DVFS1_SCHD_TIME_CON0	0x0A4C	W	0x005A01D2	DVFS1 Scheduler CMD Timing Control Register 0
DDRPHY_DVFS1_SCHD_TIME_CON1	0x0A50	W	0x640D1008	DVFS1 Scheduler CMD Timing Control Register 1
DDRPHY_DVFS1_SCHD_TIME_CON2	0x0A54	W	0x03C74780	DVFS1 Scheduler CMD Timing Control Register 2
DDRPHY_DVFS1_SCHD_TIME_CON3	0x0A58	W	0x04000001	DVFS1 Scheduler CMD Timing Control Register 3
DDRPHY_SCHD_DIRECT_CMD0	0x0A5C	W	0x00000000	Scheduler Direct CMD Register 0
DDRPHY_SCHD_DIRECT_CMD1	0x0A60	W	0x00000000	Scheduler Direct CMD Register 1
DDRPHY_SCHD_DIRECT_CMD2	0x0A64	W	0x00000000	Scheduler Direct CMD Register 2
DDRPHY_SCHD_DIRECT_CMD3	0x0A68	W	0x00000000	Scheduler Direct CMD Register 3
DDRPHY_SCHD_DIRECT_CMD4	0x0A6C	W	0x00000000	Scheduler Direct CMD Register 4
DDRPHY_SCHD_CMD_CON0	0x0A70	W	0x00000001	Scheduler CMD Control Register 0
DDRPHY_SCHD_CMD_CON1	0x0A74	W	0x00000000	Scheduler CMD Control Register 1
DDRPHY_SCHD_CMD_CON2	0x0A78	W	0x00000000	Scheduler CMD Control Register 2

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Name	Offset	Size	Reset Value	Description
DDRPHY_OP_CODE_RDC	0x0A7C	W	0x5555EEEE	OP Code Register
DDRPHY_LP4_MR_OP0	0x0A80	W	0x00000000	LPDDR4 MR Operand 0
DDRPHY_LP4_MR_OP1	0x0A84	W	0x00000000	LPDDR4 MR Operand 1
DDRPHY_LP5_MR_OP0	0x0A88	W	0x00000000	LPDDR5 MR Operand 0
DDRPHY_LP5_MR_OP1	0x0A8C	W	0x00000000	LPDDR5 MR Operand 1
DDRPHY_SCHD_FSM	0x0A90	W	0x00000000	Scheduler FSM Monitor
DDRPHY_CLKMODE_CON	0x0A94	W	0x00000009	PHY Clock Mode Control Register
DDRPHY_CASWIZZLE_CON	0x0A98	W	0x65432100	CA Swizzle Control Register
DDRPHY_TDLL_CON0	0x0A9C	W	0x00000000	TDLL Control Register 0
DDRPHY_TDLL_CON1	0x0AA0	W	0x00000000	TDLL Control Register 1
DDRPHY_TDLL_MON0_DS0	0x0AA4	W	0x00000000	TDLL Monitor Register 0 For Data Slice 0
DDRPHY_TDLL_MON1_DS0	0x0AA8	W	0x00000000	TDLL Monitor Register 1 For Data Slice 0
DDRPHY_TDLL_MON0_DS1	0x0AAC	W	0x00000000	TDLL Monitor Register 0 For Data Slice 1
DDRPHY_TDLL_MON1_DS1	0x0AB0	W	0x00000000	TDLL Monitor Register 1 For Data Slice 1
DDRPHY_DQRPARITY_LEFT_DS0	0x0AB4	W	0x00000000	DQ Rising Parity Left For Data Slice 0
DDRPHY_DQRPARITY_RIGHT_DS0	0x0AB8	W	0x00000000	DQ Rising Parity Right For Data Slice 0
DDRPHY_DQFPARITY_LEFT_DS0	0x0ABC	W	0x00000000	DQ Falling Parity Left For Data Slice 0
DDRPHY_DQFPARITY_RIGHT_DS0	0x0AC0	W	0x00000000	DQ Falling Parity Right For Data Slice 0
DDRPHY_DQRPARITY_LEFT_DS1	0x0AC4	W	0x00000000	DQ Rising Parity Left For Data Slice 1
DDRPHY_DQRPARITY_RIGHT_DS1	0x0AC8	W	0x00000000	DQ Rising Parity Right For Data Slice 1
DDRPHY_DQFPARITY_LEFT_DS1	0x0ACC	W	0x00000000	DQ Falling Parity Left For Data Slice 1
DDRPHY_DQFPARITY_RIGHT_DS1	0x0AD0	W	0x00000000	DQ Falling Parity Right For Data Slice 1
DDRPHY_READCAL_URG_DS0	0x0AD4	W	0x00000000	Read Calibration URG Data Slice 0
DDRPHY_READCAL_URG_DS1	0x0AD8	W	0x00000000	Read Calibration URG Data Slice 1
DDRPHY_WCK2CKSYNC_CON0	0x0ADC	W	0x00000000	WCK2CK SYNC CON0
DDRPHY_WCK2CKSYNC_CON1	0x0AE0	W	0x23340758	WCK2CK SYNC CON1
DDRPHY_DVFS0_WCK2CKSYNC_CON1	0x0AE4	W	0x23340758	DVFS0 WCK2CK SYNC CON1
DDRPHY_DVFS1_WCK2CKSYNC_CON1	0x0AE8	W	0x23340758	DVFS1 WCK2CK SYNC CON1
DDRPHY_SCHD_CMD_GATING0	0x0AEC	W	0x00000000	Scheduler Direct CMD Gating 0
DDRPHY_SCHD_CMD_GATING1	0x0AF0	W	0x00000000	Scheduler Direct CMD Gating 1
DDRPHY_DVFS0_WCK2CKSYNC_CON0	0x0AF4	W	0x00000000	DVFS0 WCK2CK SYNC CON0

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Name	Offset	Size	Reset Value	Description
DDRPHY_DVFS1_WCK2CK_SYNC_CON0	0x0AF8	W	0x00000000	DVFS1 WCK2CK SYNC CON0
DDRPHY_MDLL_CON2	0x0AFC	W	0x00000001	Master DLL Control Register 2
DDRPHY_TESTILP5_DQ0	0x0B00	W	0x000199E0	TEST Input Port For LP4/5 DQ0
DDRPHY_TESTILP5_DQ1	0x0B04	W	0x000199E0	TEST Input Port For LP4/5 DQ1
DDRPHY_TESTILP5_DQ2	0x0B08	W	0x000199E0	TEST Input Port For LP4/5 DQ2
DDRPHY_TESTILP5_DQ3	0x0B0C	W	0x000199E0	TEST Input Port For LP4/5 DQ3
DDRPHY_TESTILP5_DQ4	0x0B10	W	0x000199E0	TEST Input Port For LP4/5 DQ4
DDRPHY_TESTILP5_DQ5	0x0B14	W	0x000199E0	TEST Input Port For LP4/5 DQ5
DDRPHY_TESTILP5_DQ6	0x0B18	W	0x000199E0	TEST Input Port For LP4/5 DQ6
DDRPHY_TESTILP5_DQ7	0x0B1C	W	0x000199E0	TEST Input Port For LP4/5 DQ7
DDRPHY_TESTILP5_DQ8	0x0B20	W	0x000199E0	TEST Input Port For LP4/5 DQ8
DDRPHY_TESTILP5_DQ9	0x0B24	W	0x000199E0	TEST Input Port For LP4/5 DQ9
DDRPHY_TESTILP5_DQ10	0x0B28	W	0x000199E0	TEST Input Port For LP4/5 DQ10
DDRPHY_TESTILP5_DQ11	0x0B2C	W	0x000199E0	TEST Input Port For LP4/5 DQ11
DDRPHY_TESTILP5_DQ12	0x0B30	W	0x000199E0	TEST Input Port For LP4/5 DQ12
DDRPHY_TESTILP5_DQ13	0x0B34	W	0x000199E0	TEST Input Port For LP4/5 DQ13
DDRPHY_TESTILP5_DQ14	0x0B38	W	0x000199E0	TEST Input Port For LP4/5 DQ14
DDRPHY_TESTILP5_DQ15	0x0B3C	W	0x000199E0	TEST Input Port For LP4/5 DQ15
DDRPHY_TESTILP5_DM0	0x0B40	W	0x000199E0	TEST Input Port For LP4/5 DM0
DDRPHY_TESTILP5_DM1	0x0B44	W	0x000199E0	TEST Input Port For LP4/5 DM1
DDRPHY_TESTILP5_DQS0	0x0B48	W	0x000199E0	TEST Input Port For LP4/5 DQS0
DDRPHY_TESTILP5_DQS1	0x0B4C	W	0x000199E0	TEST Input Port For LP4/5 DQS1
DDRPHY_TESTILP5_CK	0x0B50	W	0x000199E0	TEST Input Port For LP4/5 CK
DDRPHY_TESTILP5_CA0	0x0B54	W	0x000199E0	TEST Input Port For LP4/5 CA0
DDRPHY_TESTILP5_CA1	0x0B58	W	0x000199E0	TEST Input Port For LP4/5 CA1
DDRPHY_TESTILP5_CA2	0x0B5C	W	0x000199E0	TEST Input Port For LP4/5 CA2
DDRPHY_TESTILP5_CA3	0x0B60	W	0x000199E0	TEST Input Port For LP4/5 CA3
DDRPHY_TESTILP5_CA4	0x0B64	W	0x000199E0	TEST Input Port For LP4/5 CA4
DDRPHY_TESTILP5_CA5	0x0B68	W	0x000199E0	TEST Input Port For LP4/5 CA5
DDRPHY_TESTILP5_CA6	0x0B6C	W	0x000199E0	TEST Input Port For LP5 CA6
DDRPHY_TESTILP5_CS0	0x0B70	W	0x000199E0	TEST Input Port For LP4/5 CS0
DDRPHY_TESTILP5_CS1	0x0B74	W	0x000199E0	TEST Input Port For LP4/5 CS1
DDRPHY_TESTILP5_WCK0	0x0B78	W	0x000199E0	TEST Input Port For LP5 WCK0
DDRPHY_TESTILP5_WCK1	0x0B7C	W	0x000199E0	TEST Input Port For LP5 WCK1
DDRPHY_DQSDUTY_CON0	0x0B80	W	0x00000000	DQS Duty Control Register 0
DDRPHY_DQSDUTY_CON1	0x0B84	W	0x00000000	DQS Duty Control Register 1
DDRPHY_DQSDUTY_CON2	0x0B88	W	0x00000000	DQS Duty Control Register 2
DDRPHY_DQSDUTY_CON3	0x0B8C	W	0x00000000	DQS Duty Control Register 3
DDRPHY_DQSDUTY_CON4	0x0B90	W	0x00000000	DQS Duty Control Register 4
DDRPHY_DQSDUTY_CON5	0x0B94	W	0x00000000	DQS Duty Control Register 5
DDRPHY_DQSDUTY_CON6	0x0B98	W	0x00000000	DQS Duty Control Register 6
DDRPHY_DQSDUTY_CON7	0x0B9C	W	0x00000000	DQS Duty Control Register 7
DDRPHY_MON_RCNT0	0x0BA0	W	0x00000000	Monitor RSTN 0
DDRPHY_MON_RCNT1	0x0BA4	W	0x00000000	Monitor RSTN 1
DDRPHY_MON_RCNT2	0x0BA8	W	0x00000000	Monitor RSTN 2
DDRPHY_MON_RCNT3	0x0BAC	W	0x00000000	Monitor RSTN 3
DDRPHY_CMD_DESKEWC_CODE0	0x0BB0	W	0x00000000	CMD De-skew Center Code Register 0
DDRPHY_CMD_DESKEWC_CODE1	0x0BB4	W	0x00000000	CMD De-skew Center Code Register 1

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Name	Offset	Size	Reset Value	Description
DDRPHY_CMD_DESKEWC_CODE2	0x0BB8	W	0x00000000	CMD De-skew Center Code Register 2
DDRPHY_CMD_DESKEWC_CODE3	0x0BBC	W	0x00000000	CMD De-skew Center Code Register 3
DDRPHY_CMD_DESKEWC_CODE4	0x0BC0	W	0x00000000	CMD De-skew Center Code Register 4
DDRPHY_CBT_CAL_STAT0	0x0BC4	W	0x00000000	CBT Calibration Status Register
DDRPHY_CMD_LEFT_CODE0	0x0BC8	W	0x00000000	CMD Left Code Register 0
DDRPHY_CMD_LEFT_CODE1	0x0BCC	W	0x00000000	CMD Left Code Register 1
DDRPHY_CMD_LEFT_CODE2	0x0BD0	W	0x00000000	CMD Left Code Register 2
DDRPHY_CMD_LEFT_CODE4	0x0BD8	W	0x00000000	CMD Left Code Register 4
DDRPHY_CMD_RIGHT_CODE0	0x0BDC	W	0x00000000	CMD Right Code Register 0
DDRPHY_CMD_RIGHT_CODE1	0x0BE0	W	0x00000000	CMD Right Code Register 1
DDRPHY_CMD_RIGHT_CODE2	0x0BE4	W	0x00000000	CMD Right Code Register 2
DDRPHY_CMD_RIGHT_CODE4	0x0BEC	W	0x00000000	CMD Right Code Register 4
DDRPHY_DVFS0_CLKMODE_CON	0x0BF0	W	0x00000009	PHY Clock Mode Control Register For DVFS0
DDRPHY_DVFS1_CLKMODE_CON	0x0BF4	W	0x00000009	PHY Clock Mode Control Register For DVFS1
DDRPHY_DVFS0_DCC_CON0	0x0BF8	W	0x00000000	DVFS0 DCC Control Register 0
DDRPHY_DVFS1_DCC_CON0	0x0BFC	W	0x00000000	DVFS1 DCC Control Register 0
DDRPHY_PTC_CON0	0x0C00	W	0x26770000	PTC Configure Register 0
DDRPHY_PTC_CON1	0x0C04	W	0x00000011	PTC Configure Register 1
DDRPHY_PTC_CON2	0x0C08	W	0x10008080	PTC Configure Register 2
DDRPHY_PTC_CON3	0x0C0C	W	0x00000000	PTC Configure Register 3
DDRPHY_PTC_CON4	0x0C10	W	0x00000000	PTC Configure Register 4
DDRPHY_PTC_CON5	0x0C14	W	0x00000000	PTC Configure Register 5
DDRPHY_PTC_CON6	0x0C18	W	0x02021100	PTC Configure Register 6
DDRPHY_PTC_CON7	0x0C1C	W	0x00FF00FF	PTC Configure Register 7
DDRPHY_PTC_CON8	0x0C20	W	0x00FF00FF	PTC Configure Register 8
DDRPHY_PTC_CON9	0x0C24	W	0x00FF00FF	PTC Configure Register 9
DDRPHY_PTC_CON10	0x0C28	W	0x00FF00FF	PTC Configure Register 10
DDRPHY_PTC_CON11	0x0C2C	W	0x80000000	PTC Configure Register 11
DDRPHY_PTC_CON12	0x0C30	W	0x00000000	PTC Configure Register 12
DDRPHY_PTC_CON13	0x0C34	W	0x00000000	PTC Configure Register 13
DDRPHY_PTC_CON14	0x0C38	W	0x00000000	PTC Configure Register 14
DDRPHY_PTC_CON15	0x0C3C	W	0x00000000	PTC Configure Register 15
DDRPHY_PTC_CON16	0x0C40	W	0x00000000	PTC Configure Register 16
DDRPHY_PTC_CON20	0x0C50	W	0x00000000	PTC Configure Register 20
DDRPHY_PTC_CON21	0x0C54	W	0x00000000	PTC Configure Register 21
DDRPHY_PTC_CON22	0x0C58	W	0x00000000	PTC Configure Register 22
DDRPHY_Periodic_ZQ_CON	0x0C70	W	0x000403F5	Periodic ZQ Control Register

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Name	Offset	Size	Reset Value	Description
DDRPHY_PRBS_LEFT_MARGIN_DQ0	0x0D00	W	0x00000000	PRBS Left Margin For DQ0
DDRPHY_PRBS_RIGHT_MARGIN_DQ0	0x0D04	W	0x00000000	PRBS Right Margin For DQ0
DDRPHY_PRBS_LEFT_MARGIN_DQ1	0x0D08	W	0x00000000	PRBS Left Margin For DQ1
DDRPHY_PRBS_RIGHT_MARGIN_DQ1	0x0D0C	W	0x00000000	PRBS Right Margin For DQ1
DDRPHY_PRBS_LEFT_MARGIN_DQ2	0x0D10	W	0x00000000	PRBS Left Margin For DQ2
DDRPHY_PRBS_RIGHT_MARGIN_DQ2	0x0D14	W	0x00000000	PRBS Right Margin For DQ2
DDRPHY_PRBS_LEFT_MARGIN_DQ3	0x0D18	W	0x00000000	PRBS Left Margin For DQ3
DDRPHY_PRBS_RIGHT_MARGIN_DQ3	0x0D1C	W	0x00000000	PRBS Right Margin For DQ3
DDRPHY_PRBS_LEFT_MARGIN_DQ4	0x0D20	W	0x00000000	PRBS Left Margin For DQ4
DDRPHY_PRBS_RIGHT_MARGIN_DQ4	0x0D24	W	0x00000000	PRBS Right Margin For DQ4
DDRPHY_PRBS_LEFT_MARGIN_DQ5	0x0D28	W	0x00000000	PRBS Left Margin For DQ5
DDRPHY_PRBS_RIGHT_MARGIN_DQ5	0x0D2C	W	0x00000000	PRBS Right Margin For DQ5
DDRPHY_PRBS_LEFT_MARGIN_DQ6	0x0D30	W	0x00000000	PRBS Left Margin For DQ6
DDRPHY_PRBS_RIGHT_MARGIN_DQ6	0x0D34	W	0x00000000	PRBS Right Margin For DQ6
DDRPHY_PRBS_LEFT_MARGIN_DQ7	0x0D38	W	0x00000000	PRBS Left Margin For DQ7
DDRPHY_PRBS_RIGHT_MARGIN_DQ7	0x0D3C	W	0x00000000	PRBS Right Margin For DQ7
DDRPHY_PRBS_LEFT_MARGIN_DQ8	0x0D40	W	0x00000000	PRBS Left Margin For DQ8
DDRPHY_PRBS_RIGHT_MARGIN_DQ8	0x0D44	W	0x00000000	PRBS Right Margin For DQ8
DDRPHY_PRBS_LEFT_MARGIN_DQ9	0x0D48	W	0x00000000	PRBS Left Margin For DQ9
DDRPHY_PRBS_RIGHT_MARGIN_DQ9	0x0D4C	W	0x00000000	PRBS Right Margin For DQ9
DDRPHY_PRBS_LEFT_MARGIN_DQ10	0x0D50	W	0x00000000	PRBS Left Margin For DQ10
DDRPHY_PRBS_RIGHT_MARGIN_DQ10	0x0D54	W	0x00000000	PRBS Right Margin For DQ10
DDRPHY_PRBS_LEFT_MARGIN_DQ11	0x0D58	W	0x00000000	PRBS Left Margin For DQ11
DDRPHY_PRBS_RIGHT_MARGIN_DQ11	0x0D5C	W	0x00000000	PRBS Right Margin For DQ11
DDRPHY_PRBS_LEFT_MARGIN_DQ12	0x0D60	W	0x00000000	PRBS Left Margin For DQ12
DDRPHY_PRBS_RIGHT_MARGIN_DQ12	0x0D64	W	0x00000000	PRBS Right Margin For DQ12
DDRPHY_PRBS_LEFT_MARGIN_DQ13	0x0D68	W	0x00000000	PRBS Left Margin For DQ13

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Name	Offset	Size	Reset Value	Description
DDRPHY_PRBS_RIGHT_MARGIN_DQ13	0x0D6C	W	0x00000000	PRBS Right Margin For DQ13
DDRPHY_PRBS_LEFT_MARGIN_DQ14	0x0D70	W	0x00000000	PRBS Left Margin For DQ14
DDRPHY_PRBS_RIGHT_MARGIN_DQ14	0x0D74	W	0x00000000	PRBS Right Margin For DQ14
DDRPHY_PRBS_LEFT_MARGIN_DQ15	0x0D78	W	0x00000000	PRBS Left Margin For DQ15
DDRPHY_PRBS_RIGHT_MARGIN_DQ15	0x0D7C	W	0x00000000	PRBS Right Margin For DQ15
DDRPHY_PRBS_LEFT_MARGIN_DM0	0x0D80	W	0x00000000	PRBS Left Margin For DM0
DDRPHY_PRBS_RIGHT_MARGIN_DM0	0x0D84	W	0x00000000	PRBS Right Margin For DM0
DDRPHY_PRBS_LEFT_MARGIN_DM1	0x0D88	W	0x00000000	PRBS Left Margin For DM1
DDRPHY_PRBS_RIGHT_MARGIN_DM1	0x0D8C	W	0x00000000	PRBS Right Margin For DM1
DDRPHY_WR_BYTE0_CYC_CS0_CODE	0x0DC0	W	0x00000000	Write CS0 Byte0 Cycle Code
DDRPHY_WR_BYTE1_CYC_CS0_CODE	0x0DC4	W	0x00000000	Write CS0 Byte1 Cycle Code
DDRPHY_WR_BYTE0_CYC_CS1_CODE	0x0DC8	W	0x00000000	Write CS1 Byte0 Cycle Code
DDRPHY_WR_BYTE1_CYC_CS1_CODE	0x0DCC	W	0x00000000	Write CS1 Byte1 Cycle Code
DDRPHY_SW_WR_BYTE0_CYC_CS0_CODE	0x0DD0	W	0x00000000	SW Write CS0 Byte0 Cycle Code
DDRPHY_SW_WR_BYTE1_CYC_CS0_CODE	0x0DD4	W	0x00000000	SW Write CS0 Byte1 Cycle Code
DDRPHY_SW_WR_BYTE0_CYC_CS1_CODE	0x0DD8	W	0x00000000	SW Write CS1 Byte0 Cycle Code
DDRPHY_SW_WR_BYTE1_CYC_CS1_CODE	0x0DDC	W	0x00000000	SW Write CS1 Byte1 Cycle Code
DDRPHY_WCKOSC_CON0	0x0DE0	W	0x04373F00	WCK Oscillator Control Register 0
DDRPHY_WCKOSC_CON1	0x0DE4	W	0x00000182	WCK Oscillator Control Register 1
DDRPHY_WCKOSC_CON2	0x0DE8	W	0x00010001	WCK Oscillator Control Register 2
DDRPHY_WCKOSC_CON3	0x0DEC	W	0x80000000	WCK Oscillator Control Register 3
DDRPHY_DVFS0_WCKOSC_CON0	0x0DF0	W	0x04373F00	DVFS0 WCK Oscillator Control Register 0
DDRPHY_DVFS1_WCKOSC_CON0	0x0DF4	W	0x04373F00	DVFS1 WCK Oscillator Control Register 0
DDRPHY_WRTRN_PARA_CON0	0x0DF8	W	0x01200316	Write Training Parameter Configure Register 0
DDRPHY_DVFS0_WRTRN_PARA_CON0	0x0DFC	W	0x01200316	DVFS0 Write Training Parameter Configure Register 0
DDRPHY_DVFS1_WRTRN_PARA_CON0	0x0E00	W	0x01200316	DVFS1 Write Training Parameter Configure Register 0
DDRPHY_DFI_LP_CON0	0x0E04	W	0x00002322	DFI Low Power Control Register 0
DDRPHY_LOCK_CHECK_CON	0x0E08	W	0x00007104	Lock Check Control Register
DDRPHY_DFI_RDDATA0	0x0E10	W	0x00000000	DFI Read Data Burst 0
DDRPHY_DFI_RDDATA1	0x0E14	W	0x00000000	DFI Read Data Burst 1
DDRPHY_DFI_RDDATA2	0x0E18	W	0x00000000	DFI Read Data Burst 2

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Name	Offset	Size	Reset Value	Description
DDRPHY_DFI_RDDATA3	0x0E1C	W	0x00000000	DFI Read Data Burst 3
DDRPHY_DFI_RDDATA4	0x0E20	W	0x00000000	DFI Read Data Burst 4
DDRPHY_DFI_RDDATA5	0x0E24	W	0x00000000	DFI Read Data Burst 5
DDRPHY_DFI_RDDATA6	0x0E28	W	0x00000000	DFI Read Data Burst 6
DDRPHY_DFI_RDDATA7	0x0E2C	W	0x00000000	DFI Read Data Burst 7
DDRPHY_DFI_RDDATA_DM	0x0E30	W	0x00000000	DFI Read DM Burst
DDRPHY_LP5_MR_OP2	0x0E34	W	0xC6BBC6BB	LPDDR5 MR Operand Register 2
DDRPHY_DVFS0_LP5_MR_OP2	0x0E38	W	0xC6BBC6BB	DVFS0 LPDDR5 MR Operand Register 2
DDRPHY_DVFS1_LP5_MR_OP2	0x0E3C	W	0xC6BBC6BB	DVFS1 LPDDR5 MR Operand Register 2
DDRPHY_PHYUPD_PARA_CON0	0x0E40	W	0x0000103F	PHY Update Parameter Configure Register 0
DDRPHY_DVFS0_PHYUPD_PARA_CON0	0x0E44	W	0x0000103F	PHY Update Parameter Configure Register 0 For DVFS0
DDRPHY_DVFS1_PHYUPD_PARA_CON0	0x0E48	W	0x0000103F	PHY Update Parameter Configure Register 0 For DVFS1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access*

7.4.6 Detail Registers Description For DDRPHY

DDRPHY_GNR_CON0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RW	0x1	ctrl_upd_time It controls when DLL is updated. Clock period information from master DLL will be updated to slave DLLs by DLL update. 2'b00: Update always 2'b01: To update depending on "ctrl_flock" 2'b10: To update periodically with interval defined by ctrl_upd_interval 2'b11: Don't update DLL
29:28	RW	0x0	ctrl_upd_range It decides how many differences between the new lock value and the current lock value which is used in slave DLL is needed for updating lock value. upd_range_ext = 2'b00 (default) 2'b00: Update when difference is greater than 0 tFS. 2'b01: Update when difference is greater than 3 tFS. 2'b10: Update when difference is greater than 7 tFS. 2'b11: Update when difference is greater than 15 tFS. upd_range_ext = 2'b01 2'b00: Update when difference is greater than 5 tFS. 2'b01: Update when difference is greater than 9 tFS. 2'b10: Update when difference is greater than 11 tFS. 2'b11: Update when difference is greater than 13 tFS. upd_range_ext = 2'b10 2'b00: Update when difference is greater than 17 tFS. 2'b01: Update when difference is greater than 19 tFS. 2'b10: Update when difference is greater than 21 tFS. 2'b11: Update when difference is greater than 23 tFS. upd_range_ext = 2'b11 2'b00: Update when difference is greater than 25 tFS. 2'b01: Update when difference is greater than 27 tFS.

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Bit	Attr	Reset Value	Description
			2'b10: Update when difference is greater than 29 tFS. 2'b11: Update when difference is greater than 31 tFS.
27	RW	0x0	ctrl_twpst Write postamble length control. Vendor specific option 1'b0: 0.5tCK 1'b1: 1.5tCK
26	RW	0x1	ctrl_dfdqs DQS I/O Receiver mode setting 1'b0: Single-ended DQS (io_dqs_se = 2'b11) 1'b1: Differential DQS (io_dqs_se =2'b00)
25:24	RW	0x0	ctrl_ddr_mode 2'b00: LPDDR4 2'b10: LPDDR5 Others: Reserved
23:21	RW	0x0	ctrl_fnc_fb FNC Feedback mode setting 3'b000: FNC Feedback disable 3'b010: External FNC Feedback mode 3'b011: Internal FNC Feedback mode Others: Reserved
20	RW	0x0	dvfs_gate_upd_mode Gate information update mode for DVFS pause. 1'b0: Gate delay information will be restored to the initial training result whenever DVFS pause occurs. 1'b1: Gate delay information will not be restore to the initial training result if DVFS pause occurs without changing dvfs_mode and clock frequency in order to make DLL relock.
19	RW	0x0	wdqs_oen_mode Write DQS drive state control mode. 1'b0: DQS will be driven except for the read duration. ds_io_pd should be set to 1. 1'b1: DQS will be driven only for write duration.
18	RW	0x0	write_se_dqs Single ended mode enable for write DQS. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for Write DQS. 1'b1: Single ended mode is enabled for Write DQS. Caution: write_se_ck should be enabled using write_se_dqs in LPDDR4.
17	RW	0x0	write_se_ck Single ended mode enable for CK. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for CK. 1'b1: Single ended mode is enabled for CK. Caution: write_se_dqs should be enabled using write_se_ck in LPDDR4. Caution: write_se_wck should be enabled using write_se_ck in LPDDR5.
16	RW	0x0	ctrl_pd_width PD (io_dqs_pd, io_dq_pd, io_dm_pd) signal width control. 1'b0: Same width with READ (io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read) 1'b1: Longer than READ

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Bit	Attr	Reset Value	Description
15	RW	0x0	ctrl_twpre Write preamble length control. Refer to DRAM spec for write preamble definition. 1'b0: 2 tCK for higher speeds 1'b1: 1 tCK for lower speeds
14	RW	0x1	ctrl_otf_bl On-the-fly BL enable 1'b0: On-the-fly BL is disabled. 1'b1: On-the-fly BL is enabled.
13:8	RW	0x10	ctrl_bstlen Fixed Burst Length (BL). This field is ignored when ctrl_otf_bl is 1'b1. 6'h10: BL = 16 6'h20: BL = 32 Others: Reserved
7	RW	0x0	ctrl_ckdis Deprecated.
6	RW	0x0	ctrl_cmosrcv This field controls the input mode of I/O. 1'b0: Differential receiver mode for high speed operation (io_dqs_cmosrcv = 2'b0, io_dm_cmosrcv = 2'b0, io_dq_cmosrcv = 16'h0000) 1'b1: CMOS receiver mode for low speed operation (under 400MHz) (io_dqs_cmosrcv = 2'b11, io_dm_cmosrcv = 2'b11, io_dq_cmosrcv = 16'hffff)
5:0	RW	0x11	ctrl_rdlat_rank0 Read latency (RL) for rank0

DDRPHY_CAL_CON0

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RW	0x1	cs_default Default dfi_wrdata_cs setting. This field will set the default value for internally generated dfi_wrdata_cs, which will be used when wr_per_rank_en is disabled.
29	RW	0x1	wr_per_rank_en Per-rank write DQ/DM DLL control enable. If this field is enabled, write training should be done for both rank0 and rank1 and dfi_wrdata_cs should be properly controlled by the memory controller. If this field is disabled, dfi_wrdata_cs will be controlled internally by PHY, and it will be fixed to the default chip select, which is specified in cs_default. 1'b1: Write DQ DLL code will be controlled per rank. 1'b0: Write DQ DLL code will be fixed for rank-to-rank write.
28	RW	0x1	rd_per_rank_en Per-rank read DQS/DQ/DM DLL control enable. If this field is enabled, Read training should be done for both rank0 and rank1. 1'b1: Read DQS/DQ/DM DLL code will be controlled per rank. 1'b0: Read DQS/DQ/DM DLL code will be fixed for rank-to-rank read.

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Bit	Attr	Reset Value	Description
27	RW	0x1	gate_rdchk_en Gate training read check enable control signal. If this is enabled, PHY will check if the read data from DRAM caused by MPC-RD DQ Calibration from the memory controller is correct or not while finding the read DQS location during gate training. 1'b1: Read check is enabled during gate training. 1'b0: Read check is disabled during gate training.
26	RW	0x0	dvfs_wr_train_en DVFS Write training enable. If enabled, write training initiation with dfi_lvl_periodic=0 will be interpreted as DVFS write training. During the initial training, dvfs_wr_train_en should be 0. 1'b1: DVFS write training enabled. Training logic will find tDQS2DQ variation. The start point is determined by dvfs_wr_start_adj. Training will finish when the valid data widow edge is found. 1'b0: DVFS write training disabled.
25:24	RW	0x0	avg_window_size Average window size for DLL lock value average. 2'b00: Lock value will be sampled 32 times and averaged (Default). 2'b01: Lock value will be sampled 16 times and averaged. 2'b10: Lock value will be sampled 8 times and averaged. 2'b11: Lock value will be sampled 64 times and averaged.
23	RW	0x1	freq_offset_en Frequency offset calculation enable. When enabled, PHY calculates the required offset based on the frequency information to get more margins at the lower frequencies. It should be set to 1'b0 if DLL is off because the frequency compensation offset will be calculated using the current DLL lock value. Frequency offset will be applied to write DQ/DM and read DQS. 1'b1: Enable frequency offset calculation. 1'b0: Disable frequency offset calculation.
22	RW	0x0	cal_vtc_en VT compensation enable. DLL delay is updated depending on the latest master DLL lock value whenever "dfi_ctrlupd_req" or "dfi_phyupd_req" is issued if cal_vtc_en=1. It compensates On-chip VT variation. 1'b1: VT compensation enabled. 1'b0: VT compensation disabled.
21	RW	0x0	ca_swap_mode_dis CA swap disable for LPDDR4 HW CAL CBT mode
20	RW	0x1	wck_vtc_en VT compensation enable for WCK. DLL delay is updated depending on the latest master DLL lock value whenever "dfi_ctrlupd_req" or "dfi_phyupd_req" is issued if wck_vtc_en=1. It compensates On-chip VT variation. 1'b1: VT compensation enabled. 1'b0: VT compensation disabled. cal_vtc_en should be 1 for use wck_vtc_en = 1.
19	RO	0x0	reserved
18	RW	0x1	rdtrn_dbi_cal_en DBI enable for LPDDR4/5 read training. 1'b0: DBI is not calibrated during read training. 1'b1: DBI is calibrated during read training.

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Bit	Attr	Reset Value	Description
17	RW	0x1	wrtrn_dbi_cal_en DBI enable for LPDDR4/5 write training. Set to 0 if data mask, write DBI and read DBI are all disabled at DRAM. Otherwise, it should be set to 1. 1'b0: DBI is not calibrated during write training. 1'b1: DBI is calibrated during write training.
16	RO	0x0	wrlvl_resp Response after write levelling is done.
15	RW	0x0	LP5_16bank_mode LP5 16bank mode 1'b1: 16bank mode 1'b0: 4bg/4bank mode 8 bank mode don't care about this field.
14:13	RW	0x0	ctrl_upd_interval DLL update interval. DLL update is done periodically with interval defined by ctrl_upd_interval when ctrl_upd_time = 2'b10. 2'b00: 2us 2'b01: 4us 2'b10: 6us 2'b11: 8us
12:11	RW	0x0	lock_sample_condition Lock value sampling condition setting for lock value averaging. Applied when lock_averge_en = 1. 2'b00: Lock value will be sampled if ctrl_flock = 1. 2'b01: Lock value will be sampled if ctrl_clock = 1. 2'b10: Lock value will be sampled if ctrl_locked = 1.
10:9	RW	0x3	wrtrn_dqs_edge_en DQS edge enable for initial write training. This field can be changed to find the effect of duty cycle error on the initial write training result for debug purpose. For normal operation, use the default value (2'b11). 2'b11: DQ/DM captured at the rising and falling edge of DQS will be used for the initial write training (Default). 2'b01: DQ/DM captured only at the rising edge of DQS will be used for the initial write training. 2'b10: DQ/DM captured only at the falling edge of DQS will be used for the initial write training. 2'b00: Do not use.
8	RW	0x0	wrlvl_start Write levelling start. It can be enabled when wrlvl_mode = 1. It should be disabled after write levelling response (wrlvl_resp) is asserted.
7:6	RW	0x3	rdlvl_dqs_edge_en DQS edge enable for initial read training. This field can be changed to find the effect of duty cycle error on the initial read training result for debug purpose. For normal operation, use the default value (2'b11). 2'b11: DQ/DM captured at the rising and falling edge of DQS will be used for the initial read training (Default). 2'b01: DQ/DM captured only at the rising edge of DQS will be used for the initial read training. 2'b10: DQ/DM captured only at the falling edge of DQS will be used for the initial read training. 2'b00: Do not use.

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Bit	Attr	Reset Value	Description
5	RW	0x0	wr_cal_mode If it is enabled, PHY will use "SDLL Code" which is calculated during write training. If disabled, PHY will use "SDLL Code" which is calculated from master DLL (T/4).
4	RW	0x0	lock_average_en Lock value average enable. If enabled, moving average will be applied to DLL lock value to remove lock value deviation due to power noise. 1'b0: DLL lock value will not be averaged (Default). 1'b1: DLL lock value will be sampled and averaged. The number of lock value that will be averaged is defined in avg_window_size.
3	RW	0x0	rd_cal_mode When rd_cal_mode=1, PHY will use "SDLL Code" which is calculated during read training. If disabled, PHY will use "SDLL Code" which is calculated from master DLL (T/4).
2	RW	0x0	ca_cal_mode CBT mode enable. For LPDDR4, if ca_cal_mode = 1 and cbt_vref_dqs_en[N] = 1, DQS/DQ/DM pad for Byte N will be set to driver mode. For LPDDR5, if ca_cal_mode = 1 and cbt_bit_dq_en[n] = 0, DQ pad for bit n will be set to driver mode.
1	RW	0x0	gate_cal_mode Gate training mode enable. If Gate training is used, this value should be high during operation. 1'b1: PHY will apply Gate cycle/offset result (GT_VWMC*_cs0/cs1 and GT_CYC*_cs0/cs1) from Gate training to gate signal. 1'b0: PHY will apply ctrl_shiftc to gate signal.
0	RW	0x0	wrlvl_mode Write levelling Mode Enable. If write levelling is configured (wrlvl_mode = 1), DQ/DM pad will be set to receiver mode (io_dq_en=16'hFFFF, io_dm_en=2'b11) and DQS pad will be set to driver mode (io_pdqs_en=2'b00, io_ndqs_en=2'b00).

DDRPHY_CAL_CON1

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RW	0x2	wrtrn_pass_adj This field controls how many times Write should be operated well to determine if it goes into VWP (Valid Window Period) or not. For write training, PHY decides that DQ is in the valid window if data check passes *4 times consecutively. The valid range is 0x1~0xF 4'h1: PHY decides that DQ is in the valid window if data check passes 4 time. 4'h2: PHY decides that DQ is in the valid window if data check passes 8 times consecutively. 4'h3: PHY decides that DQ is in the valid window if data check passes 12 times consecutively. ..... 4'hE: PHY decides that DQ is in the valid window if data check passes 56 times consecutively. 4'hF: PHY decides that DQ is in the valid window if data check passes 60 times consecutively.
27	RW	0x0	dfi_error_en Dfi error enable

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Bit	Attr	Reset Value	Description
26:20	RW	0x01	rdlvl_incr_adj Initial training step size (default: 7'h1, fine step delay). It should be smaller than 7'b0F. This is valid only for write/read DQ calibration, gate training and write levelling. [26:25]=2'b00: The step value will be "rdlvl_incr_adj[4:0]". [26:25]=2'b01: The step value will be "T/4". [26:25]=2'b10: The step value will be "T/8". [26:25]=2'b11: The step value will be "T/64".
19:16	RW	0x4	rdlvl_pass_adj This field controls how many times "Read" should be operated well to determine if it goes into VWP (Valid Window Period) or not. 4'h1: PHY decides that DQS is in the valid window if data check passes 2 time. 4'h2: PHY decides that DQS is in the valid window if data check passes 4 times consecutively. 4'h3: PHY decides that DQS is in the valid window if data check passes 6 times consecutively. 4'h4: PHY decides that DQS is in the valid window if data check passes 8 times consecutively. 4'h5: PHY decides that DQS is in the valid window if data check passes 10 times consecutively. 4'h6: PHY decides that DQS is in the valid window if data check passes 12 times consecutively. 4'h7: PHY decides that DQS is in the valid window if data check passes 14 times consecutively. Others: Do not use.
15:14	RW	0x0	ctrl_rpost_opt LPDDR5 read post-amble toggle option. Refer to read post-amble description in DRAM spec. 2'b00: Read post-amble = 0.5tWCK static. 2'b01: Read post-amble = 2.5tWCK static. 2'b10: Read post-amble = 4.5tWCK static.
13:7	RW	0x40	glvl_periodic_incr_adj Periodic (or short) gate training step size. It should be smaller than 7'h1F. Default value is 7'b1000000 (T/4). [13:12]=2'b00: The step value will be "glvl_periodic_incr_adj[4:0]". [13:12]=2'b01: The step value will be "T/2". [13:12]=2'b10: The step value will be "T/4" (default). [13:12]=2'b11: The step value will be "T/8". [13:7]=7'h00: The step value will be "T/16".
6:0	RW	0x01	rdlvl_periodic_incr_adj Periodic (or short) training step size. It decides the step value of delay line to increase during periodic read and write training. It should be smaller than 7'b0F. Default value is 7'h40 (T/32). [6:5]=2'b00: The step value will be "rdlvl_periodic_incr_adj[4:0]". [6:5]=2'b01: The step value will be "T/16". [6:5]=2'b10: The step value will be "T/32" (default). [6:5]=2'b11: The step value will be "T/64".

DDRPHY_CAL_CON2

Address: **Operational Base** + offset (0x000C)

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Bit	Attr	Reset Value	Description
31	RW	0x0	ctrl_rpre_opt Read pre-amble toggle option. Refer to read pre-amble description in DRAM spec. For LPDDR4: 1'b1: Read pre-amble = 2nCK toggle 1'b0: Read pre-amble = 2nCK static For LPDDR5: 1'b1: Read pre-amble = 2tWCK static + 2tWCK toggle 1'b0: Read pre-amble = 2tWCK static
30	RW	0x1	ctrl_rodt_disable Read ODT (On-Die-Termination) disable signal 1'b1: Read ODT disabled. Drive ctrl_read_p* to 0. If using LPDDR4, ctrl_read_p* will be always 0 by enabling this field (io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are low). 1'b0: Read ODT enabled. Drive ctrl_read_p* normally (io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are high only for read duration).
29	RW	0x0	ctrl_shgate This field controls the gate control signal 1'b0: Gate signal length = "burst length / 2" + N (Apply when DQS Pull-Down is enabled. N is determined by ctrl_gateduradj.) 1'b1: Gate signal length = "burst length / 2" ? 1 For LPDDR4, MR1 should be programmed so that read pre-amble is 2nCK static and read post-amble is 0.5tCK when shgate is 1'b0.
28	RW	0x0	ctrl_gt_fine_disable Gate fine training enable for periodic gate training
27:24	RW	0x2	ctrl_gateduradj It adjusts the duration cycle of "ctrl_gate" on a clock cycle base. MSB (bit3) controls direction: 1'b1: Subtract duration 1'b0: Add duration Bit[2:0] set duration value
23:20	RW	0x0	ctrl_gateadj It adjusts the enable time of "ctrl_gate" on a clock cycle base. The reference point is at the end of RL. MSB (bit3) controls direction: 1'b1: Subtract delay 1'b0: Add delay Bit[2:0] set delay value. When gate training is enabled, it configures the start point of gate training. If gate training is not enabled, it will be used to manually control the position of ctrl_gate.
19:16	RW	0x0	ctrl_readduradj It adjusts the duration cycle of "ctrl_read" on a clock cycle base. "ctrl_read" is the read odt control signal within PHY. MSB (bit3) controls direction: 1'b1: Subtract delay 1'b0: Add delay Bit[2:0] set delay value. It determines the high duration of io_pdqs_read, io_ndqs_read, io_dq_read and io_dm_read if ctrl_rodt_disable is 0.

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Bit	Attr	Reset Value	Description
15:12	RW	0x1	ctrl_readadj It adjusts the enable time of "ctrl_read" on a clock cycle base. The reference point is at the end of RL. MSB (bit3) controls direction: 1'b1: Subtract delay 1'b0: Add delay Bit[2:0] set delay. It determines the start cycle of high duration of io_pdqs_read, io_ndqs_read, io_dq_read and io_dm_read if ctrl_rodt_disable is 0.
11	RW	0x0	ctrl_readduradj_ext Default value is 0. This field is used for extend control range of ctrl_readduradj value. ctrl_readduradj_ext = 1'b0 (default) => Non Extended ctrl_readduradj_ext = 1'b1 => ctrl_readduradj[2:0] + 'h8
10	RW	0x0	ctrl_readadj_ext Default value is 0. This field is used for extend control range of ctrl_readadj value. ctrl_readadj_ext = 1'b0 (default) => Non Extended ctrl_readadj_ext = 1'b1 => ctrl_readadj[2:0] + 'h8
9:8	RW	0x3	ctrl_maskdur_adj Single-ended NDQS input glitch masking duration adjustment during read ODT enable timing. 2'b11 (default): SE NDQS Glitch 3.5tCK masking 2'b10: SE NDQS Glitch 4.5tCK masking 2'b00: SE NDQS Glitch 5.5tCK masking
7	RW	0x0	ctrl_long_gate_train_mode Gate training mode by long gate (shgate = 0)
6:4	RW	0x0	glvl_start_adj Gate training start point adjustment. This field adjusts the initial code provided to the gate delay line at the beginning of periodic gate training. [6:4]=3'b000: The start point code is -T from the first DQS rising edge. [6:4]=3'b001: The start point code is -7T/8 from the first DQS rising edge. [6:4]=3'b010: The start point code is -6T/8 from the first DQS rising edge. [6:4]=3'b011: The start point code is -5T/8 from the first DQS rising edge. [6:4]=3'b100: The start point code is -4T/8 from the first DQS rising edge. [6:4]=3'b101: The start point code is -3T/8 from the first DQS rising edge. [6:4]=3'b110: The start point code is -2T/8 from the first DQS rising edge. [6:4]=3'b111: The start point code is -T/8 from the first DQS rising edge.

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Bit	Attr	Reset Value	Description
3	RW	0x0	ctrl_gateduradj_ext Default value is 0. This field is used for extend control range of ctrl_gateduradj value. ctrl_gateduradj_ext = 1'b0 (default) => Non Extended ctrl_gateduradj_ext = 1'b1 => ctrl_gateduradj[2:0] + 'h8
2	RW	0x0	ctrl_gateadj_ext Default value is 0. This field is used for extend control range of ctrl_gateadj value. ctrl_gateadj_ext = 1'b0 (default) => Non Extended ctrl_gateadj_ext = 1'b1 => ctrl_gateadj[2:0] + 'h8
1:0	RW	0x0	ctrl_read_width The default is 1'b0. We strongly recommend that it should have one more idle cycle between read and write because the variation of data arrival time during read can be greater than 1 cycle. If it is 1'b1, the package and board should be carefully optimized with a short length and it should be used at the low frequency. 1'b0: Termination on (io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are driven high) period is (BL/2+1.5) cycle (Default) 1'b1: Termination on period (io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are driven high is (BL/2+1) cycle (Not recommended)

DDRPHY_CAL_CON3

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:26	RW	0x3f	vt_phyupd_req_cycle For debug purpose. For phy-initated update mode, it controls the number of cycle during which cs_phyupd FSM stays at ST_UPD_WAIT state.
25:22	RW	0x1	dvfs_wait_cycle For debug purpose. It controls the number of cycle during which cs_phydvfs FSM stays at ST_DVFS_A state.
21:16	RW	0x3f	vt_mcupd_req_cycle For debug purpose. For mc-initiated update mode, it controls the number of cycle during which cs_phyupd FSM stays at ST_UPD_WAIT state.
15:12	RW	0x9	upd_ack_cycle For debug purpose. It controls the number of cycle during which cs_phyupd FSM stays at ST_UPD_ACK state.
11	RW	0x0	auto_dqs_clean Enable Auto-DQS-Clean mode. Auto-DQS-Clean needs following conditions. 1. Gate training off 2. Use differential IO with VSSQ-Term. 3. ctrl_shgate=1'b0, ctrl_gateduradj=4'b0001 4. tDQSCK (min) =< 2*tCK: ctrl_gateadj = 4'b1001 tDQSCK (min) > 2*tCK: ctrl_gateadj = 4'b0000

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Bit	Attr	Reset Value	Description
10	RW	0x0	gt_sw_mode Gate training register RW mode control for debug purpose. pcl_pd should be set to 1'b0 to enable write mode. 1'b1: CAL_GT_CS0_VWMC0, CAL_GT_CS1_VWMC0, CAL_GT_CS0_CYC, CAL_GT_CS1_CYC are writable when dvfs_mode = 2'b00 and ctrl_shgate = 1'b1. 1'b0: CAL_GT_CS0_VWMC0, CAL_GT_CS1_VWMC0, CAL_GT_CS0_CYC, CAL_GT_CS1_CYC are read-only.
9	RW	0x0	wr_sw_mode SW write training code update control. This field will be enabled when restoring the previous write training results. pcl_pd should be set to 1'b0 to enable write mode. 1'b1: SW_WR_DESKEWC_CS0_CON*, SW_WR_DESKEWC_CS1_CON*, SW_WR_DESKEWL_CS0_CON*, SW_WR_DESKEWL_CS1_CON* will be written to internal write training code. 1'b0: SW_WR_DESKEWC_CS0_CON*, SW_WR_DESKEWC_CS1_CON*, SW_WR_DESKEWL_CS0_CON*, SW_WR_DESKEWL_CS1_CON* will not be written to internal write training code.
8	RW	0x0	rd_sw_mode SW read training code update control. This field will be enabled when restoring the previous read training registers. pcl_pd should be set to 1'b0 to enable write mode. 1'b1: SW_RD_DESKEW_CENTER_CS0_CON_*, SW_RD_DESKEW_LEFT_CS0_CON_*, SW_RD_DQS_VWMC_CS0_CON0, SW_RD_DQS_VWML_CS0_CON0, SW_RD_DESKEW_CENTER_CS1_CON_*, SW_RD_DESKEW_LEFT_CS1_CON_*, SW_RD_DQS_VWMC_CS1_CON0, SW_RD_DQS_VWML_CS1_CON0 will be written to internal Read training code. 1'b0: SW_RD_DESKEW_CENTER_CS0_CON_*, SW_RD_DESKEW_LEFT_CS0_CON_*, SW_RD_DQS_VWMC_CS0_CON0, SW_RD_DQS_VWML_CS0_CON0, SW_RD_DESKEW_CENTER_CS1_CON_*, SW_RD_DESKEW_LEFT_CS1_CON_*, SW_RD_DQS_VWMC_CS1_CON0, SW_RD_DQS_VWML_CS1_CON0 will not be written to internal read training code.
7	RW	0x0	wrlvl_sw_mode ctrl_wrlvl_code register RW mode control for debug purpose. pcl_pd should be set to 1'b0 to enable write mode. 1'b1: ctrl_wrlvl1_code and ctrl_wrlvl0_code are writable when wrlvl_mode is set and pcfg_mode[2] is high. 1'b0: ctrl_wrlvl1_code and ctrl_wrlvl0_code are read-only.
6	RW	0x0	prbs_sw_mode SW PRBS training code update control. This field will be enabled when restoring the previous PRBS training resisters. pcl_pd should be set to 1'b0 to enable write mode. 1'b1: PRBS_CON4 and PRBS_CON5 will be written to internal PRBS training code. 1'b0: PRBS_CON4 and PRBS_CON5 are not written to internal PRBS training code.

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	min_locktime_adj MDLL lock check timing control after DLL relock start during DVFS pause. 2'b00: Default. 2'b01: MDLL lock check timing will be delayed by 1 DFI cycle. 2'b10: MDLL lock check timing will be delayed by 2 DFI cycle. 2'b11: MDLL lock check timing will be delayed by 3 DFI cycle.
3	RO	0x0	reserved
2:0	RW	0x0	pcfg_mode PHY configuration register mode control signal to read the information at each data slice for debug. This field should be set to 'h0 for normal operation. [2] = 1: Read mode enable for debug. VT compensated DLL codes will be read out for RD_DESKEW_CENTER_CS0_CON_DM, RD_DESKEW_CENTER_CS0_CON*, RD_DESKEW_CENTER_CS1_CON_DM, RD_DESKEW_CENTER_CS1_CON*, WR_DESKEWC_CS0_CON*, WR_DESKEWC_CS1_CON*, DM_DESKEWC_CS0_CON*, DM_DESKEWC_CS1_CON*. The original DLL code will be read out for WR_LVL_CON*. [2] = 0: Read mode disabled. VT compensated DLL codes will be read out for WR_LVL_CON*. The original DLL codes will be read out for RD_DESKEW_CENTER_CS0_CON_DM, RD_DESKEW_CENTER_CS0_CON*, RD_DESKEW_CENTER_CS1_CON_DM, RD_DESKEW_CENTER_CS1_CON*, WR_DESKEWC_CS0_CON*, WR_DESKEWC_CS1_CON*, DM_DESKEWC_CS0_CON*, DM_DESKEWC_CS1_CON*.

DDRPHY_CAL_CON4

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RW	0x0	LP4_High_density_mode LPDDR4 high density mode 1'b1: Support R17/R18 for ACT2 1'b0: Support 2'b11 command for ACT2 This field should be disabled in LPDDR5.
30:24	RW	0x00	glvl_periodic_fine_incr_adj Periodic gate training step size at fine mode. It should be smaller than 7'h1F. Default value is 7'b0000000 (T/16). [30:29]=2'b00: The step value will be "glvl_periodic_fine_incr_adj[4:0]". [30:29]=2'b01: The step value will be "T/32". [30:29]=2'b10: The step value will be "T/4". [30:29]=2'b11: The step value will be "T/8". [30:24]=7'h00: The step value will be "T/16" (default).
23	RW	0x1	glitch_removal_length This field is used for control postamble glitch removal duration. 1'b0: 1.5tCK 1'b1: 1tCK
22	RW	0x0	glitch_removal_en This field is used for postamble glitch removal enable during Auto-DQS-Clean mode. 1'b0: Glitch removal disable 1'b1: Glitch removal enable

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Bit	Attr	Reset Value	Description
21:16	RW	0x03	lock_avg_cnt_number This field determines the lock value update counter maximum number for moving averaging.
15	RW	0x1	WCK_MASK This field is option for WCK OFF timing on rank2rank operation 1'b1: WCK off timing on rank2rank operation can be allowed as optimized parameter by SMC 1'b0: WCK off timing on rank2rank operation can be allowed same as WCK off timing on same rank operation.
14	RW	0x0	cmdfifo_wl_ext This field determines command FIFO write latency extension mode for auto dqs clean and ONLY use at LPDDR5. If this field set to 1, PHY can support RL = 21.
13:12	RW	0x0	upd_range_ext Default value is 0. This field is used for extend control range of ctrl_upd_range value. upd_range_ext = 2'b00 (default) 2'b00: Update when difference is greater than 0 tFS. 2'b01: Update when difference is greater than 3 tFS. 2'b10: Update when difference is greater than 7 tFS. 2'b11: Update when difference is greater than 15 tFS. upd_range_ext = 2'b01 2'b00: Update when difference is greater than 5 tFS. 2'b01: Update when difference is greater than 9 tFS. 2'b10: Update when difference is greater than 11 tFS. 2'b11: Update when difference is greater than 13 tFS. upd_range_ext = 2'b10 2'b00: Update when difference is greater than 17 tFS. 2'b01: Update when difference is greater than 19 tFS. 2'b10: Update when difference is greater than 21 tFS. 2'b11: Update when difference is greater than 23 tFS. upd_range_ext = 2'b11 2'b00: Update when difference is greater than 25 tFS. 2'b01: Update when difference is greater than 27 tFS. 2'b10: Update when difference is greater than 29 tFS. 2'b11: Update when difference is greater than 31 tFS.
11	RW	0x0	wrtrn_multi_pattern Multi-pattern enable during the initial write training. 1'b0: One BL16 pattern will be asserted at each DLL code during write training. 1'b1: Four BL16 patterns will be asserted at each DLL code during write training.
10:6	RW	0x01	num_repeat The number of DRAM access at each DLL code during the initial read or write training. PHY will collect pass/fail decision for num_repeat times DRAM access at each DLL code. For initial write training, 4*num_repeat DRAM access will occur at each DLL code if wrtrn_multi_pattern is 1. Don't use 0x0.
5	RW	0x1	dvfs_wrtrn_mode DVFS write training mode select. 1'b0: DVFS write training starts dvfs_wr_start_adj steps earlier from DQ right side edge. Training code will be increased to find the correct DQ/DBI location. 1'b1: DVFS write training starts at DQ right side edge determined at the initial write training. Training code will be increased or decreased to find the correct DQ/DBI location.

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Bit	Attr	Reset Value	Description
4:0	RW	0x0f	dvfs_wr_start_adj DVFS write training start point. It is valid only when dvfs_wrtrn_mode = 0 (or binary_en = 1, TBD). It determines how early DVFS write training starts from the previous write training code (T=current lock value). DVFS write training start point = Write DQ/DM Left code - (dvfs_wr_start_adj*2)

DDRPHY_LP_CON0

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x3	ctrl_wck_phy_cg_en_ignore This field support to ignore phy_cg_en for WCK at WCK free running mode. This field should be controlled at WCK free running mode. [19]: Byte1 control [18]: Byte0 control 1'b1: Ignore phy_cg_en control for WCK. 1'b0: WCK is controlled by phy_cg_en.
17:16	RW	0x0	ctrl_pulld_dq Active high signal to pull-down the high-z duration of DQ/DM signals for debug purpose. For normal operation this field should be zero. When bus is idle, it can be set to pull-down or up the bus not to make bus high-z state. 2'b11: DQ/DM pull down enabled. io_dq_pdn and io_dm_pdn will be driven high. io_dq_pup and io_dm_pup will be driven low. 2'b00: DQ/DM pull down disabled. io_dq_pdn and io_dm_pdn will be driven low. io_dq_pup and io_dm_pup will be driven low. Others: Don't use.
15	RW	0x0	cs_io_pd Command signal I/O driver power down mode select. If enabled, command signal I/O driver will be turned on and off dynamically depending on "ctrl_wake_up" to save I/O power. This field should not be changed during the normal operation. 1'b0: Command signal I/O driver will be always on (io_adct_en is always low). 1'b1: Enable command signal I/O driver dynamic power down. Command signal I/O driver will be turned on (io_adct_en is low) only when ctrl_wake_up is high.
14	RW	0x1	ds_io_pd DQ, DM, DQS I/O receiver power down will be enabled dynamically during normal operation to save I/O power. 1'b0: DQS/DQ/DM receiver power down will be disabled and receivers are always on (io_dq_pd, io_dqs_pd, io_dm_pd are low). 1'b1: DQS/DQ/DM receiver is on (io_dq_pd, io_dqs_pd, io_dm_pd is low) only for the read duration, off (io_dq_pd, io_dqs_pd, io_dm_pd is high) otherwise.
13	RW	0x0	scheduler_HW_clock_gating_disable PHY scheduler dynamic clock gating disable signal 1'b0: HW dynamic clock gating funtion enable 1'b1: HW dynamic clock gating futnion ingore

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Bit	Attr	Reset Value	Description
12	RW	0x0	pcl_pd PHY control logic clock gating enable. This field can be enabled after all the initial (or long) training is done. 1'b0: PHY control logic clock gating off 1'b1: PHY control logic clock gating on. PHY internal clock will be alive if debug_mode_en is high or if write/read/gate training is on-going. Otherwise, internal clock will be gated.
11	RW	0x0	mdll_cg_en Master DLL dynamic clock gating mode 1'b0: MDLL dynamic clock gating off 1'b1: MDLL dynamic clock gating on. MDLL clock gating will be controlled by ctrl_phy_cg_en.
10	RW	0x1	dqs_enable 1'b1: dqs enable 1'b0: dqs disable
9	RW	0x0	wck_enable 1'b1: WCK enable (LPDDR5 option) 1'b0: WCK disable (LPDDR4 option)
8	RW	0x0	ctrl_dqs_drv_off DQS driver off signal. When this field enabled, DQS driver is turned off (io_pdqs_en = 1'b1, io_ndqs_en = 1'b1). This field should be enabled when LPDDR5 is used.
7	RW	0x0	ctrl_dq_rcv_on DQ receiver on signal. When this field enabled, DQ receiver is turned on (io_dq_read = 1'b1, io_dq_pd = 1'b0).
6	RW	0x0	ctrl_scheduler_en PHY scheduler clock enable (LPDDR5 should be enabled) 1'b1: Clock enable 1'b0: Clock disable
5:4	RO	0x0	reserved
3	RW	0x0	write_se_wck wck single-ended mode 1'b1: Single-ended mode 1'b0: Differential mode Caution: write_se_ck should be enabled using write_se_wck in LPDDR5.
2	RO	0x0	reserved
1:0	RW	0x3	ctrl_pulld_dqs Active high signal to pull-up or down PDQS/NDQS signals. When using gate training in LPDDR4, this field can be zero. When bus is idle, it can be set to pull-down or up the bus to avoid high-z state (PDQS/NDQS is pulled-down/up). If not using gate training, this field should be always set for normal operation to make P/NDQS signals pull-down/up. 2'b11: DQS pull-down enabled. io_pdqs_pdn is set to high. io_ndqs_pup are set to high only if ctrl_dfdqs is high. io_pdqs_pup and io_ndqs_pdn are set to low. 2'b00: DQS pull-down disabled. io_pdqs_pdn and io_ndqs_pup are set to low. io_pdqs_pup and io_ndqs_pdn are set to low.

DDRPHY_GATE_CON0

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:24	RW	0x3	rank_en Rank enable signal for read command decoding and dynamic gate training. 2'b11: Enable rank0 and rank1, CS[1:0] used for read command decoding, which is used to generate gate signal. 2'b01: Enable rank0, CS[0] only used for read command decoding. 2'b10: Enable rank1, CS[1] only used for read command decoding.
23:14	RO	0x000	reserved
13:12	RW	0x3	rank1_dsen DQS cleaning/gate signal generation enable for rank1. [13]: Enable data slice 1 [12]: Enable data slice 0
11:2	RO	0x000	reserved
1:0	RW	0x3	rank0_dsen DQS cleaning/gate signal generation enable for rank0. [1]: Enable data slice 1 [0]: Enable data slice 0

DDRPHY_OFFSETR_CON0

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	ctrl_offsetr1 This field can be used to give offset to read DQS for debug purpose. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes high and low. The right-shifted value is limited by the quarter of the maximum delay in master delay line. Read DQS offset amount: ctrl_offsetr1[9] = 1: (tFS: fine step delay) Read DQS 90 degree delay amount or read DQS delay from read training - ctrl_offsetr1[8:0] x tFS ctrl_offsetr1[9] = 0: Read DQS 90 degree delay amount or read DQS delay from read training + ctrl_offsetr1[8:0] x tFS
15:10	RO	0x00	reserved
9:0	RW	0x000	ctrl_offsetr0 This field can be used to give offset to read DQS for debug purpose. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes high and low. The right-shifted value is limited by the quarter of the maximum delay in master delay line. Read DQS offset amount: ctrl_offsetr0[9] = 1: (tFS: fine step delay) Read DQS 90 degree delay amount or read DQS delay from read training - ctrl_offsetr0[8:0] x tFS ctrl_offsetr0[9] = 0: Read DQS 90 degree delay amount or read DQS delay from read training + ctrl_offsetr0[8:0] x tFS

DDRPHY_OFFSETW_CON0

Address: **Operational Base** + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	ctrl_offsetw1 This field can be used to give offset to write DQ/DM in byte1 for debug purpose. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes high and low. The right-shifted value is limited by the quarter of the maximum delay in master delay line. Write DQ offset amount : ctrl_offsetw1[9] = 1: (tFS: fine step delay) Write DQ 270 degree delay amount or write DQ delay from write training - ctrl_offsetw1[8:0] x tFS ctrl_offsetw1[9] = 0: Write DQ 270 degree delay amount or write DQ delay from write training + ctrl_offsetw1[8:0] x tFS
15:10	RO	0x00	reserved
9:0	RW	0x000	ctrl_offsetw0 This field can be used to give offset to write DQ/DM in byte0 for debug purpose. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes high and low. The right-shifted value is limited by the quarter of the maximum delay in master delay line. Write DQ offset amount : ctrl_offsetw0[9] = 1: (tFS: fine step delay) Write DQ 270 degree delay amount or write DQ delay from write training - ctrl_offsetw0[8:0] x tFS ctrl_offsetw0[9] = 0: Write DQ 270 degree delay amount or write DQ delay from write training + ctrl_offsetw0[8:0] x tFS

DDRPHY_OFFSET_DQ_CON0

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:7	RW	0x00	ctrl_offset_dq_ds1 Offset control for read DQ/DM bits in byte1. It is used to impose delay for read DQ/DM before read training, so that DQS is ahead of DQ/DM. Once this field is set, it should not change during operation. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes high and low. The right-shifted value is limited by the quarter of the maximum delay in master delay line. Read DQ/DM offset amount: ctrl_offset_dq_ds1[6:0] x tFS
6:0	RW	0x00	ctrl_offset_dq_ds0 Offset control for read DQ/DM bits in byte0. It is used to impose delay for read DQ/DM before read training, so that DQS is ahead of DQ/DM. Once this field is set, it should not change during operation. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes high and low. The right-shifted value is limited by the quarter of the maximum delay in master delay line. Read DQ/DM offset amount: ctrl_offset_dq_ds0[6:0] x tFS

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DDRPHY_OFFSETC_CON0

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	ctrl_offsetc1 Gate offset amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after ctrl_vtc_en is high and ctrl_vtc_en is high and dfi_ctrlupd_req becomes high and low. It is used to give offset to gate training result for debug purpose. ctrl_offsetc [9] = 1: (tFS: fine step delay) Total gate delay amount - ctrl_offsetc [8:0] x tFS ctrl_offsetc [9] = 0: Total gate delay amount + ctrl_offsetc [8:0] x tFS
15:10	RO	0x00	reserved
9:0	RW	0x000	ctrl_offsetc0 Gate offset amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after ctrl_vtc_en is high and dfi_ctrlupd_req becomes high and low. It is used to give offset to gate training result for debug purpose. ctrl_offsetc [9] = 1: (tFS: fine step delay) Total gate delay amount - ctrl_offsetc [8:0] x tFS ctrl_offsetc [9] = 0: Total gate delay amount + ctrl_offsetc [8:0] x tFS

DDRPHY_SHIFTC_CON0

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:3	RW	0x0	ctrl_shiftc1 Gate signal delay amount for DDR. This is used to adjust gate delay based on DFI PHY clock period. When gate_debug_en[3] = 1 for gate margin control. When gate_cal_mode = 0 for debug purpose. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes high and low. This value is limited by the half of the maximum delay in master delay line. 3'b000: 0 (0 degree shift) 3'b001: T (365 degree shift) 3'b010: T/2 (180 degree shift) 3'b011: T/4 (90 degree shift), 3'b100: T/8 (45 degree shift) 3'b101: T/16 (22.5 degree shift) 3'b111: 3T/4 (270 degree shift)
2:0	RW	0x0	ctrl_shiftc0 Gate signal delay amount for DDR. This is used to adjust gate delay based on DFI PHY clock period. When gate_debug_en[3] = 1 for gate margin control. When gate_cal_mode = 0 for debug purpose. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes high and low. This value is limited by the half of the maximum delay in master delay line. 3'b000: 0 (0 degree shift) 3'b001: T (365 degree shift) 3'b010: T/2 (180 degree shift)

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Bit	Attr	Reset Value	Description
			3'b011: T/4 (90 degree shift), 3'b100: T/8 (45 degree shift) 3'b101: T/16 (22.5 degree shift) 3'b111: 3T/4 (270 degree shift)

DDRPHY_OFFSETD_CON0

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	resync_handshake_mode This field controls SW DLL update policy. 1'b1: SW DLL update by handshaking between ctrl_resync and resync_done_flag*. 1'b0: SW DLL update by ctrl_resync enable and disable.
28	RW	0x0	upd_mode This field controls "PHY update" mode. 1'b1: MC-Initiated update mode. dfi_phyupd_req is not asserted by PHY. 1'b0: PHY-Initiated update mode. dfi_phyupd_req will be asserted by PHY.
27	RO	0x0	resync_done_flag_cs This field can identify resync is applied for CtrlPHY. 1'b1: Resync is applied. 1'b0: Resync is not applied.
26	RO	0x0	resync_done_flag_ds1 This field can identify resync is applied for DataPHY1. 1'b1: Resync is applied. 1'b0: Resync is not applied.
25	RO	0x0	resync_done_flag_ds0 This field can identify resync is applied for DataPHY0. 1'b1: Resync is applied. 1'b0: Resync is not applied.
24	RW	0x0	ctrl_resync Active rising edge signal. User should set this signal low after setting high for normal operation. When this bit transits from low to high, pointers of FIFO within PHY and all of the DLL information (Read/Write/CA/CS DLL) is updated. If PHY is set to PHY-initiated updated mode, dfi_phyupd_req/dfi_phyupd_ack handshake should occur after ctrl_resync transits from low to high. If PHY is set to MC-initiated update mode, FIFO reset and DLL update will progress without a handshake after ctrl_resync transits from low to high. In general, this bit should be set only during initialization and refresh cycles. NOTE: Invalid command that are not listed in JEDEC command truth table could be interpreted as Read command and it will lead to FIFO/gate signal corruption. For example, vendor specific TMRS is reported to be causing this issue. Please toggle ctrl_resync after sending TMRS so that FIFO and gate signal can be restored.
23:10	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	ctrl_offsetd DLL offset control for CA. It can be controlled to adjust delay of CA bus during command bus training. If this field is fixed, this should not be changed during normal operation. This value is valid only after dfi_ctrlupd_req becomes high and low. The right-shifted value is limited by the quarter of the maximum delay in master delay line. offset amount for CA: ctrl_offsetd[9] = 1: (tFS: fine step delay) CA deskew delay - ctrl_offsetd[8:0] x tFS ctrl_offsetd[9] = 0: CA deskew delay + ctrl_offsetd[8:0] x tFS

DDRPHY_OFFSETO_CON0

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	ctrl_offseto1 This field can be used to give offset to io_dq_en[15:8]/io_dm_en[1], which controls DQ/DM PAD OEN for byte1 for debug purpose.. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes high and low. The right-shifted value is limited by the quarter of the maximum delay in master delay line. offset amount: ctrl_offseto1[9] = 1: (tFS: fine step delay) DQ/DM OEN 270 degree delay amount - ctrl_offseto1[8:0] x tFS ctrl_offseto1[9] = 0: DQ/DM OEN 270 degree delay amount + ctrl_offseto1[8:0] x tFS
15:10	RO	0x00	reserved
9:0	RW	0x000	ctrl_offseto0 This field can be used to give offset to io_dq_en[7:0]/io_dm_en[0], which controls DQ/DM PAD OEN for byte0 for debug purpose.. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes high and low. The right-shifted value is limited by the quarter of the maximum delay in master delay line. offset amount: ctrl_offseto0[9] = 1: (tFS: fine step delay) DQ/DM OEN 270 degree delay amount - ctrl_offseto0[8:0] x tFS ctrl_offseto0[9] = 0: DQ/DM OEN 270 degree delay amount + ctrl_offseto0[8:0] x tFS

DDRPHY_WR_LVL_CON0

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	ctrl_wrlvl1_code Write levelling slave DLL code value for data slice 1. It will be applied to write DQS DLL code if wrlvl_sw_mode is enabled, wrlvl_mode is set and pcfg_mode[2] is high.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	ctrl_wrlvl0_code Write levelling slave DLL code value for data slice 0. It will be applied to write DQS DLL code if wrlvl_sw_mode is enabled, wrlvl_mode is set and pcfg_mode[2] is high.

DDRPHY_WR_LVL_CON1

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:20	RW	0x1e	tWLMRD It controls tWLMRD and tWLDQSEN parameter during write levelling. tWLMRD = DFI PHY clock period * (tWLMRD) tWLDQSEN = DFI PHY clock period * (tWLMRD/2)
19:14	RW	0x20	tWLO It controls tWLO parameter during write levelling. It controls when PHY samples DQ feedback from DRAM during write levelling. tWLO = DFI PHY clock period * tWLO
13:8	RW	0x04	tDQSL It controls tDQSL parameter during write levelling. It controls interval of DQS toggles during write levelling. tDQSL = DFI PHY clock period * tDQSL
7:4	RW	0x7	wrlvl_wck_toggle Number of WCK toggle. It control toggle of WCK when wck2ck levelling and Vref setting on CBT. 4'b0001: 4 WCK toggle 4'b0011: 6 WCK toggle 4'b0111: 8 WCK toggle (default) 4'b1111: 10 WCK toggle
3:0	RW	0x3	wrlvl_dqs_toggle Number of DQS toggle. It control toggle of DQS when write levelling and Vref setting on CBT. 4'b0001: 1tCK DQS toggle 4'b0011: 2tCK DQS toggle (default) 4'b0111: 3tCK DQS toggle 4'b1111: 4tCK DQS toggle

DDRPHY_WR_LVL_CON2

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:24	RW	0x40	twlcal_en Calibration enable duration control. Controls the duration from training enable to the first command trigger in DFI cycle.
23:16	RW	0x46	twlcal_wait For debug purpose
15:12	RW	0x5	NUM_RST_CMD Number of MPC WR/RD FIFO CMD. This controls the number of repetition of MPC WR/RD FIFO CMD that are used to reset MPC FIFO.
11:6	RW	0x16	trden2resp Calibration done check timing control. Controls when to check the training response from each byte in DFI cycle.

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Bit	Attr	Reset Value	Description
5:4	RO	0x0	wlcal_fail It will be enable if there in no pass period after WL calibration. It should be read by zero if calibration is done normally. wlcal_fail[1]: For byte 1 wlcal_fail[0]: For byte 0
3:2	RO	0x0	ctrl_dqs_extra Add extra write DQS toggle on postamble. This field will be enabled when wr_sw_mode is enabled. The maxmium is 1tCK. [1:0] = 2'b01: +1tCK [1:0] = 2'b00: +0tCK
1:0	RO	0x0	ctrl_dqs_shift Write DQS cycle code for data slice. This field will be enabled when wr_sw_mode is enabled. The maxmium is 1tCK. [1]: DQS for byte 1 [0]: DQS for byte 0 1'b1 = +1tCK 1'b0 = +0tCK

DDRPHY_WR_LVL_CON3

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RO	0x0	wrlvl_half_over Write levelling SDLL code information. If write levelling code is over half of master dll code, "wrlvl_half_over[n]" will be "1" for data slice[n]. If it is set to high after write levelling, S/W can see that CK delay is smaller than DQS delay.
15:13	RO	0x0	reserved
12:8	RW	0x0b	wrlvl_wait It controls tWLO parameter during write levelling. It controls when PHY samples DQ feedback from DRAM during write levelling. tWLO = 4 * DFI PHY clock period * wrlvl_wait
7:3	RO	0x00	reserved
2	RW	0x0	dfi_wlcal_en Write latency calibration enable. When it is high, CA and CS will be delayed as 1 PHY clock cycle and 1 extra toggle will be added to DQS. If it is set to high, write latency calibration should be done to find proper write latency after write training.
1	RW	0x0	ctrl_wrlvl_clear Write levelling DLL code clear. When it is high, ctrl_wrlvl0_code~ctrl_wrlvl1_code, wrlvl_half_over, wrlvl_fail_status and PHY internal write levelling FSM will be reset.
0	RW	0x0	ctrl_wrlvl_resync Write levelling DLL code update enable. Active rising edge signal. This signal should become low after setting high for normal operation. When this bit transits from low to high, write DQS DLL codes will be updated with the current code. Assert and de-assert ctrl_wrlvl_resync to apply ctrl_wrlvl0_code ~ ctrl_wrlvl1_code to Write DQS DLL.

DDRPHY_CA_DESKEW_CON0

Address: **Operational Base** + offset (0x007C)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	CA1DeSkewCode BDLL code for CA[1]. The delay for CA[1] signal will be CA1DeSkew value tFS.
15:10	RO	0x00	reserved
9:0	RW	0x000	CA0DeSkewCode BDLL code for CA[0]. The delay for CA[0] signal will be CA0DeSkew value tFS.

DDRPHY_CA_DESKEW_CON1

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	CA3DeSkewCode BDLL code for CA[3]. The delay for CA[3] signal will be CA3DeSkew value tFS.
15:10	RO	0x00	reserved
9:0	RW	0x000	CA2DeSkewCode BDLL code for CA[2]. The delay for CA[2] signal will be CA2DeSkew value tFS.

DDRPHY_CA_DESKEW_CON2

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	CA5DeSkewCode BDLL code for CA[5]. The delay for CA[5] signal will be CA5DeSkew value tFS.
15:10	RO	0x00	reserved
9:0	RW	0x000	CA4DeSkewCode BDLL code for CA[4]. The delay for CA[4] signal will be CA4DeSkew value tFS.

DDRPHY_CA_DESKEW_CON3

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	RSTDeSkewCode BDLL code for RST. 0x0 or 0x8: The delay for RST signal will be zero delay. 0x9~0x2B: The delay for RST signal will be RSTDeSkew value - 'h8 tFS. Others: Invalid.

DDRPHY_CA_DESKEW_CON4

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	CKDeSkewCode BDLL code for CK. 0x0 or 0x8: The delay for CK signal will be zero delay. 0x9~0x2B: The delay for CK signal will be CKDeSkew value - 'h8 tFS. Others: Invalid.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	CA6DeSkewCode BDLL code for CA[6]. The delay for CA[6] signal will be CA6DeSkew value tFS.

DDRPHY_CA_DESKEW_CON5

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	CS1DeSkewCode BDLL code for CS1. The delay for CS1 signal will be CS1DeSkew value tFS.
15:10	RO	0x00	reserved
9:0	RW	0x000	CS0DeSkewCode BDLL code for CS0. The delay for CS0 signal will be CS0DeSkew value tFS.

DDRPHY_CA_DESKEW_CON6

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	CKE1DeSkewCode BDLL code for CKE1. 0x0 or 0x8: The delay for CKE1 signal will be zero delay. 0x9~0x2B: The delay for CKE1 signal will be CKE1DeSkew value - 'h8 tFS. Others: Invalid.
15:10	RO	0x00	reserved
9:0	RW	0x000	CKE0DeSkewCode BDLL code for CKE0. 0x0 or 0x8: The delay for CKE0 signal will be zero delay. 0x9~0x2B: The delay for CKE0 signal will be CKE0DeSkew value - 'h8 tFS. Others: Invalid.

DDRPHY_CAL_WR_PATTERN_CON0

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst1_8 This fields specifies the DQ pattern for BL1 and BL2 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the first valid rising edge of DQS. wrtrn_rddata_adj_w0_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the first valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst1_8 This fields specifies the DQ pattern for BL3 and BL4 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the second valid rising edge of DQS. wrtrn_rddata_adj_w1_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the second valid falling edge of DQS.

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DDRPHY_CAL_WR_PATTERN_CON1

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst1_8 This fields specifies the DQ pattern for BL5 and BL6 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid rising edge of DQS. wrtrn_rddata_adj_w0_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst1_8 This fields specifies the DQ pattern for BL7 and BL8 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON2

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst9_16 This fields specifies the DQ pattern for BL9 and BL10 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid rising edge of DQS. wrtrn_rddata_adj_w0_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst9_16 This fields specifies the DQ pattern for BL11 and BL12 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON3

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst9_16 This fields specifies the DQ pattern for BL13 and BL14 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid rising edge of DQS. wrtrn_rddata_adj_w0_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid falling edge of DQS.

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Bit	Attr	Reset Value	Description
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst9_16 This fields specifies the DQ pattern for BL15 and BL16 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON4

Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x1	wrtrn_rddata_dm_adj_w0_bst1_8 This fields specifies the DM pattern for BL1 and BL2 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase0[0] represents expected data of DM[0] and DQ[1] at the first valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase0[1] represents expected data of DM[0] and DM[1] at the first valid falling edge of DQS.
13:12	RW	0x1	wrtrn_rddata_dm_adj_w1_bst1_8 This fields specifies the DM pattern for BL3 and BL4 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase0[0] represents expected data of DM[0] and DQ[1] at the second valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase0[1] represents expected data of DM[0] and DM[1] at the second valid falling edge of DQS.
11:10	RW	0x1	wrtrn_rddata_dm_adj_w2_bst1_8 This fields specifies the DM pattern for BL5 and BL6 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase1[0] represents expected data of DM[0] and DQ[1] at the 3rd valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase1[1] represents expected data of DM[0] and DM[1] at the 3rd valid falling edge of DQS.
9:8	RW	0x1	wrtrn_rddata_dm_adj_w3_bst1_8 This fields specifies the DM pattern for BL7 and BL8 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase1[0] represents expected data of DM[0] and DQ[1] at the 4th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase1[1] represents expected data of DM[0] and DM[1] at the 4th valid falling edge of DQS.

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Bit	Attr	Reset Value	Description
7:6	RW	0x1	wrtrn_rddata_dm_adj_w0_bst9_16 This fields specifies the DM pattern for BL9 and BL10 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DQ[1] at the 5th valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DM[1] at the 5th valid falling edge of DQS.
5:4	RW	0x1	wrtrn_rddata_dm_adj_w1_bst9_16 This fields specifies the DM pattern for BL11 and BL12 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DQ[1] at the 6th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DM[1] at the 6th valid falling edge of DQS.
3:2	RW	0x1	wrtrn_rddata_dm_adj_w2_bst9_16 This fields specifies the DM pattern for BL13 and BL14 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DQ[1] at the 7th valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DM[1] at the 7th valid falling edge of DQS.
1:0	RW	0x1	wrtrn_rddata_dm_adj_w3_bst9_16 This fields specifies the DM pattern for BL15 and BL16 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DQ[1] at the 8th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DM[1] at the 8th valid falling edge of DQS.

DDRPHY_CAL_RD_PATTERN_CON0

Address: **Operational Base** + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:24	RW	0x55	rdtrn_inv_pattern_ds0 This fields specifies the lower byte invert. The expected read data pattern is defined with this field for read training or gate training with gate_rdchk_en enabled. The value should be the same as DRAM MR15 setting (Lower-Byte Invert Register for DQ Calibration).
23:16	RW	0x55	rdtrn_inv_pattern_ds1 This fields specifies the upper byte invert. The expected read data pattern is defined with this field for read training or gate training with gate_rdchk_en enabled. The value should be the same as DRAM MR20 setting (Upper-Byte Invert Register for DQ Calibration).

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Bit	Attr	Reset Value	Description
15:8	RW	0x5a	rdtrn_rddata_pattern0 This fields specifies the DQ/DMI pattern. The expected read data pattern is defined with this field for read training or gate training with gate_rdchk_en enabled. The value should be the same as DRAM MR32 setting (DQ Calibration Pattern "A").
7:0	RW	0x3c	rdtrn_rddata_pattern1 This fields specifies the DQ/DMI pattern. The expected read data pattern is defined with this field for read training or gate training with gate_rdchk_en enabled. The value should be the same as DRAM MR40 setting (DQ Calibration Pattern "B").

DDRPHY_MDLL_CON0

Address: **Operational Base** + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:24	RW	0x20	ctrl_start_point Initial DLL lock start point. This is the number of delay cells and is the start point where "DLL" start tracing to be locked. Initial delay time is calculated by multiplying the unit delay of delay cell and this value.
23	RW	0x0	clkm_cg_en_sw S/W master DLL clock gating enable for debug purpose. It should be low for normal operation. Its function is the same as ctrl_clkm_cg_en. If ctrl_clkm_cg_en or clkm_cg_en_sw is high, master DLL clock gating is enabled. 1'b0: PHY master DLL clock gating is disabled. 1'b1: PHY master DLL clock gating is enabled.
22:19	RO	0x0	reserved
18:8	RW	0x001	ctrl_force This field is used instead of ctrl_lock_value[9:0], which represents one DRAM clock period information found by the DLL only when ctrl_dll_on is low. If the DLL is off, this field is used to generate 270 degrees clock and shift DQS by 90 degrees.
7	RW	0x0	ctrl_half_gtlich_mask_ignore 1'b1: Glitch masking ignore using ctrl_half on DVFS 1'b0: Glitch masking using ctrl_half on DVFS
6	RW	0x1	ctrl_start This field is used to start DLL locking. 1'b1: Master DLL locking is enabled. 1'b0: Master DLL reset.
5	RW	0x1	ctrl_dll_on high active start signal to turn on the DLL. This signal should be kept high for normal operation. If this signal becomes low, DLL is turned off. This bit should be kept set before ctrl_start is set to turn on the DLL.
4:1	RW	0xf	ctrl_ref This field determines the period of time when ctrl_locked is cleared. It is used to make ctrl_locked insensitive to clock jitter. 4'b0000: Don't use. 4'b0001: ctrl_flock is de-asserted during 16 clock cycles, ctrl_locked is de-asserted. 4'b0010: ctrl_flock is de-asserted during 24 clock cycles, ctrl_locked is de-asserted. ..... 4'b1110: ctrl_flock is de-asserted during 120 clock cycles, ctrl_locked is de-asserted. 4'b1111: Once ctrl_locked and dfi_init_complete are asserted,

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Bit	Attr	Reset Value	Description
			those won't be de-asserted until rst_n is asserted.
0	RW	0x0	ctrl_half This field controls low speed mode for Master DLL. If this bit is high, DLL can lock at low frequencies (266MHz <= DFI PHY clock frequency <533MHz).

DDRPHY_MDLL_CON1

Address: **Operational Base** + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:21	RO	0x001	ctrl_lock_value_init The reference lock_value for VT compensation, which has been read during the initial training. It is updated when dfi_lvl_periodic = 0 and dfi_rdlvl_gate_en/dfi_rdlvl_wr_en/dfi_rdlvl_en changes from 1'b0 to 1'b1.
20	RO	0x0	ctrl_clock Coarse lock information. According to clock jitter, ctrl_clock can be de-asserted.
19	RO	0x0	ctrl_flock Fine lock information. According to clock jitter, ctrl_flock can be de-asserted.
18	RO	0x0	ctrl_locked DLL stable lock information. This field is set after ctrl_flock is set. This field is cleared when ctrl_flock is de-asserted for some period of time specified by ctrl_ref value. This field is required for stable lock status check.
17	RW	0x0	lock_value_init_override Initial lock_value override mode. 1'b1: ctrl_lock_value_init in read/write mode. If this field is enabled, ctrl_lock_value_init will be written to the PHY internal register. 1'b0: ctrl_lock_value in read only mode. If this field is disabled, internal initial lock value will be read out.
16:11	RO	0x00	reserved
10:0	RO	0x100	ctrl_lock_value Locked delay line encoding value ctrl_lock_value[10:3]: Number of delay cells for coarse lock ctrl_lock_value[2:0]: Control value for fine lock From ctrl_lock_value[10:0], tFS (fine step delay) can be calculated. tFS = tCK / ctrl_lock_value[10:0], fine step delay.

DDRPHY_DVFS_CON

Address: **Operational Base** + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	dvfs_mode DVFS mode select. This field controls which DVFS register sets will be used after frequency change. 2'b00: Normal mode 2'b01: DVFS0 mode 2'b10: DVFS1 mode
29:14	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x1	per_dvfs_train_disable Per DVFS training register control disable 1'b0: SW_RD*, SW_WR*, PRBS_* register value will be applied to internal training code registers when frequency change occurs. 1'b1: PRBS, read and write training register will not be changed when frequency change occurs.
12	RW	0x0	dvfs_fsbst_en Vref Fast boost mode enable during DVFS pause duration. Enable to reduce SOC Vref settling time when SOC Vref level should be changed during DVFS pause. 1'b1: SOC Vref FSBST is enabled. PHY will guarantee that io_zq_ds_vref_fsbst is driven 2'b11 for at least 125ns and then stay at 2'b00 for at least 125ns during frequency change duration via dfi_init_start and dfi_init_complete handshake. 1'b0: io_zq_ds_vref_fsbst will be determined by zq_ds0_vref_fsbst and zq_ds1_vref_fsbst.
11:0	RW	0x640	freq_train DFI PHY clock frequency for the initial training (Read/Write/Gate training/Write levelling/CBT). It is used as a reference for VT compensation and frequency offset compensation. Initial training should be done only at the highest frequency. Ex) if the highest frequency is 1600MHz, freq_train should be set to 'd1600. This field should not change during the normal operation.

DDRPHY_DVFS0_CON0

Address: **Operational Base** + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:20	RW	0x640	dvfs0_freq DFI PHY clock frequency for DVFS0 mode. This field must be properly set to increase data eye margin.
19:14	RW	0x20	dvfs0_rdlat_rank0 This field will be used instead of ctrl_rdlat_rank0 during DVFS0 mode.
13	RW	0x0	dvfs0_twpre Write preamble length for DVFS0 mode. It will be used instead of ctrl_twpre in DVFS0 mode. 1'b0: 2 tCK for higher speeds 1'b1: 1 tCK for lower speeds
12	RW	0x0	dvfs0_rpre_opt Read pre-amble toggle option for DVFS0 mode. It will be used instead of ctrl_rpre_opt in DVFS0 mode. 1'b1: Read pre-amble = 2nCK toggle. 1'b0: Read pre-amble = 2nCK static.
11	RW	0x1	dvfs0_wr_per_rank_en Per rank write DQ/DM DLL control enable in DVFS0 mode. It will be used instead of wr_per_rank_en in DVFS0 mode.
10	RW	0x1	dvfs0_rd_per_rank_en Per rank read DQS/DQ/DM DLL control enable in DVFS0 mode. It will be used instead of rd_per_rank_en in DVFS0 mode.
9	RW	0x0	dvfs0_freq_offset_en Frequency offset calculation enable in DVFS0 mode. It should be set to 1'b0 if DLL is off because the frequency compensation offset will be calculated using the current DLL lock value.
8	RW	0x0	dvfs0_auto_dqs_clean Enable Auto-DQS-Clean mode in DVFS0 mode

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Bit	Attr	Reset Value	Description
7	RW	0x0	dvfs0_glitch_removal_en This field is used for postamble glitch removal enable during Auto-DQS-Clean Mode in DVFS0 mode. 1'b0: Glitch removal disable 1'b1: Glitch removal enable
6:5	RW	0x0	dvfs0_rpost_opt Read post-amble toggle option for DVFS0 mode. It will be used instead of ctrl_rpost_opt in DVFS0 mode. 2'b00: Read pre-amble = 0.5tWCK static. 2'b01: Read pre-amble = 2.5tWCK static. 2'b10: Read pre-amble = 4.5tWCK static.
4	RW	0x0	dvfs0_cbt_en LPDDR5 CBT mode enable for DVFS0 mode
3	RO	0x0	reserved
2	RW	0x1	dvfs0_rdtrn_dbi_cal_en DBI enable for LPDDR4 read training in DVFS0. 1'b0: DBI is not calibrated during read training. 1'b1: DBI is calibrated during read training.
1	RW	0x1	dvfs0_wrtrn_dbi_cal_en DBI enable for LPDDR4 write training in DVFS0. Set to 0 if Data Mask, Write DBI and Read DBI are all disabled at DRAM. Otherwise, it should be set to 1. 1'b0: DBI is not calibrated during write training. 1'b1: DBI is calibrated during write training.
0	RW	0x0	dvfs0_LP5_16bank_mode LP5 16bank mode 1'b1: 16bank mode 1'b0: 4bg/4bank mode 8 bank mode don't care about this field.

DDRPHY_DVFS1_CON0

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RW	0x640	dvfs1_freq DFI PHY clock frequency for DVFS1 mode. This field must be properly set to increase data eye margin.
19:14	RW	0x20	dvfs1_rdlat_rank0 This field will be used instead of ctrl_rdlat_rank0 during DVFS1 mode.
13	RW	0x0	dvfs1_twpre Write preamble length for DVFS1 mode. It will be used instead of ctrl_twpre in DVFS1 mode. 1'b0: 2 tCK for higher speeds 1'b1: 1 tCK for lower speeds
12	RW	0x0	dvfs1_rpre_opt Read pre-amble toggle option for DVFS1 mode. It will be used instead of ctrl_rpre_opt in DVFS1 mode. 1'b1: Read pre-amble = 2nCK toggle 1'b0: Read pre-amble = 2nCK static
11	RW	0x1	dvfs1_wr_per_rank_en Per rank write DQ/DM DLL control enable in DVFS1 mode. It will be used instead of wr_per_rank_en in DVFS1 mode.
10	RW	0x1	dvfs1_rd_per_rank_en Per rank read DQS/DQ/DM DLL control enable in DVFS1 mode. It will be used instead of rd_per_rank_en in DVFS1 mode.

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Bit	Attr	Reset Value	Description
9	RW	0x0	dvfs1_freq_offset_en Frequency offset calculation enable in DVFS1 mode. It should be set to 1'b0 if DLL is off because the frequency compensation offset will be calculated using the current DLL lock value.
8	RW	0x0	dvfs1_auto_dqs_clean Enable Auto-DQS-Clean mode in DVFS1 mode
7	RW	0x0	dvfs1_glitch_removal_en This field is used for postamble glitch removal enable during Auto-DQS-Clean Mode in DVFS1 mode. 1'b0: Glitch removal disable 1'b1: Glitch removal enable
6:5	RW	0x0	dvfs1_rpost_opt Read post-amble toggle option for DVFS1 mode. It will be used instead of ctrl_rpost_opt in DVFS1 mode. 2'b00: Read pre-amble = 0.5tWCK static. 2'b01: Read pre-amble = 2.5tWCK static. 2'b10: Read pre-amble = 4.5tWCK static.
4	RW	0x0	dvfs1_cbt_en LPDDR5 CBT mode enable for DVFS1 mode
3	RO	0x0	reserved
2	RW	0x1	dvfs1_rdtrn_dbi_cal_en DBI enable for LPDDR4 read training in DVFS1. 1'b0: DBI is not calibrated during read training. 1'b1: DBI is calibrated during read training.
1	RW	0x1	dvfs1_wrtrn_dbi_cal_en DBI enable for LPDDR4 write training in DVFS1. Set to 0 if data mask, write DBI and read DBI are all disabled at DRAM. Otherwise, it should be set to 1. 1'b0: DBI is not calibrated during write training. 1'b1: DBI is calibrated during write training.
0	RW	0x0	dvfs1_LP5_16bank_mode LP5 16bank mode in DVFS1 mode 1'b1: 16bank mode 1'b0: 4bg/4bank mode 8 bank mode don't care about this field.

DDRPHY_DVFS0_CON1

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31	RW	0x0	dvfs0_dll_on DLL on/off control during DVFS0 mode. It will be used instead of ctrl_dll_on during DVFS0 mode.
30	RW	0x0	dvfs0_half Low frequency locking enable. It will be used instead of ctrl_half during DVFS0 mode.
29:28	RW	0x3	dvfs0_wck_phy_cg_en_ignore This field support to ignore phy_cg_en for WCK at WCK free running mode in DVFS0. This field should be controlled at WCK free running mode. [27]: Byte1 control [26]: Byte0 control 1'b1: Ignore phy_cg_en control for WCK. 1'b0: WCK is controlled by phy_cg_en.
27:26	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
25:18	RW	0x20	dvfs0_start_point Initial DLL lock start point in DVFS0 mode.
17:9	RW	0x000	dvfs0_offsetr This field will be used instead of ctrl_offsetr* during DVFS0 mode. dvfs0_offsetr[7] = 1: (tFS: fine step delay) Read delay amount dvfs0_offsetr[6:0] x tFS dvfs0_offsetr[7] = 0: Read delay amount dvfs0_offsetr[6:0] x tFS Note that "ctrl_force/4" will be the base DLL code for read path if DLL is off and read training is disabled.
8:0	RW	0x000	dvfs0_offsetw Deprecated

DDRPHY_DVFS1_CON1

Address: **Operational Base** + offset (0x00C8)

Bit	Attr	Reset Value	Description
31	RW	0x0	dvfs1_dll_on DLL on/off control during DVFS1 mode. It will be used instead of ctrl_dll_on during DVFS1 mode.
30	RW	0x0	dvfs1_half Low frequency locking enable. It will be used instead of ctrl_half during DVFS1 mode.
29:28	RW	0x3	dvfs1_wck_phy_cg_en_ignore This field support to ignore phy_cg_en for WCK at WCK free running mode in DVFS1. This field should be controlled at WCK free running mode. [27]: Byte1 control [26]: Byte0 control 1'b1: Ignore phy_cg_en control for WCK. 1'b0: WCK is controlled by phy_cg_en.
27:26	RO	0x0	reserved
25:18	RW	0x20	dvfs1_start_point Initial DLL lock start point in DVFS1 mode
17:9	RW	0x000	dvfs1_offsetr This field will be used instead of ctrl_offsetr* during DVFS1 mode. dvfs1_offsetr[7] = 1: (tFS: fine step delay) Read delay amount dvfs1_offsetr[6:0] x tFS dvfs1_offsetr[7] = 0: Read delay amount dvfs1_offsetr[6:0] x tFS Note that "ctrl_force/4" will be the base DLL code for read path if DLL is off and read training is disabled.
8:0	RW	0x000	dvfs1_offsetw Deprecated

DDRPHY_DVFS0_CON2

Address: **Operational Base** + offset (0x00CC)

Bit	Attr	Reset Value	Description
31	RW	0x0	dvfs0_cmosrcv This field will control I/O receiver mode instead of ctrl_cmosrcv during DVFS0 mode.

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Bit	Attr	Reset Value	Description
30	RW	0x1	dvfs0_dfdqs Differential receiver mode enable This field will be used instead of ctrl_dfdqs in DVFS0 mode. 1'b0: Single-ended DQS 1'b1: Differential DQS
29	RW	0x1	dvfs0_rodt_disable Read ODT (On-Die-Termination) disable signal during DVFS0 mode. It will be used instead of ctrl_rodt_disable during DVFS0 mode. 1'b1: Read ODT disabled. Drive ctrl_read_p* to 0. If using LPDDR4, ctrl_read_p* will be always 0 by enabling this field (io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are low). 1'b0: Read ODT enabled. Drive ctrl_read_p* normally (io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are high only for read duration).
28	RW	0x0	dvfs0_write_se_dqs Single ended mode enable for write DQS. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for Write DQS. 1'b1: Single ended mode is enabled for Write DQS. Caution: dvfs0_write_se_ck should be enabled using dvfs0_write_se_dqs in LPDDR4.
27	RW	0x0	dvfs0_write_se_ck Single ended mode enable for CK. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for CK. 1'b1: Single ended mode is enabled for CK. Caution: dvfs0_write_se_dqs should be enabled using dvfs0_write_se_ck in LPDDR4. Caution: dvfs0_write_se_wck should be enabled using dvfs0_write_se_ck in LPDDR5.
26	RW	0x0	dvfs0_write_se_wck Single ended mode enable for LP5 WCK. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for WCK. 1'b1: Single ended mode is enabled for WCK. Caution: dvfs0_write_se_ck should be enabled using dvfs0_write_se_wck in LPDDR5.
25:24	RW	0x0	dvfs0_pulld_dqs pull-up or down PDQS/NDQS signal control in DVFS0 mode. It will be used instead of ctrl_pulld_dqs in DVFS0 mode. Please refer to ctrl_pulld_dqs description.
23	RW	0x0	dvfs0_gateduradj_ext Default value is 0. This field is used for extend control range of dvfs0_gateduradj value. dvfs0_gateduradj_ext = 1'b0 (default) => Non Extended dvfs0_gateduradj_ext = 1'b1 => dvfs0_gateduradj[2:0] + 'h8
22	RW	0x0	dvfs0_gateadj_ext Default value is 0. This field is used for extend control range of dvfs0_gateadj value. dvfs0_gateadj_ext = 1'b0 (default) => Non Extended dvfs0_gateadj_ext = 1'b1 => dvfs0_gateadj[2:0] + 'h8

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Bit	Attr	Reset Value	Description
21	RW	0x0	dvfs0_readduradj_ext Default value is 0. This field is used for extend control range of dvfs0_readduradj value. dvfs0_readduradj_ext = 1'b0 (default) => Non Extended dvfs0_readduradj_ext = 1'b1 => dvfs0_readduradj[2:0] + 'h8
20	RW	0x0	dvfs0_readadj_ext Default value is 0. This field is used for extend control range of dvfs0_readadj value. dvfs0_readadj_ext = 1'b0 (default) => Non Extended dvfs0_readadj_ext = 1'b1 => dvfs0_readadj[2:0] + 'h8
19	RO	0x0	reserved
18:17	RW	0x3	dvfs0_ndqs_maskdur_adj Single-ended NDQS input glitch masking duration adjustment during read ODT enable timing in DVFS0 mode. 2'b11: SE NDQS glitch 3.5tCK masking (default) 2'b10: SE NDQS glitch 4.5tCK masking 2'b00: SE NDQS glitch 5.5tCK masking
16	RW	0x0	dvfs0_shgate Gate signal control in DVFS0 mode. It will be used instead of ctrl_shgate in DVFS0 mode. For LPDDR4, MR1 should be programmed so that read pre-amble is 2nCK static and read post-amble is 0.5tCK when shgate is 'h0.
15:12	RW	0x2	dvfs0_gateduradj This field will be used instead of ctrl_gateduradj during DVFS0 mode.
11:8	RW	0x0	dvfs0_gateadj This field will be used instead of ctrl_gateadj during DVFS0 mode.
7:4	RW	0x0	dvfs0_readduradj It adjusts the duration cycle of "ctrl_read" on a clock cycle base in DVFS0 mode. MSB (bit3) controls direction: 1'b1: Subtract delay 1'b0: Add delay Bit[2:0] set delay value. It determines the high duration of io_pdqs_read, io_ndqs_read, io_dq_read and io_dm_read if ctrl_rodt_disable is 0.
3:0	RW	0x1	dvfs0_readadj It adjusts the enable time of "ctrl_read" on a clock cycle base in DVFS0 mode. MSB (bit3) controls direction: 1'b1: Subtract delay 1'b0: Add delay Bit[2:0] set delay value. It determines the start cycle of high duration of io_pdqs_read, io_ndqs_read, io_dq_read and io_dm_read if ctrl_rodt_disable is 0.

DDRPHY_DVFS1_CON2

Address: **Operational Base** + offset (0x00D0)

Bit	Attr	Reset Value	Description
31	RW	0x0	dvfs1_cmosrcv This field will control I/O receiver mode instead of ctrl_cmosrcv during DVFS1 mode.

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Bit	Attr	Reset Value	Description
30	RW	0x1	dvfs1_dfdqs Differential receiver mode enable This field will be used instead of ctrl_dfdqs in DVFS1 mode. 1'b0: Single-ended DQS 1'b1: Differential DQS
29	RW	0x1	dvfs1_rodt_disable Read ODT (On-Die-Termination) disable signal during DVFS1 mode. It will be used instead of ctrl_rodt_disable during DVFS1 mode. 1'b1: Read ODT disabled. Drive ctrl_read_p* to 0. If using LPDDR4, ctrl_read_p* will be always 0 by enabling this field (io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are low). 1'b0: Read ODT enabled. Drive ctrl_read_p* normally (io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are high only for read duration).
28	RW	0x0	dvfs1_write_se_dqs Single ended mode enable for write DQS. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for Write DQS. 1'b1: Single ended mode is enabled for Write DQS. Caution: dvfs1_write_se_ck should be enabled using dvfs1_write_se_dqs in LPDDR4.
27	RW	0x0	dvfs1_write_se_ck Single ended mode enable for CK. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for CK. 1'b1: Single ended mode is enabled for CK. Caution: dvfs1_write_se_dqs should be enabled using dvfs1_write_se_ck in LPDDR4. Caution: dvfs1_write_se_wck should be enabled using dvfs1_write_se_ck in LPDDR5.
26	RW	0x0	dvfs1_write_se_wck Single ended mode enable for LP5 WCK. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for WCK. 1'b1: Single ended mode is enabled for WCK. Caution: dvfs1_write_se_ck should be enabled using dvfs1_write_se_wck in LPDDR5.
25:24	RW	0x0	dvfs1_pulld_dqs pull-up or down PDQS/NDQS signal control in DVFS1 mode. It will be used instead of ctrl_pulld_dqs in DVFS0 mode. Please refer to ctrl_pulld_dqs description.
23	RW	0x0	dvfs1_gateduradj_ext Default value is 0. This field is used for extend control range of dvfs1_gateduradj value. dvfs1_gateduradj_ext = 1'b0 (default) => Non Extended dvfs1_gateduradj_ext = 1'b1 => dvfs1_gateduradj[2:0] + 'h8
22	RW	0x0	dvfs1_gateadj_ext Default value is 0. This field is used for extend control range of dvfs1_gateadj value. dvfs1_gateadj_ext = 1'b0 (default) => Non Extended dvfs1_gateadj_ext = 1'b1 => dvfs1_gateadj[2:0] + 'h8

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Bit	Attr	Reset Value	Description
21	RW	0x0	dvfs1_readduradj_ext Default value is 0. This field is used for extend control range of dvfs1_readduradj value. dvfs1_readduradj_ext = 1'b0 (default) => Non Extended dvfs1_readduradj_ext = 1'b1 => dvfs1_readduradj[2:0] + 'h8
20	RW	0x0	dvfs1_readadj_ext Default value is 0. This field is used for extend control range of dvfs1_readadj value. dvfs1_readadj_ext = 1'b0 (default) => Non Extended dvfs1_readadj_ext = 1'b1 => dvfs1_readadj[2:0] + 'h8
19	RO	0x0	reserved
18:17	RW	0x3	dvfs1_ndqs_maskdur_adj Single-ended NDQS input glitch masking duration adjustment during read ODT enable timing in DVFS1 mode. 2'b11: SE NDQS glitch 3.5tCK masking (default) 2'b10: SE NDQS glitch 4.5tCK masking 2'b00: SE NDQS glitch 5.5tCK masking
16	RW	0x0	dvfs1_shgate Gate signal control in DVFS1 mode. It will be used instead of ctrl_shgate in DVFS1 mode. For LPDDR4, MR1 should be programmed so that read pre-amble is 2nCK static and read post-amble is 0.5tCK when shgate is 'h0.
15:12	RW	0x2	dvfs1_gateduradj This field will be used instead of ctrl_gateduradj during DVFS1 mode.
11:8	RW	0x0	dvfs1_gateadj This field will be used instead of ctrl_gateadj during DVFS1 mode.
7:4	RW	0x0	dvfs1_readduradj It adjusts the duration cycle of "ctrl_read" on a clock cycle base in DVFS1 mode. MSB (bit3) controls direction: 1'b1: Subtract delay 1'b0: Add delay Bit[2:0] set delay value. It determines the high duration of io_pdqs_read, io_ndqs_read, io_dq_read and io_dm_read if ctrl_rodt_disable is 0.
3:0	RW	0x1	dvfs1_readadj It adjusts the enable time of "ctrl_read" on a clock cycle base in DVFS1 mode. MSB (bit3) controls direction: 1'b1: Subtract delay 1'b0: Add delay Bit[2:0] set delay value. It determines the start cycle of high duration of io_pdqs_read, io_ndqs_read, io_dq_read and io_dm_read if ctrl_rodt_disable is 0.

DDRPHY_DVFS0_CON3

Address: **Operational Base** + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	dvfs0_ds1_vref Vref control for data slice 1 in the internal mode during DVFS0 mode. It will be used instead of zq_ds1_vref in DVFS0 mode. It controls io_zq_ds_vref[11:6] in DVFS0 mode.

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Bit	Attr	Reset Value	Description
25:20	RW	0x00	dvfs0_ds0_vref Vref control for data slice 0 in the internal mode during DVFS0 mode. It will be used instead of zq_ds0_vref in DVFS0 mode. It controls io_zq_ds_vref[5:0] in DVFS0 mode.
19:18	RO	0x0	reserved
17:15	RW	0x7	dvfs0_zq_mode_dds Driver pull-down strength control for ctrl slice in DVFS0 mode. It controls io_zq_mode_dds in DVFS0 mode.
14:12	RW	0x7	dvfs0_zq_mode_pdds Driver pull-up strength control for ctrl slice in DVFS0 mode. It controls io_zq_mode_pdds in DVFS0 mode.
11:9	RW	0x7	dvfs0_zq_ds1_dds Driver pull-down strength control for data slice 1 in DVFS0 mode. It controls io_zq_ds_dds[5:3] in DVFS0 mode.
8:6	RW	0x7	dvfs0_zq_ds1_pdds Driver pull-up strength control for data slice 1 in DVFS0 mode. It controls io_zq_ds_pdds[5:3] in DVFS0 mode.
5:3	RW	0x7	dvfs0_zq_ds0_dds Driver pull-down strength control for data slice 0 in DVFS0 mode. It controls io_zq_ds_dds[2:0] in DVFS0 mode.
2:0	RW	0x7	dvfs0_zq_ds0_pdds Driver pull-up strength control for data slice 0 in DVFS0 mode. It controls io_zq_ds_pdds[2:0] in DVFS0 mode.

DDRPHY_DVFS1_CON3

Address: **Operational Base** + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	dvfs1_ds1_vref Vref control for data slice 1 in the internal mode during DVFS1 mode. It will be used instead of zq_ds1_vref in DVFS1 mode. It controls io_zq_ds_vref[11:6] in DVFS1 mode.
25:20	RW	0x00	dvfs1_ds0_vref Vref control for data slice 0 in the internal mode during DVFS1 mode. It will be used instead of zq_ds0_vref in DVFS1 mode. It controls io_zq_ds_vref[5:0] in DVFS1 mode.
19:18	RO	0x0	reserved
17:15	RW	0x7	dvfs1_zq_mode_dds Driver pull-down strength control for ctrl slice in DVFS1 mode. It controls io_zq_mode_dds in DVFS1 mode.
14:12	RW	0x7	dvfs1_zq_mode_pdds Driver pull-up strength control for ctrl slice in DVFS1 mode. It controls io_zq_mode_pdds in DVFS1 mode.
11:9	RW	0x7	dvfs1_zq_ds1_dds Driver pull-down strength control for data slice 1 in DVFS1 mode. It controls io_zq_ds_dds[5:3] in DVFS1 mode.
8:6	RW	0x7	dvfs1_zq_ds1_pdds Driver pull-up strength control for data slice 1 in DVFS1 mode. It controls io_zq_ds_pdds[5:3] in DVFS1 mode.
5:3	RW	0x7	dvfs1_zq_ds0_dds Driver pull-down strength control for data slice 0 in DVFS1 mode. It controls io_zq_ds_dds[2:0] in DVFS1 mode.
2:0	RW	0x7	dvfs1_zq_ds0_pdds Driver pull-up strength control for data slice 0 in DVFS1 mode. It controls io_zq_ds_pdds[2:0] in DVFS1 mode.

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DDRPHY_DVFS0_CON4

Address: **Operational Base** + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:19	RW	0x4	dvfs0_zq_ds1_term On-die-termination (ODT) resistor value selection for data slice 1 in DVFS0 mode. It determines io_zq_ds_mode_term[5:3]. 3'b100: 60 ohm far end VSSQ termination 3'b010: 120 ohm far end VSSQ termination 3'b001: 240 ohm far end VSSQ termination
18:16	RW	0x4	dvfs0_zq_ds0_term On-die-termination (ODT) resistor value selection for data slice 0 in DVFS0 mode. It determines io_zq_ds_mode_term[2:0]. 3'b100: 60 ohm far end VSSQ termination 3'b010: 120 ohm far end VSSQ termination 3'b001: 240 ohm far end VSSQ termination
15:14	RO	0x0	reserved
13:8	RW	0x3f	vt_dvfs0_mcupd_req_cycle MC initiated mode update request cycle in DVFS0 mode for cs_phyupd FSM
7:6	RO	0x0	reserved
5:0	RW	0x3f	vt_dvfs0_phyupd_req_cycle PHY initiated mode update request cycle in DVFS0 mode for cs_phyupd FSM

DDRPHY_DVFS1_CON4

Address: **Operational Base** + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:19	RW	0x4	dvfs1_zq_ds1_term On-die-termination (ODT) resistor value selection for data slice 1 in DVFS1 mode. It determines io_zq_ds_mode_term[5:3]. 3'b100: 60 ohm far end VSSQ termination 3'b010: 120 ohm far end VSSQ termination 3'b001: 240 ohm far end VSSQ termination
18:16	RW	0x4	dvfs1_zq_ds0_term On-die-termination (ODT) resistor value selection for data slice 0 in DVFS1 mode. It determines io_zq_ds_mode_term[2:0]. 3'b100: 60 ohm far end VSSQ termination 3'b010: 120 ohm far end VSSQ termination 3'b001: 240 ohm far end VSSQ termination
15:14	RO	0x0	reserved
13:8	RW	0x3f	vt_dvfs1_mcupd_req_cycle MC initiated mode update request cycle in DVFS1 mode for cs_phyupd FSM
7:6	RO	0x0	reserved
5:0	RW	0x3f	vt_dvfs1_phyupd_req_cycle PHY initiated mode update request cycle in DVFS1 mode for cs_phyupd FSM

DDRPHY_CAL_WRLVL_STAT

Address: **Operational Base** + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17:16	RO	0x0	wrlvl_fail_status It will be enabled if there is no pass period after write levelling. It should be read by zero if levelling is done normally. wrlvl_fail_status[1]: For data slice 1 wrlvl_fail_status[0]: For data slice 0
15:0	RO	0x0000	reserved

DDRPHY_CAL_FAIL_STAT0

Address: **Operational Base** + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	dq_fail_status1 It will be enabled if there is no pass period after read or write DQ calibration. It should be read by zero if calibration is done normally. The result is for data slice 1.
7:0	RO	0x00	dq_fail_status0 It will be enabled if there is no pass period after read or write DQ calibration. It should be read by zero if calibration is done normally. The result is for data slice 0.

DDRPHY_CAL_FAIL_STAT1

Address: **Operational Base** + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RO	0x0	dm_fail_status It will be enabled if there is no pass period after read or write DM calibration. It should be read by zero if calibration is done normally. [1]: DM fail status for slice 1 [0]: DM fail status for slice 0

DDRPHY_CAL_GT_CS0_VWMC0

Address: **Operational Base** + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	GT_VWMC1_cs0 Gate training code for data slice 1. It shows the number of fine step delay cells applied to gate signal after gate training.
15:10	RO	0x00	reserved
9:0	RO	0x000	GT_VWMC0_cs0 Gate training code for data slice 0. It shows the number of fine step delay cells applied to gate signal after gate training.

DDRPHY_CAL_GT_CS0_CYC

Address: **Operational Base** + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RO	0x0	GT_CYC1_cs0 Gate training cycle increment information for data slice 1. It represents how much ctrl_gate signal is delayed by DFI PHY clock cycle.
7:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	GT_CYC0_cs0 Gate training cycle increment information for data slice 0. It represents how much ctrl_gate signal is delayed by DFI PHY clock cycle.

DDRPHY_CAL_RD_VWMC0

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	rd_vwmc1 Read DQ calibration center code for data slice 1. It shows the information for the bit with the maximum center value between DQ[15:8].
15:10	RO	0x00	reserved
9:0	RO	0x000	rd_vwmc0 Read DQ calibration center code for data slice 0. It shows the information for the bit with the maximum center value between DQ[7:0].

DDRPHY_CAL_RD_VWML0

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	rd_vwml1 Left code value in read valid window margin for data slice 1. It shows the information for the bit with the maximum center value between DQ[15:8].
15:10	RO	0x00	reserved
9:0	RO	0x000	rd_vwml0 Left code value in read valid window margin for data slice 0. It shows the information for the bit with the maximum center value between DQ[7:0].

DDRPHY_CAL_RD_VWMR0

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	rd_vwmr1 Right code value in read valid window margin for data slice 1. It shows the information for the bit with the maximum center value between DQ[15:8].
15:10	RO	0x00	reserved
9:0	RO	0x000	rd_vwmr0 Right code value in read valid window margin for data slice 0. It shows the information for the bit with the maximum center value between DQ[7:0].

DDRPHY_CAL_WR_VWMC0

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	wr_vwmc1 Write DQ calibration center code for data slice 1. It shows the information for the bit with minimum center code between DQ[15:8] and DM[1].

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Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RO	0x000	wr_vwmc0 Write DQ calibration center code for data slice 0. It shows the information for the bit with minimum center code between DQ[7:0] and DM[0].

DDRPHY_CAL_WR_VWML0

Address: **Operational Base** + offset (0x0140)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	wr_vwml1 Left code value in write valid window margin for data slice 1. It shows the information for the bit with minimum center code between DQ[15:8] and DM[1].
15:11	RO	0x00	reserved
10:0	RO	0x000	wr_vwml0 Left code value in write valid window margin for data slice 0. It shows the information for the bit with minimum center code between DQ[7:0] and DM[0].

DDRPHY_CAL_WR_VWMR0

Address: **Operational Base** + offset (0x0150)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	wr_vwmr1 Right code value in write valid window margin for data slice 1. It shows the information for the bit with minimum center code between DQ[15:8] and DM[1].
15:11	RO	0x00	reserved
10:0	RO	0x000	wr_vwmr0 Right code value in write valid window margin for data slice 0. It shows the information for the bit with minimum center code between DQ[7:0] and DM[0].

DDRPHY_CAL_CON5

Address: **Operational Base** + offset (0x0160)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	binary_en This feature is TBD.
9:2	RW	0x00	wrtrn_cyc_th Write training cycle threshold. This is the minimum amount of delay line offset to determine cycle based delay on DQ/DM. For example, the first write training is completed with cycle = 1 and offset = 10 and wrtrn_cyc_th = 15. Because offset < wrtrn_cyc_th, PHY determines that cycle based delay should be reverted to 0, instead of 1. For the second write training cycle will be fixed to 0 and write training will progress increasing delay line code only. This is to guarantee the non-linearity cause by cycle delay not affect training result.

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Bit	Attr	Reset Value	Description
1	RW	0x0	wrtrn_cyc_en Write training cycle delay enable. If enabled, cycle based latency will be used along with DQ/DM delay line (cycle delay = 0.5/1.0/1.5tCK). Enable this field for LPDDR4. It will reduce the VT calculation error caused by lock value variation as DQ/DM offset is reduced. Disable for other DRAM types.
0	RW	0x0	wrtrn_cyc_mode Cycle based write training mode 1'b0: Cycle code for left edge and right edge are matched. This improves accuracy in training result but with limited training range (1GHz or over). 1'b1: Cycle code for left edge and right edge are not matched. Use for low frequencies (500MHz~1GHz).

DDRPHY_DVFS_UPD_CON0

Address: **Operational Base** + offset (0x0164)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x3f	dvfs_mcupd_req_cycle For debug purpose. For mc-initiated update mode. It controls the number of cycle during which cs_dvfsupd FSM stays at ST_DVFS_C_VTC state.
15:14	RO	0x0	reserved
13:8	RW	0x3f	dvfs_dvfs0_mcupd_req_cycle MC initiated mode update request cycle in DVFS0 mode for cs_dvfsupd FSM
7:6	RO	0x0	reserved
5:0	RW	0x3f	dvfs_dvfs1_mcupd_req_cycle MC initiated mode update request cycle in DVFS1 mode for cs_dvfsupd FSM

DDRPHY_DVFS_UPD_CON1

Address: **Operational Base** + offset (0x0168)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x3f	dvfs_phyupd_req_cycle For debug purpose. For phy-initated update mode. It controls the number of cycle during which cs_dvfsupd FSM stays at ST_DVFS_C_VTC state.
15:14	RO	0x0	reserved
13:8	RW	0x3f	dvfs_dvfs0_phyupd_req_cycle PHY initiated mode update request cycle in DVFS0 mode for cs_dvfsupd FSM
7:6	RO	0x0	reserved
5:0	RW	0x3f	dvfs_dvfs1_phyupd_req_cycle PHY initiated mode update request cycle in DVFS1 mode for cs_dvfsupd FSM

DDRPHY_RD_DESKEW_CENTER_CS0_CON_DM

Address: **Operational Base** + offset (0x018C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RDDMDeskewC1_cs0 Read DMI de-skew center code for data slice 1
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	RDDMDeskewC0_cs0 Read DMI de-skew center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS0_CON0

Address: **Operational Base** + offset (0x0190)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD0DeskewC1_cs0 Read DQ0 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD0DeskewC0_cs0 Read DQ0 de-skew center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS0_CON1

Address: **Operational Base** + offset (0x019C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD1DeskewC1_cs0 Read DQ1 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD1DeskewC0_cs0 Read DQ1 de-skew center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS0_CON2

Address: **Operational Base** + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD2DeskewC1_cs0 Read DQ2 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD2DeskewC0_cs0 Read DQ2 de-skew center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS0_CON3

Address: **Operational Base** + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD3DeskewC1_cs0 Read DQ3 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD3DeskewC0_cs0 Read DQ3 de-skew center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS0_CON4

Address: **Operational Base** + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD4DeskewC1_cs0 Read DQ4 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD4DeskewC0_cs0 Read DQ4 de-skew center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS0_CON5

Address: **Operational Base** + offset (0x01CC)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD5DeskewC1_cs0 Read DQ5 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD5DeskewC0_cs0 Read DQ5 de-skew center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS0_CON6

Address: **Operational Base** + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD6DeskewC1_cs0 Read DQ6 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD6DeskewC0_cs0 Read DQ6 de-skew center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS0_CON7

Address: **Operational Base** + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD7DeskewC1_cs0 Read DQ7 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD7DeskewC0_cs0 Read DQ7 de-skew center code for data slice 0

DDRPHY_WR_DESKEWC_CS0_CON0

Address: **Operational Base** + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR0DeskewC1_cs0 Write DQ0 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR0DeskewC0_cs0 Write DQ0 de-skew center code for data slice 0

DDRPHY_WR_DESKEWC_CS0_CON1

Address: **Operational Base** + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR1DeskewC1_cs0 Write DQ1 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR1DeskewC0_cs0 Write DQ1 de-skew center code for data slice 0

DDRPHY_WR_DESKEWC_CS0_CON2

Address: **Operational Base** + offset (0x0208)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR2DeskewC1_cs0 Write DQ2 de-skew center code for data slice 1
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	WR2DeskewC0_cs0 Write DQ2 de-skew center code for data slice 0

DDRPHY_WR_DESKEWC_CS0_CON3

Address: **Operational Base** + offset (0x0214)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR3DeskewC1_cs0 Write DQ3 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR3DeskewC0_cs0 Write DQ3 de-skew center code for data slice 0

DDRPHY_WR_DESKEWC_CS0_CON4

Address: **Operational Base** + offset (0x0220)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR4DeskewC1_cs0 Write DQ4 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR4DeskewC0_cs0 Write DQ4 de-skew center code for data slice 0

DDRPHY_WR_DESKEWC_CS0_CON5

Address: **Operational Base** + offset (0x022C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR5DeskewC1_cs0 Write DQ5 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR5DeskewC0_cs0 Write DQ5 de-skew center code for data slice 0

DDRPHY_WR_DESKEWC_CS0_CON6

Address: **Operational Base** + offset (0x0238)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR6DeskewC1_cs0 Write DQ6 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR6DeskewC0_cs0 Write DQ6 de-skew center code for data slice 0

DDRPHY_WR_DESKEWC_CS0_CON7

Address: **Operational Base** + offset (0x0244)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR7DeskewC1_cs0 Write DQ7 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR7DeskewC0_cs0 Write DQ7 de-skew center code for data slice 0

DDRPHY_DM_DESKEWC_CS0_CON0

Address: **Operational Base** + offset (0x0250)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	DMDeskewC1_cs0 Write DM de-skew center code for data slice 1. It will be the same as dm_vwmc1 right after the initial write training is done.
15:10	RO	0x00	reserved
9:0	RO	0x000	DMDeskewC0_cs0 Write DM de-skew center code for data slice 0. It will be the same as dm_vwmc0 right after the initial write training is done.

DDRPHY_VWMC_STAT0

Address: **Operational Base** + offset (0x025C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D0_VWMC1 DQ0 center code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D0_VWMC0 DQ0 center code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWMC_STAT3

Address: **Operational Base** + offset (0x0268)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D1_VWMC1 DQ1 center code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D1_VWMC0 DQ1 center code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWMC_STAT6

Address: **Operational Base** + offset (0x0274)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D2_VWMC1 DQ2 center code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D2_VWMC0 DQ2 center code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWMC_STAT9

Address: **Operational Base** + offset (0x0280)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D3_VWMC1 DQ3 center code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:0	RO	0x000	D3_VWMC0 DQ3 center code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWMC_STAT12

Address: **Operational Base** + offset (0x028C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D4_VWMC1 DQ4 center code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D4_VWMC0 DQ4 center code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWMC_STAT15

Address: **Operational Base** + offset (0x0298)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D5_VWMC1 DQ5 center code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D5_VWMC0 DQ5 center code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWMC_STAT18

Address: **Operational Base** + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D6_VWMC1 DQ6 center code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D6_VWMC0 DQ6 center code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWMC_STAT21

Address: **Operational Base** + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D7_VWMC1 DQ7 center code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D7_VWMC0 DQ7 center code for data slice 0. The latest read or write training result will be shown.

DDRPHY_DM_VWMC_STAT0

Address: **Operational Base** + offset (0x02BC)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	DM_VWMC1 DM center code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	DM_VWMC0 DM center code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT0

Address: **Operational Base** + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D0_VWML1 DQ0 left code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D0_VWML0 DQ0 left code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT3

Address: **Operational Base** + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D1_VWML1 DQ1 left code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D1_VWML0 DQ1 left code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT6

Address: **Operational Base** + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D2_VWML1 DQ2 left code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D2_VWML0 DQ2 left code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT9

Address: **Operational Base** + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D3_VWML1 DQ3 left code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:0	RO	0x000	D3_VWML0 DQ3 left code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT12

Address: **Operational Base** + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D4_VWML1 DQ4 left code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D4_VWML0 DQ4 left code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT15

Address: **Operational Base** + offset (0x0304)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D5_VWML1 DQ5 left code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D5_VWML0 DQ5 left code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT18

Address: **Operational Base** + offset (0x0310)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D6_VWML1 DQ6 left code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D6_VWML0 DQ6 left code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT21

Address: **Operational Base** + offset (0x031C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D7_VWML1 DQ7 left code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D7_VWML0 DQ7 left code for data slice 0. The latest read or write training result will be shown.

DDRPHY_DM_VWML_STAT0

Address: **Operational Base** + offset (0x0328)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	DM_VWML1 DM left code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	DM_VWML0 DM left code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT0

Address: **Operational Base** + offset (0x0334)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D0_VWMR1 DQ0 right code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D0_VWMR0 DQ0 right code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT3

Address: **Operational Base** + offset (0x0340)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D1_VWMR1 DQ1 right code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D1_VWMR0 DQ1 right code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT6

Address: **Operational Base** + offset (0x034C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D2_VWMR1 DQ2 right code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D2_VWMR0 DQ2 right code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT9

Address: **Operational Base** + offset (0x0358)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D3_VWMR1 DQ3 right code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:0	RO	0x000	D3_VWMR0 DQ3 right code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT12

Address: **Operational Base** + offset (0x0364)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D4_VWMR1 DQ4 right code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D4_VWMR0 DQ4 right code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT15

Address: **Operational Base** + offset (0x0370)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D5_VWMR1 DQ5 right code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D5_VWMR0 DQ5 right code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT18

Address: **Operational Base** + offset (0x037C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D6_VWMR1 DQ6 right code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D6_VWMR0 DQ6 right code for data slice 0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT21

Address: **Operational Base** + offset (0x0388)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	D7_VWMR1 DQ7 right code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	D7_VWMR0 DQ7 right code for data slice 0. The latest read or write training result will be shown.

DDRPHY_DM_VWMR_STAT0

Address: **Operational Base** + offset (0x0394)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	DM_VWMR1 DM right code for data slice 1. The latest read or write training result will be shown.
15:11	RO	0x00	reserved
10:0	RO	0x000	DM_VWMR0 DM right code for data slice 0. The latest read or write training result will be shown.

DDRPHY_DQ_IO_RDATA0

Address: **Operational Base** + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	DQ_IO_RD1 DQ I/O read data for data slice 1. This register simply mirrors the DQ[15:8] input value through io_dq_in[15:8]. This is used to read DQ during command bus training by S/W.
7:0	RO	0x00	DQ_IO_RD0 DQ I/O read data for data slice 0. This register simply mirrors the DQ[7:0] input value through io_dq_in[7:0]. This is used to read DQ during command bus training by S/W.

DDRPHY_VERSION_INFO_STAT0

Address: **Operational Base** + offset (0x03AC)

Bit	Attr	Reset Value	Description
31:0	RO	0x09080005	Version_Info Version Information

DDRPHY_ZQ_CON0

Address: **Operational Base** + offset (0x03C8)

Bit	Attr	Reset Value	Description
31	RW	0x1	zq_mode_lp4 VSSQ termination receiver mode selection for ctrl slice. It controls io_zq_mode_lp4. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init start falls at begin of DLL relocking period. 1'b1: Enable pull-down termination resistor only (Enable VSSQ-TERM mode of I/O). 1'b0: Deselects VSSQ-TERM mode of I/O.
30:28	RW	0x7	zq_mode_pdds Driver strength selection for ctrl slice. It controls io_zq_mode_pdds. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init start falls at begin of DLL relocking period. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver Others: Reserved

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Bit	Attr	Reset Value	Description
27	RW	0x1	zq_clk_en ZQ I/O Clock enable. It should be set to high before starting ZQ calibration. 1'b1: Enable io_zq_clk. 1'b0: Disable io_zq_clk.
26:24	RW	0x7	zq_mode_dds Driver strength selection for ctrl slice. It controls io_zq_mode_dds. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init start falls at begin of DLL relocking period. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver Others: Reserved
23:21	RW	0x4	zq_mode_term On-die-termination (ODT) resistor value selection for ctrl slice. It controls io_zq_mode_term. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init start falls at begin of DLL relocking period. 3'b100: 60 ohm far end VSSQ termination 3'b010: 120 ohm far end VSSQ termination 3'b001: 240 ohm far end VSSQ termination Others: Reserved
20	RW	0x0	zq_rgddr3 GDDR3 mode enable signal for ctrl slice (High: GDDR3 mode). It controls io_zq_mode_rgddr3. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init start falls at begin of DLL relocking period.
19	RW	0x0	zq_mode_noterm Termination disable selection for ctrl slice. It controls io_zq_mode_noterm. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init start falls at begin of DLL relocking period. 1'b1: Termination disable 1'b0: Termination enable Recommended setting LPDDR4: 1'b0 (recommended) or 1'b1 (when termination is not used)
18	RW	0x0	zq_clk_div_en Clock dividing enable for io_zq_clk. Divider setting is controlled by ctrl_zq_clk_div.
17:15	RW	0x0	zq_force_impn Immediate control code for pull-down for ctrl slice. It controls io_zq_force_impn. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init start falls at begin of DLL relocking period.

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Bit	Attr	Reset Value	Description
14:12	RW	0x7	zq_force_impp Immediate control code for pull-up for ctrl slice. It controls io_zq_force_impp. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init start falls at begin of DLL relocking period.
11:4	RW	0x40	zq_udt_dly ZQ I/O clock enable duration for auto calibration mode. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init start falls at begin of DLL relocking period.
3:2	RW	0x1	zq_manual_mode Manual ZQ calibration mode selection 2'b00: Force calibration 2'b01: Long calibration 2'b10: Reserved for short calibration 2'b11: Reserved
1	RW	0x0	zq_manual_str Manual ZQ calibration start for ZQ pad
0	RO	0x0	reserved

DDRPHY_ZQ_CON1

Address: **Operational Base** + offset (0x03CC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	zq_cal_fsm zq calibration fsm register.
27:22	RO	0x00	reserved
21:16	RW	0x14	zq_vref Vref control for ctrl slice in the internal mode. It controls io_zq_vref[5:0]. Please refer to SSTL IO datasheet for use cases.
15:9	RO	0x00	reserved
8:6	RO	0x0	zq_pmon Control code found by auto calibration for pull-up. It shows the result of ZQ calibration from ZQ PAD.
5:3	RO	0x0	zq_nmon Control code found by auto calibration for pull-down. It shows the result of ZQ calibration from ZQ PAD.
2	RO	0x0	zq_mon Calibration fail indication (High: calibration failed). It shows the result of ZQ calibration from ZQ PAD.
1	RO	0x0	zq_pending Auto calibration enable status
0	RO	0x0	zq_done ZQ Calibration is finished. The response for zq_manual_str from ZQ pad.

DDRPHY_ZQ_CON2

Address: **Operational Base** + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:16	RW	0x1e	zq_upd_ack_cycle For debug purpose. This register controls the number of cycle during which cs_phyupd_FSM stays at ST_UPD_ACK stat when ZQ periodic update occurs. It affects the duration of dfi_phyupd_ack = 1.
15:0	RW	0x0002	ctrl_zq_clk_div ZQ Clock (=io_zq_clk) divider setting value. The frequency will be determined by the following formula. This field should be set before the first ZQ calibration and should not be changed afterwards. ctrl_zq_clk_div should be between 1 to 7. "io_zq_clk frequency" (MHz) = "clk_dfi frequency" (MHz) / ((ctrl_zq_clk_div+1)*2)

DDRPHY_ZQ_CON3

Address: **Operational Base** + offset (0x03D4)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:19	RW	0x7	zq_ck_dds Driver pull-down strength control for CK pad. It controls io_zq_ck_dds. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver
18:16	RW	0x7	zq_ck_pdds Driver pull-up strength control for CK pad. It controls io_zq_ck_pdds.
15:14	RO	0x0	reserved
13:11	RW	0x7	zq_ds1_dds Driver pull-down strength control for data slice 1. It controls io_zq_ds_dds[5:3]. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver
10:8	RW	0x7	zq_ds1_pdds Driver pull-up strength control for data slice 1. It controls io_zq_ds_pdds[5:3].
7:6	RO	0x0	reserved
5:3	RW	0x7	zq_ds0_dds Driver pull-down strength control for data slice 0. It controls io_zq_ds_dds[2:0]. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver
2:0	RW	0x7	zq_ds0_pdds Driver pull-up strength control for data slice 0. It controls io_zq_ds_pdds[2:0].

DDRPHY_ZQ_CON5

Address: **Operational Base** + offset (0x03DC)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x7	zq_reset_dds Driver pull-down strength control for reset. It controls io_zq_reset_dds[2:0]. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver
23:22	RO	0x0	reserved
21:19	RW	0x7	zq_cke1_dds Driver pull-down strength control for cke (rank1). It controls io_zq_cke1_dds[2:0]. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver
18:16	RW	0x7	zq_cke0_dds Driver pull-down strength control for cke (rank0). It controls io_zq_cke0_dds[2:0]. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver
15:0	RO	0x0000	reserved

DDRPHY_ZQ_CON6

Address: **Operational Base** + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:11	RW	0x4	zq_ds1_term On-die-termination (ODT) resistor value selection for data slice 1. It determines io_zq_ds_mode_term[5:3]. Please refer to SSTL I/O datasheet for specific termination settings. 3'b100: 60 ohm far end VSSQ termination 3'b010: 120 ohm far end VSSQ termination 3'b001: 240 ohm far end VSSQ termination
10	RW	0x0	zq_ds1_rgddr3 GDDR3 mode enable signal for data slice 1 (High: GDDR3 mode). It controls io_zq_ds_rgddr[1].
9	RW	0x0	zq_ds1_noterm Termination disable selection for data slice 1. It controls io_zq_ds_noterm[1]. 1'b1: Termination disable 1'b0: Termination enable LPDDR4: 1'b0 (recommended) or 1'b1 (when termination is not used).
8	RW	0x1	zq_ds1_lp4 VSSQ termination receiver mode selection for data slice 1. It controls io_zq_ds_lp4[1]. 1'b1: Enable pull-down termination resistor only (Enable VSSQ-TERM).
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:3	RW	0x4	zq_ds0_term On-die-termination (ODT) resistor value selection for data slice 0. It determines io_zq_ds_mode_term[2:0]. Please refer to SSTL I/O datasheet for specific termination settings. 3'b100: 60 ohm far end VSSQ termination 3'b010: 120 ohm far end VSSQ termination 3'b001: 240 ohm far end VSSQ termination
2	RW	0x0	zq_ds0_rgddr3 GDDR3 mode enable signal for data slice 0 (High: GDDR3 mode). It controls io_zq_ds_rgddr[0].
1	RW	0x0	zq_ds0_noterm Termination disable selection for data slice 0. It controls io_zq_ds_noterm[0]. 1'b1: Termination disable. 1'b0: Termination enable. LPDDR4: 1'b0 (recommended) or 1'b1 (when termination is not used).
0	RW	0x1	zq_ds0_lp4 VSSQ termination receiver mode selection for data slice 0. It controls io_zq_ds_lp4[0]. 1'b1: Enable pull-down termination resistor only (Enable VSSQ-TERM).

DDRPHY_ZQ_CON9

Address: **Operational Base** + offset (0x03EC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	zq_ds1_vref_pd Vref power down for data slice 1. It controls io_zq_ds_vref_pd[1].
14	RW	0x0	zq_ds1_vref_fsbst Vref fast boost mode control for data slice 1. It controls io_zq_ds_vref_fsbst[1]. 1'b0: Normal mode 1'b1: Fast boost mode
13:8	RW	0x14	zq_ds1_vref Vref control (VSEL5~VSEL0) for data slice 1 in the internal mode. It controls io_zq_ds_vref[11:6].
7	RW	0x0	zq_ds0_vref_pd Vref power down for data slice 0. It controls io_zq_ds_vref_pd[0].
6	RW	0x0	zq_ds0_vref_fsbst Vref fast boost mode control for data slice 0. It controls io_zq_ds_vref_fsbst[0]. 1'b0: Normal mode 1'b1: Fast boost mode
5:0	RW	0x14	zq_ds0_vref Vref control (VSEL5~VSEL0) for data slice 0 in the internal mode. It controls io_zq_ds_vref[5:0].

DDRPHY_ZQ_CON12

Address: **Operational Base** + offset (0x03F8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
13:11	RW	0x0	zq_ds1_impn Immediate control code for pull-down for data slice 1. It controls io_zq_ds_impn[5:3].
10:8	RW	0x7	zq_ds1_impp Immediate control code for pull-up for data slice 1. It controls io_zq_ds_impp[5:3].
7:6	RO	0x0	reserved
5:3	RW	0x0	zq_ds0_impn Immediate control code for pull-down for data slice 0. It controls io_zq_ds_impn[2:0].
2:0	RW	0x7	zq_ds0_impp Immediate control code for pull-up for data slice 0. It controls io_zq_ds_impp[2:0].

DDRPHY_TESTIRCV_CON0

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:18	RW	0x2	zq_mode_testizq zq short cal mode control. It controls U_PHYIO_SLICE/U_IO_SLICE/IMPCNT_IO_DS1/TESTIZQ[1:0]. zq_mode_tetsizq[1] controls i_zctrl_update_opt. zq_mode_testizq[0] controls i_zctrl_short_opt in ZCTRL. zq_mode_testizq[2] controls zctrl_tune_opt. Option to control calibration sequence. 1'b0: Pull-down and pull-up are calibrated at the same time (Default). 1'b1: After calibrated pull-down, pull-up is calibrated. It controls U_PHYIO_SLICE/U_IO_SLICE/IMPCNT_IO_DS1/ZCTRL_PU_MODE_SEL.
17	RW	0x0	zq_ds1_ibias_ctrl_en Impcnt bias current control enable for data slice 1. Controls io_zq_ds_ibias_ctrl_en[1] under PHYIO_SLICE.
16	RW	0x0	zq_ds0_ibias_ctrl_en Impcnt bias current control enable for data slice 0. Controls io_zq_ds_ibias_ctrl_en[0] under PHYIO_SLICE.
15:14	RW	0x0	zq_ds1_ibias_ctrl Impcnt bias current control for data slice 1. Controls io_zq_ds_ibias_ctrl[3:2] under PHYIO_SLICE.
13:12	RW	0x0	zq_ds0_ibias_ctrl Impcnt bias current control for data slice 0. Controls io_zq_ds_ibias_ctrl[1:0] under PHYIO_SLICE.
11	RO	0x0	reserved
10	RW	0x0	zq_mode_ibias_ctrl_en Impcnt bias current control enable for CS. Controls io_zq_mode_ibias_ctrl_en under PHYIO_SLICE.
9:8	RW	0x0	zq_mode_ibias_ctrl Impcnt bias current control for CS. Controls io_zq_mode_ibias_ctrl under PHYIO_SLICE.
7:4	RW	0x0	dqs1_testircv DQS1 receiver test mode control. Controls io_dqs1_testircv under PHYIO_SLICE.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	dqs0_testircv DQS0 receiver test mode control. Controls io_dqs0_testircv under PHYIO_SLICE.

DDRPHY_WR_DESKEWC_CS1_CON0

Address: **Operational Base** + offset (0x0410)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR0DeskewC1_cs1 Write DQ0 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR0DeskewC0_cs1 Write DQ0 de-skew center code for data slice 0

DDRPHY_WR_DESKEWC_CS1_CON1

Address: **Operational Base** + offset (0x041C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR1DeskewC1_cs1 Write DQ1 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR1DeskewC0_cs1 Write DQ1 de-skew center code for data slice 0

DDRPHY_WR_DESKEWC_CS1_CON2

Address: **Operational Base** + offset (0x0428)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR2DeskewC1_cs1 Write DQ2 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR2DeskewC0_cs1 Write DQ2 de-skew center code for data slice 0

DDRPHY_WR_DESKEWC_CS1_CON3

Address: **Operational Base** + offset (0x0434)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR3DeskewC1_cs1 Write DQ3 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR3DeskewC0_cs1 Write DQ3 de-skew center code for data slice 0

DDRPHY_WR_DESKEWC_CS1_CON4

Address: **Operational Base** + offset (0x0440)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR4DeskewC1_cs1 Write DQ4 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR4DeskewC0_cs1 Write DQ4 de-skew center code for data slice 0

DDRPHY_WR_DESKEWC_CS1_CON5

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Address: **Operational Base** + offset (0x044C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR5DeskewC1_cs1 Write DQ5 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR5DeskewC0_cs1 Write DQ5 de-skew center code for data slice 0

DDRPHY_WR_DESKEWC_CS1_CON6

Address: **Operational Base** + offset (0x0458)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR6DeskewC1_cs1 Write DQ6 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR6DeskewC0_cs1 Write DQ6 de-skew center code for data slice 0

DDRPHY_WR_DESKEWC_CS1_CON7

Address: **Operational Base** + offset (0x0464)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR7DeskewC1_cs1 Write DQ7 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR7DeskewC0_cs1 Write DQ7 de-skew center code for data slice 0

DDRPHY_DM_DESKEWC_CS1_CON0

Address: **Operational Base** + offset (0x0470)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	DMDeskewC1_cs1 Write DM de-skew center code for data slice 1. It will be the same as dm_vwmc1 right after the initial write training is done.
15:10	RO	0x00	reserved
9:0	RO	0x000	DMDeskewC0_cs1 Write DM de-skew center code for data slice 0. It will be the same as dm_vwmc0 right after the initial write training is done.

DDRPHY_WR_DESKEWL_CS0_CON0

Address: **Operational Base** + offset (0x0490)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR0DeskewL1_cs0 Write DQ0 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR0DeskewL0_cs0 Write DQ0 de-skew left code for data slice 0

DDRPHY_WR_DESKEWL_CS0_CON1

Address: **Operational Base** + offset (0x049C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RO	0x000	WR1DeskewL1_cs0 Write DQ1 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR1DeskewL0_cs0 Write DQ1 de-skew left code for data slice 0

DDRPHY_WR_DESKEWL_CS0_CON2

Address: **Operational Base** + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR2DeskewL1_cs0 Write DQ2 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR2DeskewL0_cs0 Write DQ2 de-skew left code for data slice 0

DDRPHY_WR_DESKEWL_CS0_CON3

Address: **Operational Base** + offset (0x04B4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR3DeskewL1_cs0 Write DQ3 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR3DeskewL0_cs0 Write DQ3 de-skew left code for data slice 0

DDRPHY_WR_DESKEWL_CS0_CON4

Address: **Operational Base** + offset (0x04C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR4DeskewL1_cs0 Write DQ4 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR4DeskewL0_cs0 Write DQ4 de-skew left code for data slice 0

DDRPHY_WR_DESKEWL_CS0_CON5

Address: **Operational Base** + offset (0x04CC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR5DeskewL1_cs0 Write DQ5 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR5DeskewL0_cs0 Write DQ5 de-skew left code for data slice 0

DDRPHY_WR_DESKEWL_CS0_CON6

Address: **Operational Base** + offset (0x04D8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR6DeskewL1_cs0 Write DQ6 de-skew left code for data slice 1
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	WR6DeskewL0_cs0 Write DQ6 de-skew left code for data slice 0

DDRPHY_WR_DESKEWL_CS0_CON7

Address: **Operational Base** + offset (0x04E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR7DeskewL1_cs0 Write DQ7 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR7DeskewL0_cs0 Write DQ7 de-skew left code for data slice 0

DDRPHY_DM_DESKEWL_CS0_CON0

Address: **Operational Base** + offset (0x04F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	DMDeskewL1_cs0 Write DM de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	DMDeskewL0_cs0 Write DM de-skew left code for data slice 0

DDRPHY_WR_DESKEWL_CS1_CON0

Address: **Operational Base** + offset (0x0500)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR0DeskewL1_cs1 Write DQ0 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR0DeskewL0_cs1 Write DQ0 de-skew left code for data slice 0

DDRPHY_WR_DESKEWL_CS1_CON1

Address: **Operational Base** + offset (0x050C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR1DeskewL1_cs1 Write DQ1 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR1DeskewL0_cs1 Write DQ1 de-skew left code for data slice 0

DDRPHY_WR_DESKEWL_CS1_CON2

Address: **Operational Base** + offset (0x0518)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR2DeskewL1_cs1 Write DQ2 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR2DeskewL0_cs1 Write DQ2 de-skew left code for data slice 0

DDRPHY_WR_DESKEWL_CS1_CON3

Address: **Operational Base** + offset (0x0524)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR3DeskewL1_cs1 Write DQ3 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR3DeskewL0_cs1 Write DQ3 de-skew left code for data slice 0

DDRPHY_WR_DESKEWL_CS1_CON4

Address: **Operational Base** + offset (0x0530)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR4DeskewL1_cs1 Write DQ4 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR4DeskewL0_cs1 Write DQ4 de-skew left code for data slice 0

DDRPHY_WR_DESKEWL_CS1_CON5

Address: **Operational Base** + offset (0x053C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR5DeskewL1_cs1 Write DQ5 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR5DeskewL0_cs1 Write DQ5 de-skew left code for data slice 0

DDRPHY_WR_DESKEWL_CS1_CON6

Address: **Operational Base** + offset (0x0548)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR6DeskewL1_cs1 Write DQ6 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR6DeskewL0_cs1 Write DQ6 de-skew left code for data slice 0

DDRPHY_WR_DESKEWL_CS1_CON7

Address: **Operational Base** + offset (0x0554)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	WR7DeskewL1_cs1 Write DQ7 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	WR7DeskewL0_cs1 Write DQ7 de-skew left code for data slice 0

DDRPHY_DM_DESKEWL_CS1_CON0

Address: **Operational Base** + offset (0x0560)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	DMDeskewL1_cs1 Write DM de-skew left code for data slice 1
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	DMDeskewL0_cs1 Write DM de-skew left code for data slice 0

DDRPHY_RD_DQS_VWML_CS0_CON0

Address: **Operational Base** + offset (0x0574)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RO	0x000	RDDQSVWML1_cs0 Read DQS left code for data slice 1
15:9	RO	0x00	reserved
8:0	RO	0x000	RDDQSVWML0_cs0 Read DQS left code for data slice 0

DDRPHY_RD_DQS_VWMC_CS0_CON0

Address: **Operational Base** + offset (0x0580)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RO	0x000	RDDQSVWMC1_cs0 Read DQS center code for data slice 1
15:9	RO	0x00	reserved
8:0	RO	0x000	RDDQSVWMC0_cs0 Read DQS center code for data slice 0

DDRPHY_GT_STATUS_CON0

Address: **Operational Base** + offset (0x058C)

Bit	Attr	Reset Value	Description
31	RO	0x0	fifo_rd_fail_ds1 Command FIFO read fail flag for auto DQS clean mode for data slice 1. It is set to 1 if FIFO read is asserted when FIFO empty is set.
30	RO	0x0	fifo_rd_fail_ds0 Command FIFO read fail flag for auto DQS clean mode for data slice 0. It is set to 1 if FIFO read is asserted when FIFO empty is set.
29	RO	0x0	fifo_wr_fail_ds1 Command FIFO write fail flag for auto DQS clean mode for data slice 1. It is set to 1 if FIFO write is asserted when FIFO full is set.
28	RO	0x0	fifo_wr_fail_ds0 Command FIFO write fail flag for auto DQS clean mode for data slice 0. It is set to 1 if FIFO write is asserted when FIFO full is set.
27:16	RO	0x000	reserved
15	RO	0x0	gt_preamble_start_ds1_cs1 This is debug feature for gate training This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 1, rank1). gt_preamble_start means gate located at read dqs preamble state.
14	RO	0x0	gt_highz_start_ds1_cs1 This is debug feature for gate training This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 1, rank1). gt_highz_start means gate located at high-z state.

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Bit	Attr	Reset Value	Description
13	RO	0x0	gt_dqsh_start_ds1_cs1 This is debug feature for gate training This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 1, rank1). gt_dqsh_start means gate located at dqs high state.
12	RO	0x0	gt_max_cyc_ds1_cs1 This is debug feature for gate training This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 1, rank1). gt_max_cyc means gate training fail.
11	RO	0x0	gt_preamble_start_ds0_cs1 This is debug feature for gate training This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 0, rank1). gt_preamble_start means gate located at read dqs preamble state.
10	RO	0x0	gt_highz_start_ds0_cs1 This is debug feature for gate training This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 0, rank1). gt_highz_start means gate located at high-z state.
9	RO	0x0	gt_dqsh_start_ds0_cs1 This is debug feature for gate training This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 0, rank1). gt_dqsh_start means gate located at dqs high state.
8	RO	0x0	gt_max_cyc_ds0_cs1 This is debug feature for gate training This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 0, rank1). gt_max_cyc means gate training fail.
7	RO	0x0	DQS_RESP1_fall_cs1 DQS response searched by gate fall edge for data slice 1. DQS sampled at ctrl_gate falling edge for data slice 1 to monitor gate training result for rank1.
6:5	RO	0x0	reserved
4	RO	0x0	DQS_RESP1_cs1 DQS response searched by gate rise edge for data slice 1 DQS sampled at ctrl_gate rising edge for data slice 1 to monitor gate training result for rank1.
3	RO	0x0	DQS_RESP0_fall_cs1 DQS response searched by gate fall edge for data slice 0. DQS sampled at ctrl_gate falling edge for data slice 0 to monitor gate training result for rank1.
2:1	RO	0x0	reserved
0	RO	0x0	DQS_RESP0_cs1 DQS response searched by gate rise edge for data slice 0. DQS sampled at ctrl_gate rising edge for data slice 0 to monitor gate training result for rank1.

DDRPHY_GT_STATUS_CON1

Address: **Operational Base** + offset (0x0590)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15	RO	0x0	gt_preamble_start_ds1_cs0 This is debug feature for gate training. This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 1, rank0). gt_preamble_start means Gate located at read dqs preamble state.
14	RO	0x0	gt_highz_start_ds1_cs0 This is debug feature for gate training. This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 1, rank0). gt_highz_start means Gate located at high-z state.
13	RO	0x0	gt_dqsh_start_ds1_cs0 This is debug feature for gate training. This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 1, rank0). gt_dqsh_start means Gate located at dqs high state.
12	RO	0x0	gt_max_cyc_ds1_cs0 This is debug feature for gate training. This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 1, rank0). gt_max_cyc means gate training fail.
11	RO	0x0	gt_preamble_start_ds0_cs0 This is debug feature for gate training. This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 0, rank0). gt_preamble_start means Gate located at read dqs preamble state.
10	RO	0x0	gt_highz_start_ds0_cs0 This is debug feature for gate training. This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 0, rank0). gt_highz_start means Gate located at high-z state.
9	RO	0x0	gt_dqsh_start_ds0_cs0 This is debug feature for gate training. This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 0, rank0). gt_dqsh_start means Gate located at dqs high state.
8	RO	0x0	gt_max_cyc_ds0_cs0 This is debug feature for gate training. This is a status between gate and DQS for 1st MPC (read) at DVFS/periodic gate training (Data slice 0, rank0). gt_max_cyc means gate training fail.
7	RO	0x0	DQS_RESP1_fall_cs0 DQS response searched by gate fall edge for data slice 1. DQS sampled at ctrl_gate falling edge for data slice 1 to monitor gate training result for rank0.
6:5	RO	0x0	reserved
4	RO	0x0	DQS_RESP1_cs0 DQS response searched by gate rise edge for data slice 1. DQS sampled at ctrl_gate rising edge for data slice 1 to monitor gate training result for rank0.
3	RO	0x0	DQS_RESP0_fall_cs0 DQS response searched by gate fall edge for data slice 0. DQS sampled at ctrl_gate falling edge for data slice 0 to monitor gate training result for rank0.
2:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RO	0x0	DQS_RESP0_cs0 DQS response searched by gate rise edge for data slice 0. DQS sampled at ctrl_gate rising edge for data slice 0 to monitor gate training result for rank0.

DDRPHY_GT_FSM_STATUS_CON1

Address: **Operational Base** + offset (0x0594)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	GATE_LOFSM_IDLE_ds1 FSM flag of gate signal idle location for slice 1
29	RO	0x0	GATE_LOFSM_UNKNOWN_ds1 FSM flag of gate signal unknown location for slice 1
28	RO	0x0	GATE_LOFSM_PREAMBLE_ds1 FSM flag of gate signal preamble location for slice 1
27:26	RO	0x0	gate_fail_status_ds1 Fail status for gate training at slice 1. gate_fail_status_ds1[1] is for rank 1, gate_fail_status_ds1[0] is for rank0. If each bit is set to high, it indicates that dqs rising edge is not found during gate training.
25:24	RO	0x0	GATE_LOCATION_FSM_ds1 FSM of gate signal location for slice 1
23	RO	0x0	reserved
22	RO	0x0	GATE_LOFSM_IDLE_ds0 FSM flag of gate signal idle location for slice 0
21	RO	0x0	GATE_LOFSM_UNKNOWN_ds0 FSM flag of gate signal unknown location for slice 0
20	RO	0x0	GATE_LOFSM_PREAMBLE_ds0 FSM flag of gate signal preamble location for slice 0
19:18	RO	0x0	gate_fail_status_ds0 Fail status for gate training at slice 0. gate_fail_status_ds0[1] is for rank 1, gate_fail_status_ds0[0] is for rank0. If each bit is set to high, it indicates that dqs rising edge is not found during gate training.
17:16	RO	0x0	GATE_LOCATION_FSM_ds0 FSM of gate signal location for slice 0
15	RO	0x0	GATE_FSM_IDLE_DS1 IDLE state flag of gate training FSM for slice 1
14	RO	0x0	GATE_FSM_INIT_DS1 Initial state flag of gate training FSM for slice 1
13	RO	0x0	GATE_FSM_PERIODIC_DS1 Periodic state flag of gate training FSM for slice 1
12	RO	0x0	GATE_FSM_RESP_DS1 Response state flag of gate training FSM for slice 1
11	RO	0x0	reserved
10:8	RO	0x0	GATE_FSM_STATUS_ds1 FSM monitoring signal for slice 1. It shows CS_DsRdlvl FSM status in gate_training.
7	RO	0x0	GATE_FSM_IDLE_DS0 IDLE state flag of gate training FSM for slice 0
6	RO	0x0	GATE_FSM_INIT_DS0 Initial state flag of gate training FSM for slice 0
5	RO	0x0	GATE_FSM_PERIODIC_DS0 Periodic state flag of gate training FSM for slice 0

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Bit	Attr	Reset Value	Description
4	RO	0x0	GATE_FSM_RESP_DS0 Response state flag of gate training FSM for slice 0
3	RO	0x0	reserved
2:0	RO	0x0	GATE_FSM_STATUS_ds0 FSM monitoring signal for slice 0. It shows CS_DsRdlvl FSM status in gate training.

DDRPHY_CAL_GT_CS1_VWMC0

Address: **Operational Base** + offset (0x05E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	GT_VWMC1_cs1 Gate training code for data slice 1. It shows the number of fine step delay cells applied to gate signal after gate training.
15:10	RO	0x00	reserved
9:0	RO	0x000	GT_VWMC0_cs1 Gate training code for data slice 0. It shows the number of fine step delay cells applied to gate signal after gate training.

DDRPHY_CAL_GT_CS1_CYC

Address: **Operational Base** + offset (0x05F0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RO	0x0	GT_CYC1_cs1 Gate training cycle increment information for data slice 1. It represents how much ctrl_gate signal is delayed by DFI PHY clock cycle.
7:4	RO	0x0	reserved
3:0	RO	0x0	GT_CYC0_cs1 Gate training cycle increment information for data slice 0. It represents how much ctrl_gate signal is delayed by DFI PHY clock cycle.

DDRPHY_CBT_CON5

Address: **Operational Base** + offset (0x05F4)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x0d	cbt_tDSTRAIN LPDDR4 CBT: tDStrain (Data setup for VREF training mode) timing parameter setting register. RU (1/tCK), tCK = memory clock frequency
15	RO	0x0	reserved
14:10	RW	0x0d	cbt_tDHTRAIN LPDDR4 CBT: tDHtrain (Data hold for VREF training mode) timing parameter setting register. RU (1/tCK), tCK = Memory clock frequency
9:0	RO	0x000	reserved

DDRPHY_CBT_CMD

Address: **Operational Base** + offset (0x05FC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11:10	RW	0x1	cbt_cs Chip select during command bus training. In one CBT procedure, only one bit of cbt_cs[1:0] should be enabled. 2'b01: Rank0 2'b10: Rank1
9:8	RO	0x0	reserved
7:0	RW	0x3f	cbt_ca_pattern Predefined CA pattern that will be used during command bus training. io_adct_out will be set to cbt_ca_pattern.

DDRPHY_CBT_CON0

Address: **Operational Base** + offset (0x0600)

Bit	Attr	Reset Value	Description
31	RW	0x0	cbt_sw_mode SW command bus training code update control. This field will be enabled when restoring the previous command bus training registers. 1'b1: SW_CA*DeSkewCode, SW_CS*DeSkewCode will be written to internal command bus training code. 1'b0: SW_CA*DeSkewCode, SW_CS*DeSkewCode will be not written to internal command bus training code.
30:27	RO	0x0	reserved
26:25	RW	0x0	cbt_vref_dqs_en It is used for S/W CBT CA Vref setting mode. If it is enabled, DQS will be driven for Vref setting during S/W CBT. 2'b01: In case of CS0 CBT, DS0 (DQS[0], DQSB[0]) enable for CA Vref setting 2'b10: In case of CS1 CBT, DS1 (DQS[1], DQSB[1]) enable for CA Vref setting
24:23	RO	0x0	reserved
22:21	RW	0x0	cbt_vref_dq_en It is used for S/W CBT CA Vref setting mode. If it is enabled, CA Vref setting value will be driven on DQ bus. 2'b01: In case of CS0 CBT, data slice 0 (DQ[7:0]) enable for CA Vref setting 2'b10: In case of CS1 CBT, data slice 1 (DQ[15:8]) enable for CA Vref setting
20:12	RO	0x000	reserved
11	RW	0x0	cbt_cs_coarse_dis CBT cs coarse disable control
10:8	RO	0x0	reserved
7:0	RW	0x4d	cbt_ca_vref CA Vref setting value which will be driven on DQ when command bus training. Refer to LPDDR4 MR12 register information.

DDRPHY_CBT_CON2

Address: **Operational Base** + offset (0x0608)

Bit	Attr	Reset Value	Description
31	RW	0x0	cbt_vref_set_en LPDDR5 CBT: CA Vref setting value will be driven after CBT_CON2.cbt_tDSTRAIN_LP5 when the register is enabled .
30	RW	0x0	cbt_dq_rcv_en LPDDR5 CBT: PHY can be receive the captured data from memory with DQ receiver mode if the register is enabled.

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Bit	Attr	Reset Value	Description
29	RW	0x0	cbt_start LPDDR5 CBT: DQ[7] will be high to configure the memory CA calibration state.
28	RW	0x0	cbt_vref_pre_en LPDDR5 CBT: DMI will be low before changing the CA setting value during CBT.
27	RW	0x0	cbt_wck_en LPDDR5 CBT: Enable WCK toggle to set the CA Vref value by DQ bus during CBT mode.
26	RO	0x0	reserved
25	RW	0x0	cbt_ca_shift_cycle Shift the CA cycle register. If 'cbt_ca_shift_cycle' is enabled, CA is generated after 1cycle. 'cbt_ca_shift_cycle' should be used with CBT_CON0.cbt_sw_mode.
24	RW	0x0	cbt_cs_shift_cycle Shift the CS cycle register. If 'cbt_cs_shift_cycle' is enabled, CS is generated after 1cycle. 'cbt_cs_shift_cycle' should be used with CBT_CON0.cbt_sw_mode.
23:16	RW	0x00	cbt_dqdm_sel LPDDR5 CBT: DQ[7], DMI select pin 'cbt_dqdm_sel' should be set as 0x80. Other settings is not supported.
15:11	RW	0x0c	cbt_tWCK2DQ7 LPDDR5 CBT: tWCK2DQ7 (Set-up margin between DQ7 and WCK) timing parameter setting register. RU (5/tCK), tCK = memory clock frequency
10:6	RW	0x0c	cbt_tDSTRAIN_LP5 LPDDR5 CBT: tDStrain (data setup for Vref training mode) timing parameter setting register. RU (5/tCK), tCK = Memory clock frequency
5:0	RO	0x00	reserved

DDRPHY_CBT_CON3

Address: **Operational Base** + offset (0x060C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x3	cbt_cke CKE during command bus training. It controls the value driven on io_cke_out[1:0] during command bus training.
21:20	RW	0x0	cbt_odt_ca CA ODT during command bus training. It controls the value driven on io_odt_out[1:0] during command bus training.
19	RW	0x1	cbt_reset RESET during command bus training. It controls the value driven on io_reset_out during command bus training.
18	RW	0x0	cbt_cmd_cs_vwml Reserved
17	RW	0x0	cbt_cmd_cs_vwmr Command enable for CS VWMR search during command bus training. If enabled, io_cs_out[1:0] will be set to cbt_cs for 1 DFI PHY clock cycle and io_adct_out will be set to cbt_ca_pattern, and io_ck_out will be gated until io_cs_out is driven to cbt_cs.

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Bit	Attr	Reset Value	Description
16	RW	0x0	cbt_cmd_ca_vwml Command enable for CA VWML search during command bus training. If enabled, io_cs_out[1:0] will be set to cbt_cs for 1 DFI PHY clock cycle and io_adct_out will be set to cbt_ca_pattern for 1 DFI PHY clock cycle. io_cs_out and io_adct_out will be change at the same io_ck_out edge.
15	RW	0x0	cbt_cmd_ca_vwmr Command enable for CA VWMR search during command bus training. If enabled, io_cs_out[1:0] will be set to cbt_cs for 1 DFI PHY clock cycle and io_adct_out will be set to cbt_ca_pattern for 1 DFI PHY clock cycle. io_adct_out will be changed 1 DFI PHY clock after io_cs_out is changed.
14	RW	0x0	cbt_cmd_clear Command enable to set the CA feedback from DRAM ~cbt_ca_pattern during command bus training. io_adct_out will be set to ~cbt_ca_pattern when this field is set to high.
13	RW	0x0	cbt_cmd_cs_vwml_fine Command enable for CS VWML fine search during command bus training. CS fine training is to find the precise location of CS considering CK SSN, which is not applied in the first CS training. If enabled, io_cs_out[1:0] will be set to cbt_cs for 1 DFI PHY clock cycle and io_adct_out will be set to cbt_ca_pattern for 1 DFI PHY clock cycle. io_cs_out and io_adct_out will be change at the same io_ck_out edge.
12	RW	0x0	cbt_cmd_cs_vwmr_fine Command enable for CS VWMR fine search during command bus training. CS fine training is to find the precise location of CS considering CK SSN, which is not applied in the first CS training. If enabled, io_cs_out[1:0] will be set to cbt_cs for 1 DFI PHY clock cycle and io_adct_out will be set to cbt_ca_pattern for 1 DFI PHY clock cycle. io_adct_out will be changed 1 DFI PHY clock after io_cs_out is changed.
11:2	RO	0x000	reserved
1	RW	0x0	cbt_hw_cal_start LPDDR4 HW calibration start signal
0	RW	0x0	cbt_en LPDDR5 CBT mode enable

DDRPHY_RD_DESKEW_LEFT_CS0_CON_DM

Address: **Operational Base** + offset (0x0610)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RDDMDeskewLeft1_cs0 Read DMI de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RDDMDeskewLeft0_cs0 Read DMI de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS0_CON0

Address: **Operational Base** + offset (0x0614)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD0DeskewLeft1_cs0 Read DQ0 de-skew left code for data slice 1
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	RD0DeskewLeft0_cs0 Read DQ0 de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS0_CON1

Address: **Operational Base** + offset (0x0620)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD1DeskewLeft1_cs0 Read DQ1 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD1DeskewLeft0_cs0 Read DQ1 de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS0_CON2

Address: **Operational Base** + offset (0x062C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD2DeskewLeft1_cs0 Read DQ2 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD2DeskewLeft0_cs0 Read DQ2 de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS0_CON3

Address: **Operational Base** + offset (0x0638)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD3DeskewLeft1_cs0 Read DQ3 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD3DeskewLeft0_cs0 Read DQ3 de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS0_CON4

Address: **Operational Base** + offset (0x0644)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD4DeskewLeft1_cs0 Read DQ4 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD4DeskewLeft0_cs0 Read DQ4 de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS0_CON5

Address: **Operational Base** + offset (0x0650)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD5DeskewLeft1_cs0 Read DQ5 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD5DeskewLeft0_cs0 Read DQ5 de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS0_CON6

Address: **Operational Base** + offset (0x065C)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD6DeskewLeft1_cs0 Read DQ6 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD6DeskewLeft0_cs0 Read DQ6 de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS0_CON7

Address: **Operational Base** + offset (0x0668)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD7DeskewLeft1_cs0 Read DQ7 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD7DeskewLeft0_cs0 Read DQ7 de-skew left code for data slice 0

DDRPHY_FREQ_OFFSET_CON

Address: **Operational Base** + offset (0x0680)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RO	0x000000	freq_offset Frequency compensation offset read out. It is calculated based on the current frequency and DLL lock value. It will be added to write DQ/DM center code and read DQS center code internally to maximize both setup and hold margin at the lower frequencies. freq_offset will be calculated as follows: freq_offset = {current lock value * (Training frequency - current frequency) / Training frequency}/4 (tFS)

DDRPHY_PRBS_CON0

Address: **Operational Base** + offset (0x0684)

Bit	Attr	Reset Value	Description
31:16	RW	0x0005	prbs_pattern The number of PRBS patterns to use at each DLL code during PRBS training. Do not use 0 and 1.
15:8	RO	0x00	reserved
7	RW	0x0	prbs_write_cyc_en Write DQ/DM code cycle based control enabled. When enabled, DQ/DM cycle will be controlled if the offset exceeds cycle boundary. Enable this register when low frequency write training is initiated with wrtrn_cyc_mode = 1.
6	RW	0x0	read_duty_en_APB Read duty training enable register Should use prbs_per_bit_mode = 1 and prbs_read_start = 1.
5	RW	0x0	SET_USER_PATTERN_APB PRBS user pattern setting register. And this field only use duty training or PRBS debugging. 1'b1: Fix the data pattern by default value of SEED0, SEED1, SEED2 and SEED3. 1'b0: PRBS pattern generation by SEED0, SEED1, SEED2 and SEED3

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Bit	Attr	Reset Value	Description
4	RW	0x0	PRBS_MPC_MODE_APB PRBS training w/ scheduler through memory RFF/WFF 1'b1: LP5 WFF/RFF path 1'b0: LP5 cell base training
3	RW	0x0	prbs_per_bit_mode PRBS per bit training mode 1'b1: PRBS training per bit 1'b0: PRBS training per byte (default)
2	RW	0x0	prbs_write_start PRBS write training start
1	RW	0x0	prbs_read_start PRBS read training start
0	RO	0x0	prbs_done PRBS training response

DDRPHY_PRBS_CON1

Address: **Operational Base** + offset (0x0688)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x1	prbs_dbi_en DBI function enable during PRBS training. If enabled, DM signal will work as data bus inversion.
25:24	RW	0x1	prbs_cs Rank information for PRBS training.
23:18	RW	0x10	prbs_wrlat DRAM write latency setting (WL).
17:13	RW	0x10	prbs_twr2rd Write to read interval during PRBS training
12:9	RO	0x0	reserved
8:5	RW	0x8	prbs_trddata_en_adj Trddata_en adjustment for PRBS training
4:0	RW	0x0c	prbs_tresync Resync duration setting for PRBS training

DDRPHY_PRBS_CON2

Address: **Operational Base** + offset (0x068C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RO	0x0	prbs_rd_vwml_fail1 PRBS read training VWML search fail for byte1. prbs_rd_vwml_fail1[1] is for rank 0, and prbs_rd_vwml_fail1[0] is for rank 1. If it is set high, it indicates vwml search has failed until DLL code has min value ('h0) while searching VWML.
27:26	RO	0x0	prbs_rd_vwmr_fail1 PRBS read training VWMR search fail for byte1. prbs_rd_vwmr_fail1[1] is for rank 0, and prbs_rd_vwmr_fail1[0] is for rank 1. If it is set high, it indicates vwmr search has failed until DLL code has max value while searching VWMR.

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Bit	Attr	Reset Value	Description
25:16	RO	0x000	prbs_offsetr1 PRBS read training result for byte1. It indicates how much center offset PRBS training has compensated from the initial read training result. prbs_offsetr1[9] = 1: (tFS: fine step delay) Read DQS delay from initial read training - prbs_offsetr1[8:0] x tFS prbs_offsetr1[9] = 0: Read DQS delay from initial read training + prbs_offsetr1[8:0] x tFS
15:14	RO	0x0	reserved
13:12	RO	0x0	prbs_rd_vwml_fail0 PRBS read training VWML search fail for byte0. prbs_rd_vwml_fail1[1] is for rank 0, and prbs_rd_vwml_fail1[0] is for rank 1. If it is set high, it indicates vwml search has failed until DLL code has min value ('h0) while searching VWML.
11:10	RO	0x0	prbs_rd_vwmr_fail0 PRBS read training VWMR search fail for byte0. prbs_rd_vwmr_fail1[1] is for rank 0, and prbs_rd_vwmr_fail1[0] is for rank 1. If it is set high, it indicates vwmr search has failed until DLL code has max value while searching VWMR.
9:0	RO	0x000	prbs_offsetr0 PRBS read training result for byte0. It indicates how much center offset PRBS training has compensated from the initial read training result. prbs_offsetr0[9] = 1: (tFS: fine step delay) Read DQS delay from initial read training - prbs_offsetr0[8:0] x tFS prbs_offsetr0[9] = 0: Read DQS delay from initial read training + prbs_offsetr0[8:0] x tFS

DDRPHY_PRBS_CON3

Address: **Operational Base** + offset (0x0690)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	prbs_fail_byte1 Debug purpose. Information for PRBS training failure at 1st iteration for byte1. 1'b1: PRBS training is failed at 1st iteration. 1'b0: PRBS training is not failed at 1st iteration.
29:28	RO	0x0	prbs_wr_vwml_fail1 PRBS write training VWML search fail for byte1. prbs_wr_vwml_fail1[1] is for rank 0, and prbs_wr_vwml_fail1[0] is for rank 1. If it is set high, it indicates vwml search has failed until DLL code has min value ('h0) while searching VWML.
27:26	RO	0x0	prbs_wr_vwmr_fail1 PRBS write training VWMR search fail for byte1. prbs_wr_vwmr_fail1[1] is for rank 0, and prbs_wr_vwmr_fail1[0] is for rank 1. If it is set high, it indicates vwmr search has failed until DLL code has max value while searching VWMR.

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Bit	Attr	Reset Value	Description
25:16	RO	0x000	prbs_offsetw1 PRBS write training result for byte1. It indicates how much center offset PRBS training has compensated from the initial write training result. prbs_offsetr1[9] = 1: (tFS: fine step delay) write DQ/DM delay from initial write training - prbs_offsetw1[8:0] x tFS prbs_offsetr1[9] = 0: write DQ/DM delay from initial write training + prbs_offsetw1[8:0] x tFS
15	RO	0x0	reserved
14	RO	0x0	prbs_fail_byte0 Debug purpose. Information for PRBS training failure at 1st iteration for byte0. 1'b1: PRBS training is failed at 1st iteration. 1'b0: PRBS training is not failed at 1st iteration.
13:12	RO	0x0	prbs_wr_vwml_fail0 PRBS write training VWML search fail for byte0. prbs_wr_vwml_fail1[1] is for rank 0, and prbs_wr_vwml_fail1[0] is for rank 1. If it is set high, it indicates vwml search has failed until DLL code has min value ('h0) while searching VWML.
11:10	RO	0x0	prbs_wr_vwmr_fail0 PRBS write training VWMR search fail for byte0. prbs_wr_vwmr_fail1[1] is for rank 0, and prbs_wr_vwmr_fail1[0] is for rank 1. If it is set high, it indicates vwmr search has failed until DLL code has max value while searching VWMR.
9:0	RO	0x000	prbs_offsetw0 PRBS write training result for byte0. It indicates how much center offset PRBS training has compensated from the initial write training result. prbs_offsetw0[9] = 1: (tFS: fine step delay) write DQ/DM delay from initial write training - prbs_offsetw0[8:0] x tFS prbs_offsetw0[9] = 0: write DQ/DM delay from initial write training + prbs_offsetw0[8:0] x tFS

DDRPHY_PRBS_CON4

Address: **Operational Base** + offset (0x0694)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_prbs_offsetr1 PRBS read training result for byte1. It indicates how much center offset PRBS training has compensated from the initial read training result. prbs_offsetr1[9] = 1: (tFS: fine step delay) Read DQS delay from initial read training - prbs_offsetr1[8:0] x tFS prbs_offsetr1[9] = 0: Read DQS delay from initial read training + prbs_offsetr1[8:0] x tFS
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_prbs_offsetr0 PRBS read training result for byte0. It indicates how much center offset PRBS training has compensated from the initial read training result. prbs_offsetr0[9] = 1: (tFS: fine step delay) Read DQS delay from initial read training - prbs_offsetr0[8:0] x tFS prbs_offsetr0[9] = 0: Read DQS delay from initial read training + prbs_offsetr0[8:0] x tFS

DDRPHY_PRBS_CON5

Address: **Operational Base** + offset (0x0698)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_prbs_offsetw1 SW PRBS write training result for byte1
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_prbs_offsetw0 SW PRBS write training result for byte0

DDRPHY_PRBS_CON6

Address: **Operational Base** + offset (0x069C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left1 Left margin found during PRBS training for byte1. This field will be updated after each PRBS training.
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left0 Left margin found during PRBS training for byte0. This field will be updated after each PRBS training.

DDRPHY_PRBS_CON7

Address: **Operational Base** + offset (0x06A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right1 Right margin found during PRBS training for byte1. This field will be updated after each PRBS training.
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right0 Right margin found during PRBS training for byte0. This field will be updated after each PRBS training.

DDRPHY_PRBS_CON8

Address: **Operational Base** + offset (0x06A4)

Bit	Attr	Reset Value	Description
31	RW	0x1	prbs_dram_act_enable DRAM activate-precharge enable. If enabled, DRAM activate/precharge will be asserted in between MPC-WR FIFO and MPC-RD FIFO commands during PRBS training. Bank will be changed continuously (0~7) for each activate or precharge.
30:21	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
20:16	RW	0x0b	prbs_tRRD Interval between active commands to different banks during PRBS training with dram_act_enable = 1. tRRD should be set using the following: tRRD = RU ((10ns/1tCK)/2) in DFI clock cycle (1tCK: DRAM clock period).
15:0	RW	0x0000	prbs_row_addr Row address to be used for activate command during PRBS training when dram_act_enable = 1.

DDRPHY_PRBS_CON9

Address: **Operational Base** + offset (0x06A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00ff00ff	SEED0 PRBS SEED0

DDRPHY_PRBS_CON10

Address: **Operational Base** + offset (0x06AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x0f0f0f0f	SEED1 PRBS SEED1

DDRPHY_PRBS_CON11

Address: **Operational Base** + offset (0x06B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x5a5a5a5a	SEED2 PRBS SEED2

DDRPHY_PRBS_CON12

Address: **Operational Base** + offset (0x06B4)

Bit	Attr	Reset Value	Description
31:0	RW	0xff00ff00	SEED3 PRBS SEED3

DDRPHY_PRBS_CON13

Address: **Operational Base** + offset (0x06B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x1	prbs_wrdata_dm_p0_APB PRBS data mask pattern for phase0. It should be set to PRBS_MPC_MODE_APB = 1.
5:4	RW	0x1	prbs_wrdata_dm_p1_APB PRBS data mask pattern for phase1. It should be set to PRBS_MPC_MODE_APB = 1.
3:2	RW	0x1	prbs_wrdata_dm_p2_APB PRBS data mask pattern for phase2. It should be set to PRBS_MPC_MODE_APB = 1.
1:0	RW	0x1	prbs_wrdata_dm_p3_APB PRBS data mask pattern for phase3. It should be set to PRBS_MPC_MODE_APB = 1.

DDRPHY_DUTY_CAL0

Address: **Operational Base** + offset (0x06BC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24:16	RW	0x000	per_burst_duty_mask_en_APB This field mask function each burst data for duty training [24]: BL16 BL15 data mask [23]: BL14 BL13 data mask [22]: BL12 BL11 data mask [21]: BL10 BL9 data mask [20]: BL8 BL7 data mask [19]: BL6 BL5 data mask [18]: BL4 BL3 data mask [17]: BL2 BL1 data mask 1'b1: data mask 1'b0: data unmask
15:9	RO	0x00	reserved
8:0	RW	0x000	per_bit_duty_mask_en_APB This field mask function each bit for duty training [8]: DM1/DM0 [7]: DQ15/DQ7 [6]: DQ14/DQ6 [5]: DQ13/DQ5 [4]: DQ12/DQ4 [3]: DQ11/DQ3 [2]: DQ10/DQ2 [1]: DQ9/DQ1 [0]: DQ8/DQ0 1'b1: Data mask 1'b0: Data unmask

DDRPHY_MON_CON0

Address: **Operational Base** + offset (0x0700)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	dvfs_modei Current dvfs mode status
29:28	RO	0x0	dvfs_modei_prev Previous dvfs mode status
27	RW	0x0	debug_mode_en Debug mode enable
26	RO	0x0	dfi_init_start_status dfi_init_start status
25	RO	0x0	dfi_init_complete_status dfi_init_complete status
24:22	RO	0x0	cs_phydvfs Current PHY DVFS state monitor
21:20	RO	0x0	cs_phyupd Current PHY update state monitor
19	RW	0x0	write_drive_en Write data drive enable. If write_drive_en = 1, PHY will drive write data on DQS, DQ and DBI. The values driven on DQ/DBI is determined by write training pattern defined in CAL_WR_PATTERN_CON0~CAL_WR_PATTERN_CON19. Enable this field only for write data eye measurement. Note that write command will not be driven. During the write operation, write DQ/DBI DLL code will be chosen between rank0 and rank1 based on cs_default.
18	RO	0x0	ctrl_phy_cg_en_status Current ctrl_phy_cg_en status

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Bit	Attr	Reset Value	Description
17	RO	0x1	dfi_dram_clk_disable_status Current dfi_dram_clk_disable status
16	RW	0x0	ReadWriteAccess_mode Enable it before monitoring gate_rise_monitor_ds0, gate_fall_monitor_ds0, gatem_rise_monitor_ds0, gatem_fall_monitor_ds0 registers. It will initialize them to the default values ('h0).
15	RW	0x0	mdll_monitor_en Master DLL monitor enable 1'b1: LOCK_VAL0~LOCK_VAL2 registers will be updated. 1'b0: LOCK_VAL0~LOCK_VAL2 registers will not be updated.
14:11	RW	0x0	gate_debug_en This is optional register for gate training. Gate_debug_en[3]: Gate margin control by shiftc register Gate_debug_en[2]: Skip gate training iteration fine step for reduce black out time. Gate_debug_en[1]: Skip gate training iteration coarse step for reduce black out itme. Gate_debug_en[0]: Cycle update control for gate margin test.
10	RO	0x0	reserved
9	RO	0x0	rddata_en_phase_err_ds1 dfi_rddata_en phase check flag for data slice 1. 1'b0: No error 1'b1: dfi_rddata_en_p0~p3 are not enabled at the same time.
8	RO	0x0	rddata_en_phase_err_ds0 dfi_rddata_en phase check flag for data slice 0. 1'b0: No error 1'b1: dfi_rddata_en_p0~p3 are not enabled at the same time.
7:6	RO	0x0	reserved
5	RO	0x0	read_dur_err_ds1 Read data duration error flag for data slice 1. If this field is set to 'h1, it indicates that rddata duration is not a multiple of 16 at DLL update step. This field is valid when debug_mode_en is high.
4	RO	0x0	read_dur_err_ds0 Read data duration error flag for data slice 0. If this field is set to 'h1, it indicates that rddata duration is not a multiple of 16 at DLL update step. This field is valid when debug_mode_en is high.
3:2	RO	0x0	reserved
1	RO	0x0	write_dur_err_ds1 Write data duration error flag for data slice 1. If this field is set to 'h1, it indicates that wrdata duration is not a multiple of 16 at DLL update step. This field is valid when debug_mode_en is high.
0	RO	0x0	write_dur_err_ds0 Write data duration error flag for data slice 0. If this field is set to 'h1, it indicates that wrdata duration is not a multiple of 16 at DLL update step. This field is valid when debug_mode_en is high.

DDRPHY_MON_CON1

Address: **Operational Base** + offset (0x0704)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RO	0x0	wrdata_dur_ds1 dfi_wrdata_en duration counter for data slice 1. This field is valid when debug_mode_en is high.

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Bit	Attr	Reset Value	Description
19:16	RO	0x0	wrdata_dur_ds0 dfi_wrdata_en duration counter for data slice 0. This field is valid when debug_mode_en is high.
15:8	RO	0x00	reserved
7:4	RO	0x0	rddata_dur_ds1 dfi_rddata_en duration counter for data slice 1. This field is valid when debug_mode_en is high.
3:0	RO	0x0	rddata_dur_ds0 dfi_rddata_en duration counter for data slice 0. This field is valid when debug_mode_en is high.

DDRPHY_MON_CON2

Address: **Operational Base** + offset (0x0708)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_rddata_w0_status dfi_rddata_w0 status. This field is valid when debug_mode_en is high. If debug_mode_en is high, this register shows the last valid dfi_rddata_w0 for the previous read operation. dfi_rddata_w0_status mapping is as follows: dfi_rddata_w0_status[31:16] = {dfi_rddata_w0[31:24], dfi_rddata_w0[15:8]} dfi_rddata_w0_status[15:0] = {dfi_rddata_w0[23:16], dfi_rddata_w0[7:0]}

DDRPHY_MON_CON3

Address: **Operational Base** + offset (0x070C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_rddata_w1_status dfi_rddata_w1 status. This field is valid when debug_mode_en is high. If debug_mode_en is high, this register shows the last valid dfi_rddata_w1 for the previous read operation. dfi_rddata_w1_status mapping is as follows: dfi_rddata_w1_status[31:16] = {dfi_rddata_w1[31:24], dfi_rddata_w1[15:8]} dfi_rddata_w1_status[15:0] = {dfi_rddata_w1[23:16], dfi_rddata_w1[7:0]}

DDRPHY_MON_CON4

Address: **Operational Base** + offset (0x0710)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RO	0x0	dfi_rddata_dmi_w0_status dfi_rddata_dmi_w0[3:0] status. This field is valid when debug_mode_en is high. dfi_rddata_dmi_w0 status. This field is valid when debug_mode_en is high. If debug_mode_en is high, this register shows the last valid dfi_rddata_dmi_w0 for the previous read operation. dfi_rddata_dmi_w0_status mapping is as follows: dfi_rddata_dmi_w0_status[3:2] = {dfi_rddata_dmi_w0[3], dfi_rddata_dmi_w0[1]} dfi_rddata_dmi_w0_status[1:0] = {dfi_rddata_dmi_w0[2], dfi_rddata_dmi_w0[0]}
23:20	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
19:16	RO	0x0	dfi_rddata_dmi_w1_status dfi_rddata_dmi_w1[3:0] status. This field is valid when debug_mode_en is high. dfi_rddata_dmi_w1 status. This field is valid when debug_mode_en is high. If debug_mode_en is high, this register shows the last valid dfi_rddata_dmi_w1 for the previous read operation. dfi_rddata_dmi_w1_status mapping is as follows: dfi_rddata_dmi_w1_status[3:2] = {dfi_rddata_dmi_w1[3], dfi_rddata_dmi_w1[1]} dfi_rddata_dmi_w1_status[1:0] = {dfi_rddata_dmi_w1[2], dfi_rddata_dmi_w1[0]}
15:0	RO	0x0000	reserved

DDRPHY_MON_CON5

Address: **Operational Base** + offset (0x0714)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	wrtrn_fsm_idle_rank1_ds1 Idle stat flag of write training for rank1 of data slice 1
20	RO	0x0	wrtrn_fsm_first_rank1_ds1 First state flag of write training for rank1 of data slice 1
19	RO	0x0	wrtrn_fsm_codeinit_rank1_ds1 Code initialization state flag of write training for rank1 of data slice 1
18	RO	0x0	wrtrn_fsm_second_rank1_ds1 Second state flag of write training for rank1 of data slice 1
17	RO	0x0	wrtrn_fsm_periodic_rank1_ds1 Periodic state flag of write training for rank1 of data slice 1
16	RO	0x0	wrtrn_fsm_resp_rank1_ds1 Response state flag of write training for rank1 of data slice 1
15:12	RO	0x0	write_fsm_status_rank1_ds1 FSM monitoring signal for rank1 of data slice 1. It shows cs_wrtrn FSM status in write training.
11:10	RO	0x0	reserved
9	RO	0x0	wrtrn_fsm_idle_rank1_ds0 Idle stat flag of write training for rank1 of data slice 0
8	RO	0x0	wrtrn_fsm_first_rank1_ds0 First state flag of write training for rank1 of data slice 0
7	RO	0x0	wrtrn_fsm_codeinit_rank1_ds0 Code initialization state flag of write training for rank1 of data slice 0
6	RO	0x0	wrtrn_fsm_second_rank1_ds0 Second state flag of write training for rank1 of data slice 0
5	RO	0x0	wrtrn_fsm_periodic_rank1_ds0 Periodic state flag of write training for rank1 of data slice 0
4	RO	0x0	wrtrn_fsm_resp_rank1_ds0 Response state flag of write training for rank1 of data slice 0
3:0	RO	0x0	write_fsm_status_rank1_ds0 FSM monitoring signal for rank1 of data slice 0. It shows cs_wrtrn FSM status in write training.

DDRPHY_MON_CON6

Address: **Operational Base** + offset (0x0718)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

Bit	Attr	Reset Value	Description
21	RO	0x0	wrtrn_fsm_idle_rank0_ds1 Idle stat flag of write training for rank0 of data slice 1
20	RO	0x0	wrtrn_fsm_first_rank0_ds1 First state flag of write training for rank0 of data slice 1
19	RO	0x0	wrtrn_fsm_codeinit_rank0_ds1 Code initialization state flag of write training for rank0 of data slice 1
18	RO	0x0	wrtrn_fsm_second_rank0_ds1 Second state flag of write training for rank0 of data slice 1
17	RO	0x0	wrtrn_fsm_periodic_rank0_ds1 Periodic state flag of write training for rank0 of data slice 1
16	RO	0x0	wrtrn_fsm_resp_rank0_ds1 Response state flag of write training for rank0 of data slice 1
15:12	RO	0x0	write_fsm_status_rank0_ds1 FSM monitoring signal for rank0 of data slice 1. It shows cs_wrtrn FSM status in write training.
11:10	RO	0x0	reserved
9	RO	0x0	wrtrn_fsm_idle_rank0_ds0 Idle stat flag of write training for rank0 of data slice 0
8	RO	0x0	wrtrn_fsm_first_rank0_ds0 First state flag of write training for rank0 of data slice 0
7	RO	0x0	wrtrn_fsm_codeinit_rank0_ds0 Code initialization state flag of write training for rank0 of data slice 0
6	RO	0x0	wrtrn_fsm_second_rank0_ds0 Second state flag of write training for rank0 of data slice 0
5	RO	0x0	wrtrn_fsm_periodic_rank0_ds0 Periodic state flag of write training for rank0 of data slice 0
4	RO	0x0	wrtrn_fsm_resp_rank0_ds0 Response state flag of write training for rank0 of data slice 0
3:0	RO	0x0	write_fsm_status_rank0_ds0 FSM monitoring signal for rank0 of data slice 0. It shows cs_wrtrn FSM status in write training.

DDRPHY_MON_CON7

Address: **Operational Base** + offset (0x071C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	rdlvl_fsm_idle_ds1 Idle stat flag of read training for data slice 1
20	RO	0x0	rdlvl_fsm_fisrt_ds1 First state flag of read training for data slice 1
19	RO	0x0	rdlvl_fsm_codeinit_ds1 Code initialization state flag of read training for data slice 1
18	RO	0x0	rdtrn_fsm_second_ds1 Second state flag of read training for data slice 1
17	RO	0x0	rdlvl_fsm_periodic_ds1 Periodic state flag of read training for data slice 1
16	RO	0x0	rdlvl_fsm_resp_ds1 Response state flag of read training for data slice 1
15	RO	0x0	reserved
14:12	RO	0x0	rdlvl_fsm_status_ds1 FSM monitoring signal for data slice 1. It shows cs_rdlvl FSM status in read_training.
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RO	0x0	rdlvl_fsm_idle_ds0 Idle stat flag of read training for data slice 0
8	RO	0x0	rdlvl_fsm_fisrt_ds0 First state flag of read training for data slice 0
7	RO	0x0	rdlvl_fsm_codeinit_ds0 Code initialization state flag of read training for data slice 0
6	RO	0x0	rdlvl_fsm_second_ds0 Second state flag of read training for data slice 0
5	RO	0x0	rdlvl_fsm_periodic_ds0 Periodic state flag of read training for data slice 0
4	RO	0x0	rdlvl_fsm_resp_ds0 Response state flag of read training for data slice 0
3	RO	0x0	reserved
2:0	RO	0x0	rdlvl_fsm_status_ds0 FSM monitoring signal for data slice 0. It shows cs_rdlvl FSM status in read_training.

DDRPHY_WR_TRAIN_MON0

Address: **Operational Base** + offset (0x0720)

Bit	Attr	Reset Value	Description
31	RO	0x0	dvfs_wr_start_status1_cs0 DVFS write training start point status for byte1 at rank0. If this field is high, it indicates that the first access with start point DLL code passed during DVFS write training.
30	RO	0x0	dvfs_wr_start_status0_cs0 DVFS write training start point status for byte0 at rank0. If this field is high, it indicates that the first access with start point DLL code passed during DVFS write training.
29	RO	0x0	dvfs_wr_start_status1_cs1 DVFS write training start point status for byte1 at rank1. If this field is high, it indicates that the first access with start point DLL code passed during DVFS write training.
28	RO	0x0	dvfs_wr_start_status0_cs1 DVFS write training start point status for byte0 at rank1. If this field is high, it indicates that the first access with start point DLL code passed during DVFS write training.
27	RO	0x0	dvfs_wr_max_status1_cs0 DVFS write training max code status for byte1 at rank0. If this field is high, it indicates that DQ/DM bit DLL code reached max code without access pass during DVFS write training.
26	RO	0x0	dvfs_wr_max_status0_cs0 DVFS write training max code status for byte0 at rank0. If this field is high, it indicates that DQ/DM bit DLL code reached max code without access pass during DVFS write training.
25	RO	0x0	dvfs_wr_max_status1_cs1 DVFS write training max code status for byte1 at rank1. If this field is high, it indicates that DQ/DM bit DLL code reached max code without access pass during DVFS write training.
24	RO	0x0	dvfs_wr_max_status0_cs1 DVFS write training max code status for byte0 at rank1. If this field is high, it indicates that DQ/DM bit DLL code reached max code without access pass during DVFS write training.
23:0	RO	0x000000	reserved

DDRPHY_LOCK_VAL0

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Address: **Operational Base** + offset (0x0728)

Bit	Attr	Reset Value	Description
31	RO	0x0	dvfs0_locked_release ctrl_locked release indicator for DVFS mode 0. It will be detected locked release after finished relock.
30	RO	0x0	dvfs0_harmonic_err Harmonic lock error indicator for DVFS mode 0. Valid only when the core voltage is not changed.
29:20	RO	0x001	dvfs0_relock_value DLL re-lock value for DVFS mode 0. If mdll_monitor_en is high, it will be updated to ctrl_lock_value after DLL relocking that occurs during the frequency change with DVFS mode 0.
19:10	RO	0x3ff	dvfs0_lock_value_min Minimum lock value for DVFS mode 0. If mdll_monitor_en is high, it shows the minimum ctrl_lock_value during the normal operation with DVFS mode 0, except for the frequency change duration.
9:0	RO	0x001	dvfs0_lock_value_max Maximum lock value for DVFS mode 0. If mdll_monitor_en is high, it shows the maximum ctrl_lock_value during the normal operation with DVFS mode 0, except for the frequency change duration.

DDRPHY_LOCK_VAL1

Address: **Operational Base** + offset (0x072C)

Bit	Attr	Reset Value	Description
31	RO	0x0	dvfs1_locked_release ctrl_locked release indicator for DVFS mode 1. It will be detected locked release after finished relock.
30	RO	0x0	dvfs1_harmonic_err Harmonic lock error indicator for DVFS mode 1. Valid only when the core voltage is not changed.
29:20	RO	0x001	dvfs1_relock_value DLL re-lock value for DVFS mode 1. If mdll_monitor_en is high, It will be updated to ctrl_lock_value after DLL relocking that occurs during the frequency change with DVFS mode 1.
19:10	RO	0x3ff	dvfs1_lock_value_min Minimum lock value for DVFS mode 1. If mdll_monitor_en is high, it shows the minimum ctrl_lock_value during the normal operation with DVFS mode 1, except for the frequency change duration.
9:0	RO	0x001	dvfs1_lock_value_max Maximum lock value for DVFS mode 1. If mdll_monitor_en is high, it shows the maximum ctrl_lock_value during the normal operation with DVFS mode 1, except for the frequency change duration.

DDRPHY_LOCK_VAL2

Address: **Operational Base** + offset (0x0730)

Bit	Attr	Reset Value	Description
31	RO	0x0	locked_release ctrl_locked release indicator for normal mode 1. It will be detected locked release after finished relock.
30	RO	0x0	harmonic_err Harmonic lock error indicator for normal mode. Valid only when the core voltage is not changed.

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Bit	Attr	Reset Value	Description
29:20	RO	0x001	relock_value DLL re-lock value for normal mode. If mdll_monitor_en is high, it will be updated to ctrl_lock_value after DLL relocking that occurs during the frequency change with normal mode (dvfs_mode = 'h0).
19:10	RO	0x3ff	lock_value_min Minimum lock value for normal mode. If mdll_monitor_en is high, it shows the minimum ctrl_lock_value during the normal operation with normal mode (dvfs_mode = 'h0), except for the frequency change duration.
9:0	RO	0x001	lock_value_max Maximum lock value for normal mode. If mdll_monitor_en is high, it shows the maximum ctrl_lock_value during the normal operation with normal mode (dvfs_mode = 'h0), except for the frequency change duration.

DDRPHY_WR_CHECK_CON0

Address: **Operational Base** + offset (0x0750)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RO	0x0	wptr_ds0 FIFO write pointer in data slice 0. This field is valid when debug_mode_en is high.
23:20	RO	0x0	reserved
19:16	RO	0x0	rptr_ds0 FIFO read pointer in data slice 0. This field is valid when debug_mode_en is high.
15:9	RO	0x00	reserved
8	RO	0x0	fifo_err_ds0 FiFO error status in data slice 0. This field is valid when debug_mode_en is high. It will be updated when dfi_ctrlupd_ack rises, dfi_phyupd_ack rises or dfi_init_start rises. It will be asserted high if wptr_h_ds0 != rptr_h_ds0 or wptr_l_ds0 != rptr_l_ds0. If it is asserted high, dfi_init_complete will be set to low.
7:6	RO	0x0	gate_rise_monitor_ds0 Gate detector at dqs rising edge in data slice 0. debug_mode_en should be set high to make this register valid.
5:4	RO	0x0	gate_fall_monitor_ds0 Gate detector at dqs falling edge in data slice 0. debug_mode_en should be set high to make this register valid.
3:0	RO	0x0	reserved

DDRPHY_WR_CHECK_CON1

Address: **Operational Base** + offset (0x0754)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RO	0x0	wptr_ds1 FIFO write pointer in data slice 1. This field is valid when debug_mode_en is high.
23:20	RO	0x0	reserved
19:16	RO	0x0	rptr_ds1 FIFO read pointer in data slice 1. This field is valid when debug_mode_en is high.
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8	RO	0x0	fifo_err_ds1 FiFO error status in data slice 1. This field is valid when debug_mode_en is high. It will be updated when dfi_ctrlupd_ack rises, dfi_phyupd_ack rises or dfi_init_start rises. It will be asserted high if wptr_h_ds1 != rptr_h_ds1 or wptr_l_ds1 != rptr_l_ds1. If it is asserted high, dfi_init_complete will be set to low.
7:6	RO	0x0	gate_rise_monitor_ds1 Gate detector at dqs rising edge in data slice 1. debug_mode_en should be set high to make this register valid.
5:4	RO	0x0	gate_fall_monitor_ds1 Gate detector at dqs falling edge in data slice 1. debug_mode_en should be set high to make this register valid.
3:0	RO	0x0	reserved

DDRPHY_WR_CHECK_CON2

Address: **Operational Base** + offset (0x0760)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Read_command_counter_ds1 Read command counter in data slice 1 This field is valid when debug_mode_en is high.
23:16	RO	0x00	Read_command_counter_ds0 Read command counter in data slice 0 This field is valid when debug_mode_en is high.
15:0	RO	0x0000	reserved

DDRPHY_RD_DQS_VWML_CS1_CON0

Address: **Operational Base** + offset (0x0764)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RO	0x000	RDDQSVWML1_cs1 Read DQS left code for data slice 1
15:9	RO	0x00	reserved
8:0	RO	0x000	RDDQSVWML0_cs1 Read DQS left code for data slice 0

DDRPHY_RD_DQS_VWMC_CS1_CON0

Address: **Operational Base** + offset (0x0768)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RO	0x000	RDDQSVWMC1_cs1 Read DQS center code for data slice 1
15:9	RO	0x00	reserved
8:0	RO	0x000	RDDQSVWMC0_cs1 Read DQS center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS1_CON_DM

Address: **Operational Base** + offset (0x076C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RDDMDeskewC1_cs1 Read DMI de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RDDMDeskewC0_cs1 Read DMI de-skew center code for data slice 0

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DDRPHY_RD_DESKEW_CENTER_CS1_CON0

Address: **Operational Base** + offset (0x0770)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD0DeskewC1_cs1 Read DQ0 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD0DeskewC0_cs1 Read DQ0 de-skew center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS1_CON1

Address: **Operational Base** + offset (0x0774)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD1DeskewC1_cs1 Read DQ1 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD1DeskewC0_cs1 Read DQ1 de-skew center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS1_CON2

Address: **Operational Base** + offset (0x0778)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD2DeskewC1_cs1 Read DQ2 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD2DeskewC0_cs1 Read DQ2 de-skew center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS1_CON3

Address: **Operational Base** + offset (0x077C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD3DeskewC1_cs1 Read DQ3 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD3DeskewC0_cs1 Read DQ3 de-skew center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS1_CON4

Address: **Operational Base** + offset (0x0780)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD4DeskewC1_cs1 Read DQ4 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD4DeskewC0_cs1 Read DQ4 de-skew center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS1_CON5

Address: **Operational Base** + offset (0x0784)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RO	0x000	RD5DeskewC1_cs1 Read DQ5 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD5DeskewC0_cs1 Read DQ5 de-skew center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS1_CON6

Address: **Operational Base** + offset (0x0788)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD6DeskewC1_cs1 Read DQ6 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD6DeskewC0_cs1 Read DQ6 de-skew center code for data slice 0

DDRPHY_RD_DESKEW_CENTER_CS1_CON7

Address: **Operational Base** + offset (0x078C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD7DeskewC1_cs1 Read DQ7 de-skew center code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD7DeskewC0_cs1 Read DQ7 de-skew center code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS1_CON_DM

Address: **Operational Base** + offset (0x0790)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RDDMDeskewLeft1_cs1 Read DMI de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RDDMDeskewLeft0_cs1 Read DMI de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS1_CON0

Address: **Operational Base** + offset (0x0794)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD0DeskewLeft1_cs1 Read DQ0 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD0DeskewLeft0_cs1 Read DQ0 de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS1_CON1

Address: **Operational Base** + offset (0x0798)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD1DeskewLeft1_cs1 Read DQ1 de-skew left code for data slice 1
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	RD1DeskewLeft0_cs1 Read DQ1 de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS1_CON2

Address: **Operational Base** + offset (0x079C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD2DeskewLeft1_cs1 Read DQ2 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD2DeskewLeft0_cs1 Read DQ2 de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS1_CON3

Address: **Operational Base** + offset (0x07A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD3DeskewLeft1_cs1 Read DQ3 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD3DeskewLeft0_cs1 Read DQ3 de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS1_CON4

Address: **Operational Base** + offset (0x07A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD4DeskewLeft1_cs1 Read DQ4 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD4DeskewLeft0_cs1 Read DQ4 de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS1_CON5

Address: **Operational Base** + offset (0x07A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD5DeskewLeft1_cs1 Read DQ5 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD5DeskewLeft0_cs1 Read DQ5 de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS1_CON6

Address: **Operational Base** + offset (0x07AC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD6DeskewLeft1_cs1 Read DQ6 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD6DeskewLeft0_cs1 Read DQ6 de-skew left code for data slice 0

DDRPHY_RD_DESKEW_LEFT_CS1_CON7

Address: **Operational Base** + offset (0x07B0)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	RD7DeskewLeft1_cs1 Read DQ7 de-skew left code for data slice 1
15:10	RO	0x00	reserved
9:0	RO	0x000	RD7DeskewLeft0_cs1 Read DQ7 de-skew left code for data slice 0

DDRPHY_SW_RD_DQS_VWML_CS0_CON0

Address: **Operational Base** + offset (0x07C0)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	SW_RDDQSVWML1_cs0 SW read DQS left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:9	RO	0x00	reserved
8:0	RW	0x000	SW_RDDQSVWML0_cs0 SW read DQS left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DQS_VWMC_CS0_CON0

Address: **Operational Base** + offset (0x07C4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	SW_RDDQSVWMC1_cs0 SW read DQS center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:9	RO	0x00	reserved
8:0	RW	0x000	SW_RDDQSVWMC0_cs0 SW read DQS center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON_DM

Address: **Operational Base** + offset (0x07C8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RDDMDeskewC1_cs0 SW read DMI de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_RDDMDeskewC0_cs0 SW read DMI de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON0

Address: **Operational Base** + offset (0x07CC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD0DeskewC1_cs0 SW read DQ0 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD0DeskewC0_cs0 SW read DQ0 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON1

Address: **Operational Base** + offset (0x07D0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD1DeskewC1_cs0 SW read DQ1 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD1DeskewC0_cs0 SW read DQ1 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON2

Address: **Operational Base** + offset (0x07D4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD2DeskewC1_cs0 SW read DQ2 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_RD2DeskewC0_cs0 SW read DQ2 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON3

Address: **Operational Base** + offset (0x07D8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD3DeskewC1_cs0 SW read DQ3 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD3DeskewC0_cs0 SW read DQ3 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON4

Address: **Operational Base** + offset (0x07DC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD4DeskewC1_cs0 SW read DQ4 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD4DeskewC0_cs0 SW read DQ4 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON5

Address: **Operational Base** + offset (0x07E0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD5DeskewC1_cs0 SW read DQ5 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_RD5DeskewC0_cs0 SW read DQ5 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON6

Address: **Operational Base** + offset (0x07E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD6DeskewC1_cs0 SW read DQ6 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD6DeskewC0_cs0 SW read DQ6 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON7

Address: **Operational Base** + offset (0x07E8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD7DeskewC1_cs0 SW read DQ7 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD7DeskewC0_cs0 SW read DQ7 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON_DM

Address: **Operational Base** + offset (0x07F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RDDMDeskewLeft1_cs0 SW read DMI de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_RDDMDeskewLeft0_cs0 SW read DMI de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON0

Address: **Operational Base** + offset (0x07F4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD0DeskewLeft1_cs0 SW read DQ0 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD0DeskewLeft0_cs0 SW read DQ0 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON1

Address: **Operational Base** + offset (0x07F8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD1DeskewLeft1_cs0 SW read DQ1 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD1DeskewLeft0_cs0 SW read DQ1 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON2

Address: **Operational Base** + offset (0x07FC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD2DeskewLeft1_cs0 SW read DQ2 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_RD2DeskewLeft0_cs0 SW read DQ2 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON3

Address: **Operational Base** + offset (0x0800)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD3DeskewLeft1_cs0 SW read DQ3 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD3DeskewLeft0_cs0 SW read DQ3 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON4

Address: **Operational Base** + offset (0x0804)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD4DeskewLeft1_cs0 SW read DQ4 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD4DeskewLeft0_cs0 SW read DQ4 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON5

Address: **Operational Base** + offset (0x0808)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD5DeskewLeft1_cs0 SW read DQ5 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_RD5DeskewLeft0_cs0 SW read DQ5 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON6

Address: **Operational Base** + offset (0x080C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD6DeskewLeft1_cs0 SW read DQ6 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD6DeskewLeft0_cs0 SW read DQ6 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON7

Address: **Operational Base** + offset (0x0810)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD7DeskewLeft1_cs0 SW read DQ7 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD7DeskewLeft0_cs0 SW read DQ7 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DQS_VWML_CS1_CON0

Address: **Operational Base** + offset (0x0814)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	SW_RDDQSVWML1_cs1 SW read DQS left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8:0	RW	0x000	SW_RDDQSVWML0_cs1 SW read DQS left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DQS_VWMC_CS1_CON0

Address: **Operational Base** + offset (0x0818)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	SW_RDDQSVWMC1_cs1 SW read DQS center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:9	RO	0x00	reserved
8:0	RW	0x000	SW_RDDQSVWMC0_cs1 SW read DQS center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON_DM

Address: **Operational Base** + offset (0x0820)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RDDMDeskewC1_cs1 SW read DMI de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RDDMDeskewC0_cs1 SW read DMI de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON0

Address: **Operational Base** + offset (0x0824)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD0DeskewC1_cs1 SW read DQ0 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_RD0DeskewC0_cs1 SW read DQ0 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON1

Address: **Operational Base** + offset (0x0828)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD1DeskewC1_cs1 SW read DQ1 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD1DeskewC0_cs1 SW read DQ1 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON2

Address: **Operational Base** + offset (0x082C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD2DeskewC1_cs1 SW read DQ2 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD2DeskewC0_cs1 SW read DQ2 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON3

Address: **Operational Base** + offset (0x0830)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD3DeskewC1_cs1 SW read DQ3 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_RD3DeskewC0_cs1 SW read DQ3 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON4

Address: **Operational Base** + offset (0x0834)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD4DeskewC1_cs1 SW read DQ4 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD4DeskewC0_cs1 SW read DQ4 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON5

Address: **Operational Base** + offset (0x0838)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD5DeskewC1_cs1 SW read DQ5 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD5DeskewC0_cs1 SW read DQ5 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON6

Address: **Operational Base** + offset (0x083C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD6DeskewC1_cs1 SW read DQ6 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_RD6DeskewC0_cs1 SW read DQ6 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON7

Address: **Operational Base** + offset (0x0840)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD7DeskewC1_cs1 SW read DQ7 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD7DeskewC0_cs1 SW read DQ7 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON_DM

Address: **Operational Base** + offset (0x0850)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RDDMDeskewLeft1_cs1 SW read DMI de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RDDMDeskewLeft0_cs1 SW read DMI de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON0

Address: **Operational Base** + offset (0x0854)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD0DeskewLeft1_cs1 SW read DQ0 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_RD0DeskewLeft0_cs1 SW read DQ0 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON1

Address: **Operational Base** + offset (0x0858)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD1DeskewLeft1_cs1 SW read DQ1 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD1DeskewLeft0_cs1 SW read DQ1 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON2

Address: **Operational Base** + offset (0x085C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD2DeskewLeft1_cs1 SW read DQ2 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD2DeskewLeft0_cs1 SW read DQ2 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON3

Address: **Operational Base** + offset (0x0860)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD3DeskewLeft1_cs1 SW read DQ3 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_RD3DeskewLeft0_cs1 SW read DQ3 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON4

Address: **Operational Base** + offset (0x0864)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD4DeskewLeft1_cs1 SW read DQ4 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD4DeskewLeft0_cs1 SW read DQ4 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON5

Address: **Operational Base** + offset (0x0868)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD5DeskewLeft1_cs1 SW read DQ5 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD5DeskewLeft0_cs1 SW read DQ5 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON6

Address: **Operational Base** + offset (0x086C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD6DeskewLeft1_cs1 SW read DQ6 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_RD6DeskewLeft0_cs1 SW read DQ6 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON7

Address: **Operational Base** + offset (0x0870)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_RD7DeskewLeft1_cs1 SW read DQ7 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_RD7DeskewLeft0_cs1 SW read DQ7 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore read training result with rd_sw_mode=1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON0

Address: **Operational Base** + offset (0x0880)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR0DeskewC1_cs0 SW write DQ0 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR0DeskewC0_cs0 SW write DQ0 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON1

Address: **Operational Base** + offset (0x0884)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR1DeskewC1_cs0 SW write DQ1 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_WR1DeskewC0_cs0 SW write DQ1 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON2

Address: **Operational Base** + offset (0x0888)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR2DeskewC1_cs0 SW write DQ2 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR2DeskewC0_cs0 SW write DQ2 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON3

Address: **Operational Base** + offset (0x088C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR3DeskewC1_cs0 SW write DQ3 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR3DeskewC0_cs0 SW write DQ3 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON4

Address: **Operational Base** + offset (0x0890)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR4DeskewC1_cs0 SW write DQ4 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_WR4DeskewC0_cs0 SW write DQ4 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON5

Address: **Operational Base** + offset (0x0894)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR5DeskewC1_cs0 SW write DQ5 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR5DeskewC0_cs0 SW write DQ5 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON6

Address: **Operational Base** + offset (0x0898)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR6DeskewC1_cs0 SW write DQ6 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR6DeskewC0_cs0 SW write DQ6 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON7

Address: **Operational Base** + offset (0x089C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR7DeskewC1_cs0 SW write DQ7 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_WR7DeskewC0_cs0 SW write DQ7 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_DM_DESKEWC_CS0_CON0

Address: **Operational Base** + offset (0x08A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WRDMDeskewC1_cs0 SW write DM de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WRDMDeskewC0_cs0 SW write DM de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON0

Address: **Operational Base** + offset (0x08B0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR0DeskewL1_cs0 SW write DQ0 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR0DeskewL0_cs0 SW write DQ0 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON1

Address: **Operational Base** + offset (0x08B4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR1DeskewL1_cs0 SW write DQ1 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_WR1DeskewL0_cs0 SW write DQ1 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON2

Address: **Operational Base** + offset (0x08B8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR2DeskewL1_cs0 SW write DQ2 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR2DeskewL0_cs0 SW write DQ2 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON3

Address: **Operational Base** + offset (0x08BC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR3DeskewL1_cs0 SW write DQ3 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR3DeskewL0_cs0 SW write DQ3 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON4

Address: **Operational Base** + offset (0x08C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR4DeskewL1_cs0 SW write DQ4 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_WR4DeskewL0_cs0 SW write DQ4 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON5

Address: **Operational Base** + offset (0x08C4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR5DeskewL1_cs0 SW write DQ5 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR5DeskewL0_cs0 SW write DQ5 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON6

Address: **Operational Base** + offset (0x08C8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR6DeskewL1_cs0 SW write DQ6 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR6DeskewL0_cs0 SW write DQ6 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON7

Address: **Operational Base** + offset (0x08CC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR7DeskewL1_cs0 SW write DQ7 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_WR7DeskewL0_cs0 SW write DQ7 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DM_DESKEWL_CS0_CON0

Address: **Operational Base** + offset (0x08D0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WRDMDeskewL1_cs0 SW write DM de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WRDMDeskewL0_cs0 SW write DM de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON0

Address: **Operational Base** + offset (0x08E0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR0DeskewC1_cs1 SW write DQ0 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR0DeskewC0_cs1 SW write DQ0 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON1

Address: **Operational Base** + offset (0x08E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR1DeskewC1_cs1 SW write DQ1 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_WR1DeskewC0_cs1 SW write DQ1 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON2

Address: **Operational Base** + offset (0x08E8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR2DeskewC1_cs1 SW write DQ2 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR2DeskewC0_cs1 SW write DQ2 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON3

Address: **Operational Base** + offset (0x08EC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR3DeskewC1_cs1 SW write DQ3 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR3DeskewC0_cs1 SW write DQ3 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON4

Address: **Operational Base** + offset (0x08F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR4DeskewC1_cs1 SW write DQ4 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_WR4DeskewC0_cs1 SW write DQ4 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON5

Address: **Operational Base** + offset (0x08F4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR5DeskewC1_cs1 SW write DQ5 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR5DeskewC0_cs1 SW write DQ5 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON6

Address: **Operational Base** + offset (0x08F8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR6DeskewC1_cs1 SW write DQ6 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR6DeskewC0_cs1 SW write DQ6 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON7

Address: **Operational Base** + offset (0x08FC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR7DeskewC1_cs1 SW write DQ7 de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_WR7DeskewC0_cs1 SW write DQ7 de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DM_DESKEWC_CS1_CON0

Address: **Operational Base** + offset (0x0900)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WRDMDeskewC1_cs1 SW write DM de-skew center code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WRDMDeskewC0_cs1 SW write DM de-skew center code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON0

Address: **Operational Base** + offset (0x0910)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR0DeskewL1_cs1 SW write DQ0 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR0DeskewL0_cs1 SW write DQ0 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON1

Address: **Operational Base** + offset (0x0914)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR1DeskewL1_cs1 SW write DQ1 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_WR1DeskewL0_cs1 SW write DQ1 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON2

Address: **Operational Base** + offset (0x0918)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR2DeskewL1_cs1 SW write DQ2 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR2DeskewL0_cs1 SW write DQ2 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON3

Address: **Operational Base** + offset (0x091C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR3DeskewL1_cs1 SW write DQ3 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR3DeskewL0_cs1 SW write DQ3 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON4

Address: **Operational Base** + offset (0x0920)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR4DeskewL1_cs1 SW write DQ4 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_WR4DeskewL0_cs1 SW write DQ4 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON5

Address: **Operational Base** + offset (0x0924)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR5DeskewL1_cs1 SW write DQ5 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR5DeskewL0_cs1 SW write DQ5 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON6

Address: **Operational Base** + offset (0x0928)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR6DeskewL1_cs1 SW write DQ6 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WR6DeskewL0_cs1 SW write DQ6 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON7

Address: **Operational Base** + offset (0x092C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WR7DeskewL1_cs1 SW write DQ7 de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	SW_WR7DeskewL0_cs1 SW write DQ7 de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_DM_DESKEWL_CS1_CON0

Address: **Operational Base** + offset (0x0930)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	SW_WRDMDeskewL1_cs1 SW write DM de-skew left code for data slice 1. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.
15:10	RO	0x00	reserved
9:0	RW	0x000	SW_WRDMDeskewL0_cs1 SW write DM de-skew left code for data slice 0. Write to this register in following 2 situations. (1) To restore write training result with wr_sw_mode = 1. (2) Before DVFS pause to apply training result for the next DVFS level.

DDRPHY_DVFS0_CON5

Address: **Operational Base** + offset (0x0934)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	dvfs0_shiftc1 Gate signal delay amount for DDR. This is used to adjust gate delay based on DFI PHY clock period. When gate_debug_en[3] = 1 for gate margin control. When gate_cal_mode = 0 for debug purpose in DVFS0 mode. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes high and low. This value is limited by the half of the maximum delay in master delay line. 3'b000: 0 (0 degree shift) 3'b001: T (365 degree shift) 3'b010: T/2 (180 degree shift) 3'b011: T/4 (90 degree shift) 3'b100: T/8 (45 degree shift) 3'b101: T/16 (22.5 degree shift) 3'b111: 3T/4 (270 degree shift)
27	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
26:24	RW	0x0	dvfs0_shiftc0 Gate signal delay amount for DDR. This is used to adjust gate delay based on DFI PHY clock period. When gate_debug_en[3] = 1 for gate margin control. When gate_cal_mode = 0 for debug purpose in DVFS0 mode. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes high and low. This value is limited by the half of the maximum delay in master delay line. 3'b000: 0 (0 degree shift) 3'b001: T (365 degree shift) 3'b010: T/2 (180 degree shift) 3'b011: T/4 (90 degree shift) 3'b100: T/8 (45 degree shift) 3'b101: T/16 (22.5 degree shift) 3'b111: 3T/4 (270 degree shift)
23	RO	0x0	reserved
22:16	RW	0x00	dvfs0_glvl_periodic_fine_incr_adj Periodic (or short) gate training step size at fine mode for DVFS0 mode. It should be smaller than 7'h1F. Default value is 7'b0000000 (T/16). [22:21]=2'b00: The step value will be "dvfs0_glvl_periodic_fine_incr_adj[4:0]". [22:21]=2'b01: The step value will be "T/32". [22:21]=2'b10: The step value will be "T/4". [22:21]=2'b11: The step value will be "T/8". [22:16]=7'h00: The step value will be "T/16" (default).
15:14	RO	0x0	reserved
13	RW	0x0	dvfs0_cmdfifo_wl_ext This field determines command FIFO write latency extension mode for auto dqs clean on DVFS0. ONLY use at LPDDR5. If this field set to 1, PHY can support RL = 21 in LPDDR5.
12	RW	0x0	dvfs0_long_gate_train_mode Gate training mode by long gate (shgate =0) for DVFS0 mode
11	RW	0x0	dvfs0_gt_fine_disable Gate training fine mode disable for DVFS0 mode
10:8	RW	0x0	dvfs0_glvl_start_adj Gate training start point adjustment for DVFS0 mode. This field adjusts the initial code provided to the gate delay line at the beginning of periodic gate training. [10:8]=2'b000: The start point code is -T from the first DQS rising edge. [10:8]=2'b001: The start point code is -7T/8 from the first DQS rising edge. [10:8]=2'b010: The start point code is -6T/8 from the first DQS rising edge. [10:8]=2'b011: The start point code is -5T/8 from the first DQS rising edge. [10:8]=2'b100: The start point code is -4T/8 from the first DQS rising edge. [10:8]=2'b101: The start point code is -3T/8 from the first DQS rising edge. [10:8]=2'b110: The start point code is -2T/8 from the first DQS rising edge. [10:8]=2'b111: The start point code is -T/8 from the first DQS rising edge.

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Bit	Attr	Reset Value	Description
7:0	RW	0x40	dvfs0_glvl_periodic_incr_adj Periodic (or short) gate training step size for DVFS0 mode. It should be smaller than 7'h1F. Default value is 7'b1000000 (T/4). [6:5]=2'b00: The step value will be "dvfs0_glvl_periodic_incr_adj[4:0]". [6:5]=2'b01: The step value will be "T/32". [6:5]=2'b10: The step value will be "T/4" (default). [6:5]=2'b11: The step value will be "T/8". [6:0]=7'h00: The step value will be "T/16".

DDRPHY_DVFS1_CON5

Address: **Operational Base** + offset (0x0938)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	dvfs1_shiftc1 Gate signal delay amount for DDR. This is used to adjust gate delay based on DFI PHY clock period. When gate_debug_en[3] = 1 for gate margin control. When gate_cal_mode = 0 for debug purpose in DVFS1 mode. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes high and low. This value is limited by the half of the maximum delay in master delay line. 3'b000: 0 (0 degree shift) 3'b001: T (365 degree shift) 3'b010: T/2 (180 degree shift) 3'b011: T/4 (90 degree shift) 3'b100: T/8 (45 degree shift) 3'b101: T/16 (22.5 degree shift) 3'b111: 3T/4 (270 degree shift)
27	RO	0x0	reserved
26:24	RW	0x0	dvfs1_shiftc0 Gate signal delay amount for DDR. This is used to adjust gate delay based on DFI PHY clock period. When gate_debug_en[3] = 1 for gate margin control. When gate_cal_mode = 0 for debug purpose in DVFS1 mode. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes high and low. This value is limited by the half of the maximum delay in master delay line. 3'b000: 0 (0 degree shift) 3'b001: T (365 degree shift) 3'b010: T/2 (180 degree shift) 3'b011: T/4 (90 degree shift) 3'b100: T/8 (45 degree shift) 3'b101: T/16 (22.5 degree shift) 3'b111: 3T/4 (270 degree shift)
23	RO	0x0	reserved
22:16	RW	0x00	dvfs1_glvl_periodic_fine_incr_adj Periodic gate training step size at fine mode for DVFS1 mode. It should be smaller than 7'h1F. Default value is 7'b0000000 (T/16). [22:21]=2'b00: The step value will be "dvfs1_glvl_periodic_fine_incr_adj[4:0]". [22:21]=2'b01: The step value will be "T/32". [22:21]=2'b10: The step value will be "T/4". [22:21]=2'b11: The step value will be "T/8".

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Bit	Attr	Reset Value	Description
			[22:16]=7'h00: The step value will be "T/16" (default).
15:14	RO	0x0	reserved
13	RW	0x0	dvfs1_cmdfifo_wl_ext This field determines command FIFO write latency extension mode for auto dqs clean on DVFS1. ONLY use at LPDDR5. If this field set to 1, PHY can support RL = 21 in LPDDR5.
12	RW	0x0	dvfs1_long_gate_train_mode Gate training mode by long gate (shgate =0) for DVFS1 mode
11	RW	0x0	dvfs1_gt_fine_disable Gate training fine mode disable for DVFS1 mode
10:8	RW	0x0	dvfs1_glvl_start_adj Gate training start point adjustment for DVFS1 mode. This field adjusts the initial code provided to the gate delay line at the beginning of periodic gate training. [10:8]=2'b000: The start point code is -T from the first DQS rising edge. [10:8]=2'b001: The start point code is -7T/8 from the first DQS rising edge. [10:8]=2'b010: The start point code is -6T/8 from the first DQS rising edge. [10:8]=2'b011: The start point code is -5T/8 from the first DQS rising edge. [10:8]=2'b100: The start point code is -4T/8 from the first DQS rising edge. [10:8]=2'b101: The start point code is -3T/8 from the first DQS rising edge. [10:8]=2'b110: The start point code is -2T/8 from the first DQS rising edge. [10:8]=2'b111: The start point code is -T/8 from the first DQS rising edge.
7:0	RW	0x40	dvfs1_glvl_periodic_incr_adj Periodic (or short) gate training step size for DVFS1 mode. It should be smaller than 7'h1F. Default value is 7'b1000000 (T/4). [6:5]=2'b00: The step value will be "dvfs1_glvl_periodic_incr_adj[4:0]". [6:5]=2'b01: The step value will be "T/32". [6:5]=2'b10: The step value will be "T/4" (default). [6:5]=2'b11: The step value will be "T/8". [6:0]=7'h00: The step value will be "T/16".

DDRPHY_CAL_WR_PATTERN_CON5

Address: **Operational Base** + offset (0x093C)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst1_8_2nd This fields specifies the DQ pattern for BL1 and BL2 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the first valid rising edge of DQS. wrtrn_rddata_adj_w0_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the first valid falling edge of DQS.

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Bit	Attr	Reset Value	Description
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst1_8_2nd This fields specifies the DQ pattern for BL3 and BL4 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the second valid rising edge of DQS. wrtrn_rddata_adj_w1_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the second valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON6

Address: **Operational Base** + offset (0x0940)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst1_8_2nd This fields specifies the DQ pattern for BL5 and BL6 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid rising edge of DQS. wrtrn_rddata_adj_w0_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst1_8_2nd This fields specifies the DQ pattern for BL7 and BL8 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON7

Address: **Operational Base** + offset (0x0944)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst9_16_2nd This fields specifies the DQ pattern for BL9 and BL10 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid rising edge of DQS. wrtrn_rddata_adj_w0_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst9_16_2nd This fields specifies the DQ pattern for BL11 and BL12 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON8

Address: **Operational Base** + offset (0x0948)

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Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst9_16_2nd This fields specifies the DQ pattern for BL13 and BL14 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid rising edge of DQS. wrtrn_rddata_adj_w0_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst9_16_2nd This fields specifies the DQ pattern for BL15 and BL16 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON9

Address: **Operational Base** + offset (0x094C)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst1_8_3rd This fields specifies the DQ pattern for BL1 and BL2 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the first valid rising edge of DQS. wrtrn_rddata_adj_w0_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the first valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst1_8_3rd This fields specifies the DQ pattern for BL3 and BL4 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the second valid rising edge of DQS. wrtrn_rddata_adj_w1_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the second valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON10

Address: **Operational Base** + offset (0x0950)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst1_8_3rd This fields specifies the DQ pattern for BL5 and BL6 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid rising edge of DQS. wrtrn_rddata_adj_w0_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid falling edge of DQS.

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Bit	Attr	Reset Value	Description
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst1_8_3rd This fields specifies the DQ pattern for BL7 and BL8 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON11

Address: **Operational Base** + offset (0x0954)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst9_16_3rd This fields specifies the DQ pattern for BL9 and BL10 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid rising edge of DQS. wrtrn_rddata_adj_w0_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst9_16_3rd This fields specifies the DQ pattern for BL11 and BL12 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON12

Address: **Operational Base** + offset (0x0958)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst9_16_3rd This fields specifies the DQ pattern for BL13 and BL14 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid rising edge of DQS. wrtrn_rddata_adj_w0_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst9_16_3rd This fields specifies the DQ pattern for BL15 and BL16 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON13

Address: **Operational Base** + offset (0x095C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst1_8_4th This fields specifies the DQ pattern for BL1 and BL2 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the first valid rising edge of DQS. wrtrn_rddata_adj_w0_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the first valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst1_8_4th This fields specifies the DQ pattern for BL3 and BL4 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the second valid rising edge of DQS. wrtrn_rddata_adj_w1_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the second valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON14

Address: **Operational Base** + offset (0x0960)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst1_8_4th This fields specifies the DQ pattern for BL5 and BL6 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid rising edge of DQS. wrtrn_rddata_adj_w0_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst1_8_4th This fields specifies the DQ pattern for BL7 and BL8 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON15

Address: **Operational Base** + offset (0x0964)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst9_16_4th This fields specifies the DQ pattern for BL9 and BL10 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid rising edge of DQS. wrtrn_rddata_adj_w0_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid falling edge of DQS.

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Bit	Attr	Reset Value	Description
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst9_16_4th This fields specifies the DQ pattern for BL11 and BL12 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON16

Address: **Operational Base** + offset (0x0968)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst9_16_4th This fields specifies the DQ pattern for BL13 and BL14 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w0_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid rising edge of DQS. wrtrn_rddata_adj_w0_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst9_16_4th This fields specifies the DQ pattern for BL15 and BL16 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data slices. wrtrn_rddata_adj_w1_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON17

Address: **Operational Base** + offset (0x096C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x1	wrtrn_rddata_dm_adj_w0_bst1_8_2nd This fields specifies the DM pattern for BL1 and BL2 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase0[0] represents expected data of DM[0] and DQ[1] at the first valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase0[1] represents expected data of DM[0] and DM[1] at the first valid falling edge of DQS.
13:12	RW	0x1	wrtrn_rddata_dm_adj_w1_bst1_8_2nd This fields specifies the DM pattern for BL3 and BL4 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase0[0] represents expected data of DM[0] and DQ[1] at the second valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase0[1] represents expected data of DM[0] and DM[1] at the second valid falling edge of DQS.

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Bit	Attr	Reset Value	Description
11:10	RW	0x1	wrtrn_rddata_dm_adj_w2_bst1_8_2nd This fields specifies the DM pattern for BL5 and BL6 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase1[0] represents expected data of DM[0] and DQ[1] at the 3rd valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase1[1] represents expected data of DM[0] and DM[1] at the 3rd valid falling edge of DQS.
9:8	RW	0x1	wrtrn_rddata_dm_adj_w3_bst1_8_2nd This fields specifies the DM pattern for BL7 and BL8 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase1[0] represents expected data of DM[0] and DQ[1] at the 4th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase1[1] represents expected data of DM[0] and DM[1] at the 4th valid falling edge of DQS.
7:6	RW	0x1	wrtrn_rddata_dm_adj_w0_bst9_16_2nd This fields specifies the DM pattern for BL9 and BL10 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DQ[1] at the 5th valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DM[1] at the 5th valid falling edge of DQS.
5:4	RW	0x1	wrtrn_rddata_dm_adj_w1_bst9_16_2nd This fields specifies the DM pattern for BL11 and BL12 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DQ[1] at the 6th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DM[1] at the 6th valid falling edge of DQS.
3:2	RW	0x1	wrtrn_rddata_dm_adj_w2_bst9_16_2nd This fields specifies the DM pattern for BL13 and BL14 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DQ[1] at the 7th valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DM[1] at the 7th valid falling edge of DQS.
1:0	RW	0x1	wrtrn_rddata_dm_adj_w3_bst9_16_2nd This fields specifies the DM pattern for BL15 and BL16 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DQ[1] at the 8th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DM[1] at the 8th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON18

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Address: **Operational Base** + offset (0x0970)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x1	wrtrn_rddata_dm_adj_w0_bst1_8_3rd This fields specifies the DM pattern for BL1 and BL2 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase0[0] represents expected data of DM[0] and DQ[1] at the first valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase0[1] represents expected data of DM[0] and DM[1] at the first valid falling edge of DQS.
13:12	RW	0x1	wrtrn_rddata_dm_adj_w1_bst1_8_3rd This fields specifies the DM pattern for BL3 and BL4 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase0[0] represents expected data of DM[0] and DQ[1] at the second valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase0[1] represents expected data of DM[0] and DM[1] at the second valid falling edge of DQS.
11:10	RW	0x1	wrtrn_rddata_dm_adj_w2_bst1_8_3rd This fields specifies the DM pattern for BL5 and BL6 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase1[0] represents expected data of DM[0] and DQ[1] at the 3rd valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase1[1] represents expected data of DM[0] and DM[1] at the 3rd valid falling edge of DQS.
9:8	RW	0x1	wrtrn_rddata_dm_adj_w3_bst1_8_3rd This fields specifies the DM pattern for BL7 and BL8 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase1[0] represents expected data of DM[0] and DQ[1] at the 4th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase1[1] represents expected data of DM[0] and DM[1] at the 4th valid falling edge of DQS.
7:6	RW	0x1	wrtrn_rddata_dm_adj_w0_bst9_16_3rd This fields specifies the DM pattern for BL9 and BL10 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DQ[1] at the 5th valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DM[1] at the 5th valid falling edge of DQS.
5:4	RW	0x1	wrtrn_rddata_dm_adj_w1_bst9_16_3rd This fields specifies the DM pattern for BL11 and BL12 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DQ[1] at the 6th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DM[1] at the 6th valid falling edge of DQS.

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Bit	Attr	Reset Value	Description
3:2	RW	0x1	wrtrn_rddata_dm_adj_w2_bst9_16_3rd This fields specifies the DM pattern for BL13 and BL14 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DQ[1] at the 7th valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DM[1] at the 7th valid falling edge of DQS.
1:0	RW	0x1	wrtrn_rddata_dm_adj_w3_bst9_16_3rd This fields specifies the DM pattern for BL15 and BL16 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DQ[1] at the 8th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DM[1] at the 8th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON19

Address: **Operational Base** + offset (0x0974)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x1	wrtrn_rddata_dm_adj_w0_bst1_8_4th This fields specifies the DM pattern for BL1 and BL2 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase0[0] represents expected data of DM[0] and DQ[1] at the first valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase0[1] represents expected data of DM[0] and DM[1] at the first valid falling edge of DQS.
13:12	RW	0x1	wrtrn_rddata_dm_adj_w1_bst1_8_4th This fields specifies the DM pattern for BL3 and BL4 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase0[0] represents expected data of DM[0] and DQ[1] at the second valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase0[1] represents expected data of DM[0] and DM[1] at the second valid falling edge of DQS.
11:10	RW	0x1	wrtrn_rddata_dm_adj_w2_bst1_8_4th This fields specifies the DM pattern for BL5 and BL6 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase1[0] represents expected data of DM[0] and DQ[1] at the 3rd valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase1[1] represents expected data of DM[0] and DM[1] at the 3rd valid falling edge of DQS.
9:8	RW	0x1	wrtrn_rddata_dm_adj_w3_bst1_8_4th This fields specifies the DM pattern for BL7 and BL8 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase1[0] represents expected data

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Bit	Attr	Reset Value	Description
			of DM[0] and DQ[1] at the 4th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase1[1] represents expected data of DM[0] and DM[1] at the 4th valid falling edge of DQS.
7:6	RW	0x1	wrtrn_rddata_dm_adj_w0_bst9_16_4th This fields specifies the DM pattern for BL9 and BL10 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DQ[1] at the 5th valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DM[1] at the 5th valid falling edge of DQS.
5:4	RW	0x1	wrtrn_rddata_dm_adj_w1_bst9_16_4th This fields specifies the DM pattern for BL11 and BL12 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DQ[1] at the 6th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DM[1] at the 6th valid falling edge of DQS.
3:2	RW	0x1	wrtrn_rddata_dm_adj_w2_bst9_16_4th This fields specifies the DM pattern for BL13 and BL14 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DQ[1] at the 7th valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DM[1] at the 7th valid falling edge of DQS.
1:0	RW	0x1	wrtrn_rddata_dm_adj_w3_bst9_16_4th This fields specifies the DM pattern for BL15 and BL16 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data slices. wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DQ[1] at the 8th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DM[1] at the 8th valid falling edge of DQS.

DDRPHY_READ_DQ_OFFSET_CTRL0

Address: **Operational Base** + offset (0x0978)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x37	RDDQ3OFFSET_DS0 It controls the initial DLL code for read DQ3 at DS0
23	RO	0x0	reserved
22:16	RW	0x37	RDDQ2OFFSET_DS0 It controls the initial DLL code for read DQ2 at DS0
15	RO	0x0	reserved
14:8	RW	0x37	RDDQ1OFFSET_DS0 It controls the initial DLL code for read DQ1 at DS0
7	RO	0x0	reserved
6:0	RW	0x37	RDDQ0OFFSET_DS0 It controls the initial DLL code for read DQ0 at DS0

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DDRPHY_READ_DQ_OFFSET_CTRL1

Address: **Operational Base** + offset (0x097C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x37	RDDQ7OFFSET_DS0 It controls the initial DLL code for read DQ7 at DS0
23	RO	0x0	reserved
22:16	RW	0x37	RDDQ6OFFSET_DS0 It controls the initial DLL code for read DQ6 at DS0
15	RO	0x0	reserved
14:8	RW	0x37	RDDQ5OFFSET_DS0 It controls the initial DLL code for read DQ5 at DS0
7	RO	0x0	reserved
6:0	RW	0x37	RDDQ4OFFSET_DS0 It controls the initial DLL code for read DQ4 at DS0

DDRPHY_READ_DQ_OFFSET_CTRL2

Address: **Operational Base** + offset (0x0980)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x37	RDDM8OFFSET_DS0 It controls the initial DLL code for read DM at DS0

DDRPHY_READ_DQ_OFFSET_CTRL3

Address: **Operational Base** + offset (0x0984)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x37	RDDQ3OFFSET_DS1 It controls the initial DLL code for read DQ3 at DS1
23	RO	0x0	reserved
22:16	RW	0x37	RDDQ2OFFSET_DS1 It controls the initial DLL code for read DQ2 at DS1
15	RO	0x0	reserved
14:8	RW	0x37	RDDQ1OFFSET_DS1 It controls the initial DLL code for read DQ1 at DS1
7	RO	0x0	reserved
6:0	RW	0x37	RDDQ0OFFSET_DS1 It controls the initial DLL code for read DQ0 at DS1

DDRPHY_READ_DQ_OFFSET_CTRL4

Address: **Operational Base** + offset (0x0988)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x37	RDDQ7OFFSET_DS1 It controls the initial DLL code for read DQ7 at DS1
23	RO	0x0	reserved
22:16	RW	0x37	RDDQ6OFFSET_DS1 It controls the initial DLL code for read DQ6 at DS1
15	RO	0x0	reserved
14:8	RW	0x37	RDDQ5OFFSET_DS1 It controls the initial DLL code for read DQ5 at DS1
7	RO	0x0	reserved
6:0	RW	0x37	RDDQ4OFFSET_DS1 It controls the initial DLL code for read DQ4 at DS1

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DDRPHY_READ_DQ_OFFSET_CTRL5

Address: **Operational Base** + offset (0x098C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x37	RDDM8OFFSET_DS1 It controls the initial DLL code for read DM at DS1

DDRPHY_READ_DQ_OFFSET_CTRL0_CS1

Address: **Operational Base** + offset (0x0990)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x37	RDDQ3OFFSET_RANK1_DS0 It controls the initial DLL code for read DQ3 at DS0
23	RO	0x0	reserved
22:16	RW	0x37	RDDQ2OFFSET_RANK1_DS0 It controls the initial DLL code for read DQ2 at DS0
15	RO	0x0	reserved
14:8	RW	0x37	RDDQ1OFFSET_RANK1_DS0 It controls the initial DLL code for read DQ1 at DS0
7	RO	0x0	reserved
6:0	RW	0x37	RDDQ0OFFSET_RANK1_DS0 It controls the initial DLL code for read DQ0 at DS0

DDRPHY_READ_DQ_OFFSET_CTRL1_CS1

Address: **Operational Base** + offset (0x0994)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x37	RDDQ7OFFSET_RANK1_DS0 It controls the initial DLL code for read DQ7 at DS0
23	RO	0x0	reserved
22:16	RW	0x37	RDDQ6OFFSET_RANK1_DS0 It controls the initial DLL code for read DQ6 at DS0
15	RO	0x0	reserved
14:8	RW	0x37	RDDQ5OFFSET_RANK1_DS0 It controls the initial DLL code for read DQ5 at DS0
7	RO	0x0	reserved
6:0	RW	0x37	RDDQ4OFFSET_RANK1_DS0 It controls the initial DLL code for read DQ4 at DS0

DDRPHY_READ_DQ_OFFSET_CTRL2_CS1

Address: **Operational Base** + offset (0x0998)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x37	RDDM8OFFSET_RANK1_DS0 It controls the initial DLL code for read DM at DS0

DDRPHY_READ_DQ_OFFSET_CTRL3_CS1

Address: **Operational Base** + offset (0x099C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x37	RDDQ3OFFSET_RANK1_DS1 It controls the initial DLL code for read DQ3 at DS1
23	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
22:16	RW	0x37	RDDQ2OFFSET_RANK1_DS1 It controls the initial DLL code for read DQ2 at DS1
15	RO	0x0	reserved
14:8	RW	0x37	RDDQ1OFFSET_RANK1_DS1 It controls the initial DLL code for read DQ1 at DS1
7	RO	0x0	reserved
6:0	RW	0x37	RDDQ0OFFSET_RANK1_DS1 It controls the initial DLL code for read DQ0 at DS1

DDRPHY_READ_DQ_OFFSET_CTRL4_CS1

Address: **Operational Base** + offset (0x09A0)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x37	RDDQ7OFFSET_RANK1_DS1 It controls the initial DLL code for read DQ7 at DS1
23	RO	0x0	reserved
22:16	RW	0x37	RDDQ6OFFSET_RANK1_DS1 It controls the initial DLL code for read DQ6 at DS1
15	RO	0x0	reserved
14:8	RW	0x37	RDDQ5OFFSET_RANK1_DS1 It controls the initial DLL code for read DQ5 at DS1
7	RO	0x0	reserved
6:0	RW	0x37	RDDQ4OFFSET_RANK1_DS1 It controls the initial DLL code for read DQ4 at DS1

DDRPHY_READ_DQ_OFFSET_CTRL5_CS1

Address: **Operational Base** + offset (0x09A4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x37	RDDM8OFFSET_RANK1_DS1 It controls the initial DLL code for read DM at DS1

DDRPHY_WRITE_DQ_DLINE_DUTY_CTRL0

Address: **Operational Base** + offset (0x09A8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:9	RW	0x000	par_duty_wr_p_ds1 This register control duty of write DQs of data slice 1. Each 1bit is able to control 1bit DQ. Example for controlling duty. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 0: Default par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 0: Increase HI duration. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 1: Decrease HI duration. par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 1: Increase 1 fine step delay.

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Bit	Attr	Reset Value	Description
8:0	RW	0x000	par_duty_wr_p_ds0 This register control duty of write DQs of data slice 0. Each 1bit is able to control 1bit DQ. Example for controlling duty. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 0: Default par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 0: Increase HI duration. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 1: Decrease HI duration. par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 1: Increase 1 fine step delay.

DDRPHY_WRITE_DQ_DLINE_DUTY_CTRL1

Address: **Operational Base** + offset (0x09AC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:9	RW	0x000	par_duty_wr_n_ds1 This register control duty of write DQs of data slice 1. Each 1bit is able to control 1bit DQ. Example for controlling duty. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 0: Default par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 0: Increase HI duration. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 1: Decrease HI duration. par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 1: Increase 1 fine step delay.
8:0	RW	0x000	par_duty_wr_n_ds0 This register control duty of write DQs of data slice 0. Each 1bit is able to control 1bit DQ. Example for controlling duty. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 0: Default par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 0: Increase HI duration. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 1: Decrease HI duration. par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 1: Increase 1 fine step delay.

DDRPHY_READ_DQ_DLINE_DUTY_CTRL0

Address: **Operational Base** + offset (0x09B0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:9	RW	0x000	par_duty_rd0_p_ds1 This register control duty of rank0 read DQs of data slice 1. Each 1bit is able to control 1bit DQ. Example for controlling duty. par_duty_rd0_p_ds1[#] = 0 & par_duty_rd0_n_ds1[#] = 0: Default par_duty_rd0_p_ds1[#] = 1 & par_duty_rd0_n_ds1[#] = 0: Increase HI duration. par_duty_rd0_p_ds1[#] = 0 & par_duty_rd0_n_ds1[#] = 1: Decrease HI duration. par_duty_rd0_p_ds1[#] = 1 & par_duty_rd0_n_ds1[#] = 1: Increase 1 fine step delay.

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Bit	Attr	Reset Value	Description
8:0	RW	0x000	par_duty_rd0_p_ds0 This register control duty of rank0 read DQs of data slice 0. Each 1bit is able to control 1bit DQ. Example for controlling duty. par_duty_rd0_p_ds0[#] = 0 & par_duty_rd0_n_ds0[#] = 0: Default par_duty_rd0_p_ds0[#] = 1 & par_duty_rd0_n_ds0[#] = 0: Increase HI duration. par_duty_rd0_p_ds0[#] = 0 & par_duty_rd0_n_ds0[#] = 1: Decrease HI duration. par_duty_rd0_p_ds0[#] = 1 & par_duty_rd0_n_ds0[#] = 1: Increase 1 fine step delay.

DDRPHY_READ_DQ_DLINE_DUTY_CTRL1

Address: **Operational Base** + offset (0x09B4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:9	RW	0x000	par_duty_rd0_n_ds1 This register control duty of rank0 read DQs of data slice 1. Each 1bit is able to control 1bit DQ. Example for controlling duty. par_duty_rd0_p_ds1[#] = 0 & par_duty_rd0_n_ds1[#] = 0: Default par_duty_rd0_p_ds1[#] = 1 & par_duty_rd0_n_ds1[#] = 0: Increase HI duration. par_duty_rd0_p_ds1[#] = 0 & par_duty_rd0_n_ds1[#] = 1: Decrease HI duration. par_duty_rd0_p_ds1[#] = 1 & par_duty_rd0_n_ds1[#] = 1: Increase 1 fine step delay.
8:0	RW	0x000	par_duty_rd0_n_ds0 This register control duty of rank0 read DQs of data slice 0. Each 1bit is able to control 1bit DQ. Example for controlling duty. par_duty_rd0_p_ds0[#] = 0 & par_duty_rd0_n_ds0[#] = 0: Default par_duty_rd0_p_ds0[#] = 1 & par_duty_rd0_n_ds0[#] = 0: Increase HI duration. par_duty_rd0_p_ds0[#] = 0 & par_duty_rd0_n_ds0[#] = 1: Decrease HI duration. par_duty_rd0_p_ds0[#] = 1 & par_duty_rd0_n_ds0[#] = 1: Increase 1 fine step delay.

DDRPHY_READ_DQ_DLINE_DUTY_CTRL2

Address: **Operational Base** + offset (0x09B8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:9	RW	0x000	par_duty_rd1_p_ds1 This register control duty of rank1 read DQs of data slice 1. Each 1bit is able to control 1bit DQ. Example for controlling duty. par_duty_rd1_p_ds1[#] = 0 & par_duty_rd1_n_ds1[#] = 0: Default par_duty_rd1_p_ds1[#] = 1 & par_duty_rd1_n_ds1[#] = 0: Increase HI duration. par_duty_rd1_p_ds1[#] = 0 & par_duty_rd1_n_ds1[#] = 1: Decrease HI duration. par_duty_rd1_p_ds1[#] = 1 & par_duty_rd1_n_ds1[#] = 1: Increase 1 fine step delay.

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Bit	Attr	Reset Value	Description
8:0	RW	0x000	par_duty_rd1_p_ds0 This register control duty of rank1 read DQs of data slice 0. Each 1bit is able to control 1bit DQ. Example for controlling duty. par_duty_rd1_p_ds0[#] = 0 & par_duty_rd1_n_ds0[#] = 0: Default par_duty_rd1_p_ds0[#] = 1 & par_duty_rd1_n_ds0[#] = 0: Increase HI duration. par_duty_rd1_p_ds0[#] = 0 & par_duty_rd1_n_ds0[#] = 1: Decrease HI duration. par_duty_rd1_p_ds0[#] = 1 & par_duty_rd1_n_ds0[#] = 1: Increase 1 fine step delay.

DDRPHY_READ_DQ_DLINE_DUTY_CTRL3

Address: **Operational Base** + offset (0x09BC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:9	RW	0x000	par_duty_rd1_n_ds1 This register control duty of rank1 read DQs of data slice 1. Each 1bit is able to control 1bit DQ. Example for controlling duty. par_duty_rd1_p_ds1[#] = 0 & par_duty_rd1_n_ds1[#] = 0: Default par_duty_rd1_p_ds1[#] = 1 & par_duty_rd1_n_ds1[#] = 0: Increase HI duration. par_duty_rd1_p_ds1[#] = 0 & par_duty_rd1_n_ds1[#] = 1: Decrease HI duration. par_duty_rd1_p_ds1[#] = 1 & par_duty_rd1_n_ds1[#] = 1: Increase 1 fine step delay.
8:0	RW	0x000	par_duty_rd1_n_ds0 This register control duty of rank1 read DQs of data slice 0. Each 1bit is able to control 1bit DQ. Example for controlling duty. par_duty_rd1_p_ds0[#] = 0 & par_duty_rd1_n_ds0[#] = 0: Default par_duty_rd1_p_ds0[#] = 1 & par_duty_rd1_n_ds0[#] = 0: Increase HI duration. par_duty_rd1_p_ds0[#] = 0 & par_duty_rd1_n_ds0[#] = 1: Decrease HI duration. par_duty_rd1_p_ds0[#] = 1 & par_duty_rd1_n_ds0[#] = 1: Increase 1 fine step delay.

DDRPHY_WRITE_DQS_DLINE_DUTY_CTRL0

Address: **Operational Base** + offset (0x09C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	par_duty_wr_dqs_p_ds1 This register control duty of write DQS of data slice 1. Example for controlling duty. par_duty_wr_dqs_p_ds1[#] = 0 & par_duty_wr_dqs_n_ds1[#] = 0: Default par_duty_wr_dqs_p_ds1[#] = 1 & par_duty_wr_dqs_n_ds1[#] = 0: Increase HI duration. par_duty_wr_p_dqs_ds1[#] = 0 & par_duty_wr_n_dqs_ds1[#] = 1: Decrease HI duration. par_duty_wr_p_dqs_ds1[#] = 1 & par_duty_wr_n_dqs_ds1[#] = 1: Increase 1 fine step delay.

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Bit	Attr	Reset Value	Description
24	RW	0x0	par_duty_wr_dqs_p_ds0 This register control duty of write DQS of data slice 0. Example for controlling duty. par_duty_wr_dqs_p_ds1[#] = 0 & par_duty_wr_dqs_n_ds1[#] = 0: Default par_duty_wr_dqs_p_ds1[#] = 1 & par_duty_wr_dqs_n_ds1[#] = 0: Increase HI duration. par_duty_wr_dqs_p_ds1[#] = 0 & par_duty_wr_dqs_n_ds1[#] = 1: Decrease HI duration. par_duty_wr_dqs_p_ds1[#] = 1 & par_duty_wr_dqs_n_ds1[#] = 1: Increase 1 fine step delay.
23:18	RO	0x00	reserved
17	RW	0x0	par_duty_wr_dqs_n_ds1 This register control duty of write DQS of data slice 1. Each 1bit is able to control 1bit DQ. Example for controlling duty. par_duty_wr_dqs_p_ds1[#] = 0 & par_duty_wr_dqs_n_ds1[#] = 0: Default par_duty_wr_dqs_p_ds1[#] = 1 & par_duty_wr_dqs_n_ds1[#] = 0: Increase HI duration. par_duty_wr_dqs_p_ds1[#] = 0 & par_duty_wr_dqs_n_ds1[#] = 1: Decrease HI duration. par_duty_wr_dqs_p_ds1[#] = 1 & par_duty_wr_dqs_n_ds1[#] = 1: Increase 1 fine step delay.
16	RW	0x0	par_duty_wr_dqs_n_ds0 This register control duty of write DQS of data slice 0. Each 1bit is able to control 1bit DQ. Example for controlling duty. par_duty_wr_dqs_p_ds0[#] = 0 & par_duty_wr_dqs_n_ds0[#] = 0: Default par_duty_wr_dqs_p_ds0[#] = 1 & par_duty_wr_dqs_n_ds0[#] = 0: Increase HI duration. par_duty_wr_dqs_p_ds0[#] = 0 & par_duty_wr_dqs_n_ds0[#] = 1: Decrease HI duration. par_duty_wr_dqs_p_ds0[#] = 1 & par_duty_wr_dqs_n_ds0[#] = 1: Increase 1 fine step delay.
15:12	RO	0x0	reserved
11:10	RW	0x0	par_duty_rd_dqs_p_ds1 This register control duty of read DQS of data slice 1. Example for controlling duty. MSB is able to control rank1 and LSB is able to control rank0. par_duty_rd_dqs_p_ds1[#] = 0 & par_duty_rd_dqs_n_ds1[#] = 0: Default par_duty_rd_dqs_p_ds1[#] = 1 & par_duty_rd_dqs_n_ds1[#] = 0: Increase HI duration. par_duty_rd_dqs_p_ds1[#] = 0 & par_duty_rd_dqs_n_ds1[#] = 1: Decrease HI duration. par_duty_rd_dqs_p_ds1[#] = 1 & par_duty_rd_dqs_n_ds1[#] = 1: Increase 1 fine step delay.
9:8	RW	0x0	par_duty_rd_dqs_p_ds0 This register control duty of read DQS of data slice 0. Example for controlling duty. MSB is able to control rank1 and LSB is able to control rank0. par_duty_rd_dqs_p_ds0[#] = 0 & par_duty_rd_dqs_n_ds0[#] = 0: Default par_duty_rd_dqs_p_ds0[#] = 1 & par_duty_rd_dqs_n_ds0[#] = 0: Increase HI duration. par_duty_rd_dqs_p_ds0[#] = 0 & par_duty_rd_dqs_n_ds0[#] =

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Bit	Attr	Reset Value	Description
			1: Decrease HI duration. par_duty_rd_dqs_p_ds0[#] = 1 & par_duty_rd_dqs_n_ds0[#] = 1: Increase 1 fine step delay.
7:4	RO	0x0	reserved
3:2	RW	0x0	par_duty_rd_dqs_n_ds1 This register control duty of read DQS of data slice 0. Example for controlling duty. MSB is able to control rank1 and LSB is able to control rank0. par_duty_rd_dqs_p_ds1[#] = 0 & par_duty_rd_dqs_n_ds1[#] = 0: Default par_duty_rd_dqs_p_ds1[#] = 1 & par_duty_rd_dqs_n_ds1[#] = 0: Increase HI duration. par_duty_rd_dqs_p_ds1[#] = 0 & par_duty_rd_dqs_n_ds1[#] = 1: Decrease HI duration. par_duty_rd_dqs_p_ds1[#] = 1 & par_duty_rd_dqs_n_ds1[#] = 1: Increase 1 fine step delay.
1:0	RW	0x0	par_duty_rd_dqs_n_ds0 This register control duty of read DQS of data slice 0. Example for controlling duty. MSB is able to control rank1 and LSB is able to control rank0. par_duty_rd_dqs_p_ds0[#] = 0 & par_duty_rd_dqs_n_ds0[#] = 0: Default par_duty_rd_dqs_p_ds0[#] = 1 & par_duty_rd_dqs_n_ds0[#] = 0: Increase HI duration. par_duty_rd_dqs_p_ds0[#] = 0 & par_duty_rd_dqs_n_ds0[#] = 1: Decrease HI duration. par_duty_rd_dqs_p_ds0[#] = 1 & par_duty_rd_dqs_n_ds0[#] = 1: Increase 1 fine step delay.

DDRPHY_DQ_SEL_CTRL0

Address: **Operational Base** + offset (0x09C4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x2	par_sel0_dm8_l_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DM at read dqs rising edge in data slice 0. The selection is able to control the delay of DM rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
23:21	RW	0x2	par_sel0_dq7_l_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ7 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ7 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

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Bit	Attr	Reset Value	Description
20:18	RW	0x2	par_sel0_dq6_l_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ6 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ6 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
17:15	RW	0x2	par_sel0_dq5_l_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ5 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ5 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
14:12	RW	0x2	par_sel0_dq4_l_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ4 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ4 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
11:9	RW	0x2	par_sel0_dq3_l_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ3 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ3 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
8:6	RW	0x2	par_sel0_dq2_l_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ2 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ2 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
5:3	RW	0x2	par_sel0_dq1_l_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ1 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ1 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

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Bit	Attr	Reset Value	Description
2:0	RW	0x2	par_sel0_dq0_l_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ0 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ0 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

DDRPHY_DQ_SEL_CTRL1

Address: **Operational Base** + offset (0x09C8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x2	par_sel0_dm8_l_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DM at read dqs rising edge in data slice 1. The selection is able to control the delay of DM rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
23:21	RW	0x2	par_sel0_dq7_l_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ7 at read dqs rising edge in data slice 1. The selection is able to control the delay of DQ7 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
20:18	RW	0x2	par_sel0_dq6_l_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ6 at read dqs rising edge in data slice 1. The selection is able to control the delay of DQ6 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
17:15	RW	0x2	par_sel0_dq5_l_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ5 at read dqs rising edge in data slice 1. The selection is able to control the delay of DQ5 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

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Bit	Attr	Reset Value	Description
14:12	RW	0x2	par_sel0_dq4_l_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ4 at read dqs rising edge in data slice 1. The selection is able to control the delay of DQ4 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
11:9	RW	0x2	par_sel0_dq3_l_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ3 at read dqs rising edge in data_slice3. The selection is able to control the delay of DQ3 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
8:6	RW	0x2	par_sel0_dq2_l_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ2 at read dqs rising edge in data_slice2. The selection is able to control the delay of DQ2 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
5:3	RW	0x2	par_sel0_dq1_l_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ1 at read dqs rising edge in data slice 1. The selection is able to control the delay of DQ1 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
2:0	RW	0x2	par_sel0_dq0_l_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ0 at read dqs rising edge in data slice 1. The selection is able to control the delay of DQ0 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

DDRPHY_DQ_SEL_CTRL2

Address: **Operational Base** + offset (0x09CC)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x2	par_sel0_dm8_h_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DM at read dqs falling edge in data slice 0. The selection is able to control the delay of DM rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay

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Bit	Attr	Reset Value	Description
			3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
23:21	RW	0x2	par_sel0_dq7_h_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ7 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ7 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
20:18	RW	0x2	par_sel0_dq6_h_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ6 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ6 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
17:15	RW	0x2	par_sel0_dq5_h_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ5 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ5 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
14:12	RW	0x2	par_sel0_dq4_h_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ4 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ4 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
11:9	RW	0x2	par_sel0_dq3_h_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ3 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ3 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

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Bit	Attr	Reset Value	Description
8:6	RW	0x2	par_sel0_dq2_h_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ2 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ2 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
5:3	RW	0x2	par_sel0_dq1_h_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ1 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ1 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
2:0	RW	0x2	par_sel0_dq0_h_rank0_ds0 This register selects delayed output among 5 different delayed signal of rank0 DQ0 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ0 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

DDRPHY_DQ_SEL_CTRL3

Address: **Operational Base** + offset (0x09D0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x2	par_sel0_dm8_h_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DM at read dqs falling edge in data slice 1. The selection is able to control the delay of DM rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
23:21	RW	0x2	par_sel0_dq7_h_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ7 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ7 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

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Bit	Attr	Reset Value	Description
20:18	RW	0x2	par_sel0_dq6_h_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ6 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ6 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
17:15	RW	0x2	par_sel0_dq5_h_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ5 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ5 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
14:12	RW	0x2	par_sel0_dq4_h_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ4 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ4 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
11:9	RW	0x2	par_sel0_dq3_h_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ3 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ3 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
8:6	RW	0x2	par_sel0_dq2_h_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ2 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ2 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
5:3	RW	0x2	par_sel0_dq1_h_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ1 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ1 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

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Bit	Attr	Reset Value	Description
2:0	RW	0x2	par_sel0_dq0_h_rank0_ds1 This register selects delayed output among 5 different delayed signal of rank0 DQ0 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ0 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

DDRPHY_DQ_SEL_CTRL4

Address: **Operational Base** + offset (0x09D4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x2	par_sel0_dm8_l_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DM at read dqs rising edge in data slice 0. The selection is able to control the delay of DM rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
23:21	RW	0x2	par_sel0_dq7_l_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ7 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ7 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
20:18	RW	0x2	par_sel0_dq6_l_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ6 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ6 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
17:15	RW	0x2	par_sel0_dq5_l_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ5 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ5 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

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Bit	Attr	Reset Value	Description
14:12	RW	0x2	par_sel0_dq4_l_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ4 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ4 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
11:9	RW	0x2	par_sel0_dq3_l_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ3 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ3 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
8:6	RW	0x2	par_sel0_dq2_l_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ2 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ2 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
5:3	RW	0x2	par_sel0_dq1_l_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ1 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ1 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
2:0	RW	0x2	par_sel0_dq0_l_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ0 at read dqs rising edge in data slice 0. The selection is able to control the delay of DQ0 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

DDRPHY_DQ_SEL_CTRL5

Address: **Operational Base** + offset (0x09D8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x2	par_sel0_dm8_l_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DM at read dqs rising edge in data slice 1. The selection is able to control the delay of DM rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay

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Bit	Attr	Reset Value	Description
			3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
23:21	RW	0x2	par_sel0_dq7_l_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ7 at read dqs rising edge in data slice 1. The selection is able to control the delay of DQ7 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
20:18	RW	0x2	par_sel0_dq6_l_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ6 at read dqs rising edge in data slice 1. The selection is able to control the delay of DQ6 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
17:15	RW	0x2	par_sel0_dq5_l_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ5 at read dqs rising edge in data slice 1. The selection is able to control the delay of DQ5 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
14:12	RW	0x2	par_sel0_dq4_l_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ4 at read dqs rising edge in data slice 1. The selection is able to control the delay of DQ4 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
11:9	RW	0x2	par_sel0_dq3_l_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ3 at read dqs rising edge in data slice 1. The selection is able to control the delay of DQ3 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

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Bit	Attr	Reset Value	Description
8:6	RW	0x2	par_sel0_dq2_l_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ2 at read dqs rising edge in data slice 1. The selection is able to control the delay of DQ2 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
5:3	RW	0x2	par_sel0_dq1_l_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ1 at read dqs rising edge in data slice 1. The selection is able to control the delay of DQ1 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
2:0	RW	0x2	par_sel0_dq0_l_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ0 at read dqs rising edge in data slice 1. The selection is able to control the delay of DQ0 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

DDRPHY_DQ_SEL_CTRL6

Address: **Operational Base** + offset (0x09DC)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x2	par_sel0_dm8_h_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DM at read dqs falling edge in data slice 0. The selection is able to control the delay of DM rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
23:21	RW	0x2	par_sel0_dq7_h_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ7 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ7 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
20:18	RW	0x2	par_sel0_dq6_h_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ6 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ6 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay

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Bit	Attr	Reset Value	Description
			3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
17:15	RW	0x2	par_sel0_dq5_h_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ5 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ5 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
14:12	RW	0x2	par_sel0_dq4_h_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ4 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ4 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
11:9	RW	0x2	par_sel0_dq3_h_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ3 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ3 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
8:6	RW	0x2	par_sel0_dq2_h_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ2 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ2 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
5:3	RW	0x2	par_sel0_dq1_h_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ1 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ1 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
2:0	RW	0x2	par_sel0_dq0_h_rank1_ds0 This register selects delayed output among 5 different delayed signal of rank1 DQ0 at read dqs falling edge in data slice 0. The selection is able to control the delay of DQ0 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay

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Bit	Attr	Reset Value	Description
			3'd4: Default delay + 2 coarse delay

DDRPHY_DQ_SEL_CTRL7

Address: **Operational Base** + offset (0x09E0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x2	par_sel0_dm8_h_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DM at read dqs falling edge in data slice 1. The selection is able to control the delay of DM rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
23:21	RW	0x2	par_sel0_dq7_h_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ7 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ7 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
20:18	RW	0x2	par_sel0_dq6_h_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ6 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ6 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
17:15	RW	0x2	par_sel0_dq5_h_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ5 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ5 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
14:12	RW	0x2	par_sel0_dq4_h_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ4 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ4 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

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Bit	Attr	Reset Value	Description
11:9	RW	0x2	par_sel0_dq3_h_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ3 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ3 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
8:6	RW	0x2	par_sel0_dq2_h_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ2 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ2 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
5:3	RW	0x2	par_sel0_dq1_h_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ1 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ1 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay
2:0	RW	0x2	par_sel0_dq0_h_rank1_ds1 This register selects delayed output among 5 different delayed signal of rank1 DQ0 at read dqs falling edge in data slice 1. The selection is able to control the delay of DQ0 rising edge. 3'd0: Default delay - 2 coarse delay 3'd1: Default delay - 1 coarse delay 3'd2: Default delay 3'd3: Default delay + 1 coarse delay 3'd4: Default delay + 2 coarse delay

DDRPHY_CK_DLINE_DUTY_CTRL0

Address: **Operational Base** + offset (0x09E4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	par_duty_ck_n Controls par_duty_wr_n of ctrl slice
0	RW	0x0	par_duty_ck_p Controls par_duty_wr_p of ctrl slice

DDRPHY_IO_DUTY_CTRL0

Address: **Operational Base** + offset (0x09E8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:27	RW	0x5	duty_dqs_io_cntp_ds0 It controls io_dqs_duty_ctrlp[2:0] under PHYIO_SLICE.
26:24	RW	0x5	duty_dm8_io_cntp_ds0 It controls io_dm0_duty_ctrlp under PHYIO_SLICE.

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Bit	Attr	Reset Value	Description
23:21	RW	0x5	duty_dq7_io_cntp_ds0 It controls io_dq7_duty_ctrlp under PHYIO_SLICE.
20:18	RW	0x5	duty_dq6_io_cntp_ds0 It controls io_dq6_duty_ctrlp under PHYIO_SLICE.
17:15	RW	0x5	duty_dq5_io_cntp_ds0 It controls io_dq5_duty_ctrlp under PHYIO_SLICE.
14:12	RW	0x5	duty_dq4_io_cntp_ds0 It controls io_dq4_duty_ctrlp under PHYIO_SLICE.
11:9	RW	0x5	duty_dq3_io_cntp_ds0 It controls io_dq3_duty_ctrlp under PHYIO_SLICE.
8:6	RW	0x5	duty_dq2_io_cntp_ds0 It controls io_dq2_duty_ctrlp under PHYIO_SLICE.
5:3	RW	0x5	duty_dq1_io_cntp_ds0 It controls io_dq1_duty_ctrlp under PHYIO_SLICE.
2:0	RW	0x5	duty_dq0_io_cntp_ds0 It controls io_dq0_duty_ctrlp under PHYIO_SLICE.

DDRPHY_IO_DUTY_CTRL1

Address: **Operational Base** + offset (0x09EC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:27	RW	0x5	duty_dqs_io_cntp_ds1 It controls io_dqs_duty_ctrlp[5:3] under PHYIO_SLICE.
26:24	RW	0x5	duty_dm8_io_cntp_ds1 It controls io_dm1_duty_ctrlp under PHYIO_SLICE.
23:21	RW	0x5	duty_dq7_io_cntp_ds1 It controls io_dq15_duty_ctrlp under PHYIO_SLICE.
20:18	RW	0x5	duty_dq6_io_cntp_ds1 It controls io_dq14_duty_ctrlp under PHYIO_SLICE.
17:15	RW	0x5	duty_dq5_io_cntp_ds1 It controls io_dq13_duty_ctrlp under PHYIO_SLICE.
14:12	RW	0x5	duty_dq4_io_cntp_ds1 It controls io_dq12_duty_ctrlp under PHYIO_SLICE.
11:9	RW	0x5	duty_dq3_io_cntp_ds1 It controls io_dq11_duty_ctrlp under PHYIO_SLICE.
8:6	RW	0x5	duty_dq2_io_cntp_ds1 It controls io_dq10_duty_ctrlp under PHYIO_SLICE.
5:3	RW	0x5	duty_dq1_io_cntp_ds1 It controls io_dq9_duty_ctrlp under PHYIO_SLICE.
2:0	RW	0x5	duty_dq0_io_cntp_ds1 It controls io_dq8_duty_ctrlp under PHYIO_SLICE.

DDRPHY_IO_DUTY_CTRL2

Address: **Operational Base** + offset (0x09F0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:27	RW	0x3	duty_dqs_io_cntn_ds0 It controls io_dqs_duty_ctrln[1:0] under PHYIO_SLICE.
26:24	RW	0x3	duty_dm8_io_cntn_ds0 It controls io_dm0_duty_ctrln under PHYIO_SLICE.
23:21	RW	0x3	duty_dq7_io_cntn_ds0 It controls io_dq7_duty_ctrln under PHYIO_SLICE.
20:18	RW	0x3	duty_dq6_io_cntn_ds0 It controls io_dq6_duty_ctrln under PHYIO_SLICE.

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Bit	Attr	Reset Value	Description
17:15	RW	0x3	duty_dq5_io_cntn_ds0 It controls io_dq5_duty_ctrln under PHYIO_SLICE.
14:12	RW	0x3	duty_dq4_io_cntn_ds0 It controls io_dq4_duty_ctrln under PHYIO_SLICE.
11:9	RW	0x3	duty_dq3_io_cntn_ds0 It controls io_dq3_duty_ctrln under PHYIO_SLICE.
8:6	RW	0x3	duty_dq2_io_cntn_ds0 It controls io_dq2_duty_ctrln under PHYIO_SLICE.
5:3	RW	0x3	duty_dq1_io_cntn_ds0 It controls io_dq1_duty_ctrln under PHYIO_SLICE.
2:0	RW	0x3	duty_dq0_io_cntn_ds0 It controls io_dq0_duty_ctrln under PHYIO_SLICE.

DDRPHY_IO_DUTY_CTRL3

Address: **Operational Base** + offset (0x09F4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:27	RW	0x3	duty_dqs_io_cntn_ds1 It controls io_dqs_duty_ctrln[4:3] under PHYIO_SLICE.
26:24	RW	0x3	duty_dm8_io_cntn_ds1 It controls io_dm1_duty_ctrln under PHYIO_SLICE.
23:21	RW	0x3	duty_dq7_io_cntn_ds1 It controls io_dq15_duty_ctrln under PHYIO_SLICE.
20:18	RW	0x3	duty_dq6_io_cntn_ds1 It controls io_dq14_duty_ctrln under PHYIO_SLICE.
17:15	RW	0x3	duty_dq5_io_cntn_ds1 It controls io_dq13_duty_ctrln under PHYIO_SLICE.
14:12	RW	0x3	duty_dq4_io_cntn_ds1 It controls io_dq12_duty_ctrln under PHYIO_SLICE.
11:9	RW	0x3	duty_dq3_io_cntn_ds1 It controls io_dq11_duty_ctrln under PHYIO_SLICE.
8:6	RW	0x3	duty_dq2_io_cntn_ds1 It controls io_dq10_duty_ctrln under PHYIO_SLICE.
5:3	RW	0x3	duty_dq1_io_cntn_ds1 It controls io_dq9_duty_ctrln under PHYIO_SLICE.
2:0	RW	0x3	duty_dq0_io_cntn_ds1 It controls io_dq8_duty_ctrln under PHYIO_SLICE.

DDRPHY_IO_DUTY_CTRL4

Address: **Operational Base** + offset (0x09F8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	duty_dqs_io_en_ds1 It controls io_dqs_duty_ctrl_en[1] under PHYIO_SLICE.
18	RW	0x0	duty_dm8_io_en_ds1 It controls io_dm_duty_ctrl_en[1] under PHYIO_SLICE.
17	RW	0x0	duty_dq7_io_en_ds1 It controls io_dq_duty_ctrl_en[15] under PHYIO_SLICE.
16	RW	0x0	duty_dq6_io_en_ds1 It controls io_dq_duty_ctrl_en[14] under PHYIO_SLICE.
15	RW	0x0	duty_dq5_io_en_ds1 It controls io_dq_duty_ctrl_en[13] under PHYIO_SLICE.
14	RW	0x0	duty_dq4_io_en_ds1 It controls io_dq_duty_ctrl_en[12] under PHYIO_SLICE.

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Bit	Attr	Reset Value	Description
13	RW	0x0	duty_dq3_io_en_ds1 It controls io_dq_duty_ctrl_en[11] under PHYIO_SLICE.
12	RW	0x0	duty_dq2_io_en_ds1 It controls io_dq_duty_ctrl_en[10] under PHYIO_SLICE.
11	RW	0x0	duty_dq1_io_en_ds1 It controls io_dq_duty_ctrl_en[9] under PHYIO_SLICE.
10	RW	0x0	duty_dq0_io_en_ds1 It controls io_dq_duty_ctrl_en[8] under PHYIO_SLICE.
9	RW	0x0	duty_dqs_io_en_ds0 It controls io_dqs_duty_ctrl_en[0] under PHYIO_SLICE.
8	RW	0x0	duty_dm8_io_en_ds0 It controls io_dm_duty_ctrl_en[0] under PHYIO_SLICE.
7	RW	0x0	duty_dq7_io_en_ds0 It controls io_dq_duty_ctrl_en[7] under PHYIO_SLICE.
6	RW	0x0	duty_dq6_io_en_ds0 It controls io_dq_duty_ctrl_en[6] under PHYIO_SLICE.
5	RW	0x0	duty_dq5_io_en_ds0 It controls io_dq_duty_ctrl_en[5] under PHYIO_SLICE.
4	RW	0x0	duty_dq4_io_en_ds0 It controls io_dq_duty_ctrl_en[4] under PHYIO_SLICE.
3	RW	0x0	duty_dq3_io_en_ds0 It controls io_dq_duty_ctrl_en[3] under PHYIO_SLICE.
2	RW	0x0	duty_dq2_io_en_ds0 It controls io_dq_duty_ctrl_en[2] under PHYIO_SLICE.
1	RW	0x0	duty_dq1_io_en_ds0 It controls io_dq_duty_ctrl_en[1] under PHYIO_SLICE.
0	RW	0x0	duty_dq0_io_en_ds0 It controls io_dq_duty_ctrl_en[0] under PHYIO_SLICE.

DDRPHY_IO_DUTY_CTRL5

Address: **Operational Base** + offset (0x09FC)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	duty_wck_io_en_ds1 It controls io_wck_duty_ctrl_en byte1 under PHYIO_SLICE.
19:17	RW	0x0	duty_wck_io_cntn_ds1 It controls io_wck_duty_ctrln byte1 under PHYIO_SLICE.
16:14	RW	0x0	duty_wck_io_cntp_ds1 It controls io_wck_duty_ctrlp byte1 under PHYIO_SLICE.
13	RW	0x0	duty_wck_io_en_ds0 It controls io_wck_duty_ctrl_en byte0 under PHYIO_SLICE.
12:10	RW	0x0	duty_wck_io_cntn_ds0 It controls io_wck_duty_ctrln byte0 under PHYIO_SLICE.
9:7	RW	0x0	duty_wck_io_cntp_ds0 It controls io_wck_duty_ctrlp byte0 under PHYIO_SLICE.
6	RW	0x0	duty_ck_io_en It controls io_ck_duty_ctrl_en under PHYIO_SLICE.
5	RO	0x0	reserved
4:3	RW	0x3	duty_ck_io_cntn It controls io_ck_duty_ctrln under PHYIO_SLICE.
2:0	RW	0x5	duty_ck_io_cntp It controls io_ck_duty_ctrlp under PHYIO_SLICE.

DDRPHY_DVFS0_CON6

Address: **Operational Base** + offset (0x0A00)

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Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:19	RW	0x7	dvfs0_zq_ck_dds Driver pull-down strength control for CK pad. It controls io_zq_ck_dds in dvfs mode 0. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm Impedance output driver 3'b101: 40 ohm Impedance output driver 3'b110: 34 ohm Impedance output driver 3'b111: 30 ohm Impedance output driver
18:16	RW	0x7	dvfs0_zq_ck_pdds Driver pull-up strength control for CK pad. It controls io_zq_ck_pdds in dvfs mode 0.
15:14	RO	0x0	reserved
13:12	RW	0x0	dvfs0_zq_ds1_ibias_ctrl Impcnt bias current control for data slice 1. Controls io_zq_ds_ibias_ctrl[3:2] under PHYIO_SLICE in dvfs mode 0
11:10	RW	0x0	dvfs0_zq_ds0_ibias_ctrl Impcnt bias current control for data slice 0. Controls io_zq_ds_ibias_ctrl[3:2] under PHYIO_SLICE in dvfs mode 0
9:8	RW	0x0	dvfs0_zq_mode_ibias_ctrl Impcnt bias current control for CS. Controls io_zq_mode_ibias_ctrl under PHYIO_SLICE in dvfs mode 0
7:4	RW	0x0	dvfs0_ds1_testircv Controls io_dqs1_testircv under PHYIO_SLICE in dvfs mode 0
3:0	RW	0x0	dvfs0_ds0_testircv Controls io_dqs0_testircv under PHYIO_SLICE in dvfs mode 0

DDRPHY_DVFS1_CON6

Address: **Operational Base** + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:19	RW	0x7	dvfs1_zq_ck_dds Driver pull-down strength control for CK pad. It controls io_zq_ck_dds in dvfs mode 1. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm Impedance output driver 3'b101: 40 ohm Impedance output driver 3'b110: 34 ohm Impedance output driver 3'b111: 30 ohm Impedance output driver
18:16	RW	0x7	dvfs1_zq_ck_pdds Driver pull-up strength control for CK pad. It controls io_zq_ck_pdds in dvfs mode 1.
15:14	RO	0x0	reserved
13:12	RW	0x0	dvfs1_zq_ds1_ibias_ctrl Impcnt bias current control for data slice 1. Controls io_zq_ds_ibias_ctrl[3:2] under PHYIO_SLICE in dvfs mode 1.
11:10	RW	0x0	dvfs1_zq_ds_ibias_ctrl Impcnt bias current control for data slice 0. Controls io_zq_ds_ibias_ctrl[3:2] under PHYIO_SLICE in dvfs mode 1.
9:8	RW	0x0	dvfs1_zq_mode_ibias_ctrl Impcnt bias current control for CS. Controls io_zq_mode_ibias_ctrl under PHYIO_SLICE in dvfs mode 1.
7:4	RW	0x0	dvfs1_ds1_testircv Controls io_dqs1_testircv under PHYIO_SLICE in dvfs mode 1

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	dvfs1_ds0_testircv Controls io_dqs0_testircv under PHYIO_SLICE in dvfs mode 1

DDRPHY_DQOENDESKEWCODE0

Address: **Operational Base** + offset (0x0A08)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	dqoendeskewcode_dm_ds0 DM0 OEN offset control. It controls io_dm_en[1] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dm_ds0*1tFS.
23:21	RW	0x0	dqoendeskewcode_dq7_ds0 DQ7 OEN offset control. It controls io_dq_en[7] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq7_ds0*1tFS.
20:18	RW	0x0	dqoendeskewcode_dq6_ds0 DQ6 OEN offset control. It controls io_dq_en[6] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq6_ds0*1tFS.
17:15	RW	0x0	dqoendeskewcode_dq5_ds0 DQ5 OEN offset control. It controls io_dq_en[5] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq5_ds0*1tFS.
14:12	RW	0x0	dqoendeskewcode_dq4_ds0 DQ4 OEN offset control. It controls io_dq_en[4] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq4_ds0*1tFS.
11:9	RW	0x0	dqoendeskewcode_dq3_ds0 DQ3 OEN offset control. It controls io_dq_en[3] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq3_ds0*1tFS.
8:6	RW	0x0	dqoendeskewcode_dq2_ds0 DQ2 OEN offset control. It controls io_dq_en[2] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq2_ds0*1tFS.
5:3	RW	0x0	dqoendeskewcode_dq1_ds0 DQ1 OEN offset control. It controls io_dq_en[1] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq1_ds0*1tFS.
2:0	RW	0x0	dqoendeskewcode_dq0_ds0 DQ0 OEN offset control. It controls io_dq_en[0] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq0_ds0*1tFS.

DDRPHY_DQOENDESKEWCODE1

Address: **Operational Base** + offset (0x0A0C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	dqoendeskewcode_dm_ds1 DM1 OEN offset control. It controls io_dm_en[1] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dm_ds1*1tFS.

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Bit	Attr	Reset Value	Description
23:21	RW	0x0	dqoendeskewcode_dq7_ds1 DQ15 OEN offset control. It controls io_dq_en[15] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq7_ds1*1tFS.
20:18	RW	0x0	dqoendeskewcode_dq6_ds1 DQ14 OEN offset control. It controls io_dq_en[14] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq6_ds1*1tFS.
17:15	RW	0x0	dqoendeskewcode_dq5_ds1 DQ13 OEN offset control. It controls io_dq_en[13] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq5_ds1*1tFS.
14:12	RW	0x0	dqoendeskewcode_dq4_ds1 DQ12 OEN offset control. It controls io_dq_en[12] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq4_ds1*1tFS.
11:9	RW	0x0	dqoendeskewcode_dq3_ds1 DQ11 OEN offset control. It controls io_dq_en[11] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq3_ds1*1tFS.
8:6	RW	0x0	dqoendeskewcode_dq2_ds1 DQ10 OEN offset control. It controls io_dq_en[10] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq2_ds1*1tFS.
5:3	RW	0x0	dqoendeskewcode_dq1_ds1 DQ9 OEN offset control. It controls io_dq_en[9] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq1_ds1*1tFS.
2:0	RW	0x0	dqoendeskewcode_dq0_ds1 DQ8 OEN offset control. It controls io_dq_en[8] under PHYIO_SLICE under PHYIO_SLICE delay. The amount of delay is dqoendeskewcode_dq0_ds1*1tFS.

DDRPHY_DQSOENDESKEWCODE

Address: **Operational Base** + offset (0x0A10)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:3	RW	0x0	dqsoendeskewcode_ds1 DQS1 OEN offset control. It controls io_pdqs_en[1] and io_ndqs_en[1] under PHYIO_SLICE. The amount of delay is dqsoendeskewcode_ds1*1tFS.
2:0	RW	0x0	dqsoendeskewcode_ds0 DQS0 OEN offset control. It controls io_pdqs_en[0] and io_ndqs_en[0] under PHYIO_SLICE. The amount of delay is dqsoendeskewcode_ds0*1tFS.

DDRPHY_DTB

Address: **Operational Base** + offset (0x0A14)

Bit	Attr	Reset Value	Description
31	RW	0x0	DTB_enable DTB enable If DTB_enable is 1, DDRPHY_DTB will be driven depending on DTB_select. If DTB_enable is 0, DDRPHY_DTB = 4'h0.
30:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	DTB_select DTB select It determines which signal is driven on DDRPHY_DTB. 8'h0: {2'h0, dfi_init_start, dfi_init_complete} 8'h1: {dfi_phyupd_req, dfi_phyupd_ack, dfi_ctrlupd_req, dfi_ctrlupd_ack} 8'h2: {2'h0, cs_phyupd} 8'h3: {1'h0, cs_phydvfs} 8'h4: rdfifo_rptr (ds1) 8'h5: rdfifo_rptr (ds0) 8'h6: rdfifo_wptr (ds1) 8'h7: rdfifo_wptr (ds0) 8'h8: {3'h0, dfi_reset_n} 8'ha: {3'h0, ctrl_dll_on} 8'hb: {3'h0, ctrl_phy_cg_en} 8'hc: {dfi_cke_p0} 8'hd: {dfi_cke_p1} 8'he: {dfi_cke_p2} 8'hf: {dfi_cke_p3}

DDRPHY_GTCC_CON0

Address: **Operational Base** + offset (0x0A18)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	gtcc_offsetc1 Gate center control offset amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after ctrl_vtc_en is high and ctrl_vtc_en is high and dfi_ctrlupd_req becomes high and low. It is used to give offset to gate training result (T/2 from DQS rising edge by default) for debug purpose. gtcc_offsetc [9] =1: (tFS: fine step delay) Total GATE delay amount - gtcc_offsetc [8:0] x tFS gtcc_offsetc [9] = 0: Total GATE delay amount + gtcc_offsetc [8:0] x tFS
15:10	RO	0x00	reserved
9:0	RW	0x000	gtcc_offsetc0 Gate offset control offset amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after ctrl_vtc_en is high and dfi_ctrlupd_req becomes high and low. It is used to give offset to gate training result (T/2 from DQS rising edge by default) for debug purpose. gtcc_offsetc [9] = 1: (tFS: fine step delay) Total GATE delay amount - gtcc_offsetc [8:0] x tFS gtcc_offsetc [9] = 0: Total GATE delay amount + gtcc_offsetc [8:0] x tFS

DDRPHY_RANK1_CON0

Address: **Operational Base** + offset (0x0A1C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	per_rank_rl_enable Enable signal to support assymmetric rank RL. If this field is enabled, RL of rank1 (*_rdlat_rank1) should be set.

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Bit	Attr	Reset Value	Description
17:12	RW	0x20	dvfs1_rdlat_rank1 This field will be used instead of ctrl_rdlat_rank1 during DVFS1 mode.
11:6	RW	0x20	dvfs0_rdlat_rank1 This field will be used instead of ctrl_rdlat_rank1 during DVFS0 mode.
5:0	RW	0x20	ctrl_rdlat_rank1 Read latency (RL) for rank1

DDRPHY_SCHD_CON0

Address: **Operational Base** + offset (0x0A20)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	schd_fsm_clear PHY scheduler FSM reset. Please use set and clear for FSM reset.
6	RW	0x1	sw_cmd_start If this bit is disabled, the scheduler command will not be generated. When the 'sw_cmd_start' is enabled, the commands in FIFO that you already requested will be generated by the timing parameter.
5	RW	0x0	phy_mstr_cnt_en_APB Enable dfi_phymstr counter dfi_phymstr_req will be disabled 64 DFI cycles, when dfi_phymstr_ack is not asserted.
4	RW	0x0	dvfs_train_force DVFS training force start control for debug purpose. DVFS training will start when this register changes from 0 to 1 even when there is no frequency change handshake.
3	RW	0x0	periodic_train_force Periodic training force can control for debugging pupose and SW initiated training. Periodic training will be initiated one time when this register changes from 0 to 1. HW periodic training should be disabled by periodic_en = 0, before periodic training is initiated by this register. Please follow procedure below for debug purpose using HW periodic training. PHY initial training --> HW periodic training enable --> HW periodic training disable --> schd_fsm_clear set and clear --> SW periodic training enable --> SW periodic training disable. Also if this field used by SW periodic training, do not use the mix up both HW periodic training and SW periodic training for normal operation.
2	RW	0x0	phy_mstr_bypass Master Interface bypass control. If phy_mstr_bypass = 1, the handshake of DFI PHY master mode is skipped when periodic/dfs training is excuted.
1	RW	0x0	scheduler_cg_en_disable Scheduler clock gating disable
0	RW	0x0	scheduler_sw_mode SW sheduler mode enable

DDRPHY_SCHD_TRAIN_CON0

Address: **Operational Base** + offset (0x0A24)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:22	RW	0x0	periodic_wrtrn_en Enable periodic write training mode [0]: CS-0 Enable [1]: CS-1 Enable
21:20	RW	0x0	periodic_gttrn_en Enable periodic gate training mode [0]: CS-0 Enable [1]: CS-1 Enable
19:18	RW	0x0	dvfs_wrtrn_en Enable DVFS write training mode [0]: CS-0 Enable [1]: CS-1 Enable
17:16	RW	0x0	dvfs_gttrn_en Enable DVFS gate traininig mode [0]: CS-0 Enable [1]: CS-1 Enable
15:14	RW	0x0	phy_wrtrn_rank_en Per rank write training enable 2'b01: Enable Rank0 2'b10: Enable Rank1
13:12	RW	0x0	phy_rdtrn_rank_en Per rank read training enable 2'b01: Enable Rank0 2'b10: Enable Rank1
11:10	RW	0x0	phy_gttrn_rank_en Per rank gate levelling enable 2'b01: Enable Rank0 2'b10: Enable Rank1
9:8	RW	0x0	phy_wrlvl_rank_en Per rank write levelling enable 2'b01: Enable Rank0 2'b10: Enable Rank1
7	RO	0x0	reserved
6	RW	0x0	phy_wrtrn_en Enable PHY write training mode
5	RW	0x0	phy_rdtrn_en Enable PHY read training mode
4	RW	0x0	phy_gttrn_en Enable PHY gate levelling mode
3	RW	0x0	phy_wrlvl_en Enable PHY write levelling mode
2	RW	0x0	phy_cbt_en Enable PHY CBT mode
1	RO	0x0	phy_train_done When phy_train_done is high, PHY training mode is finished. Please disable phy_training_en.
0	RW	0x0	phy_train_en PHY training mode enable. It should be enabled after setting CAL_CON5[23:1]. Please disable after phy_train_done is high.

DDRPHY_SCHD_TRAIN_CON1

Address: **Operational Base** + offset (0x0A28)

Bit	Attr	Reset Value	Description
31	RW	0x0	periodic_en Periodic training enable

Bit	Attr	Reset Value	Description
30:0	RW	0x000403f5	periodic_time periodic_time is defined interval of periodic training. Total time = periodic_time* (period of clk_osc)

DDRPHY_SCHD_TIME_CON0

Address: **Operational Base** + offset (0x0A2C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RW	0x16	tMRW MRW-to-MRW delay time based on memory clk LPDDR4, LPDDR5: Refer to the Jedec spec about tMRW
17:14	RW	0x8	tMRR MRR-to-MRR delay time based on memory clk LPDDR4, LPDDR5: Refer to the Jedec spec about tMRR
13:11	RO	0x0	reserved
10:6	RW	0x07	phy_t_rddata_en dfi_rddata_en latency. It defines latency of generating dfi_rddata_en after RL (read latency from RD CMD). trddata_en is defined as (RL+phy_t_rddata_en)*memory clock. Note that RL+phy_t_rddata_en should be even number to meet dfi_rddata_en phase requirement. If the sum is odd number, increase phy_t_rddata_en by 1.
5:0	RW	0x12	WL Write latency. It decide latency of generating dfi_wrdata_en after WL (Write Latency from WR CMD).

DDRPHY_SCHD_TIME_CON1

Address: **Operational Base** + offset (0x0A30)

Bit	Attr	Reset Value	Description
31:28	RW	0x6	tNOP WR-to-NOP or NOP-to-WR delay time based on memory clk
27:22	RW	0x10	tWTR WRITE-to-READ or LP4_MPC_WR-to_LP4_MPC_RD delay time based on memory clk Refer to the Jedec spec about tWTR. If you set this bit (tWTR), the each delay will be below value. LPDDR4: (Write-to-Read) WL+1+BL/2+tWTR, (LP4_MPC_WR-to-LP4_MPC_RD) WL+BL/2+tWTR+8 LPDDR5: (Write-to-Read) WL+tBL_divn+tWTR (LP5_WFF-to-LP5_WFF) WL+tBL_divn+tWTR
21:14	RW	0x34	tRCD ACT-to-WRITE delay time based on memory clk LPDDR4, LPDDR5: Refer to the Jedec spec about tRCD
13:8	RW	0x10	tRTP READ-to-PRE delay time based on memory clk Refer to the Jedec spec about tRTP. If you set this bit (tRTP), the each delay will be below value. LPDDR4: tRTP+BL/2-8 LPDDR5: X

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Bit	Attr	Reset Value	Description
7:0	RW	0x08	tCCD LPDDR4: WRITE-to-WRITE or READ-to-READ or LP4_MPC_RD_DQ_CAL-to-LP4_MPC_RD_DQ_CAL delay time based on memory clk LPDDR5: LP5_RDC-to-LP5_RDC delay time based on memory clk Refer to the Jedec spec about tCCD range

DDRPHY_SCHD_TIME_CON2

Address: **Operational Base** + offset (0x0A34)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RW	0x0	tDES Default latency
26:21	RW	0x1e	tURTW User Read-to-Write or LP4_MPC_RD_FIFO-to-LP4_MPC_WR_FIFO delay time based on memory clk. Refer to the Jedec spec about delay of Read to Write or MPC READ FIFO to MPC WRITE FIFO. If you set this bit (tURTW), the each delay will be below value. LPDDR4: (Read-to-Write) RL+BL/2-WL+tURTW (LP4_MPC_RD-to-LP4_MPC_WR) RL+BL/2-WL+tURTW LPDDR5: X
20:13	RW	0x3a	tRP PRE-to-ACT delay or PRE-to-MRS delay time based on memory clk LPDDR4 (PRE-to-ACT): Refer to the Jedec spec about tRP
12:6	RW	0x1e	tMRD LPDDR4: MRW-to-LP4_MPC_RD_CAL or MRS-to-MRS delay time based on memory clk LPDDR5: MRW-to-CMD_LP5_RDC delay time based on memory clk If you set this bit (tMRD), the each delay will be below value. Refer to the Jedec spec about tMRD range.
5:0	RO	0x00	reserved

DDRPHY_SCHD_TIME_CON3

Address: **Operational Base** + offset (0x0A38)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x8	tBL_divn LPDDR4: X LPDDR5: BL/n
3:2	RO	0x0	reserved
1:0	RW	0x0	Additional_WL Additional control of scheduler's write latency It is for the write training. 2'b00: WL 2'b01: WL+1 2'b10: WL-1 2'b11: Reserved

DDRPHY_DVFS0_SCHD_TIME_CON0

Address: **Operational Base** + offset (0x0A3C)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RW	0x16	dfs0_tMRW MRW-to-MRW delay time based on memory clk LPDDR4, LPDDR5: Refer to the Jedec spec about tMRW
17:14	RW	0x8	dfs0_tMRR MRR-to-MRR delay time based on memory clk LPDDR4, LPDDR5: Refer to the Jedec spec about tMRR
13:11	RO	0x0	reserved
10:6	RW	0x07	dfs0_phy_t_rddata_en dfi_rddata_en latency. It defines latency of generating dfi_rddata_en after RL (read latency from RD CMD). trddata_en is defined as (RL+phy_t_rddata_en)*memory clock. Note that RL+phy_t_rddata_en should be even number to meet dfi_rddata_en phase requirement. If the sum is odd number, increase phy_t_rddata_en by 1.
5:0	RW	0x12	dfs0_WL Write latency. It decide latency of generating dfi_wrdata_en after WL (Write Latency from WR CMD).

DDRPHY_DVFS0_SCHD_TIME_CON1

Address: **Operational Base** + offset (0x0A40)

Bit	Attr	Reset Value	Description
31:28	RW	0x6	dfs0_tNOP WR-to-NOP or NOP-to-WR delay time based on memory clk
27:22	RW	0x10	dfs0_tWTR WRITE-to-READ or LP4_MPC_WR-to_LP4_MPC_RD delay time based on memory clk Refer to the Jedec spec about tWTR. If you set this bit (tWTR), the each delay will be below value. LPDDR4: (Write-to-Read) WL+1+BL/2+tWTR (LP4_MPC_WR-to-LP4_MPC_RD) WL+BL/2+tWTR+8 LPDDR5: (Write-to-Read) WL+tBL_divn+tWTR (LP5_WFF-to-LP5_WFF) WL+tBL_divn+tWTR
21:14	RW	0x34	dfs0_tRCD ACT-to-WRITE delay time based on memory clk LPDDR4, LPDDR5: Refer to the Jedec spec about tRCD
13:8	RW	0x10	dfs0_tRTP READ-to-PRE delay time based on memory clk Refer to the Jedec spec about tRTP. If you set this bit (tRTP), the each delay will be below value. LPDDR4: tRTP+BL/2-8 LPDDR5: X
7:0	RW	0x08	dfs0_tCCD LPDDR4: WRITE-to-WRITE or READ-to-READ or LP4_MPC_RD_DQ_CAL-to-LP4_MPC_RD_DQ_CAL delay time based on memory clk LPDDR5: LP5_RDC-to-LP5_RDC delay time based on memory clk Refer to the Jedec spec about tCCD range.

DDRPHY_DVFS0_SCHD_TIME_CON2

Address: **Operational Base** + offset (0x0A44)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30:27	RW	0x0	dfs0_tDES Default latency
26:21	RW	0x1e	dfs0_tURTW User Read-to-Write or LP4_MPC_RD_FIFO-to-LP4_MPC_WR_FIFO delay time based on memory clk Refer to the Jedec spec about delay of read to write or MPC READ FIFO to MPC WRITE FIFO. If you set this bit (tURTW), the each delay will be below value. LPDDR4: (Read-to-Write) RL+BL/2-WL+tURTW (LP4_MPC_RD-to-LP4_MPC_WR) RL+BL/2-WL+tURTW LPDDR5: X
20:13	RW	0x3a	dfs0_tRP PRE-to-ACT delay or PRE-to-MRS delay time based on memory clk LPDDR4 (PRE-to-ACT): Refer to the Jedec spec about tRP.
12:6	RW	0x1e	dfs0_tMRD LPDDR4: MRW-to-LP4_MPC_RD_CAL or MRS-to-MRS delay time based on memory clk LPDDR5: MRW-to-CMD_LP5_RDC delay time based on memory clk If you set this bit (tMRD), the each delay will be below value. Refer to the Jedec spec about tMRD range.
5:0	RO	0x00	reserved

DDRPHY_DVFS0_SCHD_TIME_CON3

Address: **Operational Base** + offset (0x0A48)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:27	RW	0x0	dvfs0_Additional_WL Additional control of scheduler's write latency. It is for the write training. 2'b00: WL 2'b01: WL+1 2'b10: WL-1 2'b11: Reserved
26:23	RW	0x8	dvfs0_tBL_divn LPDDR4: X LPDDR5: BL/n
22:18	RO	0x00	reserved
17	RW	0x0	dvfs0_periodic_en Periodic training enable
16	RW	0x0	dvfs0_periodic_zq_cnt_en Enable periodic ZQ calibration
15:14	RW	0x0	dvfs0_periodic_wrtrn_en Enable periodic write training mode. [0]: CS-0 Enable [1]: CS-1 Enable
13:12	RW	0x0	dvfs0_periodic_gttrn_en Enable periodic gate training mode. [0]: CS-0 Enable [1]: CS-1 Enable

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Bit	Attr	Reset Value	Description
11:10	RW	0x0	dvfs0_dvfs_wrtrn_en Enable DVFS write training mode. [0]: CS-0 Enable [1]: CS-1 Enable
9:8	RW	0x0	dvfs0_dvfs_gttrn_en Enable DVFS gate traininig mode. [0]: CS-0 Enable [1]: CS-1 Enable
7:1	RO	0x00	reserved
0	RW	0x1	dvfs0_CAS_EN LP5 WCK2CK SYNC command driven by PHY scheduler. It needs to control to LP5 PHY training mode at DVFS0. dvfs0_cas_en should be enabled during wck2ck syns always on disable mode. dvfs0_cas_en should be disabled during wck2ck sync always on mode. 1'b0: Disable 1'b1: Enable

DDRPHY_DVFS1_SCHD_TIME_CON0

Address: **Operational Base** + offset (0x0A4C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RW	0x16	dfs1_tMRW MRW-to-MRW delay time based on memory clk LPDDR4, LPDDR5: Refer to the Jedec spec about tMRW.
17:14	RW	0x8	dfs1_tMRR MRR-to-MRR delay time based on memory clk LPDDR4, LPDDR5: Refer to the Jedec spec about tMRR.
13:11	RO	0x0	reserved
10:6	RW	0x07	dfs1_phy_t_rddata_en dfi_rddata_en latency. It defines latency of generating dfi_rddata_en after RL (read latency from RD CMD). trddata_en is defined as (RL+phy_t_rddata_en)*memory clock. Note that RL+phy_t_rddata_en should be even number to meet dfi_rddata_en phase requirement. If the sum is odd number, increase phy_t_rddata_en by 1.
5:0	RW	0x12	dfs1_WL Write latency. It decide latency of generating dfi_wrdata_en after WL (Write Latency from WR CMD).

DDRPHY_DVFS1_SCHD_TIME_CON1

Address: **Operational Base** + offset (0x0A50)

Bit	Attr	Reset Value	Description
31:28	RW	0x6	dfs1_tNOP WR-to-NOP or NOP-to-WR delay time based on memory clk

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Bit	Attr	Reset Value	Description
27:22	RW	0x10	dfs1_tWTR WRITE-to-READ or LP4_MPC_WR-to_LP4_MPC_RD delay time based on memory clk Refer to the Jedec spec about tWTR. If you set this bit (tWTR), the each delay will be below value. LPDDR4: (Write-to-Read) WL+1+BL/2+tWTR (LP4_MPC_WR-to-LP4_MPC_RD) WL+BL/2+tWTR+8 LPDDR5: (Write-to-Read) WL+tBL_divn+tWTR (LP5_WFF-to-LP5_WFF) WL+tBL_divn+tWTR
21:14	RW	0x34	dfs1_tRCD ACT-to-WRITE delay time based on memory clk LPDDR4, LPDDR5: Refer to the Jedec spec about tRCD
13:8	RW	0x10	dfs1_tRTP READ-to-PRE delay time based on memory clk Refer to the Jedec spec about tRTP If you set this bit (tRTP), the each delay will be below value. LPDDR4: tRTP+BL/2-8 LPDDR5: X
7:0	RW	0x08	dfs1_tCCD LPDDR4: WRITE-to-WRITE or READ-to-READ or LP4_MPC_RD_DQ_CAL-to-LP4_MPC_RD_DQ_CAL delay time based on memory clk LPDDR5: LP5_RDC-to-LP5_RDC delay time based on memory clk Refer to the Jedec spec about tCCD range.

DDRPHY_DVFS1_SCHD_TIME_CON2

Address: **Operational Base** + offset (0x0A54)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RW	0x0	dfs1_tDES Default latency
26:21	RW	0x1e	dfs1_tURTW User Read-to-Write or LP4_MPC_RD_FIFO-to-LP4_MPC_WR_FIFO delay time based on memory clk. Refer to the Jedec spec about delay of Read to Write or MPC READ FIFO to MPC WRITE FIFO. If you set this bit (tURTW), the each delay will be below value. LPDDR4: (Read-to-Write) RL+BL/2-WL+tURTW (LP4_MPC_RD-to-LP4_MPC_WR) RL+BL/2-WL+tURTW LPDDR5: X
20:13	RW	0x3a	dfs1_tRP PRE-to-ACT delay or PRE-to-MRS delay time based on memory clk LPDDR4 (PRE-to-ACT): Refer to the Jedec spec about tRP.
12:6	RW	0x1e	dfs1_tMRD LPDDR4: MRW-to-LP4_MPC_RD_CAL or MRS-to-MRS delay time based on memory clk LPDDR5: MRW-to-CMD_LP5_RDC delay time based on memory clk If you set this bit (tMRD), the each delay will be below value. Refer to the Jedec spec about tMRD range.
5:0	RO	0x00	reserved

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DDRPHY_DVFS1_SCHD_TIME_CON3

Address: **Operational Base** + offset (0x0A58)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:27	RW	0x0	dvfs1_Additional_WL Additional control of scheduler's write Latency. It is for the write-training. 2'b00: WL 2'b01: WL+1 2'b10: WL-1 2'b11: Reserved
26:23	RW	0x8	dvfs1_tBL_divn LPDDR4: X LPDDR5: BL/n
22:18	RO	0x00	reserved
17	RW	0x0	dvfs1_periodic_en Periodic training enable
16	RW	0x0	dvfs1_periodic_zq_cnt_en Enable periodic ZQ calibration
15:14	RW	0x0	dvfs1_periodic_wrtrn_en Enable Periodic Write Training Mode. [0]: CS-0 Enable [1]: CS-1 Enable
13:12	RW	0x0	dvfs1_periodic_gttrn_en Enable periodic gate training Mode. [0]: CS-0 Enable [1]: CS-1 Enable
11:10	RW	0x0	dvfs1_dvfs_wrtrn_en Enable DVFS Write Training Mode. [0]: CS-0 Enable [1]: CS-1 Enable
9:8	RW	0x0	dvfs1_dvfs_gttrn_en Enable DVFS gate traininig Mode. [0]: CS-0 Enable [1]: CS-1 Enable
7:1	RO	0x00	reserved
0	RW	0x1	dvfs1_CAS_EN LP5 WCK2CK SYNC command driven by PHY scheduler. It needs to control to LP5 PHY training mode at DVFS1. dvfs1_cas_en should be enabled during wck2ck syns always on disable mode. dvfs1_cas_en should be disabled during wck2ck sync always on mode. 1'b0: Disable 1'b1: Enable

DDRPHY_SCHD_DIRECT_CMD0

Address: **Operational Base** + offset (0x0A5C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	DIRECT_EN_APB Direct command Enable when scheduler_sw_mode is enabled. It should be disabled before generate direct command again.

DDRPHY_SCHD_DIRECT_CMD1

Address: **Operational Base** + offset (0x0A60)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	DIRECT_CS_1 Control CS[1:0] for CMD-1 when DIRECT_EN_APB is enabled.
27:0	RW	0x0000000	DIRECT_CMD_1 Control ADD/CMD for CMD-1 when DIRECT_EN_APB is enabled. [5:0]: CMD-1 for CS high. [13:8]: CMD-1 for CS low

DDRPHY_SCHD_DIRECT_CMD2

Address: **Operational Base** + offset (0x0A64)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	DIRECT_CS_2 Control CS[1:0] for CMD-2 when DIRECT_EN_APB is enabled.
27:0	RW	0x0000000	DIRECT_CMD_2 Control ADD/CMD for CMD-2 when DIRECT_EN_APB is enabled. [5:0]: CMD-2 for CS high [13:8]: CMD-2 for CS low

DDRPHY_SCHD_DIRECT_CMD3

Address: **Operational Base** + offset (0x0A68)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	CMD_WCK_GEN_req_APB Generate WCK gen request when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
22	RW	0x0	CMD_DQS_GEN_req_APB Generate DQS gen request when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
21	RW	0x0	CMD_PRE_req_APB Generate PRECHARGE CMD when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
20	RW	0x0	CMD_PREA_req_APB Generate PRECHARGE-ALL CMD when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
19	RW	0x0	CMD_REF_req_APB Generate REFRESH CMD when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
18	RW	0x0	CMD_SRE_req_APB Generate SELF REFRESH ENTER CMD when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
17	RW	0x0	CMD_SRX_req_APB Generate SELF REFRESH EXIT CMD when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
16	RW	0x0	CMD_ACT_req_APB Generate ACTIVE CMD when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
15	RW	0x0	CMD_WR_req_APB Generate WRITE CMD when scheduler_sw_mode is enabled. It also generate dfi_wrdata_en. The CMD/ADDR is defined by SCHEDULER_CON4~6.

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Bit	Attr	Reset Value	Description
14	RW	0x0	CMD_MWR_req_APB Generate Masked WRITE CMD when scheduler_sw_mode is enabled. It also generate dfi_wrdata_en. The CMD/ADDR is defined by SCHEDULER_CON4~6.
13	RW	0x0	CMD_RD_req_APB Generate READ CMD when scheduler_sw_mode is enabled. It also generate dfi_rddata_en after t_rddata_en. The CMD/ADDR is defined by SCHEDULER_CON4~6.
12	RW	0x0	CMD_MRW_req_APB Generate MRW CMD when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
11	RW	0x0	CMD_MRR_req_APB Generate MRR CMD when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
10	RW	0x0	LP4_MPC_RD_FIFO_req_APB Generate MPC_RD_FIFO CMD for LPDDR4 when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
9	RW	0x0	LP4_MPC_RD_DQ_CAL_req_APB Generate MPC_RD_DQ_CAL CMD for LPDDR4 when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
8	RW	0x0	LP4_MPC_WR_FIFO_req_APB Generate MPC_WR_FIFO CMD for LPDDR4 when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
7:4	RO	0x0	reserved
3	RW	0x0	CMD_CKE_LOW_req_APB Control CKE to low when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6. It is for the LPDDR4.
2	RW	0x0	CMD_CKE_HIGH_req_APB Control CKE to high when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6. It is for the LPDDR4.
1	RW	0x0	CMD_NOP_req_APB Generate NOP CMD when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
0	RO	0x0	reserved

DDRPHY_SCHD_DIRECT_CMD4

Address: **Operational Base** + offset (0x0A6C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	CMD_CAS_LP5_req_APB Generates CAS CMD, when scheduler_sw_mode is enabled The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
10	RW	0x0	CMD_LP5_PDE_req_APB Generates PDE CMD, when scheduler_sw_mode is enabled The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.

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Bit	Attr	Reset Value	Description
9	RW	0x0	CMD_LP5_PDX_req_APB Generates PDX CMD, when scheduler_sw_mode is enabled The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
8	RW	0x0	CMD_LP5_WFF_req_APB Generates WFF CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
7	RW	0x0	CMD_LP5_RFF_req_APB Generates RFF CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
6	RW	0x0	CMD_LP5_RDC_req_APB Generates RDC CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
5	RW	0x0	CMD_LP5_MPC_START_WCK2DQI_req_APB Generates MPC START WCK2DQI CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
4	RW	0x0	CMD_LP5_MPC_STOP_WCK2DQI_req_APB Generates MPC STOP WCK2DQI CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
3	RW	0x0	CMD_LP5_MPC_START_WCK2DQO_req_APB Generates MPC START WCK2DQO CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
2	RW	0x0	CMD_LP5_MPC_STOP_WCK2DQO_req_APB Generates MPC STOP WCK2DQO CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
1	RW	0x0	CMD_LP5_MPC_START_ZQ_req_APB Generates MPC START ZQ CMD when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
0	RW	0x0	CMD_LP5_MPC_STOP_ZQ_req_APB Generates MPC STOP ZQ CMD when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.

DDRPHY_SCHD_CMD_CON0

Address: **Operational Base** + offset (0x0A70)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	AB_EN_APB Sets MEMORY All Bank for CMD/ADDR
27	RW	0x0	AP_EN_APB Sets MEMORY Auto Precharge for CMD/ADDR

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Bit	Attr	Reset Value	Description
26	RW	0x0	BL_EN_APB Sets MEMORY Burst Length for CMD/ADDR
25:22	RW	0x0	RANK_SEL_APB Sets MEMORY Rank Selection for CMD/ADDR
21:20	RW	0x0	BK_ORG_APB Controls Bank mode selection for LPDDR5 2'b10: 16bank 2'b01: 8bank 2'b00: 4bank 4BG Others: Reserved
19	RW	0x0	PD_EN_APB Sets MEMORY Power Down for SRE
18	RW	0x0	DSM_EN_APB Sets MEMORY Deep Sleep Mode for SRE
17	RO	0x0	reserved
16	RW	0x0	WRX_APB Sets MEMORY Write X function for CMD/ADDR
15:12	RW	0x0	DC_CODE_APB Sets MEMORY Data Copy function for CMD/ADDR
11	RW	0x0	WS_FAST_APB Sets MEMORY WS_FS for CAS
10	RW	0x0	WS_RD_APB Sets MEMORY WS_RD for CAS
9	RW	0x0	WS_WR_APB Sets MEMORY WS_WR for CAS
8	RW	0x0	EDC_EN_APB Sets MEMORY EDC for CAS
7:3	RW	0x00	B_CODE_APB Sets MEMORY Bank Address for CMD/ADDR
2:1	RW	0x0	BG_CODE_APB Sets MEMORY Bank Group Address for CMD/ADDR
0	RW	0x1	CAS_EN_APB LP5 WCK2CK SYNC command driven by PHY scheduler. It needs to control to LP5 PHY training mode. CAS_EN should be enabled during wck2ck sync always on disable mode. CAS_EN should be disabled during wck2ck sync always on mode. 1'b0: Disable 1'b1: Enable

DDRPHY_SCHD_CMD_CON1

Address: **Operational Base** + offset (0x0A74)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:18	RW	0x000	COL_CODE_APB Sets MEMORY COL ADDRESS for CMD/ADDR
17:0	RW	0x00000	ROW_CODE_APB Sets MEMORY ROW ADDRESS for CMD/ADDR

DDRPHY_SCHD_CMD_CON2

Address: **Operational Base** + offset (0x0A78)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:12	RW	0x00000	OP_CODE_APB Sets MEMORY OPCODE for MRW

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Bit	Attr	Reset Value	Description
11:4	RW	0x00	MA_CODE_APB Sets MEMORY MACODE for MRW and MRR
3:0	RW	0x0	BA_CODE_APB Sets MEMORY BACODE for CMD/ADDR

DDRPHY_OP_CODE_RDC

Address: **Operational Base** + offset (0x0A7C)

Bit	Attr	Reset Value	Description
31:24	RW	0x55	OP_CODE_PATB This field register set MEMORY OPCODE for read DQ calbration (Pattern B LP4: MR40 LP5: MR33)
23:16	RW	0x55	OP_CODE_PATA This field register set MEMORY OPCODE for read DQ calbration (Pattern A LP4: MR32 LP5: MR32)
15:8	RW	0xee	OP_CODE_INVB This field register set MEMORY OPCODE for read DQ calbration (Upper byte invert LP4: MR20 LP5: MR32)
7:0	RW	0xee	OP_CODE_INVA This field register set MEMORY OPCODE for read DQ calbration (Lowe byte invert LP4: MR15 LP5: MR31)

DDRPHY_LP4_MR_OP0

Address: **Operational Base** + offset (0x0A80)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	LP4_MR12_OP It is MR12 Register infromation for LPDDR4. It will be used for CBT on PHY initiated training. [5:0] = MR12 OP[5:0] (Vref CA) [6] = MR12 OP[6] (VR-CA)
23:16	RW	0x00	LP4_MR11_OP It is MR11 Register infromation for LPDDR4. It will be used for CBT on PHY initiated training. [2:0] = MR11 OP[2:0] (DQ ODT) [6:4] = MR11 OP[6:4] (CA ODT)
15:8	RW	0x00	LP4_MR2_OP It is MR2 Register infromation for LPDDR4. It will be used for write levelling on PHY initiated training. [2:0] = MR2 OP[2:0] (RL) [5:3] = MR2 OP[5:3] (WL) [6] = MR2 OP[6] (WLS) [7] = MR2 OP[7] (WR LEV)
7:0	RW	0x00	LP4_MR1_OP It is MR1 Register infromation for LPDDR4. It will be used for write levelling on PHY initiated training. [1:0] = MR1 OP[1:0] (BL) [2] = MR1 OP[2] (WR-PRE) [3] = MR1 OP[3] (RD-PRE) [6:4] = MR1 OP[6:4] (nWR) [7] = MR1 OP[7] (RPST)

DDRPHY_LP4_MR_OP1

Address: **Operational Base** + offset (0x0A84)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	LP4_MR13_OP It is MR13 Register infromation for LPDDR4. It will be used for CBT and Gate training on PHY initiated training. [0] = MR13 OP[0] (CBT) [1] = MR13 OP[1] (RPT) [2] = MR13 OP[2] (VRO) [3] = MR13 OP[3] (VRCG) [4] = MR13 OP[4] (RRO) [5] = MR13 OP[5] (DMD) [6] = MR13 OP[6] (FSP-WR) [7] = MR13 OP[7] (FSP-OP)

DDRPHY_LP5_MR_OP0

Address: **Operational Base** + offset (0x0A88)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	LP5_MR16_OP It is MR16 Register infromation for LPDDR5. It will be used for CBT on PHY initiated training. [1:0] = MR16 OP[1:0] (FSP-WR) [3:2] = MR16 OP[3:2] (FSP-OP) [5:4] = MR16 OP[5:4] (CBT) [6] = MR16 OP[6] (VRCG) [7] = MR16 OP[7] (CBT-PH)
23:16	RW	0x00	LP5_MR12_OP It is MR12 Register infromation for LPDDR5. It will be used for CBT on PHY initiated training. [6:0] = MR12 OP[6:0] (Vref CA) [7] = MR12 OP[7] (VBS)
15:8	RW	0x00	LP5_MR11_OP It is MR11 Register infromation for LPDDR5. It will be used for CBT on PHY initiated training. [2:0] = MR11 OP[2:0] (DQ ODT) [6:4] = MR11 OP[6:4] (CA ODT)
7:0	RW	0x00	LP5_MR10_OP It is MR10 Register infromation for LPDDR5. [3:2] = MR10 OP[3:2] (WCK PST) [5:4] = MR10 OP[5:4] (RDQS PRE) [7:6] = MR10 OP[7:6] (RDQS PST)

DDRPHY_LP5_MR_OP1

Address: **Operational Base** + offset (0x0A8C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	LP5_MR18_OP It is MR18 Register infromation for LPDDR5. It will be used for WCK2CK levelling on PHY initiated training. [2:0] = MR30 OP[2:0] (WCK Termination) [3] = MR30 OP[3] (Reserved) [4] = MR30 OP[4] (WCK ON) [5] = MR30 OP[5] (WCK SYNC) [6] = MR30 OP[6] (WCK2CK Leveling) [7] = MR30 OP[7] (CKR)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	LP5_MR17_OP It is MR17 Register infromation for LPDDR5. It will be used for CBT on PHY initiated training. [2:0] = MR17 OP[2:0] (SoC ODT) [3] = MR17 OP[3] (ODRD-CK) [4] = MR17 OP[4] (ODTD-CS) [5] = MR17 OP[5] (ODTD-CA) [6] = MR17 OP[6] (X8 ODTD Lower) [7] = MR17 OP[7] (X8 ODTD Upper)

DDRPHY_SCHD_FSM

Address: **Operational Base** + offset (0x0A90)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	dvfs_fail_status FSM monitoring signal. It shows failure of phymstr in dfs training fsm.
20	RO	0x0	periodic_fail_status FSM monitoring signal. It shows failure of phymstr in periodic training fsm.
19:16	RO	0x0	schd_train_fsm FSM monitoring signal. It shows training FSM status in all training.
15:13	RO	0x0	schd_rank_fsm FSM monitoring signal. It shows rank FSM status in per rank training.
12:9	RO	0x0	schd_periodic_fsm FSM monitoring signal. It shows periodic training start FSM status.
8:5	RO	0x0	schd_dvfs_trn_fsm FSM monitoring signal. It shows DFS training FSM status in dfs training.
4:0	RO	0x00	schd_periodic_trn_fsm FSM monitoring signal. It shows periodic training FSM status in enabled periodic training.

DDRPHY_CLKMODE_CON

Address: **Operational Base** + offset (0x0A94)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ctrl_phy_dll_2x 1'b0: PHY DLL 1x clock (=WCK/2) 1'b1: PHY DLL 2x clock (=WCK) Use only MODE4 and under 3200Mbps
3	RW	0x1	ctrl_phy_clk_2x 1'b0: PHY 1x clock 1'b1: PHY 2x clock
2:0	RW	0x1	ctrl_phy_mode Clock ratio mode between MC and PHY for LP4/5 combo. 3'h0: LP4 mode DFI clock ratio MC:CK:DQS = 1:4:4 (TBD) 3'h1: LP4 mode DFI clock ratio MC:CK:DQS = 1:2:2 3'h2: LP5 mode DFI clock ratio MC:CK:WCK/RDQS = 1:1:2 3'h3: LP5 mode DFI clock ratio MC:CK:WCK/RDQS = 2:1:4 3'h4: LP5 mode DFI clock ratio MC:CK:WCK/RDQS = 1:1:4 Others: Reseverd

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DDRPHY_CASWIZZLE_CON

Address: **Operational Base** + offset (0x0A98)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x6	ext_dfi_address_p6 Internal dfi_address bit position for external dfi_address[6] This field specifies a connection between the SOC CA[6] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[6] connection in package will be swapped in the following way. SOC CA[6] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.
27	RO	0x0	reserved
26:24	RW	0x5	ext_dfi_address_p5 Internal dfi_address bit position for external dfi_address[5] This field specifies a connection between the SOC CA[5] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[5] connection in package will be swapped in the following way. SOC CA[5] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.
23	RO	0x0	reserved
22:20	RW	0x4	ext_dfi_address_p4 Internal dfi_address bit position for external dfi_address[4] This field specifies a connection between the SOC CA[4] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[4] connection in package will be swapped in the following way. SOC CA[4] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.
19	RO	0x0	reserved
18:16	RW	0x3	ext_dfi_address_p3 Internal dfi_address bit position for external dfi_address[3] This field specifies a connection between the SOC CA[3] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[3] connection in package will be swapped in the following way. SOC CA[3] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:12	RW	0x2	ext_dfi_address_p2 Internal dfi_address bit position for external dfi_address[2] This field specifies a connection between the SOC CA[2] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[2] connection in package will be swapped in the following way. SOC CA[2] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.
11	RO	0x0	reserved
10:8	RW	0x1	ext_dfi_address_p1 Internal dfi_address bit position for external dfi_address[1] This field specifies a connection between the SOC CA[1] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[1] connection in package will be swapped in the following way. SOC CA[1] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.
7	RO	0x0	reserved
6:4	RW	0x0	ext_dfi_addressH_p0 Internal dfi_address bit position for external dfi_addressH[0] for LPDDR5 This field specifies a connection between the SOC CA[0] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[0] connection in package will be swapped in the following way. SOC CA[0] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.
3	RO	0x0	reserved
2:0	RW	0x0	ext_dfi_address_p0 Internal dfi_address bit position for external dfi_address[0] This field specifies a connection between the SOC CA[0] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[0] connection in package will be swapped in the following way. SOC CA[0] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.

DDRPHY_TDLL_CON0

Address: **Operational Base** + offset (0x0A9C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	wrdqtracken For debug purpose
17	RW	0x0	rdparityen For debug purpose
16	RW	0x0	slidingwindowen For debug purpose

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Bit	Attr	Reset Value	Description
15	RW	0x0	SLWUpEn For debug purpose
14	RW	0x0	sfr_tdll_auto For debug purpose
13	RW	0x0	sfr_tdll_dury For debug purpose
12	RW	0x0	sfr_tdll_acc For debug purpose
11	RW	0x0	sfr_tdll_resync For debug purpose
10	RW	0x0	sfr_tdll_start For debug purpose
9	RW	0x0	sfr_wDLL_en For debug purpose
8:7	RW	0x0	sfr_wDLL_sens For debug purpose
6	RW	0x0	ctrl_average For debug purpose
5	RW	0x0	ctrl_set_ref For debug purpose
4	RW	0x0	sfr_dll_fine_track For debug purpose
3:2	RW	0x0	sfr_read_parity_mask For debug purpose
1:0	RW	0x0	sfr_tdll_en For debug purpose

DDRPHY_TDLL_CON1

Address: **Operational Base** + offset (0x0AA0)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	ctrl_tdll_enc For debug purpose
15:8	RO	0x00	reserved
7:0	RW	0x00	sfr_tdll_offset For debug purpose

DDRPHY_TDLL_MON0_DS0

Address: **Operational Base** + offset (0x0AA4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	SELtCH_DS0 For debug purpose
15:14	RO	0x0	reserved
13:0	RO	0x0000	SELtCHL_DS0 For debug purpose

DDRPHY_TDLL_MON1_DS0

Address: **Operational Base** + offset (0x0AA8)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RO	0x00	CNTtCH_DS0 For debug purpose
15:6	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
5:0	RO	0x00	CNTtCHL_DS0 For debug purpose

DDRPHY_TDLL_MON0_DS1

Address: **Operational Base** + offset (0x0AAC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	SELtCH_DS1 For debug purpose
15:14	RO	0x0	reserved
13:0	RO	0x0000	SELtCHL_DS1 For debug purpose

DDRPHY_TDLL_MON1_DS1

Address: **Operational Base** + offset (0x0AB0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RO	0x00	CNTtCH_DS1 For debug purpose
15:6	RO	0x000	reserved
5:0	RO	0x00	CNTtCHL_DS1 For debug purpose

DDRPHY_DQRPARITY_LEFT_DS0

Address: **Operational Base** + offset (0x0AB4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RO	0x0000000	MON_DQRPARITY_LEFT_DS0 For debug purpose

DDRPHY_DQRPARITY_RIGHT_DS0

Address: **Operational Base** + offset (0x0AB8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RO	0x0000000	MON_DQRPARITY_RIGHT_DS0 For debug purpose

DDRPHY_DQFPARITY_LEFT_DS0

Address: **Operational Base** + offset (0x0ABC)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RO	0x0000000	MON_DQFPARITY_LEFT_DS0 For debug purpose

DDRPHY_DQFPARITY_RIGHT_DS0

Address: **Operational Base** + offset (0x0AC0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RO	0x0000000	MON_DQFPARITY_RIGHT_DS0 For debug purpose

DDRPHY_DQRPARITY_LEFT_DS1

Address: **Operational Base** + offset (0x0AC4)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RO	0x0000000	MON_DQRPARITY_LEFT_DS1 For debug purpose

DDRPHY_DQRPARITY_RIGHT_DS1

Address: **Operational Base** + offset (0x0AC8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RO	0x0000000	MON_DQRPARITY_RIGHT_DS1 For debug purpose

DDRPHY_DQFPARITY_LEFT_DS1

Address: **Operational Base** + offset (0x0ACC)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RO	0x0000000	MON_DQFPARITY_LEFT_DS1 For debug purpose

DDRPHY_DQFPARITY_RIGHT_DS1

Address: **Operational Base** + offset (0x0AD0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RO	0x0000000	MON_DQFPARITY_RIGHT_DS1 For debug purpose

DDRPHY_READCAL_URG_DS0

Address: **Operational Base** + offset (0x0AD4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RO	0x000	ctrl_read_cal_urg_DS0 For debug purpose
15:9	RO	0x00	reserved
8:0	RO	0x000	ctrl_read_cal_req_DS0 For debug purpose

DDRPHY_READCAL_URG_DS1

Address: **Operational Base** + offset (0x0AD8)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RO	0x000	ctrl_read_cal_urg_DS1 For debug purpose
15:9	RO	0x00	reserved
8:0	RO	0x000	ctrl_read_cal_req_DS1 For debug purpose

DDRPHY_WCK2CKSYNC_CON0

Address: **Operational Base** + offset (0x0ADC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	ctrl_wck_out_enable_APB I/O OEN control for WCK high-z or low generation in IDLE at DVFS0. 1'b0: Highz 1'b1: Low Bit[0]: Control for DS0 Bit[1]: Control for DS1
1:0	RW	0x0	ctrl_WCK_MODE_APB WCK driving policy 2'b00: WCK is driven by PHY at PHY training with scheduler or WCK is driven by MC at normal operation, and CAS_EN should be 1 at this mode. 2'b01: WCK always be driven by MC, this mode use only WCK always on mode, and CAS_EN should be 0 at this mode. 2'b10: WCK always be driven by PHY, this field is debug purpose. It needs to require MC CAS command related to WCK2CK (not support WS_FS), and CAS_EN should be 1 at this mode. 2'b11: Reserved

DDRPHY_WCK2CKSYNC_CON1

Address: **Operational Base** + offset (0x0AE0)

Bit	Attr	Reset Value	Description
31:28	RW	0x2	ctrl_wck_adj wck start point for write operation If CK:WCK=1:4, set to twckpre_toggle_WR/4 If CK:WCK=1:2, set to twckpre_toggle_WR/2 Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
27	RO	0x0	reserved
26:24	RW	0x3	ctrl_wck2ck_static wck static preamble If CK:WCK=1:4, set to tWCKPRE_Static If CK:WCK=1:2, set to tWCKPRE_Static Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
23:16	RW	0x34	ctrl_wckdur_adj wck duration for write operation If CK:WCK=1:4, set to (WL+4)*4twck If CK:WCK=1:2, set to (WL+8)*2twck Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
15:13	RO	0x0	reserved
12:8	RW	0x07	ctrl_rwck_adj wck start point for read operation Set to twckpre_toggle_RD/4 Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
7:0	RW	0x58	ctrl_rwckdur_adj wck duration for read operation If CK:WCK=1:4, set to (RL+4)*4twck If CK:WCK=1:2, set to (RL+8)*2twck Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.

DDRPHY_DVFS0_WCK2CKSYNC_CON1

Address: **Operational Base** + offset (0x0AE4)

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Bit	Attr	Reset Value	Description
31:28	RW	0x2	dvfs0_wck_adj wck start point for write operation If CK:WCK=1:4, set to twckpre_toggle_WR/4 If CK:WCK=1:2, set to twckpre_toggle_WR/2 Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
27	RO	0x0	reserved
26:24	RW	0x3	dvfs0_wck2ck_static wck static preamble If CK:WCK=1:4, set to tWCKPRE_Static If CK:WCK=1:2, set to tWCKPRE_Static Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
23:16	RW	0x34	dvfs0_wckdur_adj wck duration for write operation If CK:WCK=1:4, set to (WL+4)*4twck If CK:WCK=1:2, set to (WL+8)*2twck Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
15:13	RO	0x0	reserved
12:8	RW	0x07	dvfs0_rwck_adj wck start point for read operation Set to twckpre_toggle_RD/4 Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
7:0	RW	0x58	dvfs0_rwckdur_adj wck duration for read operation If CK:WCK=1:4, set to (RL+4)*4twck If CK:WCK=1:2, set to (RL+8)*2twck Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.

DDRPHY_DVFS1_WCK2CKSYNC_CON1

Address: **Operational Base** + offset (0x0AE8)

Bit	Attr	Reset Value	Description
31:28	RW	0x2	dvfs1_wck_adj wck start point for write operation If CK:WCK=1:4, set to twckpre_toggle_WR/4 If CK:WCK=1:2, set to twckpre_toggle_WR/2 Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
27	RO	0x0	reserved
26:24	RW	0x3	dvfs1_wck2ck_static wck static preamble If CK:WCK=1:4, set to tWCKPRE_Static If CK:WCK=1:2, set to tWCKPRE_Static Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
23:16	RW	0x34	dvfs1_wckdur_adj wck duration for write operation If CK:WCK=1:4, set to (WL+4)*4twck If CK:WCK=1:2, set to (WL+8)*2twck Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RW	0x07	dvfs1_rwck_adj wck start point for read operation Set to twckpre_toggle_RD/4 Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
7:0	RW	0x58	dvfs1_rwckdur_adj wck duration for read operation If CK:WCK=1:4, set to (RL+4)*4twck If CK:WCK=1:2, set to (RL+8)*2twck Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.

DDRPHY_SCHD_CMD_GATING0

Address: **Operational Base** + offset (0x0AEC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	gating_CMD_WCK_GEN_req Blocks WCK gen request when scheduler_sw_mode is enabled.
22	RW	0x0	gating_CMD_DQS_GEN_req Blocks DQS gen request when scheduler_sw_mode is enabled.
21	RW	0x0	gating_CMD_DIRECT_req Blocks DIRECT request when scheduler_sw_mode is enabled.
20	RW	0x0	gating_CMD_PRE_req Blocks PRECHARGE CMD when scheduler_sw_mode is enabled.
19	RW	0x0	gating_CMD_PREA_req Blocks PRECHARGE-ALL CMD when scheduler_sw_mode is enabled.
18	RW	0x0	gating_CMD_REF_req Blocks REFRESH CMD when scheduler_sw_mode is enabled.
17	RW	0x0	gating_CMD_SRE_req Blocks SELF REFRESH ENTER CMD when scheduler_sw_mode is enabled.
16	RW	0x0	gating_CMD_SRX_req Blocks SELF REFRESH EXIT CMD when scheduler_sw_mode is enabled.
15	RW	0x0	gating_CMD_ACT_req Blocks ACTIVE CMD when scheduler_sw_mode is enabled.
14	RW	0x0	gating_CMD_WR_req Blocks WRITE CMD when scheduler_sw_mode is enabled.
13	RW	0x0	gating_CMD_MWR_req Blocks Masked WRITE CMD when scheduler_sw_mode is enabled.
12	RW	0x0	gating_CMD_RD_req Blocks READ CMD when scheduler_sw_mode is enabled.
11	RW	0x0	gating_CMD_MRW_req Blocks MRW CMD when scheduler_sw_mode is enabled.
10	RW	0x0	gating_CMD_MRR_req Blocks MRR CMD when scheduler_sw_mode is enabled.
9	RW	0x0	gating_LP4_MPC_RD_FIFO_req Blocks MPC_RD_FIFO CMD for LPDDR4 when scheduler_sw_mode is enabled.
8	RW	0x0	gating_LP4_MPC_RD_DQ_CAL_req Blocks MPC_RD_DQ_CAL CMD for LPDDR4 when scheduler_sw_mode is enabled.

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Bit	Attr	Reset Value	Description
7	RW	0x0	gating_LP4_MPC_WR_FIFO_req Blocks MPC_WR_FIFO CMD for LPDDR4 when scheduler_sw_mode is enabled.
6	RW	0x0	gating_LP4_MPC_DQS_OSC_START_req Blocks MPC_MPC_DQ_OSC START CMD for LPDDR4 when scheduler_sw_mode is enabled.
5	RW	0x0	gating_LP4_MPC_DQS_OSC_STOP_req Blocks MPC_MPC_DQ_OSC STOP CMD for LPDDR4 when scheduler_sw_mode is enabled.
4	RW	0x0	gating_LP4_MPC_ZQCAL_START_req Blocks MPC_MPC_ZQCAL START CMD for LPDDR4 when scheduler_sw_mode is enabled.
3	RW	0x0	gating_LP4_MPC_ZQCAL_LATCH_req Blocks MPC_MPC_ZQCAL LATCH CMD for LPDDR4 when scheduler_sw_mode is enabled.
2	RW	0x0	gating_CMD_CKE_LOW_req Blocks CKE to low when scheduler_sw_mode is enabled.
1	RW	0x0	gating_CMD_CKE_HIGH_req Blocks CKE to high when scheduler_sw_mode is enabled.
0	RW	0x0	gating_CMD_NOP_req Blocks NOP CMD when scheduler_sw_mode is enabled.

DDRPHY_SCHD_CMD_GATING1

Address: **Operational Base** + offset (0x0AF0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	gating_CMD_CAS_LP5_req Blocks CAS CMD for LPDDR5 when scheduler_sw_mode is enabled.
10	RW	0x0	gating_CMD_LP5_PDE_req Blocks PDE CMD for LPDDR5 when scheduler_sw_mode is enabled.
9	RW	0x0	gating_CMD_LP5_PDX_req_APB Blocks PDX CMD for LPDDR5 when scheduler_sw_mode is enabled.
8	RW	0x0	gating_CMD_LP5_WFF_req_APB Blocks WFF CMD for LPDDR5 when scheduler_sw_mode is enabled.
7	RW	0x0	gating_CMD_LP5_RFF_req_APB Blocks RFF CMD for LPDDR5 when scheduler_sw_mode is enabled.
6	RW	0x0	gating_CMD_LP5_RDC_req_APB Blocks RDC CMD for LPDDR5 when scheduler_sw_mode is enabled.
5	RW	0x0	gating_CMD_LP5_MPC_START_WCK2DQI_req_APB Blocks MPC START WCK2DQI CMD for LPDDR5 when scheduler_sw_mode is enabled.
4	RW	0x0	gating_CMD_LP5_MPC_STOP_WCK2DQI_req_APB Blocks MPC STOP WCK2DQI CMD for LPDDR5 when scheduler_sw_mode is enabled.
3	RW	0x0	gating_CMD_LP5_MPC_START_WCK2DQO_req_APB Blocks MPC START WCK2DQO CMD for LPDDR5 when scheduler_sw_mode is enabled.

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Bit	Attr	Reset Value	Description
2	RW	0x0	gating_CMD_LP5_MPC_STOP_WCK2DQO_req_APB Blocks MPC STOP WCK2DQO CMD for LPDDR5 when scheduler_sw_mode is enabled.
1	RW	0x0	gating_CMD_LP5_MPC_START_ZQ_req_APB Blocks MPC START ZQ CMD for LPDDR5 when scheduler_sw_mode is enabled.
0	RW	0x0	gating_CMD_LP5_MPC_STOP_ZQ_req_APB Blocks MPC STOP ZQ CMD for LPDDR5 when scheduler_sw_mode is enabled.

DDRPHY_DVFS0_WCK2CKSYNC_CON0

Address: **Operational Base** + offset (0x0AF4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	dvfs0_wck_out_enable_APB I/O OEN control for WCK high-z or low generation in IDLE at DVFS0. 1'b0: Highz 1'b1: Low Bit[0]: Control for DS0 Bit[1]: Control for DS1
1:0	RW	0x0	dvfs0_WCK_MODE_APB WCK driving policy at DVFS0 2'b00: WCK is driven by PHY at PHY training with scheduler or WCK is driven by MC at normal operation, and dvfs0_CAS_EN should be 1 at this mode. 2'b01: WCK always be driven by MC, this mode use only WCK always on mode, and dvfs0_CAS_EN should be 0 at this mode. 2'b10: WCK always be driven by PHY, this field is debug purpose. It needs to require MC CAS command related to WCK2CK (not support WS_FS), and dvfs0_CAS_EN should be 1 at this mode. 2'b11: Reserved

DDRPHY_DVFS1_WCK2CKSYNC_CON0

Address: **Operational Base** + offset (0x0AF8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	dvfs1_wck_out_enable_APB I/O OEN control for WCK high-z or low generation in IDLE at DVFS1. 1'b0: Highz 1'b1: Low Bit[0]: Control for DS0 Bit[1]: Control for DS1
1:0	RW	0x0	dvfs1_WCK_MODE_APB WCK driving policy at DVFS1 2'b00: WCK is driven by PHY at PHY training with scheduler or WCK is driven by MC at normal operation, and dvfs1_CAS_EN should be 1 at this mode. 2'b01: WCK always be driven by MC, this mode use only WCK always on mode, and dvfs1_CAS_EN should be 0 at this mode. 2'b10: WCK always be driven by PHY, this field is debug purpose. It needs to require MC CAS command related to WCK2CK (not support WS_FS), and dvfs1_CAS_EN should be 1 at this mode. 2'b11: Reserved

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DDRPHY_MDLL_CON2

Address: **Operational Base** + offset (0x0AFC)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x001	SW_ctrl_lock_value_init SW ctrl_lock_value cotrolled by lock_override_APB

DDRPHY_TESTILP5_DQ0

Address: **Operational Base** + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ0 TEST input port for DQ0 I/O

DDRPHY_TESTILP5_DQ1

Address: **Operational Base** + offset (0x0B04)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ1 TEST input port for DQ1 I/O

DDRPHY_TESTILP5_DQ2

Address: **Operational Base** + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ2 TEST input port for DQ2 I/O

DDRPHY_TESTILP5_DQ3

Address: **Operational Base** + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ3 TEST input port for DQ3 I/O

DDRPHY_TESTILP5_DQ4

Address: **Operational Base** + offset (0x0B10)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ4 TEST input port for DQ4 I/O

DDRPHY_TESTILP5_DQ5

Address: **Operational Base** + offset (0x0B14)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ5 TEST input port for DQ5 I/O

DDRPHY_TESTILP5_DQ6

Address: **Operational Base** + offset (0x0B18)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ6 TEST input port for DQ6 I/O

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DDRPHY_TESTILP5_DQ7

Address: **Operational Base** + offset (0x0B1C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ7 TEST input port for DQ7 I/O

DDRPHY_TESTILP5_DQ8

Address: **Operational Base** + offset (0x0B20)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ8 TEST input port for DQ8 I/O

DDRPHY_TESTILP5_DQ9

Address: **Operational Base** + offset (0x0B24)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ9 TEST input port for DQ9 I/O

DDRPHY_TESTILP5_DQ10

Address: **Operational Base** + offset (0x0B28)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ10 TEST input port for DQ10 I/O

DDRPHY_TESTILP5_DQ11

Address: **Operational Base** + offset (0x0B2C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ11 TEST input port for DQ11 I/O

DDRPHY_TESTILP5_DQ12

Address: **Operational Base** + offset (0x0B30)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ12 TEST input port for DQ12 I/O

DDRPHY_TESTILP5_DQ13

Address: **Operational Base** + offset (0x0B34)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ13 TEST input port for DQ13 I/O

DDRPHY_TESTILP5_DQ14

Address: **Operational Base** + offset (0x0B38)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ14 TEST input port for DQ14 I/O

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DDRPHY_TESTILP5_DQ15

Address: **Operational Base** + offset (0x0B3C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQ15 TEST input port for DQ15 I/O

DDRPHY_TESTILP5_DM0

Address: **Operational Base** + offset (0x0B40)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DM0 TEST input port for DM0 I/O

DDRPHY_TESTILP5_DM1

Address: **Operational Base** + offset (0x0B44)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DM1 TEST input port for DM1 I/O

DDRPHY_TESTILP5_DQS0

Address: **Operational Base** + offset (0x0B48)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQS0 TEST input port for DQS0 I/O

DDRPHY_TESTILP5_DQS1

Address: **Operational Base** + offset (0x0B4C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_DQS1 TEST input port for DQS1 I/O

DDRPHY_TESTILP5_CK

Address: **Operational Base** + offset (0x0B50)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_CK TEST input port for CK I/O

DDRPHY_TESTILP5_CA0

Address: **Operational Base** + offset (0x0B54)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_CA0 TEST input port for CA0 I/O

DDRPHY_TESTILP5_CA1

Address: **Operational Base** + offset (0x0B58)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_CA1 TEST input port for CA1 I/O

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DDRPHY_TESTILP5_CA2

Address: **Operational Base** + offset (0x0B5C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_CA2 TEST input port for CA2 I/O

DDRPHY_TESTILP5_CA3

Address: **Operational Base** + offset (0x0B60)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_CA3 TEST input port for CA3 I/O

DDRPHY_TESTILP5_CA4

Address: **Operational Base** + offset (0x0B64)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_CA4 TEST input port for CA4 I/O

DDRPHY_TESTILP5_CA5

Address: **Operational Base** + offset (0x0B68)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_CA5 TEST input port for CA5 I/O

DDRPHY_TESTILP5_CA6

Address: **Operational Base** + offset (0x0B6C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_CA6 TEST input port for CA6 I/O

DDRPHY_TESTILP5_CS0

Address: **Operational Base** + offset (0x0B70)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_CS0 TEST input port for CS0 I/O

DDRPHY_TESTILP5_CS1

Address: **Operational Base** + offset (0x0B74)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_CS1 TEST input port for CS1 I/O

DDRPHY_TESTILP5_WCK0

Address: **Operational Base** + offset (0x0B78)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_WCK0 TEST input port for WCK0 I/O

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DDRPHY_TESTILP5_WCK1

Address: **Operational Base** + offset (0x0B7C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x199e0	TESTILP5_WCK1 TEST input port for WCK1 I/O

DDRPHY_DQSDUTY_CON0

Address: **Operational Base** + offset (0x0B80)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RW	0x0000000	DQSRiseDuty_rank0_DS0 For debug purpose

DDRPHY_DQSDUTY_CON1

Address: **Operational Base** + offset (0x0B84)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RW	0x0000000	DQSFallDuty_rank0_DS0 For debug purpose

DDRPHY_DQSDUTY_CON2

Address: **Operational Base** + offset (0x0B88)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RW	0x0000000	DQSRiseDuty_rank1_DS0 For debug purpose

DDRPHY_DQSDUTY_CON3

Address: **Operational Base** + offset (0x0B8C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RW	0x0000000	DQSFallDuty_rank1_DS0 For debug purpose

DDRPHY_DQSDUTY_CON4

Address: **Operational Base** + offset (0x0B90)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RW	0x0000000	DQSRiseDuty_rank0_DS1 For debug purpose

DDRPHY_DQSDUTY_CON5

Address: **Operational Base** + offset (0x0B94)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RW	0x0000000	DQSFallDuty_rank0_DS1 For debug purpose

DDRPHY_DQSDUTY_CON6

Address: **Operational Base** + offset (0x0B98)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RW	0x0000000	DQSRiseDuty_rank1_DS1 For debug purpose

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DDRPHY_DQSDUTY_CON7

Address: **Operational Base** + offset (0x0B9C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RW	0x0000000	DQSFallDuty_rank1_DS1 For debug purpose

DDRPHY_MON_RCNT0

Address: **Operational Base** + offset (0x0BA0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	MON_RCNT_DS0 For debug purpose

DDRPHY_MON_RCNT1

Address: **Operational Base** + offset (0x0BA4)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RO	0x0000	MON_RCNT_DS0 For debug purpose

DDRPHY_MON_RCNT2

Address: **Operational Base** + offset (0x0BA8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	MON_RCNT_DS1 For debug purpose

DDRPHY_MON_RCNT3

Address: **Operational Base** + offset (0x0BAC)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RO	0x0000	MON_RCNT_DS1 For debug purpose

DDRPHY_CMD_DESKEWC_CODE0

Address: **Operational Base** + offset (0x0BB0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	Ca1DeSkewCode CA1 De-skew center code
15:10	RO	0x00	reserved
9:0	RO	0x000	Ca0DeSkewCode CA0 De-skew center code

DDRPHY_CMD_DESKEWC_CODE1

Address: **Operational Base** + offset (0x0BB4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	Ca3DeSkewCode CA3 De-skew center code
15:10	RO	0x00	reserved
9:0	RO	0x000	Ca2DeSkewCode CA2 De-skew center code

DDRPHY_CMD_DESKEWC_CODE2

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Address: **Operational Base** + offset (0x0BB8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	Ca5DeSkewCode CA5 De-skew center code
15:10	RO	0x00	reserved
9:0	RO	0x000	Ca4DeSkewCode CA4 De-skew center code

DDRPHY_CMD_DESKEWC_CODE3

Address: **Operational Base** + offset (0x0BBC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	Ca6DeSkewCode CA6 De-skew center code

DDRPHY_CMD_DESKEWC_CODE4

Address: **Operational Base** + offset (0x0BC0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	CsFineDeSkewCode CS Fine training De-skew center code
15:10	RO	0x00	reserved
9:0	RO	0x000	CsCoarseDeSkewCode CS Coarse training De-skew center code

DDRPHY_CBT_CAL_STAT0

Address: **Operational Base** + offset (0x0BC4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x0	cbt_hw_cal_done LPDDR4 HW Calibration done signal
24:17	RO	0x00	cbt_vwm_max_flag Command bus training searching max flag cbt_fail_status[6:1]: CA0~CA5 cbt_fail_status[7]: CS Coarse cbt_fail_status[8]: CS Fine
16:9	RO	0x00	cbt_fail_status Command bus training fail status cbt_fail_status[6:1]: CA0~CA5 cbt_fail_status[7]: CS Coarse cbt_fail_status[8]: CS Fine
8:1	RO	0x00	cbt_pass_status Command bus training pass status cbt_pass_status[6:1]: CA0~CA5 cbt_pass_status[7]: CS Coarse cbt_pass_status[8]: CS Fine
0	RO	0x0	cbt_ck_offset_fail CS0 De-skew center code

DDRPHY_CMD_LEFT_CODE0

Address: **Operational Base** + offset (0x0BC8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	Ca1VWMLCode Command bus training CA1 Left code

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Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:0	RO	0x000	Ca0VWMLCode Command bus training CA0 Left code

DDRPHY_CMD_LEFT_CODE1

Address: **Operational Base** + offset (0x0BCC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	Ca3VWMLCode Command bus training CA3 Left code
15:10	RO	0x00	reserved
9:0	RO	0x000	Ca2VWMLCode Command bus training CA2 Left code

DDRPHY_CMD_LEFT_CODE2

Address: **Operational Base** + offset (0x0BD0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	Ca5VWMLCode Command bus training CA5 Left code
15:10	RO	0x00	reserved
9:0	RO	0x000	Ca4VWMLCode Command bus training CA4 Left code

DDRPHY_CMD_LEFT_CODE4

Address: **Operational Base** + offset (0x0BD8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	CsVWMLFineCode CS Fine training CS Left code
15:10	RO	0x00	reserved
9:0	RO	0x000	CsVWMLCoarseCode CS Coarse training CS Left code

DDRPHY_CMD_RIGHT_CODE0

Address: **Operational Base** + offset (0x0BDC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	Ca1VWMRCode Command bus training CA1 Right code
15:10	RO	0x00	reserved
9:0	RO	0x000	Ca0VWMRCode Command bus training CA0 Right code

DDRPHY_CMD_RIGHT_CODE1

Address: **Operational Base** + offset (0x0BE0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	Ca3VWMRCode Command bus training CA3 Right code
15:10	RO	0x00	reserved
9:0	RO	0x000	Ca2VWMRCode Command bus training CA2 Right code

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DDRPHY_CMD_RIGHT_CODE2

Address: **Operational Base** + offset (0x0BE4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	Ca5VWMRCode Command bus training CA5 Right code
15:10	RO	0x00	reserved
9:0	RO	0x000	Ca4VWMRCode Command bus training CA4 Right code

DDRPHY_CMD_RIGHT_CODE4

Address: **Operational Base** + offset (0x0BEC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	CsVWMRFineCode CS Fine training CS Right code
15:10	RO	0x00	reserved
9:0	RO	0x000	CsVWMRCoarseCode CS Coarse training CS Right code

DDRPHY_DVFS0_CLKMODE_CON

Address: **Operational Base** + offset (0x0BF0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	dvfs0_phy_dll_2x 1'b0: PHY DLL 1x clock (=WCK/2) 1'b1: PHY DLL 2x clock (=WCK) Use only MODE4 and Under 3200Mbps
3	RW	0x1	dvfs0_phy_clk_2x 1'b0: PHY 1x clock for DVFS0 1'b1: PHY 2x clock
2:0	RW	0x1	dvfs0_phy_mode Clock ratio mode between MC and PHY for DVFS0 3'h0: LP4 mode DFI clock ratio MC: CK: DQS = 1:4:4 (TBD) 3'h1: LP4 mode DFI clock ratio MC: CK: DQS = 1:2:2 3'h2: LP5 mode DFI clock ratio MC: CK: WCK/RDQS = 1:1:2 3'h3: LP5 mode DFI clock ratio MC: CK: WCK/RDQS = 2:1:4 3'h4: LP5 mode DFI clock ratio MC: CK: WCK/RDQS = 1:1:4

DDRPHY_DVFS1_CLKMODE_CON

Address: **Operational Base** + offset (0x0BF4)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	dvfs1_phy_dll_2x 1'b0: PHY DLL 1x clock (=WCK/2) 1'b1: PHY DLL 2x clock (=WCK) Use only MODE4 and Under 3200Mbps
3	RW	0x1	dvfs1_phy_clk_2x 1'b0: PHY 1x clock for DVFS1 1'b1: PHY 2x clock

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Bit	Attr	Reset Value	Description
2:0	RW	0x1	dvfs1_phy_mode Clock ratio mode between MC and PHY for DVFS1 3'h0: LP4 mode DFI clock ratio MC: CK: DQS = 1:4:4 (TBD) 3'h1: LP4 mode DFI clock ratio MC: CK: DQS = 1:2:2 3'h2: LP5 mode DFI clock ratio MC: CK: WCK/RDQS = 1:1:2 3'h3: LP5 mode DFI clock ratio MC: CK: WCK/RDQS = 2:1:4 3'h4: LP5 mode DFI clock ratio MC: CK: WCK/RDQS = 1:1:4

DDRPHY_DVFS0_DCC_CON0

Address: **Operational Base** + offset (0x0BF8)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	dvfs0_duty_manual For debug purpose
9:5	RW	0x00	dvfs0_DUTY_NCODE For debug purpose
4:0	RW	0x00	dvfs0_DUTY_PCODE For debug purpose

DDRPHY_DVFS1_DCC_CON0

Address: **Operational Base** + offset (0x0BFC)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	dvfs1_duty_manual For debug purpose
9:5	RW	0x00	dvfs1_DUTY_NCODE For debug purpose
4:0	RW	0x00	dvfs1_DUTY_PCODE For debug purpose

DDRPHY_PTC_CON0

Address: **Operational Base** + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x26	ptc_ext_zq_mode_vref For debug purpose
23	RO	0x0	reserved
22:20	RW	0x7	ptc_ext_zq_mode_dds For debug purpose
19	RO	0x0	reserved
18:16	RW	0x7	ptc_ext_zq_mode_pdds For debug purpose
15	RO	0x0	reserved
14:12	RW	0x0	ptc_ext_zq_force_impp For debug purpose
11	RO	0x0	reserved
10:8	RW	0x0	ptc_ext_zq_force_impn For debug purpose
7	RO	0x0	reserved
6:4	RO	0x0	ptc_ext_zq_pmon For debug purpose
3	RO	0x0	reserved
2:0	RO	0x0	ptc_ext_zq_nmon For debug purpose

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DDRPHY_PTC_CON1

Address: **Operational Base** + offset (0x0C04)

Bit	Attr	Reset Value	Description
31	RW	0x0	ptc_ext_zq_force For debug purpose
30	RO	0x0	reserved
29	RO	0x0	ptc_ext_zq_end For debug purpose
28:13	RO	0x0000	reserved
12:8	RW	0x00	ptc_ext_ref For debug purpose
7:5	RO	0x0	reserved
4	RW	0x1	ptc_ext_dfdqs For debug purpose
3	RW	0x0	ptc_ext_cmosrcv For debug purpose
2	RW	0x0	ptc_ext_en For debug purpose
1	RW	0x0	ptc_ext_out For debug purpose
0	RW	0x1	ptc_ext_read For debug purpose

DDRPHY_PTC_CON2

Address: **Operational Base** + offset (0x0C08)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:20	RO	0x100	ptc_ext_lock_value For debug purpose
19	RO	0x0	reserved
18:12	RW	0x08	ptc_ext_start_point For debug purpose
11	RO	0x0	reserved
10:4	RW	0x08	ptc_ext_inc For debug purpose
3	RW	0x0	ptc_ext_half For debug purpose
2	RO	0x0	ptc_ext_clock For debug purpose
1	RO	0x0	ptc_ext_flock For debug purpose
0	RO	0x0	ptc_ext_locked For debug purpose

DDRPHY_PTC_CON3

Address: **Operational Base** + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	ptc_ext_offsetr For debug purpose
15:10	RO	0x00	reserved
9:0	RW	0x000	ptc_ext_offsetw For debug purpose

DDRPHY_PTC_CON4

Address: **Operational Base** + offset (0x0C10)

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	ptc_ext_mode For debug purpose
27	RO	0x0	reserved
26:24	RW	0x0	ptc_ext_shiftc For debug purpose
23:20	RW	0x0	ptc_ext_debug For debug purpose
19:17	RO	0x0	reserved
16	RO	0x0	ptc_ext_init_complete For debug purpose
15:4	RO	0x000	reserved
3	RW	0x0	ptc_ext_rdlvl_en For debug purpose
2	RW	0x0	ptc_ext_rdlvl_wr_en For debug purpose
1	RW	0x0	ptc_ext_gatelvl_en For debug purpose
0	RW	0x0	ptc_ext_write_lvl_en For debug purpose

DDRPHY_PTC_CON5

Address: **Operational Base** + offset (0x0C14)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	test_compare Test compare
12	RW	0x0	test_end Test end
11:9	RO	0x0	reserved
8	RW	0x0	test_start Test start
7:6	RO	0x0	reserved
5	RO	0x0	test_err_ds1 For dpc1
4	RO	0x0	test_err_ds0 For dpc0
3:2	RO	0x0	reserved
1	RO	0x0	test_oky_ds1 For dpc1
0	RO	0x0	test_oky_ds0 For dpc0

DDRPHY_PTC_CON6

Address: **Operational Base** + offset (0x0C18)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x02	wrlatadj Feedback write latency
23:21	RO	0x0	reserved
20:16	RW	0x02	rdlatadj Feedback read latency
15:8	RW	0x11	wrincradj Feedback write to read latency

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Bit	Attr	Reset Value	Description
7	RW	0x0	ptc_ext_pulld_dq For debug purpose
6	RW	0x0	ptc_ext_pulld_dqs For debug purpose
5	RW	0x0	burst16_mode For debug purpose
4	RW	0x0	PAT_INIT For debug purpose
3	RO	0x0	reserved
2	RW	0x0	infinite_loop_en For debug purpose
1	RW	0x0	PTC_MODE_DS1 Set initial pattern control
0	RW	0x0	PTC_MODE_DS0 phy test control mode for DPC0

DDRPHY_PTC_CON7

Address: **Operational Base** + offset (0x0C1C)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	ptc_wrdata_p3 Data pattern for wrdata p3
15:0	RW	0x00ff	ptc_wrdata_p2 Data pattern for wrdata p2

DDRPHY_PTC_CON8

Address: **Operational Base** + offset (0x0C20)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	ptc_wrdata_p1 Data pattern for wrdata p1
15:0	RW	0x00ff	ptc_wrdata_p0 Data pattern for wrdata p0

DDRPHY_PTC_CON9

Address: **Operational Base** + offset (0x0C24)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	ptc_exp_wrdata_p3 Expected data pattern for wrdata p3
15:0	RW	0x00ff	ptc_exp_wrdata_p2 Expected data pattern for wrdata p2

DDRPHY_PTC_CON10

Address: **Operational Base** + offset (0x0C28)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	ptc_exp_wrdata_p1 Expected data pattern for wrdata p1
15:0	RW	0x00ff	ptc_exp_wrdata_p0 Expected data pattern for wrdata p0

DDRPHY_PTC_CON11

Address: **Operational Base** + offset (0x0C2C)

Bit	Attr	Reset Value	Description
31	RW	0x1	mode_phy For debug purpose
30	RW	0x0	mode_scan For debug purpose

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Bit	Attr	Reset Value	Description
29	RW	0x0	mode_nand For debug purpose
28	RW	0x0	mode_highz For debug purpose
27	RW	0x0	mode_mux For debug purpose
26:24	RW	0x0	mode_run For debug purpose
23:16	RO	0x00	reserved
15:14	RW	0x0	ptc_wrdata_mask_p3 Data mask pattern for wrdata mask p3
13:12	RW	0x0	ptc_wrdata_mask_p2 Data mask pattern for wrdata mask p2
11:10	RW	0x0	ptc_wrdata_mask_p1 Data mask pattern for wrdata mask p1
9:8	RW	0x0	ptc_wrdata_mask_p0 Data mask pattern for wrdata mask p0
7:6	RW	0x0	ptc_exp_wrdata_mask_p3 Expected data mask pattern for wrdata mask p3
5:4	RW	0x0	ptc_exp_wrdata_mask_p2 Expected data mask pattern for wrdata mask p2
3:2	RW	0x0	ptc_exp_wrdata_mask_p1 Expected data mask pattern for wrdata mask p1
1:0	RW	0x0	ptc_exp_wrdata_mask_p0 Expected data mask pattern for wrdata mask p0

DDRPHY_PTC_CON12

Address: **Operational Base** + offset (0x0C30)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	rddata_w3_q1_ds0 w3 read data for DPC0
15:0	RO	0x0000	rddata_w2_q1_ds0 w2 read data for DPC0

DDRPHY_PTC_CON13

Address: **Operational Base** + offset (0x0C34)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	rddata_w1_q1_ds0 w1 read data for DPC0
15:0	RO	0x0000	rddata_w0_q1_ds0 w0 read data for DPC0

DDRPHY_PTC_CON14

Address: **Operational Base** + offset (0x0C38)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	rddata_w3_q1_ds1 w3 read data for DPC1
15:0	RO	0x0000	rddata_w2_q1_ds1 w2 read data for DPC1

DDRPHY_PTC_CON15

Address: **Operational Base** + offset (0x0C3C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	rddata_w1_q1_ds1 w1 read data for DPC1

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	rddata_w0_q1_ds1 w0 read data for DPC1

DDRPHY_PTC_CON16

Address: **Operational Base** + offset (0x0C40)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RO	0x00	dvfs_wrtrn_monitoring_ds1_cs1 For debug purpose
23:22	RO	0x0	reserved
21:16	RO	0x00	dvfs_wrtrn_monitoring_ds0_cs1 For debug purpose
15:14	RO	0x0	reserved
13:8	RO	0x00	dvfs_wrtrn_monitoring_ds1_cs0 For debug purpose
7:6	RO	0x0	reserved
5:0	RO	0x00	dvfs_wrtrn_monitoring_ds0_cs0 For debug purpose

DDRPHY_PTC_CON20

Address: **Operational Base** + offset (0x0C50)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	test_oky_dq test_oky_dq

DDRPHY_PTC_CON21

Address: **Operational Base** + offset (0x0C54)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	test_err_dq test_err_dq

DDRPHY_PTC_CON22

Address: **Operational Base** + offset (0x0C58)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RO	0x0	test_oky_dm test_oky_dm
7:2	RO	0x00	reserved
1:0	RO	0x0	test_err_dm test_err_dm

DDRPHY_Periodic_ZQ_CON

Address: **Operational Base** + offset (0x0C70)

Bit	Attr	Reset Value	Description
31	RW	0x0	periodic_zq_cnt_en Periodic zq counter enable (Enable periodic ZQ calibration)
30:0	RW	0x000403f5	periodic_zq_time periodic_zq_time is defined interval of periodic zq calibrationn Total time = periodic_time* (period of clk_osc)

DDRPHY_PRBS_LEFT_MARGIN_DQ0

Address: **Operational Base** + offset (0x0D00)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq0 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dq0 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ0

Address: **Operational Base** + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq0 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dq0 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DQ1

Address: **Operational Base** + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq1 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dq1 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ1

Address: **Operational Base** + offset (0x0D0C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq1 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dq1 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DQ2

Address: **Operational Base** + offset (0x0D10)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq2 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	prbs_offset_left_h_dq2 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ2

Address: **Operational Base** + offset (0x0D14)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq2 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dq2 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DQ3

Address: **Operational Base** + offset (0x0D18)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq3 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dq3 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ3

Address: **Operational Base** + offset (0x0D1C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq3 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dq3 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DQ4

Address: **Operational Base** + offset (0x0D20)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq4 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dq4 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ4

Address: **Operational Base** + offset (0x0D24)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq4 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dq4 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DQ5

Address: **Operational Base** + offset (0x0D28)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq5 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dq5 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ5

Address: **Operational Base** + offset (0x0D2C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq5 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dq5 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DQ6

Address: **Operational Base** + offset (0x0D30)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq6 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dq6 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ6

Address: **Operational Base** + offset (0x0D34)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq6 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	prbs_offset_right_h_dq6 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DQ7

Address: **Operational Base** + offset (0x0D38)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq7 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dq7 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ7

Address: **Operational Base** + offset (0x0D3C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq7 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dq7 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DQ8

Address: **Operational Base** + offset (0x0D40)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq8 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dq8 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ8

Address: **Operational Base** + offset (0x0D44)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq8 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dq8 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DQ9

Address: **Operational Base** + offset (0x0D48)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq9 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dq9 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ9

Address: **Operational Base** + offset (0x0D4C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq9 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dq9 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DQ10

Address: **Operational Base** + offset (0x0D50)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq10 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dq10 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ10

Address: **Operational Base** + offset (0x0D54)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq10 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dq10 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DQ11

Address: **Operational Base** + offset (0x0D58)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq11 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	prbs_offset_left_h_dq11 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ11

Address: **Operational Base** + offset (0x0D5C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq11 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dq11 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DQ12

Address: **Operational Base** + offset (0x0D60)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq12 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dq12 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ12

Address: **Operational Base** + offset (0x0D64)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq12 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dq12 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DQ13

Address: **Operational Base** + offset (0x0D68)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq13 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dq13 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ13

Address: **Operational Base** + offset (0x0D6C)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq13 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dq13 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DQ14

Address: **Operational Base** + offset (0x0D70)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq14 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dq14 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ14

Address: **Operational Base** + offset (0x0D74)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq14 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dq14 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DQ15

Address: **Operational Base** + offset (0x0D78)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dq15 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dq15 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DQ15

Address: **Operational Base** + offset (0x0D7C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dq15 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	prbs_offset_right_h_dq15 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DM0

Address: **Operational Base** + offset (0x0D80)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dm0 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dm0 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DM0

Address: **Operational Base** + offset (0x0D84)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dm0 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dm0 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_LEFT_MARGIN_DM1

Address: **Operational Base** + offset (0x0D88)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_left_l_dm1 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_left_h_dm1 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_PRBS_RIGHT_MARGIN_DM1

Address: **Operational Base** + offset (0x0D8C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	prbs_offset_right_l_dm1 PRBS offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1
15:10	RO	0x00	reserved
9:0	RO	0x000	prbs_offset_right_h_dm1 PRBS offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1

DDRPHY_WR_BYTE0_CYC_CS0_CODE

Address: **Operational Base** + offset (0x0DC0)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RO	0x0	ctrl_shift_dm_ds0_cs0 Write DM Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
23:21	RO	0x0	ctrl_shift_dq7_ds0_cs0 Write DQ7 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
20:18	RO	0x0	ctrl_shift_dq6_ds0_cs0 Write DQ6 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
17:15	RO	0x0	ctrl_shift_dq5_ds0_cs0 Write DQ5 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RO	0x0	ctrl_shift_dq4_ds0_cs0 Write DQ4 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
11:9	RO	0x0	ctrl_shift_dq3_ds0_cs0 Write DQ3 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
8:6	RO	0x0	ctrl_shift_dq2_ds0_cs0 Write DQ2 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
5:3	RO	0x0	ctrl_shift_dq1_ds0_cs0 Write DQ1 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RO	0x0	ctrl_shift_dq0_ds0_cs0 Write DQ0 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_WR_BYTE1_CYC_CS0_CODE

Address: **Operational Base** + offset (0x0DC4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RO	0x0	ctrl_shift_dm_ds1_cs0 Write DM Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
23:21	RO	0x0	ctrl_shift_dq7_ds1_cs0 Write DQ7 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
20:18	RO	0x0	ctrl_shift_dq6_ds1_cs0 Write DQ6 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

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Bit	Attr	Reset Value	Description
17:15	RO	0x0	ctrl_shift_dq5_ds1_cs0 Write DQ5 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RO	0x0	ctrl_shift_dq4_ds1_cs0 Write DQ4 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
11:9	RO	0x0	ctrl_shift_dq3_ds1_cs0 Write DQ3 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
8:6	RO	0x0	ctrl_shift_dq2_ds1_cs0 Write DQ2 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
5:3	RO	0x0	ctrl_shift_dq1_ds1_cs0 Write DQ1 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RO	0x0	ctrl_shift_dq0_ds1_cs0 Write DQ0 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_WR_BYTE0_CYC_CS1_CODE

Address: **Operational Base** + offset (0x0DC8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RO	0x0	ctrl_shift_dm_ds0_cs1 Write DM Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
23:21	RO	0x0	ctrl_shift_dq7_ds0_cs1 Write DQ7 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
20:18	RO	0x0	ctrl_shift_dq6_ds0_cs1 Write DQ6 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
17:15	RO	0x0	ctrl_shift_dq5_ds0_cs1 Write DQ5 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RO	0x0	ctrl_shift_dq4_ds0_cs1 Write DQ4 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
11:9	RO	0x0	ctrl_shift_dq3_ds0_cs1 Write DQ3 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

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Bit	Attr	Reset Value	Description
8:6	RO	0x0	ctrl_shift_dq2_ds0_cs1 Write DQ2 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
5:3	RO	0x0	ctrl_shift_dq1_ds0_cs1 Write DQ1 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RO	0x0	ctrl_shift_dq0_ds0_cs1 Write DQ0 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_WR_BYTE1_CYC_CS1_CODE

Address: **Operational Base** + offset (0x0DCC)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RO	0x0	ctrl_shift_dm_ds1_cs1 Write DM Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
23:21	RO	0x0	ctrl_shift_dq7_ds1_cs1 Write DQ7 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
20:18	RO	0x0	ctrl_shift_dq6_ds1_cs1 Write DQ6 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
17:15	RO	0x0	ctrl_shift_dq5_ds1_cs1 Write DQ5 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RO	0x0	ctrl_shift_dq4_ds1_cs1 Write DQ4 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
11:9	RO	0x0	ctrl_shift_dq3_ds1_cs1 Write DQ3 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
8:6	RO	0x0	ctrl_shift_dq2_ds1_cs1 Write DQ2 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
5:3	RO	0x0	ctrl_shift_dq1_ds1_cs1 Write DQ1 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RO	0x0	ctrl_shift_dq0_ds1_cs1 Write DQ0 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_SW_WR_BYTE0_CYC_CS0_CODE

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Address: **Operational Base** + offset (0x0DD0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	sw_shift_dm_ds0_cs0 SW control for Write DM Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
23:21	RW	0x0	sw_shift_dq7_ds0_cs0 SW control for Write DQ7 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
20:18	RW	0x0	sw_shift_dq6_ds0_cs0 SW control for Write DQ6 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
17:15	RW	0x0	sw_shift_dq5_ds0_cs0 SW control for Write DQ5 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RW	0x0	sw_shift_dq4_ds0_cs0 SW control for Write DQ4 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
11:9	RW	0x0	sw_shift_dq3_ds0_cs0 SW control for Write DQ3 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
8:6	RW	0x0	sw_shift_dq2_ds0_cs0 SW control for Write DQ2 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
5:3	RW	0x0	sw_shift_dq1_ds0_cs0 SW control for Write DQ1 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RW	0x0	sw_shift_dq0_ds0_cs0 SW control for Write DQ0 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_SW_WR_BYTE1_CYC_CS0_CODE

Address: **Operational Base** + offset (0x0DD4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	sw_shift_dm_ds1_cs0 SW control for Write DM Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
23:21	RW	0x0	sw_shift_dq7_ds1_cs0 SW control for Write DQ7 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
20:18	RW	0x0	sw_shift_dq6_ds1_cs0 SW control for Write DQ6 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

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Bit	Attr	Reset Value	Description
17:15	RW	0x0	sw_shift_dq5_ds1_cs0 SW control for Write DQ5 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RW	0x0	sw_shift_dq4_ds1_cs0 SW control for Write DQ4 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
11:9	RW	0x0	sw_shift_dq3_ds1_cs0 SW control for Write DQ3 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
8:6	RW	0x0	sw_shift_dq2_ds1_cs0 SW control for Write DQ2 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
5:3	RW	0x0	sw_shift_dq1_ds1_cs0 SW control for Write DQ1 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RW	0x0	sw_shift_dq0_ds1_cs0 SW control for Write DQ0 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_SW_WR_BYTE0_CYC_CS1_CODE

Address: **Operational Base** + offset (0x0DD8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	sw_shift_dm_ds0_cs1 SW control for Write DM Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
23:21	RW	0x0	sw_shift_dq7_ds0_cs1 SW control for Write DQ7 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
20:18	RW	0x0	sw_shift_dq6_ds0_cs1 SW control for Write DQ6 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
17:15	RW	0x0	sw_shift_dq5_ds0_cs1 SW control for Write DQ5 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RW	0x0	sw_shift_dq4_ds0_cs1 SW control for Write DQ4 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
11:9	RW	0x0	sw_shift_dq3_ds0_cs1 SW control for Write DQ3 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

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Bit	Attr	Reset Value	Description
8:6	RW	0x0	sw_shift_dq2_ds0_cs1 SW control for Write DQ2 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
5:3	RW	0x0	sw_shift_dq1_ds0_cs1 SW control for Write DQ1 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RW	0x0	sw_shift_dq0_ds0_cs1 SW control for Write DQ0 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_SW_WR_BYTE1_CYC_CS1_CODE

Address: **Operational Base** + offset (0x0DDC)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	sw_shift_dm_ds1_cs1 SW control for Write DM Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
23:21	RW	0x0	sw_shift_dq7_ds1_cs1 SW control for Write DQ7 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
20:18	RW	0x0	sw_shift_dq6_ds1_cs1 SW control for Write DQ6 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
17:15	RW	0x0	sw_shift_dq5_ds1_cs1 SW control for Write DQ5 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RW	0x0	sw_shift_dq4_ds1_cs1 SW control for Write DQ4 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
11:9	RW	0x0	sw_shift_dq3_ds1_cs1 SW control for Write DQ3 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
8:6	RW	0x0	sw_shift_dq2_ds1_cs1 SW control for Write DQ2 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
5:3	RW	0x0	sw_shift_dq1_ds1_cs1 SW control for Write DQ1 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RW	0x0	sw_shift_dq0_ds1_cs1 SW control for Write DQ0 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_WCKOSC_CON0

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Address: **Operational Base** + offset (0x0DE0)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0437	ctrl_osc_counter Controls oscillator counter
15:8	RW	0x3f	ctrl_osc_runtime Controls oscillator runtime
7:1	RO	0x00	reserved
0	RW	0x0	ctrl_wck_osc_en Controls WCK oscillator enable

DDRPHY_WCKOSC_CON1

Address: **Operational Base** + offset (0x0DE4)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x01	wck_osc_upd_range_APB Sets WCK oscillator update range
7:6	RW	0x2	wck_osc_avg_window_size_APB Sets WCK oscillator average window size
5	RW	0x0	wck_osc_en_APB Sets WCK oscillator enable
4:3	RW	0x0	wck_osc_dq_swizzle_APB 2'b00: No SWAP 2'b01: BYTE SWAP + BIT SWAP 2'b10: BYTE SWAP 2'b11: BIT SWAP
2:0	RW	0x2	wck_osc_multiplier_APB Sets WCK oscillator multiplier

DDRPHY_WCKOSC_CON2

Address: **Operational Base** + offset (0x0DE8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0001	wck_osc_cnt_new_cs1 Read WCK oscillator counter for cs1
15:0	RO	0x0001	wck_osc_cnt_new_cs0 Read WCK oscillator counter for cs0

DDRPHY_WCKOSC_CON3

Address: **Operational Base** + offset (0x0DEC)

Bit	Attr	Reset Value	Description
31	RO	0x1	wck_osc_cnt_applied Read WCK oscillator applied counter
30:27	RO	0x0	reserved
26	RO	0x0	wck_osc_overflow_cs1 Read WCK oscillator overflow cs1
25:16	RO	0x000	offsetw_osc_cs1 Read offsetw oscillator cs1
15:11	RO	0x00	reserved
10	RO	0x0	wck_osc_overflow_cs0 Read WCK oscillator overflow cs0
9:0	RO	0x000	offsetw_osc_cs0 Read offsetw oscillator cs0

DDRPHY_DVFS0_WCKOSC_CON0

Address: **Operational Base** + offset (0x0DF0)

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Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0437	dvfs0_osc_counter Controls dvfs0 oscillator counter
15:8	RW	0x3f	dvfs0_osc_runtime Controls dvfs0 oscillator runtime
7:1	RO	0x00	reserved
0	RW	0x0	dvfs0_wck_osc_en Controls dvfs0 WCK oscillator enable

DDRPHY_DVFS1_WCKOSC_CON0

Address: **Operational Base** + offset (0x0DF4)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0437	dvfs1_osc_counter Controls dvfs1 oscillator counter
15:8	RW	0x3f	dvfs1_osc_runtime Controls dvfs1 oscillator runtime
7:1	RO	0x00	reserved
0	RW	0x0	dvfs1_wck_osc_en Controls dvfs1 WCK oscillator enable

DDRPHY_WRTRN_PARA_CON0

Address: **Operational Base** + offset (0x0DF8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:20	RW	0x12	RDLAT_LP5_RFF_DMI_ON RFU (Reserved for future use) This field control PHY read latency on write training when LP5_RFF_DMI_ON is High. Read latency on write training can be different from Normal operation because of DRAM DMI buffer is on with LP5_RFF_DMI_ON. So If LP5_RFF_DMI_ON is high, user should be set to PHY read latency with READ DBI ON additionally as per PHY and Jedec specification.
19	RO	0x0	reserved
18	RW	0x0	LP5_RFF_DMI_ON RFU (Reserved for future use) This field control RFF DMI buffer on MODE for PHY write training, 1'b1: RFF DMI buffer is on when Read dbi and Read data copy MR settings are off during write training. 1'b0: Followed by user specific condition during write training.
17	RW	0x0	ctrl_RFF_CAS_IGNORE CAS command with RFF ignore during write training 1'b1: Ignore 1'b0: No ignore
16	RW	0x0	WFF_RFF_TCCD_USER_MODE This field is MODE for control timing delay from WFF to RFF by User setting. This filed should used above 4266Mbps. 1'b1: Timing delay from WFF to RFF will be WFF_RFF_TCCD. 1'b0: Timing delay from WFF to RFF will be WL+BL_n+tWTR by SFR of PHY scheduler.

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Bit	Attr	Reset Value	Description
15:8	RW	0x03	WFF_RFF_TCCD This field control timing delay from WFF to RFF during write training using PHY scheduler. And WFF_RFF_TCCD_USER_MODE should be 1 for apply this parameter in normal operation. This filed should used above 4266Mbps. Dynamic sync mode: WFF_RFF_TCCD = FIFO tWTR +1 WCK always on mode (=free running mode): WFF_RFF_TCCD = FIFO tWTR
7	RO	0x0	reserved
6	RW	0x0	wrtrn_extra_resync This field control extra DLL update during write training.
5:0	RW	0x16	wrtrn_trden2resp This field control timing delay from t_rddata_en to t_rdlvl_resp during write training using PHY scheduler. Please only use 0x3 pr 0x16 (default value).

DDRPHY_DVFS0_WRTRN_PARA_CON0

Address: **Operational Base** + offset (0x0DFC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:20	RW	0x12	dvfs0_RDLAT_LP5_RFF_DMI_ON RFU (Reserved for future use) This field control PHY read latency on write training when dvfs0_LP5_RFF_DMI_ON is High. Read latency on write training can be different from Normal operation because of DRAM DMI buffer is on with dvfs0_LP5_RFF_DMI_ON. So If dvfs0_LP5_RFF_DMI_ON is High, User should be set to PHY read latency with READ DBI ON additionally as per PHY and Jedec specification.
19	RO	0x0	reserved
18	RW	0x0	dvfs0_LP5_RFF_DMI_ON RFU (Reserved for future use) This field control RFF DMI buffer on MODE for PHY write training. 1'b1: RFF DMI buffer is on when Read dbi and Read data copy MR settings are off during write training. 1'b0: Followed by user specific condition during write training.
17	RW	0x0	dvfs0_RFF_CAS_IGNORE CAS command with RFF ignore during write training 1'b1: Ignore 1'b0: No ignore
16	RW	0x0	dvfs0_WFF_RFF_TCCD_USER_MODE This field is MODE for control timing delay from WFF to RFF by User setting. This filed should used above 4266Mbps 1'b1: Timing delay from WFF to RFF will be WFF_RFF_TCCD. 1'b0: Timing delay from WFF to RFF will be WL+BL_n+tWTR by SFR of PHY scheduler.
15:8	RW	0x03	dvfs0_WFF_RFF_TCCD This field control timing delay from WFF to RFF during write training using PHY scheduler. And WFF_RFF_TCCD_USER_MODE should be 1 for apply this parameter in normal operation. Minimum value is 3tck. This filed should used above 4266Mbps Dynamic sync mode: WFF_RFF_TCCD = FIFO tWTR +1 WCK always on mode (=free running mode): WFF_RFF_TCCD = FIFO tWTR

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Bit	Attr	Reset Value	Description
7	RO	0x0	reserved
6	RW	0x0	dvfs0_wrtrn_extra_resync This field control extra DLL update during write training.
5:0	RW	0x16	dvfs0_wrtrn_trden2resp This field control timing delay from t_rddata_en to t_rdlvl_resp during write training using PHY scheduler. Please only use 0x3 pr 0x16 (default value).

DDRPHY_DVFS1_WRTRN_PARA_CON0

Address: **Operational Base** + offset (0x0E00)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:20	RW	0x12	dvfs1_RDLAT_LP5_RFF_DMI_ON RFU (Reserved for future use) This field control PHY read latency on write training when dvfs1_LP5_RFF_DMI_ON is High. Read latency on write training can be different from Normal operation because of DRAM DMI buffer is on with dvfs1_LP5_RFF_DMI_ON. So If dvfs1_LP5_RFF_DMI_ON is High, User should be set to PHY read latency with READ DBI ON additionally as per PHY and Jedec specification.
19	RO	0x0	reserved
18	RW	0x0	dvfs1_LP5_RFF_DMI_ON RFU (Reserved for future use) This field control RFF DMI buffer on MODE for PHY write training, 1'b1: RFF DMI buffer is on when Read dbi and Read data copy MR settings are off during write training. 1'b0: Followed by user specific condition during write training.
17	RW	0x0	dvfs1_RFF_CAS_IGNORE CAS command with RFF ignore during write training 1'b1: Ignore 1'b0: No ignore
16	RW	0x0	dvfs1_WFF_RFF_TCCD_USER_MODE This field is MODE for control timing delay from WFF to RFF by User setting. This filed should used above 4266Mbps. 1'b1: Timing delay from WFF to RFF will be WFF_RFF_TCCD 1'b0: Timing delay from WFF to RFF will be WL+BL_n+tWTR by SFR of PHY scheduler
15:8	RW	0x03	dvfs1_WFF_RFF_TCCD This field control timing delay from WFF to RFF during write training using PHY scheduler. And WFF_RFF_TCCD_USER_MODE should be 1 for apply this parameter in normal operation. Minimum value is 3tck. This filed should used above 4266Mbps Dynamic sync mode: WFF_RFF_TCCD = FIFO tWTR +1 WCK always on mode (=free running mode): WFF_RFF_TCCD = FIFO tWTR
7	RO	0x0	reserved
6	RW	0x0	dvfs1_wrtrn_extra_resync This field control extra DLL update during write training.
5:0	RW	0x16	dvfs1_wrtrn_trden2resp This field control timing delay from t_rddata_en to t_rdlvl_resp during write training using PHY scheduler. Please only use 0x3 pr 0x16 (default value)

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DDRPHY_DFI_LP_CON0

Address: **Operational Base** + offset (0x0E04)

Bit	Attr	Reset Value	Description
31	RW	0x0	DFI_LP_MODE_APB 1'b1: PHY clock gating is controlled by dfi_lp*. 1'b0: PHY clock gating is controlled by ctrl_phy_cg_en. Caution: If DFI_LP_MODE_APB is HiGH, PHY do not support. DDRPHY2XCLKGATE_ENABLE control (=PHY root clock gating)
30:15	RO	0x0000	reserved
14:12	RW	0x2	tlp_ctrl_resp_APB Actual tlp_ctrl_resp for Low power I/F. It controls the latnecy between dfi_lp_ctrl_req assertion and dfi_lp_ctrl_ack assertion when Low power mode is initated. 3'h0~3'h1: Don't use.
11	RO	0x0	reserved
10:8	RW	0x3	tlp_ctrl_wakeup_APB Actual tlp_ctrl_wakeup for Low power I/F. It controls the latency between dfi_lp_ctrl_req de-assertion and dfi_lp_ctrl_ack de-assertion when Low power mode is terminated. 3'h0~3'h1: Don't use.
7	RO	0x0	reserved
6:4	RW	0x2	tlp_data_resp_APB Actual tlp_data_resp for Low power I/F. It controls the latnecy between dfi_lp_data_req assertion and dfi_lp_data_ack assertion when Low power mode is initated. 3'h0~3'h1: Don't use.
3	RO	0x0	reserved
2:0	RW	0x2	tlp_data_wakeup_APB Actual tlp_data_wakeup for Low power I/F. It controls the latency between dfi_lp_data_req de-assertion and dfi_lp_data_ack de-assertion when Low power mode is terminated. 3'h0~3'h1: Don't use.

DDRPHY_LOCK_CHECK_CON

Address: **Operational Base** + offset (0x0E08)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	lock_check_diff_en Select the basic threshold to control the dfi_init_complete. 1'b0: Controlled by lock_ratio_threshold_APB 1'b1: Controlled by lock_diff_threshold_APB
23	RO	0x0	reserved
22:12	RW	0x007	lock_diff_threshold When lock_check_diff_en_APB = 1'b1, Set the threshold value of the difference of lock value following below equation. lock_diff_threshold_APB ={ (standard_value_difference * period (ps) * 4 * (get_avg_lock_extend_APB+1) * 2^ (lock_value_avg_n_sel_APB+3) } / 1000000 'standard_value_difference' have to be based on 1us. 'period' have to be based on ps. dfi_ init_complete will be controlled by equation. lock_value_avg_delta ('N-th lock_value_avg' - '1-st lock_value_avg') > lock_diff_threshold_APB
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:6	RW	0x04	lock_ratio_threshold When lock_check_diff_en_APB = 1'b0, Select the threshold ratio of the lock value. 5'd0: 50% of start point lock value of average window 5:d1: 37.5% of start point lock value of average window 5'd2: 25% of start point lock value of average window 5'd3: 18.75% of start point lock value of average window 5'd4: 12.5% of start point lock value of average window 5:d5: 9.375% of start point lock value of average window 5'd6: 6.25% of start point lock value of average window 5'd7: 3.125% of start point lock value of average window 5'd8: 1.5625% of start point lock value of average window 5'd9: 0.78125% of start point lock value of average window dfi_ init_complete will be controlled by equation. lock_value_avg_delta ('N-th lock_value_avg' - '1-st lock_value_avg') > 'N-th lock_value_avg' * ratio (%)
5:4	RW	0x0	get_avg_lock_extend Extend average window 2'b00: Average window * 1 2'b01: Average window * 2 2'b10: Average window * 3 2'b11: Average window * 4
3	RO	0x0	reserved
2:1	RW	0x2	lock_check_avg_n_sel Select size of average window 2'b00: 8*4 DFI cycles * period 2'b01: 16*4 DFI cycles * period 2'b10: 32*4 DFI cycles * period 2'b11: 64*4 DFI cycles * period
0	RW	0x0	lock_check_avg_en Enable lock check with average lock value This bit should be set after set of 'lock_average_en'.

DDRPHY_DFI_RDDATA0

Address: **Operational Base** + offset (0x0E10)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata0_ds1 dfi_rddata_burst0 data slice 1 when scheduler_sw_mode is on.
15:0	RO	0x0000	dfi_rddata0_ds0 dfi_rddata_burst0 data slice 0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA1

Address: **Operational Base** + offset (0x0E14)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata1_ds1 dfi_rddata_burst1 data slice 1 when scheduler_sw_mode is on.
15:0	RO	0x0000	dfi_rddata1_ds0 dfi_rddata_burst1 data slice 0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA2

Address: **Operational Base** + offset (0x0E18)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata2_ds1 dfi_rddata_burst2 data slice 1 when scheduler_sw_mode is on.

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	dfi_rddata2_ds0 dfi_rddata_burst2 data slice 0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA3

Address: **Operational Base** + offset (0x0E1C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata3_ds1 dfi_rddata_burst3 data slice 1 when scheduler_sw_mode is on.
15:0	RO	0x0000	dfi_rddata3_ds0 dfi_rddata_burst3 data slice 0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA4

Address: **Operational Base** + offset (0x0E20)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata4_ds1 dfi_rddata_burst4 data slice 1 when scheduler_sw_mode is on.
15:0	RO	0x0000	dfi_rddata4_ds0 dfi_rddata_burst4 data slice 0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA5

Address: **Operational Base** + offset (0x0E24)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata5_ds1 dfi_rddata_burst5 data slice 1 when scheduler_sw_mode is on.
15:0	RO	0x0000	dfi_rddata5_ds0 dfi_rddata_burst5 data slice 0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA6

Address: **Operational Base** + offset (0x0E28)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata6_ds1 dfi_rddata_burst6 data slice 1 when scheduler_sw_mode is on.
15:0	RO	0x0000	dfi_rddata6_ds0 dfi_rddata_burst6 data slice 0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA7

Address: **Operational Base** + offset (0x0E2C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata7_ds1 dfi_rddata_burst7 data slice 1 when scheduler_sw_mode is on.
15:0	RO	0x0000	dfi_rddata7_ds0 dfi_rddata_burst7 data slice 0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA_DM

Address: **Operational Base** + offset (0x0E30)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	dfi_rddata_dm7_ds1 dfi_rddata_burst7 data slice 1 when scheduler_sw_mode is on.
29:28	RO	0x0	dfi_rddata_dm7_ds0 dfi_rddata_burst7 data slice 0 when scheduler_sw_mode is on.
27:26	RO	0x0	dfi_rddata_dm6_ds1 dfi_rddata_burst6 data slice 1 when scheduler_sw_mode is on.
25:24	RO	0x0	dfi_rddata_dm6_ds0 dfi_rddata_burst6 data slice 0 when scheduler_sw_mode is on.

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Bit	Attr	Reset Value	Description
23:22	RO	0x0	dfi_rddata_dm5_ds1 dfi_rddata_burst5 data slice 1 when scheduler_sw_mode is on.
21:20	RO	0x0	dfi_rddata_dm5_ds0 dfi_rddata_burst5 data slice 0 when scheduler_sw_mode is on.
19:18	RO	0x0	dfi_rddata_dm4_ds1 dfi_rddata_burst4 data slice 1 when scheduler_sw_mode is on.
17:16	RO	0x0	dfi_rddata_dm4_ds0 dfi_rddata_burst4 data slice 0 when scheduler_sw_mode is on.
15:14	RO	0x0	dfi_rddata_dm3_ds1 dfi_rddata_burst3 data slice 1 when scheduler_sw_mode is on.
13:12	RO	0x0	dfi_rddata_dm3_ds0 dfi_rddata_burst3 data slice 0 when scheduler_sw_mode is on.
11:10	RO	0x0	dfi_rddata_dm2_ds1 dfi_rddata_burst2 data slice 1 when scheduler_sw_mode is on.
9:8	RO	0x0	dfi_rddata_dm2_ds0 dfi_rddata_burst2 data slice 0 when scheduler_sw_mode is on.
7:6	RO	0x0	dfi_rddata_dm1_ds1 dfi_rddata_burst1 data slice 1 when scheduler_sw_mode is on.
5:4	RO	0x0	dfi_rddata_dm1_ds0 dfi_rddata_burst1 data slice 0 when scheduler_sw_mode is on.
3:2	RO	0x0	dfi_rddata_dm0_ds1 dfi_rddata_burst0 data slice 1 when scheduler_sw_mode is on.
1:0	RO	0x0	dfi_rddata_dm0_ds0 dfi_rddata_burst0 data slice 0 when scheduler_sw_mode is on.

DDRPHY_LP5_MR_OP2

Address: **Operational Base** + offset (0x0E34)

Bit	Attr	Reset Value	Description
31:24	RW	0xc6	LP5_MR3_PHY RFU (Reserved for future use) LP5 DRAM MR3 setting during write training [31:24] = OP[7:0]
23:16	RW	0xbb	LP5_MR2_PHY RFU (Reserved for future use) LP5 DRAM MR2 setting during write training [23:16] = OP[7:0]
15:8	RW	0xc6	LP5_MR3_DRAM RFU (Reserved for future use) LP5 DRAM MR3 setting during normal operation [15:8] = OP[7:0]
7:0	RW	0xbb	LP5_MR2_DRAM RFU (Reserved for future use) LP5 DRAM MR2 setting during normal operation [7:0] = OP[7:0]

DDRPHY_DVFS0_LP5_MR_OP2

Address: **Operational Base** + offset (0x0E38)

Bit	Attr	Reset Value	Description
31:24	RW	0xc6	dvfs0_LP5_MR3_PHY RFU (Reserved for future use) LP5 DRAM MR3 setting during write training [31:24] = OP[7:0]

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Bit	Attr	Reset Value	Description
23:16	RW	0xbb	dvfs0_LP5_MR2_PHY RFU (Reserved for future use) LP5 DRAM MR2 setting during write training [23:16] = OP[7:0]
15:8	RW	0xc6	dvfs0_LP5_MR3_DRAM RFU (Reserved for future use) LP5 DRAM MR3 setting during normal operation [15:8] = OP[7:0]
7:0	RW	0xbb	dvfs0_LP5_MR2_DRAM RFU (Reserved for future use) LP5 DRAM MR2 setting during normal operation [7:0] = OP[7:0]

DDRPHY_DVFS1_LP5_MR_OP2

Address: **Operational Base** + offset (0x0E3C)

Bit	Attr	Reset Value	Description
31:24	RW	0xc6	dvfs1_LP5_MR3_PHY RFU (Reserved for future use) LP5 DRAM MR3 setting during write training [31:24] = OP[7:0]
23:16	RW	0xbb	dvfs1_LP5_MR2_PHY RFU (Reserved for future use) LP5 DRAM MR2 setting during write training [23:16] = OP[7:0]
15:8	RW	0xc6	dvfs1_LP5_MR3_DRAM RFU (Reserved for future use) LP5 DRAM MR3 setting during normal operation [15:8] = OP[7:0]
7:0	RW	0xbb	dvfs1_LP5_MR2_DRAM RFU (Reserved for future use) LP5 DRAM MR2 setting during normal operation [7:0] = OP[7:0]

DDRPHY_PHYUPD_PARA_CON0

Address: **Operational Base** + offset (0x0E40)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x1	ctrl_upd_req_timeout_en For debug purpose. If ctrl_upd_req_timeout_en = 1 and dfi_phyupd_ack is not asserted to corresponding dfi_phyupd_req assertion, dfi_phyupd_req will be de-asserted after tphyupd_resp is expired.
11:9	RO	0x0	reserved
8:0	RW	0x03f	ctrl_tphyupd_resp ctrl_tphyupd_resp parameter in term of DFI clock cycle Please should use default value during normal operation. But If write leveing need to enable during LPDDR5 WCK free running mode, Please control this register under 300ns as per memory controller specification.

DDRPHY_DVFS0_PHYUPD_PARA_CON0

Address: **Operational Base** + offset (0x0E44)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x1	dvfs0_upd_req_timeout_en For debug purpose. If dvfs0_upd_req_timeout_en = 1 and dfi_phyupd_ack is not asserted to corresponding dfi_phyupd_req assertion, dfi_phyupd_req will be de-asserted after tphyupd_resp is expired.
11:9	RO	0x0	reserved
8:0	RW	0x03f	dvfs0_tphyupd_resp dvfs0_tphyupd_resp parameter in term of DFI clock cycle. Please should use default value during normal operation. But If write leveing need to enable during LPDDR5 WCK free running mode on DVFS0, Please control this reigister under 300ns as per memory controller specification.

DDRPHY_DVFS1_PHYUPD_PARA_CON0

Address: **Operational Base** + offset (0x0E48)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x1	dvfs1_upd_req_timeout_en For debug purpose. If dvfs1_upd_req_timeout_en = 1 and dfi_phyupd_ack is not asserted to corresponding dfi_phyupd_req assertion, dfi_phyupd_req will be de-asserted after tphyupd_resp is expired.
11:9	RO	0x0	reserved
8:0	RW	0x03f	dvfs1_tphyupd_resp dvfs1_tphyupd_resp parameter in term of DFI clock cycle. Please should use default value during normal operation. But If write leveing need to enable during LPDDR5 WCK free running mode on DVFS1, Please control this register under 300ns as per memory controller specification.

7.4.7 Internal Address Mapping For DFI Scramble

Please refer to DDR_GRF chapter for DFI Scramble registers description.

7.4.8 Internal Address Mapping For DDRMON

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
DDRMON0	0x2A000000
DDRMON1	0x2A010000

7.4.9 Registers Summary For DDRMON

Name	Offset	Size	Reset Value	Description
DDRMON_IP_VERSION	0x0000	W	0x00000040	DDR Monitor IP Version
DDRMON_CTRL0	0x0004	W	0x00000008	DDR Monitor Control 0 Register
DDRMON_CTRL1	0x0008	W	0x00000000	DDR Monitor Control 1 Register
DDRMON_INT_STATUS0	0x000C	W	0x00000000	Interrupt Status 0
DDRMON_INT_STATUS1	0x0010	W	0x00000000	Interrupt Status 1
DDRMON_DDRC_IDLE_CNT_NUM	0x0014	W	0x00000000	DDRC IDLE Time
DDRMON_TIMER_COUNT	0x0018	W	0x00000000	The DFI Timer Threshold

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Name	Offset	Size	Reset Value	Description
DDRMON_FLOOR_NUMBER	0x001C	W	0x00000000	The Low Threshold In The Comparison of DDR Access
DDRMON_TOP_NUMBER	0x0020	W	0x00000000	The High Threshold In The Comparison of DDR Access
DDRMON_DFI_ACT_NUM	0x0024	W	0x00000000	DFI Active Command Number
DDRMON_DFI_ACT_WR_NUM	0x0028	W	0x00000000	DFI Write Command Number
DDRMON_DFI_ACT_RD_NUM	0x002C	W	0x00000000	DFI Read Command Number
DDRMON_COUNT_NUM	0x0030	W	0x00000000	Timer Count Number
DDRMON_DFI_ACCESS_NUM	0x0034	W	0x00000000	DFI Read And Write Command Number
DDRMON_TOP_LP_NUMBER	0x0038	W	0x00000000	The High Threshold In The Comparison Of DDR Cke Low
DDRMON_FLOOR_LP_NUMBER	0x003C	W	0x00000000	The Low Threshold In The Comparison Of DDR Cke Low
DDRMON_DFI_SREX_NUM	0x0040	W	0x00000000	Number Of DFI Self-refresh Cycles
DDRMON_DFI_PDEX_NUM	0x0044	W	0x00000000	Number Of DFI Power Down Cycles
DDRMON_DFI_CLKSTOP_NUM	0x0048	W	0x00000000	Number Of DFI Clkstop Cycles
DDRMON_DFI_SRPDEX_NUM	0x004C	W	0x00000000	Number Of DFI SRPD Cycles
DDRMON_DFI_DSMEX_NUM	0x0050	W	0x00000000	Number Of DFI DSM Cycles
DDRMON_DFI_LP_NUM	0x0054	W	0x00000000	Total Number DFI Low Power Cycles
DDRMON_DFI_PHY_LP_CTRL_NUM	0x0058	W	0x00000000	DFI PHY Low Power
DDRMON_DFI_PHY_LP_DATA_NUM	0x005C	W	0x00000000	DFI PHY Low Power
DDRMON_INT_MASK0	0x0060	W	0x0000FFFF	Interrupt Mask Control
DDRMON_INT_MASK1	0x0064	W	0x00000001	Interrupt Mask Control
DDRMON_INT_MASK2	0x0068	W	0x0000001F	Interrupt Mask Control
DDRMON_INT_MASK3	0x006C	W	0x0000001F	Interrupt Mask Control
DDRMON_CS_CONTROL	0x0070	W	0x00000002	Number of DDR Rank
DDRMON_PER_BANK_ACT_NUM	0x0100	W	0x00000000	Per-bank Active Number
DDRMON_PER_BANK_RD_NUM	0x0104	W	0x00000000	Per-bank Read Number
DDRMON_PER_BANK_WR_NUM	0x0108	W	0x00000000	Per-bank Write Number
DDRMON_PER_BANK_RD_WR_PER_ACT_MAX_NUM	0x010C	W	0x00000000	Per-bank Read-Write Per-Active Max Number

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Name	Offset	Size	Reset Value	Description
DDRMON_PER_BANK_SERIES_RD_BURST_MAX_NUM	0x0110	W	0x00000000	Per-bank Series Read Burst Max Number
DDRMON_PER_BANK_SERIES_RD_BURST_TIMES_NUM	0x0114	W	0x00000000	Per-bank Series Read Burst Times Number
DDRMON_PER_BANK_SERIES_WR_BURST_MAX_NUM	0x0118	W	0x00000000	Per-bank Series Write Burst Max Number
DDRMON_PER_BANK_SERIES_WR_BURST_TIMES_NUM	0x011C	W	0x00000000	Per-bank Series Write Burst Times Number
DDRMON_PER_BANK_RD2RD_PAGE_HIT_NUM	0x0120	W	0x00000000	Per-bank Read to Read Page-hit Number
DDRMON_PER_BANK_WR2WR_PAGE_HIT_NUM	0x0124	W	0x00000000	Per-bank Write to Write Page Hit Number
DDRMON_PER_BANK_RD2WR_PAGE_HIT_NUM	0x0128	W	0x00000000	Per-bank Read to Write Page Hit Number
DDRMON_PER_BANK_WR2RD_PAGE_HIT_NUM	0x012C	W	0x00000000	Per-bank Write To Write Page Hit Number
DDRMON_PER_BANK_RD2RD_PAGE_MISS_NUM	0x0130	W	0x00000000	Per-bank Read To Read Page Miss Number
DDRMON_PER_BANK_WR2WR_PAGE_MISS_NUM	0x0134	W	0x00000000	Per-bank Write To Write Page Miss Number
DDRMON_PER_BANK_RD2WR_PAGE_MISS_NUM	0x0138	W	0x00000000	Per-bank Read To Write Page Miss Number
DDRMON_PER_BANK_WR2RD_PAGE_MISS_NUM	0x013C	W	0x00000000	Per-bank Write To Read Page Miss Number
DDRMON_ALL_BANK_ACT_NUM	0x0140	W	0x00000000	All-bank Active Command Number
DDRMON_ALL_BANK_WR_NUM	0x0144	W	0x00000000	All-bank Write Command Number
DDRMON_ALL_BANK_RD_NUM	0x0148	W	0x00000000	All-bank Read Command Number
DDRMON_ALL_BANK_ACT_ACT_NUM	0x014C	W	0x00000000	All-bank Active To Active Number
DDRMON_ALL_BANK_ACT_PRE_NUM	0x0150	W	0x00000000	All-bank Active Precharge Number
DDRMON_ALL_BANK_ACT_RDWR_SAME_NUM	0x0154	W	0x00000000	All-bank Active Read-Write Same Number
DDRMON_ALL_BANK_PRE_ACT_NUM	0x0158	W	0x00000000	All-bank Precharge To Active Number
DDRMON_ALL_BANK_RDWR_PRE_SAME_NUM	0x015C	W	0x00000000	All-bank Read-Write Precharge Same Number

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Name	Offset	Size	Reset Value	Description
DDRMON_ALL_BANK_RD2WR_NUM	0x0160	W	0x00000000	All-bank Read To Write Number
DDRMON_ALL_BANK_WR2RD_NUM	0x0164	W	0x00000000	All-bank Write To Read Number
DDRMON_ALL_BANK_SERIES_RD_TOTAL_CNT_NUM	0x0168	W	0x00000000	All-bank Series Read Total Count Number
DDRMON_ALL_BANK_SERIES_WR_TOTAL_CNT_NUM	0x016C	W	0x00000000	All-bank Series Write Total Count Number
DDRMON_ALL_BANK_SERIES_RD_BURST_MAX_NUM	0x0170	W	0x00000000	All-bank Series Read Burst Max Number
DDRMON_ALL_BANK_SERIES_RD_BURST_TIMES_NUM	0x0174	W	0x00000000	All-bank Series Read Burst Times Number
DDRMON_ALL_BANK_SERIES_WR_BURST_MAX_NUM	0x0178	W	0x00000000	All-bank Series Write Burst Max Number
DDRMON_ALL_BANK_SERIES_WR_BURST_TIMES_NUM	0x017C	W	0x00000000	All-bank Series Write Burst Times Number
DDRMON_ALL_BANK_MWR_CNT_NUM	0x0180	W	0x00000000	All-bank Mask Write Command Count Number
DDRMON_ALL_BANK_TCCDMW_CNT_NUM	0x0184	W	0x00000000	All-bank TCCDMW Count Number
DDRMON_ALL_BANK_TCCD_L_CNT_NUM	0x0188	W	0x00000000	All-bank TCCD_L Count Number
DDRMON_ALL_BANK_SYNC_CNT_NUM	0x018C	W	0x00000000	All-bank Sync Count Number
DDRMON_ALL_BANK_CAS_B3_RD_NUM	0x0190	W	0x00000000	All-bank CAS_B3 Read Number
DDRMON_IF_CTRL	0x0200	W	0x00000000	DDR Interface Control Register
DDRMON_MSTID	0x0204	W	0x00000000	Master And AXI ID Of DDR Command
DDRMON_IDMSK	0x0208	W	0x00000000	Master And AXI ID MASK Of DDR Command
DDRMON_WR_START_ADDR_31_0	0x020C	W	0x00000000	Low 32 Bits of Write Start Address
DDRMON_WR_START_ADDR_39_32	0x0210	W	0x00000000	High 2 Bits of Write Start Address
DDRMON_WR_END_ADDR_31_0	0x0214	W	0x00000000	Low 32 Bits of Write End Address

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Name	Offset	Size	Reset Value	Description
DDRMON_WR_END_ADDR_39_32	0x0218	W	0x00000000	High 2 Bits of Write End Address
DDRMON_RD_START_ADDR_31_0	0x021C	W	0x00000000	Low 32 Bits of Read Start Address
DDRMON_RD_START_ADDR_39_32	0x0220	W	0x00000000	High 2 Bits of Read Start Address
DDRMON_RD_END_ADDR_31_0	0x0224	W	0x00000000	Low 32 Bits of Read End Address
DDRMON_RD_END_ADDR_39_32	0x0228	W	0x00000000	High 2 Bits of Read End Address
DDRMON_PORT0_FIFO0_ADDR_31_0	0x0240	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO0
DDRMON_PORT0_FIFO0_ADDR_63_32	0x0244	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO0
DDRMON_PORT0_FIFO1_ADDR_31_0	0x0248	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO1
DDRMON_PORT0_FIFO1_ADDR_63_32	0x024C	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO1
DDRMON_PORT0_FIFO2_ADDR_31_0	0x0250	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO2
DDRMON_PORT0_FIFO2_ADDR_63_32	0x0254	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO2
DDRMON_PORT0_FIFO3_ADDR_31_0	0x0258	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO3
DDRMON_PORT0_FIFO3_ADDR_63_32	0x025C	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO3
DDRMON_PORT1_FIFO0_ADDR_31_0	0x0260	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO0
DDRMON_PORT1_FIFO0_ADDR_63_32	0x0264	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO0
DDRMON_PORT1_FIFO1_ADDR_31_0	0x0268	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO1
DDRMON_PORT1_FIFO1_ADDR_63_32	0x026C	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO1
DDRMON_PORT1_FIFO2_ADDR_31_0	0x0270	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO2
DDRMON_PORT1_FIFO2_ADDR_63_32	0x0274	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO2
DDRMON_PORT1_FIFO3_ADDR_31_0	0x0278	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO3
DDRMON_PORT1_FIFO3_ADDR_63_32	0x027C	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO3
DDRMON_PORT2_FIFO0_ADDR_31_0	0x0280	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO0

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Name	Offset	Size	Reset Value	Description
DDRMON_PORT2_FIFO0_ADDR_63_32	0x0284	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO0
DDRMON_PORT2_FIFO1_ADDR_31_0	0x0288	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO1
DDRMON_PORT2_FIFO1_ADDR_63_32	0x028C	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO1
DDRMON_PORT2_FIFO2_ADDR_31_0	0x0290	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO2
DDRMON_PORT2_FIFO2_ADDR_63_32	0x0294	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO2
DDRMON_PORT2_FIFO3_ADDR_31_0	0x0298	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO3
DDRMON_PORT2_FIFO3_ADDR_63_32	0x029C	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO3
DDRMON_PORT3_FIFO0_ADDR_31_0	0x02A0	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO0
DDRMON_PORT3_FIFO0_ADDR_63_32	0x02A4	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO0
DDRMON_PORT3_FIFO1_ADDR_31_0	0x02A8	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO1
DDRMON_PORT3_FIFO1_ADDR_63_32	0x02AC	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO1
DDRMON_PORT3_FIFO2_ADDR_31_0	0x02B0	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO2
DDRMON_PORT3_FIFO2_ADDR_63_32	0x02B4	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO2
DDRMON_PORT3_FIFO3_ADDR_31_0	0x02B8	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO3
DDRMON_PORT3_FIFO3_ADDR_63_32	0x02BC	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO3
DDRMON_PORT4_FIFO0_ADDR_31_0	0x02C0	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO0
DDRMON_PORT4_FIFO0_ADDR_63_32	0x02C4	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO0
DDRMON_PORT4_FIFO1_ADDR_31_0	0x02C8	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO1
DDRMON_PORT4_FIFO1_ADDR_63_32	0x02CC	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO1
DDRMON_PORT4_FIFO2_ADDR_31_0	0x02D0	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO2
DDRMON_PORT4_FIFO2_ADDR_63_32	0x02D4	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO2
DDRMON_PORT4_FIFO3_ADDR_31_0	0x02D8	W	0x00000000	Low 32 Bits of DDR Controller Interface Address FIFO3

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Name	Offset	Size	Reset Value	Description
DDRMON_PORT4_FIFO3_ADDR_63_32	0x02DC	W	0x00000000	High 32 Bits of DDR Controller Interface Address FIFO3
DDRMON_LPR_CREDIT_TOTAL_LOW32_NUM	0x0400	W	0x00000000	Low 32 Bits LPR Credits Register
DDRMON_HPR_CREDIT_TOTAL_LOW32_NUM	0x0404	W	0x00000000	Low 32 Bits HPR Credits Register
DDRMON_WR_CREDIT_TOTAL_LOW32_NUM	0x0408	W	0x00000000	Low 32 Bits WR Credits Register
DDRMON_LPR_CREDIT_TOTAL_HIGH8_NUM	0x0410	W	0x00000000	High 8 Bits LPR Credits Register
DDRMON_HPR_CREDIT_TOTAL_HIGH8_NUM	0x0414	W	0x00000000	High 8 Bits HPR Credits Register
DDRMON_WR_CREDIT_TOTAL_HIGH8_NUM	0x0418	W	0x00000000	High 8 Bits WR Credits Register
DDRMON_LPR_CREDIT_CNT_NUM_0_15	0x0420	W	0x00000000	LPR Credits Count 0~15 Register
DDRMON_LPR_CREDIT_CNT_NUM_16_31	0x0424	W	0x00000000	LPR Credits Count 16~31 Register
DDRMON_LPR_CREDIT_CNT_NUM_32_47	0x0428	W	0x00000000	LPR Credits Count 32~47 Register
DDRMON_LPR_CREDIT_CNT_NUM_48_63	0x042C	W	0x00000000	LPR Credits Count 48~63 Register
DDRMON_LPR_CREDIT_CNT_NUM_FULL	0x0430	W	0x00000000	LPR Credits Count Full Register
DDRMON_HPR_CREDIT_CNT_NUM_0_15	0x0440	W	0x00000000	HPR Credits Count 0~15 Register
DDRMON_HPR_CREDIT_CNT_NUM_16_31	0x0444	W	0x00000000	HPR Credits Count 16~31 Register
DDRMON_HPR_CREDIT_CNT_NUM_32_47	0x0448	W	0x00000000	HPR Credits Count 32~47 Register
DDRMON_HPR_CREDIT_CNT_NUM_48_63	0x044C	W	0x00000000	HPR Credits Count 48~63 Register
DDRMON_HPR_CREDIT_CNT_NUM_FULL	0x0450	W	0x00000000	HPR Credits Count Full Register
DDRMON_WR_CREDIT_CNT_NUM_0_15	0x0460	W	0x00000000	WR Credits Count 0~15 Register
DDRMON_WR_CREDIT_CNT_NUM_16_31	0x0464	W	0x00000000	WR Credits Count 16~31 Register
DDRMON_WR_CREDIT_CNT_NUM_32_47	0x0468	W	0x00000000	WR Credits Count 32~47 Register
DDRMON_WR_CREDIT_CNT_NUM_48_63	0x046C	W	0x00000000	WR Credits Count 48~63 Register
DDRMON_WR_CREDIT_CNT_NUM_FULL	0x0470	W	0x00000000	WR Credits Count Full Register

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*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.10 Detail Registers Description For DDRMON

DDRMON_IP_VERSION

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x40	ip_version DDR monitor IP version

DDRMON_CTRL0

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15	RW	0x0	ddr23_en ddr2 or ddr3 mode 1'b1: Enable 1'b0: Disable
14:11	RW	0x0	hot_bank Define which bank is currently monitored for per-bank statistics. For ddr3/lpddr3/lpddr4, bit[13:11] is used to support 8 bank. For ddr4, bit[14:13] is used for BG select, bit[12:11] is used for bank select.
10:9	RO	0x0	reserved
8:7	RW	0x0	hot_rank Define which rank is currently monitored for per-bank statistics. 2'b01: Rank 0 2'b10: Rank 1 Other value is not valid.
6	RW	0x0	external_trigger_en This register is used to enable multiple ddr monitors at the same time. If set to 1'b0, ddr monitor is enabled by software. If set to 1'b1, after enable all ddr monitors, an external trigger enable signal set to 1'b1 will start all ddr monitors. 1'b0: Disable 1'b1: Enable
5	RW	0x0	ddr4_en 1'b1: Enable 1'b0: Disable

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Bit	Attr	Reset Value	Description
4	RW	0x0	lpddr4_en 1'b1: Enable 1'b0: Disable
3	RW	0x1	hardware_en 1'b1: Enable 1'b0: Disable
2	RW	0x0	lpddr23_en 1'b1: Enable 1'b0: Disable
1	RW	0x0	software_en 1'b1: Enable 1'b0: Disable
0	RW	0x0	timer_cnt_en 1'b1: Enable 1'b0: Disable

DDRMON_CTRL1

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:1	RW	0x0	lpddr5_bank_mode 2'b00: BG mode 2'b01: 16 bank mode 2'b10: 8 bank mode
0	RW	0x0	lpddr5_en 1'b1: Enable 1'b0: Disable

DDRMON_INT_STATUS0

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	W1C	0x0	over_int_srpdex This is the interrupt status of DDR SRPD over than high threshold. Only for LPDDR4/LPDDR5
15	W1C	0x0	bellow_int_srpdex This is the interrupt status of DDR SRPD less than low threshold. Only for LPDDR4/LPDDR5
14	W1C	0x0	over_int_dsmex This is the interrupt status of DDR deep sleep over than high threshold. Only for LPDDR5
13	W1C	0x0	bellow_int_dsmex This is the interrupt status of DDR deep sleep less than low threshold. Only for LPDDR5

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Bit	Attr	Reset Value	Description
12	W1C	0x0	over_int_phy_lp_ctrl This is the interrupt status of DDR low power ctrl interface over than high threshold.
11	W1C	0x0	bellow_int_phy_lp_ctrl This is the interrupt status of DDR low power ctrl interface less than low threshold.
10	W1C	0x0	over_int_phy_lp_data This is the interrupt status of DDR low power data interface over than high threshold.
9	W1C	0x0	below_int_phy_lp_data This is the interrupt status of DDR low power data interface less than low threshold.
8	W1C	0x0	over_int_clkstop This is the interrupt status of DDR clk stop number over than high threshold. Only valid for lpddr4/lpddr5.
7	W1C	0x0	below_int_clkstop This is the interrupt status of DDR clk stop number less than low threshold. Only valid for lpddr4/lpddr5.
6	W1C	0x0	over_int_pdex This is the interrupt status of DDR power down number over than high threshold.
5	W1C	0x0	below_int_pdex This is the interrupt status of DDR power down number less than low threshold.
4	W1C	0x0	compare_statistics This is the interrupt status to statistics the number of activate, write or read command and so on.
3	W1C	0x0	over_int_srex This is the interrupt status of DDR self refresh number over than high threshold.
2	W1C	0x0	below_int_srex This is the interrupt status of DDR self refresh number less than low threshold.
1	W1C	0x0	over_int This is the interrupt status of DDR read and write burst number over than high threshold.
0	W1C	0x0	below_int This is the interrupt status of DDR read and write burst number less than low threshold.

DDRMON_INT_STATUS1

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
20	W1C	0x0	port4_rd_addr_hit This is the DDRCTL's AXI port4 interrupt status read address hit the setting range.
19	W1C	0x0	port3_rd_addr_hit This is the DDRCTL's AXI port3 interrupt status read address hit the setting range.
18	W1C	0x0	port2_rd_addr_hit This is the DDRCTL's AXI port2 interrupt status read address hit the setting range.
17	W1C	0x0	port1_rd_addr_hit This is the DDRCTL's AXI port1 interrupt status read address hit the setting range.
16	W1C	0x0	port0_rd_addr_hit This is the DDRCTL's AXI port0 interrupt status read address hit the setting range.
15:5	RO	0x000	reserved
4	W1C	0x0	port4_wr_addr_hit This is the DDRCTL's AXI port4 interrupt status write address hit the setting range.
3	W1C	0x0	port3_wr_addr_hit This is the DDRCTL's AXI port3 interrupt status write address hit the setting range.
2	W1C	0x0	port2_wr_addr_hit This is the DDRCTL's AXI port2 interrupt status write address hit the setting range.
1	W1C	0x0	port1_wr_addr_hit This is the DDRCTL's AXI port1 interrupt status write address hit the setting range.
0	W1C	0x0	port0_wr_addr_hit This is the DDRCTL's AXI port0 interrupt status write address hit the setting range.

DDRMON_DDRC_IDLE_CNT_NUM

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ddrc_idle_cnt_number The DDRC idle time, which is calculated by DFI clock.

DDRMON_TIMER_COUNT

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	timer_count The timer counter threshold, the statistics of DDR access only be done when timer counter is less then this threshold in hardware mode, in OSC clock cycle.

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DDRMON_FLOOR_NUMBER

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	floor_number The low threshold in the comparison of DDR access.

DDRMON_TOP_NUMBER

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	top_number The high threshold in the comparison of DDR access.

DDRMON_DFI_ACT_NUM

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_act_num DFI active command number in the statistics range.

DDRMON_DFI_ACT_WR_NUM

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_act_wr_num DFI write command number in the statistics range.

DDRMON_DFI_ACT_RD_NUM

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_act_rd_num DFI read command number in the statistics range.

DDRMON_COUNT_NUM

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_count_num The DFI counter number in the statistics range, in DFI clock cycle.

DDRMON_DFI_ACCESS_NUM

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_access_num DFI read and write command number in the statistics range.

DDRMON_TOP_LP_NUMBER

Address: **Operational Base** + offset (0x0038)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	top_lp_number The high threshold in the comparison of DDR self-refresh, power down or clkstop.

DDRMON_FLOOR_LP_NUMBER

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	floor_lp_number The low threshold in the comparison of DDR self-refresh, power down or clkstop.

DDRMON_DFI_SREX_NUM

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_srex_num DFI self-refresh number during cke low.

DDRMON_DFI_PDEX_NUM

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_pdex_num DFI power down number during cke low.

DDRMON_DFI_CLKSTOP_NUM

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_clkstop_num DFI clkstop number during cke low. Only valid for lpddr2/3/4.

DDRMON_DFI_SRPDEX_NUM

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_srpdex_num DFI SRPD number during cke low. Only valid for lpddr4/5.

DDRMON_DFI_DSMEX_NUM

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_dsmex_num DFI Deep Sleep Mode number during cke low. Only valid for lpddr5.

DDRMON_DFI_LP_NUM

Address: **Operational Base** + offset (0x0054)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_lp_num The sum of DFI self-refresh, power down, clock stop, self-refresh-pd and dsm cycles.

DDRMON_DFI_PHY_LP_CTRL_NUM

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_phy_lp_ctrl_num Phy low power count number during the time both dfi_lp_ctrl_req and dfi_lp_ctrl_ack assert.

DDRMON_DFI_PHY_LP_DATA_NUM

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_phy_lp_data_num Phy low power count number during the time both dfi_lp_data_req and dfi_lp_data_ack assert.

DDRMON_INT_MASK0

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15	RW	0x1	bellow_int_srpdex Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
14	RW	0x1	over_int_dsmex Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
13	RW	0x1	bellow_int_dsmex Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
12	RW	0x1	over_int_phy_lp_ctrl Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
11	RW	0x1	bellow_int_phy_lp_ctrl Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.

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Bit	Attr	Reset Value	Description
10	RW	0x1	over_int_phy_lp_data_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
9	RW	0x1	below_int_phy_lp_data_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
8	RW	0x1	over_int_clkstop_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
7	RW	0x1	below_int_clkstop_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
6	RO	0x1	over_int_pdex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
5	RO	0x1	below_int_pdex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
4	RW	0x1	compare_statistics_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
3	RW	0x1	over_int_srex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
2	RW	0x1	below_int_srex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
1	RW	0x1	over_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
0	RW	0x1	below_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.

DDRMON_INT_MASK1

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17:16	WO	0x0	write_enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15:1	RO	0x0000	reserved
0	RW	0x1	over_int_srpdex Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.

DDRMON_INT_MASK2

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	WO	0x00	write_enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15:5	RO	0x000	reserved
4	RW	0x1	port4_wr_addr_hit_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
3	RW	0x1	port3_wr_addr_hit_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
2	RW	0x1	port2_wr_addr_hit_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
1	RW	0x1	port1_wr_addr_hit_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
0	RW	0x1	port0_wr_addr_hit_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.

DDRMON_INT_MASK3

Address: **Operational Base** + offset (0x006C)

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Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	WO	0x00	write_enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15:5	RO	0x000	reserved
4	RW	0x1	port4_rd_addr_hit_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
3	RW	0x1	port3_rd_addr_hit_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
2	RW	0x1	port2_rd_addr_hit_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
1	RW	0x1	port1_rd_addr_hit_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
0	RW	0x1	port0_rd_addr_hit_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.

DDRMON_CS_CONTROL

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	WO	0x0	write_enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software.
15:2	RO	0x0000	reserved
1:0	RW	0x2	rank_cs_num 2'b01: When there is 1-rank. 2'b10: When there is 2-rank. Other value is for 4-rank. Default 2'h2.

DDRMON_PER_BANK_ACT_NUM

Address: **Operational Base** + offset (0x0100)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_act_number Active command number for per bank statistics

DDRMON_PER_BANK_RD_NUM

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_rd_number Read command number for per bank statistics

DDRMON_PER_BANK_WR_NUM

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_wr_number Write command number for per bank statistics

DDRMON_PER_BANK_RD_WR_PER_ACT_MAX_NUM

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_rd_wr_per_act_max_number Per_bank_rd_wr_per_act_max_number number for per bank statistics. Count the max read or write command in every ACT to PRE period, for a designated bank.

DDRMON_PER_BANK_SERIES_RD_BURST_MAX_NUM

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_series_rd_burst_max_number per_bank_series_rd_burst_max_number number for per bank statistics. Count the max series read command in every ACT to PRE period, for a designated bank.

DDRMON_PER_BANK_SERIES_RD_BURST_TIMES_NUM

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_series_rd_burst_times_number per_bank_series_rd_burst_times_number number for per bank statistics. Count the total series read command in every ACT to PRE period, for a designated bank.

DDRMON_PER_BANK_SERIES_WR_BURST_MAX_NUM

Address: **Operational Base** + offset (0x0118)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_series_wr_burst_max_number per_bank_series_wr_burst_max_number number for per bank statistics. Count the max series read command in every ACT to PRE period, for a designated bank.

DDRMON_PER_BANK_SERIES_WR_BURST_TIMES_NUM

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_series_wr_burst_times_number per_bank_series_wr_burst_times_number number for per bank statistics. Count the total series write command in every ACT to PRE period, for a designated bank.

DDRMON_PER_BANK_RD2RD_PAGE_HIT_NUM

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_rank_rd2rd_page_hit_number per_rank_rd2rd_page_hit_number for per bank statistics. Count every read to read page hit for designated bank. For example, for bank n. ACT-RD-RD-PRE, count as 1. ACT-RD-RD-RD-PRE, count as 2 and so on.

DDRMON_PER_BANK_WR2WR_PAGE_HIT_NUM

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_rank_wr2wr_page_hit_number per_rank_wr2wr_page_hit_number for per bank statistics. Count every write to write page hit for designated bank. For example, for bank n. ACT-WR-WR-PRE, count as 1. ACT-WR-WR-WR-PRE, count as 2 and so on

DDRMON_PER_BANK_RD2WR_PAGE_HIT_NUM

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_rank_rd2wr_page_hit_number per_rank_rd2wr_page_hit_number for per bank statistics. Count every read to write page hit for designated bank.

DDRMON_PER_BANK_WR2RD_PAGE_HIT_NUM

Address: **Operational Base** + offset (0x012C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	per_rank_wr2rd_page_hit_number per_rank_wr2rd_page_hit_number for per bank statistics. Count every write to read page hit for designated bank.

DDRMON_PER_BANK_RD2RD_PAGE_MISS_NUM

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_rank_rd2rd_page_miss_number per_rank_rd2rd_page_miss_number for per bank statistics. Count each RD-PRE-ACT-RD pattern for designated bank.

DDRMON_PER_BANK_WR2WR_PAGE_MISS_NUM

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_rank_wr2wr_page_miss_number per_rank_wr2wr_page_miss_number for per bank statistics. Count each WR-PRE-ACT-WR pattern for designated bank.

DDRMON_PER_BANK_RD2WR_PAGE_MISS_NUM

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_rank_rd2wr_page_miss_number per_rank_rd2wr_page_miss_number for per bank statistics. Count each RD-PRE-ACT-WR pattern for designated bank.

DDRMON_PER_BANK_WR2RD_PAGE_MISS_NUM

Address: **Operational Base** + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_rank_wr2rd_page_miss_number per_rank_wr2rd_page_miss_number for per bank statistics. Count each WR-PRE-ACT-RD pattern for designated bank.

DDRMON_ALL_BANK_ACT_NUM

Address: **Operational Base** + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_act_num DFI active command number in the statistics range.

DDRMON_ALL_BANK_WR_NUM

Address: **Operational Base** + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_wr_num DFI write command number in the statistics range.

DDRMON_ALL_BANK_RD_NUM

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Address: **Operational Base** + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_rd_num DFI read command number in the statistics range.

DDRMON_ALL_BANK_ACT_ACT_NUM

Address: **Operational Base** + offset (0x014C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_act_act_number all_rank_act_act_number for all bank statistics. Count all ACT-ACT pattern in DDR command bus.

DDRMON_ALL_BANK_ACT_PRE_NUM

Address: **Operational Base** + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_act_pre_number all_rank_act_pre_number for all bank statistics. Count all ACT-PRE pattern in DDR command bus.

DDRMON_ALL_BANK_ACT_RDWR_SAME_NUM

Address: **Operational Base** + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_act_rdwr_same_number all_rank_act_rdwr_same_number for all bank statistics. Count all ACT-RD or ACT-WR pattern, which ACT and RD/WR command operation the same rank, same bank and same row.

DDRMON_ALL_BANK_PRE_ACT_NUM

Address: **Operational Base** + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_pre_act_number all_rank_pre_act_number for all bank statistics. Count all PRE-ACT pattern in DDR command bus.

DDRMON_ALL_BANK_RDWR_PRE_SAME_NUM

Address: **Operational Base** + offset (0x015C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_rdwr_pre_same_number all_rank_rdwr_pre_same_number for all bank statistics. Count all RD-PRE or WR-PRE pattern, which RD/WR command and PRE operation the same rank, same bank and same row.

DDRMON_ALL_BANK_RD2WR_NUM

Address: **Operational Base** + offset (0x0160)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_rd2wr_number all_rank_rd2wr_number for all bank statistics. Count all RD-WR pattern in DDR command bus.

DDRMON_ALL_BANK_WR2RD_NUM

Address: **Operational Base** + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_wr2rd_number all_rank_wr2rd_number for all bank statistics. Count all WR-RD pattern in DDR command bus.

DDRMON_ALL_BANK_SERIES_RD_TOTAL_CNT_NUM

Address: **Operational Base** + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_series_rd_total_cnt_number all_bank_series_rd_total_cnt_number for all bank statistics. Count all RD-RD pattern in DDR command bus.

DDRMON_ALL_BANK_SERIES_WR_TOTAL_CNT_NUM

Address: **Operational Base** + offset (0x016C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_series_wr_total_cnt_number all_bank_series_wr_total_cnt_number for all bank statistics. Count all WR-WR pattern in DDR command bus.

DDRMON_ALL_BANK_SERIES_RD_BURST_MAX_NUM

Address: **Operational Base** + offset (0x0170)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_series_rd_burst_max_number all_bank_series_rd_burst_max_number for all bank statistics. Count the max series RD pattern in DDR command bus.

DDRMON_ALL_BANK_SERIES_RD_BURST_TIMES_NUM

Address: **Operational Base** + offset (0x0174)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_series_rd_burst_times_number all_bank_series_rd_burst_times_number for all bank statistics. Count the total numer for each RD-RD pattern in DDR command bus. For example, ACT-RD-RD-WR-RD-RD-RD-PRE count as 2.

DDRMON_ALL_BANK_SERIES_WR_BURST_MAX_NUM

Address: **Operational Base** + offset (0x0178)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_series_wr_burst_max_number all_bank_series_wr_burst_max_number for all bank statistics. Count the max series WR pattern in DDR command bus.

DDRMON_ALL_BANK_SERIES_WR_BURST_TIMES_NUM

Address: **Operational Base** + offset (0x017C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_series_wr_burst_times_number all_bank_series_wr_burst_times_number for all bank statistics. Count the total numer for each WR-WR pattern in DDR command bus. For example, ACT-WR-WR-RD-WR-WR-WR-PRE count as 2.

DDRMON_ALL_BANK_MWR_CNT_NUM

Address: **Operational Base** + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	all_bank_mwr_cnt_number Count DFI mask write command number for all bank statistics.

DDRMON_ALL_BANK_TCCDMW_CNT_NUM

Address: **Operational Base** + offset (0x0184)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_tccdmw_cnt_number all_bank_tccdmw_cnt_number for all bank statistics. Count all Tccdmw in DDR command bus. For LPDDR4: 1) Count WR-MWR pattern for same rank and same bank. 2) Count MWR-MWR pattern for same rank and same bank. For LPDDR5: 1) Count WR-MWR pattern for same rank, same bank group and same bank. 2) Count MWR-MWR pattern for same rank and same bank group and same bank.

DDRMON_ALL_BANK_TCCD_L_CNT_NUM

Address: **Operational Base** + offset (0x0188)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_tccd_l_cnt_number all_bank_tccd_l_cnt_number for all bank statistics. Count all Tccd_L for DDR command bus. For LPDDR5 4bank/4 bank group mode only 1) Count all RD-RD, WR-WR and MWR-WR pattern for same rank, same bank group. 2) Count all WR-MWR, MWR-MWR for same rank, same bank group and different bank.

DDRMON_ALL_BANK_SYNC_CNT_NUM

Address: **Operational Base** + offset (0x018C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_sync_count_number all_bank_syc_number for all bank statistics. For LPDDR5 only, count all SYNC command in DDR command bus.

DDRMON_ALL_BANK_CAS_B3_RD_NUM

Address: **Operational Base** + offset (0x0190)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_cas_b3_rd_number all_bank_cas_b3_rd_number for all bank statistics. For LPDDR5 only, count all CAS command which B3 bit equals 1.

DDRMON_IF_CTRL

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15:3	RO	0x0000	reserved
2	RW	0x0	if_mon_en 1'b1: Enable 1'b0: Disable
1	RO	0x0	reserved
0	RW	0x0	direction 1'b1: Read 1'b0: Write

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DDRMON_MSTID

Address: **Operational Base** + offset (0x0204)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	ddr_mstid High 7 bits: Master ID Low 10 bits: AXI command ID

DDRMON_IDMSK

Address: **Operational Base** + offset (0x0208)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	ddr_idmsk When bit set to high, this bit of MSTID will be masked, and does not take part in the ID comparison.

DDRMON_WR_START_ADDR_31_0

Address: **Operational Base** + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_start_addr_31_0 Bit [31:0] of write start address for address comparison.

DDRMON_WR_START_ADDR_39_32

Address: **Operational Base** + offset (0x0210)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	wr_start_addr_39_32 Bit [39:32] of write start address for address comparison.

DDRMON_WR_END_ADDR_31_0

Address: **Operational Base** + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_end_addr_31_0 Bit [31:0] of write end address for address comparison.

DDRMON_WR_END_ADDR_39_32

Address: **Operational Base** + offset (0x0218)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	wr_end_addr_39_32 Bit [39:32] of write end address for address comparison.

DDRMON_RD_START_ADDR_31_0

Address: **Operational Base** + offset (0x021C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_start_addr_31_0 Bit [31:0] of read start address for address comparison.

DDRMON_RD_START_ADDR_39_32

Address: **Operational Base** + offset (0x0220)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	rd_start_addr_39_32 Bit [39:32] of read start address for address comparison.

DDRMON_RD_END_ADDR_31_0

Address: **Operational Base** + offset (0x0224)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_end_addr_31_0 Bits [31:0] of read end address for address comparison.

DDRMON_RD_END_ADDR_39_32

Address: **Operational Base** + offset (0x0228)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	rd_end_addr_39_32 Bits [39:32] of read end address for address comparison.

DDRMON_PORT0_FIFO0_ADDR_31_0

Address: **Operational Base** + offset (0x0240)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port0_ddr_fifo0_addr_31_0 Bits [31:0] of DDR controller AXI port0 interface address FIFO0. This register should be used together with PORT0_FIFO0_ADDR_63_32. The expression is as follows. {PORT0_FIFO0_ADDR_63_32, PORT0_FIFO0_ADDR_31_0} = {20'h0, awid_0/arid_0[7:0], awready_0/arready_0, awvalid_0/arvalid_0, awaddr_0/araddr_0[33:0]}

DDRMON_PORT0_FIFO0_ADDR_63_32

Address: **Operational Base** + offset (0x0244)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	ddr_fifo0_addr_63_32 Bits [63:32] of DDR controller AXI port0 interface address FIFO0. This register should be used together with PORT0_FIFO0_ADDR_63_32. The expression is as follows. {PORT0_FIFO0_ADDR_63_32, PORT0_FIFO0_ADDR_31_0} = {20'h0, awid_0/arid_0[7:0], awready_0/arready_0, awvalid_0/arvalid_0, awaddr_0/araddr_0[33:0]}

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DDRMON_PORT0_FIFO1_ADDR_31_0

Address: **Operational Base** + offset (0x0248)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port0_ddr_fifo1_addr_31_0 Bits [31:0] of DDR controller AXI port0 interface address FIFO1. This register should be used together with PORT0_FIFO1_ADDR_63_32. The expression is as follows. {PORT0_FIFO1_ADDR_63_32, PORT0_FIFO1_ADDR_31_0} = {20'h0, awid_0/arid_0[7:0], awready_0/arready_0, awvalid_0/arvalid_0, awaddr_0/araddr_0[33:0]}

DDRMON_PORT0_FIFO1_ADDR_63_32

Address: **Operational Base** + offset (0x024C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	port0_ddr_fifo1_addr_63_32 Bits [63:32] of DDR controller AXI port0 interface address FIFO1. This register should be used together with PORT0_FIFO1_ADDR_63_32. The expression is as follows. {PORT0_FIFO1_ADDR_63_32, PORT0_FIFO1_ADDR_31_0} = {20'h0, awid_0/arid_0[7:0], awready_0/arready_0, awvalid_0/arvalid_0, awaddr_0/araddr_0[33:0]}

DDRMON_PORT0_FIFO2_ADDR_31_0

Address: **Operational Base** + offset (0x0250)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port0_ddr_fifo2_addr_31_0 Bits [31:0] of DDR controller AXI port0 interface address FIFO2. This register should be used together with PORT0_FIFO2_ADDR_63_32. The expression is as follows. {PORT0_FIFO2_ADDR_63_32, PORT0_FIFO2_ADDR_31_0} = {20'h0, awid_0/arid_0[7:0], awready_0/arready_0, awvalid_0/arvalid_0, awaddr_0/araddr_0[33:0]}

DDRMON_PORT0_FIFO2_ADDR_63_32

Address: **Operational Base** + offset (0x0254)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	port0_ddr_fifo2_addr_63_32 Bits [63:32] of DDR controller AXI port0 interface address FIFO2. This register should be used together with PORT0_FIFO2_ADDR_63_32. The expression is as follows. {PORT0_FIFO2_ADDR_63_32, PORT0_FIFO2_ADDR_31_0} = {20'h0, awid_0/arid_0[7:0], awready_0/arready_0, awvalid_0/arvalid_0, awaddr_0/araddr_0[33:0]}

DDRMON_PORT0_FIFO3_ADDR_31_0

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Address: **Operational Base** + offset (0x0258)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port0_ddr_fifo3_addr_31_0 Bits [31:0] of DDR controller AXI port0 interface address FIFO3. This register should be used together with PORT0_FIFO3_ADDR_63_32. The expression is as follows. {PORT0_FIFO3_ADDR_63_32, PORT0_FIFO3_ADDR_31_0} = {20'h0, awid_0/arid_0[7:0], awready_0/arready_0, awvalid_0/arvalid_0, awaddr_0/araddr_0[33:0]}

DDRMON_PORT0_FIFO3_ADDR_63_32

Address: **Operational Base** + offset (0x025C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	port0_ddr_fifo3_addr_63_32 Bits [63:32] of DDR controller AXI port0 interface address FIFO3. This register should be used together with PORT0_FIFO3_ADDR_63_32. The expression is as follows. {PORT0_FIFO3_ADDR_63_32, PORT0_FIFO3_ADDR_31_0} = {20'h0, awid_0/arid_0[7:0], awready_0/arready_0, awvalid_0/arvalid_0, awaddr_0/araddr_0[33:0]}

DDRMON_PORT1_FIFO0_ADDR_31_0

Address: **Operational Base** + offset (0x0260)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port1_ddr_fifo0_addr_31_0 Bits [31:0] of DDR controller AXI port1 interface address FIFO0. This register should be used together with PORT1_FIFO0_ADDR_63_32. The expression is as follows. {PORT1_FIFO0_ADDR_63_32, PORT1_FIFO0_ADDR_31_0} = {20'h0, awid_1/arid_1[7:0], awready_1/arready_1, awvalid_1/arvalid_1, awaddr_1/araddr_1[33:0]}

DDRMON_PORT1_FIFO0_ADDR_63_32

Address: **Operational Base** + offset (0x0264)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	port1_ddr_fifo0_addr_63_32 Bits [63:32] of DDR controller AXI port1 interface address FIFO0. This register should be used together with PORT1_FIFO0_ADDR_63_32. The expression is as follows. {PORT1_FIFO0_ADDR_63_32, PORT1_FIFO0_ADDR_31_0} = {20'h0, awid_1/arid_1[7:0], awready_1/arready_1, awvalid_1/arvalid_1, awaddr_1/araddr_1[33:0]}

DDRMON_PORT1_FIFO1_ADDR_31_0

Address: **Operational Base** + offset (0x0268)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port1_ddr_fifo1_addr_31_0 Bits [31:0] of DDR controller AXI port1 interface address FIFO1. This register should be used together with PORT1_FIFO1_ADDR_63_32. The expression is as follows. {PORT1_FIFO1_ADDR_63_32, PORT1_FIFO1_ADDR_31_0} = {20'h0, awid_1/arid_1[7:0], awready_1/arready_1, awvalid_1/arvalid_1, awaddr_1/araddr_1[33:0]}

DDRMON_PORT1_FIFO1_ADDR_63_32

Address: **Operational Base** + offset (0x026C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	port1_ddr_fifo1_addr_63_32 Bits [63:32] of DDR controller AXI port1 interface address FIFO1. This register should be used together with PORT1_FIFO1_ADDR_63_32. The expression is as follows. {PORT1_FIFO1_ADDR_63_32, PORT1_FIFO1_ADDR_31_0} = {20'h0, awid_1/arid_1[7:0], awready_1/arready_1, awvalid_1/arvalid_1, awaddr_1/araddr_1[33:0]}

DDRMON_PORT1_FIFO2_ADDR_31_0

Address: **Operational Base** + offset (0x0270)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port1_ddr_fifo2_addr_31_0 Bits [31:0] of DDR controller AXI port1 interface address FIFO2. This register should be used together with PORT1_FIFO2_ADDR_63_32. The expression is as follows. {PORT1_FIFO2_ADDR_63_32, PORT1_FIFO2_ADDR_31_0} = {20'h0, awid_1/arid_1[7:0], awready_1/arready_1, awvalid_1/arvalid_1, awaddr_1/araddr_1[33:0]}

DDRMON_PORT1_FIFO2_ADDR_63_32

Address: **Operational Base** + offset (0x0274)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	port1_ddr_fifo2_addr_63_32 Bits [63:32] of DDR controller AXI port1 interface address FIFO2. This register should be used together with PORT1_FIFO2_ADDR_63_32. The expression is as follows. {PORT1_FIFO2_ADDR_63_32, PORT1_FIFO2_ADDR_31_0} = {20'h0, awid_1/arid_1[7:0], awready_1/arready_1, awvalid_1/arvalid_1, awaddr_1/araddr_1[33:0]}

DDRMON_PORT1_FIFO3_ADDR_31_0

Address: **Operational Base** + offset (0x0278)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port1_ddr_fifo3_addr_31_0 Bits [31:0] of DDR controller AXI port1 interface address FIFO3. This register should be used together with PORT1_FIFO3_ADDR_63_32. The expression is as follows. {PORT1_FIFO3_ADDR_63_32, PORT1_FIFO3_ADDR_31_0} = {20'h0, awid_1/arid_1[7:0], awready_1/arready_1, awvalid_1/arvalid_1, awaddr_1/araddr_1[33:0]}

DDRMON_PORT1_FIFO3_ADDR_63_32

Address: **Operational Base** + offset (0x027C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	port1_ddr_fifo3_addr_63_32 Bits [63:32] of DDR controller AXI port1 interface address FIFO3. This register should be used together with PORT1_FIFO3_ADDR_63_32. The expression is as follows. {PORT1_FIFO3_ADDR_63_32, PORT1_FIFO3_ADDR_31_0} = {20'h0, awid_1/arid_1[7:0], awready_1/arready_1, awvalid_1/arvalid_1, awaddr_1/araddr_1[33:0]}

DDRMON_PORT2_FIFO0_ADDR_31_0

Address: **Operational Base** + offset (0x0280)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port2_ddr_fifo0_addr_31_0 Bits [31:0] of DDR controller AXI port2 interface address FIFO0. This register should be used together with PORT2_FIFO0_ADDR_63_32. The expression is as follows. {PORT2_FIFO0_ADDR_63_32, PORT2_FIFO0_ADDR_31_0} = {20'h0, awid_2/arid_2[7:0], awready_2/arready_2, awvalid_2/arvalid_2, awaddr_2/araddr_2[33:0]}

DDRMON_PORT2_FIFO0_ADDR_63_32

Address: **Operational Base** + offset (0x0284)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	port2_ddr_fifo0_addr_63_32 Bits [63:32] of DDR controller AXI port2 interface address FIFO0. This register should be used together with PORT2_FIFO0_ADDR_63_32. The expression is as follows. {PORT2_FIFO0_ADDR_63_32, PORT2_FIFO0_ADDR_31_0} = {20'h0, awid_2/arid_2[7:0], awready_2/arready_2, awvalid_2/arvalid_2, awaddr_2/araddr_2[33:0]}

DDRMON_PORT2_FIFO1_ADDR_31_0

Address: **Operational Base** + offset (0x0288)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port2_ddr_fifo1_addr_31_0 Bits [31:0] of DDR controller AXI port2 interface address FIFO1. This register should be used together with PORT2_FIFO1_ADDR_63_32. The expression is as follows. {PORT2_FIFO1_ADDR_63_32, PORT2_FIFO1_ADDR_31_0} = {20'h0, awid_2/arid_2[7:0], awready_2/arready_2, awvalid_2/arvalid_2, awaddr_2/araddr_2[33:0]}

DDRMON_PORT2_FIFO1_ADDR_63_32

Address: **Operational Base** + offset (0x028C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	port2_ddr_fifo1_addr_63_32 Bits [63:32] of DDR controller AXI port2 interface address FIFO1. This register should be used together with PORT2_FIFO1_ADDR_63_32. The expression is as follows. {PORT2_FIFO1_ADDR_63_32, PORT2_FIFO1_ADDR_31_0} = {20'h0, awid_2/arid_2[7:0], awready_2/arready_2, awvalid_2/arvalid_2, awaddr_2/araddr_2[33:0]}

DDRMON_PORT2_FIFO2_ADDR_31_0

Address: **Operational Base** + offset (0x0290)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port2_ddr_fifo2_addr_31_0 Bits [31:0] of DDR controller AXI port2 interface address FIFO2. This register should be used together with PORT2_FIFO2_ADDR_63_32. The expression is as follows. {PORT2_FIFO2_ADDR_63_32, PORT2_FIFO2_ADDR_31_0} = {20'h0, awid_2/arid_2[7:0], awready_2/arready_2, awvalid_2/arvalid_2, awaddr_2/araddr_2[33:0]}

DDRMON_PORT2_FIFO2_ADDR_63_32

Address: **Operational Base** + offset (0x0294)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	port2_ddr_fifo2_addr_63_32 Bits [63:32] of DDR controller AXI port2 interface address FIFO2. This register should be used together with PORT2_FIFO2_ADDR_63_32. The expression is as follows. {PORT2_FIFO2_ADDR_63_32, PORT2_FIFO2_ADDR_31_0} = {20'h0, awid_2/arid_2[7:0], awready_2/arready_2, awvalid_2/arvalid_2, awaddr_2/araddr_2[33:0]}

DDRMON_PORT2_FIFO3_ADDR_31_0

Address: **Operational Base** + offset (0x0298)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port2_ddr_fifo3_addr_31_0 Bits [31:0] of DDR controller AXI port2 interface address FIFO3. This register should be used together with PORT2_FIFO3_ADDR_63_32. The expression is as follows. {PORT2_FIFO3_ADDR_63_32, PORT2_FIFO3_ADDR_31_0} = {20'h0, awid_2/arid_2[7:0], awready_2/arready_2, awvalid_2/arvalid_2, awaddr_2/araddr_2[33:0]}

DDRMON_PORT2_FIFO3_ADDR_63_32

Address: **Operational Base** + offset (0x029C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	port2_ddr_fifo3_addr_63_32 Bits [63:32] of DDR controller AXI port2 interface address FIFO3. This register should be used together with PORT2_FIFO3_ADDR_63_32. The expression is as follows. {PORT2_FIFO3_ADDR_63_32, PORT2_FIFO3_ADDR_31_0} = {20'h0, awid_2/arid_2[7:0], awready_2/arready_2, awvalid_2/arvalid_2, awaddr_2/araddr_2[33:0]}

DDRMON_PORT3_FIFO0_ADDR_31_0

Address: **Operational Base** + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port3_ddr_fifo0_addr_31_0 Bits [31:0] of DDR controller AXI port3 interface address FIFO0. This register should be used together with PORT3_FIFO0_ADDR_63_32. The expression is as follows. {PORT3_FIFO0_ADDR_63_32, PORT3_FIFO0_ADDR_31_0} = {20'h0, awid_3/arid_3[7:0], awready_3/arready_3, awvalid_3/arvalid_3, awaddr_3/araddr_3[33:0]}

DDRMON_PORT3_FIFO0_ADDR_63_32

Address: **Operational Base** + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	port3_ddr_fifo0_addr_63_32 Bits [63:32] of DDR controller AXI port3 interface address FIFO0. This register should be used together with PORT3_FIFO0_ADDR_63_32. The expression is as follows. {PORT3_FIFO0_ADDR_63_32, PORT3_FIFO0_ADDR_31_0} = {20'h0, awid_3/arid_3[7:0], awready_3/arready_3, awvalid_3/arvalid_3, awaddr_3/araddr_3[33:0]}

DDRMON_PORT3_FIFO1_ADDR_31_0

Address: **Operational Base** + offset (0x02A8)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port3_ddr_fifo1_addr_31_0 Bits [31:0] of DDR controller AXI port3 interface address FIFO1. This register should be used together with PORT3_FIFO1_ADDR_63_32. The expression is as follows. {PORT3_FIFO1_ADDR_63_32, PORT3_FIFO1_ADDR_31_0} = {20'h0, awid_3/arid_3[7:0], awready_3/arready_3, awvalid_3/arvalid_3, awaddr_3/araddr_3[33:0]}

DDRMON_PORT3_FIFO1_ADDR_63_32

Address: **Operational Base** + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	port3_ddr_fifo1_addr_63_32 Bits [63:32] of DDR controller AXI port3 interface address FIFO1. This register should be used together with PORT3_FIFO1_ADDR_63_32. The expression is as follows. {PORT3_FIFO1_ADDR_63_32, PORT3_FIFO1_ADDR_31_0} = {20'h0, awid_3/arid_3[7:0], awready_3/arready_3, awvalid_3/arvalid_3, awaddr_3/araddr_3[33:0]}

DDRMON_PORT3_FIFO2_ADDR_31_0

Address: **Operational Base** + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port3_ddr_fifo2_addr_31_0 Bits [31:0] of DDR controller AXI port3 interface address FIFO2. This register should be used together with PORT3_FIFO2_ADDR_63_32. The expression is as follows. {PORT3_FIFO2_ADDR_63_32, PORT3_FIFO2_ADDR_31_0} = {20'h0, awid_3/arid_3[7:0], awready_3/arready_3, awvalid_3/arvalid_3, awaddr_3/araddr_3[33:0]}

DDRMON_PORT3_FIFO2_ADDR_63_32

Address: **Operational Base** + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	port3_ddr_fifo2_addr_63_32 Bits [63:32] of DDR controller AXI port3 interface address FIFO2. This register should be used together with PORT3_FIFO2_ADDR_63_32. The expression is as follows. {PORT3_FIFO2_ADDR_63_32, PORT3_FIFO2_ADDR_31_0} = {20'h0, awid_3/arid_3[7:0], awready_3/arready_3, awvalid_3/arvalid_3, awaddr_3/araddr_3[33:0]}

DDRMON_PORT3_FIFO3_ADDR_31_0

Address: **Operational Base** + offset (0x02B8)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port3_ddr_fifo3_addr_31_0 Bits [31:0] of DDR controller AXI port3 interface address FIFO3. This register should be used together with PORT3_FIFO3_ADDR_63_32. The expression is as follows. {PORT3_FIFO3_ADDR_63_32, PORT3_FIFO3_ADDR_31_0} = {20'h0, awid_3/arid_3[7:0], awready_3/arready_3, awvalid_3/arvalid_3, awaddr_3/araddr_3[33:0]}

DDRMON_PORT3_FIFO3_ADDR_63_32

Address: **Operational Base** + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	port3_ddr_fifo3_addr_63_32 Bits [63:32] of DDR controller AXI port3 interface address FIFO3. This register should be used together with PORT3_FIFO3_ADDR_63_32. The expression is as follows. {PORT3_FIFO3_ADDR_63_32, PORT3_FIFO3_ADDR_31_0} = {20'h0, awid_3/arid_3[7:0], awready_3/arready_3, awvalid_3/arvalid_3, awaddr_3/araddr_3[33:0]}

DDRMON_PORT4_FIFO0_ADDR_31_0

Address: **Operational Base** + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port3_ddr_fifo0_addr_31_0 Bits [31:0] of DDR controller AXI port4 interface address FIFO0. This register should be used together with PORT4_FIFO0_ADDR_63_32. The expression is as follows. {PORT4_FIFO0_ADDR_63_32, PORT4_FIFO0_ADDR_31_0} = {20'h0, awid_4/arid_4[7:0], awready_4/arready_4, awvalid_4/arvalid_4, awaddr_4/araddr_4[33:0]}

DDRMON_PORT4_FIFO0_ADDR_63_32

Address: **Operational Base** + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	port4_ddr_fifo0_addr_63_32 Bits [63:32] of DDR controller AXI port4 interface address FIFO0. This register should be used together with PORT4_FIFO0_ADDR_63_32. The expression is as follows. {PORT4_FIFO0_ADDR_63_32, PORT4_FIFO0_ADDR_31_0} = {20'h0, awid_4/arid_4[7:0], awready_4/arready_4, awvalid_4/arvalid_4, awaddr_4/araddr_4[33:0]}

DDRMON_PORT4_FIFO1_ADDR_31_0

Address: **Operational Base** + offset (0x02C8)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port4_ddr_fifo1_addr_31_0 Bits [31:0] of DDR controller AXI port4 interface address FIFO1. This register should be used together with PORT4_FIFO1_ADDR_63_32. The expression is as follows. {PORT4_FIFO1_ADDR_63_32, PORT4_FIFO1_ADDR_31_0} = {20'h0, awid_4/arid_4[7:0], awready_4/arready_4, awvalid_4/arvalid_4, awaddr_4/araddr_4[33:0]}

DDRMON_PORT4_FIFO1_ADDR_63_32

Address: **Operational Base** + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	port4_ddr_fifo1_addr_63_32 Bits [63:32] of DDR controller AXI port4 interface address FIFO1. This register should be used together with PORT4_FIFO1_ADDR_63_32. The expression is as follows. {PORT4_FIFO1_ADDR_63_32, PORT4_FIFO1_ADDR_31_0} = {20'h0, awid_4/arid_4[7:0], awready_4/arready_4, awvalid_4/arvalid_4, awaddr_4/araddr_4[33:0]}

DDRMON_PORT4_FIFO2_ADDR_31_0

Address: **Operational Base** + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port4_ddr_fifo2_addr_31_0 Bits [31:0] of DDR controller AXI port4 interface address FIFO2. This register should be used together with PORT4_FIFO2_ADDR_63_32. The expression is as follows. {PORT4_FIFO2_ADDR_63_32, PORT4_FIFO2_ADDR_31_0} = {20'h0, awid_4/arid_4[7:0], awready_4/arready_4, awvalid_4/arvalid_4, awaddr_4/araddr_4[33:0]}

DDRMON_PORT4_FIFO2_ADDR_63_32

Address: **Operational Base** + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	port4_ddr_fifo2_addr_63_32 Bits [63:32] of DDR controller AXI port4 interface address FIFO2. This register should be used together with PORT4_FIFO2_ADDR_63_32. The expression is as follows. {PORT4_FIFO2_ADDR_63_32, PORT4_FIFO2_ADDR_31_0} = {20'h0, awid_4/arid_4[7:0], awready_4/arready_4, awvalid_4/arvalid_4, awaddr_4/araddr_4[33:0]}

DDRMON_PORT4_FIFO3_ADDR_31_0

Address: **Operational Base** + offset (0x02D8)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	port4_ddr_fifo3_addr_31_0 Bits [31:0] of DDR controller AXI port4 interface address FIFO3. This register should be used together with PORT4_FIFO3_ADDR_63_32. The expression is as follows. {PORT4_FIFO3_ADDR_63_32, PORT4_FIFO3_ADDR_31_0} = {20'h0, awid_4/arid_4[7:0], awready_4/arready_4, awvalid_4/arvalid_4, awaddr_4/araddr_4[33:0]}

DDRMON_PORT4_FIFO3_ADDR_63_32

Address: **Operational Base** + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	port4_ddr_fifo3_addr_63_32 Bits [63:32] of DDR controller AXI port4 interface address FIFO3. This register should be used together with PORT4_FIFO3_ADDR_63_32. The expression is as follows. {PORT4_FIFO3_ADDR_63_32, PORT4_FIFO3_ADDR_31_0} = {20'h0, awid_4/arid_4[7:0], awready_4/arready_4, awvalid_4/arvalid_4, awaddr_4/araddr_4[33:0]}

DDRMON_LPR_CREDIT_TOTAL_LOW32_NUM

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lpr_credit_total_num_31_0 Low 32 bits of DDR controller LPR credits total number.

DDRMON_HPR_CREDIT_TOTAL_LOW32_NUM

Address: **Operational Base** + offset (0x0404)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hpr_credit_total_num_31_0 Low 32 bits of DDR controller HPR credits total number.

DDRMON_WR_CREDIT_TOTAL_LOW32_NUM

Address: **Operational Base** + offset (0x0408)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_credit_total_num_31_0 Low 32 bits of DDR controller WR credits total number.

DDRMON_LPR_CREDIT_TOTAL_HIGH8_NUM

Address: **Operational Base** + offset (0x0410)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	lpr_credit_total_num_39_32 High 8 bits of DDR controller LPR credits total number.

DDRMON_HPR_CREDIT_TOTAL_HIGH8_NUM

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Address: **Operational Base** + offset (0x0414)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	hpr_credit_total_num_39_32 High 8 bits of DDR controller HPR credits total number.

DDRMON_WR_CREDIT_TOTAL_HIGH8_NUM

Address: **Operational Base** + offset (0x0418)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	wr_credit_total_num_39_32 High 8 bits of DDR controller WR credits total number.

DDRMON_LPR_CREDIT_CNT_NUM_0_15

Address: **Operational Base** + offset (0x0420)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lpr_credit_cnt_num_0_15 The sum of LPR credits which is within the range of 0 and 15(including 0 and 15).

DDRMON_LPR_CREDIT_CNT_NUM_16_31

Address: **Operational Base** + offset (0x0424)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lpr_credit_cnt_num_16_31 The sum of LPR credits which is within the range of 16 and 31(including 16 and 31).

DDRMON_LPR_CREDIT_CNT_NUM_32_47

Address: **Operational Base** + offset (0x0428)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lpr_credit_cnt_num_32_47 The sum of LPR credits which is within the range of 32 and 47(including 32 and 47).

DDRMON_LPR_CREDIT_CNT_NUM_48_63

Address: **Operational Base** + offset (0x042C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lpr_credit_cnt_num_48_63 The sum of LPR credits which is within the range of 48 and 63(including 48 and 63).

DDRMON_LPR_CREDIT_CNT_NUM_FULL

Address: **Operational Base** + offset (0x0430)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lpr_credit_cnt_num_full Everytime the LPR credit is full(It means there are no LPR commands pending in DDR controller's read CAM), this counter will increase by 1'b1. The total LPR credit number is equal to DDR controller's register SCHED0.lpr_num_entries+1.

DDRMON_HPR_CREDIT_CNT_NUM_0_15

Address: **Operational Base** + offset (0x0440)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hpr_credit_cnt_num_0_15 The sum of HPR credits which is within the range of 0 and 15(including 0 and 15).

DDRMON_HPR_CREDIT_CNT_NUM_16_31

Address: **Operational Base** + offset (0x0444)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hpr_credit_cnt_num_16_31 The sum of HPR credits which is within the range of 16 and 31(including 16 and 31).

DDRMON_HPR_CREDIT_CNT_NUM_32_47

Address: **Operational Base** + offset (0x0448)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hpr_credit_cnt_num_32_47 The sum of HPR credits which is within the range of 32 and 47(including 32 and 47).

DDRMON_HPR_CREDIT_CNT_NUM_48_63

Address: **Operational Base** + offset (0x044C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hpr_credit_cnt_num_48_63 The sum of HPR credits which is within the range of 48 and 63(including 48 and 63).

DDRMON_HPR_CREDIT_CNT_NUM_FULL

Address: **Operational Base** + offset (0x0450)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hpr_credit_cnt_num_full Everytime the HPR credit is full(It means there are no HPR commands pending in DDR controller's read CAM), this counter will increase by 1'b1. The total HPR credit number is equal to DDR controller's register 64-(SCHED0.lpr_num_entries+1).

DDRMON_WR_CREDIT_CNT_NUM_0_15

Address: **Operational Base** + offset (0x0460)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_credit_cnt_num_0_15 The sum of WR credits which is within the range of 0 and 15(including 0 and 15).

DDRMON_WR_CREDIT_CNT_NUM_16_31

Address: **Operational Base** + offset (0x0464)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_credit_cnt_num_16_31 The sum of WR credits which is within the range of 16 and 31(including 16 and 31).

DDRMON_WR_CREDIT_CNT_NUM_32_47

Address: **Operational Base** + offset (0x0468)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_credit_cnt_num_32_47 The sum of WR credits which is within the range of 32 and 47(including 32 and 47).

DDRMON_WR_CREDIT_CNT_NUM_48_63

Address: **Operational Base** + offset (0x046C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_credit_cnt_num_48_63 The sum of WR credits which is within the range of 48 and 63(including 48 and 63).

DDRMON_WR_CREDIT_CNT_NUM_FULL

Address: **Operational Base** + offset (0x0470)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_credit_cnt_num_full Everytime the WR credit is full(It means there are no HPR commands pending in DDR controller's read CAM), this counter will increase by 1'b1. The total WR credit number is equal to 64.

7.5 Interface Description

DDR IOs from DDRPHY are listed as following table.

Table 7-1 DDR Channel 0 IO description

Pad Name	Description
LP4_CLKP_A/LP4x_CLKP_A/LP5_CLKP_A	Positive differential clock
LP4_CLKN_A/LP4x_CLKN_A/LP5_CLKN_A	Negative differential clock
LP4_RESET/LP4x_RESET/LP5_RESET	When asserted LOW, this signal resets the die.
LP4_CKE0_A/LP4x_CKE0_A/LP5_CSN0_A	Active-high clock enable signal for rank0 of LPDDR4/4X and acts as chip select signal for rank0 of LPDDR5.
LP4_CKE1_A/LP4x_CKE1_A/LP5_CSN1_A	Active-high clock enable signal for rank1 of LPDDR4/4X and acts as chip select signal for rank1 of LPDDR5.
LP4_CSN0_A/LP4X_CSN0_A	Chip select signal for rank0. Only used

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	for LPDDR4/4X.
LP4_CSN1_A/LP4X_CSN1_A	Chip select signal for rank1. Only used for LPDDR4/4X
LP4_A0_A/LP4x_A0_A/LP5_A0_A	Command and address signal bit0 for LPDDR4/4X and LPDDR5
LP4_A1_A/LP4x_A1_A/LP5_A1_A	Command and address signal bit1 for LPDDR4/4X and LPDDR5
LP4_A2_A/LP4x_A2_A/LP5_A2_A	Command and address signal bit2 for LPDDR4/4X and LPDDR5
LP4_A3_A/LP4x_A3_A/LP5_A3_A	Command and address signal bit3 for LPDDR4/4X and LPDDR5
LP4_A4_A/LP4x_A4_A/LP5_A4_A	Command and address signal bit4 for LPDDR4/4X and LPDDR5
LP4_A5_A/LP4x_A5_A/LP5_A5_A	Command and address signal bit5 for LPDDR4/4X and LPDDR5
LP5_A6_A	Command and address signal bit6 for LPDDR5,not used for LPDDR4/4X
LP4_DQS0P_A/LP4x_DQS0P_A/LP5_RDQS0P_A	Positive DQS for DQ[7:0]
LP4_DQS0N_A/LP4x_DQS0N_A/LP5_RDQS0N_A	Negative DQS for DQ[7:0]
LP4_DQS1P_A/LP4x_DQS1P_A/LP5_RDQS1P_A	Positive DQS for DQ[15:8]
LP4_DQS1N_A/LP4x_DQS1N_A/LP5_RDQS1N_A	Negative DQS for DQ[15:8]
LP5_WCK0P_A	Positive differential clock used for WRITE data capture and READ data output for LPDDR5. It corresponds to DQ[7:0].
LP5_WCK0N_A	Negative differential clock used for WRITE data capture and READ data output for LPDDR5. It corresponds to DQ[7:0].
LP5_WCK1P_A	Positive differential clock used for WRITE data capture and READ data output for LPDDR5. It corresponds to DQ[15:8].
LP5_WCK1N_A	Negative differential clock used for WRITE data capture and READ data output for LPDDR5. It corresponds to DQ[15:8].
LP4_DMI0_A/LP4x_DMI0_A/LP5_DMI0_A	This signal achieves multiple function such as Data Mask (DM) and Data Bus Inversion (DBI) by setting the Mode Register and it is a bi-directional signal and each byte of data has a DMI signal. This signal corresponds to DQ[7:0].
LP4_DMI1_A/LP4x_DMI1_A/LP5_DMI1_A	This signal corresponds to DQ[15:8].
LP4_DQi_A/LP4x_DQi_A/LP5_DQi_A (i=0~15)	Bidirectional data bus
ZQ_A	Used to calibrate the output drive strength and the termination resistance as calibration reference.

Table 7-2 DDR Channel 1 IO description

Pad Name	Description
LP4_CLKP_B/LP4x_CLKP_B/LP5_CLKP_B	Positive differential clock
LP4_CLKN_B/LP4x_CLKN_B/LP5_CLKN_B	Negative differential clock
LP4_CKE0_B/LP4x_CKE0_B/LP5_CSN0_B	Active-high clock enable signal for rank0 of LPDDR4/4X and acts as chip select signal for rank0 of LPDDR5.
LP4_CKE1_B/LP4x_CKE1_B/LP5_CSN1_B	Active-high clock enable signal for

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	rank1 of LPDDR4/4X and acts as chip select signal for rank1 of LPDDR5.
LP4_CSN0_B/LP4X_CSN0_B	Chip select signal for rank0. Only used for LPDDR4/4X.
LP4_CSN1_B/LP4X_CSN1_B	Chip select signal for rank1. Only used for LPDDR4/4X
LP4_A0_B/LP4x_A0_B/LP5_A0_B	Command and address signal bit0 for LPDDR4/4X and LPDDR5
LP4_A1_B/LP4x_A1_B/LP5_A1_B	Command and address signal bit1 for LPDDR4/4X and LPDDR5
LP4_A2_B/LP4x_A2_B/LP5_A2_B	Command and address signal bit2 for LPDDR4/4X and LPDDR5
LP4_A3_B/LP4x_A3_B/LP5_A3_B	Command and address signal bit3 for LPDDR4/4X and LPDDR5
LP4_A4_B/LP4x_A4_B/LP5_A4_B	Command and address signal bit4 for LPDDR4/4X and LPDDR5
LP4_A5_B/LP4x_A5_B/LP5_A5_B	Command and address signal bit5 for LPDDR4/4X and LPDDR5
LP5_A6_B	Command and address signal bit6 for LPDDR5,not used for LPDDR4/4X
LP4_DQS0P_B/LP4x_DQS0P_B/LP5_RDQS0P_B	Positive DQS for DQ[7:0]
LP4_DQS0N_B/LP4x_DQS0N_B/LP5_RDQS0N_B	Negative DQS for DQ[7:0]
LP4_DQS1P_B/LP4x_DQS1P_B/LP5_RDQS1P_B	Positive DQS for DQ[15:8]
LP4_DQS1N_B/LP4x_DQS1N_B/LP5_RDQS1N_B	Negative DQS for DQ[15:8]
LP5_WCK0P_B	Positive differential clock used for WRITE data capture and READ data output for LPDDR5. It corresponds to DQ[7:0].
LP5_WCK0N_B	Negative differential clock used for WRITE data capture and READ data output for LPDDR5. It corresponds to DQ[7:0].
LP5_WCK1P_B	Positive differential clock used for WRITE data capture and READ data output for LPDDR5. It corresponds to DQ[15:8].
LP5_WCK1N_B	Negative differential clock used for WRITE data capture and READ data output for LPDDR5. It corresponds to DQ[15:8].
LP4_DMI0_B/LP4x_DMI0_B/LP5_DMI0_B	This signal achieves multiple function such as Data Mask (DM) and Data Bus Inversion (DBI) by setting the Mode Register and it is a bi-directional signal and each byte of data has a DMI signal. This signal corresponds to DQ[7:0].
LP4_DMI1_B/LP4x_DMI1_B/LP5_DMI1_B	This signal corresponds to DQ[15:8].
LP4_DQi_B/LP4x_DQi_B/LP5_DQi_B (i=0~15)	Bidirectional data bus
ZQ_B	Used to calibrate the output drive strength and the termination resistance as calibration reference.

7.6 Application Notes

7.6.1 Quasi Dynamic Registers of DDRCTL

In addition to the dynamic registers, there are 4 categories of registers can be written after

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reset. These 4 kinds of registers are divided into group 1, group 2, group 3 and group 4. Each category requires specific conditions for the registers to be programmed. Once the programming conditions are met, DDRCTL_SWCTL.sw_done register must be programmed to 1'b0 to enable the software programming. Once the programming is completed, DDRCTL_SWCTL.sw_done must be set to 1'b1 and DDRCTL_SWSTAT.sw_done_ack must be read as 1'b1. This is to ensure that quasi dynamic registers are propagated correctly to the destination clocks. The protocol flowchart is shown below.

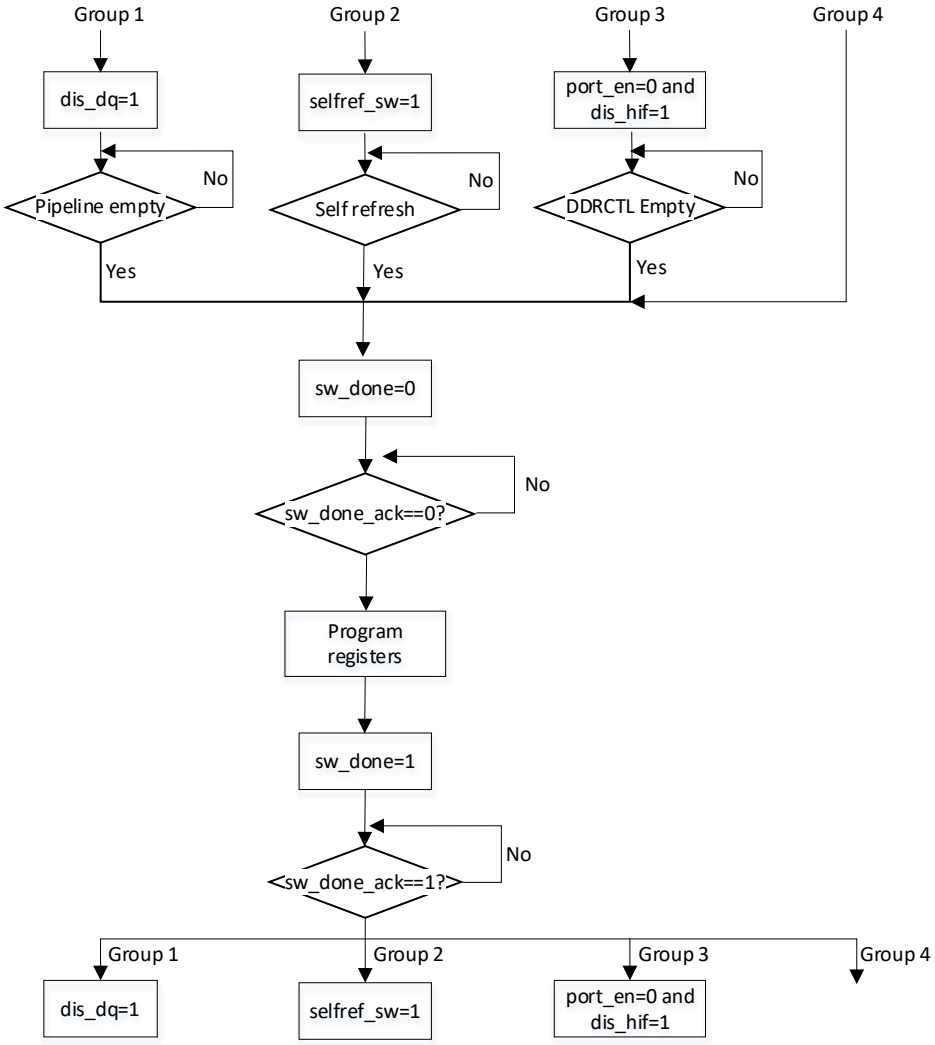


Fig. 7-5 Quasi dynamic registers program flow of DDRCTL

Group 1 refers to registers that can be written when no read/write traffic is present at the DFI. By setting DDRCTL_OPCTRL1.dis_dq register and polling DDRCTL_OPCTRLCAM.wr_data_pipeline_empty and DDRCTL_OPCTRLCAM.rd_data_pipeline_empty1, it is possible to prevent any read or write traffic from being sent on the DFI. In this mode, it is safe to write to the group 1 registers. Re-enable the traffic by writing DDRCTL_OPCTRL1.dis_dq to 1'b0.

Group 2 refers to registers that can be written in self-refresh mode. When the DDRCTL has entered self-refresh mode through software (DDRCTL_PWRCTL.selfref_sw), the DFI bus is idle until software exits self-refresh. In this mode, it is safe to write the group 2 registers. Re-enable the traffic by writing DDRCTL_PWRCTL.selfref_sw to 1'b0 and polling DDRCTL_STAT.operating_mode.

Group 3 refers to registers that can be written when controller is empty. For multi-port configurations, DDRCTL_PORTi_PCTRL.port_en(i=0~4) is used to enable or disable the input traffic per port. The controller idleness can be polled first from DDRCTL_PORTi_PSTAT register (wr_port_busy_n and rd_port_busy_n bit fields) and should read as DDRCTL_PORTi_PSTAT==32'b0 (not busy). DDRCTL_OPCTRL1.dis_hif is used to enable or disable the input traffic to the controller. Then, DDRCTL CAM/pipeline empty status must be polled ((DDRCTL_OPCTRLCAM.dbg_wr_q_empty== 1'b1) &&

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(DDRCTL_OPCTRLCAM.dbg_rd_q_empty== 1'b1) &&
(DDRCTL_OPCTRLCAM.wr_data_pipeline_empty== 1'b1) &&
(DDRCTL_OPCTRLCAM.rd_data_pipeline_empty==1'b1)). In this mode, it is safe to write the group 3 registers.
Group 4 refers to registers that can be written depending on DDRCTL_MSTR2.target_frequency. It is safe to write the registers in the other blocks other than the one is working. For example, it is safe to write registers in REGB_FREQ0, REGB_FREQ2 and REGB_FREQ3 when DDRCTL_MSTR2.target_frequency is equal to '1'.

7.6.2 2-channel Interleaving LPDDR4/4X Initialization

Following steps are for 2-channel interleaving LPDDR4/4X initialization.
1. Power up DDRPHY core supply (DDRPHY_DVDD), power up CKE power (DDRPHY_CKE_VDDQ) and then power up IO supply (DDRPHY_CK_VDDQ and DDRPHY_VDDQ).
2. Keep DDRPLL (D0APLL and D1APLL) at default configuration to output 24MHz frequency. Configure DDRPLL (D0BPLL and D1BPLL) to lock at target operation frequency. Now by default the input clk_phy2x of DDRPHY is 24MHz. Make sure that PCLK frequency of DDRPHY is not higher than clk_dfi which is generated from clk_phy2x.
3. De-assert PRESETn of DDRPHY and present of DDRCTL.
4. De-assert RESETn of DDRPHY. Wait for at least 10 cycles of clk_phy2x.
5. Set DDR_GRF_CHA/CHB_PHY_CON0[3](CHA/CHB registers are used to control DDR channel 0/1 respectively) and DDR_GRF_CHA/CHB_PHY_CON1[3] of DDR_GRF to 1'b1 to enable DDRPHY2XCLKGATE_ENABLE of each DDRPHY. Wait for at least 10 cycles of clk_phy2x.
6. De-assert div_rst_n of DDRPHY. Wait for at least 10 cycles of clk_phy2x.
7. Assert core_ddrc_rstn and aresetn_i(i=0~4)of DDRCTL.
8. De-assert rst_n of DDRPHY. Make sure that rst_n is released at 24MHz low frequency.
9. Set DDR_GRF_CHA/CHB_PHY_CON0[3] and DDR_GRF_CHA/CHB_PHY_CON1[3] of DDR_GRF to 1'b0 to disable DDRPHY2XCLKGATE_ENABLE of each DDRPHY.
10. Assert div_rst_n of DDRPHY.
11. Set DDRPHY registers to select memory type and clock mode.
    - DDRPHY_GNR_CON0.ctrl_ddr_mode='h0
    - DDRPHY_CLKMODE_CON.ctrl_phy_mode='h1
    - DDRPHY_CLKMODE_CON.ctrl_phy_clk_2x='h1
12. De-assert div_rst_n of DDRPHY.
13. Executes step 5 again to enable the output clk_dfi of DDRPHY. Clk_dfi is used as the source clock of DDRCTL. It is connected to the core_ddrc_core_clk, aclk_i(i=0~4) and bsm_clk of DDRCTL.
14. De-assert presetn of DDRCTL.
15. Set DDRCTL registers.
16. De-assert core_ddrc_rstn and aresetn_i(i=0~4) of DDRCTL.
17. Disable auto-refreshes, self-refresh, power down and assertion of dfi_dram_clk_disable by setting DDRCTL_RFSHCTL0.dis_auto_refresh = 1, DDRCTL_PWRCTL.powerdown_en = 0 and DDRCTL_PWRCTL.selfref_en = 0, DDRCTL_PWRTL.en_dfi_dram_clk_disable = 0.
18. Set DDRCTL_SWCTL.sw_done to 1'b0.
19. Set DDRCTL_DFIMISC.dfi_init_complete_en to 1'b0.
20. Set DDRCTL_SWCTL.sw_done to 1'b1.
21. Set DDRCTL_PORTi_PCTRL.port_en(i=0~4) to 1'b1 to enable AXI port 0~4 of DDRCTL.
22. Begin to set DDRPHY registers. Such as read latency, write latency and burst length and so on.
23. Apply DDRPHY IO settings before ZQ calibration.
24. Start DFI initialization
    - Set DDRPHY_MDLL_CON0.ctrl_dll_on=1'b0
    - DDRCTL should assert dfi_init_start from low to high
    - DDRCTL should wait dfi_init_complete change from low to high
25. Set DDRCTL_SWCTL.sw_done to 1'b0. Set DDRCTL_DFIMISC.dfi_init_start to 1'b0 and DDRCTL_DFIMISC.dfi_init_complete_en to 1'b1. Set DDRCTL_SWCTL.sw_done to 1'b1.
26. Wait for DDRCTL to move to normal operating mode by monitoring

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DDRCTL_STAT.operating_mode register.
27. DDRPHY vref related registers settings without vref training.
28. DDRPHY ODT related registers settings.
29. Start DDRPHY ZQ calibration.
    - Enable DDRPHY_ZQ_CON0.zq_clk_div_en
    - Enable DDRPHY_ZQ_CON0.zq_manual_str
    - Wait until DDRPHY_ZQ_CON1.zq_done is enabled
    - Disable DDRPHY_ZQ_CON0.zq_manual_str
    - Disable DDRPHY_ZQ_CON0.zq_clk_div_en
30. Frequency change to the target operation speed. Using frequency change protocol via MC-PHY handshake.
    - Set DDRCTL_SWCTL.sw_done to 1'b0.
    - Set DDRCTL_DFIMISC.dfi_init_complete_en to 1'b0.
    - Set DDRCTL_DFIMISC.dfi_init_start to 1'b1. Set DDRCTL_SWCTL.sw_done to 1'b1.
    - Poll DDRCTL_DFISTAT.dfi_init_complete=1'b0.
    - Programming DDR_GRF_CHA/CHB_PHY_CON0[3] and DDR_GRF_CHA/CHB_PHY_CON1[3] of DDR_GRF to 1'b0 to disable DDRPHY2XCLKGATE_ENABLE of each DDRPHY.
    - Assert div_rst_n of DDRPHY if LPDDR5 is used. If LP4/4X is used, don't assert div_rst_n.
    - Change clk_phy2x frequency of DDRPHY channel 0 by setting DDR0CRU_CLKSEL_CON00[0] to 1'b1 to select D0BPLL, set DDR1CRU_CLKSEL_CON00[0] to 1'b1 to select D1BPLL output clock as DDRPHY channel 1 driving clock.
    - Change PCLK of DDRPHY to high frequency such as 200MHz.
    - De-assert div_rst_n of DDRPHY if LPDDR5 is used. If LP4/4X is used, skip this flow.
    - Set DDR_GRF_CHA/CHB_PHY_CON0[3] and DDR_GRF_CHA/CHB_PHY_CON1[3] of DDR_GRF to 1'b1 to enable DDRPHY2XCLKGATE_ENABLE of each DDRPHY.
    - Set DDRCTL_SWCTL.sw_done to 1'b0. Set DDRCTL_DFIMISC.dfi_init_start to 1'b0. Set DDRCTL_SWCTL.sw_done to 1'b1.
    - Poll DDRCTL_DFISTAT.dfi_init_complete=1'b1.
    - Set DDRCTL_SWCTL.sw_done to 1'b0.
    - Set DDRCTL_DFIMISC.dfi_init_complete_en to 1'b1 to indicate to the controller that the DDRPHY has finished frequency change.
    - Set DDRCTL_SWCTL.sw_done to 1'b1.
31. Set GRF_CHA/CHB_DDRPHY_CON0[5] and GRF_CHA/CHB_DDRPHY_CON1[5] to 1'b1, then set GRF_CHA/CHB_DDRPHY_CON0[4] and GRF_CHA/CHB_DDRPHY_CON1[4] to 1'b1 to select DDRCTL's dfi_init_complete driven by DDR_GRF. This step is necessary because the following DDRPHY_MDLL_CON0.ctrl_dll_on=1 will pull dfi_init_complete low, which will cause DDRCTL abnormal.
32. Turn on DDRPHY master DLL by setting DDRPHY_MDLL_CON0.ctrl_dll_on=1'b1.
33. Start DDRPHY master DLL locking by enable DDRPHY_MDLL_CON0.ctrl_start
    - Set DDRPHY_MDLL_CON0.ctrl_start to 1'b0.
    - Set DDRPHY_MDLL_CON0.ctrl_start to 1'b1.
    - Wait until DDRPHY_MDLL_CON1.ctrl_locked=1'b1.
34. Set GRF_CHA/CHB_DDRPHY_CON0[4] and GRF_CHA/CHB_DDRPHY_CON1[4] back to 1'b0.
35. DDRPHY SFR settings. Set DDRPHY_LP_CON0.ctrl_scheduler_en to 1'b1 and other registers if necessary.
36. Start DDRPHY initial read and write training. Please refer to the following section for LPDDR4/4X training procedure.
37. DDRPHY SFR settings that should be set after training such as following registers and so on.
    - Set DDRPHY_MDLL_CON0.clkm_cg_en_sw to 1'b0.
    - Set DDRPHY_CAL_CON0.cal_vtc_en to 1'b1.
    - Set DDRPHY_CAL_CON5.wrtrn_cycle_mode=0 during normal operation.

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7.6.3 2-channel Interleaving LPDDR5 Initialization

Following steps are for 2-channel interleaving LPDDR5 initialization.

1. Power up DDRPHY core supply (DDRPHY_DVDD), power up CKE power (DDRPHY_CKE_VDDQ) and then power up IO supply (DDRPHY_CK_VDDQ and DDRPHY_VDDQ).
2. Keep DDRPLL (D0APLL and D1APLL) at default configuration to output 24MHz frequency. Configure DDRPLL (D0BPLL and D1BPLL) to lock at target operation frequency. Now by default the input clk_phy2x of DDRPHY is 24MHz. Make sure that PCLK frequency of DDRPHY is not higher than clk_dfi which is generated from clk_phy2x.
3. De-assert PRESETn of DDRPHY and present of DDRCTL.
4. De-assert RESETn of DDRPHY. Wait for at least 10 cycles of clk_phy2x.
5. Set DDR_GRF_CHA/CHB_PHY_CON0[3] and DDR_GRF_CHA/CHB_PHY_CON1[3] of DDR_GRF to 1'b1 to enable DDRPHY2XCLKGATE_ENABLE of each DDRPHY. Wait for at least 10 cycles of clk_phy2x.
6. De-assert div_rst_n of DDRPHY. Wait for at least 10 cycles of clk_phy2x.
7. Assert core_ddrc_rstn and aresetn_i(i=0~4)of DDRCTL.
8. De-assert rst_n of DDRPHY. Make sure that rst_n is released at 24MHz low frequency.
9. Set DDR_GRF_CHA/CHB_PHY_CON0[3] and DDR_GRF_CHA/CHB_PHY_CON1[3] of DDR_GRF to 1'b0 to disable DDRPHY2XCLKGATE_ENABLE of each DDRPHY.
10. Assert div_rst_n of DDRPHY.
11. Set DDRPHY registers to select memory type and clock mode. Following configuration are for 1:1:4 mode (CLK_DFI: CK: WCK).
    - DDRPHY_GNR_CON0.ctrl_ddr_mode='h2
    - DDRPHY_CLKMODE_CON.ctrl_phy_mode='h4
    - DDRPHY_CLKMODE_CON.ctrl_phy_clk_2x='h1

    If CLK_DFI: CK: WCK is 1:1:2, following configuration should be followed.
    - DDRPHY_GNR_CON0.ctrl_ddr_mode='h2
    - DDRPHY_CLKMODE_CON.ctrl_phy_mode='h2
    - DDRPHY_CLKMODE_CON.ctrl_phy_clk_2x='h1
12. De-assert div_rst_n of DDRPHY.
13. Excutes step 5 again to enable the output clk_dfi of DDRPHY. Clk_dfi is used as the source clock of DDRCTL. It is connected to the core_ddrc_core_clk, aclk_i(i=0~4) and bsm_clk of DDRCTL.
14. De-assert presetn of DDRCTL.
15. Set DDRCTL registers.
16. De-assert core_ddrc_rstn and aresetn_i(i=0~4) of DDRCTL.
17. Disable auto-refreshes, self-refresh, power down and assertion of dfi_dram_clk_disable by setting DDRCTL_RFSHCTL0.dis_auto_refresh = 1, DDRCTL_PWRCTL.powerdown_en = 0 and DDRCTL_PWRCTL.selfref_en = 0, DDRCTL_PWRTL.en_dfi_dram_clk_disable = 0.
18. Set DDRCTL_SWCTL.sw_done to 1'b0.
19. Set DDRCTL_DFIMISC.dfi_init_complete_en to 1'b0.
20. Set DDRCTL_SWCTL.sw_done to 1'b1.
21. Set DDRCTL_PORTi_PCTRL.port_en(i=0~4) to 1'b1 to enable AXI port 0~4 of DDRCTL.
22. Begin to set DDRPHY registers. Such as read latency, write latency and burst length and so on.
23. Apply DDRPHY IO settings before ZQ calibration.
24. DDRPHY DLL lock value force and update for low frequency initialization under 100MHz.
    - Set DDRPHY_MDLL_CON0.ctrl_force=11'h2ef.
    - Set DDRPHY_MDLL_CON0.ctrl_dll_on=1'b0.
25. Start DFI initialization
    - Set DDRPHY_MDLL_CON0.ctrl_dll_on=1'b0
    - DDRCTL should assert dfi_init_start from low to high
    - DDRCTL should wait dfi_init_complete change from low to high
26. Set DDRCTL_MRCTRL0=32'h8 to enable software intervention allowed before SDRAM automatic initialization.
27. Set DDRCTL_SWCTL.sw_done to 1'b0. Set DDRCTL_DFIMISC.dfi_init_start to 1'b0 and DDRCTL_DFIMISC.dfi_init_complete_en to 1'b1. Set DDRCTL_SWCTL.sw_done to 1'b1.

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28. Delay an appropriate period of time according to the DDRCTL_INITTMG1.dram_rstn_x1024 to issue power down exit asynchronously by programming following registers.
Set DDR_GRF_CHA_CON2[7:0] and DDR_GRF_CHB_CON2[7:0] of DDR_GRF to 8'hff to toggle LPDDR5 chip select signal(CS) from 1'b0 to 1'b1.
Set DDR_GRF_CHA_CON2[7:0] and DDR_GRF_CHB_CON2[7:0] of DDR_GRF to 8'h00 to toggle LPDDR5 chip select signal(CS) from 1'b1 to 1'b0.
29. Start memory initialization by DDRCTL by sending MRW command.
30. Wait for DDRCTL to move to normal operating mode by monitoring DDRCTL_STAT.operating_mode register.
31. DDRPHY vref related registers settings without vref training.
32. DDRPHY ODT related registers settings.
33. Start DDRPHY ZQ calibration.
- Enable DDRPHY_ZQ_CON0.zq_clk_div_en
- Enable DDRPHY_ZQ_CON0.zq_manual_str
- Wait until DDRPHY_ZQ_CON1.zq_done is enabled
- Disable DDRPHY_ZQ_CON0.zq_manual_str
- Disable DDRPHY_ZQ_CON0.zq_clk_div_en

34. Frequency change to the target operation speed. Using frequency change protocol via MC-PHY handshake.
- Set DDRCTL_SWCTL.sw_done to 1'b0.
- Set DDRCTL_DFIMISC.dfi_init_complete_en to 1'b0.
- Set DDRCTL_DFIMISC.dfi_init_start to 1'b1. Set DDRCTL_SWCTL.sw_done to 1'b1.
- Poll DDRCTL_DFISTAT.dfi_init_complete=1'b0.
- Programming DDR_GRF_CHA/CHB_PHY_CON0[3] and DDR_GRF_CHA/CHB_PHY_CON1[3] of DDR_GRF to 1'b0 to disable DDRPHY2XCLKGATE_ENABLE of each DDRPHY.
- Assert div_rst_n of DDRPHY if LPDDR5 is used. If LP4/4X is used, don't assert div_rst_n.
- Change clk_phy2x frequency of DDRPHY channel 0 by setting DDR0CRU_CLKSEL_CON00[0] to 1'b1 to select D0BPLL, set DDR1CRU_CLKSEL_CON00[0] to 1'b1 to select D1BPLL output clock as DDRPHY channel 1 driving clock.
- Change PCLK of DDRPHY to high frequency such as 200MHz.
- De-assert div_rst_n of DDRPHY if LPDDR5 is used. If LP4/4X is used, skip this flow.
- Set DDR_GRF_CHA/CHB_PHY_CON0[3] and DDR_GRF_CHA/CHB_PHY_CON1[3] of DDR_GRF to 1'b1 to enable DDRPHY2XCLKGATE_ENABLE of each DDRPHY.
- Set DDRCTL_SWCTL.sw_done to 1'b0. Set DDRCTL_DFIMISC.dfi_init_start to 1'b0. Set DDRCTL_SWCTL.sw_done to 1'b1.
- Poll DDRCTL_DFISTAT.dfi_init_complete=1'b1.
- Set DDRCTL_SWCTL.sw_done to 1'b0.
- Set DDRCTL_DFIMISC.dfi_init_complete_en to 1'b1 to indicate to the controller that the DDRPHY has finished frequency change.
- Set DDRCTL_SWCTL.sw_done to 1'b1.

35. Set GRF_CHA/CHB_DDRPHY_CON0[5] and GRF_CHA/CHB_DDRPHY_CON1[5] to 1'b1, then set GRF_CHA/CHB_DDRPHY_CON0[4] and GRF_CHA/CHB_DDRPHY_CON1[4] to 1'b1 to select DDRCTL's dfi_init_complete driven by DDR_GRF. This step is necessary because the following DDRPHY_MDLL_CON0.ctrl_dll_on=1 will pull dfi_init_complete low, which will cause DDRCTL abnormal.
36. Turn on DDRPHY master DLL by setting DDRPHY_MDLL_CON0.ctrl_dll_on=1'b1.
37. Start DDRPHY master DLL locking by enable DDRPHY_MDLL_CON0.ctrl_start
- Set DDRPHY_MDLL_CON0.ctrl_start to 1'b0.
- Set DDRPHY_MDLL_CON0.ctrl_start to 1'b1.
- Wait until DDRPHY_MDLL_CON1.ctrl_locked=1'b1.

38. Set GRF_CHA/CHB_DDRPHY_CON0[4] and GRF_CHA/CHB_DDRPHY_CON1[4] back to 1'b0.
39. DDRPHY SFR settings.

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- Set DDRPHY_LP_CON0.wck_enable=1'b1.
- Set DDRPHY_LP_CON0.ctrl_scheduler_en=1'b1.
- Set DDRPHY_LP_CON0.ctrl_dqs_drv_off=1'b1 if write link ECC is disabled.
- Set DDRPHY_GNR_CON0.wdqs_oen_mode=1'b1.

40. Set DDRPHY wck_adj, rwck_adj, wckdur_adj, rwckdur_adj properly. Set gate/read settings properly.
41. Start DDRPHY initial training. Please refer to the following section for LPDDR5 training procedure.
42. Please set WCK_MODE_APB before memory normal operation.
If WCK always on mode is enabled, set
DDRPHY_WCK2CKSYNC_CON0.WCK_MODE_APB=2'b1 and
DDRPHY_SCHD_CMD_CON0.CAS_EN_APB=1'b0. If WCK always on mode is disabled, set
DDRPHY_WCK2CKSYNC_CON0.WCK_MODE_APB=2'b0 and
DDRPHY_SCHD_CMD_CON0.CAS_EN_APB=1'b1.

7.6.4 LPDDR4/4X Training Procedure

Please apply the following steps before memory initialization if training are required.
Controller should not assert dfi_ctrlupd_req during training.

- Settings before training
  - Set DDRPHY_OFFSETD_CON0.upd_mode=1'b0 for PHY-initiated update mode.
  - Write current frequency to DDRPHY_DVFS_CON.freq_train
  - Initial Vref setting.
  - Set DDRPHY_MDLL_CON0.clkm_cg_en_sw=1'b1 to freeze DLL lock value during training for stability.
- Command bus training
- On-Die Termination
- Apply one of the following DQS cleaning options.
  - Auto DQS clean mode
  - IO RCV Single-Ended mode
- Read DQ training
- Write DQ training
- Save the training result to read and save training registers for PHY power in/off scenario.
- Initial training at lower frequency if necessary.
- The PHY should start the periodic training to compensate DRAM voltage/temperature variation followed by periodic training guide.

7.6.4.1 LPDDR4/4X Command Bus Training

DDRPHY supports 2 command bus training modes for LPDDR4/4X. That is SW command bus training mode and HW command bus training mode.
Following steps are for SW command bus training mode.

- Change to low frequency (under 200MHz).
- Set DDRPHY_LP_CON0.ds_io_pd=1'b0.
- Apply DQS offset.
  - DDRPHY_CAL_CON3.wrlvl_sw_mode=1'b1.
  - DDRPHY_WR_LVL_CON0.ctrl_wrlvl*_code=ck_offset (ck_offset=91ps/tFS, tFS: finedelay).
  - Enable DDRPHY_OFFSETD_CON0.ctrl_resync.
  - Disable DDRPHY_OFFSETD_CON0.ctrl_resync.
  - DDRPHY_CAL_CON3.wrlvl_sw_mode=1'b0.
- Controller should configure memory (LPDDR4/4X) in common bus training mode. Issue MRW-1 command followed by MRW-2 command to set MR13 OP[0]=1'b1 (command bus training mode enabled).
- After tMRD, configure DDRPHY in command bus training mode.
  - Set DDRPHY_CAL_CON0.ca_cal_mode=1'b1.
  - Set DDRPHY_CBT_CON0.cbt_vref_dqs_en=1'b1.
  - After tDQSCKE, set DDRPHY_CBT_CON3.cbt cke=2'b0.
- After tCKELCK, change CK frequency to the highest operating frequency.
- Configure CA Vref setting.

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- Set DDRPHY_CBT_CON0.cbt_ca_vref=CA Vref setting value(MR12 OP[6: 0]).
- Set DDRPHY_CAL_CON3.wr_sw_mode=1'b1.
- Set DDRPHY_WR_LVL_CON2.ctrl_dqs_shift=1'b1.
- After tCAENT(20ns), set DDRPHY_CBT_CON0.cbt_vref_dq_en=1'b1 to drive CA vref setting value on DQ.
- Wait until DDRPHY_CBT_CON5.cbt_tDSTRAIN+ DDRPHY_CBT_CON5.cbt_tDHTRAlN+6 DFI clock cycle.
- Set DDRPHY_CBT_CON0.cbt_vref_dq_ en=1'b0.
- Set DDRPHY_WR_LVL CON2.ctrl dqs shift=1'b0.
- Set DDRPHY_CAL_CON3.wr_sw_mode=1'b0.
- Wait for tVREF_LONG(250ns max).
- Set DDRPHY_CBT_CON0.cbt_sw_mode=1'b1.

- Run command bus training (CA training/CS fine training) as followings.

```
Following are function definition.
APB_READ(REG_NAME.field_name)
APB_WRITE(REG_NAME.field_name,VAL)
UPD_CODE{
APB_WRITE(DDRPHY_OFFSETD_CON0.ctrl_resync, 1b1)//Update code
APB_WRITE(DDRPHY_OFFSETD_CON0.ctrl_resync, 1 b0)//Update code
}
WAIT_UPD{
Wait(1us)
}
PATTERN_GEN (REG_NAME.field name){
APB_WRITE(REG_NAME.field_name, 1b1)
APB_WRITE(REG_NAME.field_name, 1b0)
}
PATTERN_CLEAR{
APB_WRITE(DDRPHY_CBT_CON3.cbt_cmd_clear, 1 b1)
APB_WRITE(DDRPHY_CBT_CON3.cbt_cmd_clear, 1'b0)
}
RD_FEEDBACK{
DQ_IO_RD=APB_READ(DDRPHY_DO_IO_RDATA0.DQ_IO_RD1)
}
Lock_value=APB_READ(DDRPHY_MDLL_CON1.ctrl_lock_value)
1. Apply CK/CS offset(OFFSET=91ps/tFS, tFS: finestep delay)
APB_WRITE(DDRPHY_CA_DESKEW_CON4.CKDeSkewCode, OFFSET)
APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS0DeSkewCode, OFFSET)
UPD_CODE
2. CA training
1) Searching CA_VWML[K] (k=0, 1.2...5)
for(search='h0; search<'h2FF; search++){
APB_WRITE(CAkDeSkewCode, search)
UPD CODE
WAIT_UPD
PATTERN_GEN(DDRPHY_CBT_CON3.cbt_cmd_ca_vwml)
RD_FEEDBACK
if(DDRPHY_DQ_IO_RD[K])!=1'b1){
    CA_VWML[k]=search-1
    break
}
}
2) Searching CA_VWMR[k](k=0, 1, 2..5)
for(search='h0; search<`h2FF; search++){
APB_WRITE(DDRPHY_CA_DESKEW_CON*.CAkDeSkewCode, search)
UPD_CODE
WAIT_UPD
```

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```
PATTERN_GEN(DDRPHY_CBT_CON3.cbt_cmd_ca_vwmr)
RD_FEEDBACK
if(DQ_IO RD[K]==1'b1){
CA_VWMR[K]= Lock_value-search
break
}
    }
3) Calculation & Update(k=0, 1, 2…5)
if(CA_VWML[K]>CA_VWMR[K]){
CA_VWMC[K]=(CA_VWML[k]-CA_VWMR[k])/2
}
    else { CA_VWMC[K]='h0}
    APB_WRITE(CAkDeSkewCode, CS_VWMC[k])
UPD_CODE
3. CS Fine training
1) Searching CS_VWML_FINE
for(search='h0; search<'h2FF; search++){
APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS0DeSkewCode, search)
UPD_CODE
WAIT_UPD
PATTERN_GEN(DDRPHY_CBT_CON3.cbt_cmd_cs_vwml_fine)
RD_FEEDBACK
if(DQ_IO_RD!=6'b111111){
CS_VWML_FINE=search-1
break
}
PATTERN CLEAR
    }
2) Searching CS_VWMR_FINE
for(search='h0; search<'h2FF; search++){
APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS0DeSkewCode, search)
UPD_CODE
WAIT_UPD
PATTERN_GEN(DDRPHY_CBT_CON3.cbt_cmd_cs_vwmr_fine)
RD_FEEDBACK
    If(DQ_IO_RD==6'b111111){
CS_VWMR_FINE=Lock_value-search
break
}
        PATTERN_CLEAR
    }
3) Calculation & Update
if(CS_VWML_FINE>CS_VWMR FINE){
CS_VWMC_FINE=(CS_VWML_FINE-CS_VWMR_FINE)/2
}
else {
 CS_VWMC_FINE='h0
}
APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS0DeSkewCode, CS_VWMC_FINE)
UPD_CODE
APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS1DeSkewCode, CS_VWMC_FINE)
UPD_CODE
```

If two ranks are used, CS1DeSkewCode should be applied by training result of CS0 (CS0DeSkewCode).

- Exit command bus training.
  - Set DDRPHY_CBT_CON3.cbt_cke= 2'b11
  - Wait for tCKEHDQS.

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- Set DDRPHY_CBT_CON0.cbt_vref_dqs_en=1'b0.
- Set DDRPHY_CAL_CON0.ca_cal_mode=1'b0.
- Set DDRPHY_CBT_CON0.cbt_sw_mode=1'b0.
- After tFC(20ns), memory controller should configure memory(LPDDR4/4X)in normal mode.

Following steps are for HW command bus training mode.

- Change to the low frequency (under 200MHz)
- Set DDRPHY_LP_CON0.ds_io_pd=1'b0.
- Set DDRPHY_CAL_CON0.ca_swap_mode_dis=1'b1.
- Apply DQS offset
  - DDRPHY_CAL_CON3.wrlvl_sw_mode=1'b1
  - DDRPHY_WR_LVL_CON0.ctrl_wrlvl*_code =ck_offset(ck_offset=91ps/tFS, tFS: finedelay).
  - Enable DDRPHY_OFFSETD_CON0.ctrl_resync.
  - Disable DDRPHY_OFFSETD_CON0.ctrl_ resync.
  - DDRPHY_CAL_CON3.wrlvl_sw_mode=1'b0.
- Controller should configure memory(LPDDR4/4X)in command bus training mode. Controller should issue MRW-1 command followed by MRW-2 command to set MR13 OP[0]=1'b1(command bus training mode enabled).
- After tMRD, configure DDRPHY in command bus training mode.
  - Enable DDRPHY_CAL CON0.ca_cal_mode.
  - Set DDRPHY_CBT_CON0.cbt_vref_dqs_en as 2'b01.
  - After tDQSCKE, set DDRPHY_CBT_CON2.cbt_cke as 2'b00.
- After tCKELCK, change CK frequency to the highest operating frequency.
- Configure CA Vref setting
  - Set CA Vref setting value(MR12 OP[6:0]) in DDRPHY_CBT_CON0.cbt_ca_vref.
  - Enable DDRPHY_CAL_CON3.wr_sw_mode.
  - Set DDRPHY_WR_LVL_CON2.ctrl_dqs_shift=1'b1.
  - After tCAENT(20ns), set DDRPHY_CBT_CON0.cbt_vref_dq_en as 2'b01 to drive CA vref setting value on DQ.
  - Wait until DDRPHY_CBT_CON5.cbt_tDSTRAIN+ DDRPHY_CBT_CON5.cbt_tDHTRAIN+6 DFI clock cycle.
  - Set DDRPHY_CBT_CON0.cbt_vref_dq_en as 2'b00.
  - Set DDRPHY_WR_LVL_CON2.ctrl_dqs_shift=1'b0.
  - Disable DDRPHY_CAL_CON3.wr_sw_mode.
  - Wait for tVREF_LONG(250ns max).
- Start CS/CA calibration.
  - Apply CK/CS offset.
    Enable DDRPHY_CBT_CON0.cbt_sw_mode.
    Set DDRPHY_CA_DESKEW_CON4.CKDeSkewCode=ck_offset(ck_offset=91ps/tFS, tFS: finedelay).
    Set DDRPHY_CA_DESKEW_CON5.CS0DeSkewCode=ck_offset(ck_offset=91ps/tFS, tFS: finedelay).
    Enable DDRPHY_OFFSETD_CON0.ctrl_resync.
    Disable DDRPHY_OFFSETD_CON0.ctrl_resync.
    Disable DDRPHY_CBT_CON0.cbt_sw_mode.
  - Enable DDRPHY_LP_CON0.scheduler_HW_clock_gating_disable.
  - Enable DDRPHY_LP_CON0.ctrl_scheduler_en.
  - Enable DDRPHY_CBT_CON0.cbt_cs_coarse_dis.
  - Enable DDRPHY_CBT_CON3.cbt_hw_cal_start.
  - Wait until DDRPHY_CBT_CAL_STAT0.cbt_hw_cal_done.
  - Disbale DDRPHY_LP_CON0.ctrl_scheduler_en.
  - Disable DDRPHY_LP_CON0.scheduler_HW_clock_gating_disable.
- Exit command bus training.
  - Set DDRPHY_CBT_CON2.cbt_cke as 2'b11.
  - Wait for tCKEHDQS.
  - Set DDRPHY_CBT_CON0.cbt_vref_dqs_en as 2'b00.

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- Set DDRPHY_CAL_CON0.ca_cal_mode to 1'b0.
- Disable DDRPHY_CBT_CON3.cbt_hw_cal_start.
- After tFC(20ns), memory controller should configure memory (LPDDR4/4X) in normal mode.

7.6.4.2 LPDDR4/4X DQS Clean Procedure

1. Auto DQS clean mode

The goal of auto DQS clean mode is to get valid read DQS without the gate training. Auto DQS clean mode can be used if VSSQ termination is enabled.

- Set DDRPHY_TESTIRCV_CON0.dqs0_testircv=4'h3, DDRPHY_TESTIRCV_CON0.dqs1_testircv=4'h3.
- Set DDRPHY_CAL_CON0.gate_cal_mode=1'b0.
- Enable DDRPHY_CAL_CON3.auto_dqs_clean.
- Set DDRPHY_CAL_CON2.ctrl_rodt_disable=1'b0.

2. DQS Clean Using IO RCV Single-Ended(SE) mode on VSSQ Termination (Mandatory under 2133Mbps)

The goal of DQS clean using IO RCV SE mode is to get valid read DQS without the gate training and auto DQS clean on VSSQ termination on. It is allowed under 2133Mbps and IO RCV SE mode and RCV ODT should be enabled.

7.6.4.3 LPDDR4/4X Read DQ Calibration

Read DQ calibration adjusts DQS and DQ delay to compensate the skew introduced by the package, board and on-chip to maximize the setup and hold timing margin.

- Configure DDRPHY training pattern registers in DDRPHY_CAL_RD_PATTERN_CON0.
  - Set rdtrn_inv_pattern_ds0=0xee, rdtrn_inv_pattern_ds1=0xee, rdtrn_rddata_pattern0=0x55 and rdtrn_rddata_pattern1=0x55.
  - Configure DDRPHY_OP_CODE_RDC registers for MR32, MR40, MR20 and MR15 such that the training pattern output from DRAM is the same as the training pattern defined above.
  - Configure MR32, MR40, MR25 and MR15 for read training pattern. OP_CODE_PATA=0x55(=rdtrn_rddata_pattern0), OP_CODE_PATB =0x55(=rdtrn_rddata_pattern1), OP_CODE_INVA=0xee(=rdtrn_inv_pattern_ds0), OP_CODE_INVB=0xee(=rdtrn_inv_pattern_ds1).
  - rdtrn_inv_pattern should be the same per BYTE.
  - Based on the DDRPHY_OP_CODE* values, DDRPHY will send MRW for MR31, MR32, MR3 and MR34 to DRAM at the beginning of Read training.
- Configure DDRPHY in read training mode.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_rdtrn_en=1'b1.
  - Set SCHD_TRAIN_CON0.phy_rdtrn_rank_en properly. For example, if phy_rdtrn_rank_en is set to 2'b11, per-rank read training will start from rank-0 to rank-1 sequentially. Any rank can be enabled for read training. For example, it is possible to set phy_rdtrn_rank_en= 2'b10.

Caution: For Read DQ's setup/hold margin maximization, read DQ delay should bigger than read DOS delay.

Caution: Pattern configuration is an example. Training pattern can be changed by user selection.

7.6.4.4 LPDDR4/4X Write DQ Calibration Initiated by DDRPHY

Write DQ calibration adjusts for the delays introduced by the memory (tDQS2DQ), package, board and on-chip that impact the write cycle.

Normal Initial Training Setting (533MHz or more)

- If data mask and DBI are all disabled at DRAM, set DDRPHY_CAL_CON0.wrtrn_dbi_cal_en=1'b0. Otherwise, set to 1'b1.
- If current frequency is equal or greater than 1066MHz
  - Set DDRPHY_CAL_CON5.wrtrn_cyc_en=1 and DDRPHY_CAL_CON5.wrtm_cyc_mode=0 (High frequency cycle based training mode).
  - Set DDRPHY_CAL_CON5.wrtrn_cyc_th=0x1f.
- If current frequency is less than 1066MHz and equal to or greater than 533MHz, set

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- DDRPHY_CAL_CON5.wrtrn_cyc_en=1 and DDRPHY_CAL_CON5.wrtm_cyc_mode=1 (Low frequency cycle based training mode).
- Increase DDRPHY_CAL_CON4.num_repeat to make the initial training result stable.
- Set DDRPHY_CAL_CON4.wrtrn_multi_pattern to 1, to use more patterns during the initial training. Additional patterns should be defined in DDRPHY_CAL_WR_PATTERN2_CON0~4, DDRPHY_CAL_WR_PATTERN3_CON0~4, DDRPHY_CAL_WR_PATTERN4_CON0~4.
- DDRPHY_CAL_CON5.wrtm_cyc_mode should be 0 during normal operation.

Low Frequency Initial Training Setting (under 533MHz)-

- Set DDRPHY_CAL_CON0.dvfs_wr_train_en=0x1.
- Set DDRPHY_CAL_CON4.dvfs_wr_start_adj=0x0.
- Set DDRPHY_CAL_CON5.wrtm_cyc_en=0.
- After low frequency write training is done, apply the following setting.
  - Store the current lockvalue/4 value.
  - Store write training results from DDRPHY_WR_DESKEWC_CS*_CON*, DDRPHY_DM_DESKEWC_CS*_CON*.
  - Write (stored write training result values+lockvalue*2/4 value) to the following registers.
    - Enable DDRPHY_CAL_CON0.wr_cal_mode.
    - Enable DDRPHY_CAL_CON3.wr_sw_mode.
    - DDRPHY_SW_WR_DESKEWC_CS*_CON, DDRPHY_SW_DM_DESKEWC_CS*_CON*.
    - Disable DDRPHY_CAL_CON3.wr_sw_mode.
    - Enable DDRPHY_OFFSETD_CON0.ctrl_resync.
    - Disable DDRPHY_OFFSETD_CON0.ctrf_resync.
- Restore DVFS write training related setting for successful DVFS write training or other initial write training.
  - Set DDRPHY_CAL_CON4.dvfs_wr_slart_adj=0xf.
  - Set DDRPHY_CAL_CON0.dvfs_wr_train_en=0.

Common Setting for Write Training

- Set write training paltem
  - DQ pattern in DDRPHY_CAL_WR_PATTERN1_CON0~ DDRPHY_CAL_WR_PATTERN1_CON3.
- Set wrtrn_rddata_adj_w0_bst1_8 for BL1~BL2 pattern.
- Set wrtrn_rddata_adj_w1_bst1_8 for BL3~BL4 pattern.
- Set wrtm_rddata_adj_w2_bst1_8 for BL5~BL6 pattern.
- Set wrtrn_rddata_adj_w3_bst1_8 for BL7~BL8 pattern.
- Set wrtm_rddata_adj_w0_bst9_16 for BL9~BL10 pattern.
- Set wrtrn_rddata_adj_w1_bst9_16 for BL11~BL12 pattern.
- Set wrtm_rddata_adj_w2_bst9_16 for BL13-BL14 pattern.
- Set wrtrn_rddata_adj_w3_bst9_16 for BL15~BL16 pattern.
- Set write DM pattern in CAL_WR_PATTERN1_CON4.
- Set wrtrn_rddata_dm_adj_w0_bst1_8 for BL1~BL2 pattern.
- Set wrtrn_rddata_dm_adj_w1_bst1_8 for BL3~BL4 pattern.
- Set wrtrn_rddata_dm_adj_w2_bst1_8 for BL5~BL6 pattern.
- Set wrtrn_rddata_dm_adj_w3_bst1_8 for BL7~BL8 pattern.
- Set wrtrn_rddata_dm_adj_w0_bst9_16 for BL9~BL10 pattern.
- Set wrtrn_rddata_dm_adj_w1_bst9_16 for BL11~BL12 pattern.
- Set wrtrn_rddata_dm_adj_w2_bst9_16 for BL13~BL14 pattern.
- Set wrtrn_rddata_dm_adj_w3_bst9_16 for BL15~BL16 pattern.
- Configure DDRPHY in write training mode.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_wrtrn_en=1.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_wrtrn_rank_en properly.
  - For example, if phy_wrtrn_rank_en is set to 0x3, per-rank write training will start from rank0 to rank1 sequentially.

7.6.4.5 LPDDR4/4X Periodic Training

Periodic training using PHY master interface

Periodic write training compensates write center shift and gate shift caused by VT variation in memory. Initial training should be completed before periodic training. During periodic training, DDRPHY uses the PHY master interface and generates MPC commands without the memory controller. When DDRPHY request PHY master mode, the controller should place the DRAM in self refresh and assert dfi_phymstr_ack. Periodic write training will be executed in sequence.

- The common parameter is same as initial training.
- Enable periodic gate training properly (refer to SFR description)
  - Set DDRPHY_SCHD_TRAIN_CON0.periodic_gttrn_en and if use DVFS, set DDRPHY_DVFS0_TRAIN_CON0.dvfs0_periodic gttrn_en and DDRPHY_DVFS1_TRAIN_CON0.dvfs1_periodic_gttrn_en.
- Enable periodic write training properly. Mandatory up to 2133Mbps.
  - Set DDRPHY_SCHD_TRAIN_CON0.periodic_wrtrn_en and if use DVFS, set DDRPHY_DVFS0_TRAIN_CON0.dvfs0_periodic_wrtrn_en and DDRPHY_DVFS1_TRAIN_CON0.dvfs1_periodic_wrtrn_en.
- Set DDRPHY_SCHD_TRAIN_CON1.periodic_time.
  - Interval of periodic training = periodic_time*tCK_osc (oscillator dock).
- Set DDRPHY_SCHD_TRAIN_CON1.periodic_en =1 and if use DVFS, set DDRPHY_DVFS0_SCHD_TIME_CON3.dvfs0_periodic_en and DDRPHY_DVFS1_SCHD_TIME_CON3.dvfs1_periodic_en properly.
- Set DDRPHY_SCHD_TRAIN_CON1.periodic en = 0 for disable periodic training and if use DVFS, set DDRPHY_DVFS0_SCHD_TIME_CON3.dvfs0_periodic_en and DDRPHY_DVFS1_SCHD_TIME_CON3.dvfs1_periodic_en properly.

DVFS training using PHY master interface

DVFS training compensates write center shift and gate shift caused by VT variation in memory. Initial write/gate training should be completed before DVFS training. During DVFS training, DDRPHY uses the PHY master interface and generates MPC commands without the memory controller. When DDRPHY request PHY master mode, the controller should place the DRAM in self refresh and assert dfi_phymstr_ack. DVFS training will be executed in sequence.

- The common parameter is same as initial training.
- Enable DVFS gate training properly
  - Set DDRPHY_SCHD_TRAIN_CON0.dvfs_gttrn_en and if use DVFS, set DDRPHY_DVFS0_SCHD_TIME_CON3.dvfs0_dvfs_gttrn_en and DDRPHY_DVFS1_SCHD_TIME_CON3.dvfs1_dvfs_gttrn_en.
- Enable DVFS write training properly.
  - Set DDRPHY_SCHD_TRAIN_CON0.dvfs_wrtrn_en and if use DVFS, set DDRPHY_DVFS0_SCHD_TIME_CON3.dvfs0_dvfs_wrtrn_en and DDRPHY_DVFS1_SCHD_TIME_CON3.dvfs1_dvfs_wrtrn_en.
- Set DDRPHY_CAL_CON0.dvfs_wr_train_en=1(DVFS mode).

7.6.5 LPDDR5 Training Procedure

Settings before training.

- Set DDRPHY_OFFSETD_CON0.upd_mode=0 for PHY-initiated update mode.
- Write the current frequency to DDRPHY_DVFS_CON.freq_train.
- Initial Vref setting.
- Set DDRPHY_MDLL_CON1.clkm_cg_en_sw=1 to freeze DLL lock value during training for stability.

Before DRAM interface training, training setting should be configured properly.

- LP5 SW CBT (command bus training)
- Auto DQS clean
- Read Calibration
- Write DQ Calibration

To set DDRPHY training under 1600Mbps at MODE4/3, under 1067Mbps at MODE2, DDRPHY training need WCK2CK sync always on mode and DDRPHY_WCK2CKSYNC_CON0.ctrl_WCK_MODE_APB=1. So please follow the DDRPHY training procedure below.

Set MR18 OP[4]=0(always on disable), CAS_EN=1, WCK_MODE=0 ==> CBT/WCK2CK

leveling(if needed) ==> set MR18 OP[4]=1(always on), CAS_EN=0,WCK_MODE=1 ==> Send CAS command to memory ==> set dfi_wck_en always 1 ==> DDRPHY training except CBT, WCK2CK leveling (if needed) ==> User choice for WCK2CK sync operation (if use wck2ck sync always on, please keep it or if not, set MR18 OP[4]=0(always on disable), CAS_EN=1,WCK_MODE=0 ==>Do normal transactions.
After training setting is done, apply the following sequence.

- Configure common parameter training properly.
  - Set DDRPHY_SCHD_TIME_CON0.phy_t_rddata_en='d6.
  - Set DDRPHY_SCHD_TIME_CON0.WL to match it with DRAM WL setting.
  - Set DDRPHY_SCHD_TIME_CON1.tCCD=0x8(LPDDR5).
  - Set DDRPHY_SCHD_TIME_CON1.tWTR=0x1f.
  - If WCK always on disable, set DDRPHY_WCK2CKSYNC_CON0.ctrl_WCK_MODE_APB=0x0 and DDRPHY_SCHD_CMD_CON0.CAS_EN_APB=0x1.
  - If WCK always on, set WCK2CKSYNC_CON0.ctrl_WCK_MODE_APB=0x1 and SCHD_CMD_CON0.CAS_EN_APB=0x0.
  - WCK should be driven by memory controller at WCK always on mode.
- Set MR operand code same as setting on memory.
  - For LPDDR5, DDRPHY_LP5_MR_OP.
- Enable DDRPHY training mode.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_train_en=0x1.
- Wait until SCHD_TRAIN_CON0.phy_train_done=0x1.
- Disable DDRPHY training mode.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_train_en=0x0.
- Setting after training.
  - Set DDRPHY_MDLL_CON0.clkm_cg_en_sw=0 to enable DLL locking.
  - Set DDRPHY_CAL_CON5.wrtrn_cyc_mode=0 during normal operation.
  - Set DDRPHY_CAL_CON0.cal_vtc_en=1 to compensate voltage, temperature variation on calibration results.
  - Set DDRPHY_CAL_CON0.dvfs_wr_train_en=1 initial write training (Write training with dfi_lvl_periodic=0) will be interpreted as DVFS write training afterwards.
- Update DDRPHY DLL
  - Enable DDRPHY_OFFSETD_CON0.ctrl_resync.
  - Disable DDRPHY_OFFSETD_CON0.ctrl_resync.
- The DDRPHY should start the periodic training to compensate DRAM voltage/temperature variation followed by periodic training guide.
  - Write periodic training.

7.6.5.1 LPDDR5 Command Bus Training

LPDDR5 only supports SW command bus training mode. LPDDR5 SW command bus training supports CA bit de-skewing function. The overall sequence is CA left edge searching-CA right edge searching-Calculation center code of CA. Because LPDDR5 CA is DDR (CA is captured at CK rising edge and falling edge), the edge should be searched with changing CBT-PH mode. **Setting before Training**

- Before CBT training start, check if MR13 OP[6]=1 for CBT mode2.
- Set DDRPHY_SCHD_CMD_CON0.RANK_SEL=cs.
- Set DDRPHY_CBT_CON2.cbt_dqdm_sel=0x80.
- Set DDRPHY_CBT_CON0.cbt_sw_mode=0x1.
- Set DDRPHY_CBT_CON2.cbt_tWCK2DQ7 satisfying memory timing parameter tWCK2DQ7H.
- Set DDRPHY_CBT_CON2.cbt_tDSTRAIN_LP5 satisfying memory timing parameter tDStrain.

CA Left Edge Searching with CBT-PH[7]=1'b0

- Entering CBT Mode
  - Configure the memory entering CBT mode.
    - Set DDRPHY_SCHD_CON0.scheduler_sw_mode=0x1.
    - Set DDRPHY_CAL_CON0.ca_cal_mode=0x1.

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- Set DDRPHY_CBT_CON0.cbt_vref_dqs_en=0x1.
- Set DDRPHY_WCK2CKSYNC_CON0.wck_out_enable=0x1.
- Set DDRPHY_SCHD_CMD_CON2.MA_CODE=0x10.
- Set DDRPHY_SCHD_CMD_CON2.OP_CODE=0x10.
- Toggle DDRPHY_SCHD_DIRECT_CMD3.CMD_MWR_req.

- Configure the PHY entering CBT mode.
  - Set DDRPHY_CBT_CON0.cbt_vref_dq_en=0x1.
  - Set DDRPHY_CBT_CON2.cbt_start=0x1.
  - Wait for tDQ7HWCK+tDQ72DQ (255ns).
  - Set DDRPHY_CBT_CON2.cbt_wck_en=0x1.
  - Toggle DDRPHY_CBT_CON2.cbt_vref_set_en.
  - Set DDRPHY_CBT_CON2.cbt_dq_rcv_en=0x1.
  - Set DDRPHY_CBT_CON3.cbt_en=0x1.
  - Toggle DDRPHY_OFFSETD_CON0.ctrl_resync.

- Searching CA Left edge as followings.

```
APB_READ (REG_NAME[bit])
APB_WRITE (REG_NAME[bit],VAL)
UPD_CODE {
    APB_WRITE (DDRPHY_OFFSETD_CON0.ctrl_resync, 1'b1)
    APB_WRITE (DDRPHY_OFFSETD_CON0.ctrl_resync, 1'b0)
}
WAIT_UPD {
     Wait(1us)
}
PATTERN_GEN_1 {
     APB_WRITE (DDRPHY_SCHD_DIRECT_CMD1.DIRECT_CS_1, cs)
     APB_WRITE (DDRPHY_SCHD_DIRECT_CMD1.DIRECT_CS_2, 0x0)
     APB_WRITE (DDRPHY_SCHD_DIRECT_CMD1.DIRECT_CMD_1, {13'h0, ca, 1'h0,
     ~ca})
     APB_WRITE (DDRPHY_SCHD_DIRECT_CMD1. DIRECT_CMD_2, {13'h0, ~ca, 1'h0,
     ~ca})
     APB_WRITE (DDRPHY_SCHD_DIRECT_CMD0.DIRECT_EN_APB, 1'b1)
     Wait(1ns)
     APB_WRITE (DDRPHY_SCHD_DIRECT_CMD0.DIRECT_EN_APB, 1'b0)
}
RD_FEEDBACK {
    DQ_IO_RD = APB_READ (REG_NAME.field_name)
}
if(DDRPHY_CLKMODE_CON == 2)
offset =APB_READ (DDRPHY_MDLL_CON1.ctrl_lock_value)/2
if (DDRPHY_CLKMODE_CON == 4)
offset = APB_READ (DDRPHY_MDLL_CON1.ctrl_lock_value)
1. Apply CK offset and CS offset
APB_WRITE (DDRPHY_CA_DESKEW_CON4.CKDeSkewCode, offset)
APB_WRITE (DDRPHY_CA_DESKEW_CON5.CS*DeSkewCode, offset)
UPD_CODE
2. Searching CA left edge CA_VWML[k] (k = 0, 1, 2...6)
for(search='h0; search < 'h2FF; search++) {
    APB_WRITE (CAkDeSkewCode, search)
    UPD_CODE
```

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```
    WAIT_UPD
    PATTERN_GEN
    RD_FEEDBACK
    if (DQ_IO_RD[k]!=1'b1) {
        CA_VWML[k] = search-1
    break
    }
}
```

3. Rollback the CK offset and CS offset

```
APB_WRITE(DDRPHY_CA_DESKEW_CON4.CKDeSkewCode,0x0).
APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS*DeSkewCode,0x0).
UPD_CODE
```

- Exiting CBT mode
  - Configure the DDRPHY exiting CBT mode
    - Set DDRPHY_CBT_CON3.cbt_en = 0x0
    - Toggle DDRPHY_OFFSETD_CON0.ctrl_resync
    - Set DDRPHY_CBT_CON2.cbt_start =0x0
    - Set DDRPHY_CBT CON2.cbt_dq_rcv_en=0x0
    - WAIT for tDQ7LWCK + 10tCK
    - Set DDRPHY_CBT_CON2.cbt_wck_en=0x0
    - Wait tXCBT
  - Configure the memory exiting CBT mode.
    - Set DDRPHY_SCHD_CMD_CON2.MA_CODE=0x10.
    - Set DDRPHY_SCHD_CMD_CON2.OP_CODE = 0x00.
    - Toggle DDRPHY_SCHD_DIRECT_CMD3.CMD_MWR_req.
    - Set DDRPHY_CBT_CON0.cbt_vref_dq_en = 0x0.
    - Set DDRPHY_WCK2CKSYNC_CON0.wck_out_enable = 0x0.
    - Set DDRPHY_CBT_CON0.cbt_vref_dqs_en = 0x0.
    - Toggle DDRPHY_CBT_CON2.cbt_vref_pre_en.
    - Set DDRPHY_CAL_CON0.ca_cal_mode =0x0.
    - Set DDRPHY_SCHD_CON0.scheduler_sw_mode =0x0.

CA Right Edge Searching with CBT-PH[7] = 1'b1

- Entering CBT Mode
  - Configure the memory entering CBT mode.
    - Set DDRPHY_SCHD_CON0.scheduler_sw_mode = 0x1.
    - Set DDRPHY_CAL CON0.ca_cal_mode = 0x1.
    - Set DDRPHY_CBT_CON0.cbt_vref_dqs_en = 0x1.
    - Set DDRPHY_WCK2CKSYNC_CON0.wck_out_enable = 0x1.
    - Set DDRPHY_SCHD_CMD_CON2.MA_CODE= 0x10.
    - Set DDRPHY_SCHD_CMD_CON2.OP_CODE= 0x90.
    - Toggle DDRPHY_SCHD_DIRECT_CMD3.CMD_MWR_req.
  - Configure the DDRPHY entering CBT mode.
    - Set DDRPHY_CBT_CON0.cbt_vref_dq_en=0x1.
    - Set DDRPHY_CBT_CON2.cbt_start =0x1.
    - Wait for tDQ7HWCK +tDQ72DQ(255ns).
    - Set DDRPHY_CBT_CON2.cbt_wck_en =0x1.
    - Toggle DDRPHY_CBT_CON2.cbt_vref_set_en.
    - Set DDRPHY_CBT_CON2.cbt_dq_rcv_en = 0x1.
    - Set DDRPHY_CBT_CON3.cbt_en = 0x1.
    - Toggle DDRPHY_OFFSETD_CON0.ctrl_resync.
- Searching CA Right edge as followings.

```
APB_READ(REG_NAME[bit])
APB_WRITE(REG_NAME[bit],VAL)
UPD_CODE {
```

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```
    APB_WRITE(DDRPHY_OFFSETD_CON0.ctrl_resync,1'b1)
    APB_WRITE(DDRPHY_OFFSETD_CON0.ctrl_resync,1'b0)
}
WAIT_UPD {
    Wait(1us)
}
PATTERN_GEN_1 {
    APB_WRITE(DDRPHY_SCHD_DIRECT_CMD1.DIRECT_CS_1,cs)
    APB_WRITE(DDRPHY_SCHD_DIRECT_CMD1.DIRECT_CS_2,0x0)
    APB_WRITE(DDRPHY_SCHD_DIRECT_CMD1.DIRECT_CMD_1,{13'h0, ca, 1'b0,
~ca})
    APB_WRITE(DDRPHY_SCHD_DIRECT_CMD1.DIRECT_CMD_2,{13'h0, ~ca, 1'b0,
ca})
}
RD_FEEDBACK {
    DQ_IO_RD=APB_READ(REG_NAME.field_name)
}
if(CLKMODE_CON == 2)
    offset=APB_READ(DDRPHY_MDLL_CON1.ctrl_lock_value)/2
if(CLKMODE_CON == 4)
    offset=APB_READ(DDRPHY_MDLL_CON1.ctrl_lock_value)
1. Apply CK offset and CS offset.
APB_WRITE(DDRPHY_CA_DESKEW_CON4.CKDeSkewCode, offset)
APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS*DeSkewCode, offset)
UPD_CODE
2. Searching CA left edge CA_VWMR[k](k=0, 1, 2…6)
for(search='h0;search<'h2ff;search++){
    APB_WRITE(CAkDeSkewCode, search)
    UPD_CODE
    WAIT_UPD
    PATTERN_GEN
    RD_FEEDBACK
    if(DQ_IO_RD[k]==1'b1){
        CA_VWMR[k]=search-1
        break
        }
}
3. Rollback the CK offset and CS offset.
APB_WRITE(DDRPHY_CA_DESKEW_CON4.CKDeSkewCode,0x0)
APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS*DeSkewCode,0x0)
UPD_CODE
```

- Exiting CBT Mode
  - Configure the DDRPHY exiting CBT mode.
    - Set DDRPHY_CBT_CON3.cbt_en=0x0.
    - Toggle DDRPHY_OFFSETD_CON0.ctrl_resync.
    - Set DDRPHY_CBT_CON2.cbt_start=0x0.
    - Set DDRPHY_CBT_CON2.cbt_dq_rcv_en=0x0.
    - WAIT for tDQ7LWCK.

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- Set DDRPHY_CBT_CON2.cbt_wck_en=0x0.
- Wait tXCBT.

- Configure the memory exiting CBT mode.
  - Set DDRPHY_SCHD_CMD_CON2.MA_CODE=0x10.
  - Set DDRPHY_SCHD_CMD_CON2.OP_CODE=0x00.
  - Toggle DDRPHY_SCHD_DIRECT_CMD3.CMD_MWR_req.
  - Set DDRPHY_CBT_CON0.cbt_vref_dq_en=0x0.
  - Set DDRPHY_WCK2CKSYNC_CON0.wck_out_enable=0x0.
  - Set DDRPHY_CBT_CON0.cbt_vref_dqs_en=0x0.
  - Toggle DDRPHY_CBT_CON2.cbt_vref_pre_en.
  - Set DDRPHY_CAL_CON0.ca_cal_mode=0x0.
  - Set DDRPHY_SCHD_CON0.scheduler_sw_mode=0x0.

Calculation of CA Center Code

- MODE2
  - CA_VWMR_TMP[k]=Lock_value – CA_VWMR[k](k=0,1,2…6)
  - If CA_VWML[k]>=CA_VWMR_TMP[k], CA_VWMC[k]=(CA_VWML[k]-CA_VWMR_TMP[k])/2+Lock_value/2
  - Else, CA_VWMC[k]=Lock_value/2-((CA_VWMR_TMP[k]-CA_VWML[k])/2)
- MODE4
  - CA_VWMR_TMP[k]=2*Lock_value-CA_VWMR[k](k=0,1,2…6).
  - If CA_VWML[k]>=CA_VWMR_TMP[k], CA_VWMC[k]=(CA_VWML[k]-CA_VWMR_TMP[k])/2+Lock_value.
  - Else, CA_VWMC[k]=Lock_value-((CA_VWMR_TMP[k]-CA_VWML[k])/2).
- Update CA center code on
  - Write DDRPHY_CA_DESKEW_CON0~2.CAkDeSkewCode as CA_VWMC[k].
  - Set DDRPHY_CBT_CON3.cbt_en=0x1.
  - Toggle DDRPHY_OFFSETD_CON0.ctrl_resync.
  - Set DDRPHY_CBT_CON0.cbt_sw_mode=0x0.

7.6.5.2 LPDDR5 DQS Clean Procedure

Auto DQS Clean (Mandatory above 3200Mbps)

The goal of auto DQS clean mode is to get valid read DQS without the gate training. Auto DQS clean mode can be used if VSSQ termination is enabled.

- Set DDRPHY_TESTIRCV_CON0.dqs0_testircv=0x3, DDRPHY_TESTIRCV_CON0.dqs1_testircv=0x3.
- Set DDRPHY_CAL_CON0.gate_cal_mode=0x0.
- Enable DDRPHY_CAL_CON3.auto_dqs_clean.
- Set DDRPHY_CAL_CON2.ctrl_rodt_disable=0x0.

If auto DQS clean mode is enabled, RL should be minimum RL of below table or more. The memory post_amble duration should be 4.5tWCK static and preamble duration should be 2tWCK static, 2tWCK toggle or 4tWCK static.

Table 7-3 Minimum Read Latency for LPDDR5 Auto DQS Clean Enable

PHY mode	0	1	2	3	4
Memory Type	LPDDR4/4X		LPDDR5		

MinReadLatencyw/AutoDQSEnable	28CK	24CK	14CK(28WCK)	9CK(36WCK)	9CK(36WCK)

DQS Clean Using IO RCV Single-Ended (SE) Mode on VSSQ Termination (Mandatory under 3200Mbps)

The goal of DQS clean using IO RCV SE mode is to get valid read DQS without the gate training and auto DQS clean on VSSQ termination ON. It is allowed under 3200Mbps and IO RCV SE MODE and RCV ODT should be enabled.

7.6.5.3 LPDDR5 Read DQ Calibration

Read Calibration adjusts DQS and DQ delay to compensate the skew introduced by the package, board and on-chip to maximize the setup and hold timing margin.

- Configure PHY training pattern registers in CAL_RD_PATTERN_CON0.
  - Set rdtrn_inv_pattern_ds0=0xee, rdtrn_inv_pattern_ds1=0xee, rdtrn_rddata_pattern0=0x55 and rdtrn_rddata_pattern1=0x55.
  - Configure DDRPHY_OP_CODE_RDC registers for MR31, MR32, MR33 and MR34 such that the training pattern output from DRAM is the same as the training pattern defined above.
  - Configure MR31, MR32, MR33 and MR34 for read training pattern.
    - OP_CODE_PATA=0x55(rdtrn_rddata_pattern0), OP_CODE_PATB=0x55(rdtrn_rddata_pattern1), OP_CODE_INVA=0xee(rdtrn_inv_pattern_ds0), OP_CODE_INVB=0xee(rdtrn_inv_pattern_ds1).
    - Rdtrn_inv_pattern should be the same per BYTE.
    - Based on the OP_CODE_* values, PHY will send MRW for MR31, MR32, MR33 and MR34 to DRAM at the beginning of read training.
- Configure DDRPHY and memory in link ECC mode, if link ECC is enabled.
  - Configure memory in link ECC mode.
    - Issue MR3 command to set DBI-WR enabled and DBI-RD disabled.
    - Issue MR22 command to enable link ECC mode.
  - Configure DDRPHY in link ECC mode.
    - Set DDRPHY_CAL_CON0.rdtrn_dbi_cal_en =0x1.
    - Set DDRPHY_CAL CON3.ctrl_link_ecc_mode=0x1.

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- Configure DDRPHY in read training mode.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_rdtrn_en=1
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_rdtrn_rank_en properly.
    - For example, if phy_rdtrn_rank_en is set to 2'b11, per-rank read training will start from rank0 to rank1 sequentially.
    - Any rank can be enabled for read training. For example, it is possible to set phy_rdtrn_rank_en=2'b10.

7.6.5.4 LPDDR5 Write DQ Calibration

Normal Initial Training Setting (533MHz or More)

- If data mask and DBI are all disabled at DRAM, set DDRPHY_CAL_CON0.wrtrn_dbi_cal_en=0. Otherwise set to 1.
- Configure DDRPHY and memory in link ECC mode if link ECC is enabled.
  - Configure memory in link ECC mode.
    - Issue MR3 command to set DBI-WR enabled and DBI-RD disabled.
    - Issue MR22 command to enable link ECC mode.
  - Configure DDRPHY in link ECC mode.
    - Set DDRPHY_CAL_CON0.wrtrn_dbi_cal_en=0x1.
    - Set DDRPHY_CAL_CON3.ctrl_link_ecc_mode=0x1.
- If current frequency is equal to or greater than 1066MHz
  - Set DDRPHY_CAL_CON5.wrtrn_cyc_en=1 and DDRPHY_CAL_CON5.wrtrn_cyc_mode=0(High frequency cycle based training mode).
  - Set DDRPHY_CAL_CON5.wrtrn_cyc_th=31(LPDDR5).
  - If PRBS write training is to be enabled after write training is done
    - Set DDRPHY_MDLL_CON0.clkm_cg_en_sw=1
    - Read DDRPHY_MDLL_CON1.ctrl_lock_value
    - Set DDRPHY_CAL_CON5.wrtrn_cyc_th=ctrl_lock_value/4
    - Set DDRPHY_MDLL_CON0.clkm_cg_en_sw=0
- If current frequency is less than 1066MHz and equal to or greater than 533MHz, set DDRPHY_CAL_CON5.wrtrn_cyc_en=1 and DDRPHY_CAL_CON5.wrtrn_cyc_mode=1(Low frequency cycle based training mode).
- Increase DDRPHY_CAL_CON4.num_repeat to make the initial training result stable.
- Set DDRPHY_CAL_CON4.wrtrn_multi_pattern to 1 to use more patterns during the initial training. Additional patterns should be defined in DDRPHY_CAL_WR_PATTERN2_CON0~4, DDRPHY_CAL_WR_PATTERN3_CON0~4, DDRPHY_CAL_WR_PATTERN4_CON0~4.
- DDRPHY_CAL_CON5.wrtrn_cyc_mode should be 0 during normal operation.

Low Frequency Initial Training Setting (under 533MHz)

- Set DDRPHY_CAL_CON0.dvfs_wr_train_en=0x1.
- Set DDRPHY_CAL_CON4.dvfs_wr_start_adj=0x0.
- Set DDRPHY_CAL_CON5.wrtrn_cyc_en=0.
- After low frequency write training is done, apply the following setting.
  - Store the current lockvalue/4 value.
  - Store write training results from DDRPHY_WR_DESKEWC_CS*_CON*, DDRPHY_DM_DESKEWC_CS*_CON*, DDRPHY_ECC_DESKEWC_CS*_CON*.
  - Write (stored write training result values + lockvalue/4) to the following register.
    - Enable DDRPHY_CAL_CON0.wr_cal_mode.
    - Enable DDRPHY_CAL_CON3.wr_sw_mode.
    - DDRPHY_SW_WR_DESKEWC_CS*_CON, DDRPHY_SW_DM_DESKEWC_CS*_CON*, DDRPHY_SW_ECC_DESKEWC_CS*_CON*.
    - Disable DDRPHY_CAL_CON3.wr_sw_mode.
  - Restore DVFS write training related setting for successful DVFS write training or other initial write training.
    - Set DDRPHY_CAL_CON4.dvfs_wr_start_adj=0xf.
    - Set DDRPHY_CAL_CON0.dvfs_wr_train_en=0.

Common Setting for Write Training

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- Set write training pattern
  - DQ pattern in DDRPHY_CAL_WR_PATTERN1_CON0~ DDRPHY_CAL_WR_PATTERN1_CON3.
- Set wrtrn_rddata_adj_w0_bst1_8 for BL1~BL2 pattern.
- Set wrtrn_rddata_adj_w1_bst1_8 for BL3~BL4 pattern.
- Set wrtm_rddata_adj_w2_bst1_8 for BL5~BL6 pattern.
- Set wrtrn_rddata_adj_w3_bst1_8 for BL7~BL8 pattern.
- Set wrtm_rddata_adj_w0_bst9_16 for BL9~BL10 pattern.
- Set wrtrn_rddata_adj_w1_bst9_16 for BL11~BL12 pattern.
- Set wrtm_rddata_adj_w2_bst9_16 for BL13-BL14 pattern.
- Set wrtrn_rddata_adj_w3_bst9_16 for BL15~BL16 pattern.
- Set write DM pattern in DDRPHY_CAL_WR_PATTERN1_CON4.
- Set wrtrn_rddata_dm_adj_w0_bst1_8 for BL1~BL2 pattern.
- Set wrtrn_rddata_dm_adj_w1_bst1_8 for BL3~BL4 pattern.
- Set wrtrn_rddata_dm_adj_w2_bst1_8 for BL5~BL6 pattern.
- Set wrtrn_rddata_dm_adj_w3_bst1_8 for BL7~BL8 pattern.
- Set wrtrn_rddata_dm_adj_w0_bst9_16 for BL9~BL10 pattern.
- Set wrtrn_rddata_dm_adj_w1_bst9_16 for BL11~BL12 pattern.
- Set wrtrn_rddata_dm_adj_w2_bst9_16 for BL13~BL14 pattern.
- Set wrtrn_rddata_dm_adj_w3_bst9_16 for BL15~BL16 pattern.
- Configure DDRPHY in write training mode.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_wrtrn_en=1.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_wrtrn_rank_en properly.
  - For example, if phy_wrtrn_rank_en is set to 0x3, per-rank write training will start from rank0 to rank1 sequentially.

7.6.5.5 LPDDR5 Periodic Training

Periodic training compensates write center shift and gate shift caused by VT variation in memory. Initial write/gate training should be completed before periodic training. During periodic training, DDRPHY uses the PHY master interface and generates RDC/WFF/RFF/MPC commands without the memory controller. When DDRPHY request PHY master mode, the controller should place the DRAM in self refresh and assert dfi_phymstr_ack. Periodic training will be executed in sequence.

- The common parameter is same as initial training.
- Enable periodic write training properly (refer to SFR description)
  - Set DDRPHY_SCHD_TRAIN_CON0.periodic_wrtrn_en and if use DVFS, set DDRPHY_DVFS0_TRAIN_CON0.dvfs0_periodic_wrtrn_en and DDRPHY_DVFS1_TRAIN_CON0.dvfs1_periodic_wrtrn_en.
- Set DDRPHY_SCHD_TRAIN_CON1.periodic_time.
  - Interval of periodic training = periodic_time*tCK_osc (oscillator clock).
- Set DDRPHY_SCHD_TRAIN_CON1/ DDRPHY_DVFS*_SCHD_TIME_CON3.periodic_en =1 and if use DVFS, set DDRPHY_DVFS0_SCHD_TIME_CON3.dvfs0_periodic_en and DDRPHY_DVFS1_SCHD_TIME_CON3.dvfs1_periodic_en properly.

7.6.5.6 LPDDR5 DVFS Training

DVFS training compensates write center shift and gate shift caused by VT variation in memory. Initial write/gate training should be completed before DVFS training. During DVFS training, DDRPHY uses the PHY master interface and generates RDC/WFF/RFF/MPC commands without the memory controller. When DDRPHY request PHY master mode, the controller should place the DRAM in self refresh and assert dfi_phymstr_ack. DVFS training will be executed in sequence.

- The common parameter is same as initial training.
- Enable DVFS write training properly.
  - Set DDRPHY_SCHD_TRAIN_CON0.dvfs_wrtrn_en and if use DVFS, set DDRPHY_DVFS0_SCHD_TIME_CON3.dvfs0_dvfs_wrtrn_en and DDRPHY_DVFS1_SCHD_TIME_CON3.dvfs1_dvfs_wrtrn_en.
- Set DDRPHY_CAL_CON0.dvfs_wr_train_en=1(DVFS mode).

7.6.6 DDR Monitor

1. DDR read or write address monitor

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DDR monitor module can store 4 consecutive read or write addresses in real time for each AXI port. We can read these addresses through APB bus for debug when system enters abnormal state. Each read or write address together with awid/arid and a*ready/a*valid signals are stored in two 32bits registers.
Following is an example of monitoring read port of AXI port n(n=0/1/2/3/4).
DDRMON_PORTn_ADDR_31_0={araddr_n[31:0]}
DDRMON_PORTn_ADDR_63_32={arid_n[7:0],arready_n,arvalid_n,araddr_n[33:32]}
Following is an example of monitoring write port of AXI port n(n=0/1/2/3/4).
DDRMON_PORTn_ADDR_31_0={awaddr_n[31:0]}
DDRMON_PORTn_ADDR_63_32={awid_n[7:0],awready_n,awvalid_n,awaddr_n[33:32]}
The steps of configuration to monitor DDR read or write address is as follows.

- Configure DDRMON_IF_CTRL.direction to select storing read or write address.
- Set DDRMON_IF_CTRL.if_mon_en to 1 to enable DDR monitor.
- When system is abnormal, we can read the register to get the current four addresses.

2. DDR access address monitor within a specified range

Sometimes we want to confirm whether DDR read or write within a specified address range on a certain AXI port, then we can configure the address range and enable this function.
The steps of configuration to monitor DDR access address within a specified range is as follows.

- Configure the write address range registers DDRMON_WR_START_ADDR, DDRMON_WR_END_ADDR, and read address registers DDRMON _RD_START_ADDR, DDRMON_RD_END_ADDR.
- Enable corresponding AXI write port access address monitor interrupt by configuring the register DDRMON_INT_MASK2[4:0], enable corresponding AXI read port access address monitor interrupt by configuring the register DDRMON_INT_MASK3[4:0].
- Set DDRMON_IF_CTRL.if_mon_en to 1 to enable DDR address monitor.
- If the read or write addresses hit the range, then interrupt will assert, and we can read the interrupt status register DDRMON_INT_STATUS1.

3. DDR access command statistics

This module can do the statistics about DDR access command, like write, read and active by monitoring DFI interface. There are two mode to do statistics, hardware mode and software mode. Two thresholds can be set, if read and write command number is more than high threshold, or less than low threshold, the interrupt will be asserted.

4. DDRCTL's LPR/HPR/WR CAM status statistics

The DDR monitor will monitor the DDRCTL's available LPR/HPR/WR CAM slot. The result can be read through LPR/HPR/WR_CREDIT_CNT* registers.

5. DDR low power statistics

It does the statistics about the low power period such as DDR self-refresh power down, power down, clkstop and PHY low power and so on. After compare statistics interrupt asserts, the low power period represent in correspond count register will be updated and can be accessed through APB bus interface.

6. DDR special pattern statistics for a designated bank

In this module, for a designated bank, which is software configured. DDRMON will statistic the count for special DDR command patterns:

- per_bank_rd_wr_per_act_max_number: count the max read and write commands in an active command to a precharge command interval.
- per_bank_series_rd_burst_max_number: count the max series read command in an active command to a precharge command interval.
- per_bank_series_rd_burst_times_number: count the total number of series read command.
- per_bank_series_wr_burst_max_number: count the max series write command in an active command to a precharge command interval.
- per_bank_series_wr_burst_times_number: count the total number of series write command.
- per_bank_rd2rd_page_hit_number: count the total number of back to back read command.
- per_bank_wr2wr_page_hit_number: count the total number of back to back write

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command.
- per_bank_rd2wr_page_hit_number: count the total number of read next to write command.
- per_bank_rd2rd_page_miss_number: count all RD-PRE-ACT-RD pattern.
- per_bank_wr2wr_page_miss_number: count all WR-PRE-ACT-WR pattern.
- per_bank_rd2wr_page_miss_number: count all RD-PRE-ACT-WR pattern.
- per_bank_wr2rd_page_miss_number: count all WR-PRE-ACT-RD pattern.

7. DDR special pattern statistics for all banks

In this module, DDRMON count the special pattern for all ranks and all banks.
- all_bank_act_act_number: count all ACT-ACT pattern
- all_bank_act_pre_number: count all ACT-PRE pattern
- all_bank_act_rdwr_same_number: count ACT-RD and ACT-WR pattern, which active command and read/write command with the same rank, same bank and same row.
- all_bank_rd2wr_number: count all RD-WR pattern.
- all_bank_wr2rd_number: count all WR-RD pattern.
- all_bank_series_rd_total_cnt_number: count all back to back read pattern.
- all_bank_series_wr_total_cnt_number: count all back to back write pattern.
- all_bank_series_rd_burst_max_number: count the longest series read command.
- all_bank_series_wr_burst_max_number: count the longest series write command.
- all_bank_series_rd_burst_times_number: count the count of all series read command interval.
- all_bank_series_wr_burst_times_number: count the count of all series write command interval.
- all_bank_tccdmw_cnt_number: count all mask write command.

8. Hardware mode

In hardware mode, a dfi timer is used to specify a statistics period, the command statistics is done in the statistics period. The dfi timer is running in 24MHz. After dfi timer counts to the threshold, and update the statistics value, the dfi timer will restart automatically, and count again.

The steps of hardware mode of DDR access command statistics is as follows.
- Configure register DDRMON_CTRL.hardware_en as 1 to enable hardware mode.
- Configure register DDRMON_TIMER_COUNT to set the dfi timer count threshold, the statistics is done in the period of timer being less than the value of DDRMON_TIMER_COUNT.
- Configure register DDRMON_CTRL.lpddr4_en and DDRMON_CTRL.lpddr5_en to set the DDR mode:

DDRMON_CTRL.lpddr4_en	DDRMON_CTRL.lpddr5_en	DDR mode
1	0	LPDDR4
0	1	LPDDR5

- Configure register DDRMON_FLOOR_NUMBER to specify the low threshold of interrupt, and configure register DDRMON_TOP_NUMBER to specify the high threshold of interrupt.
- Configure register DDRMON_CTRL.timer_cnt_en as 1 to start hardware mode.
- Wait for the interrupt to do following process. We also can read the read, write and active command number separately.

9. Software mode

In software mode, the statistics is controlled by software.

The steps of hardware mode of DDR access command statistics is as follows.
- Configure register DDRMON_CTRL.lpddr4_en and DDRMON_CTRL.lpddr5_en to set the DDR mode like hardware mode.
- Configure register DDRMON_CTRL.software_en as 1 to enable software mode statistics.

Configure register DDRMON_CTRL.software_en as 0 to stop the statistics, and generate the statistics result. We can read the read, write and active command number separately.

10. Start 2 channels DDR monitors and interconnect monitor at the same time

Each DDR channel has one DDR monitor. Following steps are to start these 2 DDR monitors and interconnect monitor working at the same time.
- Set GRF_DDR_COMMON_CON4[2:0] to 3'b111 to enable interconnect monitor

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controlled by DDR monitor.

- Set DDRMON_CTRL0.external_trigger_sel=1'b1 to select external control signal to start DDR monitor instead of setting DDRMON_CTRL0.software_start or DDRMON_CTRL0.timer_cnt_en.
- Set DDR monitor registers properly.
- Set interconnect monitor registers properly.
- Set GRF_DDR_COMMON_CON4[8] to 1'b1 to start DDR monitor and interconnect monitor. Then the 2 DDR monitor and interconnect monitor are working.

The steps to stop DDR monitor and interconnect monitor are as follows.

- Set GRF_DDR_COMMON_CON4[8] to 1'b0.

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Chapter 8 Gigabit Media Access Controller (GMAC)

8.1 Overview

The Ethernet Quality-of-Service controller(EQOS is commonly referred to as GMAC in this document) provides a complete Ethernet interface from processor to a Reduced Media Independent Interface (RMII) and Reduced Gigabit Media Independent Interface (RGMII) compliant Ethernet PHY. The GMAC includes a DMA controller. The DMA controller efficiently moves packet data from microprocessor's RAM, formats the data for an IEEE 802.3-2002 compliant packet and transmits the data to an Ethernet Physical Interface (PHY). It also efficiently moves packet data from RXFIFO to microprocessor's RAM. There are two separate GMAC in RK3576.
The following features may or may not be present in the actual product. Please contact Rockchip for the actual feature configurations and the third-party licensing requirements.

8.1.1 MAC Features

8.1.1.1 MAC Tx and Rx Common Features

- Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
- Supports 10/100-Mbps data transfer rates with the RMII interfaces
- Half-duplex operation:
  - CSMA/CD Protocol support
  - Flow control using back-pressure support (based on implementation-specific white papers and UNH Ethernet Clause 4 MAC Test Suite - Annex D)
  - Packet bursting and packet extension in 1000 Mbps half-duplex operation
- Standard IEEE 802.3az-2010 for Energy Efficient Ethernet in Reduced Gigabit Media Independent Interface (RGMII) PHYs
- 64-bit data transfer interface on the application side
- Full-duplex flow control operations (IEEE 802.3x Pause packets and Priority flow control)
- network statistics with RMON or MIB Counters (RFC2819/RFC2665)
- Support Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008 (64-bit timestamps given in the Tx or Rx status of PTP packet). Both one-step and two-step timestamping is supported in TX direction
- Flexibility to control the Pulse-Per-Second (PPS) output signal (ptp_pps_o)
- Media clock generation and recovery
- MDIO (Clause 22 and Clause 45) master interface for PHY device configuration and management

8.1.1.2 MAC Tx Features

- Preamble and start of packet data (SFD) insertion
- Separate 32-bit status for each packet transmitted from the application
- Automatic CRC and pad generation controllable on a per-packet basis
- Programmable packet length to support Standard or Jumbo Ethernet packets with up to 16 KB of size
- Programmable Inter Packet Gap (40–96 bit times in steps of 8)
- IEEE 802.3x Flow Control automatic transmission of zero-quanta Pause packet when flow control input transitions from assertion to de-assertion (in full-duplex mode)
- Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted packets with per-packet or static-global control
- Insertion, replacement, or deletion of up to two VLAN tags
- Frame Preemption for MAC Tx

8.1.1.3 MAC Rx Features

- Automatic Pad and CRC Stripping options
- Option to disable Automatic CRC checking
- Preamble and SFD deletion
- Separate 112-bit or 128-bit status

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- Programmable watchdog timeout limit
- Flexible address filtering modes:
  - Up to 31 additional 48-bit perfect (DA) address filters with masks for each byte
  - Up to 96 additional 48-bit perfect (DA) address filters that can be selected in blocks of 32 and 64 registers
  - Up to 31 48-bit SA address comparison check with masks for each byte
  - 32 bit, 64 bit, 128 bit, or 256 bit Hash filter (optional) for multicast and unicast (DA) addresses
  - Option to pass all multi-cast addressed packets
  - Promiscuous mode to pass all packets without any filtering for network monitoring
  - Pass all incoming packets (as per filter) with a status report
- Additional packet filtering:
  - VLAN tag-based: Perfect match and Hash-based (optional) filtering. Filtering based on either outer or inner VLAN tag is possible
  - Layer 3 and Layer 4-based: TCP or UDP over IPv4 or IPv6
  - Extended VLAN tag based filtering 4, 8, 16, or 32 filter selection
- IEEE 802.1Q VLAN tag detection and option to delete the VLAN tags in received packets
- Optional module to detect remote wake-up packets and AMD magic packets
- Optional forwarding of received Pause packets to the application (in full-duplex mode)
- Frame Preemption for MAC Rx

8.1.2 MTL Features

8.1.2.1 MTL Tx and Rx Common Features

- 32-bit, 64-bit, or 128-bit Transaction Layer block (bridges the application and the MAC)
- Data transfers executed using simple FIFO protocol
- Synchronization for all clocks in the design (Transmit, Receive, and Application clocks)
- Optimization for packet-oriented transfers with packets delimiters
- Option to have dual-port RAM based asynchronous FIFO controllers or Single-port RAM based synchronous FIFO controllers
- RAM memory instantiation outside the top-level module to facilitate memory testing or instantiation
- Programmable burst length, up to half the size of the MTL Rx queue or Tx queue size, to support burst data transfer in the EQOS-MTL configuration
- Programmable threshold capability for each queue (default of 64 bytes)
- Optional Debug and slave mode operation on Queue 0 (default queue)

8.1.2.2 MTL Tx Features

- TX FIFO sizes on transmission is 16 KB
- Store-and-Forward mechanism or threshold mode (cut-through) for transmission to the MAC
- Programmable queue size in configurations with multiple queues. Each queue size can be programmed in terms of 256 bytes
- Automatic retransmission of collision packets in half-duplex mode
- Discard packets on late collision, excessive collisions, excessive deferral, and under-run conditions with appropriate status
- Disabling of Data Memory RAM chip-select when inactive to reduce power consumption
- Optional module to calculate and insert IPv4 header checksum and TCP, UDP, or ICMP checksum
- Programmable interrupt options for different operational conditions
- Statistics by generating pulses for packets dropped (because of underflow) in the Tx FIFO
- Optional packet-level control for
  - VLAN tag insertion or replacement
  - Ethernet source address insertion
  - Layer3/Layer4 Checksum insertion control
  - One-step timestamp
  - Timestamp control

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  - CRC and pad control
- Following scheduling algorithms in configurations with multiple queues:
  - Weighted Round Robin (WRR)
  - (When Data Center Bridging is enabled) Deficit Weighted Round Robin (DWRR)
  - (When Data Center Bridging is enabled) Weighted Fair Queuing (WFQ)
  - Strict Priority (SP)
  - (When Audio-Video Bridging is enabled) Credit-based Shaper (CBS)
  - (When TSN is enabled), Enhancement to Scheduled Traffic (EST)
  - (When TSN is enabled), Time Based Scheduling (TBS)
- Option to support dropping of Tx Status to improve the Transmit throughput

8.1.2.3 MTL Rx Features

- Rx queue sizes in the Receive path is 32 KB
- Insertion of Rx Status vectors into the Rx queue after the EOP transfer (in Threshold mode) and before SOP (in Store-and-Forward mode) in EQOS-MTL configuration
- Programmable Rx queue threshold (default fixed at 64 bytes) in Threshold (or cut-through) mode
- Option to filter all error packets on reception and not forward them to the application in the store-and-forward mode
- Option to forward the undersized good packets
- Statistics by generating pulses for packets dropped (because of overflow) in the Rx FIFO
- Automatic generation of Pause packet control or backpressure signal to the MAC based on the Rx Queue fill level
- Arbitration among queues when multiple queues are present. The following arbitration schemes are supported:
  - Weighted Round Robin (WRR)
  - Weighted Strict priority (WSP)
  - Strict Priority (SP)
- Option to replicate received multicast packets for transfer by multiple Rx DMA channels
- Option to have a programmable lookup table based flexible Parser for filtering and steering the Rx packets

8.1.3 DMA Block Features

- 64-bit data transfers
- Separate DMA channel in the Transmit path for each queue in MTL
- Single or multiple DMA channels for any number of queues in MTL Receive path
- Fully synchronous design operating on a single application clock (except for CSR module, when a separate CSR clock is configured)
- Optimization for packet-oriented DMA transfers with packet delimiters
- Byte-aligned addressing for data buffer support
- Dual-buffer (ring) descriptor support
- Descriptor architecture to allow large blocks of data transfer with minimum CPU intervention (each descriptor can transfer up to 32 KB of data)
- Comprehensive status reporting for normal operation and transfers with errors
- Individual programmable burst length for Tx DMA and Rx DMA engines for optimal host bus utilization
- Programmable interrupt options for different operational conditions
- Per-packet Transmit or Receive Complete Interrupt control
- Round-robin or fixed-priority arbitration between the Receive and Transmit engines
- Start and Stop modes
- Separate ports for host CSR access and host data interface
- support for TCP Segmentation Offload (TSO) and UDP Segmentation Offload (USO)
- Selectable number of Tx DMA channels with TSO/USO feature enabled
- Routing of received packets to the DMA channels based on the DA or VLAN Priority in multi-channel DMA configurations
- Option to split the packet header (Layer 3 and Layer 4) and payload in a different

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buffers
- Time-sensitive conditional packet fetching from system memory by comparing the Slot Time or IEEE 1588 time information provided in the descriptor (useful for AV applications)
- Programmable control for Transmit Descriptor posted writes to improve the throughput
- Sideband signals to control starting and stopping of DMA channels

8.2 Block Diagram

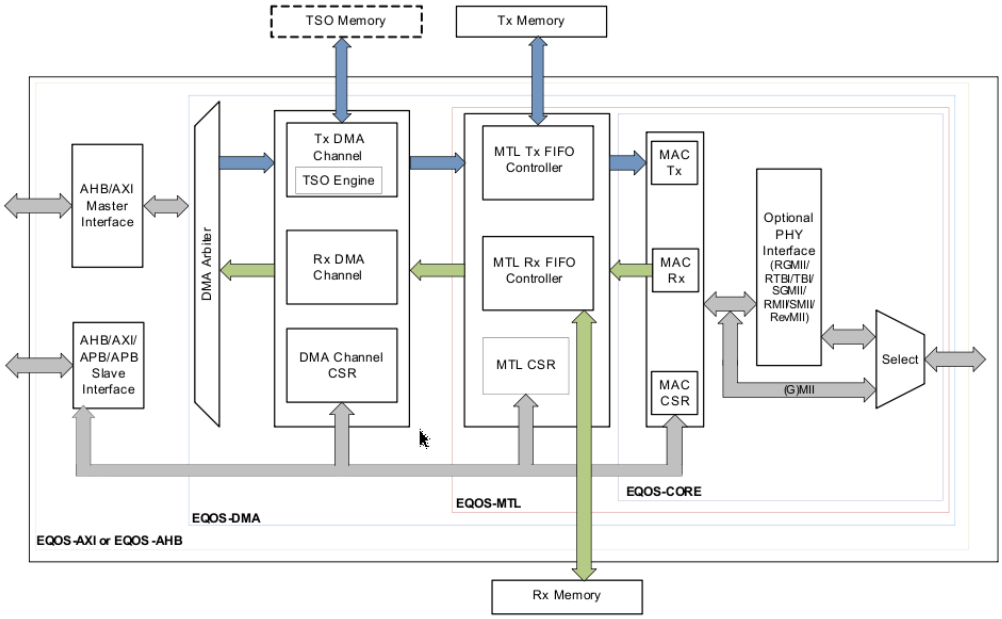


Fig. 8-1 GMAC Block Diagram

The GMAC is broken up into multiple separate functional units. These blocks are interconnected in the MAC module. The block diagram shows the general flow of data and control signals between these blocks.

The GMAC transfers data to system memory through the AXI master interface. The host CPU uses the APB Slave interface to access the GMAC subsystem's control and status registers (CSRs).

The GMAC supports the PHY interfaces of reduced GMII (RGMII) and reduced MII (RMII).

The Transmit FIFO (Tx FIFO) buffers data read from system memory by the DMA before transmission by the GMAC Core. Similarly, the Receive FIFO (Rx FIFO) stores the Ethernet frames received from the line until they are transferred to system memory by the DMA. These are asynchronous FIFOs, as they also transfer the data between the application clock and the GMAC line clocks.

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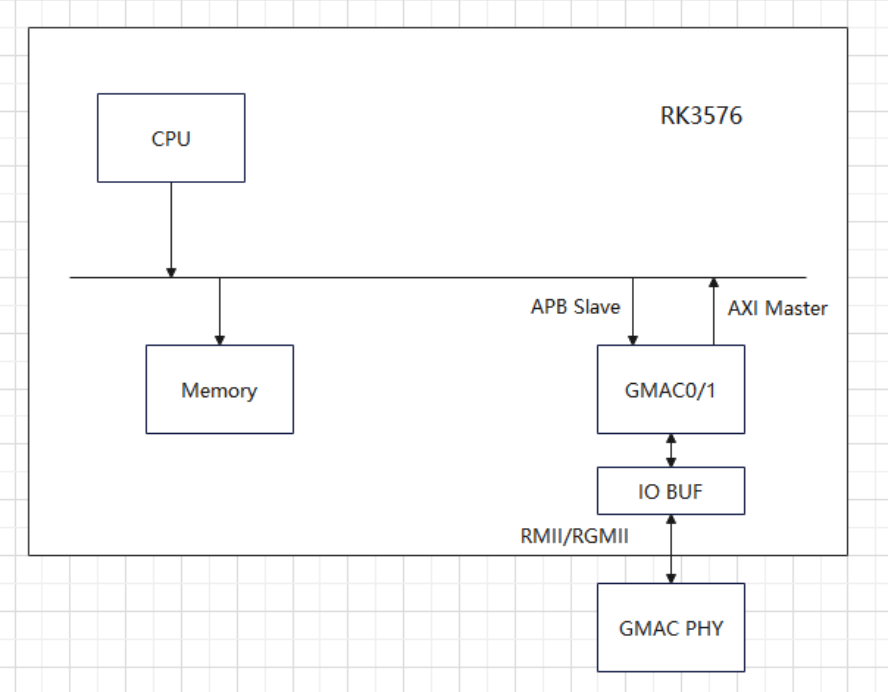


Fig. 8-2 GMAC in SOC

GMAC Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces and Supports 10/100-Mbps data transfer rates with the RMII interfaces.

8.3 Function Description

8.3.1 Frame Structure

Data frames transmitted shall have the frame format shown in figure below.



Fig. 8-3 Frame Format

The preamble <preamble> begins a frame transmission. The bit value of the preamble field consists of 7 octets with the following bit values:
10101010 10101010 10101010 10101010 10101010 10101010 10101010
The SFD (start frame delimiter) <sfd> indicates the start of a frame and follows the preamble. The bit value is 10101011.The data in a well formed frame shall consist of N octet's data.

8.3.1.1 RMII Interface timing diagram

The Reduced Media Independent Interface (RMII) specification reduces the pin count between Ethernet PHYs and Switch ASICs (only in 10/100 mode). According to the IEEE 802.3u standard, an MII contains 16 pins for data and control. In devices incorporating multiple MAC or PHY interfaces (such as switches), the number of pins adds significant cost with increase in port count. The RMII specification addresses this problem by reducing the pin count to 7 for each port - a 62.5% decrease in pin count.
The RMII module is instantiated between the GMAC and the PHY. This helps translation of the MAC's MII into the RMII. The RMII block has the following characteristics:
Supports 10-Mbps and 100-Mbps operating rates. It does not support 1000-Mbps operation. Two clock references are sourced externally or CRU, providing independent, 2-bit wide transmit and receive paths.

8.3.1.2 Transmit Bit Ordering

Each nibble from the MII must be transmitted on the RMII a di-bit at a time with the order of di-bit transmission shown in figure below. The lower order bits (D1 and D0) are transmitted first followed by higher order bits (D2 and D3).

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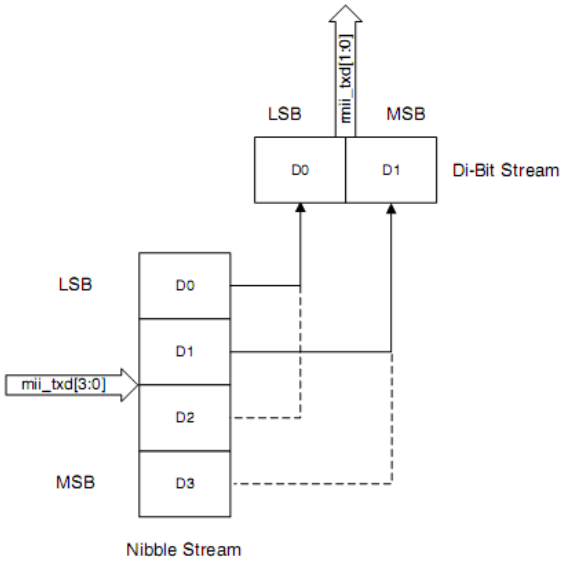


Fig. 8-4 RMII Transmission Bit Ordering

8.3.1.3 RMII Transmit Timing Diagrams

The follow figures show MII-to-RMII transaction timing. The clk_rmii_i (REF_CLK) frequency is 50MHz in RMII interface. In 10Mb/s mode, as the REF_CLK frequency is 10 times as the data rate, the value on rmii_txd_o[1:0] (TXD[1:0]) shall be valid such that TXD[1:0] may be sampled every 10th cycle, regard-less of the starting cycle within the group and yield the correct frame data.

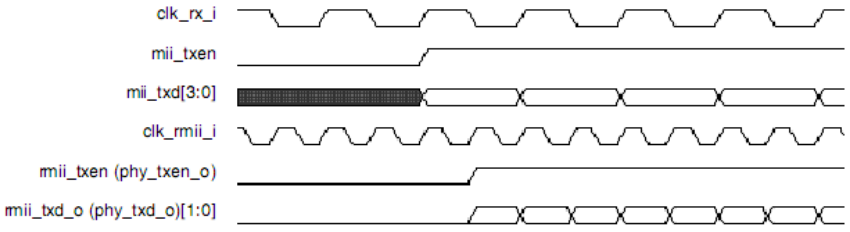


Fig. 8-5 Start of MII and RMII Transmission in 100-Mbps Mode

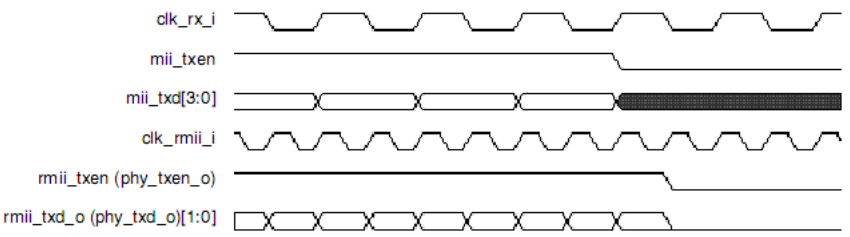


Fig. 8-6 End of MII and RMII Transmission in 100-Mbps Mode

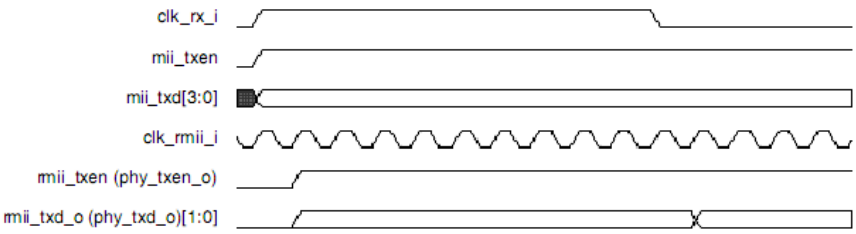


Fig. 8-7 Start of MII and RMII Transmission in 10-Mbps Mode

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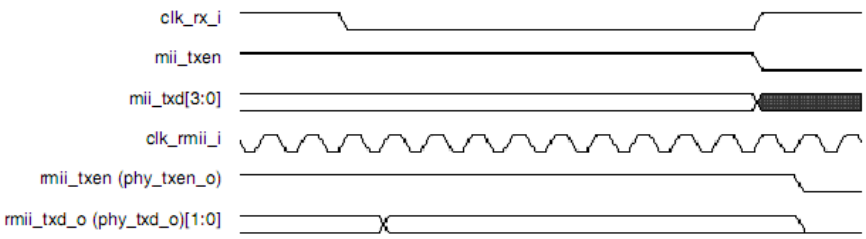


Fig. 8-8 End of MII and RMII Transmission in 10-Mbps Mode

8.3.1.4 Receive Bit Ordering

Each nibble is transmitted to the MII from the di-bit received from the RMII in the nibble transmission order shown in figure below. The lower order bits (D0 and D1) are received first, followed by the higher order bits (D2 and D3).

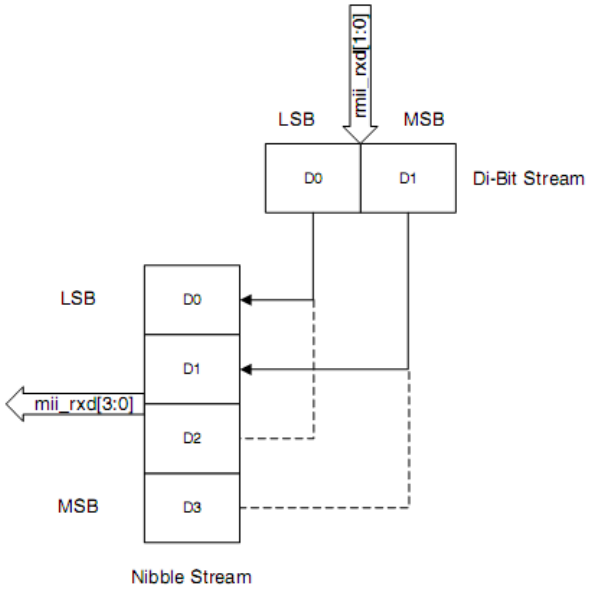


Fig. 8-9 RMII Receive Bit Ordering

8.3.1.5 RGMII Interface

The Reduced Gigabit Media Independent Interface (RGMII) specification reduces the pin count of the interconnection between the GMAC 10/100/1000 controller and the PHY for GMII and MII interfaces. To achieve this, the data path and control signals are reduced and multiplexed together with both the edges of the transmission and receive clocks. For gigabit operation the clocks operate at 125 MHz; for 10/100 operation, the clock rates are 2.5 MHz/25 MHz.

In the GMAC 10/100/1000 controller, the RGMII module is instantiated between the GMAC core's GMII and the PHY to translate the control and data signals between the GMII and RGMII protocols.

The RGMII block has the following characteristics:

- Supports 10-Mbps, 100-Mbps, and 1000-Mbps operation rates
- For the RGMII block, no extra clock is required because both the edges of the incoming clocks are used
- The RGMII block extracts the in-band (link speed, duplex mode and link status) status signals from the PHY and provides them to the GMAC core logic for link detection

8.3.2 Station Management Agent

The application can access the PHY registers through the Station Management Agent (SMA) module. SMA is a two-wire Station Management interface (MIM).

For MIM accesses, the maximum operating frequency of the MDC (gmii_mdc_o) is 2.5 MHz, as specified in the IEEE 802.3. In the GMAC core, the gmii_mdc_o clock is derived from the application clock or clk_csr_i, using a divider-counter. The divide factor depends on the clock range setting (CR field) in the MAC_MDIO_Address register Select the clock divide

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factor as mentioned in the description of CR field of MAC_MDIO_Address register, to meet IEEE specifications. However, if your system supports higher clock frequencies on the MIM interface, there is a provision to select a different divider.
The MDIO frame structure is as follows:

Table 8-1 MDIO Clause 45 Frame Structure

Field	Description
IDLE	The mdio line is in tri-state; there is no clock on gmii_mdc_o signal.
PREAMBLE	32 continuous bits of value 1
START	Start of packet is 2'b00
OPCODE	■ 2'b00 ■ 2'b01 ■ 2'b10 ■ 2'b11
PHY ADDR	5-bit address select for one of 32 PHYs
DEV ADDR	5-bit address select for one of 32 devices
TA	Turnaround ■ 2'bZ0: Read and post-read increment address ■ 2'b10: Write and address MDIO accesses Where Z is the tri-state level
DATA/ADDRESS	16-bit value: For an address cycle (OPCODE = 2'b00), this frame contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, this field contains the data to be written to the register. For read or post-read increment address frames, this field contains the contents of the register read from the PHY. ■ In address and data write cycles, the GMAC drives the MDIO line during the transfer of these 16 bits. ■ In read and post-read increment address cycles, the PHY drives the MDIO line during the transfer of these 16 bits.

The frame structure for Clause 22 frames is also supported. The C45E bit in the MAC_MDIO_Address register can be programmed to enable Clause 22 or Clause 45 mode of operation. Table.1-2 shows the Clause 22 frame format.

Table 8-2 MDIO Clause 22 Frame Structure

Field	Description
IDLE	The mdio line is in tri-state; there is no clock on gmii_mdc_o signal.
PREAMBLE	32 continuous bits of value 1
START	Start of packet is 2'b01
OPCODE	■ 2'b01 : Write ■ 2'b10 : Read
PHY ADDR	5-bit address select for one of 32 PHYs
DEV ADDR	5-bit address to select the register within each MMD
TA	Turnaround ■ 2'bZ0: Read and post-read increment address ■ 2'b10: Write and address MDIO accesses Where Z is the tri-state level
DATA/ADDRESS	Any 16-bit value: ■ In a write operation, the GMAC drives MDIO ■ In read operation, the PHY drives MDIO

In addition to normal read and write operations, the SMA also supports post-read increment address while operating in Clause 45 mode.

8.3.3 Power Management and Energy Efficient Ethernet

The GMAC supports the following techniques to save power.

- Magic Packet
- Remote Wakeup
- Energy Efficient Ethernet

The Magic Packet and Remove Wakeup techniques are used to save power in the host system when it is idle (Sleep mode) and has to be woken up only at the reception of specific packets from the Ethernet network. In the Sleep mode, the power to the host logic along with majority of the GMAC (except the MAC receiver logic), can be shut down. On receiving the specific packets from the network, the MAC provides the trigger to restore the power to the host system and come back to normal state.

The Energy Efficient Ethernet (EEE) mode is compliant with the IEEE 802.3az-2010 standard. It is primarily targeted to save power in the Ethernet port when there is no traffic on the line. In this mode, the host indicates to the far-end that it does not have any packets to transmit for near future and puts the transmitter port (MAC Controller, PCS and PHY layers) into low-power mode. Similarly, the Receiver port can also be put into low-power mode when the far-end host indicates that it does not have any traffic to transfer. This allows significant saving of power in the Ethernet port (mainly in the PHY) with intermittent and bursty traffic profile. The triggering of entry and exit out of the EEE mode is controlled by the MAC and is supported within the GMAC.

Simultaneous operation of the EEE mode along with any or both the other power saving modes is also supported in GMAC.

8.3.4 IEEE 1588 Timestamp Support

The IEEE 1588 defines a Precision Time Protocol (PTP) which enables precise synchronization of time in measurement and control systems. This protocol enables heterogeneous systems that include clocks of varying inherent precision, resolution, and stability to synchronize. The protocol supports system-wide synchronization accuracy in the sub-microsecond range with minimal network and local clock computing resources.

The GMAC supports the IEEE 1588-2002 (version 1) and IEEE 1588-2008 (version 2). The IEEE 1588-2002 supports PTP transported over UDP/IP and IEEE 1588-2008 supports PTP transported over Ethernet. The GMAC provides programmable support for both standards. The controller supports the following features:

- Provides an option to take snapshot of all packets or only PTP type packets
- Provides an option to take snapshot of only event messages
- Provides an option to take the snapshot based on the clock type: ordinary, boundary, end-to-end transparent, and peer-to-peer transparent
- Provides an option to select the node to be a master or slave for ordinary and boundary clock
- Identifies the PTP message type, version, and PTP payload in packets sent directly over Ethernet and sends the status
- Provides an option to measure sub-second time in digital or binary format

8.3.5 TCP/IP Segmentation Offload (TSO) Engine

The TCP Segmentation Offload (TSO) engine is useful in offloading the TCP segmentation functions to the hardware.

It also supports UDP Segmentation Offload (USO) in which the UDP payload is segmented in the hardware. There are no sequencing/ordering controls available or updated in the segments, so it can be used in point to point applications in which out of order packets are not expected by the receiver. The description and flow of TSO mentioned in this section is same as USO, any deviation is provided as notes.

In the TCP segmentation offload (TSO) feature, the DMA splits a large TCP packet into multiple small packets and passes these packets to the MTL Tx Queue.

8.3.6 MAC Management Counters

The GMAC supports storing the statistics about the received and transmitted packets in registers that are accessible through the application.

The counters in the MAC Management Counters (MMC) module can be viewed as an

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extension of the register address space of the CSR module. The MMC module maintains a set of registers for gathering statistics on the received and transmitted packets. The register set includes a control register for controlling the behavior of the registers, two status registers containing interrupts generated (receive and transmit), and Interrupt Enable registers (receive and transmit). These registers are accessible from the Application through the MAC Control Interface (MCI). Each register is 32-bits wide. The write data is qualified with the corresponding mci_be_i signals. Therefore, non-32-bit accesses are allowed as long as the address is word-aligned. The MMCs are accessed using transactions, in the same way the CSR address space is accessed.
The MMC counters are free running. There is no separate enable for the counters to start. If a particular MMC counter is present in the RTL, it starts counting when corresponding packet is received or transmitted. The Receive MMC counters are updated for packets that are passed by the Address Filter (AFM) block. The statistics of packets, dropped by the AFM module, are not updated unless they are runt packets of less than 6 bytes (DA bytes are not received fully). To get statistics of all packets, set Bit 0 in the “MAC_Packet_Filter” register.
The MMC module gathers statistics on encapsulated IPv4, IPv6, TCP, UDP, or ICMP payloads in received Ethernet packets.

8.4 Register Description

8.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
GMAC0	0x2A220000
GMAC1	0x2A230000

8.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GMAC_MAC_CONFIGURATION	0x0000	W	0x00000000	The MAC Configuration Register establishes the operating mode of the MAC
GMAC_MAC_EXT_CONFIGURATION	0x0004	W	0x00000000	The MAC Extended Configuration Register establishes the operating mode of the MAC
GMAC_MAC_PACKET_FILTER	0x0008	W	0x00000000	The MAC Packet Filter register contains the filter controls for receiving packets
GMAC_MAC_WATCHDOG_TIMEOUT	0x000C	W	0x00000000	The Watchdog Timeout register controls the watchdog timeout for received packets
GMAC_MAC_HASH_TABLE_REG0	0x0010	W	0x00000000	The Hash Table Register 0 contains the first 32 bits of the hash table
GMAC_MAC_HASH_TABLE_REG1	0x0014	W	0x00000000	The Hash Table Register 1 contains the second 32 bits of the hash table
GMAC_MAC_HASH_TABLE_REG2	0x0018	W	0x00000000	The Hash Table Register 2 contains the third 32 bits of the hash table

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_VLAN_TAG_CTRL	0x0050	W	0x00000000	This register is the redefined format of the MAC VLAN Tag Register. It is used for indirect addressing. It contains the address offset, command type and Busy Bit for CSR access of the Per VLAN Tag registers
GMAC_MAC_VLAN_TAG_DATA	0x0054	W	0x00000000	This register holds the read/write data for Indirect Access of the Per VLAN Tag registers.During the read access, this field contains valid read data only after the OB bit is reset. During the write access, this field should be valid prior to setting the OB bit in the MAC_VLAN_Tag_Ctrl Register
GMAC_MAC_VLAN_HASH_TABLE	0x0058	W	0x00000000	When VTHM bit of the MAC_VLAN_Tag register is set, the 16-bit VLAN Hash Table register is used for group address filtering based on the VLAN tag
GMAC_MAC_VLAN_INCL	0x0060	W	0x00000000	The VLAN Tag Inclusion or Replacement register contains the VLAN tag for insertion or replacement in the Transmit packets. It also contains the VLAN tag insertion controls
GMAC_MAC_INNER_VLAN_INCL	0x0064	W	0x00000000	The Inner VLAN Tag Inclusion or Replacement register contains the inner VLAN tag to be inserted or replaced in the Transmit packet. It also contains the inner VLAN tag insertion controls
GMAC_MAC_Q0_TX_FLOW_CTRL	0x0070	W	0x00000000	The Flow Control register controls the generation and reception of the Control (Pause Command) packets by the Flow control module of the MAC
GMAC_MAC_RX_FLOW_CTRL	0x0090	W	0x00000000	The Receive Flow Control register controls the pausing of MAC Transmit based on the received Pause packet
GMAC_MAC_RXQ_CTRL4	0x0094	W	0x00000000	The Receive Queue Control 4 register controls the routing of unicast and multicast packets that fail the Destination or Source address filter to the Rx queues
GMAC_MAC_RXQ_CTRL0	0x00A0	W	0x00000000	The Receive Queue Control 0 register controls the queue management in the MAC Receiver
GMAC_MAC_RXQ_CTRL1	0x00A4	W	0x00000000	The Receive Queue Control 1 register controls the routing of multicast, broadcast, AV, DCB, and untagged packets to the Rx queues

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_RXQ_CTRL2	0x00A8	W	0x00000000	This register controls the routing of tagged packets based on the USP (user Priority) field of the received packets to the RxQueues 0 to 3
GMAC_MAC_INTERRUPT_STATUS	0x00B0	W	0x00000000	The Interrupt Status register contains the status of interrupts
GMAC_MAC_INTERRUPT_ENABLE	0x00B4	W	0x00000000	The Interrupt Enable register contains the masks for generating the interrupts
GMAC_MAC_RX_TX_STATUS	0x00B8	W	0x00000000	The Receive Transmit Status register contains the Receive and Transmit Error status
GMAC_MAC_PMT_CONTROL_STATUS	0x00C0	W	0x00000000	The PMT Control and Status Register
GMAC_MAC_RWK_PACKET_FILTER	0x00C4	W	0x00000000	The Remote Wakeup Filter registers are implemented as 8, 16, or 32 indirect access registers (wkuppktfilter_reg#i) based on whether 4, 8, or 16 Remote Wakeup Filters are selected in the configuration and accessed by application through MAC_RWK_Packet_Filter register
GMAC_RWK_FILTER0_BYTE_MASK	0x00C4	W	0x00000000	RWK Filter0 Byte Mask
GMAC_RWK_FILTER1_BYTE_MASK	0x00C4	W	0x00000000	RWK Filter1 Byte Mask
GMAC_RWK_FILTER2_BYTE_MASK	0x00C4	W	0x00000000	RWK Filter2 Byte Mask
GMAC_RWK_FILTER3_BYTE_MASK	0x00C4	W	0x00000000	RWK Filter3 Byte Mask
GMAC_RWK_FILTER01_CRC	0x00C4	W	0x00000000	RWK Filter 0/1 CRC-16
GMAC_RWK_FILTER23_CRC	0x00C4	W	0x00000000	RWK Filter 2/3 CRC-16
GMAC_RWK_FILTER_OFFSET	0x00C4	W	0x00000000	RWK Filter Offset
GMAC_RWK_FILTER_COMMAND	0x00C4	W	0x00000000	RWK Filter Command
GMAC_MAC_LPI_CONTROL_STATUS	0x00D0	W	0x00000000	The LPI Control and Status Register controls the LPI functions and provides the LPI interrupt status. The status bits are cleared when this register is read
GMAC_MAC_LPI_TIMERS_CONTROL	0x00D4	W	0x03E80000	The LPI Timers Control register controls the timeout values in the LPI states.
GMAC_MAC_LPI_ENTRY_TIMER	0x00D8	W	0x00000000	This register controls the Tx LPI entry timer
GMAC_MAC_1US_TIC_COUNTER	0x00DC	W	0x0000003F	This register controls the generation of the Reference time (1 microsecond tic)

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_PHYIF_CONTROL_STATUS	0x00F8	W	0x00000000	PHY Interface Control and Status Register
GMAC_MAC_VERSION	0x0110	W	0x00003051	The version register identifies the version of the DWC_ether_qos
GMAC_MAC_DEBUG	0x0114	W	0x00000000	The Debug register provides the debug status of various MAC blocks
GMAC_MAC_HW_FEATURE0	0x011C	W	0x181173F3	This register indicates the presence of first set of the optional features or functions
GMAC_MAC_HW_FEATURE1	0x0120	W	0x111E41E8	This register indicates the presence of second set of the optional features or functions
GMAC_MAC_HW_FEATURE2	0x0124	W	0x11041041	This register indicates the presence of third set of the optional features or functions
GMAC_MAC_HW_FEATURE3	0x0128	W	0x0C370031	This register indicates the presence of fourth set the optional features or functions
GMAC_MAC_MDIO_ADDRESS	0x0200	W	0x00000000	The MDIO Address register controls the management cycles to external PHY through a management interface
GMAC_MAC_MDIO_DATA	0x0204	W	0x00000000	The MDIO Data register stores the Write data to be written to the PHY register located at the address specified in MAC_MDIO_Address
GMAC_MAC_ARP_ADDRESS	0x0210	W	0x00000000	The ARP Address register contains the IPv4 Destination Address of the MAC
GMAC_MAC_CSR_SW_CTRL	0x0230	W	0x00000000	This register contains SW programmable controls for changing the CSR access response and status bits clearing
GMAC_MAC_FPE_CTRL_STS	0x0234	W	0x00000000	This register controls the operation of Frame Preemption
GMAC_MAC_EXT_CFG1	0x0238	W	0x00000000	This register contains Split mode control field and offset field for Split Header feature
GMAC_MAC_PRESN_TIME_NS	0x0240	W	0x00000000	This register contains the 32-bit binary rollover equivalent time of the PTP System Time in ns
GMAC_MAC_PRESN_TIME_UPDT	0x0244	W	0x00000000	This field holds the 32-bit value of MAC 1722 Presentation Time in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_ADDRESS0_HIGH	0x0300	W	0x0000FFFF	The MAC Address0 High register holds the upper 16 bits of the first 6-byte MAC address of the station
GMAC_MAC_ADDRESS0_LOW	0x0304	W	0xFFFFFFFF	The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station
GMAC_MMC_CONTROL	0x0700	W	0x00000000	This register establishes the operating mode of MMC
GMAC_MMC_RX_INTERRUPT	0x0704	W	0x00000000	Maintains the interrupts generated from all Receive statistics counters
GMAC_MMC_TX_INTERRUPT	0x0708	W	0x00000000	Maintains the interrupts generated from all Transmit statistics counters
GMAC_MMC_RX_INTERRUPT_MASK	0x070C	W	0x00000000	This register maintains the masks for interrupts generated from all Receive statistics counters
GMAC_MMC_TX_INTERRUPT_MASK	0x0710	W	0x00000000	This register maintains the masks for interrupts generated from all Transmit statistics counters
GMAC_TX_OCTET_COUNT_GOOD_BAD	0x0714	W	0x00000000	This register provides the number of bytes transmitted by the DWC_ether_qos, exclusive of preamble and retried bytes, in good and bad packets
GMAC_TX_PACKET_COUNT_GOOD_BAD	0x0718	W	0x00000000	This register provides the number of good and bad packets, exclusive of retried packets
GMAC_TX_UNDERFLOW_ERROR_PACKETS	0x0748	W	0x00000000	This register provides the number of packets aborted because of packets underflow error
GMAC_TX_CARRIER_ERROR_PACKETS	0x0760	W	0x00000000	This register provides the number of packets aborted because of carrier sense error (no carrier or loss of carrier)
GMAC_TX_OCTET_COUNT_GOOD	0x0764	W	0x00000000	This register provides the number of bytes exclusive of preamble, only in good packets
GMAC_TX_PACKET_COUNT_GOOD	0x0768	W	0x00000000	This register provides the number of good packets transmitted by DWC_ether_qos
GMAC_TX_PAUSE_PACKETS	0x0770	W	0x00000000	This register provides the number of good Pause packets transmitted by DWC_ether_qos
GMAC_RX_PACKETS_COUNT_GOOD_BAD	0x0780	W	0x00000000	This register provides the number of good and bad packets received by DWC_ether_qos
GMAC_RX_OCTET_COUNT_GOOD_BAD	0x0784	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos, exclusive of preamble, in good and bad packets

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Name	Offset	Size	Reset Value	Description
GMAC_RX_OCTET_COUNT_GOOD	0x0788	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos, exclusive of preamble, only in good packets
GMAC_RX_MULTICAST_PACKETS_GOOD	0x0790	W	0x00000000	This register provides the number of good multicast packets received by DWC_ether_qos
GMAC_RX_CRC_ERROR_PACKETS	0x0794	W	0x00000000	This register provides the number of packets received by DWC_ether_qos with CRC error
GMAC_RX_OVERSIZE_PACKETS_GOOD	0x07A8	W	0x00000000	This register provides the number of packets received by DWC_ether_qos without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register)
GMAC_RX_LENGTH_ERROR_PACKETS	0x07C8	W	0x00000000	This register provides the number of packets received by DWC_ether_qos with length error (Length Type field not equal to packet size), for all packets with valid length field
GMAC_RX_PAUSE_PACKETS	0x07D0	W	0x00000000	This register provides the number of good and valid Pause packets received by DWC_ether_qos
GMAC_RX_FIFO_OVERFLOW_PACKETS	0x07D4	W	0x00000000	This register provides the number of missed received packets because of FIFO overflow
GMAC_RX_WATCHDOG_ERROR_PACKETS	0x07DC	W	0x00000000	This register provides the number of packets received by DWC_ether_qos with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register)
GMAC_MMC_IPC_RX_INTERRUPT_MASK	0x0800	W	0x00000000	This register maintains the mask for the interrupt generated from the receive IPC statistic counters
GMAC_MMC_IPC_RX_INTERRUPT	0x0808	W	0x00000000	This register maintains the interrupt that the receive IPC statistic counters generate

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Name	Offset	Size	Reset Value	Description
GMAC_RXIPV4_GOOD_PACKETS	0x0810	W	0x00000000	This register provides the number of good IPv4 datagrams received by DWC_ether_qos with the TCP, UDP, or ICMP payload
GMAC_RXIPV4_HEADER_ERROR_PACKETS	0x0814	W	0x00000000	This register provides the number of IPv4 datagrams received by DWC_ether_qos with header (checksum, length, or version mismatch) errors
GMAC_RXIPV6_GOOD_PACKETS	0x0824	W	0x00000000	This register provides the number of good IPv6 datagrams received by DWC_ether_qos
GMAC_RXIPV6_HEADER_ERROR_PACKETS	0x0828	W	0x00000000	This register provides the number of IPv6 datagrams received by DWC_ether_qos with header (length or version mismatch) errors
GMAC_RXUDP_ERROR_PACKETS	0x0834	W	0x00000000	This register provides the number of good IP datagrams received by DWC_ether_qos whose UDP payload has a checksum error
GMAC_RXTCP_ERROR_PACKETS	0x083C	W	0x00000000	This register provides the number of good IP datagrams received by DWC_ether_qos whose TCP payload has a checksum error
GMAC_RXICMP_ERROR_PACKETS	0x0844	W	0x00000000	This register provides the number of good IP datagrams received by DWC_ether_qos whose ICMP payload has a checksum error
GMAC_RXIPV4_HEADER_ERROR_OCTETS	0x0854	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in IPv4 datagrams with header errors (checksum, length, version mismatch)
GMAC_RXIPV6_HEADER_ERROR_OCTETS	0x0868	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in IPv6 datagrams with header errors (length, version mismatch)
GMAC_RXUDP_ERROR_OCTETS	0x0874	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in a UDP segment that had checksum errors
GMAC_RXTCP_ERROR_OCTETS	0x087C	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in a TCP segment that had checksum errors
GMAC_RXICMP_ERROR_OCTETS	0x0884	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in a good ICMP segment

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Name	Offset	Size	Reset Value	Description
GMAC_MMC_FPE_TX_INTERRUPT	0x08A0	W	0x00000000	This register maintains the interrupts generated from all FPE related Transmit statistics counters
GMAC_MMC_FPE_TX_INTERRUPT_MASK	0x08A4	W	0x00000000	This register maintains the masks for interrupts generated from all FPE related Transmit statistics counters
GMAC_MMC_TX_FPE_FRAGMENT_CNTR	0x08A8	W	0x00000000	This register provides the number of additional mPackets transmitted due to preemption
GMAC_MMC_TX_HOLD_REQ_CNTR	0x08AC	W	0x00000000	This register provides the count of number of times a hold request is given to MAC
GMAC_MMC_FPE_RX_INTERRUPT	0x08C0	W	0x00000000	This register maintains the interrupts generated from all FPE related Receive statistics counters
GMAC_MMC_FPE_RX_INTERRUPT_MASK	0x08C4	W	0x00000000	This register maintains the masks for interrupts generated from all FPE related Receive statistics counters
GMAC_MMC_RX_PACKET_ASM_ERR_CNTR	0x08C8	W	0x00000000	This register provides the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value
GMAC_MMC_RX_PACKET_SMD_ERR_CNTR	0x08CC	W	0x00000000	This register provides the number of received MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no
GMAC_MMC_RX_PACKET_ASSEMBLY_OK_CNTR	0x08D0	W	0x00000000	This register provides the number of MAC frames that were successfully reassembled and delivered to MAC
GMAC_MMC_RX_FPE_FRAGMENT_CNTR	0x08D4	W	0x00000000	This register provides the number of additional mPackets transmitted due to preemption
GMAC_MAC_L3_L4_CONTROL0	0x0900	W	0x00000000	The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4
GMAC_MAC_LAYER4_ADDRESS0	0x0904	W	0x00000000	The MAC_Layer4_Address0, MAC_L3_L4_Control0, MAC_Layer3_Addr0_Reg0, MAC_Layer3_Addr1_Reg0, MAC_Layer3_Addr2_Reg0 and MAC_Layer3_Ad dr3_Reg0 registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_LAYER3_ADDR0_REG0	0x0910	W	0x00000000	For IPv4 packets, the Layer 3 Address 0 Register 0 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field
GMAC_MAC_LAYER3_ADDR1_REG0	0x0914	W	0x00000000	For IPv4 packets, the Layer 3 Address 1 Register 0 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field
GMAC_MAC_LAYER3_ADDR2_REG0	0x0918	W	0x00000000	The Layer 3 Address 2 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field
GMAC_MAC_LAYER3_ADDR3_REG0	0x091C	W	0x00000000	The Layer 3 Address 3 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field
GMAC_MAC_TIMESTAMP_CONTROL	0x0B00	W	0x00000000	This register controls the operation of the System Time generator and processing of PTP packets for timestamping in the Receiver
GMAC_MAC_SUB_SECOND_INCREMENT	0x0B04	W	0x00000000	Specifies the value to be added to the internal system time register every cycle of clk_ptp_ref_i clock
GMAC_MAC_SYSTEM_TIME_SECS	0x0B08	W	0x00000000	The System Time Nanoseconds register, along with System Time Seconds register, indicates the current value of the system time maintained by the MAC
GMAC_MAC_SYSTEM_TIME_NS	0x0B0C	W	0x00000000	The System Time Nanoseconds register, along with System Time Seconds register, indicates the current value of the system time maintained by the MAC
GMAC_MAC_SYS_TIME_SECS_UPDATE	0x0B10	W	0x00000000	The System Time Seconds Update register, along with the System Time Nanoseconds Update register, initializes or updates the system time maintained by the MAC
GMAC_MAC_SYS_TIME_NS_UPDATE	0x0B14	W	0x00000000	MAC System Time Nanoseconds Update register

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_TIMESTAMP_ADDEND	0x0B18	W	0x00000000	Timestamp Addend register. This register value is used only when the system time is configured for Fine Update mode (TSCFUPDT bit in the MAC_Timestamp_Control register)
GMAC_MAC_TIMESTAMP_STATUS	0x0B20	W	0x00000000	Timestamp Status register. All bits except Bits[27:25] gets cleared when the application reads this register
GMAC_MAC_TX_TS_STATUS_NS	0x0B30	W	0x00000000	This register contains the nanosecond part of timestamp captured for Transmit packets when Tx status is disabled
GMAC_MAC_TX_TS_STATUS_SECS	0x0B34	W	0x00000000	The register contains the higher 32 bits of the timestamp (in seconds) captured when a PTP packet is transmitted
GMAC_MAC_AUXILIARY_CONTROL	0x0B40	W	0x00000000	The Auxiliary Timestamp Control register controls the Auxiliary Timestamp snapshot
GMAC_MAC_AUXILIARY_TS_NS	0x0B48	W	0x00000000	The Auxiliary Timestamp Nanoseconds register, along with MAC_Auxiliary_Timestamp_Seconds, gives the 64-bit timestamp stored as auxiliary snapshot
GMAC_MAC_AUXILIARY_TS_SECS	0x0B4C	W	0x00000000	The Auxiliary Timestamp - Seconds register contains the lower 32 bits of the Seconds field of the auxiliary timestamp register
GMAC_MAC_TS_INGRESS_CORR_NS	0x0B58	W	0x00000000	This register contains the correction value in nanoseconds to be used with the captured timestamp value in the ingress path
GMAC_MAC_TS_EGRESS_CORR_NS	0x0B5C	W	0x00000000	This register contains the correction value in nanoseconds to be used with the captured timestamp value in the egress path
GMAC_MAC_TS_INGRESS_LATENCY	0x0B68	W	0x00000000	This register holds the Ingress MAC latency
GMAC_MAC_TS_EGRESS_LATENCY	0x0B6C	W	0x00000000	This register holds the Egress MAC latency
GMAC_MAC_PPS_CONTROL	0x0B70	W	0x00000000	PPS Control register

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_PPS0_TARGET_TIME_SECONDS	0x0B80	W	0x00000000	The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers
GMAC_MAC_PPS0_TARGET_TIME_NS	0x0B84	W	0x00000000	PPS0 Target Time Nanoseconds register
GMAC_MAC_PPS0_INTERVAL	0x0B88	W	0x00000000	The PPS0 Interval register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output (ptp_pps_o[0])
GMAC_MAC_PPS0_WIDTH	0x0B8C	W	0x00000000	The PPS0 Width register contains the number of units of sub-second increment value
GMAC_MTL_OPERATION_MODE	0x0C00	W	0x00000000	The Operation Mode register establishes the Transmit and Receive operating modes and commands
GMAC_MTL_DBG_CTL	0x0C08	W	0x00000000	The FIFO Debug Access Control and Status register controls the operation mode of FIFO debug access
GMAC_MTL_DBG_STS	0x0C0C	W	0x01900000	The FIFO Debug Status register contains the status of FIFO debug access
GMAC_MTL_FIFO_DEBUG_DATA	0x0C10	W	0x00000000	The FIFO Debug Data register contains the data to be written to or read from the FIFOs
GMAC_MTL_INTERRUPT_STATUS	0x0C20	W	0x00000000	The software driver (application) reads this register during interrupt service routine or polling to determine the interrupt status of MTL queues and the MAC
GMAC_MTL_RXQ_DMA_MAP0	0x0C30	W	0x00000000	The Receive Queue and DMA Channel Mapping 0 register is reserved in EQOS-CORE and EQOS-MTL configurations
GMAC_MTL_TBS_CTRL	0x0C40	W	0x00000000	This register controls the operation of Time Based Scheduling
GMAC_MTL_EST_CONTROL	0x0C50	W	0x00000000	This register controls the operation of Enhancements to Scheduled Transmission (IEEE802.1Qbv)
GMAC_MTL_EST_STATUS	0x0C58	W	0x00000000	This register provides Status related to Enhancements to Scheduled Transmission

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Name	Offset	Size	Reset Value	Description
GMAC_MTL_EST_SCH_ERROR	0x0C60	W	0x00000000	This register provides the One Hot encoded Queue Numbers that are having the Scheduling related error (timeout)
GMAC_MTL_EST_FRM_SIZE_ERROR	0x0C64	W	0x00000000	This register provides the One Hot encoded Queue Numbers that are having the Frame
GMAC_MTL_EST_FRM_SIZE_CAPTURE	0x0C68	W	0x00000000	This register captures the Frame Size and Queue Number of the first occurrence of the Frame Size related error. Up on clearing it captures the data of immediate next occurrence of a similar error
GMAC_MTL_EST_INTR_ENABLE	0x0C70	W	0x00000000	This register implements the Interrupt Enable bits for the various events that generate an interrupt. Bit positions have a 1 to 1 correlation with the status bit positions in MTL_ETS_Status
GMAC_MTL_EST_GCL_CONTROL	0x0C80	W	0x00000000	This register provides the control information for reading/writing to the Gate Control lists
GMAC_MTL_EST_GCL_DATA	0x0C84	W	0x00000000	This register holds the read data or write data in case of reads and writes respectively
GMAC_MTL_FPE_CTRL_STS	0x0C90	W	0x00000000	This register controls the operation of, and provides status for Frame Preemption (IEEE802.1Qbu/802.3br)
GMAC_MTL_FPE_ADVANCE	0x0C94	W	0x00000000	This register holds the Hold and Release Advance time
GMAC_MTL_TXQ0_OPERATION_MODE	0x0D00	W	0x00060000	The Queue 0 Transmit Operation Mode register establishes the Transmit queue operating modes and commands
GMAC_MTL_TXQ0_UNDERFLOW	0x0D04	W	0x00000000	The Queue 0 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush
GMAC_MTL_TXQ0_DEBUG	0x0D08	W	0x00000000	The Queue 0 Transmit Debug register gives the debug status of various blocks related to the Transmit queue
GMAC_MTL_TXQ0_ETS_STATUS	0x0D14	W	0x00000000	The Queue 0 ETS Status register provides the average traffic transmitted in Queue 0
GMAC_MTL_TXQ0_QUANTUM_WEIGHT	0x0D18	W	0x00000000	The Queue 0 Quantum or Weights register contains the quantum value for Deficit Weighted Round Robin (DWRR), weights for the Weighted Round Robin (WRR), and Weighted Fair Queuing (WFQ) for Queue 0

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Name	Offset	Size	Reset Value	Description
GMAC_MTL_Q0_INTERRUPT_CTRL_STATUS	0x0D2C	W	0x00000000	This register contains the interrupt enable and status bits for the queue 0 interrupts
GMAC_MTL_RXQ0_OPERATION_MODE	0x0D30	W	0x00000000	The Queue 0 Receive Operation Mode register establishes the Receive queue operating modes and command
GMAC_MTL_RXQ0_MISS_PKT_OVF_CNT	0x0D34	W	0x00000000	The Queue 0 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow
GMAC_MTL_RXQ0_DEBUG	0x0D38	W	0x00000000	The Queue 0 Receive Debug register gives the debug status of various blocks related to the Receive queue
GMAC_MTL_RXQ0_CONTROL	0x0D3C	W	0x00000000	The Queue Receive Control register controls the receive arbitration and passing of received packets to the application
GMAC_DMA_MODE	0x1000	W	0x00000000	The Bus Mode register establishes the bus operating modes for the DMA
GMAC_DMA_SYSBUS_MODE	0x1004	W	0x00010000	The System Bus mode register controls the behavior of the AHB or AXI master
GMAC_DMA_INTERRUPT_STATUS	0x1008	W	0x00000000	The application reads this Interrupt Status register during interrupt service routine or polling to determine the interrupt status of DMA channels, MTL queues, and the MAC
GMAC_DMA_DEBUG_STATUS0	0x100C	W	0x00000000	The Debug Status 0 register gives the Receive and Transmit process status for DMA Channel 0-Channel 2 for debugging purpose
GMAC_AXI_LPI_ENTRY_INTERVAL	0x1040	W	0x00000000	This register is used to control the AXI LPI entry interval
GMAC_DMA_TBS_CTRL	0x1050	W	0x00000000	This register is used to control the TBS attributes
GMAC_DMA_CH0_CONTROL	0x1100	W	0x00000000	The register specifies the MSS value for segmentation, length to skip between two descriptors, and 8xPBL mode
GMAC_DMA_CH0_TX_CONTROL	0x1104	W	0x00000000	The register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights
GMAC_DMA_CH0_RX_CONTROL	0x1108	W	0x00000000	The DMA Channel0 Receive Control register controls the Rx features such as PBL, buffer size, and extended status

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Name	Offset	Size	Reset Value	Description
GMAC_DMA_CH0_TXDESC_LIST_HADDRESS	0x1110	W	0x00000000	The Channel0 Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start
GMAC_DMA_CH0_TXDESC_LIST_ADDRESS	0x1114	W	0x00000000	The Channel0 Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list
GMAC_DMA_CH0_RXDESC_LIST_HADDRESS	0x1118	W	0x00000000	The Channel0 Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start
GMAC_DMA_CH0_RXDESC_LIST_ADDRESS	0x111C	W	0x00000000	The Channel0 Rx Descriptor List Address register points the DMA to the start of Receive descriptor list
GMAC_DMA_CH0_TXDESC_TAIL_POINTER	0x1120	W	0x00000000	The Channel0 Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor
GMAC_DMA_CH0_RXDESC_TAIL_POINTER	0x1128	W	0x00000000	The Channel0 Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor
GMAC_DMA_CH0_TXDESC_RING_LENGTH	0x112C	W	0x00000000	The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring
GMAC_DMA_CH0_RXDESC_RING_LENGTH	0x1130	W	0x00000000	The Channel0 Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring
GMAC_DMA_CH0_INTERRUPT_ENABLE	0x1134	W	0x00000000	The Channel0 Interrupt Enable register enables the interrupts reported by the Status register
GMAC_DMA_CH0_RX_INTERRUPT_WD_TIMER	0x1138	W	0x00000000	The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA
GMAC_DMA_CH0_SLOT_FUNC_CTRL_STATUS	0x113C	W	0x000007C0	The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path
GMAC_DMA_CH0_CURRENT_APP_TXDESC	0x1144	W	0x00000000	The Channel0 Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA
GMAC_DMA_CH0_CURRENT_APP_RXDESC	0x114C	W	0x00000000	The Channel0 Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA
GMAC_DMA_CH0_CURRENT_APP_TXBUFFER_H	0x1150	W	0x00000000	The Channel0 Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA

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Name	Offset	Size	Reset Value	Description
GMAC_DMA_CH0_CURRENT_APP_TXBUFFER	0x1154	W	0x00000000	The Channel0 Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA
GMAC_DMA_CH0_CURRENT_APP_RXBUFFER_H	0x1158	W	0x00000000	The Channel0 Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA
GMAC_DMA_CH0_CURRENT_APP_RXBUFFER	0x115C	W	0x00000000	The Channel0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA
GMAC_DMA_CH0_STATUS	0x1160	W	0x00000000	The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA
GMAC_DMA_CH0_MISS_FRAME_CNT	0x1164	W	0x00000000	This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH0_Rx_Control register
GMAC_DMA_CH0_RX_ERI_CNT	0x1168	W	0x00000000	The DMA_CH0_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted
GMAC_MAC_ADDRESS1_HIGH	0x0308	W	0x0000FFFF	The MAC Address1 High register holds the upper 16 bits of the first 6-byte MAC address of the station
GMAC_MAC_ADDRESS1_LOW	0x030C	W	0xFFFFFFFF	The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station
GMAC_MAC_ADDRESS2_HIGH	0x0310	W	0x0000FFFF	The MAC Address2 High register holds the upper 16 bits of the first 6-byte MAC address of the station
GMAC_MAC_ADDRESS2_LOW	0x0314	W	0xFFFFFFFF	The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station
GMAC_MAC_ADDRESS3_HIGH	0x0318	W	0x0000FFFF	The MAC Address3 High register holds the upper 16 bits of the first 6-byte MAC address of the station
GMAC_MAC_ADDRESS3_LOW	0x031C	W	0xFFFFFFFF	The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station
GMAC_MAC_L3_L4_CONTROL1	0x0930	W	0x00000000	The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_LAYER4_ADDRESS1	0x0934	W	0x00000000	The MAC_Layer4_Address1, MAC_L3_L4_Control1, MAC_Layer3_Addr0_Reg1, MAC_Layer3_Addr1_Reg1, MAC_Layer3_Addr2_Reg1 and MAC_Layer3_Addr3_Reg1 registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core
GMAC_MAC_LAYER3_ADDR0_REG1	0x0940	W	0x00000000	For IPv4 packets, the Layer 3 Address 0 Register 1 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field
GMAC_MAC_LAYER3_ADDR1_REG1	0x0944	W	0x00000000	For IPv4 packets, the Layer 3 Address 1 Register 1 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field
GMAC_MAC_LAYER3_ADDR2_REG1	0x0948	W	0x00000000	The Layer 3 Address 2 Register 1 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field
GMAC_MAC_LAYER3_ADDR3_REG1	0x094C	W	0x00000000	The Layer 3 Address 3 Register 1 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field
GMAC_MTL_TXQ1_OPERATION_MODE	0x0D40	W	0x00060000	The Queue 1 Transmit Operation Mode register establishes the Transmit queue operating modes and commands
GMAC_MTL_TXQ1_UNDERFLOW	0x0D44	W	0x00000000	The Queue 1 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush
GMAC_MTL_TXQ1_DEBUG	0x0D48	W	0x00000000	The Queue 1 Transmit Debug register gives the debug status of various blocks related to the Transmit queue
GMAC_MTL_TXQ1_ETS_CONTROL	0x0D50	W	0x00000000	The Queue ETS Control register controls the enhanced transmission selection operation

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Name	Offset	Size	Reset Value	Description
GMAC_MTL_TXQ1_ETS_STATUS	0x0D54	W	0x00000000	The Queue 1 ETS Status register provides the average traffic transmitted in Queue 1
GMAC_MTL_TXQ1_QUANTUM_WEIGHT	0x0D58	W	0x00000000	The Queue 1 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 1
GMAC_MTL_TXQ1_SENDSLOPECREDIT	0x0D5C	W	0x00000000	The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue
GMAC_MTL_TXQ1_HICREDIT	0x0D60	W	0x00000000	The hiCredit register contains the hiCredit value required for the credit-based shaper
GMAC_MTL_TXQ1_LOCREDIT	0x0D64	W	0x00000000	The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue
GMAC_MTL_Q1_INTERRUPT_CTRL_STATUS	0x0D6C	W	0x00000000	This register contains the interrupt enable and status bits for the queue 1 interrupts
GMAC_MTL_RXQ1_OPERATION_MODE	0x0D70	W	0x00000000	The Queue 1 Receive Operation Mode register establishes the Receive queue operating modes and command
GMAC_MTL_RXQ1_MISS_PKT_OVF_CNT	0x0D74	W	0x00000000	The Queue 1 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow
GMAC_MTL_RXQ1_DEBUG	0x0D78	W	0x00000000	The Queue 1 Receive Debug register gives the debug status of various blocks related to the Receive queue
GMAC_MTL_RXQ1_CONTROL	0x0D7C	W	0x00000000	The Queue Receive Control register controls the receive arbitration and passing of received packets to the application
GMAC_DMA_CH1_CONTROL	0x1180	W	0x00000000	The register specifies the MSS value for segmentation, length to skip between two descriptors, and 8xPBL mode
GMAC_DMA_CH1_TX_CONTROL	0x1184	W	0x00000000	The register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights
GMAC_DMA_CH1_RX_CONTROL	0x1188	W	0x00000000	The DMA Channel1 Receive Control register controls the Rx features such as PBL, buffer size, and extended status

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Name	Offset	Size	Reset Value	Description
GMAC_DMA_CH1_TXDESC_LIST_HADDRESS	0x1190	W	0x00000000	The Channel1 Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list
GMAC_DMA_CH1_TXDESC_LIST_ADDRESS	0x1194	W	0x00000000	The Channel1 Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list
GMAC_DMA_CH1_RXDESC_LIST_HADDRESS	0x1198	W	0x00000000	The Channel1 Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list
GMAC_DMA_CH1_RXDESC_LIST_ADDRESS	0x119C	W	0x00000000	The Channel1 Rx Descriptor List Address register points the DMA to the start of Receive descriptor list
GMAC_DMA_CH1_TXDESC_TAIL_POINTER	0x11A0	W	0x00000000	The Channel1 Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor
GMAC_DMA_CH1_RXDESC_TAIL_POINTER	0x11A8	W	0x00000000	The Channel1 Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor
GMAC_DMA_CH1_TXDESC_RING_LENGTH	0x11AC	W	0x00000000	The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring
GMAC_DMA_CH1_RXDESC_RING_LENGTH	0x11B0	W	0x00000000	The Channel1 Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring
GMAC_DMA_CH1_INTERRUPT_ENABLE	0x11B4	W	0x00000000	The Channel1 Interrupt Enable register enables the interrupts reported by the Status register
GMAC_DMA_CH1_RX_INTERRUPT_WD_TIMER	0x11B8	W	0x00000000	The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA
GMAC_DMA_CH1_SLOT_FUNC_CTRL_STATUS	0x11BC	W	0x000007C0	The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path
GMAC_DMA_CH1_CURRENT_APP_TXDESC	0x11C4	W	0x00000000	The Channel1 Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA
GMAC_DMA_CH1_CURRENT_APP_RXDESC	0x11CC	W	0x00000000	The Channel1 Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA

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Name	Offset	Size	Reset Value	Description
GMAC_DMA_CH1_CURRENT_APP_TXBUFFER_H	0x11D0	W	0x00000000	The Channel1 Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA
GMAC_DMA_CH1_CURRENT_APP_TXBUFFER	0x11D4	W	0x00000000	The Channel1 Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA
GMAC_DMA_CH1_CURRENT_APP_RXBUFFER_H	0x11D8	W	0x00000000	The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA
GMAC_DMA_CH1_CURRENT_APP_RXBUFFER	0x11DC	W	0x00000000	The Channel1 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA
GMAC_DMA_CH1_STATUS	0x11E0	W	0x00000000	The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA
GMAC_DMA_CH1_MISS_FRAME_CNT	0x11E4	W	0x00000000	This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH1_Rx_Control register
GMAC_DMA_CH1_RX_ERI_CNT	0x11E8	W	0x00000000	The DMA_CH1_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

8.4.3 Detail Registers Description

GMAC_MAC_CONFIGURATION

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	ARPEN ARP Offload Enable When this bit is set, the MAC can recognize an incoming ARP request packet and schedules the ARP packet for transmission. It forwards the ARP packet to the application and also indicate the events in the RxStatus. When this bit is reset, the MAC receiver does not recognize any ARP packet and indicates them as Type frame in the RxStatus. This bit is available only when the Enable IPv4 ARP Offload is selected. Values: 1'b0: ARP Offload is disabled 1'b1: ARP Offload is enabled

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Bit	Attr	Reset Value	Description
30:28	RW	0x0	SARC Source Address Insertion or Replacement Control This field controls the source address insertion or replacement for all transmitted packets. Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits[29:28]: 2'b0x: The mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation. 2'b10: 1.If Bit 30 is set to 0, the MAC inserts the content of the MAC Address 0 registers in the SA field of all transmitted packets. 2.If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected while configuring the core, the MAC inserts the content of the MAC Address 1 registers in the SA field of all transmitted packets. 2'b11: 1.If Bit 30 is set to 0, the MAC replaces the content of the MAC Address 0 registers in the SA field of all transmitted packets. 2.If Bit 30 is set to 1 and the MAC Address Register 1 is enabled, the MAC replaces the content of the MAC Address 1 registers in the SA field of all transmitted packets. Note: Changes to this field take effect only on the start of a packet. If you write to this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. 0x0 (SA_CTRL_IN): mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation 0x2 (MAC0_INS_SA): Contents of MAC Addr-0 inserted in SA field 0x3 (MAC0_REP_SA): Contents of MAC Addr-0 replaces SA field 0x6 (MAC1_INS_SA): Contents of MAC Addr-1 inserted in SA field 0x7 (MAC1_REP_SA): Contents of MAC Addr-1 replaces SA field
27	RW	0x0	IPC Checksum Offload When set, this bit enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled.The Layer 3 and Layer 4 Packet Filter and Enable Split Header features automatically selects the IPC Full Checksum Offload Engine on the Receive side. When any of these features are enabled, you must set the IPC bit. Values: 1'b0: IP header/payload checksum checking is disabled 1'b1: IP header/payload checksum checking is enabled

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Bit	Attr	Reset Value	Description
26:24	RW	0x0	IPG Inter-Packet Gap These bits control the minimum IPG between packets during transmission. This range of minimum IPG is valid in full-duplex mode.In the half-duplex mode, the minimum IPG can be configured only for 64-bit times (IPG = 100). Lower values are not considered. When a JAM pattern is being transmitted because of backpressure activation, the MAC does not consider the minimum IPG.The above function (IPG less than 96 bit times) is valid only when EIPGEN bit in MAC_Ext_Configuration register is reset. When EIPGEN is set, then the minimum IPG (greater than 96 bit times) is controlled as per the description given in EIPG field in MAC_Ext_Configuration register. Values: 3'b000: 96 bit times IPG 3'b001: 88 bit times IPG 3'b010: 80 bit times IPG 3'b011: 72 bit times IPG 3'b100: 64 bit times IPG 3'b101: 56 bit times IPG 3'b110: 48 bit times IPG 3'b111: 40 bit times IPG
23	RW	0x0	GPSLCE Giant Packet Size Limit Control Enable When this bit is set, the MAC considers the value in GPSL field in MAC_Ext_Configuration register to declare a received packet as Giant packet. This field must be programmed to more than 1,518 bytes. Otherwise, the MAC considers 1,518 bytes as giant packet limit. When this bit is reset, the MAC considers a received packet as Giant packet when its size is greater than 1,518 bytes (1522 bytes for tagged packet).The watchdog timeout limit, Jumbo Packet Enable and 2K Packet Enable have higher precedence over this bit, that is the MAC considers a received packet as Giant packet when its size is greater than 9,018 bytes (9,022 bytes for tagged packet) with Jumbo Packet Enabled and greater than 2,000 bytes with 2K Packet Enabled. The watchdog timeout, if enabled, terminates the received packet when watchdog limit is reached. Therefore, the programmed giant packet limit should be less than the watchdog limit to get the giant packet status. Values: 1'b0: Giant Packet Size Limit Control is disabled 1'b1: Giant Packet Size Limit Control is enabled
22	RW	0x0	S2KP IEEE 802.3as Support for 2K Packets When this bit is set, the MAC considers all packets with up to 2,000 bytes length as normal packets. When the JE bit is not set, the MAC considers all received packets of size more than 2K bytes as Giant packets.When this bit is reset and the JE bit is not set, the MAC considers all received packets of size more than 1,518 bytes (1,522 bytes for tagged) as giant packets. Note: When the JE bit is set, setting this bit has no effect on the giant packet status. Values: 1'b0: Support upto 2K packet is disabled 1'b1: Support upto 2K packet is Enabled

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Bit	Attr	Reset Value	Description
21	RW	0x0	CST CRC stripping for Type packets When this bit is set, the last four bytes (FCS) of all packets of Ether type (type field greater than 1,536) are stripped and dropped before forwarding the packet to the application. Note: For information about how the settings of the ACS bit and this bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bits. Values: 1'b0: CRC stripping for Type packets is disabled 1'b1: CRC stripping for Type packets is enabled
20	RW	0x0	ACS Automatic Pad or CRC Stripping When this bit is set, the MAC strips the Pad or FCS field on the incoming packets only if the value of the length field is less than 1,536 bytes. All received packets with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field.When this bit is reset, the MAC passes all incoming packets to the application, without any modification. Note: For information about how the settings of CST bit and this bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bit. Values: 1'b0: Automatic Pad or CRC Stripping is disabled 1'b1: Automatic Pad or CRC Stripping is enabled
19	RW	0x0	WD Watchdog Disable When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive packets of up to 16,383 bytes.When this bit is reset, the MAC does not allow more than 2,048 bytes (10,240 if JE is set high) of the packet being received. The MAC cuts off any bytes received after 2,048 bytes. Values: 1'b0: Watchdog is enabled 1'b1: Watchdog is disabled
18	RW	0x0	BE Packet Burst Enable When this bit is set, the MAC allows packet bursting during transmission in the GMII half-duplex mode. Values: 1'b0: Packet Burst is disabled 1'b1: Packet Burst is enabled
17	RW	0x0	JD Jabber Disable When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer packets of up to 16,383 bytes. When this bit is reset, if the application sends more than 2,048 bytes of data (10,240 if JE is set high) during transmission, the MAC does not send rest of the bytes in that packet. Values: 1'b0: Jabber is enabled 1'b1: Jabber is disabled

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Bit	Attr	Reset Value	Description
16	RW	0x0	JE Jumbo Packet Enable When this bit is set, the MAC allows jumbo packets of 9,018 bytes (9,022 bytes for VLAN tagged packets) without reporting a giant packet error in the Rx packet status. Values: 1'b0: Jumbo packet is disabled 1'b1: Jumbo packet is enabled
15	RW	0x0	PS Port Select This bit selects the Ethernet line speed. This bit, along with Bit 14, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only (RO) with appropriate value. In default 10/100/1000 Mbps configurations, this bit is read-write (R/W). The mac_speed_o[1] signal reflects the value of this bit. Values: 1'b0: For 1000 or 2500 Mbps operations 1'b1: For 10 or 100 Mbps operations
14	RW	0x0	FES Speed This bit selects the speed mode. The mac_speed_o[0] signal reflects the value of this bit. Values: 1'b0: 10 Mbps when PS bit is 1 and 1 Gbps when PS bit is 0 1'b1: 100 Mbps when PS bit is 1 and 2.5 Gbps when PS bit is 0
13	RW	0x0	DM Duplex Mode When this bit is set, the MAC operates in the full-duplex mode in which it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configurations. Values: 1'b0: Half-duplex mode 1'b1: Full-duplex mode
12	RW	0x0	LM Loopback Mode When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Rx clock input (clk_rx_i) is required for the loopback to work properly. This is because the Tx clock is not internally looped back. Values: 1'b0: Loopback is disabled 1'b1: Loopback is enabled
11	RW	0x0	ECRSFD Enable Carrier Sense Before Transmission in Full-Duplex Mode When this bit is set, the MAC transmitter checks the CRS signal before packet transmission in the full-duplex mode. The MAC starts the transmission only when the CRS signal is low.When this bit is reset, the MAC transmitter ignores the status of the CRS signal. Values: 1'b0: ECRSFD is disabled 1'b1: ECRSFD is enabled

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Bit	Attr	Reset Value	Description
10	RW	0x0	DO Disable Receive Own When this bit is set, the MAC disables the reception of packets when the gmii_txen_o is asserted in the half-duplex mode. When this bit is reset, the MAC receives all packets given by the PHY.This bit is not applicable in the full-duplex mode. Values: 1'b0: Enable Receive Own 1'b1: Disable Receive Own
9	RW	0x0	DCRS Disable Carrier Sense During Transmission When this bit is set, the MAC transmitter ignores the (G)MII CRS signal during packet transmission in the half-duplex mode. As a result, no errors are generated because of Loss of Carrier or No Carrier during transmission. When this bit is reset, the MAC transmitter generates errors because of Carrier Sense. The MAC can even abort the transmission. Values: 1'b0: Enable Carrier Sense During Transmission 1'b1: Disable Carrier Sense During Transmission
8	RW	0x0	DR Disable Retry When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current packet transmission and reports a Packet Abort with excessive collision error in the Tx packet status.When this bit is reset, the MAC retries based on the settings of the BL field. This bit is applicable only in the half-duplex mode. Values: 1'b0: Enable Retry 1'b1: Disable Retry
7	RO	0x0	reserved
6:5	RW	0x0	BL Back-Off Limit The back-off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000/2500 Mbps; 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. n = retransmission attempt. The random integer r takes the value in the range 0 <= r < 2^k This bit is applicable only in the half-duplex mode. Values: 2'b00: k = min(n,10) 2'b01: k = min(n,8) 2'b10: k = min(n,4) 2'b11: k = min(n,1)

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Bit	Attr	Reset Value	Description
4	RW	0x0	DC Deferral Check When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Packet Abort status, along with the excessive deferral error bit set in the Tx packet status, when the Tx state machine is deferred for more than 24,288 bit times in 10 or 100 Mbps mode. If the MAC is configured for 1000/2500 Mbps operation, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0, and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode. Values: 1'b0: Deferral check function is disabled 1'b1: Deferral check function is enabled
3:2	RW	0x0	PRELEN Preamble Length for Transmit packets These bits control the number of preamble bytes that are added to the beginning of every Tx packet. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. Values: 2'b00: 7 bytes of preamble 2'b01: 5 bytes of preamble 2'b10: 3 bytes of preamble 2'b11: Reserved
1	RW	0x0	TE Transmitter Enable When this bit is set, the Tx state machine of the MAC is enabled for transmission on the GMII or MII interface. When this bit is reset, the MAC Tx state machine is disabled after it completes the transmission of the current packet. The Tx state machine does not transmit any more packets. Values: 1'b0: Transmitter is disabled 1'b1: Transmitter is enabled
0	RW	0x0	RE Receiver Enable When this bit is set, the Rx state machine of the MAC is enabled for receiving packets from the GMII or MII interface. When this bit is reset, the MAC Rx state machine is disabled after it completes the reception of the current packet. The Rx state machine does not receive any more packets from the GMII or MII interface. Values: 1'b0: Receiver is disabled 1'b1: Receiver is enabled

GMAC_MAC_EXT_CONFIGURATION

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Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	EIPG Extended Inter-Packet Gap The value in this field is applicable when the EIPGEN bit is set. This field (as Most Significant bits), along with IPG field in MAC_Configuration register, gives the minimum IPG greater than 96 bit times in steps of 8 bit times: {EIPG, IPG} 8'h00 - 104 bit times 8'h01 - 112 bit times 8'h02 - 120 bit times ---------- 8'hFF - 2144 bit times
24	RW	0x0	EIPGEN Extended Inter-Packet Gap Enable When this bit is set, the MAC interprets EIPG field and IPG field in MAC_Configuration register together as minimum IPG greater than 96 bit times in steps of 8 bit times. When this bit is reset, the MAC ignores EIPG field and interprets IPG field in MAC_Configuration register as minimum IPG less than or equal to 96 bit times in steps of 8 bit times. Note: The extended Inter-Packet Gap feature must be enabled when operating in Full-Duplex mode only. There may be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode. Values: 1'b0: Extended Inter-Packet Gap is disabled 1'b1: Extended Inter-Packet Gap is enabled
23	RO	0x0	reserved
22:20	RW	0x0	HDSMS Maximum Size for Splitting the Header Data These bits indicate the maximum header size allowed for splitting the header data in the received packet. Values: 0x0 (64BYTES): Maximum Size for Splitting the Header Data is 64 bytes 0x1 (128BYTES): Maximum Size for Splitting the Header Data is 128 bytes 0x2 (256BYTES): Maximum Size for Splitting the Header Data is 256 bytes 0x3 (512BYTES): Maximum Size for Splitting the Header Data is 512 bytes 0x4 (1024BYTES): Maximum Size for Splitting the Header Data is 1024 bytes 0x5 (RSVD): Reserved
19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18	RW	0x0	USP Unicast Slow Protocol Packet Detect When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC_Address0_High and MAC_Address0_Low registers. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). When this bit is reset, the MAC detects only Slow Protocol packets with the Slow Protocol multicast address specified in the IEEE 802.3-2015, Section 5. Values: 1'b0: Unicast Slow Protocol Packet Detection is disabled 1'b1: Unicast Slow Protocol Packet Detection is enabled
17	RW	0x0	SPEN Slow Protocol Detection Enable When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Rx status. The MAC discards the Slow Protocol packets with invalid sub-types. When this bit is reset, the MAC forwards all error-free Slow Protocol packets to the application. The MAC considers such packets as normal Type packets. Values: 1'b0: Slow Protocol Detection is disabled 1'b1: Slow Protocol Detection is enabled
16	RW	0x0	DCRCC Disable CRC Checking for Received Packets When this bit is set, the MAC receiver does not check the CRC field in the received packets. When this bit is reset, the MAC receiver always checks the CRC field in the received packets. Values: 1'b0: CRC Checking is enabled 1'b1: CRC Checking is disabled
15:14	RO	0x0	reserved
13:0	RW	0x0000	GPSL Giant Packet Size Limit If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value. When the Enable Double VLAN Processing option is selected, the MAC adds 8 bytes to the programmed value for double VLAN tagged packets. The value in this field is applicable when the GPSLCE bit is set in MAC_Configuration register.

GMAC_MAC_PACKET_FILTER

Address: **Operational Base** + offset (0x0008)

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Bit	Attr	Reset Value	Description
31	RW	0x0	RA Receive All When this bit is set, the MAC Receiver module passes all received packets to the application, irrespective of whether they pass the address filter or not. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bit in the Rx Status Word. When this bit is reset, the Receiver module passes only those packets to the application that pass the SA or DA address filter. 0x0 (DISABLE): Receive All is disabled 0x1 (ENABLE): Receive All is enabled
30:22	RO	0x000	reserved
21	RW	0x0	DNTU Drop Non-TCP/UDP over IP Packets When this bit is set, the MAC drops the non-TCP or UDP over IP packets. The MAC forward only those packets that are processed by the Layer 4 filter. When this bit is reset, the MAC forwards all non-TCP or UDP over IP packets. 0x0 (FWD): Forward Non-TCP/UDP over IP Packets 0x1 (DROP): Drop Non-TCP/UDP over IP Packets
20	RW	0x0	IPFE Layer 3 and Layer 4 Filter Enable When this bit is set, the MAC drops packets that do not match the enabled Layer 3 and Layer 4 filters. If Layer 3 or Layer 4 filters are not enabled for matching, this bit does not have any effect. When this bit is reset, the MAC forwards all packets irrespective of the match status of the Layer 3 and Layer 4 fields. 0x0 (DISABLE): Layer 3 and Layer 4 Filters are disabled 0x1 (ENABLE): Layer 3 and Layer 4 Filters are enabled
19:17	RO	0x0	reserved
16	RW	0x0	VTFE VLAN Tag Filter Enable When this bit is set, the MAC drops the VLAN tagged packets that do not match the VLAN Tag. When this bit is reset, the MAC forwards all packets irrespective of the match status of the VLAN Tag. Values: 1'b0: VLAN Tag Filter is disabled 1'b1: VLAN Tag Filter is enabled
15:11	RO	0x00	reserved
10	RW	0x0	HPF Hash or Perfect Filter When this bit is set, the address filter passes a packet if it matches either the perfect filtering or hash filtering as set by the HMC or HUC bit. When this bit is reset and the HUC or HMC bit is set, the packet is passed only if it matches the Hash filter. Values: 1'b0: Hash or Perfect Filter is disabled 2'b1: Hash or Perfect Filter is enabled

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Bit	Attr	Reset Value	Description
9	RW	0x0	SAF Source Address Filter Enable When this bit is set, the MAC compares the SA field of the received packets with the values programmed in the enabled SA registers. If the comparison fails, the MAC drops the packet. When this bit is reset, the MAC forwards the received packet to the application with updated SAF bit of the Rx Status depending on the SA address comparison. Note: According to the IEEE specification, Bit 47 of the SA is reserved. However, in DWC_ether_qos, the MAC compares all 48 bits. The software driver should take this into consideration while programming the MAC address registers for SA. 0x0 (DISABLE): SA Filtering is disabled 0x1 (ENABLE): SA Filtering is enabled
8	RW	0x0	SAIF SA Inverse Filtering When this bit is set, the Address Check block operates in the inverse filtering mode for SA address comparison. If the SA of a packet matches the values programmed in the SA registers, it is marked as failing the SA Address filter. When this bit is reset, if the SA of a packet does not match the values programmed in the SA registers, it is marked as failing the SA Address filter. 0x0 (DISABLE): SA Inverse Filtering is disabled 0x1 (ENABLE): SA Inverse Filtering is enabled
7:6	RW	0x0	PCF Pass Control Packets These bits control the forwarding of all control packets (including unicast and multicast Pause packets). Values: 2'b00: MAC filters all control packets from reaching the application 2'b01: MAC forwards all control packets except Pause packets to the application even if they fail the Address filter 2'b10: MAC forwards all control packets to the application even if they fail the Address filter 2'b11: MAC forwards the control packets that pass the Address filter
5	RW	0x0	DBF Disable Broadcast Packets When this bit is set, the AFM module blocks all incoming broadcast packets. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast packets. Values: 1'b0: Enable Broadcast Packets 1'b1: Disable Broadcast Packets
4	RW	0x0	PM Pass All Multicast When this bit is set, it indicates that all received packets with a multicast destination address (first bit in the destination address field is '1') are passed. When this bit is reset, filtering of multicast packet depends on HMC bit. Values: 1'b0: Pass All Multicast is disabled 1'b1: Pass All Multicast is enabled

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Bit	Attr	Reset Value	Description
3	RW	0x0	DAIF DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast packets. When this bit is reset, normal filtering of packets is performed. Values: 1'b0: DA Inverse Filtering is disabled 1'b1: DA Inverse Filtering is enabled
2	RW	0x0	HMC Hash Multicast When this bit is set, the MAC performs the destination address filtering of received multicast packets according to the hash table. When this bit is reset, the MAC performs the perfect destination address filtering for multicast packets, that is, it compares the DA field with the values programmed in DA registers. Values: 1'b0: Hash Multicast is disabled 1'b1: Hash Multicast is enabled
1	RW	0x0	HUC Hash Unicast When this bit is set, the MAC performs the destination address filtering of unicast packets according to the hash table. When this bit is reset, the MAC performs a perfect destination address filtering for unicast packets, that is, it compares the DA field with the values programmed in DA registers. Values: 1'b0: Hash Unicast is disabled 1'b1: Hash Unicast is enabled
0	RW	0x0	PR Promiscuous Mode When this bit is set, the Address Filtering module passes all incoming packets irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Rx Status Word are always cleared when PR is set. Values: 1'b0: Promiscuous Mode is disabled 1'b1: Promiscuous Mode is enabled

GMAC_MAC_WATCHDOG_TIMEOUT

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	PWE Programmable Watchdog Enable Programmable Watchdog Enable When this bit is set and the WD bit of the MAC_Configuration register is reset, the WTO field is used as watchdog timeout for a received packet. When this bit is cleared, the watchdog timeout for a received packet is controlled by setting of WD and JE bits in MAC_Configuration register. Values: 1'b0: Programmable Watchdog is disabled 1'b1: Programmable Watchdog is enabled
7:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	WTO Watchdog Timeout When the PWE bit is set and the WD bit of the MAC_Configuration register is reset, this field is used as watchdog timeout for a received packet. If the length of a received packet exceeds the value of this field, such packet is terminated and declared as an error packet. Note: When the PWE bit is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE 802.3-specified valid tagged packets are declared as error packets and then dropped. Values: 4'b0000: 2 KB 4'b0001: 3 KB 4'b0010: 4 KB 4'b0011: 5 KB 4'b0100: 6 KB 4'b0101: 7 KB 4'b0110: 8 KB 4'b0111: 9 KB 4'b1000: 10 KB 4'b1001: 11 KB 4'b1010: 12 KB 4'b1011: 13 KB 4'b1100: 14 KB 4'b1101: 15 KB 4'b1110: 16383 Bytes 4'b1111: Reserved

GMAC_MAC_HASH_TABLE_REG0

Address: **Operational Base** + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HT31T0 MAC Hash Table First 32 Bits This field contains the first 32 Bits [31:0] of the Hash table. The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5. The hash value of the destination address is calculated in the following way: 1. Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32). 2. Perform bitwise reversal for the value obtained in Step 1. 3. Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2. If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values. If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the Hash Table Register X registers are written.If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

GMAC_MAC_HASH_TABLE_REG1

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HT63T32 MAC Hash Table Second 32 Bits This field contains the second 32 Bits [63:32] of the Hash table.

GMAC_MAC_HASH_TABLE_REG2

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HT95T64 MAC Hash Table Third 32 Bits This field contains the third 32 Bits [95:64] of the Hash table.

GMAC_MAC_VLAN_TAG_CTRL

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31	RW	0x0	EIVLRXS Enable Inner VLAN Tag in Rx Status When this bit is set, the MAC provides the inner VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the inner VLAN Tag in Rx status. 0x0 (DISABLE): Inner VLAN Tag in Rx status is disabled

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Bit	Attr	Reset Value	Description
			0x1 (ENABLE): Inner VLAN Tag in Rx status is enabled
30	RO	0x0	reserved
29:28	RW	0x0	EIVLS Enable Inner VLAN Tag Stripping on Receive This field indicates the stripping operation on inner VLAN Tag in received packet. 0x0 (DONOT): Do not strip 0x1 (IFPASS): Strip if VLAN filter passes 0x2 (IFFAIL): Strip if VLAN filter fails 0x3 (ALWAYS): Always strip
27	RW	0x0	ERIVLT Enable Inner VLAN Tag 0x0 (DISABLE): Inner VLAN tag is disabled 0x1 (ENABLE): Inner VLAN tag is enabled
26	RW	0x0	EDVLP Enable Double VLAN Processing When this bit is set, the MAC enables processing of up to two VLAN Tags on Tx and Rx (if present). When this bit is reset, the MAC enables processing of up to one VLAN Tag on Tx and Rx (if present). 0x0 (DISABLE): Double VLAN Processing is disabled 0x1 (ENABLE): Double VLAN Processing is enabled
25	RW	0x0	VTHM VLAN Tag Hash Table Match Enable When this bit is set, the most significant four bits of CRC of VLAN Tag (ones-complement of most significant four bits of CRC of VLAN Tag when ETV bit is reset) are used to index the content of the MAC_VLAN_Hash_Table register. A value of 1 in the VLAN Hash Table register, corresponding to the index, indicates that the packet matched the VLAN hash table. When the ETV bit is set, the CRC of the 12-bit VLAN Identifier (VID) is used for comparison. When the ETV bit is reset, the ones-complement of the CRC of the 16-bit VLAN tag is used for comparison. When this bit is reset, the VLAN Hash Match operation is not performed. 0x0 (DISABLE): VLAN Tag Hash Table Match is disabled 0x1 (ENABLE): VLAN Tag Hash Table Match is enabled
24	RW	0x0	EVLRXS Enable VLAN Tag in Rx status When this bit is set, MAC provides the outer VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the outer VLAN Tag in Rx status. Values: 1'b0: VLAN Tag in Rx status is disabled 1'b1: VLAN Tag in Rx status is enabled
23	RO	0x0	reserved
22:21	RW	0x0	EVLS Enable VLAN Tag Stripping on Receive This field indicates the stripping operation on the outer VLAN Tag in received packet. Values: 2'b00: Do not strip 2'b01: Strip if VLAN filter passes 2'b10: Strip if VLAN filter fails 2'b11: Always strip

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Bit	Attr	Reset Value	Description
20:19	RO	0x0	reserved
18	RW	0x0	ESVL Enable S-VLAN When this bit is set, the MAC transmitter and receiver consider the S-VLAN packets (Type = 0x88A8) as valid VLAN tagged packets. Values: 1'b0: S-VLAN is disabled 1'b1: S-VLAN is enabled
17	RW	0x0	VTIM VLAN Tag Inverse Match Enable When this bit is set, this bit enables the VLAN Tag inverse matching. The packets without matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The packets with matched VLAN Tag are marked as matched. Values: 1'b0: VLAN Tag Inverse Match is disabled 1'b1: VLAN Tag Inverse Match is enabled
16:7	RO	0x000	reserved
6:2	RW	0x00	OFS Offset This field holds the address offset of the MAC VLAN Tag Filter Register which the application is trying to access.The width of the field depends on the number of MAC VLAN Tag Registers enabled.
1	RW	0x0	CT Command Type This bit indicates if the current register access is a read or a write. When set, it indicate a read operation. When reset, it indicates a write operation. 0x0 (WRITE): Write operation 0x1 (READ): Read operation
0	RW	0x0	OB Operation Busy This bit is set along with a read or write command for initiating the indirect access to per VLAN Tag Filter register. This bit is reset when the read or write command to per VLAN Tag Filter indirect access register is complete. The next indirect register access can be initiated only after this bit is reset. During a write operation, the bit is reset only after the data has been written into the Per VLAN Tag register. During a read operation, the data should be read from the MAC_VLAN_Tag_Data register only after this bit is reset. 0x0 (DISABLE): Operation Busy is disabled 0x1 (ENABLE): Operation Busy is enabled

GMAC_MAC_VLAN_TAG_DATA

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25	RW	0x0	DMACHN DMA Channel Number The DMA Channel number to which the VLAN Tagged Frame is to be routed if it passes this VLAN Tag Filter is programmed in this field. If the Routing based on VLAN Tag Filter is not necessary, this field need not be programmed.
24	RW	0x0	DMACHEN DMA Channel Number Enable This bit is the Enable for the DMA Channel Number value programmed in the field DMACH. When this bit is reset, the Routing does not occur based on VLAN Filter result. The frame is routed based on DA Based DMA Channel Routing. 0x0 (DISABLE): DMA Channel Number is disabled 0x1 (ENABLE): DMA Channel Number is enabled
23:21	RO	0x0	reserved
20	RW	0x0	ERIVLT Enable Inner VLAN Tag Comparison This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit and the EDVLP field are set, the MAC receiver enables operation on the inner VLAN Tag (if present). When this bit is reset, the MAC receiver enables operation on the outer VLAN Tag (if present). 0x0 (DISABLE): Inner VLAN tag comparison is disabled 0x1 (ENABLE): Inner VLAN tag comparison is enabled
19	RW	0x0	ERSVLM Enable S-VLAN Match for received Frames This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC receiver enables filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables filtering or matching for C-VLAN (Type = 0x8100) packets. 0x0 (DISABLE): Receive S-VLAN Match is disabled 0x1 (ENABLE): Receive S-VLAN Match is enabled
18	RW	0x0	DOVLTC Disable VLAN Type Comparison This bit is valid only when VLAN Tag Enable of the Filter is set.When this bit is set, the MAC does not check whether the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC filters or matches the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit only when VLAN Tag type is similar to the one specified by the Enable S-VLAN Match for received Frames bit. 0x0 (ENABLE): VLAN type comparison is enabled 0x1 (DISABLE): VLAN type comparison is disabled
17	RW	0x0	ETV 12bits or 16bits VLAN comparison This bit is valid only when VEN of the Filter is set.When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged packet. 0x0 (16BIT): 16 bit VLAN comparison 0x1 (12BIT): 12 bit VLAN comparison

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Bit	Attr	Reset Value	Description
16	RW	0x0	VEN VLAN Tag Enable This bit is used to enable or disable the VLAN Tag.When this bit is set, the MAC compares the VLAN Tag of received packet with the VLAN Tag ID. When this bit is reset, no comparison is performed irrespective of the programming of the other fields. 0x0 (DISABLE): VLAN Tag is disabled 0x1 (ENABLE): VLAN Tag is enabled
15:0	RW	0x0000	VID VLAN Tag ID This field holds the VLAN Tag value which is used by the MAC for perfect comparison. It is valid when VLAN Tag Enable is set.

GMAC_MAC_VLAN_HASH_TABLE

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	VLHT VLAN Hash Table This field contains the 16-bit VLAN Hash Table. For hash filtering, the content of the 16-bit VLAN tag or 12-bit VLAN ID (based on the ETV bit of MAC_VLAN_Tag Register) in the incoming packet is passed through the CRC logic. When ETV bit of MAC_VLAN_Tag register is set, the upper four bits of the calculated CRC are used to index the contents of the VLAN Hash table. When ETV bit of MAC_VLAN_Tag register is reset, the ones-complement of upper four bits of the calculated CRC are used to index the contents of the VLAN Hash table. For example, when ETV bit is set a hash value of 4b'1000 selects Bit 8 of the VLAN Hash table, whereas when ETV bit is reset a hash value of 4b'1000 selects Bit 7 of the VLAN Hash table. The hash value of the destination address is calculated in the following way: 1.Calculate the 32-bit CRC for the VLAN tag or ID (For steps to calculate CRC32, see Section 3.2.8 of IEEE 802.3). 2.Perform bitwise reversal for the value obtained in step 1. 3.Take the upper four bits from the value obtained in step 2. If the VLAN hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[15:8] (in little-endian mode) or Bits[7:0] (in big-endian mode) of this register are written. 1.If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

GMAC_MAC_VLAN_INCL

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31	RO	0x0	BUSY Busy This bit indicates the status of the read/write operation of indirect access to the queue/channel specific VLAN inclusion register. For write operation write to a register is complete when this bit is reset. For read operation the read data is valid when the bit is reset.

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Bit	Attr	Reset Value	Description
			The application must make sure that this bit is reset before attempting subsequent access to this register. Values: 0x0 (INACTIVE): Busy status not detected 0x1 (ACTIVE): Busy status detected
30	RW	0x0	RDWR Read write control This bit controls the read or write operation for indirectly accessing the queue/channel specific VLAN Inclusion register. When set indicates write operation and when reset indicates read operation. This does not have any effect when CBTI is reset. Values: 0x0 (READ): Read operation of indirect access 0x1 (WRITE): Write operation of indirect access
29:25	RO	0x00	reserved
24	RW	0x0	ADDR Address This field selects one of the queue/channel specific VLAN Inclusion register for read/write access. This does not have any effect when CBTI is reset.
23:22	RO	0x0	reserved
21	RW	0x0	CBTI Channel based tag insertion When this bit is set, outer VLAN tag is inserted for every packets transmitted by the MAC. The tag value is taken from the queue/channel specific VLAN tag register. The VLTI, VLP, VLC, and VLT fields of this register are ignored when this bit is set. When this bit is set, a write operation to byte 3 of this register initiates the read/write access to the indirect register. When reset, outer VLAN operation is based on the setting of VLTI, VLP, VLC and VLT fields of this register.
20	RW	0x0	VLTI VLAN Tag Input When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from the following: 1.The mti_vlan_tag_i signal in EQOS-CORE configurations 2.The control word in EQOS-MTL configurations 3.The Tx descriptor in EQOS-AHB, EQOS-AXI, or EQOS-DMA configurations Values: 0x0 (DISABLE): VLAN Tag Input is disabled 0x1 (ENABLE): VLAN Tag Input is enabled
19	RW	0x0	CSVL C-VLAN or S-VLAN When this bit is set, S-VLAN type (0x88A8) is inserted or replaced in the 13th and 14th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted or replaced in the 13th and 14th bytes of transmitted packets. Values: 0x0 (C-VLAN): C-VLAN type (0x8100) is inserted or replaced 0x1 (S-VLAN): S-VLAN type (0x88A8) is inserted or replaced

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Bit	Attr	Reset Value	Description
18	RW	0x0	VLP VLAN Priority Control When this bit is set, the control bits[17:16] are used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and bits[17:16] are ignored. Values: 0x0 (DISABLE): VLAN Priority Control is disabled 0x1 (ENABLE): VLAN Priority Control is enabled
17:16	RW	0x0	VLC VLAN Tag Control in Transmit Packets 2'b00: No VLAN tag deletion, insertion, or replacement 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 13 and 14) and VLAN tag (bytes 15 and 16) of all transmitted packets with VLAN tags. 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 15 and 16 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 13 and 14. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 15 and 16 of all VLAN-type transmitted packets (Bytes 13 and 14 are 0x8100 or 0x88a8). Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. Values: 0x0 (NONE): No VLAN tag deletion, insertion, or replacement 0x1 (DELETE): VLAN tag deletion 0x2 (INSERT): VLAN tag insertion 0x3 (REPLACE): VLAN tag replacement
15:0	RW	0x0000	VLT VLAN Tag for Transmit Packets This field contains the value of the VLAN tag to be inserted or replaced. The value must only be changed when the transmit lines are inactive or during the initialization phase.Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: 1.Bits[15:13]: User Priority 2.Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) 3.Bits[11:0]: VLAN Identifier (VID) field of VLAN tag

GMAC_MAC_INNER_VLAN_INCL

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
20	RW	0x0	VLTI VLAN Tag Input When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from the following: 1.The mti_vlan_tag_i signal in EQOS-CORE configurations 2.The control word in EQOS-MTL configurations 3.The Tx descriptor in EQOS-AHB, EQOS-AXI, or EQOS-DMA configurations 0x0 (DISABLE): VLAN Tag Input is disabled 0x1 (ENABLE): VLAN Tag Input is enabled
19	RW	0x0	CSVL C-VLAN or S-VLAN When this bit is set, S-VLAN type (0x88A8) is inserted or replaced in the 13th and 14th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted or replaced in the 13th and 14th bytes of transmitted packets. Values: 0x0 (C-VLAN): C-VLAN type (0x8100) is inserted 0x1 (S-VLAN): S-VLAN type (0x88A8) is inserted
18	RW	0x0	VLP VLAN Priority Control When this bit is set, the VLC field is used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and the VLC field is ignored. Values: 0x0 (DISABLE): VLAN Priority Control is disabled 0x1 (ENABLE): VLAN Priority Control is enabled
17:16	RW	0x0	VLC VLAN Tag Control in Transmit Packets 2'b00: No VLAN tag deletion, insertion, or replacement 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 17 and 18) and VLAN tag (bytes 19 and 20) of all transmitted packets with VLAN tags. 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 19 and 20 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 17 and 18. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 19 and 20 of all VLAN-type transmitted packets (Bytes 17 and 18 are 0x8100 or 0x88a8). Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. Values: 0x0 (NONE): No VLAN tag deletion, insertion, or replacement 0x1 (DELETE): VLAN tag deletion 0x2 (INSERT): VLAN tag insertion 0x3 (REPLACE): VLAN tag replacement

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	VLT VLAN Tag for Transmit Packets This field contains the value of the VLAN tag to be inserted or replaced. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: 1.Bits[15:13]: User Priority 2.Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) 3.Bits[11:0]: VLAN Identifier (VID) field of VLAN tag

GMAC_MAC_Q0_TX_FLOW_CTRL

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PT Pause Time This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	RO	0x00	reserved
7	RW	0x0	DZPQ Disable Zero-Quanta Pause When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. Values: 1'b0: Zero-Quanta Pause packet generation is enabled 1'b1: Zero-Quanta Pause packet generation is disabled
6:4	RW	0x0	PLT Pause Low Threshold This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. Values: 3'b000: Pause Time minus 4 Slot Times (PT -4 slot times) 3'b001: Pause Time minus 28 Slot Times (PT -28 slot times) 3'b010: Pause Time minus 36 Slot Times (PT -36 slot times) 3'b011: Pause Time minus 144 Slot Times (PT -144 slot times)

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Bit	Attr	Reset Value	Description
			3'b100: Pause Time minus 256 Slot Times (PT -256 slot times) 3'b101: Pause Time minus 512 Slot Times (PT -512 slot times) 3'b110: Reserved
3:2	RO	0x0	reserved
1	RW	0x0	TFE Transmit Flow Control Enable Full-Duplex Mode: In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. Half-Duplex Mode: In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled. Values: 1'b0: Transmit Flow Control is disabled 1'b1: Transmit Flow Control is enabled
0	RW	0x0	FCB_BPA Flow Control Busy or Backpressure Activate This bit initiates a Pause packet in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. Full-Duplex Mode: In the full-duplex mode, this bit should be read as 1'b0 before writing to this register. To initiate a Pause packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When Pause packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Half-Duplex Mode: When this bit is set (and TFE bit is set) in the half-duplex mode, the MAC asserts the backpressure. During backpressure, when the MAC receives a new packet, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Flow Control Busy or Backpressure Activate is disabled 1'b1: Flow Control Busy or Backpressure Activate is enabled

GMAC_MAC_RX_FLOW_CTRL

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	UP Unicast Pause Packet Detect A pause packet is processed when it has the unique multicast address specified in the IEEE 802.3. When this bit is set, the MAC can also detect Pause packets with unicast address of the station. This unicast address should be as specified in MAC_Address0_High and MAC_Address0_Low. When this bit is reset, the MAC only detects Pause packets with unique multicast

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Bit	Attr	Reset Value	Description
			address. Note: The MAC does not process a Pause packet if the multicast address is different from the unique multicast address. This is also applicable to the received PFC packet when the Priority Flow Control (PFC) is enabled. The unique multicast address (0x01_80_C2_00_00_01) is as specified in IEEE 802.1 Qbb-2011. Values: 1'b0: Unicast Pause Packet Detect disabled 1'b1: Unicast Pause Packet Detect enabled
0	RW	0x0	RFE Receive Flow Control Enable When this bit is set and the MAC is operating in full-duplex mode, the MAC decodes the received Pause packet and disables its transmitter for a specified (Pause) time. When this bit is reset or the MAC is operating in half-duplex mode, the decode function of the Pause packet is disabled. When PFC is enabled, flow control is enabled for PFC packets. The MAC decodes the received PFC packet and disables the Transmit queue, with matching priorities, for a duration of received Pause time. Values: 1'b0: Receive Flow Control is disabled 1'b1: Receive Flow Control is enabled

GMAC_MAC_RXQ_CTRL4

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	VFFQ VLAN Tag Filter Fail Packets Queue This field holds the Rx queue number to which the tagged packets failing the Destination or Source Address filter (and UFFQE/MFFQE not enabled) or failing the VLAN tag filter must be routed to. This field is valid only when the VFFQE bit is set.
16	RW	0x0	VFFQE VLAN Tag Filter Fail Packets Queuing Enable When this bit is set, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter, are routed to the Rx Queue Number programmed in the VFFQ. When this bit is reset, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter are routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): VLAN tag Filter Fail Packets Queuing is disabled 0x1 (ENABLE): VLAN tag Filter Fail Packets Queuing is enabled
15:10	RO	0x00	reserved
9	RW	0x0	MFFQ Multicast Address Filter Fail Packets Queue This field holds the Rx queue number to which the Multicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the MFFQE bit is set.

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Bit	Attr	Reset Value	Description
8	RW	0x0	MFFQE Multicast Address Filter Fail Packets Queuing Enable When this bit is set, the Multicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the MFFQ. When this bit is reset, the Multicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): Multicast Address Filter Fail Packets Queuing is disabled 0x1 (ENABLE): Multicast Address Filter Fail Packets Queuing is enabled
7:2	RO	0x00	reserved
1	RW	0x0	UFFQ Unicast Address Filter Fail Packets Queue This field holds the Rx queue number to which the Unicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the UFFQE bit is set.
0	RW	0x0	UFFQE Unicast Address Filter Fail Packets Queuing Enable When this bit is set, the Unicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the UFFQ. When this bit is reset, the Unicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. Values: 0x0 (DISABLE): Unicast Address Filter Fail Packets Queuing is disabled 0x1 (ENABLE): Unicast Address Filter Fail Packets Queuing is enabled

GMAC_MAC_RXQ_CTRL0

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	RXQ1EN Receive Queue 1 Enable This field is similar to the RXQ0EN field. Values: 0x0 (DISABLE): Queue not enabled 0x1 (EN_AV): Queue enabled for AV 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic 0x3 (RSVD): Reserved
1:0	RW	0x0	RXQ0EN Receive Queue 0 Enable This field indicates whether Rx Queue 0 is enabled for AV or DCB. Values: 0x0 (DISABLE): Queue not enabled 0x1 (EN_AV): Queue enabled for AV 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic 0x3 (RSVD): Reserved Note: In multiple Rx queues configuration, all the queues are disabled by default. Enable the Rx queue by programming the corresponding field in this register.

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GMAC_MAC_RXQ_CTRL1

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	FPRQ Frame Preemption Residue Queue This field holds the Rx queue number to which the residual preemption frames must be forwarded. Preemption frames that are tagged and pass the SA/DA/VLAN filtering are routed based on PSRQ and all other frames are treated as residual frames and is routed to the queue number mentioned in this field. The Queue-0 is used as a default queue for express frames, so this field cannot be programmed to a value 0.
23:22	RW	0x0	TPQC Tagged PTP over Ethernet Packets Queuing Control This field controls the routing of the VLAN Tagged PTPoE packets. If DWC_EQOS_AV_ENABLE is selected in the configuration, the following programmable options are allowed. 2'b00: VLAN Tagged PTPoE packets are routed as generic VLAN Tagged packet (based on PSRQ for only non-AV enabled Rx Queues). 2'b01: VLAN Tagged PTPoE packets are routed to Rx Queue specified by PTPQ field (That Rx Queue can be enabled for AV or non-AV traffic). 2'b10: VLAN Tagged PTPoE packets are routed to only AV enabled Rx Queues based on PSRQ. 2'b11: Reserved If DWC_EQOS_AV_ENABLE is not selected in the configuration, the following programmable options are allowed. 1'b0: VLAN Tagged PTPoE packets are routed as generic VLAN Tagged packet (based on PSRQ for DCB/Generic enabled Rx Queues). 1'b1: VLAN Tagged PTPoE packets are routed to Rx Queues specified by PTPQ field.
21	RW	0x0	TACPQE Tagged AV Control Packets Queuing Enable When set, the MAC routes the received Tagged AV Control packets to the Rx queue specified by AVCPQ field. When reset, the MAC routes the received Tagged AV Control packets based on the tag priority matching the PSRQ fields in MAC_RxQ_Ctrl2 and MAC_RxQ_Ctrl3 registers. Values: 0x0 (DISABLE): Tagged AV Control Packets Queuing is disabled 0x1 (ENABLE): Tagged AV Control Packets Queuing is enabled
20	RW	0x0	MCBCQEN Multicast and Broadcast Queue Enable This bit specifies that Multicast or Broadcast packets routing to the Rx Queue is enabled and the Multicast or Broadcast packets must be routed to Rx Queue specified in MCBCQ field. Values: 0x0 (DISABLE): Multicast and Broadcast Queue is disabled 0x1 (ENABLE): Multicast and Broadcast Queue is enabled
19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:16	RW	0x0	MCBCQ Multicast and Broadcast Queue This field specifies the Rx Queue onto which Multicast or Broadcast Packets are routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Multicast or Broadcast Packets. Values: 0x0 (QUEUE0): Receive Queue 0 0x1 (QUEUE1): Receive Queue 1 0x2 (QUEUE2): Receive Queue 2 0x3 (QUEUE3): Receive Queue 3 0x4 (QUEUE4): Receive Queue 4 0x5 (QUEUE5): Receive Queue 5 0x6 (QUEUE6): Receive Queue 6 0x7 (QUEUE7): Receive Queue 7
15	RO	0x0	reserved
14:12	RW	0x0	UPQ Untagged Packet Queue This field indicates the Rx Queue to which Untagged Packets are to be routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Untagged Packets. Values: 0x0 (QUEUE0): Receive Queue 0 0x1 (QUEUE1): Receive Queue 1 0x2 (QUEUE2): Receive Queue 2 0x3 (QUEUE3): Receive Queue 3 0x4 (QUEUE4): Receive Queue 4 0x5 (QUEUE5): Receive Queue 5 0x6 (QUEUE6): Receive Queue 6 0x7 (QUEUE7): Receive Queue 7
11:7	RO	0x00	reserved
6:4	RW	0x0	PTPQ PTP Packets Queue This field specifies the Rx queue on which the PTP packets sent over the Ethernet payload (not over IPv4 or IPv6) are routed. When the AV8021ASMEN bit of MAC_Timestamp_Control register is set, only untagged PTP over Ethernet packets are routed on an Rx Queue. If the bit is not set, then based on programming of TPQC field, both tagged and untagged PTPoE packets can be routed to this Rx Queue. Values: 0x0 (QUEUE0): Receive Queue 0 0x1 (QUEUE1): Receive Queue 1 0x2 (QUEUE2): Receive Queue 2 0x3 (QUEUE3): Receive Queue 3 0x4 (QUEUE4): Receive Queue 4 0x5 (QUEUE5): Receive Queue 5 0x6 (QUEUE6): Receive Queue 6 0x7 (QUEUE7): Receive Queue 7
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	AVCPQ AV Untagged Control Packets Queue This field specifies the Receive queue on which the received AV tagged and untagged control packets are routed. The AV tagged (when TACPQE bit is set) and untagged control packets are routed to Receive queue specified by this field. Values: 0x0 (QUEUE0): Receive Queue 0 0x1 (QUEUE1): Receive Queue 1 0x2 (QUEUE2): Receive Queue 2 0x3 (QUEUE3): Receive Queue 3 0x4 (QUEUE4): Receive Queue 4 0x5 (QUEUE5): Receive Queue 5 0x6 (QUEUE6): Receive Queue 6 0x7 (QUEUE7): Receive Queue 7

GMAC_MAC_RXQ_CTRL2

Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	PSRQ1 Priorities Selected in the Receive Queue 1 This field decides the priorities assigned to Rx Queue 1. All packets with priorities that match the values set in this field are routed to Rx Queue 1. For example, if PSRQ1[4] is set, packets with USP field equal to 4 are routed to Rx Queue 1. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. When the DCB feature is selected, this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 1 crosses the flow control threshold settings.
7:0	RW	0x00	PSRQ0 Priorities Selected in the Receive Queue 0 This field decides the priorities assigned to Rx Queue 0. All packets with priorities that match the values set in this field are routed to Rx Queue 0. For example, if PSRQ0[5] is set, packets with USP field equal to 5 are routed to Rx Queue 0. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. When the DCB feature is selected, this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 0 crosses the flow control threshold settings.

GMAC_MAC_INTERRUPT_STATUS

Address: **Operational Base** + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
20	RO	0x0	MFRIS MMC FPE Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC FPE Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support. Values: 0x0 (INACTIVE): MMC FPE Receive Interrupt status not active 0x1 (ACTIVE): MMC FPE Receive Interrupt status active
19	RO	0x0	MFTIS MMC FPE Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC FPE Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support. Values: 0x0 (INACTIVE): MMC FPE Transmit Interrupt status not active 0x1 (ACTIVE): MMC FPE Transmit Interrupt status active
18	RO	0x0	MDIOIS MDIO Interrupt Status This bit indicates an interrupt event after the completion of MDIO operation. To reset this bit, the application has to read this bit/Write 1 to this bit when RCWE bit of MAC_CSR_SW_Ctrl register is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: MDIO Interrupt status not active 1'b1: MDIO Interrupt status active
17	RO	0x0	FPEIS Frame Preemption Interrupt Status This bit indicates an interrupt event during the operation of Frame Preemption (Bits[19:16] of MAC_FPE_CTRL_STS register is set). To reset this bit, the application must clear the event in MAC_FPE_CTRL_STS that has caused the Interrupt. Values: 0x0 (INACTIVE): Frame Preemption Interrupt status not active 0x1 (ACTIVE): Frame Preemption Interrupt status active
16:15	RO	0x0	reserved
14	RO	0x0	RXSTSIS Receive Status Interrupt This bit indicates the status of received packets. This bit is set when the RWT bit is set in the MAC_Rx_Tx_Status register. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. Values: 1'b0: Receive Interrupt status not active 1'b1: Receive Interrupt status active

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Bit	Attr	Reset Value	Description
13	RO	0x0	TXSTSIS Transmit Status Interrupt This bit indicates the status of transmitted packets. This bit is set when any of the following bits is set in the MAC_Rx_Tx_Status register: 1. Excessive Collision (EXCOL) 2. Late Collision (LCOL) 3. Excessive Deferral (EXDEF) 4. Loss of Carrier (LCARR) 5. No Carrier (NCARR) 6. Jabber Timeout (TJT) This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. Values: 1'b0: Transmit Interrupt status not active 1'b1: Transmit Interrupt status active
12	RO	0x0	TSIS Timestamp Interrupt Status If the Timestamp feature is enabled, this bit is set when any of the following conditions is true: 1. The system time value is equal to or exceeds the value specified in the Target Time High and Low registers. 2. There is an overflow in the Seconds register. 3. The Target Time Error occurred, that is, programmed target time already elapsed. If the Auxiliary Snapshot feature is enabled, this bit is set when the auxiliary snapshot trigger is asserted. In configurations other than EQOS_CORE, when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Timestamp_Status register. Values: 1'b0: Timestamp Interrupt status not active 1'b1: Timestamp Interrupt status active
11	RO	0x0	MMCRXIPIS MMC Receive Checksum Offload Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) and Enable Receive TCP/IP Checksum Check options. Values: 1'b0: MMC Receive Checksum Offload Interrupt status not active 1'b1: MMC Receive Checksum Offload Interrupt status active

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Bit	Attr	Reset Value	Description
10	RO	0x0	MMCTXIS MMC Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. Values: 1'b0: MMC Transmit Interrupt status not active 1'b1: MMC Transmit Interrupt status active
9	RO	0x0	MMCRXIS MMC Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. Values: 1'b0: MMC Receive Interrupt status not active 1'b1: MMC Receive Interrupt status active
8	RO	0x0	MMCIS MMC Interrupt Status This bit is set high when Bit 11, Bit 10, or Bit 9 is set high. This bit is cleared only when all these bits are low. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. Values: 1'b0: MMC Interrupt status not active 1'b1: MMC Interrupt status active
7:6	RO	0x0	reserved
5	RO	0x0	LPIIS LPI Interrupt Status When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared when the corresponding interrupt source bit of MAC_LPI_Control_Status register is read (or corresponding interrupt source bit of MAC_LPI_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). Values: 1'b0: LPI Interrupt status not active 1'b1: LPI Interrupt status active
4	RO	0x0	PMTIS PMT Interrupt Status This bit is set when a Magic packet or Wake-on-LAN packet is received in the power-down mode (RWKPRCVD and MGKPRCVD bits in MAC_PMT_Control_Status register). This bit is cleared when corresponding interrupt source bit are cleared because of a Read operation to the MAC_PMT_Control_Status register (or corresponding interrupt source bit of MAC_PMT_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the Enable Power Management option. Values: 1'b0: PMT Interrupt status not active 1'b1: PMT Interrupt status active

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Bit	Attr	Reset Value	Description
3	RO	0x0	PHYIS PHY Interrupt This bit is set when rising edge is detected on the phy_intr_i input. This bit is cleared when this register is read (or this bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). Values: 1'b0: PHY Interrupt not detected 1'b1: PHY Interrupt detected
2:1	RO	0x0	reserved
0	RO	0x0	RGSMIIIS RGMII or SMII Interrupt Status This bit is set because of any change in value of the Link Status of RGMII or SMII interface (LNKSTS bit in MAC_PHYIF_Control_Status register). This bit is cleared when the MAC_PHYIF_Control_Status register is read (or LNKSTS bit of MAC_PHYIF_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the optional RGMII or SMII PHY interface. Values: 1'b0: RGMII or SMII Interrupt Status is not active 1'b1: RGMII or SMII Interrupt Status is active

GMAC_MAC_INTERRUPT_ENABLE

Address: **Operational Base** + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	MDIOIE MDIO Interrupt Enable When this bit is set, it enables the assertion of the interrupt when MDIOIS field is set in the MAC_Interrupt_Status register. Values: 1'b0: MDIO Interrupt is disabled 1'b1: MDIO Interrupt is enabled
17	RW	0x0	FPEIE Frame Preemption Interrupt Enable When this bit is set, it enables the assertion of the interrupt when FPEIS field is set in the MAC_Interrupt_Status register. Values: 0x0 (DISABLE): Frame Preemption Interrupt is disabled 0x1 (ENABLE): Frame Preemption Interrupt is enabled
16:15	RO	0x0	reserved
14	RW	0x0	RXSTSIE Receive Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of RXSTSIS bit in the MAC_Interrupt_Status register. Values: 1'b0: Receive Status Interrupt is disabled 1'b1: Receive Status Interrupt is enabled

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Bit	Attr	Reset Value	Description
13	RW	0x0	TXSTSIE Transmit Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of TXSTSIS bit in the MAC_Interrupt_Status register. Values: 1'b0: Timestamp Status Interrupt is disabled 1'b1: Timestamp Status Interrupt is enabled
12	RW	0x0	TSIE Timestamp Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of TSIS bit in MAC_Interrupt_Status register. Values: 1'b0: Timestamp Interrupt is disabled 1'b1: Timestamp Interrupt is enabled
11:6	RO	0x00	reserved
5	RW	0x0	LPIIE LPI Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of LPIIS bit in MAC_Interrupt_Status register. Values: 1'b0: LPI Interrupt is disabled 1'b1: LPI Interrupt is enabled
4	RW	0x0	PMTIE PMT Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of PMTIS bit in MAC_Interrupt_Status register. Values: 1'b0: PMT Interrupt is disabled 1'b1: PMT Interrupt is enabled
3	RW	0x0	PHYIE PHY Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of PHYIS bit in MAC_Interrupt_Status register. Values: 1'b0: PHY Interrupt is disabled 1'b1: PHY Interrupt is enabled
2:1	RO	0x0	reserved
0	RW	0x0	RGSMIIIE RGMII or SMII Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of RGSMIIIS bit in MAC_Interrupt_Status register. Values: 1'b0: RGMII or SMII Interrupt is disabled 1'b1: RGMII or SMII Interrupt is enabled

GMAC_MAC_RX_TX_STATUS

Address: **Operational Base** + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
8	RO	0x0	RWT Receive Watchdog Timeout This bit is set when a packet with length greater than 2,048 bytes is received (10, 240 bytes when Jumbo Packet mode is enabled) and the WD bit is reset in the MAC_Configuration register. This bit is set when a packet with length greater than 16,383 bytes is received and the WD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No receive watchdog timeout 1'b1: Receive watchdog timed out
7:6	RO	0x0	reserved
5	RO	0x0	EXCOL Excessive Collisions When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the transmission aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after the first collision and the packet transmission is aborted. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No collision 1'b1: Excessive collision is sensed
4	RO	0x0	LCOL Late Collision When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the packet transmission aborted because a collision occurred after the collision window (64 bytes including Preamble in MII mode; 512 bytes including Preamble and Carrier Extension in GMII mode). This bit is not valid if the Underflow error occurs. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No collision 1'b1: Late collision is sensed
3	RO	0x0	EXDEF Excessive Deferral When the DTXSTS bit is set in the MTL_Operation_Mode register and the DC bit is set in the MAC_Configuration register, this bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 in 1000/2500 Mbps mode or when Jumbo packet is enabled). Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No Excessive deferral 1'b1: Excessive deferral

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Bit	Attr	Reset Value	Description
2	RO	0x0	LCARR Loss of Carrier When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the loss of carrier occurred during packet transmission, that is, the phy_crs_i signal was inactive for one or more transmission clock periods during packet transmission. This bit is valid only for packets transmitted without collision. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Carrier is present 1'b1: Loss of carrier
1	RO	0x0	NCARR No Carrier When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the carrier signal from the PHY is not present at the end of preamble transmission. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Carrier is present 1'b1: No carrier
0	RO	0x0	TJT Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired which happens when the packet size exceeds 2,048 bytes (10,240 bytes when the Jumbo packet is enabled) and JD bit is reset in the MAC_Configuration register. This bit is set when the packet size exceeds 16,383 bytes and the JD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No Transmit Jabber Timeout 1'b1: Transmit Jabber Timeout occurr

GMAC_MAC_PMT_CONTROL_STATUS

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31	RW	0x0	RWKFILTRST Remote Wake-Up Packet Filter Register Pointer Reset When this bit is set, the remote wake-up packet filter register pointer is reset to 3'b000. It is automatically cleared after 1 clock cycle. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Remote Wake-Up Packet Filter Register Pointer is not Reset 1'b1: Remote Wake-Up Packet Filter Register Pointer is Reset
30:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:24	RO	0x00	RWKPTR Remote Wake-up FIFO Pointer This field gives the current value (0 to 7, 15, or 31 when 4, 8, or 16 Remote Wake-up Packet Filters are selected) of the Remote Wake-up Packet Filter register pointer. When the value of this pointer is equal to maximum for the selected number of Remote Wake-up Packet Filters, the contents of the Remote Wake-up Packet Filter Register are transferred to the clk_rx_i domain when a Write occurs to that register.
23:11	RO	0x0000	reserved
10	RW	0x0	RWKPFE Remote Wake-up Packet Forwarding Enable When this bit is set along with RWKPKTEN, the MAC receiver drops all received frames until it receives the expected Wake-up frame. All frames after that event including the received wake-up frame are forwarded to application. This bit is then self-cleared on receiving the wake-up packet. The application can also clear this bit before the expected wake-up frame is received. In such cases, the MAC reverts to the default behavior where packets received are forwarded to the application. This bit must only be set when RWKPKTEN is set high and PWRDWN is set low. The setting of this bit has no effect when PWRDWN is set high. Note: If Magic Packet Enable and Wake-Up Frame Enable are both set along with setting of this bit and Magic Packet is received prior to wake-up frame, this bit is self-cleared on receiving Magic Packet, the received Magic packet is dropped, and all frames after received Magic Packet are forwarded to application. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Remote Wake-up Packet Forwarding is disabled 1'b1: Remote Wake-up Packet Forwarding is enabled
9	RW	0x0	GLBLUCAST Global Unicast When this bit set, any unicast packet filtered by the MAC (DAF) address recognition is detected as a remote wake-up packet. Values: 1'b0: Global unicast is disabled 1'b1: Global unicast is enabled
8:7	RO	0x0	reserved
6	RO	0x0	RWKPRCVD Remote Wake-Up Packet Received When this bit is set, it indicates that the power management event is generated because of the reception of a remote wake-up packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Remote wake-up packet is received 1'b1: Remote wake-up packet is received

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Bit	Attr	Reset Value	Description
5	RO	0x0	MGKPRCVD Magic Packet Received When this bit is set, it indicates that the power management event is generated because of the reception of a magic packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No Magic packet is received 1'b1: Magic packet is received
4:3	RO	0x0	reserved
2	RW	0x0	RWKPKTEN Remote Wake-Up Packet Enable When this bit is set, a power management event is generated when the MAC receives a remote wake-up packet. Values: 1'b0: Remote wake-up packet is disabled 1'b1: Remote wake-up packet is enabled
1	RW	0x0	MGKPKTEN Magic Packet Enable When this bit is set, a power management event is generated when the MAC receives a magic packet. Values: 1'b0: Magic Packet is disabled 1'b1: Magic Packet is enabled
0	RW	0x0	PWRDWN Power Down When this bit is set, the MAC receiver drops all received packets until it receives the expected magic packet or remote wake-up packet. This bit is then self-cleared and the power-down mode is disabled. The software can clear this bit before the expected magic packet or remote wake-up packet is received. The packets received by the MAC after this bit is cleared are forwarded to the application. This bit must only be set when the Magic Packet Enable, Global Unicast, or Remote Wake-Up Packet Enable bit is set high. Note: You can gate-off the CSR clock during the power-down mode. However, when the CSR clock is gated-off, you cannot perform any read or write operations on this register. Therefore, the Software cannot clear this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Power down is disabled 1'b1: Power down is enabled

GMAC_MAC_RWK_PACKET_FILTER

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	WKUPFRMFTR RWK Packet Filter This field contains the various controls of RWK Packet filter. When the Remote Wakeup Filters are to be programmed, the entire set of wkuppktfilter_reg registers must be written. The wkuppktfilter_reg register is programmed by sequentially writing the eight, sixteen or thirty-two register values in

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Bit	Attr	Reset Value	Description
			MAC_RWK_Packet_Filter register for wkuppktfilter_reg0, wkuppktfilter_reg1, ..., wkuppktfilter_reg31 respectively. The wkuppktfilter_reg register is read in a similar way. The MAC updates the wkuppktfilter_reg register current pointer value in RWKPTR field of MAC_PMT_Control_Status register. The Remote Wakeup Filters are arranged in blocks of 4 filters each and each such block have eight 32-bit wide registers, viz. wkuppktfilter_reg0-7, wkuppktfilter_reg8-15, wkuppktfilter_reg16-23 and wkuppktfilter_reg24-31. The fields of Remote Wakeup Filter are described as follows: Filter i Command: The 4-bit filter i command controls the filter i operation. 1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet. 2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC-16 value. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2". 3. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. The details are provided below: (1) The And_Previous bit setting is applicable within a set of 4 filters. (2) Setting of And_Previous bit of filter that is not enabled has no effect, that is setting And_Previous bit of lowest number filter in the set of 4 filters has no effect. For example, setting of And_Previous bit of Filter 0 has no effect. (3) If And_Previous bit is set for filter to form AND chained filter, the AND chain breaks at the point any filter is not enabled. For example: If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set) but Filter 1 is not enabled (bit 0 in Filter 1 command is reset), then only Filter 2 result is considered. If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 3 And_Previous bit is set (bit 1 in Filter 3 command is set), but Filter 1 is not enabled (bit 0 in Filter 1 command is reset), then only Filter 2 result ANDed with Filter 3 result is considered. If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 3 And_Previous bit is set (bit 1 in Filter 3 command is set), but Filter 2 is not enabled (bit 0 in Filter 2 command is reset), then since setting of Filter 2 And_Previous bit has no effect only Filter 1 result ORed with Filter 3 result is considered.

GMAC_RWK_FILTER0_BYTE_MASK

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filter0_Byte_Mask Filter0 32-bit Mask Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1', the corresponding byte is taken into the CRC16 calculation.

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GMAC_RWK_FILTER1_BYTE_MASK

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filter1_Byte_Mask Filter1 32-bit Mask Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1', the corresponding byte is taken into the CRC16 calculation.

GMAC_RWK_FILTER2_BYTE_MASK

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filter2_Byte_Mask Filter2 32-bit Mask Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1', the corresponding byte is taken into the CRC16 calculation.

GMAC_RWK_FILTER3_BYTE_MASK

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filter3_Byte_Mask Filter3 32-bit Mask Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1', the corresponding byte is taken into the CRC16 calculation.

GMAC_RWK_FILTER01_CRC

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Filter1_CRC Filter1 CRC-16 This filter CRC-16 contains the CRC_16 value of the pattern. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15 + x^2 + 1
15:0	RW	0x0000	Filter0_CRC Filter0 CRC-16 This filter CRC-16 contains the CRC_16 value of the pattern. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15 + x^2 + 1

GMAC_RWK_FILTER23_CRC

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Filter3_CRC Filter3 CRC-16 This filter CRC-16 contains the CRC_16 value of the pattern. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15 + x^2 + 1
15:0	RW	0x0000	Filter2_CRC Filter2 CRC-16 This filter CRC-16 contains the CRC_16 value of the pattern. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15+ x^2 + 1

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GMAC_RWK_FILTER_OFFSET

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Filter3_Offset Filter3 Offset This filter offset defines the offset (within the packet) from which the filter examines the packets. 1. This 8-bit pattern-offset is the offset for the filter first byte to be examined. 2. The minimum allowed offset is 12, which refers to the 13th byte of the packet. 3. The offset value 0 refers to the first byte of the packet.
23:16	RW	0x00	Filter2_Offset Filter2 Offset This filter offset defines the offset (within the packet) from which the filter examines the packets. 1. This 8-bit pattern-offset is the offset for the filter first byte to be examined. 2. The minimum allowed offset is 12, which refers to the 13th byte of the packet. 3. The offset value 0 refers to the first byte of the packet.
15:8	RW	0x00	Filter1_Offset Filter1 Offset This filter offset defines the offset (within the packet) from which the filter examines the packets. 1. This 8-bit pattern-offset is the offset for the filter first byte to be examined. 2. The minimum allowed offset is 12, which refers to the 13th byte of the packet. 3. The offset value 0 refers to the first byte of the packet.
7:0	RW	0x00	Filter0_Offset Filter0 Offset This filter offset defines the offset (within the packet) from which the filter examines the packets. 1. This 8-bit pattern-offset is the offset for the filter first byte to be examined. 2. The minimum allowed offset is 12, which refers to the 13th byte of the packet. 3. The offset value 0 refers to the first byte of the packet.

GMAC_RWK_FILTER_COMMAND

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	Filter3_Command Filter3 Command The 4-bit filter command controls the filter operation. 1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet. 2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC_16 value. 3. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2".

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Bit	Attr	Reset Value	Description
			4. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. 5. Bit 0 is the enable for filter. If Bit 0 is not set, filter is disabled.
23:20	RO	0x0	reserved
19:16	RW	0x0	Filter2_Command Filter2 Command The 4-bit filter command controls the filter operation. 1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet. 2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC_16 value. 3. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2". 4. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. 5. Bit 0 is the enable for filter. If Bit 0 is not set, filter is disabled.
15:12	RO	0x0	reserved
11:8	RW	0x0	Filter1_Command Filter1 Command The 4-bit filter command controls the filter operation. 1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet. 2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC_16 value. 3. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2". 4. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. 5. Bit 0 is the enable for filter. If Bit 0 is not set, filter is disabled.
7:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	Filter0_Command Filter0 Command The 4-bit filter command controls the filter operation. 1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet. 2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC_16 value. 3. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2". 4. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. 5. Bit 0 is the enable for filter. If Bit 0 is not set, filter is disabled.

GMAC_MAC_LPI_CONTROL_STATUS

Address: **Operational Base** + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	LPITCSE LPI Tx Clock Stop Enable When this bit is set, the MAC asserts sbd_tx_clk_gating_ctrl_o signal high after it enters Tx LPI mode to indicate that the Tx clock to MAC can be stopped. When this bit is reset, the MAC does not assert sbd_tx_clk_gating_ctrl_o signal high after it enters Tx LPI mode. If RGMII Interface is selected, the Tx clock is required for transmitting the LPI pattern. The Tx Clock cannot be gated and so the LPITCSE bit cannot be programmed. Values: 1'b0: LPI Tx Clock Stop is disabled 1'b1: LPI Tx Clock Stop is enabled
20	RW	0x0	LPIATE LPI Timer Enable This bit controls the automatic entry of the MAC Transmitter into and exit out of the LPI state. When LPIATE, LPITXA and LPIEN bits are set, the MAC Transmitter enters LPI state only when the complete MAC TX data path is IDLE for a period indicated by the MAC_LPI_Entry_Timer register. After entering LPI state, if the data path becomes non-IDLE (due to a new packet being accepted for transmission), the Transmitter exits LPI state but does not clear LPIEN bit. This enables the re-entry into LPI state when it is IDLE again. When LPIATE is 0, the LPI Auto timer is disabled and MAC Transmitter enters LPI state based on the settings of LPITXA and LPIEN bit descriptions. Values: 1'b0: LPI Timer is disabled 1'b1: LPI Timer is enabled

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Bit	Attr	Reset Value	Description
19	RW	0x0	LPITXA LPI Tx Automate This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the Transmit side. This bit is not functional in the EQOS-CORE configurations in which the Tx clock gating is done during the LPI mode. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding packets (in the core) and pending packets (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any packet for transmission or the application issues a Tx FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If Tx FIFO Flush is set in the FTQ bit of MTL_TxQ0_Operation_Mode register, when the MAC is in the LPI mode, it exits the LPI mode. When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode. Values: 1'b0: LPI Tx Automate is disabled 1'b1: LPI Tx Automate is enabled
18	RW	0x0	PLSEN PHY Link Status Enable This bit enables the link status received on the RGMII, SGMII, or SMII Receive paths to be used for activating the LPI LS TIMER. When this bit is set, the MAC uses the link-status bits of the MAC_PHYIF_Control_Status register and the PLS bit for the LPI LS Timer trigger. When this bit is reset, the MAC ignores the link-status bits of the MAC_PHYIF_Control_Status register and takes only the PLS bit. Values: 1'b0: PHY Link Status is disabled 1'b1: PHY Link Status is enabled
17	RW	0x0	PLS PHY Link Status This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (OKAY) at least for the time indicated by the LPI LS TIMER. When this bit is set, the link is considered to be okay (UP) and when this bit is reset, the link is considered to be down. Values: 1'b0: link is down 1'b1: link is okay (UP)
16	RW	0x0	LPIEN LPI Enable When this bit is set, it instructs the MAC Transmitter to enter the LPI state. When this bit is reset, it instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission. Values: 1'b0: LPI state is disabled 1'b1: LPI state is enabled
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9	RO	0x0	RLPIST Receive LPI State When this bit is set, it indicates that the MAC is receiving the LPI pattern on the GMII or MII interface. Values: 1'b0: Receive LPI state not detected 1'b1: Receive LPI state detected
8	RO	0x0	TLPIST Transmit LPI State When this bit is set, it indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface. Values: 1'b0: Transmit LPI state not detected 1'b1: Transmit LPI state detected
7:4	RO	0x0	reserved
3	RW	0x0	RLPIEX Receive LPI Exit When this bit is set, it indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit may not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. Values: 1'b0: Receive LPI exit not detected 1'b1: Receive LPI exit detected
2	RO	0x0	RLPIEN Receive LPI Entry When this bit is set, it indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit may not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. Values: 1'b0: Receive LPI entry not detected 1'b1: Receive LPI entry detected
1	RO	0x0	TLPIEX Transmit LPI Exit When this bit is set, it indicates that the MAC transmitter exited the LPI state after the application cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Values: 1'b0: Transmit LPI exit not detected 1'b1: Transmit LPI exit detected

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Bit	Attr	Reset Value	Description
0	RO	0x0	TLPIEN Transmit LPI Entry When this bit is set, it indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Values: 1'b0: Transmit LPI entry not detected 1'b1: Transmit LPI entry detected

GMAC_MAC_LPI_TIMERS_CONTROL

Address: **Operational Base** + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3e8	LST LPI LS Timer This field specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard.
15:0	RW	0x0000	TWT LPI TW Timer This field specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer.

GMAC_MAC_LPI_ENTRY_TIMER

Address: **Operational Base** + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:3	RW	0x00000	LPIET LPI Entry Timer This field specifies the time in microseconds the MAC waits to enter LPI mode, after it has transmitted all the frames. This field is valid and used only when LPITE and LPITXA are set to 1. Bits [2:0] are read-only so that the granularity of this timer is in steps of 8 micro-seconds.
2:0	RO	0x0	reserved

GMAC_MAC_1US_TIC_COUNTER

Address: **Operational Base** + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x03f	TIC_1US_CNTR 1US TIC Counter The application must program this counter so that the number of clock cycles of CSR clock is 1us. (Subtract 1 from the value before programming). For example if the CSR clock is 100MHz then this field needs to be programmed to value 100 - 1 = 99 (which is 0x63). This is required to generate the 1US events that are used to update some of the EEE related counters.

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GMAC_MAC_PHYIF_CONTROL_STATUS

Address: **Operational Base** + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RO	0x0	LNKSTS Link Status This bit indicates whether the link is up (1'b1) or down (1'b0). Values: 1'b0: Link down 1'b1: Link up
18:17	RO	0x0	LNKSPEED Link Speed This bit indicates the current speed of the link. Bit 2 is reserved when the MAC is configured for the SMII PHY interface. Values: 2'b00: 2.5 MHz 2'b01: 25 MHz 2'b10: 125 MHz 2'b11: Reserved
16	RO	0x0	LNKMOD Link Mode This bit indicates the current mode of operation of the link. Values: 1'b0: Half-duplex mode 1'b1: Full-duplex mode
15:2	RO	0x0000	reserved
1	RW	0x0	LUD Link Up or Down This bit indicates whether the link is up or down during transmission of configuration in the RGMII, SGMII, or SMII interface. Values: 1'b0: Link down 1'b1: Link up
0	RW	0x0	TC Transmit Configuration in RGMII, SGMII, or SMII When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMII, SMII, or SGMII port. When this bit is reset, no such information is driven to the PHY. The details of this feature are provided in the following sections: 1. "Reduced Gigabit Media Independent Interface" 2. "Serial Media Independent Interface" 3. "Serial Gigabit Media Independent Interface" Values: 1'b0: Disable Transmit Configuration in RGMII, SGMII, or SMII 1'b1: Enable Transmit Configuration in RGMII, SGMII, or SMII

GMAC_MAC_VERSION

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x30	USERVER User-defined Version
7:0	RW	0x51	RKVER Rockchip-defined Version

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GMAC_MAC_DEBUG

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:17	RO	0x0	TFCSTS MAC Transmit Packet Controller Status This field indicates the state of the MAC Transmit Packet Controller module. Values: 2'b00: Idle state 2'b01: Waiting for one of the following: Status of the previous packet OR IPG or back off period to be over 2'b10: Generating and transmitting a Pause control packet (in full-duplex mode) 2'b11: Transferring input packet for transmission
16	RO	0x0	TPESTS MAC GMII or MII Transmit Protocol Engine Status When this bit is set, it indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data, and it is not in the Idle state. Values: 1'b0: MAC GMII or MII Transmit Protocol Engine Status not detected 1'b1: MAC GMII or MII Transmit Protocol Engine Status detected
15:3	RO	0x0000	reserved
2:1	RO	0x0	RFCFCSTS MAC Receive Packet Controller FIFO Status When this bit is set, this field indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Packet Controller module.
0	RO	0x0	RPESTS MAC GMII or MII Receive Protocol Engine Status When this bit is set, it indicates that the MAC GMII or MII receive protocol engine is actively receiving data, and it is not in the Idle state. Values: 1'b0: MAC GMII or MII Receive Protocol Engine Status not detected 1'b1: MAC GMII or MII Receive Protocol Engine Status detected

GMAC_MAC_HW_FEATURE0

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:28	RO	0x1	ACTPHYSEL Active PHY Selected When you have multiple PHY interfaces in your configuration, this field indicates the sampled value of phy_intf_sel_i during reset de-assertion. Values: 4'b0000: GMII or MII 4'b0001: RGMII 4'b0010: SGMII 4'b0011: TBI 4'b0100: RMII 4'b0101: RTBI 4'b0110: SMII

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Bit	Attr	Reset Value	Description
			4'b0111: RevMII
27	RO	0x1	SAVLANINS Source Address or VLAN Insertion Enable This bit is set to 1 when the Enable SA and VLAN Insertion on Tx option is selected. Values: 1'b0: Source Address or VLAN Insertion Enable option is not selected 1'b1: Source Address or VLAN Insertion Enable option is selected
26:25	RO	0x0	TSSTSSEL Timestamp System Time Source This bit indicates the source of the Timestamp system time: This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected. Values: 2'b00: Internal 2'b01: External 2'b10: Both 2'b11: Reserved
24	RO	0x0	MACADR64SEL MAC Addresses 64-127 Selected This bit is set to 1 when the Enable Additional 64 MAC Address Registers (64-127) option is selected. Values: 1'b0: MAC Addresses 64-127 Select option is not selected 1'b1: MAC Addresses 64-127 Select option is selected
23	RO	0x0	MACADR32SEL MAC Addresses 32-63 Selected This bit is set to 1 when the Enable Additional 32 MAC Address Registers (32-63) option is selected. Values: 1'b0: MAC Addresses 32-63 Select option is not selected 1'b1: MAC Addresses 32-63 Select option is selected
22:18	RO	0x04	ADDMACADRSEL MAC Addresses 1-31 Selected This bit is set to 1 when the non-zero value is selected for Enable Additional 1-31 MAC Address Registers option.
17	RO	0x0	reserved
16	RO	0x1	RXCOESEL Receive Checksum Offload Enabled This bit is set to 1 when the Enable Receive TCP/IP Checksum Check option is selected. Values: 1'b0: Receive Checksum Offload Enable option is not selected 1'b1: Receive Checksum Offload Enable option is selected
15	RO	0x0	reserved
14	RO	0x1	TXCOESEL Transmit Checksum Offload Enabled This bit is set to 1 when the Enable Transmit TCP/IP Checksum Insertion option is selected. Values: 1'b0: Transmit Checksum Offload Enable option is not selected 1'b1: Transmit Checksum Offload Enable option is selected

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Bit	Attr	Reset Value	Description
13	RO	0x1	EEESEL Energy Efficient Ethernet Enabled This bit is set to 1 when the Enable Energy Efficient Ethernet (EEE) option is selected. Values: 1'b0: Energy Efficient Ethernet Enable option is not selected 1'b1: Energy Efficient Ethernet Enable option is selected
12	RO	0x1	TSSEL IEEE 1588-2008 Timestamp Enabled This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected. Values: 1'b0: IEEE 1588-2008 Timestamp Enable option is not selected. 1'b1: IEEE 1588-2008 Timestamp Enable option is selected.
11:10	RO	0x0	reserved
9	RO	0x1	ARPOFFSEL ARP Offload Enabled This bit is set to 1 when the Enable IPv4 ARP Offload option is selected. Values: 1'b0: ARP Offload Enable option is not selected 1'b1: ARP Offload Enable option is selected
8	RO	0x1	MMCSEL RMON Module Enable This bit is set to 1 when the Enable MAC Management Counters (MMC) option is selected. Values: 1'b0: RMON Module Enable option is not selected 1'b1: RMON Module Enable option is selected
7	RO	0x1	MGKSEL PMT Magic Packet Enable This bit is set to 1 when the Enable Magic Packet Detection option is selected. Values: 1'b0: PMT Magic Packet Enable option is not selected 1'b1: PMT Magic Packet Enable option is selected
6	RO	0x1	RWKSEL PMT Remote Wake-up Packet Enable This bit is set to 1 when the Enable Remote Wake-Up Packet Detection option is selected. Values: 1'b0: PMT Remote Wake-up Packet Enable option is not selected 1'b1: PMT Remote Wake-up Packet Enable option is selected
5	RO	0x1	SMASEL SMA (MDIO) Interface This bit is set to 1 when the Enable Station Management (MDIO Interface) option is selected. Values: 1'b0: SMA (MDIO) Interface not selected 1'b1: SMA (MDIO) Interface selected

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Bit	Attr	Reset Value	Description
4	RO	0x1	VLHASH VLAN Hash Filter Selected This bit is set to 1 when the Enable VLAN Hash Table Based Filtering option is selected. Values: 1'b0: VLAN Hash Filter not selected 1'b1: VLAN Hash Filter selected
3	RO	0x0	PCSSEL PCS Registers (TBI, SGMII, or RTBI PHY interface) This bit is set to 1 when the TBI, SGMII, or RTBI PHY interface option is selected. Values: 1'b0: No PCS Registers (TBI, SGMII, or RTBI PHY interface) 1'b1: PCS Registers (TBI, SGMII, or RTBI PHY interface)
2	RO	0x0	HDSEL Half-duplex Support This bit is set to 1 when the half-duplex mode is selected. Values: 1'b0: No Half-duplex support 1'b1: Half-duplex support
1	RO	0x1	GMIISEL 1000 Mbps Support This bit is set to 1 when 1000 Mbps is selected as the Mode of Operation. Values: 1'b0: No 1000 Mbps support 1'b1: 1000 Mbps support
0	RO	0x1	MIISEL 10 or 100 Mbps Support This bit is set to 1 when 10/100 Mbps is selected as the Mode of Operation. Values: 1'b0: No 10 or 100 Mbps support 1'b1: 10 or 100 Mbps support

GMAC_MAC_HW_FEATURE1

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RO	0x2	L3L4FNUM Total number of L3 or L4 Filters This field indicates the total number of L3 or L4 filters: Values: 4'b0000: No L3 or L4 Filter 4'b0001: 1 L3 or L4 Filter 4'b0010: 2 L3 or L4 Filters 4'b0011: 3 L3 or L4 Filters 4'b0100: 4 L3 or L4 Filters 4'b0101: 5 L3 or L4 Filters 4'b0110: 6 L3 or L4 Filters 4'b0111: 7 L3 or L4 Filters 4'b1000: 8 L3 or L4 Filters
26	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
25:24	RO	0x1	HASHTBLSZ Hash Table Size This field indicates the size of the hash table: Values: 2'b00: No hash table 2'b01: 64 2'b10: 128 2'b11: 256
23	RO	0x0	POUOST One Step for PTP over UDP/IP Feature Enable This bit is set to 1 when the Enable One step timestamp for PTP over UDP/IP feature is selected. Values: 1'b0: One Step for PTP over UDP/IP Feature is not selected 1'b1: One Step for PTP over UDP/IP Feature is selected
22	RO	0x0	reserved
21	RO	0x0	RAVSEL Rx Side Only AV Feature Enable This bit is set to 1 when the Enable Audio Video Bridging option on Rx Side Only is selected. Values: 1'b0: Rx Side Only AV Feature is not selected 1'b1: Rx Side Only AV Feature is selected
20	RO	0x1	AVSEL AV Feature Enable This bit is set to 1 when the Enable Audio Video Bridging option is selected. Values: 1'b0: AV Feature is not selected 1'b1: AV Feature is selected
19	RO	0x1	DBGMEMA DMA Debug Registers Enable This bit is set to 1 when the Debug Mode Enable option is selected. Values: 1'b0: DMA Debug Registers option is not selected 1'b1: DMA Debug Registers option is selected
18	RO	0x1	TSOEN TCP Segmentation Offload Enable This bit is set to 1 when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected. Values: 1'b0: TCP Segmentation Offload Feature is not selected 1'b1: TCP Segmentation Offload Feature is selected
17	RO	0x1	SPHEN Split Header Feature Enable This bit is set to 1 when the Enable Split Header Structure option is selected. Values: 1'b0: Split Header Feature is not selected 1'b1: Split Header Feature is selected

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Bit	Attr	Reset Value	Description
16	RO	0x0	DCBEN DCB Feature Enable This bit is set to 1 when the Enable Data Center Bridging option is selected. Values: 1'b0: DCB Feature is not selected 1'b1: DCB Feature is selected
15:14	RO	0x1	ADDR64 Address Width This field indicates the configured address width: Values: 2'b00: 32 2'b01: 40 2'b10: 48 2'b11: Reserved
13	RO	0x0	ADVTHWORD IEEE 1588 High Word Register Enable This bit is set to 1 when the Add IEEE 1588 Higher Word Register option is selected. Values: 1'b0: IEEE 1588 High Word Register option is not selected 1'b1: IEEE 1588 High Word Register option is selected
12	RO	0x0	PTOEN PTP Offload Enable This bit is set to 1 when the Enable PTP Timestamp Offload Feature is selected. Values: 1'b0: PTP Offload feature is not selected 1'b1: PTP Offload feature is selected
11	RO	0x0	OSTEN One-Step Timestamping Enable This bit is set to 1 when the Enable One-Step Timestamp Feature is selected. Values: 1'b0: One-Step Timestamping feature is not selected 1'b1: One-Step Timestamping feature is selected
10:6	RO	0x07	TXFIFOSIZE MTL Transmit FIFO Size This field contains the configured value of MTL Tx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(TXFIFO_SIZE) -7: Values: 5'b00000: 128 bytes 5'b00001: 256 bytes 5'b00010: 512 bytes 5'b00011: 1024 bytes 5'b00100: 2048 bytes 5'b00101: 4096 bytes 5'b00110: 8192 bytes 5'b00111: 16384 bytes 5'b01000: 32 KB 5'b01001: 64 KB 5'b01010: 128 KB 5'b01011: Reserved

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Bit	Attr	Reset Value	Description
5	RO	0x1	SPRAM Single Port RAM Enable This bit is set to 1 when the Use single port RAM Feature is selected. Values: 1'b0: Single Port RAM feature is not selected 1'b1: Single Port RAM feature is selected
4:0	RO	0x08	RXFIFOSIZE MTL Receive FIFO Size This field contains the configured value of MTL Rx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(RXFIFO_SIZE) -7: Values: 5'b00000: 128 bytes 5'b00001: 256 bytes 5'b00010: 512 bytes 5'b00011: 1024 bytes 5'b00100: 2048 bytes 5'b00101: 4096 bytes 5'b00110: 8192 bytes 5'b00111: 16384 bytes 5'b01000: 32 KB 5'b01001: 64 KB 5'b01010: 128 KB 5'b01011: 256 KB 5'b01100: Reserved

GMAC_MAC_HW_FEATURE2

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RO	0x1	AUXSNAPNUM Number of Auxiliary Snapshot Inputs This field indicates the number of auxiliary snapshot inputs: Values: 3'b000: No auxiliary input 3'b001: 1 auxiliary input 3'b010: 2 auxiliary input 3'b011: 3 auxiliary input 3'b100: 4 auxiliary input 3'b101: Reserved
27	RO	0x0	reserved
26:24	RO	0x1	PPSOUTNUM Number of PPS Outputs This field indicates the number of PPS outputs: Values: 3'b000: No PPS output 3'b001: 1 PPS output 3'b010: 2 PPS output 3'b011: 3 PPS output 3'b100: 4 PPS output 3'b101: Reserved
23:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:18	RO	0x1	TXCHCNT Number of DMA Transmit Channels This field indicates the number of DMA Transmit channels: Values: 4'b0000: 1 MTL Tx Channel 4'b0001: 2 MTL Tx Channels 4'b0010: 3 MTL Tx Channels 4'b0011: 4 MTL Tx Channels 4'b0100: 5 MTL Tx Channels 4'b0101: 6 MTL Tx Channels 4'b0110: 7 MTL Tx Channels 4'b0111: 8 MTL Tx Channels
17:16	RO	0x0	reserved
15:12	RO	0x1	RXCHCNT Number of DMA Receive Channels This field indicates the number of DMA Receive channels: Values: 4'b0000: 1 MTL Rx Channel 4'b0001: 2 MTL Rx Channels 4'b0010: 3 MTL Rx Channels 4'b0011: 4 MTL Rx Channels 4'b0100: 5 MTL Rx Channels 4'b0101: 6 MTL Rx Channels 4'b0110: 7 MTL Rx Channels 4'b0111: 8 MTL Rx Channels
11:10	RO	0x0	reserved
9:6	RO	0x1	TXQCNT Number of MTL Transmit Queues This field indicates the number of MTL Transmit queues: Values: 4'b0000: 1 MTL Tx Queue 4'b0001: 2 MTL Tx Queues 4'b0010: 3 MTL Tx Queues 4'b0011: 4 MTL Tx Queues 4'b0100: 5 MTL Tx Queues 4'b0101: 6 MTL Tx Queues 4'b0110: 7 MTL Tx Queues 4'b0111: 8 MTL Tx Queues
5:4	RO	0x0	reserved
3:0	RO	0x1	RXQCNT Number of MTL Receive Queues This field indicates the number of MTL Receive queues: Values: 4'b0000: 1 MTL Rx Queue 4'b0001: 2 MTL Rx Queues 4'b0010: 3 MTL Rx Queues 4'b0011: 4 MTL Rx Queues 4'b0100: 5 MTL Rx Queues 4'b0101: 6 MTL Rx Queues 4'b0110: 7 MTL Rx Queues 4'b0111: 8 MTL Rx Queues

GMAC_MAC_HW_FEATURE3

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:28	RO	0x0	ASP Automotive Safety Package Following are the encoding for the different Safety features. Values: 2'b00: No Safety features selected 2'b01: Only "ECC protection for external memory" feature is selected 2'b10: All the Automotive Safety features are selected without the "Parity Port Enable for external interface" feature 2'b11: All the Automotive Safety features are selected with the "Parity Port Enable for external interface" feature
27	RO	0x1	TBSSEL Time Based Scheduling Enable This bit is set to 1 when the Time Based Scheduling feature is selected. Values: 1'b0: Time Based Scheduling Enable feature is not selected 1'b1: Time Based Scheduling Enable feature is selected
26	RO	0x1	FPESEL Frame Preemption Enable This bit is set to 1 when the Enable Frame preemption feature is selected. Values: 1'b0: Frame Preemption Enable feature is not selected 1'b1: Frame Preemption Enable feature is selected
25:22	RO	0x0	reserved
21:20	RO	0x3	ESTWID Width of the Time Interval field in the Gate Control List This field indicates the width of the Configured Time Interval Field. Values: 2'b00: Width not configured 2'b01: 16 2'b10: 20 2'b11: 24
19:17	RW	0x3	ESTDEP Depth of the Gate Control List This field indicates the depth of Gate Control list expressed as Log2(DWC_EQOS_EST_DEP)-5. Values: 3'b000: No Depth configured 3'b001: 64 3'b010: 128 3'b011: 256 3'b100: 512 3'b101: 1024 3'b110: Reserved
16	RO	0x1	ESTSEL Enhancements to Scheduling Traffic Enable This bit is set to 1 when the Enable Enhancements to Scheduling Traffic feature is selected. Values: 1'b0: Enable Enhancements to Scheduling Traffic feature is not selected 1'b1: Enable Enhancements to Scheduling Traffic feature is selected

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Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:13	RO	0x0	FRPES Flexible Receive Parser Table Entries size This field indicates the Max Number of Parser Entries supported by Flexible Receive Parser. Values: 2'b00: 64 Entries 2'b01: 128 Entries 2'b10: 256 Entries 2'b11: Reserved
12:11	RO	0x0	FRPBS Flexible Receive Parser Buffer size This field indicates the supported Max Number of bytes of the packet data to be Parsed by Flexible Receive Parser. Values: 2'b00: 64 Bytes 2'b01: 128 Bytes 2'b10: 256 Bytes 2'b11: Reserved
10	RO	0x0	FRPSEL Flexible Receive Parser Selected This bit is set to 1 when the Enable Flexible Programmable Receive Parser option is selected. Values: 1'b0: Flexible Receive Parser feature is not selected 1'b1: Flexible Receive Parser feature is selected
9	RO	0x0	PDUPSEL Broadcast/Multicast Packet Duplication This bit is set to 1 when the Broadcast/Multicast Packet Duplication feature is selected. Values: 1'b0: Broadcast/Multicast Packet Duplication feature is not selected 1'b1: Broadcast/Multicast Packet Duplication feature is selected
8:6	RO	0x0	reserved
5	RO	0x1	DVLAN Double VLAN Tag Processing Selected This bit is set to 1 when the Enable Double VLAN Processing Feature is selected. Values: 1'b0: Double VLAN option is not selected 1'b1: Double VLAN option is selected
4	RO	0x1	CBTISEL Queue/Channel based VLAN tag insertion on Tx Enable This bit is set to 1 when the Enable Queue/Channel based VLAN tag insertion on Tx Feature is selected. Values: 1'b0: Enable Queue/Channel based VLAN tag insertion on Tx feature is not selected 1'b1: Enable Queue/Channel based VLAN tag insertion on Tx feature is selected
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RO	0x1	NRVF Number of Extended VLAN Tag Filters Enabled This field indicates the Number of Extended VLAN Tag Filters selected: Values: 3'b000: No Extended Rx VLAN Filters 3'b001: 4 Extended Rx VLAN Filters 3'b010: 8 Extended Rx VLAN Filters 3'b011: 16 Extended Rx VLAN Filters 3'b100: 24 Extended Rx VLAN Filters 3'b101: 32 Extended Rx VLAN Filters 3'b110: Reserved

GMAC_MAC_MDIO_ADDRESS

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	PSE Preamble Suppression Enable When this bit is set, the SMA suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. When this bit is 0, the MDIO frame always has 32 bits of preamble as defined in the IEEE specifications. Values: 1'b0: Preamble Suppression disabled 1'b1: Preamble Suppression enabled
26	RW	0x0	BTB Back to Back transactions When this bit is set and the NTC has value greater than 0, then the MAC informs the completion of a read or write command at the end of frame transfer (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated for the previous frame. When this bit is reset, then the read/write command completion (GB is cleared) only after the trailing clocks are generated. In this mode, it is ensured that the NTC is always generated after each frame. This bit must not be set when NTC=0. Values: 1'b0: Back to Back transactions disabled 1'b1: Back to Back transactions enabled
25:21	RW	0x00	PA Physical Layer Address This field indicates which Clause 22 PHY devices (out of 32 devices) the MAC is accessing. For RevMII, this field gives the PHY Address of the RevMII module. This field indicates which Clause 45 capable PHYs (out of 32 PHYs) the MAC is accessing.
20:16	RW	0x00	RDA Register/Device Address These bits select the PHY register in selected Clause 22 PHY device. For RevMII, these bits select the CSR register in the RevMII Registers set. These bits select the Device (MMD) in selected Clause 45 capable PHY.
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:12	RW	0x0	NTC Number of Trailing Clocks This field controls the number of trailing clock cycles generated on gmii_mdc_o (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. Programming the value to 3'h3 indicates that there are additional three clock cycles on the MDC line after the end of MDIO frame transfer.
11:8	RW	0x0	CR CSR Clock Range The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design: 4'b0000: CSR clock = 60-100 MHz; MDC clock = CSR clock/42 4'b0001: CSR clock = 100-150 MHz; MDC clock = CSR clock/62 4'b0010: CSR clock = 20-35 MHz; MDC clock = CSR clock/16 4'b0011: CSR clock = 35-60 MHz; MDC clock = CSR clock/26 4'b0100: CSR clock = 150-250 MHz; MDC clock = CSR clock/102 4'b0101: CSR clock = 250-300 MHz; MDC clock = CSR clock/124 4'b0110: CSR clock = 300-500 MHz; MDC clock = CSR clock/204 4'b0111: CSR clock = 500-800 MHz; MDC clock = CSR clock/324 The suggested range of CSR clock frequency applicable for each value (when Bit 11 = 0) ensures that the MDC clock is approximately between 1.0 MHz to 2.5 MHz frequency range. When Bit 11 is set, you can achieve a higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, the resultant MDC clock is of 12.5 MHz which is above the range specified in IEEE 802.3. Program the following values only if the interfacing chips support faster MDC clocks: 4'b1000: CSR clock/4 4'b1001: CSR clock/6 4'b1010: CSR clock/8 4'b1011: CSR clock/10 4'b1100: CSR clock/12 4'b1101: CSR clock/14 4'b1110: CSR clock/16 4'b1111: CSR clock/18 These bits are not used for accessing RevMII. These bits are read-only if the RevMII interface is selected as single PHY interface.
7:5	RO	0x0	reserved
4	RW	0x0	SKAP Skip Address Packet When this bit is set, the SMA does not send the address packets before read, write, or post-read increment address packets. This bit is valid only when C45E is set. Values: 1'b0: Skip Address Packet is disabled 1'b1: Skip Address Packet is enabled

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Bit	Attr	Reset Value	Description
3	RW	0x0	GOC_1 GMII Operation Command 1 This bit is higher bit of the operation command to the PHY or RevMII, GOC_1 and GOC_O is encoded as follows: 2'b00: Reserved 2'b01: Write 2'b10: Post Read Increment Address for Clause 45 PHY 2'b11: Read When Clause 22 PHY or RevMII is enabled, only Write and Read commands are valid. Values: 1'b0: GMII Operation Command 1 is disabled 1'b1: GMII Operation Command 1 is enabled
2	RW	0x0	GOC_0 GMII Operation Command 0 This is the lower bit of the operation command to the PHY or RevMII. When in SMA mode (MDIO master) this bit along with GOC_1 determines the operation to be performed to the PHY. When only RevMII is selected in configuration this bit is read-only and tied to 1. Values: 1'b0: GMII Operation Command 0 is disabled 1'b1: GMII Operation Command 0 is enabled
1	RW	0x0	C45E Clause 45 PHY Enable When this bit is set, Clause 45 capable PHY is connected to MDIO. When this bit is reset, Clause 22 capable PHY is connected to MDIO. Values: 1'b0: Clause 45 PHY is disabled 1'b1: Clause 45 PHY is enabled
0	RW	0x0	GB GMII Busy The application sets this bit to instruct the SMA to initiate a Read or Write access to the MDIO slave. The MAC clears this bit after the MDIO frame transfer is completed. Hence the software must not write or change any of the fields in MAC_MDIO_Address and MAC_MDIO_Data registers as long as this bit is set. For write transfers, the application must first write 16-bit data in the GDl field (and also RA field when C45E is set) in MAC_MDIO_Data register before setting this bit. When C45E is set, it should also write into the RA field of MAC_MDIO_Data register before initiating a read transfer. When a read transfer is completed (GB=0), the data read from the PHY register is valid in the GD field of the MAC_MDIO_Data register. Note: Even if the addressed PHY is not present, there is no change in the functionality of this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: GMII Busy is disabled 1'b1: GMII Busy is enabled

GMAC_MAC_MDIO_DATA

Address: **Operational Base** + offset (0x0204)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	RA Register Address This field is valid only when C45E is set. It contains the Register Address in the PHY to which the MDIO frame is intended for.
15:0	RW	0x0000	GD GMII Data This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation.

GMAC_MAC_ARP_ADDRESS

Address: **Operational Base** + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ARPPA ARP Protocol Address This field contains the IPv4 Destination Address of the MAC. This address is used for perfect match with the Protocol Address of Target field in the received ARP packet. This field is available only when the Enable IPv4 ARP Offload option is selected.

GMAC_MAC_CSR_SW_CTRL

Address: **Operational Base** + offset (0x0230)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	RCWE Register Clear on Write 1 Enable When this bit is set, the access mode of some register fields changes to Clear on Write 1, the application needs to set that respective bit to 1 to clear it. When this bit is reset, the access mode of these register fields remain as Clear on Read. Values: 1'b0: Register Clear on Write 1 is disabled 1'b1: Register Clear on Write 1 is enabled

GMAC_MAC_FPE_CTRL_STS

Address: **Operational Base** + offset (0x0234)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	TRSP Transmitted Respond Frame Set when a Respond mPacket is transmitted (triggered by setting SRSP field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 0x0 (INACTIVE): Not transmitted Respond Frame 0x1 (ACTIVE): transmitted Respond Frame

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Bit	Attr	Reset Value	Description
18	RW	0x0	TVER Transmitted Verify Frame Set when a Verify mPacket is transmitted (triggered by setting SVER field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 0x0 (INACTIVE): Not transmitted Verify Frame 0x1 (ACTIVE): transmitted Verify Frame
17	RW	0x0	RRSP Received Respond Frame Set when a Respond mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 0x0 (INACTIVE): Not received Respond Frame 0x1 (ACTIVE): Received Respond Frame
16	RW	0x0	RVER Received Verify Frame Set when a Verify mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 0x0 (INACTIVE): Not received Verify Frame 0x1 (ACTIVE): Received Verify Frame
15:4	RO	0x000	reserved
3	RW	0x0	S1_SET_0 Reserved, Must be set to "0". This field is reserved for Internal use, and must always be set to "0" unless instructed by Rockchip. Setting to "1" might cause unexpected behavior in the IP.
2	RW	0x0	SRSP Send Respond mPacket When set indicates hardware to send a Respond mPacket. Reset by hardware after sending the Respond mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 0x0 (DISABLE): Send Respond mPacket is disabled 0x1 (ENABLE): Send Respond mPacket is enabled
1	RW	0x0	SVER Send Verify mPacket When set indicates hardware to send a verify mPacket. Reset by hardware after sending the Verify mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 0x0 (DISABLE): Send Verify mPacket is disabled 0x1 (ENABLE): Send Verify mPacket is enabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	EFPE Enable Tx Frame Preemption When set Frame Preemption Tx functionality is enabled. Values: 0x0 (DISABLE): Tx Frame Preemption is disabled 0x1 (ENABLE): Tx Frame Preemption is enabled

GMAC_MAC_EXT_CFG1

Address: **Operational Base** + offset (0x0238)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	SPLM Split Mode These bits indicate the mode of splitting the incoming Rx packets. Values: 0x0 (L3L4): Split at L3/L4 header 0x1 (L2OFST): Split at L2 header with an offset. Always Split at SPLOFST bytes from the beginning of Length/Type field of the Frame 0x2 (COMBN): Combination mode: Split similar to SPLM=00 for IP packets that are untagged or tagged and VLAN stripped 0x3 (RSVD): Reserved
7	RO	0x0	reserved
6:0	RW	0x00	SPLOFST Split Offset These bits indicate the value of offset from the beginning of Length/Type field at which header split should take place when the appropriate SPLM is selected. The reset value of this field is 2 bytes indicating a split at L2 header. Value is in terms of bytes.

GMAC_MAC_PRESN_TIME_NS

Address: **Operational Base** + offset (0x0240)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RO	0x000000	MPTN MAC 1722 Presentation Time in ns These bits indicate the value of the 32-bit binary rollover equivalent time of the PTP System Time in ns.

GMAC_MAC_PRESN_TIME_UPDT

Address: **Operational Base** + offset (0x0244)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MPTU MAC 1722 Presentation Time Update This field holds the init value or the update value for the presentation time. When used for update, this field holds the 32-bit value in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register). When ADDSUB field of MAC_System_Time_Nanoseconds_Update is set, this value is directly used for subtraction.

GMAC_MAC_ADDRESS0_HIGH

Address: **Operational Base** + offset (0x0300)

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Bit	Attr	Reset Value	Description
31	RO	0x0	AE Address Enable This bit is always set to 1. Values: 1'b0: This bit must be always set to 1 1'b1: This bit is always set to 1
30	RW	0x0	SA Source Address When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. Values: 0x0 (DA): Compare with Destination Address 0x1 (SA): Compare with Source Address
29:24	RW	0x00	MBC Mask Byte Control These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: Bit 29: MAC_Address0_High[15:8] Bit 28: MAC_Address0_High[7:0] Bit 27: MAC_Address0_Low[31:24] ... Bit 24: MAC_Address0_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:17	RO	0x00	reserved
16	RW	0x0	DCS DMA Channel Select If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address0 content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address0 content is routed.
15:0	RW	0xffff	ADDRHI MAC Address0[47:32] This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

GMAC_MAC_ADDRESS0_LOW

Address: **Operational Base** + offset (0x0304)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	ADDRLO MAC Address0[31:0] This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

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GMAC_MMC_CONTROL

Address: **Operational Base** + offset (0x0700)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	UCDBC Update MMC Counters for Dropped Broadcast Packets Note: The CNTRST bit has a higher priority than the CNTPRST bit. Therefore, when the software tries to set both bits in the same write cycle, all counters are cleared and the CNTPRST bit is not set. When set, the MAC updates all related MMC Counters for Broadcast packets that are dropped because of the setting of the DBF bit of MAC_Packet_Filter register. When reset, the MMC Counters are not updated for dropped Broadcast packets. Values: 1'b0: Update MMC Counters for Dropped Broadcast Packets is disabled 1'b1: Update MMC Counters for Dropped Broadcast Packets is enabled
7:6	RO	0x0	reserved
5	RW	0x0	CNTPRSTLVL Full-Half Preset When this bit is low and the CNTPRST bit is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (Half 2KBytes) and all packet-counters gets preset to 0x7FFF_FFF0 (Half 16). When this bit is high and the CNTPRST bit is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (Full 2KBytes) and all packet-counters gets preset to 0xFFFF_FFF0 (Full 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and packet counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFF0. Values: 1'b0: Full-Half Preset is disabled 1'b1: Full-Half Preset is enabled
4	RW	0x0	CNTPRST Counters Preset When this bit is set, all counters are initialized or preset to almost full or almost half according to the CNTPRSTLVL bit. This bit is cleared automatically after 1 clock cycle. This bit, along with the CNTPRSTLVL bit, is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Counters Preset is disabled 1'b1: Counters Preset is enabled

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Bit	Attr	Reset Value	Description
3	RW	0x0	CNTFREEZ MMC Counter Freeze When this bit is set, it freezes all MMC counters to their current value. Until this bit is reset to 0, no MMC counter is updated because of any transmitted or received packet. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode. Values: 1'b0: MMC Counter Freeze is disabled 1'b1: MMC Counter Freeze is enabled
2	RW	0x0	RSTONRD Reset on Read When this bit is set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (Bits[7:0]) is read. Values: 1'b0: Reset on Read is disabled 1'b1: Reset on Read is enabled
1	RW	0x0	CNTSTOPRO Counter Stop Rollover When this bit is set, the counter does not roll over to zero after reaching the maximum value. Values: 1'b0: Counter Stop Rollover is disabled 1'b1: Counter Stop Rollover is enabled
0	RW	0x0	CNTRST Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Counters are not reset 1'b1: All counters are reset

GMAC_MMC_RX_INTERRUPT

Address: **Operational Base** + offset (0x0704)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RO	0x0	RXWDOGPIS MMC Receive Watchdog Error Packet Counter Interrupt Status This bit is set when the rxwatchdog error counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 0x0 (INACTIVE): MMC Receive Watchdog Error Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Watchdog Error Packet Counter Interrupt Status detected
22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21	RO	0x0	RXFOVPIS MMC Receive FIFO Overflow Packet Counter Interrupt Status This bit is set when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive FIFO Overflow Packet Counter Interrupt Status not detected 1'b1: MMC Receive FIFO Overflow Packet Counter Interrupt Status detected
20	RO	0x0	RXPAUSPIS MMC Receive Pause Packet Counter Interrupt Status This bit is set when the rxpausepackets counter reaches half of the maximum value or the maximum value.Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 0x0 (INACTIVE): MMC Receive Pause Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Pause Packet Counter Interrupt Status detected
19	RO	0x0	reserved
18	RO	0x0	RXLENERPIS MMC Receive Length Error Packet Counter Interrupt Status This bit is set when the rxlengtherror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Length Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive Length Error Packet Counter Interrupt Status detected
17:11	RO	0x00	reserved
10	RO	0x0	RXOSIZEGPIS MMC Receive Oversize Good Packet Counter Interrupt Status This bit is set when the rxoversize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 0x0 (INACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status detected
9:6	RO	0x0	reserved
5	RO	0x0	RXCRCERPIS MMC Receive CRC Error Packet Counter Interrupt Status This bit is set when the rxcrcerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive CRC Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive CRC Error Packet Counter Interrupt Status detected

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Bit	Attr	Reset Value	Description
4	RO	0x0	RXMCGPIS MMC Receive Multicast Good Packet Counter Interrupt Status This bit is set when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Multicast Good Packet Counter Interrupt Status not detected 1'b1: MMC Receive Multicast Good Packet Counter Interrupt Status detected
3	RO	0x0	reserved
2	RO	0x0	RXGOCTIS MMC Receive Good Octet Counter Interrupt Status This bit is set when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Good Octet Counter Interrupt Status not detected 1'b1: MMC Receive Good Octet Counter Interrupt Status detected
1	RO	0x0	RXGBOCTIS MMC Receive Good Bad Octet Counter Interrupt Status This bit is set when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Good Bad Octet Counter Interrupt Status not detected 1'b1: MMC Receive Good Bad Octet Counter Interrupt Status detected
0	RO	0x0	RXGBPKTIS MMC Receive Good Bad Packet Counter Interrupt Status This bit is set when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Good Bad Packet Counter Interrupt Status not detected 1'b1: MMC Receive Good Bad Packet Counter Interrupt Status detected

GMAC_MMC_TX_INTERRUPT

Address: **Operational Base** + offset (0x0708)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23	RO	0x0	TXPAUSPIS MMC Transmit Pause Packet Counter Interrupt Status This bit is set when the txpausepacketserror counter reaches half of the maximum value or the maximum value.Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 0x0 (INACTIVE): MMC Transmit Pause Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Transmit Pause Packet Counter Interrupt Status detected
22	RO	0x0	reserved
21	RO	0x0	TXGPKTIS MMC Transmit Good Packet Counter Interrupt Status This bit is set when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Packet Counter Interrupt Status detected
20	RO	0x0	TXGOCTIS MMC Transmit Good Octet Counter Interrupt Status This bit is set when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Octet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Octet Counter Interrupt Status detected
19	RO	0x0	TXCARERPIS MMC Transmit Carrier Error Packet Counter Interrupt Status This bit is set when the txcarriererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Carrier Error Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Carrier Error Packet Counter Interrupt Status detected
18:14	RO	0x00	reserved
13	RO	0x0	TXUFLOWERPIS MMC Transmit Underflow Error Packet Counter Interrupt Status This bit is set when the txunderflowerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Underflow Error Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Underflow Error Packet Counter Interrupt Status detected

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Bit	Attr	Reset Value	Description
12:2	RO	0x000	reserved
1	RO	0x0	TXGBPKTIS MMC Transmit Good Bad Packet Counter Interrupt Status This bit is set when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Bad Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Bad Packet Counter Interrupt Status detected
0	RO	0x0	TXGBOCTIS MMC Transmit Good Bad Octet Counter Interrupt Status This bit is set when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Bad Octet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Bad Octet Counter Interrupt Status detected

GMAC_MMC_RX_INTERRUPT_MASK

Address: **Operational Base** + offset (0x070C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	RXWDOGPIM MMC Receive Watchdog Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxwatchdog counter reaches half of the maximum value or the maximum value. Values: 0x0 (DISABLE): MMC Receive Watchdog Error Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Watchdog Error Packet Counter Interrupt Mask is enabled
22	RO	0x0	reserved
21	RW	0x0	RXFOVPIM MMC Receive FIFO Overflow Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive FIFO Overflow Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive FIFO Overflow Packet Counter Interrupt Mask is enabled

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Bit	Attr	Reset Value	Description
20	RW	0x0	RXPAUSPIM MMC Receive Pause Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxpausepackets counter reaches half of the maximum value or the maximum value. Values: 0x0 (DISABLE): MMC Receive Pause Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Pause Packet Counter Interrupt Mask is enabled
19	RO	0x0	reserved
18	RW	0x0	RXLENERPIM MMC Receive Length Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxlengtherror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Length Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive Length Error Packet Counter Interrupt Mask is enabled
17:11	RO	0x00	reserved
10	RW	0x0	RXOSIZEGPIM MMC Receive Oversize Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoversize_g counter reaches half of the maximum value or the maximum value. Values: 0x0 (DISABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is enabled
9:6	RO	0x0	reserved
5	RW	0x0	RXCRCERPIM MMC Receive CRC Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxcrcerror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive CRC Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive CRC Error Packet Counter Interrupt Mask is enabled
4	RW	0x0	RXMCGPIM MMC Receive Multicast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Multicast Good Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive Multicast Good Packet Counter Interrupt Mask is enabled
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	RXGOCTIM MMC Receive Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Good Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive Good Octet Counter Interrupt Mask is enabled
1	RW	0x0	RXGBOCTIM MMC Receive Good Bad Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Good Bad Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive Good Bad Octet Counter Interrupt Mask is enabled
0	RW	0x0	RXGBPKTIM MMC Receive Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Good Bad Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive Good Bad Packet Counter Interrupt Mask is enabled

GMAC_MMC_TX_INTERRUPT_MASK

Address: **Operational Base** + offset (0x0710)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	TXPAUSPIM MMC Transmit Pause Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpausepackets counter reaches half of the maximum value or the maximum value. Values: 0x0 (DISABLE): MMC Transmit Pause Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Pause Packet Counter Interrupt Mask is enabled
22	RO	0x0	reserved
21	RW	0x0	TXGPKTIM MMC Transmit Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Packet Counter Interrupt Mask is enabled

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Bit	Attr	Reset Value	Description
20	RW	0x0	TXGOCTIM MMC Transmit Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Octet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Octet Counter Interrupt Mask is enabled
19	RW	0x0	TXCARERPIM MMC Transmit Carrier Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txcarriererror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Carrier Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Carrier Error Packet Counter Interrupt Mask is enabled
18:14	RO	0x00	reserved
13	RW	0x0	TXUFLOWERPIM MMC Transmit Underflow Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txunderflowerror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Underflow Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Underflow Error Packet Counter Interrupt Mask is enabled
12:2	RO	0x000	reserved
1	RW	0x0	TXGBPKTIM MMC Transmit Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Bad Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Bad Packet Counter Interrupt Mask is enabled
0	RW	0x0	TXGBOCTIM MMC Transmit Good Bad Octet Counter Interrupt Mask Setting this bit masks the interrupt when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Bad Octet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Bad Octet Counter Interrupt Mask is enabled

GMAC_TX_OCTET_COUNT_GOOD_BAD

Address: **Operational Base** + offset (0x0714)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXOCTGB Tx Octet Count Good Bad This field indicates the number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad packets.

GMAC_TX_PACKET_COUNT_GOOD_BAD

Address: **Operational Base** + offset (0x0718)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXPKTGB Tx Packet Count Good Bad This field indicates the number of good and bad packets transmitted, exclusive of retried packets.

GMAC_TX_UNDERFLOW_ERROR_PACKETS

Address: **Operational Base** + offset (0x0748)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXUNDRFLW Tx Underflow Error Packets This field indicates the number of packets aborted because of packets underflow error.

GMAC_TX_CARRIER_ERROR_PACKETS

Address: **Operational Base** + offset (0x0760)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXCARR Tx Carrier Error Packets This field indicates the number of packets aborted because of carrier sense error (no carrier or loss of carrier).

GMAC_TX_OCTET_COUNT_GOOD

Address: **Operational Base** + offset (0x0764)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXOCTG Tx Octet Count Good This field indicates the number of bytes transmitted, exclusive of preamble, only in good packets.

GMAC_TX_PACKET_COUNT_GOOD

Address: **Operational Base** + offset (0x0768)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXPKTG Tx Packet Count Good This field indicates the number of good packets transmitted.

GMAC_TX_PAUSE_PACKETS

Address: **Operational Base** + offset (0x0770)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXPAUSE Tx Pause Packets This field indicates the number of good Pause packets transmitted.

GMAC_RX_PACKETS_COUNT_GOOD_BAD

Address: **Operational Base** + offset (0x0780)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXPKTGB Rx Packets Count Good Bad This field indicates the number of good and bad packets received.

GMAC_RX_OCTET_COUNT_GOOD_BAD

Address: **Operational Base** + offset (0x0784)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXOCTGB Rx Octet Count Good Bad This field indicates the number of bytes received, exclusive of preamble, in good and bad packets.

GMAC_RX_OCTET_COUNT_GOOD

Address: **Operational Base** + offset (0x0788)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXOCTG Rx Octet Count Good This field indicates the number of bytes received, exclusive of preamble, only in good packets.

GMAC_RX_MULTICAST_PACKETS_GOOD

Address: **Operational Base** + offset (0x0790)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXMCASTG Rx Multicast Packets Good This field indicates the number of good multicast packets received.

GMAC_RX_CRC_ERROR_PACKETS

Address: **Operational Base** + offset (0x0794)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXCRCERR Rx CRC Error Packets This field indicates the number of packets received with CRC error.

GMAC_RX_OVERSIZE_PACKETS_GOOD

Address: **Operational Base** + offset (0x07A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXOVERSZG Rx Oversize Packets Good This field indicates the number of packets received without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register).

GMAC_RX_LENGTH_ERROR_PACKETS

Address: **Operational Base** + offset (0x07C8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXLENERR Rx Length Error Packets This field indicates the number of packets received with length error (Length Type field not equal to packet size), for all packets with valid length field.

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GMAC_RX_PAUSE_PACKETS

Address: **Operational Base** + offset (0x07D0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXPAUSEPKT Rx Pause Packets This field indicates the number of good and valid Pause packets received.

GMAC_RX_FIFO_OVERFLOW_PACKETS

Address: **Operational Base** + offset (0x07D4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXFIFOOVFL Rx FIFO Overflow Packets This field indicates the number of missed received packets because of FIFO overflow.

GMAC_RX_WATCHDOG_ERROR_PACKETS

Address: **Operational Base** + offset (0x07DC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXWDGERR Rx Watchdog Error Packets This field indicates the number of packets received with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register).

GMAC_MMC_IPC_RX_INTERRUPT_MASK

Address: **Operational Base** + offset (0x0800)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	RXICMPEROIM MMC Receive ICMP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive ICMP Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive ICMP Error Octet Counter Interrupt Mask is enabled
28	RO	0x0	reserved
27	RW	0x0	RXTCPEROIM MMC Receive TCP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive TCP Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive TCP Error Octet Counter Interrupt Mask is enabled
26	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
25	RW	0x0	RXUDPEROIM MMC Receive UDP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive UDP Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive UDP Error Octet Counter Interrupt Mask is enabled
24:23	RO	0x0	reserved
22	RW	0x0	RXIPV6HEROIM MMC Receive IPV6 Header Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value. Value: 1'b0: MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is enabled
21:18	RO	0x0	reserved
17	RW	0x0	RXIPV4HEROIM MMC Receive IPV4 Header Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is enabled
16:14	RO	0x0	reserved
13	RW	0x0	RXICMPERPIM MMC Receive ICMP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive ICMP Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive ICMP Error Packet Counter Interrupt Mask is enabled
12	RO	0x0	reserved
11	RW	0x0	RXTCPERPIM MMC Receive TCP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive TCP Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive TCP Error Packet Counter Interrupt Mask is enabled
10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	RXUDPERPIM MMC Receive UDP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive UDP Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive UDP Error Packet Counter Interrupt Mask is enabled
8:7	RO	0x0	reserved
6	RW	0x0	RXIPV6HERPIM MMC Receive IPV6 Header Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is enabled
5	RW	0x0	RXIPV6GPIM MMC Receive IPV6 Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV6 Good Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV6 Good Packet Counter Interrupt Mask is enabled
4:2	RO	0x0	reserved
1	RW	0x0	RXIPV4HERPIM MMC Receive IPV4 Header Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is enabled
0	RW	0x0	RXIPV4GPIM MMC Receive IPV4 Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV4 Good Packet Counter Interrupt Mask is disable 1'b1: MMC Receive IPV4 Good Packet Counter Interrupt Mask is enabled

GMAC_MMC_IPC_RX_INTERRUPT

Address: **Operational Base** + offset (0x0808)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RO	0x0	RXICMPEROIS MMC Receive ICMP Error Octet Counter Interrupt Status This bit is set when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive ICMP Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive ICMP Error Octet Counter Interrupt Status detected
28	RO	0x0	reserved
27	RO	0x0	RXTCPEROIS MMC Receive TCP Error Octet Counter Interrupt Status This bit is set when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive TCP Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive TCP Error Octet Counter Interrupt Status detected
26	RO	0x0	reserved
25	RO	0x0	RXUDPEROIS MMC Receive UDP Error Octet Counter Interrupt Status This bit is set when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive UDP Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive UDP Error Octet Counter Interrupt Status detected
24:23	RO	0x0	reserved
22	RO	0x0	RXIPV6HEROIS MMC Receive IPV6 Header Error Octet Counter Interrupt Status This bit is set when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV6 Header Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive IPV6 Header Error Octet Counter Interrupt Status detected
21:18	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
17	RO	0x0	RXIPV4HEROIS MMC Receive IPV4 Header Error Octet Counter Interrupt Status This bit is set when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV4 Header Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive IPV4 Header Error Octet Counter Interrupt Status detected
16:14	RO	0x0	reserved
13	RO	0x0	RXICMPERPIS MMC Receive ICMP Error Packet Counter Interrupt Status This bit is set when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive ICMP Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive ICMP Error Packet Counter Interrupt Status detected
12	RO	0x0	reserved
11	RO	0x0	RXTCPERPIS MMC Receive TCP Error Packet Counter Interrupt Status This bit is set when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive TCP Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive TCP Error Packet Counter Interrupt Status detected
10	RO	0x0	reserved
9	RO	0x0	RXUDPERPIS MMC Receive UDP Error Packet Counter Interrupt Status This bit is set when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive UDP Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive UDP Error Packet Counter Interrupt Status detected
8:7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RO	0x0	RXIPV6HERPIS MMC Receive IPV6 Header Error Packet Counter Interrupt Status This bit is set when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV6 Header Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV6 Header Error Packet Counter Interrupt Status detected
5	RO	0x0	RXIPV6GPIS MMC Receive IPV6 Good Packet Counter Interrupt Status This bit is set when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV6 Good Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV6 Good Packet Counter Interrupt Status detected
4:2	RO	0x0	reserved
1	RO	0x0	RXIPV4HERPIS MMC Receive IPV4 Header Error Packet Counter Interrupt Status This bit is set when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV4 Header Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV4 Header Error Packet Counter Interrupt Status detected
0	RO	0x0	RXIPV4GPIS MMC Receive IPV4 Good Packet Counter Interrupt Status This bit is set when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV4 Good Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV4 Good Packet Counter Interrupt Status detected

GMAC_RXIPV4_GOOD_PACKETS

Address: **Operational Base** + offset (0x0810)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV4GDPKT RxIPv4 Good Packets This field indicates the number of good IPv4 datagrams received with the TCP, UDP, or ICMP payload.

GMAC_RXIPV4_HEADER_ERROR_PACKETS

Address: **Operational Base** + offset (0x0814)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV4HDRERRPKT RxIPv4 Header Error Packets This field indicates the number of IPv4 datagrams received with header (checksum, length, or version mismatch) errors.

GMAC_RXIPV6_GOOD_PACKETS

Address: **Operational Base** + offset (0x0824)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV6GDPKT RxIPv6 Good Packets This field indicates the number of good IPv6 datagrams received with the TCP, UDP, or ICMP payload.

GMAC_RXIPV6_HEADER_ERROR_PACKETS

Address: **Operational Base** + offset (0x0828)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV6HDRERRPKT RxIPv6 Header Error Packets This field indicates the number of IPv6 datagrams received with header (length or version mismatch) errors.

GMAC_RXUDP_ERROR_PACKETS

Address: **Operational Base** + offset (0x0834)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXUDPERRPKT RxUDP Error Packets This field indicates the number of good IP datagrams received whose UDP payload has a checksum error.

GMAC_RXTCP_ERROR_PACKETS

Address: **Operational Base** + offset (0x083C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXTCPERRPKT RxTCP Error Packets This field indicates the number of good IP datagrams received whose TCP payload has a checksum error.

GMAC_RXICMP_ERROR_PACKETS

Address: **Operational Base** + offset (0x0844)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXICMPERRPKT RxICMP Error Packets This field indicates the number of good IP datagrams received whose ICMP payload has a checksum error.

GMAC_RXIPV4_HEADER_ERROR_OCTETS

Address: **Operational Base** + offset (0x0854)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV4HDRERROCT RxIPv4 Header Error Octets This field indicates the number of bytes received in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

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GMAC_RXIPV6_HEADER_ERROR_OCTETS

Address: **Operational Base** + offset (0x0868)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV6HDRERROCT RxIPv6 Header Error Octets This field indicates the number of bytes received in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

GMAC_RXUDP_ERROR_OCTETS

Address: **Operational Base** + offset (0x0874)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXUDPERROCT RxUDP Error Octets This field indicates the number of bytes received in a UDP segment that had checksum errors. This counter does not count IP header bytes.

GMAC_RXTCP_ERROR_OCTETS

Address: **Operational Base** + offset (0x087C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXTCPERROCT RxTCP Error Octets This field indicates the number of bytes received in a TCP segment that had checksum errors. This counter does not count IP header bytes.

GMAC_RXICMP_ERROR_OCTETS

Address: **Operational Base** + offset (0x0884)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXICMPERROCT RxICMP Error Octets This field indicates the number of bytes received in a ICMP segment that had checksum errors. This counter does not count IP header bytes.

GMAC_MMC_FPE_TX_INTERRUPT

Address: **Operational Base** + offset (0x08A0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	HRCIS MMC Tx Hold Request Counter Interrupt Status This bit is set when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration. Values: 0x0 (INACTIVE): MMC Tx Hold Request Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Tx Hold Request Counter Interrupt Status detected

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Bit	Attr	Reset Value	Description
0	RO	0x0	FCIS MMC Tx FPE Fragment Counter Interrupt status This bit is set when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. Values: 0x0 (INACTIVE): MMC Tx FPE Fragment Counter Interrupt status not detected 0x1 (ACTIVE): MMC Tx FPE Fragment Counter Interrupt status detected

GMAC_MMC_FPE_TX_INTERRUPT_MASK

Address: **Operational Base** + offset (0x08A4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	HRCIM MMC Transmit Hold Request Counter Interrupt Mask Setting this bit masks the interrupt when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration. Values: 0x0 (DISABLE): MMC Transmit Hold Request Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Hold Request Counter Interrupt Mask is enabled
0	RW	0x0	FCIM MMC Transmit Fragment Counter Interrupt Mask Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. Values: 0x0 (DISABLE): MMC Transmit Fragment Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Fragment Counter Interrupt Mask is enabled

GMAC_MMC_TX_FPE_FRAGMENT_CNTR

Address: **Operational Base** + offset (0x08A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXFFC Tx FPE Fragment counter This field indicates the number of additional mPackets that has been transmitted due to preemption. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

GMAC_MMC_TX_HOLD_REQ_CNTR

Address: **Operational Base** + offset (0x08AC)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXHRC Tx Hold Request Counter This field indicates count of number of a hold request is given to MAC. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration.

GMAC_MMC_FPE_RX_INTERRUPT

Address: **Operational Base** + offset (0x08C0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	FCIS MMC Rx FPE Fragment Counter Interrupt Status This bit is set when the Rx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. Values: 0x0 (INACTIVE): MMC Rx FPE Fragment Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Rx FPE Fragment Counter Interrupt Status detected
2	RO	0x0	PAOCIS MMC Rx Packet Assembly OK Counter Interrupt Status This bit is set when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. Values: 0x0 (INACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status detected
1	RO	0x0	PSECIS MMC Rx Packet SMD Error Counter Interrupt Status This bit is set when the Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. Values: 0x0 (INACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status detected

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Bit	Attr	Reset Value	Description
0	RO	0x0	PAECIS MMC Rx Packet Assembly Error Counter Interrupt Status This bit is set when the Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. Values: 0x0 (INACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status detected

GMAC_MMC_FPE_RX_INTERRUPT_MASK

Address: **Operational Base** + offset (0x08C4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	FCIM MMC Rx FPE Fragment Counter Interrupt Mask Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. Values: 0x0 (DISABLE): MMC Rx FPE Fragment Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Rx FPE Fragment Counter Interrupt Mask is enabled
2	RW	0x0	PAOCIM MMC Rx Packet Assembly OK Counter Interrupt Mask Setting this bit masks the interrupt when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. Values: 0x0 (DISABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is enabled
1	RW	0x0	PSECIM MMC Rx Packet SMD Error Counter Interrupt Mask Setting this bit masks the interrupt when the Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. Values: 0x0 (DISABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is enabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	PAECIM MMC Rx Packet Assembly Error Counter Interrupt Mask Setting this bit masks the interrupt when the Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. Values: 0x0 (DISABLE): MMC Rx Packet Assembly Error Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Rx Packet Assembly Error Counter Interrupt Mask is enabled

GMAC_MMC_RX_PACKET_ASM_ERR_CNTR

Address: **Operational Base** + offset (0x08C8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAEC Rx Packet Assembly Error Counter This field indicates the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

GMAC_MMC_RX_PACKET_SMD_ERR_CNTR

Address: **Operational Base** + offset (0x08CC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PSEC Rx Packet SMD Error Counter This field indicates the number of MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no preceding preempted frame. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

GMAC_MMC_RX_PACKET_ASSEMBLY_OK_CNTR

Address: **Operational Base** + offset (0x08D0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAOC Rx Packet Assembly OK Counter This field indicates the number of MAC frames that were successfully reassembled and delivered to MAC. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

GMAC_MMC_RX_FPE_FRAGMENT_CNTR

Address: **Operational Base** + offset (0x08D4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	FFC Rx FPE Fragment Counter This field indicates the number of additional mPackets received due to preemption. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

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GMAC_MAC_L3_L4_CONTROL0

Address: **Operational Base** + offset (0x0900)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	DMCHEN0 DMA Channel Select Enable When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter. Values: 0x0 (DISABLE): DMA Channel Select is disabled 0x1 (ENABLE): DMA Channel Select is enabled
27:25	RO	0x0	reserved
24	RW	0x0	DMCHN0 DMA Channel Number When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration.
23:22	RO	0x0	reserved
21	RW	0x0	L4DPIM0 Layer 4 Destination Port Inverse Match Enable When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM0 bit is set high. Values: 0x0 (DISABLE): Layer 4 Destination Port Inverse Match is disabled 0x1 (ENABLE): Layer 4 Destination Port Inverse Match is enabled
20	RW	0x0	L4DPM0 Layer 4 Destination Port Match Enable When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching. Values: 0x0 (DISABLE): Layer 4 Destination Port Match is disabled 0x1 (ENABLE): Layer 4 Destination Port Match is enabled
19	RW	0x0	L4SPIM0 Layer 4 Source Port Inverse Match Enable When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4SPM0 bit is set high. Values: 0x0 (DISABLE): Layer 4 Source Port Inverse Match is disabled 0x1 (ENABLE): Layer 4 Source Port Inverse Match is enabled

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Bit	Attr	Reset Value	Description
18	RW	0x0	L4SPM0 Layer 4 Source Port Match Enable When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching. Values: 0x0 (DISABLE): Layer 4 Source Port Match is disabled 0x1 (ENABLE): Layer 4 Source Port Match is enabled
17	RO	0x0	reserved
16	RW	0x0	L4PEN0 Layer 4 Protocol Enable When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching. The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set. Values: 0x0 (DISABLE): Layer 4 Protocol is disabled 0x1 (ENABLE): Layer 4 Protocol is enabled
15:11	RW	0x00	L3HDBM0 Layer 3 IP DA Higher Bits Match IPv4 Packets: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field: 0: No bits are masked. 1: LSb[0] is masked 2: Two LSbs [1:0] are masked .. 31: All bits except MSb are masked. IPv6 Packets: Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits: 0: No bits are masked. 1: LSb[0] is masked. 2: Two LSbs [1:0] are masked .. 127: All bits except MSb are masked. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set.

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Bit	Attr	Reset Value	Description
10:6	RW	0x00	L3HSBM0 Layer 3 IP SA Higher Bits Match IPv4 Packets: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field: 0: No bits are masked. 1: LSb[0] is masked 2: Two LSbs [1:0] are masked .. 31: All bits except MSb are masked. IPv6 Packets: This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high.
5	RW	0x0	L3DAIM0 Layer 3 IP DA Inverse Match Enable When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high. Values: 0x0 (DISABLE): Layer 3 IP DA Inverse Match is disabled 0x1 (ENABLE): Layer 3 IP DA Inverse Match is enabled
4	RW	0x0	L3DAM0 Layer 3 IP DA Match Enable When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering. Values: 0x0 (DISABLE): Layer 3 IP DA Match is disabled 0x1 (ENABLE): Layer 3 IP DA Match is enabled
3	RW	0x0	L3SAIM0 Layer 3 IP SA Inverse Match Enable When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when the L3SAM0 bit is set. Values: 0x0 (DISABLE): Layer 3 IP SA Inverse Match is disabled 0x1 (ENABLE): Layer 3 IP SA Inverse Match is enabled

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Bit	Attr	Reset Value	Description
2	RW	0x0	L3SAM0 Layer 3 IP SA Match Enable When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering. Values: 0x0 (DISABLE): Layer 3 IP SA Match is disabled 0x1 (ENABLE): Layer 3 IP SA Match is enabled
1	RO	0x0	reserved
0	RW	0x0	L3PEN0 Layer 3 Protocol Enable When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets. The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set. Values: 0x0 (DISABLE): Layer 3 Protocol is disabled 0x1 (ENABLE): Layer 3 Protocol is enabled

GMAC_MAC_LAYER4_ADDRESS0

Address: **Operational Base** + offset (0x0904)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	L4DP0 Layer 4 Destination Port Number Field When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets.
15:0	RW	0x0000	L4SP0 Layer 4 Source Port Number Field When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets.

GMAC_MAC_LAYER3_ADDR0_REG0

Address: **Operational Base** + offset (0x0910)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	L3A00 Layer 3 Address 0 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

GMAC_MAC_LAYER3_ADDR1_REG0

Address: **Operational Base** + offset (0x0914)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	L3A10 Layer 3 Address 1 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets.

GMAC_MAC_LAYER3_ADDR2_REG0

Address: **Operational Base** + offset (0x0918)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	L3A20 Layer 3 Address 2 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

GMAC_MAC_LAYER3_ADDR3_REG0

Address: **Operational Base** + offset (0x091C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	L3A30 Layer 3 Address 3 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

GMAC_MAC_TIMESTAMP_CONTROL

Address: **Operational Base** + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	AV8021ASMEN AV 802.1AS Mode Enable When this bit is set, the MAC processes only untagged PTP over Ethernet packets for providing PTP status and capturing timestamp snapshots, that is, IEEE 802.1AS mode of operation. When PTP offload feature is enabled, for the purpose of PTP offload, the transport specific field in the PTP header is generated and checked based on the value of this bit. Values: 1'b0: AV 802.1AS Mode is disabled 1'b1: AV 802.1AS Mode is enabled
27:25	RO	0x0	reserved
24	RW	0x0	TXTSSTSM Transmit Timestamp Status Mode When this bit is set, the MAC overwrites the earlier transmit timestamp status even if it is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. When this bit is reset, the MAC ignores the timestamp status of current packet if the timestamp status of previous packet is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. Values: 1'b0: Transmit Timestamp Status Mode is disabled 1'b1: Transmit Timestamp Status Mode is enabled
23:19	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
18	RW	0x0	TSENMACADDR Enable MAC Address for PTP Packet Filtering When this bit is set, the DA MAC address (that matches any MAC Address register) is used to filter the PTP packets when PTP is directly sent over Ethernet. When this bit is set, received PTP packets with DA containing a special multicast or unicast address that matches the one programmed in MAC address registers are considered for processing as indicated below, when PTP is directly sent over Ethernet. For normal time stamping operation, MAC address registers 0 to 31 is considered for unicast destination address matching. For PTP offload, only MAC address register 0 is considered for unicast destination address matching. Values: 1'b0: MAC Address for PTP Packet Filtering is disabled 1'b1: MAC Address for PTP Packet Filtering is enabled
17:16	RW	0x0	SNAPTYPSEL Select PTP packets for Taking Snapshots These bits, along with Bits 15 and 14, decide the set of PTP packet types for which snapshot needs to be taken. The encoding is given in Timestamp Snapshot Dependency on Register Bits Table.
15	RW	0x0	TSMSTRENA Enable Snapshot for Messages Relevant to Master When this bit is set, the snapshot is taken only for the messages that are relevant to the master node. Otherwise, the snapshot is taken for the messages relevant to the slave node. Values: 1'b0: Snapshot for Messages Relevant to Master is disabled 1'b1: Snapshot for Messages Relevant to Master is enabled
14	RW	0x0	TSEVNTENA Enable Timestamp Snapshot for Event Messages When this bit is set, the timestamp snapshot is taken only for event messages (SYNC, Delay_Req, Pdelay_Req, or Pdelay_Resp). When this bit is reset, the snapshot is taken for all messages except Announce, Management, and Signaling. For more information about the timestamp snapshots, see Timestamp Snapshot Dependency on Register Bits Table. Values: 1'b0: Timestamp Snapshot for Event Messages is disabled 1'b1: Timestamp Snapshot for Event Messages is enabled
13	RW	0x0	TSIPV4ENA Enable Processing of PTP Packets Sent over IPv4-UDP When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv4-UDP packets. When this bit is reset, the MAC ignores the PTP transported over IPv4-UDP packets. This bit is set by default. Values: 1'b0: Processing of PTP Packets Sent over IPv4-UDP is disabled 1'b1: Processing of PTP Packets Sent over IPv4-UDP is enabled

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Bit	Attr	Reset Value	Description
12	RW	0x0	TSIPV6ENA Enable Processing of PTP Packets Sent over IPv6-UDP When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv6-UDP packets. When this bit is clear, the MAC ignores the PTP transported over IPv6-UDP packets. Values: 1'b0: Processing of PTP Packets Sent over IPv6-UDP is disabled 1'b1: Processing of PTP Packets Sent over IPv6-UDP is enabled
11	RW	0x0	TSIPENA Enable Processing of PTP over Ethernet Packets When this bit is set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet packets. When this bit is reset, the MAC ignores the PTP over Ethernet packets. Values: 1'b0: Processing of PTP over Ethernet Packets is disabled 1'b1: Processing of PTP over Ethernet Packets is enabled
10	RW	0x0	TSVER2ENA Enable PTP Packet Processing for Version 2 Format When this bit is set, the IEEE 1588 version 2 format is used to process the PTP packets. When this bit is reset, the IEEE 1588 version 1 format is used to process the PTP packets. The IEEE 1588 formats are described in 'PTP Processing and Control'. Values: 1'b0: PTP Packet Processing for Version 2 Format is disabled 1'b1: PTP Packet Processing for Version 2 Format is enabled
9	RW	0x0	TSCTRLSSR Timestamp Digital or Binary Rollover Control When this bit is set, the Timestamp Low register rolls over after 0x3B9A_C9FF value (that is, 1 nanosecond accuracy) and increments the timestamp (High) seconds. When this bit is reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment must be programmed correctly depending on the PTP reference clock frequency and the value of this bit. Values: 1'b0: Timestamp Digital or Binary Rollover Control is disabled 1'b1: Timestamp Digital or Binary Rollover Control is enabled
8	RW	0x0	TSENALL Enable Timestamp for All Packets When this bit is set, the timestamp snapshot is enabled for all packets received by the MAC. Values: 1'b0: Timestamp for All Packets disabled 1'b1: Timestamp for All Packets enabled
7	RO	0x0	reserved
6	RW	0x0	PTGE Presentation Time Generation Enable When this bit is set the Presentation Time generation will be enabled. Values: 0x0 (DISABLE): Presentation Time Generation is disabled 0x1 (ENABLE): Presentation Time Generation is enabled

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Bit	Attr	Reset Value	Description
5	RW	0x0	TSADDREG Update Addend Register When this bit is set, the content of the Timestamp Addend register is updated in the PTP block for fine correction. This bit is cleared when the update is complete. This bit should be zero before it is set. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Addend Register is not updated 1'b1: Addend Register is updated
4	RO	0x0	reserved
3	RW	0x0	TSUPDT Update Timestamp When this bit is set, the system time is updated (added or subtracted) with the value specified in MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before updating it. This bit is reset when the update is complete in hardware. The Timestamp Higher Word register (if enabled during core configuration) is not updated.When Media Clock Generation and Recovery is configured (DWC_EQOS_FLEXI_PPS_OUT_EN) and enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Timestamp is not updated 1'b1: Timestamp is updated
2	RW	0x0	TSINIT Initalize Timestamp When this bit is set, the system time is initialized (overwritten) with the value specified in the MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before it is updated. This bit is reset when the initialization is complete. The Timestamp Higher Word register (if enabled during core configuration) can only be initialized.When Media Clock Generation and Recovery is configured (DWC_EQOS_FLEXI_PPS_OUT_EN) and enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Timestamp is not initialized 1'b1: Timestamp is initialized
1	RW	0x0	TSCFUPDT Fine or Coarse Timestamp Update When this bit is set, the Fine method is used to update system timestamp. When this bit is reset, Coarse method is used to update the system timestamp. Values: 1'b0: Coarse method is used to update system timestamp 1'b1: Fine method is used to update system timestamp

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Bit	Attr	Reset Value	Description
0	RW	0x0	TSENA Enable Timestamp When this bit is set, the timestamp is added for Transmit and Receive packets. When disabled, timestamp is not added for transmit and receive packets and the Timestamp Generator is also suspended. You need to initialize the Timestamp (system time) after enabling this mode.On the Receive side, the MAC processes the 1588 packets only if this bit is set. Values: 1'b0: Timestamp is disabled 1'b1: Timestamp is enabled

GMAC_MAC_SUB_SECOND_INCREMENT

Address: **Operational Base** + offset (0x0B04)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	SSINC Sub-second Increment Value The value programmed in this field is accumulated every clock cycle (of clk_ptp_i) with the contents of the sub-second register. For example, when the PTP clock is 50 MHz (period is 20 ns), you should program 20 (0x14) when the System Time Nanoseconds register has an accuracy of 1 ns [Bit 9 (TSCTRLSSR) is set in MAC_Timestamp_Control]. When TSCTRLSSR is clear, the Nanoseconds register has a resolution of ~0.465 ns. In this case, you should program a value of 43 (0x2B) which is derived by 20 ns/0.465.
15:0	RO	0x0000	reserved

GMAC_MAC_SYSTEM_TIME_SECS

Address: **Operational Base** + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSS Timestamp Second The value in this field indicates the current value in seconds of the System Time maintained by the MAC.

GMAC_MAC_SYSTEM_TIME_NS

Address: **Operational Base** + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RW	0x00000000	TSSS Timestamp Sub Seconds The value in this field has the sub-second representation of time, with an accuracy of 0.46 ns. When Bit 9 is set in MAC_Timestamp_Control, each bit represents 1 ns. The maximum value is 0x3B9A_C9FF after which it rolls-over to zero.

GMAC_MAC_SYS_TIME_SECS_UPDATE

Address: **Operational Base** + offset (0x0B10)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSS Timestamp Seconds The value in this field is the seconds part of the update. When ADDSUB is reset, this field must be programmed with the seconds part of the update value. When ADDSUB is set, this field must be programmed with the complement of the seconds part of the update value. For example, if 2.000000001 seconds need to be subtracted from the system time, the TSS field in the MAC_Timestamp_Seconds_Update register must be 0xFFFF_FFFE (that is, 2^32 - 2).

GMAC_MAC_SYS_TIME_NS_UPDATE

Address: **Operational Base** + offset (0x0B14)

Bit	Attr	Reset Value	Description
31	RW	0x0	ADDSUB Add or Subtract Time When this bit is set, the time value is subtracted with the contents of the update register. When this bit is reset, the time value is added with the contents of the update register. Values: 1'b0: Add time 1'b1: Subtract time
30:0	RW	0x00000000	TSSS Timestamp Sub Seconds The value in this field is the sub-seconds part of the update. When ADDSUB is reset, this field must be programmed with the sub-seconds part of the update value, with an accuracy based on the TSCTRLSSR bit of the MAC_Timestamp_Control register.When ADDSUB is set, this field must be programmed with the complement of the sub-seconds part of the update value as described below. When TSCTRLSSR bit in MAC_Timestamp_Control is set, the programmed value must be 10^9 - <sub-second value>. When TSCTRLSSR bit in MAC_Timestamp_Control is reset, the programmed value must be 2^31 - <sub-second_value>. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, each bit represents an accuracy of 0.46 ns. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, each bit represents 1 ns and the programmed value should not exceed 0x3B9A_C9FF. For example, if 2.000000001 seconds need to be subtracted from the system time, then the TSSS field in the MAC_Timestamp_Nanoseconds_Update register must be 0x7FFF_FFFF (that is, 2^31 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is reset and 0x3B9A_C9FF (that is, 10^9 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is set.

GMAC_MAC_TIMESTAMP_ADDEND

Address: **Operational Base** + offset (0x0B18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSAR Timestamp Addend Register This field indicates the 32-bit time value to be added to the Accumulator register to achieve time synchronization.

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GMAC_MAC_TIMESTAMP_STATUS

Address: **Operational Base** + offset (0x0B20)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	ATSNS Number of Auxiliary Timestamp Snapshots This field indicates the number of Snapshots available in the FIFO. A value equal to the selected depth of FIFO (4, 8, or 16) indicates that the Auxiliary Snapshot FIFO is full. These bits are cleared (to 00000) when the Auxiliary snapshot FIFO clear bit is set. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected.
24	RO	0x0	ATSSTM Auxiliary Timestamp Snapshot Trigger Missed This bit is set when the Auxiliary timestamp snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Values: 1'b0: Auxiliary Timestamp Snapshot Trigger Missed status not detected 1'b1: Auxiliary Timestamp Snapshot Trigger Missed status detected
23:16	RO	0x00	reserved
15	RO	0x0	TXTSSIS Tx Timestamp Status Interrupt Status In non-EQOS_CORE configurations when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the MAC_Tx_Timestamp_Status_Seconds register is read (or write to MAC_Tx_Timestamp_Status_Seconds register when RCWE bit of MAC_CSR_SW_Ctrl register is set). Values: 1'b0: Tx Timestamp Status Interrupt status not detected 1'b1: Tx Timestamp Status Interrupt status detected
14:4	RO	0x000	reserved
3	RO	0x0	TSTRGTERR0 Timestamp Target Time Error This bit is set when the latest target time programmed in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Timestamp Target Time Error status not detected 1'b1: Timestamp Target Time Error status detected

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Bit	Attr	Reset Value	Description
2	RO	0x0	AUXTSTRIG Auxiliary Timestamp Trigger Snapshot This bit is set high when the auxiliary snapshot is written to the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Auxiliary Timestamp Trigger Snapshot status not detected 1'b1: Auxiliary Timestamp Trigger Snapshot status detected
1	RO	0x0	TSTARGT0 Timestamp Target Time Reached When set, this bit indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Timestamp Target Time Reached status not detected 1'b1: Timestamp Target Time Reached status detected
0	RO	0x0	TSSOVF Timestamp Seconds Overflow When this bit is set, it indicates that the seconds value of the timestamp (when supporting version 2 format) has overflowed beyond 32'hFFFF_FFFF. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Timestamp Seconds Overflow status not detected 1'b1: Timestamp Seconds Overflow status detected

GMAC_MAC_TX_TS_STATUS_NS

Address: **Operational Base** + offset (0x0B30)

Bit	Attr	Reset Value	Description
31	RO	0x0	TXTSSMIS Transmit Timestamp Status Missed When this bit is set, it indicates one of the following: 1. The timestamp of the current packet is ignored if TXTSSTSM bit of the MAC_Timestamp_Control register is reset. 2. The timestamp of the previous packet is overwritten with timestamp of the current packet if TXTSSTSM bit of the MAC_Timestamp_Control register is set. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Transmit Timestamp Status Missed status not detected 1'b1: Transmit Timestamp Status Missed status detected
30:0	RO	0x00000000	TXTSSLO Transmit Timestamp Status Low This field contains the 31 bits of the Nanoseconds field of the Transmit packet's captured timestamp.

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GMAC_MAC_TX_TS_STATUS_SECS

Address: **Operational Base** + offset (0x0B34)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXTSSHI Transmit Timestamp Status High This field contains the lower 32 bits of the Seconds field of Transmit packet's captured timestamp.

GMAC_MAC_AUXILIARY_CONTROL

Address: **Operational Base** + offset (0x0B40)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ATSEN0 Auxiliary Snapshot 0 Enable This bit controls the capturing of Auxiliary Snapshot Trigger 0. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[0] input is enabled. When this bit is reset, the events on this input are ignored. Values: 0x0 (DISABLE): Auxiliary Snapshot 0 is disabled 0x1 (ENABLE): Auxiliary Snapshot 0 is enabled
3:1	RO	0x0	reserved
0	RW	0x0	ATSFC Auxiliary Snapshot FIFO Clear When set, this bit resets the pointers of the Auxiliary Snapshot FIFO. This bit is cleared when the pointers are reset and the FIFO is empty. When this bit is high, the auxiliary snapshots are stored in the FIFO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Auxiliary Snapshot FIFO Clear is disabled 1'b1: Auxiliary Snapshot FIFO Clear is enabled

GMAC_MAC_AUXILIARY_TS_NS

Address: **Operational Base** + offset (0x0B48)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RO	0x00000000	AUXTSLO Auxiliary Timestamp Contains the lower 31 bits (nanoseconds field) of the auxiliary timestamp.

GMAC_MAC_AUXILIARY_TS_SECS

Address: **Operational Base** + offset (0x0B4C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	AUXTSHI Auxiliary Timestamp Contains the lower 32 bits of the Seconds field of the auxiliary timestamp.

GMAC_MAC_TS_INGRESS_CORR_NS

Address: **Operational Base** + offset (0x0B58)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSIC Timestamp Ingress Correction This field contains the ingress path correction value as defined by the Ingress Correction expression.

GMAC_MAC_TS_EGRESS_CORR_NS

Address: **Operational Base** + offset (0x0B5C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSEC Timestamp Egress Correction This field contains the nanoseconds part of the egress path correction value as defined by the Egress Correction expression.

GMAC_MAC_TS_INGRESS_LATENCY

Address: **Operational Base** + offset (0x0B68)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	ITLNS Ingress Timestamp Latency, in sub-nanoseconds This register holds the average latency in sub-nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
15:8	RO	0x00	ITLSNS Ingress Timestamp Latency, in nanoseconds This register holds the average latency in nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
7:0	RO	0x00	reserved

GMAC_MAC_TS_EGRESS_LATENCY

Address: **Operational Base** + offset (0x0B6C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	ETLNS Egress Timestamp Latency, in nanoseconds This register holds the average latency in nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
15:8	RO	0x00	ETLSNS Egress Timestamp Latency, in sub-nanoseconds This register holds the average latency in sub-nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
7:0	RO	0x00	reserved

GMAC_MAC_PPS_CONTROL

Address: **Operational Base** + offset (0x0B70)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	MCGREN0 MCGR Mode Enable for PPS0 Output This field enables the 0th PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode. Values: 0x0 (PPS): 0th PPS instance is enabled to operate in PPS mode 0x1 (MCGR): 0th PPS instance is enabled to operate in MCGR mode
6:5	RW	0x0	TRGTMODSEL0 Target Time Register Mode for PPS0 Output This field indicates the Target Time registers (MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds) mode for PPS0 output signal: Values: 0x0 (ONLY_INT): Target Time registers are programmed only for generating the interrupt event. The Flexible PPS function must not be enabled in this mode, otherwise spurious transitions may be observed on the corresponding ptp_pps_o output port 0x1 (RSVD): Reserved 0x2 (INT_ST): Target Time registers are programmed for generating the interrupt event and starting or stopping the PPS0 output signal generation 0x3 (ONLY_ST): Target Time registers are programmed only for starting or stopping the PPS0 output signal generation. No interrupt is asserted
4	RW	0x0	PPSEN0 Flexible PPS Output Mode Enable When this bit is set, Bits[3:0] function as PPSCMD. When this bit is reset, Bits[3:0] function as PPSCTRL (Fixed PPS mode). Values: 0x0 (DISABLE): Flexible PPS Output Mode is disabled 0x1 (ENABLE): Flexible PPS Output Mode is enabled

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	PPSCTRL_PPSCMD PPS Output Frequency Control This field controls the frequency of the PPS0 output (ptp_pps_o[0]) signal. The default value of PPSCTRL is 0000, and the PPS output is 1 pulse (of width clk_ptp_i) every second. For other values of PPSCTRL, the PPS output becomes a generated clock of following frequencies: 4'b0001: The binary rollover is 2 Hz, and the digital rollover is 1 Hz. 4'b0010: The binary rollover is 4 Hz, and the digital rollover is 2 Hz. 4'b0011: The binary rollover is 8 Hz, and the digital rollover is 4 Hz. 4'b0100: The binary rollover is 16 Hz, and the digital rollover is 8 Hz. ... 4'b1111: The binary rollover is 32.768 KHz and the digital rollover is 16.384 KHz. Note: In the binary rollover mode, the PPS output (ptp_pps_o) has a duty cycle of 50 percent with these frequencies. In the digital rollover mode, the PPS output frequency is an average number. The actual clock is of different frequency that gets synchronized every second. For example: 1. When PPSCTRL = 0001, the PPS (1 Hz) has a low period of 537 ms and a high period of 463 ms. 2. When PPSCTRL = 0010, the PPS (2 Hz) is a sequence of One clock of 50 percent duty cycle and 537 ms period Second clock of 463 ms period (268 ms low and 195 ms high). 3. When PPSCTRL = 0011, the PPS (4 Hz) is a sequence of Three clocks of 50 percent duty cycle and 268 ms period Fourth clock of 195 ms period (134 ms low and 61 ms high). This behavior is because of the non-linear toggling of bits in the digital rollover mode in the MAC_System_Time_Nanoseconds register.

GMAC_MAC_PPS0_TARGET_TIME_SECONDS

Address: **Operational Base** + offset (0x0B80)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSTRH0 PPS Target Time Seconds Register This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register. If DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger.

GMAC_MAC_PPS0_TARGET_TIME_NS

Address: **Operational Base** + offset (0x0B84)

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Bit	Attr	Reset Value	Description
31	RW	0x0	TRGTBUSY0 PPS Target Time Register Busy The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain.The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed timegets corrupted. Values: 0x0 (INACTIVE): PPS Target Time Register Busy status is not detected 0x1 (ACTIVE): PPS Target Time Register Busy is detected
30:0	RW	0x00000000	TTSL0 Target Time Low for PPS Register This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output may have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output may have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

GMAC_MAC_PPS0_INTERVAL

Address: **Operational Base** + offset (0x0B88)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PPSINT0 PPS Output Signal Interval These bits store the interval between the rising edges of PPS0 signal output. The interval is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS0 signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register.

GMAC_MAC_PPS0_WIDTH

Address: **Operational Base** + offset (0x0B8C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PPSWIDTH0 PPS Output Signal Width These bits store the width between the rising edge and corresponding falling edge of PPS0 signal output. The width is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS0 signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register. Note: The value programmed in this register must be lesser than the value programmed in MAC_PPS0_Interval.

GMAC_MTL_OPERATION_MODE

Address: **Operational Base** + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	CNTCLR Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 0x0 (DISABLE): Counters are not reset 0x1 (ENABLE): All counters are reset
8	RW	0x0	CNTPRST Counters Preset When this bit is set, 1.MTL_TxQ[0-7]_Underflow register is initialized/preset to 12'h7F0. 2.Missed Packet and Overflow Packet counters in MTL_RxQ[0-7]_Missed_Packet_Overflow_Cnt register is initialized/preset to 12'h7F0. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 0x0 (DISABLE): Counters Preset is disabled 0x1 (ENABLE): Counters Preset is enabled
7	RO	0x0	reserved
6:5	RW	0x0	SCHALG Tx Scheduling Algorithm This field indicates the algorithm for Tx scheduling:Values: 0x0 (WRR): WRR algorithm 0x1 (WFQ): WFQ algorithm when DCB feature is selected. Otherwise, Reserved 0x2 (DWRR): DWRR algorithm when DCB feature is selected. Otherwise, Reserved 0x3 (SP): Strict priority algorithm
4:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	RAA Receive Arbitration Algorithm This field is used to select the arbitration algorithm for the Rx side. 0: Strict priority (SP) Queue 0 has the lowest priority and the last queue has the highest priority. 1: Weighted Strict Priority (WSP) Values: 0x0 (SP): Strict priority (SP) 0x1 (WSP): Weighted Strict Priority (WSP)
1	RW	0x0	DTXSTS Drop Transmit Status When this bit is set, the Tx packet status received from the MAC is dropped in the MTL. When this bit is reset, the Tx packet status received from the MAC is forwarded to the application. Values: 0x0 (DISABLE): Drop Transmit Status is disabled 0x1 (ENABLE): Drop Transmit Status is enabled
0	RO	0x0	reserved

GMAC_MTL_DBG_CTL

Address: **Operational Base** + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	STSIE Transmit Status Available Interrupt Status Enable When this bit is set, an interrupt is generated when Transmit status is available in slave mode. Values: 1'b0: Transmit Packet Available Interrupt Status is disabled 1'b1: Transmit Packet Available Interrupt Status is enabled
14	RW	0x0	PKTIE Receive Packet Available Interrupt Status Enable When this bit is set, an interrupt is generated when EOP of received packet is written to the Rx FIFO. Values: 1'b0: Receive Packet Available Interrupt Status is disabled 1'b1: Receive Packet Available Interrupt Status is enabled
13:12	RW	0x0	FIFOSEL FIFO Selected for Access This field indicates the FIFO selected for debug access: Values: 2'b00: Tx FIFO 2'b01: Tx Status FIFO (only read access when SLVMOD is set) 2'b10: TSO FIFO (cannot be accessed when SLVMOD is set) 2'b11: Rx FIFO

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Bit	Attr	Reset Value	Description
11	RW	0x0	FIFOWREN FIFO Write Enable When this bit is set, it enables the Write operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: FIFO Write is disabled 1'b1: FIFO Write is enabled
10	RW	0x0	FIFORDEN FIFO Read Enable When this bit is set, it enables the Read operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: FIFO Read is disabled 1'b1: FIFO Read is enabled
9	RW	0x0	RSTSEL Reset Pointers of Selected FIFO When this bit is set, the pointers of the currently-selected FIFO are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Reset Pointers of Selected FIFO is disabled 1'b1: Reset Pointers of Selected FIFO is enabled
8	RW	0x0	RSTALL Reset All Pointers When this bit is set, the pointers of all FIFOs are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Reset All Pointers is disabled 1'b1: Reset All Pointers is enabled
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:5	RW	0x0	PKTSTATE Encoded Packet State This field is used to write the control information to the Tx FIFO or Rx FIFO. Tx FIFO: 2'b00: Packet Data 2'b01: Control Word 2'b10: SOP Data 2'b11: EOP Data Rx FIFO: 2'b00: Packet Data 2'b01: Normal Status 2'b10: Last Status 2'b11: EOP Values: 2'b00: Packet Data 2'b01: Control Word/Normal Status 2'b10: SOP Data/Last Status 2'b11: EOP Data/EOP
4	RO	0x0	reserved
3:2	RW	0x0	BYTEEN Byte Enables This field indicates the number of data bytes valid in the data register during Write operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. Values: 2'b00: Byte 0 valid 2'b01: Byte 0 and Byte 1 are valid 2'b10: Byte 0, Byte 1, and Byte 2 are valid 2'b11: All four bytes are valid
1	RW	0x0	DBGMOD Debug Mode Access to FIFO When this bit is set, it indicates that the current access to the FIFO is read, write, and debug access. In this mode, the following access types are allowed: 1. Read and Write access to Tx FIFO, TSO FIFO, and Rx FIFO 2. Read access is allowed to Tx Status FIFO. When this bit is reset, it indicates that the current access to the FIFO is slave access bypassing the DMA. In this mode, the following access are allowed: 1. Write access to the Tx FIFO 2. Read access to the Rx FIFO and Tx Status FIFO Values: 1'b0: Debug Mode Access to FIFO is disabled 1'b1: Debug Mode Access to FIFO is enabled
0	RW	0x0	FDBGEN FIFO Debug Access Enable When this bit is set, it indicates that the debug mode access to the FIFO is enabled. When this bit is reset, it indicates that the FIFO can be accessed only through a master interface. Values: 1'b0: FIFO Debug Access is disabled 1'b1: FIFO Debug Access is enabled

GMAC_MTL_DBG_STS

Address: **Operational Base** + offset (0x0C0C)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x320	LOCR Remaining Locations in the FIFO Slave Access Mode: This field indicates the space available in selected FIFO. Debug Access Mode: This field contains the Write or Read pointer value of the selected FIFO during Write or Read operation, respectively. Reset: In single Tx Queue configurations, (DWC_EQOS_TXFIFO_SIZE/(DWC_EQOS_DATAWIDTH/8)), Otherwise 0000H.
14:10	RO	0x00	reserved
9	RW	0x0	STSI Transmit Status Available Interrupt Status When set, this bit indicates that the Slave mode Tx packet is transmitted, and the status is available in Tx Status FIFO. This bit is reset when 1 is written to this bit. Values: 1'b0: Transmit Status Available Interrupt Status not detected 1'b1: Transmit Status Available Interrupt Status detected
8	RW	0x0	PKTI Receive Packet Available Interrupt Status When set, this bit indicates that MAC layer has written the EOP of received packet to the Rx FIFO. This bit is reset when 1 is written to this bit. Values: 1'b0: Receive Packet Available Interrupt Status not detected 1'b1: Receive Packet Available Interrupt Status detected
7:5	RO	0x0	reserved
4:3	RO	0x0	BYTEEN Byte Enables This field indicates the number of data bytes valid in the data register during Read operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. Values: 2'b00: Byte 0 valid 2'b01: Byte 0 and Byte 1 are valid 2'b10: Byte 0, Byte 1, and Byte 2 are valid 2'b11: All four bytes are valid

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Bit	Attr	Reset Value	Description
2:1	RO	0x0	PKTSTATE Encoded Packet State This field is used to get the control or status information of the selected FIFO. Tx FIFO: 2'b00: Packet Data 2'b01: Control Word 2'b10: SOP Data 2'b11: EOP Data Rx FIFO: 2'b00: Packet Data 2'b01: Normal Status 2'b10: Last Status 2'b11: EOP This field is applicable only for Tx FIFO and Rx FIFO during Read operation. Values: 2'b00: Packet Data 2'b01: Control Word/Normal Status 2'b10: SOP Data/Last Status 2'b11: EOP Data/EOP
0	RO	0x0	FIFOBUSY FIFO Busy When set, this bit indicates that a FIFO operation is in progress in the MAC and content of the following fields is not valid: 1. All other fields of this register 2. All fields of the MTL_FIFO_Debug_Data register Values: 1'b0: FIFO Busy not detected 1'b1: FIFO Busy detected

GMAC_MTL_FIFO_DEBUG_DATA

Address: **Operational Base** + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FDBGDATA FIFO Debug Data During debug or slave access write operation, this field contains the data to be written to the Tx FIFO, Rx FIFO, or TSO FIFO. During debug or slave access read operation, this field contains the data read from the Tx FIFO, Rx FIFO, TSO FIFO, or Tx Status FIFO.

GMAC_MTL_INTERRUPT_STATUS

Address: **Operational Base** + offset (0x0C20)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RO	0x0	ESTIS EST (TAS- 802.1Qbv) Interrupt Status This bit indicates an interrupt event during the operation of 802.1Qbv. To reset this bit, the application must clear the error/event that has caused the Interrupt. Values: 0x0 (INACTIVE): EST (TAS- 802.1Qbv) Interrupt status not detected 0x1 (ACTIVE): EST (TAS- 802.1Qbv) Interrupt status detected

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Bit	Attr	Reset Value	Description
17	RO	0x0	DBGIS Debug Interrupt status This bit indicates an interrupt event during the slave access. To reset this bit, the application must read the FIFO Debug Access Status register to get the exact cause of the interrupt and clear its source. Values: 1'b0: Debug Interrupt status not detected 1'b1: Debug Interrupt status detected
16:2	RO	0x0000	reserved
1	RO	0x0	Q1IS Queue 1 Interrupt status This bit indicates that there is an interrupt from Queue 1. To reset this bit, the application must read the MTL_Q1_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. Values: 0x0 (INACTIVE): Queue 1 Interrupt status not detected 0x1 (ACTIVE): Queue 1 Interrupt status detected
0	RO	0x0	Q0IS Queue 0 Interrupt status This bit indicates that there is an interrupt from Queue 0. To reset this bit, the application must read Queue 0 Interrupt Control and Status register to get the exact cause of the interrupt and clear its source. Values: 1'b0: Queue 0 Interrupt status not detected 1'b1: Queue 0 Interrupt status detected

GMAC_MTL_RXQ_DMA_MAP0

Address: **Operational Base** + offset (0x0C30)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	Q1DDMACH Queue 1 Enabled for DA-based DMA Channel Selection When set, this bit indicates that the packets received in Queue 1 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 1 are routed to the DMA Channel programmed in the Q1MDMACH field (Bits[10:8]). Values: 0x0 (DISABLE): Queue 1 disabled for DA-based DMA Channel Selection 0x1 (ENABLE): Queue 1 enabled for DA-based DMA Channel Selection
11:9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	Q1MDMACH Queue 1 Mapped to DMA Channel This field controls the routing of the received packet in Queue 1 to the DMA channel: 000: DMA Channel 0 001: DMA Channel 1 010: DMA Channel 2 011: DMA Channel 3 100: DMA Channel 4 101: DMA Channel 5 110: DMA Channel 6 111: DMA Channel 7 This field is valid when the Q1DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values may be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
7:5	RO	0x0	reserved
4	RW	0x0	Q0DDMACH Queue 0 Enabled for DA-based DMA Channel Selection When set, this bit indicates that the packets received in Queue 0 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 0 are routed to the DMA Channel programmed in the Q0MDMACH field. Values: 0x0 (DISABLE): Queue 0 disabled for DA-based DMA Channel Selection 0x1 (ENABLE): Queue 0 enabled for DA-based DMA Channel Selection
3:1	RO	0x0	reserved
0	RW	0x0	Q0MDMACH Queue 0 Mapped to DMA Channel This field controls the routing of the packet received in Queue 0 to the DMA channel: 000: DMA Channel 0 001: DMA Channel 1 010: DMA Channel 2 011: DMA Channel 3 100: DMA Channel 4 101: DMA Channel 5 110: DMA Channel 6 111: DMA Channel 7 This field is valid when the Q0DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values may be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.

GMAC_MTL_TBS_CTRL

Address: **Operational Base** + offset (0x0C40)

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Bit	Attr	Reset Value	Description
31:8	RW	0x000000	LEOS Launch Expiry Offset The value in units of 256 nanoseconds that has to be added to the Launch time to compute the Launch Expiry time. Value valid only when LEOV is set. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	RO	0x0	reserved
6:4	RW	0x0	LEGOS Launch Expiry GSN Offset The number GSN slots that has to be added to the Launch GSN to compute the Launch Expiry time. Value valid only when LEOV is set.
3:2	RO	0x0	reserved
1	RW	0x0	LEOV Launch Expiry Offset Valid When set indicates the LEOS field is valid. When not set, indicates the Launch Expiry Offset is not valid and the MTL must not check for Launch expiry time. Values: 0x0 (INVALID): LEOS field is invalid 0x1 (VALID): LEOS field is valid
0	RW	0x0	ESTM EST offset Mode When this bit is set, the Launch Time value used in Time Based Scheduling is interpreted as an EST offset value and is added to the Base Time Register (BTR) of the current list. When reset, the Launch Time value is used as an absolute value that should be compared with the System time [39:8]. Values: 0x0 (DISABLE): EST offset Mode is disabled 0x1 (ENABLE): EST offset Mode is enabled

GMAC_MTL_EST_CONTROL

Address: **Operational Base** + offset (0x0C50)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	PTOV PTP Time Offset Value The value of PTP Clock period multiplied by 6 in nanoseconds. This value is needed to avoid transmission overruns at the beginning of the installation of a new GCL.
23	RO	0x0	reserved
22:11	RW	0x000	CTOV Current Time Offset Value Provides a 12 bit time offset value in nano second that is added to the current time to compensate for all the implementation pipeline delays such as the CDC sync delay, buffering delays, data path delays etc. This offset helps to ensure that the impact of gate controls is visible on the line exactly at the pre-determined schedule (or as close to the schedule as possible).

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	TILS Time Interval Left Shift Amount This field provides the left shift amount for the programmed Time Interval values used in the Gate Control Lists. 000: No left shift needed (equal to x1ns) 001: Left shift TI by 1 bit (equal to x2ns) 010: Left shift TI by 2 bits (equal to x4ns) ... 100: Left shift TI by 7 bits (equal to x128ns) Based on the configuration one or more bits of this field should be treated as Reserved/Read-Only.
7:6	RW	0x0	LCSE Loop Count to report Scheduling Error Programmable number of GCL list iterations before reporting an HLBS error defined in EST_Status register. Values: 0x0 (4_ITERNS): 4 iterations 0x1 (8_ITERNS): 8 iterations 0x2 (16_ITERNS): 16 iterations 0x3 (32_ITERNS): 32 iterations
5	RW	0x0	DFBS Drop Frames causing Scheduling Error When set frames reported to cause HOL Blocking due to not getting scheduled (HLBS field of EST_Status register) after 4,8,16,32 (based on LCSE field of this register) GCL iterations are dropped. Values: 0x0 (DONT_DROP): Do not Drop Frames causing Scheduling Error 0x1 (DROP): Drop Frames causing Scheduling Error
4	RW	0x0	DDBF Do not Drop frames during Frame Size Error When set, frames are not be dropped during Head-of-Line blocking due to Frame Size Error (HLBF field of EST_Status register). Values: 0x0 (DROP): Drop frames during Frame Size Error 0x1 (DONT_DROP): Do not Drop frames during Frame Size Error
3:2	RO	0x0	reserved
1	RW	0x0	SSWL Switch to S/W owned list When set indicates that the software has programmed that list that it currently owns (SWOL) and the hardware should switch to the new list based on the new BTR. Hardware clears this bit when the switch to the SWOL happens to indicate the completion of the switch or when an BTR error (BTRE in Status register) is set. When BTRE is set this bit is cleared but SWOL is not updated as the switch was not successful. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 0x0 (DISABLE): Switch to S/W owned list is disabled 0x1 (ENABLE): Switch to S/W owned list is enabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	EEST Enable EST When reset, the gate control list processing is halted and all gates are assumed to be in Open state. Should be set for the hardware to start processing the gate control lists. During the toggle from 0 to 1, the gate control list processing starts only after the SSWL bit it set. When DWC_EQOS_ASP_ECC is selected during the configuration, if any uncorrectable error is detected in the EST memory the hardware will reset this bit and disable the EST function. Values: 0x0 (DISABLE): EST is disabled 0x1 (ENABLE): EST is enabled

GMAC_MTL_EST_STATUS

Address: **Operational Base** + offset (0x0C58)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RO	0x0	CGSN Current GCL Slot Number Indicates the slot number of the GCL list. Slot number is a modulo 16 count of the GCL List loops executed so far. Even if a new GCL list is installed, the count is incremental.
15:12	RO	0x0	reserved
11:8	RO	0x0	BTRL BTR Error Loop Count Provides the minimum count (N) for which the equation Current Time =< New BTR + (N * New Cycle Time) becomes true. N = "1111" indicates the iterations exceeded the value of 8 and the hardware was not able to update New BTR to be equal to or greater than Current Time. Software intervention is needed to update the New BTR. Value cleared when BTRE field of this register is cleared.
7	RO	0x0	SWOL S/W owned list When '0' indicates Gate control list number "0" is owned by software and when "1" indicates the Gate Control list "1" is owned by the software. Any reads/writes by the software (using indirect access via GCL_Control) is directed to the list indicated by this value by default. The inverse of this value is treated as HWOL. R/W operations performed by hardware are directed to the list pointed by HWOL by default. Values: 0x0 (INACTIVE): Gate control list number "0" is owned by software 0x1 (ACTIVE): Gate control list number "1" is owned by software
6:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	CGCE Constant Gate Control Error This error occurs when the list length (LLR) is 1 and the programmed Time Interval (TI) value after the optional Left Shifting is less than or equal to the Cycle Time (CTR). The above programming implies Gates are either always Closed or always Open based on the Gate Control values; the same effect can be achieved by other simpler (non TSN) programming mechanisms. Since the implementation does not support such a programming an error is reported. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 0x0 (INACTIVE): Constant Gate Control Error not detected 0x1 (ACTIVE): Constant Gate Control Error detected
3	RO	0x0	HLBS Head-Of-Line Blocking due to Scheduling Set when the frame is not able to win arbitration and get scheduled even after 4 iterations of the GCL. Indicates to software a potential programming error. The one hot encoded values of the Queue Numbers that are not able to make progress are indicated in the MTL_EST_Sch_Error register. Bit cleared when MTL_EST_Sch_Error register is all zeros. Values: 0x0 (INACTIVE): Head-Of-Line Blocking due to Scheduling not detected 0x1 (ACTIVE): Head-Of-Line Blocking due to Scheduling detected
2	RO	0x0	HLBF Head-Of-Line Blocking due to Frame Size Set when HOL Blocking is noticed on one or more Queues as a result of none of the Time Intervals of gate open in the GCL being greater than or equal to the duration needed for frame size (or frame fragment size when preemption is enabled) transmission. The one hot encoded Queue numbers that are experiencing HLBF are indicated in the MTL_EST_Frm_Size_Error register. Additionally, the first Queue number that experienced HLBF along with the frame size is captured in MTL_EST_Frm_Size_Capture register. Bit cleared when MTL_EST_Frame_Size_ Error register is all zeros. Values: 0x0 (INACTIVE): Head-Of-Line Blocking due to Frame Size not detected 0x1 (ACTIVE): Head-Of-Line Blocking due to Frame Size detected

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Bit	Attr	Reset Value	Description
1	RW	0x0	BTRE BTR Error When "1" indicates a programming error in the BTR of SWOL where the programmed value is less than current time. If the BTRL = "1111", SWOL is not updated and Software should reprogram the BTR to a value greater than current time and then set SSWL to reinitiate the switch to SWOL. Else if the value of BTRL < "1111", SWOL is updated and this field indicates the number of iterations (of + CycleTime) taken by hardware to update the BTR to a value greater than Current Time. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 0x0 (INACTIVE): BTR Error not detected 0x1 (ACTIVE): BTR Error detected
0	RW	0x0	SWLC Switch to S/W owned list Complete When "1" indicates the hardware has successfully switched to the SWOL, and the SWOL bit has been updated to that effect. Cleared when the SSWL of EST_Control register transitions from 0 to 1, or on a software write. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 0x0 (INACTIVE): Switch to S/W owned list Complete not detected 0x1 (ACTIVE): Switch to S/W owned list Complete detected

GMAC_MTL_EST_SCH_ERROR

Address: **Operational Base** + offset (0x0C60)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	SEQN Schedule Error Queue Number The One Hot Encoded Queue Numbers that have experienced error/timeout described in HLBS field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

GMAC_MTL_EST_FRM_SIZE_ERROR

Address: **Operational Base** + offset (0x0C64)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	FEQN Frame Size Error Queue Number The One Hot Encoded Queue Numbers that have experienced error described in HLBF field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

GMAC_MTL_EST_FRM_SIZE_CAPTURE

Address: **Operational Base** + offset (0x0C68)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
16	RO	0x0	HBFQ Queue Number of HLBF Captures the binary value of the of the first Queue (number) experiencing HLBF error (see HLBF field of status register). Value once written is not altered by any subsequent queue errors of similar nature. Once cleared the queue number of the next occurring HLBF error is captured. Width is based on the number of Tx Queues configured; remaining bits are Read-Only. Cleared when MTL_EST_Frm_Size_Error register is all zeros.
15	RO	0x0	reserved
14:0	RO	0x0000	HBFS Frame Size of HLBF Captures the Frame Size of the dropped frame related to queue number indicated in HBFQ field of this register. Contents of this register should be considered invalid, if this field is zero. Cleared when MTL_EST_Frm_Size_Error register is all zeros.

GMAC_MTL_EST_INTR_ENABLE

Address: **Operational Base** + offset (0x0C70)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	CGCE Interrupt Enable for CGCE When set, generates interrupt when the Constant Gate Control Error occurs and is indicated in the status. When reset this event does not generate an interrupt. Values: 0x0 (DISABLE): Interrupt for CGCE is disabled 0x1 (ENABLE): Interrupt for CGCE is enabled
3	RW	0x0	IEHS Interrupt Enable for HLBS When set, generates interrupt when the Head-of-Line Blocking due to Scheduling issue and is indicated in the status. When reset this event does not generate an interrupt. Values: 0x0 (DISABLE): Interrupt for HLBS is disabled 0x1 (ENABLE): Interrupt for HLBS is enabled
2	RW	0x0	IEHF Interrupt Enable for HLBF When set, generates interrupt when the Head-of-Line Blocking due to Frame Size error occurs and is indicated in the status. When reset this event does not generate an interrupt. Values: 0x0 (DISABLE): Interrupt for HLBF is disabled 0x1 (ENABLE): Interrupt for HLBF is enabled
1	RW	0x0	IEBE Interrupt Enable for BTR Error When set, generates interrupt when the BTR Error occurs and is indicated in the status. When reset this event does not generate an interrupt. Values: 0x0 (DISABLE): Interrupt for BTR Error is disabled 0x1 (ENABLE): Interrupt for BTR Error is enabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	IECC Interrupt Enable for Switch List When set, generates interrupt when the configuration change is successful and the hardware has switched to the new list. When reset this event does not generate an interrupt. Values: 0x0 (DISABLE): Interrupt for Switch List is disabled 0x1 (ENABLE): Interrupt for Switch List is enabled

GMAC_MTL_EST_GCL_CONTROL

Address: **Operational Base** + offset (0x0C80)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	ESTEIEC ECC Inject Error Control for EST Memory When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. This filed will be valid only if DWC_EQOS_ASP_ECC feature is selected during the configuration, else it will be reserved. Values: 0x0 (1BIT): Insert 1 bit error 0x1 (2BIT): Insert 2 bit errors 0x2 (3BIT): Insert 3 bit errors 0x3 (1BIT_ADDR): Insert 1 bit error in address field
21	RO	0x0	ESTEIEE EST ECC Inject Error Enable When set along with EEST bit of MTL_EST_Control register, enables the ECC error injection feature. When reset, disables the ECC error injection feature. Values: 0x0 (DISABLE): EST ECC Inject Error is disabled 0x1 (ENABLE): EST ECC Inject Error is enabled
20	RW	0x0	ERR0 When set indicates the last write operation was aborted as software writes to GCL and GCL registers is prohibited when SSWL bit of MTL_EST_Control Register is set. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 0x0 (DISABLE): ERR0 is disabled 0x1 (ENABLE): ERR1 is enabled
19:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	ADDR Gate Control List Address: (GCLA when GCRR is "0"). Provides the address (row number) of the Gate Control List at which the R/W operation has to be performed. By default the Gate Control List pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. The width of this field is dependent on DWC_EQOS_EST_DEP; unused bits should be treated as read only. Gate Control list Related Registers Address: (GCRA when GCRR is "1"). By default the GCL related register set pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. Lower 3 bits are only used in this mode, higher order bits are treated as dont cares. 000: BTR Low (31:0) 001: BTR High (63:31) 010: CTR Low (31:0) 011: CTR High (39:32) 100: TER (31:0) 101: LLR (n:0) (where n is (log{DWC_EQOS_EST_DEP} / log2)) Others: Reserved
7:6	RO	0x0	reserved
5	RW	0x0	DBGB Debug Mode Bank Select When set to "0" indicates R/W in debug mode should be directed to Bank 0 (GCL0 and corresponding Time related registers). When set to "1" indicates R/W in debug mode should be directed to Bank 1 (GCL1 and corresponding Time related registers). This value is used when DBGM is set and overrides by value of SWOL which is normally used. Values: 0x0 (BANK0): R/W in debug mode should be directed to Bank 0 0x1 (BANK1): R/W in debug mode should be directed to Bank 1
4	RW	0x0	DBGM Debug Mode When set to "1" indicates R/W in debug mode where the memory bank (for GCL and Time related registers) is explicitly provided by DBGB value, when set to "0" SWOL bit is used to determine which bank to use. Values: 0x0 (DISABLE): Debug Mode is disabled 0x1 (ENABLE): Debug Mode is enabled
3	RO	0x0	reserved
2	RW	0x0	GCRR Gate Control Related Registers When set to "1" indicates the R/W access is for the GCL related registers (BTR, CTR, TER, LLR) whose address is provided by GCRA. When "0" indicates R/W should be directed to GCL from the address provided by GCLA. Values: 0x0 (DISABLE): Gate Control Related Registers are disabled 0x1 (ENABLE): Gate Control Related Registers are enabled

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Bit	Attr	Reset Value	Description
1	RW	0x0	R1W0 Read '1', Write '0': When set to '1': Read Operation When set to '0': Write Operation. Values: 0x0 (WRITE): Write Operation 0x1 (READ): Read Operation
0	RW	0x0	SRWO Start Read/Write Op When set indicates a Read/Write Op has started and is in progress. When reset by hardware indicates the R/W Op has completed or an error has occurred (when bit 20 is set) Reads: Data can be read from MTL_EST_GCL_Data register after this bit is reset. Writes: MTL_EST_GCL_Data should be programmed with write data before setting SRWO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 0x0 (DISABLE): Start Read/Write Op disabled 0x1 (ENABLE): Start Read/Write Op enabled

GMAC_MTL_EST_GCL_DATA

Address: **Operational Base** + offset (0x0C84)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	GCD Gate Control Data The data corresponding to the address selected in the GCL_Control register. Used for both Read and Write operations.

GMAC_MTL_FPE_CTRL_STS

Address: **Operational Base** + offset (0x0C90)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	HRS Hold/Release Status 1: Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State. 0: Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State. Values: 0x0 (SET_REL): Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State 0x1 (SET_HOLD): Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State
27:10	RO	0x00000	reserved
9:8	RW	0x0	PEC Preemption Classification When set indicates the corresponding Queue must be classified as preemptable, when '0' Queue is classified as express. When both EST (Qbv) and Preemption are enabled, Queue-0 is always assumed to be preemptable. When EST (Qbv) is enabled Queues categorized as preemptable here are always assumed to be in "Open" state in the Gate Control List.
7:2	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	AFSZ Additional Fragment Size used to indicate, in units of 64 bytes, the minimum number of bytes over 64 bytes required in non-final fragments of preempted frames. The minimum non-final fragment size is (AFSZ +1) * 64 byte.

GMAC_MTL_FPE_ADVANCE

Address: **Operational Base** + offset (0x0C94)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	RADV Release Advance The maximum time in nanoseconds that can elapse between issuing a RELEASE to the MAC and the MAC being ready to resume transmission of preemptable frames, in the absence of there being any express frames available for transmission.
15:0	RW	0x0000	HADV Hold Advance The maximum time in nanoseconds that can elapse between issuing a HOLD to the MAC and the MAC ceasing to transmit any preemptable frame that is in the process of transmission or any preemptable frames that are queued for transmission.

GMAC_MTL_TXQ0_OPERATION_MODE

Address: **Operational Base** + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x06	TQS Transmit Queue Size This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	RO	0x000	reserved
6:4	RW	0x0	TTC Transmit Threshold Control These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset. Values: 3'b000: 32 bytes 3'b001: 64 bytes 3'b010: 96 bytes 3'b011: 128 bytes 3'b100: 192 bytes 3'b101: 256 bytes 3'b110: 384 bytes 3'b111: 512 bytes

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	TXQEN Transmit Queue Enable This field is used to enable/disable the transmit queue 0. 2'b00: Not enabled 2'b01: Reserved 2'b10: Enabled 2'b11: Reserved This field is Read Only in Single Queue configurations and Read Write in Multiple Queue configurations. Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. Values: 0x0 (DISABLE): Not enabled 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV) 0x2 (ENABLE): Enabled 0x3 (RSVD2): Reserved
1	RW	0x0	TSF Transmit Store and Forward When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. Values: 1'b0: Transmit Store and Forward is disabled 1'b1: Transmit Store and Forward is enabled
0	RW	0x0	FTQ Flush Transmit Queue When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Flush Transmit Queue is disabled 1'b1: Flush Transmit Queue is enabled

GMAC_MTL_TXQ0_UNDERFLOW

Address: **Operational Base** + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11	RO	0x0	UFCNTOVF Overflow Bit for Underflow Packet Counter This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Overflow not detected for Underflow Packet Counter 1'b1: Overflow detected for Underflow Packet Counter
10:0	RO	0x000	UFFRMCNT Underflow Packet Counter This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_MTL_TXQ0_DEBUG

Address: **Operational Base** + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RO	0x0	STXSTSF Number of Status Words in Tx Status FIFO of Queue This field indicates the current number of status in the Tx Status FIFO of this queue.When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	RO	0x0	reserved
18:16	RO	0x0	PTXQ Number of Packets in the Transmit Queue This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	RO	0x000	reserved
5	RO	0x0	TXSTSFSTS MTL Tx Status FIFO Full Status When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. Values: 1'b0: MTL Tx Status FIFO Full status is not detected 1'b1: MTL Tx Status FIFO Full status is detected
4	RO	0x0	TXQSTS MTL Tx Queue Not Empty Status When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. Values: 1'b0: MTL Tx Queue Not Empty status is not detected 1'b1: MTL Tx Queue Not Empty status is detected

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Bit	Attr	Reset Value	Description
3	RO	0x0	TWCSTS MTL Tx Queue Write Controller Status When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. Values: 1'b0: MTL Tx Queue Write Controller status is not detected 1'b1: MTL Tx Queue Write Controller status is detected
2:1	RO	0x0	TRCSTS MTL Tx Queue Read Controller Status This field indicates the state of the Tx Queue Read Controller: Values: 2'b00: Idle state 2'b01: Read state (transferring data to the MAC transmitter) 2'b10: Waiting for pending Tx Status from the MAC transmitter 2'b11: Flushing the Tx queue because of the Packet Abort request from the MAC
0	RO	0x0	TXQPAUSED Transmit Queue in Pause When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: 1. Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled 2. Reception of 802.3x Pause packet when PFC is disabled Values: 1'b0: Transmit Queue in Pause status is not detected 1'b1: Transmit Queue in Pause status is detected

GMAC_MTL_TXQ0_ETS_STATUS

Address: **Operational Base** + offset (0x0D14)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	ABS Average Bits per Slot This field contains the average transmitted bits per slot. When the DCB operation is enabled for Queue 0, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

GMAC_MTL_TXQ0_QUANTUM_WEIGHT

Address: **Operational Base** + offset (0x0D18)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x000000	ISCQW Quantum or Weights When the DCB operation is enabled with DWRR algorithm for Queue 0 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. When DCB operation is enabled with WFQ algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. The higher the programmed weights lesser the bandwidth allocated for the

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Bit	Attr	Reset Value	Description
			particular Transmit Queue. This is because the weights are used to compute the packet finish time (weights*packet_size). Lesser the finish time, higher the probability of the packet getting scheduled first and using more bandwidth. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x64.Bits [20:7] must be written to zero.

GMAC_MTL_Q0_INTERRUPT_CTRL_STATUS

Address: **Operational Base** + offset (0x0D2C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	RXOIE Receive Queue Overflow Interrupt Enable When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. Values: 1'b0: Receive Queue Overflow Interrupt is disabled 1'b1: Receive Queue Overflow Interrupt is enabled
23:17	RO	0x00	reserved
16	RW	0x0	RXOVFIS Receive Queue Overflow Interrupt Status This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 1'b0: Receive Queue Overflow Interrupt Status not detected 1'b1: Receive Queue Overflow Interrupt Status detected
15:10	RO	0x00	reserved
9	RW	0x0	ABPSIE Average Bits Per Slot Interrupt Enable When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. Values: 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled
8	RW	0x0	TXUIE Transmit Queue Underflow Interrupt Enable When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. Values: 1'b0: Transmit Queue Underflow Interrupt Status is disabled 1'b1: Transmit Queue Underflow Interrupt Status is enabled
7:2	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	ABPSIS Average Bits Per Slot Interrupt Status When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected
0	RW	0x0	TXUNFIS Transmit Queue Underflow Interrupt Status This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 1'b0: Transmit Queue Underflow Interrupt Status not detected 1'b1: Transmit Queue Underflow Interrupt Status detected

GMAC_MTL_RXQ0_OPERATION_MODE

Address: **Operational Base** + offset (0x0D30)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:20	RW	0x00	RQS Receive Queue Size This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits

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Bit	Attr	Reset Value	Description
19:14	RW	0x00	RFD Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: 0: Full minus 1 KB, that is, FULL 1 KB 1: Full minus 1.5 KB, that is, FULL 1.5 KB 2: Full minus 2 KB, that is, FULL 2 KB 3: Full minus 2.5 KB, that is, FULL 2.5 KB ... 62: Full minus 32 KB, that is, FULL 32 KB 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	RW	0x00	RFA Threshold for Activating Flow Control (in half-duplex and full-duplex) These bits control the threshold (fill-level of Rx queue) at which the flow control is activated:For more information on encoding for this field, see RFD.
7	RW	0x0	EHFC Enable Hardware Flow Control When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. Values: 1'b0: Hardware Flow Control is disabled 1'b1: Hardware Flow Control is enabled
6	RW	0x0	DIS_TCP_EF Disable Dropping of TCP/IP Checksum Error Packets When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. Values: 1'b0: Dropping of TCP/IP Checksum Error Packets is enabled 1'b1: Dropping of TCP/IP Checksum Error Packets is disabled

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Bit	Attr	Reset Value	Description
5	RW	0x0	RSF Receive Queue Store and Forward When this bit is set, the DWC_ether_qos reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. Values: 1'b0: Receive Queue Store and Forward is disabled 1'b1: Receive Queue Store and Forward is enabled
4	RW	0x0	FEP Forward Error Packets When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet may be forwarded to the application or DMA. Values: 1'b0: Forward Error Packets is disabled 1'b1: Forward Error Packets is enabled
3	RW	0x0	FUP Forward Undersized Good Packets When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. Values: 1'b0: Forward Undersized Good Packets is disabled 1'b1: Forward Undersized Good Packets is enabled
2	RO	0x0	reserved
1:0	RW	0x0	RTC Receive Queue Threshold Control These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1.

GMAC_MTL_RXQ0_MISS_PKT_OVF_CNT

Address: **Operational Base** + offset (0x0D34)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27	RO	0x0	MISCNTOVF Missed Packet Counter Overflow Bit When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Missed Packet Counter overflow not detected 1'b1: Missed Packet Counter overflow detected
26:16	RO	0x000	MISPKTCNT Missed Packet Counter This field indicates the number of packets missed by the DWC_ether_qos because the application asserted ari_pkt_flush_i[] for this queue. This counter is incremented each time the application issues ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. In EQOS-DMA, EQOS-AXI, and EQOS-AHB configurations, This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	RO	0x0	reserved
11	RO	0x0	OVFCNTOVF Overflow Counter Overflow Bit When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Overflow Counter overflow not detected 1'b1: Overflow Counter overflow detected
10:0	RO	0x000	OVFPKTCNT Overflow Packet Counter This field indicates the number of packets discarded by the DWC_ether_qos because of Receive queue overflow. This counter is incremented each time the DWC_ether_qos discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_MTL_RXQ0_DEBUG

Address: **Operational Base** + offset (0x0D38)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RO	0x0	PRXQ Number of Packets in Receive Queue This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size.
15:6	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
5:4	RO	0x0	RXQSTS MTL Rx Queue Fill-Level Status This field gives the status of the fill-level of the Rx Queue: Values: 2'b00: Rx Queue empty 2'b01: Rx Queue fill-level below flow-control deactivate threshold 2'b10: Rx Queue fill-level above flow-control activate threshold 2'b11: Rx Queue full
3	RO	0x0	reserved
2:1	RO	0x0	RRCSTS MTL Rx Queue Read Controller State This field gives the state of the Rx queue Read controller: Values: 2'b00: Idle state 2'b01: Reading packet data 2'b10: Reading packet status (or timestamp) 2'b11: Flushing the packet data and status
0	RO	0x0	RWCSTS MTL Rx Queue Write Controller Active Status When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. Values: 1'b0: MTL Rx Queue Write Controller Active Status not detected 1'b1: MTL Rx Queue Write Controller Active Status detected

GMAC_MTL_RXQ0_CONTROL

Address: **Operational Base** + offset (0x0D3C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	RXQ_FRM_ARBIT Receive Queue Packet Arbitration When this bit is set, the DWC_ether_qos drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the DWC_ether_qos drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: 1.PBL amount of data (indicated by ari_qN_pbl_i[]) 2.Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the DWC_ether_qos drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). Values: 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled
2:0	RW	0x0	RXQ_WEGT Receive Queue Weight This field indicates the weight assigned to the Rx Queue 0. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle.

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GMAC_DMA_MODE

Address: **Operational Base** + offset (0x1000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	INTM Interrupt Mode This field defines the interrupt mode of DWC_ether_qos. The behavior of the following outputs changes depending on the following settings: 1. sbd_perch_tx_intr_o[] (Transmit Per Channel Interrupt) 2. sbd_perch_rx_intr_o[] (Receive Per Channel Interrupt) 3. sbd_intr_o (Common Interrupt) It also changes the behavior of the RI/TI bits in the DMA_CH0_Status. 2'b00: sbd_perch_* are pulse signals for each TX/RX packet transfer completion events (irrespective of whether corresponding interrupts are enabled) for which IOC bits are enabled in descriptor. sbd_intr_o is also asserted when corresponding interrupts are enabled and cleared only when software clears the corresponding RI/TI status bits. 2'b01: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. 2'b10: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. However, the signal is asserted again if the same event occurred again before it was cleared. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. 2'b11: Reserved Values: 2'b00: See above description 2'b01: See above description 2'b10: See above description 2'b11: Reserved
15:9	RO	0x00	reserved
8	RW	0x0	DSPW Descriptor Posted Write When this bit is set to 0, the descriptor writes are always non-posted. When this bit is set to 1, the descriptor writes are non-posted only when IOC (Interrupt on completion) is set in last descriptor, otherwise the descriptor writes are always posted. Values: 1'b0: Descriptor Posted Write is disabled 1'b1: Descriptor Posted Write is enabled
7:1	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	SWR Software Reset When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all DWC_ether_qos clock domains. Before reprogramming any DWC_ether_qos register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1. Note: The reset operation is complete only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Software Reset is disabled 1'b1: Software Reset is enabled

GMAC_DMA_SYSBUS_MODE

Address: **Operational Base** + offset (0x1004)

Bit	Attr	Reset Value	Description
31	RW	0x0	EN_LPI Enable Low Power Interface (LPI) When set to 1, this bit enables the LPI mode supported by the EQOS-AXI configuration and accepts the LPI request from the AXI System Clock controller. When set to 0, this bit disables the LPI mode and always denies the LPI request from the AXI System Clock controller. Values: 1'b0: Low Power Interface (LPI) is disabled 1'b1: Low Power Interface (LPI) is enabled
30	RW	0x0	LPI_XIT_PKT Unlock on Magic Packet or Remote Wake-Up Packet When set to 1, this bit enables the AXI master to come out of the LPI mode only when the magic packet or remote wake-up packet is received. When set to 0, this bit enables the AXI master to come out of the LPI mode when any packet is received. Values: 1'b0: Unlock on Magic Packet or Remote Wake-Up Packet is disabled 1'b1: Unlock on Magic Packet or Remote Wake-Up Packet is enabled
29:26	RO	0x0	reserved
25:24	RW	0x0	WR_OSR_LMT AXI Maximum Write Outstanding Request Limit This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT + 1 Note: 1. Bit 26 is reserved if DWC_ETHER_QOS_AXI_MAX-_WR_REQ = 4 2. Bit 27 is reserved if DWC_ETHER_QOS_AXI_MAX-_WR_REQ!= 16

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Bit	Attr	Reset Value	Description
23:19	RO	0x00	reserved
18:16	RW	0x1	RD_OSR_LMT AXI Maximum Read Outstanding Request Limit This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT + 1 Note: 1. Bit 18 is reserved if parameter DWC_ETHER_QOS_AXI_-MAX_RD_REQ = 4 2. Bit 19 is reserved if parameter DWC_ETHER_QOS_AXI_-MAX_RD_REQ!= 16
15:13	RO	0x0	reserved
12	RW	0x0	AAL Address-Aligned Beats When this bit is set to 1, the EQOS-AXI or EQOS-AHB master performs address-aligned burst transfers on Read and Write channels. Values: 1'b0: Address-Aligned Beats is disabled 1'b1: Address-Aligned Beats is enabled
11	RW	0x0	EAME Enhanced Address Mode Enable When this bit is set to 1, the DMA master enables the enhanced address mode (40-bit or 48-bit addressing mode). In this mode, the DMA engine uses either the 40-bit or 48-bit address, depending on the configuration. Values: 1'b0: Enhanced Address Mode is disabled 1'b1: Enhanced Address Mode is enabled
10	RW	0x0	AALE Automatic AXI LPI enable When set to 1, enables the AXI master to enter into LPI state when there is no activity in the DWC_ether_qos for number of system clock cycles programmed in the LPIEI field of AXI_LPI_Entry_Interval register. Values: 1'b0: Automatic AXI LPI is disabled 1'b1: Automatic AXI LPI is enabled
9:4	RO	0x00	reserved
3	RW	0x0	BLEN16 AXI Burst Length 16 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 16 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. Values: 1'b0: No effect 1'b1: AXI Burst Length 16
2	RW	0x0	BLEN8 AXI Burst Length 8 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 8 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. Values: 1'b0: No effect 1'b1: AXI Burst Length 8

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Bit	Attr	Reset Value	Description
1	RW	0x0	BLEN4 AXI Burst Length 4 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 4 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. Values: 1'b0: No effect 1'b1: AXI Burst Length 4
0	RW	0x0	FB Fixed Burst Length When this bit is set to 1, the EQOS-AXI master initiates burst transfers of specified lengths as given below. 1. Burst transfers of fixed burst lengths as indicated by the BLEN256, BLEN128, BLEN64, BLEN32, BLEN16, BLEN8, or BLEN4 field 2. Burst transfers of length 1 When this bit is set to 0, the EQOS-AXI master initiates burst transfers that are equal to or less than the maximum allowed burst length programmed in Bits[7:1]. Values: 1'b0: Fixed Burst Length is disabled 1'b1: Fixed Burst Length is enabled

GMAC_DMA_INTERRUPT_STATUS

Address: **Operational Base** + offset (0x1008)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	MACIS MAC Interrupt Status This bit indicates an interrupt event in the MAC. To reset this bit to 1'b0, the software must read the corresponding register in the MAC to get the exact cause of the interrupt and clear its source. Values: 1'b0: MAC Interrupt Status not detected 1'b1: MAC Interrupt Status detected
16	RO	0x0	MTLIS MTL Interrupt Status This bit indicates an interrupt event in the MTL. To reset this bit to 1'b0, the software must read the corresponding register in the MTL to get the exact cause of the interrupt and clear its source. Values: 1'b0: MTL Interrupt Status not detected 1'b1: MTL Interrupt Status detected
15:1	RO	0x0000	reserved
0	RO	0x0	DC0IS DMA Channel 0 Interrupt Status This bit indicates an interrupt event in DMA Channel 0. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 0 to get the exact cause of the interrupt and clear its source. Values: 1'b0: DMA Channel 0 Interrupt Status not detected 1'b1: DMA Channel 0 Interrupt Status detected

GMAC_DMA_DEBUG_STATUS0

Address: **Operational Base** + offset (0x100C)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RO	0x0	TPS1 DMA Channel 1 Transmit Process State This field indicates the Tx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt. Values: 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued) 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor) 0x2 (RUN_WS): Running (Waiting for status) 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)) 0x4 (TSTMP_WS): Timestamp write state 0x5 (RSVD): Reserved for future use 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow) 0x7 (RUN_CTD): Running (Closing Tx Descriptor)
19:16	RO	0x0	RPS1 DMA Channel 1 Receive Process State This field indicates the Rx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt. Values: 0x0 (STOP): Stopped (Reset or Stop Receive Command issued) 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor) 0x2 (RSVD): Reserved for future use 0x3 (RUN_WRP): Running (Waiting for Rx packet) 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable) 0x5 (RUN_CRD): Running (Closing the Rx Descriptor) 0x6 (TSTMP): Timestamp write state 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory)
15:12	RO	0x0	TPS0 DMA Channel 0 Transmit Process State This field indicates the Tx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. Values: 4'b0000: Stopped (Reset or Stop Transmit Command issued) 4'b0001: Running (Fetching Tx Transfer Descriptor) 4'b0010: Running (Waiting for status) 4'b0011: Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)) 4'b0100: Timestamp write state 4'b0101: Reserved for future use 4'b0110: Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow) 4'b0111: Running (Closing Tx Descriptor)

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Bit	Attr	Reset Value	Description
11:8	RO	0x0	RPS0 DMA Channel 0 Receive Process State This field indicates the Rx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. Values: 4'b0000: Stopped (Reset or Stop Receive Command issued) 4'b0001: Running (Fetching Rx Transfer Descriptor) 4'b0010: Reserved for future use 4'b0011: Running (Waiting for Rx packet) 4'b0100: Suspended (Rx Descriptor Unavailable) 4'b0101: Running (Closing the Rx Descriptor) 4'b0110: Timestamp write state 4'b0111: Running (Transferring the received packet data from the Rx buffer to the system memory)
7:2	RO	0x00	reserved
1	RO	0x0	AXRHSTS AXI Master Read Channel Status When high, this bit indicates that the read channel of the AXI master is active, and it is transferring the data. Values: 1'b0: AXI Master Read Channel Status not detected 1'b1: AXI Master Read Channel Status detected
0	RO	0x0	AXWHSTS AXI Master Write Channel or AHB Master Status EQOS-AXI Configuration: When high, this bit indicates that the write channel of the AXI master is active, and it is transferring data. EQOS-AHB Configuration: When high, this bit indicates that the AHB master FSMs are in the non-idle state. Values: 1'b0: AXI Master Write Channel or AHB Master Status not detected 1'b1: AXI Master Write Channel or AHB Master Status detected

GMAC_AXI_LPI_ENTRY_INTERVAL

Address: **Operational Base** + offset (0x1040)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	LPIEI LPI Entry Interval Contains the number of system clock cycles, multiplied by 64, to wait for an activity in the DWC_ether_qos to enter into the AXI low power state. 0 indicates 64 clock cycles.

GMAC_DMA_TBS_CTRL

Address: **Operational Base** + offset (0x1050)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	FTOS Fetch Time Offset The value in units of 256 nanoseconds, that has to be deducted from the Launch time to compute the Fetch Time. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	FGOS Fetch GSN Offset The number GSN slots that must be deducted from the Launch GSN to compute the Fetch GSN. Value valid only when FTOV is set.
3:1	RO	0x0	reserved
0	RW	0x0	FTOV Fetch Time Offset Valid When set indicates the FTOS field is valid. When not set, indicates the Fetch Offset is not valid and the DMA engine can fetch the frames from host memory without any time restrictions. Values: 0x0 (INVALID): Fetch Time Offset is invalid 0x1 (VALID): Fetch Time Offset is valid

GMAC_DMA_CH0_CONTROL

Address: **Operational Base** + offset (0x1100)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:18	RW	0x0	DSL Descriptor Skip Length This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	RO	0x0	reserved
16	RW	0x0	PBLx8 8xPBL mode When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH0_Tx_Control and Bits[21:16] in DMA_CH0_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled 0x1 (ENABLE): 8xPBL mode is enabled
15:14	RO	0x0	reserved
13:0	RW	0x0000	MSS Maximum Segment Size This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

GMAC_DMA_CH0_TX_CONTROL

Address: **Operational Base** + offset (0x1104)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:16	RW	0x00	TxPBL Transmit Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ[n]_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	RW	0x0	IPBL Ignore PBL Requirement When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL may use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it may block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled 0x1 (ENABLE): Ignore PBL Requirement is enabled
14:13	RW	0x0	TSE_MODE TSE Mode 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. 11: Reserved 0x0 (TSO_USO): TSO/USO 0x1 (UFOWC): UFO with Checksum 0x2 (UFOWOC): UFO without Checksum 0x3 (RSVD): Reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	TSE TCP Segmentation Enabled When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled 0x1 (ENABLE): TCP Segmentation is enabled
11:5	RO	0x00	reserved
4	RW	0x0	OSF Operate on Second Packet When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled 0x1 (ENABLE): Operate on Second Packet enabled
3:1	RO	0x0	reserved
0	RW	0x0	ST Start or Stop Transmission Command When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: 1.The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. 2.The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command 0x1 (START): Start Transmission Command

GMAC_DMA_CH0_RX_CONTROL
Address: **Operational Base** + offset (0x1108)

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Bit	Attr	Reset Value	Description
31	RW	0x0	RPF Rx Packet Flush When this bit is set to 1, then DWC_ether_qos automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the DWC_ether_qos not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This may in turn cause head-of-line blocking in the corresponding RxQueue. 0x0 (DISABLE): Rx Packet Flush is disabled 0x1 (ENABLE): Rx Packet Flush is enabled
30:22	RO	0x000	reserved
21:16	RW	0x00	RxPBL Receive Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ[n]_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	RO	0x0	reserved
14:4	RW	0x000	RBSZ_13_y Receive Buffer size High RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_3_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_3_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).

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Bit	Attr	Reset Value	Description
3:1	RO	0x0	RBSZ_3_0 Receive Buffer size Low RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_3_0. The RBSZ_3_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	RW	0x0	SR Start or Stop Receive When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets.The DMA tries to acquire descriptor from either of the following positions: 1.The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. 2.The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive 0x1 (START): Start Receive

GMAC_DMA_CH0_TXDESC_LIST_HADDRESS

Address: **Operational Base** + offset (0x1110)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	TDESHA Start of Transmit List This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Transmit descriptor list.

GMAC_DMA_CH0_TXDESC_LIST_ADDRESS

Address: **Operational Base** + offset (0x1114)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	TDESLA Start of Transmit List This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

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GMAC_DMA_CH0_RXDESC_LIST_HADDRESS

Address: **Operational Base** + offset (0x1118)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	RDESHA Start of Receive List This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

GMAC_DMA_CH0_RXDESC_LIST_ADDRESS

Address: **Operational Base** + offset (0x111C)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	RDESLA Start of Receive List This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH0_TXDESC_TAIL_POINTER

Address: **Operational Base** + offset (0x1120)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	TDTP Transmit Descriptor Tail Pointer This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH0_RXDESC_TAIL_POINTER

Address: **Operational Base** + offset (0x1128)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	RDRT Receive Descriptor Tail Pointer This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration

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Bit	Attr	Reset Value	Description
2:0	RO	0x0	reserved

GMAC_DMA_CH0_TXDESC_RING_LENGTH

Address: **Operational Base** + offset (0x112C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	TDRL Transmit Descriptor Ring Length This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. we recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

GMAC_DMA_CH0_RXDESC_RING_LENGTH

Address: **Operational Base** + offset (0x1130)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	RDRL Receive Descriptor Ring Length This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

GMAC_DMA_CH0_INTERRUPT_ENABLE

Address: **Operational Base** + offset (0x1134)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	NIE Normal Interrupt Summary Enable When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: Bit 0: Transmit Interrupt Bit 2: Transmit Buffer Unavailable Bit 6: Receive Interrupt Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled 0x1 (ENABLE): Normal Interrupt Summary is enabled

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Bit	Attr	Reset Value	Description
14	RW	0x0	AIE Abnormal Interrupt Summary Enable When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: Bit 1: Transmit Process Stopped Bit 7: Rx Buffer Unavailable Bit 8: Receive Process Stopped Bit 9: Receive Watchdog Timeout Bit 10: Early Transmit Interrupt Bit 12: Fatal Bus Error Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled 0x1 (ENABLE): Abnormal Interrupt Summary is enabled
13	RW	0x0	CDEE Context Descriptor Error Enable When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled 0x1 (ENABLE): Context Descriptor Error is enabled
12	RW	0x0	FBEE Fatal Bus Error Enable When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled 0x1 (ENABLE): Fatal Bus Error is enabled
11	RW	0x0	ERIE Early Receive Interrupt Enable When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled 0x1 (ENABLE): Early Receive Interrupt is enabled
10	RW	0x0	ETIE Early Transmit Interrupt Enable When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled 0x1 (ENABLE): Early Transmit Interrupt is enabled
9	RW	0x0	RWTE Receive Watchdog Timeout Enable When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled 0x1 (ENABLE): Receive Watchdog Timeout is enabled
8	RW	0x0	RSE Receive Stopped Enable When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled.

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Bit	Attr	Reset Value	Description
7	RW	0x0	RBUE Receive Buffer Unavailable Enable When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled 0x1 (ENABLE): Receive Buffer Unavailable is enabled
6	RW	0x0	RIE Receive Interrupt Enable When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled 0x1 (ENABLE): Receive Interrupt is enabled
5:3	RO	0x0	reserved
2	RW	0x0	TBUE Transmit Buffer Unavailable Enable When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled 0x1 (ENABLE): Transmit Buffer Unavailable is enabled
1	RW	0x0	TXSE Transmit Stopped Enable When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled 0x1 (ENABLE): Transmit Stopped is enabled
0	RW	0x0	TIE Transmit Interrupt Enable When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled 0x1 (ENABLE): Transmit Interrupt is enabled

GMAC_DMA_CH0_RX_INTERRUPT_WD_TIMER

Address: **Operational Base** + offset (0x1138)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	RWTU Receive Interrupt Watchdog Timer Count Units This fields indicates the number of system clock cycles corresponding to one unit in RWT field. 2'b00: 256 2'b01: 512 2'b10: 1024 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	RWT Receive Interrupt Watchdog Timer Count This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

GMAC_DMA_CH0_SLOT_FUNC_CTRL_STATUS

Address: **Operational Base** + offset (0x113C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RO	0x0	RSN Reference Slot Number This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	RW	0x07c	SIV Slot Interval Value This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us.
3:2	RO	0x0	reserved
1	RW	0x0	ASC Advance Slot Check When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is 1.equal to the reference slot number given in the RSN field 2.ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. Values: 0x0 (DISABLE): Advance Slot Check is disabled 0x1 (ENABLE): Advance Slot Check is

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Bit	Attr	Reset Value	Description
0	RW	0x0	ESC Enable Slot Comparison When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is 1.equal to the reference slot number 2.ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. Values: 0x0 (DISABLE): Slot Comparison is disabled 0x1 (ENABLE): Slot Comparison is enabled

GMAC_DMA_CH0_CURRENT_APP_TXDESC

Address: **Operational Base** + offset (0x1144)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURTDESAPTR Application Transmit Descriptor Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_CURRENT_APP_RXDESC

Address: **Operational Base** + offset (0x114C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURRDESAPTR Application Receive Descriptor Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_CURRENT_APP_TXBUFFER_H

Address: **Operational Base** + offset (0x1150)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	CURTBUFAPTRH Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_CURRENT_APP_TXBUFFER

Address: **Operational Base** + offset (0x1154)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURTBUFAPTR Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

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GMAC_DMA_CH0_CURRENT_APP_RXBUFFER_H

Address: **Operational Base** + offset (0x1158)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	CURRBUFAPTRH Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_CURRENT_APP_RXBUFFER

Address: **Operational Base** + offset (0x115C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURRBUFAPTR Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_STATUS

Address: **Operational Base** + offset (0x1160)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:19	RO	0x0	REB Rx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. 1.Bit 21 1'b1: Error during data transfer by Rx DMA 1'b0: No Error during data transfer by Rx DMA 2.Bit 20 1'b1: Error during descriptor access 1'b0: Error during data buffer access 3.Bit 19 1'b1: Error during read transfer 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	RO	0x0	TEB Tx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. 1.Bit 18 1'b1: Error during data transfer by Tx DMA 1'b0: No Error during data transfer by Tx DMA 2.Bit 17 1'b1: Error during descriptor access 1'b0: Error during data buffer access 3.Bit 16 1'b1: Error during read transfer 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.

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Bit	Attr	Reset Value	Description
15	RW	0x0	NIS Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: Bit 0: Transmit Interrupt Bit 2: Transmit Buffer Unavailable Bit 6: Receive Interrupt Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected 0x1 (ACTIVE): Normal Interrupt Summary status detected
14	RW	0x0	AIS Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: Bit 1: Transmit Process Stopped Bit 7: Receive Buffer Unavailable Bit 8: Receive Process Stopped Bit 10: Early Transmit Interrupt Bit 12: Fatal Bus Error Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected 0x1 (ACTIVE): Abnormal Interrupt Summary status
13	RW	0x0	CDE Context Descriptor Error This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected 0x1 (ACTIVE): Context Descriptor Error status detected

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Bit	Attr	Reset Value	Description
12	RW	0x0	FBE Fatal Bus Error This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected 0x1 (ACTIVE): Fatal Bus Error status detected
11	RW	0x0	ERI Early Receive Interrupt This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer.The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected 0x1 (ACTIVE): Early Receive Interrupt status detected
10	RW	0x0	ETI Early Transmit Interrupt This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected 0x1 (ACTIVE): Early Transmit Interrupt status detected
9	RW	0x0	RWT Receive Watchdog Timeout This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected 0x1 (ACTIVE): Receive Watchdog Timeout status detected
8	RW	0x0	RPS Receive Process Stopped This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected 0x1 (ACTIVE): Receive Process Stopped status detected

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Bit	Attr	Reset Value	Description
7	RW	0x0	RBU Receive Buffer Unavailable This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected 0x1 (ACTIVE): Receive Buffer Unavailable status detected
6	RW	0x0	RI Receive Interrupt This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected 0x1 (ACTIVE): Receive Interrupt status detected
5:3	RO	0x0	reserved
2	RW	0x0	TBU Transmit Buffer Unavailable This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected 0x1 (ACTIVE): Transmit Buffer Unavailable status

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Bit	Attr	Reset Value	Description
1	RW	0x0	TPS Transmit Process Stopped This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected 0x1 (ACTIVE): Transmit Process Stopped status detected
0	RW	0x0	TI Transmit Interrupt This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected 0x1 (ACTIVE): Transmit Interrupt status detected

GMAC_DMA_CH0_MISS_FRAME_CNT

Address: **Operational Base** + offset (0x1164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	MFC0 Overflow status of the MFC Counter When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred 0x1 (ACTIVE): Miss Frame Counter overflow occurred
14:11	RO	0x0	reserved
10:0	RO	0x000	MFC Dropped Packet Counters This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_DMA_CH0_RX_ERI_CNT

Address: **Operational Base** + offset (0x1168)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	ECNT ERI Counter When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter will get reset at the start of new packet.

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GMAC_MAC_ADDRESS1_HIGH

Address: **Operational Base** + offset (0x0308)

Bit	Attr	Reset Value	Description
31	RO	0x0	AE Address Enable This bit is always set to 1. Values: 1'b0: This bit must be always set to 1 1'b1: This bit is always set to 1
30	RW	0x0	SA Source Address When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. Values: 0x0 (DA): Compare with Destination Address 0x1 (SA): Compare with Source Address
29:24	RW	0x00	MBC Mask Byte Control These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: Bit 29: MAC_Address1_High[15:8] Bit 28: MAC_Address1_High[7:0] Bit 27: MAC_Address1_Low[31:24] ... Bit 24: MAC_Address1_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:17	RO	0x00	reserved
16	RW	0x0	DCS DMA Channel Select If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address1 content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address1 content is routed.
15:0	RW	0xffff	ADDRHI MAC Address1[47:32] This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

GMAC_MAC_ADDRESS1_LOW

Address: **Operational Base** + offset (0x030C)

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Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	ADDRLO MAC Address1[31:0] This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

GMAC_MAC_ADDRESS2_HIGH

Address: **Operational Base** + offset (0x0310)

Bit	Attr	Reset Value	Description
31	RO	0x0	AE Address Enable This bit is always set to 1. Values: 1'b0: This bit must be always set to 1 1'b1: This bit is always set to 1
30	RW	0x0	SA Source Address When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. Values: 0x0 (DA): Compare with Destination Address 0x1 (SA): Compare with Source Address
29:24	RW	0x00	MBC Mask Byte Control These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: Bit 29: MAC_Address2_High[15:8] Bit 28: MAC_Address2_High[7:0] Bit 27: MAC_Address2_Low[31:24] ... Bit 24: MAC_Address2_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:17	RO	0x00	reserved
16	RW	0x0	DCS DMA Channel Select If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address1 content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address1 content is routed.
15:0	RW	0xffff	ADDRHI MAC Address2[47:32] This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

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GMAC_MAC_ADDRESS2_LOW

Address: **Operational Base** + offset (0x0314)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	ADDRLO MAC Address2[31:0] This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

GMAC_MAC_ADDRESS3_HIGH

Address: **Operational Base** + offset (0x0318)

Bit	Attr	Reset Value	Description
31	RO	0x0	AE Address Enable This bit is always set to 1. Values: 1'b0: This bit must be always set to 1 1'b1: This bit is always set to 1
30	RW	0x0	SA Source Address When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. Values: 0x0 (DA): Compare with Destination Address 0x1 (SA): Compare with Source Address
29:24	RW	0x00	MBC Mask Byte Control These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: Bit 29: MAC_Address3_High[15:8] Bit 28: MAC_Address3_High[7:0] Bit 27: MAC_Address3_Low[31:24] ... Bit 24: MAC_Address3_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:17	RO	0x00	reserved
16	RW	0x0	DCS DMA Channel Select If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address1 content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address1 content is routed.

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Bit	Attr	Reset Value	Description
15:0	RW	0xffff	ADDRHI MAC Address3[47:32] This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

GMAC_MAC_ADDRESS3_LOW

Address: **Operational Base** + offset (0x031C)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	ADDRLO MAC Address3[31:0] This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

GMAC_MAC_L3_L4_CONTROL1

Address: **Operational Base** + offset (0x0930)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	DMCHEN0 DMA Channel Select Enable When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter. Values: 0x0 (DISABLE): DMA Channel Select is disabled 0x1 (ENABLE): DMA Channel Select is enabled
27:25	RO	0x0	reserved
24	RW	0x0	DMCHN0 DMA Channel Number When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration.
23:22	RO	0x0	reserved
21	RW	0x0	L4DPIM0 Layer 4 Destination Port Inverse Match Enable When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM0 bit is set high. Values: 0x0 (DISABLE): Layer 4 Destination Port Inverse Match is disabled 0x1 (ENABLE): Layer 4 Destination Port Inverse Match is enabled

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Bit	Attr	Reset Value	Description
20	RW	0x0	L4DPM0 Layer 4 Destination Port Match Enable When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching. Values: 0x0 (DISABLE): Layer 4 Destination Port Match is disabled 0x1 (ENABLE): Layer 4 Destination Port Match is enabled
19	RW	0x0	L4SPIM0 Layer 4 Source Port Inverse Match Enable When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4SPM0 bit is set high. Values: 0x0 (DISABLE): Layer 4 Source Port Inverse Match is disabled 0x1 (ENABLE): Layer 4 Source Port Inverse Match is enabled
18	RW	0x0	L4SPM0 Layer 4 Source Port Match Enable When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching. Values: 0x0 (DISABLE): Layer 4 Source Port Match is disabled 0x1 (ENABLE): Layer 4 Source Port Match is enabled
17	RO	0x0	reserved
16	RW	0x0	L4PEN0 Layer 4 Protocol Enable When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching. The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set. Values: 0x0 (DISABLE): Layer 4 Protocol is disabled 0x1 (ENABLE): Layer 4 Protocol is enabled

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Bit	Attr	Reset Value	Description
15:11	RW	0x00	L3HDBM0 Layer 3 IP DA Higher Bits Match IPv4 Packets: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field: 0: No bits are masked. 1: LSb[0] is masked 2: Two LSbs [1:0] are masked .. 31: All bits except MSb are masked. IPv6 Packets: Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits: 0: No bits are masked. 1: LSb[0] is masked. 2: Two LSbs [1:0] are masked .. 127: All bits except MSb are masked. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set.
10:6	RW	0x00	L3HSBM0 Layer 3 IP SA Higher Bits Match IPv4 Packets: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field: 0: No bits are masked. 1: LSb[0] is masked 2: Two LSbs [1:0] are masked .. 31: All bits except MSb are masked. IPv6 Packets: This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high.
5	RW	0x0	L3DAIM0 Layer 3 IP DA Inverse Match Enable When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high. Values: 0x0 (DISABLE): Layer 3 IP DA Inverse Match is disabled 0x1 (ENABLE): Layer 3 IP DA Inverse Match is enabled

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Bit	Attr	Reset Value	Description
4	RW	0x0	L3DAM0 Layer 3 IP DA Match Enable When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering. Values: 0x0 (DISABLE): Layer 3 IP DA Match is disabled 0x1 (ENABLE): Layer 3 IP DA Match is enabled
3	RW	0x0	L3SAIM0 Layer 3 IP SA Inverse Match Enable When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when the L3SAM0 bit is set. Values: 0x0 (DISABLE): Layer 3 IP SA Inverse Match is disabled 0x1 (ENABLE): Layer 3 IP SA Inverse Match is enabled
2	RW	0x0	L3SAM0 Layer 3 IP SA Match Enable When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering. Values: 0x0 (DISABLE): Layer 3 IP SA Match is disabled 0x1 (ENABLE): Layer 3 IP SA Match is enabled
1	RO	0x0	reserved
0	RW	0x0	L3PEN0 Layer 3 Protocol Enable When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets. The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set. Values: 0x0 (DISABLE): Layer 3 Protocol is disabled 0x1 (ENABLE): Layer 3 Protocol is enabled

GMAC_MAC_LAYER4_ADDRESS1

Address: **Operational Base** + offset (0x0934)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	L4DP0 Layer 4 Destination Port Number Field When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets.
15:0	RW	0x0000	L4SP0 Layer 4 Source Port Number Field When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets.

GMAC_MAC_LAYER3_ADDR0_REG1

Address: **Operational Base** + offset (0x0940)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	L3A00 Layer 3 Address 0 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

GMAC_MAC_LAYER3_ADDR1_REG1

Address: **Operational Base** + offset (0x0944)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	L3A10 Layer 3 Address 1 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets.

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GMAC_MAC_LAYER3_ADDR2_REG1

Address: **Operational Base** + offset (0x0948)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	L3A20 Layer 3 Address 2 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

GMAC_MAC_LAYER3_ADDR3_REG1

Address: **Operational Base** + offset (0x094C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	L3A30 Layer 3 Address 3 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

GMAC_MTL_TXQ1_OPERATION_MODE

Address: **Operational Base** + offset (0x0D40)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x06	TQS Transmit Queue Size This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	TTC Transmit Threshold Control These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset. Values: 3'b000: 32 bytes 3'b001: 64 bytes 3'b010: 96 bytes 3'b011: 128 bytes 3'b100: 192 bytes 3'b101: 256 bytes 3'b110: 384 bytes 3'b111: 512 bytes
3:2	RW	0x0	TXQEN Transmit Queue Enable This field is used to enable/disable the transmit queue 0. 2'b00: Not enabled 2'b01: Reserved 2'b10: Enabled 2'b11: Reserved This field is Read Only in Single Queue configurations and Read Write in Multiple Queue configurations. Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. Values: 0x0 (DISABLE): Not enabled 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV) 0x2 (ENABLE): Enabled 0x3 (RSVD2): Reserved
1	RW	0x0	TSF Transmit Store and Forward When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. Values: 1'b0: Transmit Store and Forward is disabled 1'b1: Transmit Store and Forward is enabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	FTQ Flush Transmit Queue When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Flush Transmit Queue is disabled 1'b1: Flush Transmit Queue is enabled

GMAC_MTL_TXQ1_UNDERFLOW

Address: **Operational Base** + offset (0x0D44)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RO	0x0	UFCNTOVF Overflow Bit for Underflow Packet Counter This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Overflow not detected for Underflow Packet Counter 1'b1: Overflow detected for Underflow Packet Counter
10:0	RO	0x000	UFFRMCNT Underflow Packet Counter This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_MTL_TXQ1_DEBUG

Address: **Operational Base** + offset (0x0D48)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RO	0x0	STXSTSF Number of Status Words in Tx Status FIFO of Queue This field indicates the current number of status in the Tx Status FIFO of this queue.When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:16	RO	0x0	PTXQ Number of Packets in the Transmit Queue This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	RO	0x000	reserved
5	RO	0x0	TXSTSFSTS MTL Tx Status FIFO Full Status When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. Values: 1'b0: MTL Tx Status FIFO Full status is not detected 1'b1: MTL Tx Status FIFO Full status is detected
4	RO	0x0	TXQSTS MTL Tx Queue Not Empty Status When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. Values: 1'b0: MTL Tx Queue Not Empty status is not detected 1'b1: MTL Tx Queue Not Empty status is detected
3	RO	0x0	TWCSTS MTL Tx Queue Write Controller Status When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. Values: 1'b0: MTL Tx Queue Write Controller status is not detected 1'b1: MTL Tx Queue Write Controller status is detected
2:1	RO	0x0	TRCSTS MTL Tx Queue Read Controller Status This field indicates the state of the Tx Queue Read Controller: Values: 2'b00: Idle state 2'b01: Read state (transferring data to the MAC transmitter) 2'b10: Waiting for pending Tx Status from the MAC transmitter 2'b11: Flushing the Tx queue because of the Packet Abort request from the MAC
0	RO	0x0	TXQPAUSED Transmit Queue in Pause When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: 1. Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled 2. Reception of 802.3x Pause packet when PFC is disabled Values: 1'b0: Transmit Queue in Pause status is not detected 1'b1: Transmit Queue in Pause status is detected

GMAC_MTL_TXQ1_ETS_CONTROL

Address: **Operational Base** + offset (0x0D50)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	SLC Slot Count If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH[n]_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_Tx[n]_ETS_Status register, need to be computed for Queue. The encoding is as follows: Values: 0x0 (1_SLOT): 1 slot 0x1 (2_SLOT): 2 slots 0x2 (4_SLOT): 4 slots 0x3 (8_SLOT): 8 slots 0x4 (16_SLOT): 16 slots 0x5 (RSVD): Reserved
3	RW	0x0	CC Credit Control When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. Values: 0x0 (DISABLE): Credit Control is disabled 0x1 (ENABLE): Credit Control is enabled
2	RW	0x0	AVALG AV Algorithm When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. Values: 0x0 (DISABLE): CBS Algorithm is disabled 0x1 (ENABLE): CBS Algorithm is enabled
1:0	RO	0x0	reserved

GMAC_MTL_TXQ1_ETS_STATUS

Address: **Operational Base** + offset (0x0D54)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	ABS Average Bits per Slot This field contains the average transmitted bits per slot. When the DCB operation is enabled for Queue 0, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

GMAC_MTL_TXQ1_QUANTUM_WEIGHT

Address: **Operational Base** + offset (0x0D58)

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Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x000000	ISCQW idleSlopeCredit, Quantum or Weights 1.idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. 2.Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. 3.Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

GMAC_MTL_TXQ1_SENDSLOPECREDIT

Address: **Operational Base** + offset (0x0D5C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	SSC sendSlopeCredit Value When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

GMAC_MTL_TXQ1_HICREDIT

Address: **Operational Base** + offset (0x0D60)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	HC hiCredit Value When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

GMAC_MTL_TXQ1_LOCREDIT

Address: **Operational Base** + offset (0x0D64)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	LC loCredit Value When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

GMAC_MTL_Q1_INTERRUPT_CTRL_STATUS

Address: **Operational Base** + offset (0x0D6C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24	RW	0x0	RXOIE Receive Queue Overflow Interrupt Enable When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. Values: 1'b0: Receive Queue Overflow Interrupt is disabled 1'b1: Receive Queue Overflow Interrupt is enabled
23:17	RO	0x00	reserved
16	RW	0x0	RXOVFIS Receive Queue Overflow Interrupt Status This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 1'b0: Receive Queue Overflow Interrupt Status not detected 1'b1: Receive Queue Overflow Interrupt Status detected
15:10	RO	0x00	reserved
9	RW	0x0	ABPSIE Average Bits Per Slot Interrupt Enable When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. Values: 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled
8	RW	0x0	TXUIE Transmit Queue Underflow Interrupt Enable When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. Values: 1'b0: Transmit Queue Underflow Interrupt Status is disabled 1'b1: Transmit Queue Underflow Interrupt Status is enabled
7:2	RO	0x00	reserved
1	RW	0x0	ABPSIS Average Bits Per Slot Interrupt Status When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected

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Bit	Attr	Reset Value	Description
0	RW	0x0	TXUNFIS Transmit Queue Underflow Interrupt Status This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 1'b0: Transmit Queue Underflow Interrupt Status not detected 1'b1: Transmit Queue Underflow Interrupt Status detected

GMAC_MTL_RXQ1_OPERATION_MODE

Address: **Operational Base** + offset (0x0D70)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:20	RW	0x00	RQS Receive Queue Size This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	RW	0x00	RFD Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: 0: Full minus 1 KB, that is, FULL 1 KB 1: Full minus 1.5 KB, that is, FULL 1.5 KB 2: Full minus 2 KB, that is, FULL 2 KB 3: Full minus 2.5 KB, that is, FULL 2.5 KB ... 62: Full minus 32 KB, that is, FULL 32 KB 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.

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Bit	Attr	Reset Value	Description
13:8	RW	0x00	RFA Threshold for Activating Flow Control (in half-duplex and full-duplex) These bits control the threshold (fill-level of Rx queue) at which the flow control is activated:For more information on encoding for this field, see RFD.
7	RW	0x0	EHFC Enable Hardware Flow Control When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. Values: 1'b0: Hardware Flow Control is disabled 1'b1: Hardware Flow Control is enabled
6	RW	0x0	DIS_TCP_EF Disable Dropping of TCP/IP Checksum Error Packets When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. Values: 1'b0: Dropping of TCP/IP Checksum Error Packets is enabled 1'b1: Dropping of TCP/IP Checksum Error Packets is disabled
5	RW	0x0	RSF Receive Queue Store and Forward When this bit is set, the DWC_ether_qos reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. Values: 1'b0: Receive Queue Store and Forward is disabled 1'b1: Receive Queue Store and Forward is enabled
4	RW	0x0	FEP Forward Error Packets When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet may be forwarded to the application or DMA. Values: 1'b0: Forward Error Packets is disabled 1'b1: Forward Error Packets is enabled

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Bit	Attr	Reset Value	Description
3	RW	0x0	FUP Forward Undersized Good Packets When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. Values: 1'b0: Forward Undersized Good Packets is disabled 1'b1: Forward Undersized Good Packets is enabled
2	RO	0x0	reserved
1:0	RW	0x0	RTC Receive Queue Threshold Control These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1.

GMAC_MTL_RXQ1_MISS_PKT_OVF_CNT

Address: **Operational Base** + offset (0x0D74)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RO	0x0	MISCNTOVF Missed Packet Counter Overflow Bit When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Missed Packet Counter overflow not detected 1'b1: Missed Packet Counter overflow detected
26:16	RO	0x000	MISPKTCNT Missed Packet Counter This field indicates the number of packets missed by the DWC_ether_qos because the application asserted ari_pkt_flush_i[] for this queue. This counter is incremented each time the application issues ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. In EQOS-DMA, EQOS-AXI, and EQOS-AHB configurations, This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	RO	0x0	OVFCNTOVF Overflow Counter Overflow Bit When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Overflow Counter overflow not detected 1'b1: Overflow Counter overflow detected
10:0	RO	0x000	OVFPKTCNT Overflow Packet Counter This field indicates the number of packets discarded by the DWC_ether_qos because of Receive queue overflow. This counter is incremented each time the DWC_ether_qos discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_MTL_RXQ1_DEBUG

Address: **Operational Base** + offset (0x0D78)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RO	0x0	PRXQ Number of Packets in Receive Queue This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size.
15:6	RO	0x000	reserved
5:4	RO	0x0	RXQSTS MTL Rx Queue Fill-Level Status This field gives the status of the fill-level of the Rx Queue: Values: 2'b00: Rx Queue empty 2'b01: Rx Queue fill-level below flow-control deactivate threshold 2'b10: Rx Queue fill-level above flow-control activate threshold 2'b11: Rx Queue full
3	RO	0x0	reserved
2:1	RO	0x0	RRCSTS MTL Rx Queue Read Controller State This field gives the state of the Rx queue Read controller: Values: 2'b00: Idle state 2'b01: Reading packet data 2'b10: Reading packet status (or timestamp) 2'b11: Flushing the packet data and status
0	RO	0x0	RWCSTS MTL Rx Queue Write Controller Active Status When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. Values: 1'b0: MTL Rx Queue Write Controller Active Status not detected 1'b1: MTL Rx Queue Write Controller Active Status detected

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GMAC_MTL_RXQ1_CONTROL

Address: **Operational Base** + offset (0x0D7C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	RXQ_FRM_ARBIT Receive Queue Packet Arbitration When this bit is set, the DWC_ether_qos drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the DWC_ether_qos drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: 1.PBL amount of data (indicated by ari_qN_pbl_i[]) 2.Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the DWC_ether_qos drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). Values: 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled
2:0	RW	0x0	RXQ_WEGT Receive Queue Weight This field indicates the weight assigned to the Rx Queue 0. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle.

GMAC_DMA_CH1_CONTROL

Address: **Operational Base** + offset (0x1180)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:18	RW	0x0	DSL Descriptor Skip Length This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	RO	0x0	reserved
16	RW	0x0	PBLx8 8xPBL mode When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH1_Tx_Control and Bits[21:16] in DMA_CH1_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled 0x1 (ENABLE): 8xPBL mode is enabled
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	MSS Maximum Segment Size This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH1_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

GMAC_DMA_CH1_TX_CONTROL

Address: **Operational Base** + offset (0x1184)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	TxPBL Transmit Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ[n]_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	RW	0x0	IPBL Ignore PBL Requirement When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL may use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it may block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled 0x1 (ENABLE): Ignore PBL Requirement is enabled

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Bit	Attr	Reset Value	Description
14:13	RW	0x0	TSE_MODE TSE Mode 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. 11: Reserved 0x0 (TSO_USO): TSO/USO 0x1 (UFOWC): UFO with Checksum 0x2 (UFOWOC): UFO without Checksum 0x3 (RSVD): Reserved
12	RW	0x0	TSE TCP Segmentation Enabled When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled 0x1 (ENABLE): TCP Segmentation is enabled
11:5	RO	0x00	reserved
4	RW	0x0	OSF Operate on Second Packet When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled 0x1 (ENABLE): Operate on Second Packet enabled
3:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	ST Start or Stop Transmission Command When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: 1.The current position in the list This is the base address of the Transmit list set by the DMA_CH1_TxDesc_List_Address register. 2.The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH1_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH1_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH1_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command 0x1 (START): Start Transmission Command

GMAC_DMA_CH1_RX_CONTROL

Address: **Operational Base** + offset (0x1188)

Bit	Attr	Reset Value	Description
31	RW	0x0	RPF Rx Packet Flush When this bit is set to 1, then DWC_ether_qos automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the DWC_ether_qos not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This may in turn cause head-of-line blocking in the corresponding RxQueue. 0x0 (DISABLE): Rx Packet Flush is disabled 0x1 (ENABLE): Rx Packet Flush is enabled
30:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:16	RW	0x00	RxPBL Receive Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ[n]_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	RO	0x0	reserved
14:4	RW	0x000	RBSZ_13_y Receive Buffer size High RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_3_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_3_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	RO	0x0	RBSZ_3_0 Receive Buffer size Low RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_3_0. The RBSZ_3_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).

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Bit	Attr	Reset Value	Description
0	RW	0x0	SR Start or Stop Receive When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets.The DMA tries to acquire descriptor from either of the following positions: 1.The current position in the list This is the address set by the DMA_CH1_RxDesc_List_Address register. 2.The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH1_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH1_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive 0x1 (START): Start Receive

GMAC_DMA_CH1_TXDESC_LIST_HADDRESS

Address: **Operational Base** + offset (0x1190)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	TDESHA Start of Transmit List This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Transmit descriptor list.

GMAC_DMA_CH1_TXDESC_LIST_ADDRESS

Address: **Operational Base** + offset (0x1194)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	TDESLA Start of Transmit List This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH1_RXDESC_LIST_HADDRESS

Address: **Operational Base** + offset (0x1198)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	RDESHA Start of Receive List This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

GMAC_DMA_CH1_RXDESC_LIST_ADDRESS

Address: **Operational Base** + offset (0x119C)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	RDESLA Start of Receive List This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH1_TXDESC_TAIL_POINTER

Address: **Operational Base** + offset (0x11A0)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	TDTP Transmit Descriptor Tail Pointer This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH1_RXDESC_TAIL_POINTER

Address: **Operational Base** + offset (0x11A8)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	RDRT Receive Descriptor Tail Pointer This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH1_TXDESC_RING_LENGTH

Address: **Operational Base** + offset (0x11AC)

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Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	TDRL Transmit Descriptor Ring Length This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. we recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

GMAC_DMA_CH1_RXDESC_RING_LENGTH

Address: **Operational Base** + offset (0x11B0)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	RDRL Receive Descriptor Ring Length This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

GMAC_DMA_CH1_INTERRUPT_ENABLE

Address: **Operational Base** + offset (0x11B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	NIE Normal Interrupt Summary Enable When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH1_Status register: Bit 0: Transmit Interrupt Bit 2: Transmit Buffer Unavailable Bit 6: Receive Interrupt Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled 0x1 (ENABLE): Normal Interrupt Summary is enabled
14	RW	0x0	AIE Abnormal Interrupt Summary Enable When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH1_Status register: Bit 1: Transmit Process Stopped Bit 7: Rx Buffer Unavailable Bit 8: Receive Process Stopped Bit 9: Receive Watchdog Timeout Bit 10: Early Transmit Interrupt Bit 12: Fatal Bus Error Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled 0x1 (ENABLE): Abnormal Interrupt Summary is enabled

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Bit	Attr	Reset Value	Description
13	RW	0x0	CDEE Context Descriptor Error Enable When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled 0x1 (ENABLE): Context Descriptor Error is enabled
12	RW	0x0	FBEE Fatal Bus Error Enable When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled 0x1 (ENABLE): Fatal Bus Error is enabled
11	RW	0x0	ERIE Early Receive Interrupt Enable When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled 0x1 (ENABLE): Early Receive Interrupt is enabled
10	RW	0x0	ETIE Early Transmit Interrupt Enable When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled 0x1 (ENABLE): Early Transmit Interrupt is enabled
9	RW	0x0	RWTE Receive Watchdog Timeout Enable When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled 0x1 (ENABLE): Receive Watchdog Timeout is enabled
8	RW	0x0	RSE Receive Stopped Enable When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled.
7	RW	0x0	RBUE Receive Buffer Unavailable Enable When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled 0x1 (ENABLE): Receive Buffer Unavailable is enabled
6	RW	0x0	RIE Receive Interrupt Enable When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled 0x1 (ENABLE): Receive Interrupt is enabled
5:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	TBUE Transmit Buffer Unavailable Enable When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled 0x1 (ENABLE): Transmit Buffer Unavailable is enabled
1	RW	0x0	TXSE Transmit Stopped Enable When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled 0x1 (ENABLE): Transmit Stopped is enabled
0	RW	0x0	TIE Transmit Interrupt Enable When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled 0x1 (ENABLE): Transmit Interrupt is enabled

GMAC_DMA_CH1_RX_INTERRUPT_WD_TIMER

Address: **Operational Base** + offset (0x11B8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	RWTU Receive Interrupt Watchdog Timer Count Units This fields indicates the number of system clock cycles corresponding to one unit in RWT field. 2'b00: 256 2'b01: 512 2'b10: 1024 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	RO	0x00	reserved
7:0	RW	0x00	RWT Receive Interrupt Watchdog Timer Count This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

GMAC_DMA_CH1_SLOT_FUNC_CTRL_STATUS

Address: **Operational Base** + offset (0x11BC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
19:16	RO	0x0	RSN Reference Slot Number This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	RW	0x07c	SIV Slot Interval Value This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us.
3:2	RO	0x0	reserved
1	RW	0x0	ASC Advance Slot Check When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is 1.equal to the reference slot number given in the RSN field 2.ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. Values: 0x0 (DISABLE): Advance Slot Check is disabled 0x1 (ENABLE): Advance Slot Check is
0	RW	0x0	ESC Enable Slot Comparison When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is 1.equal to the reference slot number 2.ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. Values: 0x0 (DISABLE): Slot Comparison is disabled 0x1 (ENABLE): Slot Comparison is enabled

GMAC_DMA_CH1_CURRENT_APP_TXDESC

Address: **Operational Base** + offset (0x11C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURTDESAPTR Application Transmit Descriptor Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

GMAC_DMA_CH1_CURRENT_APP_RXDESC

Address: **Operational Base** + offset (0x11CC)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURRDESAPTR Application Receive Descriptor Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

GMAC_DMA_CH1_CURRENT_APP_TXBUFFER_H

Address: **Operational Base** + offset (0x11D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	CURTBUFAPTRH Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

GMAC_DMA_CH1_CURRENT_APP_TXBUFFER

Address: **Operational Base** + offset (0x11D4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURTBUFAPTR Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

GMAC_DMA_CH1_CURRENT_APP_RXBUFFER_H

Address: **Operational Base** + offset (0x11D8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	CURRBUFAPTRH Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

GMAC_DMA_CH1_CURRENT_APP_RXBUFFER

Address: **Operational Base** + offset (0x11DC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURRBUFAPTR Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

GMAC_DMA_CH1_STATUS

Address: **Operational Base** + offset (0x11E0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:19	RO	0x0	REB Rx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. 1.Bit 21 1'b1: Error during data transfer by Rx DMA 1'b0: No Error during data transfer by Rx DMA 2.Bit 20 1'b1: Error during descriptor access 1'b0: Error during data buffer access 3.Bit 19 1'b1: Error during read transfer 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	RO	0x0	TEB Tx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. 1.Bit 18 1'b1: Error during data transfer by Tx DMA 1'b0: No Error during data transfer by Tx DMA 2.Bit 17 1'b1: Error during descriptor access 1'b0: Error during data buffer access 3.Bit 16 1'b1: Error during read transfer 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	RW	0x0	NIS Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH1_Interrupt_Enable register: Bit 0: Transmit Interrupt Bit 2: Transmit Buffer Unavailable Bit 6: Receive Interrupt Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected 0x1 (ACTIVE): Normal Interrupt Summary status detected

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Bit	Attr	Reset Value	Description
14	RW	0x0	AIS Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH1_Interrupt_Enable register: Bit 1: Transmit Process Stopped Bit 7: Receive Buffer Unavailable Bit 8: Receive Process Stopped Bit 10: Early Transmit Interrupt Bit 12: Fatal Bus Error Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected 0x1 (ACTIVE): Abnormal Interrupt Summary status
13	RW	0x0	CDE Context Descriptor Error This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected 0x1 (ACTIVE): Context Descriptor Error status detected
12	RW	0x0	FBE Fatal Bus Error This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected 0x1 (ACTIVE): Fatal Bus Error status detected
11	RW	0x0	ERI Early Receive Interrupt This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer.The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected 0x1 (ACTIVE): Early Receive Interrupt status detected

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Bit	Attr	Reset Value	Description
10	RW	0x0	ETI Early Transmit Interrupt This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected 0x1 (ACTIVE): Early Transmit Interrupt status detected
9	RW	0x0	RWT Receive Watchdog Timeout This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected 0x1 (ACTIVE): Receive Watchdog Timeout status detected
8	RW	0x0	RPS Receive Process Stopped This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected 0x1 (ACTIVE): Receive Process Stopped status detected
7	RW	0x0	RBU Receive Buffer Unavailable This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected 0x1 (ACTIVE): Receive Buffer Unavailable status detected

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Bit	Attr	Reset Value	Description
6	RW	0x0	RI Receive Interrupt This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected 0x1 (ACTIVE): Receive Interrupt status detected
5:3	RO	0x0	reserved
2	RW	0x0	TBU Transmit Buffer Unavailable This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected 0x1 (ACTIVE): Transmit Buffer Unavailable status
1	RW	0x0	TPS Transmit Process Stopped This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected 0x1 (ACTIVE): Transmit Process Stopped status detected
0	RW	0x0	TI Transmit Interrupt This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected 0x1 (ACTIVE): Transmit Interrupt status detected

GMAC_DMA_CH1_MISS_FRAME_CNT

Address: **Operational Base** + offset (0x11E4)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	MFC0 Overflow status of the MFC Counter When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred 0x1 (ACTIVE): Miss Frame Counter overflow occurred
14:11	RO	0x0	reserved
10:0	RO	0x000	MFC Dropped Packet Counters This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_DMA_CH1_RX_ERI_CNT

Address: **Operational Base** + offset (0x11E8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	ECNT ERI Counter When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter will get reset at the start of new packet.

8.5 Interface Description

There are two GMAC Controllers in RK3576, and each has two sets of IO interface, as shown below:

Table 8-3 GMAC0 Interface

Module Pin	Direction	Pad Name	IOMUX Setting
RMII/RGMII M0 Interface			
mac_clk_m0	I/O	VO_LCDC_D19/VO_EBC_SDCE3/ETH0_MCLK_M0/SAI4_MCLK_M1/DSMC_CSN1/FLEXBUS0_D8/UART10_RX_M0/SPI2_MOSI_M2/PWM0_CH0_M3/GPIO3_B0_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[3:0] = 4'h3
mac_txen_m0	O	VO_LCDC_D16/VO_EBC_SDCE0/ETH0_TXCTL_M0/PDM1_SDI0_M2/DSMC_DATA10/FLEXBUS0_D2/UART9_TX_M1/I2C8_SCL_M3/GPIO3_B3_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[15:12] = 4'h3
mac_txd3_m0	O	VO_LCDC_D9/VO_EBC_SDDO9/ETH0_TXD3_M0/SAI2_SCLK_M2/DSMC_INT1/FLEXBUS0_D9/UART11_RTSN_M0/SPI4_MISO_M1/I2C9_SCL_M3/PWM2_CH0_M3/GPIO3_C2_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[11:8] = 4'h3

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mac_txd2_m0	O	VO_LCDC_D8/VO_EBC_SDDO8/ETH0_TXD2_M0/SAI2_LRCK_M2/DSMC_INT3/FLEXBUS0_D10/FLEXBUS0_CSN_M2/UART11_CTSN_M0/SPI4_MOSI_M1/I2C9_SDA_M3/PWM2_CH1_M3/GPIO3_C3_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[15:12] = 4'h3
mac_txd1_m0	O	VO_LCDC_D15/VO_EBC_SDDO15/ETH0_TXD1_M0/SPDIF_RX1_M0/DSMC_DATA9/FLEXBUS0_D1/UART9_RTSN_M1/PWM1_CH4_M3/GPIO3_B4_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[3:0] = 4'h3
mac_txd0_m0	O	VO_LCDC_D14/VO_EBC_SDDO14/ETH0_TXD0_M0/SPDIF_TX1_M0/DSMC_DATA8/FLEXBUS0_D0/UART9_CTSN_M1/PWM1_CH5_M3/GPIO3_B5_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[7:4] = 4'h3
mac_txclk_m0	O	VO_LCDC_D13/VO_EBC_SDDO13/ETH0_TXCLK_M0/DSMC_DQS1/FLEXBUS0_CLK/SPI3_CSN0_M1/PWM0_CH1_M3/GPIO3_B6_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[11:8] = 4'h3
mac_rxdv_m0	I	VO_LCDC_D20/VO_EBC_VCOM/ETH0_RXCTL_M0/PDM1_CLK1_M2/DSMC_DATA13/FLEXBUS0_D5/UART1_TX_M2/UART10_RTSN_M0/GPIO3_A7_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[15:12] = 4'h3
mac_rxd3_m0	I	VO_LCDC_D1/VO_EBC_SDDO1/ETH0_RXD3_M0/SAI2_SDI_M2/DSMC_CSN3/FLEXBUS0_D12/FLEXBUS1_D15_M0/FLEXBUS0_CSN_M3/UART2_RTSN_M2/SPI4_CSN1_M1/I3C1_SDA_M2/PWM2_CH4_M3/GPIO3_D2_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[11:8] = 4'h3
mac_rxd2_m0	I	VO_LCDC_D0/VO_EBC_SDDO0/ETH0_RXD2_M0/SAI2_SDO_M2/DSMC_CSN0/FLEXBUS1_D2/UART2_CTSN_M2/I3C1_SCL_M2/PWM2_CH5_M3/GPIO3_D3_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[15:12] = 4'h3
mac_rxd1_m0	I	VO_LCDC_D18/VO_EBC_SDCE2/ETH0_RXD1_M0/PDM1_CLK0_M2/DSMC_DATA12/FLEXBUS0_D4/UART10_TX_M0/SPI4_CSN0_M1/PWM1_CH3_M3/GPIO3_B1_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[7:4] = 4'h3
mac_rxd0_m0	I	VO_LCDC_D17/VO_EBC_SDCE1/ETH0_RXD0_M0/PDM1_SDI1_M2/DSMC_DATA11/FLEXBUS0_D3/UART9_RX_M1/I2C8_SDA_M3/GPIO3_B2_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[11:8] = 4'h3
mac_rxclk_m0	I	VO_LCDC_D2/VO_EBC_SDDO2/ETH0_RXCLK_M0/SAI2_MCLK_M2/DSMC_CSN2/FLEXBUS0_D11/FLEXBUS1_CSN_M2/SPI4_CLK_M1/I3C1_SDA_PU_M2/GPIO3_D1_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[7:4] = 4'h3
mac_ppstrig_m0	I	VO_LCDC_D12/VO_EBC_SDDO12/ETH0_PPSTRIG_M0/SAI1_SDI0_M1/DSMC_DQS0/FLEXBUS1_D10/FLEXBUS1_CSN_M0/UART2_RX_M2/UART3_CTSN_M1/I2C4_SDA_M3/GPIO3_B7_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[15:12] = 4'h3
mac_ppsclk_m0	O	VO_LCDC_D11/VO_EBC_SDDO11/ETH0_PPSCLK_M0/SAI1_SDO3_M1/DSMC_DATA7/FLEXBUS1_D9/UART2_TX_M2/UART3_RTSN_M1/I2C4_SCL_M3/GPIO3_C0_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[3:0] = 4'h3

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mac_ptprefclk_m0	I	VO_LCDC_D10/VO_EBC_SDDO10/ETH0_PTP_REFCLK_M0/SAI1_SDO2_M1/DSMC_DATA6/FLEXBUS1_D8/UART11_RX_M0/SPI2_MISO_M2/I2C5_SDA_M3/CAN0_RX_M3/GPIO3_C1_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[7:4] = 4'h3
eth0_refclko25m_m0	O	VO_LCDC_D23/VO_EBC_SDSHR/ETH_CLK0_25M_OUT_M0/SAI4_SDI_M1/DSMC_RDYN/FLEXBUS1_D11/FLEXBUS0_CSN_M0/UART1_CTSN_M2/SPI2_CLK_M2/PWM1_CH0_M3/GPIO3_A4_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[3:0] = 4'h3
mac_mdio_m0	I/O	VO_LCDC_D22/VO_EBC_GDSP/ETH0_MDIO_M0/PDM1_SDI3_M2/DSMC_DATA15/FLEXBUS0_D7/UART1_RTSN_M2/SPI2_CSN1_M2/PWM1_CH1_M3/GPIO3_A5_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[7:4] = 4'h3
mac_mdc_m0	O	VO_LCDC_D21/VO_EBC_GDOE/ETH0_MDC_M0/PDM1_SDI2_M2/DSMC_DATA14/FLEXBUS0_D6/UART1_RX_M2/UART10_CTSN_M0/PWM1_CH2_M3/GPIO3_A6_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[11:8] = 4'h3
RMII/RGMII M1 Interface			
mac_clk_m1	I/O	CAM_CLK1_OUT_M1/ETH_CLK1_25M_OUT_M0/ETH0_MCLK_M1/SAI3_MCLK_M2/SPDIF_RX0_M2/UART9_RTSN_M0/I3C1_SDA_PU_M0/PWM2_CH6_M2/GPIO2_D6_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[11:8] = 4'h3
mac_txen_m1	O	VI_CIF_D14/SDMMC1_D1_M1/ETH0_TXCTL_M1/SAI0_SDO1_M0/UART8_RX_M1/I2C4_SDA_M2/GPIO2_A7_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[15:12] = 4'h3
mac_txd3_m1	O	VI_CIF_D11/SDMMC1_CMD_M1/ETH0_TXD3_M1/SAI0_SDI2_M0/PDM0_SDI1_M3/UART1_CTSN_M1/SPI4_CSN0_M3/PCIE0_CLKREQN_M0/GPIO2_B2_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[11:8] = 4'h3
mac_txd2_m1	O	VI_CIF_D9/SDMMC1_PWREN_M1/ETH0_TXD2_M1/SAI0_SDI3_M0/PDM0_SDI0_M3/UART7_CTSN_M0/SPI4_MOSI_M3/SATA0_ACTLED_M0/GPIO2_B4_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[3:0] = 4'h3
mac_txd1_m1	O	VI_CIF_D13/SDMMC1_D2_M1/ETH0_TXD1_M1/SAI0_SDI0_M0/PDM0_SDI3_M3/UART1_TX_M1/GPIO2_B0_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[3:0] = 4'h3
mac_txd0_m1	O	VI_CIF_D12/SDMMC1_D3_M1/ETH0_TXD0_M1/SAI0_SDI1_M0/PDM0_SDI2_M3/UART1_RX_M1/GPIO2_B1_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[7:4] = 4'h3
mac_txclk_m1	O	VI_CIF_D10/SDMMC1_CLK_M1/ETH0_TXCLK_M1/SAI0_SDO2_M0/PDM0_CLK1_M3/UART1_RTSN_M1/SPI4_CLK_M3/PCIE1_CLKREQN_M0/GPIO2_B3_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[15:12] = 4'h3
mac_rxdv_m1	I	VI_CIF_CLKO/ETH1_PPSCLK_M0/ETH0_RXCTL_M1/SAI3_SDO_M2/SPDIF_RX1_M1/UART3_CTSN_M0/SPI3_MISO_M0/CAN1_TX_M3/MIPI_TE_M1/GPIO3_A2_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[11:8] = 4'h3

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mac_rxd3_m1	I	VI_CIF_D7/ETH1_PTP_REFCLK_M1/ETH0_RXD3_M1/SAI0_SCLK_M0/UART7_TX_M0/UART8_RTSN_M1/I2C8_SCL_M2/GPIO2_B6_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[11:8] = 4'h3
mac_rxd2_m1	I	VI_CIF_D6/ETH0_RXD2_M1/SAI0_LRCK_M0/UART7_RX_M0/UART8_CTSN_M1/I2C8_SDA_M2/GPIO2_B7_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[15:12] = 4'h3
mac_rxd1_m1	I	VI_CIF_CLKI/ETH1_PTP_REFCLK_M0/ETH0_RXD1_M1/SAI3_SDI_M2/SPDIF_TX1_M1/UART3_RTSN_M0/SPI3_CSN0_M0/CAN1_RX_M3/GPIO3_A3_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[15:12] = 4'h3
mac_rxd0_m1	I	VI_CIF_D15/SDMMC1_D0_M1/ETH0_RXD0_M1/SAI0_SDO0_M0/UART8_TX_M1/SPI4_CSN1_M3/I2C4_SCL_M2/GPIO2_A6_d	TOP_IOC_GPIO2A_IOMUX_SEL_H[11:8] = 4'h3
mac_rxclk_m1	I	VI_CIF_D8/SDMMC1_DETN_M1/ETH0_RXCLK_M1/SAI0_MCLK_M0/PDM0_CLK0_M3/UART7_RTSN_M0/SPI4_MISO_M3/SATA1_ACTLED_M0/GPIO2_B5_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[7:4] = 4'h3
mac_ppstrig_m1	I	VI_CIF_D3/ETH1_RXCLK_M0/ETH0_PPSTRIG_M1/SAI2_SCLK_M1/PDM1_SDI2_M0/UART11_CTSN_M1/SPI1_MOSI_M1/PWM1_CH2_M2/GPIO2_C2_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[11:8] = 4'h3
mac_ppsclk_m1	O	VI_CIF_D4/ETH1_RXD3_M0/ETH0_PPSCLK_M1/SAI2_MCLK_M1/PDM1_CLK1_M0/UART9_TX_M0/SPI1_CSN1_M1/PWM1_CH1_M2/GPIO2_C1_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[7:4] = 4'h3
mac_ptprefclk_m1	I	VI_CIF_D5/ETH1_RXD2_M0/ETH0_PTP_REFCLK_M1/PDM1_SDI1_M0/UART9_RX_M0/PWM1_CH0_M2/GPIO2_C0_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[3:0] = 4'h3
eth0_refclko25m_m1	O	CAM_CLK2_OUT_M1/ETH1_MCLK_M0/ETH_CLK0_25M_OUT_M1/SAI0_SDO3_M0/SPDIF_TX0_M2/UART9_CTSN_M0/SPI3_CSN1_M0/PWM2_CH7_M2/GPIO2_D7_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[15:12] = 4'h3
mac_mdio_m1	I/O	VI_CIF_HREF/ETH0_MDIO_M1/SAI3_SCLK_M2/UART3_TX_M0/SPI3_CLK_M0/I2C7_SCL_M1/GPIO3_A0_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[3:0] = 4'h3
mac_mdc_m1	O	VI_CIF_VSYNC/ETH1_PPSTRIG_M0/ETH0_MDC_M1/SAI3_LRCK_M2/UART3_RX_M0/SPI3_MOSI_M0/I2C7_SDA_M1/GPIO3_A1_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[7:4] = 4'h3

Table 8-4 GMAC1 Interface

Module Pin	Direction	Pad Name	IOMUX Setting
RMII/RGMII M0 Interface			
mac_clk_m0	I/O	CAM_CLK2_OUT_M1/ETH1_MCLK_M0/ETH_CLK0_25M_OUT_M1/SAI0_SDO3_M0/SPDIF_TX0_M2/UART9_CTSN_M0/SPI3_CSN1_M0/PWM2_CH7_M2/GPIO2_D7_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[15:12] = 4'h2
mac_txen_m0	O	ETH1_TXCTL_M0/SAI4_SDI_M3/UART4_TX_M0/I2C6_SCL_M2/PWM2_CH0_M2/GPIO2_D0_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[3:0] = 4'h2

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mac_txd3_m0	O	VI_CIF_D1/ETH1_TXD3_M0/SAI2_SDO_M1/PDM1_SDI0_M0/UART11_TX_M1/SPI1_CSN0_M1/PWM1_CH3_M2/GPIO2_C4_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[3:0] = 4'h2
mac_txd2_m0	O	VI_CIF_D2/ETH1_TXD2_M0/SAI2_LRCK_M1/PDM1_SDI3_M0/UART11_RTSN_M1/SPI1_MISO_M1/PWM0_CH0_M2/GPIO2_C3_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[15:12] = 4'h2
mac_txd1_m0	O	ETH1_TXD1_M0/SAI4_LRCK_M3/UART4_RTSN_M0/I2C5_SDA_M2/PWM0_CH1_M2/GPIO2_C7_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[15:12] = 4'h2
mac_txd0_m0	O	ETH1_TXD0_M0/SAI4_SCLK_M3/UART4_CTSN_M0/I2C5_SCL_M2/PWM1_CH5_M2/GPIO2_C6_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[11:8] = 4'h2
mac_txclk_m0	O	VI_CIF_D0/ETH1_TXCLK_M0/SAI2_SDI_M1/PDM1_CLK0_M0/UART11_RX_M1/SPI1_CLK_M1/PWM1_CH4_M2/GPIO2_C5_d	TOP_IOC_GPIO2C_IOMUX_SEL_H[7:4] = 4'h2
mac_rxdv_m0	I	ETH1_RXCTL_M0/UART6_RX_M1/I3C1_SDA_M0/PWM2_CH3_M2/GPIO2_D3_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[15:12] = 4'h2
mac_rxd3_m0	I	VI_CIF_D4/ETH1_RXD3_M0/ETH0_PPSCLK_M1/SAI2_MCLK_M1/PDM1_CLK1_M0/UART9_TX_M0/SPI1_CSN1_M1/PWM1_CH1_M2/GPIO2_C1_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[7:4] = 4'h2
mac_rxd2_m0	I	VI_CIF_D5/ETH1_RXD2_M0/ETH0_PTP_REFCLK_M1/PDM1_SDI1_M0/UART9_RX_M0/PWM1_CH0_M2/GPIO2_C0_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[3:0] = 4'h2
mac_rxd1_m0	I	CAM_CLK0_OUT_M1/ETH1_RXD1_M0/SAI4_MCLK_M3/UART6_TX_M1/I3C1_SCL_M0/PWM2_CH2_M2/GPIO2_D2_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[11:8] = 4'h2
mac_rxd0_m0	I	ETH1_RXD0_M0/SAI4_SDO_M3/UART4_RX_M0/I2C6_SDA_M2/PWM2_CH1_M2/GPIO2_D1_d	TOP_IOC_GPIO2D_IOMUX_SEL_L[7:4] = 4'h2
mac_rxclk_m0	I	VI_CIF_D3/ETH1_RXCLK_M0/ETH0_PPSTRIG_M1/SAI2_SCLK_M1/PDM1_SDI2_M0/UART11_CTSN_M1/SPI1_MOSI_M1/PWM1_CH2_M2/GPIO2_C2_d	TOP_IOC_GPIO2C_IOMUX_SEL_L[11:18] = 4'h2
mac_ppstrig_m0	I	VI_CIF_VSYNC/ETH1_PPSTRIG_M0/ETH0_MDC_M1/SAI3_LRCK_M2/UART3_RX_M0/SPI3_MOSI_M0/I2C7_SDA_M1/GPIO3_A1_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[7:4] = 4'h2
mac_ppsclk_m0	O	VI_CIF_CLKO/ETH1_PPSCLK_M0/ETH0_RXCTL_M1/SAI3_SDO_M2/SPDIF_RX1_M1/UART3_CTSN_M0/SPI3_MISO_M0/CAN1_TX_M3/MIPI_TE_M1/GPIO3_A2_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[11:8] = 4'h2
mac_ptprefclk_m0	I	VI_CIF_CLKI/ETH1_PTP_REFCLK_M0/ETH0_RXD1_M1/SAI3_SDI_M2/SPDIF_TX1_M1/UART3_RTSN_M0/SPI3_CSN0_M0/CAN1_RX_M3/GPIO3_A3_d	TOP_IOC_GPIO3A_IOMUX_SEL_L[15:12] = 4'h2
eth1_refclko25m_m0	O	CAM_CLK1_OUT_M1/ETH_CLK1_25M_OUT_M0/ETH0_MCLK_M1/SAI3_MCLK_M2/SPDIF_RX0_M2/UART9_RTSN	TOP_IOC_GPIO2D_IOMUX_SEL_H[11:8] = 4'h2

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		_M0/I3C1_SDA_PU_M0/PWM2_CH6_M2/GPIO2_D6_d	
mac_mdio_m0	I/O	ISP_FLASH_TRIGOUT_M0/ETH1_MDIO_M0/UART6_CTSN_M1/I2C9_SCL_M2/PWM2_CH5_M2/GPIO2_D5_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[7:4] = 4'h2
mac_mdc_m0	O	ISP_PRELIGHT_TRIG_M0/ETH1_MDC_M0/UART6_RTSN_M1/I2C9_SDA_M2/PWM2_CH4_M2/GPIO2_D4_d	TOP_IOC_GPIO2D_IOMUX_SEL_H[3:0] = 4'h2
RMII/RGMII M1 Interface			
mac_clk_m1	I/O	ETH1_MCLK_M1/SAI2_MCLK_M0/PDM0_SDI3_M2/SPDIF_RX1_M2/UART10_RTSN_M1/I2C5_SCL_M1/GPIO1_D4_d	TOP_IOC_GPIO1D_IOMUX_SEL_H[3:0] = 4'h1
mac_txen_m1	O	ETH1_TXCTL_M1/FSPI1_D2_M1/PDM0_SDI0_M2/UART2_TX_M0/I2C8_SCL_M1/SATA_CPPOD/GPIO1_C6_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[11:8] = 4'h1
mac_txd3_m1	O	ETH1_TXD3_M1/SDMMC1_CMD_M0/PDM0_SDI2_M2/UART3_TX_M2/SPI1_CSN1_M0/PWM0_CH0_M1/GPIO1_C0_d	TOP_IOC_GPIO1C_IOMUX_SEL_L[3:0] = 4'h1
mac_txd2_m1	O	ETH1_TXD2_M1/SDMMC1_D3_M0/SAI3_SDI_M1/UART3_RTSN_M2/SPI1_CSN0_M0/GPIO1_B7_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[15:12] = 4'h1
mac_txd1_m1	O	ETH1_TXD1_M1/FSPI1_D1_M1/UART4_RX_M1/UART2_CTSN_M0/SPI2_MISO_M1/PCIE1_BUTTONRSTN/GPIO1_C5_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[7:4] = 4'h1
mac_txd0_m1	O	ETH1_TXD0_M1/FSPI1_D0_M1/UART4_TX_M1/UART2_RTSN_M0/SPI2_MOSI_M1/PCIE0_BUTTONRSTN/GPIO1_C4_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[3:0] = 4'h1
mac_txclk_m1	O	ETH1_TXCLK_M1/SDMMC1_CLK_M0/SAI3_MCLK_M1/PDM0_CLK0_M2/UART3_RX_M2/GPIO1_C1_d	TOP_IOC_GPIO1C_IOMUX_SEL_L[7:4] = 4'h1
mac_rxdv_m1	I	ETH1_RXCTL_M1/SAI2_SCLK_M0/UART10_RX_M1/I3C0_SDA_PU_M1/GPIO1_D1_d	TOP_IOC_GPIO1D_IOMUX_SEL_L[7:4] = 4'h1
mac_rxd3_m1	I	ETH1_RXD3_M1/SDMMC1_D1_M0/SAI3_LRCK_M1/I2C9_SCL_M1/SPI1_MOSI_M0/PWM1_CH1_M1/GPIO1_B5_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[7:4] = 4'h1
mac_rxd2_m1	I	ETH1_RXD2_M1/SDMMC1_D0_M0/SAI3_SCLK_M1/I2C9_SDA_M1/SPI1_CLK_M0/PCIE1_CLKREQN_M1/PWM1_CH0_M1/GPIO1_B4_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[3:0] = 4'h1
mac_rxd1_m1	I	ETH1_RXD1_M1/SAI2_SDO_M0/UART10_TX_M1/GPIO1_D0_d	TOP_IOC_GPIO1D_IOMUX_SEL_L[3:0] = 4'h1
mac_rxd0_m1	I	ETH1_RXD0_M1/FSPI1_D3_M1/PDM0_SDI1_M2/UART2_RX_M0/I2C8_SDA_M1/SATA_CPDET/GPIO1_C7_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[15:12] = 4'h1
mac_rxclk_m1	I	ETH1_RXCLK_M1/SDMMC1_D2_M0/SAI3_SDO_M1/UART3_CTSN_M2/SPI1_MISO_M0/PCIE0_CLKREQN_M1/GPIO1_B6_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[11:8] = 4'h1
mac_ppstrig_m1	I	ETH1_PPSTRIG_M1/SDMMC1_DETN_M0/FSPI1_CSN0_M1/UART4_CTSN_M	TOP_IOC_GPIO1C_IOMUX_SEL_L[15:12] = 4'h1

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		1/I2C6_SDA_M1/SPI2_CSN0_M1/GPIO1_C3_u	
mac_ppsclk_m1	O	ETH1_PPSCLK_M1/SDMMC1_PWREN_M0/FSPI1_RSTN_M1/FSPI1_CSN1_M1/UART4_RTSN_M1/I2C6_SCL_M1/SPI2_CSN1_M1/PWM1_CH2_M1/GPIO1_C2_u	TOP_IOC_GPIO1C_IOMUX_SEL_L[11:8] = 4'h1
mac_ptprefclk_m1	I	VI_CIF_D7/ETH1_PTP_REFCLK_M1/ETH0_RXD3_M1/SAI0_SCLK_M0/UART7_TX_M0/UART8_RTSN_M1/I2C8_SCL_M2/GPIO2_B6_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[11:8] = 4'h2
eth1_refclko25m_m1	O	ETH_CLK1_25M_OUT_M1/FSPI1_CLK_M1/PDM0_CLK1_M2/SPDIF_TX1_M2/UART10_CTSN_M1/I2C5_SDA_M1/SPI2_CLK_M1/SATA_MPSWIT/CLK1_32K_OUT/GPIO1_D5_d	TOP_IOC_GPIO1D_IOMUX_SEL_H[7:4] = 4'h1
mac_mdio_m1	I/O	ETH1_MDIO_M1/SAI2_SDI_M0/I3C0_SDA_M1/PWM1_CH4_M1/GPIO1_D3_d	TOP_IOC_GPIO1D_IOMUX_SEL_L[15:12] = 4'h1
mac_mdc_m1	O	ETH1_MDC_M1/SAI2_LRCK_M0/I3C0_SCL_M1/PWM1_CH3_M1/GPIO1_D2_d	TOP_IOC_GPIO1D_IOMUX_SEL_L[11:8] = 4'h1

8.6 Application Note

8.6.1 Descriptors

The DMA engine uses descriptors to efficiently move data from source to destination with minimal application CPU intervention. The DMA is designed for packet-oriented data transfers such as packets in Ethernet. The DMA controller can be programmed to interrupt the application CPU for situations such as Packet Transmit and Receive Transfer completion, and other normal or error conditions.

The DMA and the application communicate through the following two data structures:

- Control and Status registers (CSR)
- Descriptor lists and data buffers

The base address of each list is written to the respective Tx Descriptor List Address register and Rx Descriptor List Address register. The descriptor list is forward linked and the next descriptor is always considered at a fixed offset to the current one. The offset is controlled by the DSL field of DMA_Ch[n]_Control register. The number of descriptors in the list is programmed in the respective Tx (or Rx) Descriptor Ring Length register. Once the DMA processes the last descriptor in the list, it automatically jumps back to the descriptor in the List Address register to create a descriptor ring.

The descriptor lists reside in the physical memory address space of the application. Each descriptor can point to a maximum of two buffers in the system memory. This enables two buffers to be used, physically addressed, rather than contiguous buffers in memory.

A data buffer resides in the application physical memory space and consists of an entire packet or part of a packet but cannot exceed a single packet. Buffers contain only data. Buffer status is maintained in the descriptor. Data chaining refers to packets that span multiple data buffers. However, a single descriptor cannot span multiple packets. The DMA skips to the data buffer of next packet when EOP is detected.

The GMAC supports the following two types of descriptors:

- Normal Descriptor: Normal descriptors are used for packet data and to provide control information applicable to the packets to be transmitted
- Context Descriptor: Context descriptors are used to provide control information applicable to the packet to be transmitted

The GMAC supports the ring structure for the DMA descriptor.

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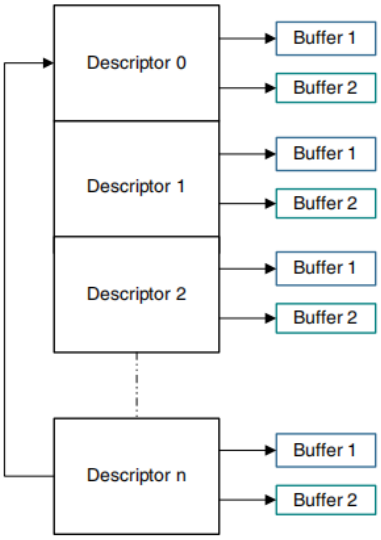


Fig. 8-10 Descriptor Ring Structure

In Ring structure, descriptors are separated by the Word, DWord, or LWord number programmed in the DSL field of the DMA_CH#_Control register. The application needs to program the total ring length, that is, the total number of descriptors in ring span in the following registers of a DMA channel:

- Transmit Descriptor Ring Length Register (DMA_CH#_TxDesc_Ring_Length)
- Receive Descriptor Ring Length Register (DMA_CH#_RxDesc_Ring_Length)

The Descriptor Tail Pointer Register contains the pointer to the descriptor address (N). The base address and the current descriptor pointer decide the address of the current descriptor that the DMA can process.

The descriptors up to one location less than the one indicated by the descriptor tail pointer (N – 1) are owned by the DMA. The DMA continues to process the descriptors until the following condition occurs:

Current Descriptor Pointer == Descriptor Tail Pointer

The DMA goes into the Suspend mode when this condition occurs. The application must perform a write to the Descriptor Tail pointer register and update the tail pointer so that the following condition is true:

Current Descriptor Pointer < Descriptor Tail Pointer

The DMA automatically wraps around the base address when the end of ring is reached. For descriptors owned by the application, the OWN bit of DES3 is reset to 0. For descriptors owned by the DMA, the OWN bit is set to 1. If the application has only one descriptor in the beginning, the application sets the last descriptor address (tail pointer) to Descriptor Base Address + 1. The DMA processes the first descriptor and then waits for the application to advance the tail pointer.

8.6.2 Transmit Descriptors

The DMA in GMAC requires at least one descriptor for a transmit packet. In addition to two buffers, two byte-count buffers, and two address pointers, the transmit descriptor has control fields which can be used to control the MAC operation on per-transmit packet basis. The Transmit Normal descriptor has two formats: Read format and Write-Back format.

8.6.3 Transmit Normal Descriptor (Read Format)

Table 8-5 TDES0 Normal Descriptor (Read Format)

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Bit	Name	Description
31:0	BUF1AP	Buffer 1 Address Pointer or TSO Header Address Pointer These bits indicate the physical address of Buffer 1. These bits indicate the TSO Header Address pointer when the following bits are set: ■ TSE bit of TDES3 ■ FD bit of TDES3

Table 8-6 TDES1 Normal Descriptor (Read Format)

Bit	Name	Description
31:0	BUF2AP	Buffer 2 or Buffer 1 Address Pointer This bit indicates the physical address of Buffer 2 when a descriptor ring structure is used. There is no limitation for the buffer address alignment. In 40- or 48-bit addressing mode, these bits indicate the most-significant 8- or 16- bits of the Buffer 1 Address Pointer.

Table 8-7 TDES2 Normal Descriptor (Read Format)

Bit	Name	Description
31	IOC	Interrupt on Completion This bit controls the setting of TI and ETI status bits in the DMA_CH#_Status register. When ETIC = 1 and TDES2[LD] = 0, this bit sets the ETI bit. When TDES3[LD] = 1, this bit sets the TI status bit.
30	TTSE/TMWD	Transmit Timestamp Enable or External TSO Memory Write Enable This bit enables the IEEE1588 time stamping for Transmit packet referenced by the descriptor, if TSE bit is not set. If TSE bit is set and external TSO memory is enabled, setting this bit disables external TSO memory writing for this packet.
29:16	B2L	Buffer 2 Length The driver sets this field. When set, this field indicates Buffer 2 length
15:14	VTIR	VLAN Tag Insertion or Replacement These bits request the MAC to perform VLAN tagging or untagging before transmitting the packets. The application must set the CRC Pad Control bits appropriately when VLAN Tag Insertion, Replacement, or Deletion is enabled for the packet. The following list describes the values of these bits: ■ 2'b00: Do not add a VLAN tag. ■ 2'b01: Remove the VLAN tag from the packets before transmission. This option should be used only with the VLAN packets. ■ 2'b10: Insert a VLAN tag with the tag value programmed in the MAC_VLAN_Incl register or context descriptor. ■ 2'b11: Replace the VLAN tag in packets with the tag value programmed in the MAC_VLAN_Incl register or context descriptor. This option should be used only with the VLAN packets. These bits are valid when the Enable SA and VLAN Insertion on Tx option is selected while configuring

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Bit	Name	Description
		the core
13:0	HL or B1L	Header Length or Buffer 1 Length For Header length only bits [9:0] are taken. The size 13:0 is applicable only when interpreting buffer 1 length. If the TCP Segmentation Offload feature is enabled through the TSE bit of TDES3, this field is equal to the header length. When the TSE bit is set in TDES3, the header length includes the length in bytes from Ethernet Source address till the end of the TCP header. The maximum header length supported for TSO feature is 1023 bytes. The maximum header length supported for TSO feature is 1023 bytes. If the TCP Segmentation Offload feature is not enabled, this field is equal to Buffer 1 length.

Table 8-8 TDES3 Normal Descriptor (Read Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit after it completes the transfer of data given in the associated buffer(s).
30	CTXT	Context Type This bit should be set to 1'b0 for normal descriptor.
29	FD	First Descriptor When this bit is set, it indicates that the buffer contains the first segment of a packet.
28	LD	Last Descriptor When this bit is set, it indicates that the buffer contains the last segment of the packet. When this bit is set, the B1L or B2L field should have a non-zero value.
27:26	CPC	CRC Pad Control This field controls the CRC and Pad Insertion for Tx packet. This field is valid only when the first descriptor bit (TDES3[29]) is set. The following list describes the values of Bits[27:26]: ■ 2'b00: CRC and Pad Insertion. The MAC appends the cyclic redundancy check (CRC) at the end of the transmitted packet of length greater than or equal to 60 bytes. The MAC automatically appends padding and CRC to a packet with length less than 60 bytes. ■ 2'b01: CRC Insertion (Disable Pad Insertion). The MAC appends the CRC at the end of the transmitted packet but it does not append padding. The application should ensure that the padding bytes are present in the packet being transferred from the Transmit Buffer, that is, the packet being transferred from the Transmit Buffer is of length greater than or equal to 60 bytes. ■ 2'b10: Disable CRC Insertion. The MAC does not append the CRC at the end of the transmitted packet. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer.

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Bit	Name	Description
		■ 2'b11: CRC Replacement. The MAC replaces the last four bytes of the transmitted packet with recalculated CRC bytes. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer. This field is valid only for the first descriptor. Note: When the TSE bit is set, the MAC ignores this field because the CRC and pad insertion is always done for segmentation.
25:23	SAIC	SA Insertion Control These bits request the MAC to add or replace the Source Address field in the Ethernet packet with the value given in the MAC Address 0 register. The application must set the CRC Pad Control bits appropriately when SA Insertion Control is enabled for the packet. Bit 25 specifies the MAC Address Register (1 or 0) value that is used for Source Address insertion or replacement. The following list describes the values of Bits[24:23]: ■ 2'b00: Do not include the source address ■ 2'b01: Include or insert the source address. For reliable transmission, the application must provide frames without source addresses. ■ 2'b10: Replace the source address. For reliable transmission, the application must provide frames with source addresses. ■ 2'b11: Reserved These bits are valid in the EQOS-DMA, EQOS-AXI, and EQOS-AHB configurations when the Enable SA and VLAN Insertion on Tx option is selected while configuring the core and when the First Segment control bit (TDES3 [29]) is set. This field is valid only for the first descriptor.
22:19	SLOTNUM or THL	SLOTNUM: Slot Number Control Bits in AV Mode These bits indicate the slot interval in which the data should be fetched from the corresponding buffers addressed by TDES0 or TDES1. When the Transmit descriptor is fetched, the DMA compares the slot number value in this field with the slot interval maintained in the RSN field DMA_CH#_Slot_Function_Control_Status. It fetches the data from the buffers only if a value matches. These bits are valid only for the AV channels. THL: TCP/UDP Header Length If the TSE bit is set, this field contains the length of the TCP/UDP header. The minimum value of this field must be 5 for TCP header. The value must be equal to 2 for UDP header. This field is valid only for the first descriptor.
18	TSE	TCP Segmentation Enable When this bit is set, the DMA performs the TCP/UDP segmentation or UDP fragmentation for a packet depending on the TSE_MODE[1:0] bit of the DMA_CH(#i)_Tx_Control Register. This bit is valid only if the FD bit is set.
17:16	CIC/TPL	Checksum Insertion Control or TCP Payload Length

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Bit	Name	Description
		These bits control the checksum calculation and insertion. The following list describes the bit encoding: ■ 2'b00: Checksum Insertion Disabled. ■ 2'b01: Only IP header checksum calculation and insertion are enabled. ■ 2'b10: IP header checksum and payload checksum calculation and insertion are enabled, but pseudo-header checksum is not calculated in hardware. ■ 2'b11: IP Header checksum and payload checksum calculation and insertion are enabled, and pseudo-header checksum is calculated in hardware. This field is valid when the Enable Transmit TCP/IP Checksum Offload option is selected and the TSE bit is reset. When the TSE bit is set, this field contains the upper bits [17:16] of the TCP Payload (or IP Payload for UDP fragmentation). This allows the TCP/UDP packet length field to be spanned across TDES3[17:0] to provide 256 KB packet length support. This field is valid only for the first descriptor.
15	TPL	Reserved or TCP Payload Length When the TSE bit is reset, this bit is reserved. When the TSE bit is set, this is Bit 15 of the TCP payload length [17:0]. This field is valid only when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected while configuring the core.
14:0	FL/TPL	Frame Length or TCP Payload Length This field is equal to the length of the packet to be transmitted in bytes. When the TSE bit is not set, this field is equal to the total length of the packet to be transmitted: Ethernet Header Length + TCP /IP Header Length – Preamble Length – SFD Length + Ethernet Payload Length When the TSE bit is set, this field is equal to the lower 15 bits of the TCP payload length in case of segmentation and IP payload in case of UDP fragmentation. In case of segmentation, this length does not include Ethernet header or TCP/UDP/IP header length. In case of fragmentation, this length does not include Ethernet header and IP header. When DWRR/WFQ algorithm is NOT enabled, value written into this field is not used when TSE = 0.

8.6.4 Transmit Normal Descriptor (Write-back Format)

The write-back format of the Transmit Descriptor includes timestamp low, timestamp high, OWN, and Status bits. The write-back format is applicable only for the last descriptor of the corresponding packet. The LD bit (TDES3[28]) is set in the descriptor where the DMA writes back the status and timestamp information for the corresponding Transmit packet. this format is only applicable to the last descriptor of a packet.

Table 8-9 TDES0 Normal Descriptor (Write-Back Format)

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Bit	Name	Description
31:0	TTSL	Transmit Packet Timestamp Low The DMA updates this field with least significant 32 bits of the timestamp captured for the corresponding Transmit packet. The DMA writes the timestamp only if TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and the Timestamp status (TTSS) bit is set

Table 8-10 TDES1 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:0	TTSH	Transmit Packet Timestamp High The DMA updates this field with the most significant 32 bits of the timestamp captured for corresponding transmit packet. The DMA writes the timestamp only if the TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and Timestamp status (TTSS) bit is set.

Table 8-11 TDES2 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:0	Reserved	Reserved

Table 8-12 TDES2 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit after it completes the transfer of data given in the associated buffer(s).
30	CTXT	Context Type This bit should be set to 1'b0 for normal descriptor.
29	FD	First Descriptor When this bit is set, it indicates that the buffer contains the first segment of a packet.
28	LD	Last Descriptor When this bit is set, it indicates that the buffer contains the last segment of the packet. When this bit is set, the B1L or B2L field should have a non-zero value.
27:24	Reserved	Reserved
23	DE	Descriptor Error When this bit is set, it indicates that the descriptor content is incorrect. The DMA sets this bit during write-back while closing the descriptor. Descriptor Errors can be: ■ Incorrect sequence from the context descriptor. For example, a location after the first descriptor for a packet ■ All 1s ■ CTXT, LD, and FD bits set to 1 Note 1: When Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1. When IOC bit in TDES2 of corresponding first

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Bit	Name	Description
		descriptor is set to 1, Transmit DMA will set the TI bit in the DMA_CH#_Status register. Note 2: Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent.
22:18	Reserved	Reserved
17	TTSS	Tx Timestamp Status This status bit indicates that a timestamp has been captured for the corresponding transmit packet. When this bit is set, TDES0 and TDES1 have timestamp values that were captured for the Transmit packet. This field is valid only when the Last Segment control bit (TDES3 [28]) in a descriptor is set. This bit is valid only when IEEE1588 timestamping feature is enabled; otherwise, it is reserved.
16	EUE	ECC Uncorrectable Error Status Indicates the ECC uncorrectable error in the TSO memory. Note: Uncorrectable error in Transmit FIFO memory is reported with (Bit 13) FF = 1. This is because, all such packets are flushed by GMAC.
15	ES	Error Summary This bit indicates the logical OR of the following bits: ■ TDES3[0]: IP Header Error ■ TDES3[14]: Jabber Timeout ■ TDES3[13]: Packet Flush ■ TDES3[12]: Payload Checksum Error ■ TDES3[11]: Loss of Carrier ■ TDES3[10]: No Carrier ■ TDES3[9]: Late Collision ■ TDES3[8]: Excessive Collision ■ TDES3[3]: Excessive Deferral ■ TDES3[2]: Underflow Error This bit is also set when EUE (bit 16) is set
14	JT	Jabber Timeout This bit indicates that the MAC transmitter has experienced a jabber time-out. This bit is set only when the JD bit of the MAC_Configuration register is not set.
13	PF	Packet Flushed This bit indicates that the DMA or MTL flushed the packet because of a software flush command given by the CPU.
12	PCE	Payload Checksum Error This bit indicates that the Checksum Offload engine had a failure and did not insert any checksum into the encapsulated TCP, UDP, or ICMP payload. This failure can be either because of insufficient bytes, as indicated by the Payload Length field of the IP Header or the MTL starting to forward the packet to the MAC transmitter in Store-and-Forward mode without the checksum having been calculated yet. This second error condition only occurs when the Transmit FIFO

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Bit	Name	Description
		depth is less than the length of the Ethernet packet being transmitted to avoid deadlock, the MTL starts forwarding the packet when the FIFO is full, even in the store-and-forward mode. This error can also occur when Bus Error is detected during packet transfer. When the Full Checksum Offload engine is not enabled, this bit is reserved.
11	LoC	Loss of Carrier This bit indicates that Loss of Carrier occurred during packet transmission (that is, the gmii_crs_i signal was inactive for one or more transmit clock periods during packet transmission). This is valid only for the packets transmitted without collision and when the MAC operates in the half-duplex mode.
10	NC	No Carrier This bit indicates that the carrier sense signal form the PHY was not asserted during transmission.
9	LC	Late Collision This bit indicates that packet transmission was aborted because a collision occurred after the collision window (64 byte times including Preamble in MII mode and 512 byte times including Preamble and Carrier Extension in GMII mode). This bit is not valid if Underflow Error is set.
8	EC	Excessive Collision This bit indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after first collision and the transmission of the packet is aborted.
7:4	CC	Collision Count This 4-bit counter value indicates the number of collisions occurred before the packet was transmitted. The count is not valid when the EC bit is set.
3	ED	Excessive Deferral This bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 bits times in 1000 Mbps mode or Jumbo Packet enabled mode) if DC bit is set in the MAC_Configuration register. When TBS is enabled in full duplex mode and this bit is set, it indicates that the frame has been dropped after the expiry time has reached.
2	UF	Underflow Error This bit indicates that the MAC aborted the packet because the data arrived late from the system memory. The underflow error can occur because of either of the following conditions: ■ The DMA encountered an empty Transmit Buffer while transmitting the packet ■ The application filled the MTL Tx FIFO slower than the MAC transmit rate The transmission process enter the suspended state and sets the underflow bit corresponding to a queue in the MTL_Interrupt_Status register.

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Bit	Name	Description
1	DB	Deferred Bit This bit indicates that the MAC deferred before transmitting because of presence of carrier. This bit is valid only in the half-duplex mode.
0	IHE	IP Header Error When IP Header Error is set, this bit indicates that the Checksum Offload engine detected an IP header error. This bit is valid only when Tx Checksum Offload is enabled. Otherwise, it is reserved. If COE detects an IP header error, it still inserts an IPv4 header checksum if the Ethernet Type field indicates an IPv4 payload. In full duplex mode, when EST/Qbv is enabled and this bit is set, it indicates the frame drop status due to Frame Size error or Schedule Error.

8.6.5 Programming Guide

8.6.5.1 Initializing DMA

Complete the following steps to initialize the DMA:
1. Provide a software reset. This resets all of the MAC internal registers and logic (bit-0 of DMA_Mode).
2. Wait for the completion of the reset process (poll bit 0 of the DMA_Mode, which is only cleared after the reset operation is completed).
3. Program the following fields to initialize the DMA_SysBus_Mode register:
a. AAL
b. Fixed burst or undefined burst
c. Burst mode values in case of AHB bus interface, OSR_LMT in case of AXI bus interface.
d. If fixed length value is enabled, select the maximum burst length possible on the AXI Bus (bits [7:1])
4. Create a descriptor list for transmit and receive. In addition, ensure that the descriptors are owned by DMA (set bit 31 of descriptor TDES3/RDES3). For more information about descriptors, see section "Descriptors".
5. Program the Transmit and Receive Ring length registers (DMA_CH(#i)_TxDesc_Ring_Length (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1) and DMA_CH(#i)_RxDesc_Ring_Length (for i = 0; i <= GMAC_NUM_DMA_RX_CH-1)). The ring length programmed must be at least 4.
6. Initialize receive and transmit descriptor list address with the base address of the transmit and receive descriptor (DMA_CH(#i)_TxDesc_List_Address (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1), DMA_CH(#i)_RxDesc_List_Address (for i = 0; i <= GMAC_NUM_DMA_RX_CH-1)). Also, program transmit and receive tail pointer registers indicating to the DMA about the available descriptors (DMA_CH(#i)_TxDesc_Tail_Pointer (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1) and DMA_CH(#i)_RxDesc_Tail_Pointer (for i = 0; i <= GMAC_NUM_DMA_RX_CH-1)).
7. Program the settings of the following registers for the parameters like maximum burst-length (PBL) initiated by DMA, descriptor skip lengths, OSP in case of TxDMA, RBSZ in case of RxDMA, and so on:
- DMA_CH(#i)_Control (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1)
- DMA_CH(#i)_TX_Control (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1)
- DMA_CH(#i)_RX_Control (for i = 0; i <= GMAC_NUM_DMA_RX_CH-1)

8. Enable the interrupts by programming the DMA_CH(#i)_Interrupt_Enable (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1) register.
9. Start the Receive and Transmit DMAs by setting SR (bit 0) of the DMA_CH(#i)_RX_Control (for i = 0; i <= GMAC_NUM_DMA_RX_CH-1) and ST (bit 0) of the DMA_CH(#i)_TX_Control (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1) register.
10. Repeat steps 4 to 9 for all the Tx DMA and Rx DMA channels selected in the hardware.

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8.6.5.2 Initializing MTL Registers

The Transaction Layer (MTL) registers must be initialized to establish the transmit and receive operating modes and commands.
Complete the following steps to initialize the MTL registers:
1. Program the Tx Scheduling (SCHALG) and Receive Arbitration Algorithm (RAA) fields in MTL_Operation_Mode to initialize the MTL operation in case of multiple Tx and Rx queues.
2. Program the Receive Queue to DMA mapping in MTL_RxQ_DMA_Map0 and MTL_RxQ_DMA_Map1 registers.
3. Program the following fields to initialize the mode of operation in the MTL_TxQ0_Operation_Mode register.
a. Transmit Store And Forward (TSF) or Transmit Threshold Control (TTC) in case of threshold mode
b. Transmit Queue Enable (TXQEN) to value 2'b10 to enable Transmit Queue0
c. Transmit Queue Size (TQS)
4. Program the following fields to initialize the mode of operation in the MTL_RxQ0_Operation_Mode register:
a. Receive Store and Forward (RSF) or RTC in case of Threshold mode
b. Flow Control Activation and De-activation thresholds for MTL Receive FIFO (RFA and RFD)
c. Error Packet and undersized good Packet forwarding enable (FEP and FUP)
d. Receive Queue Size (RQS)
5. Repeat previous two steps for all MTL Tx and Rx queues selected in the configuration.

8.6.5.3 Initializing MAC

The MAC configuration registers establish the operating mode of the MAC. These registers must be initialized before initializing the DMA.
The following MAC Initialization operations can be performed after DMA initialization. If the MAC initialization is completed before the DMA is configured, enable the MAC receiver (last step in the following sequence) only after the DMA is active. Otherwise, received frames fill the Rx FIFO and overflow.
1. Provide the MAC address registers: MAC_Address0_High and MAC_Address0_Low. If more than one MAC address is enabled in your configuration, program the MAC addresses appropriately.
2. Program the following fields to set the appropriate filters for the incoming frames in the MAC_Packet_Filter register:
a. Receive All
b. Promiscuous mode
c. Hash or Perfect Filter
d. Unicast, multicast, broadcast, and control frames filter settings
3. Program the following fields for proper flow control in the MAC_Q0_Tx_Flow_Ctrl register:
a. Pause time and other Pause frame control bits
b. Transmit Flow control bits
c. Flow Control Busy
4. Program the MAC_Interrupt_Enable register, as required, and if applicable, for your configuration.
5. Program the appropriate fields in the MAC_Configuration register. For ex: Inter-packet gap while transmission and jabber disable.
6. Set bit 0 and 1 in MAC_Configuration registers to start the MAC transmitter and receiver.

8.6.5.4 Performing Normal Receive and Transmit Operation

During normal operation of the GMAC, normal and transmit interrupts are read, descriptors polled, the DMA is suspended (if it does not own descriptors), and values of current host transmitter or receiver descriptor pointers are read for debugging.
For normal operation, complete the following steps:

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1. For normal transmit and receive interrupts, read the interrupt status. Then, poll the descriptors, reading the status of the descriptor owned by the Host (either transmit or receive).
2. Set appropriate values for the descriptors, ensuring that transmit and receive descriptors are owned by the DMA to resume the transmission and reception of data.
3. If the descriptors are not owned by the DMA (or no descriptor is available), the DMA goes into SUSPEND state. The transmission or reception can be resumed by freeing the descriptors and writing the descriptor tail pointer to Tx/Rx tail pointer register (DMA_CH[n]_TxDesc_Tail_Pointer and DMA_CH[n]_RxDesc_Tail_Pointer).
4. The values of the current host transmitter or receiver descriptor address pointer can be read for the debug process (DMA_CH[n]_Current_App_TxDesc and DMA_CH[n]_Current_App_RxDesc).
5. The values of the current host transmit buffer address pointer and receive buffer address pointer can be read for the debug process (Register DMA_CH[n]_Current_App_TxBuffer and DMA_CH[n]_Current_App_RxBuffer)

8.6.5.5 Stopping and Starting Transmission

Complete the following steps to pause the transmission for some time.
1. Disable the Transmit DMA (if applicable) by clearing Bit 0 (ST) of DMA_CH(#i)_TX_Control (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1) Register.
2. Wait for any previous frame transmissions to complete. You can check this by reading the appropriate bits of MTL_TxQ0_Debug Register (TRCSTS is not 01 and TXQSTS=0).
3. Disable the MAC transmitter and MAC receiver by clearing Bit (RE) and Bit 1(TE) of the MAC_Configuration Register.
4. Disable the Receive DMA (if applicable), after making sure that the data in the Rx FIFO is transferred to the system memory (by reading the appropriate bits of MTL_TxQ0_Debug Register, PRXQ=0 and RXQSTS=00).
5. Make sure that both Tx Queue and Rx Queue are empty (TXQSTS is 0 in MTL_TxQ0_Debug Register and RXQSTS is 0 in MTL_RxQ0_Debug Register).
6. To restart the operation, first start the DMAs, and then enable the MAC Transmitter and Receiver.

8.6.5.6 Initialization Guidelines for System Time Generation

You can enable the timestamp feature by setting Bit 0 of the MAC_Timestamp_Control Register. However, it is essential that the timestamp counter be initialized after this bit is set. Complete the following steps during GMAC initialization:
1. Mask the Timestamp Trigger interrupt by clearing the bit 16 of MAC_Interrupt_Enable Register.
2. Set Bit 0 of MAC_Timestamp_Control Register to enable timestamping.
3. Program MAC_Sub_Second_Increment Register based on the PTP clock frequency.
4. If you are using the Fine Correction approach, program MAC_Timestamp_Addend and set Bit 5 of MAC_Timestamp_Control Register.
5. Poll the MAC_Timestamp_Control Register until Bit 5 is cleared.
6. Program Bit 1 of MAC_Timestamp_Control Register to select the Fine Update method (if required).
7. Program MAC_System_Time_Seconds_Update Register and MAC_System_Time_Nanoseconds_Update Register with the appropriate time value.
8. Set Bit 2 in MAC_Timestamp_Control Register.
The timestamp counter starts operation as soon as it is initialized with the value written in the Timestamp Update registers. If one-step timestamping is enabled
a. To enable one-step timestamping, program Bit 27 of the TDES3 Context Descriptor.
b. Program registers MAC_Timestamp_Ingress_Asym_Corr and MAC_Timestamp_Egress_Asym_Corr to update the correction field in PDelay_Req PTP messages.
9. Enable the MAC receiver and transmitter for proper timestamping.

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8.6.5.7 Coarse Correction Method

To synchronize or update the system time in one process (coarse correction method), complete the following steps:
1. Set the offset (positive or negative) in the Timestamp Update registers (MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update).
2. Set Bit 3 (TSUPDT) of MAC_Timestamp_Control Register. The value in the Timestamp Update registers is added to or subtracted from the system time when the TSUPDT bit is cleared.

8.6.5.8 Programming Guidelines for TSO

The TCP Segmentation Offload (TSO) engine is used to offload the TCP segmentation functions to the hardware. To program the TSO, set the TSE bit to enable TCP packet segmentation, and program descriptor fields to enable TSO for the current packet. Complete the following steps to program TSO:
1. Program the TSE bit of corresponding DMA_CH[n]_Tx_Control register to enable TCP packet segmentation in that DMA.
2. In addition to the normal transfer descriptor setting, the following descriptor fields must be programmed to enable TSO for the current packet:
a. Enable TSE in Bit 18 of TDES3
b. Program the length of the un-segmented TCP/IP packet payload in bits [17:0] of TDES3 and the TCP header in bits [22:19] of TDES3.
c. Program the maximum size of the segment in MSS of DMA_CH[n]_Control register or MSS in the context descriptor. If MSS field is programmed in both DMA_CH[n]_Control register and in the context descriptor, the latest software programmed sequence is considered.
3. The header of the unsegmented TCP/IP packet should be in Buffer 1 of the first descriptor and this buffer must not hold any payload bytes. The payload is allocated to Buffer 2 and the buffers of the subsequent descriptors.

8.6.5.9 Programming Guidelines for Multi-Channel Multi-Queuing

Transmit

1. Program the Transmit queue size in the TQS field of MTL_TxQ[n]_Operation_Mode register. Based on the value programmed in the TQS field, the size of the queue is determined.
In the Transmit operation, the number of channels is equal to the number of the queues. Due to this reason, the Channel-to-Queue mapping is fixed.
2. For a queue to be used, the queue needs to be enabled in TXQEN in the corresponding MTL_TxQ[n]_Operation_Mode Register. In DMA configurations, the ST bit of DMA_CH[n]_Tx_Control Register and corresponding TXQEN in MTL_TxQ[n]_Operation Mode Register needs to be enabled.
3. The scheduling method needs to be programmed in SCHALG of MTL_Operation_Mode register.
4. Program the MTL_TxQ[n]_Quantum_Weight for DCB queue as per the selected algorithm. In case of CBS algorithm in AVB queues, the MTL_TxQ[n]_ETS_Control, MTL_TxQ[n]_SendSlopeCredit, MTL_TxQ[n]_HiCredit and MTL_TxQ[n]_LoCredit registers also need to be programmed as required.
5. If DCB is enabled and PFC function is required, program MAC_TxQ_Prty_Map0 Register to assign a fixed priority to the queue. This priority assigned is used for determining if the corresponding queue should stop transmitting packet based on the received PFC packet.

Receive

1. Program the Receive queue size in the RQS field of MTL_RxQ[n]_Operation_Mode Register. Based on the value programmed in RQS field, the size of the queue is determined.
2. Enable the Receive Queues 0 to 7 in the fields RXQ0EN to RXQ7EN in MAC_RxQ_Ctrl0 Register for AV or DCB. In DMA configurations, SR bit of statically or dynamically mapped DMA_CH[n]_Rx_Control Register and corresponding RXQ[n]_EN in MAC_RxQ_Ctrl0 Register needs to be enabled.

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3. The MAC routes the Rx packets to the Rx Queues based on following packet types:
   a. AV PTP Packets: Based on the programming of AVPTPQ in MAC_RxQ_Ctrl1 Register.
   b. AV Untagged Control packets: Based on the programming of AVCPQ in MAC_RxQ_Ctrl1 Register.
   c. Data Center Bridging (DCB) related Link Layer Discovery Protocol (LLDP) packets. Program
   DCBCPQ in MAC_RxQ_Ctrl1 Register to indicate to MAC which queue should get the DCB packets.
   d. VLAN Tag Priority field in VLAN Tagged packets: Program PSRQ7-0 of the MAC_RxQ_Ctrl2 and MAC_RxQ_Ctrl3 Register for the routing of tagged packets based on the USP (user Priority) field of the received packets to the Rx Queues 0 to 7.
   e. The AV tagged control and data packets are also routed based on PSRQ field of the MAC_RxQ_Ctrl2 and MAC_RxQ_Ctrl3 registers.
4. If multiple RX DMA channels are enabled, the following programming should be done for proper arbitration and mapping:
   a. Program the RAA field of MTL_Operation_Mode register to select the arbitration algorithm to decide which RxQ is read out from the RxFIFO memory.
   b. Program the MTL_RxQ[n]_Control to decide the weights and the packet arbitration for each RxQ.
   c. If static mapping is programmed in MTL_RxQ_DMA_Map[n] register (RXQ[n]DADMACH is reset to 0), bits RXQx2DMA and others need to be programmed to select the channel for which each queue is mapped.
   d. Set RXQ[n]DADMACH bit in MTL_RxQ_DMA_Map0 Register to select dynamic mapping of
   packets in each RxQueue.
   e. In dynamic channel mapping, the routing of a packet to a specific RxDMA channel is decided by the value of DCS field in the lowest MAC Address Register.

8.6.6 Transmit Context Descriptor

The context descriptor is used to provide the timestamps for one-step timestamp correction, VLAN Tag ID for VLAN insertion feature. The Transmit Context descriptor can be provided any time before a packet descriptor. The context is valid for the current packet and subsequent packets. The context descriptor is used to provide the timestamps for one-step timestamp correction and VLAN Tag ID for VLAN insertion feature. Write back is done on a context descriptor only to reset the OWN bit.

Table 8-13 TDES0 Context Descriptor

Bit	Name	Description
31:0	TTSL	Transmit Packet Timestamp Low For one-step correction, the driver can provide the lower 32 bits of timestamp in this descriptor word. The DMA uses this value as the low word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set.

Table 8-14 TDES1 Context Descriptor

Bit	Name	Description
31:0	TTSH	Transmit Packet Timestamp High For one-step correction, the driver can provide the upper 32 bits of timestamp in this descriptor. The DMA uses this value as the high word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set.

Table 8-15 TDES2 Context Descriptor

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Bit	Name	Description
31:16	IVT	Inner VLAN Tag When the IVLTV bit of TDES3 context descriptor is set and the TCMSSV and OSTC bits of TDES3 context descriptor are reset, TDES2[31:16] contains the inner VLAN Tag to be inserted in the subsequent Transmit packets.
15:14	Reserved	Reserved
13:0	MSS	Maximum Segment Size When the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected, the driver can provide maximum segment size in this field. This segment size is used while segmenting the TCP/IP payload. This field is valid only if the TCMSSV bit of TDES3 context descriptor is set and the OSTC bit of the TDES3 context descriptor is reset.

Table 8-16 TDES3 Context Descriptor

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit immediately after the read.
30	CTXT	Context Type This bit should be set to 1'b1 for Context descriptor.
29:28	Reserved	Reserved
27	OSTC	One-Step Timestamp Correction Enable When this bit is set, the DMA performs a one-step timestamp correction with reference to the timestamp values provided in TDES0 and TDES1.
26	TCMSSV	One-Step Timestamp Correction Input or MSS Valid When this bit and the OSTC bit are set, it indicates that the Timestamp Correction input provided in TDES0 and TDES1 is valid. When the OSTC bit is reset and this bit and the TSE bit of TDES3 are set in subsequent normal descriptor, it indicates that the MSS input in TDES2 is valid.
25:24	Reserved	Reserved
23	DE	Descriptor Error When this bit is set, it indicates that the descriptor content is incorrect.The DMA sets this bit during write-back while closing the context descriptor. Descriptor Errors can be: ■ Incorrect sequence from the context descriptor. For example, a location before the first descriptor for a packet ■ All 1s ■ CD, LD, and FD bits set to 1 Note 1: When Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1. When IOC bit in TDES2 of corresponding first descriptor is set to 1, Transmit DMA will set the TI bit in the DMA_CH#_Status Register. Note 2: Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might

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Bit	Name	Description
		be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent.
22:20	Reserved	Reserved
19:18	IVTIR	Inner VLAN Tag Insert or Replace When this bit is set, these bits request the MAC to perform Inner VLAN tagging or un-tagging before transmitting the packets. If the packet is modified for VLAN tags, the MAC automatically recalculates and replaces the CRC bytes. The following list describes the values of these bits: ■ 2'b00: Do not add the inner VLAN tag. ■ 2'b01: Remove the inner VLAN tag from the packets before transmission. This option should be used only with the VLAN frames. ■ 2'b10: Insert an inner VLAN tag with the tag value programmed in the MAC_Inner_VLAN_Incl register or context descriptor. ■ 2'b11: Replace the inner VLAN tag in packets with the tag value programmed in the MAC_Inner_VLAN_Incl register or context descriptor. This option should be used only with the VLAN frames. These bits are valid when the Enable SA and VLAN Insertion on Tx and Enable Double VLAN Processing options are selected.
17	IVLTV	Inner VLAN Tag Valid When this bit is set, it indicates that the IVT field of TDES2 is valid.
16	VLTV	VLAN Tag Valid When this bit is set, it indicates that the VT field of TDES3 is valid.
15:0	VT	VLAN Tag This field contains the VLAN Tag to be inserted or replaced in the packet. This field is used as VLAN Tag only when the VLTI bit of the MAC_VLAN_Incl register is reset.

8.6.7 Receive Descriptors

The DMA in GMAC attempts to read a descriptor only if the Tail Pointer is different from the Base Pointer or current pointer. It is recommended to have a descriptor ring with a length that can accommodate at least two complete packets received by the MAC. Otherwise, the performance of the DMA is impacted greatly because of the unavailability of the descriptors. In such situations, the RxFIFO in MTL becomes full and starts dropping packets.

The following Receive Descriptors are present:

- Normal descriptors
- Context descriptors

All RX descriptors are prepared by the software and given to the DMA as "Normal" Descriptors with the content as shown in Receive Normal Descriptor (Read Format). The DMA reads this descriptor and after transferring a received packet (or part of) to the buffers indicated by the descriptor, the Rx DMA will close the descriptor with the corresponding packet status. The format of this status is given in the "Receive Normal Descriptor (Write-Back Format)". For some packets, the normal descriptor bits are not enough to write the complete status. For such packets, the RX DMA writes the extended status to the next descriptor (without processing or using the Buffers/ Pointers embedded in that descriptor). The format and content of the descriptor write back is described in "Receive Context Descriptor".

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8.6.8 Receive Normal Descriptors(Read Format)

Table 8-17 TDES0 Normal Descriptor(Read Format)

Bit	Name	Description
31:0	BUF1AP	Header or Buffer 1 Address Pointer When the SPH bit of Control register of a channel is reset, these bits indicate the physical address of Buffer 1. When the SPH bit is set, these bits indicate the physical address of Header Buffer where the Rx DMA writes the L2/L3/L4 header bytes of the received packet. The application can program a byte-aligned address for this buffer which means that the LS bits of this field can be non-zero. However, while transferring the start of packet, the DMA performs a Write operation with RDES0[1:0] (or RDES0[2:0]/[3:0] in case of 64-/128-bit configuration) as zero. However, the packet data is shifted as per actual offset as given by buffer address pointer. If the address pointer points to a buffer where the middle or last part of the packet is stored, the DMA ignores the offset address and writes to the full location as indicated by the data-width.

Table 8-18 TDES1 Normal Descriptor(Read Format)

Bit	Name	Description
31:0	Reserved or BUF1AP	In 64-bit addressing mode, this field contains the most-significant 32 bits of the Buffer 1 Address Pointer. Otherwise, this field is reserved.

Table 8-19 TDES2 Normal Descriptor(Read Format)

Bit	Name	Description
31:0	Reserved or BUF1AP	In 64-bit addressing mode, this field contains the most-significant 32 bits of the Buffer 1 Address Pointer. Otherwise, this field is reserved.

Table 8-20 TDES3 Normal Descriptor(Read Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	IOC	Interrupt Enabled on Completion When this bit is set, an interrupt is issued to the application when the DMA closes this descriptor.
29:26	Reserved	Reserved
25	BUF2V	Buffer 2 Address Valid When this bit is set, it indicates to the DMA that the buffer 2 address specified in RDES2 is valid. The application must set this bit so that the DMA can use the address, to which the Buffer 2 address in RDES2 is pointing, to write received packet data.
24	BUF1V	Buffer 1 Address Valid

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Bit	Name	Description
		When set, this indicates to the DMA that the buffer 1 address specified in RDES1 is valid. The application must set this value if the address pointed to by Buffer 1 address in RDES1 can be used by the DMA to write received packet data.
23:0	Reserved	Reserved

8.6.9 Receive Normal Descriptors(Write-Back Format)

Table 8-21 TDES0 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31:16	IVT	Inner VLAN Tag This field contains the Inner VLAN tag of the received packet if the RS0V bit of RDES3 is set. This is valid only when Double VLAN tag processing and VLAN tag stripping are enabled.
15:0	OVT	Outer VLAN Tag This field contains the Outer VLAN tag of the received packet if the RS0V bit of RDES3 is set.

Table 8-22 TDES1 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31:16	OPC	OAM Sub-Type Code, or MAC Control Packet opcode OAM Sub-Type Code If Bits[18:16] of RDES3 are set to 3'b111, this field contains the OAM sub-type and code fields. MAC Control Packet opcode If Bits[18:16] of RDES3 are set to 3'b110, this field contains the MAC Control packet opcode field.
15	TD	Timestamp Dropped This bit indicates that the timestamp was captured for this packet but it got dropped in the MTL Rx FIFO because of overflow. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
14	TSA	Timestamp Available When Timestamp is present, this bit indicates that the timestamp value is available in a context descriptor word 2 (RDES2) and word 1(RDES1). This is valid only when the Last Descriptor bit (RDES3 [28]) is set. The context descriptor is written in the next descriptor just after the last normal descriptor for a packet.
13	PV	PTP Version This bit indicates that the received PTP message has the IEEE 1588 version 2 format. When this bit is reset, it indicates the IEEE 1588 version 1 format. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
12	PFT	PTP Packet Type This bit indicates that the PTP message is sent directly over Ethernet. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
11:8	PMT	PTP Message Type These bits are encoded to give the type of the message received: ■ 0000: No PTP message received ■ 0001: SYNC (all clock types)

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Bit	Name	Description
		■ 0010: Follow_Up (all clock types) ■ 0011: Delay_Req (all clock types) ■ 0100: Delay_Resp (all clock types) ■ 0101: Pdelay_Req (in peer-to-peer transparent clock) ■ 0110: Pdelay_Resp (in peer-to-peer transparent clock) ■ 0111: Pdelay_Resp_Follow_Up (in peer-to-peer transparent clock) ■ 1000: Announce ■ 1001: Management ■ 1010: Signaling ■ 1011–1110: Reserved ■ 1111: PTP packet with Reserved message type These bits are available only when you select the Timestamp feature.
7	IPCE	IP Payload Error When this bit is set, it indicates either of the following: ■ The 16-bit IP payload checksum (that is, the TCP, UDP, or ICMP checksum) calculated by the MAC does not match the corresponding checksum field in the received segment. ■ The TCP, UDP, or ICMP segment length does not match the payload length value in the IP Header field. ■ The TCP, UDP, or ICMP segment length is less than minimum allowed segment length for TCP, UDP, or ICMP. Bit 15 (ES) of RDES3 is not set when this bit is set.
6	IPCB	IP Checksum Bypassed This bit indicates that the checksum offload engine is bypassed. This bit is available when you select the Enable Receive TCP/IP Checksum Check feature.
5	IPV6	IPv6 header Present This bit indicates that an IPV6 header is detected. When the Enable Split Header Feature option is selected and the SPH bit of Control Register of a channel is set, the IPV6 header is available in the header buffer area to which RDES0 is pointing.
4	IPV4	IPV4 Header Present This bit indicates that an IPV4 header is detected. When the SPH bit of RDES3 is set, the IPV4 header is available in the header buffer area to which RDES0 is pointing.
3	IPHE	IP Header Error When this bit is set, it indicates either of the following: ■ The 16-bit IPv4 header checksum calculated by the MAC does not match the received checksum bytes. ■ The IP datagram version is not consistent with the Ethernet Type value. ■ Ethernet packet does not have the expected number of IP header bytes. This bit is valid when either Bit 5 or Bit 4 is set. This bit is available when you select the Enable Receive TCP/IP Checksum Check feature.
2:0	PT	Payload Type

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Bit	Name	Description
		These bits indicate the type of payload encapsulated in the IP datagram processed by the Receive Checksum Offload Engine (COE): ■ 3'b000: Unknown type or IP/AV payload not processed ■ 3'b001: UDP ■ 3'b010: TCP ■ 3'b011: ICMP ■ 3'b110: AV Tagged Data Packet ■ 3'b111: AV Tagged Control Packet ■ 3'b101: AV Untagged Control Packet ■ 3'b100: IGMP if IPV4 Header Present bit is set else DCB (LLDP) Control Packet If the COE does not process the payload of an IP datagram because there is an IP header error or fragmented IP, it sets these bits to 3'b000.

Table 8-23 TDES2 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31:29	L3L4FM	Layer 3 and Layer 4 Filter Number Matched These bits indicate the number of the Layer 3 and Layer 4 Filter that matched the received packet: ■ 000: Filter 0 ■ 001: Filter 1 ■ 010: Filter 2 ■ 011: Filter 3 ■ 100: Filter 4 ■ 101: Filter 5 ■ 110: Filter 6 ■ 111: Filter 7 This field is valid only when Bit 28 or Bit 27 is set high. When more than one filter matches, these bits give the number of lowest filter. Note: This status is not available when Flexible RX Parser is enabled.
28	L4FM	Layer 4 Filter Match When this bit is set, it indicates that the received packet matches one of the enabled Layer 4 Port Number fields. This status is given only when one of the following conditions is true: ■ Layer 3 fields are not enabled and all enabled Layer 4 fields match ■ All enabled Layer 3 and Layer 4 filter fields match When more than one filter matches, this bit gives the layer 4 filter status of filter indicated by Bits[31:29]. Note: This status is not available when Flexible RX Parser is enabled.
27	L3FM	Layer 3 Filter Match When this bit is set, it indicates that the received packet matches one of the enabled Layer 3 IP Address fields. This status is given only when one of the following conditions is true: ■ All enabled Layer 3 fields match and all enabled Layer 4 fields are bypassed ■ All enabled filter fields match When more than one filter matches, this bit gives the layer 3 filter status of filter indicated by Bits[31:29].

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Bit	Name	Description
		Note: This status is not available when Flexible RX Parser is enabled.
26:19	MADRM	MAC Address Match or Hash Value When the HF bit is reset, this field contains the MAC address register number that matched the Destination address of the received packet. This field is valid only if the DAF bit is reset. When the HF bit is set, this field contains the hash value computed by the MAC. A packet passes the hash filter when the bit corresponding to the hash value is set in the hash filter register. Note: This status is not available when Flexible RX Parser is enabled.
18	HF	Hash Filter Status When this bit is set, it indicates that the packet passed the MAC address hash filter. Bits[26:19] indicate the hash value. Note: This status is not available when Flexible RX Parser is enabled.
17	DAF/RXPI	Destination Address Filter Fail When Flexible RX Parser is disabled, and this bit is set, it indicates that the packet failed the DA Filter in the MAC. When Flexible RX Parser is enabled, this bit is set to indicate that the packet parsing is incomplete (RXPI) due to ECC error. Note: When this bit is set, ES bit of RDES3 is also set.
16	SAF/RXPD	SA Address Filter Fail When Flexible RX Parser is disabled, and this bit is set, it indicates that the packet failed the SA Filter in the MAC. When Flexible RX Parser is enabled, this bit is set to indicate that the packet is dropped (RXPD) by the parser. Note: When this bit is set, ES bit of RDES3 is also set.
15	OTS	VLAN Filter Status When set, this bit indicates that the VLAN Tag of the received packed passed the VLAN filter. This bit is valid only when GMAC_ERVFE is not enabled. If GMAC_ERVFE is enabled, the bit is redefined as Outer VLAN Tag Filter Status (OTS). This bit is valid for both Single and Double VLAN Tagged frames.
14	ITS	Inner VLAN Tag Filter Status (ITS) This bit is valid only when GMAC_ERVFE is enabled. This bit is valid only for Double VLAN Tagged frames, when Double VLAN Processing is enabled. For more information, see the Filter Status topic.
13:11	Reserved	Reserved
10	ARPNR	ARP Reply Not Generated When this bit is set, it indicates that the MAC did not generate the ARP Reply for received ARP Request packet. This bit is set when the MAC is busy transmitting ARP reply to earlier ARP request (only one ARP request is processed at a time).

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Bit	Name	Description
		This bit is reserved when the Enable IPv4 ARP Offload option is not selected.
9:0	HL	L3/L4 Header Length This field contains the length of the header of the packet split by the MAC at L3 or L4 header. boundary as identified by the MAC receiver. This field is valid only when the first descriptor bit is set (FD = 1). The header data is written to the Buffer 1 address of corresponding descriptor. If header length is zero, this field is not valid. It implies that the MAC did not identify and split the header. This field is valid when the Enable Split Header Feature option is selected.

Table 8-24 TDES3 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	CTXT	Receive Context Descriptor When this bit is set, it indicates that the current descriptor is a context type descriptor. The DMA writes 1'b0 to this bit for normal receive descriptor. When CTXT and FD bits are used together, {CTXT, FD} ■ 2'b00: Intermediate Descriptor ■ 2'b01: First Descriptor ■ 2'b10: Reserved ■ 2'b11: Descriptor Error (due to all 1s) Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data Receive DMA will set the CDE bit in DMA_CH#_Status register but not the RI bit even when IOC is set, as this is not marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data.
29	FD	First Descriptor When this bit is set, it indicates that this descriptor contains the first buffer of the packet. If the size of the first buffer is 0, the second buffer contains the beginning of the packet. If the size of the second buffer is also 0, the next descriptor contains the beginning of the packet. See the CTXT bit description for details of using the CTXT bit and FD bit together.
28	LD	Last Descriptor When this bit is set, it indicates that the buffers to which this descriptor is pointing are the last buffers of the packet.

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Bit	Name	Description
27	RS2V	Receive Status RDES2 Valid When this bit is set, it indicates that the status in RDES2 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
26	RS1V	Receive Status RDES1 Valid When this bit is set, it indicates that the status in RDES1 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
25	RS0V	Receive Status RDES0 Valid When this bit is set, it indicates that the status in RDES0 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
24	CE	CRC Error When this bit is set, it indicates that a Cyclic Redundancy Check (CRC) Error occurred on the received packet. This field is valid only when the LD bit of RDES3 is set.
23	GP	Giant Packet When this bit is set, it indicates that the packet length exceeds the specified maximum Ethernet size of 1518, 1522, or 2000 bytes (9018 or 9022 bytes if jumbo packet enable is set). Note: Giant packet indicates only the packet length. It does not cause any packet truncation.
22	RWT	Receive Watchdog Timeout When this bit is set, it indicates that the Receive Watchdog Timer has expired while receiving the current packet. The current packet is truncated after watchdog timeout.
21	OE	Overflow Error When this bit is set, it indicates that the received packet is damaged because of buffer overflow in Rx FIFO. Note: This bit is set only when the DMA transfers a partial packet to the application. This happens only when the Rx FIFO is operating in the threshold mode. In the store-and-forward mode, all partial packets are dropped completely in Rx FIFO.
20	RE	Receive Error When this bit is set, it indicates that the gmii_rxer_i signal is asserted while the gmii_rxdv_i signal is asserted during packet reception. This error also includes carrier extension error in the GMII and half-duplex mode. Error can be of less or no extension, or error (rxd!= 0f) during extension.
19	DE	Dribble Bit Error When this bit is set, it indicates that the received packet has a non-integer multiple of bytes (odd nibbles). This bit is valid only in the MII Mode.
18:16	LT	Length/Type Field This field indicates if the packet received is a length packet or a type packet. The encoding of the 3 bits is as follows: ■ 3'b000: The packet is a length packet ■ 3'b001: The packet is a type packet. ■ 3'b011: The packet is a ARP Request packet type

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Bit	Name	Description
		■ 3'b100: The packet is a type packet with VLAN Tag ■ 3'b101: The packet is a type packet with Double VLAN Tag ■ 3'b110: The packet is a MAC Control packet type ■ 3'b111: The packet is a OAM packet type ■ 3'b010: Reserved
15	ES	Error Summary When this bit is set, it indicates the logical OR of the following bits: ■ RDES3[24]: CRC Error ■ RDES3[19]: Dribble Error ■ RDES3[20]: Receive Error ■ RDES3[22]: Watchdog Timeout ■ RDES3[21]: Overflow Error ■ RDES3[23]: Giant Packet ■ RDES2[17]: Destination Address Filter Fail, when Flexible RX Parser is enabled ■ RDES2[16]: SA Address Filter Fail, when Flexible RX Parser is enabled This field is valid only when the LD bit of RDES3 is set.
14	PL	Packet Length These bits indicate the byte length of the received packet that was transferred to system memory (including CRC). This field is valid when the LD bit of RDES3 is set and Overflow Error bits are reset. The packet length also includes the two bytes appended to the Ethernet packet when IP checksum calculation is enabled and the received packet is not a MAC control packet. This field is valid when the LD bit of RDES3 is set. When the Last Descriptor and Error Summary bits are not set, this field indicates the accumulated number of bytes that have been transferred for the current packet.

8.6.10 Receive Context Descriptor

This descriptor is read-only for the application. Only the DMA can write to this descriptor. The context descriptor provides information about the extended status related to the last received packet. The Bit 30 of RDES3 indicates the context type descriptor.

Table 8-25 TDES0 Context Descriptor

Bit	Name	Description
31:0	RSTL	Receive Packet Timestamp Low The DMA updates this field with least significant 32 bits of the timestamp captured for corresponding Receive packet. When this field and the RTSH field of RDES1 show all-ones value, the timestamp must be considered as corrupt.

Table 8-26 TDES1 Context Descriptor

Bit	Name	Description
31:0	RSTH	Receive Packet Timestamp High The DMA updates this field with most significant 32 bits of the timestamp captured for corresponding receive packet. When this field and the RTSL field of

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Bit	Name	Description
		RDES0 show all-ones value, the timestamp must be considered as corrupt.

Table 8-27 TDES2 Context Descriptor

Bit	Name	Description
31:0	Reserved	Reserved

Table 8-28 TDES3 Context Descriptor

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	CTXT	Receive Context Descriptor When this bit is set, it indicates that the current descriptor is a context descriptor. The DMA writes 1'b1 to this bit for context descriptor. DMA writes 2’b11 to indicate a descriptor error due to all 1s. When CTXT and DE bits are used together, {CTXT, DE} ■ 2’b00: Reserved ■ 2’b01: Reserved ■ 2’b10: Context Descriptor ■ 2’b11: Descriptor Error Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data Receive DMA will set the CDE bit in DMA_CH#_Status register but not the RI bit even when IOC is set, as this is not marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data.
29	DE	Descriptor Error See the CTXT bit description for details of using theDE bit along with CTXT bit.
28:0	Reserved	Reserved

8.6.11 Clock Architecture

In RMII mode, reference clock and TX/RX clock can be from CRU or external OSC as following figure. The mux selecting rmii_speed is SDGMAC_GRF_GMAC_CON0[5]/SDGMAC_GRF_GMAC_CON1[5].

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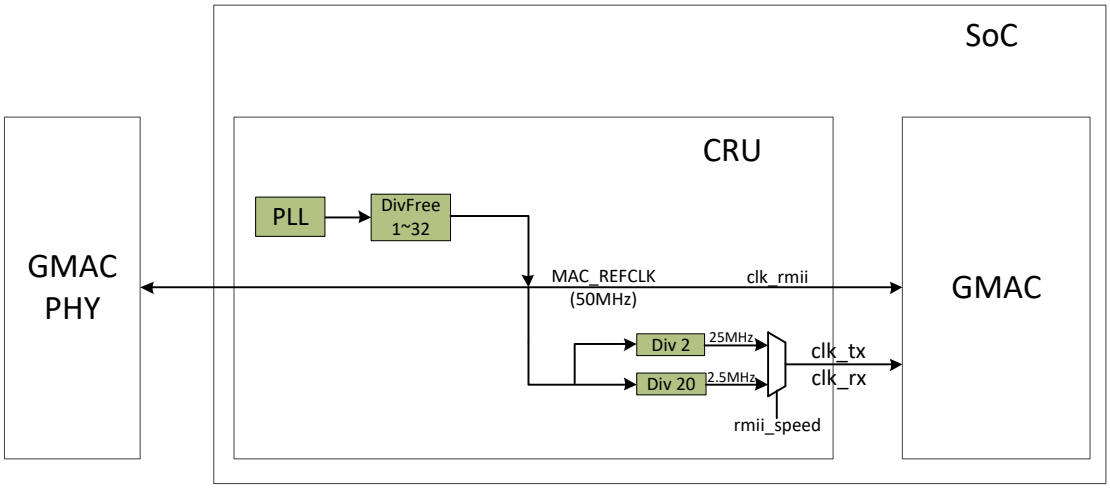


Fig. 8-11 RMII Clock Architecture When Clock Source From CRU

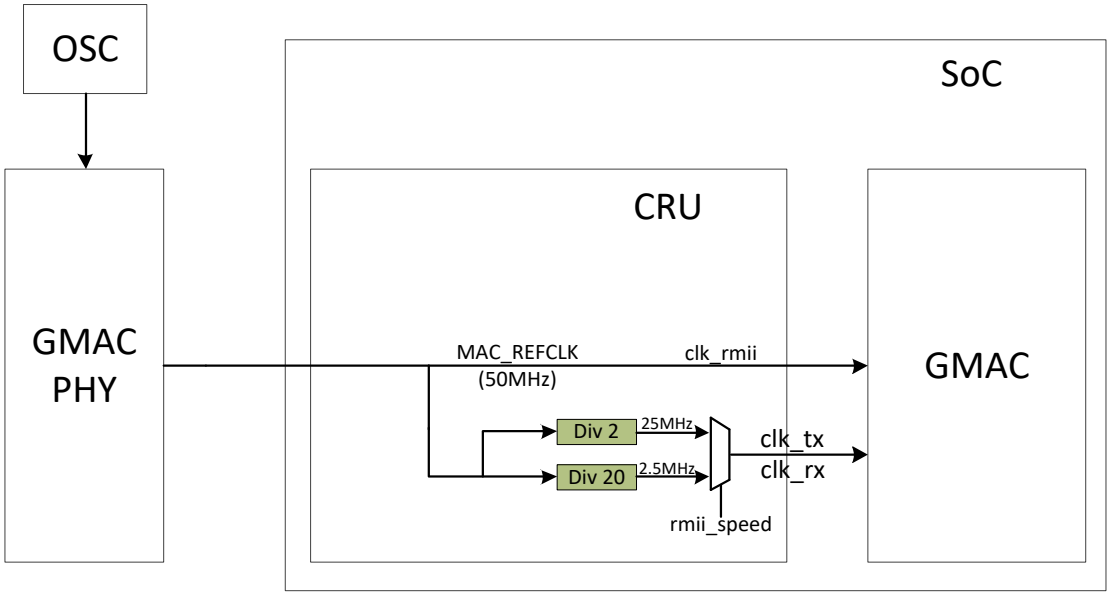


Fig. 8-12 RMII Clock Architecture When Clock Source From External OSC

In RGMII mode, clock architecture only supports that TX clock source is from CRU as following figure. In order to dynamically adjust the timing between TX/RX clocks with data, there are 4 sets of delayline which is integrated in TX and RX clock path. Please see the register VCCIO_IOC_MISC_CON2/3/4/5 about how to enable the delayline and configure the delay length. There are 100 delay elements in each delayline.

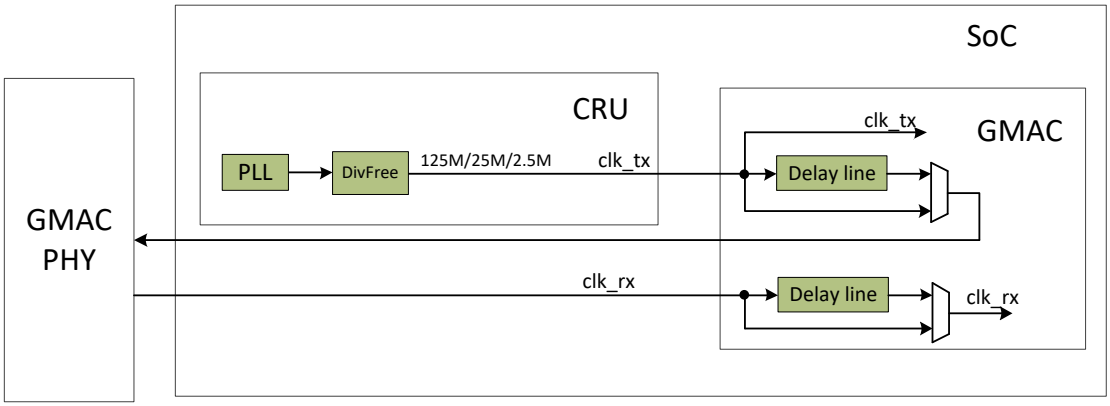


Fig. 8-13 RGMII Clock Architecture When Clock Source From CRU

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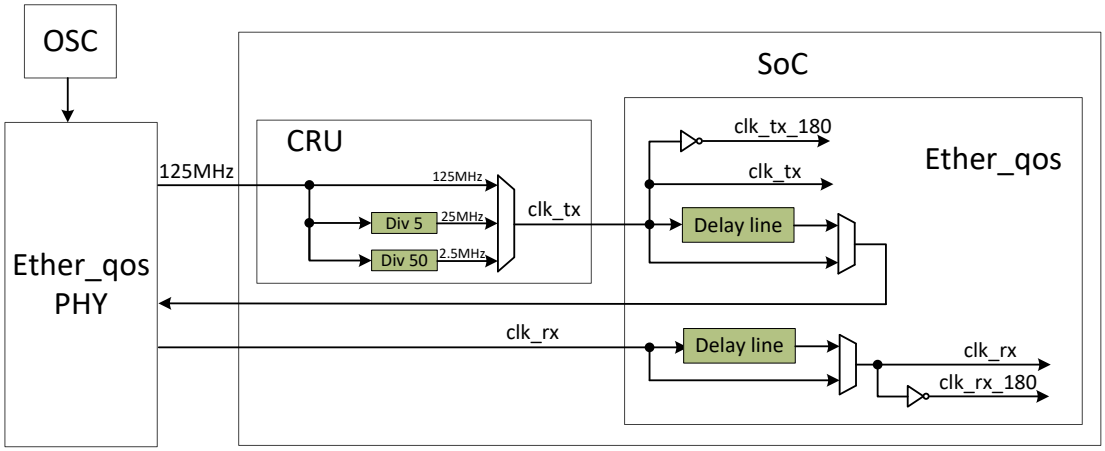


Fig. 8-14 RGMII Clock Architecture When Clock Source From External OSC

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Chapter 9 Process-Voltage-Temperature Monitor (PVTM)

9.1 Overview

The Process-Voltage-Temperature Monitor (PVTM) is used to monitor the chip performance variance caused by chip process, voltage and temperature.
PVTM supports the following features:

- A clock oscillation ring is integrated and used to generate a clock like signal, the frequency of this clock is determined by the cell delay value of clock oscillation ring circuit.
- A calculation logic is used to measure the frequency of the clock oscillation ring.
- Follow PVTM blocks are supported:
  - PMU_PVTM, used near PMU

9.2 Block Diagram

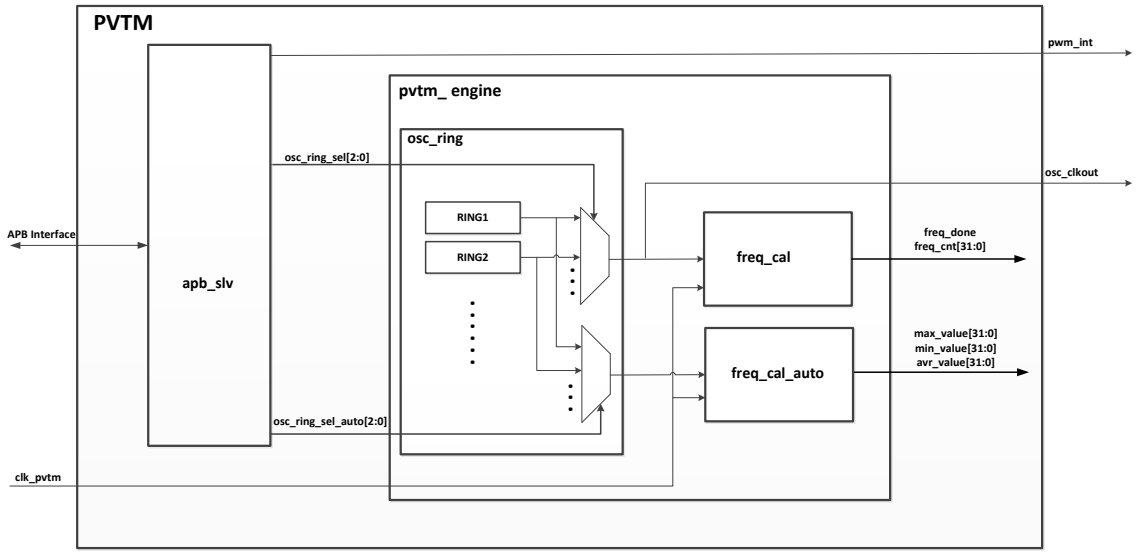


Fig. 9-1 PVTM Block Diagram

The PVTM include two main blocks:

- apb_slv

APB slave interface with 32-bit bus width.

- pvtm_engine

It is composed with inverters with odd number, which is used to generate a clock.
PMU_PVTM only supports one clock oscillation rings. The PMU_PVTM only support manual mode.

9.3 Function Description

9.3.1 Frequency Calculation

A clock is generated by the oscillation ring and a frequency fixed clock clk_pvtm is used to calculate the cycles of the clock. Supposing the time period is 1s, then the clock period of oscillation ring clock is T= 1/clock_counter(s), the cell delay value is T/2.
For manual mode, user can only get one frequency result for a calculation.
For auto mode, user can set the calculation times, and get the maximum, minimum and average frequency during calculation. It also support to generate an interrupt when the minimum or average frequency below a threshold. The threshold can be configured.

9.3.2 Low power mode usage

A clock divided from PMU_PVTM oscillation ring is used in low power mode, which can replace the function of 32KHz clock source

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9.4 Register Description

9.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PVTM_VERSION	0x0000	W	0x00000203	PVTM version register
PVTM_CON0	0x0004	W	0x00000000	PVTM control register0
PVTM_CON1	0x0008	W	0x00000000	PVTM control register 1
PVTM_CON2	0x000C	W	0x00000000	PVTM control register 2
PVTM_CON3	0x0010	W	0x00000000	PVTM control register 3
PVTM_CON4	0x0014	W	0x00000000	PVTM control register 4
PVTM_CON5	0x0018	W	0x00000000	PVTM control register 5
PVTM_CON6	0x001C	W	0x00000000	PVTM control register 6
PVTM_INT_EN	0x0070	W	0x00000000	PVTM Interrupt Enable Register
PVTM_INTSTS	0x0074	W	0x00000000	PVTM Interrupt Status Register
PVTM_STATUS0	0x0080	W	0x00000000	PVTM status register0
PVTM_STATUS1	0x0084	W	0x00000000	PVTM status register1
PVTM_STATUS2	0x0088	W	0x00000000	PVTM status register2
PVTM_STATUS3	0x008C	W	0x00000000	PVTM status register3
PVTM_STATUS4	0x0090	W	0x00000000	PVTM status register4
PVTM_STATUS5	0x0094	W	0x00000000	PVTM status register5
PVTM_STATUS6	0x0098	W	0x00000000	PVTM status register6
PVTM_STATUS7	0x009C	W	0x00000000	PVTM status register7

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

9.4.2 Detail Register Description

PVTM_VERSION

Address: Operational Base (0x273F0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RU	0x0203	version PVTM version

PVTM_CON0

Address: Operational Base (0x273F0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	pvtm_rnd_seed_en Set high to enable the round seed in PVTM.

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Bit	Attr	Reset Value	Description
4:2	RW	0x0	pvtm_osc_sel Oscillation ring selection others: Reserved For PMU_PVTM: 3'b000: oscillation ring 0 others: Reserved
1	RW	0x0	pvtm_osc_en Set high to enable the oscillation ring in the PVTM.
0	RW	0x0	pvtm_start Set high to start PVTM.

PVTM_CON1

Address: Operational Base (0x273F0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_cal_cnt PVTM calculation counter

PVTM_CON2

Address: Operational Base (0x273F0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	pvtm_osc_ring_autosel_en PVTM oscillation ring auto select enable control. It will take turns the oscillation ring (enabled by pvtm_osc_ring_autosel_en[7:0]) in order and then loop back. When none of them is enabled, use the oscillation ring selected by pvtm_osc_sel_auto. For example, when set pvtm_osc_ring_autosel_en[7:0]=8'b00000111, it will take turns oscillation ring 0, oscillation ring 1 and oscillation ring 2 in order to test and then loopback, other rings will not be tested.
7	RW	0x0	pvtm_avr_cal_mode PVTM average value calculate mode 1'b0: The average value = (summary_value-max_value-min_value) /(measurement_number-2) 1'b1: The average value = summary_value /measurement_number
6	RW	0x0	pvtm_avr_update_mode PVTM average value update mode 1'b0: Only when the number of measurement arrive pvtm_avr_period, the average value is updated. 1'b1: When the number of measurement is equal to or greater than 3, the average value is updated gradually.

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Bit	Attr	Reset Value	Description
5	RW	0x0	pvtm_start_auto_mode PVTM start mode 1'b0: When the number of measurement arrive pvtm_cal_period, calculate stop and pvtm_start_auto is cleared. 1'b1: When the number of measurement arrive pvtm_cal_period, calculate don't stop and pvtm_start_auto is not cleared.
4:2	RW	0x0	pvtm_osc_sel_auto Oscillation ring selection for auto mode others: Reserved For PMU_PVTM: 3'b000: oscillation ring 0 others: Reserved
1	RW	0x0	pvtm_osc_en_auto Set high to enable the oscillation ring in the PVTM for auto mode.
0	RW	0x0	pvtm_start_auto Set high to start PVTM for auto mode.

PVTM_CON3

Address: Operational Base (0x273F0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_cal_cnt_auto PVTM calculation counter for auto mode

PVTM_CON4

Address: Operational Base (0x273F0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pvtm_avr_period PVTM average calculation period
15:0	RW	0x0000	pvtm_cal_period PVTM calculation period

PVTM_CON5

Address: Operational Base (0x273F0000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_min_threshold PVTM minimum value threshold

PVTM_CON6

Address: Operational Base (0x273F0000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_avr_threshold PVTM average value threshold

PVTM_INT_EN

Address: Operational Base (0x273F0000) + offset (0x0070)

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Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	cal_done_Int_en 1'b0: Calculation done Interrupt disabled 1'b1: Calculation done Interrupt enabled
1	RW	0x0	avr_value_Int_en 1'b0: Average value Interrupt disabled 1'b1: Average value Interrupt enabled
0	RW	0x0	min_value_Int_en 1'b0: Minimum value Interrupt disabled 1'b1: Minimum value Interrupt enabled

PVTM_INTSTS

Address: Operational Base (0x273F0000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	W1C	0x0	cal_done_IntSts 1'b0: Calculation done Interrupt not generated 1'b1: Calculation done Interrupt generated
1	W1C	0x0	avr_value_IntSts 1'b0: Average value Interrupt not generated 1'b1: Average value Interrupt generated
0	W1C	0x0	min_value_IntSts 1'b0: Minimum value Interrupt not generated 1'b1: Minimum value Interrupt generated

PVTM_STATUS0

Address: Operational Base (0x273F0000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	pvtm_freq_done Indicates PVTM frequency count done.

PVTM_STATUS1

Address: Operational Base (0x273F0000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_freq_cnt Indicates the cycle counts of the OSC_RING clock.

PVTM_STATUS2

Address: Operational Base (0x273F0000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_rnd_seed_low_bits Indicates low 32bits of the cycle count of round seed.

PVTM_STATUS3

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Address: Operational Base (0x273F0000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_rnd_seed_high_bits Indicates high 32bits of the cycle count of round seed.

PVTM_STATUS4

Address: Operational Base (0x273F0000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_min_value PVTM minimum value

PVTM_STATUS5

Address: Operational Base (0x273F0000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_avr_value PVTM average value

PVTM_STATUS6

Address: Operational Base (0x273F0000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_max_value PVTM maximum value

PVTM_STATUS7

Address: Operational Base (0x273F0000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	pvtm_avr_cnt PVTM average calculation current count
15:0	RO	0x0000	pvtm_cal_cnt PVTM calculation current counter

9.5 Application Notes

9.5.1 PVTM Manual mode Usage Flow

1. Enable the frequency fixed clock clk_pvtm.
2. Reset the PVTM.
3. Set pvtm_osc_en to enable the generated clock.
4. Set pvtm_osc_sel to select the clock oscillation ring.
5. Set the pvtm_cal_cnt to an appropriate value.
6. Set pvtm_start to calculate the cycles of the generated clock.
7. Wait the pvtm_freq_done is asserted, then get the value of pvtm_freq_cnt. The period OSC_RING clock is T= cal_cnt*(Period of clk_pvtm clock)/freq_cnt, the cell delay value is T/2.

9.5.2 PVTM Auto mode Usage Flow

1. Enable the frequency fixed clock clk_pvtm.
2. Reset the PVTM.
3. Set pvtm_osc_en_auto to enable the generated clock.
4. Set pvtm_osc_sel_auto to select the clock oscillation ring.
5. Set pvtm_cal_cnt_auto to an appropriate value.
6. Set pvtm_cal_period to configure the all calculation times

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7. Set pvtm_avr_period to configure the average times
8. Set cal_done_Int_en to enable the interrupt
9. Set pvtm_start_auto to calculate the cycles of the generated clock.
10. Wait the interrupt is asserted, then get the value of pvtm_min_value/pvtm_max_value/ pvtm_avr_value. The minimum period OSC_RING clock is T= cal_cnt_auto*(Period of clk_pvtm clock)/pvtm_min_value, the minimum cell delay value is T/2. The frequency calculation of average and maximum value are same with minimum value.

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Chapter 10 PVTPLL

10.1 Overview

PVTPLL is used to monitor the chip performance variance caused by chip process, voltage and temperature, and generate a set of reference signals for adjusting the voltage of the chip.

PVTPLL supports the following features:

- A clock oscillation ring is integrated and used to generate a clock like signal (osc_clk), the frequency of this clock is determined by the cell delay value of clock oscillation ring circuit
- A frequency counter(osc_cnt) is used to measure the frequency of 'osc_clk'
- A externally input clock (ref_clk) is used as a reference clock for detecting the frequency of 'osc_clk'
- A calculation counter uses 'ref_clk' to generate a configurable periodic timing window
- Two clock counters are used to measure the frequency of the clock generated by OSC_WRAPPER
- Support for dividing the ref_clk and osc_clk
- Support for configuring the effective polarity of the voltage regulator signal 'OUT'
- Seven PVTPLL is instantiated in RK3576: BIGCORE_PVTPLL, LITCORE_PVTPLL, CCI_PVTPLL, DDR_PVTPLL, CRU_PVTPLL, GPU_PVTPLL and NPU_PVTPLL
- BIGCORE_PVTPLL, LITCORE_PVTPLL, CCI_PVTPLL
  - Support 4 different types of inverter cell selection
  - Support 64 levels of different length inverter osc_ring selection
- DDR_PVTPLL, CRU_PVTPLL, GPU_PVTPLL and NPU_PVTPLL
  - Support 3 different types of inverter cell selection
  - Support 64 levels of different length inverter osc_ring selection

10.2 Block Diagram

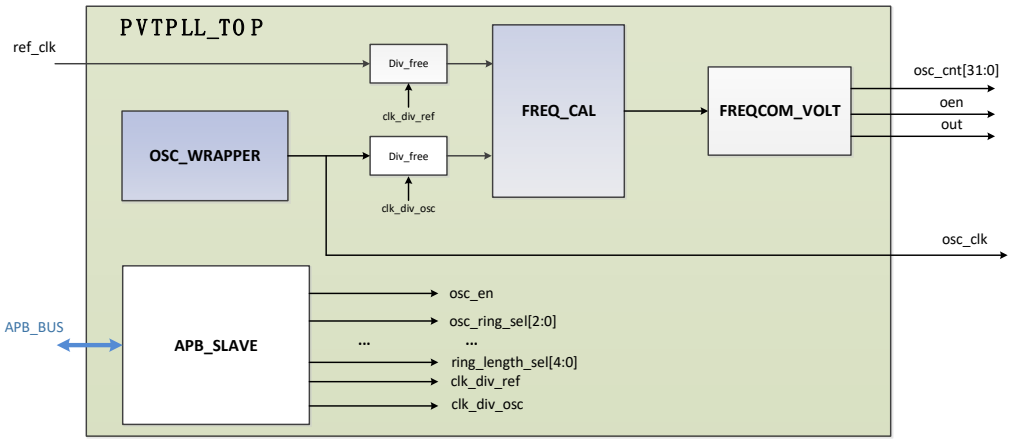


Fig. 10-1 PVTPLL Block Diagram

The PVTPLL include four main blocks:

(1)OSC_RING: it is composed with inverters with odd number, which is used to generate a clock. And PVTPLL support multiple type clock oscillation ring and different length osc_ring.

(2)FREQ_CAL: it is used to measure the frequency of clock which generated from the RING_OSC block. Clock counters are inside.

(3)FREQCOMP_VOLT: it is used to generate a set of reference signals for adjusting the voltage of the chip.

(4)APB_SLAVE: it is used to configure internal registers.

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10.3 Function Description

10.3.1 OSC RING

Each PVTPLL contains multiple OSC_RINGs that use different types of inverter cell. The number of OSC_RING is defined according to the requirements of each item. "gck_ring_sel[2:0]" is used to select which OSC_RING to use. The correspondence between "gck_ring_sel[2:0]" and the type of inverter cell is shown in the following table. The number of inverters in each OSC_RING can also be selected by the interface signal "gck_ring_len_sel". The correspondence between "gck_ring_len_sel" and the number of inverters is shown in the following table.

Table 10-1 Inverter Cell Type

Instance	ring_sel	Inverter Cell Type
BIGCORE_PVTPLL LITCORE_PVTPLL CCI_PVTPLL	0	LVT
	1	SVT
	2	SLT
	3	HVT
CRU_PVTPLL NPU_PVTPLL GPU_PVTPLL DDR_PVTPLL	0	LVT
	1	SVT
	2	HVT

10.3.2 Frequency Measurement

'osc_clk' is generated by the internal OSC_RING. The time-counter is used to measure the frequency of 'osc_clk', and the time-counter uses ref_clk as counting clock. PVTPLL generates a signal for frequency stabilization by comparing the count values of osc_cnt and ref_cnt in the same time period.

The measurement period is configured through the interface signal cal_cnt[31:0]. At the end of each measurement period, the value of osc_cnt is equivalent to the frequency of osc_clk. The osc_cnt value is compared with the reference value ref_cnt to generate a signal(out) for external voltage regulation.

10.3.3 Voltage Regulation Signal

After starting the auto-regulation function, if gck_cnt[31:0] > (gck_ref_val[31:0]+gck_thr[31:0]) or gck_cnt[31:0] < (gck_ref_val[31:0]-gck_thr[31:0]), the voltage regulation enable signal 'gck_oen' is set to 0, and the value of the voltage adjustment signal 'out' changes according to the set voltage regulation polarity signal 'out_polar', and the corresponding relationship is as shown below:

Out_polar=0: 'gck_out=1' when need to increase voltage; 'gck_out=0' when need to reduce voltage.

Out_polar=1: 'gck_out=0' when need to increase voltage; 'gck_out=1' when need to reduce voltage.

10.4 RegisterDescription

10.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

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Name	Base Address
CCI_PVTPLL	0x27250000
BIGCORE_PVTPLL	0x27258000
LITCORE_PVTPLL	0x27260000
GPU_PVTPLL	0x27268000
NPU_PVTPLL	0x27270000
CRU_PVTPLL	0x27278000
DDR_PVTPLL	0x27280000

10.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
pvtpll_ring_en	0x0000	W	0x00000000	Ring Enable
pvtpll_ring0_length	0x0004	W	0x00000000	Ring0 Length Select
pvtpll_ring1_length	0x0008	W	0x00000000	Ring1 Length Select
pvtpll_ring2_length	0x000C	W	0x00000000	Ring2 Length Select
pvtpll_ring3_length	0x0010	W	0x00000000	Ring3 Length Select
pvtpll_gck_cfg	0x0020	W	0x00000000	GCK Mode Configuration Register
pvtpll_gck_len	0x0024	W	0x00000000	GCK Mode Length Select
pvtpll_gck_div	0x0028	W	0x00000000	GCK Mode Frequency Division Configuration Register
pvtpll_gck_cal_cnt	0x002C	W	0x00000000	GCK Measurement Period Configuration Register
pvtpll_gck_ref_val	0x0030	W	0x00000000	Reference Frequency Value
pvtpll_gck_ckg_val	0x0034	W	0x00000000	Clk Gating Configuration Register
pvtpll_gck_thr	0x0038	W	0x00000000	Threshold Value
pvtpll_gfree_con	0x003C	W	0x00000000	Glitch Free Configuration Register
pvtpll_adc_cfg	0x0040	W	0x00000000	ADC Mode Configuration Register
pvtpll_adc_cal_cnt	0x0048	W	0x00000000	ADC Measurement Period Configuration Register
pvtpll_gck_cnt	0x0050	W	0x00000000	GCK Clock Frequency
pvtpll_gck_cnt_avg	0x0054	W	0x00000000	GCK Clock Frequency Average
pvtpll_gck_state	0x005C	W	0x00000000	GCK Status Register
pvtpll_adc_cnt	0x0060	W	0x00000000	ADC Clock Frequency
pvtpll_adc_cnt_avg	0x0064	W	0x00000000	ADC Clock Frequency Average
pvtpll_adc_cnt_valid	0x0068	W	0x00000000	ADC Clock Frequency Valid Flag
pvtpll_version	0x0070	W	0x20230710	VERSION

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

10.4.3 Detail Registers Description

pvtpll_ring_en

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ring3_en Ring3 enable
2	RW	0x0	ring2_en Ring2 enable
1	RW	0x0	ring1_en Ring1 enable
0	RW	0x0	ring0_en Ring0 enable

pvtpll_ring0_length

Address: **Operational Base** + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	ring0_len Ring0 Length Selection.

pvtpll_ring1_length

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	ring1_len Ring1 Length Selection.

pvtpll_ring2_length

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	ring2_len Ring2 Length Selection.

pvtpll_ring3_length

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	ring3_len Ring3 Length Selection.

pvtpll_gck_cfg

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	ring3_boot_mode osc_ring3 Boot Mode Configuration 1'b0: nand gate startup mode; 1'b1: DFF startup mode.
12	RW	0x0	ring2_boot_mode osc_ring2 Boot Mode Configuration 1'b0: nand gate startup mode; 1'b1: DFF startup mode.
11	RW	0x0	ring1_boot_mode osc_ring1 Boot Mode Configuration 1'b0: nand gate startup mode; 1'b1: DFF startup mode.
10	RW	0x0	ring0_boot_mode osc_ring0 Boot Mode Configuration 1'b0: nand gate startup mode; 1'b1: DFF startup mode.
9:7	RO	0x0	reserved
6	RW	0x0	gck_rstn reset for gck module.
5	RW	0x0	gck_mode gck_mode enable.
4	RW	0x0	clk_out_sel Output Clock Selection 1'b0: osc_clk; 1'b1: osc_clk_div50.

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Bit	Attr	Reset Value	Description
3	RW	0x0	out_polar out_polar 0: 'out=1' when need to incr volt 1: 'out=0' when need to incr volt
2	RW	0x0	gck_bypass 0: Support glitch-free frequency switching 1: Not support
1	RW	0x0	gck_en osc_en for gck_mode.
0	RW	0x0	gck_start freq_cal_gck module initiates measurement of frequency signal.

pvtpll_gck_len

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:10	RW	0x0	gck_ring_sel osc ring select for freq_gck_cal.
9	RO	0x0	reserved
8:0	RW	0x000	gck_ring_len_sel osc ring inverter length select for freq_gck_cal.

pvtpll_gck_div

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask Write Mask for gck_div[15:0].
15:12	RO	0x0	reserved
11:7	RW	0x00	clk_div_tclk Frequency division factor for test_clkout.
6	RO	0x0	reserved
5:4	RW	0x0	clk_div_out Frequency division factor for output clk.
3:2	RW	0x0	clk_div_osc Frequency division factor for osc_clk.
1:0	RW	0x0	clk_div_ref Frequency division factor for ref_clk.

pvtpll_gck_cal_cnt

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	gck_cal_cnt Used to configure the frequency measurement period of the freq_cal_adc module.

pvtpll_gck_ref_val

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	gck_ref_val Target reference frequency value

pvtpll_gck_ckg_val

Address: **Operational Base** + offset (0x0034)

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Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	gck_ckg_val Clk-gating interval control count value.

pvtpll_gck_thr

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	gck_thr Count difference threshold value.

pvtpll_gfree_con

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	filter_cycle_sel 2'b00: 1cycle; 2'b01: 2cycles; 2'b10: 3cycles; 2'b11: 4cycles.
1	RO	0x0	reserved
0	RW	0x0	glitch_free_mode 1'b0: CKG Mode; 1'b1: ICG Mode.

pvtpll_adc_cfg

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write Mask for adc_cfg[15:0].
15:4	RO	0x000	reserved
3:2	RW	0x0	adc_osc_sel Clock selection signal for the freq_cal_adc module's measurement. 2'b00: ring0_osc_clk; 2'b01: ring1_osc_clk; 2'b10: ring2_osc_clk; 2'b11: ring3_osc_clk.
1	RW	0x0	adc_en freq_cal_adc module enable signal.
0	RW	0x0	adc_start freq_cal_adc module initiates measurement of frequency signal.

pvtpll_adc_cal_cnt

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	adc_cal_cnt Used to configure the frequency measurement period of the freq_cal_adc module.

pvtpll_gck_cnt

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	gck_cnt Clock frequency value measured by freq_cal_gck.

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pvtpll_gck_cnt_avg
Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	gck_cnt_avg freq_cal_gck measured clock frequency average.

pvtpll_gck_state
Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	gck_oen Voltage regulation enable signal. Low active.
1	RO	0x0	gck_out Voltage regulation indication signal.
0	RO	0x0	gck_cnt_valid gck_cnt Valid Flag. 1'b0: Valid; 1'b1: Invalid.

pvtpll_adc_cnt
Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	adc_cnt Clock frequency value measured by freq_cal_adc.

pvtpll_adc_cnt_avg
Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	adc_cnt_avg freq_cal_adc measured clock frequency average.

pvtpll_adc_cnt_valid
Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	adc_cnt_valid adc_cnt Valid Flag. 1'b0: Valid; 1'b1: Invalid.

pvtpll_version
Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x20230710	version Version Number = 32'h20230710.

10.5 Application Notes

1. Configure gck_ring_sel and gck_ring_len_sel.
2. Set gck_mode and gck_en to 1 to enable the generated clock.
3. Configure gck_cal_cnt, gck_ref_val and gck_thr, and set out_polar to appropriate value.
4. Set gck_start to 1 to start automatic detection of the frequency.

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Chapter 11 Video Output Processor (VOP)

11.1 Overview

The VOP (video output process) module is a display output processor. It reads video data and UI data from the frame buffer of the system memory, performs corresponding processing such as cropping, color gamut space conversion, scaling, and superposition, and outputs to each high-speed display interface.

VOP supports the following features:

- Display Output Interface
  - DP Interface
    - Max support 4096x2160@yuv422-120Hz
    - Support RGB/YUV444/YUV422/YUV420 (up to 10bit) format
    - Support MST
  - HDMI / eDP Combo Interface
    - HDMI
      - Max resolution support 4096x2160@yuv444-120Hz
      - Support RGB/YUV444/YUV422/YUV420 (up to 10bit) format
    - eDP
      - Max resolution support 4096x2160@yuv444-60Hz
      - Support RGB/YUV444/YUV422 (up to 10bit) format
  - MIPI DSI2 Interface
    - Max resolution support 2560x1600@60Hz
    - Support RGB (up to 10bit) format
  - Parallel Interface
    - BT.656
      - Support PAL and NTSC
      - Support YUV422 (up to 8bit) format
      - Support Progressive and Interlace
      - Max resolution support 720x576@60Hz
    - BT.1120
      - Max resolution support 1920x1080@60Hz
      - Support Progressive and Interlace
      - Support YUV422 (up to 8bit) format
    - RGB_24BIT
      - Support RGB888/RGB565/RGB666 format
      - Max resolution support 1920x1080@60Hz
    - MCU
      - Support RGB888/RGB565/RGB666 format
      - Support Serial 2*8 RGB565 format
      - Support Serial 3*8 RGB666/RGB888 format
- Bus
  - One 32bit AHB Slave to configure registers
  - Two 128bit AXI read bus
  - One 128bit AXI write bus
- Video Ports
  - Video Port0
    - Resolution
      - Max output resolution: 4096x2160@120Hz
      - Bits per component: 10
    - Color bar
      - Horizontal mode
      - Vertical mode
    - 3D_LUT
      - Support 9x9x9 (12bit) LUT
    - ACM
      - Brightness, Saturation, Hue adjustment

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- CSC
  - 3x3 matrix: RGB2YUV, YUV2RGB, Channel swap
  - RGB2YUV: BT601_F/BT709_L/BT601_L/BT2020
- Gamma
- Dither down
  - Pre_dither_down
  - ALG
  - FRC2.0
- Sharpness
- HDR
  - Support HDR10
  - Support SDR2HLG
  - Support HDR VIVID
  - Support HLG
- Post Scale Down
  - Support video port horizontal scale rate (0.7:1]
  - Support video port vertical scale rate (0.7:1]
- Display mode
  - P2I/Interlace display
  - Blank display
  - Black display
  - Standby mode
  - X-mirror
  - Split display

- Video Port1
  - Resolution
    - Max output resolution: 2560x1600@60Hz
    - Bits per component: 10
  - Color bar
    - Horizontal mode
    - Vertical mode
  - BCSH
    - 10bit
    - Brightness (8bit), Contrast (9bit), Saturation (10bit), Hue adjustment (9bit)
  - CSC
    - YUV2RGB: BT601_F/BT709_L/BT601_L/BT2020
    - RGB2YUV: BT601_F/BT709_L/BT601_L/BT2020
  - Gamma
  - POST Scale Down
  - Dither down
    - Pre_dither_down
    - ALG
    - FRC2.0
  - Display mode
    - P2I/Interlace display
    - X-mirror
    - Blank display
    - Black display
    - Standby mode
    - Split display
- Video Port2
  - Resolution
    - Max output resolution: 1920x1080@60Hz
    - Bits per component: 8
  - Color bar
    - Horizontal mode
    - Vertical mode

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        - BCSH
            - 8bit
            - Brightness (6bit), Contrast (9bit), Saturation (10bit), Hue adjustment (9bit).
        - CSC
            - YUV2RGB: BT601-F/BT709-L/BT601-L/BT2020
            - RGB2YUV: BT601-F/BT709-L/BT601-L/BT2020
        - Gamma
        - Dither down
            - ALG
            - FRC
        - Display mode
            - P2I/Interlace display
            - Blank display
            - Black display
            - Standby mode
            - X-mirror
            - Split display
- Cluster 0/1
    - Resolution
        - Max resolution:
            - Single win:4096x2160
            - Two win: 2048x2160
    - Data format
        - AFBCD: RGBA8888/RGB888/RGBA1010102
        - RFBCD: RGBA8888/RGB888/RGBA1010102/YUV420_8bit (10bit) /YUV422_8bit (10bit) /YUV444_8bit (10bit)
        - Raster: RGBA8888/RGB888/RGB565/RGB1010102/YUV444_8bit (10bit) / YUV422_8bit (10bit) /YUV420_8bit (10bit) /YUV400_8bit (10bit)/YUV444i
        - Tile4x4_MODE0: YUV420_8bit (10bit) /YUV422_8bit (10bit) /YUV444_8bit (10bit)
        - Tile4x4_MODE1: YUV420_8bit (10bit) /YUV422_8bit (10bit) /YUV444_8bit (10bit) /YUV400_8bit (10bit)
    - Image
        - Support virtual width (max 8K word)
        - Support active offset
        - Support display offset
        - Support Y/X mirror
            - AFBC/RFBC support X mirror and Y mirror
            - Raster and tile only support Y mirror
        - Swap: alpha/RB/UV/RG swap
        - Support YUV clip
    - Cluster Line Buff Mode
        - Mode0: 1 x 4096 width layer mode
        - Mode1: 2 x 2048 width layer mode
    - Scale
        - Scale down
            - Support scale rate 1/8~1
            - Support Pre-scale: Avg2/4, Gt2/4
            - Scale mode: Best-neigh/Bilinear/Multi-phase filter
        - Scale up
            - Support scale rate 1~8
            - Y_scale mode: Best-neigh/Bilinear/Multi-phase filter
            - X_scale mode: Best-neigh/Bilinear/Multi-phase filter
    - CSC
        - YUV2RGB
            - Win0: BT601_L/BT709_L/BT601_F/BT2020/BT709_L_13/BT709_F_13/

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BT2020_L_13/BT2020_F_13
- Win1: BT601_L/BT709_L/BT601_F/BT2020

- RGB2YUV: BT601_L/BT709_L/BT601_F/BT2020

- DCI
  - Only CLUSTER0_WIN0 support

- ESMART 0/1/2/3
  - Horizontal scale up:
    - Output max resolution: 4096x2160
  - Horizontal scale down:
    - Input max resolution: 4096x2160
  - ESMART LB MODE
    - support 3*4K model and 2*4k + 2*2k model
  - Data format
    - RGB: ARGB8888/RGB888/RGB565/RGBA1010102/RGBA5551
    - YUV: YUV420/YUV422/YUV444/YUV444i/YUV400 8bit/10bit
    - YUYV: YUYV422/UYVY422
    - BPP: 8BPP
  - Image
    - Support virtual width (max 8k word)
    - Support active offset
    - Support display offset
    - Support Y-mirror
    - Swap: alpha/RB/RG/UV swap
    - Support YUV clip
  - Multi-region
    - Only one region at one line
    - All regions are RGB or YUV format
    - Up to 4 regions
  - Scale
    - Scale down
      - Support scale rate: (1/8:1]
      - Horizontal support 2 level-scale: Pre-scale (avg2/4,gt2/4)
      - Scale mode: Near-best/Bilinear
    - Scale up
      - Support scale rate [1:8]
      - Scale mode: Nearest/Bilinear/Bicubic
  - CSC
    - YUV2RGB:
      - Esmart0: BT601_L/BT709_L/BT601_F/BT2020/BT709_L_13/BT709_F_13/ BT2020_L_13/BT2020_F_13
      - Esmart1/2/3: BT601_L/BT709_L/BT601_F/BT2020
    - RGB2YUV: BT601_L/BT709_L/BT601_F/BT2020
- Overlay
  - Support 3 PORT:
    - PORT0: Max overlay 6-layers to port0;
    - PORT1: Max overlay 4-layers to port1;
    - PORT2: Max overlay 4-layers to port2;
  - Support RGB/YUV domain overlay
  - Support layers mux
  - Support per-pixel/global alpha
- Write Back
  Format: ARGB8888/RGB888/RGB565/YUV420
  Max resolution: 1920x1080
  - Support automatic write back and one frame write back model
  - Support horizontal_scale and gt2
  - Support virtual stride
- Interrupt

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- Vop_intr
  - System0 interrupt
    - AXI0 bus error
    - AXI0 dma finish
    - Write back YRGB FIFO overflow
    - Write back dma finish
    - Write back resp error
    - Write back time out
    - MMU0 interrupt
  - System1 interrupt
    - AXI1 bus error
    - AXI1 dma finish
    - MMU1 interrupt
  - Video port0/1/2 interrupt
    - Frame start interrupt
    - Line flag0 interrupt
    - Line flag1 interrupt
    - Post empty interrupt
    - Field start interrupt
    - Display hold interrupt
    - Video front porch interrupt
    - Post almost full interrupt
  - FBCD interrupt
    - Cluster0 decode error interrupt
    - Cluster0 AXI response error interrupt
    - Cluster1 decode error interrupt
    - Cluster1 AXI response error interrupt
- Vop_intr_ddr
  - Vop_dma_finish
- Vop_intr_lb
  - Video port0 post almost full
  - Video port1 post almost full
  - Video port2 post almost full

- Power domain: Independent power domains for cluster layer 0/1, esmart layer 0/1/2/3.
- Vsync of Post scan timing can connect to GPIO.

11.2 Block Diagram

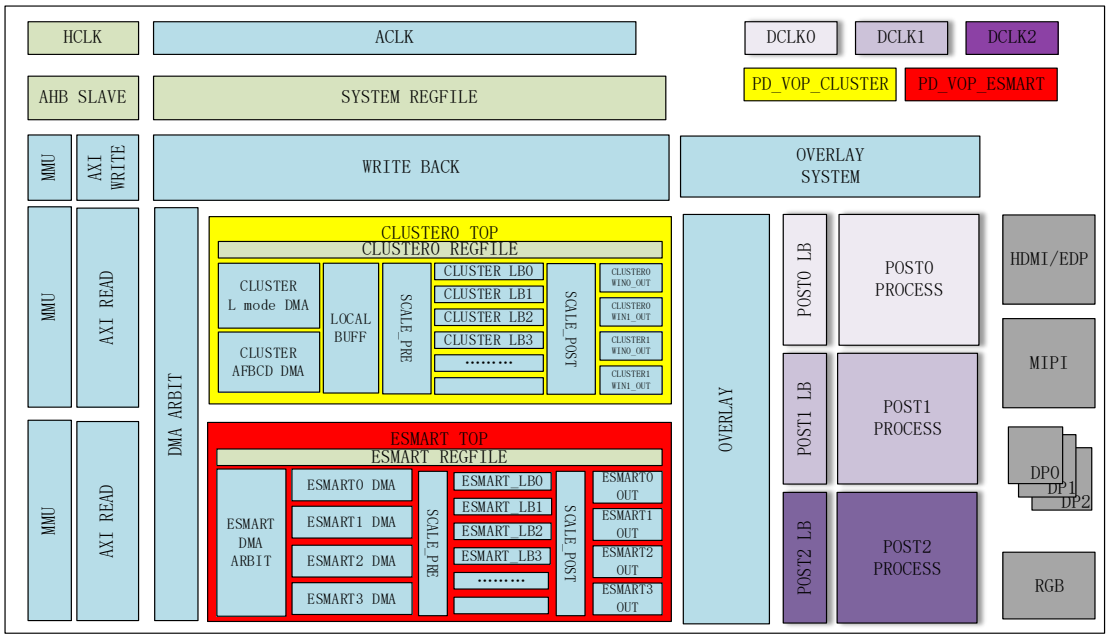


Fig. 11-1 VOP Block Diagram

VOP comprises with:

- AHB SLAVE

The VOP configuration bus is used to read and write all register configurations of the VOP. Some of the address segments are secure SLAVE address segments, which can only be accessed by a secure CPU when the security is enabled. For details, please refer to the security program description chapter.

- SYSTEM REGFILE

The register arrays, including system control, layer, overlay, and post process registers, are read and write all in the ACLK domain, and read and write use it on HCLK. When frm_st signal become 0 to 1, the control signal through from ahb domain to aclk domain.

- MMU

The Memory Management Unit maps the configured virtual address to the physical address through the page table. Since there are two buses in the system, there are two MMU addresses. In the security mode, the address of the security layer is configured as a physical address from the MMU according to the configuration. The module is bypassed, so as to avoid the address being rewritten when the MMU is mapped.

- AXI READ/WRITE

There are AXI0 and AXI1 bus in VOP interface. The AXI0 supports both write and read channel, while AXI1 only supports read channel.

- DMA ARBITER

Each layer in the system will initiate a different read request, and DMA arbiter will perform a global arbitration for internal requests based on priority settings and FIFO status.

- CLUSTERx

Cluster layer, which supports AFBCD、RFBCD、Raster mode and tile mode.

- ESMARTx

Esmart layer only supports line mode and support display up to 4 regions where the regions can’t overlap horizontally.

- OVERLAY

Perform the synthesis operation between layers according to the configuration and send it to the corresponding post process modules.

- POST PROCESS

Including GAMMA, SHARPNES, BCSH, 3D-LUT and other post-processing modules, the data is processed by the post-processing module and then store them into the POST line buffer.

- POST LINE BUFFER

The Post Process line buffer is used to store the data processed by the post process modules and output to corresponding display interface.

- INTERFACE

The VOP supports variety of output interface including HDMI, eDP, DP (SST/MST), MIPI, BT.1120, BT.656. By setting the interface mux, the corresponding PORT can be selected and output to the corresponding interface.

11.3 Operating Mode

11.3.1 Clock and Reset Description

- **HCLK**

The maximum operating frequency: 200MHz

- **ACLK**

The maximum operating frequency: 700MHz

- **DCLK0/1/2**

The maximum operating frequency of DCLK0: 600MHz
The maximum operating frequency of DCLK1: 300MHz
The maximum operating frequency of DCLK2: 150MHz

- **Hardware Reset**

System hardware reset, that is, the hardware reset of the entire VOP through the system, all the logic inside the VOP will enter the initial state, if the current screen is being displayed, there will be abnormal phenomena such as a black screen.

- **Software Frame Reset**

The frame reset of each layer is supported, that is, when the vsync signal of each frame

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arrives, the layer's internal logic will be reset exclude register logic.

- **MMU Frame Reset**

Support the MMU soft reset, when the MMU is abnormal, the entire MMU logic can be reset without causing the MMU to hang up.

11.3.2 Bus Description

- **AHB Bus**

Configuration bus for register/LUT.

- **AXI 0 Bus**

The AXI0 bus is readable and writable, which supports write back function. VOP uses AXI0 preferentially because AXI0 is on port 0 of DDR and has a dedicated debug vop_debug. The vop_rd_ urgency0 signal can stop all requests outside port0 when VOP urgently needs bandwidth, achieving the goal of almost only VOP accessing the DDR. Some of the transmission can be placed on AXI0, but because AXI1 is on port 1 of the DDR, and there are high-traffic, high-bandwidth transmission requests such as rknn on port 1, the requests on AXI1 will be greatly affected by rknn. The vop_rd_urgency1 When rknn has a large access, urgency1 cannot guarantee that VOP can compete with rknn. Therefore, AXI0 is prioritized before AXI1.

- **AXI 1 Bus**

Read-only data bus.

- **RID Default Configuration**

There are 5-bit IDs available for each bus. Among them, RID=0x0 is used to load MMU, and RID=0xf is used to achieve AXI master spanning 4KB. Therefore, these two RIDs are prohibited for users to use.

After the VOP system is powered on, the ID allocation of each layer is shown in the table below.

Fig. 11-2 Rid and bus sel in layers

LAYER_NAME	RY_RID	UV_RID	AXI_SEL	BUS SELECT
CLUSTER0_WIN0	0x2	0x3	AXI0	NO
CLUSTER0_WIN1	0x4	0x5	AXI0	NO
CLUSTER1_WIN0	0x6	0x7	AXI0	NO
CLUSTER1_WIN1	0x8	0x9	AXI0	NO
ESMART0	0xa	0xb	AXI0	YES
ESMART1	0xc	0xd	AXI0	YES
ESMART2	0xa	0xb	AXI1	YES
ESMART3	0xc	0xd	AXI1	YES
LUT_VP0	0x1~0xc		AXI1	YES
LUT_VP1	LUT_VP0+1		AXI1	YES
LUT_VP2	LUT_VP0+2		AXI1	YES
LUT_other	0x1~0xc		AXI1	YES
Note: layer rid support bit-5.lut rid support bit-4.				

- **Hurry/QoS**

VOP hurry has an enable bit and hurry value. Initiating a hurry request depends on whether the memory of the layer initiates a hurry request. When the layer's esmart_dma_rreq_hurry _en is enabled and the number of empty memory is greater than the set waterline, a hurry request is initiated.

VOP QoS has an enable bit in SYS_AXI_HURRY_CTRL0/1_IMD. When QoS is enabled and rid is greater than or equal to 0xa, QoS signal is asserted.

- **MMU Frame Valid Mechanism**

MMU support the bypass function in register mmu_bypass_en and mmu_bypass_id. When rid>=mmu_bypass_id, the AXI request and the returned data will bypass MMU. Noted that mmu_bypass_en and mmu_bypass_id is enabled immediately. At that time, rid is effective frame for the layer, so it can realize whether the layer data access is mmu_bypass.

- **Protection Mechanism**

In the protection mode, the port number of the protected layer can be set and sent to the designated protected port, otherwise the layer will be forcibly closed.

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11.3.3 Display Output Interface Description

The following figure shows the interface connection diagram of VOP. There are 3 ports in the VOP to distribute video data to different high-speed interfaces through the software setting interface MUX.

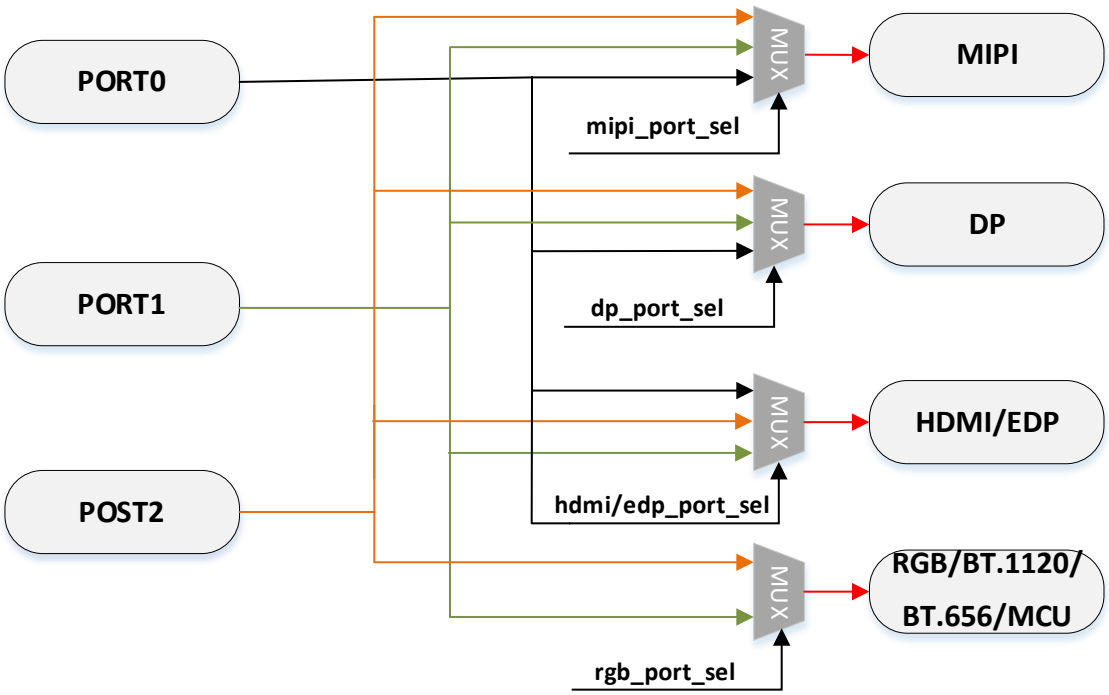


Fig. 11-3 Schematic Diagram of Display Output Interface

- HDMI/eDP Combo Interface
  - The data source of the HDMI/eDP Combo interface can come from port 0 or port 1 or port 2.
  - Maximum resolution support:
    - HDMI: 4096x2160@120 supported by PORT0
    - eDP: 4096x2160@60 supported by PORT0
  - In system, HDMI TX interface and eDP interface share the one Combo PHY, which means VOP can only work in HDMI or eDP mode.
- DP Interface
  - The data source of the DP interface can come from port 0 or port 1 or port 2.
  - The maximum supported resolution (limited by the DP TX PHY's maximum available bandwidth-25.92Gbps):
    4096x2160@120hz: supported by merged function of port 0.
  - Split mode: The one frame is split to left-right part which send to DP TX 0/1/2 respectively.
  - Support MST
    DP interface support MST to 3 channels.
    DP interface enable one DPx mode support max resolution.
    MST_DP0: 4096x2160@120Hz
    MST_DP1: 2560x1440@60Hz
    MST_DP2: 1920x1080@60Hz
    When DP interface in multi mode, transform data maximun bandwidth-25.92Gbps.
- MIPI TX DSI2 Interface
  - The maximum resolution supports 2560x1600@60Hz
    - Support RGB (up to 10bit) format
- BT.656/BT.1120/RGB/MCU
  - BT.1120 and RGB Maximum resolution support: 1080p60, pixel rate 150M/s
  - BT.656 maximum resolution support: 720x576@60Hz
  - The bit mapping relationship corresponding to each interface is as shown in the

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figure Below.

GPIO	RGB888 (MCU)	RGB666 (MCU)	RGB565 (MCU)	BT.656
LCDC_CLK	DCLK(MCU_RS)	DCLK(MCU_RS)	DCLK(MCU_RS)	BT.656_DCLK
LCDC_VSYNC	VSYNC(MCU_CSN)	VSYNC(MCU_CSN)	VSYNC(MCU_CSN)	NA
LCDC_HSYNC	HSYNC(MCU_WRN)	HSYNC(MCU_WRN)	HSYNC(MCU_WRN)	NA
LCDC_DEN	DEN(MCU_RDN)	DEN(MCU_RDN)	DEN(MCU_RDN)	NA
LCDC_D23	D23	D17	D15	BT.656_D7_M1
LCDC_D22	D22	D16	D14	BT.656_D6_M1
LCDC_D21	D21	D15	D13	BT.656_D5_M1
LCDC_D20	D20	D14	D12	BT.656_D4_M1
LCDC_D19	D19	D13	D11	BT.656_D3_M1
LCDC_D18	D18	D12	NA	NA
LCDC_D17	D17	NA	NA	NA
LCDC_D16	D16	NA	NA	NA
LCDC_D15	D15	D11	D10	BT.656_D2_M1
LCDC_D14	D14	D10	D9	BT.656_D1_M1
LCDC_D13	D13	D9	D8	BT.656_D0_M1
LCDC_D12	D12	D8	D7	BT.656_D7_M0
LCDC_D11	D11	D7	D6	BT.656_D6_M0
LCDC_D10	D10	D6	D5	BT.656_D5_M0
LCDC_D9	D9	NA	NA	NA
LCDC_D8	D8	NA	NA	NA
LCDC_D7	D7	D5	D4	BT.656_D4_M0
LCDC_D6	D6	D4	D3	BT.656_D3_M0
LCDC_D5	D5	D3	D2	BT.656_D2_M0
LCDC_D4	D4	D2	D1	BT.656_D1_M0
LCDC_D3	D3	D1	D0	BT.656_D0_M0
LCDC_D2	D2	D0	NA	NA
LCDC_D1	D1	NA	NA	NA
LCDC_D0	D0	NA	NA	NA
GPIO	BT.1120	MCU	RGB	MCU
		Serial	Serial	Serial
		3*8-bit	3*8-bit	2*8-bit(565)
LCDC_CLK	BT.1120_DCLK	MCU_RS	DCLK	MCU_RS
LCDC_VSYNC	NA	MCU_CSN	VSYNC	MCU_CSN
LCDC_HSYNC	NA	MCU_WRN	HSYNC	MCU_WRN
LCDC_DEN	NA	MCU_RDN	DEN	MCU_RDN
LCDC_D23	BT.1120_D15	MCU_D7_M1	RGB_D7_M1	MCU_D7_M1
LCDC_D22	BT.1120_D14	MCU_D6_M1	RGB_D6_M1	MCU_D6_M1
LCDC_D21	BT.1120_D13	MCU_D5_M1	RGB_D5_M1	MCU_D5_M1
LCDC_D20	BT.1120_D12	MCU_D4_M1	RGB_D4_M1	MCU_D4_M1
LCDC_D19	BT.1120_D11	MCU_D3_M1	RGB_D3_M1	MCU_D3_M1
LCDC_D18	NA	NA	NA	NA
LCDC_D17	NA	NA	NA	NA
LCDC_D16	NA	NA	NA	NA
LCDC_D15	BT.1120_D10	MCU_D2_M1	RGB_D2_M1	MCU_D2_M1

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LCDC_D14	BT.1120_D9	MCU_D1_M1	RGB_D1_M1	MCU_D1_M1
LCDC_D13	BT.1120_D8	MCU_D0_M1	RGB_D0_M1	MCU_D0_M1
LCDC_D12	BT.1120_D7	MCU_D7_M0	RGB_D7_M0	MCU_D7_M0
LCDC_D11	BT.1120_D6	MCU_D6_M0	RGB_D6_M0	MCU_D6_M0
LCDC_D10	BT.1120_D5	MCU_D5_M0	RGB_D5_M0	MCU_D5_M0
LCDC_D9	NA	NA	NA	NA
LCDC_D8	NA	NA	NA	NA
LCDC_D7	BT.1120_D4	MCU_D4_M0	RGB_D4_M0	MCU_D4_M0
LCDC_D6	BT.1120_D3	MCU_D3_M0	RGB_D3_M0	MCU_D3_M0
LCDC_D5	BT.1120_D2	MCU_D2_M0	RGB_D2_M0	MCU_D2_M0
LCDC_D4	BT.1120_D1	MCU_D1_M0	RGB_D1_M0	MCU_D1_M0
LCDC_D3	BT.1120_D0	MCU_D0_M0	RGB_D0_M0	MCU_D0_M0
LCDC_D2	NA	NA	NA	NA
LCDC_D1	NA	NA	NA	NA
LCDC_D0	NA	NA	NA	NA

GPIO	RGB Serial 2*8-bit(565)
LCDC_CLK	DCLK
LCDC_VSYNC	VSYNC
LCDC_HSYNC	HSYNC
LCDC_DEN	DEN
LCDC_D23	RGB_D7_M1
LCDC_D22	RGB_D6_M1
LCDC_D21	RGB_D5_M1
LCDC_D20	RGB_D4_M1
LCDC_D19	RGB_D3_M1
LCDC_D18	NA
LCDC_D17	NA
LCDC_D16	NA
LCDC_D15	RGB_D2_M1
LCDC_D14	RGB_D1_M1
LCDC_D13	RGB_D0_M1
LCDC_D12	RGB_D7_M0
LCDC_D11	RGB_D6_M0
LCDC_D10	RGB_D5_M0
LCDC_D9	NA
LCDC_D8	NA
LCDC_D7	RGB_D4_M0
LCDC_D6	RGB_D3_M0
LCDC_D5	RGB_D2_M0
LCDC_D4	RGB_D1_M0
LCDC_D3	RGB_D0_M0
LCDC_D2	NA
LCDC_D1	NA
LCDC_D0	NA

Fig. 11-4 Map of parallel port I/O output

11.3.4 Display Output and Interface CLK Description

The VOP_DCLK input and output architecture of dclk is shown in the following figure.

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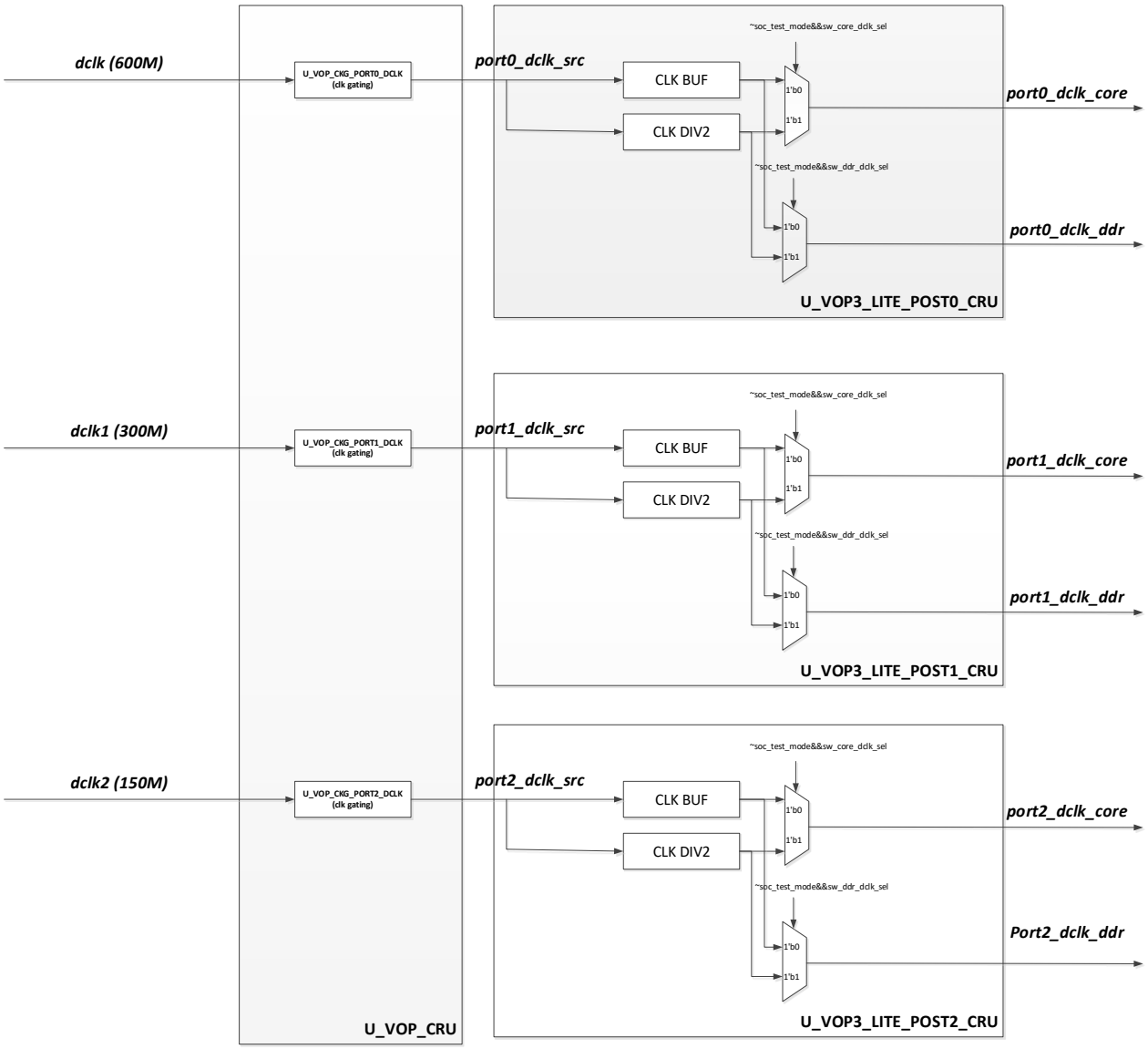


Fig. 11-5 VOP_POST_DCLK CRU

11.3.5 Interrupt Description

There are three interrupt signals.

VOP_INTR: Including the following groups of interrupt sources

- vop_intr_sys
- vop_intr_sys1
- vop_intr_post
  - vp0_intr_post
  - vp1_intr_post
  - vp2_intr_post
- vop_intr_fbcd

VOP_INTR_DDR: Conditional interrupt source dma_finish from DDR frequency conversion, refer to frequency conversion description for details.

VOP_INTR_LB: Including the following groups of interrupt sources, which can set the buffer waterline to notify the CPU that the predetermined waterline has been reached.

- INTR_STATUS_POST_FULL0
- INTR_STATUS_POST_FULL1

11.3.6 Maximum Performance and Functional Attributes of each PORT

- PORT0
  - Maximum supported resolution in single PORT mode is 4096 pixels.
  - Dual gamma
  - 9x9x9 3DLUT
  - Sharp

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- ACM
- PORT1
  - Maximum supported resolution of single PORT mode is 2560 pixels.
  - Dual gamma
  - BCSH
- PORT2
  - Maximum supported resolution is 1920 pixels.
  - Dual gamma
  - BCSH

11.3.7 Power Domain Power Up/Down Description

There are two power domains inside VOP, show as the below figures where the green border is the boundary of each power domain.

- Cluster Power Domain: One power domain for cluster0, cluster1 respectively.
- Esmart Power Domain: One power domain for esmart0, esmart1, esmart2 and esmart3.

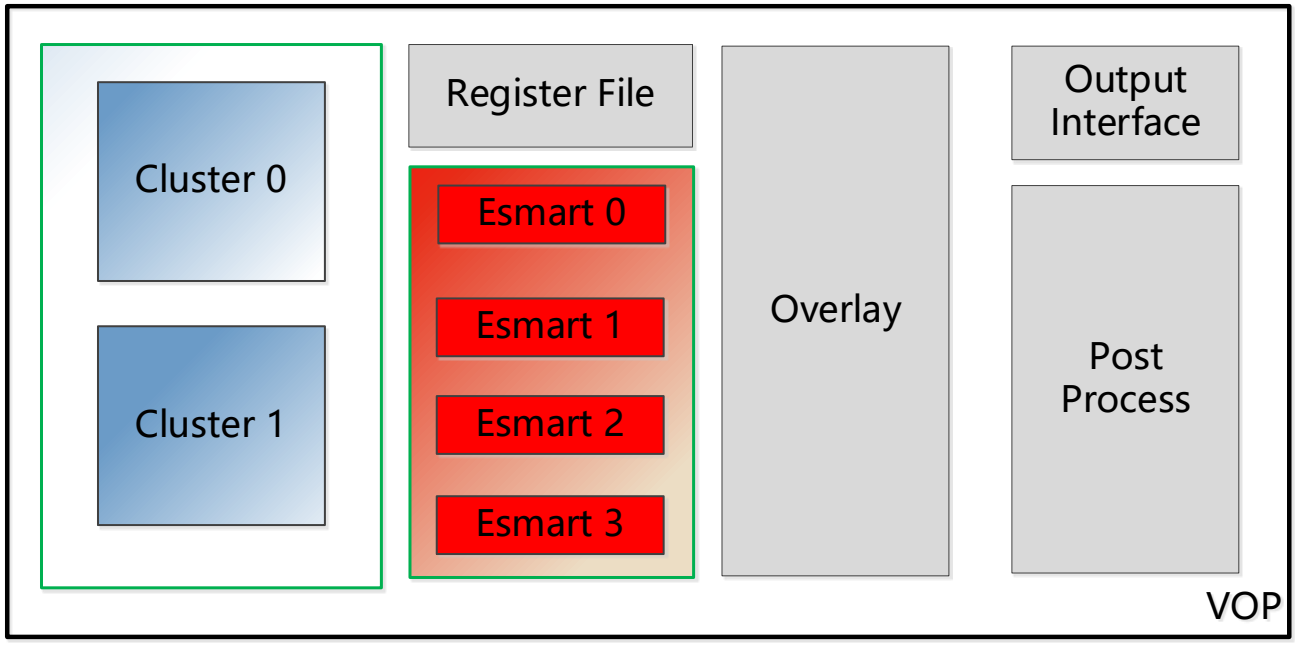


Fig. 11-6 Power Domains Structure Diagram of VOP

The cluster PD domain has 2 layers. The esmart layer 0/1/2/3 share one power domain. It is recommended that only static switches are used according to the application scenario.

11.3.8 Function Memory Chain Switch Description

Since the power domain cannot achieve the functional level power switch, in some application scenarios, when a memory function does not need to be dynamically turned on, the power supply of the memory chain can be turned off, which can reduce the power consumption as much as possible. It is divided into eight memory chains of WB, Post Process Module 0/1/2.

The register address is as follows:

- PMU_SUBMEM_PWR_GATE_SFTCON1
- PMU_SUBMEM_PWR_GATE_SFTCON2

The bit allocation of memory chain is as follows:

- #define MID_VOPPOST0 (1<<15)
- #define MID_VOPPOST1 (1<<16)
- #define MID_VOPPOST2 (1<<17)
- #define MID_VOPWB (1<<22)

11.3.9 Security Program Description

11.3.9.1 SoC Connection Diagram

(1) The switch of the security layer and the selection of the security port controlled by register vop_sec_drm_ctrl(SYS_SGRF_SOC_CON1[10:0]).

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(2) Support a certain address segment (security layer address segment) of the AHB slave can be designated as a secure address on the interconnect;
(3) The bus supports MMU bypass logic according to the layer's ID.

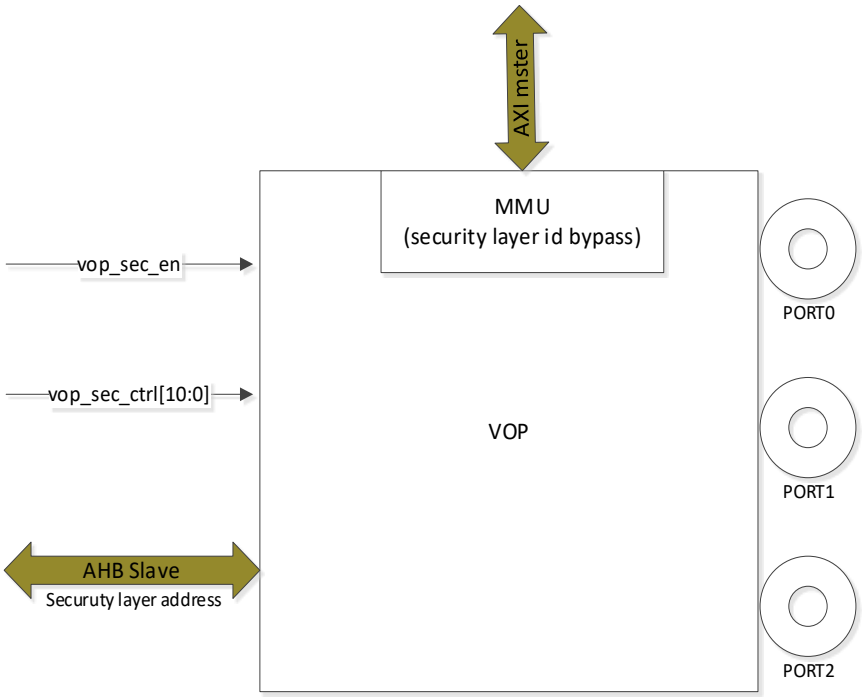


Fig. 11-7 security schematic block diagram

11.3.9.2 Hardware Security Implementation

(1) The following points shall be guaranteed:
1) The secure layer shall only be selected to the corresponding secure PORT;
2) The secure mode write back function shall be disabled;
3) In the system, DDR can be configured to only allow access to devices with security attributes on the bus;
(2) The layer address segment will not be accessed by non-secure CPU;
The address space corresponding to esmart0 is defined as a secure address, and the specific address is as follows:

0x27D01800 ~ 0x27D018ff

(3) MMU bypass logic ensures that the MMU page table will not be tampered with and accessed to other addresses;
vop_sec_ctrl[10:0] is added to the VOP interface, the specific description is as follows.

Table 11-1 Description of security-related registers

SGRF	bits	description
vop_sec_en	1	1'b0: Non-secure mode 1'b1: Secure mode
vop_sec_port	2	2'b00: Video PORT0 2'b01: Video PORT1 2'b10: Video PORT2
vop_wb_dis	1	1'b0: Normal 1'b1: Disable WB function
vop_post_dis	1	1'b0: Normal 1'b1: Disable Post process
vop_nonsec_black	1	1'b0: Normal 1'b1: Non-sec PORT display black
vop_drm_en	1	1. The security layer esmart0 is forced to vop_sec_port (check) 2. When secure PORT_mux=4'h8 (no layer) , it is forced to be equal to 4'h1, and other PORTs are forced to have no

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SGRF	bits	description
		layer, which means the value is 4'h8 3. When the non-secure PORT conflicts with the PORT_mux of the secure PORT, force the non-secure PORT mux=4'h8 (check) 4. Force the security layer to be at the top of the security PORT (check) 5. When a secure layer is selected for non-secure PORT, the layer is forcibly closed (check) 6. Alpha operation after turning off the security layer (check) 7. The sys_dsp_inface_en is not configurable

11.3.9.3 Security Scene

1. Secure payment:

- Esmart0 is a secure payment layer and support to specify a secure PORT. With vop_sec_en enable.
- Vop_sec_port selects secure PORT.
- Vop_wb_dis can disable the write-back function.
- Vop_post_dis can turn off non-secure PORT.
- Vop_nonsec_black can make non-secure PORT black screen.
- Vop_drm_en is forcibly sent to secure layer security payment enable. The layer is placed on top of the secure PORT.
- The alpha operation of the secure layer is turned off.

2. Drm

VOP uses 0x1e0~0x1ff as the secure slave address segment, which is used to configure drm related operations.

- Content to layer security

Support to set whether the layer is secure, and set whether to initiate secure access according to the rid.

- Content to PORT security

PORT_x with a secure layer can be set, the secure layer can only be sent to the designated secure PORT_x, otherwise the layer will be forcibly closed.

11.3.9.4 Secure Mode Entry and Exit Process

It is recommended that driver performs the layer transfer in secure mode and normal mode.

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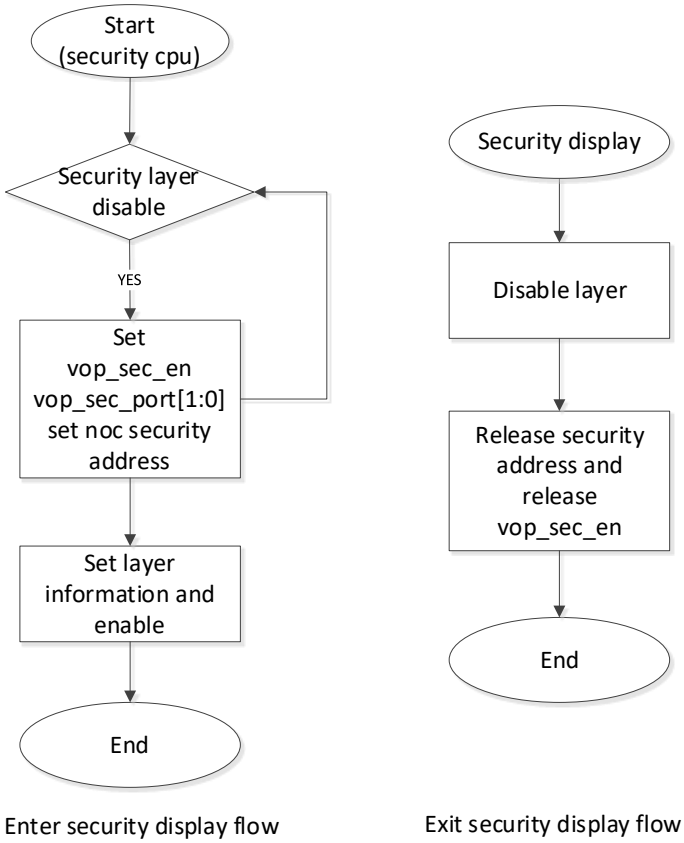


Fig. 11-8 secure mode entry and exit diagram

11.3.9.5 DDR Frequency Conversion Instructions

1. dma_finish interrupt source

This interrupt is connected to DCF and DCF can handle frequency conversion.

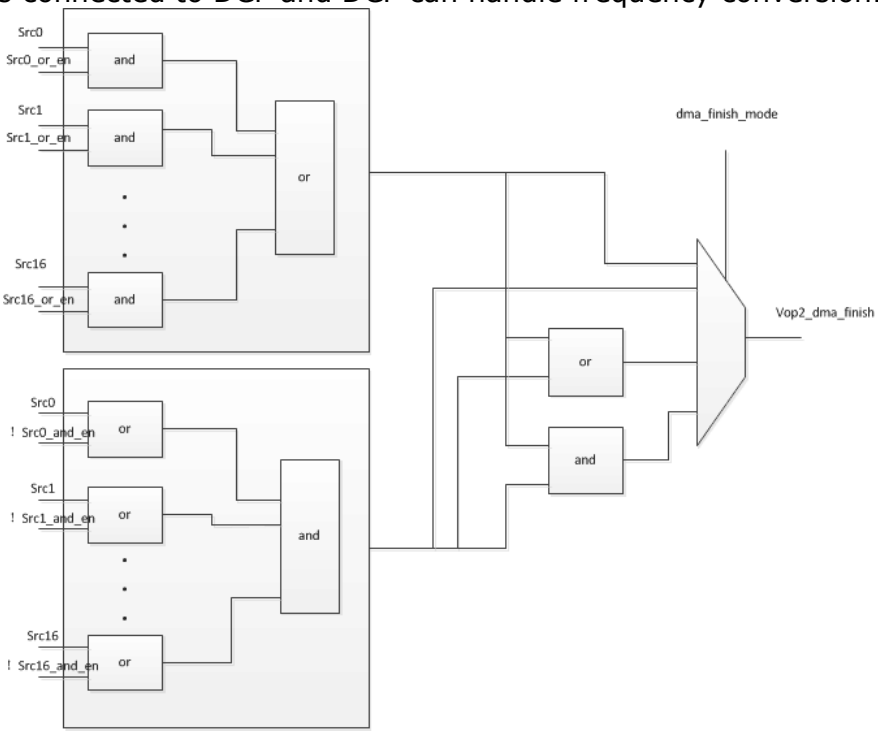


Fig. 11-9 DMA finish interrupt structure diagram

The source of dma_finish is as follows, and the logic from win almost full, vp line flag, dsp hold and almost full is combined and output.

Table 11-2 dma finish interrupt source description

source list	name	remark
dma_finish	src0	AXI0_dma_finish &AXI1_dma_finish
wb_dma_finish	src1	WB DMA finish detected
vp0_line_flag	src2	When port0 line count equals the configured line flag number
vp1_line_flag	src3	When port1 line count equals the configured line flag number
vp0_dsp_hold	src6	Port0 hold status detected
vp1_dsp_hold	src7	Port1 hold status detected
vp0_almost_full	src10	When port0 post line buffer number equals dsp_almost_full_thold
vp1_almost_full	src11	When port1 post line buffer number equals dsp_almost_full_thold

2. VOP_INTR_DDR

The VOP_INTR_DDR signal comes from dma_finish, which is connected to the system interrupt controller through an interrupt signal, and the frequency can be converted through the interrupt, which is consistent with the DCF function.

3. VOP_INTR_lb

Set the waterline of the post line buffer, and realize real-time frequency conversion through the status of line buffer, which can provide about 20us for frequency conversion.

11.4 Function Description

11.4.1 Cluster Layer

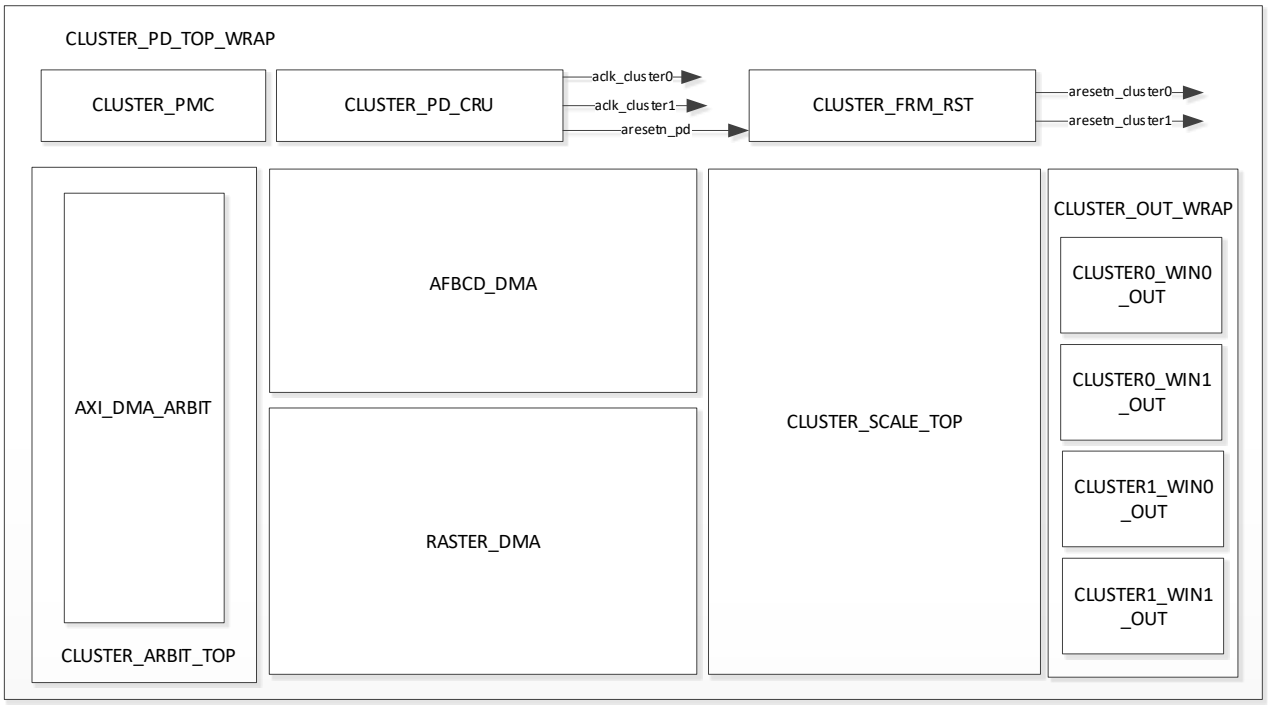


Fig. 11-10 VOP cluster block diagram

11.4.1.1 Basic Feature

- Support FBCD compression mode
- Support raster and tile mode
- Support color gamut space conversion
- Support 1/8~8 times scale
- Support mirror
- Support DCI

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- Support image virtual width

11.4.1.2 Support format description

- **RFBCD format**

When format is RFBCD, half mode and block_split must be set 0.

Parameter RFBCD_RGB565 =4'b0000
Parameter RFBCD_RGBA1010102 =4'b0010
Parameter RFBCD_RGB888 =4'b0100
Parameter RFBCD_RGBA8888 =4'b0101
Parameter RFBCD_YUV420_8b =4'b1001
Parameter RFBCD_YUV420_10b =4'b0011
Parameter RFBCD_YUV422_8b =4'b1011
Parameter RFBCD_YUV422_10b =4'b1110
Parameter RFBCD_YUV444_8b =4'b0100
Parameter RFBCD_YUV444_10b =4'b0010

- **AFBCD format**

When format is AFBCD, half mode and block_split must be set 1.

Parameter AFBCD_RGB565 =4'b0000
Parameter AFBCD_RGBA1010102 =4'b0010
Parameter AFBCD_RGB888 =4'b0100
Parameter AFBCD_RGBA8888 =4'b0101

- **AFBCD transform format**

When format is AFBCD, half mode and block_split must be set 1, color transform must be set 1.

Parameter AFBCD_RGB888 =4'b0100
Parameter AFBCD_RGBA8888 =4'b0101

- **TILE4x4 format**

When format is Tile model0, win_tile_mode_sel set 1 and fbcd_en set 0.

Parameter Tile4x4_YCbCr444_888 = 5'b01110
Parameter Tile4x4_YCbCr422_888 = 5'b01101
Parameter Tile4x4_YCbCr420_888 = 5'b01100
Parameter Tile4x4_YCbCr444_101010 = 5'b11110
Parameter Tile4x4_YCbCr422_101010 = 5'b11101
Parameter Tile4x4_YCbCr420_101010 = 5'b11100

When format is Tile model1, win_tile_mode_sel and fbcd_en must be set 0.

Parameter Tile4x4_YCbCr444_888 = 5'b01110
Parameter Tile4x4_YCbCr422_888 = 5'b01101
Parameter Tile4x4_YCbCr420_888 = 5'b01100
Parameter Tile4x4_YCbCr400_888 = 5'b01111
Parameter Tile4x4_YCbCr444_101010 = 5'b11110
Parameter Tile4x4_YCbCr422_101010 = 5'b11101
Parameter Tile4x4_YCbCr420_101010 = 5'b11100
Parameter Tile4x4_YCbCr400_101010 = 5'b11111

- **RASTER format**

Parameter ARGB8888 = 5b00000
Parameter RGB888 = 5'b01110
Parameter RGB565 = 5'b01101
Parameter RGBA1010102 = 5'b01100
Parameter YCbCr444_888 = 5'b01111
Parameter YCbCr422_888 = 5'b11110
Parameter YCbCr420_888 = 5'b11101
Parameter YCbCr400_888 = 5'b11100
Parameter YCbCr444_101010 = 5'b01111
Parameter YCbCr422_101010 = 5'b11110
Parameter YCbCr420_101010 = 5'b11101
Parameter YCbCr400_101010 = 5'b11100

Note: YUV444i format is uster RGB888 channel for data stranforamt.

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Note: The format needs to be written into the format register configuration related to FBCD. There is no one-to-one correspondence between the format and the format of the layer, and the driver needs to do a mapping.

11.4.1.3 Support line buffer mode description

Cluster line buffer supports the following three modes:
(1) Single window mode (lb mode = 2'b00): In this mode, he maximum resolution supports single 4096 pixels width layer output and layer input.

(2) Two windows mode (lb mode = 2'b01): In this mode, the cluster allows up to 2x2048 pixels width layers to be enabled and the two windows would be mixed firstly before send into overlay.

11.4.1.4 FBCD description

VOP support AFBCD and RFBCD.

AFBCD is a 32*8 based encoding method, AFBCD_SPLIT is a 32*4 based encoding method;

RFBCD is a 64*4 based encoding method;

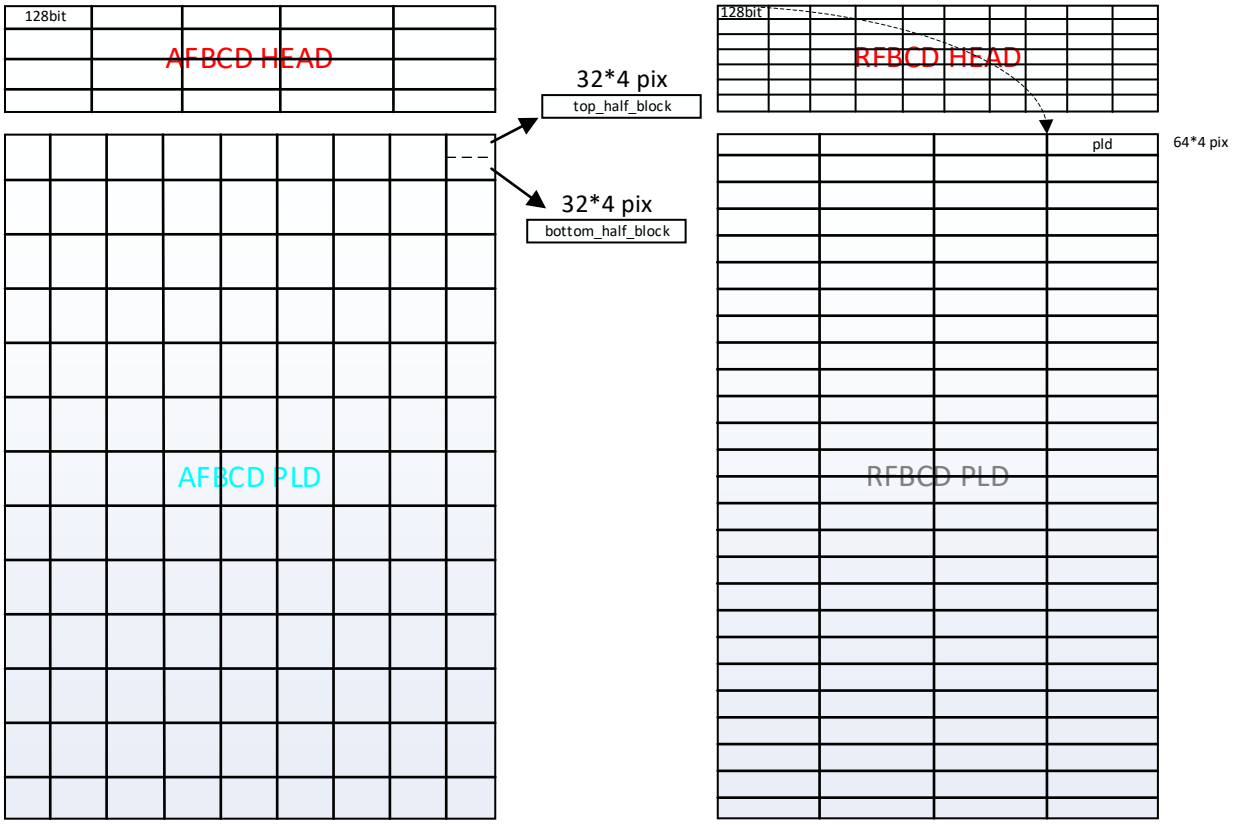


Fig. 11-11 Diagram of AFBCD_SPLIT (left) and RFBCD (right)

11.4.1.5 Scale

- Scale up:

In the horizontal direction: Bilinear, Best-neigh and Multi-phase filter
Horizontal scale up factor:

$$\text{factor} = ((\text{act_width} * 2 - 3) << 15)/(\text{dsp_widht} - 1)$$

In the vertical direction: Bilinear, Best-neigh and Multi-phase filter
Vertical scale up factor:

$$\text{factor} = ((\text{act_height} * 2 - 3) << 15)/(\text{dsp_height} - 1)$$

- Horizontal Scale Down:

When horizontal scale down up to 1/4~1:
In the horizontal direction: Bilinear, best-neigh and Multi-phase filter.

  - Horizontal scale down factor:

$$\text{factor} = ((\text{act_width} * 2 - 3) << 11)/(\text{dsp_width} - 1)$$

When scale down up to 1/8~1/4: Must be use 2 Level-Scale

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- First use xavg2 or xgt2 scale down up to 1/4 In horizontal direction
- In the horizontal direction continue to implement the remaining scaling using the following algorithm: bilinear, best-neigh, Multi-phase filter.

- Vertical Scale Down:

When vertical scale down, use Bilinear and best-neigh

- Scale dn up to 1/8~1
- Vertical scale down factor:

$$\text{factor} = ((\text{act_height} * 2 - 3) << 11)/(\text{dsp_height} - 1)$$

  - When scale down to 1/4~1/2: Must be use 2 Level-Scale to enable ygt2 or yavg2
  - When scale down up 1/4: Must be use 2 Level-Scale to enable ygt4 or yavg4
- In the horizontal direction continue to implement the remaining scaling using the following algorithm: bilinear, best-neigh.

When vertical scale down, use Multi-phase filter

- scale dn up to 1/8~1
- Vertical scale down factor:

$$\text{factor} = ((\text{act_height} * 2 - 3) << 11)/(\text{dsp_height} - 1)$$

- When scale down up to 1/8~1/4: Must be use 2 Level-Scale: ygt2 or yavg2

Note: Format is line don't support yavg.

Note: Cluster0/1 have four layers, sharing scale line buff of 8k, The allocation of line buff to layers is automatically assigned by the layer's enablement.

11.4.1.6 Mirror

In FBCD mode, cluster supports X-mirror, Y-mirror, X-mirror plus Y-mirror (equivalent to rotation180°) .

Note: VOP don't support rotation in this version.

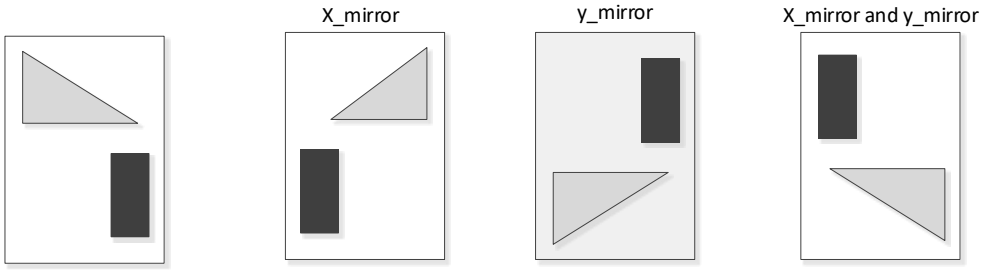


Fig. 11-12 Schematic diagram of mirror

11.4.1.7 Crop

Due to the characteristics of Android, the UI stored in the DDR is often an image larger than the actual display, so it is necessary to cut out a small image from the original image to display.

For VOP, only the following key parameters are required:

(1) Picture base ddr address

(2) Virtual stride

(3) Act_width/act_height

(4) Act_x_offset/act_y_offset

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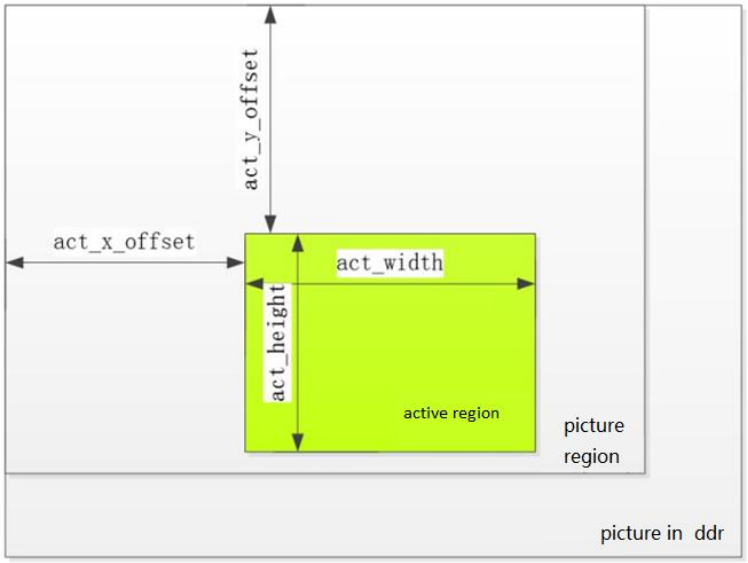


Fig. 11-13 Image storage and activation diagram

11.4.1.8 CSC module description

Support yuv2rgb, rgb2yuv color gamut space conversion, you can select the corresponding csc according to the input image format and the spatial gamut of the overlay.

RGB2YUV supports the following modes:
Parameter BT_601_L = 2'b00;
Parameter BT_709 = 2'b01;
Parameter BT_601_F = 2'b10;
Parameter BT_2020 = 2'b11;

YUV2RGB supports the following modes:
Parameter BT_601_L = 3'b000;
Parameter BT_709 = 3'b001;
Parameter BT_601_F = 3'b010;
Parameter BT_2020 = 3'b011;
Parameter BT_709_L_13 = 3'b100;
Parameter BT_709_F_13 = 3'b101;
Parameter BT_2020_L_13 = 3'b110;
Parameter BT_2020_F_13 = 3'b111;

Note: Only cluster_win0 layers support CSC 13bit model in YUV2RGB.

11.4.1.9 DCI

This module realizes dynamic picture adjustment of picture brightness and contrast by loading the statistical information of the front module (VDPP) to make the picture appear more transparent. At present, the DCI module is mainly divided into histogram processing module, curve fitting module, BBHE dual histogram equalization module, BS black level expansion module, chromaticity adjustment module, and local contrast enhancement CLAHE module.

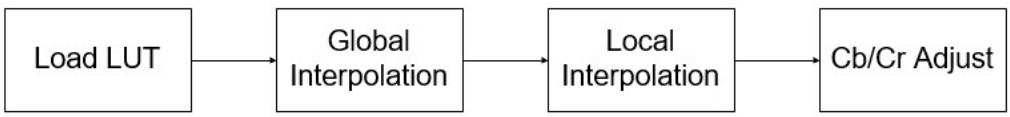


Fig. 11-14 Functional structure diagram of DCI module

*When DCI input is RGB format, use must be set csc_out_path_sel to 1'b1.

11.4.1.10 Cluster Usage Constraints

1. Line does not support X mirroring and Tile mode does not support X/Y mirroring.

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2. All pic format don't supported in the rotation mode.
3. In two win mode, the half mode bit should be set to 1.
4. Scaling ratio: (1/8~8) //TODO
5. In the case of LB two win mode, (act_width+act_xoffset%16) <= 2048.
6. When enable the win*_yrgb_vsd_gt4, the win*_act_yoffset should be 4 pixels aliged.
7. When enable the win*_yrgb_vsd_gt2, the win*_act_yoffset should be 2 pixels aliged.
8. When the data format is YUV420, the win*_act_xoffset and win*_act_yoffset should be 2 pixels aliged.
9. When the data format is YUV422, the win*_act_xoffset should be 2 pixels aliged.
10. In raster model, the data format is YUV444_10bit/YUV422_10bit/YUV420_10bit with act_xoffset should be 4 pixels aliged.
11. In raster model, the data format is YUV420_10bit/YUV422_10bit with act_width should be 2 pixels aliged.
12. In raster model, the data format is YUV420_10bit with act_height and act_yoffset should be 2 pixels aliged.
13. When the layer is in FBCD or tile format, and foramt = YUV420_8bit (10bit) , win*_*act_xoffset win*_act_yoffset should be 2 pixels aliged.
14. When the layer is in FBCD or tile format, and foramt = YUV422_8bit (10bit) , win*_act_xoffset should be 2 pixels aliged.
15. CLUSTER0/1_WIN0 layer support 13-bit Y2R.
16. Only CLUSTER0_WIN0 support DCI function.
17. In fbcd overlap mode, pld data 128-bit alignment is required.
18. In two win mode, it is strictly required that the two layers must be in the same mode state, such as fbcd/raster/tile, and mixed use is not allowed. Moreover, multiple color gamuts are not supported in the same mode.

11.4.2 Esmart layer

11.4.2.1 Schematic diagram of esmart

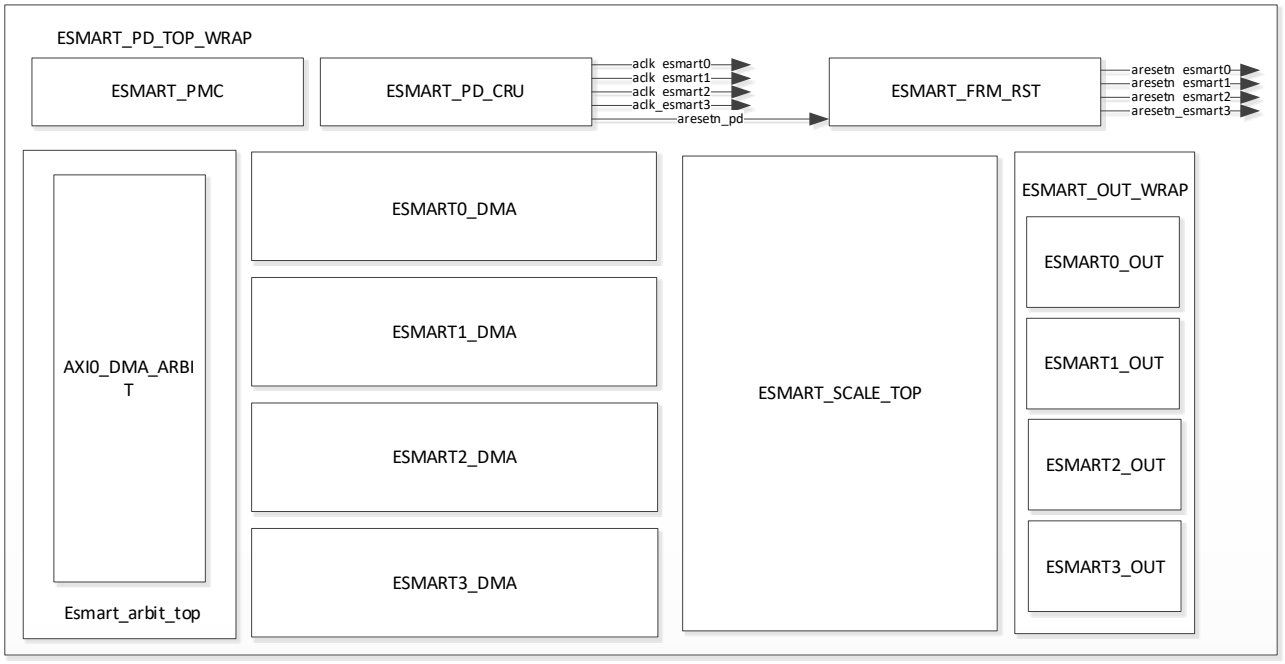


Fig. 11-15 VOP esmart block diagram

11.4.2.2 Layer

1. Feature

- Support raster mode
- Support color gamut space conversion
- Support 4 region display
- Support 1/8~8 times infinite scale
- Support image virtual width
- Support y_mirror

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2. Basic bus
The bus behavior of the esmart layer is to take one line of buffers when one line is free. It cannot be taken in two lines at a time like the 8 lines of the cluster layer. Basically, each line has a part of time for bus access. The power consumption of DDR is also not very friendly.

3. Power consumption description
The logical power consumption of the smart layer is smaller than that of the cluster layer, but because the cluster has FBCD modules, plus the power consumption of the DDR controller and phy, the overall power consumption of the smart layer is much larger than the overall power consumption of the cluster layer.
It is recommended to use FBCD as much as possible for those FBCD application, and esmart layer may be used in multi-region features.

11.4.2.3 Format

Table 11-3 Swap configuration table in esmart default format

esmart		
Format	**rb_swap**	**uv_swap**
ARGB	1	0
RGB888	1	0
RGB565	0	0
RGBA101010A2	1	0
YUV420	0	1
YUV422	0	1
YUV444	0	1
YUV400	0	0
YVYU422	0	1
VYUY422	0	1
YUV420_10bit	0	1
YUV422_10bit	0	1
YUV444_10bit	0	1
YUV400_10bit	0	0

11.4.2.4 CSC

Esmart support yuv2rgb, rgb2yuv color gamut space conversion, you can select the corresponding csc according to the input image format and the spatial gamut of the overlay.

RGB2YUV supports the following modes (csc_mode[1:0]):

```
Parameter BT_601_L    = 2'b00;
Parameter BT_709      = 2'b01;
Parameter BT_601_F    = 2'b10;
Parameter BT_2020     = 2'b11;
```

YUV2RGB supports the following modes (csc_mode[1:0]):

```
Parameter BT_601_L    = 2'b00;
Parameter BT_709      = 2'b01;
Parameter BT_601_F    = 2'b10;
Parameter BT_2020     = 2'b11;
```

Note: Only esmart0 layer support yuv2rgb 13bit model.
when esmart_yuv2rgb_13bit_en set 1.csc_mode[1:0] define change to following:

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```
Parameter BT_709_L_13    = 2'b00;
Parameter BT_709_F_13    = 2'b01;
Parameter BT_2020_L_13   = 2'b10;
Parameter BT_2020_F_13   = 2'b11;
```

11.4.2.5 Scale

Horizontal direction algorithm:

- Scl up: Best-neigh/bilinear/bicubic
- Scl dn: Best-neigh/bilinear (support 2 Level-Scale)

Vertical direction algorithm:

- Scl up: Best-neigh/bilinear/bicubic
- Scl dn: Best-neigh/bilinear

Sample:2 level-scale sample:A picture with a width of 400 and a height of 400 is scaled to a picture with a width of 150 and a height of 400 by vop:

1. Act_width = src_width (400) - 1; act_height = src_height (400) - 1; write act_width to DSP_INFO[15:0]. write act_height to DSP_INFO[31:16].
2. Dsp_width=dst_width (150) - 1;dsp_height=dst_height (400) - 1;write dsp_width to DSP _INFO[15:0]. write dsp_height to DSP_INFO[31:16].
3. Set regionx_xpre_scl_mode (REGIONx_MST_CTL[23:22]) = 2'b00.
4. Enable xavg_en (REGIONx_MST_CTL[20]) or xgr_en (REGIONx_MST_CTL[21]) .
5. After the 1 level-scale, act_width becomes 200.
6. Calculate the scale_factor width 200 to 150, set regionx_yrgb_xfactor (REGIONx_SCL _FACTOR_YGB[15:0]) = scale_factor.
7. Enable regionx_xsd_en (REGIONx_SCL_CTRL[1]) .

11.4.2.6 ESMART LB_MODE

Esmart0/1/2/3 share 8k line buff :

- Esmart lb_mode = 2'b10: Support three layers display up to 4k pixels.
- Esmart lb_mode = 2'b11: Support two layers display up to 2k pixels and two layers display up to 4k pixels.

11.4.2.7 Usage Constraints

1. Layer don't support the YUYV420/UYVY420 format.
2. Layer requires the act_width and act_xoffset of YUV422/YUV420 to be 2 pixels aligned.
3. Layer requires the act_width and act_xoffset of YUV444_10bit/YUV422_10bit/ YUV420_10bit/YUV400_10bit to be 4 pixels aligned.
4. Layer requires the act_height and act_yoffset of YUV420/YUV420_10bit to be 2 pixels aligned.
5. Layer don't support rotation and x-mirror.
6. Multiple regions within a layer cannot have spatial intersections in the Y direction.
7. ARGB5551 and RGB565 share a format_type (FMT_RGB565), and are distinguished by the sw_fmt_argb1555 (REGIONx_MST_CTRL_BIT7) bit.
8. If esmart_ygt2 (ygt4) enable, act_yoffset should be 2 (4) pixels aligned.
9. If esmart_xgt2 (xgt4) enable, act_xoffset should be 2 (4) pixels aligned.
10. Only esmart0_layer support y2r_13bit.

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11.4.3 Overlay

11.4.3.1 Schematic diagram of layer data path

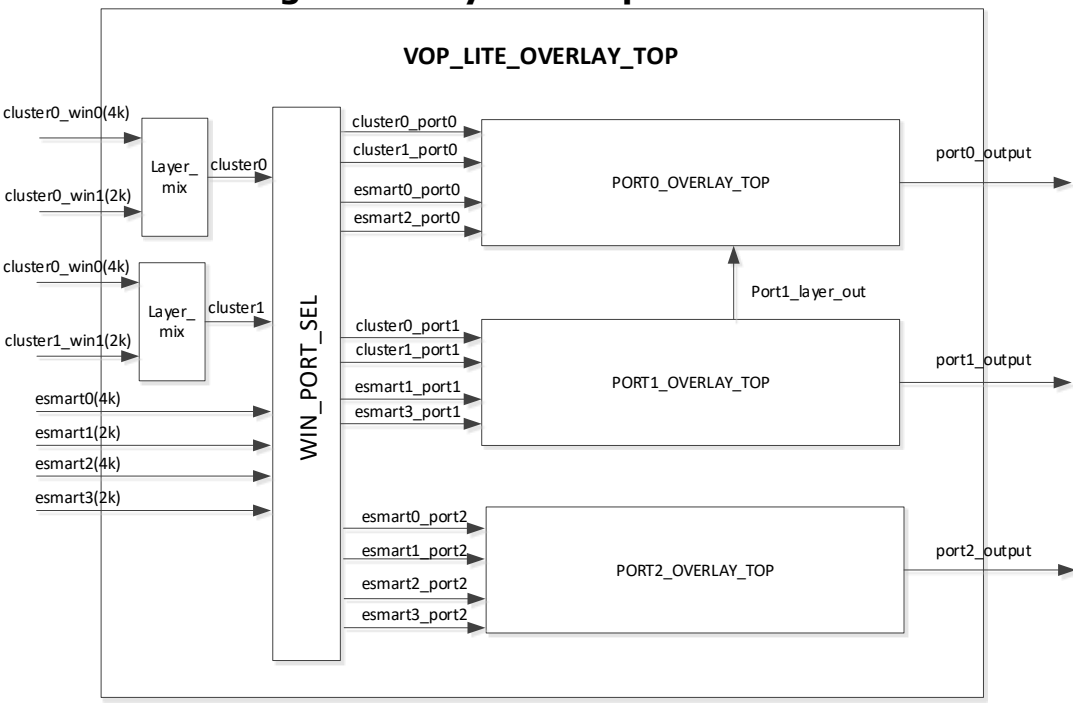


Fig. 11-16 VOP overlay block diagram

11.4.3.2 Delay setting of each function

As shown in the figure above, in the new overlay architecture. all post are output from the last stage of mux, so the value of each vp should be a fixed delay_num, and its default value is shown in the following table. Typical settings are as follows.

Table 11-4 Default table of layer delay number

Block	Delay_num
Esmart layer	0
Cluster layer	0
The delay of the port0 last mux output	20
The delay of the port1 last mux output	16

11.4.3.3 Alpha module

If there is no alpha processing, it is a direct coverage effect. Therefore, it is necessary to do an alpha effect on the corresponding layer or the corresponding position to achieve the superposition of the UI and the background or video. Most of them are aimed at the RGB data with alpha output by the GPU, such as RGBA8888; or the global alpha of the layer is configured inside the VOP to realize the special effect of superimposing between the layers. The following picture shows the basic alpha overlay effect:

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Fig. 11-17 Schematic diagram of alpha effect

1. Per-pixel Alpha

Per-pixel alpha, as the name implies, is that each point has corresponding alpha information. As shown in the picture above, the alpha value of each point in Jordan's picture increases from 0 to 255 in cycles from left to right, and the effect gradually changes from fully transparent to impermeable.

2. Global Alpha

The global alpha has nothing to do with the original data. You can set the alpha value of the entire layer separately. As shown in the figure above, the little bee layer is a global alpha effect, and the transparency of the entire layer is the same.

3. Pre-mult Alpha

Pre-multiplied alpha means that in the process of GPU operation, the original data and alpha have been multiplied accordingly, and there is no need to multiply alpha by its own RGB value during subsequent superposition.

The modes of Alpha are shown in the figure below:

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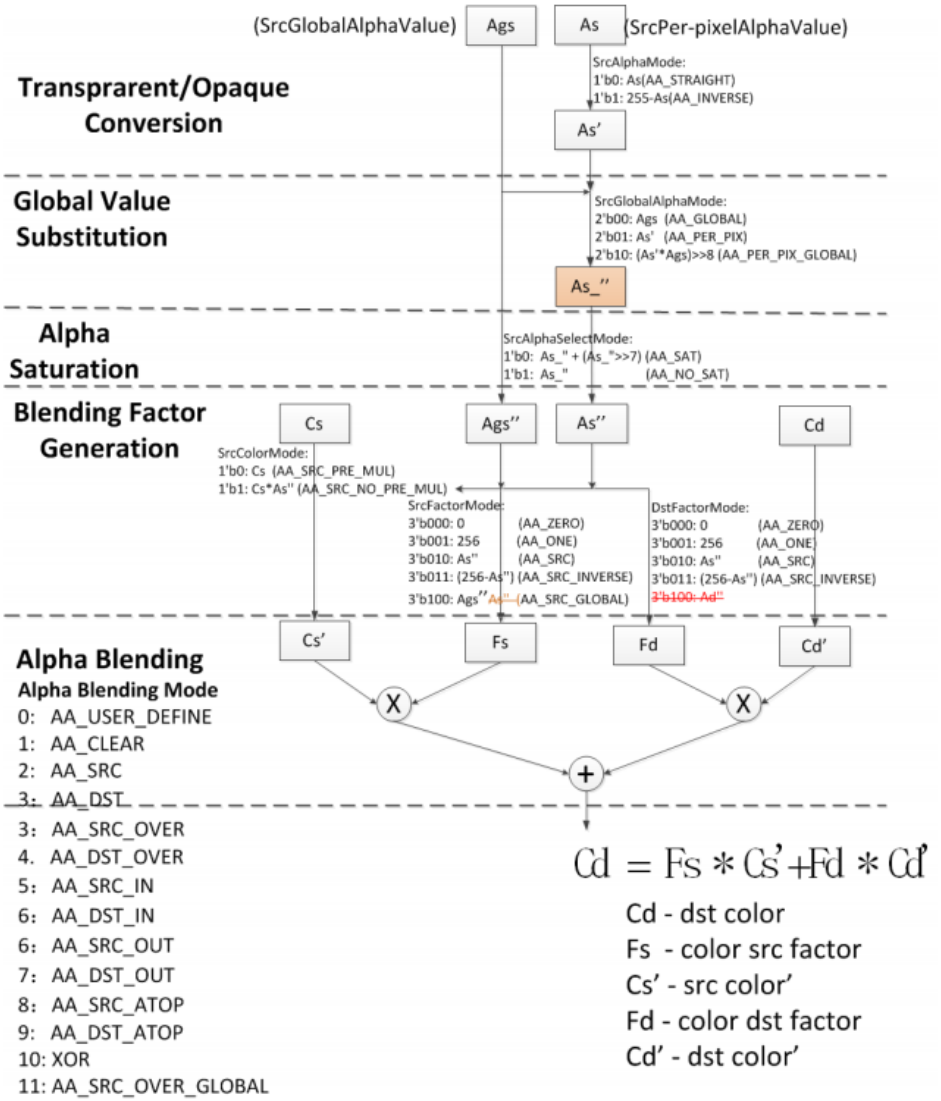


Fig. 11-18 alpha structure diagram

11.4.3.4 Secure Mode

The secure mode hardware will put the secure layer on the top layer of the selected PORT. For details, please refer to the description of 1.3.9 secure scheme.

11.4.3.5 Usage Constraints

(1) When the layer is switched by bus, the layer shall be disabled.
(2) When the post is switching mix, all the layers involved shall be disabled.

11.4.4 HDR

11.4.4.1 Feature

- Support 10-Bit data input and output
- Support 4K input and 4K output
- Support HDR VIVID
- Support HDR10
- Support HLG
- Support metadata

Note: Don't support PQHDR2HLG and HDRvivid receiver adaptation mode.

11.4.4.2 HDR overlay

For SDR2HDR scenes, the overlay process.

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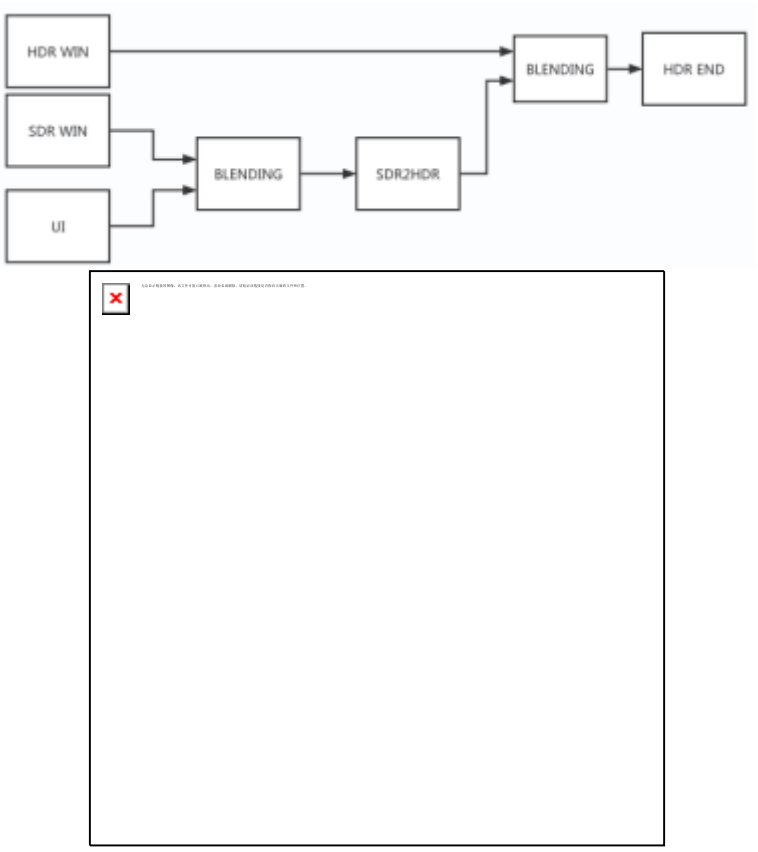


Fig. 11-19 SDR2HDR process

For HDR2SDR scenes, the overlay process.

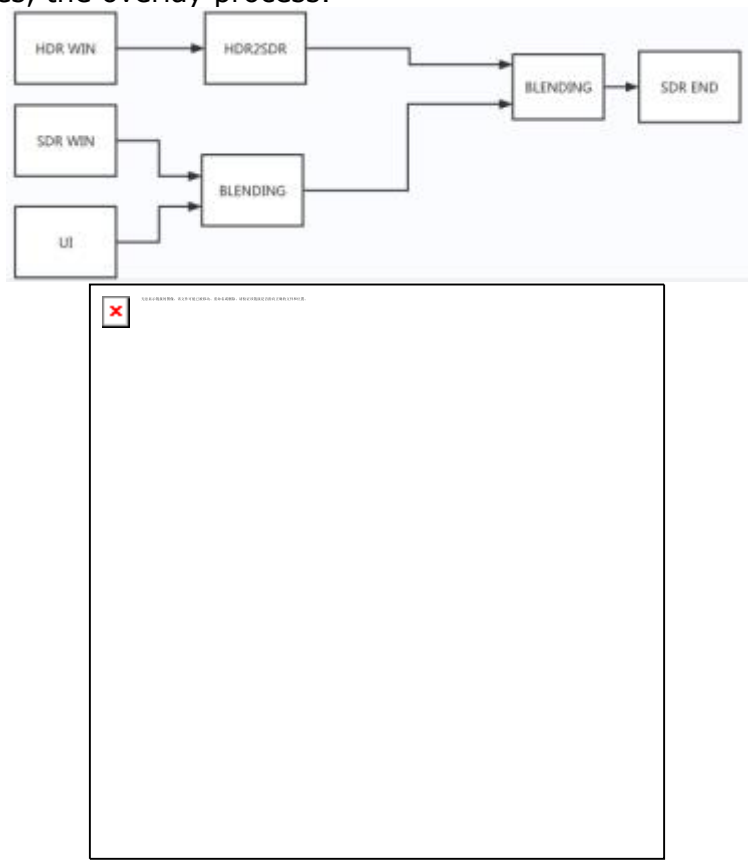


Fig. 11-20 HDR2SDR process

11.4.4.3 HDR mode delay set

Both HDR VIVID and SDR2HDR are under the overlay module. To enable the module or select different modes to work, you need to configure different delay values.

For the HDR vivid channel, there are a total of 8 modes, of which mode7 is a mode compatible with HDR10. The design is the same as mode1. The only difference is the configuration of

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curves and parameters. For the SDR2HDR/HLG path, there are a total of 2 modes. The details are as follows, including the delay of each mode

Table 11-5 HDR mode and SDR delay num

		Function model	delay
HDR VIVID	mode 0	PQHDR2HDR with Dynamic Meta	17
	mode 1	PQHDR2SDR with Dynamic Meta	29
	mode 2	HLG2PQHDR with Dynamic Meta	32
	mode 3	HLG2SDR with Dynamic Meta	44
	mode 4	HLG2PQHDR without Dynamic Meta	15
	mode 5	HLG2SDR without Dynamic Meta	38
	mode 6	HDR bypass	1
	mode 7	HDR10	29
SDR2HDR/HLG	SDR2HDR	SDR2HDR	21
	SDR2HLG	SDR2HLG	21

11.4.4.4 HDR configure

To enable HDR2SDR or SDR2HDR, the enable signal on overlay and the enable signal inside HDR2SDR or SDR2HDR must be turned on at the same time.

1. Overlay mode: Bit0 of OVERLAY_PORT0 0x0600 is set to 0 for overlay RGB mode.
2. HDR2SDR:

Bit4 of OVERLAY_PORT0 0x0600 is set to 1.
Bit0 of HDR 0x2040 is set to 1.

3. SDR2HDR:

Bit5 of OVERLAY_PORT0 0x0600 is set to 1.
Bit0 of HDR 0x2010 is set to 1.

4. Immediately effective registers: Ink related registers (0x2080 to 0x2088), lookup table configuration (0x213c to 0x29fc).
5. Frame valid register: except Ink and lookup table.

- **Lut updata**

Except for HDR vivid channel mode 0 to 3, tone and sca need to be updated every frame, and other tables can be configured once at the beginning. Configure registers directly through AHB.

Updates to tone and sca tables are divided into two modes.

1. **AHB**

The advantage of configuring the register directly through AHB is that it is easy to debug if it is not dynamically updated.

The dynamic update process is as follows.

Initialize the configuration
Detect that the frame_end interrupt is valid, and start the update of the next frame table

2. **AXI**

You don't need to configure so many registers, and directly AXI goes to the corresponding address of DDR to fetch the number. Tables for tone and sca only.

Need to configure hdr_lut_update_en=1, hdr_lut_mode=1 of hdr_lut_ctrl. Hdr_lut_mst is configured as the fetch address, and the frame takes effect. Hdr_lut_fetch_done indicates that the current table has been fetched.

11.4.5 Write Back

11.4.5.1 Support format

1. Support format

- ARGB888

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- RGB888
- RGB565
- YUV420

2. Color gamut conversion

Since the main application scenario output is RGB, but there is a need for YUV420 write-back, the write-back module adds RGB2YUV format conversion, which is enabled by configuring wb_rgb2yuv_en register bit.

11.4.5.2 Single frame/multi frame mode

(1) Single frame mode

Operating in single frame mode, enable the oneframe_clr register, and automatically disable wb_en after each frame is written, so that only one frame of content will be written out.

(2) Multi-frame mode

Each frame is configured with a different address, and the wb module will continuously write out the corresponding whole frame content.

11.4.5.3 Water line

By caching the data that needs to be written to a certain amount before starting the write output, this can improve the efficiency of data bus usage. The position of the write-back watermark varies for different write-back formats, and the formula is as follows:

$$fifo_thold = wb_width * fmt_byte/16$$

Among them, frm_byte represents the byte number of a pix in the write-back format, wb_ width indicates the output width of the write-back.

11.4.5.4 Horizontal scaling

The bilinear scaling algorithm is used in the horizontal direction.

11.4.5.5 Vertical stroke

Due to the limitation of memory, there is not enough linebuffer opened separately, so no scaling is done in the y direction. If more than twice, wb_ythrow_en is configured to control the line-throwing operation to reduce the output bandwidth.

11.4.5.6 Write back virtual stride

In this design, the virtual stride of the write-back and a separate enable switch have been added. Achieve more flexible write-back length

11.4.5.7 Usage Constraints

(1) In the case of YUV domain output, the conversion of YUV2RGB is not supported, that is, RGB format cannot be written back under YUV domain.
(2) Act_in write-back mode The width is no longer required to be an integer multiple of 16. Without the virtual width function enabled, the write-back does not require 16 pixelske alignment, but the write-back data will be automatically aligned to 16 bytes.

11.4.6 Post process

Function of each PORT 0/1/2 and the post-processing modules included in each PORT.

11.4.6.1 DSP_BLANK

When DSP_OUT_BLANK enabled, VSYNC/HSYNC/DATAEN and DATA signals are all cleared to zero.

11.4.6.2 DSP_OUT_ZERO

When DSP_OUT_ZERO enabled, the VSYNC/HSYNC/DATAEN signal is pulled low, and DATA_BUS is output normally.

11.4.6.3 DSP_BLACK

When DSP_BLACK enabled, the timing-related scan timing will be output normally, and data will be 0 on the data bus.

11.4.6.4 Color bar

Each PORT has a corresponding color bar setting, which can be used to debug to eliminate

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bus and layer problems, and it can also bypass the layer to directly adjust each high-speed output interface.
Control register color_bar_en to enable colorbar of PORT;
Control register color_bar_mode to switch horizontal colorbar or vertical colorbar.

11.4.6.5 Dither

If an 8bit film source needs to be output to the rgb666 screen, if there is no dither, it is directly connected to the screen with a high 6bit. In this case, the color gradation will be caused.

In principle, the smooth curve becomes a ladder after losing the low position. In order to solve this problem, noise is added to the ladder, so that the transition can restore the original smooth curve as much as possible.

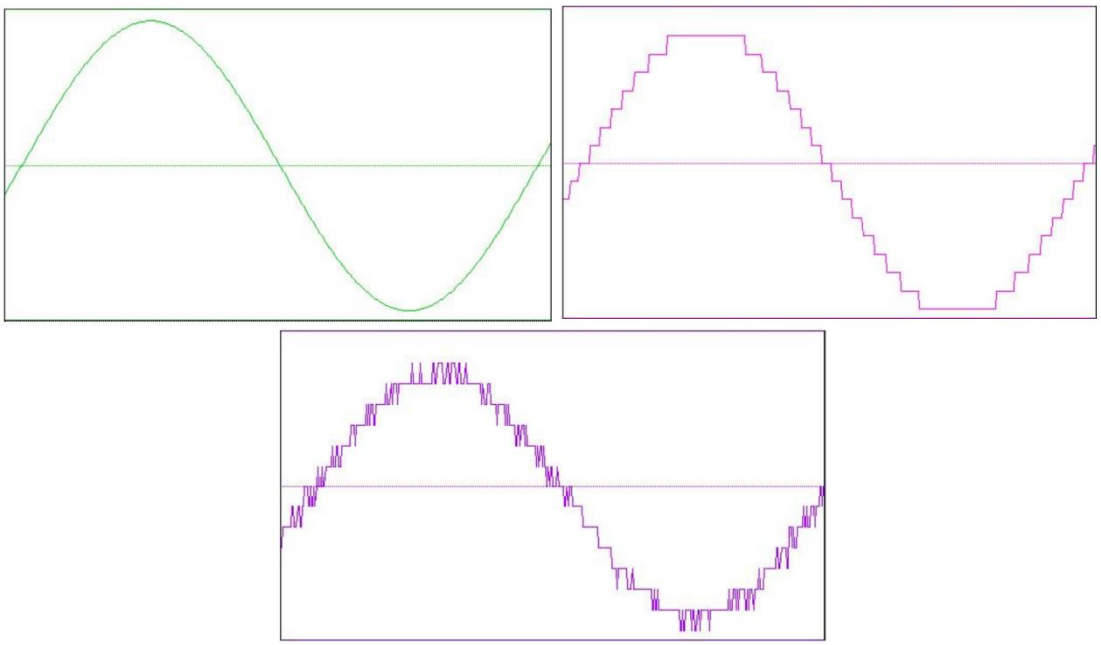


Fig. 11-21 Schematic diagram of dither principle

VOP has ALG in the dither algorithm of 10bit->8bit; there are ALG and FRC in the dither algorithm for 8bit->666/565, which can be selected by dither_down_mode.

ALG algorithm: Add fixed noise, the possible negative effect is that there will be more regular stripes similar to tire tracks;

FRC algorithm: time-domain jitter is added to the space, which works well in high frame rate scenes, and low frame rate scenes may feel a little flickering and jittery.
FRC2.0 algorithm:The Dither Noise Pattern based on 8 continuous frames in time domain, with units of pixels in the form of 16*16 in spatial domain, and YUV-differentiated color channels, is used to add random noise to the original image to achieve color dithering and reduce contouring. The random noise used is varying in the temporal domain and the noise model used is also more complex. It may be a random noise pattern generated based on some characteristics of the human visual system (such as OTF) and the construction of specific spatial filters (VP0/1 support).

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Fig. 11-22 dither effect diagram
Left: original picture; right: direct clip effect

The above picture shows the color scale effect of the original picture and the direct clip. The figure below is the figure processed by the dither algorithm. The overall effect is obvious to solve the color gradation problem caused by dither, but after partial magnification, the tire-like effect on the right side of the figure below will appear.

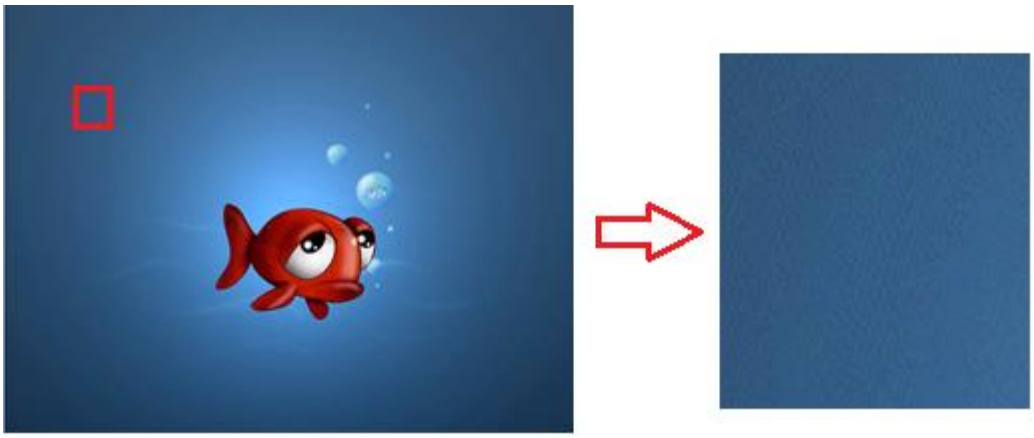


Fig. 11-23 Schematic diagram of dither's tire pattern

Note1: The dither-frc's correlation coefficient control system provides default values when it is powered up.
Note2: FRC2.0 don't support 8bit or 10bit dither down 6bit.
Note3: Post2 don't support pre_dither_down.

11.4.6.6 BCSH

BCSH mainly adjusts the following effects:
(1) CON: Contrast coefficient
(2) BRT: Bright picture adjustment value
(3) HUE: Hue adjustment angle
(4) SAT: Saturation coefficient

Y processing calculation formula

$Y_0 = Y_{input}-16$; (0<Y0<239)
$Y_1 = Y_0*CON$; (0<CON<1.992) (0<Y1<478)
$Y_2 = Y_1+BRT$; (-32<BRT<31) (-32<Y2<509)
$Y_3 = Y_2+16$; (-16<Y3<525)
Y_{output} = 4 MUX 1;

U processing calculation formula

$U_0 = U_{input}-128$; (-128, 127)
$U_1 = U_0*\cos(HUE) + V0*\sin(HUE)$; ($-30^o$<HUE<$30^o$) (-175, 174)
$U_2 = U_1*CON*SAT$; (0<CON<1.992, 0<SAT<1.992) (-695, 691)
$U_3 = U_2+128$; (-567, 819)
U_{output} = 4 MUX 1;
Cos(HUE)+sin(HUE) = (1+1/2*sin(2HUE))1/2;
So this value increases monotonically with the increase of the value of HUE. The value range of HUE is -30 ~0° .

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V processing calculation formula

$V_0 = V_{input}-128$; (-128, 127)

$V_1 = V_0*\cos(HUE) - U0*\sin(HUE)$; ($-30^o<HUE<30^o$)(-175, 174)

$V_2 = V_1*CON*SAT$; ($0<CON<1.992$, $0<SAT<1.992$) (-695, 691)

$V_3 = V_2+128$; (-567, 819)

V_{output}= 4 MUX 1;

$\cos(HUE)-\sin(HUE) = (1+1/2*\sin(-2HUE))^{1/2}$.

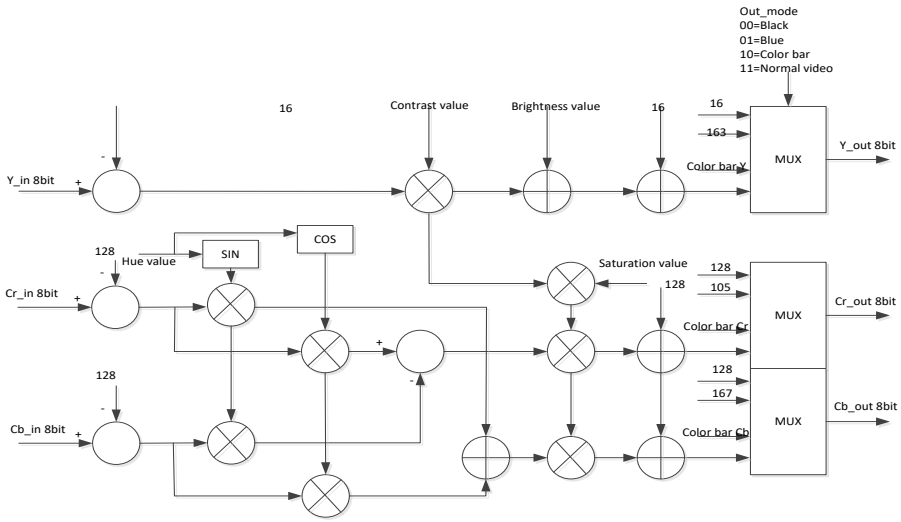


Fig. 11-24 Schematic diagram of BCSH algorithm

11.4.6.7 Gamma

Gamma basic principle:

Gamma can be understood as a 1:1 remapping of the RGB on the display channel. The three RGB curves can be consistent or inconsistent. Therefore, the display color temperature and blue light removal effects can be adjusted through the mapping relationship of the three curves.

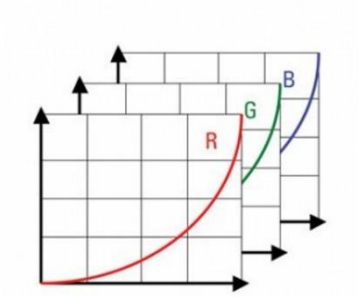


Fig. 11-25 Schematic of gamma

Dual gamma:

Because the application may adjust the gamma curve to achieve dynamic adjustment of some color temperature effects. However, the memory of the gamma table is a single-port memory. When a new table is written, it is necessary to disable gamma, which will cause screen flicker when dynamically adjusting the gamma curve.

In order to solve this flicker phenomenon, VOP adopts the ping-pong dual gamma. By statically switching gamma, one table is displayed and used in real time, and the other table is a new table that can be configured.

Note: post0/post1 gamma is 10 bit, post2 gamma is 8 bit.

11.4.6.8 ACM

ACM module, the full name of automatic color management module (auto color management), this module mainly adjusts the color of the picture by adjusting the brightness, hue and saturation to obtain a better picture with rich colors. Adjustment, more in line with the preferences of the human eye. The color correction of this module uses the three dimensions of Hue, Saturation and Brightness Value to adjust the color in the HSV system at the same

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time to achieve color correction and enhancement.
The current adjustment is mainly to convert the input YUV signal to YHS space first, adjust the color, and then convert it back to YUV space.
The ACM module is mainly divided into three components, YHS, to be adjusted respectively. Taking the adjustment interface of a certain component as an example, as shown in the figure above, the ACM module needs to adjust the delta table and two Gain tables.

- Y parameter adjustment

The delta value of the Y signal is mainly adjusted according to the Hue component. Up is to increase the brightness of the color, and down is to reduce the brightness of the color. The larger the value, the larger the adjustment amount.
This part is mainly at a certain Hue sampling point, and the corresponding gain value is adjusted according to the size of the saturation at this point. The larger the corresponding gain value, the larger the final adjustment change.
At a certain Hue sampling point, the corresponding gain value is adjusted according to the size of the corresponding brightness at that point. Similarly, the larger the corresponding gain value, the greater the final brightness adjustment change.
Y final change calculation:
Assuming that at the sampling point H of a certain Hue, the adjustment amount of Y by Hue is, the gain value of Y by Saturation is the gain value of Y by Y, and the final change amount of the brightness Y of this sampling point is the value of

$$\Delta Y_H = Delta_{YH} \cdot Gain_{YS} \cdot Gain_{YY}$$

- Hue parameter adjustment

The corresponding delta value is mainly adjusted according to the Hue component. The adjustment of the table is shown in the figure. The degree is increased upwards. After the degree is increased, the color will be shifted to the right. The greater the increase, the more colors that deviate. Down is to reduce the degree. After the degree is reduced, the color will be shifted to the left. The greater the increase, the more colors will be deviated. Take this picture as an example, adjust at the blue point, increase the degree, it will deviate in the direction of red, and decrease the degree, it will deviate in the direction of green.
Hue By Saturation can be more finely adjusted for a certain Hue sampling point according to the saturation, and the saturation of the place is searched for the gain value of the corresponding Saturation in the order from small to large. The larger the value is, the final Hue change also bigger.
At a certain Hue sampling point, the corresponding gain value is adjusted according to the size of the corresponding brightness Y. The larger the corresponding gain value, the larger the final Hue adjustment change.
Hue final change calculation:
Assuming that the adjustment amount of Hue by Hue at the sampling point H of a certain Hue is, the adjustment amount of Hue by Saturation is, and the adjustment amount of Hue by Y is, then the final change amount of chroma Hue of this sampling point is

$$\Delta H_H = Delta_{HH} \cdot Gain_{HS} \cdot Gain_{HY}$$

- Saturation parameter adjustment

The adjustment of Saturation adjusts the delta value according to the color position of the Hue point. If the point goes up, it increases the saturation, and if it goes down, it decreases the saturation.
Saturation By Saturation can be more finely adjusted according to the saturation of a certain Hue sampling point, and the saturation of the place is searched for the gain value of the corresponding Saturation in the order from small to large. The larger the value, the change amount of the final Saturation also bigger. Usually the change of saturation has a great influence on the result, so the gain value here needs to be finely adjusted.
At a certain Hue sampling point, the corresponding gain value is adjusted according to the size of the brightness Y at the sampling point. The larger the corresponding gain value, the larger the final Saturation adjustment change.
Saturation final change calculation:
Assuming that the adjustment amount of Saturation by Hue at the sampling point H of a certain Hue is, the gain value of Saturation by Saturation and the gain value of Saturation by Y, then the final change amount of Saturation of this sampling point is

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$$\Delta S_H = Delta_{SH} \cdot Gain_{SS} \cdot Gain_{SY}$$

Sample:

Taking Saturation adjustment as an example, currently, a 2D lookup table of Saturation by Saturation based on Hue sampling points and a 2D lookup table of Saturation by Y based on Hue sampling points are mainly generated according to the corresponding gain value table. As shown in the figure below, assuming the value of the input YHS signal is (Y, H, S), according to the value of the saturation S and the chroma H of the input point E1, look up the 2D lookup table of Saturation by Saturation, and find the corresponding four in the table. A sampling point A1, B1, C1, D1 and its corresponding gain value (**Gain$_{SS}$**), the gain value of E1 point is calculated by bilinear interpolation method

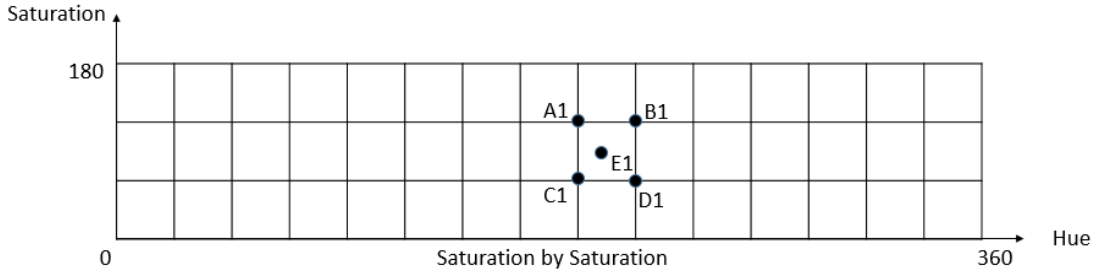


Fig. 11-26 Schematic of 2-D interpolation for Gainss

Similarly, the gain (**Gain$_{ST}$**) value at point E2 is calculated by bilinear interpolation by looking up the 2D lookup table of Saturation by Y.

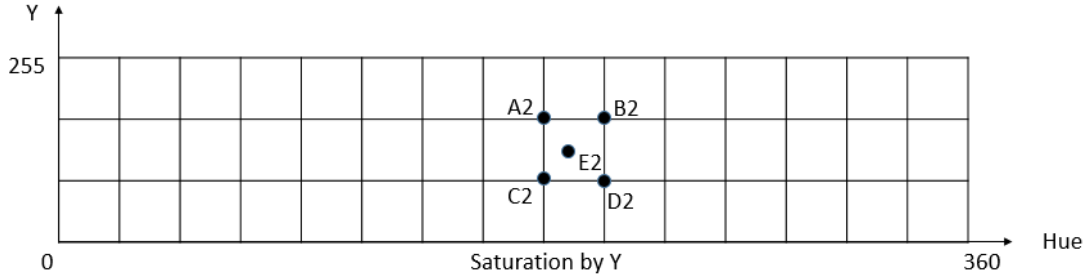


Fig. 11-27 Schematic of 2-D interpolation for Gainsy

Finally, according to the value of H, the corresponding value is linearly interpolated through the one-dimensional table of Saturation by Hue. As shown in the figure below, the delta value (Delta$_{SH}$) at E3 is linearly interpolated according to the gain values at points A3 and B3.

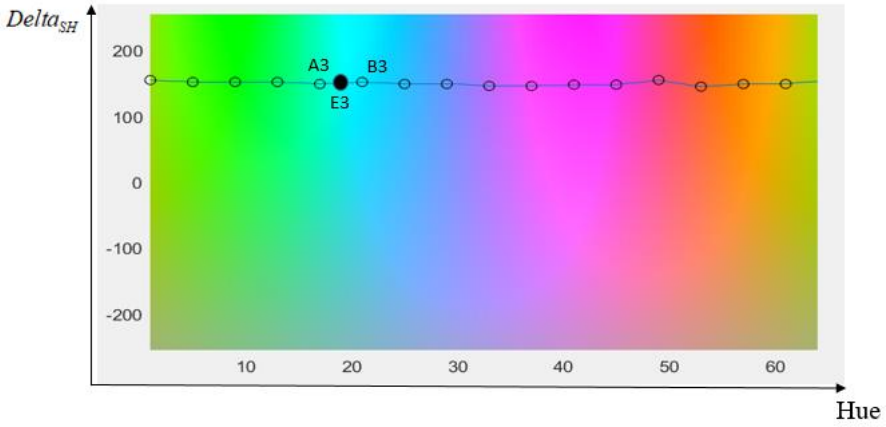


Fig. 11-28 Schematic of 2-D interpolation for Deltash

Therefore, when the value of the input YHS signal is (Y, H, S), the final value of the saturation change of the sampling point is the value of

$$\Delta S_H = Delta_{SH} \cdot Gain_{SS} \cdot Gain_{SY}$$

The calculation of the corresponding final changes of Hue and Y signals is similar to the above calculation process, that is, each YHS signal needs to look up the 2D table twice and the one-dimensional linear table once, and calculate the gain after cubic interpolation respectively. Finally, the respective changes of YHS are added to the input signal to obtain the output YHS

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signal (Y_o, H_o, S_o)

$$Y_o = \Delta Y_H + Y$$
$$H_o = \Delta H_H + H$$
$$S_o = \Delta S_H + S$$

The formula for converting YUV signal (YCbCr) to YHS signal is as follows:

$$S = \sqrt{Cr^2 + Cb^2}$$
$$H = \tan^{-1}\frac{Cr}{Cb}$$

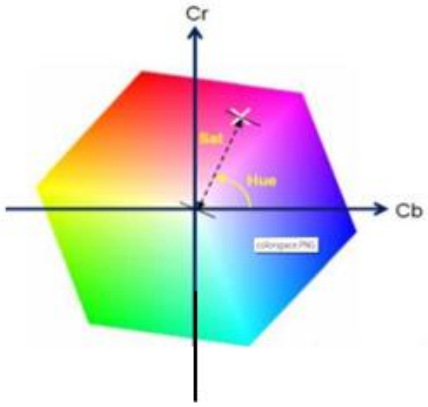


Fig. 11-29 Schematic of transform between Cb, Cr and Hue, Sat

The saturation S can be regarded as the modulo length of the Cb and Cr signals, and the chromaticity Hue can be regarded as the angle between the vector represented by the Cb and Cr signals and the horizontal axis. Similarly, the formula for converting YHS signal to YUV signal (YCbCr) is as follows:

$$Cb = S \cdot \cos H$$
$$Cr = S \cdot \sin H$$

11.4.6.9 3D LUT

Gamma can be regarded as a 1D LUT. The RGB data in the 1D LUT are independent of each other, which means that the 1D LUT can only control the gamma value, RGB balance (gray scale) and white point. In order to overcome the limitation of 1D LUT, we can form a 3×3 matrix of three 1D LUTs of RGB to control the color saturation and brightness, and perform linear scaling in the complete color space. The 3D LUT can affect the hue, saturation, brightness, etc. in a full three-dimensional color space control method.

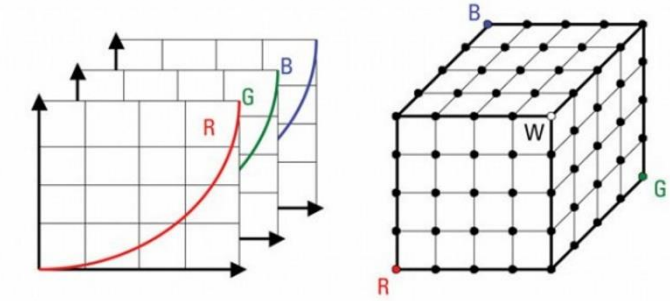


Fig. 11-30 Schematic diagram of 2D/3D-LUT

3D LUT application scenarios:

(1) Calibration (calibration LUT)

It is mainly used for the calibration of hardware and display equipment in color management. The video will be processed by different systems during the shooting, post-processing and final projection, and will appear in different forms. Therefore, the 3D LUT color space mapping can ensure that the video remains visually consistent in different systems.

(2) Technology (Technical LUT)

It is mostly used for conversion under different characteristic curves in different color

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spaces. Mapping from Log to Rec709 belongs to this type. The color standards of computer monitors, televisions, mobile phones, and Pads that we come into contact with in work and life are very close to Rec.709. However, now a large number of cameras and even SLRs can shoot log (Log) video. If the log video is sent to the Rec.709 standard monitor for monitoring, it cannot be restored normally. The fundamental reason is that the gamma difference between the two is very large, so it needs to be artificially corrected to the display system gamma.

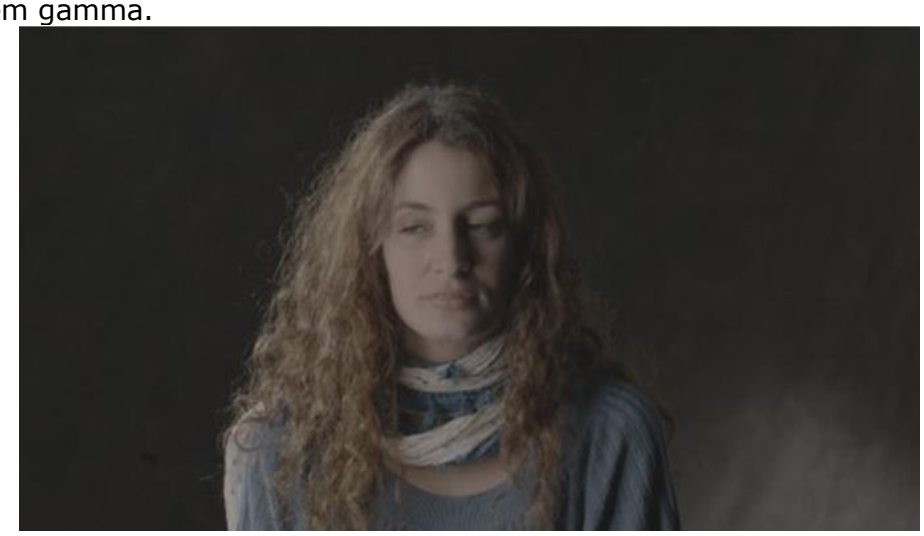


Fig. 11-31 Effect picture before correction



Fig. 11-32 Effect picture after correction

(3) Style (Creative LUT/Looks LUT)

In order to realize a certain style of LUT, the LUT produced by the director of photography during the pre-shooting and can be previewed on-site. Using LUT to calibrate the color of the monitor does not creatively process the video. Another type of use of LUT is to color, that is, creatively process the video.

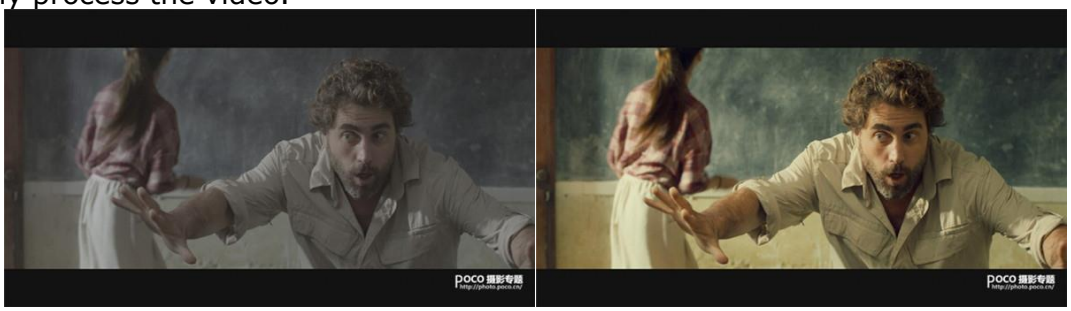


Fig. 11-33 Effect picture before and after toning

Comparison of 3D LUT before (left) and after (right) toning

Application and configuration

In the application, user can adjust the required scene effects through the 3D LUT Creator software and save the 3D LUT table configuration corresponding to 9x9x9 or 17x17x17 to

the address corresponding to the VOP.

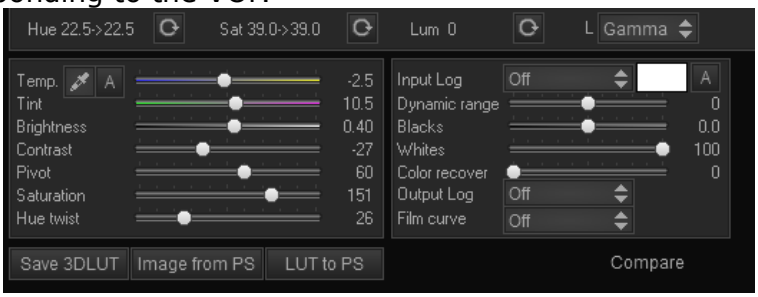


Fig. 11-34 Basic operation interface of 3D LUT Creator

For example, for a 9x9x9 LUT table, a 729-point constant needs to be written to the corresponding memory, which can be written through AXI or AHB. The arrangement is as follows:

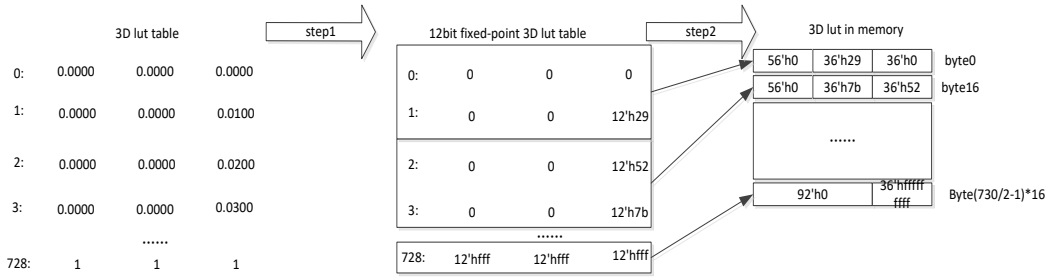


Fig. 11-35 3D LUT table sorting diagram

Note: Only port0 support 3dlut.

11.4.6.10 SHARP

The main function of this system is to enhance image details and support configuring different strengths of gain for details of different scales and directions. The strength of detail enhancement can be controlled based on the image content, including local gradients, brightness, and variance information. Additionally, it supports controlling the strength of detail enhancement for different color channels of the input.

Note:

1. Only post0 support sharp.
2. Sharp and post scale can not be used at the same time.
3. Sharp and post split can not be used at the same time.

11.4.6.11 Timing description

A. Progressive timing configuration

The POST*_PROC registers need to configure:

- VOP_DSP_HTOTAL_HS_END
- VOP_DSP_HACT_ST_END
- VOP_DSP_VTOTAL_VS_END
- VOP_DSP_VACT_ST_END

B. p timing chart example

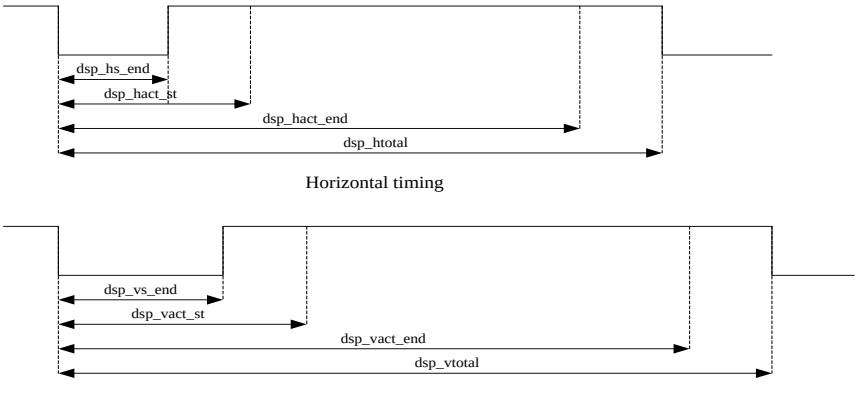


Fig. 11-36 VOP RGB interface timing diagram (progressive mode)

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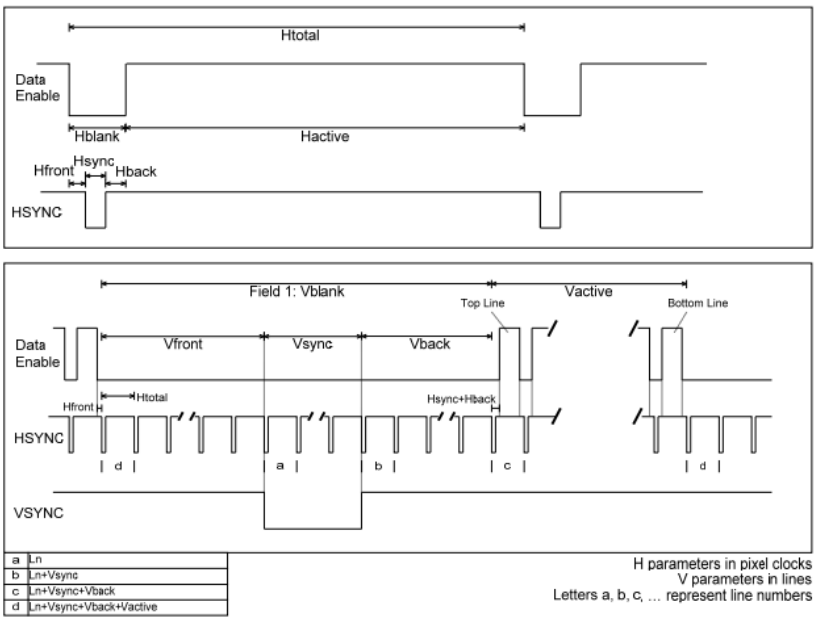


Fig. 11-37 CTA-861 standard timing diagram (progressive mode)

C. Interlace timing configuration

Need to configure the following timing registers:

- VOP_DSP_HTOTAL_HS_END
- VOP_DSP_HACT_ST_END
- VOP_DSP_VTOTAL_VS_END
- VOP_DSP_VACT_ST_END
- VOP_DSP_VS_ST_END_F1
- VOP_DSP_VACT_ST_END_F1

D. i timing chart example

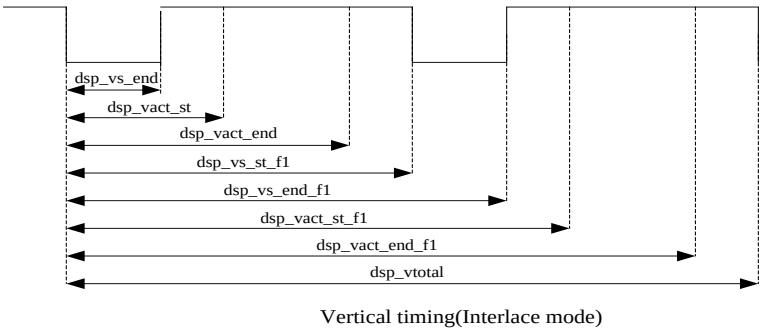


Fig. 11-38 VOP RGB interface timing diagram (interlace mode)

Points to note, the starting point of the second field is at 1/2 of htotal.

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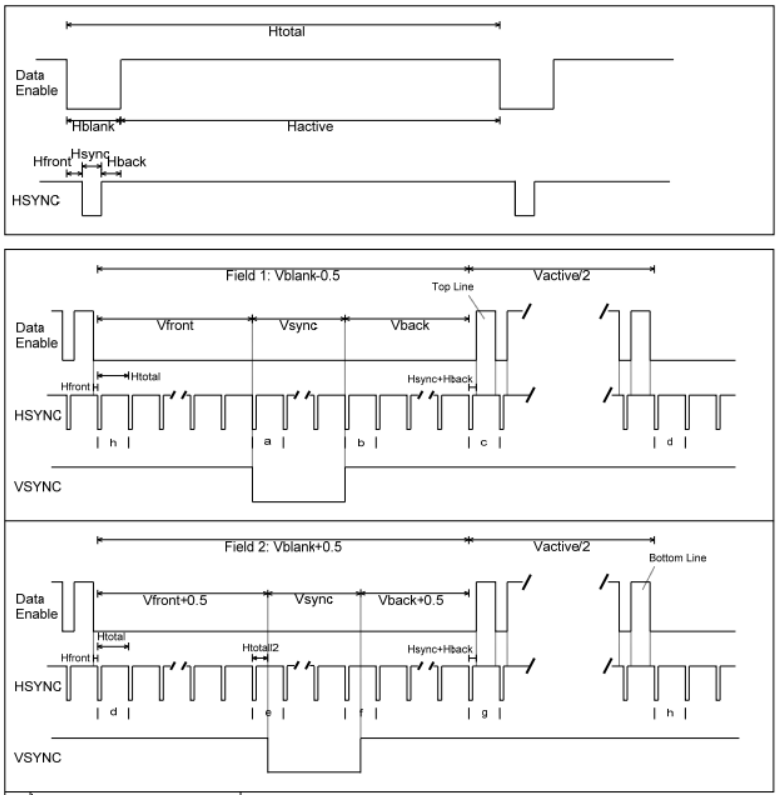


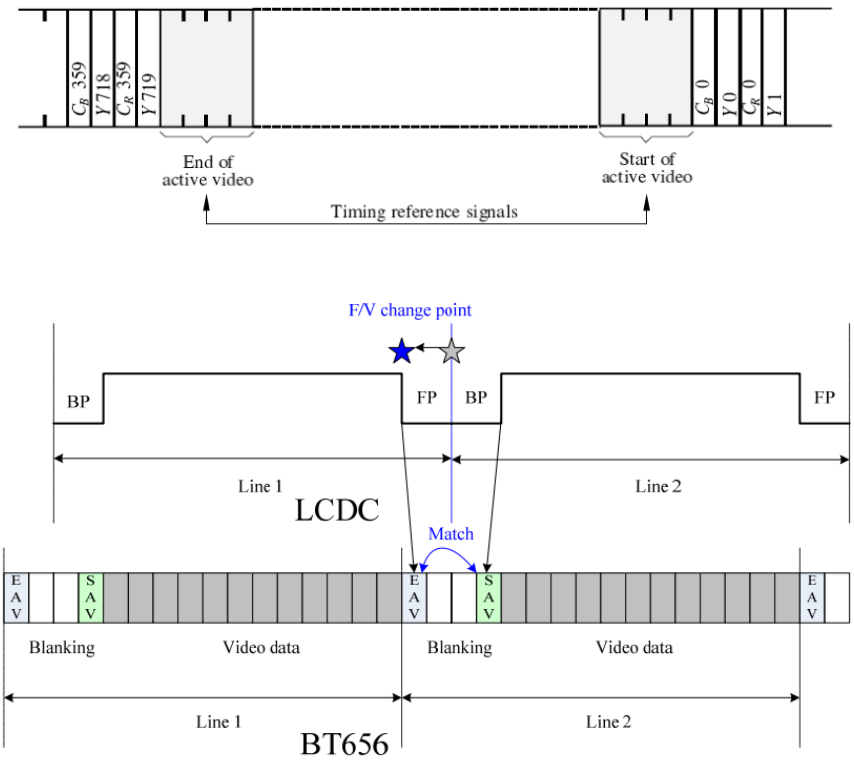
Fig. 11-39 CTA-861 standard timing diagram (interlace mode)

E. BT.656 encoder

VOP extracts the BT656 encoder module separately, the input interface is RGB parallel timing input, and the output is the standard bt656 interface output.

BT656 embeds the line and field synchronization information into the data stream in the form of encoding, which is the so-called Video timing reference codes. Each line includes four parts: SAV, EAV, blanking and video data:

每一行包括SAV、EAV、blanking和video data四个部分：



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Fig. 11-40 Timing description of BT656

F. BT.1120 encoder

The encoding method is almost the same as BT656, except that the number of data bits increases and the frequency becomes larger to support the transmission of HD data. Maximum support for data transmission up to 1080p, DCLK to 150M. Supports both interlace and progressive transmission at the same time. The specific timing diagram is as follows.

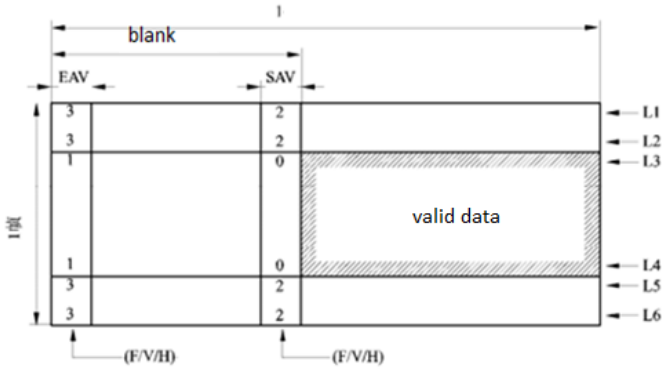


Fig. 11-41 Timing description of BT1120

G. MCU LCD Interface timing

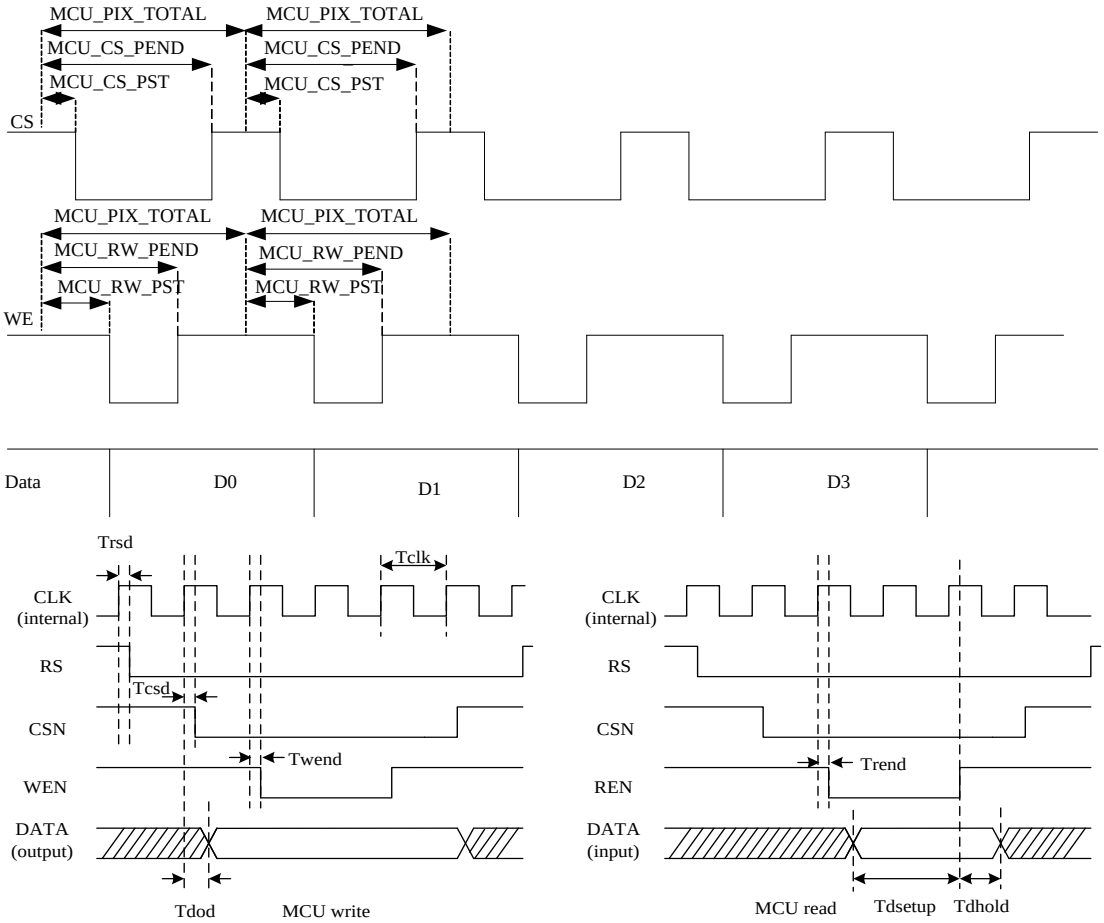


Fig. 11-42 LCDC MCU interface (i80) timing

H. Pre_scan_active

Pre_scan_active define that layers send the read data request early vop post readpixel data in post line buff.

$$Pre_scan_hactive = pre_scan_max_dly + act_width/2 - 1$$

Note: Pre_scan_max define in HDR mode delay set part and Overlay part.
Note: When act_width don't align 2, set act_width' = act_width+1.

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Note: Recommend time parameter of 2 pixel align, it must set 2pixel align when post in split mode.

11.5 Register Description

11.5.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 11-6 VOP Address Mapping

Base Address[15:8]	Module	Address Length	Offset Address Range
0x00	SYS_CTRL	512 BYTE	0X0000 ~ 0X01FF
0x05	OVERLAY_SYSTEM	256 BYTE	0X0500 ~ 0X05FF
0x06	OVERLAY_PORT0	256 BYTE	0X0600 ~ 0X06FF
0x07	OVERLAY_PORT1	256 BYTE	0X0700 ~ 0X07FF
0x08	OVERLAY_PORT2	256 BYTE	0X0800 ~ 0X08FF
0x0c	POST0	256 BYTE	0X0C00 ~ 0X0CFF
0x0d	POST1	256 BYTE	0X0D00 ~ 0X0DFF
0x0e	POST2	256 BYTE	0X0E00 ~ 0X0EFF
0x10	CLUSTER0	512 BYTE	0X1000 ~ 0X11FF
0x12	CLUSTER1	512 BYTE	0X1200 ~ 0X13FF
0x18	ESMART0	512 BYTE	0X1800 ~ 0X19FF
0x1a	ESMART1	512 BYTE	0X1A00 ~ 0X1BFF
0x1c	ESMART2	512 BYTE	0X1C00 ~ 0X1DFF
0x1e	ESMART3	512 BYTE	0X1E00 ~ 0X1FFF
0x20	HDR_VIVID	4096 BYTE	0X2000 ~ 0X2FFF
0x50	GAMMA_LUT_ADDR	4096 BYTE	0X5000 ~ 0X5FFF
0x60	BPP_LUT_ADDR	1024 BYTE	0X6000 ~ 0X63FF
0x64	ACM	2048 BYTE	0X6400 ~ 0X6BFF
0x6c	SHARP	768 BYTE	0X6C00 ~ 0X6FFF
0x7e	MMU0	256 BYTE	0X7E00 ~ 0X7EFF
0x7f	MMU1	256 BYTE	0X7F00 ~ 0X7FFF

11.5.2 Registers Summar

11.5.2.1 SYS_CTRL

Name	Offset	Size	Reset Value	Description
SYS_CTRL_SYS_REG_CFG_DONE	0x0000	W	0x00008000	Register configure done flag.
SYS_CTRL_SYS_VERSION_INFO	0x0004	W	0x50199765	RTL version.
SYS_CTRL_SYS_AUTO_GATING_CTRL_IMD	0x0008	W	0x8155E953	To control auto-gating.
SYS_CTRL_SYS_WIN_REG_CFG_DONE	0x000C	W	0x00000000	Layer Register configure done flag.
SYS_CTRL_SYS_AXI0_CTRL_IMD	0x0010	W	0x00000000	To control AXI.
SYS_CTRL_SYS_AXI_HURRY_CTRL0_IMD	0x0014	W	0x00000000	To control AXI0 hurry mode.

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Name	Offset	Size	Reset Value	Description
SYS_CTRL_SYS_AXI_HURRY_CTRL1_IMD	0x0018	W	0x00000000	To control AXI1 hurry mode.
SYS_CTRL_SYS_AXI1_CTRL_IMD	0x001C	W	0x00000000	To control AXI.
SYS_CTRL_SYS_MMU_CTRL_IMD	0x0020	W	0x00000800	To MMU CTRL register.
SYS_CTRL_SYS_AXI_LUT_CTRL_IMD	0x0024	W	0x00000210	To control the DMA of fetching LUT.
SYS_CTRL_SYS_PORT_CTRL_IMD	0x0028	W	0x00000037	To vop_post ctrl.
SYS_CTRL_SYS_CLUSTER_PD_CTRL_IMD	0x0030	W	0x00000000	To cluster layer pd ctrl
SYS_CTRL_SYS_ESMART_PD_CTRL_IMD	0x0034	W	0x000000C0	To esmart layer pd ctrl
SYS_CTRL_SYS_VAR_FERQ_CTRL_IMD	0x0038	W	0x00000000	The address is used to bypass MCU command.
SYS_CTRL_METADATA_CTRL	0x0040	W	0x00000024	To metadata ctrl.
SYS_CTRL_METADATA_MST	0x0044	W	0x00000000	Metadata address.
SYS_CTRL_FBCD_TIMEOUT_CTRL	0x0048	W	0x00000000	FBCD timeout ctrl.
SYS_CTRL_VOP_IO_VSYNC_CTRL	0x004C	W	0x0000003F	Vsync signal ouput to io.
SYS_CTRL_SYS_LUT_PORT_SEL	0x0058	W	0x0000F800	To select the video output for LUT.
SYS_CTRL_SYS_STATUS0	0x0060	W	0x00000000	The system status of video output0.
SYS_CTRL_SYS_STATUS1	0x0064	W	0x00000000	The system status of video output1.
SYS_CTRL_SYS_STATUS2	0x0068	W	0x00000000	The system status of video output2.
SYS_CTRL_SYS_LINE_FLAG0	0x0070	W	0x60000000	To set the line flag of video output0.
SYS_CTRL_SYS_LINE_FLAG1	0x0074	W	0x60000000	To set the line flag of video output1.
SYS_CTRL_SYS_LINE_FLAG2	0x0078	W	0x60000000	To set the line flag of video output2.
SYS_CTRL_SYS0_INTR_EN	0x0080	W	0x00000000	To enable system0 interrupt.
SYS_CTRL_SYS0_INTR_CLR	0x0084	W	0x00000000	To clear system0 interrupt.
SYS_CTRL_SYS0_INTR_STATUS	0x0088	W	0x00000000	System0 interrupt status.
SYS_CTRL_SYS0_INTR_RAW_STATUS	0x008C	W	0x00000000	System0 interrupt raw status.
SYS_CTRL_SYS1_INTR_EN	0x0090	W	0x00000000	To enable system1 interrupt.
SYS_CTRL_SYS1_INTR_CLR_SYS	0x0094	W	0x00000000	To clear system1 interrupt.
SYS_CTRL_SYS1_INTR_STATUS	0x0098	W	0x00000000	System1 interrupt status.
SYS_CTRL_SYS1_INTR_RAW_STATUS	0x009C	W	0x00000000	System1 interrupt raw status.

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Name	Offset	Size	Reset Value	Description
SYS_CTRL_PORT0_INTR_EN	0x00A0	W	0x00000000	To enable video output0 interrupt.
SYS_CTRL_PORT0_INTR_CLR	0x00A4	W	0x00000000	To clear video output0 interrupt.
SYS_CTRL_PORT0_INTR_STATUS	0x00A8	W	0x00000000	Video output0 interrupt status.
SYS_CTRL_PORT0_INTR_RAW_STATUS	0x00AC	W	0x00000000	Video output0 interrupt raw status.
SYS_CTRL_PORT1_INTR_EN	0x00B0	W	0x00000000	To enable video output1 interrupt.
SYS_CTRL_PORT1_INTR_CLR	0x00B4	W	0x00000000	To clear video output1 interrupt.
SYS_CTRL_PORT1_INTR_STATUS	0x00B8	W	0x00000000	Video output1 interrupt status.
SYS_CTRL_PORT1_INTR_RAW_STATUS	0x00BC	W	0x00000000	Video output1 interrupt raw status.
SYS_CTRL_PORT2_INTR_EN	0x00C0	W	0x00000000	To enable video output2 interrupt.
SYS_CTRL_PORT2_INTR_CLR	0x00C4	W	0x00000000	To clear video output2 interrupt.
SYS_CTRL_PORT2_INTR_STATUS	0x00C8	W	0x00000000	Video output2 interrupt status.
SYS_CTRL_PORT2_INTR_RAW_STATUS	0x00CC	W	0x00000000	Video output2 interrupt raw status.
SYS_CTRL_FBCD_INTR_EN0	0x00E0	W	0x00000000	To enable fbcd decode interrupt.
SYS_CTRL_FBCD_INTR_CLR0	0x00E4	W	0x00000000	To clear fbcd decode interrupt.
SYS_CTRL_FBCD_INTR_STATUS0	0x00E8	W	0x00000000	Fbcd interrupt status.
SYS_CTRL_FBCD_INTR_RAW_STATUS0	0x00EC	W	0x00000000	Fbcd interrupt raw status.
SYS_CTRL_SYS_WB_CTRL0	0x0100	W	0x02100000	To control WB.
SYS_CTRL_SYS_WB_XSPD_FACTOR	0x0104	W	0x10000030	To configure the scale factor of WB.
SYS_CTRL_SYS_WB_YRGB_MST	0x0108	W	0x00000000	WB YRGB memory starting address.
SYS_CTRL_SYS_WB_CBR_MST	0x010C	W	0x00000000	WB CbCr memory starting address.
SYS_CTRL_SYS_WB_VIR_STRIDE	0x0110	W	0x00000000	To enable optional fucntion.
SYS_CTRL_SYS_WB_TIMEOUT_CTRL	0x0114	W	0x00001F40	To WB time out cnt.
SYS_CTRL_MIPI0_INFACE_CTRL	0x0180	W	0x80000030	To MIPI0 interface ctrl.
SYS_CTRL_HDMI0_INFACE_CTRL	0x0184	W	0x80000000	To HDMI0 interface ctrl.
SYS_CTRL_EDP0_INFACE_CTRL	0x0188	W	0x80000000	To EDP0 interface ctrl.
SYS_CTRL_DP0_INFACE_CTRL	0x018C	W	0x80000000	To DP0 interface ctrl.
SYS_CTRL_RGB_INFACE_CTRL	0x0194	W	0x80000000	To RGB interface ctrl.

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Name	Offset	Size	Reset Value	Description
SYS_CTRL_DP1_INFACE_CTRL	0x01A4	W	0x80000000	To DP1 interface ctrl.
SYS_CTRL_DP2_INFACE_CTRL	0x01B0	W	0x80000000	To DP2 interface ctrl.
SYS_CTRL_SEC_DRM_CTRL	0x01E0	W	0x00000000	VOP secure information config.
SYS_CTRL_SEC_DRM_PORT_SEL	0x01E4	W	0x00000000	VOP layer sel secure port.
SYS_CTRL_SEC_PORT0_LAYER_SEL	0x01E8	W	0x00000000	Video output0 secure layer sel.
SYS_CTRL_SEC_PORT1_LAYER_SEL	0x01EC	W	0x00000000	Video output1 secure layer sel.
SYS_CTRL_SEC_PORT2_LAYER_SEL	0x01F0	W	0x00000000	Video output2 secure layer sel.
SYS_CTRL_SEC_AXI_RID_PROT	0x01F8	W	0x00000000	VOP axi secure rid.
SYS_CTRL_SYS_OTP_MIRR_CTRL_IMD	0x01FC	W	0x00000000	To disable optional function.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.5.2.2 OVERLAY_SYSTEM

Name	Offset	Size	Reset Value	Description
OVERLAY_SYSTEM_EXTRA_ALPHA_CTRL_IMD	0x0000	W	0x00000000	To vop extra mix enable.
OVERLAY_SYSTEM_CLUSTER0_SRC_COLOR_CTRL	0x0030	W	0x00000000	Cluster0_mix configure the source color.
OVERLAY_SYSTEM_CLUSTER0_DST_COLOR_CTRL	0x0034	W	0x00000000	Cluster0_mixconfigure the destination color.
OVERLAY_SYSTEM_CLUSTER0_SRC_ALPHA_CTRL	0x0038	W	0x00000000	Cluster0_mixconfigure the source alpha.
OVERLAY_SYSTEM_CLUSTER0_DST_ALPHA_CTRL	0x003C	W	0x00000000	Cluster0_mixconfigure the destination alpha.
OVERLAY_SYSTEM_CLUSTER1_SRC_COLOR_CTRL	0x0040	W	0x00000000	Cluster1_mix configure the source color.
OVERLAY_SYSTEM_CLUSTER1_DST_COLOR_CTRL	0x0044	W	0x00000000	Cluster1_mixconfigure the destination color.
OVERLAY_SYSTEM_CLUSTER1_SRC_ALPHA_CTRL	0x0048	W	0x00000000	Cluster1_mixconfigure the source alpha.
OVERLAY_SYSTEM_CLUSTER1_DST_ALPHA_CTRL	0x004C	W	0x00000000	Cluster1_mixconfigure the destination alpha.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.5.2.3 OVERLAY_PORT0

Name	Offset	Size	Reset Value	Description
OVERLAY_PORT0_OVERLAY_CTRL	0x0000	W	0x00000000	Overlay_ctrl config set.
OVERLAY_PORT0_LAYER_SEL	0x0004	W	0x0000FFFF	Overlay_Layer_select
OVERLAY_PORT0_MIX0_SRC_COLOR_CTRL	0x0020	W	0x00000000	MIX0 configure the source color.
OVERLAY_PORT0_MIX0_DST_COLOR_CTRL	0x0024	W	0x00000000	MIX0 configure the destination color.
OVERLAY_PORT0_MIX0_SRC_ALPHA_CTRL	0x0028	W	0x00000000	MIX0 configure the source alpha.

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Name	Offset	Size	Reset Value	Description
OVERLAY_PORT0_MIX0_DST_ALPHA_CTRL	0x002C	W	0x00000000	MIX0 configure the destination alpha.
OVERLAY_PORT0_MIX1_SRC_COLOR_CTRL	0x0030	W	0x00000000	MIX1 configure the source color.
OVERLAY_PORT0_MIX1_DST_COLOR_CTRL	0x0034	W	0x00000000	MIX1 configure the destination color.
OVERLAY_PORT0_MIX1_SRC_ALPHA_CTRL	0x0038	W	0x00000000	MIX1 configure the source alpha.
OVERLAY_PORT0_MIX1_DST_ALPHA_CTRL	0x003C	W	0x00000000	MIX1 configure the destination alpha.
OVERLAY_PORT0_MIX2_SRC_COLOR_CTRL	0x0040	W	0x00000000	MIX2 configure the source color.
OVERLAY_PORT0_MIX2_DST_COLOR_CTRL	0x0044	W	0x00000000	MIX2 configure the destination color.
OVERLAY_PORT0_MIX2_SRC_ALPHA_CTRL	0x0048	W	0x00000000	MIX2 configure the source alpha.
OVERLAY_PORT0_MIX2_DST_ALPHA_CTRL	0x004C	W	0x00000000	MIX2 configure the destination alpha.
OVERLAY_PORT0_EXTRA_SRC_COLOR_CTRL	0x0050	W	0x00000000	EXTRA_MIX configure the source color.
OVERLAY_PORT0_EXTRA_DST_COLOR_CTRL	0x0054	W	0x00000000	EXTRA_MIX configure the destination color
OVERLAY_PORT0_EXTRA_SRC_ALPHA_CTRL	0x0058	W	0x00000000	EXTRA_MIX configure the source alpha
OVERLAY_PORT0_EXTRA_DST_ALPHA_CTRL	0x005C	W	0x00000000	EXTRA_MIX configure the destination alpha
OVERLAY_PORT0_HDR_SRC_COLOR_CTRL	0x0060	W	0x00000000	HDR_MIX configure the source color.
OVERLAY_PORT0_HDR_DST_COLOR_CTRL	0x0064	W	0x00000000	HDR_MIX configure the destination color.
OVERLAY_PORT0_HDR_SRC_ALPHA_CTRL	0x0068	W	0x00000000	HDR_MIX configure the source alpha.
OVERLAY_PORT0_HDR_DST_ALPHA_CTRL	0x006C	W	0x00000000	HDR_MIX configure the destination alpha.
OVERLAY_PORT0_BG_MIX_CTRL	0x0070	W	0x10000000	OVERLAY_port0 delay_num.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.5.2.4 OVERLAY_PORT1

Name	Offset	Size	Reset Value	Description
OVERLAY_PORT1_OVERLAY_CTRL	0x0000	W	0x00000000	Overlay_ctrl config set.
OVERLAY_PORT1_LAYER_SEL	0x0004	W	0x0000FFFF	Overlay_Layer_select.
OVERLAY_PORT1_MIX0_SRC_COLOR_CTRL	0x0020	W	0x00000000	MIX0 configure the source color.
OVERLAY_PORT1_MIX0_DST_COLOR_CTRL	0x0024	W	0x00000000	MIX0 configure the destination color.
OVERLAY_PORT1_MIX0_SRC_ALPHA_CTRL	0x0028	W	0x00000000	MIX0 configure the source alpha.
OVERLAY_PORT1_MIX0_DST_ALPHA_CTRL	0x002C	W	0x00000000	MIX0 configure the destination alpha.
OVERLAY_PORT1_MIX1_SRC_COLOR_CTRL	0x0030	W	0x00000000	MIX1 configure the source color.

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Name	Offset	Size	Reset Value	Description
OVERLAY_PORT1_MIX1_DST_COLOR_CTRL	0x0034	W	0x00000000	MIX1 configure the destination color.
OVERLAY_PORT1_MIX1_SRC_ALPHA_CTRL	0x0038	W	0x00000000	MIX1 configure the source alpha.
OVERLAY_PORT1_MIX1_DST_ALPHA_CTRL	0x003C	W	0x00000000	MIX1 configure the destination alpha.
OVERLAY_PORT1_MIX2_SRC_COLOR_CTRL	0x0040	W	0x00000000	MIX2 configure the source color.
OVERLAY_PORT1_MIX2_DST_COLOR_CTRL	0x0044	W	0x00000000	MIX2 configure the destination color.
OVERLAY_PORT1_MIX2_SRC_ALPHA_CTRL	0x0048	W	0x00000000	MIX2 configure the source alpha.
OVERLAY_PORT1_MIX2_DST_ALPHA_CTRL	0x004C	W	0x00000000	MIX2 configure the destination alpha.
OVERLAY_PORT1_BG_MIX_CTRL	0x0070	W	0x0A000000	OVERLAY_port0 delay_num.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.5.2.5 OVERLAY_PORT2

Name	Offset	Size	Reset Value	Description
OVERLAY_PORT2_OVERLAY_CTRL	0x0000	W	0x00000000	Overlay_ctrl config set.
OVERLAY_PORT2_LAYER_SEL	0x0004	W	0x0000FFFF	Overlay_Layer_select.
OVERLAY_PORT2_MIX0_SRC_COLOR_CTRL	0x0020	W	0x00000000	MIX0 configure the source color.
OVERLAY_PORT2_MIX0_DST_COLOR_CTRL	0x0024	W	0x00000000	MIX0 configure the destination color.
OVERLAY_PORT2_MIX0_SRC_ALPHA_CTRL	0x0028	W	0x00000000	MIX0 configure the source alpha.
OVERLAY_PORT2_MIX0_DST_ALPHA_CTRL	0x002C	W	0x00000000	MIX0 configure the destination alpha.
OVERLAY_PORT2_MIX1_SRC_COLOR_CTRL	0x0030	W	0x00000000	MIX1 configure the source color.
OVERLAY_PORT2_MIX1_DST_COLOR_CTRL	0x0034	W	0x00000000	MIX1 configure the destination color.
OVERLAY_PORT2_MIX1_SRC_ALPHA_CTRL	0x0038	W	0x00000000	MIX1 configure the source alpha.
OVERLAY_PORT2_MIX1_DST_ALPHA_CTRL	0x003C	W	0x00000000	MIX1 configure the destination alpha.
OVERLAY_PORT2_MIX2_SRC_COLOR_CTRL	0x0040	W	0x00000000	MIX2 configure the source color.
OVERLAY_PORT2_MIX2_DST_COLOR_CTRL	0x0044	W	0x00000000	MIX2 configure the destination color.
OVERLAY_PORT2_MIX2_SRC_ALPHA_CTRL	0x0048	W	0x00000000	MIX2 configure the source alpha.
OVERLAY_PORT2_MIX2_DST_ALPHA_CTRL	0x004C	W	0x00000000	MIX2 configure the destination alpha.
OVERLAY_PORT2_BG_MIX_CTRL	0x0070	W	0x00000000	OVERLAY_port0 delay_num.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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11.5.2.6 POST0_CTRL

Name	Offset	Size	Reset Value	Description
POST0_CTRL_POST_DSP_CTRL	0x0000	W	0x8000000F	To control the display mode of video output0.
POST0_CTRL_POST_MIPI_CTRL	0x0004	W	0x00000000	To control the MIPI display of video output0.
POST0_CTRL_POST_COLOR_CTRL	0x0008	W	0x00000000	To control color bar.
POST0_CTRL_POST_CORE_CLK	0x000C	W	0x00000000	To post core clk sel
POST0_CTRL_POST_3D_LUT_CTRL	0x0010	W	0x00000010	To control 3D LUT.
POST0_CTRL_POST_3D_LUT_R	0x0014	W	0x00000000	To configure the red component of 3D LUT.
POST0_CTRL_POST_3D_LUT_G	0x0018	W	0x00000000	To configure the green component of 3D LUT.
POST0_CTRL_POST_3D_LUT_B	0x001C	W	0x00000000	To configure the blue component of 3D LUT.
POST0_CTRL_POST_3DLUT_MST	0x0020	W	0x00000000	To configure the starting address of 3D LUT in memory.
POST0_CTRL_POST_DSP_BG	0x002C	W	0x80000000	To configure the background color of video output0.
POST0_CTRL_POST_PRESCAN_HTIMING	0x0030	W	0x00000000	To configure the pre-process timing of video output0.
POST0_CTRL_POST_DSP_HACT_INFO	0x0034	W	0x00000000	To configure the post-process horizontal timing of video output port0.
POST0_CTRL_POST_DSP_VACT_INFO	0x0038	W	0x00000000	To configure the post-process vertical timing of video output port0.
POST0_CTRL_POST_SCL_FACTOR_YRGB	0x003C	W	0x00000000	To configure the post-process vertical timing of video output port0.
POST0_CTRL_POST_SCL_CTRL	0x0040	W	0x00000010	Post_scale_ctrl and post_check out enable.
POST0_CTRL_POST_DSP_VACT_INFO_F1	0x0044	W	0x00000000	To configure the interlace vertical timing of video output0.
POST0_CTRL_POST_DSP_HTOTAL_HS_END	0x0048	W	0x032000C8	To configure the horizontal timing of video output0.
POST0_CTRL_POST_DSP_HACT_ST_END	0x004C	W	0x01900258	To configure the horizontal timing of video output0.
POST0_CTRL_POST_DSP_VTOTAL_VS_END	0x0050	W	0x00FA000A	To configure the vertical timing of video output0.
POST0_CTRL_POST_DSP_VACT_ST_END	0x0054	W	0x000A00FA	To configure the vertical timing of video output0.
POST0_CTRL_POST_DSP_VS_ST_END_F1	0x0058	W	0x00000000	To configure the interlace vertical timing of video output0.
POST0_CTRL_POST_DSP_VACT_ST_END_F1	0x005C	W	0x00000000	To configure the interlace vertical timing of video output0.
POST0_CTRL_POST_DITHER_FRC_0	0x00A0	W	0x00000000	To configure the filter coefficients of DB.
POST0_CTRL_POST_DITHER_FRC_1	0x00A4	W	0x01000100	To configure the filter coefficients of DB.
POST0_CTRL_POST_DITHER_FRC_2	0x00A8	W	0x00000100	To configure the filter coefficients of DB.

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Name	Offset	Size	Reset Value	Description
POST0_CTRL_POST_ACM_CTRL	0x00D0	W	0x00000001	To configure acm y2r/y2r/acm_en.
POST0_CTRL_POST_ACM_Y2R_COE0102	0x00D4	W	0x00000000	To configure Y2R coe01 and coe02.
POST0_CTRL_POST_ACM_Y2R_COE1011	0x00D8	W	0x00000000	To configure Y2R coe10 and coe11.
POST0_CTRL_POST_ACM_Y2R_COE1220	0x00DC	W	0x00000000	To configure Y2R coe12 and coe20.
POST0_CTRL_POST_ACM_Y2R_COE2122	0x00E0	W	0x00000000	To configure Y2R coe21 and coe22.
POST0_CTRL_POST_ACM_Y2R_OFFSET0	0x00E4	W	0x00000000	To configure Y2R offset0.
POST0_CTRL_POST_ACM_Y2R_OFFSET1	0x00E8	W	0x00000000	To configure Y2R offset1.
POST0_CTRL_POST_ACM_Y2R_OFFSET2	0x00EC	W	0x00000000	To configure Y2R offset2.
POST0_CTRL_POST_CLK_CNT	0x00F4	W	0x00000000	To post empty clk cnt.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.5.2.7 POST1_CTRL

Name	Offset	Size	Reset Value	Description
POST1_CTRL_POST_DSP_CTRL	0x0000	W	0x8000000F	To control the display mode of video output1.
POST1_CTRL_POST_MIPI_CTRL	0x0004	W	0x00000000	To control the MIPI display of video output1.
POST1_CTRL_POST_COLOR_CTRL	0x0008	W	0x00000000	To control color bar.
POST1_CTRL_POST_CORE_CLK	0x000C	W	0x00000000	To post core clk sel.
POST1_CTRL_POST_DSP_BG	0x002C	W	0x80000000	To configure the background color of video output1.
POST1_CTRL_POST_PRESCAN_HTIMING	0x0030	W	0x00000000	To configure the pre-process timing of video output1.
POST1_CTRL_POST_DSP_HACT_INFO	0x0034	W	0x00000000	To configure the post-process horizontal timing of video output port1.
POST1_CTRL_POST_DSP_VACT_INFO	0x0038	W	0x00000000	To configure the post-process vertical timing of video output port1.
POST1_CTRL_POST_SCL_FACTOR_YRGB	0x003C	W	0x00000000	To configure the post-process vertical timing of video output port1.
POST1_CTRL_POST_SCL_CTRL	0x0040	W	0x00000010	Post_scale_ctrl and post_check out enable.
POST1_CTRL_POST_DSP_VACT_INFO_F1	0x0044	W	0x00000000	To configure the interlace vertical timing of video output1.
POST1_CTRL_POST_DSP_HTOTAL_HS_END	0x0048	W	0x032000C8	To configure the horizontal timing of video output1.
POST1_CTRL_POST_DSP_HACT_ST_END	0x004C	W	0x01900258	To configure the horizontal timing of video output1.
POST1_CTRL_POST_DSP_VTOTAL_VS_END	0x0050	W	0x00FA000A	To configure the vertical timing of video output1.

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Name	Offset	Size	Reset Value	Description
POST1_CTRL_POST_DSP_VACT_ST_END	0x0054	W	0x000A00FA	To configure the vertical timing of video output1.
POST1_CTRL_POST_DSP_VS_ST_END_F1	0x0058	W	0x00000000	To configure the interlace vertical timing of video output1.
POST1_CTRL_POST_DSP_VACT_ST_END_F1	0x005C	W	0x00000000	To configure the interlace vertical timing of video output1.
POST1_CTRL_POST_BCSH_CTRL	0x0060	W	0x00000000	To control BCSH.
POST1_CTRL_POST_BCSH_BCS	0x0064	W	0x00000000	To configure the brightness, contrast, sat and output mode of BCSH.
POST1_CTRL_POST_BCSH_H	0x0068	W	0x00000000	To configure the hue of BCSH.
POST1_CTRL_POST_BCSH_COLOR_BAR	0x006C	W	0x00000000	To enable BCSH.
POST1_CTRL_POST_DITHER_FRC_0	0x00A0	W	0x00000000	To configure the filter coefficients of DB.
POST1_CTRL_POST_DITHER_FRC_1	0x00A4	W	0x01000100	To configure the filter coefficients of DB.
POST1_CTRL_POST_DITHER_FRC_2	0x00A8	W	0x00000100	To configure the filter coefficients of DB.
POST1_CTRL_POST_CLK_CNT	0x00F4	W	0x00000000	To post empty clk cnt.
POST1_CTRL_POST_MCU_CTRL	0x00F8	W	0x00711C08	To post mcu ctrl.
POST1_CTRL_POST_MCU_RW_BYPASS	0x00FC	W	0x00000000	MCU write bypass data

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.5.2.8 POST2_CTRL

Name	Offset	Size	Reset Value	Description
POST2_CTRL_POST_DSP_CTRL	0x0000	W	0x8000000F	To control the display mode of video output2.
POST2_CTRL_POST_MIPI_CTRL	0x0004	W	0x00000000	To control the MIPI display of video output2.
POST2_CTRL_POST_COLOR_CTRL	0x0008	W	0x00000000	To control color bar.
POST2_CTRL_POST_CORE_CLK	0x000C	W	0x00000000	To post core clk sel.
POST2_CTRL_POST_DSP_BG	0x002C	W	0x80000000	To configure the background color of video output2.
POST2_CTRL_POST_PRESCAN_HTIMING	0x0030	W	0x00000000	To configure the pre-process timing of video output2.
POST2_CTRL_POST_DSP_HACT_INFO	0x0034	W	0x00000000	To configure the post-process horizontal timing of video output port2.
POST2_CTRL_POST_DSP_VACT_INFO	0x0038	W	0x00000000	To configure the post-process vertical timing of video output port2.
POST2_CTRL_POST_SCL_FACTOR_YRGB	0x003C	W	0x00000000	To configure the post-process vertical timing of video output port2.
POST2_CTRL_POST_SCL_CTRL	0x0040	W	0x00000010	Post_scale_ctrl and post_check out enable.

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Name	Offset	Size	Reset Value	Description
POST2_CTRL_POST_DSP_VACT_INFO_F1	0x0044	W	0x00000000	To configure the interlace vertical timing of video output2.
POST2_CTRL_POST_DSP_HTOTAL_HS_END	0x0048	W	0x032000C8	To configure the horizontal timing of video output2.
POST2_CTRL_POST_DSP_HACT_ST_END	0x004C	W	0x01900258	To configure the horizontal timing of video output2.
POST2_CTRL_POST_DSP_VTOTAL_VS_END	0x0050	W	0x00FA000A	To configure the vertical timing of video output2.
POST2_CTRL_POST_DSP_VACT_ST_END	0x0054	W	0x000A00FA	To configure the vertical timing of video output2.
POST2_CTRL_POST_DSP_VS_ST_END_F1	0x0058	W	0x00000000	To configure the interlace vertical timing of video output2.
POST2_CTRL_POST_DSP_VACT_ST_END_F1	0x005C	W	0x00000000	To configure the interlace vertical timing of video output2.
POST2_CTRL_POST_BCSH_CTRL	0x0060	W	0x00000000	To control BCSH.
POST2_CTRL_POST_BCSH_BCS	0x0064	W	0x00000000	To configure the brightness, contrast, sat and output mode of BCSH.
POST2_CTRL_POST_BCSH_H	0x0068	W	0x00000000	To configure the hue of BCSH.
POST2_CTRL_POST_BCSH_COLOR_BAR	0x006C	W	0x00000000	To enable BCSH.
POST2_CTRL_POST_FRC_LOWER01_0	0x00A0	W	0x12844821	To configure the filter coefficients of FRC.
POST2_CTRL_POST_FRC_LOWER01_1	0x00A4	W	0x21488412	To configure the filter coefficients of FRC.
POST2_CTRL_POST_FRC_LOWER10_0	0x00A8	W	0xA55A9696	To configure the filter coefficients of FRC.
POST2_CTRL_POST_FRC_LOWER10_1	0x00AC	W	0x5AA56969	To configure the filter coefficients of FRC.
POST2_CTRL_POST_FRC_LOWER11_0	0x00B0	W	0xDEB77BED	To configure the filter coefficients of FRC.
POST2_CTRL_POST_FRC_LOWER11_1	0x00B4	W	0xED7BB7DE	To configure the filter coefficients of FRC.
POST2_CTRL_POST_CLK_CNT	0x00F4	W	0x00000000	To post empty clk cnt.
POST2_CTRL_POST_MCU_CTRL	0x00F8	W	0x00711C08	To post mcu ctrl.
POST2_CTRL_POST_MCU_RW_BYPASS	0x00FC	W	0x00000000	MCU write bypass data

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.5.2.9 CLUSTER0

Name	Offset	Size	Reset Value	Description
CLUSTER0_WIN0_CTRL0	0x0000	W	0x00000000	WIN0 control register0.
CLUSTER0_WIN0_CTRL1	0x0004	W	0x00000000	WIN0 control register1.
CLUSTER0_WIN0_CTRL2	0x0008	W	0x00000062	WIN0 control register2.
CLUSTER0_WIN0_YRGB_MST	0x0010	W	0x00000000	WIN0 YRGB memory starting.
CLUSTER0_WIN0_CBCR_MST	0x0014	W	0x00000000	WIN0 CBCR memory starting.
CLUSTER0_WIN0_VIR	0x0018	W	0x00000000	WIN0 virtual width.

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Name	Offset	Size	Reset Value	Description
CLUSTER0_WIN0_KEY_COLOR	0x001C	W	0x00000000	Config key_color of WIN0.
CLUSTER0_WIN0_ACT_INFO	0x0020	W	0x00000000	WIN0 actual information.
CLUSTER0_WIN0_DSP_INFO	0x0024	W	0x00000000	WIN0 display information.
CLUSTER0_WIN0_DSP_ST	0x0028	W	0x00000000	WIN0 display start.
CLUSTER0_WIN0_DSP_BG	0x002C	W	0x00000000	WIN0 display background.
CLUSTER0_WIN0_SCL_FACTOR_YRGB	0x0030	W	0x00000000	WIN0 yrgb scale factor.
CLUSTER0_WIN0_SCL_OFFSET	0x0038	W	0x00000000	WIN0 scale offset.
CLUSTER0_WIN0_TRANSFORMED_OFFSET	0x003C	W	0x00000000	WIN0 transform offset
CLUSTER0_WIN0_ZME_CTRL	0x0040	W	0x00000000	WIN0 zme ctrl.
CLUSTER0_WIN0_ZME_DERING_PARA	0x0044	W	0x04100C10	WIN0 zme dering parameter config.
CLUSTER0_WIN0_FBCD_OUTPUT_CTRL	0x0050	W	0x00000010	WIN0 fbcd control register.
CLUSTER0_WIN0_FBCD_MODE	0x0054	W	0x00000000	WIN0 fbcd mode
CLUSTER0_WIN0_FBCD_HDR_PTR	0x0058	W	0x00000000	WIN0 fbcd hdr pointer.
CLUSTER0_WIN0_FBCD_VIR_WIDTH	0x005C	W	0x00000000	WIN0 fbcd virtual width.
CLUSTER0_WIN0_FBCD_SIZE	0x0060	W	0x00000000	WIN0 fbcd size.
CLUSTER0_WIN0_FBCD_PIC_OFFSET	0x0064	W	0x00000000	WIN0 fbcd picture offset.
CLUSTER0_WIN0_FBCD_DIS_OFFSET	0x0068	W	0x00000000	WIN0 fbcd display offset.
CLUSTER0_WIN0_FBCD_CTRL	0x006C	W	0x00000000	WIN0 fbcd control.
CLUSTER0_WIN0_PLD_PTR_OFFSET	0x0078	W	0x00000000	WIN0 pld and head offset in ddr.
CLUSTER0_WIN0_PLD_PTR_RANGE	0x007C	W	0x00000000	WIN0 pld range mst.
CLUSTER0_WIN1_CTRL0	0x0080	W	0x00000000	WIN1 control register0.
CLUSTER0_WIN1_CTRL1	0x0084	W	0x00000000	WIN1 control register1.
CLUSTER0_WIN1_CTRL2	0x0088	W	0x000000A4	WIN1 control register2.
CLUSTER0_WIN1_YRGB_MST	0x0090	W	0x00000000	WIN1 YRGB memory starting.
CLUSTER0_WIN1_CBCR_MST	0x0094	W	0x00000000	WIN1 CBCR memory starting.
CLUSTER0_WIN1_VIR	0x0098	W	0x00000000	WIN1 virtual width.
CLUSTER0_WIN1_KEY_COLOR	0x009C	W	0x00000000	Config key_color of WIN1.
CLUSTER0_WIN1_ACT_INFO	0x00A0	W	0x00000000	WIN1 actual information.
CLUSTER0_WIN1_DSP_INFO	0x00A4	W	0x00000000	WIN1 display information.
CLUSTER0_WIN1_DSP_ST	0x00A8	W	0x00000000	WIN1 display start.

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Name	Offset	Size	Reset Value	Description
CLUSTER0_WIN1_DSP_BG	0x00AC	W	0x00000000	WIN1 display background.
CLUSTER0_WIN1_SCL_FACTOR_YRGB	0x00B0	W	0x00000000	WIN1 yrgb scale factor.
CLUSTER0_WIN1_SCL_OFFSET	0x00B8	W	0x00000000	WIN1 scale offset.
CLUSTER0_WIN1_TRANSFORMED_OFFSET	0x00BC	W	0x00000000	WIN1 transform offset
CLUSTER0_WIN1_ZME_CTRL	0x00C0	W	0x00000000	WIN1 zme ctrl.
CLUSTER0_WIN1_ZME_DERING_PARA	0x00C4	W	0x00000000	WIN1 zme dering parameter config.
CLUSTER0_WIN1_FBCD_MASK_EN	0x00D0	W	0x00000010	WIN1 fbcd control register.
CLUSTER0_WIN1_FBCD_MODE	0x00D4	W	0x00000000	WIN1 fbcd mode
CLUSTER0_WIN1_FBCD_HDR_PTR	0x00D8	W	0x00000000	WIN1 fbcd hdr pointer.
CLUSTER0_WIN1_FBCD_VIR_WIDTH	0x00DC	W	0x00000000	WIN1 fbcd virtual width.
CLUSTER0_WIN1_FBCD_SIZE	0x00E0	W	0x00000000	WIN1 fbcd size.
CLUSTER0_WIN1_FBCD_PIC_OFFSET	0x00E4	W	0x00000000	WIN1 fbcd picture offset.
CLUSTER0_WIN1_FBCD_DIS_OFFSET	0x00E8	W	0x00000000	WIN1 fbcd display offset.
CLUSTER0_WIN1_FBCD_CTRL	0x00EC	W	0x00000000	WIN1 fbcd control.
CLUSTER0_WIN1_PLD_PTR_OFFSET	0x00F8	W	0x00000000	WIN1 pld and head offset in ddr.
CLUSTER0_WIN1_PLD_PTR_RANGE	0x00FC	W	0x00000000	WIN1 pld range mst.
CLUSTER0_CLUSTER_CTRL	0x0100	W	0xA0000000	CLUSTER control register.
CLUSTER0_DCI_BLK_SIZE	0x0104	W	0x00000000	DCI block size
CLUSTER0_DCI_BLK_OFFSET	0x0108	W	0x00000000	DCI block offset
CLUSTER0_DCI_PIX_REGION	0x010C	W	0x00000000	DCI pixel region
CLUSTER0_DCI_LUMA_SAT_ADJ_0	0x0110	W	0x00000000	LUMA_SAT_ADJ_0
CLUSTER0_DCI_LUMA_SAT_ADJ_1	0x0114	W	0x00000000	DCI_LUMA_SAT_ADJ_1
CLUSTER0_DCI_CTRL	0x0118	W	0x00000030	DCI ctrl.
CLUSTER0_DCI_LUT_MST	0x011C	W	0x00000000	DCI LUT memory start address.
CLUSTER0_DCI_DBG_PIX	0x0130	W	0x00000000	DCI debug pixel value.
CLUSTER0_CLUSTER_PORT_SEL_IMD	0x01F4	W	0x00000000	Cluster layer ouput post sel.
CLUSTER0_CLUSTER_DLY_NUM	0x01F8	W	0x00001717	Cluster win0,win1 layer delay aclk cycle.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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11.5.2.10 CLUSTER1

Name	Offset	Size	Reset Value	Description
CLUSTER1_WIN0_CTRL0	0x0000	W	0x00000000	WIN0 control register0.
CLUSTER1_WIN0_CTRL1	0x0004	W	0x00000000	WIN0 control register1.
CLUSTER1_WIN0_CTRL2	0x0008	W	0x000000E6	WIN0 control register2.
CLUSTER1_WIN0_YRGB_MST	0x0010	W	0x00000000	WIN0 YRGB memory starting.
CLUSTER1_WIN0_CBCR_MST	0x0014	W	0x00000000	WIN0 CBCR memory starting.
CLUSTER1_WIN0_VIR	0x0018	W	0x00000000	WIN0 virtual width.
CLUSTER1_WIN0_KEY_COLOR	0x001C	W	0x00000000	Config key_color of WIN0.
CLUSTER1_WIN0_ACT_INFO	0x0020	W	0x00000000	WIN0 actual information.
CLUSTER1_WIN0_DSP_INFO	0x0024	W	0x00000000	WIN0 display information.
CLUSTER1_WIN0_DSP_ST	0x0028	W	0x00000000	WIN0 display start.
CLUSTER1_WIN0_DSP_BG	0x002C	W	0x00000000	WIN0 display background.
CLUSTER1_WIN0_SCL_FACTOR_YRGB	0x0030	W	0x00000000	WIN0 yrgb scale factor.
CLUSTER1_WIN0_SCL_OFFSET	0x0038	W	0x00000000	WIN0 scale offset.
CLUSTER1_WIN0_TRANSFORMED_OFFSET	0x003C	W	0x00000000	WIN0 transform offset
CLUSTER1_WIN0_ZME_CTRL	0x0040	W	0x00000000	WIN0 zme ctrl.
CLUSTER1_WIN0_ZME_DERING_PARA	0x0044	W	0x04100C10	WIN0 zme dering parameter config.
CLUSTER1_WIN0_FBCD_OUTPUT_CTRL	0x0050	W	0x00000010	WIN0 fbcd control register.
CLUSTER1_WIN0_FBCD_MODE	0x0054	W	0x00000000	WIN0 fbcd mode
CLUSTER1_WIN0_FBCD_HDR_PTR	0x0058	W	0x00000000	WIN0 fbcd hdr pointer.
CLUSTER1_WIN0_FBCD_VIR_WIDTH	0x005C	W	0x00000000	WIN0 fbcd virtual width.
CLUSTER1_WIN0_FBCD_SIZE	0x0060	W	0x00000000	WIN0 fbcd size.
CLUSTER1_WIN0_FBCD_PIC_OFFSET	0x0064	W	0x00000000	WIN0 fbcd picture offset.
CLUSTER1_WIN0_FBCD_DIS_OFFSET	0x0068	W	0x00000000	WIN0 fbcd display offset.
CLUSTER1_WIN0_FBCD_CTRL	0x006C	W	0x00000000	WIN0 fbcd control.
CLUSTER1_WIN0_PLD_PTR_OFFSET	0x0078	W	0x00000000	WIN0 pld and head offset in ddr.
CLUSTER1_WIN0_PLD_PTR_RANGE	0x007C	W	0x00000000	WIN0 pld range mst.
CLUSTER1_WIN1_CTRL0	0x0080	W	0x00000000	WIN1 control register0.
CLUSTER1_WIN1_CTRL1	0x0084	W	0x00000000	WIN1 control register1.
CLUSTER1_WIN1_CTRL2	0x0088	W	0x00000128	WIN1 control register2.
CLUSTER1_WIN1_YRGB_MST	0x0090	W	0x00000000	WIN1 YRGB memory starting.

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Name	Offset	Size	Reset Value	Description
CLUSTER1_WIN1_CBCR_MST	0x0094	W	0x00000000	WIN1 CBCR memory starting.
CLUSTER1_WIN1_VIR	0x0098	W	0x00000000	WIN1 virtual width.
CLUSTER1_WIN1_KEY_COLOR	0x009C	W	0x00000000	Config key_color of WIN1.
CLUSTER1_WIN1_ACT_INFO	0x00A0	W	0x00000000	WIN1 actual information.
CLUSTER1_WIN1_DSP_INFO	0x00A4	W	0x00000000	WIN1 display information.
CLUSTER1_WIN1_DSP_ST	0x00A8	W	0x00000000	WIN1 display start.
CLUSTER1_WIN1_DSP_BG	0x00AC	W	0x00000000	WIN1 display background.
CLUSTER1_WIN1_SCL_FACTOR_YRGB	0x00B0	W	0x00000000	WIN1 yrgb scale factor.
CLUSTER1_WIN1_SCL_OFFSET	0x00B8	W	0x00000000	WIN1 scale offset.
CLUSTER1_WIN1_TRANSFORMED_OFFSET	0x00BC	W	0x00000000	WIN1 transform offset
CLUSTER1_WIN1_ZME_CTRL	0x00C0	W	0x00000000	WIN1 zme ctrl.
CLUSTER1_WIN1_ZME_DERING_PARA	0x00C4	W	0x00000000	WIN1 zme dering parameter config.
CLUSTER1_WIN1_FBCD_MASK_EN	0x00D0	W	0x00000010	WIN1 fbcd control register.
CLUSTER1_WIN1_FBCD_MODE	0x00D4	W	0x00000000	WIN1 fbcd mode
CLUSTER1_WIN1_FBCD_HDR_PTR	0x00D8	W	0x00000000	WIN1 fbcd hdr pointer.
CLUSTER1_WIN1_FBCD_VIR_WIDTH	0x00DC	W	0x00000000	WIN1 fbcd virtual width.
CLUSTER1_WIN1_FBCD_SIZE	0x00E0	W	0x00000000	WIN1 fbcd size.
CLUSTER1_WIN1_FBCD_PIC_OFFSET	0x00E4	W	0x00000000	WIN1 fbcd picture offset.
CLUSTER1_WIN1_FBCD_DIS_OFFSET	0x00E8	W	0x00000000	WIN1 fbcd display offset.
CLUSTER1_WIN1_FBCD_CTRL	0x00EC	W	0x00000000	WIN1 fbcd control.
CLUSTER1_WIN1_PLD_PTR_OFFSET	0x00F8	W	0x00000000	WIN1 pld and head offset in ddr.
CLUSTER1_WIN1_PLD_PTR_RANGE	0x00FC	W	0x00000000	WIN1 pld range mst.
CLUSTER1_CLUSTER_CTRL	0x0100	W	0x80000000	CLUSTER control register.
CLUSTER1_CLUSTER_PORT_SEL_IMD	0x01F4	W	0x00000000	CLUSTER layer ouput post sel.
CLUSTER1_CLUSTER_DLY_NUM	0x01F8	W	0x00001717	CLUSTER win0,win1 layer delay aclk cycle.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.5.2.11 ESMART0

Name	Offset	Size	Reset Value	Description
ESMART0_ESMART_CTRL0	0x0000	W	0x00000000	To enable the color space convertion of esmart.

Name	Offset	Size	Reset Value	Description
ESMART0_ESMART_CTRL1	0x0004	W	0x0000B0A0	To control the dma of esmart.
ESMART0_ESMART_AXI_CTRL_IMD	0x0008	W	0x00010000	To contral esmart axi bus.
ESMART0_REGION0_MST_CTL	0x0010	W	0x00000000	To enable the region0 of esmart.
ESMART0_REGION0_MST_YRGB	0x0014	W	0x00000000	To configure the starting address of YRGB in memory.
ESMART0_REGION0_MST_CBCR	0x0018	W	0x00000000	To configure the starting address of CBCR in memory.
ESMART0_REGION0_VIR	0x001C	W	0x00000000	To configure the virtual width of data in memory.
ESMART0_REGION0_ACT_INFO	0x0020	W	0x00000000	To configure the active size of data.
ESMART0_REGION0_DSP_INFO	0x0024	W	0x00000000	To configure the dsiplay size of data.
ESMART0_REGION0_DSP_OFFSET	0x0028	W	0x00000000	To configure the dsiplay offset of data.
ESMART0_REGION0_SCL_CTRL	0x0030	W	0x00000000	To enable the scaling of esmart.
ESMART0_REGION0_SCL_FACTOR_YRGB	0x0034	W	0x10001000	To configure the scaling factor of YRGB.
ESMART0_REGION0_SCL_OFFSET	0x003C	W	0x00000000	To configure the scaling offset of esmart.
ESMART0_REGION1_MST_CTL	0x0040	W	0x00000000	To enable the region1 of esmart.
ESMART0_REGION1_MST_YRGB	0x0044	W	0x00000000	To configure the starting address of YRGB in memory.
ESMART0_REGION1_MST_CBCR	0x0048	W	0x00000000	To configure the starting address of CBCR in memory.
ESMART0_REGION1_VIR	0x004C	W	0x00000000	To configure the virtual width of data in memory.
ESMART0_REGION1_ACT_INFO	0x0050	W	0x00000000	To configure the active size of data.
ESMART0_REGION1_DSP_INFO	0x0054	W	0x00000000	To configure the dsiplay size of data.
ESMART0_REGION1_DSP_OFFSET	0x0058	W	0x00000000	To configure the dsiplay offset of data.
ESMART0_REGION1_SCL_CTRL	0x0060	W	0x00000000	To enable the scaling of esmart.
ESMART0_REGION1_SCL_FACTOR_YRGB	0x0064	W	0x10001000	To configure the scaling factor of YRGB.
ESMART0_REGION1_SCL_OFFSET	0x006C	W	0x00000000	To configure the scaling offset of esmart.
ESMART0_REGION2_MST_CTL	0x0070	W	0x00000000	To enable the region2 of esmart.
ESMART0_REGION2_MST_YRGB	0x0074	W	0x00000000	To configure the starting address of YRGB in memory.
ESMART0_REGION2_MST_CBCR	0x0078	W	0x00000000	To configure the starting address of CBCR in memory.
ESMART0_REGION2_VIR	0x007C	W	0x00000000	To configure the virtual width of data in memory.
ESMART0_REGION2_ACT_INFO	0x0080	W	0x00000000	To configure the active size of data.

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Name	Offset	Size	Reset Value	Description
ESMART0_REGION2_DSP_INFO	0x0084	W	0x00000000	To configure the dsiplay size of data.
ESMART0_REGION2_DSP_OFFSET	0x0088	W	0x00000000	To configure the dsiplay offset of data.
ESMART0_REGION2_SCL_CTRL	0x0090	W	0x00000000	To enable the scaling of esmart.
ESMART0_REGION2_SCL_FACTOR_YRGB	0x0094	W	0x10001000	To configure the scaling factor of YRGB.
ESMART0_REGION2_SCL_OFFSET	0x009C	W	0x00000000	To configure the scaling offset of esmart.
ESMART0_REGION3_MST_CTL	0x00A0	W	0x00000000	To enable the region3 of esmart.
ESMART0_REGION3_MST_YRGB	0x00A4	W	0x00000000	To configure the starting address of YRGB in memory.
ESMART0_REGION3_MST_CBCR	0x00A8	W	0x00000000	To configure the starting address of CBCR in memory.
ESMART0_REGION3_VIR	0x00AC	W	0x00000000	To configure the virtual width of data in memory.
ESMART0_REGION3_ACT_INFO	0x00B0	W	0x00000000	To configure the active size of data.
ESMART0_REGION3_DSP_INFO	0x00B4	W	0x00000000	To configure the dsiplay size of data.
ESMART0_REGION3_DSP_OFFSET	0x00B8	W	0x00000000	To configure the dsiplay offset of data.
ESMART0_REGION3_SCL_CTRL	0x00C0	W	0x00000000	To enable the scaling of esmart.
ESMART0_REGION3_SCL_FACTOR_YRGB	0x00C4	W	0x10001000	To configure the scaling factor of YRGB.
ESMART0_REGION3_SCL_OFFSET	0x00CC	W	0x00000000	To configure the scaling offset of esmart.
ESMART0_ESMART_KEY_CTRL	0x00D0	W	0x00000000	To configure the color key of esmart.
ESMART0_ESMART_BG_EN	0x00D4	W	0x00000000	To enable the background of esmart.
ESMART0_ESMART_ALPHA_MAP	0x00D8	W	0x00000000	RGBA5551 alpha channel map ctrl.
ESMART0_ESMART_PORT_SEL_IMD	0x00F4	W	0x00000000	ESMART layer ouput post sel.
ESMART0_ESMART_DLY_NUM	0x00F8	W	0x00000017	ESMART layer delay aclk cycle.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.5.2.12 ESMART1

Name	Offset	Size	Reset Value	Description
ESMART1_ESMART_CTRL0	0x0000	W	0x00001000	To enable the color space convertion of esmart.
ESMART1_ESMART_CTRL1	0x0004	W	0x0000D0C0	To control the dma of esmart.
ESMART1_ESMART_AXI_CTRL_IMD	0x0008	W	0x00010000	To contral esmart axi bus.
ESMART1_REGION0_MST_CTL	0x0010	W	0x00000000	To enable the region0 of esmart.
ESMART1_REGION0_MST_YRGB	0x0014	W	0x00000000	To configure the starting address of YRGB in memory.

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Name	Offset	Size	Reset Value	Description
ESMART1_REGION0_MST_CBCR	0x0018	W	0x00000000	To configure the starting address of CBCR in memory.
ESMART1_REGION0_VIR	0x001C	W	0x00000000	To configure the virtual width of data in memory.
ESMART1_REGION0_ACT_INFO	0x0020	W	0x00000000	To configure the active size of data.
ESMART1_REGION0_DSP_INFO	0x0024	W	0x00000000	To configure the dsiplay size of data.
ESMART1_REGION0_DSP_OFFSET	0x0028	W	0x00000000	To configure the dsiplay offset of data.
ESMART1_REGION0_SCL_CTRL	0x0030	W	0x00000000	To enable the scaling of esmart.
ESMART1_REGION0_SCL_FACTOR_YRGB	0x0034	W	0x10001000	To configure the scaling factor of YRGB.
ESMART1_REGION0_SCL_OFFSET	0x003C	W	0x00000000	To configure the scaling offset of esmart.
ESMART1_REGION1_MST_CTL	0x0040	W	0x00000000	To enable the region1 of esmart.
ESMART1_REGION1_MST_YRGB	0x0044	W	0x00000000	To configure the starting address of YRGB in memory.
ESMART1_REGION1_MST_CBCR	0x0048	W	0x00000000	To configure the starting address of CBCR in memory.
ESMART1_REGION1_VIR	0x004C	W	0x00000000	To configure the virtual width of data in memory.
ESMART1_REGION1_ACT_INFO	0x0050	W	0x00000000	To configure the active size of data.
ESMART1_REGION1_DSP_INFO	0x0054	W	0x00000000	To configure the dsiplay size of data .
ESMART1_REGION1_DSP_OFFSET	0x0058	W	0x00000000	To configure the dsiplay offset of data.
ESMART1_REGION1_SCL_CTRL	0x0060	W	0x00000000	To enable the scaling of esmart.
ESMART1_REGION1_SCL_FACTOR_YRGB	0x0064	W	0x10001000	To configure the scaling factor of YRGB.
ESMART1_REGION1_SCL_OFFSET	0x006C	W	0x00000000	To configure the scaling offset of esmart.
ESMART1_REGION2_MST_CTL	0x0070	W	0x00000000	To enable the region2 of esmart.
ESMART1_REGION2_MST_YRGB	0x0074	W	0x00000000	To configure the starting address of YRGB in memory.
ESMART1_REGION2_MST_CBCR	0x0078	W	0x00000000	To configure the starting address of CBCR in memory.
ESMART1_REGION2_VIR	0x007C	W	0x00000000	To configure the virtual width of data in memory.
ESMART1_REGION2_ACT_INFO	0x0080	W	0x00000000	To configure the active size of data.
ESMART1_REGION2_DSP_INFO	0x0084	W	0x00000000	To configure the dsiplay size of data.
ESMART1_REGION2_DSP_OFFSET	0x0088	W	0x00000000	To configure the dsiplay offset of data.
ESMART1_REGION2_SCL_CTRL	0x0090	W	0x00000000	To enable the scaling of esmart.
ESMART1_REGION2_SCL_FACTOR_YRGB	0x0094	W	0x10001000	To configure the scaling factor of YRGB.

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Name	Offset	Size	Reset Value	Description
ESMART1_REGION2_SCL_OFFSET	0x009C	W	0x00000000	To configure the scaling offset of esmart.
ESMART1_REGION3_MST_CTL	0x00A0	W	0x00000000	To enable the region3 of esmart.
ESMART1_REGION3_MST_YRGB	0x00A4	W	0x00000000	To configure the starting address of YRGB in memory.
ESMART1_REGION3_MST_CBCR	0x00A8	W	0x00000000	To configure the starting address of CBCR in memory.
ESMART1_REGION3_VIR	0x00AC	W	0x00000000	To configure the virtual width of data in memory.
ESMART1_REGION3_ACT_INFO	0x00B0	W	0x00000000	To configure the active size of data.
ESMART1_REGION3_DSP_INFO	0x00B4	W	0x00000000	To configure the dsiplay size of data.
ESMART1_REGION3_DSP_OFFSET	0x00B8	W	0x00000000	To configure the dsiplay offset of data.
ESMART1_REGION3_SCL_CTRL	0x00C0	W	0x00000000	To enable the scaling of esmart.
ESMART1_REGION3_SCL_FACTOR_YRGB	0x00C4	W	0x10001000	To configure the scaling factor of YRGB.
ESMART1_REGION3_SCL_OFFSET	0x00CC	W	0x00000000	To configure the scaling offset of esmart.
ESMART1_ESMART_KEY_CTRL	0x00D0	W	0x00000000	To configure the color key of esmart.
ESMART1_ESMART_BG_EN	0x00D4	W	0x00000000	To enable the background of esmart.
ESMART1_ESMART_ALPHA_MAP	0x00D8	W	0x80000000	RGBA5551 alpha channel map ctrl.
ESMART1_ESMART_PORT_SEL_IMD	0x00F4	W	0x00000000	ESMART layer ouput post sel.
ESMART1_ESMART_DLY_NUM	0x00F8	W	0x00000017	ESMART layer delay aclk cycle.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.5.2.13 ESMART2

Name	Offset	Size	Reset Value	Description
ESMART2_ESMART_CTRL0	0x0000	W	0x00002000	To enable the color space convertion of esmart.
ESMART2_ESMART_CTRL1	0x0004	W	0x0000B0A0	To control the dma of esmart.
ESMART2_ESMART_AXI_CTRL_IMD	0x0008	W	0x00000002	To contral esmart axi bus.
ESMART2_REGION0_MST_CTL	0x0010	W	0x00000000	To enable the region0 of esmart.
ESMART2_REGION0_MST_YRGB	0x0014	W	0x00000000	To configure the starting address of YRGB in memory.
ESMART2_REGION0_MST_CBCR	0x0018	W	0x00000000	To configure the starting address of CBCR in memory.
ESMART2_REGION0_VIR	0x001C	W	0x00000000	To configure the virtual width of data in memory.
ESMART2_REGION0_ACT_INFO	0x0020	W	0x00000000	To configure the active size of data.
ESMART2_REGION0_DSP_INFO	0x0024	W	0x00000000	To configure the dsiplay size of data.

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Name	Offset	Size	Reset Value	Description
ESMART2_REGION0_DSP_OFFSET	0x0028	W	0x00000000	To configure the dsiplay offset of data.
ESMART2_REGION0_SCL_CTRL	0x0030	W	0x00000000	To enable the scaling of esmart.
ESMART2_REGION0_SCL_FACTOR_YRGB	0x0034	W	0x10001000	To configure the scaling factor of YRGB.
ESMART2_REGION0_SCL_OFFSET	0x003C	W	0x00000000	To configure the scaling offset of esmart.
ESMART2_REGION1_MST_CTL	0x0040	W	0x00000000	To enable the region1 of esmart.
ESMART2_REGION1_MST_YRGB	0x0044	W	0x00000000	To configure the starting address of YRGB in memory.
ESMART2_REGION1_MST_CBCR	0x0048	W	0x00000000	To configure the starting address of CBCR in memory.
ESMART2_REGION1_VIR	0x004C	W	0x00000000	To configure the virtual width of data in memory.
ESMART2_REGION1_ACT_INFO	0x0050	W	0x00000000	To configure the active size of data.
ESMART2_REGION1_DSP_INFO	0x0054	W	0x00000000	To configure the dsiplay size of data.
ESMART2_REGION1_DSP_OFFSET	0x0058	W	0x00000000	To configure the dsiplay offset of data.
ESMART2_REGION1_SCL_CTRL	0x0060	W	0x00000000	To enable the scaling of esmart.
ESMART2_REGION1_SCL_FACTOR_YRGB	0x0064	W	0x10001000	To configure the scaling factor of YRGB.
ESMART2_REGION1_SCL_OFFSET	0x006C	W	0x00000000	To configure the scaling offset of esmart.
ESMART2_REGION2_MST_CTL	0x0070	W	0x00000000	To enable the region2 of esmart.
ESMART2_REGION2_MST_YRGB	0x0074	W	0x00000000	To configure the starting address of YRGB in memory.
ESMART2_REGION2_MST_CBCR	0x0078	W	0x00000000	To configure the starting address of CBCR in memory.
ESMART2_REGION2_VIR	0x007C	W	0x00000000	To configure the virtual width of data in memory.
ESMART2_REGION2_ACT_INFO	0x0080	W	0x00000000	To configure the active size of data .
ESMART2_REGION2_DSP_INFO	0x0084	W	0x00000000	To configure the dsiplay size of data.
ESMART2_REGION2_DSP_OFFSET	0x0088	W	0x00000000	To configure the dsiplay offset of data.
ESMART2_REGION2_SCL_CTRL	0x0090	W	0x00000000	To enable the scaling of esmart.
ESMART2_REGION2_SCL_FACTOR_YRGB	0x0094	W	0x10001000	To configure the scaling factor of YRGB.
ESMART2_REGION2_SCL_OFFSET	0x009C	W	0x00000000	To configure the scaling offset of esmart.
ESMART2_REGION3_MST_CTL	0x00A0	W	0x00000000	To enable the region3 of esmart.
ESMART2_REGION3_MST_YRGB	0x00A4	W	0x00000000	To configure the starting address of YRGB in memory.
ESMART2_REGION3_MST_CBCR	0x00A8	W	0x00000000	To configure the starting address of CBCR in memory.

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Name	Offset	Size	Reset Value	Description
ESMART2_REGION3_VIR	0x00AC	W	0x00000000	To configure the virtual width of data in memory.
ESMART2_REGION3_ACT_INFO	0x00B0	W	0x00000000	To configure the active size of data.
ESMART2_REGION3_DSP_INFO	0x00B4	W	0x00000000	To configure the dsiplay size of data.
ESMART2_REGION3_DSP_OFFSET	0x00B8	W	0x00000000	To configure the dsiplay offset of data.
ESMART2_REGION3_SCL_CTRL	0x00C0	W	0x00000000	To enable the scaling of esmart.
ESMART2_REGION3_SCL_FACTOR_YRGB	0x00C4	W	0x10001000	To configure the scaling factor of YRGB.
ESMART2_REGION3_SCL_OFFSET	0x00CC	W	0x00000000	To configure the scaling offset of esmart.
ESMART2_ESMART_KEY_CTRL	0x00D0	W	0x00000000	To configure the color key of esmart.
ESMART2_ESMART_BG_EN	0x00D4	W	0x00000000	To enable the background of esmart.
ESMART2_ESMART_ALPHA_MAP	0x00D8	W	0x00000000	RGBA5551 alpha channel map ctrl.
ESMART2_ESMART_PORT_SEL_IMD	0x00F4	W	0x00000000	ESMART layer ouput post sel.
ESMART2_ESMART_DLY_NUM	0x00F8	W	0x00000017	ESMART layer delay aclk cycle.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.5.2.14 ESMART3

Name	Offset	Size	Reset Value	Description
ESMART3_ESMART_CTRL0	0x0000	W	0x00003000	To enable the color space convertion of esmart.
ESMART3_ESMART_CTRL1	0x0004	W	0x0000D0C0	To control the dma of esmart.
ESMART3_ESMART_AXI_CTRL_IMD	0x0008	W	0x00010002	To contral esmart axi bus.
ESMART3_REGION0_MST_CTL	0x0010	W	0x00000000	To enable the region0 of esmart.
ESMART3_REGION0_MST_YRGB	0x0014	W	0x00000000	To configure the starting address of YRGB in memory.
ESMART3_REGION0_MST_CBCR	0x0018	W	0x00000000	To configure the starting address of CBCR in memory.
ESMART3_REGION0_VIR	0x001C	W	0x00000000	To configure the virtual width of data in memory.
ESMART3_REGION0_ACT_INFO	0x0020	W	0x00000000	To configure the active size of data.
ESMART3_REGION0_DSP_INFO	0x0024	W	0x00000000	To configure the dsiplay size of data.
ESMART3_REGION0_DSP_OFFSET	0x0028	W	0x00000000	To configure the dsiplay offset of data.
ESMART3_REGION0_SCL_CTRL	0x0030	W	0x00000000	To enable the scaling of esmart.
ESMART3_REGION0_SCL_FACTOR_YRGB	0x0034	W	0x10001000	To configure the scaling factor of YRGB.
ESMART3_REGION0_SCL_OFFSET	0x003C	W	0x00000000	To configure the scaling offset of esmart.

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Name	Offset	Size	Reset Value	Description
ESMART3_REGION1_MST_CTL	0x0040	W	0x00000000	To enable the region1 of esmart.
ESMART3_REGION1_MST_YRGB	0x0044	W	0x00000000	To configure the starting address of YRGB in memory.
ESMART3_REGION1_MST_CBCR	0x0048	W	0x00000000	To configure the starting address of CBCR in memory.
ESMART3_REGION1_VIR	0x004C	W	0x00000000	To configure the virtual width of data in memory.
ESMART3_REGION1_ACT_INFO	0x0050	W	0x00000000	To configure the active size of data.
ESMART3_REGION1_DSP_INFO	0x0054	W	0x00000000	To configure the dsiplay size of data.
ESMART3_REGION1_DSP_OFFSET	0x0058	W	0x00000000	To configure the dsiplay offset of data.
ESMART3_REGION1_SCL_CTRL	0x0060	W	0x00000000	To enable the scaling of esmart.
ESMART3_REGION1_SCL_FACTOR_YRGB	0x0064	W	0x10001000	To configure the scaling factor of YRGB.
ESMART3_REGION1_SCL_OFFSET	0x006C	W	0x00000000	To configure the scaling offset of esmart.
ESMART3_REGION2_MST_CTL	0x0070	W	0x00000000	To enable the region2 of esmart.
ESMART3_REGION2_MST_YRGB	0x0074	W	0x00000000	To configure the starting address of YRGB in memory.
ESMART3_REGION2_MST_CBCR	0x0078	W	0x00000000	To configure the starting address of CBCR in memory.
ESMART3_REGION2_VIR	0x007C	W	0x00000000	To configure the virtual width of data in memory.
ESMART3_REGION2_ACT_INFO	0x0080	W	0x00000000	To configure the active size of data.
ESMART3_REGION2_DSP_INFO	0x0084	W	0x00000000	To configure the dsiplay size of data.
ESMART3_REGION2_DSP_OFFSET	0x0088	W	0x00000000	To configure the dsiplay offset of data.
ESMART3_REGION2_SCL_CTRL	0x0090	W	0x00000000	To enable the scaling of esmart.
ESMART3_REGION2_SCL_FACTOR_YRGB	0x0094	W	0x10001000	To configure the scaling factor of YRGB.
ESMART3_REGION2_SCL_OFFSET	0x009C	W	0x00000000	To configure the scaling offset of esmart.
ESMART3_REGION3_MST_CTL	0x00A0	W	0x00000000	To enable the region3 of esmart.
ESMART3_REGION3_MST_YRGB	0x00A4	W	0x00000000	To configure the starting address of YRGB in memory.
ESMART3_REGION3_MST_CBCR	0x00A8	W	0x00000000	To configure the starting address of CBCR in memory.
ESMART3_REGION3_VIR	0x00AC	W	0x00000000	To configure the virtual width of data in memory.
ESMART3_REGION3_ACT_INFO	0x00B0	W	0x00000000	To configure the active size of data.
ESMART3_REGION3_DSP_INFO	0x00B4	W	0x00000000	To configure the dsiplay size of data.
ESMART3_REGION3_DSP_OFFSET	0x00B8	W	0x00000000	To configure the dsiplay offset of data.

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Name	Offset	Size	Reset Value	Description
ESMART3_REGION3_SCL_CTRL	0x00C0	W	0x00000000	To enable the scaling of esmart.
ESMART3_REGION3_SCL_FACTOR_YRGB	0x00C4	W	0x10001000	To configure the scaling factor of YRGB.
ESMART3_REGION3_SCL_OFFSET	0x00CC	W	0x00000000	To configure the scaling offset of esmart.
ESMART3_ESMART_KEY_CTRL	0x00D0	W	0x00000000	To configure the color key of esmart.
ESMART3_ESMART_BG_EN	0x00D4	W	0x00000000	To enable the background of esmart.
ESMART3_ESMART_ALPHA_MAP	0x00D8	W	0x00000000	RGBA5551 alpha channel map ctrl.
ESMART3_ESMART_PORT_SEL_IMD	0x00F4	W	0x00000000	ESMART layer ouput post sel.
ESMART3_ESMART_DLY_NUM	0x00F8	W	0x00000017	ESMART layer delay aclk cycle.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.5.2.15 HDR_VIVID

Name	Offset	Size	Reset Value	Description
HDR_VIVID_HDR_LUT_CTRL	0x0000	W	0x00000000	To configure HDR dynamic LUT update mode and enable.
HDR_VIVID_HDR_LUT_MST	0x0004	W	0x00000000	It's HDR dynamic LUT address.
HDR_VIVID_HDR_LUT_STATUS	0x0008	W	0x00000000	HDR LUT fetch status.
HDR_VIVID_SDR2HDR_CTRL	0x0010	W	0x00000002	To configure SDR2HDR common setting.
HDR_VIVID_SDR_CFG_COE0	0x0014	W	0x00000000	To configure SDR2HDR parameters.
HDR_VIVID_SDR_CFG_COE1	0x0018	W	0x00000000	To configure SDR2HDR parameters.
HDR_VIVID_SDR_CSC_COE00_01	0x001C	W	0x00000000	To configure SDR2HDR CSC.
HDR_VIVID_SDR_CSC_COE02_10	0x0020	W	0x00000300	To configure SDR2HDR CSC.
HDR_VIVID_SDR_CSC_COE11_12	0x0024	W	0x316201EE	To configure SDR2HDR CSC.
HDR_VIVID_SDR_CSC_COE20_21	0x0028	W	0x00002800	To configure SDR2HDR CSC.
HDR_VIVID_SDR_CSC_COE22	0x002C	W	0x00000000	To configure SDR2HDR CSC.
HDR_VIVID_HDRVIVID_CTRL	0x0040	W	0x00000002	To configure HDR vivid common setting.
HDR_VIVID_HDR_PQ_GAMMA	0x0044	W	0x00000000	To configure HDR vivid parameters.
HDR_VIVID_HLG_RFIX_SCALEFAC	0x0048	W	0x00000000	To configure HDR vivid parameters.
HDR_VIVID_HLG_MAXLUMA	0x004C	W	0x00000000	To configure HDR vivid parameters.
HDR_VIVID_HLG_R_TM_LIN2NON	0x0050	W	0x00000000	To configure HDR vivid parameters.

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Name	Offset	Size	Reset Value	Description
HDR_VIVID_HDR_CSC_COE00_01	0x0054	W	0x00000000	To configure HDR vivid CSC.
HDR_VIVID_HDR_CSC_COE02_10	0x0058	W	0x00000000	To configure HDR vivid CSC.
HDR_VIVID_HDR_CSC_COE11_12	0x005C	W	0x00000000	To configure HDR vivid CSC.
HDR_VIVID_HDR_CSC_COE20_21	0x0060	W	0x00000000	To configure HDR vivid CSC.
HDR_VIVID_HDR_CSC_COE22	0x0064	W	0x00000000	To configure HDR vivid CSC.
HDR_VIVID_HDR_TONE_SCA	0x013C	W	0x00000000	It's HDR LUT address.
HDR_VIVID_HDRGAMMA_CURVE	0x0540	W	0x00000000	It's HDR LUT address.
HDR_VIVID_HDRGAMMA_MDFVALUE	0x0690	W	0x00000000	It's HDR LUT address.
HDR_VIVID_SDRINVGAMMA_CURVE	0x0700	W	0x00000000	It's SDR LUT address.
HDR_VIVID_SDRINVGAMMA_STARTIDX	0x0820	W	0x00000000	It's SDR LUT address.
HDR_VIVID_SDRINVGAMMA_CHANGEIDX	0x0840	W	0x00000000	It's SDR LUT address.
HDR_VIVID_SDR_SMGAIN	0x0900	W	0x00000000	It's SDR LUT address.

Notes:Size:B- Byte (8 bits) access, HW- Half WORD (16 bits) access, W-WORD (32 bits) access, DW-Double WORD (64 bits) access

11.5.2.16 ACM

Name	Offset	Size	Reset Value	Description
ACM_ACM_CTRL	0x0000	W	0x00000002	ACM enable control.
ACM_DELTA_RANGE	0x0004	W	0x00000000	Delta Y/H/S value.
ACM_FETCH_START	0x0008	W	0x00000000	ACM lut configure start enable.
ACM_FETCH_DONE	0x0020	W	0x00000000	ACM lut configure done configure.
ACM_YHS_GAIN_BY_Y_SEG0	0x0100	W	0x00000000	YHS_DEL Y parameter0 start.
ACM_YHS_GAIN_BY_Y_SEG152	0x0360	W	0x00000000	YHS_DEL Y parameter152 end.
ACM_YHS_GAIN_BY_S_SEG0	0x0364	W	0x00000000	YHS_DEL S parameter0 start.
ACM_YHS_GAIN_BY_S_SEG220	0x06D4	W	0x00000000	YHS_DEL S parameter220 end.
ACM_YHS_DEL_BY_H_SEG0	0x06D8	W	0x00000000	YHS_DEL H parameter0 start.
ACM_YHS_DEL_BY_H_SEG64	0x07D8	W	0x00000000	YHS_DEL H parameter64 end.

Notes:Size:B- Byte (8 bits) access, HW- Half WORD (16 bits) access, W-WORD (32 bits) access, DW-Double WORD (64 bits) access

11.5.2.17 SHARP

Name	Offset	Size	Reset Value	Description
SHARP_CTRL	0x0000	W	0x00000000	Sharp function enable control.
SHARP_AUTO_GATING_IMD	0x0004	W	0x000007FE	To control auto-gating.
SHARP_PEAKING_FILTER_COE0	0x0008	W	0x00000000	Sharp peaking filter coe0.

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Name	Offset	Size	Reset Value	Description
SHARP_PEAKING_FILTER_COE1	0x000C	W	0x00000000	Sharp peaking filter coe1.
SHARP_PEAKING_FILTER_COE2	0x0010	W	0x00000000	Sharp peaking filter coe2.
SHARP_PEAKING_FILTER_COE3	0x0014	W	0x00000000	Sharp peaking filter coe3.
SHARP_PEAKING_FILTER_COE4	0x0018	W	0x00000000	Sharp peaking filter coe4.
SHARP_PEAKING_FILTER_COE5	0x001C	W	0x00000000	Sharp peaking filter coe5.
SHARP_PEAKING_FILTER_COE6	0x0020	W	0x00000000	Sharp peaking filter coe6.
SHARP_PEAKING_FILTER_COE7	0x0024	W	0x00000000	Sharp peaking filter coe7.
SHARP_PEAKING_FILTER_COE8	0x0028	W	0x00000000	Sharp peaking filter coe8.
SHARP_PEAKING_FILTER_COE9	0x002C	W	0x00000000	Sharp peaking filter coe9.
SHARP_PEAKING0_CTRL_COE0	0x0030	W	0x00000000	Sharp peaking0 control coe0.
SHARP_PEAKING0_CTRL_COE1	0x0034	W	0x00000000	Sharp peaking control coe1.
SHARP_PEAKING0_CTRL_COE2	0x0038	W	0x00000000	Sharp peaking0 control coe2.
SHARP_PEAKING0_CTRL_COE3	0x003C	W	0x00000000	Sharp peaking0 control coe3.
SHARP_PEAKING0_CTRL_COE4	0x0040	W	0x00000000	Sharp peaking0 control coe4.
SHARP_PEAKING0_CTRL_COE5	0x0044	W	0x00000000	Sharp peaking0 control coe5.
SHARP_PEAKING0_CTRL_COE6	0x0048	W	0x00000000	Sharp peaking0 control coe6.
SHARP_PEAKING0_CTRL_COE7	0x004C	W	0x00000000	Sharp peaking0 control coe7.
SHARP_PEAKING0_CTRL_COE8	0x0050	W	0x00000000	Sharp peaking0 control coe8.
SHARP_PEAKING0_CTRL_COE9	0x0054	W	0x00000000	Sharp peaking0 control coe9.
SHARP_PEAKING0_CTRL_COE10	0x0058	W	0x00000000	Sharp peaking0 control coe10.
SHARP_PEAKING1_CTRL_COE0	0x005C	W	0x00000000	Sharp peaking1 control coe0.
SHARP_PEAKING1_CTRL_COE1	0x0060	W	0x00000000	Sharp peaking1 control coe1.
SHARP_PEAKING1_CTRL_COE2	0x0064	W	0x00000000	Sharp peaking1 control coe2.
SHARP_PEAKING1_CTRL_COE3	0x0068	W	0x00000000	Sharp peaking1 control coe3.
SHARP_PEAKING1_CTRL_COE4	0x006C	W	0x00000000	Sharp peaking1 control coe4.
SHARP_PEAKING1_CTRL_COE5	0x0070	W	0x00000000	Sharp peaking1 control coe5.
SHARP_PEAKING1_CTRL_COE6	0x0074	W	0x00000000	Sharp peaking1 control coe6.

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Name	Offset	Size	Reset Value	Description
SHARP_PEAKING1_CTRL_COE7	0x0078	W	0x00000000	Sharp peaking1 control coe7.
SHARP_PEAKING1_CTRL_COE8	0x007C	W	0x00000000	Sharp peaking1 control coe8.
SHARP_PEAKING1_CTRL_COE9	0x0080	W	0x00000000	Sharp peaking1 control coe9.
SHARP_PEAKING1_CTRL_COE10	0x0084	W	0x00000000	Sharp peaking1 control coe10.
SHARP_PEAKING2_CTRL_COE0	0x0088	W	0x00000000	Sharp peaking2 control coe0.
SHARP_PEAKING2_CTRL_COE1	0x008C	W	0x00000000	Sharp peaking2 control coe1.
SHARP_PEAKING2_CTRL_COE2	0x0090	W	0x00000000	Sharp peaking2 control coe2.
SHARP_PEAKING2_CTRL_COE3	0x0094	W	0x00000000	Sharp peaking2 control coe3.
SHARP_PEAKING2_CTRL_COE4	0x0098	W	0x00000000	Sharp peaking2 control coe4.
SHARP_PEAKING2_CTRL_COE5	0x009C	W	0x00000000	Sharp peaking2 control coe5.
SHARP_PEAKING2_CTRL_COE6	0x00A0	W	0x00000000	Sharp peaking2 control coe6.
SHARP_PEAKING2_CTRL_COE7	0x00A4	W	0x00000000	Sharp peaking2 control coe7.
SHARP_PEAKING2_CTRL_COE8	0x00A8	W	0x00000000	Sharp peaking2 control coe8.
SHARP_PEAKING2_CTRL_COE9	0x00AC	W	0x00000000	Sharp peaking2 control coe9.
SHARP_PEAKING2_CTRL_COE10	0x00B0	W	0x00000000	Sharp peaking2 control coe10.
SHARP_PEAKING3_CTRL_COE0	0x00B4	W	0x00000000	Sharp peaking3 control coe0.
SHARP_PEAKING3_CTRL_COE1	0x00B8	W	0x00000000	Sharp peaking3 control coe1.
SHARP_PEAKING3_CTRL_COE2	0x00BC	W	0x00000000	Sharp peaking3 control coe2.
SHARP_PEAKING3_CTRL_COE3	0x00C0	W	0x00000000	Sharp peaking3 control coe3.
SHARP_PEAKING3_CTRL_COE4	0x00C4	W	0x00000000	Sharp peaking3 control coe4.
SHARP_PEAKING3_CTRL_COE5	0x00C8	W	0x00000000	Sharp peaking3 control coe5.
SHARP_PEAKING3_CTRL_COE6	0x00CC	W	0x00000000	Sharp peaking3 control coe6.
SHARP_PEAKING3_CTRL_COE7	0x00D0	W	0x00000000	Sharp peaking3 control coe7.
SHARP_PEAKING3_CTRL_COE8	0x00D4	W	0x00000000	Sharp peaking3 control coe8.
SHARP_PEAKING3_CTRL_COE9	0x00D8	W	0x00000000	Sharp peaking3 control coe9.
SHARP_PEAKING3_CTRL_COE10	0x00DC	W	0x00000000	Sharp peaking3 control coe10.
SHARP_PEAKING4_CTRL_COE0	0x00E0	W	0x00000000	Sharp peaking4 control coe0.

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Name	Offset	Size	Reset Value	Description
SHARP_PEAKING4_CTRL_COE1	0x00E4	W	0x00000000	Sharp peaking4 control coe1.
SHARP_PEAKING4_CTRL_COE2	0x00E8	W	0x00000000	Sharp peaking4 control coe2.
SHARP_PEAKING4_CTRL_COE3	0x00EC	W	0x00000000	Sharp peaking4 control coe3.
SHARP_PEAKING4_CTRL_COE4	0x00F0	W	0x00000000	Sharp peaking4 control coe4.
SHARP_PEAKING4_CTRL_COE5	0x00F4	W	0x00000000	Sharp peaking4 control coe5.
SHARP_PEAKING4_CTRL_COE6	0x00F8	W	0x00000000	Sharp peaking4 control coe6.
SHARP_PEAKING4_CTRL_COE7	0x00FC	W	0x00000000	Sharp peaking4 control coe7.
SHARP_PEAKING4_CTRL_COE8	0x0100	W	0x00000000	Sharp peaking4 control coe8.
SHARP_PEAKING4_CTRL_COE9	0x0104	W	0x00000000	Sharp peaking4 control coe9.
SHARP_PEAKING4_CTRL_COE10	0x0108	W	0x00000000	Sharp peaking4 control coe10.
SHARP_PEAKING5_CTRL_COE0	0x010C	W	0x00000000	Sharp peaking5 control coe0.
SHARP_PEAKING5_CTRL_COE1	0x0110	W	0x00000000	Sharp peaking5 control coe1.
SHARP_PEAKING5_CTRL_COE2	0x0114	W	0x00000000	Sharp peaking5 control coe2.
SHARP_PEAKING5_CTRL_COE3	0x0118	W	0x00000000	Sharp peaking5 control coe3.
SHARP_PEAKING5_CTRL_COE4	0x011C	W	0x00000000	Sharp peaking5 control coe4.
SHARP_PEAKING5_CTRL_COE5	0x0120	W	0x00000000	Sharp peaking5 control coe5.
SHARP_PEAKING5_CTRL_COE6	0x0124	W	0x00000000	Sharp peaking5 control coe6.
SHARP_PEAKING5_CTRL_COE7	0x0128	W	0x00000000	Sharp peaking5 control coe7.
SHARP_PEAKING5_CTRL_COE8	0x012C	W	0x00000000	Sharp peaking5 control coe8.
SHARP_PEAKING5_CTRL_COE9	0x0130	W	0x00000000	Sharp peaking5 control coe9.
SHARP_PEAKING5_CTRL_COE10	0x0134	W	0x00000000	Sharp peaking5 control coe10.
SHARP_PEAKING6_CTRL_COE0	0x0138	W	0x00000000	Sharp peaking6 control coe0.
SHARP_PEAKING6_CTRL_COE1	0x013C	W	0x00000000	Sharp peaking6 control coe1.
SHARP_PEAKING6_CTRL_COE2	0x0140	W	0x00000000	Sharp peaking6 control coe2.
SHARP_PEAKING6_CTRL_COE3	0x0144	W	0x00000000	Sharp peaking6 control coe3.
SHARP_PEAKING6_CTRL_COE4	0x0148	W	0x00000000	Sharp peaking6 control coe4.
SHARP_PEAKING6_CTRL_COE5	0x014C	W	0x00000000	Sharp peaking6 control coe5.

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Name	Offset	Size	Reset Value	Description
SHARP_PEAKING6_CTRL_COE6	0x0150	W	0x00000000	Sharp peaking6 control coe6.
SHARP_PEAKING6_CTRL_COE7	0x0154	W	0x00000000	Sharp peaking6 control coe7.
SHARP_PEAKING6_CTRL_COE8	0x0158	W	0x00000000	Sharp peaking6 control coe8.
SHARP_PEAKING6_CTRL_COE9	0x015C	W	0x00000000	Sharp peaking6 control coe9.
SHARP_PEAKING6_CTRL_COE10	0x0160	W	0x00000000	Sharp peaking6 control coe10.
SHARP_PEAKING7_CTRL_COE0	0x0164	W	0x00000000	Sharp peaking7 control coe0.
SHARP_PEAKING7_CTRL_COE1	0x0168	W	0x00000000	Sharp peaking7 control coe1.
SHARP_PEAKING7_CTRL_COE2	0x016C	W	0x00000000	Sharp peaking7 control coe2.
SHARP_PEAKING7_CTRL_COE3	0x0170	W	0x00000000	Sharp peaking7 control coe3.
SHARP_PEAKING7_CTRL_COE4	0x0174	W	0x00000000	Sharp peaking7 control coe4.
SHARP_PEAKING7_CTRL_COE5	0x0178	W	0x00000000	Sharp peaking7 control coe5.
SHARP_PEAKING7_CTRL_COE6	0x017C	W	0x00000000	Sharp peaking7 control coe6.
SHARP_PEAKING7_CTRL_COE7	0x0180	W	0x00000000	Sharp peaking7 control coe7.
SHARP_PEAKING7_CTRL_COE8	0x0184	W	0x00000000	Sharp peaking7 control coe8.
SHARP_PEAKING7_CTRL_COE9	0x0188	W	0x00000000	Sharp peaking7 control coe9.
SHARP_PEAKING7_CTRL_COE10	0x018C	W	0x00000000	Sharp peaking7 control coe10.
SHARP_PEAKING_CTRL0	0x0190	W	0x00000000	Sharp peaking control cfg0.
SHARP_PEAKING_CTRL1	0x0194	W	0x00000000	Sharp peaking control cfg1.
SHARP_PEAKING_CTRL2	0x0198	W	0x00000000	Sharp peaking control cfg2.
SHARP_PEAKING_CTRL3	0x019C	W	0x00000000	Sharp peaking control cfg3.
SHARP_PEAKING_CTRL4	0x01A0	W	0x00000000	Sharp peaking control cfg4.
SHARP_PEAKING_CTRL5	0x01A4	W	0x00000000	Sharp peaking control cfg5.
SHARP_PEAKING_CTRL6	0x01A8	W	0x00000000	Sharp peaking control cfg6.
SHARP_PEAKING_CTRL7	0x01AC	W	0x00000000	Sharp peaking control cfg7.
SHARP_PEAKING_CTRL8	0x01B0	W	0x00000000	Sharp peaking control cfg8.
SHARP_PEAKING_CTRL9	0x01B4	W	0x00000000	Sharp peaking control cfg9.
SHARP_SHOOT_CTRL0	0x01B8	W	0x00000000	Sharp shoot control cfg0.
SHARP_SHOOT_CTRL1	0x01BC	W	0x00000000	Sharp shoot control cfg1.
SHARP_GAIN_CTRL0	0x01C0	W	0x00000000	Sharp gain control cfg0.
SHARP_GAIN_CTRL1	0x01C4	W	0x00000000	Sharp gain control cfg1.
SHARP_GAIN_CTRL2	0x01C8	W	0x00000000	Sharp gain control cfg2.
SHARP_GAIN_CTRL3	0x01CC	W	0x00000000	Sharp gain control cfg3.
SHARP_GAIN_CTRL4	0x0200	W	0x00000000	Sharp gain control cfg4.
SHARP_GAIN_CTRL5	0x0204	W	0x00000000	Sharp gain control cfg5.
SHARP_GAIN_CTRL6	0x0208	W	0x00000000	Sharp gain control cfg6.
SHARP_GAIN_CTRL7	0x020C	W	0x00000000	Sharp gain control cfg7.
SHARP_GAIN_CTRL8	0x0210	W	0x00000000	Sharp gain control cfg8.

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Name	Offset	Size	Reset Value	Description
SHARP_GAIN_CTRL9	0x0214	W	0x00000000	Sharp gain control cfg9.
SHARP_GAIN_CTRL10	0x0218	W	0x00000000	Sharp gain control cfg10.
SHARP_GAIN_CTRL11	0x021C	W	0x00000000	Sharp gain control cfg11.
SHARP_GAIN_CTRL12	0x0220	W	0x00000000	Sharp gain control cfg12.
SHARP_GAIN_CTRL13	0x0224	W	0x00000000	Sharp gain control cfg13.
SHARP_GAIN_CTRL14	0x0228	W	0x00000000	Sharp gain control cfg14.
SHARP_GAIN_CTRL15	0x022C	W	0x00000000	Sharp gain control cfg15.
SHARP_COLORADJ_CTRL0	0x0230	W	0x00000000	Sharp color adjust control cfg0.
SHARP_COLORADJ_CTRL1	0x0234	W	0x00000000	Sharp color adjust control cfg1.
SHARP_COLORADJ_CTRL2	0x0238	W	0x00000000	Sharp color adjust control cfg2.
SHARP_COLORADJ_CTRL3	0x023C	W	0x00000000	Sharp color adjust control cfg3.
SHARP_COLORADJ_CTRL4	0x0240	W	0x00000000	Sharp color adjust control cfg4.
SHARP_COLORADJ_CTRL5	0x0244	W	0x00000000	Sharp color adjust control cfg5.
SHARP_COLORADJ_CTRL6	0x0248	W	0x00000000	Sharp color adjust control cfg6.
SHARP_COLORADJ_CTRL7	0x024C	W	0x00000000	Sharp color adjust control cfg7.
SHARP_COLORADJ_CTRL8	0x0250	W	0x00000000	Sharp color adjust control cfg8.
SHARP_COLORADJ_CTRL9	0x0254	W	0x00000000	Sharp color adjust control cfg9.
SHARP_COLORADJ_CTRL10	0x0258	W	0x00000000	Sharp color adjust control cfg10.
SHARP_COLORADJ_CTRL11	0x025C	W	0x00000000	Sharp color adjust control cfg11.
SHARP_COLORADJ_CTRL12	0x0260	W	0x00000000	Sharp color adjust control cfg12.
SHARP_COLORADJ_CTRL13	0x0264	W	0x00000000	Sharp color adjust control cfg13.
SHARP_COLORADJ_CTRL14	0x0268	W	0x00000000	Sharp color adjust control cfg14.
SHARP_COLORADJ_CTRL15	0x026C	W	0x00000000	Sharp color adjust control cfg15.
SHARP_TEXTURE_CTRL0	0x0270	W	0x00000000	Sharp texture control cfg0.
SHARP_TEXTURE_CTRL1	0x0274	W	0x00000000	Sharp texture control cfg1.
SHARP_TEXTURE_CTRL2	0x0278	W	0x00000000	Sharp texture control cfg2.
SHARP_TEXTURE_CTRL3	0x027C	W	0x00000000	Sharp texture control cfg3.
SHARP_TEXTURE_CTRL4	0x0280	W	0x00000000	Sharp texture control cfg4.
SHARP_TEXTURE_CTRL5	0x0284	W	0x00000000	Sharp texture control cfg5.
SHARP_LTI_CTRL0	0x0288	W	0x00000000	Sharp lti control cfg0.
SHARP_LTI_CTRL1	0x028C	W	0x00000000	Sharp lti control cfg1.
SHARP_LTI_CTRL2	0x0290	W	0x00000000	Sharp lti control cfg2.
SHARP_LTI_CTRL3	0x0294	W	0x00000000	Sharp lti control cfg3.
SHARP_CTI_CTRL0	0x0298	W	0x00000000	Sharp cti control cfg0.
SHARP_CTI_CTRL1	0x029C	W	0x00000000	Sharp cti control cfg1.
SHARP_CTI_CTRL2	0x02A0	W	0x00000000	Sharp cti control cfg2.
SHARP_CTI_CTRL3	0x02A4	W	0x00000000	Sharp cti control cfg3.
SHARP_DBG_CTRL0	0x02A8	W	0x00000000	Debug signals select.
SHARP_ROI_CTRL0	0x02AC	W	0x00000000	ROI control cfg0.
SHARP_ROI_CTRL1	0x02B0	W	0x00000000	ROI control cfg1.

Notes:Size:B- Byte (8 bits) access, HW- Half WORD (16 bits) access, W-WORD (32 bits) access, DW-Double WORD (64 bits) access

11.5.2.18 MMU0

Name	Offset	Size	Reset Value	Description
MMU0_MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address.
MMU0_MMU_STATUS	0x0004	W	0x00000000	MMU status register.
MMU0_MMU_COMMAND	0x0008	W	0x00000000	MMU command register.

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Name	Offset	Size	Reset Value	Description
MMU0_MMU_PAGE_FAULT_ADDR	0x000C	W	0x00000000	MMU logical address of last page fault.
MMU0_MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register.
MMU0_MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register.
MMU0_MMU_INT_CLEAR	0x0018	W	0x00000000	MMU interrupt clear register.
MMU0_MMU_INT_MASK	0x001C	W	0x00000000	MMU interrupt mask register.
MMU0_MMU_INT_STATUS	0x0020	W	0x00000000	MMU interrupt status register.
MMU0_MMU_AUTO_GATING	0x0024	W	0x00000000	MMU auto gating.

Notes:Size:B- Byte (8 bits) access, HW- Half WORD (16 bits) access, W-WORD (32 bits) access, DW-Double WORD (64 bits) access

11.5.2.19 MMU1

Name	Offset	Size	Reset Value	Description
MMU1_MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address.
MMU1_MMU_STATUS	0x0004	W	0x00000000	MMU status register.
MMU1_MMU_COMMAND	0x0008	W	0x00000000	MMU command register.
MMU1_MMU_PAGE_FAULT_ADDR	0x000C	W	0x00000000	MMU logical address of last page fault.
MMU1_MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register.
MMU1_MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register.
MMU1_MMU_INT_CLEAR	0x0018	W	0x00000000	MMU interrupt clear register.
MMU1_MMU_INT_MASK	0x001C	W	0x00000000	MMU interrupt mask register.
MMU1_MMU_INT_STATUS	0x0020	W	0x00000000	MMU interrupt status register.
MMU1_MMU_AUTO_GATING	0x0024	W	0x00000000	MMU auto gating.

Notes:Size:B- Byte (8 bits) access, HW- Half WORD (16 bits) access, W-WORD (32 bits) access, DW-Double WORD (64 bits) access

11.5.3 Detail Register Description

11.5.3.1 SYS_CTRL

SYS_CTRL_SYS_REG_CFG_DONE

Address: Operational Base(0x27D00000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit. When every bit LOW, don't care the writing corresponding bit.
15	RW	0x1	sw_global_regdone_en Global regdone enable. 1'b0: Disable 1'b1: Enable
14	RW	0x0	reg_load_wb_en In the first setting of the register, the new value was saved into the mirror register.When all the wb register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
13:7	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	reg_load_sys2_en In the first setting of the register, the new value was saved into the mirror register.When all the system2 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
5	RW	0x0	reg_load_sys1_en In the first setting of the register, the new value was saved into the mirror register.When all the system1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
4	RW	0x0	reg_load_sys0_en In the first setting of the register, the new value was saved into the mirror register.When all the system0 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
3	RO	0x0	reserved
2	RW	0x0	reg_load_global2_en In the first setting of the register, the new value was saved into the mirror register.When all the register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
1	RW	0x0	reg_load_global1_en In the first setting of the register, the new value was saved into the mirror register.When all the register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
0	RW	0x0	reg_load_global0_en In the first setting of the register, the new value was saved into the mirror register.When all the register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

SYS_CTRL_SYS_VERSION_INFO

Address: Operational Base(0x27D00000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RW	0x50	major Used for IP structure.
23:16	RW	0x19	minor Big feature change under same structure.
15:0	RW	0x9765	svnbuild RTL current svn number.

SYS_CTRL_SYS_AUTO_GATING_CTRL_IMD

Address: Operational Base(0x27D00000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x1	auto_gating_en 1'b0: Disable auto gating 1'b1: Enable auto gating default auto gating enable

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Bit	Attr	Reset Value	Description
30	RW	0x0	axi1_aclk_static_gating_en If axi1 is not used, axi_aclk_gating_en and axi1_aclk_static_gating_en can be enabled to reduce power consumption. 1'b0: Disable 1'b1: Enable
29	RW	0x0	axi0_aclk_static_gating_en If axi0 is not used, axi_aclk_gating_en and axi0_aclk_static_gating_en can be enabled to reduce power consumption. 1'b0: Disable 1'b1: Enable
28:25	RO	0x0	reserved
24	RW	0x1	rgb_clk_gating_en 1'b0: Disable 1'b1: Enable
23	RO	0x0	reserved
22	RW	0x1	edp_pix_clk_en 1'b0: Disable 1'b1: Enable
21	RO	0x0	reserved
20	RW	0x1	mipi_pix_clk_gating_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x1	hdmi_pix_clk_gating_en 1'b0: Disable 1'b1: Enable
17	RO	0x0	reserved
16	RW	0x1	dp_pix_clk_gating_en 1'b0: Disable 1'b1: Enable
15	RW	0x1	axi_aclk_gating_en 1'b0: Disable 1'b1: Enable
14	RW	0x1	port_dclk_gating_en 1'b0: Disable 1'b1: Enable
13	RW	0x1	prescan_aclk_gating_en 1'b0: Disable 1'b1: Enable
12	RO	0x0	reserved
11	RW	0x1	wb_aclk_gating_en 1'b0: Disable 1'b1: Enable
10:9	RO	0x0	reserved
8	RW	0x1	overlay_aclk_gating_en 1'b0: Disable 1'b1: Enable
7	RW	0x0	aclk_pre_auto_gating_en 1'b0: Disable 1'b1: Enable
6	RW	0x1	win_aclk_gating_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RO	0x0	reserved
4	RW	0x1	esmart_scl_gating_en 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1	RW	0x1	cluster1_aclk_gating_en 1'b0: Disable 1'b1: Enable
0	RW	0x1	cluster0_aclk_gating_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_SYS_WIN_REG_CFG_DONE

Address: Operational Base(0x27D00000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit. When every bit LOW, don't care the writing corresponding bit.
15:8	RO	0x00	reserved
7	RW	0x0	reg_load_esmart3_en In the first setting of the register, the new value was saved into the mirror register. When all the esmart3 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
6	RW	0x0	reg_load_esmart2_en In the first setting of the register, the new value was saved into the mirror register. When all the esmart2 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
5	RW	0x0	reg_load_esmart1_en In the first setting of the register, the new value was saved into the mirror register. When all the esmart1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
4	RW	0x0	reg_load_esmart0_en In the first setting of the register, the new value was saved into the mirror register. When all the esmart0 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
3:2	RO	0x0	reserved
1	RW	0x0	reg_load_cluster1_en In the first setting of the register, the new value was saved into the mirror register. When all the cluster1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

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Bit	Attr	Reset Value	Description
0	RW	0x0	reg_load_cluster0_en In the first setting of the register, the new value was saved into the mirror register. When all the cluster0 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

SYS_CTRL_SYS_AXI0_CTRL_IMD

Address: Operational Base(0x27D00000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	axi0_mmu_idle AXI0 MMU idle status. 1'b0: MMU is busy status. 1'b1: MMU is idle status.
15:10	RO	0x00	reserved
9:4	RW	0x00	axi0_outstanding_num The outstanding number of AXI0.
3:2	RO	0x0	reserved
1	RW	0x0	axi0_outstanding_en AXI0 bus max outstanding enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	axi0_dma_stop Stop AXI0 dma. 1'b0: Disable 1'b1: Enable

SYS_CTRL_SYS_AXI_HURRY_CTRL0_IMD

Address: Operational Base(0x27D00000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:27	RO	0x00000	reserved
26	RW	0x0	axi0_port2_urgency_en 1'b0: Disable 1'b1: Enable
25	RW	0x0	axi0_port1_urgency_en 1'b0: Disable 1'b1: Enable
24	RW	0x0	axi0_port0_urgency_en 1'b0: Disable 1'b1: Enable
23:15	RO	0x00000	reserved
14:13	RW	0x0	axi0_qos_value Noc qos value
12	RW	0x0	axi0_qos_en Noc qos enable. 2'b00: Low priority 2'b11: High priority
11	RW	0x0	axi0_hurry_threshold Noc hurry threshold value.
10:9	RW	0x0	axi0_hurry_value Noc hurry value. 2'b00: Low priority 2'b11: High priority

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Bit	Attr	Reset Value	Description
8	RW	0x0	axi0_hurry_en Noc hurry enable. 1'b0: Disable 1'b1: Enable
7:5	RO	0x0	reserved
4:3	RW	0x0	axi0_hurry_w_mode 2'b00: Noc_hurry_w disable 2'b01: Left 1/4 fifo empty 2'b10: Left 1/2 fifo empty 2'b11: Left 3/4 fifo empty
2:1	RW	0x0	axi0_hurry_w_value Noc hurry value. 2'b00: Low priority 2'b11: High priority
0	RW	0x0	axi0_hurry_w_en Noc hurry enable. 1'b0: Disable 1'b1: Enable

SYS_CTRL_SYS_AXI_HURRY_CTRL1_IMD

Address: Operational Base(0x27D00000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:13	RW	0x0	axi1_qos_value Noc qos value.
12	RW	0x0	axi1_qos_en Noc qos enable.
11	RW	0x0	axi1_hurry_threshold Noc hurry threshold value.
10:9	RW	0x0	axi1_hurry_value Noc hurry value. 2'b00: Low priority 2'b11: High priority
8	RW	0x0	axi1_hurry_en Noc hurry enable. 2'b00: Low priority 2'b11: High priority
7:5	RO	0x0	reserved
4:3	RW	0x0	axi1_hurry_w_mode 2'b00: Noc_hurry_w disable. 2'b01: Left 1/4 fifo empty 2'b10: Left 1/2 fifo empty 2'b11: Left 3/4 fifo empty
2:1	RW	0x0	axi1_hurry_w_value Noc hurry value. 2'b00: Low priority 2'b11: High priority
0	RW	0x0	axi1_hurry_w_en Noc hurry enable. 2'b00: Low priority 2'b11: High priority

SYS_CTRL_SYS_AXI1_CTRL_IMD

Address: Operational Base(0x27D00000) + offset (0x001C)

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Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	axi1_mmu_idle AXI1 MMU idle status. 1'b0: MMU is busy status. 1'b1: MMU is idle status.
15:10	RO	0x00	reserved
9:4	RW	0x00	axi1_outstanding_num The outstanding number of AXI1.
3:2	RO	0x0	reserved
1	RW	0x0	axi1_outstanding_en Axi1 bus max outstanding enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	axi1_dma_stop Stop axi1 dma. 1'b0: Disable 1'b1: Enable

SYS_CTRL_SYS_MMU_CTRL_IMD

Address: Operational Base(0x27D00000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit. When every bit LOW, don't care the writing corresponding bit.
15:14	RW	0x0	mmu1_regdone_sel MMU1 reg done post sel. 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved
13:12	RW	0x0	mmu_regdone_sel MMU0 reg done post sel. 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved
11	RW	0x1	mmu2.0_soft_rst_en 1'b0: MMU2.0 soft resetn disable 1'b1: MMU2.0 soft resetn enable
10	RO	0x0	reserved
9	RW	0x0	mmu1_bypass_en If axi rid > mmu_bypass_id , bypass mmu. 1'b0: Disable 1'b1: Enable
8:4	RW	0x00	mmu_bypass_id If axi rid > mmu_bypass_id , bypass mmu.
3	RO	0x0	reserved
2	RW	0x0	mmu_bypass_en If axi rid > mmu_bypass_id , bypass mmu. 1'b0: Disable 1'b1: Enable
1	RW	0x0	rkmmu2.0_sel 1'b0: AXI0 1'b1: AXI1

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Bit	Attr	Reset Value	Description
0	RW	0x0	rkmmu2.0_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_SYS_AXI_LUT_CTRL_IMD

Address: Operational Base(0x27D00000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x1	lut_use_axi1 1'b0: AXI0 1'b1: AXI1
8	RO	0x0	reserved
7:4	RW	0x1	lut_dma_rid LUT axi read id. VP0 lut axi id = lut_dma_rid. VP1 lut axi id = lut_dma_rid + 1. VP2 lut axi id = lut_dma_rid + 2.
3:2	RW	0x0	lut_dma_rlen LUT axi read brust. 2'b00: Burst16 2'b01: Burst8 2'b1x: Burst4
1	RW	0x0	lut_dma_stop Stop LUT dma. 1'b0: Disable 1'b1: Enable
0	RW	0x0	lut_dma_en Enable LUT dma. 1'b0: Disable 1'b1: Enable

SYS_CTRL_SYS_PORT_CTRL_IMD

Address: Operational Base(0x27D00000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit. When every bit LOW, don't care the writing corresponding bit.
15	RO	0x0	reserved
14	RW	0x0	vp_intr_merge_en Merge vp0, vp1 and vp2 raw interrupt signal to enable interrupt 1'b0: Disable 1'b1: Enable
13:11	RO	0x0	reserved
10	RW	0x0	vfp2_dma_stop_en 1'b0: Disable 1'b1: Enable
9	RW	0x0	vfp1_dma_stop_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	vfp0_dma_stop_en 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5	RW	0x1	auto_cs_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x1	dsp_vs_t_sel 1'b0: Dsp_vs_t_out 1'b1: Dsp_vs_t_pre
3	RO	0x0	reserved
2	RW	0x1	vp2_interlace_frm_reg_done Video output2 reg done framd valid. 1'b0: Reg done every field for interlace. 1'b1: Reg done every frame for interlace.
1	RW	0x1	vp1_interlace_frm_reg_done Video output1 reg done framd valid. 1'b0: Reg done every field for interlace. 1'b1: Reg done every frame for interlace.
0	RW	0x1	vp0_interlace_frm_reg_done Video output0 reg done framd valid. 1'b0: Reg done every field for interlace. 1'b1: Reg done every frame for interlace.

SYS_CTRL_SYS_CLUSTER_PD_CTRL_IMD

Address: Operational Base(0x27D00000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit. When every bit LOW, don't care the writing corresponding bit.
15:1	RO	0x0000	reserved
0	RW	0x0	cluster01_pd_en Power Control to whole Cluster Power Domain, include the cluster0/1 1'b0: Power on (immediate effect) 1'b1: Power down (set corresponding regdone bit and it will be vaild on the next frame start)

SYS_CTRL_SYS_ESMART_PD_CTRL_IMD

Address: Operational Base(0x27D00000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit. When every bit LOW, don't care the writing corresponding bit.
15:12	RO	0x0	reserved
11:10	RW	0x0	bpp_win_sel Select 8BPP lut esmart num. 2'b00: Esmart0 2'b01: Esmart1 2'b10: Esmart2 2'b11: Esmart3
9	RO	0x0	reserved
8	RW	0x0	bpp_lut_en 1'b0: Disable 1'b1: Enable
7:6	RW	0x3	esmart_lb_mode 2'b10: 3 4k 2'b11: 2 4k + 2 2k Other: Reserved
5:1	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	esmart_pd_en Power Control to whole Esmart Power Domain, include the esmart0/1/2/3 1'b0: Power on (immediate effect) 1'b1: Power down (set corresponding regdone bit and it will be vaild on the next frame start)

SYS_CTRL_SYS_VAR_FERQ_CTRL_IMD

Address: Operational Base(0x27D00000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	vp2_almost_full_or_en 1'b0: Disable 1'b1: Enable
29	RW	0x0	vp1_almost_full_or_en 1'b0: Disable 1'b1: Enable
28	RW	0x0	vp0_almost_full_or_en 1'b0: Disable 1'b1: Enable
27	RO	0x0	reserved
26	RW	0x0	vp2_dsp_hold_or_en 1'b0: Disable 1'b1: Enable
25	RW	0x0	vp1_dsp_hold_or_en 1'b0: Disable 1'b1: Enable
24	RW	0x0	vp0_dsp_hold_or_en 1'b0: Disable 1'b1: Enable
23	RO	0x0	reserved
22	RW	0x0	vp2_line_flag_or_en 1'b0: Disable 1'b1: Enable
21	RW	0x0	vp1_line_flag_or_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	vp0_line_flag_or_en 1'b0: Disable 1'b1: Enable
19	RW	0x0	wb_dma_finish_or_en 1'b0: Disable 1'b1: Enable
18	RW	0x0	axi_dma_finish_or_en 1'b0: Disable 1'b1: Enable
17:15	RO	0x0	reserved
14	RW	0x0	vp2_almost_full_and_en 1'b0: Disable 1'b1: Enable
13	RW	0x0	vp1_almost_full_and_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
12	RW	0x0	vp0_almost_full_and_en 1'b0: Disable 1'b1: Enable
11	RO	0x0	reserved
10	RW	0x0	vp2_dsp_hold_and_en 1'b0: Disable 1'b1: Enable
9	RW	0x0	vp1_dsp_hold_and_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	vp0_dsp_hold_and_en 1'b0: Disable 1'b1: Enable
7	RO	0x0	reserved
6	RW	0x0	vp2_line_flag_and_en 1'b0: Disable 1'b1: Enable
5	RW	0x0	vp1_line_flag_and_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	vp0_line_flag_and_en 1'b0: Disable 1'b1: Enable
3	RW	0x0	wb_dma_finish_and_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	axi_dma_finish_and_en 1'b0: Disable 1'b1: Enable
1:0	RW	0x0	dma_finish_mode 2'b00: Src_or 2'b01: Src_and 2'b10: Src_or && src_and 2'b11: Src_or || src_and

SYS_CTRL_METADATA_CTRL

Address: Operational Base(0x27D00000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	metadata_port_sel 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved
29:27	RO	0x0	reserved
26:16	RW	0x000	metadata_size The unit is byte,real-1.
15	RO	0x0	reserved
14:8	RW	0x00	metadata_mem_mst The start write address of the metadata memory.
7:4	RW	0x2	metadata_rid Metadata rid.
3	RO	0x0	metadata_rd_err_t Metadata read error flag 1'b0: Read data normal. 1'b1: Read data error.

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Bit	Attr	Reset Value	Description
2	RO	0x1	metadata_is_writing Metadata write enable 1: Enable 0: Disable
1	RW	0x0	metadata_rd_err_clr Clean metadata read error flag. 1'b0: Disable 1'b1: Enable
0	RW	0x0	metadata_lut_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_METADATA_MST

Address: Operational Base(0x27D00000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	metadata_mst The start read address of metadata in ddr.

SYS_CTRL_FBCD_TIMEOUT_CTRL

Address: Operational Base(0x27D00000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31	RW	0x0	fbcd_timeout_en 1'b0: Disable 1'b1: Enable
30:0	RW	0x00000000	fbcd_timeout_cnt FBCD max time cnt set.

SYS_CTRL_VOP_IO_VSYNC_CTRL

Address: Operational Base(0x27D00000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x3	vop_io_vp2_vsync_sel vsync signal to io. 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: 1'b1
3:2	RW	0x3	vop_io_vp1_vsync_sel vsync signal to io. 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: 1'b1
1:0	RW	0x3	vop_io_vp0_vsync_sel vsync signal to io. 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: 1'b1

SYS_CTRL_SYS_LUT_PORT_SEL

Address: Operational Base(0x27D00000) + offset (0x0058)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit. When every bit LOW, don't care the writing corresponding bit.
15:14	RW	0x3	acm_ahb_port_sel 2'b00: Write sharp select video output0 Other: Reserved
13:12	RW	0x3	gamma_ahb_write_sel 2'b00: Video output0 gamma 2'b01: Video output1 gamma 2'b10: Video output2 gamma Other: Reserved
11:10	RW	0x2	sharp_ahb_port_sel 2'b00: Write sharp select video output0 Other: Reserved
9:0	RO	0x000	reserved

SYS_CTRL_SYS_STATUS0

Address: Operational Base(0x27D00000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vcnt0 Read the video output0 vertical counter.
15:2	RO	0x0000	reserved
1	RW	0x0	mmu_idle MMU idle status.
0	RW	0x0	dma_stop_valid0 AXI dma stop status.

SYS_CTRL_SYS_STATUS1

Address: Operational Base(0x27D00000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vcnt1 Read the video output1 vertical counter.
15:2	RO	0x0000	reserved
1	RW	0x0	mmu_idle MMU idle status.
0	RW	0x0	dma_stop_valid1 AXI dma stop status.

SYS_CTRL_SYS_STATUS2

Address: Operational Base(0x27D00000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vcnt2 Read the video output2 vertical counter.
15:0	RO	0x0000	reserved

SYS_CTRL_SYS_LINE_FLAG0

Address: Operational Base(0x27D00000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:29	RW	0x3	dsp_almost_full_thold If the number of post full lb >= dsp_almost_full_thold + 1,intr_raw_post_full is asserted.

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Bit	Attr	Reset Value	Description
28:16	RW	0x0000	dsp_line_flag_num_1 The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15	RW	0x0	dsp_line_flag0_sel 1'b0: Line_flag0 1'b1: Line_flag1
14:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_line_flag_num_0 The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

SYS_CTRL_SYS_LINE_FLAG1

Address: Operational Base(0x27D00000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:29	RW	0x3	dsp_almost_full_thold If the number of post full lb >= dsp_almost_full_thold + 1,intr_raw_post_full is asserted.
28:16	RW	0x0000	dsp_line_flag_num_1 The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15	RW	0x0	dsp_line_flag1_sel 1'b0: Line_flag0 1'b1: Line_flag1
14:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_line_flag_num_0 The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

SYS_CTRL_SYS_LINE_FLAG2

Address: Operational Base(0x27D00000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:29	RW	0x3	dsp_almost_full_thold If the number of post full lb >= dsp_almost_full_thold + 1,intr_raw_post_full is asserted.
28:16	RW	0x0000	dsp_line_flag_num_1 The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15	RW	0x0	dsp_line_flag2_sel 1'b0: Line_flag0 1'b1: Line_flag1
14:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_line_flag_num_0 The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

SYS_CTRL_SYS0_INTR_EN

Address: Operational Base(0x27D00000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_en_wb_time_out 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
8	RW	0x0	intr_en_wb_resp_err 1'b0: Disable 1'b1: Enable
7	RW	0x0	intr_en_mmu 1'b0: Disable 1'b1: Enable
6	RO	0x0	reserved
5	RW	0x0	int_en_wb_finish 1'b0: Disable 1'b1: Enable
4	RW	0x0	int_en_wb_yrgb_fifo_full 1'b0: Disable 1'b1: Enable
3	RW	0x0	int_en_wb_uv_fifo_full 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_dma0_finish 1'b0: Disable 1'b1: Enable
1	RW	0x0	intr_en_bus0_error 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

SYS_CTRL_SYS0_INTR_CLR

Address: Operational Base(0x27D00000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_clr_wb_time_out Interrupt clear(Auto clear).
8	RW	0x0	intr_clr_wb_resp_err Interrupt clear(Auto clear).
7	RW	0x0	intr_clr_mmu Interrupt clear(Auto clear).
6	RO	0x0	reserved
5	RW	0x0	intr_clr_wb_dma_finish WB_DMA finish interrupt clear(Auto clear).
4	RW	0x0	intr_clr_wb_yrgb_fifo_full Interrupt clear(Auto clear).
3	RW	0x0	intr_clr_wb_uv_fifo_full Interrupt clear(Auto clear).
2	RW	0x0	intr_clr_dma_finish DMA finish interrupt clear(Auto clear).
1	RW	0x0	intr_clr_bus_error Bus error Interrupt clear(Auto clear).
0	RO	0x0	reserved

SYS_CTRL_SYS0_INTR_STATUS

Address: Operational Base(0x27D00000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_status_wb_time_out Wb time out Interrupt status.

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Bit	Attr	Reset Value	Description
8	RW	0x0	intr_status_wb_resp_err Wb resp error Interrupt status
7	RW	0x0	intr_status_mmu Interrupt status of MMU.
6	RO	0x0	reserved
5	RW	0x0	intr_status_wb_dma_finish Interrupt status.
4	RW	0x0	intr_status_wb_yrgb_fifo_full Interrupt status.
3	RW	0x0	intr_status_wb_uv_fifo_full Interrupt status.
2	RW	0x0	intr_status_dma_finish DMA finish interrupt status.
1	RW	0x0	intr_status_bus_error Bus error Interrupt clear status.
0	RO	0x0	reserved

SYS_CTRL_SYS0_INTR_RAW_STATUS

Address: Operational Base(0x27D00000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_status_wb_time_out Wb time out Interrupt raw status.
8	RW	0x0	intr_status_wb_resp_err Wb resp error Interrupt raw status
7	RW	0x0	intr_raw_status_mmu0 Interrupt of MMU0 raw status.
6	RO	0x0	reserved
5	RW	0x0	intr_raw_status_wb_dma_finish Interrupt raw status.
4	RW	0x0	intr_raw_status_wb_yrgb_fifo_full Interrupt raw status.
3	RW	0x0	intr_raw_status_wb_uv_fifo_full Interrupt raw status.
2	RW	0x0	intr_raw_status_dma_finish DMA finish interrupt raw status.
1	RW	0x0	intr_raw_status_bus_error Bus error Interrupt raw status.
0	RO	0x0	reserved

SYS_CTRL_SYS1_INTR_EN

Address: Operational Base(0x27D00000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:8	RO	0x00	reserved
7	RW	0x0	intr_en_mmu1 1'b0: Disable 1'b1: Enable
6:3	RO	0x0	reserved
2	RW	0x0	intr_en_dma1_finish 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	intr_en_bus1_error 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

SYS_CTRL_SYS1_INTR_CLR_SYS

Address: Operational Base(0x27D00000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:8	RO	0x00	reserved
7	RW	0x0	intr_clr_mmu1 Interrupt clear(Auto clear).
6:3	RO	0x0	reserved
2	RW	0x0	intr_clr_dma_finish DMA finish interrupt clear(Auto clear).
1	RW	0x0	intr_clr_bus_error Bus error Interrupt clear(Auto clear).
0	RO	0x0	reserved

SYS_CTRL_SYS1_INTR_STATUS

Address: Operational Base(0x27D00000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	intr_status_mmu1 Interrupt status.
6:3	RO	0x0	reserved
2	RW	0x0	intr_status_dma_finish DMA finish interrupt status.
1	RW	0x0	intr_status_bus_error Bus error Interrupt status.
0	RO	0x0	reserved

SYS_CTRL_SYS1_INTR_RAW_STATUS

Address: Operational Base(0x27D00000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	intr_raw_status_mmu1 Interrupt raw_status.
6:3	RO	0x0	reserved
2	RW	0x0	intr_raw_status_dma_finish DMA finish interrupt raw_status.
1	RW	0x0	intr_raw_status_bus_error Bus error Interrupt raw_status.
0	RO	0x0	reserved

SYS_CTRL_PORT0_INTR_EN

Address: Operational Base(0x27D00000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x0	intr_en_dolby_core3 1'b0: Disable 1'b1: Enable
13	RW	0x0	intr_en_dolby_core2 1'b0: Disable 1'b1: Enable
12	RW	0x0	intr_en_dolby_core1 1'b0: Disable 1'b1: Enable
11:10	RO	0x0	reserved
9	RW	0x0	intr_en_post_full 1'b0: Disable 1'b1: Enable
8	RO	0x0	reserved
7	RW	0x0	intr_en_vfp 1'b0: Disable 1'b1: Enable
6	RW	0x0	intr_en_dsp_hold_valid 1'b0: Disable 1'b1: Enable
5	RW	0x0	intr_en_fs_field 1'b0: Disable 1'b1: Enable
4	RW	0x0	intr_en_post_buf_empty 1'b0: Disable 1'b1: Enable
3	RW	0x0	intr_en_line_flag1 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_line_flag0 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	intr_en_fs 1'b0: Disable 1'b1: Enable

SYS_CTRL_PORT0_INTR_CLR

Address: Operational Base(0x27D00000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_clr_post_full Post buffer almost full interrupt clear(Auto clear).
8	RO	0x0	reserved
7	RW	0x0	intr_clr_vfp Display vfp interrupt clear(Auto clear).
6	RW	0x0	intr_clr_dsp_hold_valid Display hold valid interrupt clear(Auto clear).
5	RW	0x0	intr_clr_fs_field Field start interrupt clear(Auto clear).
4	RW	0x0	intr_clr_post_buf_empty Post buffer empty interrupt clear(Auto clear).

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Bit	Attr	Reset Value	Description
3	RW	0x0	intr_clr_line_flag1 Line flag 1 Interrupt clear(Auto clear).
2	RW	0x0	intr_clr_line_flag0 Line flag 0 Interrupt clear(Auto clear).
1	RW	0x0	intr_clr_fs_new Frame new start interrupt clear(Auto clear).
0	RW	0x0	intr_clr_fs Frame start interrupt clear(Auto clear).

SYS_CTRL_PORT0_INTR_STATUS

Address: Operational Base(0x27D00000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_status_post_full Post buffer almost full interrupt status.
8	RO	0x0	reserved
7	RW	0x0	intr_status_vfp Display vfp interrupt status.
6	RW	0x0	intr_status_dsp_hold_valid Display hold valid interrupt status.
5	RW	0x0	intr_status_fs_field Field start interrupt status.
4	RW	0x0	intr_status_post_buf_empty Post buffer empty interrupt status.
3	RW	0x0	intr_status_line_flag1 Line flag 1 interrupt status.
2	RW	0x0	intr_status_line_flag0 Line flag 0 Interrupt status.
1	RO	0x0	reserved
0	RW	0x0	intr_status_fs Frame start interrupt status.

SYS_CTRL_PORT0_INTR_RAW_STATUS

Address: Operational Base(0x27D00000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_raw_status_post_full Post buffer almost full interrupt raw status.
8	RO	0x0	reserved
7	RW	0x0	intr_raw_status_vfp Display vfp interrupt raw status.
6	RW	0x0	intr_raw_status_dsp_hold_valid Display hold valid interrupt raw status.
5	RW	0x0	intr_raw_status_fs_field Field start interrupt craw status.
4	RW	0x0	intr_raw_status_post_buf_empty Post buffer empty interrupt raw status.
3	RW	0x0	intr_raw_status_line_flag1 Line flag 1 Interrupt raw status.
2	RW	0x0	intr_raw_status_line_flag0 Line flag 0 Interrupt raw status.
1	RO	0x0	reserved
0	RW	0x0	intr_raw_status_fs Frame start interrupt raw status.

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SYS_CTRL_PORT1_INTR_EN

Address: Operational Base(0x27D00000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_en_post_full 1'b0: Disable 1'b1: Enable
8	RO	0x0	reserved
7	RW	0x0	intr_en_vfp 1'b0: Disable 1'b1: Enable
6	RW	0x0	intr_en_dsp_hold_valid 1'b0: Disable 1'b1: Enable
5	RW	0x0	intr_en_fs_field 1'b0: Disable 1'b1: Enable
4	RW	0x0	intr_en_post_buf_empty 1'b0: Disable 1'b1: Enable
3	RW	0x0	intr_en_line_flag1 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_line_flag0 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	intr_en_fs 1'b0: Disable 1'b1: Enable

SYS_CTRL_PORT1_INTR_CLR

Address: Operational Base(0x27D00000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_clr_post_full Post buffer almost full interrupt clear(Auto clear).
8	RO	0x0	reserved
7	RW	0x0	intr_clr_vfp Display vfp interrupt clear(Auto clear).
6	RW	0x0	intr_clr_dsp_hold_valid Display hold valid interrupt clear(Auto clear).
5	RW	0x0	intr_clr_fs_field Field start interrupt clear(Auto clear).
4	RW	0x0	intr_clr_post_buf_empty Post buffer empty interrupt clear(Auto clear).
3	RW	0x0	intr_clr_line_flag1 Line flag 1 Interrupt clear(Auto clear).
2	RW	0x0	intr_clr_line_flag0 Line flag 0 Interrupt clear(Auto clear).
1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	intr_clr_fs Frame start interrupt clear(Auto clear).

SYS_CTRL_PORT1_INTR_STATUS

Address: Operational Base(0x27D00000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_status_post_full Post buffer almost full interrupt status.
8	RO	0x0	reserved
7	RW	0x0	intr_status_vfp Display vfp interrupt status.
6	RW	0x0	intr_status_dsp_hold_valid Display hold valid interrupt status.
5	RW	0x0	intr_status_fs_field Field start interrupt status.
4	RW	0x0	intr_status_post_buf_empty Post buffer empty interrupt status.
3	RW	0x0	intr_status_line_flag1 Line flag 1 interrupt status.
2	RW	0x0	intr_status_line_flag0 Line flag 0 Interrupt status.
1	RO	0x0	reserved
0	RW	0x0	intr_status_fs Frame start interrupt status.

SYS_CTRL_PORT1_INTR_RAW_STATUS

Address: Operational Base(0x27D00000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_raw_status_post_full Post buffer almost full interrupt raw status.
8	RO	0x0	reserved
7	RW	0x0	intr_raw_status_vfp Display vfp interrupt raw status.
6	RW	0x0	intr_raw_status_dsp_hold_valid Display hold valid interrupt raw status.
5	RW	0x0	intr_raw_status_fs_field Field start interrupt craw status.
4	RW	0x0	intr_raw_status_post_buf_empty Post buffer empty interrupt raw status.
3	RW	0x0	intr_raw_status_line_flag1 Line flag 1 Interrupt raw status.
2	RW	0x0	intr_raw_status_line_flag0 Line flag 0 Interrupt raw status.
1	RO	0x0	reserved
0	RW	0x0	intr_raw_status_fs Frame start interrupt raw status.

SYS_CTRL_PORT2_INTR_EN

Address: Operational Base(0x27D00000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.

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Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9	RW	0x0	intr_en_post_full 1'b0: Disable 1'b1: Enable
8	RO	0x0	reserved
7	RW	0x0	intr_en_vfp 1'b0: Disable 1'b1: Enable
6	RW	0x0	intr_en_dsp_hold_valid 1'b0: Disable 1'b1: Enable
5	RW	0x0	intr_en_fs_field 1'b0: Disable 1'b1: Enable
4	RW	0x0	intr_en_post_buf_empty 1'b0: Disable 1'b1: Enable
3	RW	0x0	intr_en_line_flag1 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_line_flag0 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	intr_en_fs 1'b0: Disable 1'b1: Enable

SYS_CTRL_PORT2_INTR_CLR

Address: Operational Base(0x27D00000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_clr_post_full Post buffer almost full interrupt clear(Auto clear).
8	RO	0x0	reserved
7	RW	0x0	intr_clr_vfp Display vfp interrupt clear(Auto clear).
6	RW	0x0	intr_clr_dsp_hold_valid Display hold valid interrupt clear(Auto clear).
5	RW	0x0	intr_clr_fs_field Field start interrupt clear(Auto clear).
4	RW	0x0	intr_clr_post_buf_empty Post buffer empty interrupt clear(Auto clear).
3	RW	0x0	intr_clr_line_flag1 Line flag 1 Interrupt clear(Auto clear).
2	RW	0x0	intr_clr_line_flag0 Line flag 0 Interrupt clear(Auto clear).
1	RO	0x0	reserved
0	RW	0x0	intr_clr_fs Frame start interrupt clear(Auto clear).

SYS_CTRL_PORT2_INTR_STATUS

Address: Operational Base(0x27D00000) + offset (0x00C8)

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Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_status_post_full Post buffer almost full interrupt status.
8	RO	0x0	reserved
7	RW	0x0	intr_status_vfp Display vfp interrupt status.
6	RW	0x0	intr_status_dsp_hold_valid Display hold valid interrupt status.
5	RW	0x0	intr_status_fs_field Field start interrupt status.
4	RW	0x0	intr_status_post_buf_empty Post buffer empty interrupt status.
3	RW	0x0	intr_status_line_flag1 Line flag 1 interrupt status.
2	RW	0x0	intr_status_line_flag0 Line flag 0 Interrupt status.
1	RO	0x0	reserved
0	RW	0x0	intr_status_fs Frame start interrupt status.

SYS_CTRL_PORT2_INTR_RAW_STATUS

Address: Operational Base(0x27D00000) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_raw_status_post_full Post buffer almost full interrupt raw status.
8	RO	0x0	reserved
7	RW	0x0	intr_raw_status_vfp Display vfp interrupt raw status.
6	RW	0x0	intr_raw_status_dsp_hold_valid Display hold valid interrupt raw status.
5	RW	0x0	intr_raw_status_fs_field Field start interrupt craw status.
4	RW	0x0	intr_raw_status_post_buf_empty Post buffer empty interrupt raw status.
3	RW	0x0	intr_raw_status_line_flag1 Line flag 1 Interrupt raw status.
2	RW	0x0	intr_raw_status_line_flag0 Line flag 0 Interrupt raw status.
1	RO	0x0	reserved
0	RW	0x0	intr_raw_status_fs Frame start interrupt raw status.

SYS_CTRL_FBCD_INTR_EN0

Address: Operational Base(0x27D00000) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	intr_en_axi0_hdr3_ctrl_err 1'b0: Disable 1'b1: Enable
6	RW	0x0	intr_en_axi0_hdr2_ctrl_err 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	intr_en_axi0_hdr1_ctrl_err 1'b0: Disable 1'b1: Enable
4	RW	0x0	intr_en_axi0_hdr0_ctrl_err 1'b0: Disable 1'b1: Enable
3	RW	0x0	intr_en_axi0_buff_ctrl_err 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_axi0_pld_dec_err 1'b0: Disable 1'b1: Enable
1	RW	0x0	intr_en_axi0_pld_overflow_err 1'b0: Disable 1'b1: Enable
0	RW	0x0	intr_en_axi0_pld_raddr_err 1'b0: Disable 1'b1: Enable

SYS_CTRL_FBCD_INTR_CLR0

Address: Operational Base(0x27D00000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	intr_clr_axi0_hdr3_ctrl_err Interrupt clear(Auto clear).
6	RW	0x0	intr_clr_axi0_hdr2_ctrl_err Interrupt clear(Auto clear).
5	RW	0x0	intr_clr_axi0_hdr1_ctrl_err Interrupt clear(Auto clear).
4	RW	0x0	intr_clr_axi0_hdr0_ctrl_err Interrupt clear(Auto clear).
3	RW	0x0	intr_clr_axi0_buff_ctrl_err Interrupt clear (Auto clear).
2	RW	0x0	intr_clr_axi0_pld_dec_err Interrupt clear(Auto clear).
1	RW	0x0	intr_clr_axi0_pld_overflow_err Interrupt clear(Auto clear).
0	RW	0x0	intr_clr_axi0_pld_raddr_err Interrupt clear(Auto clear).

SYS_CTRL_FBCD_INTR_STATUS0

Address: Operational Base(0x27D00000) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	intr_status_axi0_hdr3_ctrl_err Interrupt status.
6	RW	0x0	intr_status_axi0_hdr2_ctrl_err Interrupt status.
5	RW	0x0	intr_status_axi0_hdr1_ctrl_err Interrupt status.
4	RW	0x0	intr_status_axi0_hdr0_ctrl_err Interrupt status.
3	RW	0x0	intr_status_axi0_buff_ctrl_err Interrupt status.

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Bit	Attr	Reset Value	Description
2	RW	0x0	intr_status_axi0_pld_dec_err Interrupt status.
1	RW	0x0	intr_status_axi0_pld_overflow_err Interrupt status.
0	RW	0x0	intr_status_axi0_pld_raddr_err Interrupt status.

SYS_CTRL_FBCD_INTR_RAW_STATUS0

Address: Operational Base(0x27D00000) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	intr_raw_status_axi0_hdr3_ctrl_err Interrupt raw status.
6	RW	0x0	intr_raw_status_axi0_hdr2_ctrl_err Interrupt raw status.
5	RW	0x0	intr_raw_status_axi0_hdr1_ctrl_err Interrupt raw status.
4	RW	0x0	intr_raw_status_axi0_hdr0_ctrl_err Interrupt raw status.
3	RW	0x0	intr_raw_status_axi0_buff_ctrl_err Interrupt raw status.
2	RW	0x0	intr_raw_status_axi0_pld_dec_err Interrupt raw status.
1	RW	0x0	intr_raw_status_axi0_pld_overflow_err Interrupt raw status.
0	RW	0x0	intr_raw_status_axi0_pld_raddr_err Interrupt raw status.

SYS_CTRL_SYS_WB_CTRL0

Address: Operational Base(0x27D00000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	wb_port_sel_imd 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved
29:28	RO	0x0	reserved
27:24	RW	0x2	wb_uv_id Use default 0xe.
23:20	RW	0x1	wb_yrgb_id Use default 0xd.
19	RO	0x0	reserved
18	RW	0x0	wb_xgt2_en 1'b0: Disable 1'b1: Enable
17:16	RO	0x0	reserved
15	RW	0x0	wb_rg_swap_en 1'b0: Disable 1'b1: Enable
14	RW	0x0	wb_rb_swap_en 1'b0: Disable 1'b1: Enable
13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	wb_oneframe_mode 1'b0: Disable 1'b1: Enable
11	RW	0x0	wb_post_empty_stop_en 1'b0: Disable 1'b1: Enable
10	RO	0x0	reserved
9	RW	0x0	wb_ythrow_mode 1'b0: Throw odd line 1'b1: Throw even line
8	RW	0x0	wb_ythrow_en 1'b0: Disable 1'b1: Enable
7	RW	0x0	wb_xpsd_bil_en 1'b0: Enable scale 1'b1: Disable scale
6	RW	0x0	wb_rgb2yuv_mode 1'b0: BT601 1'b1: BT709
5	RW	0x0	wb_rgb2yuv_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	wb_dither_en When wb_fmt is RGB565. 1'b0: No dither ,RGB888 clip to RGB565 1'b1: With dither,RGB888 dither to RGB565
3:1	RW	0x0	wb_fmt 3'b000: ARGB888 3'b001: RGB888 3'b010: RGB565 3'b100: YcbCr420 Other: Reserved
0	RW	0x0	wb_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_SYS_WB_XSPD_FACTOR

Address: Operational Base(0x27D00000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x1000	wb_xpsd_bil_factor Factor=((src_width[11:0])/(dst_width[11:0]))*2^12.
15:10	RO	0x00	reserved
9:0	RW	0x030	fifo_thold When wb_fifo_wcnt < fifo_thold, hold the pre_scan timing. fifo_thold = wb_width * fmt_byte / 16. 3'b000: ARGB888,fmt_byte = 4 3'b001: RGB888,fmt_byte = 3 3'b010: RGB565,fmt_byte = 2 3'b100: YcbCr420,fmt_byte = 1 Other: Reserved

SYS_CTRL_SYS_WB_YRGB_MST

Address: Operational Base(0x27D00000) + offset (0x0108)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wb_yrgb_mst YRGB mst address.

SYS_CTRL_SYS_WB_CBR_MST

Address: Operational Base(0x27D00000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wb_cbr_mst CBR mst adress.

SYS_CTRL_SYS_WB_VIR_STRIDE

Address: Operational Base(0x27D00000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	wb_dsp_width The active width of WB picture.
15	RW	0x0	wb_vir_stride_en 1'b0: Disable 1'b1: Enable
14:13	RO	0x0	reserved
12:0	RW	0x0000	wb_vir_stride The virtual width of WB picture.

SYS_CTRL_SYS_WB_TIMEOUT_CTRL

Address: Operational Base(0x27D00000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RW	0x00001f40	wb_timeout_cnt WB time_out cnt.

SYS_CTRL_MIPI0_INFACE_CTRL

Address: Operational Base(0x27D00000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31	RW	0x1	regdone_imd_en Enable interface control register regdone immediately.
30:22	RO	0x000	reserved
21	RW	0x0	mipi_dclk_sel 1'b0: Dclk core 1'b1: Dclk out
20	RW	0x0	mipi_pix_clk_sel 1'b0: Div 2 1'b1: Div 4
19:12	RO	0x00	reserved
11	RW	0x0	mipi_cmd_mode 1'b0: Video mode 1'b1: Command mode
10	RO	0x0	reserved
9	RW	0x0	mipi_data1_sel 1'b0: Select the data0 of video port 1'b1: Select the data1 of video port
8	RW	0x0	mipi_split_en 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x1	mipi_vsync_pol 1'b0: Negative 1'b1: Positive
4	RW	0x1	mipi_hsync_pol 1'b0: Negative 1'b1: Positive
3:2	RW	0x0	mipi_port_sel Select the display output of MIPI interface. 2'b00: Video output0 2'b01: Video output1 2'b1x: Video output2
1	RW	0x0	mipi_clk_out_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	mipi_out_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_HDMI0_INFACE_CTRL

Address: Operational Base(0x27D00000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31	RW	0x1	regdone_imd_en Enable interface control register regdone immediately.
30:22	RO	0x000	reserved
21	RW	0x0	hdmi_dclk_sel 1'b0: Dclk core 1'b1: Dclk out
20	RW	0x0	hdmi_pix_clk_sel 1'b0: Div 2 1'b1: Div 4
19:18	RO	0x0	reserved
17	RW	0x0	hdmi_uv_swap Swap U and V component. 1'b0: Disable 1'b1: Enable
16	RW	0x0	hdmi_yc_swap Swap gray and color component. 1'b0: Disable 1'b1: Enable
15:14	RW	0x0	hdmi_r2y_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
13	RO	0x0	reserved
12	RW	0x0	hdmi_r2y_en 1'b0: Disable 1'b1: Enable
11:10	RO	0x0	reserved
9	RW	0x0	hdmi_data1_sel 1'b0: Select the data0 of video port 1'b1: Select the data1 of video port

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Bit	Attr	Reset Value	Description
8	RW	0x0	hdmi_split_en 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5	RW	0x0	hdmi_vsync_pol 1'b0: Negative 1'b1: Positive
4	RW	0x0	hdmi_hsync_pol 1'b0: Negative 1'b1: Positive
3:2	RW	0x0	hdmi_port_sel Select the display output of MIPI interface. 2'b00: Video output0 2'b01: Video output1 2'b1x: Video output2
1	RW	0x0	hdmi_clk_out_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	hdmi_out_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_EDP0_INFACE_CTRL

Address: Operational Base(0x27D00000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31	RW	0x1	regdone_imd_en Enable interface control register regdone immediately.
30:22	RO	0x000	reserved
21	RW	0x0	edp_dclk_sel 1'b0: Dclk core 1'b1: Dclk out
20	RW	0x0	edp_pix_clk_sel 1'b0: Dclk 1'b1: Port0 dclk
19:10	RO	0x000	reserved
9	RW	0x0	edp_data1_sel 1'b0: Select the data0 of video port 1'b1: Select the data1 of video port
8	RW	0x0	edp_split_en 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5	RW	0x0	edp_vsync_pol 1'b0: Negative 1'b1: Positive
4	RW	0x0	edp_hsync_pol 1'b0: Negative 1'b1: Positive
3:2	RW	0x0	edp_port_sel Select the display output of MIPI interface. 2'b00: Video output0 2'b01: Video output1 2'b1x: Video output2

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Bit	Attr	Reset Value	Description
1	RW	0x0	edp_clk_out_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	edp_out_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_DP0_INFACE_CTRL

Address: Operational Base(0x27D00000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31	RW	0x1	regdone_imd_en Enable interface control register regdone immediately.
30:22	RO	0x000	reserved
21	RW	0x0	dp_dclk_sel 1'b0: Dclk core 1'b1: Dclk out
20	RW	0x0	dp_pix_clk_sel 1'b0: Dclk 1'b1: Dclk div2
19:10	RO	0x000	reserved
9	RW	0x0	dp_data1_sel 1'b0: Select the data0 of video port 1'b1: Select the data1 of video port
8	RW	0x0	dp_split_en 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5	RW	0x0	dp_vsync_pol 1'b0: Negative 1'b1: Positive
4	RW	0x0	dp_hsync_pol 1'b0: Negative 1'b1: Positive
3:2	RW	0x0	dp_port_sel Select the display output of MIPI interface. 2'b00: Video output0 2'b01: Video output1 2'b1x: Video output2
1	RW	0x0	dp_clk_out_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	dp_out_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_RGB_INFACE_CTRL

Address: Operational Base(0x27D00000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31	RW	0x1	regdone_imd_en Enable interface control register regdone immediately.
30:22	RO	0x000	reserved
21	RW	0x0	rgb_dclk_sel 1'b0: Dclk core 1'b1: Dclk out
20:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18	RW	0x0	bt1120_yc_swap Swap gray and color component. 1'b0: Disable 1'b1: Enable
17	RW	0x0	bt1120_uv_swap Swap U and V component. 1'b0: Disable 1'b1: Enable
16	RW	0x0	bt1120_out_en 1'b0: Disable 1'b1: Enable
15	RO	0x0	reserved
14	RW	0x0	bt656_yc_swap Swap GRAY and COLOR component of BT656. 1'b0: Disable 1'b1: Enable
13	RW	0x0	bt656_uv_swap Swap U and V component of BT656. 1'b0: Disable 1'b1: Enable
12	RW	0x0	bt656_out_en 1'b0: Disable 1'b1: Enable
11:10	RO	0x0	reserved
9	RW	0x0	rgb_data1_sel 1'b0: Select the data0 of video port 1'b1: Select the data1 of video port
8	RW	0x0	rgb_split_en 1'b0: Disable 1'b1: Enable
7	RO	0x0	reserved
6	RW	0x0	rgb_den_pol 1'b0: Negative 1'b1: Positive
5	RW	0x0	rgb_vsync_pol 1'b0: Negative 1'b1: Positive
4	RW	0x0	rgb_hsync_pol 1'b0: Negative 1'b1: Positive
3:2	RW	0x0	rgb_port_sel Select the display output of RGB interface. 2'b01: Video output1 2'b1x: Video output2 Other: Reserved
1	RW	0x0	rgb_clk_out_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	rgb_out_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_DP1_INFACE_CTRL

Address: Operational Base(0x27D00000) + offset (0x01A4)

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Bit	Attr	Reset Value	Description
31	RW	0x1	regdone_imd_en Enable interface control register regdone immediately.
30:22	RO	0x000	reserved
21	RW	0x0	dp_dclk_sel 1'b0: Dclk core 1'b1: Dclk out
20	RW	0x0	dp_pix_clk_sel 1'b0: Dclk 1'b1: Dclk div2
19:10	RO	0x000	reserved
9	RW	0x0	dp_data1_sel 1'b0: Select the data0 of video port 1'b1: Select the data1 of video port
8	RW	0x0	dp_split_en 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5	RW	0x0	dp_vsync_pol 1'b0: Negative 1'b1: Positive
4	RW	0x0	dp_hsync_pol 1'b0: Negative 1'b1: Positive
3:2	RW	0x0	dp_port_sel Select the display output of MIPI interface. 2'b00: Video output0 2'b01: Video output1 2'b1x: Video output2
1	RW	0x0	dp_clk_out_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	dp_out_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_DP2_INFACE_CTRL

Address: Operational Base(0x27D00000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31	RW	0x1	regdone_imd_en Enable interface control register regdone immediately.
30:22	RO	0x000	reserved
21	RW	0x0	dp_dclk_sel 1'b0: Dclk core 1'b1: Dclk out
20	RW	0x0	dp_pix_clk_sel 1'b0: Dclk 1'b1: Dclk div2
19:10	RO	0x000	reserved
9	RW	0x0	dp_data1_sel 1'b0: Select the data0 of video port 1'b1: Select the data1 of video port
8	RW	0x0	dp_split_en 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x0	dp_vsync_pol 1'b0: Negative 1'b1: Positive
4	RW	0x0	dp_hsync_pol 1'b0: Negative 1'b1: Positive
3:2	RW	0x0	dp_port_sel Select the display output of MIPI interface. 2'b00: Video output0 2'b01: Video output1 2'b1x: Video output2
1	RW	0x0	dp_clk_out_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	dp_out_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_SEC_DRM_CTRL

Address: Operational Base(0x27D00000) + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	sec_axi1_rid3_prot_en 1'b0: Disable 1'b1: Enable
22	RW	0x0	sec_axi1_rid2_prot_en 1'b0: Disable 1'b1: Enable
21	RW	0x0	sec_axi1_rid1_prot_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	sec_axi1_rid0_prot_en 1'b0: Disable 1'b1: Enable
19	RW	0x0	sec_axi0_rid3_prot_en 1'b0: Disable 1'b1: Enable
18	RW	0x0	sec_axi0_rid2_prot_en 1'b0: Disable 1'b1: Enable
17	RW	0x0	sec_axi0_rid1_prot_en 1'b0: Disable 1'b1: Enable
16	RW	0x0	sec_axi0_rid0_prot_en 1'b0: Disable 1'b1: Enable
15	RW	0x0	sec_esmart3_en 1'b0: Disable 1'b1: Enable
14	RW	0x0	sec_esmart2_en 1'b0: Disable 1'b1: Enable
13	RW	0x0	sec_esmart1_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
12	RW	0x0	sec_esmart0_en 1'b0: Disable 1'b1: Enable
11:10	RO	0x0	reserved
9	RW	0x0	sec_cluster1_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	sec_cluster0_en 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5	RW	0x0	sec_rid_lock_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	sec_wb_dis 1'b0: Disable 1'b1: Enable
3:1	RO	0x0	reserved
0	RW	0x0	sec_drm_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_SEC_DRM_PORT_SEL

Address: Operational Base(0x27D00000) + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	drm_esmart3_port_sel 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved
27:26	RO	0x0	reserved
25:24	RW	0x0	drm_esmart2_port_sel 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved
23:22	RO	0x0	reserved
21:20	RW	0x0	drm_esmart1_port_sel 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved
19:18	RO	0x0	reserved
17:16	RW	0x0	drm_esmart0_port_sel 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved
15:6	RO	0x000	reserved
5:4	RW	0x0	drm_cluster1_port_sel 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved

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Bit	Attr	Reset Value	Description
3:2	RO	0x0	reserved
1:0	RW	0x0	drm_cluster0_port_sel 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved

SYS_CTRL_SEC_PORT0_LAYER_SEL

Address: Operational Base(0x27D00000) + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	drm_layer3_sel_en Enable sec_layer3 sel. 1'b0: Disable 1'b1: Enable
14:12	RW	0x0	drm_layer3_sel Secure layer3 sel. 3'b0000: Cluster0 3'b0001: Cluster1 3'b0010: Esmart0 3'b0011: Esmart2 Other: Reserved
11	RW	0x0	drm_layer2_sel_en Enable sec_layer2 sel. 1'b0: Disable 1'b1: Enable
10:8	RW	0x0	drm_layer2_sel Secure layer2 sel. 3'b0000: Cluster0 3'b0001: Cluster1 3'b0010: Esmart0 3'b0011: Esmart2 Other: Reserved
7	RW	0x0	drm_layer1_sel_en Enable sec_layer1 sel. 1'b0: Disable 1'b1: Enable
6:4	RW	0x0	drm_layer1_sel Secure layer1 sel. 3'b0000: Cluster0 3'b0001: Cluster1 3'b0010: Esmart0 3'b0011: Esmart2 Other: Reserved
3	RW	0x0	drm_layer0_sel_en Enable sec_layer0 sel. 1'b0: Disable 1'b1: Enable
2:0	RW	0x0	drm_layer0_sel Secure layer0 sel. 3'b0000: Cluster0 3'b0001: Cluster1 3'b0010: Esmart0 3'b0011: Esmart2 Other: Reserved

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SYS_CTRL_SEC_PORT1_LAYER_SEL

Address: Operational Base(0x27D00000) + offset (0x01EC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	drm_layer3_sel_en Enable sec_layer3 sel. 1'b0: Disable 1'b1: Enable
14:12	RW	0x0	drm_layer3_sel Secure layer3 sel. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart1 3'b011: Esmart3 Other: Reserved
11	RW	0x0	drm_layer2_sel_en Enable sec_layer2 sel. 1'b0: Disable 1'b1: Enable
10:8	RW	0x0	drm_layer2_sel Secure layer2 sel. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart1 3'b011: Esmart3 Other: Reserved
7	RW	0x0	drm_layer1_sel_en Enable sec_layer1 sel. 1'b0: Disable 1'b1: Enable
6:4	RW	0x0	drm_layer1_sel Secure layer1 sel. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart1 3'b011: Esmart3 Other: Reserved
3	RW	0x0	drm_layer0_sel_en Enable sec_layer0 sel. 1'b0: Disable 1'b1: Enable
2:0	RW	0x0	drm_layer0_sel Secure layer0 sel. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart1 3'b011: Esmart3 Other: Reserved

SYS_CTRL_SEC_PORT2_LAYER_SEL

Address: Operational Base(0x27D00000) + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15	RW	0x0	drm_layer3_sel_en Enable sec_layer3 sel. 1'b0: Disable 1'b1: Enable
14:12	RW	0x0	drm_layer3_sel Secure layer3 sel. 3'b0000: Esmart0 3'b0001: Esmart1 3'b0010: Esmart2 3'b0011: Esmart3 Other: Reserved
11	RW	0x0	drm_layer2_sel_en Enable sec_layer2 sel. 1'b0: Disable 1'b1: Enable
10:8	RW	0x0	drm_layer2_sel Secure layer2 sel. 3'b0000: Esmart0 3'b0001: Esmart1 3'b0010: Esmart2 3'b0011: Esmart3 Other: Reserved
7	RW	0x0	drm_layer1_sel_en Enable sec_layer1 sel. 1'b0: Disable 1'b1: Enable
6:4	RW	0x0	drm_layer1_sel Secure layer1 sel. 3'b0000: Esmart0 3'b0001: Esmart1 3'b0010: Esmart2 3'b0011: Esmart3 Other: Reserved
3	RW	0x0	drm_layer0_sel_en Enable sec_layer0 sel. 1'b0: Disable 1'b1: Enable
2:0	RW	0x0	drm_layer0_sel Secure layer0 sel. 3'b0000: Esmart0 3'b0001: Esmart1 3'b0010: Esmart2 3'b0011: Esmart3 Other: Reserved

SYS_CTRL_SEC_AXI_RID_PROT

Address: Operational Base(0x27D00000) + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sec_axi1_rid3_prot Secure axi1 read id.
27:24	RW	0x0	sec_axi1_rid2_prot Secure axi1 read id.
23:20	RW	0x0	sec_axi1_rid1_prot Secure axi1 read id.

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Bit	Attr	Reset Value	Description
19:16	RW	0x0	sec_axi1_rid0_prot Secure axi1 read id.
15:12	RW	0x0	sec_axi0_rid3_prot Secure axi0 read id.
11:8	RW	0x0	sec_axi0_rid2_prot Secure axi0 read id.
7:4	RW	0x0	sec_axi0_rid1_prot Secure axi0 read id.
3:0	RW	0x0	sec_axi0_rid0_prot Secure axi0 read id.

SYS_CTRL_SYS_OTP_MIRR_CTRL_IMD

Address: Operational Base(0x27D00000) + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dis_otp_fuction Disable otp function step by step. step One: Write 32'h20151223 step Two: Write 32'h20180224

11.5.3.2 OVERLAY_SYSTEM

OVERLAY_SYSTEM_EXTRA_ALPHA_CTRL_IMD

Address: Operational Base(0x27D00500) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	port0_extra_alpha_en 1'b0: Disable 1'b1: Enable

OVERLAY_SYSTEM_CLUSTER0_SRC_COLOR_CTRL

Address: Operational Base(0x27D00500) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0

OVERLAY_SYSTEM_CLUSTER0_DST_COLOR_CTRL

Address: Operational Base(0x27D00500) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0

OVERLAY_SYSTEM_CLUSTER0_SRC_ALPHA_CTRL

Address: Operational Base(0x27D00500) + offset (0x0038)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_SYSTEM_CLUSTER0_DST_ALPHA_CTRL

Address: Operational Base(0x27D00500) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

OVERLAY_SYSTEM_CLUSTER1_SRC_COLOR_CTRL

Address: Operational Base(0x27D00500) + offset (0x0040)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0

OVERLAY_SYSTEM_CLUSTER1_DST_COLOR_CTRL

Address: Operational Base(0x27D00500) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0

OVERLAY_SYSTEM_CLUSTER1_SRC_ALPHA_CTRL

Address: Operational Base(0x27D00500) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_SYSTEM_CLUSTER1_DST_ALPHA_CTRL

Address: Operational Base(0x27D00500) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

11.5.3.3 OVERLAY_PORT0

OVERLAY_PORT0_OVERLAY_CTRL

Address: Operational Base(0x27D00600) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	sdr2hdr_path_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	hdr10_path_en 1'b0: Disable 1'b1: Enable
3:1	RO	0x0	reserved
0	RW	0x0	overlay_mode 1'b0: RGB overlay 1'b1: YUV overlay

OVERLAY_PORT0_LAYER_SEL

Address: Operational Base(0x27D00600) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0xf	layer3_sel Layer3_select port. 4'b0000: Cluster0 4'b0001: Cluster1 4'b0010: Esmart0 4'b0011: Esmart2 4'b1xxx: Disable

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Bit	Attr	Reset Value	Description
11:8	RW	0xf	layer2_sel Layer2_select port. 4'b0000: Cluster0 4'b0001: Cluster1 4'b0010: Esmart0 4'b0011: Esmart2 4'b1xxx: Disable
7:4	RW	0xf	layer1_sel Layer1_select port. 4'b0000: Cluster0 4'b0001: Cluster1 4'b0010: Esmart0 4'b0011: Esmart2 4'b1xxx: Disable
3:0	RW	0xf	layer0_sel Layer0_select port. 4'b0000: Cluster0 4'b0001: Cluster1 4'b0010: Esmart0 4'b0011: Esmart2 4'b1xxx: Disable

OVERLAY_PORT0_MIX0_SRC_COLOR_CTRL

Address: Operational Base(0x27D00600) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8

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Bit	Attr	Reset Value	Description
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0

OVERLAY_PORT0_MIX0_DST_COLOR_CTRL

Address: Operational Base(0x27D00600) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0

OVERLAY_PORT0_MIX0_SRC_ALPHA_CTRL

Address: Operational Base(0x27D00600) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT0_MIX0_DST_ALPHA_CTRL

Address: Operational Base(0x27D00600) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

OVERLAY_PORT0_MIX1_SRC_COLOR_CTRL

Address: Operational Base(0x27D00600) + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0

OVERLAY_PORT0_MIX1_DST_COLOR_CTRL

Address: Operational Base(0x27D00600) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0

OVERLAY_PORT0_MIX1_SRC_ALPHA_CTRL

Address: Operational Base(0x27D00600) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT0_MIX1_DST_ALPHA_CTRL

Address: Operational Base(0x27D00600) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

OVERLAY_PORT0_MIX2_SRC_COLOR_CTRL

Address: Operational Base(0x27D00600) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0

OVERLAY_PORT0_MIX2_DST_COLOR_CTRL

Address: Operational Base(0x27D00600) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0

OVERLAY_PORT0_MIX2_SRC_ALPHA_CTRL

Address: Operational Base(0x27D00600) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT0_MIX2_DST_ALPHA_CTRL

Address: Operational Base(0x27D00600) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

OVERLAY_PORT0_EXTRA_SRC_COLOR_CTRL

Address: Operational Base(0x27D00600) + offset (0x0050)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0

OVERLAY_PORT0_EXTRA_DST_COLOR_CTRL

Address: Operational Base(0x27D00600) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0

OVERLAY_PORT0_EXTRA_SRC_ALPHA_CTRL

Address: Operational Base(0x27D00600) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT0_EXTRA_DST_ALPHA_CTRL

Address: Operational Base(0x27D00600) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

OVERLAY_PORT0_HDR_SRC_COLOR_CTRL

Address: Operational Base(0x27D00600) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0

OVERLAY_PORT0_HDR_DST_COLOR_CTRL

Address: Operational Base(0x27D00600) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0

OVERLAY_PORT0_HDR_SRC_ALPHA_CTRL

Address: Operational Base(0x27D00600) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT0_HDR_DST_ALPHA_CTRL

Address: Operational Base(0x27D00600) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

OVERLAY_PORT0_BG_MIX_CTRL

Address: Operational Base(0x27D00600) + offset (0x0070)

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Bit	Attr	Reset Value	Description
31:24	RW	0x10	bg_dly_num BG delay cycle number.
23:16	RO	0x00	reserved
15:8	RW	0x00	bg_global_alpha Source global alpha value(Ags).
7:5	RO	0x0	reserved
4	RW	0x0	bg_line_end_mode P2I bg line end sel 1'b0: Pre_line_end 1'b1: Bg_line_en
3	RW	0x0	bg_alpha_sat_mode Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_
2	RW	0x0	bg_alpha_pre_mul Source color mode. 1'b0: Cs 1'b1: Cs*As0
1	RW	0x0	bg_alpha_mode Select source alpha. 1'b0: Global alpha 1'b1: Per_pixel alpha
0	RW	0x0	bg_alpha_en Enable bg alpha blending. 1'b0: Disable 1'b1: Enable

11.5.3.4 OVERLAY_PORT1

OVERLAY_PORT1_OVERLAY_CTRL

Address: Operational Base(0x27D00700) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	overlay_mode 1'b0: RGB overlay 1'b1: YUV overlay

OVERLAY_PORT1_LAYER_SEL

Address: Operational Base(0x27D00700) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0xf	layer3_sel layer3 select port. 4'b0000: Cluster0 4'b0001: Cluster1 4'b0010: Esmart1 4'b0011: Esmart3 4'b1xxx: Disable
11:8	RW	0xf	layer2_sel layer2 select port. 4'b0000: Cluster0 4'b0001: Cluster1 4'b0010: Esmart1 4'b0011: Esmart3 4'b1xxx: Disable

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Bit	Attr	Reset Value	Description
7:4	RW	0xf	layer1_sel layer1 select port. 4'b0000: Cluster0 4'b0001: Cluster1 4'b0010: Esmart1 4'b0011: Esmart3 4'b1xxx: Disable
3:0	RW	0xf	layer0_sel Layer0 select port. 4'b0000: Cluster0 4'b0001: Cluster1 4'b0010: Esmart1 4'b0011: Esmart3 4'b1xxx: Disable

OVERLAY_PORT1_MIX0_SRC_COLOR_CTRL

Address: Operational Base(0x27D00700) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As

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Bit	Attr	Reset Value	Description
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0

OVERLAY_PORT1_MIX0_DST_COLOR_CTRL

Address: Operational Base(0x27D00700) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0

OVERLAY_PORT1_MIX0_SRC_ALPHA_CTRL

Address: Operational Base(0x27D00700) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT1_MIX0_DST_ALPHA_CTRL

Address: Operational Base(0x27D00700) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

OVERLAY_PORT1_MIX1_SRC_COLOR_CTRL

Address: Operational Base(0x27D00700) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0

OVERLAY_PORT1_MIX1_DST_COLOR_CTRL

Address: Operational Base(0x27D00700) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0

OVERLAY_PORT1_MIX1_SRC_ALPHA_CTRL

Address: Operational Base(0x27D00700) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT1_MIX1_DST_ALPHA_CTRL

Address: Operational Base(0x27D00700) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

OVERLAY_PORT1_MIX2_SRC_COLOR_CTRL

Address: Operational Base(0x27D00700) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As

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Bit	Attr	Reset Value	Description
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0

OVERLAY_PORT1_MIX2_DST_COLOR_CTRL

Address: Operational Base(0x27D00700) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0

OVERLAY_PORT1_MIX2_SRC_ALPHA_CTRL

Address: Operational Base(0x27D00700) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT1_MIX2_DST_ALPHA_CTRL

Address: Operational Base(0x27D00700) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

OVERLAY_PORT1_BG_MIX_CTRL

Address: Operational Base(0x27D00700) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RW	0x0a	bg_dly_num BG delay cycle number.
23:16	RO	0x00	reserved
15:8	RW	0x00	bg_global_alpha Source global alpha value(Ags).
7:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	bg_line_end_mode P2I bg line end sel 1'b0: Pre_line_end 1'b1: Bg_line_en
3	RW	0x0	bg_alpha_sat_mode Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_
2	RW	0x0	bg_alpha_pre_mul Source color mode. 1'b0: Cs 1'b1: Cs*As0
1	RW	0x0	bg_alpha_mode Select source alpha. 1'b0: Global alpha 1'b1: Per_pixel alpha
0	RW	0x0	bg_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable

11.5.3.5 OVERLAY_PORT2

OVERLAY_PORT2_OVERLAY_CTRL

Address: Operational Base(0x27D00800) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	overlay_mode 1'b0: RGB overlay 1'b1: YUV overlay

OVERLAY_PORT2_LAYER_SEL

Address: Operational Base(0x27D00800) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0xf	layer3_sel layer3 select port. 4'b0000: Cluster0 4'b0001: Cluster1 4'b0010: Esmart1 4'b0011: Esmart3 4'b1xxx: Disable
11:8	RW	0xf	layer2_sel layer2 select port. 4'b0000: Cluster0 4'b0001: Cluster1 4'b0010: Esmart1 4'b0011: Esmart3 4'b1xxx: Disable
7:4	RW	0xf	layer1_sel layer1 select port. 4'b0000: Cluster0 4'b0001: Cluster1 4'b0010: Esmart1 4'b0011: Esmart3 4'b1xxx: Disable

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Bit	Attr	Reset Value	Description
3:0	RW	0xf	layer0_sel Layer0 select port. 4'b0000: Cluster0 4'b0001: Cluster1 4'b0010: Esmart1 4'b0011: Esmart3 4'b1xxx: Disable

OVERLAY_PORT2_MIX0_SRC_COLOR_CTRL

Address: Operational Base(0x27D00800) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0

OVERLAY_PORT2_MIX0_DST_COLOR_CTRL

Address: Operational Base(0x27D00800) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0

OVERLAY_PORT2_MIX0_SRC_ALPHA_CTRL

Address: Operational Base(0x27D00800) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8

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Bit	Attr	Reset Value	Description
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT2_MIX0_DST_ALPHA_CTRL

Address: Operational Base(0x27D00800) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

OVERLAY_PORT2_MIX1_SRC_COLOR_CTRL

Address: Operational Base(0x27D00800) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0

OVERLAY_PORT2_MIX1_DST_COLOR_CTRL

Address: Operational Base(0x27D00800) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8

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Bit	Attr	Reset Value	Description
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0

OVERLAY_PORT2_MIX1_SRC_ALPHA_CTRL

Address: Operational Base(0x27D00800) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT2_MIX1_DST_ALPHA_CTRL

Address: Operational Base(0x27D00800) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

OVERLAY_PORT2_MIX2_SRC_COLOR_CTRL

Address: Operational Base(0x27D00800) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0

OVERLAY_PORT2_MIX2_DST_COLOR_CTRL

Address: Operational Base(0x27D00800) + offset (0x0044)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0

OVERLAY_PORT2_MIX2_SRC_ALPHA_CTRL

Address: Operational Base(0x27D00800) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0 3'b101: Ags Other: Reserved
4	RW	0x0	src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_+As0_>>7 1'b1: As0_
3:2	RW	0x0	src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8

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Bit	Attr	Reset Value	Description
1	RW	0x0	src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

OVERLAY_PORT2_MIX2_DST_ALPHA_CTRL

Address: Operational Base(0x27D00800) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Agd Other: Reserved
4	RW	0x0	dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_+Ad0_>>7 1'b1: Ad0_
3:2	RW	0x0	dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

OVERLAY_PORT2_BG_MIX_CTRL

Address: Operational Base(0x27D00800) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	bg_dly_num BG delay cycle number.
23:16	RO	0x00	reserved
15:8	RW	0x00	bg_global_alpha Source global alpha value(Ags).
7:5	RO	0x0	reserved
4	RW	0x0	bg_line_end_mode P2I bg line end sel 1'b0: Pre_line_end 1'b1: Bg_line_en
3	RW	0x0	bg_alpha_sat_mode Source alpha select mode of color channel. 1'b0: As0_+As0_>>7 1'b1: As0_
2	RW	0x0	bg_alpha_pre_mul Source color mode. 1'b0: Cs 1'b1: Cs*As0

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Bit	Attr	Reset Value	Description
1	RW	0x0	bg_alpha_mode Select source alpha. 1'b0: Global alpha 1'b1: Per_pixel alpha
0	RW	0x0	bg_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable

11.5.3.6 POST0_CTRL

POST0_CTRL_POST_DSP_CTRL

Address: Operational Base(0x27D00C00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x1	vop_standby_en_imd Writing 1 to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame.The output would be blank.When writing 0 to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable *Black display is recommended before setting standby mode enable.
30	RW	0x0	vop_fp_standby_en_imd Writing 1 to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame.The output would be blank.When writing 0 to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable *Black display is recommended before setting standby mode enable.
29	RO	0x0	reserved
28	RW	0x0	dsp_lut_en 1'b0: Disable 1'b1: Enable *This bit should be 0 when CPU updates the LUT, and should be 1 when Display LUT mode enable.
27	RW	0x0	dsp_black_en When this bit enable, the pixel data output is all black(0x000000).
26	RW	0x0	dsp_out_zero 1'b0: Normal output 1'b1: All output '0'
25	RO	0x0	reserved
24	RW	0x0	dsp_blank_en When this bit enable, the Hsync/Vsync/Den output is blank.
23	RW	0x0	post_lb_mode 1'b0 : 4x4096 1'b1 : 8x2048 *If post_act_width > 2048 post_lb_mode =0else config 0 or 1
22	RW	0x0	gamma_update_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
21	RO	0x0	reserved
20	RW	0x0	dither_down_mode 1'b0: RGB888 to RGB565 1'b1: RGB888 to RGB666
19:18	RW	0x0	dither_down_sel 2'b0: ALG 2'b1: FRC2.0
17	RW	0x0	dither_down_en 1'b0: Disable 1'b1: Enable
16	RW	0x0	pre_dither_down_en 10bit->8bit (allegro).
15	RW	0x0	dsp_out_rgb_yuv 1'b0: RGB = {0x0,0x0,0x0} 1'b1: YUV = {0x80,0x0,0x0}
14	RO	0x0	reserved
13	RW	0x0	dsp_x_mir_en Post dsp x mirror. 1'b0: Disable 1'b1: Enable
12	RW	0x0	dsp_dummy_swap 1'b0: B+G+R+dummy 1'b1: Dummy+B+G+R
11	RW	0x0	dsp_delta_swap 1'b0: Disable 1'b1: Enable *See detail description in Delta display charpter
10	RW	0x0	dsp_rg_swap 1'b0: RGB 1'b1: GRB
9	RW	0x0	dsp_rb_swap 1'b0: RGB 1'b1: BGR
8	RW	0x0	dsp_bg_swap 1'b0: RGB 1'b1: RBG
7	RW	0x0	dsp_interlace 1'b0: Disable 1'b1: Enable
6	RW	0x0	dsp_filed_pol 1'b0: Normal 1'b1: Invert
5	RW	0x0	dsp_p2i_en Enable p2i. 1'b0: Disable 1'b1: Enable
4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0xf	dsp_out_mode 4'b0000: Parallel 24-bit output{R[7:0],2'b0,G[7:0],2'b0,B[7:0],2'b0} 4'b0001: Parallel 18-bit RGB666 output{R[5:0],4'b0,G[5:0],4'b0,B[5:0],4'b0} 4'b0010: Parallel 16-bit RGB565 output{R[4:0],5'b0,G[5:0],4'b0,B[4:0],5'b0} 4'b1100: DP/EDP YUV422 4'b1101: HDMI YUV422 4'b1110: DP/HDMI YUV420 4'b1111: Parallel 30-bit RGBaaa output{R[9:0],G[9:0],B[9:0]} Others: Reserved

POST0_CTRL_POST_MIPI_CTRL

Address: Operational Base(0x27D00C00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	edpi_wms_fs Frame start in hold mode. 1'b0: Disable 1'b1: Enable
30	RW	0x0	edpi_wms_hold_en Enable hold mode. 1'b0: Disable 1'b1: Enable
29	RW	0x0	edpi_te_mode 1'b0: New frame is started by te. 1'b1: New frame is started by te and wms_fs.
28	RW	0x0	edpi_te_en Enable MIPI TE. 1'b0: Disable 1'b1: Enable
27:24	RW	0x0	doub_channel_overlap_num 4'h0: Overlap num 0 4'h1: Overlap num 2 4'h2: Overlap num 4 4'h3: Overlap num 6 4'h4: Overlap num 8 4'h5: Overlap num 10 4'h6: Overlap num 12 4'h7: Overlap num 14 4'h8: Overlap num 16
23:22	RO	0x0	reserved
21	RW	0x0	doub_channel_swap Swap two channel data of MIPI.
20	RW	0x0	doub_channel_en Enable mipi double channel. 1'b0: Disable 1'b1: Enable
19:0	RO	0x00000	reserved

POST0_CTRL_POST_COLOR_CTRL

Address: Operational Base(0x27D00C00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:20	RW	0x0	sw_urgency_thh When post_lb > sw_urgency_thh, post set urgency to 1 ‘b0. Realse the priority of the layer on the AXI0 bus.
19:16	RW	0x0	sw_urgency_thl When post_lb < sw_urgency_thl, post set urgency to 1 ‘b1. Increase the priority of the layer on the AXI0 bus.
15:9	RO	0x00	reserved
8	RW	0x0	sw_urgency_en 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5:4	RW	0x0	io_vsync_sel 2'b00: 1'b1 2'b01: Line_flag0 2'b10: Line_flag1 2'b11: Vsync
3:2	RO	0x0	reserved
1	RW	0x0	color_bar_mode Select color bar mode. 1'b0: Horizontal mode 1'b1: Vertical mode
0	RW	0x0	color_bar_en Enable color bar. 1'b0: Disable 1'b1: Enable

POST0_CTRL_POST_CORE_CLK

Address: Operational Base(0x27D00C00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	dclk_out_sel 1'b0: Dclk 1'b1: Dclk_div2
1	RO	0x0	reserved
0	RW	0x0	dclk_core_sel 1'b0: Dclk 1'b1: Dclk_div2

POST0_CTRL_POST_3D_LUT_CTRL

Address: Operational Base(0x27D00C00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsp_3dlut_addr AHB write or read lut address of 3d_lut.
15:5	RO	0x000	reserved
4	RW	0x1	dsp_3dlut_gating_en 1'b0: Disable 1'b1: Enable
3	RW	0x0	dsp_3dlut_mode 1'b0: Lut is fetched by axi 1'b1: Lut is fetched by ahb
2	RW	0x0	dsp_3dlut_update_en Update the lut of 3d_lut. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	dsp_3dlut_bypass_en Bypass 3d_lut fuction. 1'b0: Disable 1'b1: Enable
0	RW	0x0	dsp_3dlut_en 1'b0: Disable 1'b1: Enable

POST0_CTRL_POST_3D_LUT_R

Address: Operational Base(0x27D00C00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	lut_3d_r_comp 3D_lut red component.

POST0_CTRL_POST_3D_LUT_G

Address: Operational Base(0x27D00C00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	lut_3d_g_comp 3D_lut green component.

POST0_CTRL_POST_3D_LUT_B

Address: Operational Base(0x27D00C00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	lut_3d_b_comp 3D_lut blue component.

POST0_CTRL_POST_3DLUT_MST

Address: Operational Base(0x27D00C00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	post_3dlut_mst 3D_lut memory start address.

POST0_CTRL_POST_DSP_BG

Address: Operational Base(0x27D00C00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x1	bg_display_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	dsp_bg_red 10bit red color of background.
19:10	RW	0x000	dsp_bg_blue 10bit blue color of background.
9:0	RW	0x000	dsp_bg_green 10bit green color of background.

POST0_CTRL_POST_PRE_SCAN_HTIMING

Address: Operational Base(0x27D00C00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:16	RW	0x0000	pre_scan_hactive Pre_scan horizontal active pixel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	pre_scan_hblank Pre_scan horizontal blank pixel.

POST0_CTRL_POST_DSP_HACT_INFO

Address: Operational Base(0x27D00C00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_hact_st_post Panel display scanning horizontal active start point
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hact_end_post Panel display scanning horizontal active end point

POST0_CTRL_POST_DSP_VACT_INFO

Address: Operational Base(0x27D00C00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_post Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_post Panel display scanning horizontal active end point.

POST0_CTRL_POST_SCL_FACTOR_YRGB

Address: Operational Base(0x27D00C00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	post_vs_factor Factor=((src_height[31:16])/(dst_height[31:16]))*2^12
15:0	RW	0x0000	post_hs_factor Factor=((src_width[15:0])/(dst_width[15:0]))*2^12

POST0_CTRL_POST_SCL_CTRL

Address: Operational Base(0x27D00C00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	sharpness_cheating_en 1'b0: Disable 1'b1: Enable
5	RW	0x0	post_empty_cheating_en 1'b0: Disable 1'b1: Enable
4	RW	0x1	post_vsd_dly_en 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1	RW	0x0	post_ver_sd_en 1'b0: Post ver scl down disable 1'b1: Post ver scl down enable
0	RW	0x0	post_hor_sd_en 1'b0: Post hor scl down disable 1'b1: Post hor scl down enable

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POST0_CTRL_POST_DSP_VACT_INFO_F1

Address: Operational Base(0x27D00C00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_post_f1 Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_post_f1 Panel display scanning horizontal active end point.

POST0_CTRL_POST_DSP_HTOTAL_HS_END

Address: Operational Base(0x27D00C00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0320	dsp_htotal Panel display scanning horizontal period.
15:13	RO	0x0	reserved
12:0	RW	0x00c8	dsp_hs_end Panel display scanning hsync pulse width.

POST0_CTRL_POST_DSP_HACT_ST_END

Address: Operational Base(0x27D00C00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0190	dsp_hact_st Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0258	dsp_hact_end Panel display scanning horizontal active end point.

POST0_CTRL_POST_DSP_VTOTAL_VS_END

Address: Operational Base(0x27D00C00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00fa	dsp_vtotal Panel display scanning vertical period.
15	RW	0x0	sw_dsp_vtotal_imd Dsp vtotal number valid immediately enable. 1'b0: Valid after frame start 1'b1: Valid immediately
14:13	RO	0x0	reserved
12:0	RW	0x000a	dsp_vs_end Panel display scanning vsync pulse width.

POST0_CTRL_POST_DSP_VACT_ST_END

Address: Operational Base(0x27D00C00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_vact_st Panel display scanning vertical active start point.
15:13	RO	0x0	reserved
12:0	RW	0x00fa	dsp_vact_end Panel display scanning vertical active end point.

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POST0_CTRL_POST_DSP_VS_ST_END_F1

Address: Operational Base(0x27D00C00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode).

POST0_CTRL_POST_DSP_VACT_ST_END_F1

Address: Operational Base(0x27D00C00) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode).

POST0_CTRL_POST_DITHER_FRC_0

Address: Operational Base(0x27D00C00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	sw_frc_bcb_pattern Bcb channel pattern choose 2'b0: DA1 2'b1: DA2 2'b2: DA3 2'b3: None
5:4	RW	0x0	sw_frc_gy_pattern Gy channel pattern choose 2'b0: DA1 2'b1: DA2 2'b2: DA3 2'b3: None
3:2	RW	0x0	sw_frc_rcr_pattern Rcr channel pattern choose 2'b0: DA1 2'b1: DA2 2'b2: DA3 2'b3: None
1:0	RW	0x0	sw_frc_dither_mode Frc2.0 dither mode sel. 2'b0: 10->8 2'b1: 10->10 2'b10: 8->10 2'b11: 8->8

POST0_CTRL_POST_DITHER_FRC_1

Address: Operational Base(0x27D00C00) + offset (0x00A4)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x100	sw_frc_gy_strength Gy channel dither strength
15:10	RO	0x00	reserved
9:0	RW	0x100	sw_frc_rcr_strength Rcr channel dither strength

POST0_CTRL_POST_DITHER_FRC_2

Address: Operational Base(0x27D00C00) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_range_sca Dither coef 8->8, 10->10: 0~1023 8->10: 0~4108 10->8: 0~1027
15:10	RO	0x00	reserved
9:0	RW	0x100	sw_frc_bcb_strength Bcb channel dither strength

POST0_CTRL_POST_ACM_CTRL

Address: Operational Base(0x27D00C00) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	acm_y2r_coe00 The coe00 of csc matrix.
15:11	RO	0x00	reserved
10:8	RW	0x0	acm_r2y_mode 3'b000: BT601L 3'b001: BT709L 3'b010: BT601F 3'b011: BT2020L
7:3	RO	0x00	reserved
2	RW	0x0	acm_r2y_en 1'b0: Disable 1'b1: Enable
1	RW	0x0	acm_y2r_en 1'b0: Disable 1'b1: Enable
0	RW	0x1	acm_bypass_en 1'b0: Disable acm bypass 1'b1: Enable acm bypass

POST0_CTRL_POST_ACM_Y2R_COE0102

Address: Operational Base(0x27D00C00) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	acm_y2r_coe02 The coe02 of csc matrix.
15:0	RW	0x0000	acm_y2r_coe01 The coe01 of csc matrix.

POST0_CTRL_POST_ACM_Y2R_COE1011

Address: Operational Base(0x27D00C00) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	acm_y2r_coe11 The coe11 of csc matrix.

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	acm_y2r_coe10 The coe10 of csc matrix.

POST0_CTRL_POST_ACM_Y2R_COE1220

Address: Operational Base(0x27D00C00) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	acm_y2r_coe20 The coe20 of csc matrix.
15:0	RW	0x0000	acm_y2r_coe12 The coe12 of csc matrix.

POST0_CTRL_POST_ACM_Y2R_COE2122

Address: Operational Base(0x27D00C00) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	acm_y2r_coe22 The coe22 of csc matrix.
15:0	RW	0x0000	acm_y2r_coe21 The coe21 of csc matrix.

POST0_CTRL_POST_ACM_Y2R_OFFSET0

Address: Operational Base(0x27D00C00) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	acm_y2r_offset0 The offset0 of csc matrix.

POST0_CTRL_POST_ACM_Y2R_OFFSET1

Address: Operational Base(0x27D00C00) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	acm_y2r_offset1 The offset1 of csc matrix.

POST0_CTRL_POST_ACM_Y2R_OFFSET2

Address: Operational Base(0x27D00C00) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	acm_y2r_offset2 The offset2 of csc matrix.

POST0_CTRL_POST_CLK_CNT

Address: Operational Base(0x27D00C00) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	calc_aclk_cnt the count number of aclk, when the count number of hclk is 5000.
15	RW	0x0	calc_clk_en 1'b0: Disable 1'b1: Enable
14:0	RO	0x0000	calc_dclk_cnt The count number of dclk, when the count number of hclk is 5000.

11.5.3.7 POST1_CTRL

POST1_CTRL_POST_DSP_CTRL

Address: Operational Base(0x27D00D00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x1	vop_standby_en_imd Writing 1 to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame.The output would be blank.When writing 0 to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable *Black display is recommended before setting standby mode enable.
30	RW	0x0	vop_fp_standby_en_imd Writing 1 to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame.The output would be blank.When writing 0 to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable *Black display is recommended before setting standby mode enable.
29	RO	0x0	reserved
28	RW	0x0	dsp_lut_en 1'b0: Disable 1'b1: Enable *This bit should be 0 when CPU updates the LUT, and should be 1 when Display LUT mode enable.
27	RW	0x0	dsp_black_en When this bit enable, the pixel data output is all black(0x000000).
26	RW	0x0	dsp_out_zero 1'b0: Normal output 1'b1: All output '0'
25	RO	0x0	reserved
24	RW	0x0	dsp_blank_en When this bit enable, the Hsync/Vsync/Den output is blank.
23	RO	0x0	reserved
22	RW	0x0	gamma_update_en 1'b0: Disable 1'b1: Enable
21	RO	0x0	reserved
20	RW	0x0	dither_down_mode 1'b0: RGB888 to RGB565 1'b1: RGB888 to RGB666
19:18	RW	0x0	dither_down_sel 2'b0: ALG 2'b1: FRC2.0
17	RW	0x0	dither_down_en 1'b0: Disable 1'b1: Enable
16	RW	0x0	pre_dither_down_en 10bit->8bit (allegro).
15	RW	0x0	dsp_out_rgb_yuv 1'b0: RGB={0x0,0x0,0x0} 1'b1: YUV={0x80,0x0,0x0}
14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	dsp_x_mir_en Post dsp x mirror. 1'b0: Disable 1'b1: Enable
12	RW	0x0	dsp_dummy_swap 1'b0: B+G+R+dummy 1'b1: Dummy+B+G+R
11	RW	0x0	dsp_delta_swap 1'b0: Disable 1'b1: Enable *See detail description in Delta display charpter
10	RW	0x0	dsp_rg_swap 1'b0: RGB 1'b1: GRB
9	RW	0x0	dsp_rb_swap 1'b0: RGB 1'b1: BGR
8	RW	0x0	dsp_bg_swap 1'b0: RGB 1'b1: RBG
7	RW	0x0	dsp_interlace 1'b0: Disable 1'b1: Enable
6	RW	0x0	dsp_filed_pol 1'b0: Normal 1'b1: Invert
5	RW	0x0	dsp_p2i_en Enable p2i. 1'b0: Disable 1'b1: Enable
4	RO	0x0	reserved
3:0	RW	0xf	dsp_out_mode 4'b0000: Parallel 24-bit output{R[7:0],2'b0,G[7:0],2'b0,B[7:0],2'b0} 4'b0001: Parallel 18-bit RGB666 output{R[5:0],4'b0,G[5:0],4'b0,B[5:0],4'b0} 4'b0010: Parallel 16-bit RGB565 output{R[4:0],5'b0,G[5:0],4'b0,B[4:0],5'b0} 4'h1000: MCU 24-bit serial 3*8 4'h1010: MCU 16-bit serial 2*8 4'b1100: DP/EDP YUV422 4'b1101: HDMI YUV422 4'b1110: DP/HDMI YUV420 4'b1111: Parallel 30-bit RGBaaa output{R[9:0],G[9:0],B[9:0]} Others: Reserved

POST1_CTRL_POST_MIPI_CTRL

Address: Operational Base(0x27D00D00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	edpi_wms_fs Frame start in hold mode. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
30	RW	0x0	edpi_wms_hold_en Enable hold mode. 1'b0: Disable 1'b1: Enable
29	RW	0x0	edpi_te_mode 1'b0: New frame is started by te. 1'b1: New frame is started by te and wms_fs.
28	RW	0x0	edpi_te_en Enable MIPI TE. 1'b0: Disable 1'b1: Enable
27:24	RW	0x0	doub_channel_overlap_num 4'h0: Overlap num 0 4'h1: Overlap num 2 4'h2: Overlap num 4 4'h3: Overlap num 6 4'h4: Overlap num 8 4'h5: Overlap num 10 4'h6: Overlap num 12 4'h7: Overlap num 14 4'h8: Overlap num 16
23:22	RO	0x0	reserved
21	RW	0x0	doub_channel_swap Swap two channel data of MIPI.
20	RW	0x0	doub_channel_en Enable mipi double channel. 1'b0: Disable 1'b1: Enable
19:0	RO	0x00000	reserved

POST1_CTRL_POST_COLOR_CTRL

Address: Operational Base(0x27D00D00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x0	sw_urgency_thh When post_lb > sw_urgency_thh, post set urgency to 1 ‘b0. Realse the priority of the layer on the AXI0 bus.
19:16	RW	0x0	sw_urgency_thl When post_lb < sw_urgency_thl, post set urgency to 1 ‘b1. Increase the priority of the layer on the AXI0 bus.
15:9	RO	0x00	reserved
8	RW	0x0	sw_urgency_en 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5:4	RW	0x0	io_vsync_sel 2'b00: 1'b1 2'b01: Line_flag0 2'b10: Line_flag1 2'b11: Vsync
3:2	RO	0x0	reserved
1	RW	0x0	color_bar_mode Select color bar mode. 1'b0: Horizontal mode 1'b1: Vertical mode

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Bit	Attr	Reset Value	Description
0	RW	0x0	color_bar_en Enable color bar. 1'b0: Disable 1'b1: Enable

POST1_CTRL_POST_CORE_CLK

Address: Operational Base(0x27D00D00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	dclk_out_sel 1'b0: Dclk 1'b1: Dclk_div2
1	RO	0x0	reserved
0	RW	0x0	dclk_core_sel 1'b0: Dclk 1'b1: Dclk_div2

POST1_CTRL_POST_DSP_BG

Address: Operational Base(0x27D00D00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x1	bg_display_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	dsp_bg_red 10bit red color of background.
19:10	RW	0x000	dsp_bg_blue 10bit blue color of background.
9:0	RW	0x000	dsp_bg_green 10bit green color of background.

POST1_CTRL_POST_PRE_SCAN_HTIMING

Address: Operational Base(0x27D00D00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	pre_scan_hactive Pre_scan horizontal active pixel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	pre_scan_hblank Pre_scan horizontal blank pixel.

POST1_CTRL_POST_DSP_HACT_INFO

Address: Operational Base(0x27D00D00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_hact_st_post Panel display scanning horizontal active start point
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hact_end_post Panel display scanning horizontal active end point

POST1_CTRL_POST_DSP_VACT_INFO

Address: Operational Base(0x27D00D00) + offset (0x0038)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_post Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_post Panel display scanning horizontal active end point.

POST1_CTRL_POST_SCL_FACTOR_YRGB

Address: Operational Base(0x27D00D00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	post_vs_factor Factor=((src_height[31:16])/(dst_height[31:16]))*2^12
15:0	RW	0x0000	post_hs_factor Factor=((src_width[15:0])/(dst_width[15:0]))*2^12

POST1_CTRL_POST_SCL_CTRL

Address: Operational Base(0x27D00D00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	post_empty_cheating_en 1'b0: Disable 1'b1: Enable
4	RW	0x1	post_vsd_dly_en 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1	RW	0x0	post_ver_sd_en 1'b0: Post ver scl down disable 1'b1: Post ver scl down enable
0	RW	0x0	post_hor_sd_en 1'b0: Post hor scl down disable 1'b1: Post hor scl down enable

POST1_CTRL_POST_DSP_VACT_INFO_F1

Address: Operational Base(0x27D00D00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_post_f1 Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_post_f1 Panel display scanning horizontal active end point.

POST1_CTRL_POST_DSP_HTOTAL_HS_END

Address: Operational Base(0x27D00D00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0320	dsp_htotal Panel display scanning horizontal period.
15:13	RO	0x0	reserved
12:0	RW	0x00c8	dsp_hs_end Panel display scanning hsync pulse width.

POST1_CTRL_POST_DSP_HACT_ST_END

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Address: Operational Base(0x27D00D00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0190	dsp_hact_st Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0258	dsp_hact_end Panel display scanning horizontal active end point.

POST1_CTRL_POST_DSP_VTOTAL_VS_END

Address: Operational Base(0x27D00D00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00fa	dsp_vtotal Panel display scanning vertical period.
15	RW	0x0	sw_dsp_vtotal_imd Dsp vtotal number valid immediately enable. 1'b0: Valid after frame start 1'b1: Valid immediately
14:13	RO	0x0	reserved
12:0	RW	0x000a	dsp_vs_end Panel display scanning vsync pulse width.

POST1_CTRL_POST_DSP_VACT_ST_END

Address: Operational Base(0x27D00D00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_vact_st Panel display scanning vertical active start point.
15:13	RO	0x0	reserved
12:0	RW	0x00fa	dsp_vact_end Panel display scanning vertical active end point.

POST1_CTRL_POST_DSP_VS_ST_END_F1

Address: Operational Base(0x27D00D00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode).

POST1_CTRL_POST_DSP_VACT_ST_END_F1

Address: Operational Base(0x27D00D00) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode).

POST1_CTRL_POST_BCSH_CTRL

Address: Operational Base(0x27D00D00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	bcsh_r2y_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
5	RO	0x0	reserved
4	RW	0x0	bcsh_r2y_en 1'b0: Bypass 1'b1: Enable
3:2	RW	0x0	bcsh_y2r_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RO	0x0	reserved
0	RW	0x0	bcsh_y2r_en 1'b0: Bypass 1'b1: Enable

POST1_CTRL_POST_BCSH_BCS

Address: Operational Base(0x27D00D00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	out_mode 2'b00: Black 2'b01: Blue 2'b10: Color bar 2'b11: Normal video
29:20	RW	0x000	sat_con Saturation*Contrast*256: {0,1.992*1.992}.
19:17	RO	0x0	reserved
16:8	RW	0x000	contrast Contrast*256: {0,1.992}.
7:0	RW	0x00	brightness Brightness: {-32,31}.

POST1_CTRL_POST_BCSH_H

Address: Operational Base(0x27D00D00) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	cos_hue Cos hue value.
15:9	RO	0x00	reserved
8:0	RW	0x000	sin_hue Sin hue value.

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POST1_CTRL_POST_BCSH_COLOR_BAR

Address: Operational Base(0x27D00D00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31	RW	0x0	bcsh_en 1'b0: Bcsh bypass 1'b1: Bcsh enable
30	RO	0x0	reserved
29:20	RW	0x000	color_bar_v V component value of BCSH color bar.
19:10	RW	0x000	color_bar_u U component value of BCSH color bar.
9:0	RW	0x000	color_bar_y Y component value of BCSH color bar.

POST1_CTRL_POST_DITHER_FRC_0

Address: Operational Base(0x27D00D00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	sw_frc_bcb_pattern Bcb channel pattern choose. 2'b00: DA1 2'b01: DA2 2'b10: DA3 2'b11: None
5:4	RW	0x0	sw_frc_gy_pattern Gy channel pattern choose 2'b00: DA1 2'b01: DA2 2'b10: DA3 2'b11: None
3:2	RW	0x0	sw_frc_rcr_pattern Rcr channel pattern choose 2'b00: DA1 2'b01: DA2 2'b10: DA3 2'b11: None
1:0	RW	0x0	sw_frc_dither_mode Frc2.0 dither mode sel 2'b00: 10->8 2'b01: 10->10 2'b10: 8->10 2'b11: 8->8

POST1_CTRL_POST_DITHER_FRC_1

Address: Operational Base(0x27D00D00) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x100	sw_frc_gy_strength Gy channel dither strength.
15:10	RO	0x00	reserved
9:0	RW	0x100	sw_frc_rcr_strength Rcr channel dither strength.

POST1_CTRL_POST_DITHER_FRC_2

Address: Operational Base(0x27D00D00) + offset (0x00A8)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_range_sca Dither coef 8->8, 10->10: 0~1023 8->10: 0~4108 10->8: 0~1027
15:10	RO	0x00	reserved
9:0	RW	0x100	sw_frc_bcb_strength Bcb channel dither strength

POST1_CTRL_POST_CLK_CNT

Address: Operational Base(0x27D00D00) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	calc_aclk_cnt The count number of aclk, when the count number of hclk is 5000.
15	RW	0x0	calc_clk_en 1'b0: Disable 1'b1: Enable
14:0	RO	0x0000	calc_dclk_cnt The count number of dclk, when the count number of hclk is 5000.

POST1_CTRL_POST_MCU_CTRL

Address: Operational Base(0x27D00D00) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31	RW	0x0	mcu_type_en MCU LCD output SELECT
30	RW	0x0	mcu_bypass_en MCU LCD BYPASS MODE Select
29	RW	0x0	mcu_rs MCU LCD RS Select 1'b0: Command 1'b1: Data
28	RW	0x0	mcu_frm_st Write1: MCU HOLD Mode Frame Start Read: MCU/LCDC standby HOLD status
27	RW	0x0	mcu_hold_mode MCU HOLD Mode Select
26	RO	0x0	reserved
25:20	RW	0x07	mcu_rw_pend MCU_RW signal end point (0-63)
19:16	RW	0x1	mcu_rw_pst MCU_RW signal start point (0-15)
15:10	RW	0x07	mcu_cs_pend MCU_CS signal end point (0-63)
9:6	RW	0x0	mcu_cs_pst MCU_CS signal start point (0-15)
5:0	RW	0x08	mcu_pix_total MCU LCD Interface writing period (1-63)

POST1_CTRL_POST_MCU_RW_BYPASS

Address: Operational Base(0x27D00D00) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:0	WO	0x000000	mcu_bypass_wdata MCU write bypass data

11.5.3.8 POST2_CTRL

POST2_CTRL_POST_DSP_CTRL

Address: Operational Base(0x27D00E00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x1	vop_standby_en_imd Writing 1 to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame.The output would be blank.When writing 0 to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable *Black display is recommended before setting standby mode enable.
30	RW	0x0	vop_fp_standby_en_imd Writing 1 to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame.The output would be blank.When writing 0 to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable *Black display is recommended before setting standby mode enable.
29	RO	0x0	reserved
28	RW	0x0	dsp_lut_en 1'b0: Disable 1'b1: Enable *This bit should be 0 when CPU updates the LUT, and should be 1 when Display LUT mode enable.
27	RW	0x0	dsp_black_en When this bit enable, the pixel data output is all black(0x000000).
26	RW	0x0	dsp_out_zero 1'b0: Normal output 1'b1: All output '0'
25	RO	0x0	reserved
24	RW	0x0	dsp_blank_en When this bit enable, the Hsync/Vsync/Den output is blank.
23	RW	0x0	post_lb_mode 1'b0: 4x4096 1'b1: 8x2048 If post_act_width > 2048 post_lb_mode =0else config 0 or 1
22	RW	0x0	gamma_update_en 1'b0: Disable 1'b1: Enable
21	RO	0x0	reserved
20	RW	0x0	dither_down_mode 1'b0: RGB888 to RGB565 1'b1: RGB888 to RGB666

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Bit	Attr	Reset Value	Description
19:18	RW	0x0	dither_down_sel 2'b0: ALG 2'b1: FRC
17	RW	0x0	dither_down_en 1'b0: Disable 1'b1: Enable
16	RO	0x0	reserved
15	RW	0x0	dsp_out_rgb_yuv 1'b0: RGB={0x0,0x0,0x0} 1'b1: YUV={0x80,0x0,0x0}
14	RO	0x0	reserved
13	RW	0x0	dsp_x_mir_en Post dsp x mirror. 1'b0: Disable 1'b1: Enable
12	RW	0x0	dsp_dummy_swap 1'b0: B+G+R+dummy 1'b1: Dummy+B+G+R
11	RW	0x0	dsp_delta_swap 1'b0: Disable 1'b1: Enable *See detail description in Delta display charpter
10	RW	0x0	dsp_rg_swap 1'b0: RGB 1'b1: GRB
9	RW	0x0	dsp_rb_swap 1'b0: RGB 1'b1: BGR
8	RW	0x0	dsp_bg_swap 1'b0: RGB 1'b1: RBG
7	RW	0x0	dsp_interlace 1'b0: Disable 1'b1: Enable
6	RW	0x0	dsp_filed_pol 1'b0: Normal 1'b1: Invert
5	RW	0x0	dsp_p2i_en Enable p2i. 1'b0: Disable 1'b1: Enable
4	RO	0x0	reserved
3:0	RW	0xf	dsp_out_mode 4'b0000: Parallel 24-bit output{R[7:0],2'b0,G[7:0],2'b0,B[7:0],2'b0} 4'b0001: Parallel 18-bit RGB666 output{R[5:0],4'b0,G[5:0],4'b0,B[5:0],4'b0} 4'b0010: Parallel 16-bit RGB565 output{R[4:0],5'b0,G[5:0],4'b0,B[4:0],5'b0} 4'h1000: MCU 24-bit serial 3*8 4'h1010: MCU 16-bit serial 2*8 4'b1100: DP YUV422 4'b1101: HDMI YUV422 4'b1110: DP/HDMI YUV420 Others: Reserved

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POST2_CTRL_POST_MIPI_CTRL

Address: Operational Base(0x27D00E00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	edpi_wms_fs Frame start in hold mode. 1'b0: Disable 1'b1: Enable
30	RW	0x0	edpi_wms_hold_en Enable hold mode. 1'b0: Disable 1'b1: Enable
29	RW	0x0	edpi_te_mode 1'b0: New frame is started by te. 1'b1: New frame is started by te and wms_fs.
28	RW	0x0	edpi_te_en Enable MIPI TE. 1'b0: Disable 1'b1: Enable
27:24	RW	0x0	doub_channel_overlap_num 4'h0: Overlap num 0 4'h1: Overlap num 2 4'h2: Overlap num 4 4'h3: Overlap num 6 4'h4: Overlap num 8 4'h5: Overlap num 10 4'h6: Overlap num 12 4'h7: Overlap num 14 4'h8: Overlap num 16
23:22	RO	0x0	reserved
21	RW	0x0	doub_channel_swap Swap two channel data of MIPI.
20	RW	0x0	doub_channel_en Enable mipi double channel. 1'b0: Disable 1'b1: Enable
19:0	RO	0x00000	reserved

POST2_CTRL_POST_COLOR_CTRL

Address: Operational Base(0x27D00E00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x0	sw_urgency_thh When post_lb > sw_urgency_thh, post set urgency to 1 ‘b0. Realse the priority of the layer on the AXI0 bus.
19:16	RW	0x0	sw_urgency_thl When post_lb < sw_urgency_thl, post set urgency to 1 ‘b1. Increase the priority of the layer on the AXI0 bus.
15:9	RO	0x00	reserved
8	RW	0x0	sw_urgency_en 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	io_vsync_sel 2'b00: 1'b1 2'b01: Line_flag0 2'b10: Line_flag1 2'b11: Vsync
3:2	RO	0x0	reserved
1	RW	0x0	color_bar_mode Select color bar mode. 1'b0: Horizontal mode 1'b1: Vertical mode
0	RW	0x0	color_bar_en Enable color bar. 1'b0: Disable 1'b1: Enable

POST2_CTRL_POST_CORE_CLK

Address: Operational Base(0x27D00E00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	dclk_out_sel 1'b0: Dclk 1'b1 :Dclk_div2
1	RO	0x0	reserved
0	RW	0x0	dclk_core_sel 1'b0: Dclk 1'b1: Dclk_div2

POST2_CTRL_POST_DSP_BG

Address: Operational Base(0x27D00E00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x1	bg_display_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	dsp_bg_red 10bit red color of background.
19:10	RW	0x000	dsp_bg_blue 10bit blue color of background.
9:0	RW	0x000	dsp_bg_green 10bit green color of background.

POST2_CTRL_POST_PRE_SCAN_HTIMING

Address: Operational Base(0x27D00E00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	pre_scan_hactive Pre_scan horizontal active pixel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	pre_scan_hblank Pre_scan horizontal blank pixel.

POST2_CTRL_POST_DSP_HACT_INFO

Address: Operational Base(0x27D00E00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:16	RW	0x0000	dsp_hact_st_post Panel display scanning horizontal active start point
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hact_end_post Panel display scanning horizontal active end point

POST2_CTRL_POST_DSP_VACT_INFO

Address: Operational Base(0x27D00E00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_post Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_post Panel display scanning horizontal active end point.

POST2_CTRL_POST_SCL_FACTOR_YRGB

Address: Operational Base(0x27D00E00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	post_vs_factor Factor=((src_height[31:16])/(dst_height[31:16]))*2^12
15:0	RW	0x0000	post_hs_factor Factor=((src_width[15:0])/(dst_width[15:0]))*2^12

POST2_CTRL_POST_SCL_CTRL

Address: Operational Base(0x27D00E00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	post_empty_cheating_en 1'b0: Disable 1'b1: Enable
4	RW	0x1	post_vsd_dly_en 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1	RW	0x0	post_ver_sd_en 1'b0: Post ver scl down disable 1'b1: Post ver scl down enable
0	RW	0x0	post_hor_sd_en 1'b0: Post hor scl down disable 1'b1: Post hor scl down enable

POST2_CTRL_POST_DSP_VACT_INFO_F1

Address: Operational Base(0x27D00E00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_post_f1 Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_post_f1 Panel display scanning horizontal active end point.

POST2_CTRL_POST_DSP_HTOTAL_HS_END

Address: Operational Base(0x27D00E00) + offset (0x0048)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0320	dsp_htotal Panel display scanning horizontal period.
15:13	RO	0x0	reserved
12:0	RW	0x00c8	dsp_hs_end Panel display scanning hsync pulse width.

POST2_CTRL_POST_DSP_HACT_ST_END

Address: Operational Base(0x27D00E00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0190	dsp_hact_st Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0258	dsp_hact_end Panel display scanning horizontal active end point.

POST2_CTRL_POST_DSP_VTOTAL_VS_END

Address: Operational Base(0x27D00E00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00fa	dsp_vtotal Panel display scanning vertical period.
15	RW	0x0	sw_dsp_vtotal_imd Dsp vtotal number valid immediately enable. 1'b0: Valid after frame start 1'b1: Valid immediately
14:13	RO	0x0	reserved
12:0	RW	0x000a	dsp_vs_end Panel display scanning vsync pulse width.

POST2_CTRL_POST_DSP_VACT_ST_END

Address: Operational Base(0x27D00E00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_vact_st Panel display scanning vertical active start point.
15:13	RO	0x0	reserved
12:0	RW	0x00fa	dsp_vact_end Panel display scanning vertical active end point.

POST2_CTRL_POST_DSP_VS_ST_END_F1

Address: Operational Base(0x27D00E00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode).

POST2_CTRL_POST_DSP_VACT_ST_END_F1

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Address: Operational Base(0x27D00E00) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode).

POST2_CTRL_POST_BCSH_CTRL

Address: Operational Base(0x27D00E00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	bcsh_r2y_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
5	RO	0x0	reserved
4	RW	0x0	bcsh_r2y_en 1'b0: Bypass 1'b1: Enable
3:2	RW	0x0	bcsh_y2r_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RO	0x0	reserved
0	RW	0x0	bcsh_y2r_en 1'b0: Bypass 1'b1: Enable

POST2_CTRL_POST_BCSH_BCS

Address: Operational Base(0x27D00E00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	out_mode 2'b00: Black 2'b01: Blue 2'b10: Color bar 2'b11: Normal video
29:20	RW	0x000	sat_con Saturation*Contrast*256: {0,1.992*1.992}.
19:17	RO	0x0	reserved
16:8	RW	0x000	contrast Contrast*256: {0,1.992}.
7:0	RW	0x00	brightness Brightness: {-32,31}.

POST2_CTRL_POST_BCSH_H

Address: Operational Base(0x27D00E00) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24:16	RW	0x000	cos_hue Cos hue value.
15:9	RO	0x00	reserved
8:0	RW	0x000	sin_hue Sin hue value.

POST2_CTRL_POST_BCSH_COLOR_BAR

Address: Operational Base(0x27D00E00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31	RW	0x0	bcsh_en 1'b0: Bcsh bypass 1'b1: Bcsh enable
30	RO	0x0	reserved
29:20	RW	0x000	color_bar_v V component value of BCSH color bar.
19:10	RW	0x000	color_bar_u U component value of BCSH color bar.
9:0	RW	0x000	color_bar_y Y component value of BCSH color bar.

POST2_CTRL_POST_FRC_LOWER01_0

Address: Operational Base(0x27D00E00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x1284	lower01_frm1 FRC parameter lowerbit = 2'b01,frm1.
15:0	RW	0x4821	lower01_frm0 FRC parameter lowerbit = 2'b01,frm0.

POST2_CTRL_POST_FRC_LOWER01_1

Address: Operational Base(0x27D00E00) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x2148	lower01_frm3 FRC parameter lowerbit = 2'b01,frm3.
15:0	RW	0x8412	lower01_frm2 FRC parameter lowerbit = 2'b01,frm2.

POST2_CTRL_POST_FRC_LOWER10_0

Address: Operational Base(0x27D00E00) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RW	0xa55a	lower10_frm1 FRC parameter lowerbit = 2'b10,frm1.
15:0	RW	0x9696	lower10_frm0 FRC parameter lowerbit = 2'b10,frm0.

POST2_CTRL_POST_FRC_LOWER10_1

Address: Operational Base(0x27D00E00) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x5aa5	lower10_frm3 FRC parameter lowerbit = 2'b10,frm3.
15:0	RW	0x6969	lower10_frm2 FRC parameter lowerbit = 2'b10,frm2.

POST2_CTRL_POST_FRC_LOWER11_0

Address: Operational Base(0x27D00E00) + offset (0x00B0)

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Bit	Attr	Reset Value	Description
31:16	RW	0xdeb7	lower11_frm1 FRC parameter lowerbit = 2'b11,frm1.
15:0	RW	0x7bed	lower11_frm0 FRC parameter lowerbit = 2'b11,frm0.

POST2_CTRL_POST_FRC_LOWER11_1

Address: Operational Base(0x27D00E00) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RW	0xed7b	lower11_frm3 FRC parameter lowerbit = 2'b11,frm3.
15:0	RW	0xb7de	lower11_frm2 FRC parameter lowerbit = 2'b11,frm2.

POST2_CTRL_POST_CLK_CNT

Address: Operational Base(0x27D00E00) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	calc_aclk_cnt the count number of aclk, when the count number of hclk is 5000.
15	RW	0x0	calc_clk_en 1'b0: Disable 1'b1: Enable
14:0	RO	0x0000	calc_dclk_cnt the count number of dclk, when the count number of hclk is 5000.

POST2_CTRL_POST_MCU_CTRL

Address: Operational Base(0x27D00E00) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31	RW	0x0	mcu_type_en MCU LCD output SELECT
30	RW	0x0	mcu_bypass_en MCU LCD BYPASS MODE Select
29	RW	0x0	mcu_rs MCU LCD RS Select 1'b0: Command 1'b1: Data
28	RW	0x0	mcu_frm_st Write1: MCU HOLD Mode Frame Start Read: MCU/LCDC standby HOLD status
27	RW	0x0	mcu_hold_mode MCU HOLD Mode Select
26	RO	0x0	reserved
25:20	RW	0x07	mcu_rw_pend MCU_RW signal end point (0-63)
19:16	RW	0x1	mcu_rw_pst MCU_RW signal start point (0-15)
15:10	RW	0x07	mcu_cs_pend MCU_CS signal end point (0-63)
9:6	RW	0x0	mcu_cs_pst MCU_CS signal start point (0-15)
5:0	RW	0x08	mcu_pix_total MCU LCD Interface writing period (1-63)

POST2_CTRL_POST_MCU_RW_BYPASS

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Address: Operational Base(0x27D00E00) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	WO	0x000000	mcu_bypass_wdata MCU write bypass data

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CLUSTER0_WIN0_CTRL0

Address: Operational Base(0x27D01000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	win0_csc_out_path_sel When enable the bit. layer out data sel yuv2rgb path. 1'b0: Disable out data normal. 1'b1: Enable out data sel yuv2rgb path.
23:22	RO	0x0	reserved
21	RW	0x0	win0_y_mir 1'b0: Disable 1'b1: Enable
20	RO	0x0	reserved
19	RW	0x0	win0_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
18	RW	0x0	win0_dither_up_en 1'b0: Disable 1'b1: Enable
17	RW	0x0	win0_uv_swap 1'b0: {Y,U,V} 1'b1: {Y,V,U}
16	RW	0x0	win0_rg_swap Swap R and G component. 1'b0: RGB 1'b1: GRB
15	RW	0x0	win0_alpha_swap 1'b0: {A,R,G,B} 1'b1: {R,G,B,A}
14	RW	0x0	win0_rb_swap 1'b0: RGB 1'b1: BGR
13	RO	0x0	reserved
12:10	RW	0x0	win0_csc_mode Color space conversion: 3'b000: BT601_L 3'b001: BT709_L 3'b010: BT601_F 3'b011: BT2020 3'b100: BT709_L_13(Y2R) 3'b101: BT709_F_13(Y2R)) 3'b110: BT2020_L_13(Y2R) 3'b111: BT2020_F_13(Y2R)
9	RW	0x0	win0_csc_r2y_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
8	RW	0x0	win0_csc_y2r_en 1'b0: Disable 1'b1: Enable
7	RW	0x0	win0_tile_mode_sel Tile4x4_mode sel: 1'b0: Tile4x4 format sel mode1 1'b1: None
6:1	RW	0x00	win0_data_fmt 6'b00000: ARGB888 6'b00001: RGB888 6'b00_0010: RGB565 6'b00_0011: RGBA1010102 6'b00_0100: YCbCr420 6'b00_0101: YCbCr422 6'b00_0110: YCbCr444 6'b00_0111: YCbCr400 6'b01_0100: YCbCr420_101010 6'b01_0101: YCbCr422_101010 6'b01_0110: YCbCr444_101010 6'b01_0111: YCbCr400_101010 6'b00_1100: Tile4x4_YCbCr420 6'b00_1101: Tile4x4_YCbCr422 6'b00_1110: Tile4x4_YCbCr444 6'b00_1111: Tile4x4_YCbCr400 6'b01_1100: Tile4x4_YCbCr420_101010 6'b01_1101: Tile4x4_YCbCr422_101010 6'b01_1110: Tile4x4_YCbCr444_101010 6'b01_1111: Tile4x4_YCbCr400_101010 Others: Reserved
0	RW	0x0	win0_en 1'b0: Disable 1'b1: Enable

CLUSTER0_WIN0_CTRL1

Address: Operational Base(0x27D01000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_cbcr_vsd_gt4 1'b0: Disable 1'b1: Enable
30	RW	0x0	win0_cbcr_vsd_gt2 1'b0: Disable 1'b1: Enable
29	RW	0x0	win0_yrgb_vsd_gt4 1'b0: Disable 1'b1: Enable
28	RW	0x0	win0_yrgb_vsd_gt2 1'b0: Disable 1'b1: Enable
27	RW	0x0	win0_xavg_en 1'b0: Disable 1'b1: Enable
26:25	RW	0x0	win0_xgt_mode 2'bx0: Xgt2 or Xavg2 2'bx1: Xgt4 or Xavg4

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Bit	Attr	Reset Value	Description
24	RW	0x0	win0_xgt_en 1'b0: Disable 1'b1: Enable
23	RW	0x0	win0_xsd_en Xscale down enable 1'b0: Disable 1'b1: Enable
22	RW	0x0	win0_xsu_en Xscale up enable 1'b0: Disable 1'b1: Enable
21:20	RW	0x0	win0_xscl_mode 2'b00: Best-neigh 2'b01: Bilinear 2'b11: Multi-phase filter Others: Reserved
19	RW	0x0	win0_vsd_avg4 1'b0: Disable 1'b1: Enable
18	RW	0x0	win0_vsd_avg2 1'b0: Disable 1'b1: Enable
17:16	RO	0x0	reserved
15	RW	0x0	win0_ysd_en Yscale down enable. 1'b0: Disable 1'b1: Enable
14	RW	0x0	win0_ysu_en Yscale up enable. 1'b0: Disable 1'b1: Enable
13:12	RW	0x0	win0_yscl_mode 2'b00: Best-neigh 2'b01: Bilinear 2'b11: Multi-phase filter Others: Reserved
11:8	RW	0x0	win0_cbcr_gather_num 4'b0000: Gather2 4'b0001: Gather4 4'b0010: Gather8 4'b0011: Gather16 Others: Reserved
7:4	RW	0x0	win0_yrgb_gather_num 4'b0000: Gather2 4'b0001: Gather4 4'b0010: Gather8 4'b0011: Gather16 Others: Reserved
3:1	RO	0x0	reserved
0	RW	0x0	win0_yrgb_axi_gather_en Win0 axi bus yrgb data gather transfer enable. 1'b0: Disable 1'b1: Enable

CLUSTER0_WIN0_CTRL2

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Address: Operational Base(0x27D01000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:5	RW	0x03	win0_rid_cbr AXI read id of win0 cbr channel.
4:0	RW	0x02	win0_rid_yrgb AXI read id of win0 yrgb channel.

CLUSTER0_WIN0_YRGB_MST

Address: Operational Base(0x27D01000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_yrgb_mst Win0 YRGB frame buffer memory start address.

CLUSTER0_WIN0_CBCR_MST

Address: Operational Base(0x27D01000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_cbcr_mst Win0 CBCR frame buffer memory start address.

CLUSTER0_WIN0_VIR

Address: Operational Base(0x27D01000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	win0_vir_stride Number of words of win0 yrgb virtual width. ARGB888: Win0_vir_width RGB888: (Win0_vir_width*3/4) + (Win0_vir_width%3) RGB565: Ceil(win0_vir_width/2) YUV: Ceil(win0_vir_width/4) YUV tile: Ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win0_vir_width/4)

CLUSTER0_WIN0_KEY_COLOR

Address: Operational Base(0x27D01000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	win0_key_color_en 1'b0: Disable 1'b1: Enable
29:20	RW	0x000	win0_key_color_ry when pic_data is RGB: check pic_data_r[9:2] and win0_key_color_ry[7:0]. when pic_data is YUV: check pic_data_y[9:0] and win0_key_color_ry[9:0].
19:10	RW	0x000	win0_key_color_gu when pic_data is RGB: check pic_data_g[9:2] and win0_key_color_gu[7:0]. when pic_data is YUV: check pic_data_u[9:0] and win0_key_color_gu[9:0].
9:0	RW	0x000	win0_key_color_bv when pic_data is RGB: check pic_data_b[9:2] and win0_key_color_bv[7:0]. when pic_data is YUV: check pic_data_v[9:0] and win0_key_color_bv[9:0].

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CLUSTER0_WIN0_ACT_INFO

Address: Operational Base(0x27D01000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win0_act_height Win_act_height = win0 vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	win0_act_width Win_act_width = win0 horizontal size - 1

CLUSTER0_WIN0_DSP_INFO

Address: Operational Base(0x27D01000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	win0_dsp_height Win0_dsp_height = win0 vertical size - 1.
15:12	RO	0x0	reserved
11:0	RW	0x000	win0_dsp_width Win0_dsp_width = win0 horizontal size - 1.

CLUSTER0_WIN0_DSP_ST

Address: Operational Base(0x27D01000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win0_dsp_yst Win0 vertical start point(y) of the display region.
15:13	RO	0x0	reserved
12:0	RW	0x0000	win0_dsp_xst Win0 horizontal start point(x) of the display region.

CLUSTER0_WIN0_DSP_BG

Address: Operational Base(0x27D01000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	win0_dsp_bg_red Win0 layer background red color.
19:10	RW	0x000	win0_dsp_bg_green Win0 layer background green color.
9:0	RW	0x000	win0_dsp_bg_blue Win0 layer background blue color.

CLUSTER0_WIN0_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_vs_factor_yrgb Factor=((LCDC_WIN0_ACT_INFO[31:16]) / (LCDC_WIN0_DSP_INFO[31:16]))*2^12
15:0	RW	0x0000	win0_hs_factor_yrgb Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12

CLUSTER0_WIN0_SCL_OFFSET

Address: Operational Base(0x27D01000) + offset (0x0038)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	win0_vs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.
15:8	RO	0x00	reserved
7:0	RW	0x00	win0_hs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.

CLUSTER0_WIN0_TRANSFORMED_OFFSET

Address: Operational Base(0x27D01000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	transformed_yoffset The y_offset between the first acitve pixel and the first pixel of column.
15:4	RO	0x000	reserved
3:0	RW	0x0	transformed_xoffset The x_offset between the first acitve pixel and the first pixel of line.

CLUSTER0_WIN0_ZME_CTRL

Address: Operational Base(0x27D01000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_zme_gating_en 1'b0: Disable 1'b1: Enable
30:4	RO	0x0000000	reserved
3	RW	0x0	win0_zme_dering_en 1'b0: Disable 1'b1: Enable
2:0	RO	0x0	reserved

CLUSTER0_WIN0_ZME_DERING_PARA

Address: Operational Base(0x27D01000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x04	win0_dering_sen1 Dering sen1 parameter.
23:21	RO	0x0	reserved
20:16	RW	0x10	win0_dering_sen0 Dering sen0 parameter.
15:13	RO	0x0	reserved
12:8	RW	0x0c	win0_dering_beta Dering beta parameter.
7:5	RO	0x0	reserved
4:0	RW	0x10	win0_dering_alpha Dering alpha parameter.

CLUSTER0_WIN0_FBCD_OUTPUT_CTRL

Address: Operational Base(0x27D01000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x1	win0_fbcd_gating_en Win0 fbcd gating enable. 1'b0: Disable 1'b1: Enable
3:0	RO	0x0	reserved

CLUSTER0_WIN0_FBCD_MODE

Address: Operational Base(0x27D01000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	win0_ymir_en 1'b0: Ymirror disable 1'b1: Ymirror when fbcd output
2	RW	0x0	win0_xmir_en 1'b0: Xmirror disable 1'b1: Xmirror when fbcd output
1:0	RO	0x0	reserved

CLUSTER0_WIN0_FBCD_HDR_PTR

Address: Operational Base(0x27D01000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_fbcd_hdr_ptr FBCD encode stream starting address in DDR.

CLUSTER0_WIN0_FBCD_VIR_WIDTH

Address: Operational Base(0x27D01000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_fbcd_tail_num Header/payload arbiter tail number. Full mode: (act_width+63)/64 Half mode: (act_width+31)/32
15:0	RW	0x0000	win0_fbcd_pic_vir_width It must be aligned to afbcd_mode. Full mode: (rfbcd_vir_width+63)/64*16 Half mode: (afbcd_vir_width+31)/32*16

CLUSTER0_WIN0_FBCD_SIZE

Address: Operational Base(0x27D01000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_fbcd_pic_height Fbcd_act_height.
15:0	RW	0x0000	win0_fbcd_pic_width Fbcd_act_width.

CLUSTER0_WIN0_FBCD_PIC_OFFSET

Address: Operational Base(0x27D01000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_fbcd_pic_yoffset Display image vertical offset in DDR.
15:0	RW	0x0000	win0_fbcd_pic_xoffset Display image horizon offset in DDR.

CLUSTER0_WIN0_FBCD_DIS_OFFSET

Address: Operational Base(0x27D01000) + offset (0x0068)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_fbcd_dis_yoffset Display image vertical offset in panel. it can be random.
15:0	RW	0x0000	win0_fbcd_dis_xoffset Display image horizon offset in panel. it can be random.

CLUSTER0_WIN0_FBCD_CTRL

Address: Operational Base(0x27D01000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	win0_fbcd_pld_range_en 1'b0: Disable 1'b1: Enable
16	RW	0x0	win0_fbcd_pld_offset_en 1'b0: Disable 1'b1: Enable
15:13	RO	0x0	reserved
12	RW	0x0	win0_fbcd_bg_swap_en Win0 fbcd mode bg swap enable.
11	RW	0x0	win0_fbcd_alpha_swap_en Win0 fbcd mode alpha swap enable.
10	RW	0x0	win0_fbcd_uv_swap_en Win0 afbcd mode uv swap enable.
9	RW	0x0	win0_fbcd_rb_swap_en Win0 fbcd mode rb swap enable.
8	RW	0x0	win0_fbcd_block_split 1'b0: Disable 1'b1: Enable
7	RW	0x0	win0_fbcd_half_block 1'b0: Fbcd full mode, 4 line one tail line 1'b1: Fbcd half mode, 8 line one tail line
6:2	RW	0x00	win0_fbcd_pixel_packing_fmt FBCD data format. 4'h0: RGB565 4'h2: RGBA1010102/YUV444_10B 4'h3: YUV420_101010 4'h4: RGB888/YUV444 4'h5: RGBA8888 4'h9: YUV420_888 4'hb: YUV422_888 4'he: YUV422_101010 Others: Reserved [4]: Color transform 1'b0: Disable 1'b1: Enable
1:0	RO	0x0	reserved

CLUSTER0_WIN0_PLD_PTR_OFFSET

Address: Operational Base(0x27D01000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_pld_ptr_offset

CLUSTER0_WIN0_PLD_PTR_RANGE

Address: Operational Base(0x27D01000) + offset (0x007C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_pld_ptr_range

CLUSTER0_WIN1_CTRL0

Address: Operational Base(0x27D01000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	win1_csc_out_path_sel When enable the bit. layer out data sel yuv2rgb path. 1'b0: Disable out data normal. 1'b1: Enable out data sel yuv2rgb path.
23:21	RO	0x0	reserved
20	RW	0x0	win1_y_mir 1'b0: Disable 1'b1: Enable
19	RW	0x0	win1_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
18	RW	0x0	win1_dither_up_en 1'b0: Disable 1'b1: Enable
17	RW	0x0	win1_uv_swap 1'b0: {Y,U,V} 1'b1: {Y,V,U}
16	RW	0x0	win1_rg_swap Swap R and G component. 1'b0: RGB 1'b1: GRB
15	RW	0x0	win1_alpha_swap 1'b0: {A,R,G,B} 1'b1: {R,G,B,A}
14	RW	0x0	win1_rb_swap 1'b0: RGB 1'b1: BGR
13:12	RO	0x0	reserved
11:10	RW	0x0	win1_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
9	RW	0x0	win1_csc_r2y_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	win1_csc_y2r_en 1'b0: Disable 1'b1: Enable
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:1	RW	0x00	win1_data_fmt 6'b00000: ARGB888 6'b00001: RGB888 6'b00_0010: RGB565 6'b00_0011: RGBA1010102 6'b00_0100: YCbCr420 6'b00_0101: YCbCr422 6'b00_0110: YCbCr444 6'b00_0111: YCbCr400 6'b01_0100: YCbCr420_101010 6'b01_0101: YCbCr422_101010 6'b01_0110: YCbCr444_101010 6'b01_0111: YCbCr400_101010 6'b00_1100: Tile4x4_YCbCr420 6'b00_1101: Tile4x4_YCbCr422 6'b00_1110: Tile4x4_YCbCr444 6'b00_1111: Tile4x4_YCbCr400 6'b01_1100: Tile4x4_YCbCr420_101010 6'b01_1101: Tile4x4_YCbCr422_101010 6'b01_1110: Tile4x4_YCbCr444_101010 6'b01_1111: Tile4x4_YCbCr400_101010 Others: Reserved
0	RW	0x0	win1_en 1'b0: Disable 1'b1: Enable

CLUSTER0_WIN1_CTRL1

Address: Operational Base(0x27D01000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_cbcr_vsd_gt4 1'b0: Disable 1'b1: Enable
30	RW	0x0	win1_cbcr_vsd_gt2 1'b0: Disable 1'b1: Enable
29	RW	0x0	win1_yrgb_vsd_gt4 1'b0: Disable 1'b1: Enable
28	RW	0x0	win1_yrgb_vsd_gt2 1'b0: Disable 1'b1: Enable
27	RW	0x0	win1_xavg_en 1'b0: Disable 1'b1: Enable
26:25	RW	0x0	win1_xgt_mode 2'bx0: Xgt2 or Xavg2 2'bx1: Xgt4 or Xavg4
24	RW	0x0	win1_xgt_en 1'b0: Disable 1'b1: Enable
23	RW	0x0	win1_xsd_en Xscale down enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
22	RW	0x0	win1_xsu_en Xscale up enable 1'b0: Disable 1'b1: Enable
21:20	RW	0x0	win1_xscl_mode 2'b00: Best-neigh 2'b01: Bilinear 2'b11: Multi-phase filter Others: Reserved
19	RW	0x0	win1_vsd_avg4 1'b0: Disable 1'b1: Enable
18	RW	0x0	win1_vsd_avg2 1'b0: Disable 1'b1: Enable
17:16	RO	0x0	reserved
15	RW	0x0	win1_ysd_en Yscale down enable 1'b0: Disable 1'b1: Enable
14	RW	0x0	win1_ysu_en Yscale up enable 1'b0: Disable 1'b1: Enable
13:12	RW	0x0	win1_yscl_mode 2'b00: Best-neigh 2'b01: Bilinear 2'b11: Multi-phase filter Others: Reserved
11:8	RW	0x0	win1_cbcr_gather_num 4'b0000: Gather2 4'b0001: Gather4 4'b0010: Gather8 4'b0011: Gather16 Others: Reserved
7:4	RW	0x0	win1_yrgb_gather_num 4'b0000: Gather2 4'b0001: Gather4 4'b0010: Gather8 4'b0011: Gather16 Others: Reserved
3:1	RO	0x0	reserved
0	RW	0x0	win1_yrgb_axi_gather_en Win1 axi bus yrgb data gather transfer enable.

CLUSTER0_WIN1_CTRL2

Address: Operational Base(0x27D01000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:5	RW	0x05	win1_rid_cbr AXI read id of win1 cbr channel.
4:0	RW	0x04	win1_rid_yrgb AXI read id of win1 yrgb channel.

CLUSTER0_WIN1_YRGB_MST

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Address: Operational Base(0x27D01000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_yrgb_mst WIN1 YRGB frame buffer memory start address.

CLUSTER0_WIN1_CBCR_MST

Address: Operational Base(0x27D01000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_cbcr_mst WIN1 CBCR frame buffer memory start address.

CLUSTER0_WIN1_VIR

Address: Operational Base(0x27D01000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	win1_vir_stride Number of words of win1 yrgb virtual width. ARGB888: Win1_vir_width RGB888: (Win1_vir_width*3/4) + (Win1_vir_width%3) RGB565: ceil(Win1_vir_width/2) YUV: ceil(Win1_vir_width/4) YUV tile: ceil(Win1_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(Win1_vir_width/4)

CLUSTER0_WIN1_KEY_COLOR

Address: Operational Base(0x27D01000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	win1_key_color_en 1'b0: Disable 1'b1: Enable
29:20	RW	0x000	win1_key_color_ry when pic_data is RGB: check pic_data_r[9:2] and win0_key_color_ry[7:0]. when pic_data is YUV: check pic_data_y[9:0] and win0_key_color_ry[9:0].
19:10	RW	0x000	win1_key_color_gu when pic_data is RGB: check pic_data_g[9:2] and win0_key_color_gu[7:0]. when pic_data is YUV: check pic_data_u[9:0] and win0_key_color_gu[9:0].
9:0	RW	0x000	win1_key_color_bv when pic_data is RGB: check pic_data_b[9:2] and win0_key_color_bv[7:0]. when pic_data is YUV: check pic_data_v[9:0] and win0_key_color_bv[9:0].

CLUSTER0_WIN1_ACT_INFO

Address: Operational Base(0x27D01000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win1_act_height Win_act_height = win1 vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	win1_act_width Win_act_width = win1 horizontal size - 1

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CLUSTER0_WIN1_DSP_INFO

Address: Operational Base(0x27D01000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	win1_dsp_height Win1_dsp_height = win1 vertical size - 1
15:12	RO	0x0	reserved
11:0	RW	0x000	win1_dsp_width Win1_dsp_width = win1 horizontal size - 1

CLUSTER0_WIN1_DSP_ST

Address: Operational Base(0x27D01000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win1_dsp_yst Win1 vertical start point(y) of the display region.
15:13	RO	0x0	reserved
12:0	RW	0x0000	win1_dsp_xst Win1 horizontal start point(x) of the display region.

CLUSTER0_WIN1_DSP_BG

Address: Operational Base(0x27D01000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	win1_dsp_bg_red Win1 layer background red color.
19:10	RW	0x000	win1_dsp_bg_green Win1 layer background green color.
9:0	RW	0x000	win1_dsp_bg_blue Win1 layer background blue color.

CLUSTER0_WIN1_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_vs_factor_yrgb Factor=((LCDC_win1_ACT_INFO[31:16]) / (LCDC_win1_DSP_INFO[31:16]))*2^12
15:0	RW	0x0000	win1_hs_factor_yrgb Factor=((LCDC_win1_ACT_INFO[15:0]) / (LCDC_win1_DSP_INFO[15:0]))*2^12

CLUSTER0_WIN1_SCL_OFFSET

Address: Operational Base(0x27D01000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	win1_vs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.
15:8	RO	0x00	reserved
7:0	RW	0x00	win1_hs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.

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CLUSTER0_WIN1_TRANSFORMED_OFFSET

Address: Operational Base(0x27D01000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	transformed_yoffset The y_offset between the first acitve pixel and the first pixel of column.
15:4	RO	0x000	reserved
3:0	RW	0x0	transformed_xoffset The x_offset between the first acitve pixel and the first pixel of line.

CLUSTER0_WIN1_ZME_CTRL

Address: Operational Base(0x27D01000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_zme_gating_en 1'b0: Disable 1'b1: Enable
30:4	RO	0x0000000	reserved
3	RW	0x0	win1_zme_dering_en 1'b0: Disable 1'b1: Enable
2:0	RO	0x0	reserved

CLUSTER0_WIN1_ZME_DERING_PARA

Address: Operational Base(0x27D01000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	win1_dering_sen1 Dering sen1 parameter.
23:21	RO	0x0	reserved
20:16	RW	0x00	win1_dering_sen0 Dering sen0 parameter.
15:13	RO	0x0	reserved
12:8	RW	0x00	win1_dering_beta Dering beta parameter.
7:5	RO	0x0	reserved
4:0	RW	0x00	win1_dering_alpha Dering alpha parameter.

CLUSTER0_WIN1_FBCD_MASK_EN

Address: Operational Base(0x27D01000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x1	win1_fbcd_gating_en Win1 fbcd gating enable. 1'b0: Disable 1'b1: Enable
3:0	RO	0x0	reserved

CLUSTER0_WIN1_FBCD_MODE

Address: Operational Base(0x27D01000) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3	RW	0x0	win1_ymir_en 1'b0: Ymirror disable 1'b1: Ymirror when fbcd output
2	RW	0x0	win1_xmir_en 1'b0: Xmirror disable 1'b1: Xmirror when fbcd output
1:0	RO	0x0	reserved

CLUSTER0_WIN1_FBCD_HDR_PTR

Address: Operational Base(0x27D01000) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_fbcd_hdr_ptr FBCD encode stream starting address in DDR.

CLUSTER0_WIN1_FBCD_VIR_WIDTH

Address: Operational Base(0x27D01000) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_fbcd_tail_num Header/payload arbiter tail number. Full mode: (act_width+63)/64 Half mode: (act_width+31)/32
15:0	RW	0x0000	win1_fbcd_pic_vir_width It must be aligned to fbcd_mode. Full mode: (rfbcd_vir_width+63)/64*16 Half mode: (afbcd_vir_width+31)/32*16

CLUSTER0_WIN1_FBCD_SIZE

Address: Operational Base(0x27D01000) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_fbcd_pic_height Win1_fbcd_act_height.
15:0	RW	0x0000	win1_fbcd_pic_width Win1_fbcd_act_width.

CLUSTER0_WIN1_FBCD_PIC_OFFSET

Address: Operational Base(0x27D01000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_fbcd_pic_yoffset Display image vertical offset in DDR.
15:0	RW	0x0000	win1_fbcd_pic_xoffset Display image horizon offset in DDR.

CLUSTER0_WIN1_FBCD_DIS_OFFSET

Address: Operational Base(0x27D01000) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_fbcd_dis_yoffset Display image vertical offset in panel. it can be random.
15:0	RW	0x0000	win1_fbcd_dis_xoffset Display image horizon offset in panel. it can be random.

CLUSTER0_WIN1_FBCD_CTRL

Address: Operational Base(0x27D01000) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17	RW	0x0	win1_fbcd_pld_range_en 1'b0: Disable 1'b1: Enable
16	RW	0x0	win1_fbcd_pld_offset_en 1'b0: Disable 1'b1: Enable
15:11	RO	0x00	reserved
10	RW	0x0	win1_fbcd_uv_swap_en Win1 fbcd mode uv swap enable.
9	RW	0x0	win1_fbcd_rb_swap_en Win1 fbcd mode rb swap enable.
8	RW	0x0	win1_fbcd_block_split 1'b0: Disable 1'b1: Enable
7	RW	0x0	win1_fbcd_half_block 1'b0: Fbcd full mode, 4 line one tail line 1'b1: Fbcd half mode, 8 line one tail line
6:2	RW	0x00	win1_fbcd_pixel_packing_fmt FBCD data format. 4'h0: RGB565 4'h2: RGBA1010102/YUV444_10B 4'h3: YUV420_101010 4'h4: RGB888/YUV444 4'h5: RGBA8888 4'h9: YUV420_888 4'hb: YUV422_888 4'he: YUV422_101010 Others: Reserved [4]: Color transform 1'b0: Disable 1'b1: Enable
1:0	RO	0x0	reserved

CLUSTER0_WIN1_PLD_PTR_OFFSET

Address: Operational Base(0x27D01000) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_pld_ptr_offset

CLUSTER0_WIN1_PLD_PTR_RANGE

Address: Operational Base(0x27D01000) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_pld_ptr_range

CLUSTER0_CLUSTER_CTRL

Address: Operational Base(0x27D01000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RW	0x1	cluster_frm_resetn_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29	RW	0x1	clusrer_dma_stride_4k 1'b0: Enable 1'b1: Disable

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Bit	Attr	Reset Value	Description
28	RW	0x0	cluster_fbcd_overlap_en Nxt pld data save to lb. 1'b0: Disable 1'b1: Enable
27	RW	0x0	cluster_pld_dma_priority_en 1'b0: Disable 1'b1: Enable
26:19	RO	0x00	reserved
18:17	RW	0x0	cluster_dma_hurry_thold 2'b00: Ready_buff_cnt <= total_buff*3/4 2'b01: Ready_buff_cnt <= total_buff/2 2'b10: Ready_buff_cnt <= total_buff/4 2'b11: Ready_buff_cnt <= total_buff/8
16	RW	0x0	cluster_dma_hurry_en 1'b0: Disable hurry_en 1'b1: Enable hurry_en
15	RO	0x0	reserved
14	RW	0x0	cluster_mmu_bypass 1'b0: Disable 1'b1: Enable
13	RO	0x0	reserved
12	RW	0x0	cluster_dma_stop Cluster dma stop enable. 1'b0: Disable 1'b1: Enable
11:6	RO	0x00	reserved
5:4	RW	0x0	cluster_lb_mode CLUSTER line buffer mode, calculated by driver. 2'b00: One window, max width is 4096 2'b01: Two window, max width is 2048
3:2	RO	0x0	reserved
1	RW	0x0	cluster_fbcd_en 1'b0: Win0 and Win1 fbcd disable 1'b1: Win0 and Win1 fbcd enable
0	RW	0x0	cluster_en 1'b0: Disable 1'b1: Enable

CLUSTER0_DCI_BLK_SIZE

Address: Operational Base(0x27D01000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	blk_size_v DCI block size v.
15:9	RO	0x00	reserved
8:0	RW	0x000	blk_size_h DCI block size h.

CLUSTER0_DCI_BLK_OFFSET

Address: Operational Base(0x27D01000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	blk_offset_v DCI block offset v.
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8:0	RW	0x000	blk_offset_h DCI block offset h.

CLUSTER0_DCI_PIX_REGION

Address: Operational Base(0x27D01000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:26	RW	0x00	pix_region_start_v DCI pixel region start v.
25	RO	0x0	reserved
24:20	RW	0x00	pix_region_start_h DCI pixel region start h.
19:0	RW	0x00000	blk_size_fix The fixed point of block size reciprocal.

CLUSTER0_DCI_LUMA_SAT_ADJ_0

Address: Operational Base(0x27D01000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sat_adj_thr When luma greater than this threshold, the sat_w will be set to constant.
15:0	RW	0x0000	sat_adj_zero Luma at which to start chroma adjust, the sat_w will be set to zero.

CLUSTER0_DCI_LUMA_SAT_ADJ_1

Address: Operational Base(0x27D01000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x00	sat_w The weight value for the opeartions of addition and multiplication chroma adjust action.
15:0	RW	0x0000	sat_adj_k The slope of 1 / (luma_sat_adj_thr - luma_sat_adj_zero) with fixed point.

CLUSTER0_DCI_CTRL

Address: Operational Base(0x27D01000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	dma_rlen LUT AXI read brust. 2'b00: Burst16 2'b01: Burst8 2'b1x: Burst4
11:8	RO	0x0	reserved
7:4	RW	0x3	dma_rid DCI DMA RID.
3	RO	0x0	reserved
2	RW	0x0	csc_range Indicate DCI source CSC range. 1'b0: Limited 1'b1: Full

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Bit	Attr	Reset Value	Description
1	RW	0x0	uv_adjust_en CB / Cr adjust enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	dci_en DCI enable. 1'b0: Disable 1'b1: Enable

CLUSTER0_DCI_LUT_MST

Address: Operational Base(0x27D01000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dci_dma_mst DCI LUT memory start address.

CLUSTER0_DCI_DBG_PIX

Address: Operational Base(0x27D01000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	dci_debug_pix DCI obvserve pixel value{2'b0, V, U, Y}

CLUSTER0_CLUSTER_PORT_SEL_IMD

Address: Operational Base(0x27D01000) + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	cluster_port_sel 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved

CLUSTER0_CLUSTER_DLY_NUM

Address: Operational Base(0x27D01000) + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x17	win1_dly_num Win1 delay ack cycle.
7:0	RW	0x17	win0_dly_num Win0 delay ack cycle.

11.5.3.10 CLUSTER1

CLUSTER1_WIN0_CTRL0

Address: Operational Base(0x27D01200) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	win0_csc_out_path_sel When enable the bit. layer out data sel yuv2rgb path. 1'b0: Disable out data normal. 1'b1: Enable out data sel yuv2rgb path.
23:22	RO	0x0	reserved
21	RW	0x0	win0_y_mir 1'b0: Disable 1'b1: Enable
20	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
19	RW	0x0	win0_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
18	RW	0x0	win0_dither_up_en 1'b0: Disable 1'b1: Enable
17	RW	0x0	win0_uv_swap 1'b0: {Y,U,V} 1'b1: {Y,V,U}
16	RW	0x0	win0_rg_swap Swap R and G component. 1'b0: RGB 1'b1: GRB
15	RW	0x0	win0_alpha_swap 1'b0: {A,R,G,B} 1'b1: {R,G,B,A}
14	RW	0x0	win0_rb_swap 1'b0: RGB 1'b1: BGR
13	RO	0x0	reserved
12:10	RW	0x0	win0_csc_mode Color space conversion: 3'b000: BT601_L 3'b001: BT709_L 3'b010: BT601_F 3'b011: BT2020 3'b100: BT709_L_13(Y2R) 3'b101: BT709_F_13(Y2R)) 3'b110: BT2020_L_13(Y2R) 3'b111: BT2020_F_13(Y2R)
9	RW	0x0	win0_csc_r2y_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	win0_csc_y2r_en 1'b0: Disable 1'b1: Enable
7	RW	0x0	win0_tile_mode_sel Tile4x4_mode sel: 1'b0: Tile4x4 format sel mode1 1'b1: None

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Bit	Attr	Reset Value	Description
6:1	RW	0x00	win0_data_fmt 6'b00000: ARGB888 6'b00001: RGB888 6'b00_0010: RGB565 6'b00_0011: RGBA1010102 6'b00_0100: YCbCr420 6'b00_0101: YCbCr422 6'b00_0110: YCbCr444 6'b00_0111: YCbCr400 6'b01_0100: YCbCr420_101010 6'b01_0101: YCbCr422_101010 6'b01_0110: YCbCr444_101010 6'b01_0111: YCbCr400_101010 6'b00_1100: Tile4x4_YCbCr420 6'b00_1101: Tile4x4_YCbCr422 6'b00_1110: Tile4x4_YCbCr444 6'b00_1111: Tile4x4_YCbCr400 6'b01_1100: Tile4x4_YCbCr420_101010 6'b01_1101: Tile4x4_YCbCr422_101010 6'b01_1110: Tile4x4_YCbCr444_101010 6'b01_1111: Tile4x4_YCbCr400_101010 Others: Reserved
0	RW	0x0	win0_en 1'b0: Disable 1'b1: Enable

CLUSTER1_WIN0_CTRL1

Address: Operational Base(0x27D01200) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_cbcr_vsd_gt4 1'b0: Disable 1'b1: Enable
30	RW	0x0	win0_cbcr_vsd_gt2 1'b0: Disable 1'b1: Enable
29	RW	0x0	win0_yrgb_vsd_gt4 1'b0: Disable 1'b1: Enable
28	RW	0x0	win0_yrgb_vsd_gt2 1'b0: Disable 1'b1: Enable
27	RW	0x0	win0_xavg_en 1'b0: Disable 1'b1: Enable
26:25	RW	0x0	win0_xgt_mode 2'bx0 : Xgt2 or Xavg2 2'bx1 : Xgt4 or Xavg4
24	RW	0x0	win0_xgt_en 1'b0: Disable 1'b1: Enable
23	RW	0x0	win0_xsd_en Xscale down enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
22	RW	0x0	win0_xsu_en Xscale up enable 1'b0: Disable 1'b1: Enable
21:20	RW	0x0	win0_xscl_mode 2'b00: Best-neigh 2'b01: Bilinear 2'b11: Multi-phase filter Others: Reserved
19	RW	0x0	win0_vsd_avg4 1'b0: Disable 1'b1: Enable
18	RW	0x0	win0_vsd_avg2 1'b0: Disable 1'b1: Enable
17:16	RO	0x0	reserved
15	RW	0x0	win0_ysd_en Yscale down enable 1'b0: Disable 1'b1: Enable
14	RW	0x0	win0_ysu_en Yscale up enable 1'b0: Disable 1'b1: Enable
13:12	RW	0x0	win0_yscl_mode 2'b00: Best-neigh 2'b01: Bilinear 2'b11: Multi-phase filter Others: Reserved
11:8	RW	0x0	win0_cbcr_gather_num 4'b0000: Gather2 4'b0001: Gather4 4'b0010: Gather8 4'b0011: Gather16 Others: Reserved
7:4	RW	0x0	win0_yrgb_gather_num 4'b0000: Gather2 4'b0001: Gather4 4'b0010: Gather8 4'b0011: Gather16 Others: Reserved
3:1	RO	0x0	reserved
0	RW	0x0	win0_yrgb_axi_gather_en Win0 axi bus yrgb data gather transfer enable. 1'b0: Disable 1'b1: Enable

CLUSTER1_WIN0_CTRL2

Address: Operational Base(0x27D01200) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:5	RW	0x07	win0_rid_cbr AXI read id of win0 cbr channel.
4:0	RW	0x06	win0_rid_yrgb AXI read id of win0 yrgb channel.

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CLUSTER1_WIN0_YRGB_MST

Address: Operational Base(0x27D01200) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_yrgb_mst Win0 YRGB frame buffer memory start address.

CLUSTER1_WIN0_CBCR_MST

Address: Operational Base(0x27D01200) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_cbcr_mst Win0 CBCR frame buffer memory start address.

CLUSTER1_WIN0_VIR

Address: Operational Base(0x27D01200) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	win0_vir_stride Number of words of win0 yrgb virtual width. ARGB888: Win0_vir_width RGB888: (Win0_vir_width*3/4) + (Win0_vir_width%3) RGB565: Ceil(win0_vir_width/2) YUV: Ceil(win0_vir_width/4) YUV tile: Ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win0_vir_width/4)

CLUSTER1_WIN0_KEY_COLOR

Address: Operational Base(0x27D01200) + offset (0x001C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	win0_key_color_en 1'b0: Disable 1'b1: Enable
29:20	RW	0x000	win0_key_color_ry when pic_data is RGB: check pic_data_r[9:2] and win0_key_color_ry[7:0]. when pic_data is YUV: check pic_data_y[9:0] and win0_key_color_ry[9:0].
19:10	RW	0x000	win0_key_color_gu when pic_data is RGB: check pic_data_g[9:2] and win0_key_color_gu[7:0]. when pic_data is YUV: check pic_data_u[9:0] and win0_key_color_gu[9:0].
9:0	RW	0x000	win0_key_color_bv when pic_data is RGB: check pic_data_b[9:2] and win0_key_color_bv[7:0]. when pic_data is YUV: check pic_data_v[9:0] and win0_key_color_bv[9:0].

CLUSTER1_WIN0_ACT_INFO

Address: Operational Base(0x27D01200) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win0_act_height Win_act_height = win0 vertical size - 1
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	win0_act_width Win_act_width = win0 horizontal size - 1

CLUSTER1_WIN0_DSP_INFO

Address: Operational Base(0x27D01200) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	win0_dsp_height Win0_dsp_height = win0 vertical size - 1
15:12	RO	0x0	reserved
11:0	RW	0x000	win0_dsp_width Win0_dsp_width = win0 horizontal size - 1

CLUSTER1_WIN0_DSP_ST

Address: Operational Base(0x27D01200) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win0_dsp_yst Win0 vertical start point(y) of the display region.
15:13	RO	0x0	reserved
12:0	RW	0x0000	win0_dsp_xst Win0 horizontal start point(x) of the display region.

CLUSTER1_WIN0_DSP_BG

Address: Operational Base(0x27D01200) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	win0_dsp_bg_red Win0 layer background red color.
19:10	RW	0x000	win0_dsp_bg_green Win0 layer background green color.
9:0	RW	0x000	win0_dsp_bg_blue Win0 layer background blue color.

CLUSTER1_WIN0_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01200) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_vs_factor_yrgb Factor=((LCDC_WIN0_ACT_INFO[31:16]) / (LCDC_WIN0_DSP_INFO[31:16]))*2^12
15:0	RW	0x0000	win0_hs_factor_yrgb Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12

CLUSTER1_WIN0_SCL_OFFSET

Address: Operational Base(0x27D01200) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	win0_vs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	win0_hs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.

CLUSTER1_WIN0_TRANSFORMED_OFFSET

Address: Operational Base(0x27D01200) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	transformed_yoffset The y_offset between the first acitve pixel and the first pixel of column.
15:4	RO	0x000	reserved
3:0	RW	0x0	transformed_xoffset The x_offset between the first acitve pixel and the first pixel of line.

CLUSTER1_WIN0_ZME_CTRL

Address: Operational Base(0x27D01200) + offset (0x0040)

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_zme_gating_en 1'b0: Disable 1'b1: Enable
30:4	RO	0x0000000	reserved
3	RW	0x0	win0_zme_dering_en 1'b0: Disable 1'b1: Enable
2:0	RO	0x0	reserved

CLUSTER1_WIN0_ZME_DERING_PARA

Address: Operational Base(0x27D01200) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x04	win0_dering_sen1 Dering sen1 parameter.
23:21	RO	0x0	reserved
20:16	RW	0x10	win0_dering_sen0 Dering sen0 parameter.
15:13	RO	0x0	reserved
12:8	RW	0x0c	win0_dering_beta Dering beta parameter.
7:5	RO	0x0	reserved
4:0	RW	0x10	win0_dering_alpha Dering alpha parameter.

CLUSTER1_WIN0_FBCD_OUTPUT_CTRL

Address: Operational Base(0x27D01200) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x1	win0_fbcd_gating_en Win0 fbcd gating enable. 1'b0: Disable 1'b1: Enable
3:0	RO	0x0	reserved

CLUSTER1_WIN0_FBCD_MODE

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Address: Operational Base(0x27D01200) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	win0_ymir_en 1'b0: Ymirror disable 1'b1: Ymirror when fbcd output
2	RW	0x0	win0_xmir_en 1'b0: Xmirror disable 1'b1: Xmirror when fbcd output
1:0	RO	0x0	reserved

CLUSTER1_WIN0_FBCD_HDR_PTR

Address: Operational Base(0x27D01200) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_fbcd_hdr_ptr FBCD encode stream starting address in DDR.

CLUSTER1_WIN0_FBCD_VIR_WIDTH

Address: Operational Base(0x27D01200) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_fbcd_tail_num Header/payload arbiter tail number. Full mode: (act_width+63)/64 Half mode: (act_width+31)/32
15:0	RW	0x0000	win0_fbcd_pic_vir_width It must be aligned to afbcd_mode. Full mode: (rfbcd_vir_width+63)/64*16 Half mode: (afbcd_vir_width+31)/32*16

CLUSTER1_WIN0_FBCD_SIZE

Address: Operational Base(0x27D01200) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_fbcd_pic_height Fbcd_act_height.
15:0	RW	0x0000	win0_fbcd_pic_width Fbcd_act_width.

CLUSTER1_WIN0_FBCD_PIC_OFFSET

Address: Operational Base(0x27D01200) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_fbcd_pic_yoffset Display image vertical offset in DDR.
15:0	RW	0x0000	win0_fbcd_pic_xoffset Display image horizon offset in DDR.

CLUSTER1_WIN0_FBCD_DIS_OFFSET

Address: Operational Base(0x27D01200) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_fbcd_dis_yoffset Display image vertical offset in panel. it can be random.
15:0	RW	0x0000	win0_fbcd_dis_xoffset Display image horizon offset in panel. it can be random.

CLUSTER1_WIN0_FBCD_CTRL

Address: Operational Base(0x27D01200) + offset (0x006C)

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Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	win0_fbcd_pld_range_en 1'b0: Disable 1'b1: Enable
16	RW	0x0	win0_fbcd_pld_offset_en 1'b0: Disable 1'b1: Enable
15:13	RO	0x0	reserved
12	RW	0x0	win0_fbcd_bg_swap_en Win0 fbcd mode bg swap enable.
11	RW	0x0	win0_fbcd_alpha_swap_en Win0 fbcd mode alpha swap enable.
10	RW	0x0	win0_fbcd_uv_swap_en Win0 fbcd mode uv swap enable.
9	RW	0x0	win0_fbcd_rb_swap_en Win0 fbcd mode rb swap enable.
8	RW	0x0	win0_fbcd_block_split 1'b0: Disable 1'b1: Enable
7	RW	0x0	win0_fbcd_half_block 1'b0: Fbcd full mode, 4 line one tail line 1'b1: Fbcd half mode, 8 line one tail line
6:2	RW	0x00	win0_fbcd_pixel_packing_fmt FBCD data format. 4'h0: RGB565 4'h2: RGBA1010102/YUV444_10B 4'h3: YUV420_101010 4'h4: RGB888/YUV444 4'h5: RGBA8888 4'h9: YUV420_888 4'hb: YUV422_888 4'he: YUV422_101010 Others: Reserved [4]: Color transform 1'b0: Disable 1'b1: Enable
1:0	RO	0x0	reserved

CLUSTER1_WIN0_PLD_PTR_OFFSET

Address: Operational Base(0x27D01200) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_pld_ptr_offset

CLUSTER1_WIN0_PLD_PTR_RANGE

Address: Operational Base(0x27D01200) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_pld_ptr_range

CLUSTER1_WIN1_CTRL0

Address: Operational Base(0x27D01200) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24	RW	0x0	win1_csc_out_path_sel When enable the bit. layer out data sel yuv2rgb path. 1'b0: Disable out data normal. 1'b1: Enable out data sel yuv2rgb path.
23:21	RO	0x0	reserved
20	RW	0x0	win1_y_mir 1'b0: Disable 1'b1: Enable
19	RW	0x0	win1_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
18	RW	0x0	win1_dither_up_en 1'b0: Disable 1'b1: Enable
17	RW	0x0	win1_uv_swap 1'b0: {Y,U,V} 1'b1: {Y,V,U}
16	RW	0x0	win1_rg_swap Swap R and G component. 1'b0: RGB 1'b1: GRB
15	RW	0x0	win1_alpha_swap 1'b0: {A,R,G,B} 1'b1: {R,G,B,A}
14	RW	0x0	win1_rb_swap 1'b0: RGB 1'b1: BGR
13:12	RO	0x0	reserved
11:10	RW	0x0	win1_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
9	RW	0x0	win1_csc_r2y_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	win1_csc_y2r_en 1'b0: Disable 1'b1: Enable
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:1	RW	0x00	win1_data_fmt 6'b00000: ARGB888 6'b00001: RGB888 6'b00_0010: RGB565 6'b00_0011: RGBA1010102 6'b00_0100: YCbCr420 6'b00_0101: YCbCr422 6'b00_0110: YCbCr444 6'b00_0111: YCbCr400 6'b01_0100: YCbCr420_101010 6'b01_0101: YCbCr422_101010 6'b01_0110: YCbCr444_101010 6'b01_0111: YCbCr400_101010 6'b00_1100: Tile4x4_YCbCr420 6'b00_1101: Tile4x4_YCbCr422 6'b00_1110: Tile4x4_YCbCr444 6'b00_1111: Tile4x4_YCbCr400 6'b01_1100: Tile4x4_YCbCr420_101010 6'b01_1101: Tile4x4_YCbCr422_101010 6'b01_1110: Tile4x4_YCbCr444_101010 6'b01_1111: Tile4x4_YCbCr400_101010 Others: Reserved
0	RW	0x0	win1_en 1'b0: Disable 1'b1: Enable

CLUSTER1_WIN1_CTRL1

Address: Operational Base(0x27D01200) + offset (0x0084)

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_cbcr_vsd_gt4 1'b0: Disable 1'b1: Enable
30	RW	0x0	win1_cbcr_vsd_gt2 1'b0: Disable 1'b1: Enable
29	RW	0x0	win1_yrgb_vsd_gt4 1'b0: Disable 1'b1: Enable
28	RW	0x0	win1_yrgb_vsd_gt2 1'b0: Disable 1'b1: Enable
27	RW	0x0	win1_xavg_en 1'b0: Disable 1'b1: Enable
26:25	RW	0x0	win1_xgt_mode 2'bx0: Xgt2 or Xavg2 2'bx1: Xgt4 or Xavg4
24	RW	0x0	win1_xgt_en 1'b0: Disable 1'b1: Enable
23	RW	0x0	win1_xsd_en Xscale down enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
22	RW	0x0	win1_xsu_en Xscale up enable 1'b0: Disable 1'b1: Enable
21:20	RW	0x0	win1_xscl_mode 2'b00: Best-neigh 2'b01: Bilinear 2'b11: Multi-phase filter Others: Reserved
19	RW	0x0	win1_vsd_avg4 1'b0: Disable 1'b1: Enable
18	RW	0x0	win1_vsd_avg2 1'b0: Disable 1'b1: Enable
17:16	RO	0x0	reserved
15	RW	0x0	win1_ysd_en Yscale down enable 1'b0: Disable 1'b1: Enable
14	RW	0x0	win1_ysu_en Yscale up enable 1'b0: Disable 1'b1: Enable
13:12	RW	0x0	win1_yscl_mode 2'b00: Best-neigh 2'b01: Bilinear 2'b11: Multi-phase filter Others: Reserved
11:8	RW	0x0	win1_cbcr_gather_num 4'b0000: Gather2 4'b0001: Gather4 4'b0010: Gather8 4'b0011: Gather16 Others: Reserved
7:4	RW	0x0	win1_yrgb_gather_num 4'b0000: Gather2 4'b0001: Gather4 4'b0010: Gather8 4'b0011: Gather16 Others: Reserved
3:1	RO	0x0	reserved
0	RW	0x0	win1_yrgb_axi_gather_en Win1 axi bus yrgb data gather transfer enable.

CLUSTER1_WIN1_CTRL2

Address: Operational Base(0x27D01200) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:5	RW	0x09	win1_rid_cbr AXI read id of win1 cbr channel.
4:0	RW	0x08	win1_rid_yrgb AXI read id of win1 yrgb channel.

CLUSTER1_WIN1_YRGB_MST

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Address: Operational Base(0x27D01200) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_yrgb_mst WIN1 YRGB frame buffer memory start address.

CLUSTER1_WIN1_CBCR_MST

Address: Operational Base(0x27D01200) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_cbcr_mst WIN1 CBCR frame buffer memory start address.

CLUSTER1_WIN1_VIR

Address: Operational Base(0x27D01200) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	win1_vir_stride Number of words of win1 yrgb virtual width. ARGB888: Win1_vir_width RGB888: (Win1_vir_width*3/4) + (Win1_vir_width%3) RGB565: ceil(Win1_vir_width/2) YUV: ceil(Win1_vir_width/4) YUV tile: ceil(Win1_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(Win1_vir_width/4)

CLUSTER1_WIN1_KEY_COLOR

Address: Operational Base(0x27D01200) + offset (0x009C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	win1_key_color_en 1'b0: Disable 1'b1: Enable
29:20	RW	0x000	win1_key_color_ry when pic_data is RGB: check pic_data_r[9:2] and win0_key_color_ry[7:0]. when pic_data is YUV: check pic_data_y[9:0] and win0_key_color_ry[9:0].
19:10	RW	0x000	win1_key_color_gu when pic_data is RGB: check pic_data_g[9:2] and win0_key_color_gu[7:0]. when pic_data is YUV: check pic_data_u[9:0] and win0_key_color_gu[9:0].
9:0	RW	0x000	win1_key_color_bv when pic_data is RGB: check pic_data_b[9:2] and win0_key_color_bv[7:0]. when pic_data is YUV: check pic_data_v[9:0] and win0_key_color_bv[9:0].

CLUSTER1_WIN1_ACT_INFO

Address: Operational Base(0x27D01200) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win1_act_height Win_act_height = win1 vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	win1_act_width Win_act_width = win1 horizontal size - 1

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CLUSTER1_WIN1_DSP_INFO

Address: Operational Base(0x27D01200) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	win1_dsp_height Win1_dsp_height = win1 vertical size - 1
15:12	RO	0x0	reserved
11:0	RW	0x000	win1_dsp_width Win1_dsp_width = win1 horizontal size - 1

CLUSTER1_WIN1_DSP_ST

Address: Operational Base(0x27D01200) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win1_dsp_yst Win1 vertical start point(y) of the display region.
15:13	RO	0x0	reserved
12:0	RW	0x0000	win1_dsp_xst Win1 horizontal start point(x) of the display region.

CLUSTER1_WIN1_DSP_BG

Address: Operational Base(0x27D01200) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	win1_dsp_bg_red Win1 layer background red color.
19:10	RW	0x000	win1_dsp_bg_green Win1 layer background green color.
9:0	RW	0x000	win1_dsp_bg_blue Win1 layer background blue color.

CLUSTER1_WIN1_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01200) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_vs_factor_yrgb Factor=((LCDC_win1_ACT_INFO[31:16]) / (LCDC_win1_DSP_INFO[31:16]))*2^12
15:0	RW	0x0000	win1_hs_factor_yrgb Factor=((LCDC_win1_ACT_INFO[15:0]) / (LCDC_win1_DSP_INFO[15:0]))*2^12

CLUSTER1_WIN1_SCL_OFFSET

Address: Operational Base(0x27D01200) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	win1_vs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.
15:8	RO	0x00	reserved
7:0	RW	0x00	win1_hs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.

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CLUSTER1_WIN1_TRANSFORMED_OFFSET

Address: Operational Base(0x27D01200) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	transformed_yoffset The y_offset between the first acitve pixel and the first pixel of column.
15:4	RO	0x000	reserved
3:0	RW	0x0	transformed_xoffset The x_offset between the first acitve pixel and the first pixel of line.

CLUSTER1_WIN1_ZME_CTRL

Address: Operational Base(0x27D01200) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_zme_gating_en 1'b0: Disable 1'b1: Enable
30:4	RO	0x0000000	reserved
3	RW	0x0	win1_zme_dering_en 1'b0: Disable 1'b1: Enable
2:0	RO	0x0	reserved

CLUSTER1_WIN1_ZME_DERING_PARA

Address: Operational Base(0x27D01200) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	win1_dering_sen1 Dering sen1 parameter.
23:21	RO	0x0	reserved
20:16	RW	0x00	win1_dering_sen0 Dering sen0 parameter.
15:13	RO	0x0	reserved
12:8	RW	0x00	win1_dering_beta Dering beta parameter.
7:5	RO	0x0	reserved
4:0	RW	0x00	win1_dering_alpha Dering alpha parameter.

CLUSTER1_WIN1_FBCD_MASK_EN

Address: Operational Base(0x27D01200) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x1	win1_fbcd_gating_en Win1 fbcd gating enable. 1'b0: Disable 1'b1: Enable
3:0	RO	0x0	reserved

CLUSTER1_WIN1_FBCD_MODE

Address: Operational Base(0x27D01200) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3	RW	0x0	win1_ymir_en 1'b0: Ymirror disable 1'b1: Ymirror when fbcd output
2	RW	0x0	win1_xmir_en 1'b0: Xmirror disable 1'b1: Xmirror when fbcd output
1:0	RO	0x0	reserved

CLUSTER1_WIN1_FBCD_HDR_PTR

Address: Operational Base(0x27D01200) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_fbcd_hdr_ptr FBCD encode stream starting address in DDR.

CLUSTER1_WIN1_FBCD_VIR_WIDTH

Address: Operational Base(0x27D01200) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_fbcd_tail_num Header/payload arbiter tail number. Full mode: (act_width+63)/64 Half mode: (act_width+31)/32
15:0	RW	0x0000	win1_fbcd_pic_vir_width It must be aligned to afbcd_mode. Full mode: (rfbcd_vir_width+63)/64*16 Half mode: (afbcd_vir_width+31)/32*16

CLUSTER1_WIN1_FBCD_SIZE

Address: Operational Base(0x27D01200) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_fbcd_pic_height Win1_fbcd_act_height.
15:0	RW	0x0000	win1_fbcd_pic_width Win1_fbcd_act_width.

CLUSTER1_WIN1_FBCD_PIC_OFFSET

Address: Operational Base(0x27D01200) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_fbcd_pic_yoffset Display image vertical offset in DDR.
15:0	RW	0x0000	win1_fbcd_pic_xoffset Display image horizon offset in DDR.

CLUSTER1_WIN1_FBCD_DIS_OFFSET

Address: Operational Base(0x27D01200) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_fbcd_dis_yoffset Display image vertical offset in panel. it can be random.
15:0	RW	0x0000	win1_fbcd_dis_xoffset Display image horizon offset in panel. it can be random.

CLUSTER1_WIN1_FBCD_CTRL

Address: Operational Base(0x27D01200) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17	RW	0x0	win1_fbcd_pld_range_en 1'b0: Disable 1'b1: Enable
16	RW	0x0	win1_fbcd_pld_offset_en 1'b0: Disable 1'b1: Enable
15:11	RO	0x00	reserved
10	RW	0x0	win1_fbcd_uv_swap_en Win1 fbcd mode uv swap enable
9	RW	0x0	win1_fbcd_rb_swap_en Win1 fbcd mode rb swap enable
8	RW	0x0	win1_fbcd_block_split 1'b0: Disable 1'b1: Enable
7	RW	0x0	win1_fbcd_half_block 1'b0: Fbcd full mode, 4 line one tail line 1'b1: Fbcd half mode, 8 line one tail line
6:2	RW	0x00	win1_fbcd_pixel_packing_fmt FBCD data format. 4'h0: RGB565 4'h2: RGBA1010102/YUV444_10B 4'h3: YUV420_101010 4'h4: RGB888/YUV444 4'h5: RGBA8888 4'h9: YUV420_888 4'hb: YUV422_888 4'he: YUV422_101010 Others: Reserved [4]: Color transform 1'b0: Disable 1'b1: Enable
1:0	RO	0x0	reserved

CLUSTER1_WIN1_PLD_PTR_OFFSET

Address: Operational Base(0x27D01200) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_pld_ptr_offset

CLUSTER1_WIN1_PLD_PTR_RANGE

Address: Operational Base(0x27D01200) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_pld_ptr_range

CLUSTER1_CLUSTER_CTRL

Address: Operational Base(0x27D01200) + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RW	0x1	cluster_frm_resetn_en 1'b0: Disable 1'b1: Enable
30:15	RO	0x0000	reserved
14	RW	0x0	cluster_mmu_bypass 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
13	RO	0x0	reserved
12	RW	0x0	cluster_dma_stop Cluster dma stop enable. 1'b0: Disable 1'b1: Enable
11:6	RO	0x00	reserved
5:4	RW	0x0	cluster_lb_mode CLUSTER line buffer mode, calculated by driver. 2'b00: One window, max width is 4096 2'b01: Two window, max width is 2048
3:2	RO	0x0	reserved
1	RW	0x0	cluster_fbcd_en 1'b0: Win0 and Win1 fbcd disable 1'b1: Win0 and Win1 fbcd enable
0	RW	0x0	cluster_en 1'b0: Disable 1'b1: Enable

CLUSTER1_CLUSTER_PORT_SEL_IMD

Address: Operational Base(0x27D01200) + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	cluster_port_sel 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved

CLUSTER1_CLUSTER_DLY_NUM

Address: Operational Base(0x27D01200) + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x17	win1_dly_num Win1 delay ack cycle.
7:0	RW	0x17	win0_dly_num Win0 delay ack cycle.

11.5.3.11 ESMART0

ESMART0_ESMART_CTRL0

Address: Operational Base(0x27D01800) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_frm_resetn_en 1'b0: Disable 1'b1: Enable
30:25	RO	0x00	reserved
24	RW	0x0	esmart_yuv2rgb_force_en When enable the bit. layer out data foce support yuv2rgb. 1'b0: Disable out data force data transform 1'b1: Enable out data force transform
23:17	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	esmart_y2r_csc_13bit_en Color space conversion: 1'b0: Disable 13bit Y2R 1'b1: When esmart_csc_mode = 2'b00, BT709_L_13(only support y2r) 1'b1: When esmart_csc_mode = 2'b01, BT709_F_13(only support y2r) 1'b1: When esmart_csc_mode = 2'b10, BT2020_L_13(only support y2r) 1'b1: When esmart_csc_mode = 2'b11, BT2020_F_13(only support y2r)
15:14	RO	0x0	reserved
13:12	RW	0x0	esmart_scl_num 2'b00: Scale engine0 2'b01: Scale engine1 2'b10: Scale engine2 2'b11: Scale engine3
11:10	RO	0x0	reserved
9	RW	0x0	esmart_endian_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte0,byte1,byte2,byte3}
8	RW	0x0	esmart_mid_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte3,byte1,byte2,byte0}
7:6	RO	0x0	reserved
5	RW	0x0	esmart_8bpp_alpha_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	esmart_8bpp_lut_en To enable 8bpp LUT.
3:2	RW	0x0	esmart_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	esmart_rgb2yuv_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	esmart_yuv2rgb_en 1'b0: Disable 1'b1: Enable

ESMART0_ESMART_CTRL1

Address: Operational Base(0x27D01800) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_ymir_en 1'b0: AXI addr add vstep 1'b1: AXI addr sub vstep
30:29	RW	0x0	esmart_dma_rreq_thold Esmart dma hurry read request thold. If esmart empty lb number >= esmart_dma_rreq_thold, dma_rreq_hurry is asserted.

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Bit	Attr	Reset Value	Description
28	RW	0x0	esmart_dma_rreq_hurry_en Enable esmart dma hurry read request. 1'b0: Disable 1'b1: Enable
27:24	RW	0x0	esmart_cbcr_gather_num The gather number of CBCR.
23:20	RW	0x0	esmart_yrgb_gather_num The gather number of YRGB.
19:17	RO	0x0	reserved
16:12	RW	0x0b	esmart_cbcr_rid AXI read id of esmart cbcr channel.
11:9	RO	0x0	reserved
8:4	RW	0x0a	esmart_yrgb_rid AXI read id of esmart yrgb channel.
3	RW	0x0	esmart_cbcr_gather_en To enable CBCR gather transfer. 1'b0: Disable 1'b1: Enable
2	RW	0x0	esmart_yrgb_gather_en To enable YRGB gather transfer. 1'b0: Disable 1'b1: Enable
1:0	RW	0x0	esmart_esmart_axi_rlen 2'b00: Burst16 (burst 15 in rgb888 pack mode) 2'b01: Burst8 (burst 12 in rgb888 pack mode) 2'b10: Burst4 (burst 6 in rgb888 pack mode) 2'b11: Reserved

ESMART0_ESMART_AXI_CTRL_IMD

Address: Operational Base(0x27D01800) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x1	esmart_dma_4k_addr_opt 1'b0: Esmart_rburst cross 4kb address, master auto opt 1'b1: Esmart_rburst cross 4kb address, dma2x auto opt
15:9	RO	0x00	reserved
8	RW	0x0	esmart_auto_gating_en 1'b0: Disable 1'b1: Enable
7:4	RW	0x0	esmart_outstanding_num Esmart outstanding number.
3	RW	0x0	esmart_outstanding_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	esmart_mmu_bypass Esmart mmu bypass enable.
1	RW	0x0	esmart_axi_sel 1'b0: Select axi0 1'b1: Select axi1
0	RW	0x0	esmart_dma_sop 1'b0: Disable 1'b1: Enable

ESMART0_REGION0_MST_CTL

Address: Operational Base(0x27D01800) + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region0_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region0_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region0_avg_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x0	region0_rg_swap Swap R and G component.
17	RW	0x0	region0_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region0_uv_swap Swap U and V component.
15	RW	0x0	region0_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region0_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region0_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region0_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region0_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region0_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region0_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region0_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7	RW	0x0	region0_argb5551_en When data_fmt = RGB565. 1'b0: Fmt sel RGB565 1'b1: Fmt sel RGBA5551
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region0_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h07: YUV400 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B 5'h17: YUV400_10B Others: Reserved
0	RW	0x0	region0_mst_en 1'b0: Disable 1'b1: Enable

ESMART0_REGION0_MST_YRGB

Address: Operational Base(0x27D01800) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_yrgb_mst Esmart region0 YRGB frame buffer memory start address.

ESMART0_REGION0_MST_CBCR

Address: Operational Base(0x27D01800) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_cbcr_mst Esmart region0 CBCR frame buffer memory start address.

ESMART0_REGION0_VIR

Address: Operational Base(0x27D01800) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region0_vir_stride_uv Number of words of mst0 uv virtual width.
15:0	RW	0x0000	region0_vir_stride Number of words of mst0 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART0_REGION0_ACT_INFO

Address: Operational Base(0x27D01800) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:16	RW	0x0000	region0_act_heigth Win_act_height = win0 vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_act_width Win_act_width = win0 horizontal size - 1

ESMART0_REGION0_DSP_INFO

Address: Operational Base(0x27D01800) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_width Dsp_width = horizontal size - 1

ESMART0_REGION0_DSP_OFFSET

Address: Operational Base(0x27D01800) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_xoff Display image horizon offset in panel.

ESMART0_REGION0_SCL_CTRL

Address: Operational Base(0x27D01800) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region0_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region0_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region0_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region0_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region0_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region0_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region0_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART0_REGION0_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01800) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region0_yrgb_yfactor When yrgb_ysu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_ysd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region0_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART0_REGION0_SCL_OFFSET

Address: Operational Base(0x27D01800) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region0_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region0_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART0_REGION1_MST_CTL

Address: Operational Base(0x27D01800) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region1_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region1_xgt_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
20	RW	0x0	region1_avg_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x0	region1_rg_swap Swap R and G component.
17	RW	0x0	region1_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region1_uv_swap Swap U and V component.
15	RW	0x0	region1_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region1_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region1_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region1_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region1_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region1_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region1_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region1_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7	RW	0x0	region1_argb5551_en When data_fmt = RGB565 1'b0: Fmt sel RGB565 1'b1: Fmt sel RGBA5551
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region1_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Other: Reserved
0	RW	0x0	region1_mst_en 1'b0: Disable 1'b1: Enable

ESMART0_REGION1_MST_YRGB

Address: Operational Base(0x27D01800) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_yrgb_mst Esmart region1 YRGB frame buffer memory start address.

ESMART0_REGION1_MST_CBCR

Address: Operational Base(0x27D01800) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_cbcr_mst Esmart region1 CBCR frame buffer memory start address.

ESMART0_REGION1_VIR

Address: Operational Base(0x27D01800) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region1_vir_stride_uv Number of words of mst1 uv virtual width.
15:0	RW	0x0000	region1_vir_stride Number of words of mst1 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART0_REGION1_ACT_INFO

Address: Operational Base(0x27D01800) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_act_heigth Win_act_height = win1 vertical size - 1
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region1_act_width Win_act_width = win1 horizontal size - 1

ESMART0_REGION1_DSP_INFO

Address: Operational Base(0x27D01800) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_width Dsp_width = horizontal size - 1

ESMART0_REGION1_DSP_OFFSET

Address: Operational Base(0x27D01800) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_xoff Display image horizon offset in panel.

ESMART0_REGION1_SCL_CTRL

Address: Operational Base(0x27D01800) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region1_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region1_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region1_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region1_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region1_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region1_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region1_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART0_REGION1_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01800) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region1_yrgb_yfactor When yrgb_ysu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_ysd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.
15:0	RW	0x1000	region1_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART0_REGION1_SCL_OFFSET

Address: Operational Base(0x27D01800) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region1_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region1_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART0_REGION2_MST_CTL

Address: Operational Base(0x27D01800) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region2_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region2_xgt_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
20	RW	0x0	region2_avg_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x0	region2_rg_swap Swap R and G component.
17	RW	0x0	region2_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region2_uv_swap Swap U and V component.
15	RW	0x0	region2_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region2_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region2_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region2_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region2_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region2_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region2_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region2_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7	RW	0x0	region2_argb5551_en When data_fmt = RGB565 1'b0: Fmt sel RGB565 1'b1: Fmt sel RGBA5551
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region2_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Other: Reserved
0	RW	0x0	region2_mst_en 1'b0: Disable 1'b1: Enable

ESMART0_REGION2_MST_YRGB

Address: Operational Base(0x27D01800) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_yrgb_mst Esmart region2 YRGB frame buffer memory start address.

ESMART0_REGION2_MST_CBCR

Address: Operational Base(0x27D01800) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_cbcr_mst Esmart region2 CBCR frame buffer memory start address.

ESMART0_REGION2_VIR

Address: Operational Base(0x27D01800) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region2_vir_stride_uv Number of words of mst2 uv virtual width.
15:0	RW	0x0000	region2_vir_stride Number of words of mst2 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win0_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART0_REGION2_ACT_INFO

Address: Operational Base(0x27D01800) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_act_heigth Win_act_height = win2 vertical size - 1
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region2_act_width Win_act_width = win2 horizontal size - 1

ESMART0_REGION2_DSP_INFO

Address: Operational Base(0x27D01800) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_width Dsp_width = horizontal size - 1

ESMART0_REGION2_DSP_OFFSET

Address: Operational Base(0x27D01800) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_xoff Display image horizon offset in panel.

ESMART0_REGION2_SCL_CTRL

Address: Operational Base(0x27D01800) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region2_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region2_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region2_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region2_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region2_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region2_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region2_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART0_REGION2_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01800) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region2_yrgb_yfactor When yrgb_ysu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_ysd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.
15:0	RW	0x1000	region2_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART0_REGION2_SCL_OFFSET

Address: Operational Base(0x27D01800) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region2_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region2_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART0_REGION3_MST_CTL

Address: Operational Base(0x27D01800) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region3_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region3_xgt_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
20	RW	0x0	region3_avg_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x0	region3_rg_swap Swap R and G component.
17	RW	0x0	region3_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region3_uv_swap Swap U and V component.
15	RW	0x0	region3_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region3_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region3_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region3_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region3_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region3_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region3_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region3_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region3_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Other: Reserved
0	RW	0x0	region3_mst_en 1'b0: Disable 1'b1: Enable

ESMART0_REGION3_MST_YRGB

Address: Operational Base(0x27D01800) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_yrgb_mst Esmart region3 YRGB frame buffer memory start address.

ESMART0_REGION3_MST_CBCR

Address: Operational Base(0x27D01800) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_cbcr_mst Esmart region3 CBCR frame buffer memory start address.

ESMART0_REGION3_VIR

Address: Operational Base(0x27D01800) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region3_vir_stride_uv Number of words of mst3 uv virtual width.
15:0	RW	0x0000	region3_vir_stride Number of words of mst3 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win0_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART0_REGION3_ACT_INFO

Address: Operational Base(0x27D01800) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_act_heigth Win_act_height = win3 vertical size - 1
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region3_act_width Win_act_width = win3 horizontal size - 1

ESMART0_REGION3_DSP_INFO

Address: Operational Base(0x27D01800) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_width Dsp_width = horizontal size - 1

ESMART0_REGION3_DSP_OFFSET

Address: Operational Base(0x27D01800) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_xoff Display image horizon offset in panel.

ESMART0_REGION3_SCL_CTRL

Address: Operational Base(0x27D01800) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region3_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region3_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region3_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region3_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region3_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region3_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region3_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART0_REGION3_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01800) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region3_yrgb_yfactor When yrgb_ysu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_ysd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region3_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART0_REGION3_SCL_OFFSET

Address: Operational Base(0x27D01800) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region3_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region3_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART0_ESMART_KEY_CTRL

Address: Operational Base(0x27D01800) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_key_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_key_value Esmart RED color key.
19:10	RW	0x000	esmart_g_key_value Esmart GREEN color key.
9:0	RW	0x000	esmart_b_key_value Esmart Blue color key.

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ESMART0_ESMART_BG_EN

Address: Operational Base(0x27D01800) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_value Esmart background red color.
19:10	RW	0x000	esmart_g_value Esmart background green color.
9:0	RW	0x000	esmart_b_value Esmart background blue color.

ESMART0_ESMART_ALPHA_MAP

Address: Operational Base(0x27D01800) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31	RW	0x0	alpha_map_en 1'b0: Disable 1'b1: Enable
30:16	RO	0x0000	reserved
15:8	RW	0x00	alpha_1_map When format = rgba5551, alpha value = 1'b1 mapping value.
7:0	RW	0x00	alpha_0_map When format = rgba5551, alpha value = 1'b0 mapping value.

ESMART0_ESMART_PORT_SEL_IMD

Address: Operational Base(0x27D01800) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	esmart_port_sel 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved

ESMART0_ESMART_DLY_NUM

Address: Operational Base(0x27D01800) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x17	esmart_dly_num Esmart delay cycle number.

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ESMART1_ESMART_CTRL0

Address: Operational Base(0x27D01A00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_frm_resetn_en 1'b0: Disable 1'b1: Enable
30:25	RO	0x00	reserved
24	RW	0x0	esmart_yuv2rgb_force_en When enable the bit. layer out data foce support yuv2rgb. 1'b0: Disable out data force data transform 1'b1: Enable out data force transform

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Bit	Attr	Reset Value	Description
23:14	RO	0x000	reserved
13:12	RW	0x1	esmart_scl_num 2'b00: Scale engine0 2'b01: Scale engine1 2'b10: Scale engine2 2'b11: Scale engine3
11:10	RO	0x0	reserved
9	RW	0x0	esmart_endian_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte0,byte1,byte2,byte3}
8	RW	0x0	esmart_mid_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte3,byte1,byte2,byte0}
7:6	RO	0x0	reserved
5	RW	0x0	esmart_8bpp_alpha_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	esmart_8bpp_lut_en To enable 8bpp LUT.
3:2	RW	0x0	esmart_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	esmart_rgb2yuv_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	esmart_yuv2rgb_en 1'b0: Disable 1'b1: Enable

ESMART1_ESMART_CTRL1

Address: Operational Base(0x27D01A00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_ymir_en 1'b0: AXI addr add vstep 1'b1: AXI addr sub vstep
30:29	RW	0x0	esmart_dma_rreq_thold Esmart dma hurry read request thold. If esmart empty lb number >= esmart_dma_rreq_thold, dma_rreq_hurry is asserted.
28	RW	0x0	esmart_dma_rreq_hurry_en Enable esmart dma hurry read request. 1'b0: Disable 1'b1: Enable
27:24	RW	0x0	esmart_cbcr_gather_num The gather number of CBCR.
23:20	RW	0x0	esmart_yrgb_gather_num The gather number of YRGB.
19:17	RO	0x0	reserved
16:12	RW	0x0d	esmart_cbcr_rid AXI read id of esmart cbcr channel.
11:9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x0c	esmart_yrgb_rid AXI read id of esmart yrgb channel.
3	RW	0x0	esmart_cbcr_gather_en To enable CBCR gather transfer. 1'b0: Disable 1'b1: Enable
2	RW	0x0	esmart_yrgb_gather_en To enable YRGB gather transfer. 1'b0: Disable 1'b1: Enable
1:0	RW	0x0	esmart_esmart_axi_rlen 2'b00: Burst16 (burst 15 in rgb888 pack mode) 2'b01: Burst8 (burst 12 in rgb888 pack mode) 2'b10: Burst4 (burst 6 in rgb888 pack mode) 2'b11: Reserved

ESMART1_ESMART_AXI_CTRL_IMD

Address: Operational Base(0x27D01A00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x1	esmart_dma_4k_addr_opt 1'b0: Esmart_rburst cross 4kb address, master auto opt 1'b1: Esmart_rburst cross 4kb address, dma2x auto opt
15:9	RO	0x00	reserved
8	RW	0x0	esmart_auto_gating_en 1'b0: Disable 1'b1: Enable
7:4	RW	0x0	esmart_outstanding_num Esmart outstanding number.
3	RW	0x0	esmart_outstanding_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	esmart_mmu_bypass Esmart mmu bypass enable.
1	RW	0x0	esmart_axi_sel 1'b0: Select axi0 1'b1: Select axi1
0	RW	0x0	esmart_dma_sop 1'b0: Disable 1'b1: Enable

ESMART1_REGION0_MST_CTL

Address: Operational Base(0x27D01A00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region0_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region0_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region0_avg_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
19	RO	0x0	reserved
18	RW	0x0	region0_rg_swap Swap R and G component.
17	RW	0x0	region0_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region0_uv_swap Swap U and V component.
15	RW	0x0	region0_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region0_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region0_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region0_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region0_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region0_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region0_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region0_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7	RW	0x0	region0_argb5551_en When data_fmt = RGB565. 1'b0: Fmt sel RGB565 1'b1: Fmt sel RGBA5551
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region0_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h07: YUV400 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B 5'h17: YUV400_10B Other: Reserved
0	RW	0x0	region0_mst_en 1'b0: Disable 1'b1: Enable

ESMART1_REGION0_MST_YRGB

Address: Operational Base(0x27D01A00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_yrgb_mst Esmart region0 YRGB frame buffer memory start address.

ESMART1_REGION0_MST_CBCR

Address: Operational Base(0x27D01A00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_cbcr_mst Esmart region0 CBCR frame buffer memory start address.

ESMART1_REGION0_VIR

Address: Operational Base(0x27D01A00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region0_vir_stride_uv Number of words of mst0 uv virtual width.
15:0	RW	0x0000	region0_vir_stride Number of words of mst0 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART1_REGION0_ACT_INFO

Address: Operational Base(0x27D01A00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:16	RW	0x0000	region0_act_heigth Win_act_height = win0 vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_act_width Win_act_width = win0 horizontal size - 1

ESMART1_REGION0_DSP_INFO

Address: Operational Base(0x27D01A00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_width Dsp_width = horizontal size - 1

ESMART1_REGION0_DSP_OFFSET

Address: Operational Base(0x27D01A00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_xoff Display image horizon offset in panel.

ESMART1_REGION0_SCL_CTRL

Address: Operational Base(0x27D01A00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region0_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region0_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region0_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region0_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region0_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region0_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region0_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART1_REGION0_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01A00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region0_yrgb_yfactor When yrgb_ysu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_ysd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region0_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART1_REGION0_SCL_OFFSET

Address: Operational Base(0x27D01A00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region0_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region0_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART1_REGION1_MST_CTL

Address: Operational Base(0x27D01A00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region1_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region1_xgt_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
20	RW	0x0	region1_avg_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x0	region1_rg_swap Swap R and G component.
17	RW	0x0	region1_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region1_uv_swap Swap U and V component.
15	RW	0x0	region1_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region1_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region1_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region1_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region1_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region1_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region1_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region1_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7	RW	0x0	region1_argb5551_en When data_fmt = RGB565 1'b0: Fmt sel RGB565 1'b1: Fmt sel RGBA5551
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region1_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Other: Reserved
0	RW	0x0	region1_mst_en 1'b0: Disable 1'b1: Enable

ESMART1_REGION1_MST_YRGB

Address: Operational Base(0x27D01A00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_yrgb_mst Esmart region1 YRGB frame buffer memory start address.

ESMART1_REGION1_MST_CBCR

Address: Operational Base(0x27D01A00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_cbcr_mst Esmart region1 CBCR frame buffer memory start address.

ESMART1_REGION1_VIR

Address: Operational Base(0x27D01A00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region1_vir_stride_uv Number of words of mst1 uv virtual width.
15:0	RW	0x0000	region1_vir_stride Number of words of mst1 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART1_REGION1_ACT_INFO

Address: Operational Base(0x27D01A00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_act_heigth Win_act_height = win1 vertical size - 1
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region1_act_width Win_act_width = win1 horizontal size - 1

ESMART1_REGION1_DSP_INFO

Address: Operational Base(0x27D01A00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_width Dsp_width = horizontal size - 1

ESMART1_REGION1_DSP_OFFSET

Address: Operational Base(0x27D01A00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_xoff Display image horizon offset in panel.

ESMART1_REGION1_SCL_CTRL

Address: Operational Base(0x27D01A00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region1_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region1_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region1_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region1_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region1_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region1_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region1_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART1_REGION1_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01A00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region1_yrgb_yfactor When yrgb_ysu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_ysd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region1_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART1_REGION1_SCL_OFFSET

Address: Operational Base(0x27D01A00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region1_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region1_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART1_REGION2_MST_CTL

Address: Operational Base(0x27D01A00) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region2_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region2_xgt_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
20	RW	0x0	region2_avg_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x0	region2_rg_swap Swap R and G component.
17	RW	0x0	region2_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region2_uv_swap Swap U and V component.
15	RW	0x0	region2_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region2_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region2_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region2_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region2_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region2_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region2_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region2_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7	RW	0x0	region2_argb5551_en When data_fmt = RGB565 1'b0: Fmt sel RGB565 1'b1: Fmt sel RGBA5551
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region2_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Other: Reserved
0	RW	0x0	region2_mst_en 1'b0: Disable 1'b1: Enable

ESMART1_REGION2_MST_YRGB

Address: Operational Base(0x27D01A00) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_yrgb_mst Esmart region2 YRGB frame buffer memory start address.

ESMART1_REGION2_MST_CBCR

Address: Operational Base(0x27D01A00) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_cbcr_mst Esmart region2 CBCR frame buffer memory start address.

ESMART1_REGION2_VIR

Address: Operational Base(0x27D01A00) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region2_vir_stride_uv Number of words of mst2 uv virtual width.
15:0	RW	0x0000	region2_vir_stride Number of words of mst2 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win0_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART1_REGION2_ACT_INFO

Address: Operational Base(0x27D01A00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_act_heigth Win_act_height = win2 vertical size - 1
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region2_act_width Win_act_width = win2 horizontal size - 1

ESMART1_REGION2_DSP_INFO

Address: Operational Base(0x27D01A00) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_width Dsp_width = horizontal size - 1

ESMART1_REGION2_DSP_OFFSET

Address: Operational Base(0x27D01A00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_xoff Display image horizon offset in panel.

ESMART1_REGION2_SCL_CTRL

Address: Operational Base(0x27D01A00) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region2_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region2_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region2_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region2_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region2_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region2_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region2_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART1_REGION2_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01A00) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region2_yrgb_yfactor When yrgb_ysu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_ysd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region2_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART1_REGION2_SCL_OFFSET

Address: Operational Base(0x27D01A00) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region2_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region2_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART1_REGION3_MST_CTL

Address: Operational Base(0x27D01A00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region3_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region3_xgt_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
20	RW	0x0	region3_avg_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x0	region3_rg_swap Swap R and G component.
17	RW	0x0	region3_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region3_uv_swap Swap U and V component.
15	RW	0x0	region3_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region3_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region3_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region3_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region3_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region3_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region3_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region3_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region3_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Other: Reserved
0	RW	0x0	region3_mst_en 1'b0: Disable 1'b1: Enable

ESMART1_REGION3_MST_YRGB

Address: Operational Base(0x27D01A00) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_yrgb_mst Esmart region3 YRGB frame buffer memory start address.

ESMART1_REGION3_MST_CBCR

Address: Operational Base(0x27D01A00) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_cbcr_mst Esmart region3 CBCR frame buffer memory start address.

ESMART1_REGION3_VIR

Address: Operational Base(0x27D01A00) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region3_vir_stride_uv Number of words of mst3 uv virtual width.
15:0	RW	0x0000	region3_vir_stride Number of words of mst3 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win0_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART1_REGION3_ACT_INFO

Address: Operational Base(0x27D01A00) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_act_heigth Win_act_height = win3 vertical size - 1
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region3_act_width Win_act_width = win3 horizontal size - 1

ESMART1_REGION3_DSP_INFO

Address: Operational Base(0x27D01A00) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_width Dsp_width = horizontal size - 1

ESMART1_REGION3_DSP_OFFSET

Address: Operational Base(0x27D01A00) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_xoff Display image horizon offset in panel.

ESMART1_REGION3_SCL_CTRL

Address: Operational Base(0x27D01A00) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region3_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region3_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region3_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region3_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region3_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region3_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region3_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART1_REGION3_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01A00) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region3_yrgb_yfactor When yrgb_ysu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_ysd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region3_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART1_REGION3_SCL_OFFSET

Address: Operational Base(0x27D01A00) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region3_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region3_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART1_ESMART_KEY_CTRL

Address: Operational Base(0x27D01A00) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_key_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_key_value Esmart RED color key.
19:10	RW	0x000	esmart_g_key_value Esmart GREEN color key.
9:0	RW	0x000	esmart_b_key_value Esmart Blue color key.

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ESMART1_ESMART_BG_EN

Address: Operational Base(0x27D01A00) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_value Esmart background red color.
19:10	RW	0x000	esmart_g_value Esmart background green color.
9:0	RW	0x000	esmart_b_value Esmart background blue color.

ESMART1_ESMART_ALPHA_MAP

Address: Operational Base(0x27D01A00) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31	RW	0x1	alpha_map_en 1'b0: Disable 1'b1: Enable
30:16	RO	0x0000	reserved
15:8	RW	0x00	alpha_1_map When format = rgba5551, alpha value = 1'b1 mapping value.
7:0	RW	0x00	alpha_0_map When format = rgba5551, alpha value = 1'b0 mapping value.

ESMART1_ESMART_PORT_SEL_IMD

Address: Operational Base(0x27D01A00) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	esmart_port_sel 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved

ESMART1_ESMART_DLY_NUM

Address: Operational Base(0x27D01A00) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x17	esmart_dly_num Esmart delay cycle number.

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ESMART2_ESMART_CTRL0

Address: Operational Base(0x27D01C00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_frm_resetn_en 1'b0: Disable 1'b1: Enable
30:25	RO	0x00	reserved
24	RW	0x0	esmart_yuv2rgb_force_en When enable the bit, layer out data foce support yuv2rgb. 1'b0: Disable out data force data transform 1'b1: Enable out data force transform

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Bit	Attr	Reset Value	Description
23:14	RO	0x000	reserved
13:12	RW	0x2	esmart_scl_num 2'b00: Scale engine0 2'b01: Scale engine1 2'b10: Scale engine2 2'b11: Scale engine3
11:10	RO	0x0	reserved
9	RW	0x0	esmart_endian_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte0,byte1,byte2,byte3}
8	RW	0x0	esmart_mid_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte3,byte1,byte2,byte0}
7:6	RO	0x0	reserved
5	RW	0x0	esmart_8bpp_alpha_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	esmart_8bpp_lut_en To enable 8bpp LUT.
3:2	RW	0x0	esmart_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	esmart_rgb2yuv_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	esmart_yuv2rgb_en 1'b0: Disable 1'b1: Enable

ESMART2_ESMART_CTRL1

Address: Operational Base(0x27D01C00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_ymir_en 1'b0: AXI addr add vstep 1'b1: AXI addr sub vstep
30:29	RW	0x0	esmart_dma_rreq_thold Esmart dma hurry read request thold. If esmart empty lb number >= esmart_dma_rreq_thold, dma_rreq_hurry is asserted.
28	RW	0x0	esmart_dma_rreq_hurry_en Enable esmart dma hurry read request. 1'b0: Disable 1'b1: Enable
27:24	RW	0x0	esmart_cbcr_gather_num The gather number of CBCR.
23:20	RW	0x0	esmart_yrgb_gather_num The gather number of YRGB.
19:17	RO	0x0	reserved
16:12	RW	0x0b	esmart_cbcr_rid AXI read id of esmart cbcr channel.
11:9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x0a	esmart_yrgb_rid AXI read id of esmart yrgb channel.
3	RW	0x0	esmart_cbcr_gather_en To enable CBCR gather transfer. 1'b0: Disable 1'b1: Enable
2	RW	0x0	esmart_yrgb_gather_en To enable YRGB gather transfer. 1'b0: Disable 1'b1: Enable
1:0	RW	0x0	esmart_esmart_axi_rlen 2'b00: Burst16 (burst 15 in rgb888 pack mode) 2'b01: Burst8 (burst 12 in rgb888 pack mode) 2'b10: Burst4 (burst 6 in rgb888 pack mode) 2'b11: Reserved

ESMART2_ESMART_AXI_CTRL_IMD

Address: Operational Base(0x27D01C00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	esmart_dma_4k_addr_opt 1'b0: Esmart_rburst cross 4kb address, master auto opt 1'b1: Esmart_rburst cross 4kb address, dma2x auto opt
15:9	RO	0x00	reserved
8	RW	0x0	esmart_auto_gating_en 1'b0: Disable 1'b1: Enable
7:4	RW	0x0	esmart_outstanding_num Esmart outstanding number.
3	RW	0x0	esmart_outstanding_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	esmart_mmu_bypass Esmart mmu bypass enable.
1	RW	0x1	esmart_axi_sel 1'b0: Select axi0 1'b1: Select axi1
0	RW	0x0	esmart_dma_sop 1'b0: Disable 1'b1: Enable

ESMART2_REGION0_MST_CTL

Address: Operational Base(0x27D01C00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region0_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region0_xgt_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	region0_avg_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
19	RO	0x0	reserved
18	RW	0x0	region0_rg_swap Swap R and G component.
17	RW	0x0	region0_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region0_uv_swap Swap U and V component.
15	RW	0x0	region0_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region0_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region0_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region0_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region0_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region0_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region0_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region0_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7	RW	0x0	region0_argb5551_en When data_fmt = RGB565. 1'b0: Fmt sel RGB565 1'b1: Fmt sel RGBA5551
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region0_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h07: YUV400 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B 5'h17: YUV400_10B Other: Reserved
0	RW	0x0	region0_mst_en 1'b0: Disable 1'b1: Enable

ESMART2_REGION0_MST_YRGB

Address: Operational Base(0x27D01C00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_yrgb_mst Esmart region0 YRGB frame buffer memory start address.

ESMART2_REGION0_MST_CBCR

Address: Operational Base(0x27D01C00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_cbcr_mst Esmart region0 CBCR frame buffer memory start address.

ESMART2_REGION0_VIR

Address: Operational Base(0x27D01C00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region0_vir_stride_uv Number of words of mst0 uv virtual width.
15:0	RW	0x0000	region0_vir_stride Number of words of mst0 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART2_REGION0_ACT_INFO

Address: Operational Base(0x27D01C00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:16	RW	0x0000	region0_act_heigth Win_act_height = win0 vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_act_width Win_act_width = win0 horizontal size - 1

ESMART2_REGION0_DSP_INFO

Address: Operational Base(0x27D01C00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_width Dsp_width = horizontal size - 1

ESMART2_REGION0_DSP_OFFSET

Address: Operational Base(0x27D01C00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_xoff Display image horizon offset in panel.

ESMART2_REGION0_SCL_CTRL

Address: Operational Base(0x27D01C00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region0_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region0_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved when yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region0_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region0_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region0_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region0_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region0_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART2_REGION0_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01C00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region0_yrgb_yfactor When yrgb_ysu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_ysd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region0_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART2_REGION0_SCL_OFFSET

Address: Operational Base(0x27D01C00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region0_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region0_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART2_REGION1_MST_CTL

Address: Operational Base(0x27D01C00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region1_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region1_xgt_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
20	RW	0x0	region1_avg_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x0	region1_rg_swap Swap R and G component.
17	RW	0x0	region1_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region1_uv_swap Swap U and V component.
15	RW	0x0	region1_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region1_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region1_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region1_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region1_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region1_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region1_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region1_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7	RW	0x0	region1_argb5551_en When data_fmt = RGB565 1'b0: Fmt sel RGB565 1'b1: Fmt sel RGBA5551
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region1_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Other: Reserved
0	RW	0x0	region1_mst_en 1'b0: Disable 1'b1: Enable

ESMART2_REGION1_MST_YRGB

Address: Operational Base(0x27D01C00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_yrgb_mst Esmart region1 YRGB frame buffer memory start address.

ESMART2_REGION1_MST_CBCR

Address: Operational Base(0x27D01C00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_cbcr_mst Esmart region1 CBCR frame buffer memory start address.

ESMART2_REGION1_VIR

Address: Operational Base(0x27D01C00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region1_vir_stride_uv Number of words of mst1 uv virtual width.
15:0	RW	0x0000	region1_vir_stride Number of words of mst1 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART2_REGION1_ACT_INFO

Address: Operational Base(0x27D01C00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_act_heigth Win_act_height = win1 vertical size - 1
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region1_act_width Win_act_width = win1 horizontal size - 1

ESMART2_REGION1_DSP_INFO

Address: Operational Base(0x27D01C00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_width Dsp_width = horizontal size - 1

ESMART2_REGION1_DSP_OFFSET

Address: Operational Base(0x27D01C00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_xoff Display image horizon offset in panel.

ESMART2_REGION1_SCL_CTRL

Address: Operational Base(0x27D01C00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region1_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region1_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region1_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region1_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region1_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region1_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region1_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART2_REGION1_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01C00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region1_yrgb_yfactor When yrgb_ysu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_ysd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region1_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART2_REGION1_SCL_OFFSET

Address: Operational Base(0x27D01C00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region1_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region1_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART2_REGION2_MST_CTL

Address: Operational Base(0x27D01C00) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region2_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region2_xgt_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
20	RW	0x0	region2_avg_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x0	region2_rg_swap Swap R and G component.
17	RW	0x0	region2_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region2_uv_swap Swap U and V component.
15	RW	0x0	region2_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region2_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region2_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region2_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region2_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region2_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region2_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region2_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7	RW	0x0	region2_argb5551_en When data_fmt = RGB565 1'b0: Fmt sel RGB565 1'b1: Fmt sel RGBA5551
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region2_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Other: Reserved
0	RW	0x0	region2_mst_en 1'b0: Disable 1'b1: Enable

ESMART2_REGION2_MST_YRGB

Address: Operational Base(0x27D01C00) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_yrgb_mst Esmart region2 YRGB frame buffer memory start address.

ESMART2_REGION2_MST_CBCR

Address: Operational Base(0x27D01C00) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_cbcr_mst Esmart region2 CBCR frame buffer memory start address.

ESMART2_REGION2_VIR

Address: Operational Base(0x27D01C00) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region2_vir_stride_uv Number of words of mst2 uv virtual width.
15:0	RW	0x0000	region2_vir_stride Number of words of mst2 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win0_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART2_REGION2_ACT_INFO

Address: Operational Base(0x27D01C00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_act_heigth Win_act_height = win2 vertical size - 1
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region2_act_width Win_act_width = win2 horizontal size - 1

ESMART2_REGION2_DSP_INFO

Address: Operational Base(0x27D01C00) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_width Dsp_width = horizontal size - 1

ESMART2_REGION2_DSP_OFFSET

Address: Operational Base(0x27D01C00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_xoff Display image horizon offset in panel.

ESMART2_REGION2_SCL_CTRL

Address: Operational Base(0x27D01C00) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region2_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region2_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region2_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region2_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region2_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region2_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region2_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART2_REGION2_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01C00) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region2_yrgb_yfactor When yrgb_ysu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_ysd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region2_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART2_REGION2_SCL_OFFSET

Address: Operational Base(0x27D01C00) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region2_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region2_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART2_REGION3_MST_CTL

Address: Operational Base(0x27D01C00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region3_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region3_xgt_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
20	RW	0x0	region3_avg_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x0	region3_rg_swap Swap R and G component.
17	RW	0x0	region3_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region3_uv_swap Swap U and V component.
15	RW	0x0	region3_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region3_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region3_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region3_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region3_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region3_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region3_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region3_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region3_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Other: Reserved
0	RW	0x0	region3_mst_en 1'b0: Disable 1'b1: Enable

ESMART2_REGION3_MST_YRGB

Address: Operational Base(0x27D01C00) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_yrgb_mst Esmart region3 YRGB frame buffer memory start address.

ESMART2_REGION3_MST_CBCR

Address: Operational Base(0x27D01C00) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_cbcr_mst Esmart region3 CBCR frame buffer memory start address.

ESMART2_REGION3_VIR

Address: Operational Base(0x27D01C00) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region3_vir_stride_uv Number of words of mst3 uv virtual width.
15:0	RW	0x0000	region3_vir_stride Number of words of mst3 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win0_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART2_REGION3_ACT_INFO

Address: Operational Base(0x27D01C00) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_act_heigth Win_act_height = win3 vertical size - 1
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region3_act_width Win_act_width = win3 horizontal size - 1

ESMART2_REGION3_DSP_INFO

Address: Operational Base(0x27D01C00) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_width Dsp_width = horizontal size - 1

ESMART2_REGION3_DSP_OFFSET

Address: Operational Base(0x27D01C00) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_xoff Display image horizon offset in panel.

ESMART2_REGION3_SCL_CTRL

Address: Operational Base(0x27D01C00) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region3_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region3_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region3_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region3_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region3_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region3_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region3_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART2_REGION3_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01C00) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region3_yrgb_yfactor When yrgb_ysu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_ysd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region3_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART2_REGION3_SCL_OFFSET

Address: Operational Base(0x27D01C00) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region3_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region3_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART2_ESMART_KEY_CTRL

Address: Operational Base(0x27D01C00) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_key_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_key_value Esmart RED color key.
19:10	RW	0x000	esmart_g_key_value Esmart GREEN color key.
9:0	RW	0x000	esmart_b_key_value Esmart Blue color key.

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ESMART2_ESMART_BG_EN

Address: Operational Base(0x27D01C00) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_value Esmart Background Red color.
19:10	RW	0x000	esmart_g_value Esmart Background Green color.
9:0	RW	0x000	esmart_b_value Esmart Background Blue color.

ESMART2_ESMART_ALPHA_MAP

Address: Operational Base(0x27D01C00) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31	RW	0x0	alpha_map_en 1'b0: Disable 1'b1: Enable
30:16	RO	0x0000	reserved
15:8	RW	0x00	alpha_1_map When format = rgba5551, alpha value = 1'b1 mapping value.
7:0	RW	0x00	alpha_0_map When format = rgba5551, alpha value = 1'b0 mapping value.

ESMART2_ESMART_PORT_SEL_IMD

Address: Operational Base(0x27D01C00) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	esmart_port_sel 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved

ESMART2_ESMART_DLY_NUM

Address: Operational Base(0x27D01C00) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x17	esmart_dly_num Esmart delay cycle number.

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ESMART3_ESMART_CTRL0

Address: Operational Base(0x27D01E00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_frm_resetn_en 1'b0: Disable 1'b1: Enable
30:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24	RW	0x0	esmart_yuv2rgb_force_en When enable the bit, layer out data foce support yuv2rgb. 1'b0: Disable out data force data transform 1'b1: Enable out data force transform
23:14	RO	0x000	reserved
13:12	RW	0x3	esmart_scl_num 2'b00: Scale engine0 2'b01: Scale engine1 2'b10: Scale engine2 2'b11: Scale engine3
11:10	RO	0x0	reserved
9	RW	0x0	esmart_endian_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte0,byte1,byte2,byte3}
8	RW	0x0	esmart_mid_swap 1'b0: {byte3,byte2,byte1,byte0} 1'b1: {byte3,byte1,byte2,byte0}
7:6	RO	0x0	reserved
5	RW	0x0	esmart_8bpp_alpha_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	esmart_8bpp_lut_en To enable 8bpp LUT.
3:2	RW	0x0	esmart_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	esmart_rgb2yuv_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	esmart_yuv2rgb_en 1'b0: Disable 1'b1: Enable

ESMART3_ESMART_CTRL1

Address: Operational Base(0x27D01E00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_ymir_en 1'b0: AXI addr add vstep 1'b1: AXI addr sub vstep
30:29	RW	0x0	esmart_dma_rreq_thold Esmart dma hurry read request thold. If esmart empty lb number >= esmart_dma_rreq_thold, dma_rreq_hurry is asserted.
28	RW	0x0	esmart_dma_rreq_hurry_en Enable esmart dma hurry read request. 1'b0: Disable 1'b1: Enable
27:24	RW	0x0	esmart_cbcr_gather_num The gather number of CBCR.
23:20	RW	0x0	esmart_yrgb_gather_num The gather number of YRGB.
19:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16:12	RW	0x0d	esmart_cbcr_rid AXI read id of esmart cbcr channel.
11:9	RO	0x0	reserved
8:4	RW	0x0c	esmart_yrgb_rid AXI read id of esmart yrgb channel.
3	RW	0x0	esmart_cbcr_gather_en To enable CBCR gather transfer. 1'b0: Disable 1'b1: Enable
2	RW	0x0	esmart_yrgb_gather_en To enable YRGB gather transfer. 1'b0: Disable 1'b1: Enable
1:0	RW	0x0	esmart_esmart_axi_rlen 2'b00: Burst16 (burst 15 in rgb888 pack mode) 2'b01: Burst8 (burst 12 in rgb888 pack mode) 2'b10: Burst4 (burst 6 in rgb888 pack mode) 2'b11: Reserved

ESMART3_ESMART_AXI_CTRL_IMD

Address: Operational Base(0x27D01E00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x1	esmart_dma_4k_addr_opt 1'b0: Esmart_rburst cross 4kb address, master auto opt 1'b1: Esmart_rburst cross 4kb address, dma2x auto opt
15:9	RO	0x00	reserved
8	RW	0x0	esmart_auto_gating_en 1'b0: Disable 1'b1: Enable
7:4	RW	0x0	esmart_outstanding_num Esmart outstanding number.
3	RW	0x0	esmart_outstanding_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	esmart_mmu_bypass Esmart mmu bypass enable.
1	RW	0x1	esmart_axi_sel 1'b0: Select axi0 1'b1: Select axi1
0	RW	0x0	esmart_dma_sop 1'b0: Disable 1'b1: Enable

ESMART3_REGION0_MST_CTL

Address: Operational Base(0x27D01E00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region0_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region0_xgt_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
20	RW	0x0	region0_avg_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x0	region0_rg_swap Swap R and G component.
17	RW	0x0	region0_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region0_uv_swap Swap U and V component.
15	RW	0x0	region0_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region0_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region0_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region0_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region0_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region0_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region0_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region0_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7	RW	0x0	region0_argb5551_en When data_fmt = RGB565. 1'b0: Fmt sel RGB565 1'b1: Fmt sel RGBA5551
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region0_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h07: YUV400 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B 5'h17: YUV400_10B Other: Reserved
0	RW	0x0	region0_mst_en 1'b0: Disable 1'b1: Enable

ESMART3_REGION0_MST_YRGB

Address: Operational Base(0x27D01E00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_yrgb_mst Esmart region0 YRGB frame buffer memory start address.

ESMART3_REGION0_MST_CBCR

Address: Operational Base(0x27D01E00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_cbcr_mst Esmart region0 CBCR frame buffer memory start address.

ESMART3_REGION0_VIR

Address: Operational Base(0x27D01E00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region0_vir_stride_uv Number of words of mst0 uv virtual width.
15:0	RW	0x0000	region0_vir_stride Number of words of mst0 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART3_REGION0_ACT_INFO

Address: Operational Base(0x27D01E00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:16	RW	0x0000	region0_act_heigth Win_act_height = win0 vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_act_width Win_act_width = win0 horizontal size - 1

ESMART3_REGION0_DSP_INFO

Address: Operational Base(0x27D01E00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_width Dsp_width = horizontal size - 1

ESMART3_REGION0_DSP_OFFSET

Address: Operational Base(0x27D01E00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_xoff Display image horizon offset in panel.

ESMART3_REGION0_SCL_CTRL

Address: Operational Base(0x27D01E00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region0_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region0_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved when yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region0_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region0_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region0_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region0_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region0_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART3_REGION0_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01E00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region0_yrgb_yfactor When yrgb_ysu:factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_ysd:factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.
15:0	RW	0x1000	region0_yrgb_xfactor When yrgb_xsu:factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_xsd:factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

ESMART3_REGION0_SCL_OFFSET

Address: Operational Base(0x27D01E00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region0_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region0_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART3_REGION1_MST_CTL

Address: Operational Base(0x27D01E00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region1_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region1_xgt_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
20	RW	0x0	region1_avg_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x0	region1_rg_swap Swap R and G component.
17	RW	0x0	region1_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region1_uv_swap Swap U and V component.
15	RW	0x0	region1_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region1_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region1_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region1_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region1_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region1_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region1_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region1_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7	RW	0x0	region1_argb5551_en When data_fmt = RGB565 1'b0: Fmt sel RGB565 1'b1: Fmt sel RGBA5551
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region1_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Other: Reserved
0	RW	0x0	region1_mst_en 1'b0: Disable 1'b1: Enable

ESMART3_REGION1_MST_YRGB

Address: Operational Base(0x27D01E00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_yrgb_mst Esmart region1 YRGB frame buffer memory start address.

ESMART3_REGION1_MST_CBCR

Address: Operational Base(0x27D01E00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_cbcr_mst Esmart region1 CBCR frame buffer memory start address.

ESMART3_REGION1_VIR

Address: Operational Base(0x27D01E00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region1_vir_stride_uv Number of words of mst1 uv virtual width.
15:0	RW	0x0000	region1_vir_stride Number of words of mst1 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART3_REGION1_ACT_INFO

Address: Operational Base(0x27D01E00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_act_heigth Win_act_height = win1 vertical size - 1
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region1_act_width Win_act_width = win1 horizontal size - 1

ESMART3_REGION1_DSP_INFO

Address: Operational Base(0x27D01E00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_width Dsp_width = horizontal size - 1

ESMART3_REGION1_DSP_OFFSET

Address: Operational Base(0x27D01E00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_xoff Display image horizon offset in panel.

ESMART3_REGION1_SCL_CTRL

Address: Operational Base(0x27D01E00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region1_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region1_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region1_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region1_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region1_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region1_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region1_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART3_REGION1_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01E00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region1_yrgb_yfactor When yrgb_ysu:factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_ysd:factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.
15:0	RW	0x1000	region1_yrgb_xfactor When yrgb_xsu:factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_xsd:factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

ESMART3_REGION1_SCL_OFFSET

Address: Operational Base(0x27D01E00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region1_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region1_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART3_REGION2_MST_CTL

Address: Operational Base(0x27D01E00) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region2_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region2_xgt_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
20	RW	0x0	region2_avg_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x0	region2_rg_swap Swap R and G component.
17	RW	0x0	region2_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region2_uv_swap Swap U and V component.
15	RW	0x0	region2_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region2_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region2_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region2_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region2_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region2_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region2_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region2_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7	RW	0x0	region2_argb5551_en When data_fmt = RGB565. 1'b0: Fmt sel RGB565 1'b1: Fmt sel RGBA5551
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region2_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Other: Reserved
0	RW	0x0	region2_mst_en 1'b0: Disable 1'b1: Enable

ESMART3_REGION2_MST_YRGB

Address: Operational Base(0x27D01E00) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_yrgb_mst Esmart region2 YRGB frame buffer memory start address.

ESMART3_REGION2_MST_CBCR

Address: Operational Base(0x27D01E00) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_cbcr_mst Esmart region2 CBCR frame buffer memory start address.

ESMART3_REGION2_VIR

Address: Operational Base(0x27D01E00) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region2_vir_stride_uv Number of words of mst2 uv virtual width.
15:0	RW	0x0000	region2_vir_stride Number of words of mst2 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win0_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART3_REGION2_ACT_INFO

Address: Operational Base(0x27D01E00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_act_heigth Win_act_height = win2 vertical size - 1
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region2_act_width Win_act_width = win2 horizontal size - 1

ESMART3_REGION2_DSP_INFO

Address: Operational Base(0x27D01E00) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_width Dsp_width = horizontal size - 1

ESMART3_REGION2_DSP_OFFSET

Address: Operational Base(0x27D01E00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_xoff Display image horizon offset in panel.

ESMART3_REGION2_SCL_CTRL

Address: Operational Base(0x27D01E00) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region2_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region2_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region2_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region2_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region2_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region2_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region2_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART3_REGION2_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01E00) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region2_yrgb_yfactor When yrgb_ysu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_ysd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region2_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

ESMART3_REGION2_SCL_OFFSET

Address: Operational Base(0x27D01E00) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region2_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region2_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART3_REGION3_MST_CTL

Address: Operational Base(0x27D01E00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	region3_xgt_mode 2'b00: Xgt2 or Xavg2 2'b01: Xgt4 or Xavg4 Other: Reserved
21	RW	0x0	region3_xgt_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
20	RW	0x0	region3_avg_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x0	region3_rg_swap Swap R and G component.
17	RW	0x0	region3_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region3_uv_swap Swap U and V component.
15	RW	0x0	region3_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region3_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region3_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region3_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region3_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enable.
10	RW	0x0	region3_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enable.
9	RW	0x0	region3_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enable.
8	RW	0x0	region3_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enable.
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:1	RW	0x00	region3_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h03: RGBA1010102 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h0a: VYUY422 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B Other: Reserved
0	RW	0x0	region3_mst_en 1'b0: Disable 1'b1: Enable

ESMART3_REGION3_MST_YRGB

Address: Operational Base(0x27D01E00) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_yrgb_mst Esmart region3 YRGB frame buffer memory start address.

ESMART3_REGION3_MST_CBCR

Address: Operational Base(0x27D01E00) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_cbcr_mst Esmart region3 CBCR frame buffer memory start address.

ESMART3_REGION3_VIR

Address: Operational Base(0x27D01E00) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region3_vir_stride_uv Number of words of mst3 uv virtual width.
15:0	RW	0x0000	region3_vir_stride Number of words of mst3 yrgb virtual width. ARGB888: Win_vir_width RGB888: (Win_vir_width*3/4) + (Win_vir_width%3) RGB565: Ceil(win0_vir_width/2) YUV: Ceil(win_vir_width/4) YUV tile: Ceil(win_vir_width/4) YUYV,YVYU,UYVY,VYUY: Ceil(win_vir_width/4)

ESMART3_REGION3_ACT_INFO

Address: Operational Base(0x27D01E00) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_act_heigth Win_act_height = win3 vertical size - 1
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region3_act_width Win_act_width = win3 horizontal size - 1

ESMART3_REGION3_DSP_INFO

Address: Operational Base(0x27D01E00) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_height Dsp_height = vertical size - 1
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_width Dsp_width = horizontal size - 1

ESMART3_REGION3_DSP_OFFSET

Address: Operational Base(0x27D01E00) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_xoff Display image horizon offset in panel.

ESMART3_REGION3_SCL_CTRL

Address: Operational Base(0x27D01E00) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	region3_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:8	RO	0x00	reserved
7:6	RW	0x0	region3_yrgb_yscl_mode When yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
5	RW	0x0	region3_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region3_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	region3_yrgb_xscl_mode When yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic Other: Reserved When yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear Other: Reserved
1	RW	0x0	region3_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region3_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

ESMART3_REGION3_SCL_FACTOR_YRGB

Address: Operational Base(0x27D01E00) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region3_yrgb_yfactor When yrgb_ysu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_ysd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.
15:0	RW	0x1000	region3_yrgb_xfactor When yrgb_xsu: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: Factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12

ESMART3_REGION3_SCL_OFFSET

Address: Operational Base(0x27D01E00) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region3_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region3_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

ESMART3_ESMART_KEY_CTRL

Address: Operational Base(0x27D01E00) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_key_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_key_value Esmart RED color key.
19:10	RW	0x000	esmart_g_key_value Esmart GREEN color key.
9:0	RW	0x000	esmart_b_key_value Esmart Blue color key.

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ESMART3_ESMART_BG_EN

Address: Operational Base(0x27D01E00) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_value Esmart background red color.
19:10	RW	0x000	esmart_g_value Esmart background green color.
9:0	RW	0x000	esmart_b_value Esmart background blue color.

ESMART3_ESMART_ALPHA_MAP

Address: Operational Base(0x27D01E00) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31	RW	0x0	alpha_map_en 1'b0: Disable 1'b1: Enable
30:16	RO	0x0000	reserved
15:8	RW	0x00	alpha_1_map When format = rgba5551, alpha value = 1'b1 mapping value.
7:0	RW	0x00	alpha_0_map When format = rgba5551, alpha value = 1'b0 mapping value.

ESMART3_ESMART_PORT_SEL_IMD

Address: Operational Base(0x27D01E00) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	esmart_port_sel 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 Other: Reserved

ESMART3_ESMART_DLY_NUM

Address: Operational Base(0x27D01E00) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x17	esmart_dly_num Esmart delay cycle number.

11.5.3.15 HDR_VIVID

HDR_VIVID_HDR_LUT_CTRL

Address: Operational Base(0x27D02000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	hdr_lut_mode 1'b0: Normal 1'b1: AXI HDR LUT
0	RW	0x0	hdr_lut_update_en 1'b0: Disable AXI HDR LUT update 1'b1: Enable AXI HDR LUT update

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HDR_VIVID_HDR_LUT_MST

Address: Operational Base(0x27D02000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hdr_lut_mst AXI HDR LUT address.

HDR_VIVID_HDR_LUT_STATUS

Address: Operational Base(0x27D02000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	hdr_lut_fetch_done When hdr_lut_fetch_done is 1'b1, lut fetch is done. DDR lut data can be updated. hdr_lut_fetch_done is self-clear when frame_start comes.

HDR_VIVID_SDR2HDR_CTRL

Address: Operational Base(0x27D02000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	sdr2hdr_dstmode 1'b0: ST2084 1'b1: HLG
2	RW	0x0	sdr2hdr_bypass_en 1'b1: SDR2HDR bypass mode 1'b0: Normal
1	RW	0x1	sdr2hdr_gating_en 1'b0: Disable gating 1'b1: Enable gating
0	RW	0x0	sdr2hdr_en 1'b0: Disable SDR2HDR 1'b1: Enable SDR2HDR

HDR_VIVID_SDR_CFG_COE0

Address: Operational Base(0x27D02000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sdr_r_fix S2H parameters, range is [-512,1024].
15:12	RO	0x0	reserved
11:0	RW	0x000	sdr_s_fix S2H parameters, range is [0,4080].

HDR_VIVID_SDR_CFG_COE1

Address: Operational Base(0x27D02000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sdr_t_fix S2H parameters, range is [0,9826].

HDR_VIVID_SDR_CSC_COE00_01

Address: Operational Base(0x27D02000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	coe01 S2H colormatrix convert parameters.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	coe00 S2H colormatrix convert parameters.

HDR_VIVID_SDR_CSC_COE02_10

Address: Operational Base(0x27D02000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	coe10 S2H colormatrix convert parameters.
15:14	RO	0x0	reserved
13:0	RW	0x0300	coe02 S2H colormatrix convert parameters.

HDR_VIVID_SDR_CSC_COE11_12

Address: Operational Base(0x27D02000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x3162	coe12 S2H colormatrix convert parameters.
15:14	RO	0x0	reserved
13:0	RW	0x01ee	coe11 S2H colormatrix convert parameters.

HDR_VIVID_SDR_CSC_COE20_21

Address: Operational Base(0x27D02000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	coe21 S2H colormatrix convert parameters.
15:14	RO	0x0	reserved
13:0	RW	0x2800	coe20 S2H colormatrix convert parameters.

HDR_VIVID_SDR_CSC_COE22

Address: Operational Base(0x27D02000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	coe22 S2H colormatrix convert parameters.

HDR_VIVID_HDRVIVID_CTRL

Address: Operational Base(0x27D02000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	sca_bypass_en 1'b0: SCA enable 1'b1: SCA disable
8	RW	0x0	pqmode_max_y 1'b0: Use RGB max 1'b1: Use calcY
7	RO	0x0	reserved
6	RW	0x0	dstgamut 1'b0: BT709 1'b1: BT2020

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Bit	Attr	Reset Value	Description
5:3	RW	0x0	path_mode HDRvivid mode 0~5 3'b000: Mode0 3'b001: Mode1 3'b010: Mode2 3'b011: Mode3 3'b100: Mode4 3'b101: Mode5
2	RW	0x0	hdrvivid_bypass_en 1'b1: HDR2SDR bypass mode 1'b0: Normal
1	RW	0x1	hdrvivid_gating_en 1'b0: Disable gating 1'b1: Enable gating
0	RW	0x0	hdrvivid_en 1'b0: Disable HDRvivid 1'b1: Enable HDRvivid

HDR_VIVID_HDR_PQ_GAMMA

Address: Operational Base(0x27D02000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	pq_gamma_k HDRvivid parameters.
15:8	RO	0x00	reserved
7:0	RW	0x00	pq_gamma_b HDRvivid parameters.

HDR_VIVID_HLG_RFIX_SCALEFAC

Address: Operational Base(0x27D02000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	scalefac HDRvivid parameters.
15:12	RO	0x0	reserved
11:0	RW	0x000	r_fix HDRvivid parameters.

HDR_VIVID_HLG_MAXLUMA

Address: Operational Base(0x27D02000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	maxsetluma HDRvivid parameters.
15:12	RO	0x0	reserved
11:0	RW	0x000	maxdstluma HDRvivid parameters.

HDR_VIVID_HLG_R_TM_LIN2NON

Address: Operational Base(0x27D02000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	r_tm_lin2non HDRvivid parameters.

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HDR_VIVID_HDR_CSC_COE00_01

Address: Operational Base(0x27D02000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	coe01 HDRvivid colormatrix convert parameters.
15:0	RW	0x0000	coe00 HDRvivid colormatrix convert parameters.

HDR_VIVID_HDR_CSC_COE02_10

Address: Operational Base(0x27D02000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	coe10 HDRvivid colormatrix convert parameters.
15:0	RW	0x0000	coe02 HDRvivid colormatrix convert parameters.

HDR_VIVID_HDR_CSC_COE11_12

Address: Operational Base(0x27D02000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	coe12 HDRvivid colormatrix convert parameters.
15:0	RW	0x0000	coe11 HDRvivid colormatrix convert parameters.

HDR_VIVID_HDR_CSC_COE20_21

Address: Operational Base(0x27D02000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	coe21 HDRvivid colormatrix convert parameters.
15:0	RW	0x0000	coe20 HDRvivid colormatrix convert parameters.

HDR_VIVID_HDR_CSC_COE22

Address: Operational Base(0x27D02000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	coe22 HDRvivid colormatrix convert parameters.

HDR_VIVID_HDR_TONE_SCA

Address: Operational Base(0x27D02000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	addr Addr: 0x013c ~ 0x053 Csca_y0[25:16] ,tm_y0[12:0]. Sca_y1[25:16] ,tm_y1[12:0]. Sca_y255[25:16] ,tm_y255[12:0]. Sca_y256[25:16] ,tm_y256[12:0].

HDR_VIVID_HDRGAMMA_CURVE

Address: Operational Base(0x27D02000) + offset (0x0540)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	addr Addr: 0x0540 ~ 0x0680 y1[29:16], y0[13:0], y3[29:16], y2[13:0] .. y159[29:16], y158[13:0], y160[13:0]

HDR_VIVID_HDRGAMMA_MDFVALUE

Address: Operational Base(0x27D02000) + offset (0x0690)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	addr Addr: 0x0690 - 0x06b0 y1[30:16], y0[14:0], y3[30:16], y2[14:0] .. y16[14:0]

HDR_VIVID_SDRINVGAMMA_CURVE

Address: Operational Base(0x27D02000) + offset (0x0700)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	addr 0x700 - 0x810 y1[28:16], y0[12:0], y3[28:16], y2[12:0] .. y135[28:16], y134[12:0], y136[12:0]

HDR_VIVID_SDRINVGAMMA_STARTIDX

Address: Operational Base(0x27D02000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	addr 0x820 - 0x834 y1[26:16], y0[10:0], y3[26:16], y2[10:0] .. y9[26:16], y8[10:0],y10[10:0]

HDR_VIVID_SDRINVGAMMA_CHANGEIDX

Address: Operational Base(0x27D02000) + offset (0x0840)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	addr 0x840 - 0x854 y1[25:16], y0[9:0], y3[25:16], y2[9:0] .. y9[25:16], y8[9:0], y10[9:0]

HDR_VIVID_SDR_SMGAIN

Address: Operational Base(0x27D02000) + offset (0x0900)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	addr Addr: 0x0900 ~ 0x09fc y1[26:16], y0[10:0], y3[26:16], y2[10:0] .. y127[26:16], y126[10:0]

11.5.3.16 ACM

ACM_ACM_CTRL

Address: Operational Base(0x27D06400) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	acm_height Active height.

Bit	Attr	Reset Value	Description
19:8	RW	0x000	acm_width Active width.
7	RO	0x0	reserved
6:4	RW	0x0	debug_data_sel 3'b000: YUV in data 3'b001: YUV2YHS data 3'b010: Interlation data 3'b011: YUV out data 3'b100: Csc_out 3'b101: Sharp_data 3'b1xx: Reserved
3	RO	0x0	reserved
2	RW	0x0	debug_en 1'b0: Disable 1'b1: Enable
1	RW	0x1	acm_bypass 1'b0: No bypass 1'b1: Bypass
0	RW	0x0	acm_en 1'b0: Disable 1'b1: Enable

ACM_DELTA_RANGE

Address: Operational Base(0x27D06400) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	s_gain Range of s_delta.
19:10	RW	0x000	h_gain Range of h_delta.
9:0	RW	0x000	y_gain Range of y_delta.

ACM_FETCH_START

Address: Operational Base(0x27D06400) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	fetch_start Start fetching lut data.

ACM_FETCH_DONE

Address: Operational Base(0x27D06400) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	fetch_done End of lut data fetching.

ACM_YHS_GAIN_BY_Y_SEG0

Address: Operational Base(0x27D06400) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	sgain_y_0 Value of 9x17LUT SgainByY.
15:8	RW	0x00	hgain_y_0 Value of 9x17LUT HgainByY.

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	ygain_y_0 Value of 9x17LUT YgainByY.

ACM_YHS_GAIN_BY_Y_SEG152

Address: Operational Base(0x27D06400) + offset (0x0360)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	sgain_y_152 Value of 9x17LUT SgainByY.
15:8	RW	0x00	hgain_y_152 Value of 9x17LUT HgainByY.
7:0	RW	0x00	ygain_y_152 Value of 9x17LUT YgainByY.

ACM_YHS_GAIN_BY_S_SEG0

Address: Operational Base(0x27D06400) + offset (0x0364)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	sgain_s_0 Value of 13x17LUT SgainByS.
15:8	RW	0x00	hgain_s_0 Value of 13x17LUT HgainByS.
7:0	RW	0x00	ygain_s_0 Value of 13x17LUT YgainByS.

ACM_YHS_GAIN_BY_S_SEG220

Address: Operational Base(0x27D06400) + offset (0x06D4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	sgain_s_220 Value of 13x17LUT SgainByS.
15:8	RW	0x00	hgain_s_220 Value of 13x17LUT HgainByS.
7:0	RW	0x00	ygain_s_220 Value of 13x17LUT YgainByS.

ACM_YHS_DEL_BY_H_SEG0

Address: Operational Base(0x27D06400) + offset (0x06D8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sdel_h_0 Value of 1x65LUT SDeltaByH.
19:12	RW	0x00	hdel_h_0 Value of 1x65LUT HDeltaByH.
11:10	RO	0x0	reserved
9:0	RW	0x000	ydel_h_0 Value of 1x65LUT YDeltaByH.

ACM_YHS_DEL_BY_H_SEG64

Address: Operational Base(0x27D06400) + offset (0x07D8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sdel_h_64 Value of 1x65LUT SDeltaByH.

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Bit	Attr	Reset Value	Description
19:12	RW	0x00	hdel_h_64 Value of 1x65LUT HDeltaByH.
11:10	RO	0x0	reserved
9:0	RW	0x000	ydel_h_64 Value of 1x65LUT YDeltaByH.

11.5.3.17 SHARP

SHARP_CTRL

Address: Operational Base(0x27D06C00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
12	RW	0x0	sw_ink_enable Ink module enable bit. 1'b1: Enable 1'b0: Disable
11	RO	0x0	reserved
10	RW	0x0	sw_texture_adj_enable Texture_adj module enable bit, protect flat area. 1'b1: Enable 1'b0: Disable
9	RW	0x0	sw_color_adj_enable Color_adj module enable bit, adjust high frequency by chromaticity component. 1'b1: Enable 1'b0: Disable
8	RW	0x0	sw_gain_ctrl_enable Gain_ctrl module enable bit, adjust high frequency by luma, variance and gradient. 1'b1: Enable 1'b0: Disable
7	RW	0x0	sw_shoot_ctrl_enable Shoot ctrl module enable bit, suppress overshoot and undershoot generate by sharp. 1'b1: Enable 1'b0: Disable
6	RW	0x0	sw_edge_proc_enable Peaking edge process module enable bit. 1'b1: Enable 1'b0: Disable
5	RW	0x0	sw_peaking_shoot_ctrl_enable Shoot ctrl module in peaking enable bit, suppress overshoot and undershoot generate by peaking's bands. 1'b1: Enable 1'b0: Disable
4	RW	0x0	sw_peaking_ctrl_enable Peaking ctrl process enable bit. 1'b1: Enable 1'b0: Disable
3	RW	0x0	sw_peaking_enable Peaking module enable bit. 1'b1: Enable 1'b0: Disable

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Bit	Attr	Reset Value	Description
2	RW	0x0	sw_cti_enable Cti module enable bit. 1'b1: Enable 1'b0: Disable
1	RW	0x0	sw_lti_enable Lti module enable bit. 1'b1: Enable 1'b0: Disable
0	RW	0x0	sw_sharp_enable Sharp module enable bit. 1'b1: Enable 1'b0: Disable

SHARP_AUTO_GATING_IMD

Address: Operational Base(0x27D06C00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x1	sw_texture_adj_gating_en 1'b1: Enable 1'b0: Disable
9	RW	0x1	sw_color_adj_gating_en 1'b1: Enable 1'b0: Disable
8	RW	0x1	sw_gain_ctrl_gating_en 1'b1: Enable 1'b0: Disable
7	RW	0x1	sw_shoot_ctrl_gating_en 1'b1: Enable 1'b0: Disable
6	RW	0x1	sw_edge_proc_gating_en 1'b1: Enable 1'b0: Disable
5	RW	0x1	sw_peaking_shoot_ctrl_gating_en 1'b1: Enable 1'b0: Disable
4	RW	0x1	sw_peaking_ctrl_gating_en 1'b1: Enable 1'b0: Disable
3	RW	0x1	sw_peaking_gating_en 1'b1: Enable 1'b0: Disable
2	RW	0x1	sw_cti_gating_en 1'b1: Enable 1'b0: Disable
1	RW	0x1	sw_lti_gating_en 1'b1: Enable 1'b0: Disable
0	RO	0x0	reserved

SHARP_PEAKING_FILTER_COE0

Address: Operational Base(0x27D06C00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x0	sw_peaking_v12 Peaking ver-direct filter1 coef2.

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Bit	Attr	Reset Value	Description
19:16	RW	0x0	sw_peaking_v11 Peaking ver-direct filter1 coef1.
15:12	RW	0x0	sw_peaking_v10 Peaking ver-direct filter1 coef0.
11:8	RW	0x0	sw_peaking_v02 Peaking ver-direct filter0 coef2.
7:4	RW	0x0	sw_peaking_v01 Peaking ver-direct filter0 coef1.
3:0	RW	0x0	sw_peaking_v00 Peaking ver-direct filter0 coef0.

SHARP_PEAKING_FILTER_COE1

Address: Operational Base(0x27D06C00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	sw_diag_coef Peaking diagonal filter core ctrl coef.
23:20	RW	0x0	sw_peaking_usm2 Peaking non-direct filter coef2.
19:16	RW	0x0	sw_peaking_usm1 Peaking non-direct filter coef1.
15:12	RW	0x0	sw_peaking_usm0 Peaking non-direct filter coef0.
11:8	RW	0x0	sw_peaking_v22 Peaking ver-direct filter2 coef2.
7:4	RW	0x0	sw_peaking_v21 Peaking ver-direct filter2 coef1.
3:0	RW	0x0	sw_peaking_v20 Peaking ver-direct filter2 coef0.

SHARP_PEAKING_FILTER_COE2

Address: Operational Base(0x27D06C00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking_h02 Peaking hor-direct filter0 coef2.
15	RO	0x0	reserved
14:8	RW	0x00	sw_peaking_h01 Peaking hor-direct filter0 coef1.
7:5	RO	0x0	reserved
4:0	RW	0x00	sw_peaking_h00 Peaking hor-direct filter0 coef0.

SHARP_PEAKING_FILTER_COE3

Address: Operational Base(0x27D06C00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:21	RW	0x000	sw_peaking_h05 Peaking hor-direct filter0 coef5.
20:10	RW	0x000	sw_peaking_h04 Peaking hor-direct filter0 coef4.
9:0	RW	0x000	sw_peaking_h03 Peaking hor-direct filter0 coef3.

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SHARP_PEAKING_FILTER_COE4

Address: Operational Base(0x27D06C00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking_h12 Peaking hor-direct filter1 coef2.
15	RO	0x0	reserved
14:8	RW	0x00	sw_peaking_h11 Peaking hor-direct filter1 coef1.
7:5	RO	0x0	reserved
4:0	RW	0x00	sw_peaking_h10 Peaking hor-direct filter1 coef0.

SHARP_PEAKING_FILTER_COE5

Address: Operational Base(0x27D06C00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:21	RW	0x000	sw_peaking_h15 Peaking hor-direct filter1 coef5.
20:10	RW	0x000	sw_peaking_h14 Peaking hor-direct filter1 coef4.
9:0	RW	0x000	sw_peaking_h13 Peaking hor-direct filter1 coef3.

SHARP_PEAKING_FILTER_COE6

Address: Operational Base(0x27D06C00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking_h22 Peaking hor-direct filter2 coef2.
15	RO	0x0	reserved
14:8	RW	0x00	sw_peaking_h21 Peaking hor-direct filter2 coef1.
7:5	RO	0x0	reserved
4:0	RW	0x00	sw_peaking_h20 Peaking hor-direct filter2 coef0.

SHARP_PEAKING_FILTER_COE7

Address: Operational Base(0x27D06C00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:21	RW	0x000	sw_peaking_h25 Peaking hor-direct filter2 coef5.
20:10	RW	0x000	sw_peaking_h24 Peaking hor-direct filter2 coef4.
9:0	RW	0x000	sw_peaking_h23 Peaking hor-direct filter2 coef3.

SHARP_PEAKING_FILTER_COE8

Address: Operational Base(0x27D06C00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_peaking_h32 Peaking hor-direct filter3 coef2.
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:8	RW	0x00	sw_peaking_h31 Peaking hor-direct filter3 coef1.
7:5	RO	0x0	reserved
4:0	RW	0x00	sw_peaking_h30 Peaking hor-direct filter3 coef0.

SHARP_PEAKING_FILTER_COE9

Address: Operational Base(0x27D06C00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:21	RW	0x000	sw_peaking_h35 Peaking hor-direct filter3 coef5.
20:10	RW	0x000	sw_peaking_h34 Peaking hor-direct filter3 coef4.
9:0	RW	0x000	sw_peaking_h33 Peaking hor-direct filter3 coef3.

SHARP_PEAKING0_CTRL_COE0

Address: Operational Base(0x27D06C00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking0_idx_n1 Peaking_ctrl band0 negative half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking0_idx_n0 Peaking_ctrl band0 negative half axis ctrl point index0.

SHARP_PEAKING0_CTRL_COE1

Address: Operational Base(0x27D06C00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking0_idx_n3 Peaking_ctrl band0 negative half axis ctrl point index3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking0_idx_n2 Peaking_ctrl band0 negative half axis ctrl point index2.

SHARP_PEAKING0_CTRL_COE2

Address: Operational Base(0x27D06C00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking0_idx_p1 Peaking_ctrl band0 positive half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking0_idx_p0 Peaking_ctrl band0 positive half axis ctrl point index0.

SHARP_PEAKING0_CTRL_COE3

Address: Operational Base(0x27D06C00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking0_idx_p3 Peaking_ctrl band0 positive half axis ctrl point index3.
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x000	sw_peaking0_idx_p2 Peaking_ctrl band0 positive half axis ctrl point index2.

SHARP_PEAKING0_CTRL_COE4

Address: Operational Base(0x27D06C00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking0_value_n2 Peaking_ctrl band0 negative half axis ctrl point value2.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking0_value_n1 Peaking_ctrl band0 negative half axis ctrl point value1.

SHARP_PEAKING0_CTRL_COE5

Address: Operational Base(0x27D06C00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking0_value_p1 Peaking_ctrl band0 positive half axis ctrl point value1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking0_value_n3 Peaking_ctrl band0 negative half axis ctrl point value3.

SHARP_PEAKING0_CTRL_COE6

Address: Operational Base(0x27D06C00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking0_value_p3 Peaking_ctrl band0 positive half axis ctrl point value3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking0_value_p2 Peaking_ctrl band0 positive half axis ctrl point value2.

SHARP_PEAKING0_CTRL_COE7

Address: Operational Base(0x27D06C00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking0_ratio_n12 Peaking_ctrl band0 negative half axis slope12.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking0_ratio_n01 Peaking_ctrl band0 negative half axis slope01.

SHARP_PEAKING0_CTRL_COE8

Address: Operational Base(0x27D06C00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking0_ratio_p01 Peaking_ctrl band0 positive half axis slope01.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking0_ratio_n23 Peaking_ctrl band0 negative half axis slope23.

SHARP_PEAKING0_CTRL_COE9

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Address: Operational Base(0x27D06C00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_peaking0_shoot_delta_offset Peaking_ctrl band0 shoot ctrl delta offset.
23:12	RW	0x000	sw_peaking0_ratio_p23 Peaking_ctrl band0 positive half axis slope23.
11:0	RW	0x000	sw_peaking0_ratio_p12 Peaking_ctrl band0 positive half axis slope12.

SHARP_PEAKING0_CTRL_COE10

Address: Operational Base(0x27D06C00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_peaking0_shoot_alpha_under_unlimit Peaking_ctrl band0 shoot ctrl undershoot unlimit ctrl.
23	RO	0x0	reserved
22:16	RW	0x00	sw_peaking0_shoot_alpha_over_unlimit Peaking_ctrl band0 shoot ctrl overshoot unlimit ctrl.
15	RO	0x0	reserved
14:8	RW	0x00	sw_peaking0_shoot_alpha_under Peaking_ctrl band0 shoot ctrl undershoot ctrl.
7	RO	0x0	reserved
6:0	RW	0x00	sw_peaking0_shoot_alpha_over Peaking_ctrl band0 shoot ctrl overshoot ctrl.

SHARP_PEAKING1_CTRL_COE0

Address: Operational Base(0x27D06C00) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking1_idx_n1 Peaking_ctrl band1 negative half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking1_idx_n0 Peaking_ctrl band1 negative half axis ctrl point index0.

SHARP_PEAKING1_CTRL_COE1

Address: Operational Base(0x27D06C00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking1_idx_n3 Peaking_ctrl band1 negative half axis ctrl point index3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking1_idx_n2 Peaking_ctrl band1 negative half axis ctrl point index2.

SHARP_PEAKING1_CTRL_COE2

Address: Operational Base(0x27D06C00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking1_idx_p1 Peaking_ctrl band1 positive half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking1_idx_p0 Peaking_ctrl band1 positive half axis ctrl point index0.

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SHARP_PEAKING1_CTRL_COE3

Address: Operational Base(0x27D06C00) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking1_idx_p3 Peaking_ctrl band1 positive half axis ctrl point index3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking1_idx_p2 Peaking_ctrl band1 positive half axis ctrl point index2.

SHARP_PEAKING1_CTRL_COE4

Address: Operational Base(0x27D06C00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking1_value_n2 Peaking_ctrl band1 negative half axis ctrl point value2.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking1_value_n1 Peaking_ctrl band1 negative half axis ctrl point value1.

SHARP_PEAKING1_CTRL_COE5

Address: Operational Base(0x27D06C00) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking1_value_p1 Peaking_ctrl band1 positive half axis ctrl point value1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking1_value_n3 Peaking_ctrl band1 negative half axis ctrl point value3.

SHARP_PEAKING1_CTRL_COE6

Address: Operational Base(0x27D06C00) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking1_value_p3 Peaking_ctrl band1 positive half axis ctrl point value3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking1_value_p2 Peaking_ctrl band1 positive half axis ctrl point value2.

SHARP_PEAKING1_CTRL_COE7

Address: Operational Base(0x27D06C00) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking1_ratio_n12 Peaking_ctrl band1 negative half axis slope12.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking1_ratio_n01 Peaking_ctrl band1 negative half axis slope01.

SHARP_PEAKING1_CTRL_COE8

Address: Operational Base(0x27D06C00) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x000	sw_peaking1_ratio_p01 Peaking_ctrl band1 positive half axis slope01.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking1_ratio_n23 Peaking_ctrl band1 negative half axis slope23.

SHARP_PEAKING1_CTRL_COE9

Address: Operational Base(0x27D06C00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_peaking1_shoot_delta_offset Peaking_ctrl band1 shoot ctrl delta offset.
23:12	RW	0x000	sw_peaking1_ratio_p23 Peaking_ctrl band1 positive half axis slope23.
11:0	RW	0x000	sw_peaking1_ratio_p12 Peaking_ctrl band1 positive half axis slope12.

SHARP_PEAKING1_CTRL_COE10

Address: Operational Base(0x27D06C00) + offset (0x0084)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_peaking1_shoot_alpha_under_unlimit Peaking_ctrl band1 shoot ctrl undershoot unlimit ctrl.
23	RO	0x0	reserved
22:16	RW	0x00	sw_peaking1_shoot_alpha_over_unlimit Peaking_ctrl band1 shoot ctrl overshoot unlimit ctrl.
15	RO	0x0	reserved
14:8	RW	0x00	sw_peaking1_shoot_alpha_under Peaking_ctrl band1 shoot ctrl undershoot ctrl.
7	RO	0x0	reserved
6:0	RW	0x00	sw_peaking1_shoot_alpha_over Peaking_ctrl band1 shoot ctrl overshoot ctrl.

SHARP_PEAKING2_CTRL_COE0

Address: Operational Base(0x27D06C00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking2_idx_n1 Peaking_ctrl band2 negative half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking2_idx_n0 Peaking_ctrl band2 negative half axis ctrl point index0.

SHARP_PEAKING2_CTRL_COE1

Address: Operational Base(0x27D06C00) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking2_idx_n3 Peaking_ctrl band2 negative half axis ctrl point index3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking2_idx_n2 Peaking_ctrl band2 negative half axis ctrl point index2.

SHARP_PEAKING2_CTRL_COE2

Address: Operational Base(0x27D06C00) + offset (0x0090)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking2_idx_p1 Peaking_ctrl band2 positive half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking2_idx_p0 Peaking_ctrl band2 positive half axis ctrl point index0.

SHARP_PEAKING2_CTRL_COE3

Address: Operational Base(0x27D06C00) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking2_idx_p3 Peaking_ctrl band2 positive half axis ctrl point index3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking2_idx_p2 Peaking_ctrl band2 positive half axis ctrl point index2.

SHARP_PEAKING2_CTRL_COE4

Address: Operational Base(0x27D06C00) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking2_value_n2 Peaking_ctrl band2 negative half axis ctrl point value2.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking2_value_n1 Peaking_ctrl band2 negative half axis ctrl point value1.

SHARP_PEAKING2_CTRL_COE5

Address: Operational Base(0x27D06C00) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking2_value_p1 Peaking_ctrl band2 positive half axis ctrl point value1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking2_value_n3 Peaking_ctrl band2 negative half axis ctrl point value3.

SHARP_PEAKING2_CTRL_COE6

Address: Operational Base(0x27D06C00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking2_value_p3 Peaking_ctrl band2 positive half axis ctrl point value3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking2_value_p2 Peaking_ctrl band2 positive half axis ctrl point value2.

SHARP_PEAKING2_CTRL_COE7

Address: Operational Base(0x27D06C00) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking2_ratio_n12 Peaking_ctrl band2 negative half axis slope12.
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	sw_peaking2_ratio_n01 Peaking_ctrl band2 negative half axis slope01.

SHARP_PEAKING2_CTRL_COE8

Address: Operational Base(0x27D06C00) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking2_ratio_p01 Peaking_ctrl band2 positive half axis slope01.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking2_ratio_n23 Peaking_ctrl band2 negative half axis slope23.

SHARP_PEAKING2_CTRL_COE9

Address: Operational Base(0x27D06C00) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_peaking2_shoot_delta_offset Peaking_ctrl band2 shoot ctrl delta offset.
23:12	RW	0x000	sw_peaking2_ratio_p23 Peaking_ctrl band2 positive half axis slope23.
11:0	RW	0x000	sw_peaking2_ratio_p12 Peaking_ctrl band2 positive half axis slope12.

SHARP_PEAKING2_CTRL_COE10

Address: Operational Base(0x27D06C00) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_peaking2_shoot_alpha_under_unlimit Peaking_ctrl band2 shoot ctrl undershoot unlimit ctrl.
23	RO	0x0	reserved
22:16	RW	0x00	sw_peaking2_shoot_alpha_over_unlimit Peaking_ctrl band2 shoot ctrl overshoot unlimit ctrl.
15	RO	0x0	reserved
14:8	RW	0x00	sw_peaking2_shoot_alpha_under Peaking_ctrl band2 shoot ctrl undershoot ctrl.
7	RO	0x0	reserved
6:0	RW	0x00	sw_peaking2_shoot_alpha_over Peaking_ctrl band2 shoot ctrl overshoot ctrl.

SHARP_PEAKING3_CTRL_COE0

Address: Operational Base(0x27D06C00) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking3_idx_n1 Peaking_ctrl band3 negative half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking3_idx_n0 Peaking_ctrl band3 negative half axis ctrl point index0.

SHARP_PEAKING3_CTRL_COE1

Address: Operational Base(0x27D06C00) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:16	RW	0x000	sw_peaking3_idx_n3 Peaking_ctrl band3 negative half axis ctrl point index3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking3_idx_n2 Peaking_ctrl band3 negative half axis ctrl point index2.

SHARP_PEAKING3_CTRL_COE2

Address: Operational Base(0x27D06C00) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking3_idx_p1 Peaking_ctrl band3 positive half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking3_idx_p0 Peaking_ctrl band3 positive half axis ctrl point index0.

SHARP_PEAKING3_CTRL_COE3

Address: Operational Base(0x27D06C00) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking3_idx_p3 Peaking_ctrl band3 positive half axis ctrl point index3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking3_idx_p2 Peaking_ctrl band3 positive half axis ctrl point index2.

SHARP_PEAKING3_CTRL_COE4

Address: Operational Base(0x27D06C00) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking3_value_n2 Peaking_ctrl band3 negative half axis ctrl point value2.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking3_value_n1 Peaking_ctrl band3 negative half axis ctrl point value1.

SHARP_PEAKING3_CTRL_COE5

Address: Operational Base(0x27D06C00) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking3_value_p1 Peaking_ctrl band3 positive half axis ctrl point value1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking3_value_n3 Peaking_ctrl band3 negative half axis ctrl point value3.

SHARP_PEAKING3_CTRL_COE6

Address: Operational Base(0x27D06C00) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking3_value_p3 Peaking_ctrl band3 positive half axis ctrl point value3.
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x000	sw_peaking3_value_p2 Peaking_ctrl band3 positive half axis ctrl point value2.

SHARP_PEAKING3_CTRL_COE7

Address: Operational Base(0x27D06C00) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking3_ratio_n12 Peaking_ctrl band3 negative half axis slope12.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking3_ratio_n01 Peaking_ctrl band3 negative half axis slope01.

SHARP_PEAKING3_CTRL_COE8

Address: Operational Base(0x27D06C00) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking3_ratio_p01 Peaking_ctrl band3 positive half axis slope01.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking3_ratio_n23 Peaking_ctrl band3 negative half axis slope23.

SHARP_PEAKING3_CTRL_COE9

Address: Operational Base(0x27D06C00) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_peaking3_shoot_delta_offset Peaking_ctrl band3 shoot ctrl delta offset.
23:12	RW	0x000	sw_peaking3_ratio_p23 Peaking_ctrl band3 positive half axis slope23.
11:0	RW	0x000	sw_peaking3_ratio_p12 Peaking_ctrl band3 positive half axis slope12.

SHARP_PEAKING3_CTRL_COE10

Address: Operational Base(0x27D06C00) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_peaking3_shoot_alpha_under_unlimit Peaking_ctrl band3 shoot ctrl undershoot unlimit ctrl.
23	RO	0x0	reserved
22:16	RW	0x00	sw_peaking3_shoot_alpha_over_unlimit Peaking_ctrl band3 shoot ctrl overshoot unlimit ctrl.
15	RO	0x0	reserved
14:8	RW	0x00	sw_peaking3_shoot_alpha_under Peaking_ctrl band3 shoot ctrl undershoot ctrl.
7	RO	0x0	reserved
6:0	RW	0x00	sw_peaking3_shoot_alpha_over Peaking_ctrl band3 shoot ctrl overshoot ctrl.

SHARP_PEAKING4_CTRL_COE0

Address: Operational Base(0x27D06C00) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:16	RW	0x000	sw_peaking4_idx_n1 Peaking_ctrl band4 negative half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking4_idx_n0 Peaking_ctrl band4 negative half axis ctrl point index0.

SHARP_PEAKING4_CTRL_COE1

Address: Operational Base(0x27D06C00) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking4_idx_n3 Peaking_ctrl band4 negative half axis ctrl point index3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking4_idx_n2 Peaking_ctrl band4 negative half axis ctrl point index2.

SHARP_PEAKING4_CTRL_COE2

Address: Operational Base(0x27D06C00) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking4_idx_p1 Peaking_ctrl band4 positive half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking4_idx_p0 Peaking_ctrl band4 positive half axis ctrl point index0.

SHARP_PEAKING4_CTRL_COE3

Address: Operational Base(0x27D06C00) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking4_idx_p3 Peaking_ctrl band4 positive half axis ctrl point index3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking4_idx_p2 Peaking_ctrl band4 positive half axis ctrl point index2.

SHARP_PEAKING4_CTRL_COE4

Address: Operational Base(0x27D06C00) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking4_value_n2 Peaking_ctrl band4 negative half axis ctrl point value2.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking4_value_n1 Peaking_ctrl band4 negative half axis ctrl point value1.

SHARP_PEAKING4_CTRL_COE5

Address: Operational Base(0x27D06C00) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking4_value_p1 Peaking_ctrl band4 positive half axis ctrl point value1.
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x000	sw_peaking4_value_n3 Peaking_ctrl band4 negative half axis ctrl point value3.

SHARP_PEAKING4_CTRL_COE6

Address: Operational Base(0x27D06C00) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking4_value_p3 Peaking_ctrl band4 positive half axis ctrl point value3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking4_value_p2 Peaking_ctrl band4 positive half axis ctrl point value2.

SHARP_PEAKING4_CTRL_COE7

Address: Operational Base(0x27D06C00) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking4_ratio_n12 Peaking_ctrl band4 negative half axis slope12.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking4_ratio_n01 Peaking_ctrl band4 negative half axis slope01.

SHARP_PEAKING4_CTRL_COE8

Address: Operational Base(0x27D06C00) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking4_ratio_p01 Peaking_ctrl band4 positive half axis slope01.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking4_ratio_n23 Peaking_ctrl band4 negative half axis slope23.

SHARP_PEAKING4_CTRL_COE9

Address: Operational Base(0x27D06C00) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_peaking4_shoot_delta_offset Peaking_ctrl band4 shoot ctrl delta offset.
23:12	RW	0x000	sw_peaking4_ratio_p23 Peaking_ctrl band4 positive half axis slope23.
11:0	RW	0x000	sw_peaking4_ratio_p12 Peaking_ctrl band4 positive half axis slope12.

SHARP_PEAKING4_CTRL_COE10

Address: Operational Base(0x27D06C00) + offset (0x0108)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_peaking4_shoot_alpha_under_unlimit Peaking_ctrl band4 shoot ctrl undershoot unlimit ctrl.
23	RO	0x0	reserved
22:16	RW	0x00	sw_peaking4_shoot_alpha_over_unlimit Peaking_ctrl band4 shoot ctrl overshoot unlimit ctrl.
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:8	RW	0x00	sw_peaking4_shoot_alpha_under Peaking_ctrl band4 shoot ctrl undershoot ctrl.
7	RO	0x0	reserved
6:0	RW	0x00	sw_peaking4_shoot_alpha_over Peaking_ctrl band4 shoot ctrl overshoot ctrl.

SHARP_PEAKING5_CTRL_COE0

Address: Operational Base(0x27D06C00) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking5_idx_n1 Peaking_ctrl band5 negative half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking5_idx_n0 Peaking_ctrl band5 negative half axis ctrl point index0.

SHARP_PEAKING5_CTRL_COE1

Address: Operational Base(0x27D06C00) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking5_idx_n3 Peaking_ctrl band5 negative half axis ctrl point index3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking5_idx_n2 Peaking_ctrl band5 negative half axis ctrl point index2.

SHARP_PEAKING5_CTRL_COE2

Address: Operational Base(0x27D06C00) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking5_idx_p1 Peaking_ctrl band5 positive half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking5_idx_p0 Peaking_ctrl band5 positive half axis ctrl point index0.

SHARP_PEAKING5_CTRL_COE3

Address: Operational Base(0x27D06C00) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking5_idx_p3 Peaking_ctrl band5 positive half axis ctrl point index3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking5_idx_p2 Peaking_ctrl band5 positive half axis ctrl point index2.

SHARP_PEAKING5_CTRL_COE4

Address: Operational Base(0x27D06C00) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking5_value_n2 Peaking_ctrl band5 negative half axis ctrl point value2.
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x000	sw_peaking5_value_n1 Peaking_ctrl band5 negative half axis ctrl point value1.

SHARP_PEAKING5_CTRL_COE5

Address: Operational Base(0x27D06C00) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking5_value_p1 Peaking_ctrl band5 positive half axis ctrl point value1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking5_value_n3 Peaking_ctrl band5 negative half axis ctrl point value3.

SHARP_PEAKING5_CTRL_COE6

Address: Operational Base(0x27D06C00) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking5_value_p3 Peaking_ctrl band5 positive half axis ctrl point value3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking5_value_p2 Peaking_ctrl band5 positive half axis ctrl point value2.

SHARP_PEAKING5_CTRL_COE7

Address: Operational Base(0x27D06C00) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking5_ratio_n12 Peaking_ctrl band5 negative half axis slope12.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking5_ratio_n01 Peaking_ctrl band5 negative half axis slope01.

SHARP_PEAKING5_CTRL_COE8

Address: Operational Base(0x27D06C00) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking5_ratio_p01 Peaking_ctrl band5 positive half axis slope01.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking5_ratio_n23 Peaking_ctrl band5 negative half axis slope23.

SHARP_PEAKING5_CTRL_COE9

Address: Operational Base(0x27D06C00) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_peaking5_shoot_delta_offset Peaking_ctrl band5 shoot ctrl delta offset.
23:12	RW	0x000	sw_peaking5_ratio_p23 Peaking_ctrl band5 positive half axis slope23.
11:0	RW	0x000	sw_peaking5_ratio_p12 Peaking_ctrl band5 positive half axis slope12.

SHARP_PEAKING5_CTRL_COE10

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Address: Operational Base(0x27D06C00) + offset (0x0134)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_peaking5_shoot_alpha_under_unlimit Peaking_ctrl band5 shoot ctrl undershoot unlimit ctrl.
23	RO	0x0	reserved
22:16	RW	0x00	sw_peaking5_shoot_alpha_over_unlimit Peaking_ctrl band5 shoot ctrl overshoot unlimit ctrl.
15	RO	0x0	reserved
14:8	RW	0x00	sw_peaking5_shoot_alpha_under Peaking_ctrl band5 shoot ctrl undershoot ctrl.
7	RO	0x0	reserved
6:0	RW	0x00	sw_peaking5_shoot_alpha_over Peaking_ctrl band5 shoot ctrl overshoot ctrl.

SHARP_PEAKING6_CTRL_COE0

Address: Operational Base(0x27D06C00) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking6_idx_n1 Peaking_ctrl band6 negative half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking6_idx_n0 Peaking_ctrl band6 negative half axis ctrl point index0.

SHARP_PEAKING6_CTRL_COE1

Address: Operational Base(0x27D06C00) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking6_idx_n3 Peaking_ctrl band6 negative half axis ctrl point index3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking6_idx_n2 Peaking_ctrl band6 negative half axis ctrl point index2.

SHARP_PEAKING6_CTRL_COE2

Address: Operational Base(0x27D06C00) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking6_idx_p1 Peaking_ctrl band6 positive half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking6_idx_p0 Peaking_ctrl band6 positive half axis ctrl point index0.

SHARP_PEAKING6_CTRL_COE3

Address: Operational Base(0x27D06C00) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking6_idx_p3 Peaking_ctrl band6 positive half axis ctrl point index3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking6_idx_p2 Peaking_ctrl band6 positive half axis ctrl point index2.

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SHARP_PEAKING6_CTRL_COE4

Address: Operational Base(0x27D06C00) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking6_value_n2 Peaking_ctrl band6 negative half axis ctrl point value2.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking6_value_n1 Peaking_ctrl band6 negative half axis ctrl point value1.

SHARP_PEAKING6_CTRL_COE5

Address: Operational Base(0x27D06C00) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking6_value_p1 Peaking_ctrl band6 positive half axis ctrl point value1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking6_value_n3 Peaking_ctrl band6 negative half axis ctrl point value3.

SHARP_PEAKING6_CTRL_COE6

Address: Operational Base(0x27D06C00) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking6_value_p3 Peaking_ctrl band6 positive half axis ctrl point value3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking6_value_p2 Peaking_ctrl band6 positive half axis ctrl point value2.

SHARP_PEAKING6_CTRL_COE7

Address: Operational Base(0x27D06C00) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking6_ratio_n12 Peaking_ctrl band6 negative half axis slope12.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking6_ratio_n01 Peaking_ctrl band6 negative half axis slope01.

SHARP_PEAKING6_CTRL_COE8

Address: Operational Base(0x27D06C00) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking6_ratio_p01 Peaking_ctrl band6 positive half axis slope01.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking6_ratio_n23 Peaking_ctrl band6 negative half axis slope23.

SHARP_PEAKING6_CTRL_COE9

Address: Operational Base(0x27D06C00) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_peaking6_shoot_delta_offset Peaking_ctrl band6 shoot ctrl delta offset.

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Bit	Attr	Reset Value	Description
23:12	RW	0x000	sw_peaking6_ratio_p23 Peaking_ctrl band6 positive half axis slope23.
11:0	RW	0x000	sw_peaking6_ratio_p12 Peaking_ctrl band6 positive half axis slope12.

SHARP_PEAKING6_CTRL_COE10

Address: Operational Base(0x27D06C00) + offset (0x0160)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_peaking6_shoot_alpha_under_unlimit Peaking_ctrl band6 shoot ctrl undershoot unlimit ctrl.
23	RO	0x0	reserved
22:16	RW	0x00	sw_peaking6_shoot_alpha_over_unlimit Peaking_ctrl band6 shoot ctrl overshoot unlimit ctrl.
15	RO	0x0	reserved
14:8	RW	0x00	sw_peaking6_shoot_alpha_under Peaking_ctrl band6 shoot ctrl undershoot ctrl.
7	RO	0x0	reserved
6:0	RW	0x00	sw_peaking6_shoot_alpha_over Peaking_ctrl band6 shoot ctrl overshoot ctrl.

SHARP_PEAKING7_CTRL_COE0

Address: Operational Base(0x27D06C00) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking7_idx_n1 Peaking_ctrl band7 negative half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking7_idx_n0 Peaking_ctrl band7 negative half axis ctrl point index0.

SHARP_PEAKING7_CTRL_COE1

Address: Operational Base(0x27D06C00) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking7_idx_n3 Peaking_ctrl band7 negative half axis ctrl point index3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking7_idx_n2 Peaking_ctrl band7 negative half axis ctrl point index2.

SHARP_PEAKING7_CTRL_COE2

Address: Operational Base(0x27D06C00) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking7_idx_p1 Peaking_ctrl band7 positive half axis ctrl point index1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking7_idx_p0 Peaking_ctrl band7 positive half axis ctrl point index0.

SHARP_PEAKING7_CTRL_COE3

Address: Operational Base(0x27D06C00) + offset (0x0170)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking7_idx_p3 Peaking_ctrl band7 positive half axis ctrl point index3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking7_idx_p2 Peaking_ctrl band7 positive half axis ctrl point index2.

SHARP_PEAKING7_CTRL_COE4

Address: Operational Base(0x27D06C00) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking7_value_n2 Peaking_ctrl band7 negative half axis ctrl point value2.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking7_value_n1 Peaking_ctrl band7 negative half axis ctrl point value1.

SHARP_PEAKING7_CTRL_COE5

Address: Operational Base(0x27D06C00) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking7_value_p1 Peaking_ctrl band7 positive half axis ctrl point value1.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking7_value_n3 Peaking_ctrl band7 negative half axis ctrl point value3.

SHARP_PEAKING7_CTRL_COE6

Address: Operational Base(0x27D06C00) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_peaking7_value_p3 Peaking_ctrl band7 positive half axis ctrl point value3.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_peaking7_value_p2 Peaking_ctrl band7 positive half axis ctrl point value2.

SHARP_PEAKING7_CTRL_COE7

Address: Operational Base(0x27D06C00) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking7_ratio_n12 Peaking_ctrl band7 negative half axis slope12.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_peaking7_ratio_n01 Peaking_ctrl band7 negative half axis slope01.

SHARP_PEAKING7_CTRL_COE8

Address: Operational Base(0x27D06C00) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_peaking7_ratio_p01 Peaking_ctrl band7 positive half axis slope01.
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	sw_peaking7_ratio_n23 Peaking_ctrl band7 negative half axis slope23.

SHARP_PEAKING7_CTRL_COE9

Address: Operational Base(0x27D06C00) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_peaking7_shoot_delta_offset Peaking_ctrl band7 shoot ctrl delta offset.
23:12	RW	0x000	sw_peaking7_ratio_p23 Peaking_ctrl band7 positive half axis slope23.
11:0	RW	0x000	sw_peaking7_ratio_p12 Peaking_ctrl band7 positive half axis slope12.

SHARP_PEAKING7_CTRL_COE10

Address: Operational Base(0x27D06C00) + offset (0x018C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_peaking7_shoot_alpha_under_unlimit Peaking_ctrl band7 shoot ctrl undershoot unlimit ctrl.
23	RO	0x0	reserved
22:16	RW	0x00	sw_peaking7_shoot_alpha_over_unlimit Peaking_ctrl band7 shoot ctrl overshoot unlimit ctrl.
15	RO	0x0	reserved
14:8	RW	0x00	sw_peaking7_shoot_alpha_under Peaking_ctrl band7 shoot ctrl undershoot ctrl.
7	RO	0x0	reserved
6:0	RW	0x00	sw_peaking7_shoot_alpha_over Peaking_ctrl band7 shoot ctrl overshoot ctrl.

SHARP_PEAKING_CTRL0

Address: Operational Base(0x27D06C00) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	sw_nondir_wgt_ratio Ratio for non-direct weight.
23:20	RW	0x0	sw_dir_cmp_ratio Ratio for direction judgment.
19	RO	0x0	reserved
18:12	RW	0x00	sw_nondir_thr Peaking-edge proc non-dir threshold.
11:10	RO	0x0	reserved
9:0	RW	0x000	sw_peaking_gain Peaking gain.

SHARP_PEAKING_CTRL1

Address: Operational Base(0x27D06C00) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:20	RW	0x00	sw_diag_dir_thr Threshold of diagonal direction.
19:16	RW	0x0	sw_dir_cnt_offset Offset of direction count.
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:12	RW	0x0	sw_dir_cnt_avg Setting average direction count.
11:8	RW	0x0	sw_dir_cnt_thr Threshold of direction count.
7:0	RW	0x00	sw_nondir_wgt_offset Offset for non-direct weight.

SHARP_PEAKING_CTRL2

Address: Operational Base(0x27D06C00) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_diag_adjgain_tab7 Diagonal adjust gain table idx7.
27:24	RW	0x0	sw_diag_adjgain_tab6 Diagonal adjust gain table idx6.
23:20	RW	0x0	sw_diag_adjgain_tab5 Diagonal adjust gain table idx5.
19:16	RW	0x0	sw_diag_adjgain_tab4 Diagonal adjust gain table idx4.
15:12	RW	0x0	sw_diag_adjgain_tab3 Diagonal adjust gain table idx3.
11:8	RW	0x0	sw_diag_adjgain_tab2 Diagonal adjust gain table idx2.
7:4	RW	0x0	sw_diag_adjgain_tab1 Diagonal adjust gain table idx1.
3:0	RW	0x0	sw_diag_adjgain_tab0 Diagonal adjust gain table idx0.

SHARP_PEAKING_CTRL3

Address: Operational Base(0x27D06C00) + offset (0x019C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_edge_alpha_under_unlimit_non Peaking-edge proc shoot ctrl undershoot unlimit ctrl for non-direct area.
23	RO	0x0	reserved
22:16	RW	0x00	sw_edge_alpha_over_unlimit_non Peaking-edge proc shoot ctrl overshoot unlimit ctrl for non-direct area.
15	RO	0x0	reserved
14:8	RW	0x00	sw_edge_alpha_under_non Peaking-edge proc shoot ctrl undershoot ctrl for non-direct area.
7	RO	0x0	reserved
6:0	RW	0x00	sw_edge_alpha_over_non Peaking-edge proc shoot ctrl overshoot ctrl for non-direct area.

SHARP_PEAKING_CTRL4

Address: Operational Base(0x27D06C00) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_edge_alpha_under_unlimit_v Peaking-edge proc shoot ctrl undershoot unlimit ctrl for ver-direct area.
23	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
22:16	RW	0x00	sw_edge_alpha_over_unlimit_v Peaking-edge proc shoot ctrl overshoot unlimit ctrl for ver-direct area.
15	RO	0x0	reserved
14:8	RW	0x00	sw_edge_alpha_under_v Peaking-edge proc shoot ctrl undershoot ctrl for ver-direct area.
7	RO	0x0	reserved
6:0	RW	0x00	sw_edge_alpha_over_v Peaking-edge proc shoot ctrl overshoot ctrl for ver-direct area.

SHARP_PEAKING_CTRL5

Address: Operational Base(0x27D06C00) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_edge_alpha_under_unlimit_h Peaking-edge proc shoot ctrl undershoot unlimit ctrl for hor-direct area.
23	RO	0x0	reserved
22:16	RW	0x00	sw_edge_alpha_over_unlimit_h Peaking-edge proc shoot ctrl overshoot unlimit ctrl for hor-direct area.
15	RO	0x0	reserved
14:8	RW	0x00	sw_edge_alpha_under_h Peaking-edge proc shoot ctrl undershoot ctrl for hor-direct area.
7	RO	0x0	reserved
6:0	RW	0x00	sw_edge_alpha_over_h Peaking-edge proc shoot ctrl overshoot ctrl for hor-direct area

SHARP_PEAKING_CTRL6

Address: Operational Base(0x27D06C00) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_edge_alpha_under_unlimit_d0 Peaking-edge proc shoot ctrl undershoot unlimit ctrl for diag0-direct area.
23	RO	0x0	reserved
22:16	RW	0x00	sw_edge_alpha_over_unlimit_d0 Peaking-edge proc shoot ctrl overshoot unlimit ctrl for diag0-direct area.
15	RO	0x0	reserved
14:8	RW	0x00	sw_edge_alpha_under_d0 Peaking-edge proc shoot ctrl undershoot ctrl for diag0-direct area.
7	RO	0x0	reserved
6:0	RW	0x00	sw_edge_alpha_over_d0 Peaking-edge proc shoot ctrl overshoot ctrl for diag0-direct area.

SHARP_PEAKING_CTRL7

Address: Operational Base(0x27D06C00) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_edge_alpha_under_unlimit_d1 Peaking-edge proc shoot ctrl undershoot unlimit ctrl for diag1-direct area.

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Bit	Attr	Reset Value	Description
23	RO	0x0	reserved
22:16	RW	0x00	sw_edge_alpha_over_unlimit_d1 Peaking-edge proc shoot ctrl overshoot unlimit ctrl for diag1-direct area.
15	RO	0x0	reserved
14:8	RW	0x00	sw_edge_alpha_under_d1 Peaking-edge proc shoot ctrl undershoot ctrl for diag1-direct area.
7	RO	0x0	reserved
6:0	RW	0x00	sw_edge_alpha_over_d1 Peaking-edge proc shoot ctrl overshoot ctrl for diag1-direct area.

SHARP_PEAKING_CTRL8

Address: Operational Base(0x27D06C00) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	sw_edge_delta_offset_h Peaking-edge proc hor-direct shoot ctrl delta offset.
15:8	RW	0x00	sw_edge_delta_offset_v Peaking-edge proc ver-direct shoot ctrl delta offset.
7:0	RW	0x00	sw_edge_delta_offset_non Peaking-edge proc non-direct shoot ctrl delta offset.

SHARP_PEAKING_CTRL9

Address: Operational Base(0x27D06C00) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	sw_edge_delta_offset_d1 Peaking-edge proc diag1-direct shoot ctrl delta offset.
7:0	RW	0x00	sw_edge_delta_offset_d0 Peaking-edge proc diag0-direct shoot ctrl delta offset.

SHARP_SHOOT_CTRL0

Address: Operational Base(0x27D06C00) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:20	RW	0x00	sw_shoot_alpha_under Shoot ctrl undershoot ctrl.
19	RO	0x0	reserved
18:12	RW	0x00	sw_shoot_alpha_over Shoot ctrl overshoot ctrl.
11:4	RW	0x00	sw_shoot_delta_offset Shoot ctrl delta offset.
3:1	RO	0x0	reserved
0	RW	0x0	sw_shoot_filt_radius Shoot ctrl max/min filter radius.

SHARP_SHOOT_CTRL1

Address: Operational Base(0x27D06C00) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x00	sw_shoot_alpha_under_unlimit Shoot ctrl undershoot unlimit ctrl.
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:0	RW	0x00	sw_shoot_alpha_over_unlimit Shoot ctrl overshoot unlimit ctrl.

SHARP_GAIN_CTRL0

Address: Operational Base(0x27D06C00) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_adp_idx2 Ctrl index2 for sharpness strength ctrl by gradient.
19:10	RW	0x000	sw_adp_idx1 Ctrl index1 for sharpness strength ctrl by gradient.
9:0	RW	0x000	sw_adp_idx0 Ctrl index0 for sharpness strength ctrl by gradient.

SHARP_GAIN_CTRL1

Address: Operational Base(0x27D06C00) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:20	RW	0x00	sw_adp_gain1 Ctrl gain1 for sharpness strength ctrl by gradient.
19	RO	0x0	reserved
18:12	RW	0x00	sw_adp_gain0 Ctrl gain0 for sharpness strength ctrl by gradient.
11:10	RO	0x0	reserved
9:0	RW	0x000	sw_adp_idx3 Ctrl index3 for sharpness strength ctrl by gradient.

SHARP_GAIN_CTRL2

Address: Operational Base(0x27D06C00) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x00	sw_adp_gain4 Ctrl gain4 for sharpness strength ctrl by gradient.
15	RO	0x0	reserved
14:8	RW	0x00	sw_adp_gain3 Ctrl gain3 for sharpness strength ctrl by gradient.
7	RO	0x0	reserved
6:0	RW	0x00	sw_adp_gain2 Ctrl gain2 for sharpness strength ctrl by gradient.

SHARP_GAIN_CTRL3

Address: Operational Base(0x27D06C00) + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:12	RW	0x000	sw_adp_slp12 Ctrl slope12 for sharpness strength ctrl by gradient.
11	RO	0x0	reserved
10:0	RW	0x000	sw_adp_slp01 Ctrl slope01 for sharpness strength ctrl by gradient.

SHARP_GAIN_CTRL4

Address: Operational Base(0x27D06C00) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:12	RW	0x000	sw_adp_slp34 Ctrl slope34 for sharpness strength ctrl by gradient.
11	RO	0x0	reserved
10:0	RW	0x000	sw_adp_slp23 Ctrl slope23 for sharpness strength ctrl by gradient.

SHARP_GAIN_CTRL5

Address: Operational Base(0x27D06C00) + offset (0x0204)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:21	RW	0x000	sw_var_idx1 Ctrl index1 for sharpness strength ctrl by gradient.
20:11	RW	0x000	sw_var_idx0 Ctrl index0 for sharpness strength ctrl by gradient.
10:0	RW	0x000	sw_adp_slp45 Ctrl slope45 for sharpness strength ctrl by gradient.

SHARP_GAIN_CTRL6

Address: Operational Base(0x27D06C00) + offset (0x0208)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_var_gain0 Ctrl gain0 for sharpness strength ctrl by gradient.
23:22	RO	0x0	reserved
21:12	RW	0x000	sw_var_idx3 Ctrl index3 for sharpness strength ctrl by gradient.
11:10	RO	0x0	reserved
9:0	RW	0x000	sw_var_idx2 Ctrl index2 for sharpness strength ctrl by gradient.

SHARP_GAIN_CTRL7

Address: Operational Base(0x27D06C00) + offset (0x020C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_var_gain4 Ctrl gain4 for sharpness strength ctrl by gradient.
23	RO	0x0	reserved
22:16	RW	0x00	sw_var_gain3 Ctrl gain3 for sharpness strength ctrl by gradient.
15	RO	0x0	reserved
14:8	RW	0x00	sw_var_gain2 Ctrl gain2 for sharpness strength ctrl by gradient.
7	RO	0x0	reserved
6:0	RW	0x00	sw_var_gain1 Ctrl gain1 for sharpness strength ctrl by gradient.

SHARP_GAIN_CTRL8

Address: Operational Base(0x27D06C00) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:12	RW	0x000	sw_var_slp12 Ctrl slope12 for sharpness strength ctrl by gradient.
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x000	sw_var_slp01 Ctrl slope01 for sharpness strength ctrl by gradient.

SHARP_GAIN_CTRL9

Address: Operational Base(0x27D06C00) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:12	RW	0x000	sw_var_slp34 Ctrl slope34 for sharpness strength ctrl by gradient.
11	RO	0x0	reserved
10:0	RW	0x000	sw_var_slp23 Ctrl slope23 for sharpness strength ctrl by gradient.

SHARP_GAIN_CTRL10

Address: Operational Base(0x27D06C00) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_lum_idx0 Ctrl index0 for sharpness strength ctrl by luma.
19:18	RO	0x0	reserved
17:16	RW	0x0	sw_lum_select Luma mode select. 2'b00: Yin 2'b01: Mean3x3 filt result 2'b10: Mean5x5 filt result
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_var_slp45 Ctrl slope45 for sharpness strength ctrl by gradient.

SHARP_GAIN_CTRL11

Address: Operational Base(0x27D06C00) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_lum_idx3 Ctrl index3 for sharpness strength ctrl by luma.
19:10	RW	0x000	sw_lum_idx2 Ctrl index2 for sharpness strength ctrl by luma.
9:0	RW	0x000	sw_lum_idx1 Ctrl index1 for sharpness strength ctrl by luma.

SHARP_GAIN_CTRL12

Address: Operational Base(0x27D06C00) + offset (0x0220)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_lum_gain3 Ctrl gain3 for sharpness strength ctrl by luma.
23	RO	0x0	reserved
22:16	RW	0x00	sw_lum_gain2 Ctrl gain2 for sharpness strength ctrl by luma.
15	RO	0x0	reserved
14:8	RW	0x00	sw_lum_gain1 Ctrl gain1 for sharpness strength ctrl by luma.
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:0	RW	0x00	sw_lum_gain0 Ctrl gain0 for sharpness strength ctrl by luma.

SHARP_GAIN_CTRL13

Address: Operational Base(0x27D06C00) + offset (0x0224)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:20	RW	0x000	sw_lum_slp12 Ctrl slope12 for sharpness strength ctrl by luma.
19	RO	0x0	reserved
18:8	RW	0x000	sw_lum_slp01 Ctrl slope01 for sharpness strength ctrl by luma.
7	RO	0x0	reserved
6:0	RW	0x00	sw_lum_gain4 Ctrl gain4 for sharpness strength ctrl by luma.

SHARP_GAIN_CTRL14

Address: Operational Base(0x27D06C00) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:12	RW	0x000	sw_lum_slp34 Ctrl slope34 for sharpness strength ctrl by luma.
11	RO	0x0	reserved
10:0	RW	0x000	sw_lum_slp23 Ctrl slope23 for sharpness strength ctrl by luma.

SHARP_GAIN_CTRL15

Address: Operational Base(0x27D06C00) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x000	sw_lum_slp45 Ctrl slope45 for sharpness strength ctrl by luma.

SHARP_COLORADJ_CTRL0

Address: Operational Base(0x27D06C00) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	sw_adj_scaling_coef0 Color adjust point0, gain_curve scaleing coef.
23:22	RO	0x0	reserved
21:12	RW	0x000	sw_adj_point_y0 Color adjust point0, v value.
11:10	RO	0x0	reserved
9:0	RW	0x000	sw_adj_point_x0 Color adjust point0, u value.

SHARP_COLORADJ_CTRL1

Address: Operational Base(0x27D06C00) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_coloradj_tab0_5 Color adjust point0, gain_curve_5.
24:20	RW	0x00	sw_coloradj_tab0_4 Color adjust point0, gain_curve_4.

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Bit	Attr	Reset Value	Description
19:15	RW	0x00	sw_coloradj_tab0_3 Color adjust point0, gain_curve_3.
14:10	RW	0x00	sw_coloradj_tab0_2 Color adjust point0, gain_curve_2.
9:5	RW	0x00	sw_coloradj_tab0_1 Color adjust point0, gain_curve_1.
4:0	RW	0x00	sw_coloradj_tab0_0 Color adjust point0, gain_curve_0.

SHARP_COLORADJ_CTRL2

Address: Operational Base(0x27D06C00) + offset (0x0238)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_coloradj_tab0_11 Color adjust point0, gain_curve_11.
24:20	RW	0x00	sw_coloradj_tab0_10 Color adjust point0, gain_curve_10.
19:15	RW	0x00	sw_coloradj_tab0_9 Color adjust point0, gain_curve_9.
14:10	RW	0x00	sw_coloradj_tab0_8 Color adjust point0, gain_curve_8.
9:5	RW	0x00	sw_coloradj_tab0_7 Color adjust point0, gain_curve_7.
4:0	RW	0x00	sw_coloradj_tab0_6 Color adjust point0, gain_curve_6.

SHARP_COLORADJ_CTRL3

Address: Operational Base(0x27D06C00) + offset (0x023C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x00	sw_coloradj_tab0_15 Color adjust point0, gain_curve_15.
14:10	RW	0x00	sw_coloradj_tab0_14 Color adjust point0, gain_curve_14.
9:5	RW	0x00	sw_coloradj_tab0_13 Color adjust point0, gain_curve_13.
4:0	RW	0x00	sw_coloradj_tab0_12 Color adjust point0, gain_curve_12.

SHARP_COLORADJ_CTRL4

Address: Operational Base(0x27D06C00) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	sw_adj_scaling_coef1 Color adjust point1, gain_curve scaleing coef.
23:22	RO	0x0	reserved
21:12	RW	0x000	sw_adj_point_y1 Color adjust point1, v value.
11:10	RO	0x0	reserved
9:0	RW	0x000	sw_adj_point_x1 Color adjust point1, u value.

SHARP_COLORADJ_CTRL5

Address: Operational Base(0x27D06C00) + offset (0x0244)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_coloradj_tab1_5 Color adjust point1, gain_curve_5.
24:20	RW	0x00	sw_coloradj_tab1_4 Color adjust point1, gain_curve_4.
19:15	RW	0x00	sw_coloradj_tab1_3 Color adjust point1, gain_curve_3.
14:10	RW	0x00	sw_coloradj_tab1_2 Color adjust point1, gain_curve_2.
9:5	RW	0x00	sw_coloradj_tab1_1 Color adjust point1, gain_curve_1.
4:0	RW	0x00	sw_coloradj_tab1_0 Color adjust point1, gain_curve_0.

SHARP_COLORADJ_CTRL6

Address: Operational Base(0x27D06C00) + offset (0x0248)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_coloradj_tab1_11 Color adjust point1, gain_curve_11.
24:20	RW	0x00	sw_coloradj_tab1_10 Color adjust point1, gain_curve_10.
19:15	RW	0x00	sw_coloradj_tab1_9 Color adjust point1, gain_curve_9.
14:10	RW	0x00	sw_coloradj_tab1_8 Color adjust point1, gain_curve_8.
9:5	RW	0x00	sw_coloradj_tab1_7 Color adjust point1, gain_curve_7.
4:0	RW	0x00	sw_coloradj_tab1_6 Color adjust point1, gain_curve_6.

SHARP_COLORADJ_CTRL7

Address: Operational Base(0x27D06C00) + offset (0x024C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x00	sw_coloradj_tab1_15 Color adjust point1, gain_curve_15.
14:10	RW	0x00	sw_coloradj_tab1_14 Color adjust point1, gain_curve_14.
9:5	RW	0x00	sw_coloradj_tab1_13 Color adjust point1, gain_curve_13.
4:0	RW	0x00	sw_coloradj_tab1_12 Color adjust point1, gain_curve_12.

SHARP_COLORADJ_CTRL8

Address: Operational Base(0x27D06C00) + offset (0x0250)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	sw_adj_scaling_coef2 Color adjust point2, gain_curve scaleing coef.
23:22	RO	0x0	reserved
21:12	RW	0x000	sw_adj_point_y2 Color adjust point2, v value.
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_adj_point_x2 Color adjust point2, u value.

SHARP_COLORADJ_CTRL9

Address: Operational Base(0x27D06C00) + offset (0x0254)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_coloradj_tab2_5 Color adjust point2, gain_curve_5.
24:20	RW	0x00	sw_coloradj_tab2_4 Color adjust point2, gain_curve_4.
19:15	RW	0x00	sw_coloradj_tab2_3 Color adjust point2, gain_curve_3.
14:10	RW	0x00	sw_coloradj_tab2_2 Color adjust point2, gain_curve_2.
9:5	RW	0x00	sw_coloradj_tab2_1 Color adjust point2, gain_curve_1.
4:0	RW	0x00	sw_coloradj_tab2_0 Color adjust point2, gain_curve_0.

SHARP_COLORADJ_CTRL10

Address: Operational Base(0x27D06C00) + offset (0x0258)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_coloradj_tab2_11 Color adjust point2, gain_curve_11.
24:20	RW	0x00	sw_coloradj_tab2_10 Color adjust point2, gain_curve_10.
19:15	RW	0x00	sw_coloradj_tab2_9 Color adjust point2, gain_curve_9.
14:10	RW	0x00	sw_coloradj_tab2_8 Color adjust point2, gain_curve_8.
9:5	RW	0x00	sw_coloradj_tab2_7 Color adjust point2, gain_curve_7.
4:0	RW	0x00	sw_coloradj_tab2_6 Color adjust point2, gain_curve_6.

SHARP_COLORADJ_CTRL11

Address: Operational Base(0x27D06C00) + offset (0x025C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x00	sw_coloradj_tab2_15 Color adjust point2, gain_curve_15.
14:10	RW	0x00	sw_coloradj_tab2_14 Color adjust point2, gain_curve_14.
9:5	RW	0x00	sw_coloradj_tab2_13 Color adjust point2, gain_curve_13.
4:0	RW	0x00	sw_coloradj_tab2_12 Color adjust point2, gain_curve_12.

SHARP_COLORADJ_CTRL12

Address: Operational Base(0x27D06C00) + offset (0x0260)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:24	RW	0x0	sw_adj_scaling_coef3 Color adjust point3, gain_curve scaleing coef.
23:22	RO	0x0	reserved
21:12	RW	0x000	sw_adj_point_y3 Color adjust point3, v value.
11:10	RO	0x0	reserved
9:0	RW	0x000	sw_adj_point_x3 Color adjust point3, u value.

SHARP_COLORADJ_CTRL13

Address: Operational Base(0x27D06C00) + offset (0x0264)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_coloradj_tab3_5 Color adjust point3, gain_curve_5.
24:20	RW	0x00	sw_coloradj_tab3_4 Color adjust point3, gain_curve_4.
19:15	RW	0x00	sw_coloradj_tab3_3 Color adjust point3, gain_curve_3.
14:10	RW	0x00	sw_coloradj_tab3_2 Color adjust point3, gain_curve_2.
9:5	RW	0x00	sw_coloradj_tab3_1 Color adjust point3, gain_curve_1.
4:0	RW	0x00	sw_coloradj_tab3_0 Color adjust point3, gain_curve_0.

SHARP_COLORADJ_CTRL14

Address: Operational Base(0x27D06C00) + offset (0x0268)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_coloradj_tab3_11 Color adjust point3, gain_curve_11.
24:20	RW	0x00	sw_coloradj_tab3_10 Color adjust point3, gain_curve_10.
19:15	RW	0x00	sw_coloradj_tab3_9 Color adjust point3, gain_curve_9.
14:10	RW	0x00	sw_coloradj_tab3_8 Color adjust point3, gain_curve_8.
9:5	RW	0x00	sw_coloradj_tab3_7 Color adjust point3, gain_curve_7.
4:0	RW	0x00	sw_coloradj_tab3_6 Color adjust point3, gain_curve_6.

SHARP_COLORADJ_CTRL15

Address: Operational Base(0x27D06C00) + offset (0x026C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x00	sw_coloradj_tab3_15 Color adjust point3, gain_curve_15.
14:10	RW	0x00	sw_coloradj_tab3_14 Color adjust point3, gain_curve_14.
9:5	RW	0x00	sw_coloradj_tab3_13 Color adjust point3, gain_curve_13.

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	sw_coloradj_tab3_12 Color adjust point3, gain_curve_12.

SHARP_TEXTURE_CTRL0

Address: Operational Base(0x27D06C00) + offset (0x0270)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_tex_idx1 Texture adjust index1.
15:14	RO	0x0	reserved
13:4	RW	0x000	sw_tex_idx0 Texture adjust index0.
3	RO	0x0	reserved
2:1	RW	0x0	sw_ymode_select Texture adjust result mode select. 2'b00: Sharp_result 2'b01: Y_ori 2'b10: Mean3x3 filt result 2'b11: Mean5x5 filt result
0	RW	0x0	sw_idxmode_select Texture adjust idx mode select. 1'b0: Direct_wgt 1'b1: Y_high_freq

SHARP_TEXTURE_CTRL1

Address: Operational Base(0x27D06C00) + offset (0x0274)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_tex_gain0 Texture adjust gain0.
23:22	RO	0x0	reserved
21:12	RW	0x000	sw_tex_idx3 Texture adjust index3.
11:10	RO	0x0	reserved
9:0	RW	0x000	sw_tex_idx2 Texture adjust index2.

SHARP_TEXTURE_CTRL2

Address: Operational Base(0x27D06C00) + offset (0x0278)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_tex_gain4 Texture adjust gain4.
23	RO	0x0	reserved
22:16	RW	0x00	sw_tex_gain3 Texture adjust gain3.
15	RO	0x0	reserved
14:8	RW	0x00	sw_tex_gain2 Texture adjust gain2.
7	RO	0x0	reserved
6:0	RW	0x00	sw_tex_gain1 Texture adjust gain1.

SHARP_TEXTURE_CTRL3

Address: Operational Base(0x27D06C00) + offset (0x027C)

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Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:12	RW	0x000	sw_tex_slp12 Texture adjust slope12.
11	RO	0x0	reserved
10:0	RW	0x000	sw_tex_slp01 Texture adjust slope01.

SHARP_TEXTURE_CTRL4

Address: Operational Base(0x27D06C00) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:12	RW	0x000	sw_tex_slp34 Texture adjust slope34.
11	RO	0x0	reserved
10:0	RW	0x000	sw_tex_slp23 Texture adjust slope23.

SHARP_TEXTURE_CTRL5

Address: Operational Base(0x27D06C00) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x000	sw_tex_slp45 Texture adjust slope45.

SHARP_LTI_CTRL0

Address: Operational Base(0x27D06C00) + offset (0x0288)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_ltih_thr1 Hor-direct lti gain threshold.
15:13	RO	0x0	reserved
12:4	RW	0x000	sw_ltih_slp1 Hor-direct lti gain slope.
3:1	RO	0x0	reserved
0	RW	0x0	sw_ltih_radius Hor-direct lti max/min filter radius. 1'b0: Radius = 3 1'b1: Radius = 5

SHARP_LTI_CTRL1

Address: Operational Base(0x27D06C00) + offset (0x028C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	sw_ltih_tigain Hor-direct lti gain.
23:22	RO	0x0	reserved
21:12	RW	0x000	sw_ltih_noisethrpos Hor-direct lti positive noise threshold.
11:10	RO	0x0	reserved
9:0	RW	0x000	sw_ltih_noisethrneg Hor-direct lti negative noise threshold.

SHARP_LTI_CTRL2

Address: Operational Base(0x27D06C00) + offset (0x0290)

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Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_ltiv_thr1 Ver-direct lti gain threshold.
15:13	RO	0x0	reserved
12:4	RW	0x000	sw_ltiv_slp1 Ver-direct lti gain slope.
3:1	RO	0x0	reserved
0	RW	0x0	sw_ltiv_radius Ver-direct lti max/min filter radius. 1'b0: Radius = 3 1'b1: Radius = 5

SHARP_LTI_CTRL3

Address: Operational Base(0x27D06C00) + offset (0x0294)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	sw_ltiv_tigain Ver-direct lti gain.
23:22	RO	0x0	reserved
21:12	RW	0x000	sw_ltiv_noisethrpos Ver-direct lti positive noise threshold.
11:10	RO	0x0	reserved
9:0	RW	0x000	sw_ltiv_noisethrneg Ver-direct lti negative noise threshold.

SHARP_CTI_CTRL0

Address: Operational Base(0x27D06C00) + offset (0x0298)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_ctih_thr1 Hor-direct cti gain threshold.
15:13	RO	0x0	reserved
12:4	RW	0x000	sw_ctih_slp1 Hor-direct cti gain slope.
3:1	RO	0x0	reserved
0	RW	0x0	sw_ctih_radius Hor-direct cti max/min filter radius. 1'b0: Radius = 3 1'b1: Radius = 5

SHARP_CTI_CTRL1

Address: Operational Base(0x27D06C00) + offset (0x029C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	sw_ctih_tigain Hor-direct cti gain.
23:22	RO	0x0	reserved
21:12	RW	0x000	sw_ctih_noisethrpos Hor-direct cti positive noise threshold.
11:10	RO	0x0	reserved
9:0	RW	0x000	sw_ctih_noisethrneg Hor-direct cti negative noise threshold.

SHARP_CTI_CTRL2

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Address: Operational Base(0x27D06C00) + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_ctiv_thr1 Ver-direct cti gain threshold.
15:13	RO	0x0	reserved
12:4	RW	0x000	sw_ctiv_slp1 Ver-direct cti gain slope.
3:1	RO	0x0	reserved
0	RW	0x0	sw_ctiv_radius Ver-direct cti max/min filter radius. 1'b0: Radius = 3 1'b1: Radius = 5

SHARP_CTI_CTRL3

Address: Operational Base(0x27D06C00) + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	sw_ctiv_tigain Ver-direct cti gain.
23:22	RO	0x0	reserved
21:12	RW	0x000	sw_ctiv_noisethrpos Ver-direct cti positive noise threshold.
11:10	RO	0x0	reserved
9:0	RW	0x000	sw_ctiv_noisethrneg Ver-direct cti negative noise threshold.

SHARP_DBG_CTRL0

Address: Operational Base(0x27D06C00) + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	sw_debug_mode Sharp debug data sel mode. 4'b0000: Src Y 4'b0001: Src UV 4'b0010: Lti result 4'b0011: Cti result(dst UV) 4'b0100: Peaking result 4'b0101: Shoot_ctrl result 4'b0110: Global_gain result 4'b0111: Color_adj result 4'b1000: Sharp result(dst Y) 4'b1001: Peaking_result hv 4'b1010: Peaking_result D0 D1 4'b1011: Peaking_result USM 4'b1100: Edge info 4'b1101: Y_add_direct and y_add_non_direct 4'b1110: Grad_sum and std_value 4'b1111: Mean3x3 and mean5x5_result

SHARP_ROI_CTRL0

Address: Operational Base(0x27D06C00) + offset (0x02AC)

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Bit	Attr	Reset Value	Description
31	RW	0x0	sw_roi_en Sharp roi_process enable. 1'b1: Enable 1'b0: Disable
30:28	RO	0x0	reserved
27:16	RW	0x000	sw_roi_ystart Sharp roi-area ver-direct start coordinates.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_roi_xstart Sharp roi-area hor-direct start coordinates.

SHARP_ROI_CTRL1

Address: Operational Base(0x27D06C00) + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_roi_yend Sharp roi-area ver-direct end coordinates.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_roi_xend Sharp roi-area hor-direct end coordinates.

11.5.3.18 MMU0

MMU0_MMU_DTE_ADDR

Address: Operational Base(0x27D07E00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dte_addr Current page table address.

MMU0_MMU_STATUS

Address: Operational Base(0x27D07E00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RW	0x00	page_fault_bus_id Index of master responsible for last page fault.
5	RW	0x0	page_fault_is_write The direction of access for last page fault. 1'b0: Read 1'b1: Write
4	RW	0x0	replay_buffer_empty The MMU replay buffer is empty.
3	RW	0x0	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RW	0x0	stail_active MMU stall mode currently enabled. The mode is enabled by command.
1	RW	0x0	page_fault_active MMU page fault mode currently enabled. The mode is enabled by command.
0	RW	0x0	paging_en Paging is enabled. 1'b0: Disable 1'b1: Enable

MMU0_MMU_COMMAND

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Address: Operational Base(0x27D07E00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	mmu_cmd 3'd0: MMU_ENABLE_PAGING 3'd1: MMU_DISABLE_PAGING 3'd2: MMU_ENABLE_STALL 3'd3: MMU_DISABLE_STALL 3'd4: MMU_ZAP_CACHE 3'd5: MMU_PAGE_FAULT_DONE 3'd6: MMU_FORCE_RESET Others: Reserved

MMU0_MMU_PAGE_FAULT_ADDR

Address: Operational Base(0x27D07E00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	page_fault_addr Address of last page fault.

MMU0_MMU_ZAP_ONE_LINE

Address: Operational Base(0x27D07E00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zap_one_line Address to be invalidated from the page table cache.

MMU0_MMU_INT_RAWSTAT

Address: Operational Base(0x27D07E00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rawst_bus_error Raw interrupt status of read bus error.
0	RW	0x0	rawst_page_fault Raw interrupt status of page fault.

MMU0_MMU_INT_CLEAR

Address: Operational Base(0x27D07E00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	clr_bus_error Clear interrupt of bus error.
0	RW	0x0	clr_page_fault Clear interrupt of page fault.

MMU0_MMU_INT_MASK

Address: Operational Base(0x27D07E00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	mask_bus_error Mask interrupt of bus error.
0	RW	0x0	mask_page_fault Mask interrupt of page fault.

MMU0_MMU_INT_STATUS

Address: Operational Base(0x27D07E00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	st_bus_error Interrupt status of bus error.
0	RW	0x0	st_page_fault Interrupt status of page fault.

MMU0_MMU_AUTO_GATING

Address: Operational Base(0x27D07E00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	mmu_cfg_mode 1'b0: Regdone when frame start 1'b1: Regdone immediately
0	RW	0x0	mmu_auto_gating When it is 1'b1, the mmu will auto gating it self.

11.5.3.19 MMU1

MMU1_MMU_DTE_ADDR

Address: Operational Base(0x27D07F00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dte_addr Current page table address.

MMU1_MMU_STATUS

Address: Operational Base(0x27D07F00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RW	0x00	page_fault_bus_id Index of master responsible for last page fault.
5	RW	0x0	page_fault_is_write The direction of access for last page fault. 1'b0: Read 1'b1: Write
4	RW	0x0	replay_buffer_empty The MMU replay buffer is empty.
3	RW	0x0	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RW	0x0	stail_active MMU stall mode currently enabled. The mode is enabled by command.
1	RW	0x0	page_fault_active MMU page fault mode currently enabled. The mode is enabled by command.
0	RW	0x0	paging_en Paging is enabled. 1'b0: Disable 1'b1: Enable

MMU1_MMU_COMMAND

Address: Operational Base(0x27D07F00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	mmu_cmd 3'd0: MMU_ENABLE_PAGING 3'd1: MMU_DISABLE_PAGING 3'd2: MMU_ENABLE_STALL 3'd3: MMU_DISABLE_STALL 3'd4: MMU_ZAP_CACHE 3'd5: MMU_PAGE_FAULT_DONE 3'd6: MMU_FORCE_RESET Others: Reserved

MMU1_MMU_PAGE_FAULT_ADDR

Address: Operational Base(0x27D07F00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	page_fault_addr Address of last page fault.

MMU1_MMU_ZAP_ONE_LINE

Address: Operational Base(0x27D07F00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zap_one_line Address to be invalidated from the page table cache.

MMU1_MMU_INT_RAWSTAT

Address: Operational Base(0x27D07F00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rawst_bus_error Raw interrupt status of read bus error.
0	RW	0x0	rawst_page_fault Raw interrupt status of page fault.

MMU1_MMU_INT_CLEAR

Address: Operational Base(0x27D07F00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	clr_bus_error Clear interrupt of bus error.
0	RW	0x0	clr_page_fault Clear interrupt of page fault.

MMU1_MMU_INT_MASK

Address: Operational Base(0x27D07F00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	mask_bus_error Mask interrupt of bus error.
0	RW	0x0	mask_page_fault Mask interrupt of page fault.

MMU1_MMU_INT_STATUS

Address: Operational Base(0x27D07F00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	st_bus_error Interrupt status of bus error.

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Bit	Attr	Reset Value	Description
0	RW	0x0	st_page_fault Interrupt status of page fault.

MMU1_MMU_AUTO_GATING

Address: Operational Base(0x27D07F00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	mmu_cfg_mode 1'b0: Regdone when frame start 1'b1: Regdone immediately
0	RW	0x0	mmu_auto_gating When it is 1'b1, the mmu will auto gating it self.

11.6 Application Notes

11.6.1 VOP Pixel Clock Configuration

- **dclk**: The clock source of the post-processing module and interface pixel clock, provided by the CRU module in the PD_VOP subsystem.
- **dclk_core**: The operating clock of the scanning timing of the post-processing module.
- **dclk_out**: Output interface operating clock.

11.6.1.1 eDP Interface Clock Frequency Requirements

Only edp interface is connected withzza post0, clk requires 2 frequencies.

edp_clk = post0_core_clk * 2

11.6.2 VOP POST FUNCTION

- Post_split: sharp and post split can not be used at the same time.
  Post_scale and post_split can not be used at the same time.
- Post_sharp: sharp and post split can not be used at the same time.
  Post_scale and post_sharp can not be used at the same time.
- Recommend enable VP0 axi0_urgency_en and set sw_urgency_thl=4, sw_urgency_thh=6.

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Chapter 12 EBC

12.1 Overview

EBC is the TCON module for E-ink Electronic Paper Display (EPD).

12.1.1 Features

- **System interface**
  - AHB slave for register configuration
  - AXI master for frame data transfer (DMA)
  - Interrupt output
- **EPD interface**
  - E-ink EPD compatible
  - Up to 2560x1920 resolution, 85fps
  - Up to 32 level gray scale
  - Up to 256 frames every scanning
  - LUT updateable (16KB)
  - Direct mode and LUT mode, THREE_WIN_MODE, EINK_mode
  - All-update mode and Diff-update mode
  - Single-phase and multi-phase mode
  - Support window display
  - Source driver interface
  - Gate driver interface
- **VOP_LITE interface**

EBC and VOP_LITE are mutually exclusive interfaces and can only be configured as one interface statically.

  - Parallel MCU/RGB LCD Interface: 24-bit(RGB888), 18-bit(RGB666), 16-bit(RGB565)
  - Serial MCU/RGB LCD Interface: 3x8-bit(RGB888), 3x6-bit(RGB666), 2x8-bit(RGB565)
  - BT.1120 Interface
  - BT.656 Interface
  - Max output resolution
    - 1920x1080
  - Win2 layer
    - RGB888, ARGB888, RGB565
    - Support virtual display
    - RGB2YUV(BT601/BT709)
  - Support dither down allegro RGB888to666 RGB888to565 and dither down FRC(Frame Rate Control) (configurable) RGB888to666
  - Blank and black display
  - Standby mode
  -

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12.2 Block Diagram

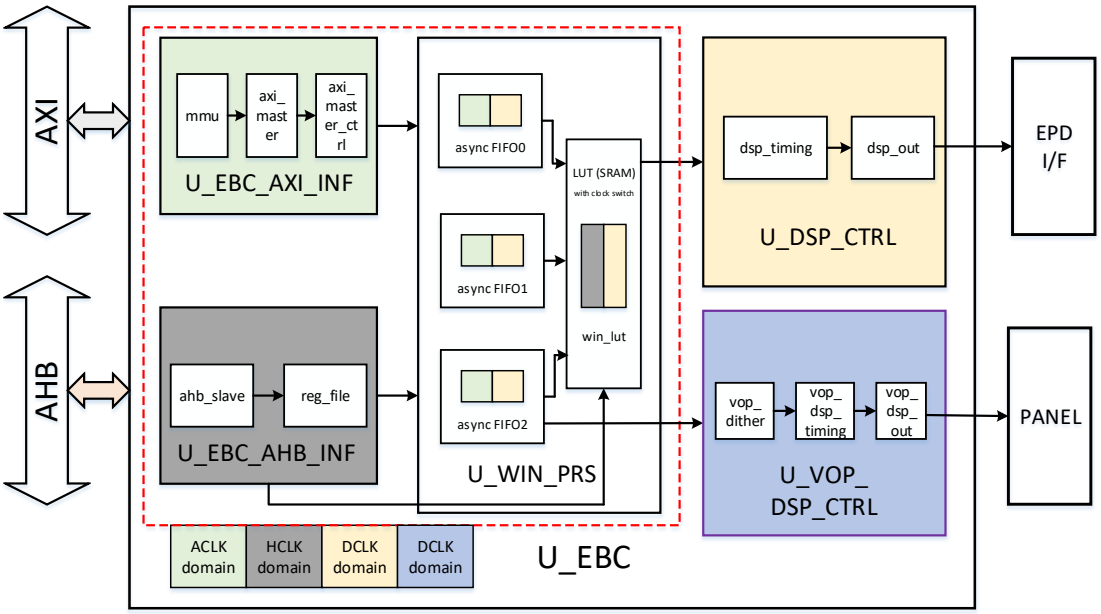


Fig. 12-1 EBC Block Diagram

12.3 Function Description

12.3.1 EBC Data Format

Table 12-1 EBC Input Data Format

DSP_LUT MODE	WIN_FMT [2:0]	Data format	Bit Map
0	xxx	S-data(2bpp)	{S3[7:0], S2[7:0], S1[7:0], S0[7:0]}
1	000	Y-data(4bpp)	{Y7[3:0], Y6[3:0], Y5[3:0], Y4[3:0], Y3[3:0], Y2[3:0], Y1[3:0], Y0[3:0]}
1	001	Y-data(8bpp)	{Y3[7:0], Y2[7:0], Y1[7:0], Y0[7:0]}
1	010	RGB565	{ R1[4:0], G1[5:0], B1[4:0], R0[4:0], G0[5:0], B0[4:0]}
1	011	XRGB8888	{8'bx, R[7:0], G[7:0], B[7:0]}
1	100	Y-data(5bpp)	{Y3[7:0], Y2[7:0], Y1[7:0], Y0[7:0]}

12.3.2 EBC Waveform generation mode

5. Direct mode

In direct scanning mode, the source data is just read by internal DMA and sent to the display output directly.

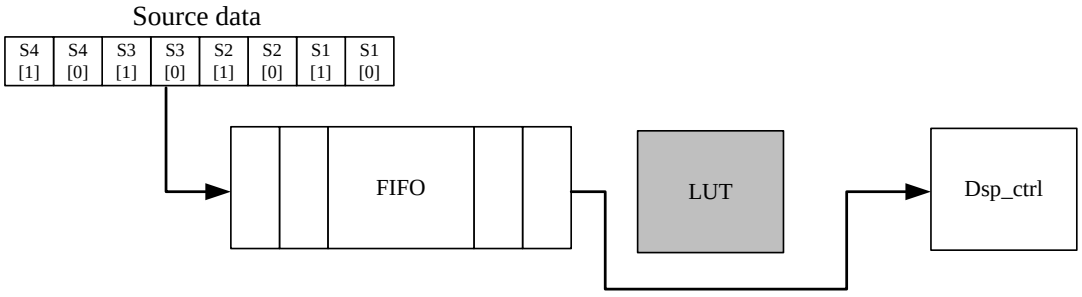


Fig. 12-2 EBC Block Diagram

6. LUT mode

In LUT scanning mode, internal DMA read the original pixel data into the FIFO, then the

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pixel data is sent to the look-up table to be translated the EPD source data.

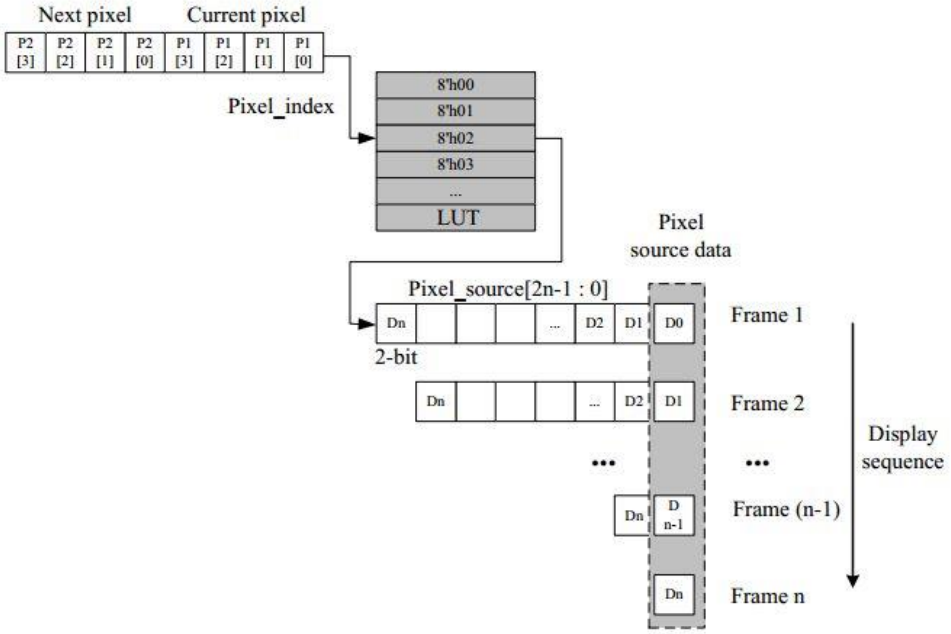


Fig. 12-3 LUT Mode Diagram

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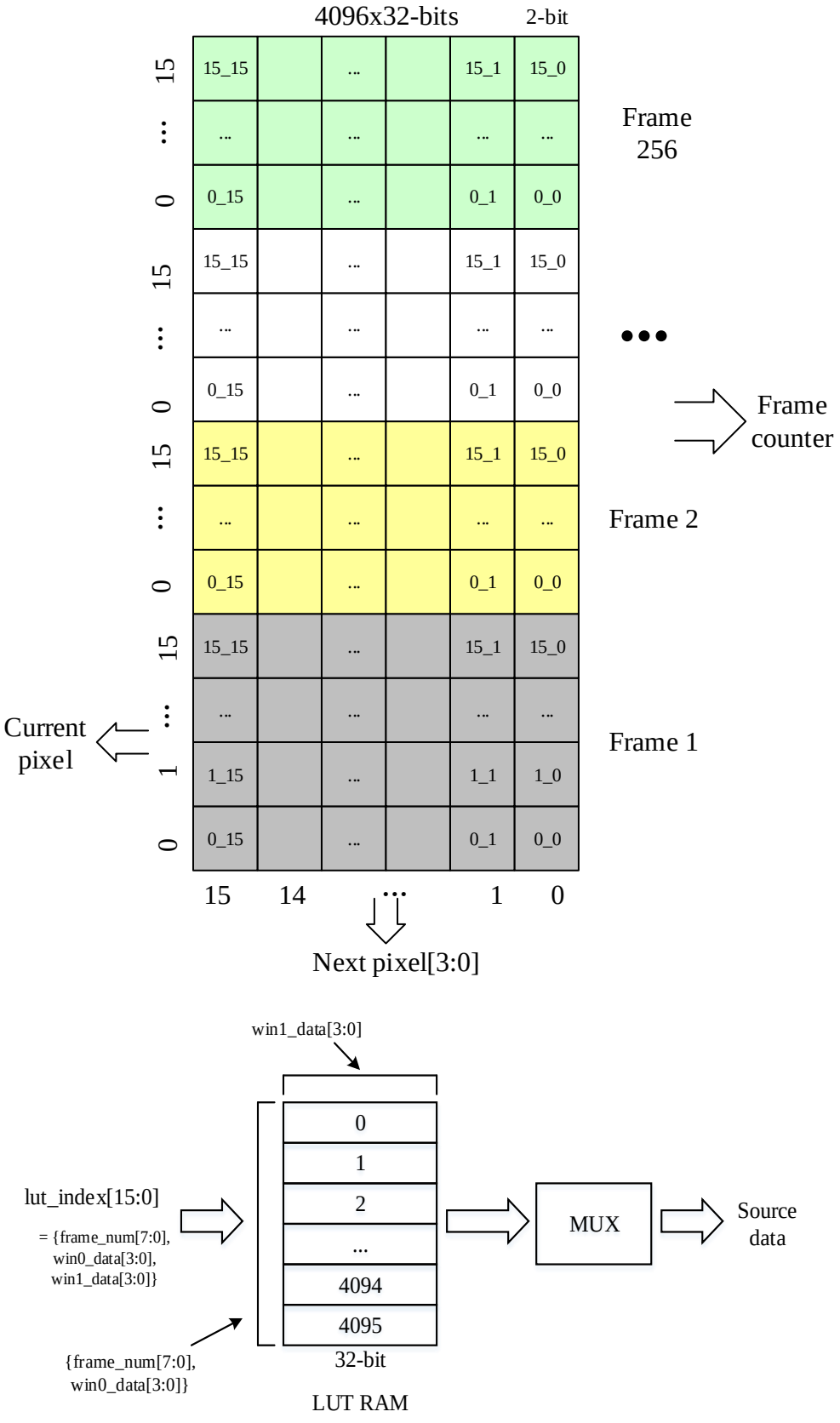


Fig. 12-4 EBC LUT Structure

7. 3win LUT mode

Compared with the LUT mode, in addition to the current image and the target image, the memory also contains frame number information. The frame number information in the

original LUT mode is counted by a counter, while the frame number information in 3win_mode is read from memory.

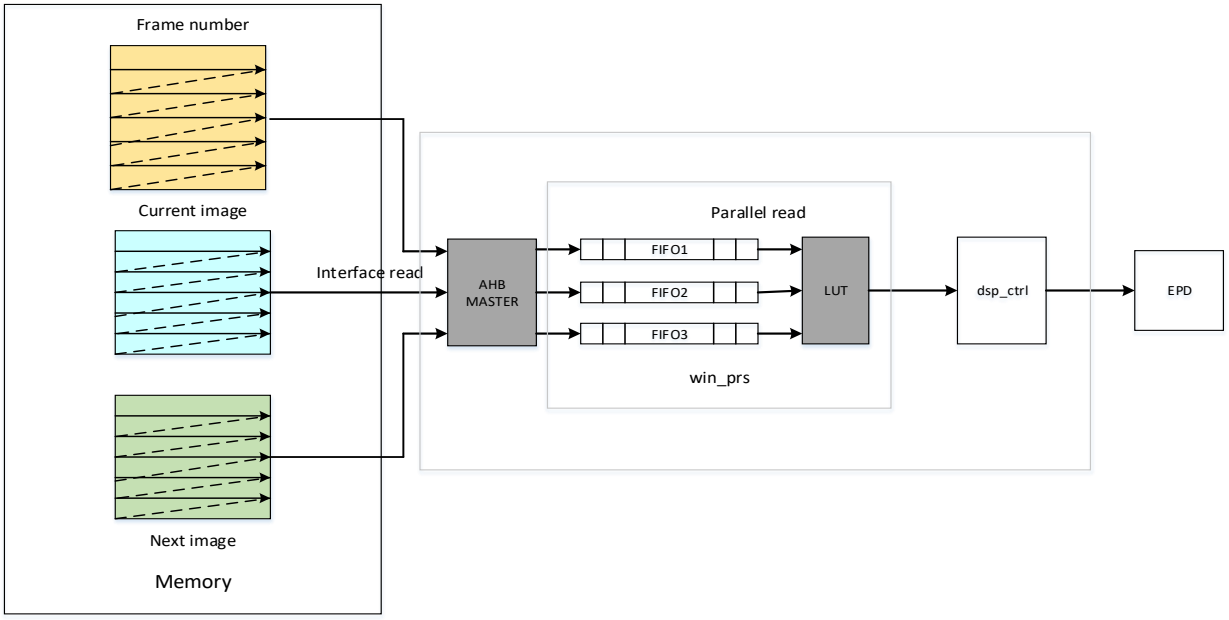


Fig. 12-5 EBC 3win Mode

12.3.3 EBC Window display mode

Window display is supported in EBC, dsp_win_width/dsp_win_height and dsp_win_st should be set to define the display window. The source value of other area is background value, which is configurable.

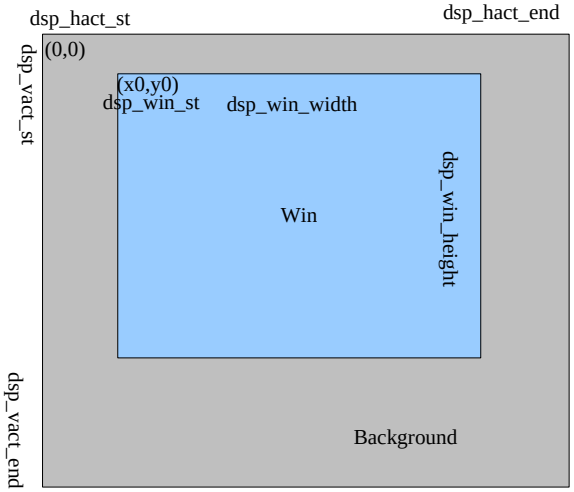


Fig. 12-6 EBC Window Display

12.3.4 EBC IO description

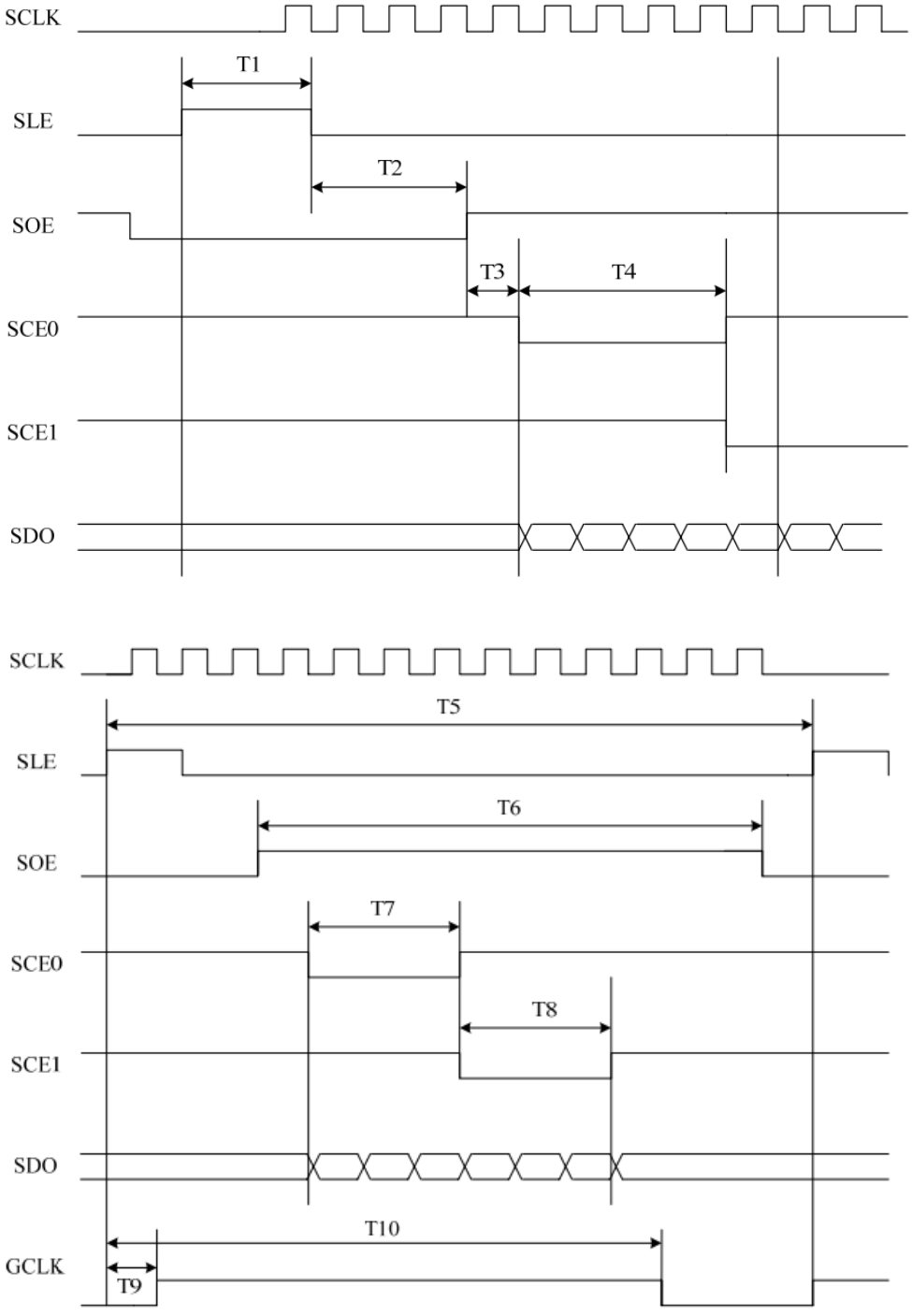
Table 12-2 EBC Output Pins

EBC	Description
ebc_sdclk	Source clock
ebc_sdle	Source latch data enable
ebc_sdoe	Source output enable
ebc_sdce[3:0]	Source chip select
ebc_sddo[15:0]	Source data output
ebc_sdshr	X scanning direction
ebc_gdclk	Gate clock
ebc_gdsp	Gate start pulse
ebc_gdoe	Gate output enable
ebc_vcom	COM voltage control
ebc_pwr[2:0]	POWER control

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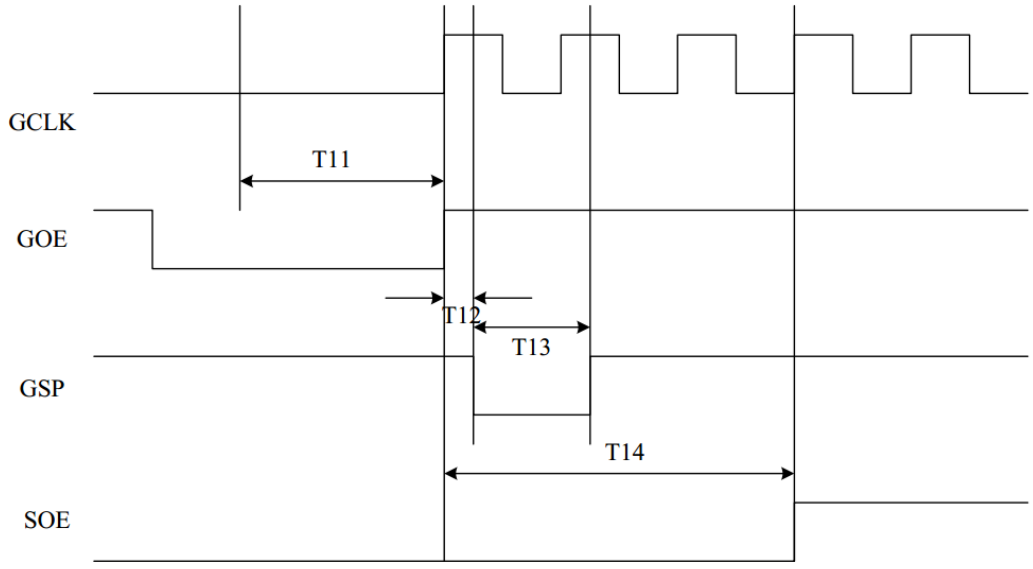
12.3.5 Eink EPD driver interface

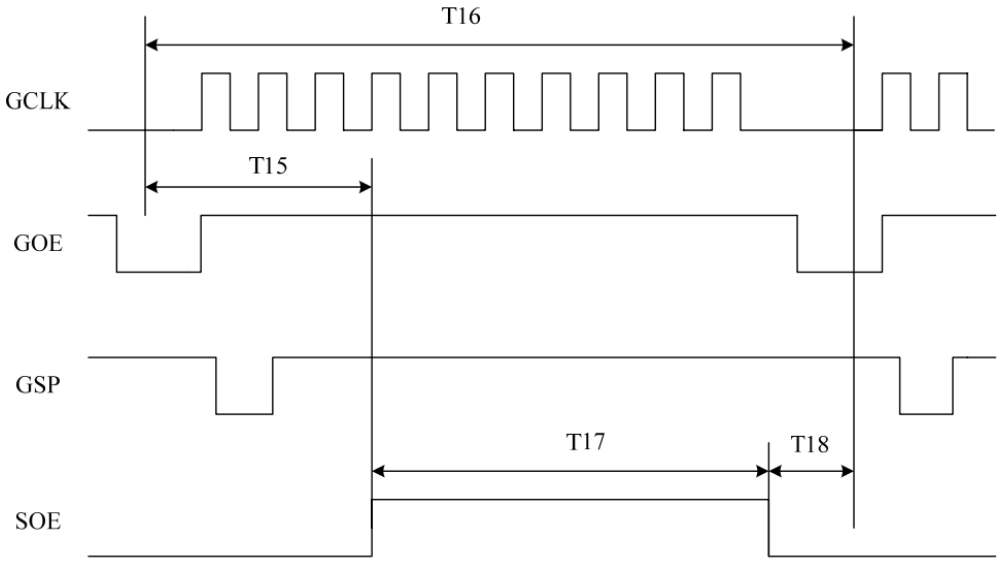
a. Source driver interface



Timing	Value （6-inch 800x600）	Register setting
DCLK	33.25MHz	
SCLK	4 DCLK(8.3125 MHz)	(DSP_CLK_DIV+1)
T1	10 SCLK	DSP_HS_END
T2	3 SCLK	(DSP_HACT_ST – DSP_HS_END)
T3	1 SCLK	Fixed
T1+T2+T3	14 SCLK	DSP_WIN_XST
T4	100 SCLK	DSP_SCE_WIDTH
T5	315 SCLK	DSP_HTOTAL
T6	300 SCLK	(DSP_HACT_END – DSP_HACT_ST)
T7	100 SCLK	DSP_SCE_WIDTH
T8	100 SCLK	DSP_SCE_WIDTH
T9	0 SCLK	DSP_GCLK_ST
T10	215 SCLK	DSP_GCLK_END

b. Gate driver interface





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Timing	Value (6-inch 800x600)	Register setting
GCLK	315 SCLK	DSP_HTOTAL
T11	4 GCLK	DSP_VS_END
T12	107 SCLK	(DSP_GD_END/2)
T13	1 GCLK	Fixed
T14	4 GCLK	(DSP_VACT_ST - DSP_VS_END)
T15	8 GCLK	DSP_VACT_ST
T16	619 GCLK	DSP_VTOTAL
T17	601 GCLK	(DSP_VACT_END - DSP_VACT_ST)
T18	11 GCLK	(DSP_VTOTAL - DSP_VACT_END)

12.3.6 VOP_LITE Data Format

VOP_LITE master read the frame data from the frame buffer in the system memory. There are total 3 formats supported in one layer.

Win2: RGB888, ARGB888, RGB565.

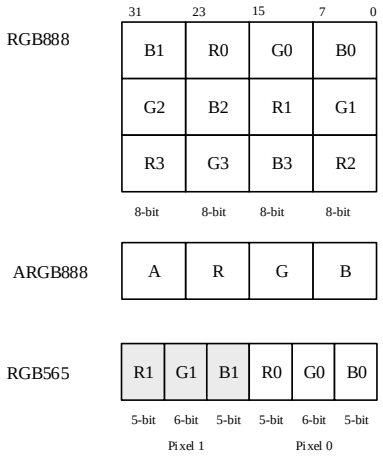


Fig. 12-7 VOP_LITE Frame Buffer Data Format

12.3.7 VOP_LITE Data Path

There is only one data input path which is internal DMA for VOP_LITE to get display layers' pixel data.

Internal DMA

Internal DMA can fetch the pixel data through AXI bus from system memory (DDR) for the display layers. Data fetching is driven by display output requirement.

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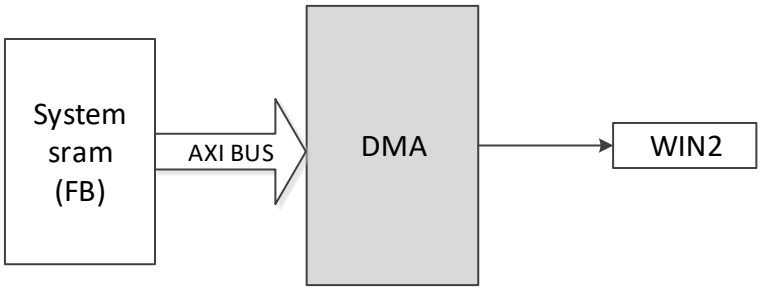


Fig. 12-8 VOP_LITE Internal DMA

12.3.8 VOP_LITE Virtual display

Virtual display is supported in Win2. The active image is part of the virtual (original) image in frame buffer memory. The virtual width is indicated by setting WIN2_VIR_STRIDE for different data format.

The virtual stride should be multiples of word (32-bit). That means dummy bytes in the end of virtual line if the real pixels are not 32-bit aligned.

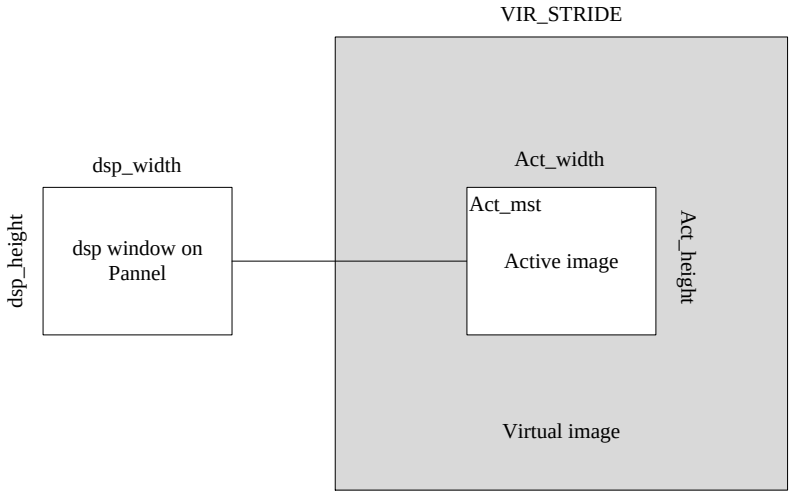


Fig. 12-9 VOP_LITE Virtual Display Mode

12.3.9 VOP_LITE Replication and dither down

1 Replication (dither up)

If the interface data bus is wider than the pixel format size, by programming the pixel components replication active/inactive, the MSB is replicated to the LSB of the interface data bus or the LSB is filled with 0s.

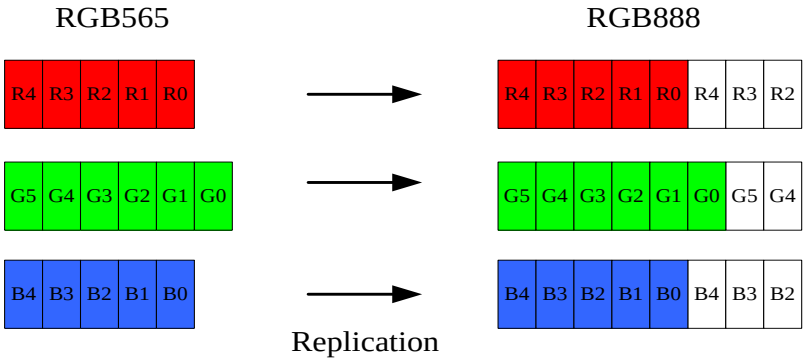


Fig. 12-10 VOP_LITE Replication

Dithering is used to improve the quality of display the pixel data in a lower color depth on the LCD panel. The Dithering algorithm is based on the (x, y) pixel position, the value of removed bits and frame counter.

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2 Dither down

Here we support three kinds of dithering arithmetic. RGB888 to RGB666 has two ways, one is allegro, the other is FRC. RGB888 to RGB565 has only one arithmetic, which is allegro. When Dithering is not enabled, the MSBs of the pixel color components are output on the interface data bus if the interface data bus is smaller than the pixel format size.

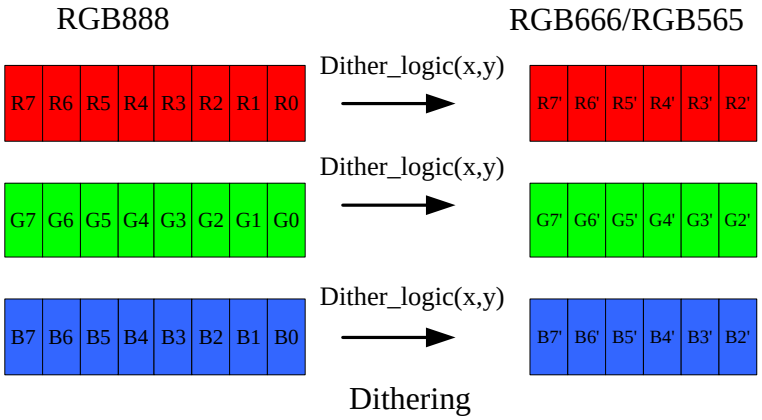
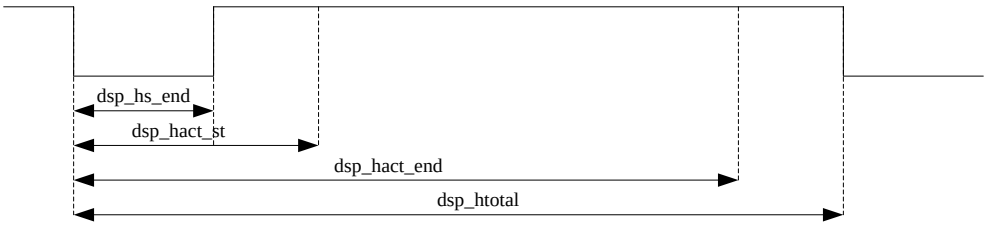


Fig. 12-11 VOP_LITE Dithering

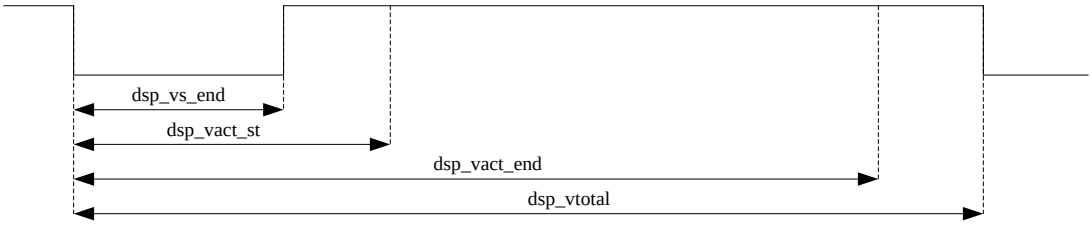
The following figure is the recommended pattern picture in VOP_LITE, you can configure different value of register 0x130~0x144，to change the pattern picture(default value is recommended values below).

12.3.10 VOP_LITE Timing Diagram

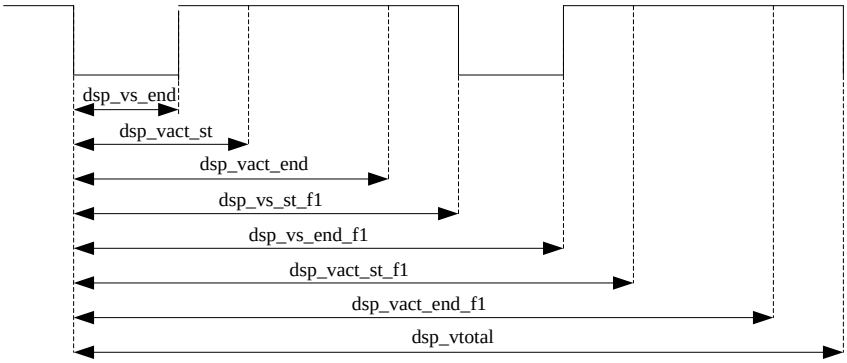
a. RGB Timing



Horizontal timing



Vertical timing(Progressive mode)



Vertical timing(Interlace mode)

Fig. 12-12 VOP_LITE RGB Interface Timing Setting

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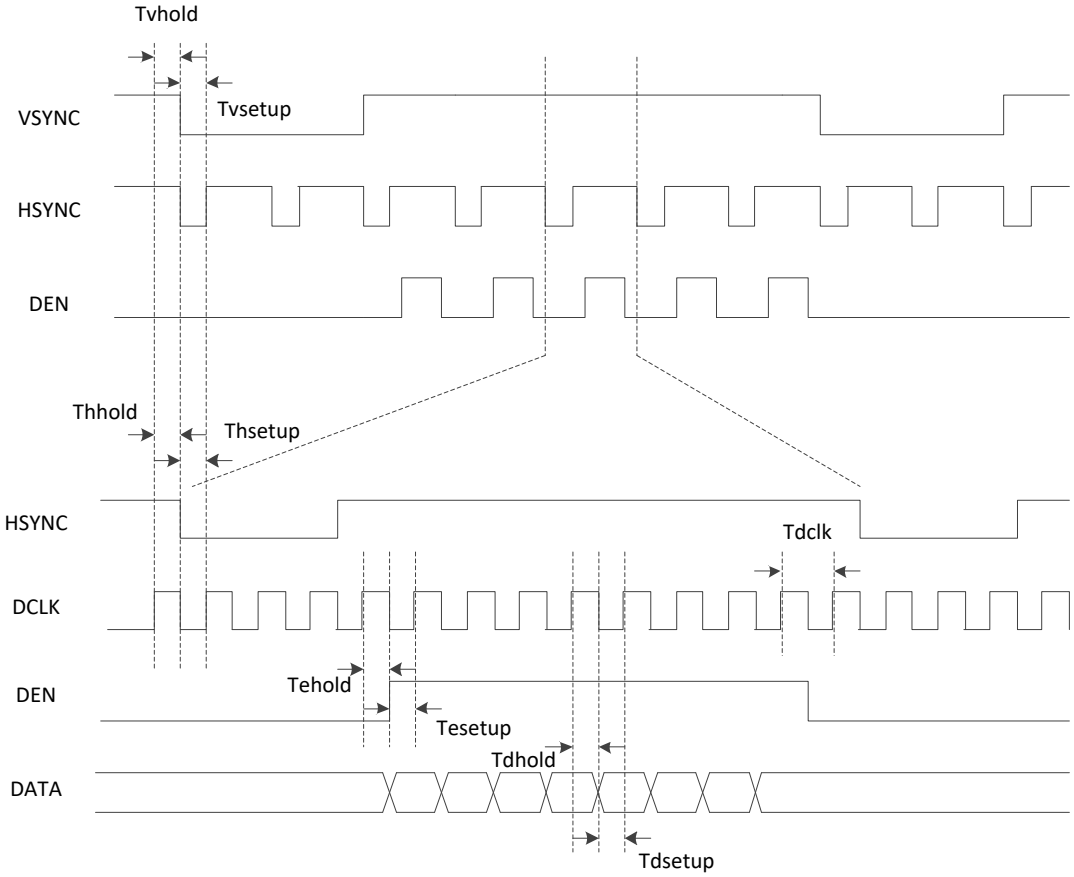


Fig. 12-13 VOP_LITE RGB Interface Timing(SDR)

b. MCU Timing

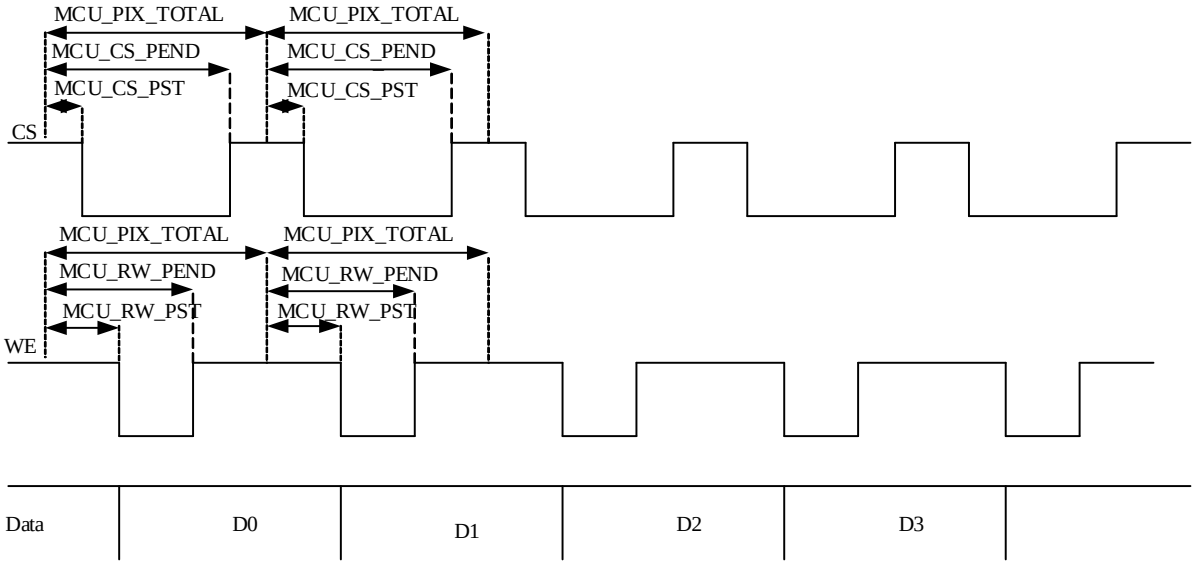


Fig. 12-14 LCDC MCU Interface Timing Setting

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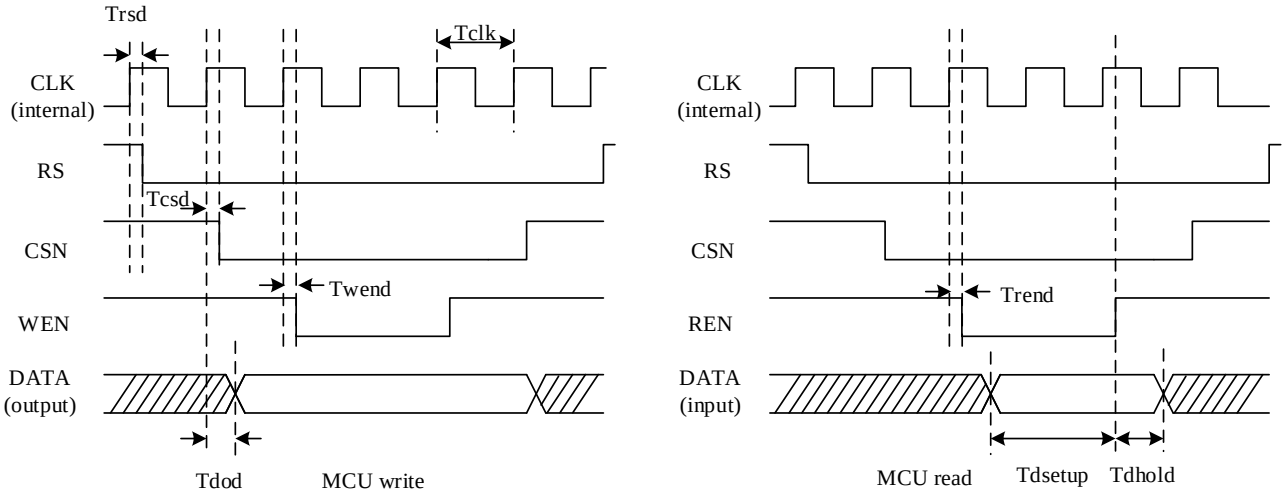


Fig. 12-15 LCDC MCU Interface (i80) Timing

c. BT1120 Timing

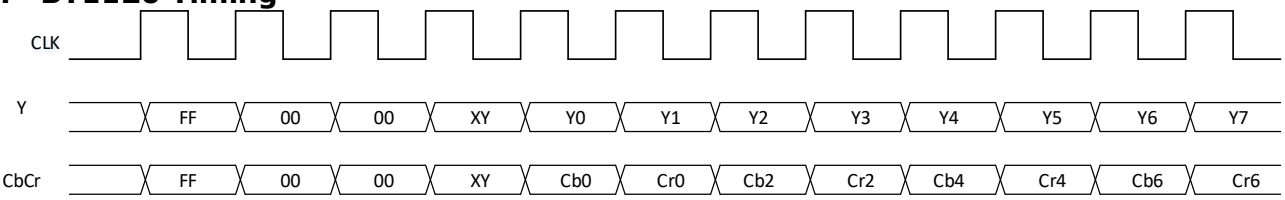


Fig. 12-16 BT1120 Interface Timing

d. BT656 Timing

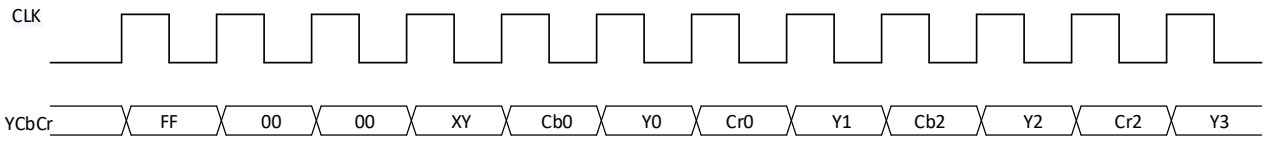


Fig. 12-17 BT656 Interface Timing

12.4 Register Description

12.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
EBC_DSP_START	0x0000	W	0x00000000	Frame start register
EBC_EPD_CTRL	0x0004	W	0x00000000	EPD control register
EBC_DSP_CTRL	0x0008	W	0x00000000	Display control register
EBC_DSP_HTIMING0	0x000C	W	0x00000000	Panel scanning timing register(horizontal period, hsync pulse width)
EBC_DSP_HTIMING1	0x0010	W	0x00000000	Panel scanning timing register(horizontal active start/end point)
EBC_DSP_VTIMING0	0x0014	W	0x00000000	Panel scanning timing register(vertical period, vsync pulse width)
EBC_DSP_VTIMING1	0x0018	W	0x00000000	Panel scanning timing register(vertical active start/end point)
EBC_DSP_ACT_INFO	0x001C	W	0x00000000	Display width/height register
EBC_WIN_CTRL	0x0020	W	0x001F0F00	Win control
EBC_WIN_MST0	0x0024	W	0x00000000	Current image data start address in memory

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Name	Offset	Size	Reset Value	Description
EBC_WIN_MST1	0x0028	W	0x00000000	Next image data start address in memory
EBC_WIN_VIR	0x002C	W	0x00000320	Win virtual width/height register
EBC_WIN_ACT	0x0030	W	0x02580320	Win active width/height register
EBC_WIN_DSP	0x0034	W	0x02580320	Win display width/height register
EBC_WIN_DSP_ST	0x0038	W	0x00080004	Win display start point
EBC_INT_STATUS	0x003C	W	0x070000F0	Interrupt status register
EBC_VCOM0	0x0040	W	0x00000000	VCOM setting register
EBC_VCOM1	0x0044	W	0x00000000	VCOM setting register
EBC_VCOM2	0x0048	W	0x00000000	VCOM setting register
EBC_VCOM3	0x004C	W	0x00000000	VCOM setting register
EBC_CONFIG_DONE	0x0050	W	0x00000000	Register config done flag
EBC_VNUM	0x0054	W	0x00000000	EBC line flag number
EBC_WIN_MST2	0x0058	W	0x00000000	Frame win memory start
EBC_DSP_CTRL2	0x005C	W	0x00064000	Display control register2
EBC_DSP_CTRL3	0x0060	W	0x00000000	Display control register3
EBC_WIN0_CTRL	0x0064	W	0x00000000	Win0 control
EBC_WIN1_CTRL	0x0068	W	0x00000000	Win1 control
EBC_WIN2_CTRL	0x006C	W	0x00000000	Win2 control
EBC_SYS_CTRL	0x0070	W	0x00000000	System control
EBC_VOP_SYS_CTRL	0x0100	W	0x00000000	VOP_LITE system control
EBC_VOP_DSP_CTRL0	0x0104	W	0x00000001	VOP_LITE display control0
EBC_VOP_DSP_CTRL1	0x0108	W	0x00000000	VOP_LITE display control1
EBC_VOP_MCU_CTRL	0x010C	W	0x00711C08	MCU control register
EBC_DSP_HTOTAL_HS_END	0x0110	W	0x014A000A	Panel scanning horizontal width and hsync pulse end point
EBC_DSP_HACT_ST_END	0x0114	W	0x000A014A	Panel active horizontal scanning start point and end point
EBC_DSP_VTOTAL_VS_END	0x0118	W	0x00FA000A	Panel scanning vertical height and vsync pulse end point
EBC_DSP_VACT_ST_END	0x011C	W	0x000A00FA	Panel active vertical scanning start point and end point
EBC_DSP_VS_ST_END_F1	0x0120	W	0x00000000	Vertical scanning start point and vsync pulse end point of even file
EBC_DSP_VACT_ST_END_F1	0x0124	W	0x00000000	Vertical scanning active start point and end point of even filed in interlace
EBC_DSP_BG	0x0128	W	0x00000000	VOP_LITE display background
EBC_BLANKING_VALUE	0x012C	W	0x00000000	The value of vsync blanking
EBC_FRC_LOWER01_0	0x0130	W	0x12844821	Frc algorithm configuration register
EBC_FRC_LOWER01_1	0x0134	W	0x21488412	Frc algorithm configuration register
EBC_FRC_LOWER10_0	0x0138	W	0xA55A9696	Frc algorithm configuration register
EBC_FRC_LOWER10_1	0x013C	W	0x5AA56969	Frc algorithm configuration register
EBC_FRC_LOWER11_0	0x0140	W	0xDEB77BED	Frc algorithm configuration register
EBC_FRC_LOWER11_1	0x0144	W	0xED7BB7DE	Frc algorithm configuration register
EBC_LINE_FLAG	0x0148	W	0x00000000	Flag register value before frame valid

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Name	Offset	Size	Reset Value	Description
EBC_VOP_SCAN_LINE_NUM	0x014C	W	0x00000000	The current scan line number
EBC_VOP_WIN_VIR	0x0150	W	0x00000000	VOP_LITE win virtual stride
EBC_VOP_INT_EN	0x0154	W	0x00000000	Interrupt enable register
EBC_VOP_WIN_DSP_INFO	0x0158	W	0x00000000	VOP_LITE win display width/height on panel
EBC_VOP_WIN_DSP_ST	0x015C	W	0x00000000	VOP_LITE win display start point on panel
EBC_MCU_RW_BYPASS_PORT	0x0160	W	0x00000000	MCU panel write data
EBC_VOP_INT_CLR	0x0164	W	0x00000000	Interrupt clear register
EBC_VOP_INT_STATUS	0x0168	W	0x00000000	Interrupt raw status and interrupt status
EBC_LUT_ADDRESS_MAP_0	0x1000	W	0x00000000	LUT ADDRESS_0
EBC_LUT_ADDRESS_MAP_4095	0x4FFC	W	0x00000000	LUT ADDRESS_4095

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

12.4.2 Detail Register Description

EBC_DSP_START

Address: Operational Base(0x27900000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	dsp_rst soft reset bit
0	RW	0x0	dsp_frm_st frame start bit writing '1' to trigger frame display. read this bit for hold status.

EBC_EPD_CTRL

Address: Operational Base(0x27900000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	eink_mode_swap 1'b0: No swap 1'b1: Swap
30	RW	0x0	eink_mode_frm_sel 1'b0: Frame cnt 1'b1: Win2 data
29	RW	0x0	dsp_three_win_mode three win mode enable 1'b0: Lut mode or direct mode 1'b1: Three win mode
28	RW	0x0	sw_auto_gating_en auto gating enable 1'b0: Disable 1'b1: Enable
27	RW	0x0	ebc_dma_stop 1'b0: Disable 1'b1: Enable If DMA is working, the stop mode would not be active until current bus transfer is finished.

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Bit	Attr	Reset Value	Description
26:16	RW	0x000	dsp_gd_end GCLK falling edge point(SCLK), which count from the falling edge of hsync
15:8	RW	0x00	dsp_gd_st GCLK rising edge point(SCLK), which count from the falling edge of hsync
7:6	RW	0x0	dsp_sddw_mode source data output width 1'b0: 8-bit output 1'b1: 16-bit output
5	RW	0x0	epd_auo EPD panel 1'b0: Eink 1'b1: AUO
4:2	RW	0x0	epd_pwr power enable
1	RW	0x0	epd_gdrl gate scanning direction 1'b0: Top to button 1'b1: Button to top
0	RW	0x0	epd_sdshr source scanning direction 1'b0: Left to right 1'b1: Right to left

EBC_DSP_CTRL

Address: Operational Base(0x27900000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	dsp_swap_mode display swap for 8bit output 2'b00: SDO[7:0] = {P3,P2,P1,P0} 2'b01: SDO[7:0] = {P1,P0,P3,P2} 2'b10: SDO[7:0] = {P2,P3,P0,P1} 2'b11: SDO[7:0] = {P0,P1,P2,P3} for 16bit output 2'b00: SDO[15:0] = {P7,P6,P5,P4,P3,P2,P1,P0} 2'b01: SDO[15:0] = {P4,P5,P6,P7,P0,P1,P2,P3} 2'b10: SDO[15:0] = {P0,P1,P2,P3,P4,P5,P6,P7} 2'b11: SDO[15:0] = {P3,P2,P1,P0,P7,P6,P5,P4}
29	RW	0x0	dsp_diff_mode diff update mode enable 1'b0: Normal update mode 1'b1: Diff update mode
28	RW	0x0	dsp_lut_mode display mode 1'b0: Direct mode 1'b1: LUT mode
27	RW	0x0	dsp_vcom_mode VCOM Mode 1'b0: One phase scanning mode 1'b1: Multi phase scanning mode

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Bit	Attr	Reset Value	Description
26	RW	0x0	dsp_gdoe_pol DSP OUTPUT GOE polarity invert 1'b0: Default 1'b1: Invert
25	RW	0x0	dsp_gdsp_pol DSP OUTPUT GSP polarity invert 1'b0: Default 1'b1: Invert
24	RW	0x0	dsp_gdclk_pol DSP OUTPUT GCLK polarity invert 1'b0: Default 1'b1: Invert
23	RW	0x0	dsp_sdce_pol DSP OUTPUT SCE polarity invert 1'b0: Default 1'b1: Invert
22	RW	0x0	dsp_sdoe_pol DSP OUTPUT SOE polarity invert 1'b0: Default 1'b1: Invert
21	RW	0x0	dsp_sdle_pol DSP OUTPUT SLE polarity invert 1'b0: Default 1'b1: Invert
20	RW	0x0	dsp_sdclk_pol DSP_OUTPUT SCLK polarity invert 1'b0: Default 1'b1: Invert
19:16	RW	0x0	dsp_sdclk_div SCLK divide rate SCLK = (DSP_CLK_DIV + 1) * DCLK
15:1	RO	0x0000	reserved
0	RW	0x0	dsp_sdoe_mode SDO default value

EBC_DSP_HTIMING0

Address: Operational Base(0x27900000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsp_htotal panel display scanning horizontal period.
15:0	RW	0x0000	dsp_hs_end panel display scanning hsync(SLE) pulse width.

EBC_DSP_HTIMING1

Address: Operational Base(0x27900000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsp_hact_end panel display scanning horizontal active end point
15:0	RW	0x0000	dsp_hact_st panel display scanning horizontal active start point

EBC_DSP_VTIMING0

Address: Operational Base(0x27900000) + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsp_vtotal panel display scanning vertical period.
15:0	RW	0x0000	dsp_vs_end panel display scanning vsync(GOE) pulse width.

EBC_DSP_VTIMING1

Address: Operational Base(0x27900000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsp_vact_end panel display scanning vertical active end point
15:0	RW	0x0000	dsp_vact_st panel display scanning vertical active start point

EBC_DSP_ACT_INFO

Address: Operational Base(0x27900000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsp_height display height
15:0	RW	0x0000	dsp_width display width

EBC_WIN_CTRL

Address: Operational Base(0x27900000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RW	0x0	dma_burst_length dma burst length 2'b00: Burst16 2'b01: Burst8 2'b10: Burst4 2'b11: Reserved
23:21	RO	0x0	reserved
20:12	RW	0x1f0	win2_fifo_almost_full_level win2(frame_num) fifo almost full level
11:4	RW	0xf0	win_fifo_almost_full_level win fifo almost full level
3	RO	0x0	reserved
2:0	RW	0x0	win_fmt win source data format: 3'b000: Y-data(4bpp) 3'b001: Y-data(8bpp) 3'b010: RGB565(16bpp) 3'b011: XRGB8888(32bpp) 3'b100: Y-data(5bpp+3'b0)

EBC_WIN_MST0

Address: Operational Base(0x27900000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win_mst0 start address of current image data in memory

EBC_WIN_MST1

Address: Operational Base(0x27900000) + offset (0x0028)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win_mst1 start address of next image data in memory

EBC_WIN_VIR

Address: Operational Base(0x27900000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win_vir_height win virtual height
15:0	RW	0x0320	win_vir_width win virtual width

EBC_WIN_ACT

Address: Operational Base(0x27900000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0258	win_act_height win active height
15:0	RW	0x0320	win_act_width win active width

EBC_WIN_DSP

Address: Operational Base(0x27900000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x0258	win_dsp_height win display height
15:0	RW	0x0320	win_dsp_width win display width

EBC_WIN_DSP_ST

Address: Operational Base(0x27900000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RW	0x0008	win_dsp_yst win display y start point
15:0	RW	0x0004	win_dsp_xst win display x start point

EBC_INT_STATUS

Address: Operational Base(0x27900000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	win2_empty_int_st win2 fifo empty interrupt status
29	RW	0x0	win1_empty_int_st win1 fifo empty interrupt status
28	RW	0x0	win0_empty_int_st win0 fifo empty interrupt status
27	RO	0x0	reserved
26	RW	0x1	win2_empty_int_msk win2 empty interrupt mask: 1'b0: Unmask 1'b1: Mask
25	RW	0x1	win1_empty_int_msk win1 empty interrupt mask: 1'b0: Unmask 1'b1: Mask

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Bit	Attr	Reset Value	Description
24	RW	0x1	win0_empty_int_msk win0 empty interrupt mask: 1'b0: Unmask 1'b1: Mask
23	RO	0x0	reserved
22	RW	0x0	win2_empty_clr win2 empty interrupt clear: after be set to 1, this bit will clear by itself 1 cycle later.
21	RW	0x0	win1_empty_clr win1 empty interrupt clear: after be set to 1, this bit will clear by itself 1 cycle later.
20	RW	0x0	win0_empty_clr win0 empty interrupt clear: after be set to 1, this bit will clear by itself 1 cycle later.
19:12	RW	0x00	dsp_frm_int_num frame number of the scanning flag interrupt the display frame number when the flag interrupt occur, the range is (0~DSP_FRM_NUM-1).
11	RW	0x0	line_flag_int_clr line flag interrupt clear: after be set to 1, this bit will clear by itself 1 cycle later.
10	RW	0x0	dsp_frm_int_clr display frame interrupt clear: after be set to 1, this bit will clear by itself 1 cycle later.
9	RW	0x0	dsp_end_int_clr display end interrupt clear: after be set to 1, this bit will clear by itself 1 cycle later.
8	RW	0x0	frm_end_int_clr frame end interrupt clear: after be set to 1, this bit will clear by itself 1 cycle later.
7	RW	0x1	line_flag_int_msk line flag interrupt mask 1'b0: Unmask 1'b1: Mask
6	RW	0x1	dsp_frm_int_msk frame flag interrupt mask: 1'b0: Unmask 1'b1: Mask
5	RW	0x1	dsp_end_int_msk display end interrupt mask: 1'b0: Unmask 1'b1: Mask
4	RW	0x1	frm_end_int_msk frame end interrupt mask: 1'b0: Unmask 1'b1: Mask
3	RO	0x0	line_flag_int_st line flag interrupt status
2	RO	0x0	dsp_frm_int_st frame flag interrupt status
1	RO	0x0	dsp_end_int_st display end interrupt status
0	RO	0x0	frm_end_int_st frame end interrupt status

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EBC_VCOM0

Address: Operational Base(0x27900000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dsp_border_0 VCOM[1:0] values in 0-15 frame. The VCOM [1:0] indicate the COM voltage in one frame. The VCOM can be different in different frame. So we can set the VCOM [1:0] sequence using display frames before start the display.

EBC_VCOM1

Address: Operational Base(0x27900000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dsp_border_1 VCOM[1:0] values in 16-31 frame. The VCOM [1:0] indicate the COM voltage in one frame. The VCOM can be different in different frame. So we can set the VCOM [1:0] sequence using display frames before start the display.

EBC_VCOM2

Address: Operational Base(0x27900000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dsp_border_2 VCOM[1:0] values in 32-47 frame. The VCOM [1:0] indicate the COM voltage in one frame. The VCOM can be different in different frame. So we can set the VCOM [1:0] sequence using display frames before start the display.

EBC_VCOM3

Address: Operational Base(0x27900000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dsp_border_3 VCOM[1:0] values in 48-64 frame. The VCOM [1:0] indicate the COM voltage in one frame. The VCOM can be different in different frame. So we can set the VCOM [1:0] sequence using display frames before start the display.

EBC_CONFIG_DONE

Address: Operational Base(0x27900000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	reg_config_done In the first setting of the register, the new value was saved into the mirror register. when all the register config finish, writing this register to enable the copyright of the mirror register to real register. then register would be updated at the start of every frame.

EBC_VNUM

Address: Operational Base(0x27900000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dsp_vcnt readable register for Internal line number

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	line_flag_num line number of the scanning flag interrupt the display line number when the flag interrupt occur, the range is (0~DSP_VTOTAL-1).

EBC_WIN_MST2

Address: Operational Base(0x27900000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win_mst2 start address of frame data in memory

EBC_DSP_CTRL2

Address: Operational Base(0x27900000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:12	RW	0x064	dsp_sdce_width source driver length
11:4	RW	0x00	dsp_frm_total frame total number(n) frame_num = n+1
3	RO	0x0	reserved
2	RW	0x0	dsp_eink_mode eink mode enable 1'b0: Lut mode or direct mode or 3win mode 1'b1: Eink mode
1	RW	0x0	sw_burst_ctrl 1'b0: Original burst 1'b1: Modified burst
0	RW	0x0	dsp_out_low 1'b0: Normal 1'b1: Outputs are low

EBC_DSP_CTRL3

Address: Operational Base(0x27900000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	dsp_background EBC display background

EBC_WIN0_CTRL

Address: Operational Base(0x27900000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	win0_axi_gather_num win0 axi gather_num gather number
7:4	RW	0x0	win0_rid win0 axi read id
3	RO	0x0	reserved
2	RW	0x0	win0_no_outstanding 1'b0: Enable 1'b1: Disable
1	RW	0x0	win0_axi_gather_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	win0_en win0 enable

EBC_WIN1_CTRL

Address: Operational Base(0x27900000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	win1_axi_gather_num win1 axi gather_num gather number
7:4	RW	0x0	win1_rid win1 axi read id
3	RO	0x0	reserved
2	RW	0x0	win1_no_outstanding 1'b0: Enable 1'b1: Disable
1	RW	0x0	win1_axi_gather_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	win1_en win1 enable

EBC_WIN2_CTRL

Address: Operational Base(0x27900000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	win2_axi_gather_num win2 axi gather_num gather number
7:4	RW	0x0	win2_rid win2 axi read id
3	RO	0x0	reserved
2	RW	0x0	win2_no_outstanding 1'b0: Enable 1'b1: Disable
1	RW	0x0	win2_axi_gather_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	win2_en win2 enable

EBC_SYS_CTRL

Address: Operational Base(0x27900000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	sw_axi_rd_urgency_en AXI read urgency enable 1'b0: Disable 1'b1: Enable
23:21	RO	0x0	reserved
20:16	RW	0x00	sw_axi_max_outstand_num AXI max outstanding number
15:13	RO	0x0	reserved
12	RW	0x0	sw_axi_max_outstand_en AXI max outstand enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	sw_biu_hurry_threshold BIU hurry threshold
7	RO	0x0	reserved
6:5	RW	0x0	sw_biu_hurry_value BIU hurry value
4	RW	0x0	sw_biu_hurry_en Hurry enable for BIU 1'b0: Disable 1'b1: Enable
3	RO	0x0	reserved
2:1	RW	0x0	sw_biu_qos_value BIU QoS value
0	RW	0x0	sw_biu_qos_en QoS enable for BIU 1'b0: Disable 1'b1: Enable

EBC_VOP_SYS_CTRL

Address: Operational Base(0x27900000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	sw_vop_inf_out_en If the output is to the HDMI/MIPI/EDP interface, the signal needs to be configured as 1, otherwise there will be no signal output. 1'b0: Disable 1'b1: Enable
7	RW	0x0	sw_bt_uv_swap 1'b0: BT.1120/BT.656 u/v no swap 1'b1: BT.1120/BT.656 u/v swap
6	RW	0x0	sw_bt_yc_swap 1'b0: BT.1120/BT.656 y/c no swap 1'b1: BT.1120/BT.656 y/c swap
5:4	RW	0x0	vop_data_fmt 2'b00: ARGB888 2'b01: RGB888 2'b10: RGB565 others: reserved
3	RW	0x0	vop_win_interlace_read 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_r2y_mode Color space conversion: 1'b0: BT601, Y{16,235}, UV{16,240} 1'b1: BT709, Y{16,235}, UV{16,240}
1	RW	0x0	sw_r2y_en 1'b0: Bypass 1'b1: Enable
0	RW	0x0	sw_vop_en 1'b0: EBC output 1'b1: VOP output

EBC_VOP_DSP_CTRL0

Address: Operational Base(0x27900000) + offset (0x0104)

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Bit	Attr	Reset Value	Description
31	RW	0x0	sw_vop_inf_out_dresetn If the output is to the HDMI/MIPI interface, the signal needs to be configured to be high. 1'b0: Tie 0 1'b1: Tie 1
30:18	RO	0x0000	reserved
17	RW	0x0	sw_dcf_idle_en 1'b0: DCF idle disable 1'b1: DCF idle enable
16	RW	0x0	sw_imd_dsp_out_zero 1'b0: Normal output 1'b1: Output '0' means:{hsync,vsync,den}={1'b0,1'b0,1'b0}
15	RW	0x0	sw_imd_vop_standby_en Writing "1" to turn VOP into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the VOP go back to work immediately. 1'b0: Disable 1'b1: Enable Black display is recommended before setting standby mode enable.
14	RO	0x0	reserved
13	RW	0x0	sw_imd_dsp_data_out_mode 1'b0: Normal output mode 1'b1: Output 24'b0
12	RW	0x0	sw_io_pad_clk_sel 1'b0: Normal dclk out 1'b1: Gating dclk out
11:8	RO	0x0	reserved
7	RW	0x0	sw_rgb_den_pol 1'b0: Positive 1'b1: Negative When this channel dclk_en = 0, this signal is used to control corresponding bit.
6	RW	0x0	sw_rgb_hsync_pol 1'b0: Negative 1'b1: Positive When this channel dclk_en = 0, this signal is used to control corresponding bit.
5	RW	0x0	sw_rgb_vsync_pol 1'b0: Negative 1'b1: Positive When this channel dclk_en = 0, this signal is used to control corresponding bit.
4	RO	0x0	reserved
3	RW	0x0	sw_imd_core_clk_sel 1'b0: Dclk_core sel dclk 1'b1: Dclk_core sel dclk div2
2	RW	0x0	sw_bt656_en 1'b0: RGB or BT.1120 output 1'b1: BT.656 output

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Bit	Attr	Reset Value	Description
1	RW	0x0	sw_bt1120_en 1'b0: RGB output 1'b1: BT.1120 output
0	RW	0x1	sw_rgb_en 1'b0: RGB disable 1'b1: RGB enable

EBC_VOP_DSP_CTRL1

Address: Operational Base(0x27900000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	sw_dsp_out_mode 4'b0000: Parallel 24-bit RGB888 output {R[7:0],G[7:0],B[7:0]} 4'b0001: Parallel 18-bit RGB666 output {6'b0,R[5:0],G[5:0],B[5:0]} 4'b0010: Parallel 16-bit RGB565 output {8'b0,R[4:0],G[5:0],B[4:0]} 4'b1000: Serial 3x8-bit RGB888 {16'b0, B[7:0]} + {16'b0,G[7:0]} + {16'b0,R[7:0]} 4'b1001: Serial 3x6-bit RGB666 {16'b0, B[5:0],2'b0} + {16'b0,G[5:0],2'b0} + {16'b0,R[5:0],2'b0} 4'b1010: Serial 2x8-bit RGB565 {16'b0, B[4:0],G[5:3]} + {16'b0,G[2:0],R[4:0]} 4'b1100: Serial 3x8-bit RGB888 + dummy {16'b0, B[7:0]} + {16'b0,G[7:0]} + {16'b0,R[7:0]} + dummy Others: Reserved
15	RW	0x0	sw_dsp_blank_en When this bit enable, the hsync/vsync/den output is blank. means:{hsync,vsync,den}={1'b1,1'b1,1'b0} 1'b0: Disable 1'b1: Enable
14	RW	0x0	sw_dsp_black_en When this bit enable, the pixel data output is all black (0x000000) 1'b0: Disable 1'b1: Enable
13:11	RO	0x0	reserved
10	RW	0x0	sw_dsp_rg_swap 1'b0: RGB 1'b1: GRB
9	RW	0x0	sw_dsp_rb_swap 1'b0: RGB 1'b1: BGR
8	RW	0x0	sw_dsp_bg_swap 1'b0: RGB 1'b1: RBG
7	RW	0x0	sw_dither_down_sel 1'b0: Allegro 1'b1: FRC
6	RW	0x0	sw_dither_down_mode 1'b0: RGB888 to RGB565 1'b1: RGB888 to RGB666

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Bit	Attr	Reset Value	Description
5	RW	0x0	sw_dither_down 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_dither_up 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1	RW	0x0	sw_dsp_interlace_field_pol 1'b0: Normal 1'b1: Invert
0	RW	0x0	sw_dsp_interlace 1'b0: Disable 1'b1: Enable This mode is related to the TVE output, the display timing of odd field must be set correctly. (vop_dsp_vs_st_end_f1/vop_dsp_vact_end_f1)

EBC_VOP_MCU_CTRL

Address: Operational Base(0x27900000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31	RW	0x0	mcu_type MCU LCD output select
30	RW	0x0	mcu_bypass MCU LCD BYPASS MODE select
29	RW	0x0	mcu_rs MCU LCD RS Select 1'b0: Command 1'b1: Data
28	RW	0x0	mcu_frame_st Write "1": MCU HOLD Mode Frame Start Read: MCU/LCDC standby HOLD status
27	RW	0x0	mcu_hold_mode MCU HOLD Mode Select
26	RO	0x0	reserved
25:20	RW	0x07	mcu_rw_pend MCU_RW signal end point (0-63)
19:16	RW	0x1	mcu_rw_pst MCU_RW signal start point (0-15)
15:10	RW	0x07	mcu_cs_pend MCU_CS signal end point (0-63)
9:6	RW	0x0	mcu_cs_pst MCU_CS signal start point (0-15)
5:0	RW	0x08	mcu_pix_total MCU LCD Interface writing period (1-63)

EBC_DSP_HTOTAL_HS_END

Address: Operational Base(0x27900000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x14a	dsp_htotal dsp_htotal
15:12	RO	0x0	reserved
11:0	RW	0x00a	dsp_hs_end dsp_hs_end

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EBC_DSP_HACT_ST_END

Address: Operational Base(0x27900000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	dsp_hact_st dsp_hact_st
15:12	RO	0x0	reserved
11:0	RW	0x14a	dsp_hact_end dsp_hact_end

EBC_DSP_VTOTAL_VS_END

Address: Operational Base(0x27900000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0fa	dsp_vtotal dsp_vtotal
15:13	RO	0x0	reserved
12	RW	0x0	sw_imd_dsp_timing_imd Whether the signal(dsp_vtotal) takes effect immediately.
11:0	RW	0x00a	dsp_vs_end dsp_vs_end

EBC_DSP_VACT_ST_END

Address: Operational Base(0x27900000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	dsp_vact_st dsp_vact_st
15:12	RO	0x0	reserved
11:0	RW	0x0fa	dsp_vact_end dsp_vact_end

EBC_DSP_VS_ST_END_F1

Address: Operational Base(0x27900000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode)
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode)

EBC_DSP_VACT_ST_END_F1

Address: Operational Base(0x27900000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode)
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode)

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EBC_DSP_BG

Address: Operational Base(0x27900000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dsp_bg_red Background Red color
15:8	RW	0x00	dsp_bg_green Background Green color
7:0	RW	0x00	dsp_bg_blue Background Blue color

EBC_BLANKING_VALUE

Address: Operational Base(0x27900000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	blanking_value_config_en 1'b0: Disable 1'b1: Enable
23:0	RW	0x000000	sw_blanking_value Blank value

EBC_FRC_LOWER01_0

Address: Operational Base(0x27900000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	RW	0x1284	lower01_frm1 lower01 frame1
15:0	RW	0x4821	lower01_frm0 lower01 frame0

EBC_FRC_LOWER01_1

Address: Operational Base(0x27900000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	RW	0x2148	lower01_frm3 lower01 frame3
15:0	RW	0x8412	lower01_frm2 lower01 frame2

EBC_FRC_LOWER10_0

Address: Operational Base(0x27900000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:16	RW	0xa55a	lower10_frm1 lower10 frame1
15:0	RW	0x9696	lower10_frm0 lower10 frame0

EBC_FRC_LOWER10_1

Address: Operational Base(0x27900000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:16	RW	0x5aa5	lower10_frm3 lower10 frame3
15:0	RW	0x6969	lower10_frm2 lower10 frame2

EBC_FRC_LOWER11_0

Address: Operational Base(0x27900000) + offset (0x0140)

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Bit	Attr	Reset Value	Description
31:16	RW	0xdeb7	lower11_frm1 lower11 frame1
15:0	RW	0x7bed	lower11_frm0 lower11 frame0

EBC_FRC_LOWER11_1

Address: Operational Base(0x27900000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RW	0xed7b	lower11_frm3 lower11 frame3
15:0	RW	0xb7de	lower11_frm2 lower11 frame2

EBC_LINE_FLAG

Address: Operational Base(0x27900000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_line_flag1_num The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_line_flag0_num The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

EBC_VOP_SCAN_LINE_NUM

Address: Operational Base(0x27900000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	scan_line_num The current scan line number

EBC_VOP_WIN_VIR

Address: Operational Base(0x27900000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	win_vir_stride Number of words of Win Virtual width ARGB888: win_vir_width RGB888: (win_vir_width*3/4) + (win_vir_width%3) RGB565: ceil(win_vir_width/2)

EBC_VOP_INT_EN

Address: Operational Base(0x27900000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	dsp_hold_valid_int_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	bus_error_int_en 1'b0: Disable 1'b1: Enable
3	RW	0x0	line_flag1_int_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x0	line_flag0_int_en 1'b0: Disable 1'b1: Enable
1	RW	0x0	dma_frm_fsh_int_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	fs_int_en 1'b0: Disable 1'b1: Enable

EBC_VOP_WIN_DSP_INFO

Address: Operational Base(0x27900000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	dsp_win_height win_dsp_height = (win dsp vertical size -1)
15:11	RO	0x00	reserved
10:0	RW	0x000	dsp_win_width win_dsp_width = (win dsp horizontal size -1)

EBC_VOP_WIN_DSP_ST

Address: Operational Base(0x27900000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_win_yst win y-axis start point
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_win_xst win x-axis start point

EBC_MCU_RW_BYPASS_PORT

Address: Operational Base(0x27900000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mcu_write_data_bypass MCU write bypass data

EBC_VOP_INT_CLR

Address: Operational Base(0x27900000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	vop_dsp_frm_end_int_clr 1'b0: Not clear 1'b1: Clear
5	RW	0x0	dsp_hold_valid_int_clr 1'b0: Not clear 1'b1: Clear
4	RW	0x0	bus_error_int_clr 1'b0: Not clear 1'b1: Clear
3	RW	0x0	line_flag1_int_clr 1'b0: Not clear 1'b1: Clear

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Bit	Attr	Reset Value	Description
2	RW	0x0	line_flag0_int_clr 1'b0: Not clear 1'b1: Clear
1	RW	0x0	dma_frm_fsh_int_clr 1'b0: Not clear 1'b1: Clear
0	RW	0x0	fs_int_clr 1'b0: Not clear 1'b1: Clear

EBC_VOP_INT_STATUS

Address: Operational Base(0x27900000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	dsp_hold_valid_int_raw_sts Display hold interrupt raw status
12	RW	0x0	bus_error_int_raw_sts Bus error interrupt raw status
11	RW	0x0	line_flag1_int_raw_sts Line flag1 interrupt raw status
10	RW	0x0	line_flag0_int_raw_sts Line flag0 interrupt raw status
9	RW	0x0	dma_frm_fsh_int_raw_sts DMA finish interrupt raw status
8	RW	0x0	fs_int_raw_sts Frame start interrupt raw status
7:6	RO	0x0	reserved
5	RW	0x0	dsp_hold_valid_int_sts Display hold interrupt status
4	RW	0x0	bus_error_int_sts Bus error interrupt status
3	RW	0x0	line_flag1_int_sts Line flag1 interrupt status
2	RW	0x0	line_flag0_int_sts Line flag0 interrupt status
1	RW	0x0	dma_frm_fsh_int_sts DMA finish interrupt status
0	RW	0x0	fs_int_sts Frame start interrupt status

EBC_LUT_ADDRESS_MAP_0

Address: Operational Base(0x27900000) + offset (0x1000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lut_data0 LUT data0

EBC_LUT_ADDRESS_MAP_4095

Address: Operational Base(0x27900000) + offset (0x4FFC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lut_data4095 LUT data4095

12.5 Interface Description

12.5.1 EBC IO List

Table 12-3 EBC Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
VO_EBC_SDDO0	I/O	VO_LCDC_D0/VO_EBC_SDDO0/ETH0_RXD2_M0/SAI2_SDO_M2/DSMC_CSN0/FLEXBUS1_D2/UART2_CTSN_M2/I3C1_SCL_M2/PWM2_CH5_M3/GPIO3_D3_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[15:12] = 4'h2
VO_EBC_SDDO1	I/O	VO_LCDC_D1/VO_EBC_SDDO1/ETH0_RXD3_M0/SAI2_SDI_M2/DSMC_CSN3/FLEXBUS0_D12/FLEXBUS1_D15_M0/FLEXBUS0_CSN_M3/UART2_RTSN_M2/SPI4_CSN1_M1/I3C1_SDA_M2/PWM2_CH4_M3/GPIO3_D2_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[11:8] = 4'h2
VO_EBC_SDDO2	I/O	VO_LCDC_D2/VO_EBC_SDDO2/ETH0_RXCLK_M0/SAI2_MCLK_M2/DSMC_CSN2/FLEXBUS0_D11/FLEXBUS1_CSN_M2/SPI4_CLK_M1/I3C1_SDA_PU_M2/GPIO3_D1_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[7:4] = 4'h2
VO_EBC_SDDO3	I/O	VO_LCDC_D3/VO_EBC_SDDO3/SAI1_MCLK_M1/DSMC_DATA1/FLEXBUS1_D3/UART8_CTSN_M0/SPI1_CSN0_M2/PWM2_CH3_M3/GPIO3_D0_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[3:0] = 4'h2
VO_EBC_SDDO4	I/O	VO_LCDC_D4/VO_EBC_SDDO4/SAI1_SCLK_M1/DSMC_DATA2/FLEXBUS1_D4/UART8_RTSN_M0/SPI1_CLK_M2/GPIO3_C7_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[15:12] = 4'h2
VO_EBC_SDDO5	I/O	VO_LCDC_D5/VO_EBC_SDDO5/SAI1_LRCK_M1/DSMC_DATA3/FLEXBUS1_D5/UART8_TX_M0/SPI1_MOSI_M2/GPIO3_C6_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[11:8] = 4'h2
VO_EBC_SDDO6	I/O	VO_LCDC_D6/VO_EBC_SDDO6/SAI1_SDO0_M1/DSMC_DATA4/FLEXBUS1_D6/UART8_RX_M0/SPI1_MISO_M2/PWM2_CH2_M3/GPIO3_C5_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[7:4] = 4'h2
VO_EBC_SDDO7	I/O	VO_LCDC_D7/VO_EBC_SDDO7/SAI1_SDO1_M1/DSMC_DATA5/FLEXBUS1_D7/UART11_TX_M0/SPI2_CSN0_M2/I2C5_SCL_M3/CAN0_TX_M3/GPIO3_C4_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[3:0] = 4'h2
VO_EBC_SDDO8	I/O	VO_LCDC_D8/VO_EBC_SDDO8/ETH0_TXD2_M0/SAI2_LRCK_M2/DSMC_INT3/FLEXBUS0_D10/FLEXBUS0_CSN_M2/UART11_CTSN_M0/SPI4_MOSI_M1/I2C9_SDA_M3/PWM2_CH1_M3/GPIO3_C3_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[15:12] = 4'h2
VO_EBC_SDDO9	I/O	VO_LCDC_D9/VO_EBC_SDDO9/ETH0_TXD3_M0/SAI2_SCLK_M2/DSMC_INT1/FLEXBUS0_D9/UART11_RTSN_M0/SPI4_MISO_M1/I2C9_SCL_M3/PWM2_CH0_M3/GPIO3_C2_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[11:8] = 4'h2
VO_EBC_SDDO10	I/O	VO_LCDC_D10/VO_EBC_SDDO10/ETH0_PTP_REFCLK_M0/SAI1_SDO2_M1/DSMC_DATA6/FLEXBUS1_D8/UART11_RX_M0/SPI2_MISO_M2/I2C5_SDA_M3/CAN0_RX_M3/GPIO3_C1_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[7:4] = 4'h2
VO_EBC_SDDO11	I/O	VO_LCDC_D11/VO_EBC_SDDO11/ETH0_PPSCLK_M0/SAI1_SDO3_M1/DSMC_DATA7/FLEXBUS1_D9/UART2_TX_M2/	TOP_IOC_GPIO3C_IOMUX_SEL_L[3:0] = 4'h2

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Module Pin	Direction	Pad Name	IOMUX Setting
		UART3_RTSN_M1/I2C4_SCL_M3/GPIO3_C0_d	
VO_EBC_SDDO12	I/O	VO_LCDC_D12/VO_EBC_SDDO12/ETH0_PPSTRIG_M0/SAI1_SDI0_M1/DSMC_DQS0/FLEXBUS1_D10/FLEXBUS1_CSN_M0/UART2_RX_M2/UART3_CTSN_M1/I2C4_SDA_M3/GPIO3_B7_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[15:12] = 4'h2
VO_EBC_SDDO13	I/O	VO_LCDC_D13/VO_EBC_SDDO13/ETH0_TXCLK_M0/DSMC_DQS1/FLEXBUS0_CLK/SPI3_CSN0_M1/PWM0_CH1_M3/GPIO3_B6_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[11:8] = 4'h2
VO_EBC_SDDO14	I/O	VO_LCDC_D14/VO_EBC_SDDO14/ETH0_TXD0_M0/SPDIF_TX1_M0/DSMC_DATA8/FLEXBUS0_D0/UART9_CTSN_M1/PWM1_CH5_M3/GPIO3_B5_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[7:4] = 4'h2
VO_EBC_SDDO15	I/O	VO_LCDC_D15/VO_EBC_SDDO15/ETH0_TXD1_M0/SPDIF_RX1_M0/DSMC_DATA9/FLEXBUS0_D1/UART9_RTSN_M1/PWM1_CH4_M3/GPIO3_B4_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[3:0] = 4'h2
VO_EBC_SDCE0	I/O	VO_LCDC_D16/VO_EBC_SDCE0/ETH0_TXCTL_M0/PDM1_SDI0_M2/DSMC_DATA10/FLEXBUS0_D2/UART9_TX_M1/I2C8_SCL_M3/GPIO3_B3_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[15:12] = 4'h2
VO_EBC_SDCE1	I/O	VO_LCDC_D17/VO_EBC_SDCE1/ETH0_RXD0_M0/PDM1_SDI1_M2/DSMC_DATA11/FLEXBUS0_D3/UART9_RX_M1/I2C8_SDA_M3/GPIO3_B2_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[11:8] = 4'h2
VO_EBC_SDCE2	I/O	VO_LCDC_D18/VO_EBC_SDCE2/ETH0_RXD1_M0/PDM1_CLK0_M2/DSMC_DATA12/FLEXBUS0_D4/UART10_TX_M0/SPI4_CSN0_M1/PWM1_CH3_M3/GPIO3_B1_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[7:4] = 4'h2
VO_EBC_SDCE3	I/O	VO_LCDC_D19/VO_EBC_SDCE3/ETH0_MCLK_M0/SAI4_MCLK_M1/DSMC_CSN1/FLEXBUS0_D8/UART10_RX_M0/SPI2_MOSI_M2/PWM0_CH0_M3/GPIO3_B0_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[3:0] = 4'h2
VO_EBC_VCOM	I/O	VO_LCDC_D20/VO_EBC_VCOM/ETH0_RXCTL_M0/PDM1_CLK1_M2/DSMC_DATA13/FLEXBUS0_D5/UART1_TX_M2/UART10_RTSN_M0/GPIO3_A7_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[15:12] = 4'h2
VO_EBC_GDOE	I/O	VO_LCDC_D21/VO_EBC_GDOE/ETH0_MDC_M0/PDM1_SDI2_M2/DSMC_DATA14/FLEXBUS0_D6/UART1_RX_M2/UART10_CTSN_M0/PWM1_CH2_M3/GPIO3_A6_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[11:8] = 4'h2
VO_EBC_GDSP	I/O	VO_LCDC_D22/VO_EBC_GDSP/ETH0_MDIO_M0/PDM1_SDI3_M2/DSMC_DATA15/FLEXBUS0_D7/UART1_RTSN_M2/SPI2_CSN1_M2/PWM1_CH1_M3/GPIO3_A5_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[7:4] = 4'h2
VO_EBC_SDSHR	I/O	VO_LCDC_D23/VO_EBC_SDSHR/ETH_CLK0_25M_OUT_M0/SAI4_SDI_M1/DSMC_RDYN/FLEXBUS1_D11/FLEXBUS0_CSN_M0/UART1_CTSN_M2/SPI2_CLK_M2/PWM1_CH0_M3/GPIO3_A4_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[3:0] = 4'h2

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Module Pin	Direction	Pad Name	IOMUX Setting
VO_EBC_SDOE	I/O	VO_LCDC_CLK/VO_EBC_SDOE/CAM_CLK0_OUT_M0/SAI4_SCLK_M1/DSMC_RESETN/FLEXBUS0_D15_M0/FLEXBUS1_D12_M0/FLEXBUS1_CSN_M1/UART5_RTSN_M0/SPI3_CSN1_M1/PWM2_CH7_M3/GPIO3_D7_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[15:12] = 4'h2
VO_EBC_SDCLK	I/O	VO_LCDC_VSYNC/VO_EBC_SDCLK/SAI1_SDI3_M1/DSMC_CLKN/FLEXBUS1_CLK/UART5_CTSN_M0/SPI3_MOSI_M1/PWM2_CH6_M3/GPIO3_D6_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[11:8] = 4'h2
VO_EBC_GDCLK	I/O	VO_LCDC_HSYNC/VO_EBC_GDCLK/SAI1_SDI2_M1/DSMC_CLKP/FLEXBUS1_D0/UART5_TX_M0/SPI3_MISO_M1/I2C3_SDA_M2/GPIO3_D5_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[7:4] = 4'h2
VO_EBC_SDLE	I/O	VO_LCDC_DEN/VO_EBC_SDLE/SAI1_SDI1_M1/DSMC_DATA0/FLEXBUS1_D1/UART5_RX_M0/SPI3_CLK_M1/I2C3_SCL_M2/GPIO3_D4_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[3:0] = 4'h2

Notes: I=input, O=output, I/O=input/output, bidirectional

12.5.2 VOP_LITE IO List

Table 12-4 VOP_LITE Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
VO_LCDC_D0	I/O	VO_LCDC_D0/VO_EBC_SDDO0/ETH0_RXD2_M0/SAI2_SDO_M2/DSMC_CSN0/FLEXBUS1_D2/UART2_CTSN_M2/I3C1_SCL_M2/PWM2_CH5_M3/GPIO3_D3_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[15:12] = 4'h1
VO_LCDC_D1	I/O	VO_LCDC_D1/VO_EBC_SDDO1/ETH0_RXD3_M0/SAI2_SDI_M2/DSMC_CSN3/FLEXBUS0_D12/FLEXBUS1_D15_M0/FLEXBUS0_CSN_M3/UART2_RTSN_M2/SPI4_CSN1_M1/I3C1_SDA_M2/PWM2_CH4_M3/GPIO3_D2_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[11:8] = 4'h1
VO_LCDC_D2	I/O	VO_LCDC_D2/VO_EBC_SDDO2/ETH0_RXCLK_M0/SAI2_MCLK_M2/DSMC_CSN2/FLEXBUS0_D11/FLEXBUS1_CSN_M2/SPI4_CLK_M1/I3C1_SDA_PU_M2/GPIO3_D1_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[7:4] = 4'h1
VO_LCDC_D3	I/O	VO_LCDC_D3/VO_EBC_SDDO3/SAI1_MCLK_M1/DSMC_DATA1/FLEXBUS1_D3/UART8_CTSN_M0/SPI1_CSN0_M2/PWM2_CH3_M3/GPIO3_D0_d	TOP_IOC_GPIO3D_IOMUX_SEL_L[3:0] = 4'h1
VO_LCDC_D4	I/O	VO_LCDC_D4/VO_EBC_SDDO4/SAI1_SCLK_M1/DSMC_DATA2/FLEXBUS1_D4/UART8_RTSN_M0/SPI1_CLK_M2/GPIO3_C7_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[15:12] = 4'h1
VO_LCDC_D5	I/O	VO_LCDC_D5/VO_EBC_SDDO5/SAI1_LRCK_M1/DSMC_DATA3/FLEXBUS1_D5/UART8_TX_M0/SPI1_MOSI_M2/GPIO3_C6_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[11:8] = 4'h1
VO_LCDC_D6	I/O	VO_LCDC_D6/VO_EBC_SDDO6/SAI1_SDO0_M1/DSMC_DATA4/FLEXBUS1_D6/UART8_RX_M0/SPI1_MISO_M2/PWM2_CH2_M3/GPIO3_C5_d	TOP_IOC_GPIO3C_IOMUX_SEL_H[7:4] = 4'h1
VO_LCDC_D	I/O	VO_LCDC_D7/VO_EBC_SDDO7/SAI1_S	TOP_IOC_GPIO3C_I

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Module Pin	Direction	Pad Name	IOMUX Setting
7		DO1_M1/DSMC_DATA5/FLEXBUS1_D7/UART11_TX_M0/SPI2_CSN0_M2/I2C5_SCL_M3/CAN0_TX_M3/GPIO3_C4_d	OMUX_SEL_H[3:0] = 4'h1
VO_LCDC_D8	I/O	VO_LCDC_D8/VO_EBC_SDDO8/ETH0_TXD2_M0/SAI2_LRCK_M2/DSMC_INT3/FLEXBUS0_D10/FLEXBUS0_CSN_M2/UART11_CTSN_M0/SPI4_MOSI_M1/I2C9_SDA_M3/PWM2_CH1_M3/GPIO3_C3_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[15:12] = 4'h1
VO_LCDC_D9	I/O	VO_LCDC_D9/VO_EBC_SDDO9/ETH0_TXD3_M0/SAI2_SCLK_M2/DSMC_INT1/FLEXBUS0_D9/UART11_RTSN_M0/SPI4_MISO_M1/I2C9_SCL_M3/PWM2_CH0_M3/GPIO3_C2_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[11:8] = 4'h1
VO_LCDC_D10	I/O	VO_LCDC_D10/VO_EBC_SDDO10/ETH0_PTP_REFCLK_M0/SAI1_SDO2_M1/DSMC_DATA6/FLEXBUS1_D8/UART11_RX_M0/SPI2_MISO_M2/I2C5_SDA_M3/CAN0_RX_M3/GPIO3_C1_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[7:4] = 4'h1
VO_LCDC_D11	I/O	VO_LCDC_D11/VO_EBC_SDDO11/ETH0_PPSCLK_M0/SAI1_SDO3_M1/DSMC_DATA7/FLEXBUS1_D9/UART2_TX_M2/UART3_RTSN_M1/I2C4_SCL_M3/GPIO3_C0_d	TOP_IOC_GPIO3C_IOMUX_SEL_L[3:0] = 4'h1
VO_LCDC_D12	I/O	VO_LCDC_D12/VO_EBC_SDDO12/ETH0_PPSTRIG_M0/SAI1_SDI0_M1/DSMC_DQS0/FLEXBUS1_D10/FLEXBUS1_CSN_M0/UART2_RX_M2/UART3_CTSN_M1/I2C4_SDA_M3/GPIO3_B7_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[15:12] = 4'h1
VO_LCDC_D13	I/O	VO_LCDC_D13/VO_EBC_SDDO13/ETH0_TXCLK_M0/DSMC_DQS1/FLEXBUS0_CLK/SPI3_CSN0_M1/PWM0_CH1_M3/GPIO3_B6_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[11:8] = 4'h1
VO_LCDC_D14	I/O	VO_LCDC_D14/VO_EBC_SDDO14/ETH0_TXD0_M0/SPDIF_TX1_M0/DSMC_DATA8/FLEXBUS0_D0/UART9_CTSN_M1/PWM1_CH5_M3/GPIO3_B5_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[7:4] = 4'h1
VO_LCDC_D15	I/O	VO_LCDC_D15/VO_EBC_SDDO15/ETH0_TXD1_M0/SPDIF_RX1_M0/DSMC_DATA9/FLEXBUS0_D1/UART9_RTSN_M1/PWM1_CH4_M3/GPIO3_B4_d	TOP_IOC_GPIO3B_IOMUX_SEL_H[3:0] = 4'h1
VO_LCDC_D16	I/O	VO_LCDC_D16/VO_EBC_SDCE0/ETH0_TXCTL_M0/PDM1_SDI0_M2/DSMC_DATA10/FLEXBUS0_D2/UART9_TX_M1/I2C8_SCL_M3/GPIO3_B3_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[15:12] = 4'h1
VO_LCDC_D17	I/O	VO_LCDC_D17/VO_EBC_SDCE1/ETH0_RXD0_M0/PDM1_SDI1_M2/DSMC_DATA11/FLEXBUS0_D3/UART9_RX_M1/I2C8_SDA_M3/GPIO3_B2_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[11:8] = 4'h1
VO_LCDC_D18	I/O	VO_LCDC_D18/VO_EBC_SDCE2/ETH0_RXD1_M0/PDM1_CLK0_M2/DSMC_DATA12/FLEXBUS0_D4/UART10_TX_M0/SPI4_CSN0_M1/PWM1_CH3_M3/GPIO3_B1_d	TOP_IOC_GPIO3B_IOMUX_SEL_L[7:4] = 4'h1
VO_LCDC_D19	I/O	VO_LCDC_D19/VO_EBC_SDCE3/ETH0_MCLK_M0/SAI4_MCLK_M1/DSMC_CSN	TOP_IOC_GPIO3B_IOMUX_SEL_L[3:0] =

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Module Pin	Direction	Pad Name	IOMUX Setting
		1/FLEXBUS0_D8/UART10_RX_M0/SPI2_MOSI_M2/PWM0_CH0_M3/GPIO3_B0_d	4'h1
VO_LCDC_D20	I/O	VO_LCDC_D20/VO_EBC_VCOM/ETH0_RXCTL_M0/PDM1_CLK1_M2/DSMC_DATA13/FLEXBUS0_D5/UART1_TX_M2/UART10_RTSN_M0/GPIO3_A7_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[15:12] = 4'h1
VO_LCDC_D21	I/O	VO_LCDC_D21/VO_EBC_GDOE/ETH0_MDC_M0/PDM1_SDI2_M2/DSMC_DATA14/FLEXBUS0_D6/UART1_RX_M2/UART10_CTSN_M0/PWM1_CH2_M3/GPIO3_A6_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[11:8] = 4'h1
VO_LCDC_D22	I/O	VO_LCDC_D22/VO_EBC_GDSP/ETH0_MDIO_M0/PDM1_SDI3_M2/DSMC_DATA15/FLEXBUS0_D7/UART1_RTSN_M2/SPI2_CSN1_M2/PWM1_CH1_M3/GPIO3_A5_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[7:4] = 4'h1
VO_LCDC_D23	I/O	VO_LCDC_D23/VO_EBC_SDSHR/ETH_CLK0_25M_OUT_M0/SAI4_SDI_M1/DSMC_RDYN/FLEXBUS1_D11/FLEXBUS0_CSN_M0/UART1_CTSN_M2/SPI2_CLK_M2/PWM1_CH0_M3/GPIO3_A4_d	TOP_IOC_GPIO3A_IOMUX_SEL_H[3:0] = 4'h1
VO_LCDC_CLK	I/O	VO_LCDC_CLK/VO_EBC_SDOE/CAM_CLK0_OUT_M0/SAI4_SCLK_M1/DSMC_RESETN/FLEXBUS0_D15_M0/FLEXBUS1_D12_M0/FLEXBUS1_CSN_M1/UART5_RTSN_M0/SPI3_CSN1_M1/PWM2_CH7_M3/GPIO3_D7_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[15:12] = 4'h1
VO_LCDC_VSYNC	I/O	VO_LCDC_VSYNC/VO_EBC_SDCLK/SAI1_SDI3_M1/DSMC_CLKN/FLEXBUS1_CLK/UART5_CTSN_M0/SPI3_MOSI_M1/PWM2_CH6_M3/GPIO3_D6_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[11:8] = 4'h1
VO_LCDC_HSYNC	I/O	VO_LCDC_HSYNC/VO_EBC_GDCLK/SAI1_SDI2_M1/DSMC_CLKP/FLEXBUS1_D0/UART5_TX_M0/SPI3_MISO_M1/I2C3_SDA_M2/GPIO3_D5_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[7:4] = 4'h1
VO_LCDC_DEN	I/O	VO_LCDC_DEN/VO_EBC_SDLE/SAI1_SDI1_M1/DSMC_DATA0/FLEXBUS1_D1/UART5_RX_M0/SPI3_CLK_M1/I2C3_SCL_M2/GPIO3_D4_d	TOP_IOC_GPIO3D_IOMUX_SEL_H[3:0] = 4'h1

Notes: I=input, O=output, I/O=input/output, bidirectional

12.6 Application Notes

12.6.1 Common

12.6.1.1 DMA transfer mode

There are three DMA transfer modes for loading win0/win1/win2 frame data determined by following parameters:
dma_burst_length
winx_no_outstanding
winx_gather_en
winx_gather_thres

12.6.1.2 auto outstanding transfer mode(random transfer)

When winx_no_outstanding is 0, multi-bursts transfer command could be sent out to AXI master interface continuously if the internal memory has enough space to store new data. The continuous random burst number is in the range of 1 to 4, mainly depending on the

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empty level of internal memory, dma_burst_length, data format and active image width.

12.6.1.3 configured outstanding transfer mode(fixed transfer)

When winx_gather_en is 1, fixed-number of bursts transfer command should be sent out to AXI master interface continuously if the internal memory has enough space to store new data. The fixed-number is determined by win1_gather_thres.

12.6.1.4 DMA control (QoS/Hurry/Outstanding)

If you want to get higher priority for VOP_LITE to access external memory when the frame data is urgent, a QoS and hurry request can be generated and sent out basing on the configured values:
sw_biu_qos_en: SYS_CTRL[0]
sw_biu_qos_value: SYS_CTRL[2:1]
sw_biu_hurry_en: SYS_CTRL[4]
sw_biu_hurry_value: SYS_CTRL[6:5]
sw_biu_hurry_threshold: SYS_CTRL[11:8]
sw_axi_max_outstand_en: SYS_CTRL[12]
sw_axi_max_outstand_num: SYS_CTRL[20:16]
sw_axi_rd_urgency_en: SYS_CTRL[24]
QoS request for higher bus priority for winx.
Max Outstanding number is configurable.

12.6.2 EBC

If you select ebc output, sw_vop_en must be set to 0.
There are three modes in EBC and the specific configuration is as follow.

12.6.2.1 Direct mode

Step1: set dsp_eink_mode=0, dsp_three_win_mode=0, dsp_lut_mode=0;
Step2: set dsp_sdclk_div=4'd3 for 8-bit screen or set dsp_sdclk_div=4'd7 for 16-bit screen;

12.6.2.2 LUT mode

Step1: set dsp_eink_mode=0, dsp_three_win_mode=0, dsp_lut_mode=1;
Step2: set dsp_sdclk_div=4'd3 for 8-bit screen or set dsp_sdclk_div=4'd7 for 16-bit screen;

12.6.2.3 3win LUT mode

Step1: set dsp_eink_mode=0, dsp_three_win_mode=1, dsp_lut_mode=0;
Step2: set dsp_sdclk_div=4'd3 for 8-bit screen or set dsp_sdclk_div=4'd7 for 16-bit screen;

12.6.2.4 Interrupt

EBC interrupt is comprised of 7 interrupt sources:

- Frame end interrupt (when every frame end)
- Display end interrupt (when frame_cnt equals to the dsp_frm_total)
- Frame flag interrupt (when frame_cnt equals to the dsp_frm_int_num)
- Line flag interrupt (when line_cnt equals to the line_flag_int_num)
- Win0 empty interrupt
- Win1 empty interrupt
- Win2 empty interrupt

Every interrupt has independent interrupt mask signal(when xxx_int_msk is 0), interrupt clear signal(xxx_int_clr) and interrupt raw status signal (xxx_int_st).

There is only one interrupt combined with all this interrupt signals to CPU, and it high active.
DMA finish interrupt is used for changing DDR frequency. This interrupt will be asserted when DMA finish getting all the Pixel DATA every frame. This interrupt is asserted at the end of the frame.

Address same interrupt will be asserted at this kind of scenario that all the memory start address configured in EBC register are same compared with the former frame. This interrupt is asserted at the beginning of frame start.

12.6.3 VOP_LITE

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If you select vop_lite output, sw_vop_en must be set to 1.
VOP_LITE has two outputs, one is the same as EBC, directly to IO, one is to VO0 module, output to MIPI/HDMI/EDP and so on. If the output is to VO0, then sw_vop_inf_out_en and sw_vop_inf_out_dresetn must be set to 1, otherwise there will be no signal output. If the output interface is MIPI/HDMI, it will also pass through a 1to4 module, which will convert the data out of VOP_LITE into the input required by MIPI/HDMI.
Note that if vop_lite output is selected, it only uses win2, so only configure win2-related registers.

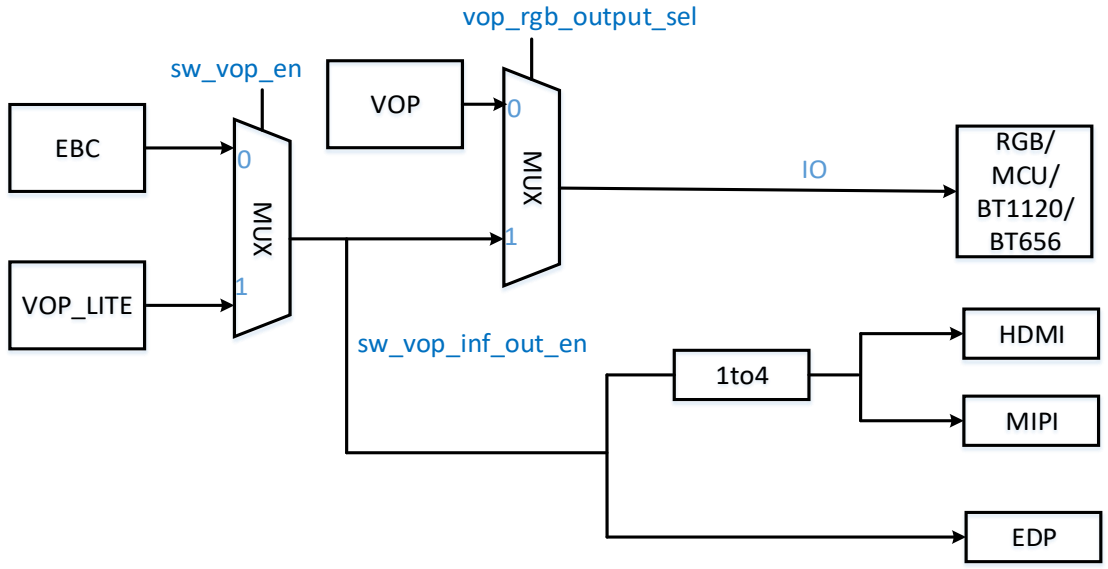


Fig. 12-18 VOP_LITE Path to IO or VO0

12.6.3.1 RGB display mode

RGB display mode is used for RGB panel display. It is a continuous frames display mode.

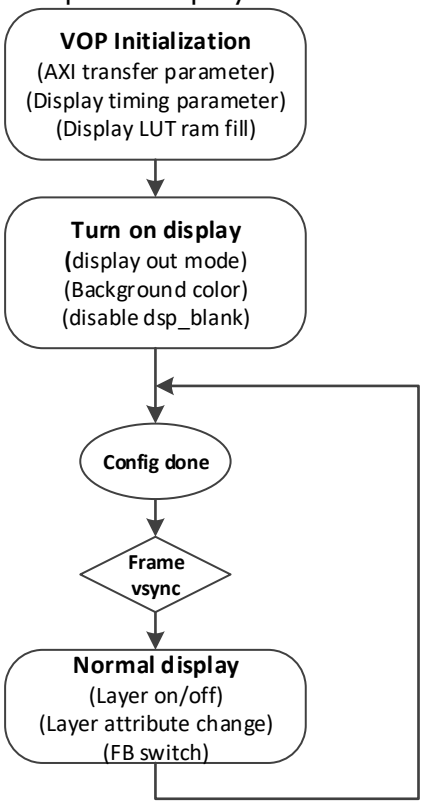


Fig. 12-19 VOP_LITE RGB Mode Programming Flow

1.VOP_LITE initialization

VOP_LITE initialization should be done before turning display on.
First, AXI bus parameter (SYS_CTRL) should be set for DMA transfer.

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Second, display panel/interface timing should be set for display output. The registers are: VOP_DSP_HTOTAL_HS_END/ VOP_DSP_HACT_ST_END/ VOP_DSP_VTOTAL_HS_END/ VOP_DSP_VACT_ST_END/ VOP_DSP_VS_ST_END_F1/ VOP_DSP_VACT_ST_END_F1

2.Background display
Before normal display, the background display could be turn on.
First, set display output mode (VOP_DSP_CTRL0/1) according to display device.
Second, disable dsp_blank mode, which would not be enable until frame synchronization.
Finally, writing '1' to "CONFIG_DONE" register then all the frame-sync registers will be enable at the beginning of next frame.

3.Normal display
In normal display, all the display layers' attribute could be different according display scenario. So there is a programming loop in this mode.
First, configure all the display layers' attribute registers for the change of image format, location, size and so on. Those register would not be enable until frame synchronization.

Finally, write 1 to "CONFIG_DONE" register then all the frame-sync registers will be enabled at the beginning of next frame.

12.6.3.2 Interrupt

VOP_LITE interrupt is comprised of 6 interrupt sources:

- frame start interrupt
- bus error interrupt
- DMA finish interrupt
- line flag0 interrupt
- line flag1 interrupt
- Display hold interrupt

Every interrupt has independent interrupt enable signal(VOP_INT_EN), interrupt clear signal(VOP_INT_CLR) and interrupt raw status signal (VOP_INT_STATUS).

12.6.3.3 Parallel IO Select

VOP_LITE outputs directly to IO and makes a mux with VOP. If the output is vop_lite, set vop_rgb_output_sel to 1 (VCCIO_IOC_MISC_CON8[11], refer to the related register description). If the output interface is mcu, set vop_mcu_sel (VCCIO_IOC_MISC_CON8[10]) to 1.

There are vop_dclk_inv_sel (VCCIO_IOC_MISC_CON8[9]) and vop_dclk_dll_sel (VCCIO_IOC_MISC_CON8[8]) , which adjust the phase of the output dclk clock.

12.6.3.4 VO0 setting

The path from VOP_LITE to VO0 will be output to the HDMI/MIPI/EDP module. The following is the relevant configuration to each module.

a. VOP_LITE -> MIPI DSI2 Host
Step1: set VO0_GRF_SOC_CON9[8] = 1, enable DSI Host data source come from EBC;
Step2: set VO0_GRF_SOC_CON13[3:0] = 0x7, config timing polar and mode;

b. VOP_LITE -> HDMI TX Controller
Step1: GRF_V00_CON13 [4] = 1 ; // it enable the grf_sw_hdmi_1to4 with hdmi mode.
Step2: GRF_VO0_CON09 [9] = 1 ; // it enable the hdmi controller data source com from ebc.

c. VOP_LITE -> EDP TX Controller
Step1: set VO0_GRF_SOC_CON9[10] = 1, enable EDP TX data source come from EBC.

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Chapter 13 USB3.0 Controller

13.1 Overview

USB3.0 sub-system include USB3.0 controller and some PHYs. The two USB3.0 controller (marked as USB0 and USB1) can act as static host, static device, USB2.0/3.0 A device or B device basing on the status of input ID from USB2.0 PHY. The controller respectively connect to one USB3.0 PHY and one USB2.0 PHY and can perform data transmission between host and device as host or device for Super-Speed/High-Speed/Full-Speed/Low-Speed.
USB3.0 sub-system supports the following features:

- General Features
  1. Compatible Specification
     - Universal Serial Bus 3.0 Specification, Revision 1.0
     - Universal Serial Bus Specification, Revision 2.0
     - eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
  2. Support Control/Bulk (including stream)/Interrupt/Isochronous Transfer
  3. Simultaneous IN and OUT transfer for USB3.0, up to 8Gbps bandwidth
  4. Descriptor caching and data pre-fetching used to improve system performance in high-latency systems
  5. LPM protocol in USB 2.0 and U0, U1, U2, and U3 states for USB 3.0
  6. Dynamic FIFO memory allocation for endpoints
  7. Keep-Alive feature in LS mode and (micro-)SOFs in HS/FS modes
  8. Low MIPS requirement
     - Driver involved only in setting up transfers and high-level error recovery
     - Hardware handles data packing and routing to a specific pipe
- Application Interface Features
  1. AHB Slave interface
  2. AXI Master interface
     - Programmable burst lengths up to 16
     - Handle fixed burst address alignment
     - Programmable number of outstanding read/write requests up to 16
     - Concurrent read/write to get best performance of USB3.0 duplex operation
- USB3.0 Device Features
  1. Up to 10 IN endpoints, including control endpoint 0
  2. Up to 6 OUT endpoints, including control endpoint 0
  3. Up to 16 endpoint transfer resources, each one for each endpoint
  4. Flexible endpoint configuration for multiple applications/USB set-configuration modes
  5. Hardware handles ERDY and burst
  6. Stream-based bulk endpoints with controller automatically initiating data movement
  7. Isochronous endpoints with isochronous data in data buffers
  8. Flexible Descriptor with rich set of features to support buffer interrupt moderation, multiple transfers, isochronous, control, and scattered buffering support
- USB Class-Specific Device Features
  1. Stream support for UASP application
  2. Gathering of scattered packet to support Ethernet Over USB
  3. Scheduling of multiple Ethernet packets without interrupt
  4. Variable FIFO buffer allocation for each endpoint
  5. For isochronous applications, scheduling of variable-length payloads for each microframe
  6. Microframe precise scheduling for isochronous applications
  7. Configurable endpoint type selection and dynamic FIFO allocation to facilitate multi-function/composite device implementation. During set-config or alternate-setting, device resources are reconfigured to meet the configuration or alternate setting requirements.
- USB 3.0 xHCI Host Features

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1. Support up to 64 devices
2. Support 1 interrupter
3. Support 1 USB2.0 port and 1 Super-Speed port
4. Support standard or open-source xHCI and class driver

- USB 3.0 Dual-Role Device (DRD) Features
  1. Static Device Operation
  2. Static Host Operation
  3. USB3.0/USB2.0 OTG A device and B device basing on ID
  4. Not Support USB3.0/USB2.0 OTG session request protocol (SRP), host negotiation protocol (HNP) and Role Swap Protocol (RSP)
- Miscellaneous Features
  5. USB2.0 PHY support Battery Charge detection
  6. USB3.0 PHY combos with PCIE/SATA or DP

13.2 Block Diagram

USB comprises with:

- Bus Interface: Register Interface/Data and Descriptors DMA management
- SS/HS/FS/LS MAC: USB part logic
- USB2.0 PHY: UTMI+ interface USB2.0 PHY
- USB3.0 PHY: USB3.0/PCIE/SATA combo or USB3.0/DP combo

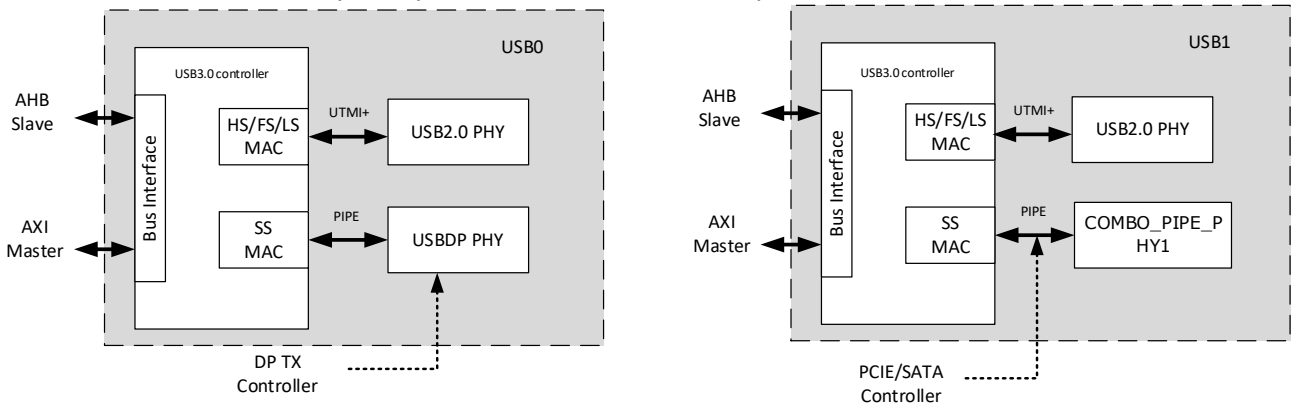


Fig. 13-1 USB3 Block Diagram

13.3 Function Description

USB can act as static xHCI host controller, static device controller, USB3.0/2.0 OTG A device or B device basing on ID of USB2.0 PHY. As device controller, it can work on either USB2.0 speed or Super-Speed basing on speed of host attached to, and process USB transactions described in the descriptors (read back from external memory by AXI master) to/from UTMI+ interface and Pipe Interface.

As host controller, it can work on USB2.0 speed, Super-Speed or both basing on speed or type of attached device, and process USB transactions described in the descriptors (read back from external memory by AXI master) to/from UTMI+ interface and Pipe Interface.

13.4 Register Description

13.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
USB0	0x23000000
USB1	0x23400000

13.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
USB3OTG_GSBUSCFG0	0xC100	W	0x00000001	Global SoC Bus Configuration Register 0
USB3OTG_GSBUSCFG1	0xC104	W	0x00000300	Global SoC Bus Configuration Register 1
USB3OTG_GTXTHRCFG	0xC108	W	0x00000000	Global Tx Threshold Control Register
USB3OTG_GRXTHRCFG	0xC10C	W	0x00000000	Global Rx Threshold Control Register
USB3OTG_GCTL	0xC110	W	0x13512004	Global Core Control Register
USB3OTG_GSTS	0xC118	W	0x7E800000	Global Status Register
USB3OTG_GUCTL1	0xC11C	W	0x0004018A	Global User Control Register 1
USB3OTG_GSNPSID	0xC120	W	0x5533300A	Global SNPS ID Register
USB3OTG_GGPIO	0xC124	W	0x00000000	Global General Purpose Input/Output Register
USB3OTG_GUID	0xC128	W	0x20190520	Global User ID Register
USB3OTG_GUCTL	0xC12C	W	0x02008010	Global User Control Register
USB3OTG_GBUSERRADDRLO	0xC130	W	0x00000000	Global SoC Bus Error Address Register - Low
USB3OTG_GBUSERRADDRHI	0xC134	W	0x00000000	Global SoC Bus Error Address Register - High
USB3OTG_GPRTBIMAPLO	0xC138	W	0x00000000	Global SS Port to Bus Instance Mapping Register
USB3OTG_GHWPARAMS0	0xC140	W	0x2020400A	Global Hardware Parameters Register 0
USB3OTG_GHWPARAMS1	0xC144	W	0x0120C93B	Global Hardware Parameters Register 1
USB3OTG_GHWPARAMS2	0xC148	W	0x20190520	Global Hardware Parameters Register 2
USB3OTG_GHWPARAMS3	0xC14C	W	0x069CD084	Global Hardware Parameters Register 3
USB3OTG_GHWPARAMS4	0xC150	W	0x47822010	Global Hardware Parameters Register 4
USB3OTG_GHWPARAMS5	0xC154	W	0x04204018	Global Hardware Parameters Register 5
USB3OTG_GHWPARAMS6	0xC158	W	0x09D78020	Global Hardware Parameters Register 6
USB3OTG_GHWPARAMS7	0xC15C	W	0x00000000	Global Hardware Parameters Register 7
USB3OTG_GDBGFIFOSPACE	0xC160	W	0x000A0000	Global Debug Queue/FIFO Space Available Register
USB3OTG_GDBGLNMCC	0xC168	W	0x00000000	Global Debug LNMCC Register
USB3OTG_GDBGBMU	0xC16C	W	0x00000000	Global Debug BMU Register
USB3OTG_GDBGLSPMUX	0xC170	W	0x003F0000	Global Debug LSP MUX Register - Device
USB3OTG_GDBGLSP	0xC174	W	0x00000000	Global Debug LSP Register
USB3OTG_GDBGEPINFO0	0xC178	W	0x00000000	Global Debug Endpoint Information Register 0
USB3OTG_GDBGEPINFO1	0xC17C	W	0x00800000	Global Debug Endpoint Information Register 1
USB3OTG_GPRTBIMAP_HSLO	0xC180	W	0x00000000	Global High-Speed Port to Bus Instance Mapping Register - Low
USB3OTG_GPRTBIMAP_FSLO	0xC188	W	0x00000000	Global Full-Speed Port to Bus Instance Mapping Register - Low

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Name	Offset	Size	Reset Value	Description
USB3OTG_GUSB2PHYCFG0	0xC200	W	0x40102400	Global USB2 PHY Configuration Register 0
USB3OTG_GUSB3PIPECTL0	0xC2C0	W	0x00000000	Global PIPE PHY Configuration Register 0
USB3OTG_GTXFIFOSIZn	0xC300	W	0x00000042	Global Transmit FIFO Size Register n, offset (0xc300 + 4*n), n=0~6
USB3OTG_GRXFIFOSIZn	0xC380	W	0x03340185	Global Receive FIFO Size Register n,
USB3OTG_GEVNTADRLO0	0xC400	W	0x00000000	Global Event Buffer Address (Low) Register 0
USB3OTG_GEVNTADRHI0	0xC404	W	0x00000000	Global Event Buffer Address (High) Register 0
USB3OTG_GEVNTSIZ0	0xC408	W	0x00000000	Global Event Buffer Size Register 0
USB3OTG_GEVNTCOUNT0	0xC40C	W	0x00000000	Global Event Buffer Count Register 0
USB3OTG_GHWPARAMS8	0xC600	W	0x0000047C	Global Hardware Parameters Register 8
USB3OTG_GTXFIFOPRIDEV	0xC610	W	0x00000000	Global Device TX FIFO DMA Priority Register
USB3OTG_GTXFIFOPRIHST	0xC618	W	0x00000000	Global Host TX FIFO DMA Priority Register
USB3OTG_GRXFIFOPRIHST	0xC61C	W	0x00000000	Global Host RX FIFO DMA Priority Register
USB3OTG_GFIFOPRIDBC	0xC620	W	0x00000000	Global Host Debug Capability DMA Priority Register
USB3OTG_GDMAHLRATIO	0xC624	W	0x00000000	Global Host FIFO DMA High-Low Priority Ratio Register
USB3OTG_GFLADJ	0xC630	W	0x00000000	Global Frame Length Adjustment Register
USB3OTG_DCFG	0xC700	W	0x00080000	Device Configuration Register
USB3OTG_DCTL	0xC704	W	0x00F00000	Device Control Register
USB3OTG_DEVTEN	0xC708	W	0x00000000	Device Event Enable Register
USB3OTG_DSTS	0xC70C	W	0x00520000	Device Status Register
USB3OTG_DGCMDPAR	0xC710	W	0x00000000	Device Generic Command Parameter Register
USB3OTG_DGCMD	0xC714	W	0x00000000	Device Generic Command Register
USB3OTG_DALEPENA	0xC720	W	0x00000000	Device Active USB Endpoint Enable Register
USB3OTG_DEPnCMDPAR2	0xC800	W	0x00000000	Device Physical Endpoint-n Command Parameter 2 Register, offset (0xc800 + 4*n), n=0~12
USB3OTG_DEPnCMDPAR1	0xC804	W	0x00000000	Device Physical Endpoint-n Command Parameter 1 Register, offset (0xc804 + 4*n), n=0~12
USB3OTG_DEPnCMDPAR0	0xC808	W	0x00000000	Device Physical Endpoint-n Command Parameter 0 Register, offset (0xc808 + 4*n), n=0~12
USB3OTG_DEPnCMD	0xC80C	W	0x00000000	Device Physical Endpoint-n Command Register, offset (0xc80c + 4*n), n=0~12

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

13.4.3 Detail Registers Description

USB3OTG_GSBUSCFG0

Address: **Operational Base** + offset (0xC100)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	datrdreqinfo AXI-cache for Data Read (DatRdReqInfo).
27:24	RW	0x0	desrdreqinfo AXI-cache for Descriptor Read (DesRdReqInfo).
23:20	RW	0x0	datwrreqinfo AXI-cache for Data Write (DatWrReqInfo).
19:16	RW	0x0	deswrreqinfo AXI-cache for Descriptor Write (DesWrReqInfo).
15:12	RO	0x0	reserved
11	RW	0x0	datbigend This bit controls the endian mode for data accesses. 1'b0: Little-endian (default) 1'b1: Big-endian
10	RW	0x0	desbigend This bit controls the endian mode for descriptor accesses. 1'b0: Little-endian (default) 1'b1: Big-endian
9:8	RO	0x0	reserved
7	RW	0x0	incr256brstena If software set this bit to 1, the AXI master uses INCR to do the 256-beat burst.
6	RW	0x0	incr128brstena If software set this bit to 1, the AXI master uses INCR to do the 128-beat burst.
5	RW	0x0	incr64brstena If software set this bit to 1, AXI master uses INCR to do the 64-beat burst.
4	RW	0x0	incr32brstena If software set this bit to 1, the AXI master uses INCR to do the 32-beat burst.
3	RW	0x0	incr16brstena If software set this bit to 1, the AXI master uses INCR to do the 16-beat burst.
2	RW	0x0	incr8brstena If software set this bit to 1, the AXI master uses INCR to do the 8-beat burst.
1	RW	0x0	incr4brstena When this bit is enabled the controller is allowed to do bursts of beat length 1, 2, 3, and 4. It is highly recommended that this bit is enabled to prevent descriptor reads and writes from being broken up into separate transfers.

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Bit	Attr	Reset Value	Description
0	RW	0x1	incrbrstena This bit determines the set of burst lengths the master interface uses. It works in conjunction with the GSBUSCFG0[7:1] enables(INCR256/128/64/32/16/8/4). 0: INCRX burst mode ARLEN/AWLEN do not use INCR. They use only the following burst lengths: 4 (if GSBUSCFG0.INCR4BrstEna = 1); 8 (if GSBUSCFG0.INCR8BrstEna = 1); 16 (if GSBUSCFG0.INCR16BrstEna = 1); 32 (if GSBUSCFG0.INCR32BrstEna = 1); 64 (if GSBUSCFG0.INCR64BrstEna = 1); 128 (if GSBUSCFG0.INCR128BrstEna = 1); 256 (if GSBUSCFG0.INCR256BrstEna = 1); 1: INCR (undefined length) burst mode; ARLEN/AWLEN uses any length less than or equal to the largest-enabled burst length of INCR4/8/16/32/64/128/256. For cache line-aligned applications, this bit is typically set to 0 to ensure that the master interface uses only power-of-2 burst lengths (as enabled via GSBUSCFG0[7:0]).

USB3OTG_GSBUSCFG1

Address: **Operational Base** + offset (0xC104)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	en1kpage 1K Page Boundary Enable. By default (this bit is disabled) the AXI breaks transfers at the 4k page boundary. When this bit is enabled, the AXI master (DMA data) breaks transfers at the 1k page boundary.
11:8	RW	0x3	pipe_trans_limit AXI Pipelined Transfers Burst Request Limit. The field controls the number of outstanding pipelined transfer requests the AXI master pushes to the AXI slave. When the AXI master reaches this limit, it does not make any more requests on the AXI ARADDR and AWADDR buses until the associated data phases complete. This field is encoded as follows: 4'h0: 1 request 4'h1: 2 requests 4'h2: 3 requests 4'h3: 4 requests ... 4'hF: 16 requests
7:0	RO	0x00	reserved

USB3OTG_GTXTHRCFG

Address: **Operational Base** + offset (0xC108)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29	RO	0x0	USBTxPktCntSel This field enables/disables the USB transmission multi-packet thresholding: 1'b0: USB transmission multi-packet thresholding is disabled; the core can only start transmission on the USB after the entire packet has been fetched into the corresponding TXFIFO. 1'b1: USB transmission multi-packet thresholding is enabled. The core can only start transmission on the USB after USB Transmit Packet Count amounts of packets for the USB transaction (burst) are already in the corresponding TXFIFO. This mode is only valid in the host mode. It is only used for SuperSpeed.
28	RO	0x0	reserved
27:24	RW	0x0	USBTxPktCnt This field specifies the number of packets that must be in the TXFIFO before the core can start transmission for the corresponding USB transaction (burst). This field is only valid when the USB Transmit Packet Count Enable field is set to one. Valid values are from 1 to 15. Note: This field must be less than or equal to the USB Maximum TX Burst Size field.
23:16	RW	0x00	USBMaxTxBurstSize USB Maximum TX Burst Size When USBTxPktCntSel is one, this field specifies the Maximum Bulk OUT burst the core can do. When the system bus is slower than the USB, TX FIFO can underrun during a long burst. You can program a smaller value to this field to limit the TX burst size that the core can execute. Host mode: It only applies to SS Bulk, Isochronous, and Interrupt OUT endpoints. Device mode: This value is not used in device mode, but users need to program a value when using the TX threshold feature to make sure that the value programmed in USBTxPktCnt is less than this value. Valid values are from 1 to 16.
15:0	RO	0x0000	reserved

USB3OTG_GRXTHRCFG

Address: **Operational Base** + offset (0xC10C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	usb_rx_pkt_cntsel USB ReceivePacket Count Enable. This field enables/disables the USB reception multi-packet thresholding: 1'b0: The core can only start reception on the USB when the RX FIFO has space for at least one packet. 1'b1: Not applied. If you are using external buffer control (EBC) feature, disable this mode by setting USBRxPktCntSel to 0.
28:13	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	resvl_socout_spc Space reserved in rx fifo for ISOC OUT. In host mode, this field is not applicable and must be programmed to 0. In device mode, this value represents the amount of space to be reserved for ISOC OUT packets. The value to be programmed should be chosen so as to ensure that non ISOC packets are not completely dropped, If no space needs to be reserved for ISOC OUT packets, program this field to 0. This field is valid only in device mode. The maximum configurable depth of rx fifo is 8192. Therefore, this field is 13 bits wide. For HS/FS, the space reservation is the actual value.

USB3OTG_GCTL

Address: **Operational Base** + offset (0xC110)

Bit	Attr	Reset Value	Description
31:19	RW	0x026a	pwrdnscale Not applied.
18	RW	0x0	masterfiltbypass Master Filter Bypass When this bit is set to 1'b1, all the filters are bypassed. The double synchronizers to mac_clk preceding the filters are also bypassed. For enabling the filters, this bit must be 1'b0.
17	RW	0x0	bypassetaddr Bypass SetAddress in Device Mode. When BYPSSETADDR bit is set, the device core uses the value in the DCFG[DevAddr] bits directly for comparing the device address in the tokens. For simulation, you can use this feature to avoid sending an actual SET ADDRESS control transfer on the USB, and make the device core respond to a new address. Note: You can set this bit for simulation purposes only. In the actual hardware, this bit must be set to 1'b0.
16	RW	0x1	u2rstecn Device controller on USB 2.0 reset checks for receiver termination eight times per attempt if this bit is set to zero, or only once per attempt if the bit is set to one. Note: This bit is applicable only in device mode.
15:14	RW	0x0	frmscldwn This field scales down device view of a SOF/USOF duration. For HS mode: Value of 2'h3 implements interval to be 15.625 us Value of 2'h2 implements interval to be 31.25 us Value of 2'h1 implements interval to be 62.5 us Value of 2'h0 implements interval to be 125us For FS mode, the scale-down value is multiplied by 8. This field also scales down the MaxPacketSize of the IN and OUT bulk endpoint to allow more traffic during simulation. It can only be changed from a non-zero value during simulation. 2'h0: 1024 bytes 2'h1: 512 bytes 2'h2: 256 bytes 2'h3: 128 bytes

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Bit	Attr	Reset Value	Description
13:12	RW	0x2	prtcapdir PRTCAPDIR: Port Capability Direction (PrtCapDir) 2'b01: for Host configurations 2'b10: for Device configurations SW should base on IDDIG input to set usb controller as an OTG 2.0 device with A-device or B-device.
11	RW	0x0	coresoftreset Core Soft Reset (CoreSoftReset) 1'b0: No soft reset; 1'b1: Soft reset to core Clears the interrupts and all the CSRs except the following registers: GCTL; GUCTL; GSTS; GSNPSID; GGPIO; GUID; GUSB2PHYCFGn registers; GUSB3PIPECTLn registers; DCFG; DCTL; DEVTEN; DSTS.
10	RW	0x0	sofitpsync Not applied.
9	RW	0x0	u1u2_timescale Not applied.
8	RW	0x0	debugattach Debug Attach. Not applied.
7:6	RW	0x0	ramclksel RAM Clock Select (RAMClkSel) 2'b00: bus clock 2'b01: pipe clock (Only used in device mode) 2'b10: In device mode, pipe/2 clock. In Host mode, controller switches ram_clk between pipe/2 clock, mac2_clk and bus_clk based on the status of the U2 ports 2'b11: In device mode, selects mac2_clk as ram_clk (when 8-bit UTMI or ULPI used. Not supported in 16-bit UTMI mode); In Host mode, controller switches ram_clk between pipe_clk, mac2_clk and bus_clk based on the status of the U2 ports. In device mode, upon a USB reset and USB disconnect, the hardware clears these bits to 2'b00.
5:4	RW	0x0	scaledown Scale-Down Mode (ScaleDown) When Scale-Down mode is enabled for simulation, the core uses scaled-down timing values, resulting in faster simulations. When Scale-Down mode is disabled, actual timing values are used. This is required for hardware operation. HS/FS/LS Modes: 2'b00: Disables all scale-downs. Actual timing values are used. 2'b01: Enables scale-down of all timing values except Device mode suspend and resume. These include Speed enumeration, HNP/SRP, and Host mode suspend and resume 2'b10: Enables scale-down of Device mode suspend and resume timing values only. 2'b11: Enables bit 0 and bit 1 scale-down timing values.
3	RW	0x0	disscramble Disable Scrambling (DisScramble) Transmit request to Link Partner on next transition to Recovery or Polling.

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Bit	Attr	Reset Value	Description
2	RW	0x1	u2exit_lfps If this bit is: 1'b0: the link treats 248ns LFPS as a valid U2 exit. 1'b1: the link waits for 8us of LFPS before it detects a valid U2 exit. This bit is added to improve interoperability with a third part host controller. This host controller in U2 state while performing receiver detection generates an LFPS glitch of about 4ms duration. This causes the device to exit from U2 state because the LFPS filter value is 248ns. With the new functionality enabled, the device can stay in U2 while ignoring this glitch from the host controller.
1	RO	0x0	gbl_hibernation_en This bit enables hibernation at the global level. If hibernation is not enabled through this bit, the PMU immediately accepts the D0->D3 and D3->D0 power state change requests, but does not save or restore any core state. In addition, the PMUs never drive the PHY interfaces and let the core continue to drive the PHY interfaces.
0	RW	0x0	dsblclkgtng Disable Clock Gating. This bit is set to 1 and the core is in Low Power mode, internal clock gating is disabled. You can set this bit to 1'b1 after Power On Reset.

USB3OTG_GSTS

Address: **Operational Base** + offset (0xC118)

Bit	Attr	Reset Value	Description
31:20	RO	0x7e8	cbelt Current BELT Value. In Host mode, this field indicates the minimum value of all received device BELT values and the BELT value that is set by the Set Latency Tolerance Value command.
19:12	RO	0x00	reserved
11	RO	0x0	SSIC_IP Not applied.
10	RO	0x0	OTG_IP OTG Interrupt Pending. This field indicates that there is a pending interrupt pertaining to OTG in OEVT register.
9	RO	0x0	bc_ip Battery Charger Interrupt Pending This field indicates that there is a pending interrupt pertaining to BC in BCEVT register.
8	RO	0x0	adp_ip ADP Interrupt Pending. This field indicates that there is a pending interrupt pertaining to ADP in ADPEVT register.
7	RO	0x0	host_ip Host Interrupt Pending. This field indicates that there is a pending interrupt pertaining to xHC in the Host event queue.
6	RO	0x0	device_ip Device Interrupt Pending This field indicates that there is a pending interrupt pertaining to peripheral (device) operation in the Device event queue.

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Bit	Attr	Reset Value	Description
5	W1C	0x0	csr_timeout When this bit is 1'b1, it indicates that the software performed a write or read to a core register that could not be completed within DWC_USB3_CSR_ACCESS_TIMEOUT bus clock cycles (default: h1FFFF).
4	W1C	0x0	buserraddrvld us Error Address Valid Indicates that the GBUSERRADDR register is valid and reports the first bus address that encounters a bus error.
3:2	RO	0x0	reserved
1:0	RO	0x0	curmod Current Mode of Operation.

USB3OTG_GUCTL1

Address: **Operational Base** + offset (0xC11C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	filter_se0_fsls_eop 1'b0: Default behaviour, no change in Linestate check for SE0 detection in FS/LS. 1'b1: Feature enabled, FS/LS SE0 is filtered for 2 clocks for detecting EOP. This bit is applicable for FS/LS operation. If this feature is enabled, then SE0 on the Linestate is validated for 2 consecutive utmi/ulpi clock edges for EOP detection. This feature is applicable only in FS in device mode and FS/LS mode of operation in host mode. Device mode: FS - If GUCTL1.FILTER_SE0_FSLS_EOP is set, then for device LPM handshake, the core will ignore single SE0 glitch on the Linestate during transmit. Only 2 or more SE0 is considered as a valid EOP on FS. Host mode: FS/LS - If GUCTL1.FILTER_SE0_FSLS_EOP is set, then the core will ignore single SE0 glitch on the Linestate during transmit. Only 2 or more SE0 is considered as a valid EOP on FS/LS port. Enable this feature if the Linestate has SE0 glitches during transmission. This bit is quasi-static, i.e., should not be changed during device operation.

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Bit	Attr	Reset Value	Description
28	RW	0x0	tx_ipgap_linecheck_dis 1'b0: Default behavior, no change in Linestate check. 1'b1: Feature enable, 2.0 MAC disables Linestate check during HS transmit. This bit is applicable for HS operation of u2mac. If this feature is enabled, then the 2.0 mac operating in HS ignores the UTMI/ULPI Linestate during the transmit of a token (during token-to-token and token-to-data IPGAP). When enabled, the controller implements a fixed 40-bit TxEndDelay after the packet is given on UTMI and ignores the Linestate during this time. This feature is applicable only in HS mode of operation. Device mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then for device LPM handshake, the core will ignore the Linestate after TX and wait for a fixed clocks (40 bit times equivalent) after transmitting ACK on utmi. Host mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then the ipgap between (tkn to tkn/data) is added by 40 bit times of TXENDDELAY, and linestate is ignored during this 40 bit times delay. Enable this bit if the LineState will not reflect the expected line state (J) during transmission. This bit is quasi-static, i.e., should not be changed during device operation.
27	RW	0x0	dev_trb_out_spr_ind 1'b0: Default behavior, no change in TRB status dword. 1'b1: Feature enable, OUT TRB status indicates Short Packet. This bit is applicable for device mode only (and ignored in host mode). If the device application (SW/HW) wants to know if a short packet was received for an OUT in the TRB status itself, then this feature can be enabled, so that a bit is set in the TRB writeback in the buf_size dword. Bit[26] - SPR of the trbstatus, RSVD, SPR,PCM1, bufsize dword will be set during an OUT transfer TRB write back if this is the last TRB used for that transfer descriptor. This bit is quasi-static, i.e., should not be changed during device operation.
26	RW	0x0	dve_force_20clk_for_30clk Not applied.
25	RW	0x0	p3_in_u2 Not applied.

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Bit	Attr	Reset Value	Description
24	RW	0x0	dev_l1_exit_by_hw 1'b0: Default behavior, disables device L1 hardware exit logic. 1'b1: Feature enabled This bit is applicable for device mode (2.0) only. This field enables device controller sending remote wakeup for L1 if the device becomes ready for sending/accepting data when in L1 state. If the host expects the device to send remote wkp signaling to resume after going into L1 in flow controlled state, then this bit can be set to send the remote wake signal automatically when the device controller becomes ready. This HW remote wake feature is applicable only to bulk and interrupt transfers, and not for Isoch/Control When control transfers are in progress, the LPM will be rejected (NYET response). Only after control transfers are completed (either with ACK/STALL), LPM will be accepted For Isoch transfers, the host needs to do the wake-up and start the transfer. Device controller will not do remote-wakeup when Isoch endpoints get ready. The device SW needs to keep the GUSB2PHYCFG[EnblSlpM] reset in order to keep the PHY clock to be running for keeping track of SOF intervals. When L1 hibernation is enabled, the controller will not do automatic exit for hibernation requests thru L1. This bit is quasi-static, i.e., should not be changed during device operation.
23:21	RW	0x0	ip_gap_add_on This register field is used to add on to the default inter packet gap setting in the USB 2.0 MAC.
20	RW	0x0	dev_lsp_tail_lock_dis 1'b0: Default behaviour, enables device lsp lock logic for tail TRB update. 1'b1: Fix disabled This is a bug fix for STAR 9000716195 that affects the CSP mode for OUT endpoints in device mode. The issue is that tail TRB index is not synchronized with the cache Scratchpad bytecount update. If the fast-forward request comes in-between the bytecount update on a newly fetched TRB and the tail-index write update in TPF, the RDP works on an incorrect tail index and misses the byte count decrement for the newly fetched TRB in the fast-forwarding process. This fix needs to be present all the times.
19	RW	0x0	nak_per_enh_fs 1'b1: Enables performance enhancement for FS async endpoints in the presence of NAKs. 1'b0: Enhancement not applied. If a periodic endpoint is present, and if a bulk endpoint which is also active is being NAKed by the device, then this could result in a decrease in performance of other Full Speed bulk endpoint which is ACKed by the device. Setting this bit to 1, will enable the host controller to schedule more transactions to the async endpoints (bulk/ control) and hence will improve the performance of the bulk endpoint. This control bit should be enabled only if the existing performance with the default setting is not sufficient for your FullSpeed application. Setting this bit will only control, and is only required for Full Speed transfers.

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Bit	Attr	Reset Value	Description
18	RW	0x1	nak_per_enh_hs 1'b1: Enables performance enhancement for HS async endpoints in the presence of NAKs. 1'b0: Enhancement not applied. If a periodic endpoint is present, and if a bulk endpoint which is also active is being NAKed by the device, then this could result in a decrease in performance of other High Speed bulk endpoint which is ACKed by the device. Setting this bit to 1, will enable the host controller to schedule more transactions to the async endpoints (bulk/ control) and hence will improve the performance of the bulk endpoint. This control bit should be enabled only if the existing performance with the default setting is not sufficient for your HighSpeed application. Setting this bit will only control, and is only required for High Speed transfers.
17	RW	0x0	parkmode_disbale_ss Not applied.
16	RW	0x0	parkmode_disable_hs This bit is used only in host mode. When this bit is set to 1 all HS bus instances park mode are disabled. To improve performance in park mode, the xHCI scheduler queues in three requests of 4 packets each for High Speed asynchronous endpoints in a micro-frame. But if a device is slow and if it NAKs more than 3 times, then it is rescheduled only in the next micro-frame. This could decrease the performance of a slow device even further. In a few High Speed devices (such as Sandisk Cruzer Blade 4GB VID: 1921, PID: 21863 and Flex Drive VID: 3744, PID: 8552) when an IN request is sent within 900ns of the ACK of the previous packet, these devices send a NAK. When connected to these devices, if required, the software can disable the park mode if you see performance drop in your system. When park mode is disabled, pipelining of multiple packet is disabled and instead one packet at a time is requested by the scheduler. This allows up to 12 NAKs in a micro-frame and improves performance of these slow devices.
15	RW	0x0	parkmod_disavale_fsls This bit is used only in host mode, and is for debug purpose only. When this bit is set to 1 all FS/LS bus instances in park mode disabled.
14:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x1	l1_susp_thrld_en_for_host This bit is used only in host mode. The host controller asserts the utmi_l1_suspend_n and utmi_sleep_n output signals (see LPM Interface Signals table in the Databook) as follows: The controller asserts the utmi_l1_suspend_n signal to put the PHY into deep low-power mode in L1 when both of the following are true: The HIRD/BESL value used is greater than or equal to the value in L1_SUSP_THRLD_FOR_HOST field. The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b1. The controller asserts utmi_sleep_n on L1 when one of the following is true: The HIRD/BESL value used is less than the value in L1_SUSP_THRLD_FOR_HOST field. The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b0.
7:4	RW	0x8	l1_susp_thrld_for_host This field is effective only when the L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1. For more details, refer to the description of the L1_SUSP_THRLD_EN_FOR_HOST bit.
3	RW	0x1	hc_errata_enable Not applied.
2	RW	0x0	hc_parchk_disable Host Parameter Check Disable. When this bit is set to 0 (by default), the xHC checks that the input slot/EP context fields comply to the xHCI Specification. Upon detection of a parameter error during command execution, the xHC generates an event TRB with completion code indicating PARAMETER ERROR. When the bit is set to 1, the xHC does not perform parameter checks and does not generate PARAMETER ERROR completion code.
1	RW	0x1	ovrld_l1_susp_com If this bit is set, the utmi_l1_suspend_com_n is overloaded with the utmi_sleep_n signal. This bit is usually set if the PHY stops the port clock during L1 sleep condition.
0	RW	0x0	loa_filter_en If this bit is set, the USB 2.0 port babble is checked at least three consecutive times before the port is disabled. This prevents false triggering of the babble condition when using low quality cables. Note: This bit is valid only in host mode.

USB3OTG_GSNPSID

Address: **Operational Base** + offset (0xC120)

Bit	Attr	Reset Value	Description
31:0	RO	0x5533300a	snpsid SNPSID[31:16] indicates Core Identification Number. 0x5533 is ASCII for U3 (DWC_usb3). SNPSID[15:0] indicates the release number. Current Release is 3.00a. Software uses this register to configure release-specific features in the driver.

USB3OTG_GGPIO

Address: **Operational Base** + offset (0xC124)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	gpo General Purpose Output This field's value is driven out on the gp_out[15:0] core output port.
15:0	RO	0x0000	gpi General Purpose Input This field's read value reflects the gp_in[15:0] core input value.

USB3OTG_GUID

Address: **Operational Base** + offset (0xC128)

Bit	Attr	Reset Value	Description
31:0	RW	0x20190520	userid Application-programmable ID field.

USB3OTG_GUCTL

Address: **Operational Base** + offset (0xC12C)

Bit	Attr	Reset Value	Description
31:22	RW	0x008	refclkper This field indicates in terms of nano seconds the period of ref_clk. The default value of this register is set to 'h8 (8ns/125 MHz). This field needs to be updated during power-on initialization, if GCTL.SOFITPSYNC or GFLADJ.GFLADJ_REFCLK_LPM_SEL is set to 1. The programmable maximum value is 62ns, and the minimum value is 8ns. You must use a reference clock with a period that is an integer multiple, so that ITP can meet the jitter margin of 32ns. The allowable ref_clk frequencies whose period is not integer multiples are 16/17/19.2/24/39.7MHz. This field must not be set to 0 at any time. If you never plan to use this feature, then set this field to 'h8, the default value.
21	RW	0x0	no_extr_di No Extra Delay Between SOF and the First. Some HS devices misbehave when the host sends a packet immediately after a SOF. However, adding an extra delay between a SOF and the first packet can reduce the USB data rate and performance. This bit is used to control whether the host must wait for 2 microseconds before it sends the first packet after a SOF, or not. User can set this bit to one to improve the performance if those problematic devices are not a concern in the user's host environment. 1'b0: Host waits for 2 microseconds after a SOF before it sends the first USB packet. 1'b1: Host doesn't wait after a SOF before it sends the first USB packet.
20:18	RO	0x0	reserved
17	RW	0x0	sprs_ctrl_trans_en Sparse Control Transaction Enable. Some devices are slow in responding to Control transfers. Scheduling multiple transactions in one microframe/frame can cause these devices to misbehave. If this bit is set to 1'b1, the host controller schedules transactions for a Control transfer in different microframes/frames.

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Bit	Attr	Reset Value	Description
16	RW	0x0	res_bw_hs_esp Reserving 85% Bandwidth for HS Periodic EPs. By default, HC reserves 80% of the bandwidth for periodic EPs. If this bit is set, the bandwidth is relaxed to 85% to accommodate two high speed, high bandwidth ISOC EPs. USB 2.0 required 80% bandwidth allocated for ISOC traffic. If two High-bandwidth ISOC devices (HD Webcams) are connected, and if each requires 1024-bytes X 3 packets per Micro-Frame, then the bandwidth required is around 82%. If this bit is set, then it is possible to connect two Webcams of 1024bytes X 3 payload per Micro-Frame each. Otherwise, you may have to reduce the resolution of the Webcams. This bit is valid in Host and DRD configuration and is used in host mode operation only. Ignore this bit in device mode.
15	RW	0x1	cm_dev_addr Compliance Mode for Device Address. When this bit is 1'b1, Slot ID may have different value than Device Address if max_slot_enabled < 128. 1'b1: Increment Device Address on each Address Device command. 1'b0: Device Address is equal to Slot ID. The xHCI compliance requires this bit to be set to 1. The 0 mode is for debug purpose only. This allows you to easily identify a device connected to a port in the Lecroy or Eliisys trace during hardware debug. This bit is valid in Host and DRD configuration and is used in host mode operation only. Ignore this bit in device mode.
14	RW	0x0	usb_host_in_auto_retry_en Host IN Auto Retry. 1'b0: Auto Retry Disabled 1'b1: Auto Retry Enabled Note: This bit is also applicable to the device mode.
13	RW	0x0	en_overlap_chk Not applied.

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Bit	Attr	Reset Value	Description
12	RW	0x0	ext_cap_suppt_en External Extended Capability Support Enable When set, this field enables extended capabilities to be implemented outside the core. When the ExtCapSupEN is set and the Debug Capability is enabled, the Next Capability pointer in Debug Capability returns 16. A read to the first DWORD of the last internal extended capability (the "xHCI Supported Protocol Capability for USB 3.0" when the Debug Capability is not enabled) returns a value of 4 in the Next Capability Pointer field. This indicates to software that there is another capability four DWORDs after this capability (for example, at address N+16 where N is the address of this DWORD). If enabled, an external address decoder that snoops the xHC slave interface must be implemented. If it sees an access to N+16 or greater, the slave access is re-routed to a piece of hardware which returns the external capability pointer register of the new capability and also handles reads/writes to this new capability and the side effects. If disabled, a read to the first DWORD of the last internal extended capability returns 0 in the 'Next Capability Pointer' field. This indicates there are no more capabilities.
11	RW	0x0	insrt_extr_fsbodi Insert Extra Delay Between FS Bulk OUT. Some FS devices are slow to receive Bulk OUT data and can get stuck when there are consecutive Bulk OUT transactions with short inter-transaction delays. This bit is used to control whether the host inserts extra delay between consecutive Bulk OUT transactions to a FS Endpoint. 1'b0: Host doesn't insert extra delay between consecutive Bulk OUT transactions to a FS Endpoint. 1'b1: Host inserts about 12us extra delay between consecutive Bulk OUT transactions to a FS Endpoint to work around the device issue. Note: Setting this bit to one will reduce the Bulk OUT transfer performance for most of the FS devices.
10:9	RW	0x0	dtct Device Timeout Coarse Tuning. This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. The core first checks the DTCT value. If it is 0, then the timeout value is defined by the DTFT. If it is non-zero, then it uses the following timeout values: 2'b00: 0 usec -> use DTFT value instead 2'b01: 500 usec 2'b10: 1.5 msec 2'b11: 6.5 msec

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Bit	Attr	Reset Value	Description
8:0	RW	0x010	ctft Device Timeout Fine Tuning. This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. For the DTFT field to take effect, DTCT must be set to 2'b00. The DTFT value is the number of 125 MHz clocks * 256 to count before considering a device timeout. The minimum value of DTFT is 2. For example, if the mac3_clk is 125 MHz clk (8 ns period), this is calculated as follows: (DTFT value) * 256 * (8 ns) Quick Reference: if DTFT = 0x2, 2*256*8 = 4usec timeout if DTFT = 0x5, 5*256*8 = 10usec timeout if DTFT = 0xA, 10*256*8 = 20usec timeout if DTFT = 0x10, 16*256*8 = 32usec timeout if DTFT = 0x19, 25*256*8 = 51usec timeout if DTFT = 0x31, 49*256*8 = 100usec timeout if DTFT = 0x62, 98*256*8 = 200usec timeout

USB3OTG_GBUSERRADDRLO

Address: **Operational Base** + offset (0xC130)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	buserraddr Bus Address - Low. This register contains the lower 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the core. Note: Only supported in AHB and AXI configurations.

USB3OTG_GBUSERRADDRHI

Address: **Operational Base** + offset (0xC134)

Bit	Attr	Reset Value	Description
31:0	RU	0x00000000	buserraddr Bus Address - High. This register contains the higher 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the core. Note: Only supported in AHB and AXI configurations.

USB3OTG_GPRTBIMAPLO

Address: **Operational Base** + offset (0xC138)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	BINUM1 SS USB Instance Number for Port 1 Application-programmable ID field.

USB3OTG_GHWPARAMS0

Address: **Operational Base** + offset (0xC140)

Bit	Attr	Reset Value	Description
31:0	RO	0x2020400a	ghwparams0 Global Hardware Parameters Register 0.

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USB3OTG_GHWPARAMS1

Address: **Operational Base** + offset (0xC144)

Bit	Attr	Reset Value	Description
31:0	RO	0x0120c93b	ghwparams1 Global Hardware Parameters Register 1.

USB3OTG_GHWPARAMS2

Address: **Operational Base** + offset (0xC148)

Bit	Attr	Reset Value	Description
31:0	RO	0x20190520	ghwparams2 Global Hardware Parameters Register 2.

USB3OTG_GHWPARAMS3

Address: **Operational Base** + offset (0xC14C)

Bit	Attr	Reset Value	Description
31:0	RO	0x069cd084	ghwparams3 Global Hardware Parameters Register 3.

USB3OTG_GHWPARAMS4

Address: **Operational Base** + offset (0xC150)

Bit	Attr	Reset Value	Description
31:0	RO	0x47822010	ghwparams4 Global Hardware Parameters Register 4.

USB3OTG_GHWPARAMS5

Address: **Operational Base** + offset (0xC154)

Bit	Attr	Reset Value	Description
31:0	RO	0x04204018	ghwparams5 Global Hardware Parameters Register 5.

USB3OTG_GHWPARAMS6

Address: **Operational Base** + offset (0xC158)

Bit	Attr	Reset Value	Description
31:0	RO	0x09d78020	ghwparams6 Global Hardware Parameters Register 6.

USB3OTG_GHWPARAMS7

Address: **Operational Base** + offset (0xC15C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ghwparams7 Global Hardware Parameters Register 7.

USB3OTG_GDBGFIFOSPACE

Address: **Operational Base** + offset (0xC160)

Bit	Attr	Reset Value	Description
31:16	RO	0x000a	space_available Space Available.
15:9	RO	0x00	reserved
8:0	RW	0x000	fifo_queue_select FIFO/Queue Select (or) Port-Select. FIFO/Queue Select[8:5] indicates the FIFO/Queue Type. FIFO/Queue Select[4:0] indicates the FIFO/Queue Number. Port-Select[3:0] selects the port-number when accessing GDBGLTSSM register.

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USB3OTG_GDBGLNMCC

Address: **Operational Base** + offset (0xC168)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RO	0x000	lnmcc_berc This field indicates the bit error rate information for the port selected in the GDBGFIFOSPACE.PortSelect field. This field is for debug purposes only.

USB3OTG_GDBGBMU

Address: **Operational Base** + offset (0xC16C)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	bmu_bcu BMU_BCU Debug information.
7:4	RO	0x0	bmu_dcu BMU_DCU Debug information.
3:0	RO	0x0	bmu_ccu BMU_CCU Debug information.

USB3OTG_GDBGLSPMUX

Address: **Operational Base** + offset (0xC170)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x3f	logic_analyzer_trace Logic Analyzer Trace Port MUX Select. Currently only bits[21:16] are used. A value of 6'h3F drives "0"s on the logic_analyzer_trace signal. If you plan to OR (instead using a mux) this signal with other trace signals in your system to generate a common trace signal, you can use this feature.
15	RW	0x0	endbc Enable debugging of Debug capability LSP in Host mode. Use HostSelect to select DbC LSP debug information presented in the GDBGLSP register.
14	RO	0x0	reserved
13:8	RW	0x00	hostselect Host LSP Select. Selects the LSP debug information presented in the GDBGLSP register in host mode.
7:4	RW	0x0	devselect Device LSP Select. Selects the LSP debug information presented in the GDBGLSP register in device mode. Or bit[7:4] of HOSTSELECT, Selects the LSP debug information presented in the GDBGLSP register in host mode.
3:0	RW	0x0	epselect Device Endpoint Select. Selects the Endpoint debug information presented in the GDBGEPINFO registers in device mode. Or bit[3:0] of HOSTSELECT, Selects the LSP debug information presented in the GDBGLSP register in host mode.

USB3OTG_GDBGLSP

Address: **Operational Base** + offset (0xC174)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lspdebug LSP Debug Information.

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USB3OTG_GDBGEPINFO0

Address: **Operational Base** + offset (0xC178)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	epdebug Endpoint Debug Information Low 32-bit.

USB3OTG_GDBGEPINFO1

Address: **Operational Base** + offset (0xC17C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00800000	epdebug Endpoint Debug Information High 32-bit.

USB3OTG_GPRTBIMAP_HSLO

Address: **Operational Base** + offset (0xC180)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	binum1 HS USB Instance Number for Port 1. Application-programmable ID field.

USB3OTG_GPRTBIMAP_FSLO

Address: **Operational Base** + offset (0xC188)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	binum1 FS USB Instance Number for Port 1. Application-programmable ID field.

USB3OTG_GUSB2PHYCFG0

Address: **Operational Base** + offset (0xC200)

Bit	Attr	Reset Value	Description
31	RW	0x0	physoftrst UTMI PHY Soft Reset. Causes the usb2phy_reset signal to be asserted to reset a UTMI PHY. Not applicable to ULPI because ULPI PHYs are reset via their FunctionControl. Reset register, and the core automatically writes to this register when the core is reset (vcc_reset_n, USBCMD.HCRST, DCTL.SoftReset, or GCTL.SoftReset).
30	RW	0x1	u2_freeclk_exists Specifies whether your USB 2.0 PHY provides a free-running PHY clock, which is active when the clock control input is active. If your USB 2.0 PHY provides a free-running PHY clock, it must be connected to the utmi_clk[0] input. The remaining utmi_clk[n] must be connected to the respective port clocks. The core uses the Port-0 clock for generating the internal mac2 clock. 1'b0: USB 2.0 free clock does not exist 1'b1: USB 2.0 free clock exists Note: When the core is configured as device-only, do not set this bit to 1.
29:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24:22	RW	0x0	lstrd LS Turnaround Time. This field indicates the value of the Rx-to-Tx packet gap for LS devices. The encoding is as follows: 3'h0: 2 bit times 3'h1: 2.5 bit times 3'h2: 3 bit times 3'h3: 3.5 bit times 3'h4: 4 bit times 3'h5: 4.5 bit times 3'h6: 5 bit times 3'h7: 5.5 bit times Note: This field is applicable only in Host mode. For normal operation (to work with most LS devices), set the default value of this field to 3'h0 (2 bit times). The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the Open LS mouse requires 3 bit times of inter-packet gap to work correctly.
21:19	RW	0x2	lsipd LS Inter-Packet Time. This field indicates the value of Tx-to-Tx packet gap for LS devices. The encoding is as follows: 3'h0: 2 bit times 3'h1: 2.5 bit times 3'h2: 3 bit times 3'h3: 3.5 bit times 3'h4: 4 bit times 3'h5: 4.5 bit times 3'h6: 5 bit times 3'h7: 5.5 bit times Note: This field is applicable only in Host mode. For normal operation (to work with most LS devices), set the default value of this field to 3'h2 (3 bit times). The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the AOpen LS mouse requires 3 bit times of inter-packet gap to work correctly.
18:14	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
13:10	RW	0x9	usbtrdim USB 2.0 Turnaround Time. Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM). The following are the required values for the minimum SoC bus frequency of 60 MHz. USB turnaround time is a critical certification criteria when using long cables and five hub levels. The required values for this field: 4'h5: When the MAC interface is 16-bit UTMI+. 4'h9: When the MAC interface is 8-bit UTMI+/ULPI. If SoC bus clock is less than 60 MHz, and USB turnaround time is not critical, this field can be set to a larger value. Note: This field is valid only in device mode.
9	RW	0x0	xcvrdly Transceiver Delay. Enables a delay between the assertion of the UTMI/ULPI Transceiver Select signal (for HS) and the assertion of the TxValid signal during a HS Chirp. When this bit is set to 1, a delay (of approximately 2.5 us) is introduced from the time when the Transceiver Select is set to 2'b00 (HS) to the time the TxValid is driven to 0 for sending the chirp-K. This delay is required for some UTMI/ULPI PHYs. Note: If you enable the hibernation feature when the device core comes out of power-off, you must re-initialize this bit with the appropriate value because the core does not save and restore this bit value during hibernation. This bit is valid only in device mode.
8	RW	0x0	enblslpm Enable utmi_sleep_n and utmi_l1_suspend_n. The application uses this bit to control utmi_sleep_n and utmi_l1_suspend_n assertion to the PHY in the L1 state. 1'b0: utmi_sleep_n and utmi_l1_suspend_n assertion from the core is not transferred to the external PHY. 1'b1: utmi_sleep_n and utmi_l1_suspend_n assertion from the core is transferred to the external PHY. Note: This bit must be set high for Port0 if SNPS PHY is used. In Device mode - Before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. Without disabling this bit, if a command is issued when the device is in L1 state and if mac2_clk (utmi_clk/ulpi_clk) is gated off, the command will not get completed.
7	RO	0x0	physel USB 2.0 High-Speed PHY or USB 1.1 Full-Speed. 1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY. 1'b1: USB 1.1 full-speed serial transceiver.

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Bit	Attr	Reset Value	Description
6	RW	0x0	suspendusb20 Suspend USB2.0 HS/FS/LS PHY. When set, USB2.0 PHY enters Suspend mode if Suspend conditions are valid. If it is set to 1, then the application must clear this bit after power-on reset. Application needs to set it to 1 after the core initialization completes. For all other configurations, this bit can be set to 1 during core configuration. Note: In host mode, on reset, this bit is set to 1. Software can override this bit after reset. In device mode, before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. If you issue a command without disabling this bit when the device is in L2 state and if mac2_clk (utmi_clk/ulpi_clk) is gated off, the command will not get completed.
5	RO	0x0	reserved
4	RO	0x0	ulpi_utmi_sel ULPI or UTMI+ Select. 1'b0: UTMI+ Interface 1'b1: ULPI Interface
3	RW	0x0	phyif If UTMI+ is selected, the application uses this bit to configure the core to support a UTMI+ PHY with an 8- or 16-bit interface. 1'b0: 8 bits 1'b1: 16 bits
2:0	RW	0x0	tout_cal HS/FS Timeout Calibration. The number of PHY clocks, as indicated by the application in this field, is multiplied by a bit-time factor; this factor is added to the high-speed/full-speed interpacket timeout duration in the core to account for additional delays introduced by the PHY. This may be required, since the delay introduced by the PHY in generating the linestate condition may vary among PHYs. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The application must program this field based on the speed of connection. The number of bit times added per PHY clock are: High-speed operation: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full-speed operation: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times

USB3OTG_GUSB3PIPECTL0

Address: **Operational Base** + offset (0xC2C0)

Bit	Attr	Reset Value	Description
31	RW	0x0	PHYSoftRst USB3 PHY Soft Reset After setting this bit to 1, the software needs to clear this bit.

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Bit	Attr	Reset Value	Description
30	RW	0x0	HstPrtCmpl This feature tests the PIPE PHY compliance patterns without having to have a test fixture on the USB 3.0 cable. This bit enables placing the SS port link into a compliance state. By default, this bit must be set to 1'b0. In compliance lab testing, the SS port link enters compliance after failing the first polling sequence after power on. Set this bit to 0, when you run compliance tests. The sequence for using this functionality is as follows: 1. Disconnect any plugged in devices. 2. Perform USBCMD.HCRST or power-on-chip reset. 3. Set PORTSC.PP=0. 4. Set GUSB3PIPECTL. HstPrtCmpl=1. This places the link into compliance state. To advance the compliance pattern, follow this sequence (toggle the set GUSB3PIPECTL. HstPrtCmpl): 1. Set GUSB3PIPECTL.HstPrtCmpl=0. 2. Set GUSB3PIPECTL.HstPrtCmpl=1. This advances the link to the next compliance pattern. To exit from the compliance state perform USBCMD.HCRST or power-on-chip reset.
29	RW	0x0	U2SSInactP3ok 1'b0: During link state U2/SS.Inactive, put PHY in P2 (Default) 1'b1: During link state U2/SS.Inactive, put PHY in P3
28	RW	0x0	DisRxDetP3 Disabled receiver detection in P3 1'b0: If PHY is in P3 and Core needs to perform receiver detection, The core performs receiver detection in P3. (Default) 1'b1: If PHY is in P3 and Core needs to perform receiver detection, The core changes the PHY power state to P2 and then performs receiver detection. After receiver detection, the cores changes PHY power state to P3.
27	RW	0x0	Ux_exit_in_Px 1'b0: The core does U1/U2/U3 exit in PHY power state P0 (default behavior). 1'b1: The core does U1/U2/U3 exit in PHY power state P1/P2/P3 respectively.
26	RW	0x0	ping_enhancement_en Ping Enhancement Enable When set, the Downstream port U1 ping receive timeout becomes 500 ms instead of 300 ms. Minimum Ping.LFPS receive duration is 8 ns (one mac3_clk). This field is valid for the downstream port only.
25	RW	0x0	u1u2exitfail_to_recov U1U2exitfail to Recovery When set, and U1/U2 LFPS handshake fails, the LTSSM transitions from U1/U2 to Recovery instead of SS Inactive. If Recovery fails, then the LTSSM can enter SS.Inactive. This is an enhancement only. It prevents interoperability issue if the remote link does not do proper handshake.

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Bit	Attr	Reset Value	Description
24	RW	0x0	request_p1p2p3 Always Request P1/P2/P3 for U1/U2/U3 When set, the core always requests PHY power change from P0 to P1/P2/P3 during U0 to U1/U2/U3 transition. If this bit is 0, and immediate Ux exit (remotely initiated, or locally initiated) happens, the core does not request P1/P2/P3 power state change.
23	RW	0x0	StartRxDetU3RxDet Start Receiver Detection in U3/Rx.Detect (StartRxdetU3RxDet) If DWC_USB3_GUSB3PIPECTL_INIT[22] is set, and the link is in either U3 or Rx.Detect state, the core starts receiver detection on the rising edge of this bit. This can only be used for Downstream ports. This bit must be set to '0' for Upstream ports. This feature must not be enabled for normal operation.
22	RW	0x0	DisRxDetU3RxDet Disable Receiver Detection in U3/Rx.Det When set, the core does not handle receiver detection in either U3 or Rx.Detect states. DWC_USB3_GUSB3PIPECTL_INIT[23] must be used to start receiver detection manually. This bit can only be used for the downstream port. This bit must be set to 0 for Upstream ports. This feature must not be enabled for normal operation. If you have to use this feature, contact SNPS.
21:19	RW	0x0	DelayP1P2P3 Delay P1P2P3 Delay P0 to P1/P2/P3 request when entering U1/U2/U3 until (DWC_USB3_GUSB3PIPECTL_INIT[21:19]*8) 8B10B error occurs, or Pipe3_RxValid drops to 0. DWC_USB3_GUSB3PIPECTL_INIT[18] must be 1 to enable this functionality.
18	RW	0x0	DELAYP1TRANS DELAYP1TRANS Delay PHY power change from P0 to P1/P2/P3 when link state changing from U0 to U1/U2/U3 respectively. 1'b1: When entering U1/U2/U3, delay the transition to P1/P2/P3 until the pipe3 signals, Pipe3_RxElecIlde is 1 and pipe3_RxValid is 0 1'b0: When entering U1/U2/U3, transition to P1/P2/P3 without checking for Pipe3_RxElecIlde and pipe3_RxValid. Note: This bit must be set to '1' for SNPS PHY. It is also used by third-party SS PHY.
17	RO	0x0	reserved
16:15	RW	0x0	DATWIDTH 2'b00: 32 bits 2'b01: 16 bits 2'b10: 8 bits One clock after reset, these bits receive the value seen on the pipe3_DataBusWidth.
14	RW	0x0	AbortRxDetInU2 Abort Rx Detect in U2 (AbortRxDetInU2) When set, and the link state is U2, then the core will abort receiver detection if it receives U2 exit LFPS from the remote link partner. This bit is for the downstream port only.

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Bit	Attr	Reset Value	Description
13	RW	0x0	SkipRxDet Skip Rx Detect: When set, the core skips Rx Detection if pipe3_RxElecIdle is low. Skip is defined as waiting for the appropriate timeout, then repeating the operation.
12	RW	0x0	LFPSP0Algn LFPS P0 Align When set: 1. The core deasserts LFPS transmission on the clock edge that it requests Phy power state 0 when exiting U1, U2, or U3 low power states. Otherwise, LFPS transmission is asserted one clock earlier. 2. The core requests symbol transmission two pipe3_rx_pclks periods after the PHY asserts PhyStatus as a result of the PHY switching from P1 or P2 state to P0 state.
11	RW	0x0	P3P2TranOK P3 P2 Transitions OK (P3P2TranOK) When set, the core transitions directly from Phy power state P2 to P3 or from state P3 to P2. When not set, P0 is always entered as an intermediate state during transitions between P2 and P3, as defined in the PIPE3 Specification. According to the PIPE3 Specification, any direct transition between P3 and P2 is illegal.
10	RW	0x0	P3ExSigP2 P3 Exit Signal in P2 When this bit is set, the core always changes the PHY power state to P2, before attempting a U3 exit handshake. This bit is used only for some non-SNPS PHYs that cannot do LFPS in P3. Note: This bit is used by third-party SS PHY. It must be set to '0' for SNPS PHY.
9	RW	0x0	LFPSFILTER LFPS Filter When set, filter LFPS reception with pipe3_RxValid in PHY power state P0, that is, ignore LFPS reception from the PHY unless both pipe3_Rxelecidle and pipe3_RxValid are deasserted.
8	RW	0x0	RX_DETECT_to_Polling_L RX_DETECT to Polling.LFPS Control 1'b0 (Default): Enables a 400us delay to start Polling LFPS after RX_DETECT. This allows VCM offset to settle to a proper level. 1'b1: Disables the 400us delay to start Polling LFPS after RX_DETECT. During controller certification with third party PHY it is observed that the PHY is not able to meet the Tx AC common mode voltage active (VTX-CM-ACPP_ACTIVE <100mv) if the link starts polling within 80us from the time rx.detect is performed. To meet this VTX-CM-ACPP_ACTIVE specification, the polling must be delayed further. If the PHY does not have issue then they can set this bit to 1 which allows polling to start within 80us.
7	RO	0x0	reserved
6	RW	0x0	TX_SWING Tx Swing (TxSwing) Refer to the PIPE3 specification.
5:3	RW	0x0	TX_MARGIN Tx Margin[2:0] (TxMargin) Refer to Table 5-3 of the PIPE3 Specification.

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Bit	Attr	Reset Value	Description
2:1	RW	0x0	TX_DE_EPPHASIS Tx Deemphasis The value driven to the PHY is controlled by the LTSSM during USB3 Compliance mode.
0	RW	0x0	ELASTIC_BUFFER_MODE Elastic Buffer Mode (ElasticBufferMode) (Refer to Table 5-3 of the PIPE3 specification.)

USB3OTG_GTXFIFOSIZn

Address: **Operational Base** + offset (0xC300)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	txfstaddr_n Transmit FIFOn RAM Start Address. This field contains the memory start address for TxFIFOn in 64-bit words.
15:0	RW	0x0042	txfdep_n TxFIFO Depth. This field contains the depth of TxFIFOn in 64-bit words. Minimum value: 32; Maximum value: 32,768.

USB3OTG_GRXFIFOSIZn

Address: **Operational Base** + offset (0xC380)

Bit	Attr	Reset Value	Description
31:16	RW	0x0334	rxfstaddr_n RxFIFOn RAM Start Address. This field contains the memory start address for RxFIFOn in 64-bit words.
15:0	RW	0x0185	rxfdep_n RxFIFOn RAM Start Address. This field contains the memory start address for RxFIFOn in 64-bit words.

USB3OTG_GEVNTADRLO0

Address: **Operational Base** + offset (0xC400)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	evntadrlo Event Buffer Address. Holds the lower 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address.

USB3OTG_GEVNTADRHI0

Address: **Operational Base** + offset (0xC404)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	evntadrhi Event Buffer Address. Holds the higher 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address.

USB3OTG_GEVNTSIZ0

Address: **Operational Base** + offset (0xC408)

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Bit	Attr	Reset Value	Description
31	RW	0x0	evntintrptmask Event Interrupt Mask. When set to '1', this prevents the interrupt from being generated. However, even when the mask is set, the events are queued.
30:16	RO	0x0000	reserved
15:0	RW	0x0000	eventsiz Event Buffer Size in bytes. Holds the size of the Event Buffer in bytes; must be a multiple of four. This is programmed by software once during initialization. The minimum size of the event buffer is 32 bytes.

USB3OTG_GEVNTCOUNT0

Address: **Operational Base** + offset (0xC40C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	evntcount Event Count. When read, returns the number of valid events in the Event Buffer (in bytes). When written, hardware decrements the count by the value written. The interrupt line remains high when count is not 0.

USB3OTG_GHWPARAMS8

Address: **Operational Base** + offset (0xC600)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000047c	ghwparams8_32_0 ghwparams8

USB3OTG_GTXFIFOPRIDEV

Address: **Operational Base** + offset (0xC610)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	gtxfifopridev Device TxFIFO priority. This register specifies the relative DMA priority level among the Device TXFIFOs (one per IN endpoint). Each register bit[n] controls the priority (1: high, 0: low) of each TXFIFO[n]. When multiple TXFIFOs compete for DMA service at a given time (that is, multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: 1. High-priority TXFIFOs are granted access using round-robin arbitration 2. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. When configuring periodic IN endpoints, software must set register bit[n]=1, where n is the TXFIFO assignment. This ensures that the DMA for isochronous or interrupt IN endpoints are prioritized over bulk or control IN endpoints. This register is present only when the core is configured to operate in the device mode. The register size corresponds to the number of Device IN endpoints.

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USB3OTG_GTXFIFOPRIHST

Address: **Operational Base** + offset (0xC618)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	gtxfifoprihst Host TxFIFO priority. This register specifies the relative DMA priority level among the Host TXFIFOs (one per USB bus instance) within the associated speed group (HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of TXFIFO[n] within a speed group. When multiple TXFIFOs compete for DMA service at a given time (i.e., multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: 1. Among the FIFOs in the same speed group (HS/FSLS): a. High-priority TXFIFOs are granted access using round-robin arbitration b. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). 2. The TX DMA arbiter prioritizes the HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. This register is present only when the core is configured to operate in the host mode (includes DRD and OTG modes). The register size corresponds to the number of configured USB bus instances; for example, in the default configuration, there are 2 USB bus instances (1 HS, and 1 FSLS).

USB3OTG_GRXFIFOPRIHST

Address: **Operational Base** + offset (0xC61C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	grxfifoprihst Host RxFIFO priority This register specifies the relative DMA priority level among the Host RXFIFOs (one per USB bus instance) within the associated speed group (HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of RXFIFO[n] within a speed group. When multiple RXFIFOs compete for DMA service at a given time (i.e., multiple RXQs contain RX DMA requests and their corresponding RXFIFOs have data available), the RX DMA arbiter grants access on a packet-basis in the following manner: 1. Among the FIFOs in the same speed group (HS/FSLS): a. High-priority RXFIFOs are granted access using round-robin arbitration b. Low-priority RXFIFOs are granted access using round-robin arbitration only after high-priority RXFIFOs have no further processing to do (that is, either the RXQs are empty or the corresponding RXFIFOs do not have the required data). 2. The RX DMA arbiter prioritizes the HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. This register is present only when the core is configured to operate in the host mode (includes DRD and OTG modes). The register size corresponds to the number of configured USB bus instances; for example, in the default configuration, there are 2 USB bus instances (1 HS, and 1 FSLS).

USB3OTG_GFIFOPRIDBC

Address: **Operational Base** + offset (0xC620)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	gfifopridbc Host DbC DMA priority. This register specifies the relative priority of the RXFIFOs and TXFIFOs associated with the DbC mode. It overrides the priority assigned in the corresponding indexes of the Host RXFIFO and TXFIFO DMA priority registers, when the DbC mode is enabled.

USB3OTG_GDMAHLRATIO

Address: **Operational Base** + offset (0xC624)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:8	RW	0x0000	hstrxfifo Host RXFIFO DMA High-Low Priority.
7:5	RO	0x0	reserved
4:0	RW	0x00	hsttxfifo Host TXFIFO DMA High-Low Priority.

USB3OTG_GFLADJ

Address: **Operational Base** + offset (0xC630)

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Bit	Attr	Reset Value	Description
31	RW	0x0	gfladj_refclk_240mhzdecr_pls1 This field indicates that the decrement value that the controller applies for each ref_clk must be GFLADJ_REFCLK_240MHZ_DECR and GFLADJ_REFCLK_240MHZ_DECR +1 alternatively on each ref_clk. Set this bit to a 1 only if GFLADJ_REFCLK_LPM_SEL is set to 1 and the fractional component of 240/ref_frequency is greater than or equal to 0.5. Examples: If the ref_clk is 24 MHz then 1. GUCTL.REF_CLK_PERIOD = 41 2. GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = (240/24) = 10 3. GFLADJ.GFLADJ_REFCLK_240MHZDECR_PLS1 = 0
30:24	RW	0x00	gfladj_refclk_240mhz_decr This field indicates the decrement value that the controller applies for each ref_clk in order to derive a frame timer in terms of a 240-MHz clock. This field must be programmed to a non-zero value only if GFLADJ_REFCLK_LPM_SEL is set to 1. The value is derived as follows: GFLADJ_REFCLK_240MHZ_DECR = 240/ref_clk_frequency Examples: If the ref_clk is 24 MHz then 1. GUCTL.REF_CLK_PERIOD = 41 2. GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = 240/24 = 10
23	RW	0x0	gfladj_refclk_lpm_sel This bit enables the functionality of running SOF counters on the ref_clk. This bit must not be set to 1 if GCTL.SOFITPSYNC bit is set to 1. Similarly, if GFLADJ_REFCLK_LPM_SEL set to 1, GCTL.SOFITPSYNC must not be set to 1. Note that the ref_clk frequencies supported in this mode are 16/17/19.2/20/24/39.7/40 MHz. The utmi_clk[0] signal of the core must be connected to the FREECLK of the PHY. Note: If you set this bit to 1, the GUSB2PHYCFG.U2_FREECLK_EXISTS bit must be set to 0.
22	RO	0x0	reserved
21:8	RW	0x0000	gfladj_refclk_fladj This field indicates the frame length adjustment to be applied when SOF counter is running on the ref_clk. SOF interval when GLADJ.GFLADJ_REFCLK_LPM_SEL is set to 1. This field must be programmed to a non-zero value only if GFLADJ_REFCLK_LPM_SEL is set to 1 or GCTL.SOFITPSYNC is set to 1. The value is derived as follows: FLADJ_REF_CLK_FLADJ=((125000/ref_clk_period_integer)-(125000/ref_clk_period)) * ref_clk_period where: 1. The ref_clk_period_integer is the integer value of the ref_clk period got by truncating the decimal (fractional) value that is programmed in the GUCTL.REF_CLK_PERIOD field. 2. The ref_clk_period is the ref_clk period including the fractional value. Examples: If the ref_clk is 24 MHz then 1. GUCTL.REF_CLK_PERIOD = 41 2. GFLADJ.GLADJ_REFCLK_FLADJ = ((125000/41)-(125000/41.6666))*41.6666 = 2032 (ignoring the fractional value).

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Bit	Attr	Reset Value	Description
7	RW	0x0	gfladj_30mhz_sdbnd_sel This field selects whether to use the input signal fladj_30mhz_reg or the GFLADJ.GFLADJ_30MHZ to adjust the frame length for the SOF. When this bit is set to: 1'b1: the controller uses the register field GFLADJ.GFLADJ_30MHZ value 1'b0: the controller uses the input signal fladj_30mhz_reg value.
6	RO	0x0	reserved
5:0	RW	0x00	gfadj_30mhz This field indicates the value that is used for frame length adjustment instead of considering from the sideband input signal fladj_30mhz_reg. This enables post-silicon frame length adjustment in case the input signal fladj_30mhz_reg is connected to a wrong value or is not valid. For details on how to set this value, refer to section 5.2.4, "Frame Length Adjustment Register (FLADJ)," of the xHCI Specification.

USB3OTG_DCFG

Address: **Operational Base** + offset (0xC700)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	ignstrmpp This bit only affects stream-capable bulk endpoints. Not applied.
22	RW	0x0	lpmcap LPM Capable. Not applied.
21:17	RW	0x04	nump Number of Receive Buffers. Not applied.
16:12	RW	0x00	intrnum Interrupt number. Indicates interrupt/EventQ number on which non-endpoint-specific device-related interrupts (see DEVT) are generated.
11:10	RO	0x0	reserved
9:3	RW	0x00	devaddr Device Address. The application must perform the following: 1. Program this field after every SetAddress request. 2. Reset this field to zero after USB reset.
2:0	RW	0x0	devspd Device Speed. Indicates the speed at which the application requires the core to connect, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the core is connected. 3'b000: High-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 3'b001: Full-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz)

USB3OTG_DCTL

Address: **Operational Base** + offset (0xC704)

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Bit	Attr	Reset Value	Description
31	RW	0x0	run_stop The software writes 1 to this bit to start the device controller operation. To stop the device controller operation, the software must remove any active transfers and write 0 to this bit. When the controller is stopped, it sets the DSTS.DevCtrlHlt bit when the core is idle and the lower layer finishes the disconnect process. The Run/Stop bit must be used in following cases as specified: 1. After power-on reset and CSR initialization, the software must write 1 to this bit to start the device controller. The controller does not signal connect to the host until this bit is set. 2. The software uses this bit to control the device controller to perform a soft disconnect. When the software writes 0 to this bit, the host does not see that the device is connected. The device controller stays in the disconnected state until the software writes 1 to this bit. The minimum duration of keeping this bit cleared is specified in the Note below. If the software attempts a connect after the soft disconnect or detects a disconnect event, it must set DCTL[8:5] to 5 before reasserting the Run/Stop bit. 3. When the USB is in a lower power state and the Two Power Rails configuration is selected, software writes 0 to this bit to indicate that it is going to turn off the Core Power Rail. After the software turns on the Core Power Rail again and re-initializes the device controller, it must set this bit to start the device controller. Note: The following is the minimum duration under various conditions for which the soft disconnect (SftDiscon) bit must be set for the USB host to detect a device disconnect: 10ms: For high-speed, when the device state is Suspended, Idle, or not Idle/Suspended (performing transactions); For full-speed/low-speed, when the device state is Suspended, Idle, or not Idle/Suspended (performing transactions). To accommodate clock jitter, it is recommended that the application add extra delay to the specified minimum duration.
30	R/WSC	0x0	csftrst Core Soft Reset. Reset all clock domains as follows: 1. This bit clears the interrupts and all the CSRs except GSTS, GSNPSID, GGPIO, GUID, GUSB2PHYCFGn registers, GUSB3PIPECTLn registers, DCFG, DCTL, DEVTEN, and DSTS registers. 2. All module state machines (except the SoC Bus Slave Unit) are reset to the IDLE state, and all the TxFIFOs and the RxFIFO are flushed. 3. Any transactions on the SoC bus Master are terminated as soon as possible, after gracefully completing the last data phase of a SoC bus transfer. Any transactions on the USB are terminated immediately. The application can write this bit at any time to reset the core. This is a self-clearing bit; the core clears this bit after all necessary logic is reset in the core, which may take several clocks depending on the core's current state. Once this bit is cleared, the software must wait at least 3 PHY clocks before accessing the PHY domain (synchronization delay). Typically, software reset is used during software development and also when you dynamically change the PHY selection bits in the

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Bit	Attr	Reset Value	Description
			USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain must be reset for proper operation.
29	RO	0x0	reserved
28:24	RW	0x00	hirdthres HIRD Threshold. The core asserts output signals utmi_l1_suspend_n and utmi_sleep_n on the basis of this signal: The core asserts utmi_l1_suspend_n to put the PHY into Deep Low-Power mode in L1 when both of the following are true: 1. HIRD value is greater than or equal to the value in DCTL.HIRD_Thres[3:0] 2. HIRD_Thres[4] is set to 1'b1. The core asserts utmi_sleep_n on L1 when one of the following is true: 1. If the HIRD value is less than HIRD_Thres[3:0] or 2. HIRD_Thres[4] is set to 1'b0. Note: This field must be set to '0' during SuperSpeed mode of operation.
23:20	RW	0xf	lpm_nyet_thres LPM NYET Threshold Handshake response to LPM token specified by device application. Response depends on DCFG.LPMCap. DCFG.LPMCap is 1'b0 - The core always responds with Timeout (that is, no response). DCFG.LPMCap is 1'b1 - The core responds with an ACK on successful LPM transaction, which requires that all of the following are satisfied: 1. There are no PID or CRC5 errors in both the EXT token and the LPM token (if not true, inactivity results in a timeout ERROR). 2. No data is pending in the Transmit FIFO and OUT endpoints not in flow controlled state (else NYET). 3. The BESL value in the LPM token is less than or equal to LPM_NYET_thres[3:0].
19	RW	0x0	keep_connect When 1, this bit enables the save and restore programming model by preventing the core from disconnecting from the host when DCTL.RunStop is set to 0. The device core disconnects from the host when DCTL.RunStop is set to 0. This bit indicates whether to preserve this behavior (0), or if the core must not disconnect when RunStop is set to 0 (1).
18	RW	0x0	l1_hibernation_en When this bit is set along with KeepConnect, the device core generates a Hibernation Request Event if L1 is enabled and the HIRD value in the LPM token is larger than the threshold programmed in DCTL.HIRD_Thres. The core does not exit the LPM L1 state until software writes Recovery into the DCTL.ULStChngReq field. This prevents corner cases where the device is entering hibernation at the same time the host is attempting to exit L1.

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Bit	Attr	Reset Value	Description
17	RW	0x0	crs Controller Restore State. This command is similar to the USBCMD.CRS bit in host mode and initiates the restore process. When software sets this bit to 1, the controller immediately sets DSTS.RSS to 1. When the controller has finished the restore process, it sets DSTS.RSS to 0. Note: When read, this field always returns 0.
16	RW	0x0	css Controller Save State. This command is similar to the USBCMD.CSS bit in host mode and initiates the save process. When software sets this bit to 1, the controller immediately sets DSTS.SSS to 1. When the controller has finished the save process, it sets DSTS.SSS to 0. Note: When read, this field always returns 0.
15:13	RO	0x0	reserved
12	RW	0x0	initu2ena Not applied.
11	RW	0x0	acceptu2ena Not applied.
10	RW	0x0	initu1ena Not applied.
9	RW	0x0	acceptu1ena Not applied.
8:5	RW	0x0	ulstchngreq Software writes this field to issue a USB state change request. A change in this field indicates a new request to the core. If software wants to issue the same request back-to-back, it must write a 0 to this field between the two requests. The result of the state change request is reflected in the USB State in DSTS. These bits are self-cleared on the MAC Layer exiting suspended state. If software is updating other fields of the DCTL register and not intending to force any link state change, then it must write a 0 to this field. In HS/FS/LS mode: Value: Requested USB state transition 8: Remote wakeup request Others: Reserved The Remote wakeup request must be issued 2us after the device goes into suspend state (DSTS[21:18] is 3). Note: After coming out of hibernation, software must write 8 (Recovery) into this field to confirm exit from the suspended state.
4:1	RW	0x0	tstctl Test Control. 4'b000: Test mode disabled 4'b001: Test_J mode 4'b010: Test_K mode 4'b011: Test_SE0_NAK mode 4'b100: Test_Packet mode 4'b101: Test_Force_Enable Others: Reserved
0	RO	0x0	reserved

USB3OTG_DEVTEN

Address: **Operational Base** + offset (0xC708)

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Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	vendevtstrcvden Vendor Device Test LMP Received Event. 1'b0: Disable this event 1'b1: Enable this event
11:10	RO	0x0	reserved
9	RW	0x0	errticerrevten Erratic Error Event Enable. 1'b0: Disable this event 1'b1: Enable this event
8	RO	0x0	reserved
7	RW	0x0	softevten Start of (u)frame Event Enable. 1'b0: Disable this event 1'b1: Enable this event
6	RW	0x0	u3l2l1_susp_en U3/L2-L1 Suspend Event Enable. 1'b0: Disable this event 1'b1: Enable this event
5	RW	0x0	hibernation_req_evt_en Hibernation Request Event Enable. 1'b0: Disable this event 1'b1: Enable this event
4	RW	0x0	wkupevten Resume/Remote Wakeup Detected Event Enable. 1'b0: Disable this event 1'b1: Enable this event
3	RW	0x0	ulstcngen USB State Change Event Enable. 1'b0: Disable this event 1'b1: Enable this event
2	RW	0x0	connectdoneevten Connection Done Event Enable. 1'b0: Disable this event 1'b1: Enable this event
1	RW	0x0	usbrstevten USB Reset Event Enable. 1'b0: Disable this event 1'b1: Enable this event
0	RW	0x0	disconnevten Disconnect Detected Event Enable. 1'b0: Disable this event 1'b1: Enable this event

USB3OTG_DSTS

Address: **Operational Base** + offset (0xC70C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29	RW	0x0	dcnrd Device Controller Not Ready. The bit indicates that the core is in the process of completing the state transitions after exiting from hibernation. To complete the state transitions, it takes 256 bus clock cycles from the time DCTL[31].Run/Stop is set. During hibernation, if the UTMI/ULPI PHY is in suspended state, then the 256-bus clock cycle delay starts after the PHY exited suspended state. Software must set DCTL[31].Run/Stop to 1 and wait for this bit to be de-asserted to zero before processing DSTS.USBLnkSt.
28:26	RO	0x0	reserved
25	RW	0x0	rss Restore State Status. This bit is similar to the USBSTS.RSS in host mode. When the controller finishes the restore process, it completes the command by setting DSTS.RSS to 0.
24	RO	0x0	sss Save State Status. This bit is similar to the USBSTS.SSS in host mode. When the controller has finished the save process, it completes the command by setting DSTS.SSS to 0.
23	RO	0x0	coreidle Core Idle. The bit indicates that the core finished transferring all RxFIFO data to system memory, writing out all completed descriptors, and all Event Counts are zero. Note: While testing for Reset values, mask out the read value. This bit represents the changing state of the core and does not hold a static value.
22	RO	0x1	devctrlhlt Device Controller Halted. This bit is set to 0 when the Run/Stop bit in the DCTL register is set to 1. The core sets this bit to 1 when, after SW sets Run/Stop to 0, the core is idle and the lower layer finishes the disconnect process. When Halted=1, the core does not generate Device events. Note: The core does not set this bit to 1 if GEVNTCOUNTn has some valid value. Software needs to acknowledge the events that are generated (by writing to GEVNTCOUNTn) while it is waiting for this bit to be set to 1.

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Bit	Attr	Reset Value	Description
21:18	RO	0x4	usblnkst USB/Link State In SS mode: LTSSM State 4'h0: U0 4'h1: U1 4'h2: U2 4'h3: U3 4'h5: RX_DET 4'h6: SS_INACT 4'h7: POLL 4'h8: RECOV 4'h9: HRESET 4'ha: CMPLY 4'hb: LPBK 4'hf: Resume/Reset In HS/FS/LS mode: 4'h0: On state 4'h2: Sleep (L1) state 4'h3: Suspend (L2) state 4'h4: Disconnected state (Default state) 4'h5: Early Suspend state (valid only when Hibernation is disabled, GCTL[1].GblHibernationEn = 0) 4'he: Reset (valid only when Hibernation is enabled, GCTL[1].GblHibernationEn = 1) 4'hf: Resume (valid only when Hibernation is enabled, GCTL[1].GblHibernationEn = 1) The link state Resume/Reset indicates that the core received a resume or USB reset request from the host while the link was in hibernation. Software must write 8 (Recovery) to the DCTL.ULStChngReq field to acknowledge the resume/reset request. When Hibernation is enabled, GCTL[1].GblHibernationEn = 1, this field USBLnkSt is valid only when DCTL[31].Run/Stop set to 1 and DSTS[29].DCNRD = 0.
17	RO	0x1	rx_fifo_empty Rx Fifo Empty.
16:3	RO	0x0000	reserved
2:0	RU	0x0	connectspd Connected Speed. Indicates the speed at which the DWC_usb3 core has come up after speed detection through a chirp sequence. 3'b000: High-speed (PHY clock is running at 30 or 60 MHz) 3'b001: Full-speed (PHY clock is running at 30 or 60 MHz)

USB3OTG_DGCMDPAR

Address: **Operational Base** + offset (0xC710)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the device command parameter. This must be programmed before or along with the device command. The available device commands are listed in DGCMD register.

USB3OTG_DGCMD

Address: **Operational Base** + offset (0xC714)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:12	RO	0x0	cmdstatus Command Status: 1'b1: CmdErr: Indicates that the device controller encountered an error while processing the command. 1'b0: Indicates command success
11:10	RO	0x0	reserved
9	R/WSC	0x0	cmdact Command Active. The software sets this bit to 1 to enable the device controller to execute the generic command. The device controller sets this bit to 0 after executing the command.
8	RW	0x0	cmdioc Command Interrupt on Complete. When this bit is set, the device controller issues a Generic Command Completion event after executing the command. Note that this interrupt is mapped to DCFG.IntrNum. Note: This field must not set to 1 if the DCTL.RunStop field is 0.
7:0	RW	0x00	cmdtyp Command Type. Specifies the type of command the software driver is requesting the core to perform. 8'h0: Reserved 8'h1: Set Endpoint Configuration - 64 or 96-bit Parameter 8'h2: Set Endpoint Transfer Resource Configuration - 32-bit Parameter 8'h3: Get Endpoint State - No Parameter Needed 8'h4: Clear Stall (see Set Stall) - No Parameter Needed 8'h5: Start Transfer - 64-bit Parameter 8'h6: Update Transfer - No Parameter Needed 8'h7: End Transfer - No Parameter Needed 8'h8 Start New Configuration - No Parameter Needed

USB3OTG_DALEPENA

Address: **Operational Base** + offset (0xC720)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usbactep USB Active Endpoints. This field indicates if a USB endpoint is active in the current configuration and interface. It applies to USB IN endpoints 0~15 and OUT endpoints 0~15, with one bit for each of the 32 possible endpoints. Even numbers are for USB OUT endpoints, and odd numbers are for USB IN endpoints, as follows: Bit[0]: USB EP0-OUT Bit[1]: USB EP0-IN Bit[2]: USB EP1-OUT Bit[3]: USB EP1-IN ... The entity programming this register must set bits 0 and 1 because they enable control endpoints that map to physical endpoints (resources) after USBReset. Hardware clears these bits for all endpoints (other than EP0-OUT and EP0-IN) after detecting a USB reset event. After receiving SetConfiguration and SetInterface requests, the application must program endpoint registers accordingly and set these bits.

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USB3OTG_DEPnCMDPAR2

Address: **Operational Base** + offset (0xC800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the physical endpoint command Parameter 2. It must be programmed before issuing the command.

USB3OTG_DEPnCMDPAR1

Address: **Operational Base** + offset (0xC804)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the physical endpoint command Parameter 1. It must be programmed before issuing the command.

USB3OTG_DEPnCMDPAR0

Address: **Operational Base** + offset (0xC808)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the physical endpoint command Parameter 0. It must be programmed before issuing the command.

USB3OTG_DEPnCMD

Address: **Operational Base** + offset (0xC80C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	commandparam Command Parameters or Event Parameters when this register is written: For Start Transfer command: The 16-bit StreamID assigned to this transfer. For Start Transfer command applied to an isochronous endpoint: StartMicroFramNum, Indicates the (micro) frame number to which the first TRB applies. For Update Transfer, End Transfer, and Start New Configuration commands: [22:16]: Transfer Resource Index (XferRscIdx). The hardware-assigned transfer resource index for the transfer, which was returned in response to the Start Transfer command. The application software-assigned transfer resource index for a Start New Configuration command. Event Parameters (EventParam), when this register is read.
15:12	RW	0x0	cmdstatus Command Completion Status. The information is in the same format as bits 15:12 of the Endpoint Command Complete event.
11	RW	0x0	hipri_forcerm HighPriority: Only valid for Start Transfer command. ForceRM: Only valid for End Transfer command. ClearPendIN: Only valid for Clear Stall command. Software sets this bit to clear any pending IN transaction (on that endpoint) stuck at the lower layers when a Clear Stall command is issued.
10	RW	0x0	cmdact Command Active. Software sets this bit to 1 to enable the device endpoint controller to execute the generic command. The device controller sets this bit to 0 when the CmdStatus field is valid and the endpoint is ready to accept another command. This does not imply that all the effects of the previously-issued command have taken place.

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Bit	Attr	Reset Value	Description
9	RO	0x0	reserved
8	RW	0x0	cmdioc Command Interrupt on Complete. When this bit is set, the device controller issues a generic Endpoint Command Complete event after executing the command. Note that this interrupt is mapped to DEPCFG.IntrNum. When the DEPCFG command is executed, the command interrupt on completion goes to the interrupt pointed by the DEPCFG.IntrNum in the current command. Note: This field must not set to 1 if the DCTL.RunStop field is 0.
7:4	RO	0x0	reserved
3:0	RW	0x0	cmdtyp Command Type. Specifies the type of command the software driver is requesting the core to perform. 4'h0: Reserved 4'h1: Set Endpoint Configuration 64 or 96-bit Parameter 4'h2: Set Endpoint Transfer Resource Configuration - 32-bitparameter 4'h3: Get Endpoint State - No Parameter Needed 4'h4: Set Stall - No Parameter Needed 4'h5: Clear Stall (see Set Stall) - No Parameter Needed 4'h6: Start Transfer - 64-bit Parameter 4'h7: Update Transfer - No Parameter Needed 4'h8: End Transfer - No Parameter Needed 4'h9: Start New Configuration - No Parameter Needed

13.5 Application Notes

13.5.1 Some Settings About USB3OTG0

- **USB3 mode initial sequence**

In this application USBDP PHY will use 24Mhz or 26Mhz reference clock, some initial sequence should be set and USB mode should be configured before working. Please refer to USBDP PHY section.

- **Power Down Mode**

When no transfer happened, PD_USB can be power down in application. At this time the PowerDown signal to USBDP PHY PIPE interface will be clamped to 3'b3. But there is also a MUX near USBDP PHY which could choose form GRF. Also, RxTermination, TxElecIdle and TxDetectRxLoopbx can also be control by GRF, this could be found in USBDPPHY_GRF_CON3 in GRF section.

If USB and DP not be used, USBDPPHY could also be power down, and before power down, USBDPPHY_GRF_CON2[15] will use to clamp the PHY output signal.

- **PhyStatus in PIPE Interface for USB2 only**

If only USB2 is used and USBDP PHY initial sequence not correctly processes, the PIPE interface signal PhyStatus may be set to 1'b1,
USB_GRF_USB3OTG0_CON1/PHP_GRF_USB3OTG1_CON1[3:2] can be set to control PhyStatus.

13.5.2 USB3OTG1 mode setting

USB3.0 PHY is combo with PCIE, so you must set some GRF to set USB mode.

- Set COMBO_PIPE_PHY_GRF_PIPE_CON0[3:2] to 1'b1 to select USB mode.
- Set COMBO_PIPE_PHY_GRF_PIPE_CON2[12] and [15] to 1'b0. This will select TxElecidle and TxCompliance form controller.

13.5.3 Battery Charge

The USB2.0 PHY supports battery charger detection to enable device draw increased

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current from VBUS for charging and/or powering up from dedicated charging ports or charging downstream ports.
The related signals with GRF are following:

Table 13-1 USB2PHY Battery Charging GRF Description

GRF	Description
USB2PHY_GRF_CON2[5]	CHRGSEL: This signal selects whether the Battery Charger circuit sets voltage sourcing on the DP line and sensing on the DM line or voltage sourcing on DM and sensing on DP.
USB2PHY_GRF_CON2[6]	VDATDETENB: This signal activates the Battery Charger comparator and enables detection of the DP and DM lines according to the Battery Charging specification.
USB2PHY_GRF_CON2[7]	VDATSRCENB: This signal activates the voltage sourcing on the DP or DM line.
USB2PHY_GRF_STATUS0[0]	CHGDET: This signal is the battery charge detection (VDAT_REF) comparator output.
USB2PHY_GRF_STATUS0[1]	FSVPLUS: This signal is the DP FS/LS single ended receiver output, which is also the VLGC output.
USB2PHY_GRF_STATUS0[2]	FSVMINUS: This signal is the DM FS/LS single ended receiver output, which is also the VLGC output.
USB2PHY_GRF_STATUS0[11]	OTGSESSVLD0: This signal is the VBUS session valid detection and can be used by a portable device to detect the VBUS voltage from the host or charger port.

Next lists the detection flow.

Table 13-2 USB2PHY Battery Charging Operations

Mode of Operation	Inputs			Outputs			
	CHRGSEL	VDATDETENB	VDATSRCENB	OTGSESSVLD	CHGDET	FSVPUS	FSVMINUS
Battery charging is disabled	X	0	0	X	0	X	X
PHY is operating as a portable device (PD) and is not attached to host nor charger port.	X	0	0	0	X	X	X
PHY is operating as a PD using the Dead Battery Provision (DBP) - Unconfigured Clause, while attached to a standard downstream port (SDP).	0	1	1	1	0	X	0
PHY is operating as a PD using the DBP - Unconfigured Clause, while attached to a special port (such as a PS2 or proprietary charger) that pulls D+/D− high.	0	1	1	1	1	X	1
PHY is operating as a PD using the DBP - Unconfigured Clause, while attached to a charging downstream port (CDP) or a dedicated charging port (DCP).	0	1	1	1	1	X	0
PHY is operating as a PD that is performing Primary Detection while attached to an SDP.	1	1	1	1	0	X	0

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Mode of Operation	Inputs			Outputs			
	CHRGSEL	VDATDETENB	VDATSRCENB	OTGSESSVLD	CHGDET	FSVPUS	FSVMINUS
PHY is operating as a PD that is performing Primary Detection while attached to a special port (such as a PS2 or proprietary charger) that pulls D+/D− high.	0	1	1	1	1	X	1
PHY is operating as a PD that is performing Primary Detection while attached to a CDP or DCP.	0	1	1	1	1	X	0
PHY is operating as a PD that is performing Secondary Detection while attached to a CDP.	1	1	1	1	0	X	X
PHY is operating as a PD that is performing Secondary Detection while attached to a DCP.	1	1	1	1	1	X	X
PHY is operating as a host CDP with no PD detected.	1	1	0	X	0	0	X
PHY is operating as a host CDP that detects an attached PD, which supports the BC specification.	1	1	1	X	1	0	X
PHY is operating as a host CDP that detects a connect from the PD D+ pullup.	1	1	0	X	X	1	0

13.5.4 USB1 Limit

USB1 cannot work when COMBO_PIPE_PHY1 is used as PCIe or SATA. This limit includes USB3.0 and USB2.0 mode.

13.5.5 OTG Programming Model

When detect ID change event (see VOGRF) or VBUS change event (see VOGRF) after disconnect, it means a USB2.0/3.0 OTG A device or B device may connect, then check status of ID (see VOGRF). If ID==0, it will work as A device, then follow host programming flow; if ID==1, it will work as B device, then it follows device programming flow.
Note: USB3OTG doesn’t support host/device mode swapping through HNP and RSP.

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Chapter 14 PCIe Controller

14.1 Overview

The PCI Express (PCIe) is a high performance, general purpose I/O interconnect defined for a wide variety of future computing and communication platforms. The PCIe designed to be used as a general-purpose serial I/O interconnect in multiple market segments, including desktop, mobile, server, storage, and embedded communications. The PCIe controller implements the three PCI Express protocol layers (Transaction layer, Data Link layer, and the MAC portion of the physical layer). It also implements the application-dependent functionality of the PCI Express Transaction Layer for packet transmission, which is located between application logic and the PCI Express protocol layers.

The PCIe controller is compliant with PCI Express Specifications 1.1, 2.1. The PCIe controller subsystem consists of 1 controller, refer to Block Diagram for details.

PCIe controller subsystem supports the following features:
- Compatible with PCI Express Base Specification Revision 2.1
- Including 2 PCIe controller
  - RC mode only
    - Maximum payload size is 128 bytes
    - 8 ATU inbound regions, 8 ATU outbound regions
    - Up to Gen2 X 1 link when connecting with Combo PIPE PHY
- The following optional features of the specification
  - Alternative Routing-ID Interpretation (ARI)
  - TLP Prefix
  - Dynamic Power Allocation (DPA)
  - L1 Substates (L1SS)
  - PCI Express Active State Power Management (ASPM)
  - PCI Express Advanced Error Reporting (AER) with Multiple Header Logging
- Support Latency Tolerance Reporting (LTR)
- Support Optimized Buffer Flush and Fill (OBFF)
- Internal Datapath Operating at 62.5 MHz, 125 MHz
- Advanced Power and Clock Management
- Internal Address Translation Unit
- Integrated MSI/MSI-X Receiver Module
- RAS DES (Debug, Error Injection, and Statistics)
- ECRC Generation and Checking
- Store-and-forward Queue Modes for Rx TLPs
- Configurable Filtering Rules for Posted, Non-posted, and Completion Traffic
- Configurable BAR Filtering, I/O Filtering, Configuration Filtering and Completion Lookup/Timeout
- Three Application Transmit Clients
- MSI with Per-Vector Masking (PVM), Extended message data for MSI
- MSI-X with Per-Vector Masking (PVM)

14.2 Block Diagram

PCIe comprises with:
- APB: APB Interface
- AXI_S: AXI Slave Interface
- AXI_M: AXI Master Interface
- AXI_DBI: AXI Slave Interface for configuration
- Client: Client Logic
- CLKRST: Clock and Reset related logic
- Memory: SRAMs and Buffers
- AMBA Bridge: AXI to Core Bridge
- PCIe Core: PCIe Controller Core

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- PM: Power Management Unit
- Combo PIPE PHY

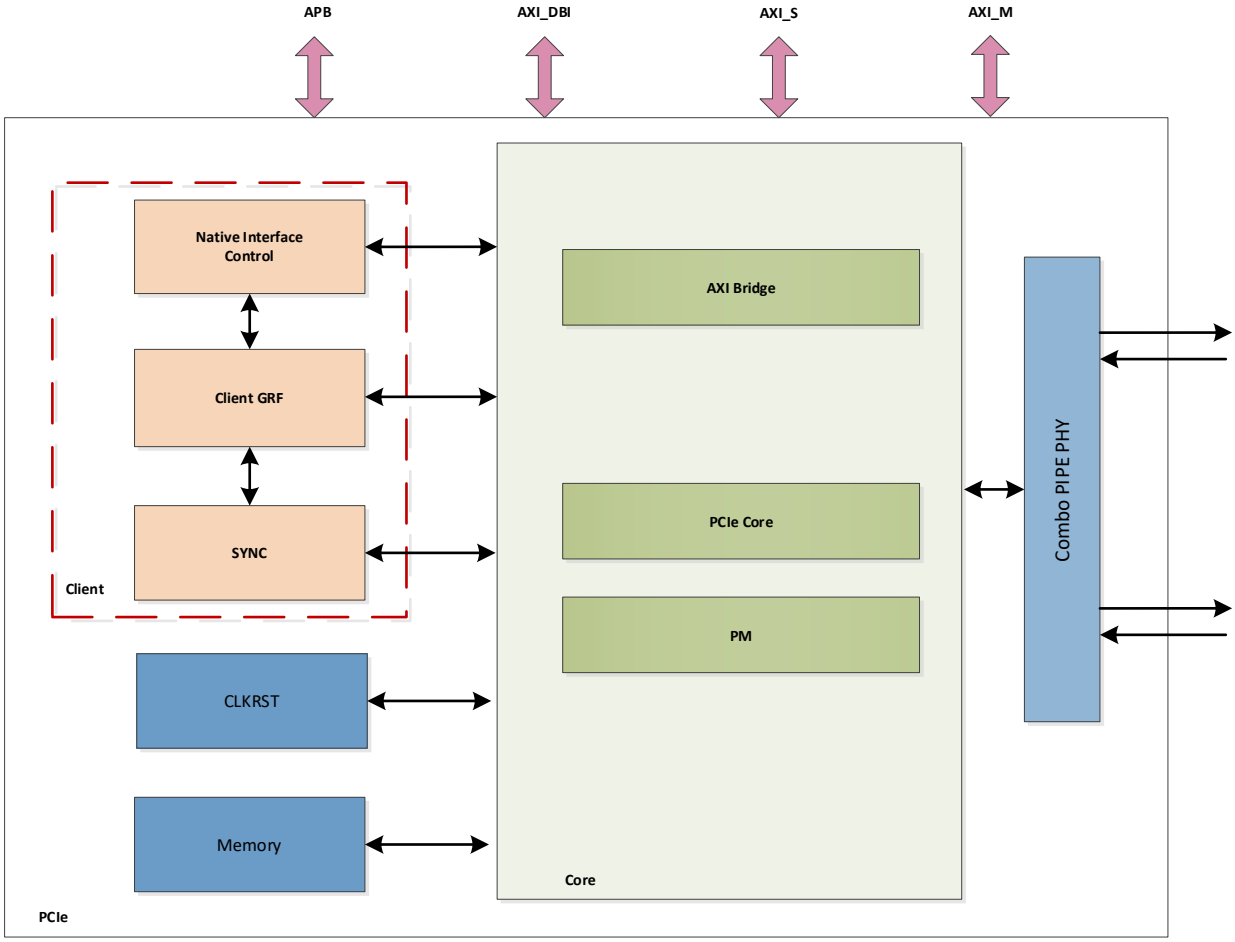


Fig. 14-1 PCIe Block Diagram

Block function description will be discussed in next section.

14.3 Function Description

14.3.1 Application Interface and AXI Bridge

Application Interface comprises with four standard interfaces: one AXI master interface, two AXI slave interface and one APB interface. These interfaces bridging capability for directly adding a PCI Express link to an AXI system fabric.

The AXI bridge module acts as a bridge between the standard AXI interfaces and the PCIe controller native interfaces. The bridge interconnects the AXI interfaces within an AXI-embedded system with a remote PCIe link, as either a root complex port or as an endpoint port.

The AXI master interfaces enable a remote PCIe device to read and write to an AXI slave (in System Interface) connected to the AXI bridge. The AXI link slave interface enables an AXI master (in System Interface) to read and write through the AXI bridge to a remote PCIe device. The DBI slave enables an AXI master (in System Interface) to access the controller's registers. The APB enables Application to access the Client registers.

14.3.2 Client

Client Logic Consists of some additional logic used for application to interact with PCIe Controller. For example, applications can access client registers to send/receive PCIe Message, request to enter/exit PM state, deal with interrupts, configure some basic operation mode, read some basic debug information, and so on. For more details, please

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refer to Client registers description and application notes for more information.

14.3.3 CXPL

PCIe Core deal with the PCIe protocol, and consists of three main modules:

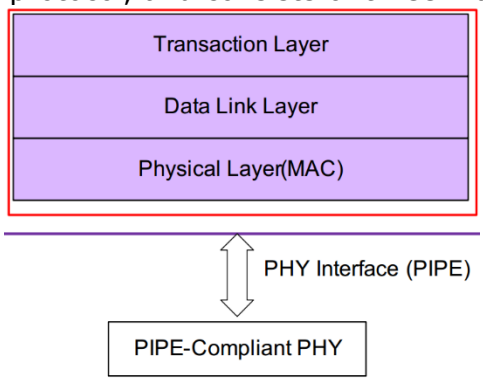


Fig. 14-2 PCIe Core Architecture Overview

The PCIe Core implements the basic functionality for the PCI Express physical, link, and transaction layers. This module implements a large part of the transaction layer logic, all of the data link layer logic, and the MAC portion of the physical layer, including the link training and status state machine (LTSSM). The Core connects to the external PHY through the standard PIPE interface.

14.3.4 PMC

PCIe Controller support PCIe ASPM, L1 Substate and PCI PM. For proper understanding of PCIe Power Management, you should be familiar with Power Management of the PCI Express Base Specification, and PCI-SIG Engineering Change Notice ECN L1 Substates with CLKREQ#. For application details, please refer to Application Notes for more information.

14.3.5 XADM

Transmit Application-Dependent Module (XADM) implements the application-specific functionality of the PCI Express transaction layer for packet transmission. Its functions include:

- TLP Arbitration
- TLP Formation
- Flow Control (FC) Credit checking

The transmit path uses a cut-through architecture. It does not implement transmit buffering/queues (other than the retry buffer). The controller maintains an internal Target Completion Lookup Table to store certain TLP header information from the Rx request.

14.3.6 RADM

Receive Application-Dependent Module (RADM) implements application-specific functionality of the PCI Express transaction layer for packet reception. Its functions include:

- Sorting/filtering of received TLPs. The filtering rules and routing are configurable.
- Buffering and queuing of the received TLPs.
- Routing of received TLP to the controller’s receive interfaces.

The RADM maintains a Receive Completion Lookup Table (LUT) for completion tracking and completion-timeout monitoring of Tx non-posted requests. It indicates a timeout when an expected Rx completion does not arrive within the timeout period.

14.3.7 CDM

Configuration-Dependent Module (CDM) implements:

- Standard PCI Express configuration space
- Controller-specific register space (Port Logic Registers)
-

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14.4 Register Description

14.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 14-1 PCIe RC G2 Client and Core Register Address Mapping

Base Address	Name	Device	Address Length	Offset Address Range
0x22000000	PCIe2_1L0_DBI/PCIE0_DBI	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0xa00000000	PCIe2_1L0_DBI/PCIE0_DBI	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0x20000000	PCIe2_1L0_S/PCIE0_S	PCIe Outbound Memory	16M BYTE	0x0000000~0xffffff
0x900000000	PCIe2_1L0_S/PCIE0_S	PCIe Outbound Memory	2G BYTE	0x00000000~0x7fffffff
0x2A200000	PCIe2_1L0_APB/PCIE0_APB	Client Register	64K BYTE	0x0000~0xffff
0x22400000	PCIe2_1L1_DBI/PCIE1_DBI	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0xa00400000	PCIe2_1L1_DBI/PCIE1_DBI	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0x21000000	PCIe2_1L1_S/PCIE1_S	PCIe Outbound Memory	16M BYTE	0x0000000~0xffffff
0x980000000	PCIe2_1L1_S/PCIE1_S	PCIe Outbound Memory	2G BYTE	0x00000000~0x7fffffff
0x2A210000	PCIe2_1L1_APB/PCIE1_APB	Client Register	64K BYTE	0x0000~0xffff

Table 14-2 PCIe RC G2 Core Register Map in RC mode

Offset	Register Block	Description
0x0000	TYPE1_HDR	PCI-Compatible Configuration Space Header Type1
0x0040	PM_CAP	PCI Power Management Capability Structure
0x0050	MSI_CAP	MSI Capability Structure
0x0070	PCIE_CAP	PCI Express Capability Structure
0x00b0	MSIX_CAP	MSI-X Capability Structure
0x0100	AER_CAP	Advanced Error Reporting Capability Structure
0x0148	SPCIE_CAP	Secondary PCI Express Capability Structure
0x0160	L1SUB_CAP	L1 Substates Capability Structure
0x0170	RAS_DES_CAP	RAS D.E.S. Capability Structure
0x0700	PORT_LOGIC	Port Logic
0x100000	PCIE_CAP_DBI2	DBI2 Shadow Block: PF PCI

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Offset	Register Block	Description
		Express Capability Structure
0x1000b0	MSIX_CAP_DBI2	Shadow Block: MSI-X Capability Structure
0x300000	ATU_CAP	ATU Port Logic Structure

14.4.2 Client Register

14.4.2.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
PCIE0_CLIENT	0x2A200000
PCIE1_CLIENT	0x2A210000

14.4.2.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_GENERAL_CON	0x0000	W	0x00000000	General Control Register
PCIE_CLIENT_INTR_STATUS_MSG_RX	0x0004	W	0x00000000	Interrupt Status Register Related to Message Reception
PCIE_CLIENT_INTR_STATUS_LEGACY	0x0008	W	0x00000000	Interrupt Status Register Related to Legacy Interrupt
PCIE_CLIENT_INTR_STATUS_ERR	0x000C	W	0x00000000	Interrupt Status Register Related to Error Detection
PCIE_CLIENT_INTR_STATUS_MISC	0x0010	W	0x00000000	Interrupt Status Register Related to Miscellaneous Operation
PCIE_CLIENT_INTR_STATUS_PMC	0x0014	W	0x00000000	Interrupt Status Register Related Power Management Control
PCIE_CLIENT_INTR_MASK_MSG_RX	0x0018	W	0x00007737	Interrupt Mask Register Related to Message Reception
PCIE_CLIENT_INTR_MASK_LEGACY	0x001C	W	0x000000FF	Interrupt Mask Register Related to Legacy Interrupt
PCIE_CLIENT_INTR_MASK_ERR	0x0020	W	0x0000177F	Interrupt Mask Register Related to Error Detection
PCIE_CLIENT_INTR_MASK_MISC	0x0024	W	0x0000FFFF	Interrupt Mask Register Related to Miscellaneous Operation
PCIE_CLIENT_INTR_MASK_PMC	0x0028	W	0x000001FF	Interrupt Mask Register Related Power Management Control
PCIE_CLIENT_POWER_CON	0x002C	W	0x00000008	Power Management Control Register
PCIE_CLIENT_POWER_STATUS	0x0030	W	0x00000000	Power Management Status Register
PCIE_CLIENT_MSG_GEN_CON	0x0034	W	0x00000000	Message Generation Control Register
PCIE_CLIENT_MSI_GEN_CON	0x0038	W	0x00000000	MSI Generation Control Register
PCIE_CLIENT_MSI_GEN_FNUM_TC	0x0040	W	0x00000000	MSI Function Number and TC set Register
PCIE_CLIENT_RBAR_SIZE_INFO0	0x0044	W	0x00000000	Resizable BAR2 to BAR0 Size Information Register
PCIE_CLIENT_RBAR_SIZE_INFO1	0x0048	W	0x00000000	Resizable BAR5 to BAR3 Size Information Register
PCIE_CLIENT_DMA_HSHAKE_TOGG	0x004C	W	0x00000000	DMA Handshake Toggle Register

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Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_VEN_MSG_RX_INFO0	0x0050	W	0x00000000	Register That Contains Header Information of Vendor Message That Controller Received
PCIE_CLIENT_VEN_MSG_RX_INFO1	0x0054	W	0x00000000	Register That Contains Header Information of Vendor Message That Controller Received
PCIE_CLIENT_VEN_MSG_RX_INFO2	0x0058	W	0x00000000	Register That Contains Header Information of Vendor Message That Controller Received
PCIE_CLIENT_VEN_MSG_TX_CFG0	0x005C	W	0x00000000	Vendor Message Transmit Configuration Register 0
PCIE_CLIENT_VEN_MSG_TX_CFG1	0x0060	W	0x00000000	Vendor Message Transmit Configuration Register 1
PCIE_CLIENT_VEN_MSG_TX_CFG2	0x0064	W	0x00000000	Vendor Message Transmit Configuration Register 2
PCIE_CLIENT_LTR_MSG_TX_INFO	0x0068	W	0x00000000	LTR Message Transmit Data Register
PCIE_CLIENT_APP_ERR_RPT_INFO0	0x006C	W	0x00000000	Application Error Report Information Register 0
PCIE_CLIENT_APP_ERR_RPT_INFO1	0x0070	W	0x00000000	Application Error Report Information Register 1
PCIE_CLIENT_APP_ERR_RPT_INFO2	0x0074	W	0x00000000	Application Error Report Information Register 2
PCIE_CLIENT_APP_ERR_RPT_INFO3	0x0078	W	0x00000000	Application Error Report Information Register 3
PCIE_CLIENT_APP_ERR_RPT_INFO4	0x007C	W	0x00000000	Application Error Report Information Register 4
PCIE_CLIENT_OBFF_WAKE_ELE_CFG	0x0080	W	0xB4F05064	OBFF Wake Configuration Register
PCIE_CLIENT_OBFF_WAKE_DEBUG	0x0084	W	0x00000000	OBFF Wake Decoder Debug Register
PCIE_CLIENT_RX_CPL_TIME_OUT_INFO	0x0088	W	0x00000000	RX CPL Timeout Information
PCIE_CLIENT_TX_CPL_TIME_OUT_INFO0	0x008C	W	0x00000000	TX CPL Timeout Information 0
PCIE_CLIENT_TX_CPL_TIME_OUT_INFO1	0x0090	W	0x00000000	TX CPL Timeout Information 1
PCIE_CLIENT_LOCAL_CRU_CTRL	0x009C	W	0x00000000	Local Clock and Reset Control Register
PCIE_CLIENT_GENERAL_DEBUG_CON	0x0100	W	0x00000000	General Debug Control Register
PCIE_CLIENT_GENERAL_DEBUG_INFO	0x0104	W	0x00000000	General Debug Information Register
PCIE_CLIENT_SLC_DEBUG_INFO_CMN	0x0108	W	0x00000000	Silicon Debug Information Common Register
PCIE_CLIENT_SLC_DEBUG_INFO_LN	0x010C	W	0x00000000	Silicon Debug Information Lane N Register
PCIE_CLIENT_SLC_DEBUG_INFO_V0	0x0114	W	0x00000000	Silicon Debug Information Virtual Channel 0 Register
PCIE_CLIENT_DIAG_STATUS_BUS_SEL	0x0118	W	0x00000000	Diagnostic Status Bus Select Register
PCIE_CLIENT_DIAG_STATUS_BUS_INFO	0x011C	W	0x00000000	Diagnostic Status Bus Information Register

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Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_CDM_RASDES_EC_INFO_CON	0x0140	W	0x00000000	CDM RASDES Control Register
PCIE_CLIENT_CDM_RASDES_EC_INFO_CMN	0x0144	W	0x00000000	CDM RASDES Information Common Data Register
PCIE_CLIENT_CDM_RASDES_EC_INFO_LN	0x0148	W	0x00000000	Lane N CDM RASDES Information Register
PCIE_CLIENT_CDM_RASDES_TBA_CON	0x0150	W	0x00000000	CDM RASDES TBA Control Register
PCIE_CLIENT_CDM_RASDES_TBA_INFO_CMN	0x0154	W	0x00000000	CDM RASDES TBA Common Information Register
PCIE_CLIENT_HOT_RESET_CTRL	0x0180	W	0x00000000	Hot Reset Control Register
PCIE_CLIENT_INTR_EN_MSG_RX	0x0190	W	0x00007737	Interrupt Enable Register Related to Message Reception
PCIE_CLIENT_INTR_EN_LEGACY	0x0194	W	0x000000FF	Interrupt Enable Register Related to Legacy Interrupt
PCIE_CLIENT_INTR_EN_ERR	0x0198	W	0x0000177F	Interrupt Enable Register Related to Error Detection
PCIE_CLIENT_INTR_EN_MISC	0x019C	W	0x0000FFFF	Interrupt Enable Register Related to Miscellaneous Operation
PCIE_CLIENT_INTR_EN_PMC	0x01A0	W	0x000001FF	Interrupt Enable Register Related Power Management Control
PCIE_CLIENT_MSI_INT_RX_VEC	0x01C0	W	0x00000000	MSI Interrupt Vector
PCIE_CLIENT_AXI_MSTR_MISC_CON	0x0200	W	0x00000000	AXI Master Sideband Signals Control Register
PCIE_CLIENT_AXI_SLV_ATU_BYPASS	0x0204	W	0x00000000	Address Translate Unit Bypass set Register
PCIE_CLIENT_AXI_SLV_AWMISC_HDR	0x0208	W	0x00000000	AXI Slave Write Address Sideband Signals HDR Register
PCIE_CLIENT_AXI_SLV_AWMISC_HDR3	0x020C	W	0x00000000	AXI Slave Write Address Sideband Signals 3rd HDR Register
PCIE_CLIENT_AXI_SLV_AWMISC_HDR4	0x0210	W	0x00000000	AXI Slave Write Address Sideband Signals 4th HDR Register
PCIE_CLIENT_AXI_SLV_AWMISC_TAG	0x0214	W	0x00000000	AXI Slave Write Request Tag Register
PCIE_CLIENT_AXI_SLV_MISC_INFO	0x0218	W	0x00000000	AXI Slave Read Address and Write Data Sideband Signals Control Register
PCIE_CLIENT_AXI_SLV_AW_TLP_PRFX	0x0220	W	0x00000000	AXI Slave Write TLP Prefix
PCIE_CLIENT_AXI_SLV_AR_TLP_PRFX	0x0224	W	0x00000000	AXI Slave Read TLP Prefix
PCIE_CLIENT_DBI_MISC_CON	0x0270	W	0x00000000	DBI Miscellaneous Control Register
PCIE_CLIENT_PORT_BDF	0x0274	W	0x00000000	Port BDF Register
PCIE_CLIENT_LTSSM_STATUS	0x0300	W	0x00000000	LTSSM Status Register
PCIE_CLIENT_DBG_FIFO_MODE_CON	0x0310	W	0x00000000	Debug FIFO Mode Control Register
PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA0	0x0320	W	0x00000000	Debug FIFO Pattern hit Data Register 0
PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA1	0x0324	W	0x00000000	Debug FIFO Pattern hit Data Register 1

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Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA0	0x0328	W	0x00000000	Debug FIFO Transition Pattern hit Data Register 0
PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA1	0x032C	W	0x00000000	Debug FIFO Transition Pattern hit Data Register 1
PCIE_CLIENT_DBG_FIFO_STATUS	0x0350	W	0x00000000	Debug FIFO Status Register
PCIE_CLIENT_CFG_ERR_STATUS	0x0354	W	0x00000000	Configuration Error Status
PCIE_CLIENT_TLP_PRFX_LOG0	0x0380	W	0x00000000	TLP Prefixes Log Register 0
PCIE_CLIENT_TLP_PRFX_LOG1	0x0384	W	0x00000000	TLP Prefixes Log Register 1
PCIE_CLIENT_TLP_PRFX_LOG2	0x0388	W	0x00000000	TLP Prefixes Log Register 2
PCIE_CLIENT_TLP_PRFX_LOG3	0x038C	W	0x00000000	TLP Prefixes Log Register 3
PCIE_CLIENT_CLIENT_VER	0x0800	W	0x00050611	Client Version Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.2.3 Detail Registers Description

PCIE_CLIENT_GENERAL_CON

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	mem_auto_clk_gating_disable Control the memory auto clock gating when it is inactive. 1'b0: Auto gating enable 1'b1: Auto gating disable
13	RW	0x0	link_req_rst_grt_sel Link down reset request grant control select: 1'b1: From client grf GENERAL_CON bit 3 1'b0: From pcie grf PCIE_CON0 bit 2 Reserved after r5p6 (version 50600).
12	R/WSC	0x0	app_hdr_valid Alias "app_err_report" in old client version. One-clock-cycle pulse indicating that the data app_hdr_log, app_err_bus, app_err_func_num, and app_tlp_prfx_log is valid. Set 1 to report application error to controller. It is a self-clear bit to generate a pulse to controller. Application should provide error information in VEN_ERR_INFOx registers before setting this bit.
11	RW	0x0	app_sris_mode SRIS operating mode 1'b0: non-SRIS mode 1'b1: SRIS mode

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Bit	Attr	Reset Value	Description
10	RW	0x0	app_dbi_ro_wr_disable DBI Read-only Write Disable 1'b0: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is read-write. 1'b1: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is forced to 0 and is read-only
9	RW	0x0	tx_lane_flip_en Performs manual lane reversal for transmit lanes. For use whenautomatic lane reversal does not occur because lane 0 is not detected. In most cases, tx_lane_flip_en should be wired to a static value at thechip level. For more information, see 'Lane Reversal and Broken Lanes'. This signal is only used in Conventional PCIe mode. When in M-PCIe mode, mpcie_tx_lane_flip_en is used. 1'b0: Disable 1'b1: Enable
8	RW	0x0	rx_lane_flip_en Performs manual lane reversal for receive lanes. For use when automatic lane reversal does not occur because lane 0 is not detected. In most cases, rx_lane_flip_en should be wired to a static value at the chip level. For more information, see 'Lane Reversal and Broken Lanes'. This signal is only used in Conventional PCIe mode. When in M-PCIe mode, mpcie_rx_lane_flip_en is used. 1'b0: Disable 1'b1: Enable
7:4	RW	0x0	device_type Device/port type. Indicates the specific type of this PCI Express function. It is also used to set the 'Device/Port Type' field of the 'PCI Express Capabilities Register'. The controller uses this input to determine the operating mode of the controller at run time. Defined encodings are: 4'h0: PCI Express endpoint 4'h1: Legacy PCI Express endpoint 4'h4: Root port of PCI Express root complex
3	RW	0x0	link_req_rst_grt Link down reset request grant control. 1'b0: Disable link down reset request grant 1'b1: Enable link down reset request grant Reserved after r5p6(version 50600).
2	RW	0x0	app_ltssm_enable Driven low by your application after cold, warm, or hot reset to hold the LTSSM in the Detect state until your application is ready for the link training to begin. When your application has finished reprogramming the controller configuration registers using the DBI, it asserts app_ltssm_enable to allow the LTSSM to continue link establishment. Can also be used to delay hot resetting of the controller until you have read out any register status.

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Bit	Attr	Reset Value	Description
1	RW	0x0	app_req_retry_en Provides a capability to defer incoming configuration requests until initialization is complete. When app_req_retry_en is asserted, the controller completes incoming configuration requests with a configuration request retry status. Other incoming requests are not affected. When the Readiness Notification mechanism is supported, DRS messaging is blocked when app_req_retry_en=1. When app_req_retry_en=0 and app_drs_ready=1, the controller autonomously transmits a DRS message when the link transitions from DL_Down to DL_Up.
0	R/WSC	0x0	app_init_rst Request from your application to send a hot reset to the upstream port. The hot reset request is sent when a single cycle pulse is applied to this pin. In an upstream port, you should set this input to '0'.

PCIE_CLIENT_INTR_STATUS_MSG_RX

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	W1C	0x0	obff_cpu_active_int Interrupt indicates that the controller received an 'CPU Active' OBFF message. 1'b0: No interrupt 1'b1: Interrupt EP only. One-clock-cycle pulse that indicates that the controller received a 'CPU Active' OBFF message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message. Only usable in an upstream port.
13	W1C	0x0	obff_obff_int Interrupt indicates that the controller received an 'OBFF' OBFF message. 1'b0: No interrupt 1'b1: Interrupt EP only. if cfg_obff_en is not equal to 2'b11, then radm_msg_obff One-clock-cycle pulse that indicates that the controller received an 'OBFF' OBFF message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message. Only usable in an upstream port.
12	W1C	0x0	obff_idle_int Interrupt indicates that the controller received an 'IDLE' OBFF message. 1'b0: No interrupt 1'b1: Interrupt EP only. if cfg_obff_en is not equal to 2'b11, then radm_msg_idle One-clock-cycle pulse that indicates that the controller received an 'IDLE' OBFF message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message. Only usable in an upstream port.
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10	W1C	0x0	pm_turnoff_int Interrupt indicates that the controller received a PME Turnoff message. 1'b0: No interrupt 1'b1: Interrupt EP mode only. radm_pm_turnoff One-clock-cycle pulse that indicates that the controller received a PME Turnoff message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no indication is given for the second message.
9	W1C	0x0	pm_to_ack_int Interrupt indicates that the controller received a PME_TO_Ack message. 1'b0: No interrupt 1'b1: Interrupt RC mode only. radm_pm_to_ackOne-clock-cycle pulse that indicates that the controller received a PME_TO_Ack message. Upstream port: Reserved.
8	W1C	0x0	pm_pme_int Interrupt indicates that the controller received a PM_PME message. 1'b0: No interrupt 1'b1: Interrupt RC mode only. radm_pm_pme One-clock-cycle pulse that indicates that the controller received a PM_PME message.
7:6	RO	0x0	reserved
5	W1C	0x0	cfg_pme_msi_int Interrupt that indicates the controller received a cfg_pme_msi pulse. 1'b0: No interrupt 1'b1: Interrupt cfg_pme_msi asserted when all of the following conditions are true: 1. MSI or MSI-X is enabled. 2. The PME Interrupt Enable bit in Root Control register is set to 1. 3. The PME Status bit in Root Status register is set to 1. The controller does not check if the associated MSI vector (asserted cfg_pcie_cap_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked.
4	RO	0x0	cfg_pme_int Asserted when all of the following conditions are true: 1. The INTx Assertion Disable bit in the Command register is 0. 2. The PME Interrupt Enable bit in the Root Control register is set to 1. 3. The PME Status bit in the Root Status register is set to 1. The cfg_pme_msi output is a pulse signal (only asserted for one clock cycle). But cfg_pme_int is a level signal; essentially an AND of the PME interrupt enable and receipt of the pm_pme message.
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	W1C	0x0	ltr_msg_int Interrupt that indicates the controller received a LTR message. The LTR message information is available in PL_LTR_LATENCY_OFF registers. 1'b0: No interrupt 1'b1: Interrupt radm_msg_ltr One-clock-cycle pulse that indicates that the controller received an LTR message. The controller makes the message header available the radm_msg_payload output. It is also available the app_ltr_latency output. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message.
1	W1C	0x0	unlock_msg_int Interrupt indicates that the controller received an unlock message. 1'b0: No interrupt 1'b1: Interrupt radm_msg_unlock One-cycle pulse that indicates that the controller received an Unlock message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message.
0	W1C	0x0	ven_msg_int Interrupt that indicates radm_vendor_msg One-cycle pulse is received. The message header is available in VEN_MSG_RX_INFO registers. 1'b0: No interrupt 1'b1: Interrupt radm_vendor_msg One-cycle pulse that indicates the controller received a vendor-defined message. The controller makes the message header available the radm_msg_payload output. When FX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then both bits are asserted.

PCIE_CLIENT_INTR_STATUS_LEGACY

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	tx_intd_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTD Message to the upstream device. The signal assert_intd_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTD Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTD Message to the upstream device. The signal deassert_intd_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTD Message to the upstream device. EP mode only.

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Bit	Attr	Reset Value	Description
6	RO	0x0	tx_intc_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTC Message to the upstream device. The signal assert_intc_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTC Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTC Message to the upstream device. The signal deassert_intc_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTC Message to the upstream device. EP mode only.
5	RO	0x0	tx_intb_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTB Message to the upstream device. The signal assert_intb_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTB Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTB Message to the upstream device. The signal deassert_intb_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTB Message to the upstream device. EP mode only.
4	RO	0x0	tx_inta_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTA Message to the upstream device. The signal assert_inta_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTA Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTA Message to the upstream device. The signal deassert_inta_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTA Message to the upstream device. EP mode only.
3	RO	0x0	rx_intd_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTD Message from the downstream device. radm_intd_asserted One-clock-cycle pulse that indicates that the controller received an Assert_INTD Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTD Message from the downstream device. radm_intd_deasserted One-clock-cycle pulse that indicates that the controller received a Deassert_INTD Message from the downstream device. RC mode only.

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Bit	Attr	Reset Value	Description
2	RO	0x0	rx_intc_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTC Message from the downstream device. radm_intc_asserted One-clock-cycle pulse that indicates that the controller received an Assert_INTC Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTC Message from the downstream device. radm_intc_deasserted One-clock-cycle pulse that indicates that the controller received a Deassert_INTC Message from the downstream device. RC mode only.
1	RO	0x0	rx_intb_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTB Message from the downstream device. radm_intb_asserted One-clock-cycle pulse that indicates that the controller received an Assert_INTB Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTB Message from the downstream device. radm_intb_deasserted One-clock-cycle pulse that indicates that the controller received a Deassert_INTB Message from the downstream device. RC mode only.
0	RO	0x0	rx_inta_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTA Message from the downstream device. radm_inta_asserted One-clock-cycle pulse that indicates that the controller received an Assert_INTA Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTA Message from the downstream device. radm_inta_deasserted One-clock-cycle pulse that indicates that the controller received a Deassert_INTA Message from the downstream device. RC mode only.

PCIE_CLIENT_INTR_STATUS_ERR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	W1C	0x0	radm_qoverflow_int Pulse radm_qoverflow indicating that one or more of the P/NP/CPL receive queues have overflowed. There is a 1-bit indication for each configured virtual channel. You can connect this output to your internal error reporting mechanism 1'b0: No interrupt 1'b1: Interrupt
11	RO	0x0	reserved
10	W1C	0x0	f_err_rx_int One-clock-cycle radm_fatal_err pulse that indicates that the controller received an ERR_FATAL message. 1'b0: No interrupt 1'b1: Interrupt RC mode only.

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Bit	Attr	Reset Value	Description
9	W1C	0x0	nf_err_rx_int One-clock-cycle radm_nonfatal_err pulse that indicates that the controller received an ERR_NONFATAL message. 1'b0: No interrupt 1'b1: Interrupt RC mode only.
8	W1C	0x0	cor_err_rx_int One-clock-cycle radm_correctable_err pulse that indicates that the controller received an ERR_COR message. The controller makes the message header available the radm_msg_payload output. 1'b0: No interrupt 1'b1: Interrupt RC mode only.
7	RO	0x0	reserved
6	W1C	0x0	f_err_sent_int cfg_send_f_err indicates Sent Fatal Error. Controller has sent a message towards the Root Complex indicating that an Rx TLP that contained a fatal error, and that can not be corrected, has been received by the EndPoint. 1'b0: No interrupt 1'b1: Interrupt EP mode only.
5	W1C	0x0	nf_err_sent_int cfg_send_nf_err indicates Sent Non-Fatal Error. Controller has sent a message towards the Root Complex indicating that an Rx TLP that contained a non-fatal error, and that can not be corrected, has been received by the EndPoint. 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	cor_err_sent_int cfg_send_cor_err indicates sent correctable error. Controller has sent a message towards the Root Complex indicating that an Rx TLP that contained an error, and that can be corrected, has been received by the EndPoint 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	tx_cpl_timeout_int trgt_cpl_timeout indicates that the application has not generated a completion for an incoming request within the required time interval. Information about the timed-out completion is available the trgt_timeout_* outputs listed later. When a completion timeout occurs, the controller does not clear the corresponding entry from the completion lookup table. The default completion timeout value is approximately 10 ms. 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	rx_cpl_timeout_int radm_cpl_timeout indicates that the completion TLP for a request has not been received within the expected time window. 1'b0: No interrupt 1'b1: Interrupt Can find the timed-out completion information in RX_CPL_TIME_OUT_INFO register.

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Bit	Attr	Reset Value	Description
1	W1C	0x0	aer_rc_err_msi The controller asserts cfg_aer_rc_err_msi for one clock cycle when all of the following conditions are true: 1. MSI or MSI-X is enabled. 2. A reported error condition causes a bit to be set in the Root Error Status register. 3. The associated error message reporting enable bit is set in the Root Error Command register. The controller does not check if the associated MSI vector (asserted cfg_aer_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked. RC mode only.
0	RO	0x0	aer_rc_err_int Asserted when a reported error condition causes a bit to be set in the Root Error Status register and the associated error message reporting enable bit is set in the Root Error Command register. cfg_aer_rc_err_int is set when the RC internally generates an error or when an error message is received by the RC. Because the RC itself generates it, this needs to be propagated up to the system software which would then need to read the error registers to see which error occurred. Note: This signal is used when MSI/MSI-X is NOT enabled; otherwise see cfg_aer_rc_err_msi. RC mode only.

PCIE_CLIENT_INTR_STATUS_MISC

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	ep_elbi_app_int Interrupt generated by ELBI application register access. 1'b0: No interrupt 1'b1: Interrupt
14	RO	0x0	link_eq_req_int Interrupt indicating to your application that the Link Equalization Request bit in the Link Status 2 Register has been set and the Link Equalization Request Interrupt Enable (Link Control 3 Register bit 1) is set. cfg_link_eq_req_int 1'b1: Interrupt 1'b0: No interrupt
13	W1C	0x0	rbar_update_int Indicates that a resizable BAR control register has been updated: 1 bit per Physical function. 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
12	W1C	0x0	dpa_sub_upd_int DPA Substate-Updated Indication Signal Bus. The controller asserts "dpa_substate_update" for one core_clk cycle when the Substate Control field of the DPA Control Register has been updated with a new value for the associated function. The controller asserts it when the updated value of the Substate Control field does not match the Substate Status field of the Status Register when the Substate Control Enable bit field of the Status Register is set to "1". Note: Your application logic is required to do the following: 1. Detect the one cycle pulse on the signal for the relevant function. 2. Read the function's substate control register to determine the software's target substate (transition). 3. Read the function's transition latency value, unit, and indicator. Calculate the maximum transition latency for the substate transition. 4. Execute the substate transition and complete it within the maximum transition latency. 5. Update the substate status after completing the transition through a DBI write. The controller updates the substate status during the substate transition if the transition is from a lower power substate to a higher; the status is the higher power substate during the substate transition.
11	RO	0x0	edma_rd_int DMA read channel interrupt. Indicates that the DMA transfer has completed or that an error has occurred. 1'b0: No interrupt 1'b1: Interrupt
10	RO	0x0	edma_wr_int DMA write channel interrupt. Indicates that the DMA transfer has completed or that an error has occurred. This is a level interrupt. 1'b0: No interrupt 1'b1: Interrupt
9	W1C	0x0	bw_mgt_msi The controller sets this pin when following conditions are true: 1. MSI or MSI-X is enabled. 2. The Link Bandwidth Management Status register (Link Control Status register bit 14) is updated 3. The Link Bandwidth Management Interrupt Enable (Link Control register bit 10) is set. reuse-pragma begin Attr Description This pin is set as a notification when the Link Bandwidth Management Status register (Link Status register bit 14) is updated and the Link Bandwidth Management Interrupt Enable (Link Control register bit 10) is set and in addition the msi or msix are enabled . This bit is not applicable to, and is reserved, for endpoint devices and upstream ports of Switches. For upstream port: Reserved. <ct:CX_IS_EP>Reserved.

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Bit	Attr	Reset Value	Description
8	RO	0x0	bw_mgt_int The controller asserts cfg_bw_mgt_int when all of the following conditions are true: 1. The INTx Assertion Disable bit in the Command register is 0, and 2. The Bandwidth Management Interrupt Enable bit in the Link Control register is set to 1, and 3. The Bandwidth Management Interrupt Status bit in the Link Status register is set to 1. The cfg_bw_mgt_msi output is a pulse signal (only asserted for one clock cycle); but cfg_bw_mgt_int is a level signal. For upstream port: Reserved.
7	W1C	0x0	link_auto_bw_msi The controller sets this pin when following conditions are true: 1. MSI or MSI-X is enabled. 2. The Link Autonomous Bandwidth Status register (Link Status register bit 15) is updated. 3. The Link Autonomous Bandwidth Interrupt Enable (Link Control register bit 11) is set. The controller does not check if the associated MSI vector (asserted cfg_pcie_cap_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked. For upstream port: Reserved. <ct:CX_IS_EP>Reserved.
6	RO	0x0	link_auto_bw_int The controller asserts cfg_link_auto_bw_int when all of the following conditions are true: 1. The INTx assertion disable bit in the Command register is 0, and 2. The Link Autonomous Bandwidth Interrupt Enable bit in the Link Control register is set to 1, and 3. The Link Autonomous Bandwidth Interrupt Status bit in the Link Status register is set to 1. The cfg_link_auto_bw_msi output is a pulse signal (only asserted for one clock cycle); but cfg_link_auto_bw_int is a level signal. For upstream port: Reserved.
5	W1C	0x0	hp_msi The controller asserts hp_msi (as a one-cycle pulse) when the logical AND of the following conditions transitions from false to true: 1. MSI or MSI-X is enabled. 2. Hot-Plug interrupts are enabled in the Slot Control register. 3. Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function. The controller pulses the hp_msi output only when any of the hot plug status bits change from 0 to 1 (as is hp_pme).

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Bit	Attr	Reset Value	Description
4	RO	0x0	hp_int The controller asserts hp_int when all of the following conditions are true: 1. The INTx Assertion Disable bit in the Command register is 0. 2. Hot-Plug interrupts are enabled in the Slot Control register. 3. Any bit in the Slot Status register is equal to 1, and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function.
3	W1C	0x0	hp_pme_int The controller asserts hp_pme when all of the following conditions are true: 1. The PME Enable bit in the Power Management Control and Status register is set to 1. 2. Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. The controller does not check if the PM state is D1, D2, or D3hot. It is up to your application to check the value pm_dstate to make sure the device is in D1, D2, or D3hot. There is one bit of hp_pme for each configured function. The controller pulses the hp_pme output only when any hot plug status bit changes from 0 to 1 (as is hp_msi). hp_int stays asserted as long as the status bit is set. In addition, it asserts hp_pme only if PME is enabled, but it does not matter if hot-plug interrupts are enabled.
2	W1C	0x0	link_req_rst_not_int Early version of the link_req_rst_not signal. For more information, see the 'Warm and Hot Resets' section in the Architecture chapter of the Databook. smlh_req_rst_not. 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	dll_link_up_int Data link layer up/down indicator (rdlh_link_up): This status from the flow control initialization state machine indicates that flow control has been initiated and the Data link layer is ready to transmit and receive packets. For multi-VC designs, this signal indicates status for VC0 only. 1'b0: Link is down 1'b1: Link is up
0	W1C	0x0	phy_link_up_int PHY "smlh_link_up" Link up/down indicator. 1'b0: Link is down 1'b1: Link is up

PCIE_CLIENT_INTR_STATUS_PMC

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
8	W1C	0x0	pm_dstate_update_int Interrupt indicates that the current power management D-state have changed. The current power management D-state of pm_dstate the function: 1. 000b: D0 2. 001b: D1 3. 010b: D2 4. 011b: D3 5. 100b: Uninitialized 6. Other values: Not applicable There are 3 bits of pm_dstate for each configured function. 1'b0: No interrupt 1'b1: Interrupt
7	W1C	0x0	linkst_out_l0s_int Power management is in L0s state. Indicates in L0_STALL state when M-PCIe Interrupt that indicates link has entered L0s state (falling edge detected of pm_linkst_in_l0s in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
6	W1C	0x0	linkst_out_l2_int Power management is in L2 state. Interrupt that indicates link has entered L2 state (falling edge detected of pm_linkst_in_l2 in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
5	W1C	0x0	linkst_out_l1_int Power management is in L1 state. Interrupt that indicates link has entered L1 state (falling edge detected of pm_linkst_in_l1 in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	linkst_out_l1sub_int Power management is in L1 substate. Indicates when the link has entered L1 substates. It is used to ensure that the switching back of aux_clk from AUXCLK to PCLK occurs only after L1 substates have been exited. For L1.2 this signal is de-asserted at the end of the L1.2.Exit state, after the t_power_on constraint has been satisfied. External logic can use the transition high to low on this signal to initiate REFCLK restore. Interrupt indicates link has entered L1 substate (falling edge detected of pm_linkst_in_l1sub in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	linkst_in_l0s_int Power management is in L0s state. Indicates in L0_STALL state when M-PCIe Interrupt that indicates link has entered L0s state (rising edge detected of pm_linkst_in_l0s in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt

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Bit	Attr	Reset Value	Description
2	W1C	0x0	linkst_in_l2_int Power management is in L2 state. Interrupt that indicates link has entered L2 state (rising edge detected of pm_linkst_in_l2 in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	linkst_in_l1_int Power management is in L1 state. Interrupt that indicates link has entered L1 state (rising edge detected of pm_linkst_in_l1 in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	linkst_in_l1sub_int Power management is in L1 substate. Indicates when the link has entered L1 substates. It is used to ensure that the switching back of aux_clk from AUXCLK to PCLK occurs only after L1 substates have been exited. For L1.2 this signal is de-asserted at the end of the L1.2.Exit state, after the t_power_on constraint has been satisfied. External logic can use the transition high to low on this signal to initiate REFCLK restore. Interrupt indicates link has entered L1 substate (rising edge detected of pm_linkst_in_l1sub in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt

PCIE_CLIENT_INTR_MASK_MSG_RX

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x1	obff_cpu_active_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
13	RW	0x1	obff_obff_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
12	RW	0x1	obff_idle_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
11	RO	0x0	reserved
10	RW	0x1	pm_turnoff_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
9	RW	0x1	pm_to_ack_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

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Bit	Attr	Reset Value	Description
8	RW	0x1	pm_pme_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
7:6	RO	0x0	reserved
5	RW	0x1	cfg_pme_msi_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
4	RW	0x1	cfg_pme_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
3	RO	0x0	reserved
2	RW	0x1	ltr_msg_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
1	RW	0x1	unlock_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
0	RW	0x1	ven_msg_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

PCIE_CLIENT_INTR_MASK_LEGACY

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	tx_intd_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
6	RW	0x1	tx_intc_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
5	RW	0x1	tx_intb_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
4	RW	0x1	tx_inta_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
3	RW	0x1	rx_intd_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

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Bit	Attr	Reset Value	Description
2	RW	0x1	rx_intc_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
1	RW	0x1	rx_intb_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
0	RW	0x1	rx_inta_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

PCIE_CLIENT_INTR_MASK_ERR

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x1	radm_qoverflow_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
11	RO	0x0	reserved
10	RW	0x1	f_err_rx_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
9	RW	0x1	nf_err_rx_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
8	RW	0x1	cor_err_rx_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
7	RO	0x0	reserved
6	RW	0x1	f_err_sent_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
5	RW	0x1	nf_err_sent_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
4	RW	0x1	cor_err_sent_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
3	RW	0x1	tx_cpl_timeout_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

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Bit	Attr	Reset Value	Description
2	RW	0x1	rx_cpl_timeout_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
1	RW	0x1	aer_rc_err_msi_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
0	RW	0x1	aer_rc_err_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

PCIE_CLIENT_INTR_MASK_MISC

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	ep_elbi_app_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
14	RW	0x1	link_eq_req_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
13	RW	0x1	rbar_update_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
12	RW	0x1	dpa_sub_upd_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
11	RW	0x1	edma_rd_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
10	RW	0x1	edma_wr_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
9	RW	0x1	bw_mgt_msi_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
8	RW	0x1	bw_mgt_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

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Bit	Attr	Reset Value	Description
7	RW	0x1	link_auto_bw_msi_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
6	RW	0x1	link_auto_bw_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
5	RW	0x1	hp_msi_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
4	RW	0x1	hp_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
3	RW	0x1	hp_pme_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
2	RW	0x1	link_req_rst_not_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
1	RW	0x1	dll_link_up_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
0	RW	0x1	phy_link_up_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

PCIE_CLIENT_INTR_MASK_PMC

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x1	pm_dstate_update_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
7	RW	0x1	linkst_out_l0s_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
6	RW	0x1	linkst_out_l2_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

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Bit	Attr	Reset Value	Description
5	RW	0x1	linkst_out_l1_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
4	RW	0x1	linkst_out_l1sub_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
3	RW	0x1	linkst_in_l0s_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
2	RW	0x1	linkst_in_l2_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
1	RW	0x1	linkst_in_l1_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
0	RW	0x1	linkst_in_l1sub_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

PCIE_CLIENT_POWER_CON

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_req_n_con Valid when clk_req_n_bypass set to 1. 1'b1: Tristate CLKREQ# 1'b0: Pull down CLKREQ#
12	RW	0x0	clk_req_n_bypass 1'b0: clk_req_n does not bypass, CLKREQ# driven by controller 1'b1: clk_req_n bypass, CLKREQ# driven by bit 13 of POWER_CON
11:10	RW	0x0	p2_cpm_disable 2'b00: When phy in P2 power state, enable clock PM for both L1 and L2 2'b01: When phy in P2 power state, enable clock PM for L2 but disable for L1 2'b10: When phy in P2 power state, disable clock PM for L2 but enable for L1 2'b11: When phy in P2 power state, disable clock PM for both L1 and L2 Reserved after r5p6(version 50600).
9	RW	0x0	app_clk_pm_en Clock PM feature enabled by application. Used to inhibit the programming of the Clock PM in Link Control Register. For more information, see 'L1 with Clock PM (L1 with REFCLK removal/PLL Off)'.

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Bit	Attr	Reset Value	Description
8	RW	0x0	sys_aux_pwr_det Auxiliary Power Detected. Used to report to the host software that auxiliary power (Vaux) is present. 1'b0: Auxiliary power is not present 1'b1: Auxiliary power is present
7	RO	0x0	reserved
6	RW	0x0	app_l1sub_disable The application can set this input to 1'b1 to prevent entry to L1 Sub-states. This pin is used to gate the L1 sub-state enable bits from the L1 PM Substates Control 1 Register.
5	RW	0x0	app_xfer_pending Indicates that your application has transfers pending. 1'b1: There are transactions outside the controller that the controller needs to transmit. For EP mode, prevents generation of requests to enter L1. Triggers exit if already in L1. For RC mode, triggers exit if already in L1. 1'b0: There are no transactions outside the controller. Indicates that your application has transfers pending and prevents the controller from entering L1. If the entry into L1 is already in progress, assertion of app_xfer_pending causes an exit from L1. This is a level signal used to inform the controller about the state of external queues and pipeline stages that contain transactions to be transmitted by the controller. The controller uses this information to determine when to enter/exit L1. When this signal is asserted, it indicates that there are transactions outside the controller that the controller needs to transmit. When de-asserted, it indicates that there are no transactions outside the controller. The controller responds to an assertion on this signal as follows: 1. Upstream Ports: Prevents generation of requests to enter L1. Triggers exit if already in L1. 2. Downstream Ports: Triggers exit if already in L1. You can instruct the controller to exit L1 by asserting either or both of app_xfer_pending and app_req_exit_l1. The controller only samples app_req_exit_l1 when the controller is already in the L1 state.
4	R/WSC	0x0	app_req_exit_l1 1'b0: Self clear to generate a pulse to controller. 1'b1: Application request to Exit L1. Application request to Exit L1. Request from your application to exit L1. It is only effective when L1 is enabled.
3	RW	0x1	app_ready_entr_l23 1'b0: Application not ready to enter L23. 1'b1: Application ready to enter L23. Application Ready to Enter L23. Indication from your application that it is ready to enter the L23 state. The app_ready_entr_l23 signal is provided for applications that must control L23 entry (in case certain tasks must be performed before going into L23). The controller delays sending PM_Enter_L23 (in response to PM_Turn_Off) until this signal becomes active. When this signal has been asserted by the application, it must be kept asserted until L2 entry has completed. Hardwire to 1 for applications that do not require this feature. Note: The controller ignores this input in RC mode.

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Bit	Attr	Reset Value	Description
2	R/WSC	0x0	app_req_entr_l1 Application request to Enter L1 ASPM state. 1'b0: Self clear to generate a pulse to controller 1'b1: Application request to enter L1 state Application request to Enter L1 ASPM state. The app_req_entr_l1 signal is for use by applications that need to control L1 entry instead of using the L1 entry timer as defined in the PCI Express Specification. It is only effective when L1 is enabled. The controller latches this request when in L0 or L0s; to be acted upon later. Note: The controller ignores this input in RC mode.
1	R/WSC	0x0	app_pm_xmt_pme Wake Up. If PME is enabled and PME support is configured for current PMCSR D-state asserting this signal (apps_pm_xmt_pme) causes the controller to wake from either L1 or L2 state. When the controller has transitioned back to the L0 state it transmits a PME message and set the PME_Status. Upon receiving the PME message the root complex should clear the PME_Status and change the D-state back to D0.
0	RW	0x0	app_clk_req_n Indicates that the application logic is ready to have reference clock removed. In designs which support reference clock removal through either L1 PM Sub-states or L1 CPM, the application should set this signal to 1'b1 if it supports reference clock removal. If the application does not want to remove reference clock it should set this signal to 1'b0. This signal should be asserted or de-asserted when L1 CPM or L1 Sub-states are being configured, it should not be changed dynamically during L1. Indicates that the application is ready to have reference clock removed. 1'b0: Application does not want to remove reference clock 1'b1: Application is ready to have reference clock removed

PCIE_CLIENT_POWER_STATUS

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	pm_clkreq_in Status of wire CLKREQ# GPIO.
27	RO	0x0	pm_clkreq_out Status of CLKREQ# output drive signal.
26	RO	0x0	pm_wake_in Status of wire WAKE# GPIO.
25	RO	0x0	pm_wake_out The wake state of the wake_out 1'b0: Controller is not in wake process or Link already back to L0 1'b1: Controller assert WAKE# signal to request to make link back to L0 EP only.
24	RO	0x0	pm_linkst_in_l0s Power management is in L0s state. 1'b0: Power management is not in L0s. 1'b1: Power management is in L0s.

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Bit	Attr	Reset Value	Description
23	RO	0x0	pm_linkst_in_l2 Power management is in L2 state. 1'b0: Power management is not in L2 1'b1: Power management is in L2
22	RO	0x0	pm_linkst_in_l1 Power management is in L1 state. 1'b0: Power management is not in L1 1'b1: Power management is in L1
21	RO	0x0	pm_linkst_in_l1sub Power management is in L1 substate. Indicates when the link has entered L1 substates. It is used to ensure that the switching back of aux_clk from AUXCLK to PCLK occurs only after L1 substates have been exited. For L1.2 this signal is de-asserted at the end of the L1.2.Exit state, after the t_power_on constraint has been satisfied. External logic can use the transition high to low on this signal to initiate REFCLK restore. 1'b0: Power management is not in L1 substate 1'b1: Power management is in L1 substate
20	RO	0x0	reserved
19:17	RO	0x0	pm_l1sub_state Power management L1 sub-states FSM state. For debugging purposes, not for system operation. 3'b000: L1_U 3'b001: L1_0 3'b010: L1_0_WAIT4_ACK 3'b011: L1_0_WAIT4_CLKREQ 3'b100: L1_N_ENTRY 3'b101: L1_N 3'b110: L1_N_EXIT 3'b111: L1_N_ABORT
16:15	RO	0x0	reserved
14:10	RO	0x00	pm_slave_state Power management slave FSM state. For debugging purposes, not for system operation.
9	RO	0x0	reserved
8:4	RO	0x00	pm_master_state Power management master FSM state. For debugging purposes, not for system operation.
3	RO	0x0	reserved
2:0	RO	0x0	pm_curnt_state Indicates the current power state. For debugging purposes, not for system operation.

PCIE_CLIENT_MSG_GEN_CON

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	R/W SC	0x0	obff_cpu_active_msg_req Request controller to generate a "CPU Active" OBFF message. This bit clears automatically when request has been sent. Only usable in a downstream port. When application sets OBFF Enable bit in Device Control 2 Register to choose to use OBFF message or WAKE# signaling.
13	R/W SC	0x0	obff_obff_msg_req Request controller to generate a "OBFF" OBFF message. This bit clears automatically when request has been sent. Only usable in a downstream port. When application sets OBFF Enable bit in Device Control 2 Register to choose to use OBFF message or WAKE# signaling.
12	R/W SC	0x0	obff_idle_msg_req Request controller to generate a "IDLE" OBFF message. This bit clears automatically when request has been sent. Only usable in a downstream port. When application sets OBFF Enable bit in Device Control 2 Register to choose to use OBFF message or WAKE# signaling.
11:9	RO	0x0	reserved
8	R/W SC	0x0	app_ltr_msg_req Indicates that your application is requesting to send an LTR message. Once asserted, app_ ltr_msg_req must remain asserted until the controller asserts app_ltr_msg_grant. Set to request controller to send a LTR Message. This bit clears automatically when request is granted by controller. Application should put LTR message information ready in LTR_MSG_TX_INFO register before setting this bit.
7:6	RO	0x0	reserved
5	R/W SC	0x0	app_unlock_msg Request from your application to generate an Unlock message. You must assert this signal for one clock cycle. The controller does not return an acknowledgment or grant signal. You must not pulse the same signal again, until the previous message has been transmitted.
4	R/W SC	0x0	apps_pm_xmt_turnoff Request from your application to generate a PM_Turn_Off message. You must assert this signal for one clock cycle. The controller does not return an acknowledgment or grant signal. You must not pulse the same signal again, until the previous message has been transmitted.
3:2	RO	0x0	reserved
1	RW	0x0	legacy_int_req When legacy_int_req (sys_int) goes from low to high, the controller generates an Assert_INTx Message. When sys_int goes from high to low, the controller generates a Deassert_INTx Message. There is a separate sys_int input bit for each function in your controller configuration. The Interrupt Pin register for the corresponding function determines which INTx Message the controller generates (INTA, INTB, INTC, or INTD). Legacy and native PCIe devices capable of generating an interrupt must support both Assert_INTx/Deassert_INTx and MSI or MSI-X. sys_int is intended to generate a message that emulates the legacy PCI Interrupts.

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Bit	Attr	Reset Value	Description
0	R/W SC	0x0	ven_msg_req Set to request controller to send a vendor-defined Message. This bit clears automatically when request is granted by controller. Application should put vendor message information ready in VEN_MSG_TX_CFGx registers before setting this bit. Request from your application to send a vendor-defined Message. Once asserted, ven_msg_req must remain asserted until the controller asserts ven_msg_grant.

PCIE_CLIENT_MSI_GEN_CON

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	R/W SC	0x00000000	msi_gen_req 32 bits write only MSI generation request signals. MSB has the highest priority and LSB has the lowest priority. Write 1 to a certain bit request the controller send a MSI interrupt. Software should use MSI capability register to access MSI mask or pending status.

PCIE_CLIENT_MSI_GEN_FNUM_TC

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	ven_msi_tc Traffic Class of the MSI request, valid when ven_msi_req is asserted.
3	RO	0x0	reserved
2:0	RW	0x0	ven_msi_func_num The function number of the MSI request.

PCIE_CLIENT_RBAR_SIZE_INFO0

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RO	0x00	bar2_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.
15:14	RO	0x0	reserved
13:8	RO	0x00	bar1_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.
7:6	RO	0x0	reserved
5:0	RO	0x00	bar0_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.

PCIE_CLIENT_RBAR_SIZE_INFO1

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:16	RO	0x00	bar5_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.
15:14	RO	0x0	reserved
13:8	RO	0x00	bar4_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.
7:6	RO	0x0	reserved
5:0	RO	0x00	bar3_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.

PCIE_CLIENT_DMA_HSHAKE_TOGG

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	dma_rdxfer_done_togg DMA read engine descriptor transfer done toggle signal. One bit for each implemented DMA read channel. After a doorbell command, this signal is de-asserted. When a channel is operating in non-linked list mode this signal does not toggles.
11:8	RO	0x0	dma_wdxfer_done_togg DMA write engine descriptor transfer done toggle signal. One bit for each implemented DMA write channel. After a doorbell command, this signal is de-asserted. When a channel is operating in non-linked list mode this signal does not toggles.
7:4	RW	0x0	app_rdxfer_go_togg DMA read engine descriptor transfer go toggle signal. One bit for each implemented DMA read channel. This signal is ignored whenever a DMA channel operates in non-linked mode.
3:0	RW	0x0	app_wdxfer_go_togg DMA Write engine descriptor transfer go toggle signal. One bit for each implemented DMA write channel. This signal is ignored whenever a DMA channel operates in non-linked mode.

PCIE_CLIENT_VEN_MSG_RX_INFO0

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	ven_msg_req_id The requester ID of the received Message(radm_msg_req_id). Bit[15:8]: Bus number Bit[7:3]: Device number Bit[2:0]: Function number

PCIE_CLIENT_VEN_MSG_RX_INFO1

Address: **Operational Base** + offset (0x0054)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ven_msg_header_l The third double word of the Vendor Defined Message header. Received message header information. When a vendor-defined or ltr message is received (radm_vendor_msg=1 or radm_ltr_msg=1), the controller maps radm_msg_payload to the Rx TLP header dwords as follows: When RX_TLP =1 Bit[31:0] = bytes 12-15 (4th dword), where [7:0] =byte 15 Bit[63:32] = bytes 8-11 (3rd dword)

PCIE_CLIENT_VEN_MSG_RX_INFO2

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ven_msg_header_h The fourth double word of the Vendor Defined Message header. Received message header information. When a vendor-defined or ltr message is received (radm_vendor_msg=1 or radm_ltr_msg=1), the controller maps radm_msg_payload to the Rx TLP header dwords as follows: When RX_TLP =1 Bit[31:0] = bytes 12-15 (4th dword), where [7:0] =byte 15 Bit[63:32] = bytes 8-11 (3rd dword)

PCIE_CLIENT_VEN_MSG_TX_CFG0

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	ven_msg_code The Message Code for the vendor-defined Message TLP.
23:16	RW	0x00	ven_msg_tag Tag for the vendor-defined Message TLP.
15:11	RO	0x00	reserved
10:9	RW	0x0	ven_msg_attr The Attributes field for the vendor-defined Message TLP. bit1: Relaxed ordering. bit0: No snoop.
8	RW	0x0	ven_msg_ep The Poisoned TLP (EP) bit for the vendor-defined Message TLP.
7:5	RW	0x0	ven_msg_tc The Traffic Class field for the vendor-defined Message TLP.
4:0	RW	0x00	ven_msg_type The TYPE field for the vendor-defined Message TLP.

PCIE_CLIENT_VEN_MSG_TX_CFG1

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ven_msg_data_l The third double word of the Vendor Defined Message header. Third and fourth dwords of the Vendor Defined Message header where: 1. Bytes 8-11 (third header dword) =ven_msg_data[63:32] 2. Bytes 12-15 (fourth header dword) =ven_msg_data[31:0], where ven_msg_data[7:0] =byte 15 For more information, see the 'Endianness' advanced information chapter.

PCIE_CLIENT_VEN_MSG_TX_CFG2

Address: **Operational Base** + offset (0x0064)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ven_msg_data_h The fourth double word of the Vendor Defined Message header. Third and fourth dwords of the Vendor Defined Message header where: 1. Bytes 8-11 (third header dword) =ven_msg_data[63:32] 2. Bytes 12-15 (fourth header dword) =ven_msg_data[31:0], where ven_msg_data[7:0] =byte 15 For more information, see the 'Endianness' advanced information chapter.

PCIE_CLIENT_LTR_MSG_TX_INFO

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_ltr_msg_latency LTR message that your application is requesting to send. The message format is defined in the PCI Express Specification.

PCIE_CLIENT_APP_ERR_RPT_INFO0

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_hdr_log0 The header(bit 0 to bit 31) of the TLP that contained the error. The header of the TLP that contained the error indicated app_err_bus, valid when 1. app_hdr_valid is asserted. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register.

PCIE_CLIENT_APP_ERR_RPT_INFO1

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_hdr_log1 The header(bit 32 to bit 63) of the TLP that contained the error. The header of the TLP that contained the error indicated app_err_bus, valid when 1. app_hdr_valid is asserted. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register.

PCIE_CLIENT_APP_ERR_RPT_INFO2

Address: **Operational Base** + offset (0x0074)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_hdr_log2 The header(bit 64 to bit 95) of the TLP that contained the error. The header of the TLP that contained the error indicated app_err_bus, valid when 1. app_hdr_valid is asserted. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register.

PCIE_CLIENT_APP_ERR_RPT_INFO3

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_hdr_log3 The header (bit 96 to bit 127) of the TLP that contained the error. The header of the TLP that contained the error indicated app_err_bus, valid when 1. app_hdr_valid is asserted. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register.

PCIE_CLIENT_APP_ERR_RPT_INFO4

Address: **Operational Base** + offset (0x007C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	app_err_advisory Indicates that your application error is an advisory error. Your application should assert app_err_advisory under either of the following conditions: 1. The controller is configured to mask completion timeout errors, your application is reporting a completion timeout error app_err_bus, and your application intends to resend the request. In such cases the error is an advisory error, as described in PCI Express Specification. When your application does not intend to resend the request, then your application must keep app_err_advisory de-asserted when reporting a completion timeout error. 2. The controller is configured to forward poisoned TLPs to your application and your application is going to treat the poisoned TLP as a normal TLP, as described in PCI Express Specification. Upon receipt of a poisoned TLP, your application must report the error app_err_bus, and either assert app_err_advisory (to indicate an advisory error) or de-assert app_err_advisory (to indicate that your application is dropping the TLP). 1'b0: Application error is not an advisory error 1'b1: Application error is an advisory error
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	app_err_bus The type of error that application detected. The controller combines the values err_bus bits with the internally detected error signals to set the corresponding bit in the Un-correctable or Correctable Error Status Registers [0]: Malformed TLP [1]: Receiver Overflow [2]: Unexpected completion [3]: Completer abort [4]: Completion Timeout [5]: Unsupported request [6]: ECRC Check Failed [7]: Poisoned TLP received [8]: AtomicOp Egress Blocked [9]: Un-correctable Internal Error [10]: Corrected Internal Error [11]: TLP Prefix Blocked Error Status: only valid for RC and when CX_NPRFX >0 [12]: ACS Violation: only valid when CX_ACS_ENABLE =1

PCIE_CLIENT_OBFF_WAKE_ELE_CFG

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RW	0xb4	wk_min_f2f_wdt Configure the minimum falling edge to falling edge width. The minimum value Specification define is 700ns. Application set this value equals to wk_min_f2f_wdt * core_clock_period(8ns in gen1 and 4ns in gen2).
23:16	RW	0xf0	wk_max_f2f_wdt Configure the maximum falling edge to falling edge width. The maximum value Specification define is 1000ns. Application set this value equals to wk_max_f2f_wdt * core_clock_period(8ns in gen1 and 4ns in gen2).
15:8	RW	0x50	wk_mim_pls_wdt Configure the minimum WAKE# pulse width for both active-inactive-active and inactive-active-inactive pulse. The minimum value Specification define is 300ns. Application set this value equals to wk_mim_pls_wdt * core_clock_period(8ns in gen1 and 4ns in gen2).
7:0	RW	0x64	wk_max_pls_wdt Configure the maximum WAKE# pulse width for both active-inactive-active and inactive-active-inactive pulse. The maximum value Specification define is 500ns. Application set this value equals to wk_max_pls_wdt * core_clock_period(8ns in gen1 and 4ns in gen2). Setting this value less than 50% of {wk_max_f2f_wdt * core_clock_period}.

PCIE_CLIENT_OBFF_WAKE_DEBUG

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	obff_wake_dec_err Error state of OBFF decoder FSM, used for debug.
7:4	RO	0x0	obff_wake_dec_state Current state of OBFF decoder FSM, used for debug.

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Bit	Attr	Reset Value	Description
3	RW	0x0	obff_wake_dec_cpu 1'b0: Do not initialize to CPU ACTIVE state 1'b1: Initialize the OBFF decoder to CPU ACTIVE state when obff_wake_dec_init is set
2	RW	0x0	obff_wake_dec_obff 1'b0: Do not initialize to OBFF state 1'b1: Initialize the OBFF decoder to OBFF state when obff_wake_dec_init is set
1	RW	0x0	obff_wake_dec_idle 1'b0: Do not initialize to IDLE state 1'b1: Initialize the OBFF decoder to IDLE state when obff_wake_dec_init is set
0	RW	0x0	obff_wake_dec_init 1'b0: Do not initialize the OBFF decoder 1'b1: Initialize the OBFF decoder

PCIE_CLIENT_RX_CPL_TIME_OUT_INFO

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	radm_timeout_cpl_tag The Tag field of the timeout completion (radm_timeout_cpl_tag).
23:12	RO	0x000	radm_timeout_cpl_len Length (in bytes) of the timeout completion. For a split completion, it indicates the number of bytes remaining to be delivered when the completion timeout (radm_timeout_cpl_len).
11:10	RO	0x0	reserved
9:8	RO	0x0	radm_timeout_cpl_attr The Attributes field of the timeout completion (radm_timeout_cpl_attr).
7	RO	0x0	reserved
6:4	RO	0x0	radm_timeout_cpl_tc The Traffic Class of the timed-out completion (radm_timeout_cpl_tc).
3	RO	0x0	reserved
2:0	RO	0x0	radm_timeout_func_num The function Number of the timed-out completion (radm_timeout_func_num). Function numbering starts at '0'.

PCIE_CLIENT_TX_CPL_TIME_OUT_INFO0

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:12	RO	0x000	trgt_timeout_cpl_len The Length of the timeout completion (trgt_timeout_cpl_len).
11:10	RO	0x0	reserved
9:8	RO	0x0	trgt_timeout_cpl_attr The Attributes value of the timeout completion (trgt_timeout_cpl_attr).
7	RO	0x0	reserved
6:4	RO	0x0	trgt_timeout_cpl_tc The TC of the timeout completion (trgt_timeout_cpl_tc).
3	RO	0x0	reserved
2:0	RO	0x0	trgt_timeout_func_num The function number of the timed-out completion. Function numbering starts at '0' (trgt_timeout_cpl_func_num).

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PCIE_CLIENT_TX_CPL_TIME_OUT_INFO1

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	trgt_lookup_empty When this signal is asserted with radm_trgt1_hv, it indicates that the target completion LUT is not full. The application can use this signal to determine a back-pressure mechanism to the controller so that there is not an overflow condition when the number of outstanding non-posted transactions received is more than expected. Your application logic must drive trgt1_radm_halt with the logical OR of your application halt signal and the inverse of this output.
15:8	RO	0x00	trgt_lookup_id The target completion LUT lookup ID for the incoming request TLP. When using the optional target completion lookup table feature, the application must save the lookup ID and assert the same lookup ID client0/1/2_cpl_lookup_id when generating a completion for the request.
7:0	RO	0x00	trgt_timeout_lookup_id The target completion LUT lookup ID of the timeout completion

PCIE_CLIENT_LOCAL_CRU_CTRL

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	radm_gate_disable Disable the radm_clk gating in local cru.
12	RW	0x0	aux_gate_disable Disable the aux_clk gating in local cru. Reserved after r5p6 (version 50600)
11	RW	0x0	link_down_gate_disable Disable the link down clock gating in local cru. Reserved after r5p6 (version 50600)
10	RW	0x0	dbi_aclk_gate_disable Disable the dbi_aclk gating in local cru. Reserved after r5p6 (version 50600)
9	RW	0x0	slv_aclk_gate_disable Disable the slv_aclk gating in local cru. Reserved after r5p6 (version 50600)
8	RW	0x0	mstr_aclk_gate_disable Disable the mstr_aclk gating in local cru. Reserved after r5p6 (version 50600)
7:4	RO	0x0	reserved
3	RW	0x0	pcie_pm_phy_req_disable Mask the phy reset request from controller pm. Reserved after r5p6 (version 50600)
2	RW	0x0	pcie_pm_srst_req_disable Mask the sticky reset request from controller pm. Reserved after r5p6 (version 50600)

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Bit	Attr	Reset Value	Description
1	RW	0x0	pcie_pm_nsrst_req_disable Mask the non-sticky reset request from controller pm. Reserved after r5p6 (version 50600)
0	RW	0x0	pcie_pm_crst_req_disable Mask the core reset request from controller pm. Reserved after r5p6 (version 50600)

PCIE_CLIENT_GENERAL_DEBUG_CON

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	sd_hold_ltssm app_ras_des_sd_hold_ltssm Hold and release LTSSM. For as long as this signal is '1', the controller stays in the current LTSSM. 1'b0: Release LTSSM 1'b1: Hold LTSSM
5	RW	0x0	dbg_pba MSIX PBA RAM Debug Mode. Use this input to activate the debug mode and allow direct read/write access to the PBA. You can also use the MSIX_RAM_CTRL_DBG_PBA field in MSIX_RAM_CTRL_OFF to activate debug mode. Debug mode turns off the PF/VF/Offset-based addressing into the RAM and maps the entire array linearly from the base address of the BAR (indicated by the BIR) in function 0. When you assert dbg_table and dbg_pba simultaneously, you can access the traffic class (TC) information bits. For more information, see the Interrupts section in the "Controller Operations" chapter of the Databook.
4	RW	0x0	dbg_table MSIX Table RAM Debug Mode. Use this input to activate the debug mode and allow direct read/write access to the Table. You can also use the MSIX_RAM_CTRL_DBG_TABLE field in MSIX_RAM_CTRL_OFF to activate debug mode. Debug mode turns off the PF/VF/Offset-based addressing into the RAM and maps the entire table linearly from the base address of the BAR (indicated by the BIR) in function 0. When you assert dbg_table and dbg_pba simultaneously, you can access the traffic class (TC) information bits. For more information, see the Interrupts section in the "Controller Operations" chapter of the Databook.
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	diag_ctrl_bus Diagnostic Control Bus 1. x01: Insert LCRC error by inverting the LSB of LCRC 2. x10: Insert ECRC error by inverting the LSB of ECRC 2.1 The rising edge of these two signals ([1:0]) enable the controller to assert an LCRC or ECRC to the packet that it currently being transferred. 2.2 When LCRC or ECRC error packets are transmitted by the controller, the controller asserts diag_status_bus[lcrc_err_asserted] or diag_status_bus[ecrc_err_asserted] to report that the requested action has been completed. This handshake between control and status allows your application to control a specific packet being injected with an CRC or ECRC error. 2.3 The LCRC and ECRC errors are generated by simply inverting the last bit of the LCRC or ECRC value. 3. 1xx: Select Fast Link Mode. 3.1 Sets all internal LTSSM millisecond timers to Fast Mode for speeding up simulation purposes. Forces the LTSSM training (link initialization) to use shorter timeouts and to link up faster. 3.2 The default scaling factor is 1024 for all internal timers. The default scaling factor can be changed using the DEFAULT_FAST_LINK_SCALING_FACTOR parameter or through the FAST_LINK_SCALING_FACTOR field in the TIMER_CTRL_MAX_FUNC_NUM_OFF register. 3.3 Fast Link Mode can also be activated by setting the FAST_LINK_MODE field in the PORT_LINK_CTRL_OFF register. 3.4 For more information, see the "Fast Link Simulation Mode" section in the "Integrating the Controller with the PHY or Application RTL or Verification IP" chapter of the User Guide.

PCIE_CLIENT_GENERAL_DEBUG_INFO

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	smlh_ltssm_state Current state of the LTSSM.
9	RO	0x0	reserved
8	RO	0x0	radm_q_not_empty Level indicating that the receive queues contain TLP header/data. 1'b0: Receive queues do not contain TLP header/data 1'b1: Receive queues contain TLP header/data
7	RO	0x0	radm_xfer_pending Receive request pending status. Indicates Receive TLP requests are pending, that is, requests sent to the RTRGT1 or RTRGT0 interfaces are awaiting a response from your application. For debugging purposes. 1'b0: Receive TLP requests are not pending 1'b1: Receive TLP requests are pending
6	RO	0x0	edma_xfer_pending eDMA transfer pending status. Indicates eDMA Write or Read Channel transfers are pending, that is, DMA Write or Read Channels have not finished transferring data. For debugging purposes. 1'b0: eDMA DBI transfer not pending 1'b1: eDMA transfer pending

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Bit	Attr	Reset Value	Description
5	RO	0x0	brdg_dbi_xfer_pending AXI Slave DBI transfer pending status. Indicates AXI DBI Slave Read or Write transfers are pending, that is, AXI Slave transfers are awaiting a response from the controller. For debugging purposes. 1'b0: AXI Slave DBI transfer not pending 1'b1: AXI Slave DBI transfer pending
4	RO	0x0	brdg_slv_xfer_pending AXI Slave non-DBI transfer pending status. Indicates AXI non-DBI Slave Read or Write transfers are pending, that is, AXI Slave transfers are awaiting a response from the controller. For debugging purposes. 1'b0: AXI Slave non-DBI transfer not pending 1'b1: AXI Slave non-DBI transfer pending
3	RO	0x0	reserved
2	RO	0x0	radm_idle RADM activity status signal. The controller creates the en_radm_clk_g output by gating this signal with the output of the RADM_CLK_GATING_EN field in the CLOCK_GATING_CTRL_OFF register. For debug purposes only. 1'b0: RADM is not idle in status 1'b1: RADM is in idle status
1	RO	0x0	rdlh_link_up Data link layer up/down indicator: This status from the flow control initialization state machine indicates that flow control has been initiated and the Data link layer is ready to transmit and receive packets. For multi-VC designs, this signal indicates status for VC0 only. 1'b0: Data link layer down 1'b1: Data link layer up
0	RO	0x0	smlh_link_up PHY Link up/down indicator. 1'b0: PHY link is down 1'b1: PHY link is up

PCIE_CLIENT_SLC_DEBUG_INFO_CMN

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	bus_select Select the 16bit of total 78 bit of common silicon debug information: 3'b000: Select bit 15 to 0 3'b001: Select bit 31 to 16 3'b010: Select bit 47 to 32 3'b011: Select bit 63 to 48 3'b100: Select bit 79 to 64 Other: Reserved
27:16	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	cdm_ras_des_sd_info_common Common debug signal bus that is used in RAS D.E.S. silicon debug Bit [78]: init_eq_pending_g4: Level: Equalization sequence Gen5 Bit [77:75]: l1sub_state: Level: L1 sub state Bit [74]: init_eq_pending_g4: Level: Equalization sequence Gen4 Bit [73]: init_eq_pending: Level: Equalization sequence Gen3 Bit [72:61]: xdlh_curnt_seqnum [11:0]: Level: Tx TLP SEQ# Bit [60:49]: rdlh_curnt_rx_ack_seqnum[11:0]: Level: Rx ACK SEQ# Bit [48]: rdlh_vc0_initfc2_status: Level: Init-FC Flag2 VC0 Bit [47]: rdlh_vc0_initfc1_status: Level: Init-FC Flag1 VC0 Bit [46:45]: rdlh_dlcntrl_state [1:0]: Level: DLCM Bit [44:37]: latched_ts_nfts[7:0]: Level: Latched NFTS Bit [36:34]: ltssm_powerdown[1:0]: Level: PIPE: Power Down Bit [33:18]: smlh_ltssm_variable [15:0]: Level: LTSSM Variable Bit [17]: pm_pme_resend_flag: Pulse: PME Re-Send flag Bit [16]: smlh_lane_reversed: Level: Lane Reversal Operation Bit [15:9]: rmlh_framing_err_ptr[6:0]: Pulse: 1st Framing Error Pointer Bit [8:5]: pm_slave_state[3:0]: Level: PM Internal State (Slave) Bit [4:0]: pm_master_state[4:0]: Level: PM Internal State (Master)

PCIE_CLIENT_SLC_DEBUG_INFO_LN

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	bus_select Select the 16bit of total 78 bit of Lane N silicon debug information: 3'b000: Select bit 15 to 0 3'b001: Select bit 31 to 16 3'b010: Select bit 47 to 32 3'b011: Select bit 63 to 48 3'b100: Select bit 79 to 64 Others: Reserved
27:24	RW	0x0	lane_sel cdm_ras_des_sd_info_li source selects 4'h0: Lane 0 4'h1: Lane 1 4'h2: Lane 2 4'h3: Lane 3
23:16	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	cdm_ras_des_sd_info_li 16 of total 78-bit lane N silicon debug information, selected by bus_select field. [77:76]: eq_convergence_sts [1:0]: Level: Equalization convergence information Gen3 [75]: eqpa_violate_rule_123[2]: Level: Rule C Violation Event Status Gen3 [74]: eqpa_violate_rule_123[1]: Level: Rule B Violation Event Status Gen3 [73]: eqpa_violate_rule_123[0]: Level: Rule A Violation Event Status Gen3 [72]: mac_cdm_ras_des_reject_rtx: Level: Receive Reject Coefficient Event status Gen3 [71:64]: phy_cdm_ras_des_fomfeedback: Level: Current Figure of Merit Gen3 [63:61]: mac_cdm_ras_des_pset_lrx: Level: Current Local Receiver Preset Hint Gen3 [60:55]: mac_cdm_ras_des_coef_ltx[5:0]: Level: Current Local Transmitter Pre Cursor coefficient Gen3 [54:49]: mac_cdm_ras_des_coef_ltx[11:6]: Level: Current Local Transmitter Cursor coefficient Gen3 [48:43]: mac_cdm_ras_des_coef_ltx[17:12]: Level: Current Local Transmitter Post Cursor coefficient Gen3 [42:37]: mac_cdm_ras_des_coef_rtx[5:0]: Level: Current Remote Transmitter Pre Cursor coefficient Gen3 [36:31]: mac_cdm_ras_des_coef_rtx[11:6]: Level: Current Remote Transmitter Cursor coefficient Gen3 [30:25]: mac_cdm_ras_des_coef_rtx[17:12]: Level: Current Remote Transmitter Post Cursor coefficient Gen3 [24:19]: mac_cdm_ras_des_lf: Level: Remote Device LF Gen3 [18:13]: mac_cdm_ras_des_fs: Level: Remote Device FS Gen3 [12:5]: rmlh_deskew_fifo_ptr: Level: Deskew Pointer [4]: mac_phy_rxpolarity: Level: PIPE: RxPolarity [3]: latched_rxdetected: Level: PIPE: Detect Lane [2]: phy_mac_rxvalid_rxburst: Level: PIPE: RxValid/RxBurst [1]: phy_mac_rxelec_rxh8exit: Level: PIPE: RxElecIdle/RxHibern8ExitType1 [0]: mac_phy_txelec_txburst: Level: PIPE: TxElecIdle/TxBurst

PCIE_CLIENT_SLC_DEBUG_INFO_V0

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	bus_select Select the 16bit of total 240 bit of virtual channel 0 silicon debug information: 4'd0: Select bit 15 to 0 4'd1: Select bit 31 to 16 ... 4'd14: Select bit 239 to bit 224 Other: Reserved
27:16	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	cdm_ras_des_sd_info_vi 16 of total 240-bit l1 silicon debug information, selected by bus_select field. [239:228]: rtlh_fc_allctd_cpld: Level: Credit Allocated (CD) [227:220]: rtlh_fc_allctd_cplh: Level: Credit Allocated (CH) [219:208]: rtlh_fc_allctd_npd: Level: Credit Allocated (ND) [207:200]: rtlh_fc_allctd_nph: Level: Credit Allocated (NH) [199:188]: rtlh_fc_allctd_pd: Level: Credit Allocated (PD) [187:180]: rtlh_fc_allctd_ph: Level: Credit Allocated (PH) [179:168]: rtlh_fc_rcvd_cpld: Level: Credit Received (CD) [167:160]: rtlh_fc_rcvd_cplh: Level: Credit Received (CH) [159:148]: rtlh_fc_rcvd_npd: Level: Credit Received (ND) [147:140]: rtlh_fc_rcvd_nph: Level: Credit Received (NH) [139:128]: rtlh_fc_rcvd_pd: Level: Credit Received (PD) [127:120]: rtlh_fc_rcvd_ph: Level: Credit Received (PH) [119:108]: xadm_fc_limit_cpld: Level: Credit Limit (CD) [107:100]: xadm_fc_limit_cplh: Level: Credit Limit (CH) [99:88]: xadm_fc_limit_npd: Level: Credit Limit (ND) [87:80]: xadm_fc_limit_nph: Level: Credit Limit (NH) [79:68]: xadm_fc_limit_pd: Level: Credit Limit (PD) [67:60]: xadm_fc_limit_ph: Level: Credit Limit (PH) [59:48]: xadm_fc_cnsmd_cpld: Level: Credit Consumed (CD) [47:40]: xadm_fc_cnsmd_cplh: Level: Credit Consumed (CH) [39:28]: xadm_fc_cnsmd_npd: Level: Credit Consumed (ND) [27:20]: xadm_fc_cnsmd_nph: Level: Credit Consumed (NH) [19:8]: xadm_fc_cnsmd_pd: Level: Credit Consumed (PD) [7:0]: xadm_fc_cnsmd_ph: Level: Credit Consumed (PH)

PCIE_CLIENT_DIAG_STATUS_BUS_SEL

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	diag_bus_sel Select the 32bit of total 1024 bit of diag_status_bus that present on register DIAG_STATUS_BUS_INFO. 5'd0: bit 31 to 0 5'd1: bit 63 to 32 ... 5'd31: bit 1023 to 992

PCIE_CLIENT_DIAG_STATUS_BUS_INFO

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	diag_status_bus 32 bit of total 1024-bit width diag_status_bus. Selected by DIAG_STATUS_BUS_SEL register. Contains all the important status signals from each controller module. Debug only.

PCIE_CLIENT_CDM_RASDES_EC_INFO_CON

Address: **Operational Base** + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	cdm_rasdes_ec_info_lane_sel cdm_ras_des_ec_info_li source selects 4'h0: Lane 0 4'h1: Lane 1 4'h2: Lane 2 4'h3: Lane 3
3:0	RW	0x0	cdm_rasdes_ec_info_con Select the 32bit rasdes_ec_info_cmn 4'd0: Select bit 31 to 0 4'd1: Select bit 63 to 32 ..... Others: Reserved

PCIE_CLIENT_CDM_RASDES_EC_INFO_CMN

Address: **Operational Base** + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cdm_ras_des_ec_info_common Common event signal bus that is used in RAS D.E.S. event counters

PCIE_CLIENT_CDM_RASDES_EC_INFO_LN

Address: **Operational Base** + offset (0x0148)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RO	0x0000	cdm_ras_des_ec_info_li Lanei event signal bus that is used in RAS D.E.S. event counters.

PCIE_CLIENT_CDM_RASDES_TBA_CON

Address: **Operational Base** + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x0	app_ras_des_tba_ctrl Controls the start/end of time-based analysis. You must only set the pins to the required value for the duration of one clock cycle. This signal must be 2'b00 while the TIMER_START field in TIME_BASED_ANALYSIS_CONTROL_REG register is controlled by the DBI interface or the accesses from the wire side. 2'b00: No action 2'b01: Start 2'b10: End. This setting is only used when the TIME_BASED_DURATION_SELECT field of TIME_BASED_ANALYSIS_CONTROL_REG is set to "manual control". 2'b11: Reserved These pins also set the contents of the TIMER_START field in TIME_BASED_ANALYSIS_CONTROL_REG register.

PCIE_CLIENT_CDM_RASDES_TBA_INFO_CMN

Address: **Operational Base** + offset (0x0154)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6:0	RW	0x00	cdm_ras_des_tba_info_common Common event signal status bus used in RAS D.E.S. time-based analysis. Indicates the internal signals that are used in the time-based analysis. The results are in TIME_BASED_ANALYSIS_DATA_REG. Each bit indicates the state that the controller stays in. All signals are level sensitive unless otherwise indicated. [6]: smlh_link_in_training: Config/Recovery [5]: pm_in_l12: L1.2 [4]: pm_in_l11: L1.1 [3]: smlh_in_l1: L1 [2]: smlh_in_l0: L0 [1]: smlh_in_rl0s: Rx L0s [0]: smlh_in_l0s: Tx L0s

PCIE_CLIENT_HOT_RESET_CTRL

Address: **Operational Base** + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	app_ltssm_enable_enhance Set "1" to enable ltssm_enbale enhance mode. In this mode, the host-reset and link-down reset can be optionaly delayed. Available after version 50600.
3	RW	0x0	app_dly2_done Set "1" to end the delaying of the link training after Hot Reset. This bit is self-cleared. Available after version 50600.
2	RW	0x0	app_dly1_done Set "1" to end the delaying of the controller Hot Reset. This bit is self-cleared. Available after version 50600.
1	RW	0x0	app_dly2_en Set "1" to enable delaying the link training after Hot Reset Available after version 50600.
0	RW	0x0	app_dly1_en Set "1" to enable delaying the controller Hot Reset Available after version 50600.

PCIE_CLIENT_INTR_EN_MSG_RX

Address: **Operational Base** + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x1	obff_cpu_active_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

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Bit	Attr	Reset Value	Description
13	RW	0x1	obff_obff_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
12	RW	0x1	obff_idle_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
11	RO	0x0	reserved
10	RW	0x1	pm_turnoff_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
9	RW	0x1	pm_to_ack_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
8	RW	0x1	pm_pme_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
7:6	RO	0x0	reserved
5	RW	0x1	cfg_pme_msi_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
4	RW	0x1	cfg_pme_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
3	RO	0x0	reserved
2	RW	0x1	ltr_msg_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
1	RW	0x1	unlock_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
0	RW	0x1	ven_msg_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

PCIE_CLIENT_INTR_EN_LEGACY

Address: **Operational Base** + offset (0x0194)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	tx_intd_int_en Reserved
6	RW	0x1	tx_intc_int_en Reserved
5	RW	0x1	tx_intb_int_en Reserved
4	RW	0x1	tx_inta_int_en Reserved
3	RW	0x1	rx_intd_int_en Reserved
2	RW	0x1	rx_intc_int_en Reserved
1	RW	0x1	rx_intb_int_en Reserved
0	RW	0x1	rx_inta_int_en Reserved

PCIE_CLIENT_INTR_EN_ERR

Address: **Operational Base** + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x1	radm_qoverflow_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
11	RO	0x0	reserved
10	RW	0x1	f_err_rx_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
9	RW	0x1	nf_err_rx_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
8	RW	0x1	cor_err_rx_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x1	f_err_sent_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
5	RW	0x1	nf_err_sent_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
4	RW	0x1	cor_err_sent_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
3	RW	0x1	tx_cpl_timeout_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
2	RW	0x1	rx_cpl_timeout_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
1	RW	0x1	aer_rc_err_msi_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
0	RW	0x1	aer_rc_err_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

PCIE_CLIENT_INTR_EN_MISC

Address: **Operational Base** + offset (0x019C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	ep_elbi_app_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
14	RW	0x1	link_eq_req_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

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Bit	Attr	Reset Value	Description
13	RW	0x1	rbar_update_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
12	RW	0x1	dpa_sub_upd_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
11	RW	0x1	edma_rd_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
10	RW	0x1	edma_wr_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
9	RW	0x1	bw_mgt_msi_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
8	RW	0x1	bw_mgt_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
7	RW	0x1	link_auto_bw_msi_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
6	RW	0x1	link_auto_bw_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
5	RW	0x1	hp_msi_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
4	RW	0x1	hp_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
3	RW	0x1	hp_pme_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

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Bit	Attr	Reset Value	Description
2	RW	0x1	link_req_rst_not_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
1	RW	0x1	dll_link_up_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
0	RW	0x1	phy_link_up_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

PCIE_CLIENT_INTR_EN_PMC

Address: **Operational Base** + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x1	pm_dstate_update_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
7	RW	0x1	linkst_out_l0s_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
6	RW	0x1	linkst_out_l2_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
5	RW	0x1	linkst_out_l1_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
4	RW	0x1	linkst_out_l1sub_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
3	RW	0x1	linkst_in_l0s_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

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Bit	Attr	Reset Value	Description
2	RW	0x1	linkst_in_l2_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
1	RW	0x1	linkst_in_l1_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
0	RW	0x1	linkst_in_l1sub_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

PCIE_CLIENT_MSI_INT_RX_VEC

Address: **Operational Base** + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	msi_ctrl_int_vec DSP AXI MSI Interrupt Vector. Asserted when an MSI interrupt is pending. De-asserted when there is no MSI interrupt pending

PCIE_CLIENT_AXI_MSTR_MISC_CON

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	mstr_rmisc_ep AXI Master Read Response Transaction Associated Misc Information. This is a signal that the application can optionally use. It is not part of standard AXI interface. [1:0]: Reserved [2]: Reserved [6:3]: Reserved [7]: TLP's EP bit [12:8]: Reserved
3:2	RW	0x0	mstr_rmisc_info_cpl_stat AXI Master Read Response selection bus. This bus controls the response sent on the PCIe wire in the case of successful read requests. The controller always sends a CA (Completer Abort) response when it receives SLVERR/DECERR. 2'b00: SC (Successful Completion) 2'b01: CA (Completer Abort) 2'b10: UR (Unsupported Request) 2'b11: SC (Successful Completion) Your application must drive the same value on mstr_rmisc_info_cpl_stat throughout the complete response. For a multi-beat response, when you set mstr_rmisc_info_cpl_stat to UR: 1. If the first beat of the response produces a slave error/decode error, the controller sends a CPL with status as CA.

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Bit	Attr	Reset Value	Description
			2. If any beat (other than the first beat) of the response has a slave/decode error, the controller sends a CPL with status as UR.
1:0	RW	0x0	mstr_bmisc_info_cpl_stat AXI Master Write Response selection bus. This controls the response to be sent on the wire in the case of successful write requests. The controller always sends a CA (Completer Abort) response when it receives SLVERR/DECERR. 2'b00: SC (Successful Completion) 2'b01: CA (Completer Abort) 2'b10: UR (Unsupported Request) 2'b11: SC (Successful Completion) Your application must drive the same value on mstr_bmisc_info_cpl_stat throughout the complete response. For a multi-beat response, when you set mstr_bmisc_info_cpl_stat to UR: 1. If the first beat of the response produces a slave error/decode error, the controller sends a CPL with status as CA. 2. If any beat (other than the first beat) of the response has a slave/decode error, the controller sends a CPL with status as UR.

PCIE_CLIENT_AXI_SLV_ATU_BYPASS

Address: **Operational Base** + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	slv_armisc_info_atu_bypass AXI Slave Read Request Internal ATU Bypass. When set it indicates that this request should not be processed by the internal address translation unit. 1'b0: Not bypass 1'b1: AXI slave read address ATU bypass
0	RW	0x0	slv_awmisc_info_atu_bypass AXI Slave Write Request Internal ATU Bypass. When set it indicates that this request should not be processed by the internal address translation unit. 1'b0: Not bypass 1'b1: AXI slave write address ATU bypass

PCIE_CLIENT_AXI_SLV_AWMISC_HDR

Address: **Operational Base** + offset (0x0208)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	slv_awmisc_info AXI Slave Write Transaction Associated Misc Information. This is a signal that the application can optionally use. It is not part of the standard AXI interface. For more information, see 'AXI Slave Interface Sideband Signals'. You must set all reserved bits to '0'. [4:0]: TLP's TYPE. [5]: Serialize NP Requests [6]: TLP's EP bit [7]: Reserved [8]: TLP's NS bit [9]: TLP's RO bit

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Bit	Attr	Reset Value	Description
			[12:10]: TLP's TC bits [20:13]: TLP's MSG code [21]: AXI transaction is a DBI access. This is for SHARED DBI mode only. [24:22]: TLP's Function number. Function numbering starts at '0'. Not used when CX_SRIOV_ENABLE =1 or CX_ARI_ENABLE =1. For more information, see slv_awmisc_info_func_num. This field is only present when multifunction support (CX_NFUNC > 1) is enabled. For a configuration transfer, you must drive the bus number, device number, function number, and register number onto the address bus as follows: bus_number = addr[31:24] dev_number = addr[23:19] func_number = addr[18:16] ext_reg_number = addr[11:8] reg_number = addr[7:2]

PCIE_CLIENT_AXI_SLV_AWMISC_HDR3

Address: **Operational Base** + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	slv_awmisc_info_hdr_3dw AXI Slave 3rd and 4th header DWs. The application drives this bus with the 3rd and 4th Header DWs it intends to send on a PCIe Msg/MsgD. Note: The data is in big endian format, that is, slv_awmisc_info_hdr_34dw[7:0] contains byte 15 of header DW.

PCIE_CLIENT_AXI_SLV_AWMISC_HDR4

Address: **Operational Base** + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	slv_awmisc_info_hdr_4dw AXI Slave 3rd and 4th header DWs. The application drives this bus with the 3rd and 4th Header DWs it intends to send on a PCIe Msg/MsgD. Note: The data is in big endian format, that is, slv_awmisc_info_hdr_34dw[7:0] contains byte 15 of header DW.

PCIE_CLIENT_AXI_SLV_AWMISC_TAG

Address: **Operational Base** + offset (0x0214)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	slv_awmisc_info_p_tag AXI Slave Write Request Tag. Sets the TAG number for output posted requests. It is expected that your application normally sets this to '0' except when generating ATS invalidate requests.

PCIE_CLIENT_AXI_SLV_MISC_INFO

Address: **Operational Base** + offset (0x0218)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22	RW	0x0	slv_wmisc_info_ep AXI Slave Write Data transaction related misc information. This is an optional signal that your application can use to poison write requests. When asserted, the controller sets the Poisoned TLP (EP) bit in the TLP header of the current and subsequent Write Data transactions. It is not a part of the standard AXI interface.
21:0	RW	0x000000	slv_armisc_info AXI Slave Read Transaction Associated Miscellaneous Information. This is a signal that the application can optionally use. It is not part of the standard AXI interface. [4:0]: TLP's TYPE [5]: Serialize NP Requests [6]: TLP's EP bit [7]: Reserved [8]: TLP's NS bit [9]: TLP's RO bit [12:10]: TLP's TC bits [20:13]: TLP's MSG code [21]: AXI transaction is a DBI access. This is for SHARED DBI mode only. [24:22]: TLP's function number. Function numbering starts at '0'. Not used when CX_SRIOV_ENABLE =1 or CX_ARI_ENABLE =1. For more information, see slv_armisc_info_func_num. This field is only present when multifunction support (CX_NFUNC > 1) is enabled. For a configuration transfer, you must drive the bus number, device number, function number, and register number onto the address bus as follows: bus_number = addr[31:24] dev_number = addr[23:19] func_number = addr[18:16] ext_reg_number = addr[11:8] reg_number = addr[7:2]

PCIE_CLIENT_AXI_SLV_AW_TLP_PRFX

Address: **Operational Base** + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	slv_awmisc_info_tlpprfx AXI Slave Write Request TLP Prefixes. The field [31:0] represents the first prefix to be transmitted. The optional TLP prefixes are implemented as little endian. Using the example of a controller with just one prefix (CX_NPRFX =1), this means that slv_awmisc_info_tlpprfx[31:0] has prefix byte #0 in the lower byte position of the dword slv_awmisc_info_tlpprfx[31:0]. That is, FMT =bits 7:5, and Type =bits 4:0. Your application is responsible for passing Local and End-End prefixes in the correct order for transmission. Local prefixes must precede End-End prefixes. Any parity bits that your application appends (when RAS data protection is enabled) to the most significant bits are routed but not checked by the controller. The controller passes along and appends to the prefix, any protection codes it receives, when datapath protection is enabled. Available after version 50610.

PCIE_CLIENT_AXI_SLV_AR_TLP_PRFX

Address: **Operational Base** + offset (0x0224)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	slv_armisc_info_tlpprfx AXI Slave Read Request TLP Prefixes. The field [31:0] represents the first prefix to be transmitted. The optional TLP prefixes are implemented as little endian. Using the example of a controller with just one prefix (CX_NPRFX =1), this means that slv_armisc_info_tlpprfx[31:0] has prefix byte #0 in the lower byte position of the dword slv_armisc_info_tlpprfx[31:0]. That is, FMT =bits 7:5, and Type =bits 4:0. Your application is responsible for passing Local and End-End prefixes in the correct order for transmission. Local prefixes must precede End-End prefixes. Any parity bits that your application appends (when RAS data protection is enabled) to the most significant bits are routed but not checked by the controller. The controller passes along and appends to the prefix, any protection codes it receives, when datapath protection is enabled. Available after version 50610.

PCIE_CLIENT_DBI_MISC_CON

Address: **Operational Base** + offset (0x0270)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	dbi_msix_table_access_ctrl Control the bit 30 of the DBI awaddr. Set 1 to enable access, and shoud clear to 0 when access done.

PCIE_CLIENT_PORT_BDF

Address: **Operational Base** + offset (0x0274)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	app_bus_dev Bus number. Your application must drive this signal to set the bus number in the Requester ID for RC port and Switch DSP port.
7:3	RW	0x00	app_dev_num Device number. Your application must drive this signal to set the device number in the Requester ID for RC port and Switch DSP port.
2:0	RO	0x0	reserved

PCIE_CLIENT_LTSSM_STATUS

Address: **Operational Base** + offset (0x0300)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:20	RO	0x0	pm_current_data_rate The current link operating rate. 3'b000: 2.5 GT/s signalling rate 3'b001: 5.0 GT/s signalling rate 3'b010: 8.0 GT/s signalling rate for PCIe mode or ESM data rate0 for ESM mode 3'b011: 16.0 GT/s signalling rate for PCIe mode or ESM data rate1 for ESM mode 3'b100: 32.0 GT/s signalling rate
19:18	RO	0x0	reserved
17	RO	0x0	rdlh_link_up Data link layer up/down indicator: This status from the flow control initialization state machine indicates that flow control has been initiated and the Data link layer is ready to transmit and receive packets. For multi-VC designs, this signal indicates status for VC0 only. 1'b0: Link is down 1'b1: Link is up
16	RO	0x0	smlh_link_up PHY Link up/down indicator: 1'b0: Link is down 1'b1: Link is up
15:11	RO	0x00	reserved
10:8	RO	0x0	l1sub_state Power management L1 sub-states FSM state.
7:6	RO	0x0	reserved
5:0	RO	0x00	smlh_ltssm_state smlh_ltssm_state Current state of the LTSSM. Encoding is defined as follows: 6'h00: S_DETECT_QUIET 6'h01: S_DETECT_ACT 6'h02: S_POLL_ACTIVE 6'h03: S_POLL_COMPLIANCE 6'h04: S_POLL_CONFIG 6'h05: S_PRE_DETECT_QUIET 6'h06: S_DETECT_WAIT 6'h07: S_CFG_LINKWD_START 6'h08: S_CFG_LINKWD_ACEPT 6'h09: S_CFG_LANENUM_WAI 6'h0A: S_CFG_LANENUM_ACEPT 6'h0B: S_CFG_COMPLETE 6'h0C: S_CFG_IDLE 6'h0D: S_RCVRY_LOCK 6'h0E: S_RCVRY_SPEED 6'h0F: S_RCVRY_RCVRCFG 6'h10: S_RCVRY_IDLE 6'h11: S_L0 6'h12: S_L0S 6'h13: S_L123_SEND_EIDLE 6'h14: S_L1_IDLE 6'h15: S_L2_IDLE 6'h16: S_L2_WAKE 6'h17: S_DISABLED_ENTRY 6'h18: S_DISABLED_IDLE 6'h19: S_DISABLED 6'h1A: S_LPBK_ENTRY

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Bit	Attr	Reset Value	Description
			6'h1B: S_LPBK_ACTIVE 6'h1C: S_LPBK_EXIT 6'h1D: S_LPBK_EXIT_TIMEOUT 6'h1E: S_HOT_RESET_ENTRY 6'h1F: S_HOT_RESET 6'h20: S_RCVRY_EQ0 6'h21: S_RCVRY_EQ1 6'h22: S_RCVRY_EQ2 6'h23: S_RCVRY_EQ3

PCIE_CLIENT_DBG_FIFO_MODE_CON

Address: **Operational Base** + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x0	dbg_fifo_hit_mode Hit mode control. Bit0 enable pattern 0 match mode Bit1 enable pattern 1 match mode Bit2 enable pattern 0 transition mode
7:6	RO	0x0	reserved
5:4	RW	0x0	dbg_fifo_mode Debug FIFO store debug status mode 2'b00: Default 2'b01: If hit pattern, disable FIFO write 2'b10: If FIFO full, disable FIFO write 2'b11: Reserved
3	RO	0x0	reserved
2	RW	0x0	dbg_fifo_l1sub_en Debug FIFO enable for L1SS 1'b0: Disable 1'b1: Enable
1	RW	0x0	dbg_fifo_ltssm_en Debug FIFO enable for LTSSM 1'b0: Disable 1'b1: Enable
0	RW	0x0	dbg_fifo_en Debug FIFO enable 1'b0: Disable 1'b1: Enable

PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA0

Address: **Operational Base** + offset (0x0320)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	ptn_hit_data0 Hit mode data pattern 0

PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA1

Address: **Operational Base** + offset (0x0324)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	ptn_hit_data1 Hit mode data pattern 1

PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA0

Address: **Operational Base** + offset (0x0328)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	trn_hit_data0 Transition state data 0

PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA1

Address: **Operational Base** + offset (0x032C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	trn_hit_data1 Transition state data 1

PCIE_CLIENT_DBG_FIFO_STATUS

Address: **Operational Base** + offset (0x0350)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RO	0x0	dbg_pm_current_data_rate The current link operating rate. 3'b000: 2.5 GT/s signalling rate 3'b001: 5.0 GT/s signalling rate 3'b010: 8.0 GT/s signalling rate for PCIe mode or ESM data rate0 for ESM mode 3'b011: 16.0 GT/s signalling rate for PCIe mode or ESM data rate1 for ESM mode 3'b100: 32.0 GT/s signalling rate Available after version 50610.
19	RO	0x0	reserved
18:16	RO	0x0	dbg_space2empty Debug FIFO space to empty.
15	RO	0x0	reserved
14	RO	0x0	dbg_fifo_wr_overfollow Debug FIFO overfollow flag 1'b0: Not overfollow 1'b1: Overfollow
13	RO	0x0	dbg_fifo_full Debug FIFO full flag 1'b0: Not full 1'b1: Full
12	RO	0x0	dgb_fifo_empty Debug FIFO empty flag 1'b0: Not empty 1'b1: Empty
11	RO	0x0	reserved
10:8	RO	0x0	dbg_fifo_l1sub_state Power management L1 sub-states FSM state.
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RO	0x00	dbg_fifo_ltssm_state smlh_ltssm_state Current state of the LTSSM. Encoding is defined as follows: 6'h00: S_DETECT_QUIET 6'h01: S_DETECT_ACT 6'h02: S_POLL_ACTIVE 6'h03: S_POLL_COMPLIANCE 6'h04: S_POLL_CONFIG 6'h05: S_PRE_DETECT_QUIET 6'h06: S_DETECT_WAIT 6'h07: S_CFG_LINKWD_START 6'h08: S_CFG_LINKWD_ACEPT 6'h09: S_CFG_LANENUM_WAI 6'h0A: S_CFG_LANENUM_ACEPT 6'h0B: S_CFG_COMPLETE 6'h0C: S_CFG_IDLE 6'h0D: S_RCVRY_LOCK 6'h0E: S_RCVRY_SPEED 6'h0F: S_RCVRY_RCVRCFG 6'h10: S_RCVRY_IDLE 6'h11: S_L0 6'h12: S_L0S 6'h13: S_L123_SEND_EIDLE 6'h14: S_L1_IDLE 6'h15: S_L2_IDLE 6'h16: S_L2_WAKE 6'h17: S_DISABLED_ENTRY 6'h18: S_DISABLED_IDLE 6'h19: S_DISABLED 6'h1A: S_LPBK_ENTRY 6'h1B: S_LPBK_ACTIVE 6'h1C: S_LPBK_EXIT 6'h1D: S_LPBK_EXIT_TIMEOUT 6'h1E: S_HOT_RESET_ENTRY 6'h1F: S_HOT_RESET 6'h20: S_RCVRY_EQ0 6'h21: S_RCVRY_EQ1 6'h22: S_RCVRY_EQ2 6'h23: S_RCVRY_EQ3

PCIE_CLIENT_CFG_ERR_STATUS

Address: **Operational Base** + offset (0x0354)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	cfg_uncor_internal_err_sts Indication from the controller that the controller has detected an Uncorrectable Internal Error.
11	RO	0x0	cfg_rcvr_overflow_err_sts Indication from the controller that the controller has detected an Receiver Overflow Error.
10	RO	0x0	cfg_fc_protocol_err_sts Indication from the controller that the controller has detected an Flow Control Protocol Error.
9	RO	0x0	cfg_mlf_tlp_err_sts Indication from the controller that the controller detected an Malformed TLP Error.

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Bit	Attr	Reset Value	Description
8	RO	0x0	cfg_surprise_down_err_sts Indication from the controller that the controller detected an Surprise Down Error.
7	RO	0x0	cfg_dl_protocol_err_sts Indication from the controller that the controller detected an Data Link Protocol Error.
6	RO	0x0	cfg_ecrc_err_sts Indication from the controller that the controller detected an ECRC Error.
5	RO	0x0	cfg_corrected_internal_err_sts Indication from the controller that the controller detected an Corrected Internal Error.
4	RO	0x0	cfg_replay_number_rollover_err_sts Indication from the controller that the controller detected an REPLAY_NUMBER Rollover Error.
3	RO	0x0	cfg_replay_timer_timeout_err_sts Indication from the controller that the controller detected an Replay Timer Timeout.
2	RO	0x0	cfg_bad_dllp_err_sts Indication from the controller that the controller detected an Bad DLLP Error.
1	RO	0x0	cfg_bad_tlp_err_sts Indication from the controller that the controller detected an Bad TLP Error.
0	RO	0x0	cfg_rcvr_err_sts Indication from the controller that the controller detected an Receiver Error.

PCIE_CLIENT_TLP_PRFX_LOG0

Address: **Operational Base** + offset (0x0380)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_tlp_prfx_log_0 End-End TLP prefixes of the TLP that contained an error. Valid when 1. app_hdr_valid is asserted. The header of the TLP that contained the error indicated on app_err_bus. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register. Available after version 50610.

PCIE_CLIENT_TLP_PRFX_LOG1

Address: **Operational Base** + offset (0x0384)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_tlp_prfx_log_1 End-End TLP prefixes of the TLP that contained an error. Valid when 1. app_hdr_valid is asserted. The header of the TLP that contained the error indicated on app_err_bus. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that

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Bit	Attr	Reset Value	Description
			contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register. Available after version 50610.

PCIE_CLIENT_TLP_PRFX_LOG2

Address: **Operational Base** + offset (0x0388)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_tlp_prfx_log_2 End-End TLP prefixes of the TLP that contained an error. Valid when 1. app_hdr_valid is asserted. The header of the TLP that contained the error indicated on app_err_bus. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register. Available after version 50610.

PCIE_CLIENT_TLP_PRFX_LOG3

Address: **Operational Base** + offset (0x038C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_tlp_prfx_log_3 End-End TLP prefixes of the TLP that contained an error. Valid when 1. app_hdr_valid is asserted. The header of the TLP that contained the error indicated on app_err_bus. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register. Available after version 50610.

PCIE_CLIENT_CLIENT_VER

Address: **Operational Base** + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RO	0x00050611	version Client version ID

14.4.3 Downstream Port Register

14.4.3.1 PCIE_DSP_PF0_TYPE1_HDR Register Description

14.4.3.1.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_TYPE1_HDR_TYPE1_DEV_ID_VEND_ID_REG	0x0000	W	0x35761D87	This register holds the device ID and vendor ID.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_TYPE1_HDR_TYPE1_STATUS_COMMAND_REG	0x0004	W	0x00100000	This register provides the status and controls the behavior of a function.
PCIE_DSP_PF0_TYPE1_HDR_TYPE1_CLASS_CODE_REV_ID_REG	0x0008	W	0x00000001	This register specifies the class code and revision ID of a function.
PCIE_DSP_PF0_TYPE1_HDR_TYPE1_BIST_HDR_TYPE_LAT_CACHE_LINE_SIZE_REG	0x000C	W	0x00010000	This register provides the status and controls BIST. It also holds information regarding the header layout, latency timer, and cache line size.
PCIE_DSP_PF0_TYPE1_HDR_BAR0_REG	0x0010	W	0x00000000	System software must build a consistent address map before booting the machine to an operating system. This means it has to determine how much memory is in the system, and how much address space the Functions in the system require. After determining this information, system software can map the Functions into reasonable locations and proceed with system boot. In order to do this mapping in a device-independent manner, the base registers for this mapping are placed in the predefined header portion of Configuration Space. It is strongly recommended that power-up firmware/software also support the optional Enhanced Configuration Access Mechanism (ECAM).
PCIE_DSP_PF0_TYPE1_HDR_BAR1_REG	0x0014	W	0x00000000	System software must build a consistent address map before booting the machine to an operating system. This means it has to determine how much memory is in the system, and how much address space the Functions in the system require. After determining this information, system software can map the Functions into reasonable locations and proceed with system boot. In order to do this mapping in a device-independent manner, the base registers for this mapping are placed in the predefined header portion of Configuration Space. It is strongly recommended that power-up firmware/software also support the optional Enhanced

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Name	Offset	Size	Reset Value	Description
				Configuration Access Mechanism (ECAM).
PCIE_DSP_PF0_TYPE1_HDR_SEC_LAT_TIMER_SUB_BUS_SEC_BUS_PRI_BUS_REG	0x0018	W	0x00000000	This register holds information regarding secondary latency timer, subordinate bus number, secondary bus number, and primary bus number.
PCIE_DSP_PF0_TYPE1_HDR_SEC_STAT_IO_LIMIT_IO_BASE_REG	0x001C	W	0x00000000	The I/O Limit and I/O Base registers are optional and define an address range that is used by the bridge to determine when to forward I/O transactions from one interface to the other. If a bridge does not implement an I/O address range, then both the I/O Limit and I/O Base registers must be implemented as read-only registers that return zero when read. If a bridge supports an I/O address range, then these registers must be initialized by configuration software so default states are not specified.
PCIE_DSP_PF0_TYPE1_HDR_MEM_LIMIT_MEM_BASE_REG	0x0020	W	0x00000000	The Memory Limit and Memory Base registers define a memory mapped address range which is used by the bridge to determine when to forward memory transactions from one interface to the other. If there is no prefetchable memory space, and there is no memory-mapped space on the secondary side of the bridge, then the bridge will not forward any memory transactions from the primary bus to the secondary bus and will forward all memory transactions from the secondary bus to the primary bus.
PCIE_DSP_PF0_TYPE1_HDR_PREF_MEM_LIMIT_PREF_MEM_BASE_REG	0x0024	W	0x00010001	The Prefetchable Memory Limit and Prefetchable Memory Base registers must indicate that 64-bit addresses are supported.The Prefetchable Memory Limit and Prefetchable Memory Base registers are optional. They define a prefetchable memory address range which is used by the bridge to determine when to forward memory transactions from one interface to the other (see the PCI-to-PCI Bridge Architecture Specification for additional details).

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_TYPE1_HDR_PREF_BASE_UPPER_REG	0x0028	W	0x00000000	The Prefetchable Base Upper 32 Bits register is an optional extension to the Prefetchable Memory Base register.
PCIE_DSP_PF0_TYPE1_HDR_PREF_LIMIT_UPPER_REG	0x002C	W	0x00000000	The Prefetchable Limit Upper 32 Bits register is an optional extension to the Prefetchable Memory Limit register.
PCIE_DSP_PF0_TYPE1_HDR_IO_LIMIT_UPPER_IO_BASE_UPPER_REG	0x0030	W	0x00000000	The I/O Limit Upper 16 Bits and I/O Base Upper 16 Bits registers are optional extensions to the I/O Limit and I/O Base registers.
PCIE_DSP_PF0_TYPE1_HDR_TYPE1_CAP_PTR_REG	0x0034	W	0x00000040	This register is used to point to a linked list of capabilities implemented by a Function.
PCIE_DSP_PF0_TYPE1_HDR_TYPE1_EXP_ROM_BASE_REG	0x0038	W	0x00000000	This register is defined to handle the base address and size information for this expansion ROM. The mask for this ROM BAR exists (if implemented) as a shadow register at this address. The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the second register at this address.
PCIE_DSP_PF0_TYPE1_HDR_BRIDGE_CTRL_INT_PIN_INT_LINE_REG	0x003C	W	0x000001FF	This register provides many of the same controls for the secondary interface that are provided by the Command Register for theprimary interface. This register also identifies the legacy interrupt Message(s) a Function uses and communicates interrupt line routing information.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3.1.2 Detail Registers Description

PCIE_DSP_PF0_TYPE1_HDR_TYPE1_DEV_ID_VEND_ID_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x3576	DEVICE_ID Device ID. The Device ID register identifies the particular Function. This identifier is allocated by the vendor. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:0	RO	0x1d87	VENDOR_ID Vendor ID. The Vendor ID register identifies the manufacturer of the Function. Valid vendor identifiers are allocated by the PCI-SIG to ensure uniqueness. It is not permitted to populate this register with a value of FFFFh, which is an invalid value for Vendor ID. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

PCIE_DSP_PF0_TYPE1_HDR_TYPE1_STATUS_COMMAND_REG

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	DETECTED_PARITY_ERROR Detected Parity Error. The bit is set when the Poisoned TLP is received by a Function's primary side.
30	RW	0x0	SIGNALED_SYS_ERROR Signaled System Error.
29	RW	0x0	RCVD_MASTER_ABORT Received Master Abort. This bit is set when a Requester receives a Completion with Unsupported Request Completion status. The bit is set when the Unsupported Request is received by a Function's primary side.
28	RW	0x0	RCVD_TARGET_ABORT Received Target Abort. This bit is set when a Requester receives a Completion with Completer Abort Completion status. The bit is set when the Completer Abort is received by a Function's primary side.
27	RW	0x0	SIGNALED_TARGET_ABORT Signaled Target Abort. This bit is set when a Function completes a Posted or Non-Posted Request as a Completer Abort error. This applies to a Function when the Completer Abort was generated by its primary side.
26:25	RO	0x0	DEV_SEL_TIMING DEVSEL Timing. This field was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires it to 00b.
24	RW	0x0	MASTER_DPE Master Data Parity Error. This bit is set by a Function if the Parity Error Response bit in the Command register is 1b and either of the following two conditions occurs: - Port receives a Poisoned Completion going downstream - Port transmits a Poisoned Request upstream If the Parity Error Response bit is 0b, this bit is never set.

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Bit	Attr	Reset Value	Description
23	RO	0x0	FAST_B2B_CAP Fast Back-to-Back Transactions Capable. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b.
22	RO	0x0	RSVDP_22 Reserved for future use.
21	RO	0x0	FAST_66MHZ_CAP 66 MHz Capable. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b.
20	RO	0x1	CAP_LIST Capabilities List. Indicates the presence of an Extended Capability list item. Since all PCI Express device Functions are required to implement the PCI Express Capability structure, the controller hardwires this bit to 1b.
19	RO	0x0	INT_STATUS Interrupt Status. INTx emulation interrupts forwarded by Functions from the secondary side are not reflected in this bit. Setting the Interrupt Disable bit has no effect on the state of this bit. For Functions that do not generate INTx interrupts, the controller hardwires this bit to 0b.
18:17	RO	0x0	RSVDP_17 Reserved for future use.
16	RO	0x0	reserved
15:11	RO	0x00	RESERV Reserved.
10	RW	0x0	INT_EN Interrupt Disable. Controls the ability of a Function to generate INTx emulation interrupts. Note: - Any INTx emulation interrupts already asserted by the Function must be deasserted when this bit is set. INTx interrupts use virtual wires that must, if asserted, be deasserted using the appropriate Deassert_INTx message(s) when this bit is set. - Only the INTx virtual wire interrupt(s) associated with the Function(s) for which this bit is set are affected. - For Functions that generate INTx interrupts on their own behalf, this bit is required. This bit has no effect on interrupts forwarded from the secondary side. For Functions that do not generate INTx interrupts on their own behalf this bit is optional. If this bit is not implemented, the controller hardwires it to 0b.
9	RO	0x0	RSVDP_9 Reserved for future use.

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Bit	Attr	Reset Value	Description
8	RW	0x0	SERREN SERR# Enable. Note: - The errors are reported if enabled either through this bit or through the PCI Express specific bits in the Device Control register. - In addition, this bit controls transmission by the primary interface of ERR_NONFATAL and ERR_FATAL error Messages forwarded from the secondary interface. This bit does not affect the transmission of forwarded ERR_COR messages.
7	RO	0x0	IDSEL IDSEL Stepping/Wait Cycle Control. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b.
6	RW	0x0	PERREN Parity Error Response. This bit controls the logging of poisoned TLPs in the Master Data Parity Error bit in the Status register.
5	RO	0x0	VGAPS VGA Palette Snoop. This bit was originally described in the PCI Local Bus Specification and the PCI-to-PCI Bridge Architecture Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b.
4	RO	0x0	MWI_EN Memory Write and Invalidate. This bit was originally described in the PCI Local Bus Specification and the PCI-to-PCI Bridge Architecture Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b. For PCI Express to PCI/PCI-X Bridges, refer to the PCI Express to PCI/PCI-X Bridge Specification for requirements for this register.
3	RO	0x0	SCO Special Cycle Enable. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b.
2	RW	0x0	BME Bus Master Enable. This bit controls forwarding of Memory or I/O requests by a port in the Upstream direction. When this bit is 0b, Memory and I/O Requests received at a Root Port must be handled as Unsupported Requests (UR) For Non-Posted Requests a Completion with UR completion status must be returned. This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O Requests is not controlled by this bit.

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Bit	Attr	Reset Value	Description
1	RW	0x0	MSE Memory Space Enable. This bit controls a Function's response to Memory Space accesses received on its primary side. You cannot write to this register if your configuration has no MEM BARs; that is, the internal signal has_mem_bar =0. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: !has_mem_bar ? RO : RW
0	RW	0x0	IO_EN IO Space Enable. This bit controls a Function's response to I/O Space accesses received on its primary side. You cannot write to this register if your configuration has no IO BARs; that is, the internal signal has_io_bar =0. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: !has_io_bar ? RO : RW

PCIE_DSP_PF0_TYPE1_HDR_TYPE1_CLASS_CODE_REV_ID_REG

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	BASE_CLASS_CODE Base Class Code. A code that broadly classifies the type of operation the Function performs. Encodings for base class, are provided in the PCI Code and ID Assignment Specification. All unspecified encodings are reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
23:16	RO	0x00	SUBCLASS_CODE Sub-Class Code. Specifies a base class sub-class, which identifies more specifically the operation of the Function. Encodings for sub-class are provided in the PCI Code and ID Assignment Specification. All unspecified encodings are reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	PROGRAM_INTERFACE Programming Interface. This field identifies a specific register level programming interface (if any) so that device independent software can interact with the Function. Encodings for interface are provided in the PCI Code and ID Assignment Specification. All unspecified encodings are reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
7:0	RO	0x01	REVISION_ID Revision ID. The value of this field specifies a Function specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. The Revision ID should be viewed as a vendor defined extension to the Device ID. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

PCIE_DSP_PF0_TYPE1_HDR_TYPE1_BIST_HDR_TYPE_LAT_CACHE_LINE_SIZE_REG

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	BIST BIST. This register is used for control and status of BIST. Functions that do not support BIST must hardwire the register to 00h. A Function whose BIST is invoked must not prevent normal operation of the PCI Express Link. Bit descriptions: - [31]: BIST Capable. When set, this bit indicates that the Function supports BIST. When Clear, the Function does not support BIST. - [30]: Start BIST. If BIST Capable is set, set this bit to invoke BIST. The Function resets the bit when BIST is complete. Software is permitted to fail the device if this bit is not Clear (BIST is not complete) 2 seconds after it had been set. Writing this bit to 0b has no effect. The controller hardwires this bit to 0b if BIST Capable is clear. - [29:28]: Reserved. - [27:24]: Completion Code. This field encodes the status of the most recent test. A value of 0000b means that the Function has passed its test. Non-zero values mean the Function failed. Function-specific failure codes can be encoded in the non-zero values. This field's value is only meaningful when BIST Capable is set and Start BIST is Clear. This field must be hardwired to 0000b if BIST Capable is clear.

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Bit	Attr	Reset Value	Description
23	RO	0x0	MULTI_FUNC Multi-Function Device. Except where stated otherwise, it is recommended that this bit be set if there are multiple Functions, and clear if there is only one Function. Note: This register field is sticky.
22:16	RO	0x01	HEADER_TYPE Header Layout. This field identifies the layout of the second part of the predefined header. The controller uses 000 0001b encoding. The encoding 000 0010b is reserved. This encoding was originally described in the PC Card Standard Electrical Specification and is used in previous versions of the programming model. Careful consideration should be given to any attempt to re-purpose it.
15:8	RO	0x00	LATENCY_MASTER_TIMER Latency Timer. This register is also referred to as Primary Latency Timer. The Latency Timer was originally described in the PCI Local Bus Specification and the PCI-to-PCI Bridge Architecture Specification. Its functionality does not apply to PCI Express. The controller hardwires this register to 00h.
7:0	RW	0x00	CACHE_LINE_SIZE Cache Line Size. The Cache Line Size register is programmed by the system firmware or the operating system to system cache line size. However, legacy conventional PCI software may not always be able to program this register correctly especially in the case of Hot-Plug devices. This read-write register is implemented for legacy compatibility purposes but has no effect on any PCI Express device behavior.

PCIE_DSP_PF0_TYPE1_HDR_BAR0_REG

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	BAR0_START BAR0 Base Address. - Memory Space: Base Address. - IO Space: bits[31:2] are used to map the function into IO space/Base. Address. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R(Sticky)/W(Sticky) if enabled else R(Sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
3	RO	0x0	BAR0_PREFETCH BAR0 Prefetchable. - Memory Space: Set to one if data is prefetchable. A Function is permitted to mark a range as prefetchable. If there are no side effects on reads, the function returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors. Bit must me clear otherwise. - IO Space: Not applicable Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky.
2:1	RO	0x0	BAR0_TYPE BAR0 Type. - Memory Space: Base Address registers that map into Memory Space can be 32 bits or 64 bits wide (to support mapping into a 64-bit address space). The encodings defined in Values: apply. - IO Space: Bit 1 is reserved and must return 0b on reads. Bits[31:2] are used to map the function into IO space. The encodings defined in Values: do not apply. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky.
0	RO	0x0	BAR0_MEM_IO BAR0 Memory Space Indicator. This bit is used to determine whether the register maps into Memory or I/O Space. Base Address registers that map to Memory Space must return a 0b. Base Address registers that map to I/O Space must return a 1b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky.

PCIE_DSP_PF0_TYPE1_HDR_BAR1_REG

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	BAR1_START BAR1 Base Address. - Memory Space: Base Address. - IO Space: bits[31:2] are used to map the function into IO space/Base. Address. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R(Sticky)/W(Sticky) if enabled else R(Sticky)

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Bit	Attr	Reset Value	Description
			Note: This register field is sticky.
3	RO	0x0	BAR1_PREFETCH BAR1 Prefetchable. - Memory Space: Set to one if data is prefetchable. A Function is permitted to mark a range as prefetchable. If there are no side effects on reads, the function returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors. Bit must me clear otherwise. - IO Space: Not applicable Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky.
2:1	RO	0x0	BAR1_TYPE BAR1 Type. - Memory Space: Base Address registers that map into Memory Space can be 32 bits or 64 bits wide (to support mapping into a 64-bit address space). The encodings defined in Values: apply. - IO Space: Bit 1 is reserved and must return 0b on reads. Bits[31:2] are used to map the function into IO space. The encodings defined in Values: do not apply. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky.
0	RO	0x0	BAR1_MEM_IO BAR1 Memory Space Indicator. This bit is used to determine whether the register maps into Memory or I/O Space. Base Address registers that map to Memory Space must return a 0b. Base Address registers that map to I/O Space must return a 1b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky.

PCIE_DSP_PF0_TYPE1_HDR_SEC_LAT_TIMER_SUB_BUS_SEC_BUS_PRI_BUS_REG

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	SEC_LAT_TIMER Secondary Latency Timer. This register does not apply to PCI Express. The controller hardwires it to 00h.

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	SUB_BUS Subordinate Bus Number. The Subordinate Bus Number register is used to record the bus number of the highest numbered PCI bus segment which is behind (or subordinate to) the bridge. Configuration software programs the value in this register. The bridge uses this register in conjunction with the Secondary Bus Number register to determine when to respond to and pass on a Type 1 configuration transaction on the primary interface to the secondary interface.
15:8	RW	0x00	SEC_BUS Secondary Bus Number. The Secondary Bus Number register is used to record the bus number of the PCI bus segment to which the secondary interface of the bridge is connected. Configuration software programs the value in this register. The bridge uses this register to determine when to respond to and convert a Type 1 configuration transaction on the primary interface into a Type 0 transaction on the secondary interface.
7:0	RW	0x00	PRIM_BUS Primary Bus Number. This register is not used by PCI Express Functions. It is implemented for compatibility with legacy software.

PCIE_DSP_PF0_TYPE1_HDR_SEC_STAT_IO_LIMIT_IO_BASE_REG

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31	RW	0x0	SEC_STAT_DPE Detected Parity Error. This bit is set by a Function when a Poisoned TLP is received by its secondary side, regardless of the state the Parity Error Response Enable bit in the Bridge Control register.
30	RW	0x0	SEC_STAT_RCVD_SYS_ERR Received System Error. This bit is set when the secondary side of a Function receives an ERR_FATAL or ERR_NONFATAL message.
29	RW	0x0	SEC_STAT_RCVD_MSTR_ABRT Received Master Abort. This bit is set when the secondary side of a Function (for requests initiated by the Type 1 header Function itself) receives a Completion with Unsupported Request Completion status.
28	RW	0x0	SEC_STAT_RCVD_TRGT_ABRT Received Target Abort. This bit is set when the secondary side of a Function (for requests initiated by the Type 1 header Function itself) receives a Completion with Completer Abort Completion status.
27	RW	0x0	SEC_STAT_SIG_TRGT_ABRT Signaled Target Abort. This bit is set when the secondary side of the Function (for Requests completed by the Type 1 header Function itself) completes a Posted or Non-Posted request as a Completer Abort error.
26:25	RO	0x0	RSVDP_25 Reserved for future use.

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Bit	Attr	Reset Value	Description
24	RW	0x0	SEC_STAT_MDPE Master Data Parity Error. This bit is set by a Function if the Parity Error Response Enable bit in the Bridge Control register is set, and either of the following two conditions occurs: - Port receives a Poisoned Completion coming Upstream - Port transmits a Poisoned Request Downstream If the Parity Error Response Enable bit is clear, this bit is never set.
23	RO	0x0	RSVDP_23 Reserved for future use.
22:16	RO	0x00	SEC_STAT_RESERV Reserved.
15:12	RW	0x0	IO_LIMIT I/O Limit Address. These bits correspond to the address[15:12] of IO address range. For the purpose of address decoding, the bridge assumes that the lower 12 address bits, address[11:0], of the I/O limit address (not implemented in the I/O Limit register) are FFFh. The I/O Limit register can be programmed to a smaller value than the I/O Base register, if there are no I/O addresses on the secondary side of the bridge. In this case, the bridge will not forward any I/O transactions from the primary bus to the secondary and will forward all I/O transactions from the secondary bus to the primary bus.
11:9	RO	0x0	IO_RESERV1 Reserved.
8	RO	0x0	IO_DECODE_BIT8 I/O Addressing Encode (IO Limit Address). This bit encodes the IO addressing capability of the bridge. Note: - For 16bit I/O address decoding, the bridge must still perform a full 32-bit decode of the I/O address (that is, check that Address[31:16] are 0000h). In this case, the I/O address range supported by the bridge will be restricted to the first 64 KB of I/O Space (0000 0000h to 0000 FFFFh). - For 16bit I/O address decoding, the bridge assumes that the upper 16 address bits, Address[31:16], of the I/O limit address (not implemented in I/O Limit register) are zero. - For 32bit I/O address decoding, and the I/O Limit Upper 16 Bits hold the upper 16 bits, corresponding to Address[31:16], of the 32-bit Limit address. In this case, system configuration software is permitted to locate the I/O address range supported by the bridge anywhere in the 4-GB I/O Space. - The 4-KB alignment and granularity restrictions still apply when the bridge supports 32-bit I/O addressing. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	IO_BASE I/O Base Address. These bits correspond to the address[15:12] of IO address range. For the purpose of address decoding, the bridge assumes that the lower 12 address bits, address[11:0], of the I/O base address (not implemented in the I/O Base register) are zero.
3:1	RO	0x0	IO_RESERV Reserved.
0	RO	0x0	IO_DECODE I/O Addressing Encode (IO Base Address). This bit encodes the IO addressing capability of the bridge. Note: - For 16bit I/O address decoding, the bridge must still perform a full 32-bit decode of the I/O address (that is, check that Address[31:16] are 0000h). In this case, the I/O address range supported by the bridge will be restricted to the first 64 KB of I/O Space (0000 0000h to 0000 FFFFh). - For 16bit I/O address decoding, the bridge assumes that the upper 16 address bits, Address[31:16], of the I/O limit address (not implemented in I/O Limit register) are zero. - For 32bit I/O address decoding, and the I/O Limit Upper 16 Bits hold the upper 16 bits, corresponding to Address[31:16], of the 32-bit Limit address. In this case, system configuration software is permitted to locate the I/O address range supported by the bridge anywhere in the 4-GB I/O Space. - The 4-KB alignment and granularity restrictions still apply when the bridge supports 32-bit I/O addressing. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

PCIE_DSP_PF0_TYPE1_HDR_MEM_LIMIT_MEM_BASE_REG

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	MEM_LIMIT Memory Limit Address. These bits correspond to the upper 12 address bits, Address[31:20], of 32-bit addresses. For the purpose of address decoding, the bridge assumes that the lower 20 address bits, Address[19:0], of the memory limit address (not implemented in the Memory Limit register) are F FFFFh. The Memory Limit register must be programmed to a smaller value than the Memory Base register if there is no memory-mapped address space on the secondary side of the bridge.
19:16	RO	0x0	MEM_LIMIT_RESERV Reserved.
15:4	RW	0x000	MEM_BASE Memory Base Address. These bits correspond to the upper 12 address bits, Address[31:20], of 32-bit addresses. For the purpose of address decoding, the bridge assumes that the lower 20 address bits, Address[19:0], of the memory base address (not implemented in the Memory Base register) are zero.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	MEM_BASE_RESERV Reserved.

PCIE_DSP_PF0_TYPE1_HDR_PREF_MEM_LIMIT_PREF_MEM_BASE_REG

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	PREF_MEM_LIMIT Prefetchable Memory Limit Address. - If the Prefetchable Memory Limit register indicates support for 32-bit addressing, then the Prefetchable Limit Upper 32 Bits register is implemented as a read-only register that returns zero when read. - If the Prefetchable Memory Limit registers indicate support for 64-bit addressing, then the Prefetchable Limit Upper 32 Bits register is implemented as a read/write register which must be initialized by configuration software. - If a 64-bit prefetchable memory address range is supported, the Prefetchable Limit Upper 32 Bits register specifies the upper 32 bits, corresponding to Address[63:32], of the 64-bit limit addresses which specify the prefetchable memory address range.
19:17	RO	0x0	PREF_RESERV1 Reserved.
16	RO	0x1	PREF_MEM_LIMIT_DECODE Prefetchable Memory Limit Decode. This bit encodes whether or not the bridge supports 64-bit addresses. Note: This bit is a copy of the PREF_MEM_DECODE bit and always reflects the current value of that bit.
15:4	RW	0x000	PREF_MEM_BASE Prefetchable Memory Base Address. - If the Prefetchable Memory Base register indicates support for 32-bit addressing, then the Prefetchable Base Upper 32 Bits register is implemented as a read-only register that returns zero when read. - If the Prefetchable Memory Base register indicates support for 64-bit addressing, then the Prefetchable Limit Upper 32 Bits register is implemented as a read/write register which must be initialized by configuration software. - If a 64-bit prefetchable memory address range is supported, the Prefetchable Base Upper 32 Bits register specifies the upper 32 bits, corresponding to Address[63:32], of the 64-bit base addresses which specify the prefetchable memory address range.
3:1	RO	0x0	PREF_RESERV Reserved.

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Bit	Attr	Reset Value	Description
0	RO	0x1	PREF_MEM_DECODE Prefetchable Memory Base Decode. This bit encodes whether or not the bridge supports 64-bit addresses. Note: By default the bit is set to 1'b1 indicating that 64-bit addresses are supported. If the bridge only supports 32-bit prefetchable memory address range, or if there is no prefetchable memory address range, then the configuration parameter MEM_DECODE_64_0 must be changed to 0. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

PCIE_DSP_PF0_TYPE1_HDR_PREF_BASE_UPPER_REG

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PREF_MEM_BASE_UPPER Prefetchable Base Upper 32 Bit. - If the Prefetchable Memory Base register indicates support for 32-bit addressing, then this register is implemented as read-only register that returns zero when read. - If the Prefetchable Memory Base register indicate support for 64-bit addressing, then this register is implemented as read/write register which must be initialized by configuration software. - This register specifies the upper 32 bits, corresponding to Address[63:32], of the 64-bit base addresses which specify the prefetchable memory address range. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: PREF_MEM_LIMIT_PREF_MEM_BASE_REG.PREF_MEM_DECODE ? RW : RO

PCIE_DSP_PF0_TYPE1_HDR_PREF_LIMIT_UPPER_REG

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PREF_MEM_LIMIT_UPPER Prefetchable Limit Upper 32 Bit. - If the Prefetchable Memory Limit register indicate support for 64-bit addressing, then this register is implemented as read/write register which must be initialized by configuration software. - This register specifies the upper 32 bits, corresponding to Address[63:32], of the 64-bit base addresses which specify the prefetchable memory address range. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: PREF_MEM_LIMIT_PREF_MEM_BASE_REG.PREF_MEM_DECODE ? RW : RO

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PCIE_DSP_PF0_TYPE1_HDR_IO_LIMIT_UPPER_IO_BASE_UPPER_REG

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	IO_LIMIT_UPPER I/O Limit Upper 16 Bits. - If the I/O Limit register indicates support for 16-bit I/O address decoding, then this register is implemented as a read-only register which return zero when read. - If the I/O Limit register indicates support for 32-bit I/O addressing, then this register must be initialized by configuration software. - If 32-bit I/O address decoding is supported, this register specifies the upper 16 bits, corresponding to Address[31:16], of the 32-bit limit address, that specify the I/O address range. - See the PCI-to-PCI Bridge Architecture Specification for additional details). Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: SEC_STAT_IO_LIMIT_IO_BASE_REG.IO_DECODE ? RW : RO
15:0	RO	0x0000	IO_BASE_UPPER I/O Base Upper 16 Bits. - If the I/O Base register indicates support for 16-bit I/O address decoding, then this register is implemented as a read-only register which return zero when read. - If the I/O base register indicates support for 32-bit I/O addressing, then this register must be initialized by configuration software. - If 32-bit I/O address decoding is supported, this register specifies the upper 16 bits, corresponding to Address[31:16], of the 32-bit base address, that specify the I/O address range. - See the PCI-to-PCI Bridge Architecture Specification for additional details. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: SEC_STAT_IO_LIMIT_IO_BASE_REG.IO_DECODE ? RW : RO

PCIE_DSP_PF0_TYPE1_HDR_TYPE1_CAP_PTR_REG

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	RSVDP_8 Reserved for future use.

Bit	Attr	Reset Value	Description
7:0	RO	0x40	CAP_POINTER Capabilities Pointer. This register is used to point to a linked list of capabilities implemented by this Function. Since all PCI Express Functions are required to implement the PCI Express Capability structure, this register must point to a valid capability structure and either this structure is the PCI Express Capability structure, or a subsequent list item points to the PCI Express Capability structure. The bottom two bits are Reserved and must be set to 00b. Software must mask these bits off before using this register as a pointer in Configuration Space to the first entry of a linked list of new capabilities. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

PCIE_DSP_PF0_TYPE1_HDR_TYPE1_EXP_ROM_BASE_REG

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:11	RW	0x000000	EXP_ROM_BASE_ADDRESS Expansion ROM Base Address. Upper 21 bits of the Expansion ROM base address. The number of bits (out of these 21) that a Function actually implements depends on how much address space the Function requires. The mask for this ROM BAR exists (if implemented) as a shadow register at this address. The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the second register at this address. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1) then R/W else R
10:8	RO	0x0	RSVDP_8 Reserved for future use.

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	ROM_BAR_VALIDATION_DETAILS Expansion ROM Validation Details. The field contains optional, implementation-specific details associated with Expansion ROM Validation. - If validation is in progress (Expansion ROM Validation Status is 001b), non-zero values of this field represent implementation-specific indications of the phase of the validation progress (e.g., 50% complete). The value 0000b indicates that no validation progress information is provided. - If validation is completed (Expansion ROM Validation Status 010b to 111b inclusive), non-zero values in this field represent additional implementation-specific information. The value 0000b indicates that no information is provided. - When validation is supported and this field is not implemented, this field must be hardwired to 0000b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1 && DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
3:1	RW	0x0	ROM_BAR_VALIDATION_STATUS Expansion ROM Validation Status. When this field is non-zero, it indicates the status of hardware validation of the Expansion ROM contents. - If the Function does not support validation, this field must be hardwired to 000b. - It is optional whether an implementation is capable of returning Validation Status values 011b, 101b, 110b, or 111b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1 && DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
0	RW	0x0	ROM_BAR_ENABLE Expansion ROM Enable. This bit controls whether or not the Function accepts accesses to its expansion ROM. The Memory Space Enable bit in the Command register has precedence over the Expansion ROM Enable bit. A Function must claim accesses to its expansion ROM only if both the Memory Space Enable bit and the Expansion ROM Enable bit are set. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1) then R/W else R

PCIE_DSP_PF0_TYPE1_HDR_BRIDGE_CTRL_INT_PIN_INT_LINE_REG

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	BRIDGE_CTRL_RESERV Reserved.

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Bit	Attr	Reset Value	Description
22	RW	0x0	SBR Secondary Bus Reset. Setting this bit triggers a hot reset on the corresponding PCI Express Port. Software must ensure a minimum reset duration (Trst) as defined in the PCI Local Bus Specification. Software and systems must honor first-access-following-reset timing requirements, unless the Readiness Notifications mechanism is used or if the Immediate Readiness bit in the relevant Function's Status Register register is set. Port configuration registers must not be changed, except as required to update Port status.
21	RO	0x0	MSTR_ABORT_MODE Master Abort Mode. This bit was originally described in the PCI-to-PCI Bridge Architecture Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
20	RO	0x0	VGA_16B_DEC VGA 16 bit decode. This bit only has meaning if VGA Enable bit is set. This bit enables system configuration software to select between 10-bit and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from primary to secondary. For Functions that do not support VGA, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
19	RO	0x0	VGA_EN VGA Enable. Modifies the response by the bridge to VGA compatible addresses. If the VGA Enable bit is set, the bridge will positively decode and forward the following accesses on the primary interface to the secondary interface (and, conversely, block the forwarding of these addresses from the secondary to primary interface): - Memory accesses in the range 000A 0000h to 000B FFFFh - I/O addresses in the first 64 KB of the I/O address space (Address[31:16] are 0000h) where Address[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases determined by the setting of VGA 16-bit Decode) If the VGA Enable bit is set, forwarding of these accesses is independent of the I/O address range and memory address ranges defined by the I/O Base and Limit registers, the Memory Base and Limit registers, and the Prefetchable Memory Base and Limit registers of the bridge. (Forwarding of these accesses is also independent of the setting of the ISA Enable bit (in the Bridge Control register) when the VGA Enable bit is set. Forwarding of these accesses is qualified by the I/O Space Enable and Memory Space Enable bits in the Command register.)

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Bit	Attr	Reset Value	Description
			For Functions that do not support VGA, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
18	RW	0x0	ISA_EN ISA Enable. Modifies the response by the bridge to ISA I/O addresses. This applies only to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of I/O address space (0000 0000h to 0000 FFFFh). If this bit is set, the bridge will block any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions will be forwarded if they address the last 768 bytes in each 1-KB block.
17	RW	0x0	SERR_EN SERR# Enable. This bit controls forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary.
16	RW	0x0	PERE Parity Error Response Enable. This bit controls the logging of poisoned TLPs in the Master Data Parity Error bit in the Secondary Status register.
15:8	RO	0x01	INT_PIN Reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
7:0	RW	0xff	INT_LINE Reserved

14.4.3.2 PCIE_DSP_PF0_PM_CAP Register Description

14.4.3.2.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PM_CAP_CAP_ID_NXT_PTR_REG	0x0000	W	0xDFC35001	This register provides information refarding the Power Management Capabilities.
PCIE_DSP_PF0_PM_CAP_CON_STATUS_REG	0x0004	W	0x00000008	This register is used to manage the PCI function's power management state as well as to enable/monitor PMEs.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3.2.2 Detail Registers Description

PCIE_DSP_PF0_PM_CAP_CAP_ID_NXT_PTR_REG

Address: Operational Base(0x00000040) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:27	RO	0x1b	PME_SUPPORT PME_Support. This 5-bit field indicates the power states in which the function may generate a PME and/or forward PME messages. A value of 0b for any bit indicates that the function is not capable of asserting PME while in that power state. - bit(27) X XXX1b - PME can be generated from D0 - bit(28) X XX1Xb - PME can be generated from D1 - bit(29) X X1XXb - PME can be generated from D2 - bit(30) X 1XXXb - PME can be generated from D3hot - bit(31) 1 XXXXb - PME can be generated from D3cold Bit 31 (PME can be asserted from D3cold) represents a special case. Functions that set this bit require some sort of auxiliary power source. Implementation specific mechanisms are recommended to validate that the power source is available before setting this bit. Each bit that corresponds to a supported D-state must be set for PCI-PCI Bridge structures representing Ports on Root Complexes/Switches to indicate that the Bridge will forward PME Messages. Bit 31 must only be set if the Port is still able to forward PME Messages when main power is not available. The read value from this field is the write value && (sys_aux_pwr_det, 1'b1, D2_SUPPORT, D1_SUPPORT, 1'b1), where D1_SUPPORT and D2_SUPPORT are fields in this register. The reset value PME_SUPPORT_n && (sys_aux_pwr_det, 1'b1, D2_SUPPORT, D1_SUPPORT, 1'b1), where PME_SUPPORT_n is a configuration parameter. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
26	RO	0x1	D2_SUPPORT D2_Support. If this bit is set, this function supports the D2 Power Management state. Functions that do not support D2 must always return a value of 0b for this bit. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
25	RO	0x1	D1_SUPPORT D1_Support. If this bit is set, this function supports the D1 Power Management state. Functions that do not support D1 must always return a value of 0b for this bit. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
24:22	RO	0x7	AUX_CURR Aux_Current. This 3 bit field reports the Vaux auxiliary current requirements for the function. If this function implements the Data Register, the controller hardwires this field to 000b. If PME_Support is 0 xxxxb (PME assertion from D3cold is not supported), the controller hardwires this field to 0000b. For functions where PME_Support is 1 xxxxb (PME assertion from D3cold is supported), and which do not implement the Data field, the encodings defined in Values: apply: Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
21	RO	0x0	DSI Device Specific Initialization. The DSI bit indicates whether special initialization of this function is required. When set, indicates that the function requires a device specific initialization sequence following a transition to the D0uninitialized state. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
20	RO	0x0	reserved
19	RO	0x0	PME_CLK PME Clock. Does not apply to PCI Express, the controller hardwires it to 0b. Note: This register field is sticky.
18:16	RO	0x3	PM_SPEC_VER Version. This field provides the Power Management specification version. The controller hardwires this field to 011b for functions compliant to PCI Express Base Specification, Revision 4.0, Version 1.0>. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:8	RO	0x50	PM_NEXT_POINTER Next Capability Pointer. This field provides an offset into the function's configuration space pointing to the location of next item in the capabilities list. If there are no additional items in the capabilities list, this field is set to 00h. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
7:0	RO	0x01	PM_CAP_ID Capability ID. This field returns 01h to indicate that this is the PCI Power Management Capability. Each function may have only one item in its capability list with Capability ID set to 01h.

PCIE_DSP_PF0_PM_CAP_CON_STATUS_REG

Address: Operational Base(0x00000040) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DATA_REG_ADD_INFO Data. This field is used to report the state dependent data requested by the Data_Select field. The value of this field is scaled by the value reported by the Data_Scale field.
23	RO	0x0	BUS_PWR_CLK_CON_EN Bus Power/Clock Control Enable. If this field is set, Bus Power/Clock Control is Enable.
22	RO	0x0	B2_B3_SUPPORT B2B3 Support for D3hot. If this field is set, B2B3 support for D3hot is available.
21:16	RO	0x00	RSVDP_16 Reserved for future use.
15	RW	0x0	PME_STATUS PME_Status. This bit is set when the function normally generates a PME signal. The value of this bit is not affected by the value of the PME_En bit. If PME_Support bit 31 of the Power Management Capabilities register is clear, this bit is permitted to be hardwired to 0b. Functions that consume Aux power must preserve the value of this sticky register when Aux power is available. In such functions, this register value is not modified by Conventional Reset or FLR. Note: This register field is sticky.
14:13	RO	0x0	DATA_SCALE Data_Scale. This field indicates the scaling factor to be used when interpreting the value of the Data field. The value and meaning of this field varies depending on which data value has been selected by the Data_Select field. For more details, see 7.5.2.3 section of PCI Express Base Specification.

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Bit	Attr	Reset Value	Description
12:9	RO	0x0	DATA_SELECT Data_Select. This 4-bit field is used to select which data is to be reported through the Data and Data_Scale field. If the Data field is not implemented, this field must be hardwired to 0000b.
8	RW	0x0	PME_ENABLE PME_En. - When set, the function is permitted to generate a PME. - When clear, the function is not permitted to generate a PME. If PME_Support is 1 xxxxb (PME generation from D3cold) or the function consumes Aux power and Aux power is available this bit is RWS and the bit is not modified by Conventional Reset or FLR. If PME_Support is 0 xxxxb, this field is not sticky (RW). If PME_Support is 0 0000b, the controller hardwires this bit to 0b. Note: This register field is sticky.
7:4	RO	0x0	RSVDP_4 Reserved for future use.
3	RO	0x1	NO_SOFT_RST No_Soft_Reset. This bit indicates the state of the function after writing the PowerState field to transition the function from D3hot to D0. - When set, this transition preserves internal function state. The function is in D0Active and no additional software intervention is required. - When clear, this transition results in undefined internal function state. Regardless of this bit, functions that transition from D3hot to D0 by Fundamental Reset will return to D0Uninitialized with only PME context preserved if PME is supported and enabled. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
2	RO	0x0	RSVDP_2 Reserved for future use.
1:0	RW	0x0	POWER_STATE PowerState. This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. You can write to this register; however, the read-back value is the actual power state, not the write value. If you attempt to write an unsupported, optional state to this field, the write operation completes normally; however, the data is discarded and no state change occurs. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

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14.4.3.3 PCIE_DSP_PF0_MSI_CAP Register Description

14.4.3.3.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_MSI_CAP_PCI_MSI_CAP_ID_NEXT_CTRL_REG	0x0000	W	0x008A7005	This register holds MSI Capability Header information and controls the MSI behaviour.
PCIE_DSP_PF0_MSI_CAP_MSI_CAP_OFF_04H_REG	0x0004	W	0x00000000	This register holds the system specified message address for an MSI transaction.
PCIE_DSP_PF0_MSI_CAP_MSI_CAP_OFF_08H_REG	0x0008	W	0x00000000	For a function that supports a 32-bit message address, - bits[31:16] of this register represent the Extended Message Data, and - bits[15:0] of this register represent the Message DataFor a function that supports a 64-bit message address (bit 23 in PCI_MSI_CAP_ID_NEXT_CTRL_REG register set), this register represents the Message Upper Address Register for MSI (Offset 08h). It specifies the Message Upper Address (System-specified message upper address). This register is required for PCI Express Endpoints and is optional for other function types. If the Message Enable bit (bit 0 of the Message Control register) is set, the contents of this register (if non-zero) specify the upper 32-bits of a 64-bit message address (Address[63:32]). If the contents of this register are zero, the Function uses the 32 bit address specified by the Message Address register.
PCIE_DSP_PF0_MSI_CAP_MSI_CAP_OFF_0CH_REG	0x000C	W	0x00000000	For a function that supports a 32-bit message address, this register contains the Mask Bits when the Per-Vector Masking Capable bit (bit 24 of PCI_MSI_CAP_ID_NEXT_CTRL_REG) is set.For a function that supports a 64-bit message address, this register contains Message Data.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3.3.2 Detail Registers Description

PCIE_DSP_PF0_MSI_CAP_PCI_MSI_CAP_ID_NEXT_CTRL_REG

Address: Operational Base(0x00000050) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	RSVDP_27 Reserved for future use.

Bit	Attr	Reset Value	Description
26	RW	0x0	PCI_MSI_EXT_DATA_EN Extended Message Data Enable. - If set, the function is enabled to provide Extended Message Data. - If clear, the function is not enabled to provide Extended Message Data. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: PCI_MSI_CAP_ID_NEXT_CTRL_REG.PCI_MSI_EXT_DATA_CAP ? RW : RO
25	RO	0x0	PCI_MSI_EXT_DATA_CAP Extended Message Data Capable. - If set, the function is capable of providing Extended Message Data. - If clear, the function does not support providing Extended Message Data. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
24	RO	0x0	PCI_PVM_SUPPORT Per-Vector Masking Capable. - If set, the function supports MSI Per-Vector Masking. - If clear, the function does not support MSI Per-Vector Masking.
23	RO	0x1	PCI_MSI_64_BIT_ADDR_CAP 64 bit address capable. - If set, the function is capable of sending a 64-bit message address. - If clear, the function is not capable of sending a 64-bit message address. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
22:20	RW	0x0	PCI_MSI_MULTIPLE_MSG_EN Multiple Message Enable. Software writes to this field to indicate the number of allocated vectors (equal to or less than the number of requested vectors). The number of allocated vectors is aligned to a power of two. If a function requests four vectors (indicated by a Multiple Message Capable encoding of 010b), system software can allocate either four, two, or one vector by writing a 010b, 001b, or 000b to this field, respectively. When MSI is enabled, a function will be allocated at least 1 vector. All encodings other than the defined encodings are reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

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Bit	Attr	Reset Value	Description
19:17	RO	0x5	PCI_MSI_MULTIPLE_MSG_CAP Multiple Message Capable. System software reads this field to determine the number of requested vectors. The number of requested vectors must be aligned to a power of two (if a function requires three vectors, it requests four by initializing this field to 010b). All encodings other than the defined encodings are reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
16	RW	0x0	PCI_MSI_ENABLE MSI Enable. - If set and the MSI-X Enable bit in the MSI-X Message Control register is clear, the function is permitted to use MSI to request service and is prohibited from using INTx interrupts. System configuration software sets this bit to enable MSI. A device driver is prohibited from writing this bit to mask a function's service request. For more details on control of INTx interrupts, see section 7.5.1.1 of PCI Express Base Specification. - If clear, the function is prohibited from using MSI to request service. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
15:8	RO	0x70	PCI_MSI_CAP_NEXT_OFFSET Next Capability Pointer. This field contains the offset to the next PCI Capability structure or 00h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
7:0	RO	0x05	PCI_MSI_CAP_ID Capability ID. Indicates the MSI Capability structure. This field returns a Capability ID of 05h indicating that this is an MSI Capability structure.

PCIE_DSP_PF0_MSI_CAP_MSI_CAP_OFF_04H_REG

Address: Operational Base(0x00000050) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	PCI_MSI_CAP_OFF_04H Message Address - System-specified message address. If the Message Enable bit (bit 16 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG register) is set, the contents of this field specify the DWORD-aligned address (Address[31:02]) for the MSI transaction. Address[1:0] are set to 00b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

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Bit	Attr	Reset Value	Description
1:0	RO	0x0	RSVDP_0 Reserved for future use.

PCIE_DSP_PF0_MSI_CAP_MSI_CAP_OFF_08H_REG

Address: Operational Base(0x00000050) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PCI_MSI_CAP_OFF_0AH For a function that supports a 32-bit message address, this field contains Extended Message Data (System-specified message data). For the MSI Capability structures without per-vector masking, it must be implemented if the Extended Message Data Capable bit is set; otherwise, it is outside the MSI Capability structure and undefined. For the MSI Capability structures with Per-vector Masking, it must be implemented if the Extended Message Data Capable bit is set; otherwise, it is RsvdP. If the Extended Message Data Enable bit (bit 26 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) is set, the DWORD Memory Write transaction uses Extended Message Data for the upper 16 bits; otherwise, it uses 0000h for the upper 16 bits. For a function that supports a 64-bit message address, it contains upper 16 bits of the Message Upper Address. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: PCI_MSI_64_BIT_ADDR_CAP || `DEFAULT_EXT_MSI_DATA_CAPABLE ? R/W : R
15:0	RW	0x0000	PCI_MSI_CAP_OFF_08H For a function that supports a 32-bit message address, this field contains Message Data (System-specified message data). If the Message Enable bit (bit 16 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) is set, the function sends a DWORD Memory Write transaction using Message Data for the lower 16 bits. All 4 Byte Enables are set. The Multiple Message Enable field (bits 22:20 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010b indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000b, the Function is not permitted to modify the message data. For a function that supports a 64-bit message address, it contains lower 16 bits of the Message Upper Address. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

PCIE_DSP_PF0_MSI_CAP_MSI_CAP_OFF_0CH_REG

Address: Operational Base(0x00000050) + offset (0x000C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PCI_MSI_CAP_OFF_0EH For a function that supports a 32-bit message address, this field contains the upper Mask Bits when the Per Vector Masking Capable bit (PCI_MSI_CAP_ID_NEXT_CTRL_REG.PCI_PVM_SUPPORT) is set. For a function that supports a 64-bit message address, this field contains Message Data (System-specified message data). Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: (!MSI_64_EN && MSI_PVM_EN_VALUE) ? RW: MSI_64_EN && DEFAULT_EXT_MSI_DATA_CAPABLE ? RW : RO
15:0	RW	0x0000	PCI_MSI_CAP_OFF_0CH For a function that supports a 32-bit message address, this field contains the lower Mask Bits when the Per Vector Masking Capable bit (PCI_MSI_CAP_ID_NEXT_CTRL_REG.PCI_PVM_SUPPORT) is set. For a function that supports a 64-bit message address, this field contains Message Data (System-specified message data). If the Message Enable bit (bit 16 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) is set, the function sends a DWORD Memory Write transaction using Message Data for the lower 16 bits. All 4 Byte Enables are set. The Multiple Message Enable field (bits 22:20 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010b indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000b, the Function is not permitted to modify the message data. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: PCI_MSI_64_BIT_ADDR_CAP || MSI_PVM_EN ? R/W : R

14.4.3.4 PCIE_DSP_PF0_PCIE_CAP Register Description

14.4.3.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PCIE_CAP_PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP_REG	0x0000	W	0x0042B010	This is the PCI Express Capabilities, ID, and Next Pointer Register.
PCIE_DSP_PF0_PCIE_CAP_DEVICE_CAPABILITIES_REG	0x0004	W	0x00008000	The Device Capabilities register identifies PCI Express device function specific capabilities.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PCIE_CAP_DEVICE_CONTROL_DEVICE_STATUS	0x0008	W	0x00102010	This register controls PCI Express device specific parameters and provides information about PCI Express device (function) specific parameters.
PCIE_DSP_PF0_PCIE_CAP_LINK_CAPABILITIES_REG	0x000C	W	0x0072AC13	The Link Capabilities register identifies PCI Express Link specific capabilities.
PCIE_DSP_PF0_PCIE_CAP_LINK_CONTROL_LINK_STATUS_REG	0x0010	W	0x10110000	This register controls and provides information about PCI Express Link specific parameters.
PCIE_DSP_PF0_PCIE_CAP_SLOT_CAPABILITIES_REG	0x0014	W	0x00000000	The Slot Capabilities register identifies PCI Express slot specific capabilities.
PCIE_DSP_PF0_PCIE_CAP_SLOT_CONTROL_SLOT_STATUS	0x0018	W	0x004003C0	This register controls and provides information about PCI Express Slot specific parameters.
PCIE_DSP_PF0_PCIE_CAP_ROOT_CONTROL_ROOT_CAPABILITIES_REG	0x001C	W	0x00010000	This register controls PCI Express Root Complex specific parameters and identifies PCI Express Root Port specific capabilities.
PCIE_DSP_PF0_PCIE_CAP_ROOT_STATUS_REG	0x0020	W	0x00000000	The Root Status register provides information about PCI Express device specific parameters.
PCIE_DSP_PF0_PCIE_CAP_DEVICE_CAPABILITIES2_REG	0x0024	W	0x000C0C10	This register identifies PCI Express device specific capabilities; in addition to the Device Capabilities Register.
PCIE_DSP_PF0_PCIE_CAP_DEVICE_CONTROL2_DEVICE_STATUS2_REG	0x0028	W	0x00000000	This register controls PCI Express device specific parameters and provides information about PCI Express device (function) specific parameters; in addition to the Device Control and Device Status Register.
PCIE_DSP_PF0_PCIE_CAP_LINK_CAPABILITIES2_REG	0x002C	W	0x0000000E	This register identifies PCI Express Link specific capabilities; in addition to the Link Capabilities Register.
PCIE_DSP_PF0_PCIE_CAP_LINK_CONTROL2_LINK_STATUS2_REG	0x0030	W	0x00010003	This register controls and provides information about PCI Express Link specific parameters; in addition to the Link Control and Link Status Register.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3.4.2 Detail Registers Description

PCIE_DSP_PF0_PCIE_CAP_PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP_REG

Address: Operational Base(0x00000070) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	RSVDP_31 Reserved for future use.
30	RO	0x0	RSVD Reserved.
29:25	RO	0x00	PCIE_INT_MSG_NUM

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Bit	Attr	Reset Value	Description
			PCIE Interrupt Message Number. Interrupt Message Number. This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability structure. For MSI, the value in this field indicates the offset between the base Message Data and the interrupt message that is generated. Hardware is required to update this field so that it is correct if the number of MSI Messages assigned to the Function changes when software writes to the Multiple Message Enable field in the MSI Message Control register. For MSI-X, the value in this field indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant. If both MSI and MSI-X are implemented, they are permitted to use different vectors, though software is permitted to enable only one mechanism at a time. If MSI-X is enabled, the value in this field must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this field must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this field is undefined. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
24	RO	0x0	PCIE_SLOT_IMP Slot Implemented. When set, this bit indicates that the Link associated with this Port is connected to a slot (as compared to being connected to a system-integrated device or being disabled). This bit is valid for Downstream Ports. This bit is undefined for Upstream Ports. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

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Bit	Attr	Reset Value	Description
23:20	RO	0x4	PCIE_DEV_PORT_TYPE Device/Port Type. Indicates the specific type of this PCI Express function. Note: Different functions in a Multi-Function Device can generally be of different types. Defined encodings for functions that implement a Type 00h PCI Configuration Space header are: Defined encodings for functions that implement a Type 01h PCI Configuration Space header are: All other encodings are Reserved. Note: Different Endpoint types have notably different requirements in Section 1.3.2 of PCI Express Base Specification regarding I/O resources, Extended Configuration Space, and other capabilities.
19:16	RO	0x2	PCIE_CAP_REG Capability Version. Indicates PCI-SIG defined PCI Express Capability structure version number. A version of the specification that changes the PCI Express Capability structure in a way that is not otherwise identifiable (for example, through a new Capability field) is permitted to increment this field. All such changes to the PCI Express Capability structure must be software-compatible. Software must check for Capability Version numbers that are greater than or equal to the highest number defined when the software is written, as functions reporting any such Capability Version numbers will contain a PCI Express Capability structure that is compatible with that piece of software. The controller hardwires this field to 2h for functions compliant to PCI Express Base Specification, Revision 4.0, Version 1.0. Note: This register field is sticky.
15:8	RO	0xb0	PCIE_CAP_NEXT_PTR Next Capability Pointer. This field contains the offset to the next PCI Capability structure or 00h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
7:0	RO	0x10	PCIE_CAP_ID Capability ID. Indicates the PCI Express Capability structure. This field must return a Capability ID of 10h indicating that this is a PCI Express Capability structure.

PCIE_DSP_PF0_PCIE_CAP_DEVICE_CAPABILITIES_REG

Address: Operational Base(0x00000070) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	RSVDP_16 Reserved for future use.

Bit	Attr	Reset Value	Description
15	RO	0x1	PCIE_CAP_ROLE_BASED_ERR_REPORT Role-Based Error Reporting. When set, this bit indicates that the function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be set by all functions conforming to the ECN, PCI Express Base Specification, Revision 1.1., or subsequent PCI Express Base Specification revisions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
14:6	RO	0x000	RSVDP_6 Reserved for future use.
5	RO	0x0	PCIE_CAP_EXT_TAG_SUPP Extended Tag Field Supported. This bit, in combination with the 10-Bit Tag Requester Supported bit in the Device Capabilities 2 register, indicates the maximum supported size of the Tag field as a Requester. This bit must be set if the 10-Bit Tag Requester Supported bit is set. Note: 8-bit Tag field generation must be enabled by the Extended Tag Field Enable bit in the Device Control register of the Requester Function before 8-bit Tags can be generated by the Requester. See Section 2.2.6.2 of PCI Express Base Specification for interactions with enabling the use of 10-Bit Tags. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
4:3	RO	0x0	PCIE_CAP_PHANTOM_FUNC_SUPPORT Phantom Functions Supported. This field indicates the support for use of unclaimed function numbers to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers (called Phantom Functions) with the Tag identifier (see Section 2.2.6.2 of PCI Express Base Specification for a description of Tag Extensions). With every Function in an ARI Device, the Phantom Functions Supported field must be set to 00b. The remainder of this field description applies only to non-ARI Multi-Function Devices. This field indicates the number of most significant bits of the Function Number portion of Requester ID that are logically combined with the Tag identifier. Note: Phantom Function support for the function must be enabled by the Phantom Functions Enable field in the Device Control register before the Function is permitted to use the Function Number field in the Requester ID for Phantom Functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
2:0	RO	0x0	PCIE_CAP_MAX_PAYLOAD_SIZE Max_Payload_Size Supported. This field indicates the maximum payload size that the function can support for TLPs. All encodings other than the defined encodings are reserved. The functions of a Multi-Function Device are permitted to report different values for this field. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

PCIE_DSP_PF0_PCIE_CAP_DEVICE_CONTROL_DEVICE_STATUS

Address: Operational Base(0x00000070) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	RSVDP_22 Reserved for future use.
21	RO	0x0	PCIE_CAP_TRANS_PENDING Transactions Pending. Root and Switch Ports: The controller hardwires this bit to 0b.
20	RO	0x1	PCIE_CAP_AUX_POWER_DETECTED AUX Power Detected. Functions that require Aux power report this bit as set if Aux power is detected by the function. This bit is derived by sampling the sys_aux_pwr_det input.

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Bit	Attr	Reset Value	Description
19	RW	0x0	PCIE_CAP_UNSUPPORTED_REQ_DETECTED Unsupported Request Detected. This bit indicates that the function received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function Device, each function indicates status of errors as perceived by the respective function.
18	RW	0x0	PCIE_CAP_FATAL_ERR_DETECTED Fatal Error Detected. This bit indicates status of Fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function device, each function indicates status of errors as perceived by the respective Function. For Functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register.
17	RW	0x0	PCIE_CAP_NON_FATAL_ERR_DETECTED Non-Fatal Error Detected. This bit indicates status of Non-fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function device, each function indicates status of errors as perceived by the respective Function. For functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register.
16	RW	0x0	PCIE_CAP_CORR_ERR_DETECTED Correctable Error Detected. This bit indicates status of correctable errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function device, each function indicates status of errors as perceived by the respective function. For functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Correctable Error Mask register.
15	RO	0x0	reserved
14:12	RW	0x2	PCIE_CAP_MAX_READ_REQ_SIZE Max_Read_Request_Size. This field sets the maximum Read Request size for the function as a Requester. The function must not generate Read Requests with a size exceeding the set value. For functions that do not generate Read Requests larger than 128 bytes and functions that do not generate Read Requests on their own behalf, the controller implements this field as Read Only (RO) with a value of 000b.

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Bit	Attr	Reset Value	Description
11	RO	0x0	PCIE_CAP_EN_NO_SNOOP Enable No Snoop. If this bit is set, the function is permitted to Set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency (see section 2.2.6.5 in PCI Express Base Specification). Note: Setting this bit to 1b should not cause a function to set the No Snoop attribute on all transactions that it initiates. Even when this bit is set, a function is only permitted to set the No Snoop attribute on a transaction when it can guarantee that the address of the transaction is not stored in any cache in the system. The controller hardwires this bit 0b if a function would never set the No Snoop attribute in transactions it initiates. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
10	RW	0x0	PCIE_CAP_AUX_POWER_PM_EN Aux Power PM Enable. This bit is derived by sampling the sys_aux_pwr_det input. When set this bit, enables a function to draw Aux power independent of PME Aux power. Functions that require Aux power on legacy operating systems should continue to indicate PME Aux power requirements. Aux power is allocated as requested in the Aux_Current field of the Power Management Capabilities register (PMC), independent of the PME_En bit in the Power Management Control/Status register (PMCSR). For Multi-Function devices, a component is allowed to draw Aux power if at least one of the functions has this bit set. Note: Functions that consume Aux power must preserve the value of this sticky register when Aux power is available. In such functions, this bit is not modified by Conventional Reset. For functions that do not implement this capability, the controller hardwires this bit to 0b. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
9	RO	0x0	PCIE_CAP_PHANTOM_FUNC_EN Phantom Functions Enable. This bit, in combination with the 10-Bit Tag Requester Enable bit in the Device Control 2 register, determines how many Tag field bits a Requester is permitted to use. When the 10-Bit Tag Requester Enable bit is clear, - If this bit is set, it enables a function to use unclaimed functions as Phantom functions to extend the number of outstanding transaction identifiers - If this bit is clear, the function is not allowed to use Phantom functions For more details, see section 2.2.6.2 of PCI Express Base Specification. Software should not change the value of this bit while the function has outstanding Non-Posted Requests; otherwise, the result is undefined. For functions that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: DEVICE_CAPABILITIES_REG.PCIE_CAP_PHANTOM_FUNC_SUPPORT ? RW : RO
8	RO	0x0	PCIE_CAP_EXT_TAG_EN Extended Tag Field Enable. This bit, in combination with the 10-Bit Tag Requester Enable bit in the Device Control 2 register, determines how many Tag field bits a Requester is permitted to use. When the 10-Bit Tag Requester Enable bit is clear, - If the Extended Tag Field Enable bit is set, the function is permitted to use an 8-bit Tag field as a Requester - If the Extended Tag Field Enable bit is clear, the Function is restricted to a 5-bit Tag field See section 2.2.6.2 of PCI Express Base Specification for required behavior when the 10-Bit Tag Requester Enable bit is set. If software changes the value of the Extended Tag Field Enable bit while the function has outstanding Non-Posted Requests, the result is undefined. For functions that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: DEVICE_CAPABILITIES_REG.PCIE_CAP_EXT_TAG_SUPP ? RW : RO

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	PCIE_CAP_MAX_PAYLOAD_SIZE_CS Max_Payload_Size. This field sets maximum TLP payload size for the Function. As a Receiver, the Function must handle TLPs as large as the set value. As a Transmitter, the Function must not generate TLPs exceeding the set value. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported field (PCIE_CAP_MAX_PAYLOAD_SIZE) in the Device Capabilities (DEVICE_CAPABILITIES_REG) register (for more details, see section 7.5.3.3 of PCI Express Base Specification). This field sets the maximum Read Request size for the function as a Requester. The function must not generate Read Requests with a size exceeding the set value. For Functions that support only the 128-byte max payload size, the controller hardwires this field to 000b. System software is not required to program the same value for this field for all the Functions of a Multi-Function device (for more details, see section 2.2.2 of PCI Express Base Specification). For ARI Devices, Max_Payload_Size is determined solely by the setting in Function0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
4	RW	0x1	PCIE_CAP_EN_REL_ORDER Enable Relaxed Ordering. If this bit is set, the function is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering (for more details, see section 2.2.6.4 and section 2.4 of PCI Express Base Specification). For a function that never sets the Relaxed Ordering attribute in transactions it initiates as a Requester, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
3	RW	0x0	PCIE_CAP_UNSUPPORT_REQ_REP_EN Unsupported Request Reporting Enable. This bit, in conjunction with other bits, controls the signaling of Unsupported Request Errors by sending error Messages (for more details, see section 6.2.5 and section 6.2.6 of PCI Express Base Specification). For a Multi-Function Device, this bit controls error reporting for each Function from point-of-view of the respective Function.

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Bit	Attr	Reset Value	Description
2	RW	0x0	PCIE_CAP_FATAL_ERR_REPORT_EN Fatal Error Reporting Enable. This bit, in conjunction with other bits, controls sending ERR_FATAL Messages (for more details, see section 6.2.5 and section 6.2.6 of of PCI Express Base Specification). For a Multi-Function device, this bit controls error reporting for each function from point-of-view of the respective function. For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL Message is generated.
1	RW	0x0	PCIE_CAP_NON_FATAL_ERR_REPORT_EN Non-Fatal Error Reporting Enable. This bit, in conjunction with other bits, controls sending ERR_NONFATAL Messages (for more details, see section 6.2.5 and Section 6.2.6 of PCI Express Base Specification). For a Multi-Function Device, this bit controls error reporting for each function from point-of-view of the respective Function. For a Root Port, the reporting of Non-fatal errors is internal to the root. No external ERR_NONFATAL Message is generated.
0	RW	0x0	PCIE_CAP_CORR_ERR_REPORT_EN Correctable Error Reporting Enable. This bit, in conjunction with other bits, controls sending ERR_COR Messages (for more details, see section 6.2.5, section 6.2.6, and section 6.2.10.2 of PCI Express Base Specification). For a Multi-Function device, this bit controls error reporting for each function from point-of-view of the respective function. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR Message is generated.

PCIE_DSP_PF0_PCIE_CAP_LINK_CAPABILITIES_REG

Address: Operational Base(0x00000070) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	PCIE_CAP_PORT_NUM Port Number. This field indicates the PCI Express Port number for the given PCI Express Link. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
23	RO	0x0	RSVDP_23 Reserved for future use.

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Bit	Attr	Reset Value	Description
22	RO	0x1	PCIE_CAP_ASPM_OPT_COMPLIANCE ASPM Optionality Compliance. This field must be set to 1b in all functions. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
21	RO	0x1	PCIE_CAP_LINK_BW_NOT_CAP Link Bandwidth Notification Capability. A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. This capability is required for all Root Ports and Switch Downstream Ports supporting Links wider than x1 and/or multiple Link speeds. This field is not applicable and is Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
20	RO	0x1	PCIE_CAP_DLL_ACTIVE_REP_CAP Data Link Layer Link Active Reporting Capable. For a Downstream Port, the controller hardwires this bit to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port (as indicated by the Hot-Plug Capable bit of the Slot Capabilities register) or a Downstream Port that supports Link speeds greater than 5.0 GT/s, the controller hardwires this bit to 1b. For Upstream Ports and components that do not support this optional capability, the controller hardwires this bit to 0b.
19	RO	0x0	PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP Surprise Down Error Reporting Capable. For a Downstream Port, this bit must be set if the component supports the optional capability of detecting and reporting a Surprise Down error condition. For Upstream Ports and components that do not support this optional capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
18	RO	0x0	PCIE_CAP_CLOCK_POWER_MAN Clock Power Management. For Upstream Ports, a value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) via the "clock request" (CLKREQ#) mechanism when the Link is in the L1 and L2/L3 Ready Link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these Link states. L1 PM Substates defines other semantics for the CLKREQ# signal, which are managed independently of Clock Power Management. This Capability is applicable only in form factors that support "clock request" (CLKREQ#) capability. For a Multi-Function device associated with an Upstream Port, each Function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the Multi-Function device indicate a 1b in this bit. For ARI Devices, all Functions must indicate the same value in this bit. For Downstream Ports, the controller hardwires this bit to 0b. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
17:15	RO	0x5	PCIE_CAP_L1_EXIT_LATENCY L1 Exit Latency. This field indicates the L1 exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from ASPM L1 to L0. If ASPM L1 is not supported, the value is undefined. Note: Exit latencies may be influenced by PCI Express reference clock configuration depending upon whether a component uses a common or separate reference clock. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. There are two each of these register fields, this one and a shadow one at the same address. The Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG) determines which one is used by the controller and which one is accessed by a read request. Common Clock operation is supported (possible) in the controller when one or more of the following expressions is true: - CX_NFTS !=CX_COMM_NFTS - DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY - DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Common Clock operation is enabled in the controller when you set the Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG). The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the shadow field at this location. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
14:12	RO	0x2	PCIE_CAP_L0S_EXIT_LATENCY L0s Exit Latency. This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0. If L0s is not supported, the value is undefined; however, see the Implementation Note "Potential Issues With Legacy Software When L0s is Not Supported" in section 5.4.1.1 of PCI Express Base Specification for the recommended value. Note: Exit latencies may be influenced by PCI Express reference clock configuration depending upon whether a component uses a common or separate reference clock. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. There are two each of these register fields, this one and a shadow one at the same address. The Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG) determines which one is used by the controller and which one is accessed by a read request. Common Clock operation is supported (possible) in the controller when one or more of the following expressions is true: - CX_NFTS !=CX_COMM_NFTS - DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY - DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Common Clock operation is enabled in the controller when you set the Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG). The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the shadow field at this location. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
11:10	RO	0x3	PCIE_CAP_ACTIVE_STATE_LINK_PM_SUPPORT Active State Power Management (ASPM) Support. This field indicates the level of ASPM supported on the given PCI Express Link. For more details on ASPM support requirements, see section 5.4.1 of PCI Express Base Specification. Multi-Function devices associated with an Upstream Port must report the same value in this field for all functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
9:4	RO	0x01	PCIE_CAP_MAX_LINK_WIDTH Maximum Link Width. This field indicates the maximum Link width (xN - corresponding to N Lanes) implemented by the component. This value is permitted to exceed the number of Lanes routed to the slot (Downstream Port), adapter connector (Upstream Port), or in the case of component-to-component connections, the actual wired connection width. All encodings other than the defined encodings are reserved. Multi-Function devices associated with an Upstream Port must report the same value in this field for all functions. In M-PCIe mode, the reset and dynamic values of this field are calculated by the controller. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
3:0	RO	0x3	PCIE_CAP_MAX_LINK_SPEED Max Link Speed. This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. All encodings other than the defined encodings are reserved. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. In M-PCIe mode, the reset and dynamic values of this field are calculated by the controller. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

PCIE_DSP_PF0_PCIE_CAP_LINK_CONTROL_LINK_STATUS_REG

Address: Operational Base(0x00000070) + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	PCIE_CAP_LINK_AUTO_BW_STATUS Link Autonomous Bandwidth Status. This bit is set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG.

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Bit	Attr	Reset Value	Description
			This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b.
30	RW	0x0	PCIE_CAP_LINK_BW_MAN_STATUS Link Bandwidth Management Status. This bit is set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit. Note: This bit is set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. The default value of this bit is 0b. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG.
29	RO	0x0	PCIE_CAP_DLL_ACTIVE Data Link Layer Link Active. This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. This bit must be implemented if the Data Link Layer Link Active Reporting Capable bit is 1b. Otherwise, the controller hardwires it to 0b.
28	RO	0x1	PCIE_CAP_SLOT_CLK_CONFIG Slot Clock Configuration. This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference clock on the connector, this bit must be clear. For a Multi-Function Device, each Function must report the same value for this bit. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

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Bit	Attr	Reset Value	Description
27	RO	0x0	PCIE_CAP_LINK_TRAINING Link Training. This read-only bit indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state. This bit is not applicable and Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches, and the controller hardwires it to 0b.
26	RO	0x0	RSVDP_26 Reserved for future use.
25:20	RO	0x01	PCIE_CAP_NEGO_LINK_WIDTH Negotiated Link Width. This field indicates the negotiated width of the given PCI Express Link. All encodings other than the defined encodings are reserved. The value in this field is undefined when the Link is not up.
19:16	RO	0x1	PCIE_CAP_LINK_SPEED Current Link Speed. This field indicates the negotiated Link speed of the given PCI Express Link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. All encodings other than the defined encodings are reserved. The value in this field is undefined when the Link is not up.
15:14	RW	0x0	PCIE_CAP_DRS_SIGNALING_CONTROL DRS Signaling Control. Indicates the mechanism used to report reception of a DRS message. Must be implemented for Downstream Ports with the DRS Supported bit Set in the Link Capabilities 2 Register. Encodings are: If DRS Supported is set, receiving a DRS Message will set DRS Message Received in the Link Status 2 Register but will otherwise have no effect If the DRS Message Received bit in the Link Status 2 Register transitions from 0 to 1, and either MSI or MSI-X is enabled, an MSI or MSI-X interrupt is generated using the vector in Interrupt Message Number (section 7.5.3.2) If the DRS Message Received bit in the Link Status 2 Register transitions from 0 to 1, the Port must send an FRS Message Upstream with the FRS Reason field set to DRS Message Received. Behavior is undefined if this field is set to 10b and the FRS Supported bit in the Device Capabilities 2 Register is Clear. Behavior is undefined if this field is set to 11b. For Downstream Ports with the DRS Supported bit clear in the Link Capabilities 2 register, the controller hardwires this field to 00b. This field is Reserved for Upstream Ports. Note: The access attributes of this field are as follows:

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Bit	Attr	Reset Value	Description
			- Wire: No access. - Dbi: LINK_CAPABILITIES2_REG.DRS_SUPPORTED ? RW : RO
13:12	RO	0x0	RSVDP_12 Reserved for future use.
11	RW	0x0	PCIE_CAP_LINK_AUTO_BW_INT_EN Link Autonomous Bandwidth Management Interrupt Enable. When set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been set. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_LINK_BW_NOT_CAP ? RW : RO
10	RW	0x0	PCIE_CAP_LINK_BW_MAN_INT_EN Link Bandwidth Management Interrupt Enable. When set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been set. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_LINK_BW_NOT_CAP ? RW : RO

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Bit	Attr	Reset Value	Description
9	RW	0x0	PCIE_CAP_HW_AUTO_WIDTH_DISABLE Hardware Autonomous Width Disable. When set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RW, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. For components that do not implement the ability autonomously to change Link width, the ciontroller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
8	RW	0x0	PCIE_CAP_EN_CLK_POWER_MAN Enable Clock Power Management. Applicable only for Upstream Ports and with form factors that support a "Clock Request" (CLKREQ#) mechanism, this bit operates as follows: For a non-ARI Multi-Function Device, power-management-configuration software must only Set this bit if all Functions of the Multi-Function Device indicate a 1b in the Clock Power Management bit of the Link Capabilities register. The component is permitted to use the CLKREQ# signal to power manage Link clock only if this bit is Set for all Functions. For ARI Devices, Clock Power Management is enabled solely by the setting in Function 0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. The CLKREQ# signal may also be controlled via the L1 PM Substates mechanism. Such control is not affected by the setting of this bit. For Downstream Ports and components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities register), the controller hardwires this bit to 0b. The write value is gated with the PCIE_CAP_CLOCK_POWER_MAN field in LINK_CAPABILITIES_REG. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_CLOCK_POWER_MAN ? RWS : ROS Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
7	RW	0x0	PCIE_CAP_EXTENDED_SYNCH Extended Synch. When set, this bit forces the transmission of additional Ordered Sets when exiting the L0s state (see section 4.2.4.5 of PCI Express Base Specification) and when in the Recovery state (see section 4.2.6.4.1 of PCI Express Base Specification). This mode provides external devices (for example, logic analyzers) monitoring the Link time to achieve bit and Symbol lock before the Link enters the L0 state and resumes communication. For Multi-Function devices if any function has this bit set, then the component must transmit the additional Ordered Sets when exiting L0s or when in Recovery.
6	RW	0x0	PCIE_CAP_COMMON_CLK_CONFIG Common Clock Configuration. When set, this bit indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. A value of 0b indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. For non-ARI Multi-Function Devices, software must program the same value for this bit in all Functions. If not all Functions are Set, then the component must as a whole assume that its reference clock is not common with the Upstream component. For ARI Devices, Common Clock Configuration is determined solely by the setting in Function 0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Components utilize this common clock configuration information to report the correct L0s and L1 Exit Latencies. After changing the value in this bit in both components on a Link, software must trigger the Link to retrain by writing a 1b to the Retrain Link bit of the Downstream Port.
5	RW	0x0	PCIE_CAP_RETRAIN_LINK Retrain Link. A write of 1b to this bit initiates Link retraining by directing the Physical Layer LTSSM to the Recovery state. If the LTSSM is already in Recovery or Configuration, re-entering Recovery is permitted but not required. If the Port is in DPC when a write of 1b to this bit occurs, the result is undefined. Reads of this bit always return 0b. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress. This bit is not applicable and is Reserved for Endpoints, PCI

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Bit	Attr	Reset Value	Description
			Express to PCI/PCI-X bridges, and Upstream Ports of Switches. This bit always returns 0b when read. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: see description
4	RW	0x0	PCIE_CAP_LINK_DISABLE Link Disable. This bit disables the Link by directing the LTSSM to the Disabled state when set; this bit is Reserved on Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state. After clearing this bit, software must honor timing requirements defined in Section 6.6.1 with respect to the first Configuration Read following a Conventional Reset. In a DSP that supports crosslink, the controller gates the write value with the CROSS_LINK_EN field in PORT_LINK_CTRL_OFF. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: CX_CROSSLINK_ENABLE=1 && PORT_LINK_CTRL_OFF.CROSS_LINK_EN=1||CX_CROSSLINK_ENABLE=0 && dsp=1? RW : RO
3	RO	0x0	PCIE_CAP_RCB Read Completion Boundary (RCB). Root Ports: Indicates the RCB value for the Root Port. Refer to section 2.3.1.1 of PCI Express Base Specification for the definition of the parameter RCB. The controller hardwires this bit for a Root Port and returns its RCB support capabilities. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
2	RO	0x0	RSVDP_2 Reserved for future use.

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	PCIE_CAP_ACTIVE_STATE_LINK_PM_CONTROL Active State Power Management (ASPM) Control. This field controls the level of ASPM enabled on the given PCI Express Link. See section 5.4.1.3 of PCI Express Base Specification for requirements on when and how to enable ASPM. Note: "L0s Entry Enabled" enables the Transmitter to enter L0s. If L0s is supported, the Receiver must be capable of entering L0s even when the Transmitter is disabled from entering L0s (00b or 10b). ASPM L1 must be enabled by software in the Upstream component on a Link prior to enabling ASPM L1 in the Downstream component on that Link. When disabling ASPM L1, software must disable ASPM L1 in the Downstream component on a Link prior to disabling ASPM L1 in the Upstream component on that Link. ASPM L1 must only be enabled on the Downstream component if both components on a Link support ASPM L1. For Multi-Function Devices (including ARI Devices), it is recommended that software program the same value for this field in all Functions. For non-ARI Multi-Function Devices, only capabilities enabled in all Functions are enabled for the component as a whole. For ARI Devices, ASPM Control is determined solely by the setting in Function0, regardless of Function 0's D-state. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Software must not enable L0s in either direction on a given Link unless components on both sides of the Link each support L0s; otherwise, the result is undefined.

PCIE_DSP_PF0_PCIE_CAP_SLOT_CAPABILITIES_REG

Address: Operational Base(0x00000070) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	PCIE_CAP_PHY_SLOT_NUM Physical Slot Number. This field indicates the physical slot number attached to this Port. This field must be hardware initialized to a value that assigns a slot number that is unique within the chassis, regardless of the form factor associated with the slot. This field must be initialized to zero for Ports connected to devices that are either integrated on the system board or integrated within the same silicon as the Switch device or Root Port. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

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Bit	Attr	Reset Value	Description
18	RO	0x0	PCIE_CAP_NO_CMD_CPL_SUPPORT No Command Completed Support. When set, this bit indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller. This bit is only permitted to be set if the hot-plug capable Port is able to accept writes to all fields of the Slot Control register without delay between successive writes. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
17	RO	0x0	PCIE_CAP_ELECTROMECH_INTERLOCK Electromechanical Interlock Present. When set, this bit indicates that an Electromechanical Interlock is implemented on the chassis for this slot. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
16:15	RO	0x0	PCIE_CAP_SLOT_POWER_LIMIT_SCALE Slot Power Limit Scale. Specifies the scale used for the Slot Power Limit Value (for more details, see Section 6.9 of PCI Express Base Specification). This register must be implemented if the Slot Implemented bit is set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 00b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
14:7	RO	0x00	PCIE_CAP_SLOT_POWER_LIMIT_VALUE Slot Power Limit Value. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by the slot (for more detais, see Section 6.9 of PCI Express Base Specification) or by other means to the adapter. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field except when the Slot Power Limit Scale field equals 00b (1.0x) and Slot Power Limit Value exceeds EFh, the alternative encodings defined in Values: are used. Value F3h to FFh are Reserved for Slot Power Limit values above 300 W. This register must be implemented if the Slot Implemented bit is set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 0000 0000b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

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Bit	Attr	Reset Value	Description
6	RO	0x0	PCIE_CAP_HOT_PLUG_CAPABLE Hot-Plug Capable. When set, this bit indicates that this slot is capable of supporting hot-plug operations. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
5	RO	0x0	PCIE_CAP_HOT_PLUG_SURPRISE Hot-Plug Surprise. When set, this bit indicates that an adapter present in this slot might be removed from the system without any prior notification. This is a form factor specific capability. This bit is an indication to the operating system to allow for such removal without impacting continued software operation. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
4	RO	0x0	PCIE_CAP_POWER_INDICATOR Power Indicator Present. When set, this bit indicates that a Power Indicator is electrically controlled by the chassis for this slot. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
3	RO	0x0	PCIE_CAP_ATTENTION_INDICATOR Attention Indicator Present. When set, this bit indicates that an Attention Indicator is electrically controlled by the chassis. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
2	RO	0x0	PCIE_CAP_MRL_SENSOR MRL Sensor Present. When set, this bit indicates that an MRL Sensor is implemented on the chassis for this slot. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
1	RO	0x0	PCIE_CAP_POWER_CONTROLLER Power Controller Present. When set, this bit indicates that a software programmable Power Controller is implemented for this slot/adapter (depending on form factor). Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
0	RO	0x0	PCIE_CAP_ATTENTION_INDICATOR_BUTTON Attention Button Present. When set, this bit indicates that an Attention Button for this slot is electrically controlled by the chassis. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

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PCIE_DSP_PF0_PCIE_CAP_SLOT_CONTROL_SLOT_STATUS

Address: Operational Base(0x00000070) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	RSVDP_25 Reserved for future use.
24	RW	0x0	PCIE_CAP_DLL_STATE_CHANGED Data Link Layer State Changed. This bit is set when the value reported in the Data Link Layer Link Active bit of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read the Data Link Layer Link Active bit of the Link Status register to determine if the Link is active before initiating configuration cycles to the hot plugged device.
23	RO	0x0	PCIE_CAP_ELECTROMECH_INTERLOCK_STATUS Electromechanical Interlock Status. If an Electromechanical Interlock is implemented, this bit indicates the status of the Electromechanical Interlock.
22	RO	0x1	PCIE_CAP_PRESENCE_DETECT_STATE Presence Detect State. This bit indicates the presence of an adapter in the slot, reflected by the logical "OR" of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. Note that the in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected. Consequently, form factors that require a power controller for hot-plug must implement a physical pin presence detect mechanism. This bit must be implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities register is 0b), the controller hardwires this bit to 1b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
21	RO	0x0	PCIE_CAP_MRL_SENSOR_STATE MRL Sensor State. This bit reports the status of the MRL sensor if implemented. Encodings are define as above.
20	RW	0x0	PCIE_CAP_CMD_CPLD Command Completed. If Command Completed notification is supported (if the No Command Completed Support bit in the Slot Capabilities register is 0b), this bit is set when a hot-plug command has completed and the Hot-Plug Controller is ready to accept a subsequent command. The Command Completed status bit is set as an indication to host software that the Hot-Plug Controller has processed the previous command and is ready to receive the next command; it provides no guarantee that the action corresponding to the command is complete. If Command Completed notification is not supported, the controller hardwires this bit to 0b.

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Bit	Attr	Reset Value	Description
19	RW	0x0	PCIE_CAP_PRESENCE_DETECTED_CHANGED Presence Detect Changed. This bit is set when the value reported in the Presence Detect State bit is changed.
18	RW	0x0	PCIE_CAP_MRL_SENSOR_CHANGED MRL Sensor Changed. If an MRL sensor is implemented, this bit is set when a MRL Sensor state change is detected. If an MRL sensor is not implemented, this bit must not be set.
17	RW	0x0	PCIE_CAP_POWER_FAULT_DETECTED Power Fault Detected. If a Power Controller that supports power fault detection is implemented, this bit issSet when the Power Controller detects a power fault at this slot. Note: Depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot. If power fault detection is not supported, this bit must not be set.
16	RW	0x0	PCIE_CAP_ATTENTION_BUTTON_PRESSED Attention Button Pressed. If an Attention Button is implemented, this bit is set when the attention button is pressed. If an Attention Button is not supported, this bit must not be set.
15:14	RO	0x0	RSVDP_14 Reserved for future use.
13	RO	0x0	reserved
12	RW	0x0	PCIE_CAP_DLL_STATE_CHANGED_EN Data Link Layer State Changed Enable. If the Data Link Layer Link Active Reporting capability is 1b, this bit enables software notification when Data Link Layer Link Active bit is changed. If the Data Link Layer Link Active Reporting Capable bit is 0b, this bit is permitted to be read-only with a value of 0b.
11	WO	0x0	PCIE_CAP_ELECTROMECH_INTERLOCK_CTRL Electromechanical Interlock Control. If an Electromechanical Interlock is implemented, a write of 1b to this bit causes the state of the interlock to toggle. A write of 0b to this bit has no effect. A read of this bit always returns a 0b.
10	RW	0x0	PCIE_CAP_POWER_CONTROLLER_CTRL Power Controller Control. If a Power Controller is implemented, this bit when written sets the power state of the slot per the defined encodings. Reads of this bit must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write, if required to, without waiting for the previous command to complete in which case the read value is undefined. Note: In some cases the power controller may autonomously remove slot power or not respond to a power-up request based on a detected fault condition, independent of the Power Controller Control setting. If the Power Controller Present bit in the Slot Capabilities register is clear, then writes to this bit have no effect and the read value of this bit is undefined.

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Bit	Attr	Reset Value	Description
9:8	RW	0x3	PCIE_CAP_POWER_INDICATOR_CTRL Power Indicator Control. If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting, if required to, for the previous command to complete in which case the read value is undefined. Note: The default value of this field must be one of the non-Reserved values. If the Power Indicator Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 00b.
7:6	RW	0x3	PCIE_CAP_ATTENTION_INDICATOR_CTRL Attention Indicator Control. If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting, if required to, for the previous command to complete in which case the read value is undefined. Note: The default value of this field must be one of the non-Reserved values. If the Attention Indicator Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 00b.
5	RW	0x0	PCIE_CAP_HOT_PLUG_INT_EN Hot-Plug Interrupt Enable. When set, this bit enables generation of an interrupt on enabled hot-plug events. If the Hot Plug Capable bit in the Slot Capabilities register is clear, this bit is permitted to be read-only with a value of 0b.
4	RW	0x0	PCIE_CAP_CMD_CPL_INT_EN Command Completed Interrupt Enable. If Command Completed notification is supported (if the No Command Completed Support bit in the Slot Capabilities register is 0b), when set, this bit enables software notification when a hot-plug command is completed by the Hot-Plug Controller. If Command Completed notification is not supported, the controller hardwires this bit must to 0b. Write value is gated with PCIE_CAP_NO_CMD_CPL_SUPPORT field in SLOT_CAPABILITIES_REG. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: SLOT_CAPABILITIES_REG.PCIE_CAP_NO_CMD_CPL_SUPPORT ? RO : RW
3	RW	0x0	PCIE_CAP_PRESENCE_DETECT_CHANGE_EN Presence Detect Changed Enable. When set, this bit enables software notification on a presence detect changed event (for more details, see Section 6.7.3 of PCI Express Base Specification). If the Hot-Plug Capable bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b.

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Bit	Attr	Reset Value	Description
2	RW	0x0	PCIE_CAP_MRL_SENSOR_CHANGED_EN MRL Sensor Changed Enable. When set, this bit enables software notification on a MRL sensor changed event (for more details, see Section 6.7.3 of PCI Express Base Specification). If the MRL Sensor Present bit in the Slot Capabilities register is Clear, this bit is permitted to be read-only with a value of 0b.
1	RW	0x0	PCIE_CAP_POWER_FAULT_DETECTED_EN Power Fault Detected Enable. When set, this bit enables software notification on a power fault event (for more details, see Section 6.7.3 of PCI Express Base Specification). If a Power Controller that supports power fault detection is not implemented, this bit is permitted to be read-only with a value of 0b.
0	RW	0x0	PCIE_CAP_ATTENTION_BUTTON_PRESSED_EN Attention Button Pressed Enable. When set to 1b, this bit enables software notification on an attention button pressed event (for more details, see Section 6.7.3 of PCI Express Base Specification). If the Attention Button Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b.

PCIE_DSP_PF0_PCIE_CAP_ROOT_CONTROL_ROOT_CAPABILITIES_REG

Address: Operational Base(0x00000070) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	RSVDP_17 Reserved for future use.
16	RO	0x1	PCIE_CAP_CRS_SW_VISIBILITY CRS Software Visibility Capable. When set, this bit indicates that the Root Port is capable of returning Configuration Request Retry Status (CRS) Completion Status to software (for more details, see section 2.3.1 of PCI Express Base Specification). Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W (Sticky) else R (Sticky) Note: This register field is sticky.
15:5	RO	0x000	RSVDP_5 Reserved for future use.
4	RW	0x0	PCIE_CAP_CRS_SW_VISIBILITY_EN CRS Software Visibility Enable. When set, this bit enables the Root Port to return Configuration Request Retry Status (CRS) Completion Status to software (for more details, see section 2.3.1 of PCI Express Base Specification). For Root Ports that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: ROOT_CONTROL_ROOT_CAPABILITIES_REG.PCIE_CAP_CRS_SW_VISIBILITY ? RW : RO

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Bit	Attr	Reset Value	Description
3	RW	0x0	PCIE_CAP_PME_INT_EN PME Interrupt Enable. When set, this bit enables PME interrupt generation upon receipt of a PME Message as reflected in the PME Status bit (for more details, see Table 7-29 of PCI Express Base Specification). A PME interrupt is also generated if the PME Status bit is set when this bit is changed from clear to set.
2	RW	0x0	PCIE_CAP_SYS_ERR_ON_FATAL_ERR_EN System Error on Fatal Error Enable. If set, this bit indicates that a System Error should be generated if a Fatal error (ERR_FATAL) is reported by any of the devices in the Hierarchy Domain associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system is system specific.
1	RW	0x0	PCIE_CAP_SYS_ERR_ON_NON_FATAL_ERR_EN System Error on Non-Fatal Error Enable. If set, this bit indicates that a System Error should be generated if a Non-fatal error (ERR_NONFATAL) is reported by any of the devices in the Hierarchy Domain associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system is system specific.
0	RW	0x0	PCIE_CAP_SYS_ERR_ON_CORR_ERR_EN System Error on Correctable Error Enable. If set, this bit indicates that a System Error should be generated if a correctable error (ERR_COR) is reported by any of the devices in the Hierarchy Domain associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system is system specific.

PCIE_DSP_PF0_PCIE_CAP_ROOT_STATUS_REG

Address: Operational Base(0x00000070) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	RSVDP_18 Reserved for future use.
17	RO	0x0	PCIE_CAP_PME_PENDING PME Pending. This bit indicates that another PME is pending when the PME Status bit is s et. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the PME Requester ID field appropriately. The PME Pending bit is cleared by hardware if no more PMEs are pending.
16	RW	0x0	PCIE_CAP_PME_STATUS PME Status. This bit indicates that PME was asserted by the PME Requester indicated in the PME Requester ID field. Subsequent PMEs are kept pending until the status register is cleared by software by writing a 1b.
15:0	RO	0x0000	PCIE_CAP_PME_REQ_ID PME Requester ID. This field indicates the PCI Requester ID of the last PME Requester. This field is only valid when the PME Status bit is set.

PCIE_DSP_PF0_PCIE_CAP_DEVICE_CAPABILITIES2_REG

Address: Operational Base(0x00000070) + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RO	0x00	RSVDP_24 Reserved for future use.

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Bit	Attr	Reset Value	Description
23:20	RO	0x0	reserved
19:18	RO	0x3	PCIE_CAP_OBFF_SUPPORT OBFF Supported. This field indicates if OBFF is supported and, if so, what signaling mechanism is used. The value reported in this field must indicate support for WAKE# signaling only if: - for a Downstream Port, driving the WAKE# signal for OBFF is supported and the connector or component connected Downstream is known to receive that same WAKE# signal - for an Upstream Port, receiving the WAKE# signal for OBFF is supported and, if the component is on an add-in-card, that the component is connected to the WAKE# signal on theconnector. Root Ports, Switch Ports, and Endpoints are permitted to implement this capability. For a Multi-Function Device associated with an Upstream Port, each Function must report the same value for this field. For Bridges and Ports that do not implement this capability, the controller hardwires this field to 00b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(Sticky) else R(Sticky) Note: This register field is sticky.
17	RO	0x0	PCIE_CAP2_10_BIT_TAG_REQ_SUPPORT 10-Bit Tag Requester Supported. If this bit is set, the Function supports 10-Bit Tag Requester capability; otherwise, the Function does not. This bit must not be set if the 10-Bit Tag Completer Supported bit is clear. Note: 10-Bit Tag field generation must be enabled by the 10-Bit Tag Requester Enable bit in the Device Control 2 register of the Requester Function before 10-Bit Tags can be generated by the Requester. For more details, see section 2.2.6.2. of PCI Express Base Specification.
16	RO	0x0	PCIE_CAP2_10_BIT_TAG_COMP_SUPPORT 10-Bit Tag Completer Supported. If this bit is set, the Function supports 10-Bit Tag Completer capability; otherwise, the Function does not. For more details, see section 2.2.6.2. of PCI Express Base Specification.
15:14	RO	0x0	reserved
13	RO	0x0	PCIE_CAP_TPH_CMPLT_SUPPORT_1 TPH Completer Supported Bit 1.

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Bit	Attr	Reset Value	Description
12	RO	0x0	PCIE_CAP_TPH_CMPLT_SUPPORT_0 TPH Completer Supported Bit 0. Value of this bit along with TPH Completer Supported Bit 1 indicates Completer support for TPH or Extended TPH. Applicable only to Root Ports and Endpoints. For all other Functions, this field is Reserved. For more details, see section 6.17 of PCI Express Base Specification.
11	RO	0x1	PCIE_CAP_LTR_SUPP LTR Mechanism Supported. A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism. Root Ports, Switches and Endpoints are permitted to implement this capability. For a Multi-Function Device associated with an Upstream Port, each Function must report the same value for this bit. For Bridges and other Functions that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(Sticky) else R(Sticky) Note: This register field is sticky.
10	RO	0x1	PCIE_CAP_NO_RO_EN_PR2PR_PAR No RO-enabled PR-PR Passing. If this bit is set, the routing element never carries out the passing permitted by Table 2-39 of PCI Express Base Specification entry A2b that is associated with the Relaxed Ordering Attribute field being Set. This bit applies only for Switches and RCs that support peer-to-peer traffic between Root Ports. This bit applies only to Posted Requests being forwarded through the Switch or RC and does not apply to traffic originating or terminating within the Switch or RC itself. All Ports on a Switch or RC must report the same value for this bit. For all other functions, this bit must be 0b.
9	RO	0x0	PCIE_CAP_128_CAS_CPL_SUPP 128-bit CAS Completer Supported. Applicable to Functions with Memory Space BARs as well as all Root Ports; must be 0b otherwise. This bit must be set to 1b if the Function supports this optional capability. For more details, see section 6.15 of PCI Express Base Specification.
8	RO	0x0	PCIE_CAP_64_ATOMIC_CPL_SUPP 64-bit AtomicOp Completer Supported. Applicable to Functions with Memory Space BARs as well as all Root Ports; must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability. For more details on additional RC requirements, see section 6.15.3.1 of PCI Express Base Specification.
7	RO	0x0	PCIE_CAP_32_ATOMIC_CPL_SUPP 32-bit AtomicOp Completer Supported. Applicable to Functions with Memory Space BARs as well as all Root Ports; must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability. For more details on additional RC requirements, see section 6.15.3.1 of PCI Express Base Specification.

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Bit	Attr	Reset Value	Description
6	RO	0x0	PCIE_CAP_ATOMIC_ROUTING_SUPP AtomicOp Routing Supported. Applicable only to Switch Upstream Ports, Switch Downstream Ports, and Root Ports; must be 0b for other Function types. This bit must be set to 1b if the Port supports this optional capability. For more details, see section 6.15 of PCI Express Base Specification.
5	RO	0x0	PCIE_CAP_ARI_FORWARD_SUPPORT ARI Forwarding Supported. Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. For more details, see section 6.13 of PCI Express Base Specification.
4	RO	0x1	PCIE_CAP_CPL_TIMEOUT_DISABLE_SUPPORT Completion Timeout Disable Supported. A value of 1b indicates support for the Completion Timeout Disable mechanism. The Completion Timeout Disable mechanism is required for Endpoints that issue Requests on their own behalf and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. This mechanism is optional for Root Ports. For all other Functions this field is Reserved and the controller hardwires this bit to 0b.
3:0	RO	0x0	PCIE_CAP_CPL_TIMEOUT_RANGE Completion Timeout Ranges Supported. This field indicates device Function support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is Reserved and must be hardwired to 0000b. Four time value ranges are defined: - Range A: 50 us to 10 ms - Range B: 10 ms to 250 ms - Range C: 250 ms to 4 s - Range D: 4 s to 64 s Bits are set according to the list below to show timeout value ranges supported. All encodings other than the defined encodings are reserved. It is strongly recommended that the Completion Timeout mechanism not expire in less than 10 ms.

PCIE_DSP_PF0_PCIE_CAP_DEVICE_CONTROL2_DEVICE_STATUS2_REG

Address: Operational Base(0x00000070) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
14:13	RW	0x0	PCIE_CAP_OBFF_EN OBFF Enable. This field enables the OBFF mechanism and selects the signaling method. For more details on these encodings, see section 6.19 of PCI Express Base Specification. This field is required for all Ports that support the OBFF Capability. For a Multi-Function Device associated with an Upstream Port of a Device that implements OBFF, the field in Function 0 is of type RW, and only Function 0 controls the Component's behavior. In all other Functions of that Device, this field is of type RsvdP. Ports that do not implement OBFF are permitted to hardwire this field to 00b Note: RW for function #0 and RsdvP for all other functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (pf=0 && DEVICE_CAPABILITIES2_REG.PCIE_CAP_OBFF_SUPPORT) then R/W else R
12:11	RO	0x0	reserved
10	RW	0x0	PCIE_CAP_LTR_EN LTR Mechanism Enable. When set to 1b, this bit enables Upstream Ports to send LTR messages and Downstream Ports to process LTR Messages. For a Multi-Function Device associated with an Upstream Port of a device that implements LTR, the bit in Function 0 is RW, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is RsvdP. Functions that do not implement the LTR mechanism are permitted to hardwire this bit to 0b. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. The write value is gated with the PCIE_CAP_LTR_SUPP field of DEVICE_CAPABILITIES2_REG. Note: RW for function #0 and RsdvP for all other functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (pf=0 && DEVICE_CAPABILITIES2_REG.PCIE_CAP_LTR_SUPP) then R/W else R
9:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	RO	0x0	PCIE_CAP_ARI_FORWARD_SUPPORT_CS ARI Forwarding Enable. When set, the Downstream Port disables its traditional Device Number field being 0 enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port. For more details, see Section 6.13 of PCI Express Base Specification. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
4	RW	0x0	PCIE_CAP_CPL_TIMEOUT_DISABLE Completion Timeout Disable. When set, this bit disables the Completion Timeout mechanism. This bit is required for all Functions that support the Completion Timeout Disable Capability. Functions that do not support this optional capability are permitted to hardwire this bit to 0b Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding Requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding Requests. If this is done, it is permitted to base the start time for each Request on either the time this bit was cleared or the time each Request was issued.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	PCIE_CAP_CPL_TIMEOUT_VALUE Completion Timeout Value. In device Functions that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is Reserved and controller hardwires it to 0000b. A Function that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50 us to 50 ms. Functions that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Ranges Supported field. All encodings other than the defined encodings are reserved. It is strongly recommended that the Completion Timeout mechanism not expire in less than 10 ms. Values available if Range A (50 us to 10 ms) programmability range is supported: Values available if Range B (10 ms to 250 ms) programmability range is supported: Values available if Range C (250 ms to 4 s) programmability range is supported: Values available if the Range D (4 s to 64 s) programmability range is supported: Software is permitted to change the value in this field at any time. For Requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding Requests, and is permitted to base the start time for each Request either on when this value was changed or on when each request was issued. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

PCIE_DSP_PF0_PCIE_CAP_LINK_CAPABILITIES2_REG

Address: Operational Base(0x00000070) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:25	RO	0x00	RSVDP_25 Reserved for future use.
24:23	RO	0x0	reserved
22:9	RO	0x0000	RSVDP_9 Reserved for future use.

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Bit	Attr	Reset Value	Description
8	RO	0x0	PCIE_CAP_CROSS_LINK_SUPPORT Crosslink Supported. When set to 1b, this bit indicates that the associated Port supports crosslinks (for more details, see section 4.2.6.3.1 of PCI Express Base Specification). When set to 0b on a Port that supports Link speeds of 8.0 GT/s or higher, this bit indicates that the associated Port does not support crosslinks. When set to 0b on a Port that only supports Link speeds of 2.5 GT/s or 5.0 GT/s, this bit provides no information regarding the Port's level of crosslink support. It is recommended that this bit be Set in any Port that supports crosslinks even though doing so is only required for Ports that also support operating at 8.0 GT/s or higher Link speeds. Note: Software should use this bit when referencing fields whose definition depends on whether or not the Port supports crosslinks (for more details, see section 7.7.3.4 of PCI Express Base Specification). Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions.
7:1	RO	0x07	PCIE_CAP_SUPPORT_LINK_SPEED_VECTOR Supported Link Speeds Vector. This field indicates the supported Link speed(s) of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. For more details, see section 8.2.1 of PCI Express Base Specification. Bit definitions within this field are: - Bit 0 2.5 GT/s - Bit 1 5.0 GT/s - Bit 2 8.0 GT/s - Bit 3 16.0 GT/s - Bit 4 32.0 GT/s - Bits 6:5 RsvdP Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions. This field has a default of (PCIE_CAP_MAX_LINK_SPEED == 0101) ? 0011111 : (PCIE_CAP_MAX_LINK_SPEED == 0100) ? 0001111 : (PCIE_CAP_MAX_LINK_SPEED == 0011) ? 0000111 : (PCIE_CAP_MAX_LINK_SPEED == 0010) ? 0000011 : 0000001 where PCIE_CAP_MAX_LINK_SPEED is a field in the LINK_CAPABILITIES_REG register.
0	RO	0x0	RSVDP_0 Reserved for future use.

PCIE_DSP_PF0_PCIE_CAP_LINK_CONTROL2_LINK_STATUS2_REG

Address: Operational Base(0x00000070) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:26	RO	0x0	RSVDP_26 Reserved for future use.
25:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21	RW	0x0	PCIE_CAP_LINK_EQ_REQ Link Equalization Request 8.0 GT/s. This bit is set by hardware to request the 8.0 GT/s Link equalization process to be performed on the Link. For more details, see sections 4.2.3 and 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky.
20	RO	0x0	PCIE_CAP_EQ_CPL_P3 EEqualization 8.0 GT/s Phase 3 Successful. When set to 1b, this bit indicates that Phase 3 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky.
19	RO	0x0	PCIE_CAP_EQ_CPL_P2 Equalization 8.0 GT/s Phase 2 Successful. When set to 1b, this bit indicates that Phase 2 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky.
18	RO	0x0	PCIE_CAP_EQ_CPL_P1 Equalization 8.0 GT/s Phase 1 Successful. When set to 1b, this bit indicates that Phase 1 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
17	RO	0x0	PCIE_CAP_EQ_CPL Equalization 8.0 GT/s Complete. When set to 1b, this bit indicates that the Transmitter Equalization procedure at the 8.0 GT/s data rate has completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky.
16	RO	0x1	PCIE_CAP_CURR_DEEMPHASIS Current De-emphasis Level. When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. For components that support speeds greater than 2.5 GT/s, Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions of the Port. In M-PCIe mode this register is always 0x0. In C-PCIe mode, its contents are derived by sampling the PIPE.
15:12	RW	0x0	PCIE_CAP_COMPLIANCE_PRESET Compliance Preset/De-emphasis. - For 8.0 GT/s and higher Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. The encodings are defined in section 4.2.3.2 of PCI Express Base Specification . Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. - For 5.0 GT/s Data Rate: This field sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. - When the Link is operating at 2.5 GT/s, the setting of this field has no effect. Components that support only 2.5 GT/s speed are permitted to hardwire this field to 0000b. - For a Multi-Function Device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. - This field is intended for debug and compliance testing purposes. System firmware and software is allowed to modify this field only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
11	RW	0x0	PCIE_CAP_COMPLIANCE_SOS Compliance SOS. When set to 1b, the LTSSM is required to send SKP Ordered Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only. For components that support only the 2.5 GT/s speed, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
10	RW	0x0	PCIE_CAP_ENTER_MODIFIED_COMPLIANCE Enter Modified Compliance. When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
9:7	RW	0x0	PCIE_CAP_TX_MARGIN Transmit Margin, This field controls the value of the non-deemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see Chapter 4 of PCI Express Base Specification for details of how the Transmitter voltage level is determined in various states). - 001b-111b: As defined in Section 8.3.4 not all encodings are required to be implemented. For a Multi-Function Device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. For components that support only the 2.5 GT/s speed, the controller hardwires this bit to 000b. This field is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this field only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value. Note: This register field is sticky.
6	RO	0x0	PCIE_CAP_SEL_DEEMPHASIS Selectable De-emphasis. When the Link is operating at 5.0 GT/s speed, this bit is used to control the transmit de-emphasis of the link in specific situations. For more details, see section 4.2.6 of PCI Express Base Specification. When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. This bit is not applicable and Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
5	RW	0x0	PCIE_CAP_HW_AUTO_SPEED_DISABLE Hardware Autonomous Speed Disable. When set, this bit disables hardware from changing the Link speed for device-specific reasons other than attempting to correct unreliable Link operation by reducing Link speed. Initial transition to the highest supported common link speed is not blocked by this bit. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
4	RW	0x0	PCIE_CAP_ENTER_COMPLIANCE Enter Compliance. Software is permitted to force a Link to enter Compliance mode (at the speed indicated in the Target Link Speed field and the de-emphasis/preset level indicated by the Compliance Preset/De-emphasis field) by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
3:0	RW	0x3	PCIE_CAP_TARGET_LINK_SPEED Target Link Speed. For Downstream Ports, this field sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the desired target Link speed. All encodings other than the defined encodings are reserved. If a value is written to this field that does not correspond to a supported speed (as indicated by the Supported Link Speeds Vector), the result is undefined. If either of the Enter Compliance or Enter Modified Compliance bits are implemented, then this field must also be implemented. The default value of this field is the highest Link speed supported by the component (as reported in the Max Link Speed field of the Link Capabilities register) unless the corresponding platform/form factor requires a different default value. For both Upstream and Downstream Ports, this field is used to set the target compliance mode speed when software is using the Enter Compliance bit to force a Link into compliance mode. For Upstream Ports, if the Enter Compliance bit is Clear, this field is permitted to have no effect. For a Multi-Function Device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Components that support only the 2.5 GT/s speed are permitted to hardwire this field to 0000b. In M-PCIe mode, the contents of this field are derived from other registers. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

14.4.3.5 PCIE_DSP_PF0_PCIE_CAP Register Description

14.4.3.5.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PCIE_CAP_PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP_REG	0x0000	W	0x0042B010	This is the PCI Express Capabilities, ID, and Next Pointer Register.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PCIE_CAP_DEVICE_CAPABILITIES_REG	0x0004	W	0x00008000	The Device Capabilities register identifies PCI Express device function specific capabilities.
PCIE_DSP_PF0_PCIE_CAP_DEVICE_CONTROL_DEVICE_STATUS	0x0008	W	0x00102010	This register controls PCI Express device specific parameters and provides information about PCI Express device (function) specific parameters.
PCIE_DSP_PF0_PCIE_CAP_LINK_CAPABILITIES_REG	0x000C	W	0x0072AC13	The Link Capabilities register identifies PCI Express Link specific capabilities.
PCIE_DSP_PF0_PCIE_CAP_LINK_CONTROL_LINK_STATUS_REG	0x0010	W	0x10110000	This register controls and provides information about PCI Express Link specific parameters.
PCIE_DSP_PF0_PCIE_CAP_SLOT_CAPABILITIES_REG	0x0014	W	0x00000000	The Slot Capabilities register identifies PCI Express slot specific capabilities.
PCIE_DSP_PF0_PCIE_CAP_SLOT_CONTROL_SLOT_STATUS	0x0018	W	0x004003C0	This register controls and provides information about PCI Express Slot specific parameters.
PCIE_DSP_PF0_PCIE_CAP_ROOT_CONTROL_ROOT_CAPABILITIES_REG	0x001C	W	0x00010000	This register controls PCI Express Root Complex specific parameters and identifies PCI Express Root Port specific capabilities.
PCIE_DSP_PF0_PCIE_CAP_ROOT_STATUS_REG	0x0020	W	0x00000000	The Root Status register provides information about PCI Express device specific parameters.
PCIE_DSP_PF0_PCIE_CAP_DEVICE_CAPABILITIES2_REG	0x0024	W	0x000C0C10	This register identifies PCI Express device specific capabilities; in addition to the Device Capabilities Register.
PCIE_DSP_PF0_PCIE_CAP_DEVICE_CONTROL2_DEVICE_STATUS2_REG	0x0028	W	0x00000000	This register controls PCI Express device specific parameters and provides information about PCI Express device (function) specific parameters; in addition to the Device Control and Device Status Register.
PCIE_DSP_PF0_PCIE_CAP_LINK_CAPABILITIES2_REG	0x002C	W	0x0000000E	This register identifies PCI Express Link specific capabilities; in addition to the Link Capabilities Register.
PCIE_DSP_PF0_PCIE_CAP_LINK_CONTROL2_LINK_STATUS2_REG	0x0030	W	0x00010003	This register controls and provides information about PCI Express Link specific parameters; in addition to the Link Control and Link Status Register.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3.5.2 Detail Registers Description

PCIE_DSP_PF0_PCIE_CAP_PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP_REG

Address: Operational Base(0x00000070) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	RSVDP_31 Reserved for future use.

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Bit	Attr	Reset Value	Description
30	RO	0x0	RSVD Reserved.
29:25	RO	0x00	PCIE_INT_MSG_NUM PCIE Interrupt Message Number. Interrupt Message Number. This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability structure. For MSI, the value in this field indicates the offset between the base Message Data and the interrupt message that is generated. Hardware is required to update this field so that it is correct if the number of MSI Messages assigned to the Function changes when software writes to the Multiple Message Enable field in the MSI Message Control register. For MSI-X, the value in this field indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant. If both MSI and MSI-X are implemented, they are permitted to use different vectors, though software is permitted to enable only one mechanism at a time. If MSI-X is enabled, the value in this field must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this field must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this field is undefined. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
24	RO	0x0	PCIE_SLOT_IMP Slot Implemented. When set, this bit indicates that the Link associated with this Port is connected to a slot (as compared to being connected to a system-integrated device or being disabled). This bit is valid for Downstream Ports. This bit is undefined for Upstream Ports. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

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Bit	Attr	Reset Value	Description
23:20	RO	0x4	PCIE_DEV_PORT_TYPE Device/Port Type. Indicates the specific type of this PCI Express function. Note: Different functions in a Multi-Function Device can generally be of different types. Defined encodings for functions that implement a Type 00h PCI Configuration Space header are: Defined encodings for functions that implement a Type 01h PCI Configuration Space header are: All other encodings are Reserved. Note: Different Endpoint types have notably different requirements in Section 1.3.2 of PCI Express Base Specification regarding I/O resources, Extended Configuration Space, and other capabilities.
19:16	RO	0x2	PCIE_CAP_REG Capability Version. Indicates PCI-SIG defined PCI Express Capability structure version number. A version of the specification that changes the PCI Express Capability structure in a way that is not otherwise identifiable (for example, through a new Capability field) is permitted to increment this field. All such changes to the PCI Express Capability structure must be software-compatible. Software must check for Capability Version numbers that are greater than or equal to the highest number defined when the software is written, as functions reporting any such Capability Version numbers will contain a PCI Express Capability structure that is compatible with that piece of software. The controller hardwires this field to 2h for functions compliant to PCI Express Base Specification, Revision 4.0, Version 1.0. Note: This register field is sticky.
15:8	RO	0xb0	PCIE_CAP_NEXT_PTR Next Capability Pointer. This field contains the offset to the next PCI Capability structure or 00h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
7:0	RO	0x10	PCIE_CAP_ID Capability ID. Indicates the PCI Express Capability structure. This field must return a Capability ID of 10h indicating that this is a PCI Express Capability structure.

PCIE_DSP_PF0_PCIE_CAP_DEVICE_CAPABILITIES_REG

Address: Operational Base(0x00000070) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	RSVDP_16 Reserved for future use.

Bit	Attr	Reset Value	Description
15	RO	0x1	PCIE_CAP_ROLE_BASED_ERR_REPORT Role-Based Error Reporting. When set, this bit indicates that the function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be set by all functions conforming to the ECN, PCI Express Base Specification, Revision 1.1., or subsequent PCI Express Base Specification revisions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
14:6	RO	0x000	RSVDP_6 Reserved for future use.
5	RO	0x0	PCIE_CAP_EXT_TAG_SUPP Extended Tag Field Supported. This bit, in combination with the 10-Bit Tag Requester Supported bit in the Device Capabilities 2 register, indicates the maximum supported size of the Tag field as a Requester. This bit must be set if the 10-Bit Tag Requester Supported bit is set. Note: 8-bit Tag field generation must be enabled by the Extended Tag Field Enable bit in the Device Control register of the Requester Function before 8-bit Tags can be generated by the Requester. See Section 2.2.6.2 of PCI Express Base Specification for interactions with enabling the use of 10-Bit Tags. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
4:3	RO	0x0	PCIE_CAP_PHANTOM_FUNC_SUPPORT Phantom Functions Supported. This field indicates the support for use of unclaimed function numbers to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers (called Phantom Functions) with the Tag identifier (see Section 2.2.6.2 of PCI Express Base Specification for a description of Tag Extensions). With every Function in an ARI Device, the Phantom Functions Supported field must be set to 00b. The remainder of this field description applies only to non-ARI Multi-Function Devices. This field indicates the number of most significant bits of the Function Number portion of Requester ID that are logically combined with the Tag identifier. Note: Phantom Function support for the function must be enabled by the Phantom Functions Enable field in the Device Control register before the Function is permitted to use the Function Number field in the Requester ID for Phantom Functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

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Bit	Attr	Reset Value	Description
			Note: This register field is sticky.
2:0	RO	0x0	PCIE_CAP_MAX_PAYLOAD_SIZE Max_Payload_Size Supported. This field indicates the maximum payload size that the function can support for TLPs. All encodings other than the defined encodings are reserved. The functions of a Multi-Function Device are permitted to report different values for this field. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

PCIE_DSP_PF0_PCIE_CAP_DEVICE_CONTROL_DEVICE_STATUS

Address: Operational Base(0x00000070) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	RSVDP_22 Reserved for future use.
21	RO	0x0	PCIE_CAP_TRANS_PENDING Transactions Pending. Root and Switch Ports: The controller hardwires this bit to 0b.
20	RO	0x1	PCIE_CAP_AUX_POWER_DETECTED AUX Power Detected. Functions that require Aux power report this bit as set if Aux power is detected by the function. This bit is derived by sampling the sys_aux_pwr_det input.
19	RW	0x0	PCIE_CAP_UNSUPPORTED_REQ_DETECTED Unsupported Request Detected. This bit indicates that the function received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function Device, each function indicates status of errors as perceived by the respective function.
18	RW	0x0	PCIE_CAP_FATAL_ERR_DETECTED Fatal Error Detected. This bit indicates status of Fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function device, each function indicates status of errors as perceived by the respective Function. For Functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register.

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Bit	Attr	Reset Value	Description
17	RW	0x0	PCIE_CAP_NON_FATAL_ERR_DETECTED Non-Fatal Error Detected. This bit indicates status of Non-fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function device, each function indicates status of errors as perceived by the respective Function. For functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register.
16	RW	0x0	PCIE_CAP_CORR_ERR_DETECTED Correctable Error Detected. This bit indicates status of correctable errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function device, each function indicates status of errors as perceived by the respective function. For functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Correctable Error Mask register.
15	RO	0x0	reserved
14:12	RW	0x2	PCIE_CAP_MAX_READ_REQ_SIZE Max_Read_Request_Size. This field sets the maximum Read Request size for the function as a Requester. The function must not generate Read Requests with a size exceeding the set value. For functions that do not generate Read Requests larger than 128 bytes and functions that do not generate Read Requests on their own behalf, the controller implements this field as Read Only (RO) with a value of 000b.
11	RO	0x0	PCIE_CAP_EN_NO_SNOOP Enable No Snoop. If this bit is set, the function is permitted to Set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency (see section 2.2.6.5 in PCI Express Base Specification). Note: Setting this bit to 1b should not cause a function to set the No Snoop attribute on all transactions that it initiates. Even when this bit is set, a function is only permitted to set the No Snoop attribute on a transaction when it can guarantee that the address of the transaction is not stored in any cache in the system. The controller hardwires this bit 0b if a function would never set the No Snoop attribute in transactions it initiates. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R

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Bit	Attr	Reset Value	Description
10	RW	0x0	PCIE_CAP_AUX_POWER_PM_EN Aux Power PM Enable. This bit is derived by sampling the sys_aux_pwr_det input. When set this bit, enables a function to draw Aux power independent of PME Aux power. Functions that require Aux power on legacy operating systems should continue to indicate PME Aux power requirements. Aux power is allocated as requested in the Aux_Current field of the Power Management Capabilities register (PMC), independent of the PME_En bit in the Power Management Control/Status register (PMCSR). For Multi-Function devices, a component is allowed to draw Aux power if at least one of the functions has this bit set. Note: Functions that consume Aux power must preserve the value of this sticky register when Aux power is available. In such functions, this bit is not modified by Conventional Reset. For functions that do not implement this capability, the controller hardwires this bit to 0b. Note: This register field is sticky.
9	RO	0x0	PCIE_CAP_PHANTOM_FUNC_EN Phantom Functions Enable. This bit, in combination with the 10-Bit Tag Requester Enable bit in the Device Control 2 register, determines how many Tag field bits a Requester is permitted to use. When the 10-Bit Tag Requester Enable bit is clear, - If this bit is set, it enables a function to use unclaimed functions as Phantom functions to extend the number of outstanding transaction identifiers - If this bit is clear, the function is not allowed to use Phantom functions For more details, see section 2.2.6.2 of PCI Express Base Specification. Software should not change the value of this bit while the function has outstanding Non-Posted Requests; otherwise, the result is undefined. For functions that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: DEVICE_CAPABILITIES_REG.PCIE_CAP_PHANTOM_FUNC_SUPPORT ? RW : RO

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Bit	Attr	Reset Value	Description
8	RO	0x0	PCIE_CAP_EXT_TAG_EN Extended Tag Field Enable. This bit, in combination with the 10-Bit Tag Requester Enable bit in the Device Control 2 register, determines how many Tag field bits a Requester is permitted to use. When the 10-Bit Tag Requester Enable bit is clear, - If the Extended Tag Field Enable bit is set, the function is permitted to use an 8-bit Tag field as a Requester - If the Extended Tag Field Enable bit is clear, the Function is restricted to a 5-bit Tag field See section 2.2.6.2 of PCI Express Base Specification for required behavior when the 10-Bit Tag Requester Enable bit is set. If software changes the value of the Extended Tag Field Enable bit while the function has outstanding Non-Posted Requests, the result is undefined. For functions that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: DEVICE_CAPABILITIES_REG.PCIE_CAP_EXT_TAG_SUPP ? RW : RO
7:5	RW	0x0	PCIE_CAP_MAX_PAYLOAD_SIZE_CS Max_Payload_Size. This field sets maximum TLP payload size for the Function. As a Receiver, the Function must handle TLPs as large as the set value. As a Transmitter, the Function must not generate TLPs exceeding the set value. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported field (PCIE_CAP_MAX_PAYLOAD_SIZE) in the Device Capabilities (DEVICE_CAPABILITIES_REG) register (for more details, see section 7.5.3.3 of PCI Express Base Specification). This field sets the maximum Read Request size for the function as a Requester. The function must not generate Read Requests with a size exceeding the set value. For Functions that support only the 128-byte max payload size, the controller hardwires this field to 000b. System software is not required to program the same value for this field for all the Functions of a Multi-Function device (for more details, see section 2.2.2 of PCI Express Base Specification). For ARI Devices, Max_Payload_Size is determined solely by the setting in Function0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

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Bit	Attr	Reset Value	Description
4	RW	0x1	PCIE_CAP_EN_REL_ORDER Enable Relaxed Ordering. If this bit is set, the function is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering (for more details, see section 2.2.6.4 and section 2.4 of PCI Express Base Specification). For a function that never sets the Relaxed Ordering attribute in transactions it initiates as a Requester, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
3	RW	0x0	PCIE_CAP_UNSUPPORT_REQ_REP_EN Unsupported Request Reporting Enable. This bit, in conjunction with other bits, controls the signaling of Unsupported Request Errors by sending error Messages (for more details, see section 6.2.5 and section 6.2.6 of PCI Express Base Specification). For a Multi-Function Device, this bit controls error reporting for each Function from point-of-view of the respective Function.
2	RW	0x0	PCIE_CAP_FATAL_ERR_REPORT_EN Fatal Error Reporting Enable. This bit, in conjunction with other bits, controls sending ERR_FATAL Messages (for more details, see section 6.2.5 and section 6.2.6 of of PCI Express Base Specification). For a Multi-Function device, this bit controls error reporting for each function from point-of-view of the respective function. For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL Message is generated.
1	RW	0x0	PCIE_CAP_NON_FATAL_ERR_REPORT_EN Non-Fatal Error Reporting Enable. This bit, in conjunction with other bits, controls sending ERR_NONFATAL Messages (for more details, see section 6.2.5 and Section 6.2.6 of PCI Express Base Specification). For a Multi-Function Device, this bit controls error reporting for each function from point-of-view of the respective Function. For a Root Port, the reporting of Non-fatal errors is internal to the root. No external ERR_NONFATAL Message is generated.
0	RW	0x0	PCIE_CAP_CORR_ERR_REPORT_EN Correctable Error Reporting Enable. This bit, in conjunction with other bits, controls sending ERR_COR Messages (for more details, see section 6.2.5, section 6.2.6, and section 6.2.10.2 of PCI Express Base Specification). For a Multi-Function device, this bit controls error reporting for each function from point-of-view of the respective function. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR Message is generated.

PCIE_DSP_PF0_PCIE_CAP_LINK_CAPABILITIES_REG

Address: Operational Base(0x00000070) + offset (0x000C)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	PCIE_CAP_PORT_NUM Port Number. This field indicates the PCI Express Port number for the given PCI Express Link. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
23	RO	0x0	RSVDP_23 Reserved for future use.
22	RO	0x1	PCIE_CAP_ASPM_OPT_COMPLIANCE ASPM Optionality Compliance. This field must be set to 1b in all functions. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
21	RO	0x1	PCIE_CAP_LINK_BW_NOT_CAP Link Bandwidth Notification Capability. A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. This capability is required for all Root Ports and Switch Downstream Ports supporting Links wider than x1 and/or multiple Link speeds. This field is not applicable and is Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
20	RO	0x1	PCIE_CAP_DLL_ACTIVE_REP_CAP Data Link Layer Link Active Reporting Capable. For a Downstream Port, the controller hardwires this bit to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port (as indicated by the Hot-Plug Capable bit of the Slot Capabilities register) or a Downstream Port that supports Link speeds greater than 5.0 GT/s, the controller hardwires this bit to 1b. For Upstream Ports and components that do not support this optional capability, the controller hardwires this bit to 0b.

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Bit	Attr	Reset Value	Description
19	RO	0x0	PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP Surprise Down Error Reporting Capable. For a Downstream Port, this bit must be set if the component supports the optional capability of detecting and reporting a Surprise Down error condition. For Upstream Ports and components that do not support this optional capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
18	RO	0x0	PCIE_CAP_CLOCK_POWER_MAN Clock Power Management. For Upstream Ports, a value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) via the "clock request" (CLKREQ#) mechanism when the Link is in the L1 and L2/L3 Ready Link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these Link states. L1 PM Substates defines other semantics for the CLKREQ# signal, which are managed independently of Clock Power Management. This Capability is applicable only in form factors that support "clock request" (CLKREQ#) capability. For a Multi-Function device associated with an Upstream Port, each Function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the Multi-Function device indicate a 1b in this bit. For ARI Devices, all Functions must indicate the same value in this bit. For Downstream Ports, the controller hardwires this bit to 0b. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
17:15	RO	0x5	PCIE_CAP_L1_EXIT_LATENCY L1 Exit Latency. This field indicates the L1 exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from ASPM L1 to L0. If ASPM L1 is not supported, the value is undefined. Note: Exit latencies may be influenced by PCI Express reference clock configuration depending upon whether a component uses a common or separate reference clock. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. There are two each of these register fields, this one and a shadow one at the same address. The Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG) determines which one is used by the controller and which one is accessed by a read request. Common Clock operation is supported (possible) in the controller when one or more of the following expressions is true: - CX_NFTS !=CX_COMM_NFTS - DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY - DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Common Clock operation is enabled in the controller when you set the Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG). The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the shadow field at this location. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
14:12	RO	0x2	PCIE_CAP_L0S_EXIT_LATENCY L0s Exit Latency. This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0. If L0s is not supported, the value is undefined; however, see the Implementation Note "Potential Issues With Legacy Software When L0s is Not Supported" in section 5.4.1.1 of PCI Express Base Specification for the recommended value. Note: Exit latencies may be influenced by PCI Express reference clock configuration depending upon whether a component uses a common or separate reference clock. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. There are two each of these register fields, this one and a shadow one at the same address. The Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG) determines which one is used by the controller and which one is accessed by a read request. Common Clock operation is supported (possible) in the controller when one or more of the following expressions is true: - CX_NFTS !=CX_COMM_NFTS - DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY - DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Common Clock operation is enabled in the controller when you set the Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG). The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the shadow field at this location. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
11:10	RO	0x3	PCIE_CAP_ACTIVE_STATE_LINK_PM_SUPPORT Active State Power Management (ASPM) Support. This field indicates the level of ASPM supported on the given PCI Express Link. For more details on ASPM support requirements, see section 5.4.1 of PCI Express Base Specification. Multi-Function devices associated with an Upstream Port must report the same value in this field for all functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
9:4	RO	0x01	PCIE_CAP_MAX_LINK_WIDTH Maximum Link Width. This field indicates the maximum Link width (xN - corresponding to N Lanes) implemented by the component. This value is permitted to exceed the number of Lanes routed to the slot (Downstream Port), adapter connector (Upstream Port), or in the case of component-to-component connections, the actual wired connection width. All encodings other than the defined encodings are reserved. Multi-Function devices associated with an Upstream Port must report the same value in this field for all functions. In M-PCIe mode, the reset and dynamic values of this field are calculated by the controller. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
3:0	RO	0x3	PCIE_CAP_MAX_LINK_SPEED Max Link Speed. This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. All encodings other than the defined encodings are reserved. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. In M-PCIe mode, the reset and dynamic values of this field are calculated by the controller. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

PCIE_DSP_PF0_PCIE_CAP_LINK_CONTROL_LINK_STATUS_REG

Address: Operational Base(0x00000070) + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	PCIE_CAP_LINK_AUTO_BW_STATUS Link Autonomous Bandwidth Status. This bit is set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG.

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Bit	Attr	Reset Value	Description
			This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b.
30	RW	0x0	PCIE_CAP_LINK_BW_MAN_STATUS Link Bandwidth Management Status. This bit is set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit. Note: This bit is set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. The default value of this bit is 0b. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG.
29	RO	0x0	PCIE_CAP_DLL_ACTIVE Data Link Layer Link Active. This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. This bit must be implemented if the Data Link Layer Link Active Reporting Capable bit is 1b. Otherwise, the controller hardwires it to 0b.
28	RO	0x1	PCIE_CAP_SLOT_CLK_CONFIG Slot Clock Configuration. This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference clock on the connector, this bit must be clear. For a Multi-Function Device, each Function must report the same value for this bit. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

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Bit	Attr	Reset Value	Description
27	RO	0x0	PCIE_CAP_LINK_TRAINING Link Training. This read-only bit indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state. This bit is not applicable and Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches, and the controller hardwires it to 0b.
26	RO	0x0	RSVDP_26 Reserved for future use.
25:20	RO	0x01	PCIE_CAP_NEGO_LINK_WIDTH Negotiated Link Width. This field indicates the negotiated width of the given PCI Express Link. All encodings other than the defined encodings are reserved. The value in this field is undefined when the Link is not up.
19:16	RO	0x1	PCIE_CAP_LINK_SPEED Current Link Speed. This field indicates the negotiated Link speed of the given PCI Express Link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. All encodings other than the defined encodings are reserved. The value in this field is undefined when the Link is not up.
15:14	RW	0x0	PCIE_CAP_DRS_SIGNALING_CONTROL DRS Signaling Control. Indicates the mechanism used to report reception of a DRS message. Must be implemented for Downstream Ports with the DRS Supported bit Set in the Link Capabilities 2 Register. Encodings are: If DRS Supported is set, receiving a DRS Message will set DRS Message Received in the Link Status 2 Register but will otherwise have no effect If the DRS Message Received bit in the Link Status 2 Register transitions from 0 to 1, and either MSI or MSI-X is enabled, an MSI or MSI-X interrupt is generated using the vector in Interrupt Message Number (section 7.5.3.2) If the DRS Message Received bit in the Link Status 2 Register transitions from 0 to 1, the Port must send an FRS Message Upstream with the FRS Reason field set to DRS Message Received. Behavior is undefined if this field is set to 10b and the FRS Supported bit in the Device Capabilities 2 Register is Clear. Behavior is undefined if this field is set to 11b. For Downstream Ports with the DRS Supported bit clear in the Link Capabilities 2 register, the controller hardwires this field to 00b. This field is Reserved for Upstream Ports. Note: The access attributes of this field are as follows:

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Bit	Attr	Reset Value	Description
			- Wire: No access. - Dbi: LINK_CAPABILITIES2_REG.DRS_SUPPORTED ? RW : RO
13:12	RO	0x0	RSVDP_12 Reserved for future use.
11	RW	0x0	PCIE_CAP_LINK_AUTO_BW_INT_EN Link Autonomous Bandwidth Management Interrupt Enable. When set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been set. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_LINK_BW_NOT_CAP ? RW : RO
10	RW	0x0	PCIE_CAP_LINK_BW_MAN_INT_EN Link Bandwidth Management Interrupt Enable. When set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been set. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_LINK_BW_NOT_CAP ? RW : RO

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Bit	Attr	Reset Value	Description
9	RW	0x0	PCIE_CAP_HW_AUTO_WIDTH_DISABLE Hardware Autonomous Width Disable. When set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RW, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. For components that do not implement the ability autonomously to change Link width, the ciontroller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
8	RW	0x0	PCIE_CAP_EN_CLK_POWER_MAN Enable Clock Power Management. Applicable only for Upstream Ports and with form factors that support a "Clock Request" (CLKREQ#) mechanism, this bit operates as follows: For a non-ARI Multi-Function Device, power-management-configuration software must only Set this bit if all Functions of the Multi-Function Device indicate a 1b in the Clock Power Management bit of the Link Capabilities register. The component is permitted to use the CLKREQ# signal to power manage Link clock only if this bit is Set for all Functions. For ARI Devices, Clock Power Management is enabled solely by the setting in Function 0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. The CLKREQ# signal may also be controlled via the L1 PM Substates mechanism. Such control is not affected by the setting of this bit. For Downstream Ports and components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities register), the controller hardwires this bit to 0b. The write value is gated with the PCIE_CAP_CLOCK_POWER_MAN field in LINK_CAPABILITIES_REG. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_CLOCK_POWER_MAN ? RWS : ROS Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
7	RW	0x0	PCIE_CAP_EXTENDED_SYNCH Extended Synch. When set, this bit forces the transmission of additional Ordered Sets when exiting the L0s state (see section 4.2.4.5 of PCI Express Base Specification) and when in the Recovery state (see section 4.2.6.4.1 of PCI Express Base Specification). This mode provides external devices (for example, logic analyzers) monitoring the Link time to achieve bit and Symbol lock before the Link enters the L0 state and resumes communication. For Multi-Function devices if any function has this bit set, then the component must transmit the additional Ordered Sets when exiting L0s or when in Recovery.
6	RW	0x0	PCIE_CAP_COMMON_CLK_CONFIG Common Clock Configuration. When set, this bit indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. A value of 0b indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. For non-ARI Multi-Function Devices, software must program the same value for this bit in all Functions. If not all Functions are Set, then the component must as a whole assume that its reference clock is not common with the Upstream component. For ARI Devices, Common Clock Configuration is determined solely by the setting in Function 0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Components utilize this common clock configuration information to report the correct L0s and L1 Exit Latencies. After changing the value in this bit in both components on a Link, software must trigger the Link to retrain by writing a 1b to the Retrain Link bit of the Downstream Port.
5	RW	0x0	PCIE_CAP_RETRAIN_LINK Retrain Link. A write of 1b to this bit initiates Link retraining by directing the Physical Layer LTSSM to the Recovery state. If the LTSSM is already in Recovery or Configuration, re-entering Recovery is permitted but not required. If the Port is in DPC when a write of 1b to this bit occurs, the result is undefined. Reads of this bit always return 0b. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress. This bit is not applicable and is Reserved for Endpoints, PCI

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Bit	Attr	Reset Value	Description
			Express to PCI/PCI-X bridges, and Upstream Ports of Switches. This bit always returns 0b when read. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: see description
4	RW	0x0	PCIE_CAP_LINK_DISABLE Link Disable. This bit disables the Link by directing the LTSSM to the Disabled state when set; this bit is Reserved on Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state. After clearing this bit, software must honor timing requirements defined in Section 6.6.1 with respect to the first Configuration Read following a Conventional Reset. In a DSP that supports crosslink, the controller gates the write value with the CROSS_LINK_EN field in PORT_LINK_CTRL_OFF. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: CX_CROSSLINK_ENABLE=1 && PORT_LINK_CTRL_OFF.CROSS_LINK_EN=1||CX_CROSSLINK_ENABLE=0 && dsp=1? RW : RO
3	RO	0x0	PCIE_CAP_RCB Read Completion Boundary (RCB). Root Ports: Indicates the RCB value for the Root Port. Refer to section 2.3.1.1 of PCI Express Base Specification for the definition of the parameter RCB. The controller hardwires this bit for a Root Port and returns its RCB support capabilities. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
2	RO	0x0	RSVDP_2 Reserved for future use.

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	PCIE_CAP_ACTIVE_STATE_LINK_PM_CONTROL Active State Power Management (ASPM) Control. This field controls the level of ASPM enabled on the given PCI Express Link. See section 5.4.1.3 of PCI Express Base Specification for requirements on when and how to enable ASPM. Note: "L0s Entry Enabled" enables the Transmitter to enter L0s. If L0s is supported, the Receiver must be capable of entering L0s even when the Transmitter is disabled from entering L0s (00b or 10b). ASPM L1 must be enabled by software in the Upstream component on a Link prior to enabling ASPM L1 in the Downstream component on that Link. When disabling ASPM L1, software must disable ASPM L1 in the Downstream component on a Link prior to disabling ASPM L1 in the Upstream component on that Link. ASPM L1 must only be enabled on the Downstream component if both components on a Link support ASPM L1. For Multi-Function Devices (including ARI Devices), it is recommended that software program the same value for this field in all Functions. For non-ARI Multi-Function Devices, only capabilities enabled in all Functions are enabled for the component as a whole. For ARI Devices, ASPM Control is determined solely by the setting in Function0, regardless of Function 0's D-state. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Software must not enable L0s in either direction on a given Link unless components on both sides of the Link each support L0s; otherwise, the result is undefined.

PCIE_DSP_PF0_PCIE_CAP_SLOT_CAPABILITIES_REG

Address: Operational Base(0x00000070) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	PCIE_CAP_PHY_SLOT_NUM Physical Slot Number. This field indicates the physical slot number attached to this Port. This field must be hardware initialized to a value that assigns a slot number that is unique within the chassis, regardless of the form factor associated with the slot. This field must be initialized to zero for Ports connected to devices that are either integrated on the system board or integrated within the same silicon as the Switch device or Root Port. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

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Bit	Attr	Reset Value	Description
18	RO	0x0	PCIE_CAP_NO_CMD_CPL_SUPPORT No Command Completed Support. When set, this bit indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller. This bit is only permitted to be set if the hot-plug capable Port is able to accept writes to all fields of the Slot Control register without delay between successive writes. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
17	RO	0x0	PCIE_CAP_ELECTROMECH_INTERLOCK Electromechanical Interlock Present. When set, this bit indicates that an Electromechanical Interlock is implemented on the chassis for this slot. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
16:15	RO	0x0	PCIE_CAP_SLOT_POWER_LIMIT_SCALE Slot Power Limit Scale. Specifies the scale used for the Slot Power Limit Value (for more details, see Section 6.9 of PCI Express Base Specification). This register must be implemented if the Slot Implemented bit is set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 00b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
14:7	RO	0x00	PCIE_CAP_SLOT_POWER_LIMIT_VALUE Slot Power Limit Value. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by the slot (for more detais, see Section 6.9 of PCI Express Base Specification) or by other means to the adapter. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field except when the Slot Power Limit Scale field equals 00b (1.0x) and Slot Power Limit Value exceeds EFh, the alternative encodings defined in Values: are used. Value F3h to FFh are Reserved for Slot Power Limit values above 300 W. This register must be implemented if the Slot Implemented bit is set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 0000 0000b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

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Bit	Attr	Reset Value	Description
6	RO	0x0	PCIE_CAP_HOT_PLUG_CAPABLE Hot-Plug Capable. When set, this bit indicates that this slot is capable of supporting hot-plug operations. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
5	RO	0x0	PCIE_CAP_HOT_PLUG_SURPRISE Hot-Plug Surprise. When set, this bit indicates that an adapter present in this slot might be removed from the system without any prior notification. This is a form factor specific capability. This bit is an indication to the operating system to allow for such removal without impacting continued software operation. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
4	RO	0x0	PCIE_CAP_POWER_INDICATOR Power Indicator Present. When set, this bit indicates that a Power Indicator is electrically controlled by the chassis for this slot. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
3	RO	0x0	PCIE_CAP_ATTENTION_INDICATOR Attention Indicator Present. When set, this bit indicates that an Attention Indicator is electrically controlled by the chassis. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
2	RO	0x0	PCIE_CAP_MRL_SENSOR MRL Sensor Present. When set, this bit indicates that an MRL Sensor is implemented on the chassis for this slot. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
1	RO	0x0	PCIE_CAP_POWER_CONTROLLER Power Controller Present. When set, this bit indicates that a software programmable Power Controller is implemented for this slot/adapter (depending on form factor). Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
0	RO	0x0	PCIE_CAP_ATTENTION_INDICATOR_BUTTON Attention Button Present. When set, this bit indicates that an Attention Button for this slot is electrically controlled by the chassis. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

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PCIE_DSP_PF0_PCIE_CAP_SLOT_CONTROL_SLOT_STATUS

Address: Operational Base(0x00000070) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	RSVDP_25 Reserved for future use.
24	RW	0x0	PCIE_CAP_DLL_STATE_CHANGED Data Link Layer State Changed. This bit is set when the value reported in the Data Link Layer Link Active bit of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read the Data Link Layer Link Active bit of the Link Status register to determine if the Link is active before initiating configuration cycles to the hot plugged device.
23	RO	0x0	PCIE_CAP_ELECTROMECH_INTERLOCK_STATUS Electromechanical Interlock Status. If an Electromechanical Interlock is implemented, this bit indicates the status of the Electromechanical Interlock.
22	RO	0x1	PCIE_CAP_PRESENCE_DETECT_STATE Presence Detect State. This bit indicates the presence of an adapter in the slot, reflected by the logical "OR" of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. Note that the in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected. Consequently, form factors that require a power controller for hot-plug must implement a physical pin presence detect mechanism. This bit must be implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities register is 0b), the controller hardwires this bit to 1b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
21	RO	0x0	PCIE_CAP_MRL_SENSOR_STATE MRL Sensor State. This bit reports the status of the MRL sensor if implemented. Encodings are define as above.
20	RW	0x0	PCIE_CAP_CMD_CPLD Command Completed. If Command Completed notification is supported (if the No Command Completed Support bit in the Slot Capabilities register is 0b), this bit is set when a hot-plug command has completed and the Hot-Plug Controller is ready to accept a subsequent command. The Command Completed status bit is set as an indication to host software that the Hot-Plug Controller has processed the previous command and is ready to receive the next command; it provides no guarantee that the action corresponding to the command is complete. If Command Completed notification is not supported, the controller hardwires this bit to 0b.

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Bit	Attr	Reset Value	Description
19	RW	0x0	PCIE_CAP_PRESENCE_DETECTED_CHANGED Presence Detect Changed. This bit is set when the value reported in the Presence Detect State bit is changed.
18	RW	0x0	PCIE_CAP_MRL_SENSOR_CHANGED MRL Sensor Changed. If an MRL sensor is implemented, this bit is set when a MRL Sensor state change is detected. If an MRL sensor is not implemented, this bit must not be set.
17	RW	0x0	PCIE_CAP_POWER_FAULT_DETECTED Power Fault Detected. If a Power Controller that supports power fault detection is implemented, this bit issSet when the Power Controller detects a power fault at this slot. Note: Depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot. If power fault detection is not supported, this bit must not be set.
16	RW	0x0	PCIE_CAP_ATTENTION_BUTTON_PRESSED Attention Button Pressed. If an Attention Button is implemented, this bit is set when the attention button is pressed. If an Attention Button is not supported, this bit must not be set.
15:14	RO	0x0	RSVDP_14 Reserved for future use.
13	RO	0x0	reserved
12	RW	0x0	PCIE_CAP_DLL_STATE_CHANGED_EN Data Link Layer State Changed Enable. If the Data Link Layer Link Active Reporting capability is 1b, this bit enables software notification when Data Link Layer Link Active bit is changed. If the Data Link Layer Link Active Reporting Capable bit is 0b, this bit is permitted to be read-only with a value of 0b.
11	WO	0x0	PCIE_CAP_ELECTROMECH_INTERLOCK_CTRL Electromechanical Interlock Control. If an Electromechanical Interlock is implemented, a write of 1b to this bit causes the state of the interlock to toggle. A write of 0b to this bit has no effect. A read of this bit always returns a 0b.
10	RW	0x0	PCIE_CAP_POWER_CONTROLLER_CTRL Power Controller Control. If a Power Controller is implemented, this bit when written sets the power state of the slot per the defined encodings. Reads of this bit must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write, if required to, without waiting for the previous command to complete in which case the read value is undefined. Note: In some cases the power controller may autonomously remove slot power or not respond to a power-up request based on a detected fault condition, independent of the Power Controller Control setting. If the Power Controller Present bit in the Slot Capabilities register is clear, then writes to this bit have no effect and the read value of this bit is undefined.

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Bit	Attr	Reset Value	Description
9:8	RW	0x3	PCIE_CAP_POWER_INDICATOR_CTRL Power Indicator Control. If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting, if required to, for the previous command to complete in which case the read value is undefined. Note: The default value of this field must be one of the non-Reserved values. If the Power Indicator Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 00b.
7:6	RW	0x3	PCIE_CAP_ATTENTION_INDICATOR_CTRL Attention Indicator Control. If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting, if required to, for the previous command to complete in which case the read value is undefined. Note: The default value of this field must be one of the non-Reserved values. If the Attention Indicator Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 00b.
5	RW	0x0	PCIE_CAP_HOT_PLUG_INT_EN Hot-Plug Interrupt Enable. When set, this bit enables generation of an interrupt on enabled hot-plug events. If the Hot Plug Capable bit in the Slot Capabilities register is clear, this bit is permitted to be read-only with a value of 0b.
4	RW	0x0	PCIE_CAP_CMD_CPL_INT_EN Command Completed Interrupt Enable. If Command Completed notification is supported (if the No Command Completed Support bit in the Slot Capabilities register is 0b), when set, this bit enables software notification when a hot-plug command is completed by the Hot-Plug Controller. If Command Completed notification is not supported, the controller hardwires this bit must to 0b. Write value is gated with PCIE_CAP_NO_CMD_CPL_SUPPORT field in SLOT_CAPABILITIES_REG. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: SLOT_CAPABILITIES_REG.PCIE_CAP_NO_CMD_CPL_SUPPORT ? RO : RW
3	RW	0x0	PCIE_CAP_PRESENCE_DETECT_CHANGE_EN Presence Detect Changed Enable. When set, this bit enables software notification on a presence detect changed event (for more details, see Section 6.7.3 of PCI Express Base Specification). If the Hot-Plug Capable bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b.

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Bit	Attr	Reset Value	Description
2	RW	0x0	PCIE_CAP_MRL_SENSOR_CHANGED_EN MRL Sensor Changed Enable. When set, this bit enables software notification on a MRL sensor changed event (for more details, see Section 6.7.3 of PCI Express Base Specification). If the MRL Sensor Present bit in the Slot Capabilities register is Clear, this bit is permitted to be read-only with a value of 0b.
1	RW	0x0	PCIE_CAP_POWER_FAULT_DETECTED_EN Power Fault Detected Enable. When set, this bit enables software notification on a power fault event (for more details, see Section 6.7.3 of PCI Express Base Specification). If a Power Controller that supports power fault detection is not implemented, this bit is permitted to be read-only with a value of 0b.
0	RW	0x0	PCIE_CAP_ATTENTION_BUTTON_PRESSED_EN Attention Button Pressed Enable. When set to 1b, this bit enables software notification on an attention button pressed event (for more details, see Section 6.7.3 of PCI Express Base Specification). If the Attention Button Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b.

PCIE_DSP_PF0_PCIE_CAP_ROOT_CONTROL_ROOT_CAPABILITIES_REG

Address: Operational Base(0x00000070) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	RSVDP_17 Reserved for future use.
16	RO	0x1	PCIE_CAP_CRS_SW_VISIBILITY CRS Software Visibility Capable. When set, this bit indicates that the Root Port is capable of returning Configuration Request Retry Status (CRS) Completion Status to software (for more details, see section 2.3.1 of PCI Express Base Specification). Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W (Sticky) else R (Sticky) Note: This register field is sticky.
15:5	RO	0x000	RSVDP_5 Reserved for future use.
4	RW	0x0	PCIE_CAP_CRS_SW_VISIBILITY_EN CRS Software Visibility Enable. When set, this bit enables the Root Port to return Configuration Request Retry Status (CRS) Completion Status to software (for more details, see section 2.3.1 of PCI Express Base Specification). For Root Ports that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: ROOT_CONTROL_ROOT_CAPABILITIES_REG.PCIE_CAP_CRS_SW_VISIBILITY ? RW : RO

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Bit	Attr	Reset Value	Description
3	RW	0x0	PCIE_CAP_PME_INT_EN PME Interrupt Enable. When set, this bit enables PME interrupt generation upon receipt of a PME Message as reflected in the PME Status bit (for more details, see Table 7-29 of PCI Express Base Specification). A PME interrupt is also generated if the PME Status bit is set when this bit is changed from clear to set.
2	RW	0x0	PCIE_CAP_SYS_ERR_ON_FATAL_ERR_EN System Error on Fatal Error Enable. If set, this bit indicates that a System Error should be generated if a Fatal error (ERR_FATAL) is reported by any of the devices in the Hierarchy Domain associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system is system specific.
1	RW	0x0	PCIE_CAP_SYS_ERR_ON_NON_FATAL_ERR_EN System Error on Non-Fatal Error Enable. If set, this bit indicates that a System Error should be generated if a Non-fatal error (ERR_NONFATAL) is reported by any of the devices in the Hierarchy Domain associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system is system specific.
0	RW	0x0	PCIE_CAP_SYS_ERR_ON_CORR_ERR_EN System Error on Correctable Error Enable. If set, this bit indicates that a System Error should be generated if a correctable error (ERR_COR) is reported by any of the devices in the Hierarchy Domain associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system is system specific.

PCIE_DSP_PF0_PCIE_CAP_ROOT_STATUS_REG

Address: Operational Base(0x00000070) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	RSVDP_18 Reserved for future use.
17	RO	0x0	PCIE_CAP_PME_PENDING PME Pending. This bit indicates that another PME is pending when the PME Status bit is s et. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the PME Requester ID field appropriately. The PME Pending bit is cleared by hardware if no more PMEs are pending.
16	RW	0x0	PCIE_CAP_PME_STATUS PME Status. This bit indicates that PME was asserted by the PME Requester indicated in the PME Requester ID field. Subsequent PMEs are kept pending until the status register is cleared by software by writing a 1b.
15:0	RO	0x0000	PCIE_CAP_PME_REQ_ID PME Requester ID. This field indicates the PCI Requester ID of the last PME Requester. This field is only valid when the PME Status bit is set.

PCIE_DSP_PF0_PCIE_CAP_DEVICE_CAPABILITIES2_REG

Address: Operational Base(0x00000070) + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RO	0x00	RSVDP_24 Reserved for future use.

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Bit	Attr	Reset Value	Description
23:20	RO	0x0	reserved
19:18	RO	0x3	PCIE_CAP_OBFF_SUPPORT OBFF Supported. This field indicates if OBFF is supported and, if so, what signaling mechanism is used. The value reported in this field must indicate support for WAKE# signaling only if: - for a Downstream Port, driving the WAKE# signal for OBFF is supported and the connector or component connected Downstream is known to receive that same WAKE# signal - for an Upstream Port, receiving the WAKE# signal for OBFF is supported and, if the component is on an add-in-card, that the component is connected to the WAKE# signal on theconnector. Root Ports, Switch Ports, and Endpoints are permitted to implement this capability. For a Multi-Function Device associated with an Upstream Port, each Function must report the same value for this field. For Bridges and Ports that do not implement this capability, the controller hardwires this field to 00b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(Sticky) else R(Sticky) Note: This register field is sticky.
17	RO	0x0	PCIE_CAP2_10_BIT_TAG_REQ_SUPPORT 10-Bit Tag Requester Supported. If this bit is set, the Function supports 10-Bit Tag Requester capability; otherwise, the Function does not. This bit must not be set if the 10-Bit Tag Completer Supported bit is clear. Note: 10-Bit Tag field generation must be enabled by the 10-Bit Tag Requester Enable bit in the Device Control 2 register of the Requester Function before 10-Bit Tags can be generated by the Requester. For more details, see section 2.2.6.2. of PCI Express Base Specification.
16	RO	0x0	PCIE_CAP2_10_BIT_TAG_COMP_SUPPORT 10-Bit Tag Completer Supported. If this bit is set, the Function supports 10-Bit Tag Completer capability; otherwise, the Function does not. For more details, see section 2.2.6.2. of PCI Express Base Specification.
15:14	RO	0x0	reserved
13	RO	0x0	PCIE_CAP_TPH_CMPLT_SUPPORT_1 TPH Completer Supported Bit 1.

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Bit	Attr	Reset Value	Description
12	RO	0x0	PCIE_CAP_TPH_CMPLT_SUPPORT_0 TPH Completer Supported Bit 0. Value of this bit along with TPH Completer Supported Bit 1 indicates Completer support for TPH or Extended TPH. Applicable only to Root Ports and Endpoints. For all other Functions, this field is Reserved. For more details, see section 6.17 of PCI Express Base Specification.
11	RO	0x1	PCIE_CAP_LTR_SUPP LTR Mechanism Supported. A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism. Root Ports, Switches and Endpoints are permitted to implement this capability. For a Multi-Function Device associated with an Upstream Port, each Function must report the same value for this bit. For Bridges and other Functions that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(Sticky) else R(Sticky) Note: This register field is sticky.
10	RO	0x1	PCIE_CAP_NO_RO_EN_PR2PR_PAR No RO-enabled PR-PR Passing. If this bit is set, the routing element never carries out the passing permitted by Table 2-39 of PCI Express Base Specification entry A2b that is associated with the Relaxed Ordering Attribute field being Set. This bit applies only for Switches and RCs that support peer-to-peer traffic between Root Ports. This bit applies only to Posted Requests being forwarded through the Switch or RC and does not apply to traffic originating or terminating within the Switch or RC itself. All Ports on a Switch or RC must report the same value for this bit. For all other functions, this bit must be 0b.
9	RO	0x0	PCIE_CAP_128_CAS_CPL_SUPP 128-bit CAS Completer Supported. Applicable to Functions with Memory Space BARs as well as all Root Ports; must be 0b otherwise. This bit must be set to 1b if the Function supports this optional capability. For more details, see section 6.15 of PCI Express Base Specification.
8	RO	0x0	PCIE_CAP_64_ATOMIC_CPL_SUPP 64-bit AtomicOp Completer Supported. Applicable to Functions with Memory Space BARs as well as all Root Ports; must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability. For more details on additional RC requirements, see section 6.15.3.1 of PCI Express Base Specification.
7	RO	0x0	PCIE_CAP_32_ATOMIC_CPL_SUPP 32-bit AtomicOp Completer Supported. Applicable to Functions with Memory Space BARs as well as all Root Ports; must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability. For more details on additional RC requirements, see section 6.15.3.1 of PCI Express Base Specification.

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Bit	Attr	Reset Value	Description
6	RO	0x0	PCIE_CAP_ATOMIC_ROUTING_SUPP AtomicOp Routing Supported. Applicable only to Switch Upstream Ports, Switch Downstream Ports, and Root Ports; must be 0b for other Function types. This bit must be set to 1b if the Port supports this optional capability. For more details, see section 6.15 of PCI Express Base Specification.
5	RO	0x0	PCIE_CAP_ARI_FORWARD_SUPPORT ARI Forwarding Supported. Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. For more details, see section 6.13 of PCI Express Base Specification.
4	RO	0x1	PCIE_CAP_CPL_TIMEOUT_DISABLE_SUPPORT Completion Timeout Disable Supported. A value of 1b indicates support for the Completion Timeout Disable mechanism. The Completion Timeout Disable mechanism is required for Endpoints that issue Requests on their own behalf and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. This mechanism is optional for Root Ports. For all other Functions this field is Reserved and the controller hardwires this bit to 0b.
3:0	RO	0x0	PCIE_CAP_CPL_TIMEOUT_RANGE Completion Timeout Ranges Supported. This field indicates device Function support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is Reserved and must be hardwired to 0000b. Four time value ranges are defined: - Range A: 50 us to 10 ms - Range B: 10 ms to 250 ms - Range C: 250 ms to 4 s - Range D: 4 s to 64 s Bits are set according to the list below to show timeout value ranges supported. All encodings other than the defined encodings are reserved. It is strongly recommended that the Completion Timeout mechanism not expire in less than 10 ms.

PCIE_DSP_PF0_PCIE_CAP_DEVICE_CONTROL2_DEVICE_STATUS2_REG

Address: Operational Base(0x00000070) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
14:13	RW	0x0	PCIE_CAP_OBFF_EN OBFF Enable. This field enables the OBFF mechanism and selects the signaling method. For more details on these encodings, see section 6.19 of PCI Express Base Specification. This field is required for all Ports that support the OBFF Capability. For a Multi-Function Device associated with an Upstream Port of a Device that implements OBFF, the field in Function 0 is of type RW, and only Function 0 controls the Component's behavior. In all other Functions of that Device, this field is of type RsvdP. Ports that do not implement OBFF are permitted to hardwire this field to 00b Note: RW for function #0 and RsdvP for all other functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (pf=0 && DEVICE_CAPABILITIES2_REG.PCIE_CAP_OBFF_SUPPORT) then R/W else R
12:11	RO	0x0	reserved
10	RW	0x0	PCIE_CAP_LTR_EN LTR Mechanism Enable. When set to 1b, this bit enables Upstream Ports to send LTR messages and Downstream Ports to process LTR Messages. For a Multi-Function Device associated with an Upstream Port of a device that implements LTR, the bit in Function 0 is RW, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is RsvdP. Functions that do not implement the LTR mechanism are permitted to hardwire this bit to 0b. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. The write value is gated with the PCIE_CAP_LTR_SUPP field of DEVICE_CAPABILITIES2_REG. Note: RW for function #0 and RsdvP for all other functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (pf=0 && DEVICE_CAPABILITIES2_REG.PCIE_CAP_LTR_SUPP) then R/W else R
9:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	RO	0x0	PCIE_CAP_ARI_FORWARD_SUPPORT_CS ARI Forwarding Enable. When set, the Downstream Port disables its traditional Device Number field being 0 enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port. For more details, see Section 6.13 of PCI Express Base Specification. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
4	RW	0x0	PCIE_CAP_CPL_TIMEOUT_DISABLE Completion Timeout Disable. When set, this bit disables the Completion Timeout mechanism. This bit is required for all Functions that support the Completion Timeout Disable Capability. Functions that do not support this optional capability are permitted to hardwire this bit to 0b Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding Requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding Requests. If this is done, it is permitted to base the start time for each Request on either the time this bit was cleared or the time each Request was issued.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	PCIE_CAP_CPL_TIMEOUT_VALUE Completion Timeout Value. In device Functions that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is Reserved and controller hardwires it to 0000b. A Function that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50 us to 50 ms. Functions that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Ranges Supported field. All encodings other than the defined encodings are reserved. It is strongly recommended that the Completion Timeout mechanism not expire in less than 10 ms. Values available if Range A (50 us to 10 ms) programmability range is supported: Values available if Range B (10 ms to 250 ms) programmability range is supported: Values available if Range C (250 ms to 4 s) programmability range is supported: Values available if the Range D (4 s to 64 s) programmability range is supported: Software is permitted to change the value in this field at any time. For Requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding Requests, and is permitted to base the start time for each Request either on when this value was changed or on when each request was issued. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

PCIE_DSP_PF0_PCIE_CAP_LINK_CAPABILITIES2_REG

Address: Operational Base(0x00000070) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:25	RO	0x00	RSVDP_25 Reserved for future use.
24:23	RO	0x0	reserved
22:9	RO	0x0000	RSVDP_9 Reserved for future use.

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Bit	Attr	Reset Value	Description
8	RO	0x0	PCIE_CAP_CROSS_LINK_SUPPORT Crosslink Supported. When set to 1b, this bit indicates that the associated Port supports crosslinks (for more details, see section 4.2.6.3.1 of PCI Express Base Specification). When set to 0b on a Port that supports Link speeds of 8.0 GT/s or higher, this bit indicates that the associated Port does not support crosslinks. When set to 0b on a Port that only supports Link speeds of 2.5 GT/s or 5.0 GT/s, this bit provides no information regarding the Port's level of crosslink support. It is recommended that this bit be Set in any Port that supports crosslinks even though doing so is only required for Ports that also support operating at 8.0 GT/s or higher Link speeds. Note: Software should use this bit when referencing fields whose definition depends on whether or not the Port supports crosslinks (for more details, see section 7.7.3.4 of PCI Express Base Specification). Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions.
7:1	RO	0x07	PCIE_CAP_SUPPORT_LINK_SPEED_VECTOR Supported Link Speeds Vector. This field indicates the supported Link speed(s) of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. For more details, see section 8.2.1 of PCI Express Base Specification. Bit definitions within this field are: - Bit 0 2.5 GT/s - Bit 1 5.0 GT/s - Bit 2 8.0 GT/s - Bit 3 16.0 GT/s - Bit 4 32.0 GT/s - Bits 6:5 RsvdP Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions. This field has a default of (PCIE_CAP_MAX_LINK_SPEED == 0101) ? 0011111 : (PCIE_CAP_MAX_LINK_SPEED == 0100) ? 0001111 : (PCIE_CAP_MAX_LINK_SPEED == 0011) ? 0000111 : (PCIE_CAP_MAX_LINK_SPEED == 0010) ? 0000011 : 0000001 where PCIE_CAP_MAX_LINK_SPEED is a field in the LINK_CAPABILITIES_REG register.
0	RO	0x0	RSVDP_0 Reserved for future use.

PCIE_DSP_PF0_PCIE_CAP_LINK_CONTROL2_LINK_STATUS2_REG

Address: Operational Base(0x00000070) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:26	RO	0x0	RSVDP_26 Reserved for future use.
25:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21	RW	0x0	PCIE_CAP_LINK_EQ_REQ Link Equalization Request 8.0 GT/s. This bit is set by hardware to request the 8.0 GT/s Link equalization process to be performed on the Link. For more details, see sections 4.2.3 and 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky.
20	RO	0x0	PCIE_CAP_EQ_CPL_P3 EEqualization 8.0 GT/s Phase 3 Successful. When set to 1b, this bit indicates that Phase 3 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky.
19	RO	0x0	PCIE_CAP_EQ_CPL_P2 Equalization 8.0 GT/s Phase 2 Successful. When set to 1b, this bit indicates that Phase 2 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky.
18	RO	0x0	PCIE_CAP_EQ_CPL_P1 Equalization 8.0 GT/s Phase 1 Successful. When set to 1b, this bit indicates that Phase 1 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
17	RO	0x0	PCIE_CAP_EQ_CPL Equalization 8.0 GT/s Complete. When set to 1b, this bit indicates that the Transmitter Equalization procedure at the 8.0 GT/s data rate has completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky.
16	RO	0x1	PCIE_CAP_CURR_DEEMPHASIS Current De-emphasis Level. When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. For components that support speeds greater than 2.5 GT/s, Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions of the Port. In M-PCIe mode this register is always 0x0. In C-PCIe mode, its contents are derived by sampling the PIPE.
15:12	RW	0x0	PCIE_CAP_COMPLIANCE_PRESET Compliance Preset/De-emphasis. - For 8.0 GT/s and higher Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. The encodings are defined in section 4.2.3.2 of PCI Express Base Specification . Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. - For 5.0 GT/s Data Rate: This field sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. - When the Link is operating at 2.5 GT/s, the setting of this field has no effect. Components that support only 2.5 GT/s speed are permitted to hardwire this field to 0000b. - For a Multi-Function Device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. - This field is intended for debug and compliance testing purposes. System firmware and software is allowed to modify this field only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
11	RW	0x0	PCIE_CAP_COMPLIANCE_SOS Compliance SOS. When set to 1b, the LTSSM is required to send SKP Ordered Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only. For components that support only the 2.5 GT/s speed, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
10	RW	0x0	PCIE_CAP_ENTER_MODIFIED_COMPLIANCE Enter Modified Compliance. When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
9:7	RW	0x0	PCIE_CAP_TX_MARGIN Transmit Margin, This field controls the value of the non-deemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see Chapter 4 of PCI Express Base Specification for details of how the Transmitter voltage level is determined in various states). - 001b-111b: As defined in Section 8.3.4 not all encodings are required to be implemented. For a Multi-Function Device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP.

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Bit	Attr	Reset Value	Description
			For components that support only the 2.5 GT/s speed, the controller hardwires this bit to 000b. This field is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this field only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value. Note: This register field is sticky.
6	RO	0x0	PCIE_CAP_SEL_DEEMPHASIS Selectable De-emphasis. When the Link is operating at 5.0 GT/s speed, this bit is used to control the transmit de-emphasis of the link in specific situations. For more details, see section 4.2.6 of PCI Express Base Specification. When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. This bit is not applicable and Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
5	RW	0x0	PCIE_CAP_HW_AUTO_SPEED_DISABLE Hardware Autonomous Speed Disable. When set, this bit disables hardware from changing the Link speed for device-specific reasons other than attempting to correct unreliable Link operation by reducing Link speed. Initial transition to the highest supported common link speed is not blocked by this bit. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
4	RW	0x0	PCIE_CAP_ENTER_COMPLIANCE Enter Compliance. Software is permitted to force a Link to enter Compliance mode (at the speed indicated in the Target Link Speed field and the de-emphasis/preset level indicated by the Compliance Preset/De-emphasis field) by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
			PCIE_CAP_TARGET_LINK_SPEED Target Link Speed. For Downstream Ports, this field sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the desired target Link speed. All encodings other than the defined encodings are reserved. If a value is written to this field that does not correspond to a supported speed (as indicated by the Supported Link Speeds Vector), the result is undefined. If either of the Enter Compliance or Enter Modified Compliance bits are implemented, then this field must also be implemented. The default value of this field is the highest Link speed supported by the component (as reported in the Max Link Speed field of the Link Capabilities register) unless the corresponding platform/form factor requires a different default value.
3:0	RW	0x3	For both Upstream and Downstream Ports, this field is used to set the target compliance mode speed when software is using the Enter Compliance bit to force a Link into compliance mode. For Upstream Ports, if the Enter Compliance bit is Clear, this field is permitted to have no effect. For a Multi-Function Device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Components that support only the 2.5 GT/s speed are permitted to hardwire this field to 0000b. In M-PCIe mode, the contents of this field are derived from other registers. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

14.4.3.6 PCIE_DSP_PF0_AER_CAP Register Description

14.4.3.6.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_AER_CAP_AER_EXT_CAP_HDR_OFF	0x0000	W	0x14820001	Advanced Error Reporting Extended Capability Header provides information about Capability ID, Version, and next offset.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_AER_CAP_UNCORR_ERR_STATUS_OFF	0x0004	W	0x00000000	The Uncorrectable Error Status Register (Offset 04h) indicates error detection status of individual errors on a PCI Express device Function.An individual error status bit that is Set indicates that a particular error was detected; software may clear an error status by writing a 1b to the respective bit.Register bits not implemented by the Function are hardwired to 0b.
PCIE_DSP_PF0_AER_CAP_UNCORR_ERR_MASK_OFF	0x0008	W	0x00400000	The Uncorrectable Error Mask Register controls reporting of individual errors by the device Function to the PCI Express Root Complex through a PCI Express error Message.A masked error (respective bit Set in the mask register) is not recorded or reported in the Header Log, TLP Prefix Log, or First Error Pointer, and is not reported to the PCI Express Root Complex by this Function.There is a mask bit per error bit of the Uncorrectable Error Status register. Register fields for bits not implemented by the Function are hardwired to 0b.
PCIE_DSP_PF0_AER_CAP_UNCORR_ERR_SEV_OFF	0x000C	W	0x00462030	The Uncorrectable Error Severity Register controls whether an individual error is reported as a Non-fatal or Fatal error.An error is reported as fatal when the corresponding error bit in the severity register is Set. If the bit is Clear, the corresponding error is considered non-fatal.
PCIE_DSP_PF0_AER_CAP_CORR_ERR_STATUS_OFF	0x0010	W	0x00000000	The Correctable Error Status register reports error status of individual correctable error sources on a PCI Express device Function.When an individual error status bit is Set, it indicates that a particular error occurred; software may clear an error status by writing a 1b to the respective bit.Register bits not implemented by the Function are hardwired to 0b by the controller.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_AER_CAP_CORR_ERR_MASK_OFF	0x0014	W	0x0000E000	The Correctable Error Mask Register controls reporting of individual correctable errors by this Function to the PCI Express Root Complex through a PCI Express error Message.A masked error (respective bit Set in the mask register) is not reported to the PCI Express Root Complex by this Function.There is a mask bit per error bit in the Correctable Error Status register. Register fields for bits not implemented by the Function are hardwired to 0b by the controller.
PCIE_DSP_PF0_AER_CAP_ADV_ERR_CAP_CTRL_OFF	0x0018	W	0x000000A0	Advanced Error Capabilities and Control Register provides information whether the individual capability is supported or not. If the capability is supported then it is enabled or not.
PCIE_DSP_PF0_AER_CAP_HDR_LOG_0_OFF	0x001C	W	0x00000000	The Header Log Register 0 contains the header for the TLP corresponding to a detected error; The header is captured such that, when read using DW accesses, the fields of the header are laid out in the same way the headers are presented in the specification.Therefore, byte 0 of the header is located in byte 3 of the Header Log Register 0, byte 1 of the header is in byte 2 of the Header Log Register 0, and so forth. For 12-byte headers, only bytes 0 through 11 of the Header Log Register are used and values in bytes 12 through 15 are undefined.In certain cases where a Malformed TLP is reported, the Header Log Register may contain TLP Prefix information.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_AER_CAP_HDR_LOG_1_OFF	0x0020	W	0x00000000	The Header Log Register 1 contains the header for the TLP corresponding to a detected error; The header is captured such that, when read using DW accesses, the fields of the header are laid out in the same way the headers are presented in the specification.Therefore, byte 0 of the header is located in byte 3 of the Header Log Register 1, byte 1 of the header is in byte 2 of the Header Log Register 1 and so forth. For 12-byte headers, only bytes 0 through 11 of the Header Log Register are used and values in bytes 12 through 15 are undefined.In certain cases where a Malformed TLP is reported, the Header Log Register may contain TLP Prefix information.
PCIE_DSP_PF0_AER_CAP_HDR_LOG_2_OFF	0x0024	W	0x00000000	The Header Log Register 2 contains the header for the TLP corresponding to a detected error; The header is captured such that, when read using DW accesses, the fields of the header are laid out in the same way the headers are presented in the specification.Therefore, byte 0 of the header is located in byte 3 of the Header Log Register 2, byte 1 of the header is in byte 2 of the Header Log Register 2 and so forth. For 12-byte headers, only bytes 0 through 11 of the Header Log Register are used and values in bytes 12 through 15 are undefined.In certain cases where a Malformed TLP is reported, the Header Log Register may contain TLP Prefix information.
PCIE_DSP_PF0_AER_CAP_HDR_LOG_3_OFF	0x0028	W	0x00000000	The Header Log Register 3 contains the header for the TLP corresponding to a detected error; The header is captured such that, when read using DW accesses, the fields of the header are laid out in the same way the headers are presented in the specification.Therefore, byte 0 of the header is located in byte 3 of the Header Log Register 3, byte 1 of the header is in byte 2 of the Header Log Register 3 and so

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Name	Offset	Size	Reset Value	Description
				forth. For 12-byte headers, only bytes 0 through 11 of the Header Log Register are used and values in bytes 12 through 15 are undefined.In certain cases where a Malformed TLP is reported, the Header Log Register may contain TLP Prefix information.
PCIE_DSP_PF0_AER_CAP_ROOT_ERR_CMD_OFF	0x002C	W	0x00000000	The Root Error Command Register allows further control of Root Complex response to Correctable, Non-Fatal, and Fatal error Messages than the basic Root Complex capability to generatesystem errors in response to error Messages.
PCIE_DSP_PF0_AER_CAP_ROOT_ERR_STATUS_OFF	0x0030	W	0x48000000	The Root Error Status Register reports status of error Messages (ERR_COR, ERR_NONFATAL, and ERR_FATAL) received by the Root Port, and of errors detected by the Root Port itself(The Root Port had sent an error Message to itself).In order to update this register, error Messages received by the Root Port and/or internally generated error Messages must be enabled for i°transmissioni± by the primary interface of the Root Port.
PCIE_DSP_PF0_AER_CAP_ERR_SRC_ID_OFF	0x0034	W	0x00000000	The Error Source Identification Register identifies the source (Requester ID) of first correctable and uncorrectable (Non-fatal/Fatal) errors reported in the Root Error Status Register.This register is updated regardless of the settings of the Root Control register and the Root Error Command Register.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_1_OFF	0x0038	W	0x00000000	The First TLP Prefix Log Register contains the first End-End TLP Prefix from the TLP corresponding to the detected error. The TLP Prefix Log Register is only meaningful when the TLP Prefix Log Present bit is Set.The TLP Prefixes are captured such that, when read using DW accesses, the fields of the TLP Prefix are laid out in the same way the fields of the TLP Prefix are described.Therefore, byte 0 of a TLP Prefix is located in byte 3 of the associated TLP Prefix Log Register; byte 1 of a TLP Prefix is located in byte 2; and so forth. The TLP Prefix Log Registers beyond the number supported by the Function are hardwired to zero by controller.If the End-End TLP Prefix Supported bit is Clear, the TLP Prefix Log Register is not required to be implemented.
PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_2_OFF	0x003C	W	0x00000000	The Second TLP Prefix Log Register contains the second End-End TLP Prefix from the TLP corresponding to the detected error. The TLP Prefix Log Register is only meaningful when the TLP Prefix Log Present bit is Set.The TLP Prefixes are captured such that, when read using DW accesses, the fields of the TLP Prefix are laid out in the same way the fields of the TLP Prefix are described.Therefore, byte 0 of a TLP Prefix is located in byte 3 of the associated TLP Prefix Log Register; byte 1 of a TLP Prefix is located in byte 2; and so forth. The TLP Prefix Log Registers beyond the number supported by the Function are hardwired to zero by controller.If the End-End TLP Prefix Supported bit is Clear, the TLP Prefix Log Register is not required to be implemented.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_3_OFF	0x0040	W	0x00000000	The Third TLP Prefix Log Register contains the third End-End TLP Prefix from the TLP corresponding to the detected error. The TLP Prefix Log Register is only meaningful when the TLP Prefix Log Present bit is Set.The TLP Prefixes are captured such that, when read using DW accesses, the fields of the TLP Prefix are laid out in the same way the fields of the TLP Prefix are described.Therefore, byte 0 of a TLP Prefix is located in byte 3 of the associated TLP Prefix Log Register; byte 1 of a TLP Prefix is located in byte 2; and so forth. The TLP Prefix Log Registers beyond the number supported by the Function are hardwired to zero by controller.If the End-End TLP Prefix Supported bit is Clear, the TLP Prefix Log Register is not required to be implemented.
PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_4_OFF	0x0044	W	0x00000000	The Fourth TLP Prefix Log Register contains the fourth End-End TLP Prefix from the TLP corresponding to the detected error. The TLP Prefix Log Register is only meaningful when the TLP Prefix Log Present bit is Set.The TLP Prefixes are captured such that, when read using DW accesses, the fields of the TLP Prefix are laid out in the same way the fields of the TLP Prefix are described.Therefore, byte 0 of a TLP Prefix is located in byte 3 of the associated TLP Prefix Log Register; byte 1 of a TLP Prefix is located in byte 2; and so forth. The TLP Prefix Log Registers beyond the number supported by the Function are hardwired to zero by controller.If the End-End TLP Prefix Supported bit is Clear, the TLP Prefix Log Register is not required to be implemented.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3.6.2 Detail Registers Description

PCIE_DSP_PF0_AER_CAP_AER_EXT_CAP_HDR_OFF

Address: Operational Base(0x00000100) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:20	RO	0x148	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
19:16	RO	0x2	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field must be 2h if the End-End TLP Prefix Supported bit is set and must be 1h or 2h otherwise. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
15:0	RO	0x0001	CAP_ID AER Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Advanced Error Reporting Capability is 0001h. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_UNCORR_ERR_STATUS_OFF

Address: Operational Base(0x00000100) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	RSVDP_27 Reserved for future use.
26:24	RO	0x0	reserved
23	RO	0x0	RSVDP_23 Reserved for future use.

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Bit	Attr	Reset Value	Description
22	RW	0x0	INTERNAL_ERR_STATUS Uncorrectable Internal Error Status. This field gives status of the Uncorrectable Internal Error. The controller sets this bit when your application asserts app_err_bus[9]. It does not set this bit when it detects internal uncorrectable internal errors such as parity and ECC failures. You should use the outputs from these errors to drive the app_err_bus[9] input. For more details, see the "Data Integrity (Wire, Datapath, and RAM Protection)" section in the Databook. Note: This register field is sticky.
21	RO	0x0	reserved
20	RW	0x0	UNSUPPORTED_REQ_ERR_STATUS Unsupported Request Error Status. This field represents status of Unsupported Request Error. Note: This register field is sticky.
19	RW	0x0	ECRC_ERR_STATUS ECRC Error Status. This field represents status of ECRC Error. Note:If CX_ECRC_ENABLE=0 the register field always reads 0. Note: This register field is sticky.
18	RW	0x0	MALF_TLP_ERR_STATUS Malformed TLP Status. This field represents status of Malformed TLP. Note: This register field is sticky.
17	RW	0x0	REC_OVERFLOW_ERR_STATUS Receiver Overflow Status. Status bit for Receiver Overflow. Note: This register field is sticky.
16	RW	0x0	UNEXP_CMPLT_ERR_STATUS Unexpected Completion Status. Status bit for Unexpected Completion. Note: This register field is sticky.
15	RW	0x0	CMPLT_ABORT_ERR_STATUS Completer Abort Status. Status bit for Completer Abort. Note: This register field is sticky.
14	RW	0x0	CMPLT_TIMEOUT_ERR_STATUS Completion Timeout Status. Status for Completion Timeout. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
13	RW	0x0	FC_PROTOCOL_ERR_STATUS Flow Control Protocol Error Status. Status bit for Flow Control Protocol Error. Note: This register field is sticky.
12	RW	0x0	POIS_TLP_ERR_STATUS Poisoned TLP Status. Status bit for Poisoned TLP. Note: This register field is sticky.
11:6	RO	0x00	RSVDP_6 Reserved for future use.
5	RW	0x0	SURPRISE_DOWN_ERR_STATUS Surprise Down Error Status (Optional). Status bit for Surprise Down Error. Note: This register field is sticky.
4	RW	0x0	DL_PROTOCOL_ERR_STATUS Data Link Protocol Error Status. Status bit for Data Link Protocol Error. Note: This register field is sticky.
3:0	RO	0x0	RSVDP_0 Reserved for future use.

PCIE_DSP_PF0_AER_CAP_UNCORR_ERR_MASK_OFF

Address: Operational Base(0x00000100) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	RSVDP_27 Reserved for future use.
26:24	RO	0x0	reserved
23	RO	0x0	RSVDP_23 Reserved for future use.
22	RW	0x1	INTERNAL_ERR_MASK Uncorrectable Internal Error Mask (Optional). Mask bit for Uncorrectable Internal Error. Note: This register field is sticky.
21	RO	0x0	reserved
20	RW	0x0	UNSUPPORTED_REQ_ERR_MASK Unsupported Request Error Mask. Mask bit for Unsupported Request Error. Note: This register field is sticky.
19	RW	0x0	ECRC_ERR_MASK ECRC Error Mask (Optional). Mask bit for ECRC Error. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
18	RW	0x0	MALF_TLP_ERR_MASK Malformed TLP Mask. Mask bit for Malformed TLP. Note: This register field is sticky.
17	RW	0x0	REC_OVERFLOW_ERR_MASK Receiver Overflow Mask (Optional). This field represents Receiver Overflow Mask. Note: This register field is sticky.
16	RW	0x0	UNEXP_CMPLT_ERR_MASK Unexpected Completion Mask. Mask bit for Unexpected Completion Error. Note: This register field is sticky.
15	RW	0x0	CMPLT_ABORT_ERR_MASK Completer Abort Error Mask (Optional). Mask bit for Completer Abort Error. Note: This register field is sticky.
14	RW	0x0	CMPLT_TIMEOUT_ERR_MASK Completion Timeout Error Mask. Mask bit for Completion Timeout Error. Note: This register field is sticky.
13	RW	0x0	FC_PROTOCOL_ERR_MASK Flow Control Protocol Error Mask. Mask bit for Flow Control Protocol Error. Note: This register field is sticky.
12	RW	0x0	POIS_TLP_ERR_MASK Poisoned TLP Error Mask. Mask bit for Poisoned TLP Error. Note: This register field is sticky.
11:6	RO	0x00	RSVDP_6 Reserved for future use.
5	RO	0x0	SURPRISE_DOWN_ERR_MASK Surprise Down Error Mask. Mask bit for Surprise Down Error. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP ? RW : RO Note: This register field is sticky.
4	RW	0x0	DL_PROTOCOL_ERR_MASK Data Link Protocol Error Mask. This field informs whether Data Link Protocol Error is masked or not. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	RSVDP_0 Reserved for future use.

PCIE_DSP_PF0_AER_CAP_UNCORR_ERR_SEV_OFF

Address: Operational Base(0x00000100) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	RSVDP_27 Reserved for future use.
26:24	RO	0x0	reserved
23	RO	0x0	RSVDP_23 Reserved for future use.
22	RW	0x1	INTERNAL_ERR_SEVERITY Uncorrectable Internal Error Severity (Optional). Severity bit for Uncorrectable Internal Error. Note: This register field is sticky.
21	RO	0x0	reserved
20	RW	0x0	UNSUPPORTED_REQ_ERR_SEVERITY Unsupported Request Error Severity. Severity bit for Unsupported Request Error. Note: This register field is sticky.
19	RW	0x0	ECRC_ERR_SEVERITY ECRC Error Severity (Optional). Severity bit for ECRC Error. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
18	RW	0x1	MALF_TLP_ERR_SEVERITY Malformed TLP Severity. Severity bit for Malformed TLP. Note: This register field is sticky.
17	RW	0x1	REC_OVERFLOW_ERR_SEVERITY Receiver Overflow Error Severity (Optional). Severity bit for Receiver Overflow Error. Note: This register field is sticky.
16	RW	0x0	UNEXP_CMPLT_ERR_SEVERITY Unexpected Completion Error Severity. Severity bit for Unexpected Completion Error. Note: This register field is sticky.
15	RW	0x0	CMPLT_ABORT_ERR_SEVERITY Completer Abort Error Severity (Optional). Severity bit for Completer Abort Error. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
14	RW	0x0	CMPLT_TIMEOUT_ERR_SEVERITY Completion Timeout Error Severity. Severity bit for Completion Timeout Error. Note: This register field is sticky.
13	RW	0x1	FC_PROTOCOL_ERR_SEVERITY Flow Control Protocol Error Severity (Optional). Severity bit for Flow Control Protocol Error. Note: This register field is sticky.
12	RW	0x0	POIS_TLP_ERR_SEVERITY Poisoned TLP Severity. Severity bit for Poisoned TLP. Note: This register field is sticky.
11:6	RO	0x00	RSVDP_6 Reserved for future use.
5	RO	0x1	SURPRISE_DOWN_ERR_SVRITY Surprise Down Error Severity (Optional). Severity bit for Surprise Down Error. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP ? RW : RO Note: This register field is sticky.
4	RW	0x1	DL_PROTOCOL_ERR_SEVERITY Data Link Protocol Error Severity. Severity bit for Data Link Protocol Error. Note: This register field is sticky.
3:0	RO	0x0	RSVDP_0 Reserved for future use.

PCIE_DSP_PF0_AER_CAP_CORR_ERR_STATUS_OFF

Address: Operational Base(0x00000100) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	RSVDP_16 Reserved for future use.
15	RW	0x0	HEADER_LOG_OVERFLOW_STATUS Header Log Overflow Error Status (Optional). This field provides status of Header Log Overflow Error. Note: This register field is sticky.
14	RW	0x0	CORRECTED_INT_ERR_STATUS Corrected Internal Error Status (Optional). This field provides status of Corrected Internal Error. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
13	RW	0x0	ADVISORY_NON_FATAL_ERR_STATUS Advisory Non-Fatal Error Status. Status bit for Advisory Non-Fatal Error. Note: This register field is sticky.
12	RW	0x0	RPL_TIMER_TIMEOUT_STATUS Replay Timer Timeout Status. Status bit for Replay Timer Timeout. Note: This register field is sticky.
11:9	RO	0x0	RSVDP_9 Reserved for future use.
8	RW	0x0	REPLAY_NO_ROLEOVER_STATUS REPLAY_NUM Rollover Status. Status bit for REPLAY_NUM Rollover. Note: This register field is sticky.
7	RW	0x0	BAD_DLLP_STATUS Bad DLLP Status. Status bit for Bad DLLP. Note: This register field is sticky.
6	RW	0x0	BAD_TLP_STATUS Bad TLP Status. Status bit for Bad TLP. Note: This register field is sticky.
5:1	RO	0x00	RSVDP_1 Reserved for future use.
0	RW	0x0	RX_ERR_STATUS Receiver Error Status (Optional). This field provides status of Receiver Error. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_CORR_ERR_MASK_OFF

Address: Operational Base(0x00000100) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	RSVDP_16 Reserved for future use.
15	RW	0x1	HEADER_LOG_OVERFLOW_MASK Header Log Overflow Error Mask (Optional). Masking bit for Header Log Overflow Error. Note: This register field is sticky.
14	RW	0x1	CORRECTED_INT_ERR_MASK Corrected Internal Error Mask (Optional). Masking bit for Corrected Internal Error Mask. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
13	RW	0x1	ADVISORY_NON_FATAL_ERR_MASK Advisory Non-Fatal Error Mask. Masking bit for Advisory Non-Fatal Error. Note: This register field is sticky.
12	RW	0x0	RPL_TIMER_TIMEOUT_MASK Replay Timer Timeout Mask. Masking bit for Replay Timer Timeout. Note: This register field is sticky.
11:9	RO	0x0	RSVDP_9 Reserved for future use.
8	RW	0x0	REPLAY_NO_ROLEOVER_MASK REPLAY_NUM Rollover Mask. Masking bit for REPLAY_NUM Rollover. Note: This register field is sticky.
7	RW	0x0	BAD_DLLP_MASK Bad DLLP Mask. Masking bit for Bad DLLP. Note: This register field is sticky.
6	RW	0x0	BAD_TLP_MASK Bad TLP Mask. Masking bit for Bad TLP. Note: This register field is sticky.
5:1	RO	0x00	RSVDP_1 Reserved for future use.
0	RW	0x0	RX_ERR_MASK Receiver Error Mask (Optional). Masking bit for Receiver Error. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_ADV_ERR_CAP_CTRL_OFF

Address: Operational Base(0x00000100) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	RSVDP_13 Reserved for future use.
12	RO	0x0	CTO_PRFX_HDR_LOG_CAP TLP Prefix Log Present. If Set, this bit indicates that the Function records the prefix/header of Request TLPs that experience a Completion Timeout error.
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10	RO	0x0	MULTIPLE_HEADER_EN Multiple Header Recording Enable. When Set, this bit enables the Function to record more than one error header. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.
9	RO	0x0	MULTIPLE_HEADER_CAP Multiple Header Recording Capable. If Set, this bit indicates that the Function is capable of recording more than one error header. Note: This register field is sticky.
8	RW	0x0	ECRC_CHECK_EN ECRC Check Enable. When Set, ECRC checking is enabled. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b. Note: This register field is sticky.
7	RO	0x1	ECRC_CHECK_CAP ECRC Check Capable. If Set, this bit indicates that the Function is capable of checking ECRC. Note: This register field is sticky.
6	RW	0x0	ECRC_GEN_EN ECRC Generation Enable. When Set, ECRC generation is enabled. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b. Note: This register field is sticky.
5	RO	0x1	ECRC_GEN_CAP ECRC Generation Capable. If Set, this bit indicates that the Function is capable of generating ECRC. Note: This register field is sticky.
4:0	RO	0x00	FIRST_ERR_POINTER First Error Pointer. The First Error Pointer is a field that identifies the bit position of the first error reported in the Uncorrectable Error Status register. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_HDR_LOG_0_OFF

Address: Operational Base(0x00000100) + offset (0x001C)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	FIRST_DWORD_FOURTH_BYTE Byte 3 of Header log register of First 32-bit Data Word. This field represents fourth byte of First DW of Header. Note: This register field is sticky.
23:16	RO	0x00	FIRST_DWORD_THIRD_BYTE Byte 2 of Header log register of First 32-bit Data Word. This field represents third byte of First DW of Header. Note: This register field is sticky.
15:8	RO	0x00	FIRST_DWORD_SECOND_BYTE Byte 1 of Header log register of First 32-bit Data Word. This field represents second byte of First DW of Header. Note: This register field is sticky.
7:0	RO	0x00	FIRST_DWORD_FIRST_BYTE Byte 0 of Header log register of First 32-bit Data Word. This field represents first byte of First DW of Header. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_HDR_LOG_1_OFF

Address: Operational Base(0x00000100) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	SECOND_DWORD_FOURTH_BYTE Byte 3 of Header log register of Second 32-bit Data Word. This field represents fourth byte of Second DW of Header. Note: This register field is sticky.
23:16	RO	0x00	SECOND_DWORD_THIRD_BYTE Byte 2 of Header log register of Second 32-bit Data Word. This field represents third byte of Second DW of Header. Note: This register field is sticky.
15:8	RO	0x00	SECOND_DWORD_SECOND_BYTE Byte 1 of Header log register of Second 32-bit Data Word. This field represents second byte of Second DW of Header. Note: This register field is sticky.
7:0	RO	0x00	SECOND_DWORD_FIRST_BYTE Byte 0 of Header log register of Second 32-bit Data Word. This field represents first byte of Second DW of Header. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_HDR_LOG_2_OFF

Address: Operational Base(0x00000100) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	THIRD_DWORD_FOURTH_BYTE Byte 3 of Header log register of Third 32-bit Data Word. This field represents fourth byte of Third DW of Header. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
23:16	RO	0x00	THIRD_DWORD_THIRD_BYTE Byte 2 of Header log register of Third 32-bit Data Word. This field represents third byte of Third DW of Header. Note: This register field is sticky.
15:8	RO	0x00	THIRD_DWORD_SECOND_BYTE Byte 1 of Header log register of Third 32-bit Data Word. This field represents second byte of Third DW of Header. Note: This register field is sticky.
7:0	RO	0x00	THIRD_DWORD_FIRST_BYTE Byte 0 of Header log register of Third 32-bit Data Word. This field represents first byte of Third DW of Header. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_HDR_LOG_3_OFF

Address: Operational Base(0x00000100) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	FOURTH_DWORD_FOURTH_BYTE Byte 3 of Header log register of Fourth 32-bit Data Word. This field represents fourth byte of Fourth DW of Header. Note: This register field is sticky.
23:16	RO	0x00	FOURTH_DWORD_THIRD_BYTE Byte 2 of Header log register of Fourth 32-bit Data Word. This field represents third byte of Fourth DW of Header. Note: This register field is sticky.
15:8	RO	0x00	FOURTH_DWORD_SECOND_BYTE Byte 1 of Header log register of Fourth 32-bit Data Word. This field represents second byte of Fourth DW of Header. Note: This register field is sticky.
7:0	RO	0x00	FOURTH_DWORD_FIRST_BYTE Byte 0 of Header log register of Fourth 32-bit Data Word. This field represents first byte of Fourth DW of Header. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_ROOT_ERR_CMD_OFF

Address: Operational Base(0x00000100) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	RSVDP_3 Reserved for future use.
2	RW	0x0	FATAL_ERR_REPORTING_EN Fatal Error Reporting Enable. When Set, this bit enables the generation of an interrupt when a Fatal error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port. Root Complex Event Collectors provide support for the above described functionality for RCiEPs.

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Bit	Attr	Reset Value	Description
1	RW	0x0	NON_FATAL_ERR_REPORTING_EN Non-Fatal Error Reporting Enable. When Set, this bit enables the generation of an interrupt when a Non-fatal error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port. Root Complex Event Collectors provide support for the above described functionality for RCiEPs.
0	RW	0x0	CORR_ERR_REPORTING_EN Correctable Error Reporting Enable. When Set, this bit enables the generation of an interrupt when a correctable error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port. Root Complex Event Collectors provide support for the above described functionality for RCiEPs (Root Complex integrated Endpoint).

PCIE_DSP_PF0_AER_CAP_ROOT_ERR_STATUS_OFF

Address: Operational Base(0x00000100) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:27	RO	0x09	ADV_ERR_INT_MSG_NUM Advanced Error Interrupt Message Number. This register indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability. For MSI, the value in this register indicates the offset between the base Message Data and the interrupt message that is generated. For MSI-X, the value in this register indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant. If MSI-X is enabled, the value in this register must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this register must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this register is undefined. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
26:7	RO	0x00000	RSVDP_7 Reserved for future use.
6	RW	0x0	FATAL_ERR_MSG_RX One or more Fatal Error Messages Received. Set when one or more Fatal Uncorrectable error Messages have been received. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
5	RW	0x0	NON_FATAL_ERR_MSG_RX One or more Non-Fatal Error Messages Received. Set when one or more Non-Fatal Uncorrectable error Messages have been received. Note: This register field is sticky.
4	RW	0x0	FIRST_UNCORR_FATAL First Uncorrectable Error is Fatal. Set when the first Uncorrectable error Message received is for a Fatal error. Note: This register field is sticky.
3	RW	0x0	MUL_ERR_FATAL_NON_FATAL_RX Multiple Fatal or Non-Fatal Errors Received. Set when either a Fatal or a Non-fatal error is received and ERR_FATAL_NON_FATAL_RX is already Set. Note: This register field is sticky.
2	RW	0x0	ERR_FATAL_NON_FATAL_RX Fatal or Non-Fatal Error Received. Set when either a Fatal or a Non-fatal error Message is received and this bit is not already Set. Note: This register field is sticky.
1	RW	0x0	MUL_ERR_COR_RX Multiple Correctable Errors Received. Set when a Correctable error Message is received and ERR_COR_RX is already Set. Note: This register field is sticky.
0	RW	0x0	ERR_COR_RX Correctable Error Received. Set when a Correctable error Message is received and this bit is not already Set. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_ERR_SRC_ID_OFF

Address: Operational Base(0x00000100) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ERR_FATAL_NON_FATAL_SOURCE_ID Source of Fatal/Non-Fatal Error. Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message when the ERR_FATAL/NONFATAL Received bit is not already set. Note: This register field is sticky.
15:0	RO	0x0000	ERR_COR_SOURCE_ID Source of Correctable Error. Loaded with the Requester ID indicated in the received ERR_COR Message when the ERR_COR Received bit is not already set. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_1_OFF

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Address: Operational Base(0x00000100) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CFG_TLP_PFX_LOG_1_FOURTH_BYTE Byte 3 of Error TLP Prefix Log 1. This field contains fourth byte of First DW of TLP Prefix. Note: This register field is sticky.
23:16	RO	0x00	CFG_TLP_PFX_LOG_1_THIRD_BYTE Byte 2 of Error TLP Prefix Log 1. This field contains third byte of First DW of TLP Prefix. Note: This register field is sticky.
15:8	RO	0x00	CFG_TLP_PFX_LOG_1_SECOND_BYTE Byte 1 of Error TLP Prefix Log 1. This field contains second byte of First DW of TLP Prefix. Note: This register field is sticky.
7:0	RO	0x00	CFG_TLP_PFX_LOG_1_FIRST_BYTE Byte 0 of Error TLP Prefix Log 1. This field contains first byte of First DW of TLP Prefix. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_2_OFF

Address: Operational Base(0x00000100) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CFG_TLP_PFX_LOG_2_FOURTH_BYTE Byte 3 Error TLP Prefix Log 2. This field contains fourth byte of Second DW of TLP Prefix. Note: This register field is sticky.
23:16	RO	0x00	CFG_TLP_PFX_LOG_2_THIRD_BYTE Byte 2 Error TLP Prefix Log 2. This field contains third byte of Second DW of TLP Prefix. Note: This register field is sticky.
15:8	RO	0x00	CFG_TLP_PFX_LOG_2_SECOND_BYTE Byte 1 Error TLP Prefix Log 2. This field contains second byte of Second DW of TLP Prefix. Note: This register field is sticky.
7:0	RO	0x00	CFG_TLP_PFX_LOG_2_FIRST_BYTE Byte 0 Error TLP Prefix Log 2. This field contains first byte of Second DW of TLP Prefix. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_3_OFF

Address: Operational Base(0x00000100) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CFG_TLP_PFX_LOG_3_FOURTH_BYTE Byte 3 Error TLP Prefix Log 3. This field contains fourth byte of Third DW of TLP Prefix. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
23:16	RO	0x00	CFG_TLP_PFX_LOG_3_THIRD_BYTE Byte 2 Error TLP Prefix Log 3. This field contains third byte of Third DW of TLP Prefix. Note: This register field is sticky.
15:8	RO	0x00	CFG_TLP_PFX_LOG_3_SECOND_BYTE Byte 1 Error TLP Prefix Log 3. This field contains second byte of Third DW of TLP Prefix. Note: This register field is sticky.
7:0	RO	0x00	CFG_TLP_PFX_LOG_3_FIRST_BYTE Byte 0 Error TLP Prefix Log 3. This field contains first byte of Third DW of TLP Prefix. Note: This register field is sticky.

PCIE_DSP_PF0_AER_CAP_TLP_PREFIX_LOG_4_OFF

Address: Operational Base(0x00000100) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CFG_TLP_PFX_LOG_4_FOURTH_BYTE Byte 3 Error TLP Prefix Log 4. This field contains fourth byte of Fourth DW of TLP Prefix. Note: This register field is sticky.
23:16	RO	0x00	CFG_TLP_PFX_LOG_4_THIRD_BYTE Byte 2 Error TLP Prefix Log 4. This field contains third byte of Fourth DW of TLP Prefix. Note: This register field is sticky.
15:8	RO	0x00	CFG_TLP_PFX_LOG_4_SECOND_BYTE Byte 1 Error TLP Prefix Log 4. This field contains second byte of Fourth DW of TLP Prefix. Note: This register field is sticky.
7:0	RO	0x00	CFG_TLP_PFX_LOG_4_FIRST_BYTE Byte 0 Error TLP Prefix Log 4. This field contains first byte of Fourth DW of TLP Prefix. Note: This register field is sticky.

14.4.3.7 PCIE_DSP_PF0_SPCIE_CAP Register Description

14.4.3.7.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_SPCIE_CAP_SPCIE_CAP_HEADER_REG	0x0000	W	0x16010019	This Register provides Capability Id, Capability Version, and next Offset of SPCIE Structure.
PCIE_DSP_PF0_SPCIE_CAP_LINK_CONTROL3_REG	0x0004	W	0x00000000	This Register controls equilization and equilization interrupt.
PCIE_DSP_PF0_SPCIE_CAP_LANE_ERR_STATUS_REG	0x0008	W	0x00000000	This Register contains Lane Error Status Bits per Lane.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_SPCIE_CAP_SPCIE_CAP_OFF_0CH_REG	0x000C	W	0x00007F7F	This register provides Transmitter Preset and Receiver Preset Hint for Downstream Port and Upstream Port.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3.7.2 Detail Registers Description

PCIE_DSP_PF0_SPCIE_CAP_SPCIE_CAP_HEADER_REG

Address: Operational Base(0x00000148) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RO	0x160	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
19:16	RO	0x1	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
15:0	RO	0x0019	EXTENDED_CAP_ID Secondary PCI Express Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

PCIE_DSP_PF0_SPCIE_CAP_LINK_CONTROL3_REG

Address: Operational Base(0x00000148) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	RSVDP_2 Reserved for future use.

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Bit	Attr	Reset Value	Description
1	RW	0x0	EQ_REQ_INT_EN Link Equalization Request Interrupt Enable. This bit is RW for Downstream Ports and for Upstream Ports when Crosslink Supported is 1b. This bit is not applicable and is RsvdP for Upstream Ports when the Crosslink Supported bit is 0b. If the Port does not support 8.0 GT/s, this bit is permitted to be hardwired to 0b by the controller. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
0	RW	0x0	PERFORM_EQ Perform Equalization. This bit is RW for Downstream Ports and for Upstream Ports when Crosslink Supported is 1b. This bit is not applicable and is RsvdP for Upstream Ports when the Crosslink Supported bit is 0b. If the Port does not support 8.0 GT/s, this bit is permitted to be hardwired to 0b by the controller. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

PCIE_DSP_PF0_SPCIE_CAP_LANE_ERR_STATUS_REG

Address: Operational Base(0x00000148) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	RSVDP_LANE_ERR_STATUS Reserved for future use.
0	RW	0x0	LANE_ERR_STATUS Lane Error Status Bits per Lane. Each bit indicates if the corresponding Lane detected a Lane-based error. A value of 1b indicates that a Lane based-error was detected on the corresponding Lane Number. For Ports that are narrower than 32 Lanes, the unused upper bits [31: Maximum Link Width] are RsvdZ. For Ports that do not support 8.0 GT/s and do not set these bits based on 8b/10b errors , this field is permitted to be hardwired to 0 by the controller. Note: This register field is sticky.

PCIE_DSP_PF0_SPCIE_CAP_SPCIE_CAP_OFF_0CH_REG

Address: Operational Base(0x00000148) + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RO	0x0	RSVDP_31 Reserved for future use.
30:24	RO	0x00	reserved
23	RO	0x0	RSVDP_23 Reserved for future use.
22:16	RO	0x00	reserved
15	RO	0x0	RSVDP_15 Reserved for future use.

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Bit	Attr	Reset Value	Description
14:12	RO	0x7	USP_RX_PRESET_HINT0 Upstream Port 8.0 GT/s Receiver Preset Hint 0. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Receiver preset hint 0 value sent or received during 8.0 GT/s Link Equalization. - Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. - Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. - Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky)
11:8	RO	0xf	USP_TX_PRESET0 Upstream Port 8.0 GT/s Transmitter Preset 0. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Transmitter preset 0 value sent or received during 8.0 GT/s Link Equalization. - Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. - Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. - Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky)
7	RO	0x0	RSVDP_7 Reserved for future use.

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Bit	Attr	Reset Value	Description
6:4	RO	0x7	DSP_RX_PRESET_HINT0 Downstream Port 8.0 GT/s Receiver Preset Hint 0. Receiver preset hint 0 value that may be used as a suggested setting for 8.0 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky)
3:0	RO	0xf	DSP_TX_PRESET0 Downstream Port 8.0 GT/s Transmitter Preset 0. Transmitter preset 0 value used for 8.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky)

14.4.3.8 PCIE_DSP_PF0_L1SUB_CAP Register Description

14.4.3.8.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CAP_HEADER_REG	0x0000	W	0x1701001E	L1 Substates Extended Capability Header provides capability ID, capability version and next offset value for L1 Substates.
PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CAPABILITY_REG	0x0004	W	0x00280A1F	This register provides extended capability of L1 Substates.
PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CONTROL1_REG	0x0008	W	0x00000A00	This register Controls that the individual extended capability is enabled ot not.
PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CONTROL2_REG	0x000C	W	0x00000028	This register Controls that the individual extended capability is enabled ot not.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3.8.2 Detail Registers Description

PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CAP_HEADER_REG

Address: Operational Base(0x00000160) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:20	RO	0x170	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Capability structure or 000h, if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
19:16	RO	0x1	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field is depends on version of the specification. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
15:0	RO	0x001e	EXTENDED_CAP_ID L1SUB Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for L1 PM Substates is 001Eh. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CAPABILITY_REG

Address: Operational Base(0x00000160) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	RSVDP_24 Reserved for future use.

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Bit	Attr	Reset Value	Description
23:19	RW	0x05	PWR_ON_VALUE_SUPPORT Port T Power On Value. Along with the Port T_POWER_ON_SCALE field in the L1 PM Substates Capabilities register sets the time (in us) that this Port requires the port on the opposite side of Link to wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. The value of Port T_POWER_ON is calculated by multiplying the value in this field by the scale value in the Port T_POWER_ON_SCALE field in the L1 PM Substates Capabilities register. Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP
18	RO	0x0	RSVDP_18 Reserved for future use.
17:16	RW	0x0	PWR_ON_SCALE_SUPPORT Port T Power On Scale. Specifies the scale used for the Port T_POWER_ON_VALUE field in the L1 PM Substates Capabilities register. Range of values are given below. Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP
15:8	RW	0x0a	COMM_MODE_SUPPORT Port Common Mode Restore Time. Time (in us) required for this Port to re-establish common mode. Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP
7:5	RO	0x0	RSVDP_5 Reserved for future use.

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Bit	Attr	Reset Value	Description
4	RW	0x1	L1_PMSUB_SUPPORT L1 PM Substates ECN Supported. When Set this field indicates that this Port supports L1 PM Substates. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky)
3	RW	0x1	L1_1_ASPM_SUPPORT ASPM L11 Supported. When Set this field indicates that ASPM L1.1 is supported. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky)
2	RW	0x1	L1_2_ASPM_SUPPORT ASPM L12 Supported. When Set this field indicates that ASPM L1.2 is supported. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky)
1	RW	0x1	L1_1_PCIPM_SUPPORT PCI-PM L11 Supported. When Set this field indicates that PCI-PM L1.1 is supported, and must be Set by all Ports implementing L1 PM Substates. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky)
0	RW	0x1	L1_2_PCIPM_SUPPORT PCI-PM L12 Supported. When Set this field indicates that PCI-PM L1.2 is supported. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky)

PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CONTROL1_REG

Address: Operational Base(0x00000160) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	L1_2_TH_SCA LTR L12 Threshold Scale. This field provides a scale for the value contained within the LTR_L1.2_THRESHOLD_Value. Hardware operation is undefined if software writes a Not-Permitted value to this field. Required for all Ports Ports for which the ASPM L12 Supported bit is Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT ? RW : RSVDP
28:26	RO	0x0	RSVDP_26 Reserved for future use.

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	L1_2_TH_VAL LTR L12 Threshold Value. Along with the LTR_L1.2_THRESHOLD_Scale, this field indicates the LTR threshold used to determine if entry into L1 results in L1.1 (if enabled) or L1.2 (if enabled). Required for all Ports for which the ASPM L12 Supported bit is Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT ? RW : RSVDP
15:8	RW	0x0a	T_COMMON_MODE Common Mode Restore Time. Sets value of TCOMMONMODE (in us), which must be used by the Downstream Ports for timing the re-establishment of common mode. This field is of type RsvdP for Upstream Ports. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RW : RSVDP
7:4	RO	0x0	RSVDP_4 Reserved for future use.
3	RW	0x0	L1_1_ASPM_EN ASPM L11 Enable. When Set this field, enables ASPM L1.1. For Ports for which the ASPM L1.1 Supported bit is clear, this bit is permitted to be hardwired to 0. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set.
2	RW	0x0	L1_2_ASPM_EN ASPM L12 Enable. When Set this field, enables ASPM L1.2. For Ports for which the ASPM L1.2 Supported bit is clear, this bit is permitted to be hardwired to 0. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set.
1	RW	0x0	L1_1_PCIPM_EN PCI-PM L11 Enable. When Set this field, enables PCI-PM L1.1. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set.

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Bit	Attr	Reset Value	Description
0	RW	0x0	L1_2_PCIPM_EN PCI-PM L12 Enable. When Set this field, enables PCI-PM L1.2. For Ports for which the PCI-PM L1.2 Supported bit is clear, this bit is permitted to be hardwired to 0. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set.

PCIE_DSP_PF0_L1SUB_CAP_L1SUB_CONTROL2_REG

Address: Operational Base(0x00000160) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	RSVDP_8 Reserved for future use.
7:3	RW	0x05	T_POWER_ON_VALUE T Power On Value. Along with the T_POWER_ON_SCALE sets the minimum amount of time (in us) that the Port must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. T_POWER_ON is calculated by multiplying the value in this field by the value in the T_POWER_ON_SCALE field. Required for all Ports that support L1.2, otherwise this field is of type RsvdP.This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. The Port behavior is undefined if this field is modified when either the ASPM L1.2 Enable and/or PCI-PM L1.2 Enable bit(s) are set. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP
2	RO	0x0	RSVDP_2 Reserved for future use.
1:0	RW	0x0	T_POWER_ON_SCALE T Power On Scale. Specifies the scale used for T_POWER_ON_VALUE. Range of values are given below. Required for all Ports that support L1.2, otherwise this field is of type RsvdP. This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. The Port behavior is undefined if this field is modified when either the ASPM L1.2 Enable and/or PCI-PM L1.2 Enable bit(s) are set. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP

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14.4.3.9 PCIE_DSP_PF0_RAS_DES_CAP Register Description

14.4.3.9.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_RAS_DES_CAP_HEADER_REG	0x0000	W	0x0001000B	The Vendor-Specific Extended Capability (VSEC Capability) is an optional Extended Capability that is permitted to be implemented by any PCI Express Function or RCRB.This Register contains Capability Id, Capability Version and Next Offset value for Vendor-Specific Extended Capability.
PCIE_DSP_PF0_RAS_DES_CAP_VENDOR_SPECIFIC_HEADER_REG	0x0004	W	0x10040002	This Register field provides VSEC Length, VSEC ID and VSEC Rev(Version Number).Vendor-specific software must qualify the associated Vendor ID of the PCI Express Function or RCRB before attempting to interpret the values in the VSEC ID or VSEC Rev fields.
PCIE_DSP_PF0_RAS_DES_CAP_EVENT_COUNTER_CONTROL_REG	0x0008	W	0x00000000	This is a viewport control register. - Setting the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register determine the Event Counter data returned by the EVENT_COUNTER_DATA_REG viewport register. - Setting the EVENT_COUNTER_ENABLE field in this register enables the Event Counter selected by the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register. - Setting the EVENT_COUNTER_CLEAR field in this register clears the Event Counter selected by the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register. - Reading the EVENT_COUNTER_STATUS field in this register returns the Enable status of the Event Counter selected by the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EVENT_COUNTER_DATA_REG	0x000C	W	0x00000000	This viewport register returns the data selected by the following fields: - EVENT_COUNTER_EVENT_SELECT in EVENT_COUNTER_CONTROL_REG - EVENT_COUNTER_LANE_SELECT in EVENT_COUNTER_CONTROL_REG For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_TIME_BASED_ANALYSIS_CONTROL_REG	0x0010	W	0x00000100	Used for controlling the measurement of RX/TX data throughput and time spent in each low-power LTSSM state.For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_TIME_BASED_ANALYSIS_DATA_REG	0x0014	W	0x00000000	Contains the measurement results of RX/TX data throughput and time spent in each low-power LTSSM state.This viewport register returns the data selected by the TIME_BASED_REPORT_SELECT field in TIME_BASED_ANALYSIS_CONTROL_REG.For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_TIME_BASED_ANALYSIS_DATA_63_32_REG	0x0018	W	0x00000000	This viewport register returns the data selected by the TIME_BASED_REPORT_SELECT field in TIME_BASED_ANALYSIS_CONTROL_REG.For more details, see the "Reliability, Availability, and Serviceability (RAS)" section in the "Controller Operations" chapter of the Databook.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ_ENABLE_REG	0x0030	W	0x00000000	Each type of error insertion is enabled by the corresponding bit in this register. The specific injection controls for each type of error are defined in the following registers: - 0: CRC Error: EINJ0_CRC_REG - 1: Sequence Number Error: EINJ1_SEQNUM_REG - 2: DLLP Error: EINJ2_DLLP_REG - 3: Symbol DataK Mask Error or Sync Header Error: EINJ3_SYMBOL_REG - 4: FC Credit Update Error: EINJ4_FC_REG - 5: TLP Duplicate/Nullify Error: EINJ5_SP_TLP_REG - 6: Specific TLP Error: EINJ6_COMPARE_*_REG/EINJ6_CHANGE_*_REG/EINJ6_TLP_REGAfter the errors have been inserted by controller, it will clear each bit here.For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ0_CRC_REG	0x0034	W	0x00000000	Controls the insertion of errors into the CRC, and parity of ordered sets for the selected type of the packets as follows: - LCRC. Bad TLP will be detected at the receiver side; receiver responds with NAK DLLP; Data Link Retry starts. - 16-bit CRC of ACK/NAK DLLPs. Bad DLLP occurs at the receiver side; Replay NUM Rollover occurs. - 16-bit CRC of UpdateFC DLLPs. Error insertion continues for the specific time; LTSSM transitions to the Recovery state because of the UpdateFC timeout (if the timeout is implemented at the receiver of the UpdateFCs). - ECRC. If ECRC check is enabled, ECRC error is detected at the receiver side. - FCRC. Framing error will be detected, TLP is discarded, and the LTSSM transitions to Recovery state. - Parity of TSOS. Error insertion continues for the specific time; LTSSM Recovery/Configuration timeout will occur. - Parity of SKPOS. Lane error will be detected at the

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Name	Offset	Size	Reset Value	Description
				receiver side.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ1_SEQNUM_REG	0x0038	W	0x00000000	Controls the sequence number of the specific TLPs and ACK/NAK DLLPs.Data Link Protocol Error will be detected at the Rx side of ACK/NAL DLLPs when one of these conditions is true: - ((NEXT_TRANSMIT_SEQ -1) - AckNak_Seq_Num) mod 4096 > 2048 - (AckNak_Seq_Num - ACKD_SEQ) mod 4096 >= 2048TLP is treated as Duplicate TLP at the Rx side when all these conditions are true: - Sequence Number != NEXT_RCV_SEQ - (NEXT_RCV_SEQ - Sequence Number) mod 4096 <= 2048TLP is treated as Bad TLP at the Rx side when all these conditions are true: - Sequence Number != NEXT_RCV_SEQ and - (NEXT_RCV_SEQ - Sequence Number) mod 4096 > 2048
PCIE_DSP_PF0_RAS_DES_CAP_EINJ2_DLLP_REG	0x003C	W	0x00000000	Controls the transmission of DLLPs and inserts the following errors: - If "ACK/NAK DLLP's transmission block" is selected, replay timeout error will occur at the transmitter of the TLPs and then Data Link Retry will occur. - If "Update FC DLLP's transmission block" is selected, LTSSM will transition to the Recovery state because of the UpdateFC timeout (if the timeout is implemented at the receiver of the UpdateFCs). - If "Always Transmission for NAK DLLP" is selected, Data Link Retry will occur at the transmitter of the TLPs. Furthermore, Replay NUM Rollover will occur when the transmitter has been requested four times to send the TLP with the same sequence number.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ3_SYMBOL_REG	0x0040	W	0x00000000	When 8b/10b encoding is used, this register controls error insertion into the special (K code) symbols. - If TS1/TS2/FTS/E-Idle/SKP is selected, it affects whole of the ordered set. It might cause timeout of the LTSSM. - If END/EDB/STP/SDP is selected, TLP/DLLP will be discarded at the receiver side.When 128b/130b encoding is used, this register controls error insertion into the sync-header.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ4_FC_REG	0x0044	W	0x00000000	Controls error insertion into the credit value in the UpdateFCs. It is possible to insert errors for any of the following types: - Posted TLP Header credit - Non-Posted TLP Header credit - Completion TLP Header credit - Posted TLP Data credit - Non-Posted TLP Data credit - Completion TLP Data creditThese errors are not correctable while error insertion is enabled. Receiver buffer overflow error might occur.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ5_SP_TLP_REG	0x0048	W	0x00000000	Controls the generation of specified TLPs. Correctable errors will occur which will be fixed by the PCIe protocol. - For Duplicate TLP, the controller initiates Data Link Retry by handling ACK DLLP as NAK DLLP. These TLPs will be duplicate TLPs at the receiver side. - For Nullified TLP, the TLPs that the controller transmits are changed into nullified TLPs and the original TLPs are stored in the retry buffer. The receiver of these TLPs will detect the lack of seq# and send NAK DLLP at the next TLP. Then the original TLPs are sent from retry buffer and the data controls are recovered. For 128 bit controller or more than 128 bit, the controller inserts errors the number of times of EINJ5_COUNT but doesn't ensure that the errors are continuously inserted into TLPs.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H0_REG	0x004C	W	0x00000000	Program this register for the 1st DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW0[7:0], TLP_DW0[15:8], TLP_DW0[23:16], TLP_DW0[31:24]The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP.The type and number of errors are specified by the EINJ6_TLP_REG register.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H1_REG	0x0050	W	0x00000000	Program this register for the 2nd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW1[7:0], TLP_DW1[15:8], TLP_DW1[23:16], TLP_DW1[31:24]The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP.The type and number of errors are specified by the EINJ6_TLP_REG register.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H2_REG	0x0054	W	0x00000000	Program this register for the 3rd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW2[7:0], TLP_DW2[15:8], TLP_DW2[23:16], TLP_DW2[31:24]The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP.The type and number of errors are specified by the EINJ6_TLP_REG register.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H3_REG	0x0058	W	0x00000000	Program this register for the 4th DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW3[7:0], TLP_DW3[15:8], TLP_DW3[23:16], TLP_DW3[31:24]The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP.The type and number of errors are specified by the EINJ6_TLP_REG register.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H0_REG	0x005C	W	0x00000000	Program this register for the 1st DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW0[7:0], TLP_DW0[15:8], TLP_DW0[23:16], TLP_DW0[31:24]The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP.The type and number of errors are specified by the EINJ6_TLP_REG register.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H1_REG	0x0060	W	0x00000000	Program this register for the 2nd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW1[7:0], TLP_DW1[15:8], TLP_DW1[23:16], TLP_DW1[31:24]The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP.The type and number of errors are specified by the EINJ6_TLP_REG register.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H2_REG	0x0064	W	0x00000000	Program this register for the 3rd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW2[7:0], TLP_DW2[15:8], TLP_DW2[23:16], TLP_DW2[31:24]The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP.The type and number of errors are specified by the EINJ6_TLP_REG register.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H3_REG	0x0068	W	0x00000000	Program this register for the 4th DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW3[7:0], TLP_DW3[15:8], TLP_DW3[23:16], TLP_DW3[31:24]The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP.The type and number of errors are specified by the EINJ6_TLP_REG register.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H0_REG	0x006C	W	0x00000000	Program this register for the 1st DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW0[7:0], TLP_DW0[15:8], TLP_DW0[23:16], TLP_DW0[31:24]The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register.Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H1_REG	0x0070	W	0x00000000	Program this register for the 2nd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW1[7:0], TLP_DW1[15:8], TLP_DW1[23:16], TLP_DW1[31:24]The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register.Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H2_REG	0x0074	W	0x00000000	Program this register for the 3rd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW2[7:0], TLP_DW2[15:8], TLP_DW2[23:16], TLP_DW2[31:24]The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register.Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H3_REG	0x0078	W	0x00000000	Program this register for the 4th DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW3[7:0], TLP_DW3[15:8], TLP_DW3[23:16], TLP_DW3[31:24]The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register.Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H0_REG	0x007C	W	0x00000000	Program this register for the 1st DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW0[7:0], TLP_DW0[15:8], TLP_DW0[23:16], TLP_DW0[31:24]The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register.Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H1_REG	0x0080	W	0x00000000	Program this register for the 2nd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW1[7:0], TLP_DW1[15:8], TLP_DW1[23:16], TLP_DW1[31:24]The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register.Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H2_REG	0x0084	W	0x00000000	Program this register for the 3rd DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW2[7:0], TLP_DW2[15:8], TLP_DW2[23:16], TLP_DW2[31:24]The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register.Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H3_REG	0x0088	W	0x00000000	Program this register for the 4th DWORD of TLP header/prefix. It is necessary to carefully consider the endianness when you program this register.Bits [31:0] = TLP_DW3[7:0], TLP_DW3[15:8], TLP_DW3[23:16], TLP_DW3[31:24]The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the EINJ6_TLP_REG register.Only applies when EINJ6_INVERTED_CONTROL in EINJ6_TLP_REG =0.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_TLP_REG	0x008C	W	0x00000000	The Packet Compare Point registers (EINJ6_COMPARE_POINT*) specify which Tx TLP header bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*).When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP.The type and number of errors are specified by the this register.The Packet Change Point registers (EINJ6_CHANGE_POINT*) specify which Tx TLP header bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*).The type and number of errors are specified by the this register.Only applies when EINJ6_INVERTED_CONTROL in this register =0.The TLP into that errors are injected will not arrive at the transaction layer of the remote device when all of the following conditions are true. - Using 128b/130b encoding - Injecting errors into TLP Length field / TLP digest bit
PCIE_DSP_PF0_RAS_DES_CAP_SD_CONTROL1_REG	0x00A0	W	0x00000000	For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_CONTROL2_REG	0x00A4	W	0x00000000	For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L1LANE_REG	0x00B0	W	0x00180000	This viewport register returns the data selected by the following field: - LANE_SELECT in SD_STATUS_L1LANE_REGFor more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L1LTSSM_REG	0x00B4	W	0x00000200	For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_PM_REG	0x00B8	W	0x00000000	For more details, see the RAS DES section in the Core Operations chapter of the Databook.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L2_REG	0x00BC	W	0x00FFF000	For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L3FC_REG	0x00C0	W	0x00000000	The CREDIT_DATA[0/1] fields in this viewport register return the data for the VC and TLP Type selected by the following fields: - CREDIT_SEL_VC - CREDIT_SEL_CREDIT_TYPE - CREDIT_SEL_TLP_TYPE - CREDIT_SEL_HDFor more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L3_REG	0x00C4	W	0x00000000	Silicon Debug Status(Layer3).For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_CONTROL1_REG	0x00D0	W	0x00000000	This is a viewport control register. Setting the EQ_RATE_SEL and EQ_LANE_SEL fields in this register determine the per-lane Silicon Debug EQ Status data returned by the SD_EQ_STATUS[1/2/3] viewport registers.For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_CONTROL2_REG	0x00D4	W	0x00000000	This viewport register returns the value for the rate and lane selected by the EQ_RATE_SEL and EQ_LANE_SEL fields in the SD_EQ_CONTROL1_REG register.For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_CONTROL3_REG	0x00D8	W	0x00000000	This viewport register returns the value for the rate and lane selected by the EQ_RATE_SEL and EQ_LANE_SEL fields in the SD_EQ_CONTROL1_REG register.For more details, see the RAS DES section in the Core Operations chapter of the Databook.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_STATUS1_REG	0x00E0	W	0x00000000	This viewport register returns the first of three words of Silicon Debug EQ Status data for the rate and lane selected by the EQ_RATE_SEL and EQ_LANE_SEL fields in the SD_EQ_CONTROL1_REG register.The following fields are available when Equalization finished unsuccessfully(EQ_CONVERGENCE_INFO=2). - EQ_RULEA_VIOLATION - EQ_RULEB_VIOLATION - EQ_RULEC_VIOLATION - EQ_REJECT_EVENTFor more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_STATUS2_REG	0x00E4	W	0x00000000	This viewport register returns the second of three words of Silicon Debug EQ Status data for the rate and lane selected by the EQ_RATE_SEL and EQ_LANE_SEL fields in the SD_EQ_CONTROL1_REG register.Each field is available when Equalization finished successfully(EQ_CONVERGENCE_INFO=1).For more details, see the RAS DES section in the Core Operations chapter of the Databook.
PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_STATUS3_REG	0x00E8	W	0x00000000	This viewport register returns the third of three words of Silicon Debug EQ Status data for the rate and lane selected by the EQ_RATE_SEL and EQ_LANE_SEL fields in the SD_EQ_CONTROL1_REG register.Each field is available when Equalization finished successfully(EQ_CONVERGENCE_INFO=1).For more details, see the RAS DES section in the Core Operations chapter of the Databook.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3.9.2 Detail Registers Description

PCIE_DSP_PF0_RAS_DES_CAP_RAS_DES_CAP_HEADER_REG

Address: Operational Base(0x00000170) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
19:16	RO	0x1	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Value of this field is depends on the version of the specification. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
15:0	RO	0x000b	EXTENDED_CAP_ID PCI Express Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Vendor-Specific Extended Capability is 000Bh. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_VENDOR_SPECIFIC_HEADER_REG

Address: Operational Base(0x00000170) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:20	RO	0x100	VSEC_LENGTH VSEC Length. This field indicates the number of bytes in the entire VSEC structure, including the Vendor-Specific Extended Capability Header, the Vendor-Specific Header, and the vendor-specific registers.
19:16	RO	0x4	VSEC_REV VSEC Rev. This field is a vendor-defined version number that indicates the version of the VSEC structure. Software must qualify the Vendor ID and VSEC ID before interpreting this field.

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Bit	Attr	Reset Value	Description
15:0	RO	0x0002	VSEC_ID VSEC ID. This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure. Software must qualify the Vendor ID before interpreting this field.

PCIE_DSP_PF0_RAS_DES_CAP_EVENT_COUNTER_CONTROL_REG

Address: Operational Base(0x00000170) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	RSVDP_28 Reserved for future use.
27:16	RW	0x000	EVENT_COUNTER_EVENT_SELECT Event Counter Data Select. This field in conjunction with the EVENT_COUNTER_LANE_SELECT field indexes the Event Counter data returned by the EVENT_COUNTER_DATA_REG register. - 27-24: Group number(4-bit: 0..0x7) - 23-16: Event number(8-bit: 0..0x13) within the Group - .. For detailed definitions of Group number and Event number, see the RAS DES chapter in the Databook. Note: This register field is sticky.
15:12	RO	0x0	RSVDP_12 Reserved for future use.
11:8	RW	0x0	EVENT_COUNTER_LANE_SELECT Event Counter Lane Select. This field in conjunction with EVENT_COUNTER_EVENT_SELECT indexes the Event Counter data returned by the EVENT_COUNTER_DATA_REG register. Note: This register field is sticky.
7	RO	0x0	EVENT_COUNTER_STATUS Event Counter Status. This register returns the current value of the Event Counter selected by the following fields: - EVENT_COUNTER_EVENT_SELECT - EVENT_COUNTER_LANE_SELECT Note: This register field is sticky.
6:5	RO	0x0	RSVDP_5 Reserved for future use.
4:2	WO	0x0	EVENT_COUNTER_ENABLE Event Counter Enable. Enables/disables the Event Counter selected by the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register. By default, all event counters are disabled. You can enable/disable a specific Event Counter by writing the 'per event off' or 'per event on' codes. You can enable/disable all event counters by writing the 'all on' or 'all off' codes. The read value is always '0'. For other values no change.

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Bit	Attr	Reset Value	Description
1:0	WO	0x0	EVENT_COUNTER_CLEAR Event Counter Clear. Clears the Event Counter selected by the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register. You can clear the value of a specific Event Counter by writing the 'per clear' code and you can clear all event counters at once by writing the 'all clear' code. The read value is always '0'. Other values are reserved.

PCIE_DSP_PF0_RAS_DES_CAP_EVENT_COUNTER_DATA_REG

Address: Operational Base(0x00000170) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EVENT_COUNTER_DATA Event Counter Data. This register returns the data selected by the following fields: - EVENT_COUNTER_EVENT_SELECT in EVENT_COUNTER_CONTROL_REG Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_TIME_BASED_ANALYSIS_CONTROL_REG

Address: Operational Base(0x00000170) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	TIME_BASED_REPORT_SELECT Time-based Report Select. Selects what type of data is measured for the selected duration (TIME_BASED_DURATION_SELECT), and returned in TIME_BASED_ANALYSIS_DATA. Each type of data is measured using one of three types of units: - Core_clk Cycles for 2.5GT/s, 5.0GT/s, 8.0GT/s, 16.0GT/s, 32GT/s. Total time in ps is [Value of TIME_BASED_ANALYSIS_DATA returned when TIME_BASED_REPORT_SELECT=0x00] * TIME_BASED_ANALYSIS_DATA. Values 0-4 and 7-8 correspond to Core_clk Cycles for 2.5GT/s, 5.0GT/s, 8.0GT/s, 16.0GT/s, 32GT/s. - Aux_clk Cycles. Total time in ps is [Period of platform specific clock] * TIME_BASED_ANALYSIS_DATA. Values 5, 6, and 9 correspond to aux_clk Cycles. - Core_clk Cycles for 20GT/s, 25GT/s (CCIX ESM data rate). Total time in ps is [Value of TIME_BASED_ANALYSIS_DATA returned when TIME_BASED_REPORT_SELECT=0x10] * TIME_BASED_ANALYSIS_DATA. Values 10-14 and 17-18 correspond to Core_clk Cycles for 2.5GT/s, 5.0GT/s, 8.0GT/s, 16.0GT/s, 32GT/s. - Data Bytes. Actual amount of bytes is 16 * TIME_BASED_ANALYSIS_DATA. Values 20-23 correspond to data bytes. All encodings other than the defined encodings are reserved. Note: This register field is sticky.
23:16	RO	0x00	RSVDP_16 Reserved for future use.

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Bit	Attr	Reset Value	Description
15:8	RW	0x01	TIME_BASED_DURATION_SELECT Time-based Duration Select. Selects the duration of time-based analysis. When "manual control" is selected and TIMER_START is set to '1', this analysis never stops until TIMER_STOP is set to '0'. All encodings other than the defined encodings are reserved. Note: This register field is sticky.
7:1	RO	0x00	RSVDP_1 Reserved for future use.
0	RW	0x0	TIMER_START Timer Start. This bit will be cleared automatically when the measurement is finished. Note: The app_ras_des_tba_ctrl input also sets the contents of this field and controls the measurement start/stop. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_TIME_BASED_ANALYSIS_DATA_REG

Address: Operational Base(0x00000170) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TIME_BASED_ANALYSIS_DATA Time Based Analysis Data. This register returns the data selected by the TIME_BASED_REPORT_SELECT field in TIME_BASED_ANALYSIS_CONTROL_REG. The results are cleared when next measurement starts. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_TIME_BASED_ANALYSIS_DATA_63_32_REG

Address: Operational Base(0x00000170) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TIME_BASED_ANALYSIS_DATA_63_32 Upper 32 bits of Time Based Analysis Data. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ_ENABLE_REG

Address: Operational Base(0x00000170) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	RSVDP_7 Reserved for future use.

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Bit	Attr	Reset Value	Description
6	RW	0x0	ERROR_INJECTION6_ENABLE Error Injection6 Enable (Specific TLP Error). Enables insertion of errors into the packets that you select. You can set this bit to '1' when you have disabled RAS datapath protection (DP) by setting CX_RASDP = CX_RASDP_RAM_PROT =0. You can set this bit to '1' when you have disabled the address translation by setting ADDR_TRANSLATION_SUPPORT_EN=0. For more details, see the EINJ6_COMPARE_*_REG/EINJ6_CHANGE_*_REG/EINJ6_TLP_REG registers. Note: This register field is sticky.
5	RW	0x0	ERROR_INJECTION5_ENABLE Error Injection5 Enable (TLP Duplicate/Nullify Error). Enables insertion of duplicate/nullified TLPs. For more details, see the EINJ5_SP_TLP_REG register. Note: This register field is sticky.
4	RW	0x0	ERROR_INJECTION4_ENABLE Error Injection4 Enable (FC Credit Update Error). Enables insertion of errors into UpdateFCs. For more details, see the EINJ4_FC_REG register. Note: This register field is sticky.
3	RW	0x0	ERROR_INJECTION3_ENABLE Error Injection3 Enable (Symbol DataK Mask Error or Sync Header Error). Enables DataK masking of special symbols or the breaking of the sync header. For more details, see the EINJ3_SYMBOL_REG register. Note: This register field is sticky.
2	RW	0x0	ERROR_INJECTION2_ENABLE Error Injection2 Enable (DLLP Error). Enables insertion of DLLP errors. For more details, see the EINJ2_DLLP_REG register. Note: This register field is sticky.
1	RW	0x0	ERROR_INJECTION1_ENABLE Error Injection1 Enable (Sequence Number Error). Enables insertion of errors into sequence numbers. For more details, see the EINJ1_SEQNUM_REG register. Note: This register field is sticky.
0	RW	0x0	ERROR_INJECTION0_ENABLE Error Injection0 Enable (CRC Error). Enables insertion of errors into various CRC. For more details, see the EINJ0_CRC_REG register. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ0_CRC_REG

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Address: Operational Base(0x00000170) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	RSVDP_12 Reserved for future use.
11:8	RW	0x0	EINJ0_CRC_TYPE Error injection type. Selects the type of CRC error to be inserted. All encodings other than the defined encodings are reserved. Note: This register field is sticky.
7:0	RW	0x00	EINJ0_COUNT Error injection count. Indicates the number of errors. This register is decremented when the errors have been inserted. - If the counter value is 0x01 and error is inserted, ERROR_INJECTION0_ENABLE in EINJ_ENABLE_REG returns 0b. - If the counter value is 0x00 and ERROR_INJECTION0_ENABLE=1, the errors are inserted until ERROR_INJECTION0_ENABLE is set to '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ1_SEQNUM_REG

Address: Operational Base(0x00000170) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	RSVDP_29 Reserved for future use.
28:16	RW	0x0000	EINJ1_BAD_SEQNUM Bad sequence number. Indicates the value to add/subtract from the naturally-assigned sequence numbers. This value is represented by two's complement. For example: - Set Type, SEQ# and Count -- EINJ1_SEQNUM_TYPE =0 (Insert errors into new TLPs) -- EINJ1_BAD_SEQNUM =0x1FFD (represents -3) -- EINJ1_COUNT =1 - Enable Error Injection -- ERROR_INJECTION1_ENABLE =1 - Send a TLP From the Core's Application Interface -- Assume SEQ#5 is given to the TLP. - The SEQ# is Changed to #2 by the Error Injection Function in Layer2. -- 5 + (-3) = 2 - The TLP with SEQ#2 is Transmitted to PCIe Link. Note: This register field is sticky.
15:9	RO	0x00	RSVDP_9 Reserved for future use.
8	RW	0x0	EINJ1_SEQNUM_TYPE Sequence number type. Selects the type of sequence number. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	EINJ1_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. - If the counter value is 0x01 and error is inserted, ERROR_INJECTION1_ENABLE in EINJ_ENABLE_REG returns '0'. - If the counter value is 0x00 and ERROR_INJECTION1_ENABLE=1, the errors are inserted until ERROR_INJECTION1_ENABLE is set to '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ2_DLLP_REG

Address: Operational Base(0x00000170) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	RSVDP_10 Reserved for future use.
9:8	RW	0x0	EINJ2_DLLP_TYPE DLLP Type. Selects the type of DLLP errors to be inserted. Note: This register field is sticky.
7:0	RW	0x00	EINJ2_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. - If the counter value is 0x01 and the error is inserted, ERROR_INJECTION2_ENABLE in EINJ_ENABLE_REG returns '0'. - If the counter value is 0x00 and ERROR_INJECTION2_ENABLE =1, the errors are inserted until ERROR_INJECTION2_ENABLE is set to '0'. This register is affected only when EINJ2_DLLP_TYPE =2'10b. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ3_SYMBOL_REG

Address: Operational Base(0x00000170) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	RSVDP_11 Reserved for future use.
10:8	RW	0x0	EINJ3_SYMBOL_TYPE Error Type. 8b/10b encoding - Mask K symbol. It is not supported to insert errors into the first ordered-set after exiting from TxElecIdle when CX_FREQ_STEP_EN has been enabled. All encodings other than the defined encodings are reserved. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	EINJ3_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. - If the counter value is 0x01 and error is inserted, ERROR_INJECTION3_ENABLE in EINJ_ENABLE_REG returns '0'. - If the counter value is 0x00 and ERROR_INJECTION3_ENABLE =1, the errors are inserted until ERROR_INJECTION3_ENABLE is set to '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ4_FC_REG

Address: Operational Base(0x00000170) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	RSVDP_29 Reserved for future use.
28:16	RW	0x0000	EINJ4_BAD_UPDFC_VALUE Bad update-FC credit value. Indicates the value to add/subtract from the UpdateFC credit. This value is represented by two's complement. Note: This register field is sticky.
15	RO	0x0	RSVDP_15 Reserved for future use.
14:12	RW	0x0	EINJ4_VC_NUMBER VC Number. Indicates target VC Number. Note: This register field is sticky.
11	RO	0x0	RSVDP_11 Reserved for future use.
10:8	RW	0x0	EINJ4_UPDFC_TYPE Update-FC type. Selects the credit type. Note: This register field is sticky.
7:0	RW	0x00	EINJ4_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. - If the counter value is 0x01 and error is inserted, ERROR_INJECTION4_ENABLE in EINJ_ENABLE_REG returns '0'. - If the counter value is 0x00 and ERROR_INJECTION4_ENABLE =1, the errors are inserted until ERROR_INJECTION4_ENABLE is set to '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ5_SP_TLP_REG

Address: Operational Base(0x00000170) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	RSVDP_9 Reserved for future use.

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Bit	Attr	Reset Value	Description
8	RW	0x0	EINJ5_SPECIFIED_TLP Specified TLP. Selects the specified TLP to be inserted. Note: This register field is sticky.
7:0	RW	0x00	EINJ5_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. - If the counter value is 0x01 and error is inserted, ERROR_INJECTION5_ENABLE in EINJ_ENABLE_REG returns '0'. - If the counter value is 0x00 and ERROR_INJECTION5_ENABLE =1, the errors are inserted until ERROR_INJECTION5_ENABLE is set to '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H0_REG

Address: Operational Base(0x00000170) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H0 Packet Compare Point: 1st DWORD. Specifies which Tx TLP header DWORD#0 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H1_REG

Address: Operational Base(0x00000170) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H1 Packet Compare Point: 2nd DWORD. Specifies which Tx TLP header DWORD#1 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H2_REG

Address: Operational Base(0x00000170) + offset (0x0054)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H2 Packet Compare Point: 3rd DWORD. Specifies which Tx TLP header DWORD#2 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_POINT_H3_REG

Address: Operational Base(0x00000170) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H3 Packet Compare Point: 4th DWORD. Specifies which Tx TLP header DWORD#3 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H0_REG

Address: Operational Base(0x00000170) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H0 Packet Compare Value: 1st DWORD. Specifies the value to compare against Tx the TLP header DWORD#0 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H1_REG

Address: Operational Base(0x00000170) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H1 Packet Compare Value: 2nd DWORD. Specifies the value to compare against Tx the TLP header DWORD#1 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H2_REG

Address: Operational Base(0x00000170) + offset (0x0064)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H2 Packet Compare Value: 3rd DWORD. Specifies the value to compare against Tx the TLP header DWORD#2 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_COMPARE_VALUE_H3_REG

Address: Operational Base(0x00000170) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H3 Packet Compare Value: 4th DWORD. Specifies the value to compare against Tx the TLP header DWORD#3 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H0_REG

Address: Operational Base(0x00000170) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H0 Packet Change Point: 1st DWORD. Specifies which Tx TLP header DWORD#0 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H1_REG

Address: Operational Base(0x00000170) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H1 Packet Change Point: 2nd DWORD. Specifies which Tx TLP header DWORD#1 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H2_REG

Address: Operational Base(0x00000170) + offset (0x0074)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H2 Packet Change Point: 3rd DWORD. Specifies which Tx TLP header DWORD#2 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_POINT_H3_REG

Address: Operational Base(0x00000170) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H3 Packet Change Point: 4th DWORD. Specifies which Tx TLP header DWORD#3 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H0_REG

Address: Operational Base(0x00000170) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H0 Packet Change Value: 1st DWORD. Specifies replacement values for the Tx TLP header DWORD#0 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H1_REG

Address: Operational Base(0x00000170) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H1 Packet Change Value: 2nd DWORD. Specifies replacement values for the Tx TLP header DWORD#1 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H2_REG

Address: Operational Base(0x00000170) + offset (0x0084)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H2 Packet Change Value: 3rd DWORD. Specifies replacement values for the Tx TLP header DWORD#2 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_CHANGE_VALUE_H3_REG

Address: Operational Base(0x00000170) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H3 Packet Change Value: 4th DWORD. Specifies replacement values for the Tx TLP header DWORD#3 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_EINJ6_TLP_REG

Address: Operational Base(0x00000170) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	RSVDP_12 Reserved for future use.
11:9	RW	0x0	EINJ6_PACKET_TYPE Packet type. Selects the TLP packets to inject errors into. All encodings other than the specified encodings are reserved. Note: This register field is sticky.
8	RW	0x0	EINJ6_INVERTED_CONTROL Inverted Error Injection Control. Encodded vlues given as above. Note: This register field is sticky.
7:0	RW	0x00	EINJ6_COUNT Error Injection Count. Indicates the number of errors to insert. This counter is decremented while errors are been inserted. - If the counter value is 0x01 and error is inserted, ERROR_INJECTION6_ENABLE in EINJ_ENABLE_REG returns '0'. - If the counter value is 0x00 and ERROR_INJECTION6_ENABLE=1, errors are inserted until ERROR_INJECTION6_ENABLE is set to '0'. Note: This register field is sticky.

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PCIE_DSP_PF0_RAS_DES_CAP_SD_CONTROL1_REG

Address: Operational Base(0x00000170) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	RSVDP_24 Reserved for future use.
23:22	RW	0x0	LOW_POWER_INTERVAL Low Power Entry Interval Time. Interval Time that the controller starts monitoring RXELECIDLE signal after L0s/L1/L2 entry. You should set the value according to the latency from receiving EIOS to, RXELECIDLE assertion at the PHY. Note: This register field is sticky.
21:20	RW	0x0	TX_EIOS_NUM Number of Tx EIOS. This register sets the number of transmit EIOS for L0s/L1 entry and Disable/Loopback/Hot-reset exit. The controller selects the greater value between this register and the value defined by the PCI-SIG specification. Note: This register field is sticky.
19:17	RO	0x0	RSVDP_17 Reserved for future use.
16	RW	0x0	FORCE_DETECT_LANE_EN Force Detect Lane Enable. Note: This register field is sticky.
15:0	RW	0x0000	FORCE_DETECT_LANE Force Detect Lane. When the FORCE_DETECT_LANE_EN field is set, the controller ignores receiver detection from PHY during LTSSM Detect state and uses this value instead. Value represents lane number. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_CONTROL2_REG

Address: Operational Base(0x00000170) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	RSVDP_17 Reserved for future use.
16	RW	0x0	FRAMING_ERR_RECOVERY_DISABLE Framing Error Recovery Disable. This bit disables a transition to Recovery state when a Framing Error is occurred. Note: This register field is sticky.
15:11	RO	0x00	RSVDP_11 Reserved for future use.
10	RW	0x0	DIRECT_LPBKSLV_TO_EXIT Direct Loopback Slave To Exit. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
9	RW	0x0	DIRECT_POLCOMP_TO_DETECT Direct Polling.Compliance to Detect. Note: This register field is sticky.
8	RW	0x0	DIRECT_RECIDLE_TO_CONFIG Direct Recovery.Idle to Configuration. Note: This register field is sticky.
7:3	RO	0x00	RSVDP_3 Reserved for future use.
2	RW	0x0	NOACK_FORCE_LINKDOWN Force LinkDown. Note: This register field is sticky.
1	WO	0x0	RECOVERY_REQUEST Recovery Request.
0	RW	0x0	HOLD_LTSSM Hold and Release LTSSM. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L1LANE_REG

Address: Operational Base(0x00000170) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DESKEW_POINTER Deskew Pointer. Indicates Deskew pointer of internal Deskew buffer of selected lane number(LANE_SELECT). Note: This register field is sticky.
23:21	RO	0x0	RSVDP_21 Reserved for future use.
20	RO	0x1	PIPE_TXELECIDLE PIPE:TxElecIdle. Indicates PIPE TXELECIDLE signal of selected lane number(LANE_SELECT). Note: This register field is sticky.
19	RO	0x1	PIPE_RXELECIDLE PIPE:RxElecIdle. Indicates PIPE RXELECIDLE signal of selected lane number(LANE_SELECT). Note: This register field is sticky.
18	RO	0x0	PIPE_RXVALID PIPE:RxValid. Indicates PIPE RXVALID signal of selected lane number(LANE_SELECT). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
17	RO	0x0	PIPE_DETECT_LANE PIPE:Detect Lane. Indicates whether PHY indicates receiver detection or not on selected lane number(LANE_SELECT). Note: This register field is sticky.
16	RO	0x0	PIPE_RXPOLARITY PIPE:RxPolarity. Indicates PIPE RXPOLARITY signal of selected lane number(LANE_SELECT). Note: This register field is sticky.
15:4	RO	0x000	RSVDP_4 Reserved for future use.
3:0	RW	0x0	LANE_SELECT Lane Select. Lane Select register for Silicon Debug Status Register of Layer1-PerLane. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L1LTSSM_REG

Address: Operational Base(0x00000170) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	LTSSM_VARIABLE LTSSM Variable. Indicates internal LTSSM variables defined in the PCI Express Base Specification. For other value idle_to_rlock_transitioned. Note: This register field is sticky.
15	RO	0x0	LANE_REVERSAL Lane Reversal Operation. Receiver detected lane reversal. This field is only valid in the L0 LTSSM state. Note: This register field is sticky.
14:11	RO	0x0	RSVDP_11 Reserved for future use.
10:8	RO	0x2	PIPE_POWER_DOWN PIPE:PowerDown. Indicates PIPE PowerDown signal. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
7	RW	0x0	FRAMING_ERR Framing Error. Indicates Framing Error detection status. Note: This register field is sticky.
6:0	RO	0x00	FRAMING_ERR_PTR First Framing Error Pointer. Identifies the first Framing Error using the following encoding. The field contents are only valid value when FRAMING_ERR =1. - Received Unexpected Framing Token (Values 01h to 06h) - Received Unexpected STP Token (Values 11h to 13h) - Received Unexpected Block (Values 21h to 2Eh) All encodings other than the defined encodings are reserved. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_PM_REG

Address: Operational Base(0x00000170) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	RSVDP_24 Reserved for future use.
23:16	RO	0x00	LATCHED_NFTS Latched N_FTS. Indicates the value of N_FTS in the received TS Ordered Sets from the Link Partner. Note: This register field is sticky.
15:13	RO	0x0	L1SUB_STATE L1Sub State. Indicates internal state machine of L1Sub state. Note: This register field is sticky.
12	RW	0x0	PME_RESEND_FLAG PME Re-send flag. When the DUT sends a PM_PME message TLP, the DUT sets PME_Status bit. If host software does not clear PME_Status bit for 100ms(+50%/-5%), the DUT resends the PM_PME Message. This bit indicates that a PM_PME was resent. Note: This register field is sticky.
11:8	RO	0x0	INTERNAL_PM_SSTATE Internal PM State(Slave). Indicates internal state machine of Power Management Slave controller. Note: This register field is sticky.
7:5	RO	0x0	RSVDP_5 Reserved for future use.

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Bit	Attr	Reset Value	Description
4:0	RO	0x00	INTERNAL_PM_MSTATE Internal PM State(Master). Indicates internal state machine of Power Management Master controller. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L2_REG

Address: Operational Base(0x00000170) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	RSVDP_28 Reserved for future use.
27	RO	0x0	FC_INIT2 FC_INIT2. Indicates the controller is in FC_INIT2(VC0) state. Note: This register field is sticky.
26	RO	0x0	FC_INIT1 FC_INIT1. Indicates the controller is in FC_INIT1(VC0) state. Note: This register field is sticky.
25:24	RO	0x0	DLCMSM DLCMSM. Indicates the current DLCMSM. Note: This register field is sticky.
23:12	RO	0xfff	RX_ACK_SEQ_NO Tx Ack Sequence Number. Indicates ACKD_SEQ which is updated by receiving ACK/NAK DLLP. Note: This register field is sticky.
11:0	RO	0x000	TX_TLP_SEQ_NO Tx Tlp Sequence Number. Indicates next transmit sequence number for transmit TLP. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L3FC_REG

Address: Operational Base(0x00000170) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	CREDIT_DATA1 Credit Data1. Current FC credit data selected by the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields. - Rx: Credit Allocated Value - Tx: Credit Limit Value. This value is valid when DLCMSM=0x3(DL_ACTIVE). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
19:8	RO	0x000	CREDIT_DATA0 Credit Data0. Current FC credit data selected by the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields. - Rx: Credit Received Value - Tx: Credit Consumed Value Note: This register field is sticky.
7	RO	0x0	RSVDP_7 Reserved for future use.
6	RW	0x0	CREDIT_SEL_HD Credit Select(HeaderData). This field in conjunction with the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, and CREDIT_SEL_TLP_TYPE viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky.
5:4	RW	0x0	CREDIT_SEL_TLP_TYPE Credit Select(TLP Type). This field in conjunction with the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, and CREDIT_SEL_HD viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky.
3	RW	0x0	CREDIT_SEL_CREDIT_TYPE Credit Select(Credit Type). This field in conjunction with the CREDIT_SEL_VC, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky.
2:0	RW	0x0	CREDIT_SEL_VC Credit Select(VC). This field in conjunction with the CREDIT_SEL_CREDIT_TYPE, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_STATUS_L3_REG

Address: Operational Base(0x00000170) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	RSVDP_8 Reserved for future use.
7	RW	0x0	MFTLP_STATUS Malformed TLP Status. Indicates malformed TLP has occurred. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
6:0	RO	0x00	MFTLP_POINTER First Malformed TLP Error Pointer. Indicates the element of the received first malformed TLP. This pointer is validated by MFTLP_STATUS. All encodings other than the defined encodings are reserved. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_CONTROL1_REG

Address: Operational Base(0x00000170) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	FOM_TARGET FOM Target. Indicates figure of merit target criteria value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2). This field is only valid when GEN3_EQ_FB_MODE is 0001b(Figure Of Merit). Note: This register field is sticky.
23	RW	0x0	FOM_TARGET_ENABLE FOM Target Enable. Enables the FOM_TARGET fields. Note: This register field is sticky.
22:18	RO	0x00	RSVDP_18 Reserved for future use.
17:16	RW	0x0	EVAL_INTERVAL_TIME Eval Interval Time. Indicates interval time of RxEqEval assertion. This field is used for EQ Master(DSP in EQ Phase3/USP in EQ Phase2). Note: This register field is sticky.
15:10	RO	0x00	RSVDP_10 Reserved for future use.
9:8	RW	0x0	EXT_EQ_TIMEOUT Extends EQ Phase2/3 Timeout. This field is used when the LTSSM is in Recovery.EQ2/3. When this field is set, the value of EQ2/3 timeout is extended. Note: This register field is sticky.
7:6	RO	0x0	RSVDP_6 Reserved for future use.
5:4	RW	0x0	EQ_RATE_SEL EQ Status Rate Select. Setting this field in conjunction with the EQ_LANE_SEL field determines the per-lane Silicon Debug EQ Status data returned by the SD_EQ_CONTROL[2/3] and SD_EQ_STATUS[1/2/3] viewport registers. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	EQ_LANE_SEL EQ Status Lane Select. Setting this field in conjunction with the EQ_RATE_SEL field determines the per-lane Silicon Debug EQ Status data returned by the SD_EQ_CONTROL[2/3] and SD_EQ_STATUS[1/2/3] viewport registers. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_CONTROL2_REG

Address: Operational Base(0x00000170) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31	RO	0x0	RSVDP_31 Reserved for future use.
30	RW	0x0	FORCE_LOCAL_TX_PRESET_ENABLE Force Local Transmitter Preset Enable. Enables the FORCE_LOCAL_TX_PRESET field. If select rate in the EQ_RATE_SEL field is 32.0GT/s Speed, this feature is not available. Note: This register field is sticky.
29	RW	0x0	FORCE_LOCAL_RX_HINT_ENABLE Force Local Receiver Preset Hint Enable. Enables the FORCE_LOCAL_RX_HINT field. If select rate in the EQ_RATE_SEL field is other than 8.0GT/s Speed, this feature is not available. Note: This register field is sticky.
28	RW	0x0	FORCE_LOCAL_TX_COEF_ENABLE Force Local Transmitter Coefficient Enable. Enables the following fields: - FORCE_LOCAL_TX_PRE_CURSOR - FORCE_LOCAL_TX_CURSOR - FORCE_LOCAL_TX_POST_CURSOR Note: This register field is sticky.
27:24	RW	0x0	FORCE_LOCAL_TX_PRESET Force Local Transmitter Preset. Indicates initial preset value of USP in EQ Slave(EQ Phase2) instead of receiving EQ TS2. If select rate in the EQ_RATE_SEL field is 32.0GT/s Speed, this feature is not available. Note: This register field is sticky.
23:21	RO	0x0	RSVDP_21 Reserved for future use.
20:18	RW	0x0	FORCE_LOCAL_RX_HINT Force Local Receiver Preset Hint. Indicates the RxPresetHint value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of received or set value. If select rate in the EQ_RATE_SEL field is other than 8.0GT/s Speed, this feature is not available. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
17:12	RW	0x00	FORCE_LOCAL_TX_POST_CURSOR Force Local Transmitter Post-Cursor. Indicates the coefficient value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of the value instructed from link partner. Note: This register field is sticky.
11:6	RW	0x00	FORCE_LOCAL_TX_CURSOR Force Local Transmitter Cursor. Indicates the coefficient value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of the value instructed from link partner. Note: This register field is sticky.
5:0	RW	0x00	FORCE_LOCAL_TX_PRE_CURSOR Force Local Transmitter Pre-cursor. Indicates the coefficient value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of the value instructed from link partner. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_CONTROL3_REG

Address: Operational Base(0x00000170) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	RSVDP_29 Reserved for future use.
28	RW	0x0	FORCE_REMOTE_TX_COEF_ENABLE Force Remote Transmitter Coefficient Enable. Enables the following fields: - FORCE_REMOTE_TX_PRE_CURSOR - FORCE_REMOTE_TX_CURSOR - FORCE_REMOTE_TX_POST_CURSOR This function can only be used when GEN3_EQ_FB_MODE = 0000b(Direction Change) Note: This register field is sticky.
27:18	RO	0x000	RSVDP_18 Reserved for future use.
17:12	RW	0x00	FORCE_REMOTE_TX_POST_CURSOR Force Remote Transmitter Post-Cursor. Indicates the coefficient value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2), instead of the value instructed from local phy in dirchange mode. Note: This register field is sticky.
11:6	RW	0x00	FORCE_REMOTE_TX_CURSOR Force Remote Transmitter Cursor. Indicates the coefficient value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2), instead of the value instructed from local phy in dirchange mode. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
5:0	RW	0x00	FORCE_REMOTE_TX_PRE_CURSOR Force Remote Transmitter Pre-Cursor. Indicates the coefficient value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2), instead of the value instructed from local phy in dirchange mode. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_STATUS1_REG

Address: Operational Base(0x00000170) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	RSVDP_8 Reserved for future use.
7	RO	0x0	EQ_REJECT_EVENT EQ Reject Event. Indicates that the controller receives two consecutive TS1 OS w/Reject=1b during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky.
6	RO	0x0	EQ_RULEC_VIOLATION EQ Rule C Violation. Indicates that coefficients rule C violation is detected in the values provided by PHY using direction change method during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). The coefficients rule C correspond to the rules c) from section "Rules for Transmitter Coefficents" in the PCI Express Base Specification. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky.
5	RO	0x0	EQ_RULEB_VIOLATION EQ Rule B Violation. Indicates that coefficients rule B violation is detected in the values provided by PHY using direction change method during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). The coefficients rules B correspond to the rules b) from section "Rules for Transmitter Coefficents" in the PCI Express Base Specification. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
4	RO	0x0	EQ_RULEA_VIOLATION EQ Rule A Violation. Indicates that coefficients rule A violation is detected in the values provided by PHY using direction change method during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). The coefficients rules A correspond to the rules a) from section "Rules for Transmitter Coefficents" in the PCI Express Base Specification. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky.
3	RO	0x0	RSVDP_3 Reserved for future use.
2:1	RO	0x0	EQ_CONVERGENCE_INFO EQ Convergence Info. Indicates equalization convergence information. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky.
0	RO	0x0	EQ_SEQUENCE EQ Sequence. Indicates that the controller is starting the equalization sequence. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_STATUS2_REG

Address: Operational Base(0x00000170) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EQ_LOCAL_FOM_VALUE EQ Local Figure of Merit. Indicates Local maximum Figure of Merit value. Note: This register field is sticky.
23:21	RO	0x0	RSVDP_21 Reserved for future use.
20:18	RO	0x0	EQ_LOCAL_RX_HINT EQ Local Receiver Preset Hint. Indicates Local Receiver Preset Hint value. If select rate in the EQ_RATE_SEL field is other than 8.0GT/s Speed, this feature is not available. Note: This register field is sticky.
17:12	RO	0x00	EQ_LOCAL_POST_CURSOR EQ Local Post-Cursor. Indicates Local post cursor coefficient value. Note: This register field is sticky.
11:6	RO	0x00	EQ_LOCAL_CURSOR EQ Local Cursor. Indicates Local cursor coefficient value. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
5:0	RO	0x00	EQ_LOCAL_PRE_CURSOR EQ Local Pre-Cursor. Indicates Local pre cursor coefficient value. Note: This register field is sticky.

PCIE_DSP_PF0_RAS_DES_CAP_SD_EQ_STATUS3_REG

Address: Operational Base(0x00000170) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	RSVDP_30 Reserved for future use.
29:24	RO	0x00	EQ_REMOTE_FS EQ Remote FS. Indicates Remote FS value. Note: This register field is sticky.
23:18	RO	0x00	EQ_REMOTE_LF EQ Remote LF. Indicates Remote LF value. Note: This register field is sticky.
17:12	RO	0x00	EQ_REMOTE_POST_CURSOR EQ Remote Post-Cursor. Indicates Remote post cursor coefficient value. Note: This register field is sticky.
11:6	RO	0x00	EQ_REMOTE_CURSOR EQ Remote Cursor. Indicates Remote cursor coefficient value. Note: This register field is sticky.
5:0	RO	0x00	EQ_REMOTE_PRE_CURSOR EQ Remote Pre-Cursor. Indicates Remote pre cursor coefficient value. Note: This register field is sticky.

14.4.3.10 PCIE_DSP_PF0_PORT_LOGIC Register Description

14.4.3.10.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_ACK_LATENCY_TIMER_OFF	0x0000	W	0x0C23040B	This register holds the ack latency timer limit and replay timer limit values.
PCIE_DSP_PF0_PORT_LOGIC_VENDOR_SPEC_DLLP_OFF	0x0004	W	0xFFFFFFFF	This register holds the vendor specific DLLP.
PCIE_DSP_PF0_PORT_LOGIC_PORT_FORCE_OFF	0x0008	W	0x00000004	This register can be used for testing and debuggong the link.
PCIE_DSP_PF0_PORT_LOGIC_ACK_F_ASPM_CTRL_OFF	0x000C	W	0x1BFFFF00	This register is used to control ack frequency and L0-L1 ASPM behaviour.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_PORT_LINK_CTRL_OFF	0x0010	W	0x00010120	Using this register you can control the port link behaviour.
PCIE_DSP_PF0_PORT_LOGIC_LANE_SKEW_OFF	0x0014	W	0x00000000	This register is used to control the lane skew behaviour.
PCIE_DSP_PF0_PORT_LOGIC_TIMER_CTRL_MAX_FUNC_NUM_OFF	0x0018	W	0x00018000	This register holds the ack frequency, latency, replay, fast link scaling timers, and max function number values.
PCIE_DSP_PF0_PORT_LOGIC_SYMBOL_TIMER_FILTER_1_OFF	0x001C	W	0x00000140	The Filter Mask 1 Register modifies the RADM filtering and error handling rules. For more details, see the "Receive Filtering" section. In each case, '0' applies the associated filtering rule and '1' masks the associated filtering rule.
PCIE_DSP_PF0_PORT_LOGIC_FILTER_MASK_2_OFF	0x0020	W	0x00000000	This register modifies the RADM filtering and error handling rules. For more details, see the "Receive Filtering" section. In each case, '0' applies the associated filtering rule and '1' masks the associated filtering rule.
PCIE_DSP_PF0_PORT_LOGIC_AMBA_MUL_OB_DECOMP_NP_SUB_REQ_CTRL_OFF	0x0024	W	0x00000001	This register controls multiple outbound decomposed NP subRequests operation.
PCIE_DSP_PF0_PORT_LOGIC_PL_DEBUG0_OFF	0x0028	W	0x00000000	This register holds cxpl_debug_info[31:0].
PCIE_DSP_PF0_PORT_LOGIC_PL_DEBUG1_OFF	0x002C	W	0x00000000	This register holds cxpl_debug_info[63:32].
PCIE_DSP_PF0_PORT_LOGIC_TX_P_FC_CREDIT_STATUS_OFF	0x0030	W	0x00000000	This register provides transmit posted FC credit status.
PCIE_DSP_PF0_PORT_LOGIC_TX_NP_FC_CREDIT_STATUS_OFF	0x0034	W	0x00000000	This register provides the transmit Non-Posted FC credit status.
PCIE_DSP_PF0_PORT_LOGIC_TX_CPL_FC_CREDIT_STATUS_OFF	0x0038	W	0x00000000	This register provides transmit completion FC credit status.
PCIE_DSP_PF0_PORT_LOGIC_QUEUE_STATUS_OFF	0x003C	W	0x00000000	This register provides the queue status.
PCIE_DSP_PF0_PORT_LOGIC_VC_TX_ARBI_1_OFF	0x0040	W	0x0000000F	This register is used for setting the WRR weights for VC0 - VC3.
PCIE_DSP_PF0_PORT_LOGIC_VC_TX_ARBI_2_OFF	0x0044	W	0x00000000	This register is used for setting the WRR weights for VC4 - VC7.
PCIE_DSP_PF0_PORT_LOGIC_VC0_P_RX_Q_CTRL_OFF	0x0048	W	0x45217038	This register controls segmented-buffer VC0 posted receive queue operation.
PCIE_DSP_PF0_PORT_LOGIC_VC0_NP_RX_Q_CTRL_OFF	0x004C	W	0x05217005	This register controls the segmented-buffer VC0 non-posted receive queue operation.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_VC0_CPL_RX_Q_CTRL_OFF	0x0050	W	0x05200000	This register controls the segmented-buffer VC0 completion receive queue operation.
PCIE_DSP_PF0_PORT_LOGIC_GEN2_CTRL_OFF	0x010C	W	0x000001FF	This register controls various functions of the controller related to link training, lane reversal, and equalization.
PCIE_DSP_PF0_PORT_LOGIC_PHY_STATUS_OFF	0x0110	W	0x00000000	Memory mapped register from phy_cfg_status GPIO input pins.
PCIE_DSP_PF0_PORT_LOGIC_PHY_CONTROL_OFF	0x0114	W	0x00000000	Memory mapped register to cfg_phy_control GPIO output pins.
PCIE_DSP_PF0_PORT_LOGIC_TRGT_MAP_CTRL_OFF	0x011C	W	0x0000007F	This register controls the target map.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_ADDR_OFF	0x0120	W	0x00000000	This register holds the integrated MSI reception module address.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_UPPER_ADDR_OFF	0x0124	W	0x00000000	This register holds the integrated MSI reception module upper address.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_0_EN_OFF	0x0128	W	0x00000000	This register enables integrated MSI reception module interrupt0.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_0_MASK_OFF	0x012C	W	0x00000000	This register provides information regarding the MSI Interrupt0 mask.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_0_STATUS_OFF	0x0130	W	0x00000000	This register provides the MSI Interrupt0 status.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_1_EN_OFF	0x0134	W	0x00000000	This register enables integrated MSI reception module interrupt1.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_1_MASK_OFF	0x0138	W	0x00000000	This register provides information regarding the MSI Interrupt1 mask.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_1_STATUS_OFF	0x013C	W	0x00000000	This register provides the MSI Interrupt1 status.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_2_EN_OFF	0x0140	W	0x00000000	This register enables integrated MSI reception module interrupt2.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_2_MASK_OFF	0x0144	W	0x00000000	This register provides information regarding the MSI Interrupt2 mask.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_2_STATUS_OFF	0x0148	W	0x00000000	This register provides the MSI Interrupt2 status.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_3_EN_OFF	0x014C	W	0x00000000	This register enables integrated MSI reception module interrupt3.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_3_MASK_OFF	0x0150	W	0x00000000	This register provides information regarding the MSI Interrupt3 mask.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_3_STATUS_OFF	0x0154	W	0x00000000	This register provides the MSI Interrupt3 status.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_4_EN_OFF	0x0158	W	0x00000000	This register enables integrated MSI reception module interrupt4.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_4_MASK_OFF	0x015C	W	0x00000000	This register provides information regarding the MSI Interrupt4 mask.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_4_STATUS_OFF	0x0160	W	0x00000000	This register provides the MSI Interrupt4 status.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_5_EN_OFF	0x0164	W	0x00000000	This register enables integrated MSI reception module interrupt5.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_5_MASK_OFF	0x0168	W	0x00000000	This register provides information regarding the MSI Interrupt5 mask.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_5_STATUS_OFF	0x016C	W	0x00000000	This register provides the MSI Interrupt5 status.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_6_EN_OFF	0x0170	W	0x00000000	This register enables integrated MSI reception module interrupt6.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_6_MASK_OFF	0x0174	W	0x00000000	This register provides information regarding the MSI Interrupt6 mask.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_6_STATUS_OFF	0x0178	W	0x00000000	This register provides the MSI Interrupt6 status.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_7_EN_OFF	0x017C	W	0x00000000	This register enables integrated MSI reception module interrupt7.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_7_MASK_OFF	0x0180	W	0x00000000	This register provides information regarding the MSI Interrupt7 mask.
PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_7_STATUS_OFF	0x0184	W	0x00000000	This register provides the MSI Interrupt7 status.
PCIE_DSP_PF0_PORT_LOGIC_MSI_GPIO_IO_OFF	0x0188	W	0x00000000	The contents of this register drive the top-level GPIO msi_ctrl_io[31:0].
PCIE_DSP_PF0_PORT_LOGIC_CLOCK_GATING_CTRL_OFF	0x018C	W	0x00000003	This register enables you to disable dynamic clock gating. By default dynamic clock gating is on, allowing the controller to autonomously enable and disable its clocks. The clock gating is performed in the clock and reset module, DWC_pcie_clk_rst.v, and is initiated by the controllers clock enable signals. The following modules support dynamic clock gating: - AXI Bridge - RADM

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_GEN3_RELATED_OFF	0x0190	W	0x00002001	There is no Gen3-specific N_FTS field. The N_FTS field in the "Link Width and Speed Change Control Register" is used for both Gen2 and Gen3 speed modes. There is no Gen3-specific "Directed Speed Change" field. The "Directed Speed Change" field in the "Link Width and Speed Change Control Register" is used to change to Gen2 or Gen3 speed. A speed change to Gen3 occurs if (1) the "Directed Speed Change" field is set to '1' and (2) the "Target Link Speed" field in the Link Control 2 Register is set to Gen3. Gen3 support is advertised by both sides of the link during link training.
PCIE_DSP_PF0_PORT_LOGIC_GEN3_EQ_CONTROL_OFF	0x01A8	W	0x04059F61	This register controls equalization for Phase2 in an upstream port (USP), or Phase3 in a downstream port (DSP).
PCIE_DSP_PF0_PORT_LOGIC_GEN3_EQ_FB_MODE_DIR_CHANGE_OFF	0x01AC	W	0x00000040	Equalization controls to be used in Phase2 (USP) or Phase 3 (DSP), when you set the Feedback Mode in "Gen3 EQ Control Register" to "Direction Change." These fields allow control over the initial starting point for the search of optimal coefficient settings, and allow control over the criteria used to determine when the optimal settings have been achieved. The values are applied to all the lanes.
PCIE_DSP_PF0_PORT_LOGIC_ORDER_RULE_CTRL_OFF	0x01B4	W	0x00000000	This register controls the order rule.
PCIE_DSP_PF0_PORT_LOGIC_PIPE_LOOPBACK_CONTROL_OFF	0x01B8	W	0x00000001	This register controls the PIPE Loopback.
PCIE_DSP_PF0_PORT_LOGIC_MISC_CONTROL_1_OFF	0x01BC	W	0x000BFF40	This is the DBI Read-Only write enable register.
PCIE_DSP_PF0_PORT_LOGIC_MULTI_LANE_CONTROL_OFF	0x01C0	W	0x00000000	Used when upsizing or downsizing the link width through Configuration state without bringing the link down.For more details, see the "Link Establishment" section in the "ControllerOperations" chapter of the Databook.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_PHY_INTEROP_CTRL_OFF	0x01C4	W	0x0001E201	This register controls the PHY interoperability.
PCIE_DSP_PF0_PORT_LOGIC_TRGT_CPL_LUT_DELETE_ENTRY_OFF	0x01C8	W	0x00000000	Using this register you can delete one entry in the target completion LUT. You should only use this register when you know that your application will never send the completion because of an FLR or any other reason.Note:: The target completion LUT (and associated target completion timeout event) is watching for completions (from your application on XALI0/1/2 or AXI master read channel) corresponding to previously received non-posted requests from the PCIe wire.
PCIE_DSP_PF0_PORT_LOGIC_LINK_FLUSH_CONTROL_OFF	0x01CC	W	0xFF000001	This register controls link reset request flush behaviour.
PCIE_DSP_PF0_PORT_LOGIC_AMBA_ERROR_RESPONSE_DEFAULT_OFF	0x01D0	W	0x00009C00	This register holds the AXI bridge slave error responses.
PCIE_DSP_PF0_PORT_LOGIC_AMBA_LINK_TIMEOUT_OFF	0x01D4	W	0x00000032	If your application AXI master issues outbound requests to the AXI bridge slave interface before the PCIe link is operational, the controller starts a "flush" timer. The timeout value of the timer is set by this register. If the timer times out before the PCIe link is operational, the bridge TX request queues are flushed. For more details, see the "AXI Bridge Initialization, Clocking and Reset" section in the AXI chapter of the Databook.
PCIE_DSP_PF0_PORT_LOGIC_AMBA_ORDERING_CTRL_OFF	0x01D8	W	0x00000000	This register controls the AXI Bridge Ordering.
PCIE_DSP_PF0_PORT_LOGIC_COHERENCY_CONTROL_1_OFF	0x01E0	W	0x00000000	This register controls the ACE cache coherency operation.
PCIE_DSP_PF0_PORT_LOGIC_COHERENCY_CONTROL_2_OFF	0x01E4	W	0x00000000	This register controls the ACE cache coherency operation.
PCIE_DSP_PF0_PORT_LOGIC_COHERENCY_CONTROL_3_OFF	0x01E8	W	0x00000000	This register controls the ACE cache coherency operation.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_AXI_MSTR_MSG_ADDR_LOW_OFF	0x01F0	W	0x00000000	Lower 20 bits of the programmable AXI address to which Messages coming from wire are mapped. Bits [11:0] of the register are tied to zero for the address to be 4k-aligned. In previous releases, the third and fourth DWORDs of a message (Msg/MsgD) TLP header were delivered though the AXI master address bus (mstr_awaddr). These DWORDS are now supplied through the mstr_awmisc_info_hdr_34dw[63:0] output; and the value on mstr_awaddr is driven to the value you have programmed into the AXI_MSTR_MSG_ADDR_LOW_OFF and AXI_MSTR_MSG_ADDR_HIGH_OFF registers.
PCIE_DSP_PF0_PORT_LOGIC_AXI_MSTR_MSG_ADDR_HIGH_OFF	0x01F4	W	0x00000000	Upper 32 bits of the programmable AXI address to which Messages coming from wire are mapped.
PCIE_DSP_PF0_PORT_LOGIC_PCIE_VERSION_NUMBER_OFF	0x01F8	W	0x3536302A	The version number is given in hex format. You should convert each pair of hex characters to ASCII to interpret.Using 4.70a (GA) as an example: - VERSION_NUMBER = 0x3437302a which translates to 470* - VERSION_TYPE = 0x67612a2a which translates to ga**Using 4.70a-ea01 as an example: - VERSION_NUMBER = 0x3437302a which translates to 470* - VERSION_TYPE = 0x65613031 which translates to ea01GA is a general release available on www.designware.comEA is an early release available on a per-customer basis.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PORT_LOGIC_PCIE_VERSION_TYPE_OFF	0x01FC	W	0x6C703035	The type is given in hex format. You should convert each pair of hex characters to ASCII to interpret.Using 4.70a (GA) as an example: - VERSION_NUMBER = 0x3437302a which translates to 470* - VERSION_TYPE = 0x67612a2a which translates to ga**Using 4.70a-ea01 as an example: - VERSION_NUMBER = 0x3437302a which translates to 470* - VERSION_TYPE = 0x65613031 which translates to ea01GA is a general release available on www.designware.comEA is an early release available on a per-customer basis.
PCIE_DSP_PF0_PORT_LOGIC_PL_APP_BUS_DEV_NUM_STATUS_OFF	0x0410	W	0x00000000	This register reflects the application driven bus and device number.
PCIE_DSP_PF0_PORT_LOGIC_PCIPM_TRAFFIC_CTRL_OFF	0x041C	W	0x00000000	This register provides control over TLP Traffic during Non-D0 States.
PCIE_DSP_PF0_PORT_LOGIC_PL_LTR_LATENCY_OFF	0x0430	W	0x00000000	The function of this register field (and all other fields in this register) differs between an upstream port and a downstream port. For an upstream port, the register fields capture the corresponding fields in the LTR messages that are transmitted by the port. For a downstream port, the register fields capture the corresponding fields in the LTR messages that are received by the port. The full content of the register is reflected on the app_ltr_latency[31:0] output.
PCIE_DSP_PF0_PORT_LOGIC_AUX_CLK_FREQ_OFF	0x0440	W	0x00000018	This register controls the auxiliary clock frequency.
PCIE_DSP_PF0_PORT_LOGIC_L1_SUBSTATES_OFF	0x0444	W	0x000000D2	This register holds L1 substates timing information.
PCIE_DSP_PF0_PORT_LOGIC_POWERDOWN_CTRL_STATUS_OFF	0x0448	W	0x00000220	This is the Powerdown Control and Status register.
PCIE_DSP_PF0_PORT_LOGIC_PIPE_RELATED_OFF	0x0490	W	0x00000000	This register controls the PIPE's capabitity, control, and status parameters.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3.10.2 Detail Registers Description

PCIE_DSP_PF0_PORT_LOGIC_ACK_LATENCY_TIMER_OFF

Address: Operational Base(0x00000700) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0c23	REPLAY_TIME_LIMIT Replay Timer Limit. The replay timer expires when it reaches this limit. The controller initiates a replay upon reception of a NAK or when the replay timer expires. For more details, see "Transmit Replay" in the Databook. - You can modify the effective timer limit through the TIMER_MOD_REPLAY_TIMER field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register. - After reset, the controller updates the default according to the Negotiated Link Width, Max_Payload_Size, and speed. The value is determined from Tables 3-4, 3-5, and 3-6 of the PCI Express Base Specification. - If there is a change in the payload size or link speed, the controller overrides any value that you have written to this register field, and resets the field back to the specification-defined value. The controller does not change the value in the TIMER_MOD_REPLAY_TIMER field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register.
15:0	RW	0x040b	ROUND_TRIP_LATENCY_TIME_LIMIT Ack Latency Timer Limit. The Ack latency timer expires when it reaches this limit. For more details, see "ACK/NAK Scheduling" in the Databook. - You can modify the effective timer limit through the TIMER_MOD_ACK_NAK field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register. - After reset, the controller updates the default according to the Negotiated Link Width, Max_Payload_Size, and speed. The value is determined from Tables 3-7, 3-8, and 3-9 of the PCI Express Base Specification. - The limit must reflect the round trip latency from requester to completer. - If there is a change in the payload size or link width, the controller overrides any value that you have written to this register field, and resets the field back to the specification-defined value. The controller does not change the value in the TIMER_MOD_ACK_NAK field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register.

PCIE_DSP_PF0_PORT_LOGIC_VENDOR_SPEC_DLLP_OFF

Address: Operational Base(0x00000700) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	VENDOR_SPEC_DLLP Vendor Specific DLLP Register. You can use this register to send a specific PCI Express DLLP. Your application can write 8-bit DLLP Type and 24-bit Payload data into this register, and set the VENDOR_SPECIFIC_DLLP_REQ field of the PORT_LINK_CTRL_OFF, to send the DLLP. - Bits[7:0]: DLLP Type - Bits[31:8]: Vendor Defined Payload (24 bits) Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_PORT_FORCE_OFF

Address: Operational Base(0x00000700) + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	RSVDP_24 Reserved for future use.
23	RW	0x0	DO_DESKEW_FOR_SRIS Use the transitions from TS2 to Logical Idle Symbol, SKP OS to Logical Idle Symbol, EIEOS to Logical Idle Symbol, and FTS Sequence to SKP OS to do deskew instead of using received SKP OS or TS1 to TS2 transition if DO_DESKEW_FOR_SRIS is set to '1'. Note: This register field is sticky.
22	RW	0x0	SUPPORT_PART_LANES_RXEI_EXIT Support LTSSM transition from Polling.Active to Polling.Config based on Rx 8 TSs on any lanes which are Rx EI exit too from base spec after 24ms timeout. This prevents some lanes detected but not Rx EI exit and LTSSM cannot move to Polling.Config. You must set the parameter CX_AUTO_LANE_FLIP_CTRL_EN true for the auto lanes reversal. Note: This register field is sticky.
21:16	RW	0x00	LINK_STATE Forced LTSSM State. The LTSSM state that the controller is forced to when you set the FORCE_EN bit (Force Link). LTSSM state encoding is defined by the lts_state variable in workspace/src/Layer1/smlh_ltssm.v. Note: This register field is sticky.
15	WO	0x0	FORCE_EN Force Link. The controller supports a testing and debug capability to allow your software to force the LTSSM state machine into a specific state, and to force the controller to transmit a specific Link Command. Asserting this bit triggers the following actions: - Forces the LTSSM to the state specified by the Forced LTSSM State field. - Forces the controller to transmit the command specified by the Forced Link Command field. This is a self-clearing register field. Reading from this register field always returns a '0'.
14:12	RO	0x0	RSVDP_12 Reserved for future use.
11:8	RW	0x0	FORCED_LTSSM Forced Link Command. The link command that the controller is forced to transmit when you set FORCE_EN bit (Force Link). Link command encoding is defined by the ltssm_cmd variable in workspace/src/Layer1/smlh_ltssm.v. Note: This register field is sticky.
7:0	RW	0x04	LINK_NUM Link Number. Not used for endpoint. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_ACK_F_ASPM_CTRL_OFF

Address: Operational Base(0x00000700) + offset (0x000C)

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Bit	Attr	Reset Value	Description
31	RO	0x0	RSVDP_31 Reserved for future use.
30	RW	0x0	ENTER_ASPM ASPM L1 Entry Control. Note: This register field is sticky.
29:27	RW	0x3	L1_ENTRANCE_LATENCY L1 Entrance Latency. Note: Programming this timer with a value greater that 32us has no effect unless extended sync is used, or all of the credits are infinite. Note: This register field is sticky.
26:24	RW	0x3	L0S_ENTRANCE_LATENCY L0s Entrance Latency. Note: This register field is sticky.
23:16	RW	0xff	COMMON_CLK_N_FTS Common Clock N_FTS. This is the N_FTS when common clock is used. The number of Fast Training Sequence ordered sets to be transmitted when transitioning from L0s to L0. This field is only writable (sticky) when all of the following configuration parameter equations are true: - CX_NFTS !=CX_COMM_NFTS - DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY - DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
15:8	RW	0xff	ACK_N_FTS The number of Fast Training Sequence(N_FTS) ordered sets to be transmitted when transitioning from L0s to L0. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	ACK_FREQ Ack Frequency. The controller accumulates the number of pending ACKs specified here (up to 255) before scheduling an ACK DLLP. - 0: Indicates that this Ack Frequency Counter feature is turned off. The controller generates a low-priority ACK request for every TLP that it receives. The controller waits until the ACK Latency Timer expires, then converts the current low-priority ACK request to a high-priority ACK request and schedules the DLLP for transmission to the remote link partner. - 1-255: Indicates that the controller will schedule a high-priority ACK after receiving this number of TLPs. It might schedule the ACK before receiving this number of TLPs if the ACK Latency Timer expires, but never later. For a typical system, you do not have to modify the default setting. For more details, see "ACK/NAK Scheduling" in the Databook. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_PORT_LINK_CTRL_OFF

Address: Operational Base(0x00000700) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	RSVDP_28 Reserved for future use.
27	RW	0x0	TRANSMIT_LANE_REVERSALE_ENABLE TRANSMIT_LANE_REVERSALE_ENABLE is an internally reserved field. Do not use. Note: This register field is sticky.
26	RW	0x0	EXTENDED_SYNCH EXTENDED_SYNCH is an internally reserved field. Do not use. Note: This register field is sticky.
25	RW	0x0	CORRUPT_LCRC_ENABLE CORRUPT_LCRC_ENABLE is an internally reserved field. Do not use. Note: This register field is sticky.
24	RW	0x0	BEACON_ENABLE BEACON_ENABLE is an internally reserved field. Do not use. Note: This register field is sticky.
23:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:16	RW	0x01	LINK_CAPABLE Link Mode Enable. Sets the number of lanes in the link that you want to connect to the link partner. When you have unused lanes in your system, then you must change the value in this register to reflect the number of lanes. You must also change the value in the "Predetermined Number of Lanes" field of the "Link Width and Speed Change Control Register". For more information, see "How to Tie Off Unused Lanes". For information on upsizing and downsizing the link width, see "Link Establishment". Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
15:12	RO	0x0	RSVDP_12 Reserved for future use.
11:8	RW	0x1	LINK_RATE LINK_RATE is an internally reserved field. Do not use. Note: This register field is sticky.
7	RW	0x0	FAST_LINK_MODE Fast Link Mode. Sets all internal LTSSM millisecond timers to Fast Mode for speeding up simulation. Forces the LTSSM training (link initialization) to use shorter time-outs and to link up faster. - The default scaling factor can be changed using the DEFAULT_FAST_LINK_SCALING_FACTOR parameter or through the FAST_LINK_SCALING_FACTOR field in the TIMER_CTRL_MAX_FUNC_NUM_OFF register. - Fast Link Mode can also be activated by setting the diag_ctrl_bus[2] pin to '1'. For more details, see the "Fast Link Simulation Mode" section in the "Integrating the Controller with the PHY or Application RTL or Verification IP" chapter of the User Guide. Note: This register field is sticky.
6	RW	0x0	LINK_DISABLE LINK_DISABLE is an internally reserved field. Do not use. Note: This register field is sticky.
5	RW	0x1	DLL_LINK_EN DLL Link Enable. Note: This register field is sticky.
4	RO	0x0	RSVDP_4 Reserved for future use.
3	RW	0x0	RESET_ASSERT Reset Assert. Triggers a recovery and forces the LTSSM to the hot reset state (downstream port only). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
2	RW	0x0	LOOPBACK_ENABLE Loopback Enable. Turns on loopback. For more details, see "Loopback" in the Databook. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
1	RW	0x0	SCRAMBLE_DISABLE Scramble Disable. Turns off data scrambling. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
0	RW	0x0	VENDOR_SPECIFIC_DLLP_REQ Vendor Specific DLLP Request. Reading from this self-clearing register field always returns a '0'.

PCIE_DSP_PF0_PORT_LOGIC_LANE_SKEW_OFF

Address: Operational Base(0x00000700) + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RW	0x0	DISABLE_LANE_TO_LANE_DESKEW Disable Lane-to-Lane Deskew. Causes the controller to disable the internal Lane-to-Lane deskew logic. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
30:27	RW	0x0	IMPLEMENT_NUM_LANES Implementation-specific Number of Lanes. Set the implementation-specific number of lanes. The number of lanes to be used when in Loopback Master. The number of lanes programmed must be equal to or less than the valid number of lanes set in LINK_CAPABLE field. You must configure this field before initiating Loopback by writing in the LOOPBACK_ENABLE field. The controller will transition from Loopback.Entry to Loopback.Active after receiving two consecutive TS1 Ordered Sets with the Loopback bit asserted on the implementation specific number of lanes configured in this field. Note: This register field is sticky.
26	RW	0x0	ELASTIC_BUFFER_MODE Selects Elasticity Buffer operating mode: Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
25	RW	0x0	ACK_NAK_DISABLE Ack/Nak Disable. Prevents the controller from sending ACK and NAK DLLPs. Note: This register field is sticky.
24	RW	0x0	FLOW_CTRL_DISABLE Flow Control Disable. Prevents the controller from sending FC DLLPs. Note: This register field is sticky.
23:0	RW	0x000000	INSERT_LANE_SKEW INSERT_LANE_SKEW is an internally reserved field. Do not use. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_TIMER_CTRL_MAX_FUNC_NUM_OFF

Address: Operational Base(0x00000700) + offset (0x0018)

Bit	Attr	Reset Value	Description
31	RO	0x0	RSVDP_31 Reserved for future use.
30:29	RW	0x0	FAST_LINK_SCALING_FACTOR Fast Link Timer Scaling Factor. Sets the scaling factor of LTSSM timer when FAST_LINK_MODE field in PORT_LINK_CTRL_OFF is set to '1'. Default is set by the hidden configuration parameter DEFAULT_FAST_LINK_SCALING_FACTOR which defaults to '0'. Note: This register field is sticky.
28:24	RW	0x00	UPDATE_FREQ_TIMER UPDATE_FREQ_TIMER is an internally reserved field. Do not use. Note: This register field is sticky.
23:19	RW	0x00	TIMER_MOD_ACK_NAK Ack Latency Timer Modifier. Increases the timer value for the Ack latency timer in increments of 64 clock cycles. A value of '0' represents no modification to the timer value. For more details, see the ROUND_TRIP_LATENCY_TIME_LIMIT field of the ACK_LATENCY_TIMER_OFF register. Note: This register field is sticky.
18:14	RW	0x06	TIMER_MOD_REPLAY_TIMER Replay Timer Limit Modifier. Increases the time-out value for the replay timer in increments of 64 clock cycles at Gen1 or Gen2 speed, and in increments of 256 clock cycles at Gen3 speed. A value of '0' represents no modification to the timer limit. For more details, see the REPLAY_TIME_LIMIT field of the ACK_LATENCY_TIMER_OFF register. At Gen3 speed, the controller automatically changes the value of this field to DEFAULT_GEN3_REPLAY_ADJ. Note: This register field is sticky.
13:8	RO	0x00	RSVDP_8 Reserved for future use.

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	MAX_FUNC_NUM Maximum function number that can be used in a request. Configuration requests targeted at function numbers above this value are returned with UR (unsupported request). Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_SYMBOL_TIMER_FILTER_1_OFF

Address: Operational Base(0x00000700) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	MASK_RADM_1 Filter Mask 1. The Filter Mask 1 Register modifies the RADM filtering and error handling rules. For more details, see the "Receive Filtering" section. In each case, '0' applies the associated filtering rule and '1' masks the associated filtering rule. [31]: CX_FLT_MASK_RC_CFG_DISCARD - 0: For RADM RC filter to not allow CFG transaction being received - 1: For RADM RC filter to allow CFG transaction being received [30]: CX_FLT_MASK_RC_IO_DISCARD - 0: For RADM RC filter to not allow IO transaction being received - 1: For RADM RC filter to allow IO transaction being received [29]: CX_FLT_MASK_MSG_DROP - 0: Drop MSG TLP (except for Vendor MSG). Send decoded message on the SII. - 1: Do not Drop MSG (except for Vendor MSG). Send message TLPs to your application on TRGT1 and send decoded message on the SII. - The default for this bit is the inverse of FLT_DROP_MSG. That is, if FLT_DROP_MSG =1, then the default of this bit is '0' (drop message TLPs). This bit only controls message TLPs other than Vendor MSGs. Vendor MSGs are controlled by Filter Mask Register 2, bits [1:0]. The controller never passes ATS Invalidate messages to the SII interface regardless of this filter rule setting. The controller passes all ATS Invalidate messages to TRGT1 (or AXI bridge master), as they are too big for the SII. [28]: CX_FLT_MASK_CPL_ECRC_DISCARD - Only used when completion queue is advertised with infinite credits and is in store-and-forward mode. - 0: Discard completions with ECRC errors - 1: Allow completions with ECRC errors to be passed up - Reserved field for SW. [27]: CX_FLT_MASK_ECRC_DISCARD - 0: Discard TLPs with ECRC errors - 1: Allow TLPs with ECRC errors to be passed up [26]: CX_FLT_MASK_CPL_LEN_MATCH - 0: Enforce length match for completions; a violation results in cpl_abort, and possibly AER of unexp_cpl_err - 1: Mask length match for completions [25]: CX_FLT_MASK_CPL_ATTR_MATCH - 0: Enforce attribute match for completions; a violation results in a malformed TLP error, and possibly AER of unexp_cpl_err,

Bit	Attr	Reset Value	Description
			cpl_rcvd_ur, cpl_rcvd_ca - 1: Mask attribute match for completions [24]: CX_FLT_MASK_CPL_TC_MATCH - 0: Enforce Traffic Class match for completions; a violation results in a malformed TLP error, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca - 1: Mask Traffic Class match for completions [23]: CX_FLT_MASK_CPL_FUNC_MATCH - 0: Enforce function match for completions; a violation results in cpl_abort, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca - 1: Mask function match for completions [22]: CX_FLT_MASK_CPL_REQID_MATCH - 0: Enforce Req. Id match for completions; a violation result in cpl_abort, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca - 1: Mask Req. Id match for completions [21]: CX_FLT_MASK_CPL_TAGERR_MATCH - 0: Enforce Tag Error Rules for completions; a violation result in cpl_abort, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca - 1: Mask Tag Error Rules for completions [20]: CX_FLT_MASK_LOCKED_RD_AS_UR - 0: Treat locked Read TLPs as UR for EP; Supported for RC - 1: Treat locked Read TLPs as Supported for EP; UR for RC [19]: CX_FLT_MASK_CFG_TYPE1_REQ_AS_UR - 0: Treat CFG type1 TLPs as UR for EP; Supported for RC - 1: Treat CFG type1 TLPs as Supported for EP; UR for RC - When CX_SRIOV_ENABLE is set then this bit is set to allow the filter to process Type 1 Config requests if the EP consumes more than one bus number. [18]: CX_FLT_MASK_UR_OUTSIDE_BAR - 0: Treat out-of-bar TLPs as UR - 1: Do not treat out-of-bar TLPs as UR [17]: CX_FLT_MASK_UR_POIS - 0: Treat poisoned request TLPs as UR - 1: Do not treat poisoned request TLPs as UR - The native controller always passes poisoned completions to your application except when you are using the DMA read channel. [16]: CX_FLT_MASK_UR_FUNC_MISMATCH - 0: Treat Function MisMatched TLPs as UR - 1: Do not treat Function MisMatched TLPs as UR Note: This register field is sticky.
15	RW	0x0	DISABLE_FC_WD_TIMER Disable FC Watchdog Timer. Note: This register field is sticky.
14:11	RW	0x0	EIDLE_TIMER EIDLE_TIMER is an internally reserved field. Do not use. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
10:0	RW	0x140	SKP_INT_VAL SKP Interval Value. The number of symbol times to wait between transmitting SKP ordered sets. The controller waits the number of symbol times in this register plus 1, between transmitting SKP ordered sets. Your application must program this register accordingly. For example, if 1536 were programmed into this register (in a 250 MHz controller), then the controller actually transmits SKP ordered sets once every 1537 symbol times. The value programmed to this register is actually clock ticks and not symbol times. In a 125 MHz controller, programming the value programmed to this register should be scaled down by a factor of 2 (because one clock tick =two symbol times in this case). Note: This value is not used at Gen3 speed; the skip interval is hardcoded to 370 blocks. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_FILTER_MASK_2_OFF

Address: Operational Base(0x00000700) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MASK_RADM_2 Filter Mask 2. This field modifies the RADM filtering and error handling rules. For more details, see the "Receive Filtering" in the Databook. In each case, '0' applies the associated filtering rule and '1' masks the associated filtering rule. [31:10]: Reserved [9]: CX_FLT_MASK_CPL_IN_LUT_CHECK - 0: Disable masking of checking if the tag of CPL is registered in LUT - 1: Enable masking of checking if the tag of CPL is registered in LUT [8]: CX_FLT_MASK_POIS_ERROR_REPORTING - 0: Disable masking of error reporting for Poisoned TLPs - 1: Enable masking of error reporting for Poisoned TLPs [7]: CX_FLT_MASK_PRS_DROP - 0: Allow PRS message to pass through - 1: Drop PRS Messages silently - This bit is ignored when the CX_FLT_MASK_MSG_DROP bit in the MASK_RADM_1 field of the SYMBOL_TIMER_FILTER_1_OFF register is set to '1'. [6]: CX_FLT_UNMASK_TD - 0: Disable unmask TD bit if CX_STRIP_ECRC_ENABLE - 1: Enable unmask TD bit if CX_STRIP_ECRC_ENABLE [5]: CX_FLT_UNMASK_UR_POIS_TRGT0 - 0: Disable unmask CX_FLT_MASK_UR_POIS with TRGT0 destination - 1: Enable unmask CX_FLT_MASK_UR_POIS with TRGT0 destination

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Bit	Attr	Reset Value	Description
			[4]: CX_FLT_MASK_LN_VENMSG1_DROP - 0: Allow LN message to pass through - 1: Drop LN Messages silently [3]: CX_FLT_MASK_HANDLE_FLUSH - 0: Disable controller Filter to handle flush request - 1: Enable controller Filter to handle flush request [2]: CX_FLT_MASK_DABORT_4UCPL - 0: Enable DLLP abort for unexpected completion - 1: Do not enable DLLP abort for unexpected completion [1]: CX_FLT_MASK_VENMSG1_DROP - 0: Vendor MSG Type 1 dropped silently - 1: Vendor MSG Type 1 not dropped [0]: CX_FLT_MASK_VENMSG0_DROP - 0: Vendor MSG Type 0 dropped with UR error reporting - 1: Vendor MSG Type 0 not dropped Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_AMBA_MUL_OB_DECOMP_NP_SUB_REQ_CTRL_OFF

Address: Operational Base(0x00000700) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	RSVDP_1 Reserved for future use.
0	RW	0x1	OB_RD_SPLIT_BURST_EN Enable AMBA Multiple Outbound Decomposed NP SubRequests. You should not clear this register unless your application master is requesting an amount of read data greater than Max_Read_Request_Size, and the remote device (or switch) is reordering completions that have different tags. For more details, see "AXI Bridge Ordering" in the AXI chapter of the Databook. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_PL_DEBUG0_OFF

Address: Operational Base(0x00000700) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DEB_REG_0 The value on cxpl_debug_info[31:0].

PCIE_DSP_PF0_PORT_LOGIC_PL_DEBUG1_OFF

Address: Operational Base(0x00000700) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DEB_REG_1 The value on cxpl_debug_info[63:32].

PCIE_DSP_PF0_PORT_LOGIC_TX_P_FC_CREDIT_STATUS_OFF

Address: Operational Base(0x00000700) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	RSVDP_TX_P_FC_CREDIT_STATUS Reserved for future use.

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Bit	Attr	Reset Value	Description
19:12	RO	0x00	TX_P_HEADER_FC_CREDIT Transmit Posted Header FC Credits. - The posted Header credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. - Default value depends on the number of advertised credits for header and data - Scaled Flow Control: [4'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. - No Scaling: [12'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].
11:0	RO	0x000	TX_P_DATA_FC_CREDIT Transmit Posted Data FC Credits. - The posted Data credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. - Default value depends on the number of advertised credits for header and data - Scaled Flow Control: [4'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. - No Scaling: [12'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].

PCIE_DSP_PF0_PORT_LOGIC_TX_NP_FC_CREDIT_STATUS_OFF

Address: Operational Base(0x00000700) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	RSVDP_TX_NP_FC_CREDIT_STATUS Reserved for future use.
19:12	RO	0x00	TX_NP_HEADER_FC_CREDIT Transmit Non-Posted Header FC Credits. - The non-posted Header credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. - Default value depends on the number of advertised credits for header and data - Scaled Flow Control: [4'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. - No Scaling: [12'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].

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Bit	Attr	Reset Value	Description
11:0	RO	0x000	TX_NP_DATA_FC_CREDIT Transmit Non-Posted Data FC Credits. - The non-posted Data credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. - Default value depends on the number of advertised credits for header and data - Scaled Flow Control: [4'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. - No Scaling: [12'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].

PCIE_DSP_PF0_PORT_LOGIC_TX_CPL_FC_CREDIT_STATUS_OFF

Address: Operational Base(0x00000700) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	RSVDP_TX_CPL_FC_CREDIT_STATUS Reserved for future use.
19:12	RO	0x00	TX_CPL_HEADER_FC_CREDIT Transmit Completion Header FC Credits. - The Completion Header credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. - Default value depends on the number of advertised credits for header and data - Scaled Flow Control: [4'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. - No Scaling: [12'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].
11:0	RO	0x000	TX_CPL_DATA_FC_CREDIT Transmit Completion Data FC Credits. - The Completion Data credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. - Default value depends on the number of advertised credits for header and data - Scaled Flow Control: [4'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. - No Scaling: [12'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].

PCIE_DSP_PF0_PORT_LOGIC_QUEUE_STATUS_OFF

Address: Operational Base(0x00000700) + offset (0x003C)

Bit	Attr	Reset Value	Description
31	RW	0x0	TIMER_MOD_FLOW_CONTROL_EN FC Latency Timer Override Enable. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
30:29	RO	0x0	RSVDP_29 Reserved for future use.
28:16	RW	0x0000	TIMER_MOD_FLOW_CONTROL FC Latency Timer Override Value. When you set the "FC Latency Timer Override Enable" in this register, the value in this field will override the FC latency timer value that the controller calculates according to the PCIe specification. For more details, see "Flow Control" in the Databook. Note: This register field is sticky.
15:14	RO	0x0	reserved
13	RO	0x0	RX_SERIALIZATION_Q_NON_EMPTY Receive Serialization Queue Not Empty.
12:4	RO	0x000	RSVDP_4 Reserved for future use.
3	RW	0x0	RX_QUEUE_OVERFLOW Receive Credit Queue Overflow.
2	RO	0x0	RX_QUEUE_NON_EMPTY Receive Credit Queue Not Empty.
1	RO	0x0	TX_RETRY_BUFFER_NE Transmit Retry Buffer Not Empty.
0	RO	0x0	RX_TLP_FC_CREDIT_NON_RETURN Received TLP FC Credits Not Returned.

PCIE_DSP_PF0_PORT_LOGIC_VC_TX_ARBI_1_OFF

Address: Operational Base(0x00000700) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	WRR_WEIGHT_VC_3 WRR Weight for VC3. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
23:16	RO	0x00	WRR_WEIGHT_VC_2 WRR Weight for VC2. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
15:8	RO	0x00	WRR_WEIGHT_VC_1 WRR Weight for VC1. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
7:0	RO	0x0f	WRR_WEIGHT_VC_0 WRR Weight for VC0. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R

PCIE_DSP_PF0_PORT_LOGIC_VC_TX_ARBI_2_OFF

Address: Operational Base(0x00000700) + offset (0x0044)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	WRR_WEIGHT_VC_7 WRR Weight for VC7. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
23:16	RO	0x00	WRR_WEIGHT_VC_6 WRR Weight for VC6. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
15:8	RO	0x00	WRR_WEIGHT_VC_5 WRR Weight for VC5. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R
7:0	RO	0x00	WRR_WEIGHT_VC_4 WRR Weight for VC4. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R

PCIE_DSP_PF0_PORT_LOGIC_VC0_P_RX_Q_CTRL_OFF

Address: Operational Base(0x00000700) + offset (0x0048)

Bit	Attr	Reset Value	Description
31	RW	0x0	VC_ORDERING_RX_Q VC Ordering for Receive Queues. Determines the VC ordering rule for the receive queues, used only in the segmented-buffer configuration: Note: This register field is sticky.
30	RW	0x1	TLP_TYPE_ORDERING_VC0 TLP Type Ordering for VC0. Determines the TLP type ordering rule for VC0 receive queues, used only in the segmented-buffer configuration: Note: This register field is sticky.
29:28	RW	0x0	RESERVED5 Reserved. Note: This register field is sticky.
27:26	RW	0x1	VC0_P_DATA_SCALE VC0 Scale Posted Data Credits. Note: This register field is sticky.
25:24	RW	0x1	VC0_P_HDR_SCALE VC0 Scale Posted Header Credits. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
23:21	RW	0x1	VC0_P_TLP_Q_MODE Reserved. Note: This register field is sticky.
20	RW	0x0	RESERVED4 Reserved. Note: This register field is sticky.
19:12	RO	0x17	VC0_P_HEADER_CREDIT VC0 Posted Header Credits. The number of initial posted header credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.
11:0	RO	0x038	VC0_P_DATA_CREDIT VC0 Posted Data Credits. The number of initial posted data credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_VC0_NP_RX_Q_CTRL_OFF

Address: Operational Base(0x00000700) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RESERVED7 Reserved. Note: This register field is sticky.
27:26	RW	0x1	VC0_NP_DATA_SCALE VC0 Scale Non-Posted Data Credits. Note: This register field is sticky.
25:24	RW	0x1	VC0_NP_HDR_SCALE VC0 Scale Non-Posted Header Credits. Note: This register field is sticky.
23:21	RW	0x1	VC0_NP_TLP_Q_MODE Reserved. Note: This register field is sticky.
20	RW	0x0	RESERVED6 Reserved. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
19:12	RO	0x17	VC0_NP_HEADER_CREDIT VC0 Non-Posted Header Credits. The number of initial non-posted header credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.
11:0	RO	0x005	VC0_NP_DATA_CREDIT VC0 Non-Posted Data Credits. The number of initial non-posted data credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_VC0_CPL_RX_Q_CTRL_OFF

Address: Operational Base(0x00000700) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RESERVED9 Reserved. Note: This register field is sticky.
27:26	RW	0x1	VC0_CPL_DATA_SCALE VC0 Scale CPL Data Credits. Note: This register field is sticky.
25:24	RW	0x1	VC0_CPL_HDR_SCALE VC0 Scale CPL Header Credits. Note: This register field is sticky.
23:21	RW	0x1	VC0_CPL_TLP_Q_MODE Reserved. Note: This register field is sticky.
20	RW	0x0	RESERVED8 Reserved. Note: This register field is sticky.
19:12	RO	0x00	VC0_CPL_HEADER_CREDIT VC0 Completion Header Credits. The number of initial Completion header credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
11:0	RO	0x000	VC0_CPL_DATA_CREDIT VC0 Completion Data Credits. The number of initial Completion data credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_GEN2_CTRL_OFF

Address: Operational Base(0x00000700) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	SELECTABLE_DEEMPH_BIT_MUX The selectable deemphasis bit (Symbol 4 bit 6) of the transmitted TS2 Ordered Sets for DSP in Recovery.RcvrCfg state is muxed between the Selectable De-emphasis field in the Link Control 2 register and the value requested by USP in Recovery.RcvrLock state through Tx TS1s from USP. Note: This register field is sticky.
22	RW	0x0	SELECT_DEEMPH_VAR_MUX The select_deemphasis variable for DSP on entry to Recovery.RcvrCfg state is muxed between the Selectable De-emphasis field in the Link Control 2 register and the value requested by the Upstream Port in the eight consecutive TS1 Ordered Sets it received. Note: This register field is sticky.
21	RW	0x0	GEN1_EI_INFERENCE Electrical Idle Inference Mode at Gen1 Rate. Programmable mode to determine inferred electrical idle (EI) in Recovery.Speed or Loopback.Active (as slave) state at Gen1 speed by looking for a '1' value on RxElecIdle instead of looking for a '0' on RxValid. If the PHY fails to deassert the RxValid signal in Recovery.Speed or Loopback.Active (because of corrupted EIOS for example), then EI cannot be inferred successfully in the controller by just detecting the condition RxValid=0. Note: This register field is sticky.
20	RW	0x0	SEL_DEEMPHASIS Used to set the de-emphasis level for upstream ports. This bit selects the level of de-emphasis the link operates at. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
19	RW	0x0	CONFIG_TX_COMP_RX Config Tx Compliance Receive Bit. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
18	RW	0x0	CONFIG_PHY_TX_CHANGE Config PHY Tx Swing. Controls the PHY transmitter voltage swing level. The controller drives the mac_phy_txswing output from this register bit field. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
17	RW	0x0	DIRECT_SPEED_CHANGE Directed Speed Change. When the speed change occurs, the controller will clear the contents of this field; and a read to this field by your software will return a '0'. To manually initiate the speed change: - Write to LINK_CONTROL2_LINK_STATUS2_REG.PCIE_CAP_TARGET_LINK_SPEED in the local device - Deassert this field - Assert this field If you set the default of this field using the DEFAULT_GEN2_SPEED_CHANGE configuration parameter to '1', then the speed change is initiated automatically after link up, and the controller clears the contents of this field. If you want to prevent this automatic speed change, then write a lower speed value to the Target Link Speed field of the Link Control 2 register (LINK_CONTROL2_LINK_STATUS2_OFF.PCIE_CAP_TARGET_LINK_SPEED) through the DBI before link up. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
16	RW	0x0	AUTO_LANE_FLIP_CTRL_EN Enable Auto flipping of the lanes. You must set the CX_AUTO_LANE_FLIP_CTRL_EN configuration parameter to include the hardware for this feature in the controller. For more details, see the 'Lane Reversal' appendix in the Databook. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:13	RW	0x0	PRE_DET_LANE Predetermined Lane for Auto Flip. This field defines which physical lane is connected to logical Lane0 by the flip operation performed in Detect. This field is used to restrict the receiver detect procedure to a particular lane when the default detect and polling procedure performed on all lanes cannot be successful. A notable example of when it is useful to program this field to a value different from the default, is when a lane is asymmetrically broken, that is, it is detected in Detect LTSSM state but it cannot exit Electrical Idle in Polling LTSSM state. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
12:8	RW	0x01	NUM_OF_LANES Predetermined Number of Lanes. Defines the number of lanes which are connected and not bad. Used to limit the effective link width to ignore 'broken" or "unused" lanes that detect a receiver. Indicates the number of lanes to check for exit from Electrical Idle in Polling.Active and L2.Idle. It is possible that the LTSSM might detect a receiver on a bad or broken lane during the Detect Substate. However, it is also possible that such a lane might also fail to exit Electrical Idle and therefore prevent a valid link from being configured. This value is referred to as the "Predetermined Number of Lanes" in section 4.2.6.2.1 of the PCI Express Base Specification. When you have unused lanes in your system, then you must change the value in this register to reflect the number of lanes. You must also change the value in the "Link Mode Enable" field of PORT_LINK_CTRL_OFF. The value in this register is normally the same as the encoded value in PORT_LINK_CTRL_OFF. If you find that one of your used lanes is bad then you must reduce the value in this register. For more information, see "How to Tie Off Unused Lanes" in the Databook. For information on upsizing and downsizing the link width, see "Link Establishment" in the Databook. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
7:0	RW	0xff	FAST_TRAINING_SEQ Sets the Number of Fast Training Sequences (N_FTS) that the controller advertises as its N_FTS during Gen2 or Gen3 link training. This value is used to inform the link partner about the PHY's ability to recover synchronization after a low power state. The number should be provided by the PHY vendor. Do not set N_FTS to zero; doing so can cause the LTSSM to go into the recovery state when exiting from L0s. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.

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PCIE_DSP_PF0_PORT_LOGIC_PHY_STATUS_OFF

Address: Operational Base(0x00000700) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PHY_STATUS PHY Status. Data received directly from the phy_cfg_status bus. These is a GPIO register reflecting the values on the static phy_cfg_status input signals. The usage is left completely to the user and does not in any way influence controller functionality. You can use it for any static sideband status signalling requirements that you have for your PHY. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_PHY_CONTROL_OFF

Address: Operational Base(0x00000700) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PHY_CONTROL PHY Control. Data sent directly to the cfg_phy_control bus. This is a GPIO register driving the values on the static cfg_phy_control output signals, and does not in any way influence controller functionality. It can be used for any static sideband control signaling requirements that you have for your PHY. Usage of this register and the associated GPIO bus is RESERVED when the controller is connected to a Synopsys PHY. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_TRGT_MAP_CTRL_OFF

Address: Operational Base(0x00000700) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	TARGET_MAP_RESERVED_21_31 Reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky)
20:16	RW	0x00	TARGET_MAP_INDEX The number of the PF Function on which the Target Values are set. This register does not respect the Byte Enable setting, any write will affect all register bits.
15:13	RO	0x0	TARGET_MAP_RESERVED_13_15 Reserved. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky)
12:7	RO	0x00	reserved
6	RW	0x1	TARGET_MAP_ROM Target Value for the ROM page of the PF Function selected by the index number. This register does not respect the Byte Enable setting, any write will affect all register bits.
5:0	RW	0x3f	TARGET_MAP_PF Target Values for each BAR on the PF Function selected by the index number. This register does not respect the Byte Enable setting, any write will affect all register bits.

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PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_ADDR_OFF

Address: Operational Base(0x00000700) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_ADDR Integrated MSI Reception Module Address. System specified address for MSI memory write transaction termination. Within the AXI Bridge, every received Memory Write request is examined to see if it targets the MSI Address that has been specified in this register; and also to see if it satisfies the definition of an MSI interrupt request. When these conditions are satisfied the Memory Write request is marked as an MSI request. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_UPPER_ADDR_OFF

Address: Operational Base(0x00000700) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_UPPER_ADDR Integrated MSI Reception Module Upper Address. System specified upper address for MSI memory write transaction termination. Allows functions to support a 64-bit MSI address. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_0_EN_OFF

Address: Operational Base(0x00000700) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_0_EN MSI Interrupt0 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_0_MASK_OFF

Address: Operational Base(0x00000700) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_0_MASK MSI Interrupt0 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_0_STATUS_OFF

Address: Operational Base(0x00000700) + offset (0x0130)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_0_STATUS MSI Interrupt0 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_1_EN_OFF

Address: Operational Base(0x00000700) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_1_EN MSI Interrupt1 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_1_MASK_OFF

Address: Operational Base(0x00000700) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_1_MASK MSI Interrupt1 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_1_STATUS_OFF

Address: Operational Base(0x00000700) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_1_STATUS MSI Interrupt1 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_2_EN_OFF

Address: Operational Base(0x00000700) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_2_EN MSI Interrupt2 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_2_MASK_OFF

Address: Operational Base(0x00000700) + offset (0x0144)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_2_MASK MSI Interrupt2 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_2_STATUS_OFF

Address: Operational Base(0x00000700) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_2_STATUS MSI Interrupt2 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_3_EN_OFF

Address: Operational Base(0x00000700) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_3_EN MSI Interrupt3 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_3_MASK_OFF

Address: Operational Base(0x00000700) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_3_MASK MSI Interrupt3 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_3_STATUS_OFF

Address: Operational Base(0x00000700) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_3_STATUS MSI Interrupt3 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_4_EN_OFF

Address: Operational Base(0x00000700) + offset (0x0158)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_4_EN MSI Interrupt4 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_4_MASK_OFF

Address: Operational Base(0x00000700) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_4_MASK MSI Interrupt4 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_4_STATUS_OFF

Address: Operational Base(0x00000700) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_4_STATUS MSI Interrupt4 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_5_EN_OFF

Address: Operational Base(0x00000700) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_5_EN MSI Interrupt5 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_5_MASK_OFF

Address: Operational Base(0x00000700) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_5_MASK MSI Interrupt5 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_5_STATUS_OFF

Address: Operational Base(0x00000700) + offset (0x016C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_5_STATUS MSI Interrupt5 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_6_EN_OFF

Address: Operational Base(0x00000700) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_6_EN MSI Interrupt6 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_6_MASK_OFF

Address: Operational Base(0x00000700) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_6_MASK MSI Interrupt6 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_6_STATUS_OFF

Address: Operational Base(0x00000700) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_6_STATUS MSI Interrupt6 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_7_EN_OFF

Address: Operational Base(0x00000700) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_7_EN MSI Interrupt7 Enable. Specifies which interrupts are enabled. When an MSI is received from a disabled interrupt, no status bit gets set in MSI controller interrupt status register. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_7_MASK_OFF

Address: Operational Base(0x00000700) + offset (0x0180)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_7_MASK MSI Interrupt7 Mask. Allows enabled interrupts to be masked. When an MSI is received for a masked interrupt, the corresponding status bit gets set in the interrupt status register but the msi_ctrl_int output is not set HIGH. Each bit corresponds to a single MSI Interrupt Vector. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MSI_CTRL_INT_7_STATUS_OFF

Address: Operational Base(0x00000700) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_CTRL_INT_7_STATUS MSI Interrupt7 Status. When an MSI is detected for EP#i, one bit in this register is set. The decoding of the data payload of the MSI Memory Write request determines which bit gets set. A status is bit is cleared by writing a 1 to the bit. Each bit corresponds to a single MSI Interrupt Vector.

PCIE_DSP_PF0_PORT_LOGIC_MSI_GPIO_IO_OFF

Address: Operational Base(0x00000700) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSI_GPIO_REG MSI GPIO Register. The contents of this register drive the top-level GPIO msi_ctrl_io[31:0]. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_CLOCK_GATING_CTRL_OFF

Address: Operational Base(0x00000700) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	RSVDP_2 Reserved for future use.
1	RW	0x1	AXI_CLK_GATING_EN AXI Clock Gating Enable. This register enables the AXI Bridge to autonomously enable and disable the AXI Master clock, the AXI Slave clock and the AXI DBI slave clock. The DWC_pcie_clk_rst.v module provides the gated clock, mstr_axi_aclk_gated, to the AXI Bridge and is enabled when the controllers clock enable signal, mstr_aclk_active, is asserted. For the AXI Slave this module provides the gated clock, slv_axi_aclk_gated, to the AXI Bridge and is enabled when the controllers clock enable signal, slv_aclk_active, is asserted. If the AXI DBI Slave is enabled (DBI_4SLAVE_POPULATED=1) the module provides the gated clock, dbi_axi_aclk_gated, to the AXI Bridge and is enabled when the controllers clock enable signal, dbi_aclk_active, is asserted. The controller de-asserts the clock enable signals when the respective AXI Master/Slave interfaces are idle. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
0	RW	0x1	RADM_CLK_GATING_EN RADM Clock Gating Enable. This register, if set, enables the RADM to autonomously enable and disable its clock. The DWC_pcie_clk_rst.v module provides the gated clock, radm_clk_g, to the RADM and is enabled when the controllers clock enable signal, en_radm_clk_g, is asserted. The RADM clock is a gated version of the controller clock, core_clk. The controller de-asserts en_radm_clk_g when there is no Rx traffic, Rx queues and pre/post-queue pipelines are empty, RADM completion LUT is empty, and there are no FLR actions pending. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_GEN3_RELATED_OFF

Address: Operational Base(0x00000700) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	RSVDP_26 Reserved for future use.
25:24	RO	0x0	reserved
23	RW	0x0	GEN3_EQ_INVREQ_EVAL_DIFF_DISABLE Eq InvalidRequest and RxEqEval Different Time Assertion Disable. Disable the assertion of Eq InvalidRequest and RxEqEval at different time. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky.
22:21	RO	0x0	reserved
20:19	RO	0x0	RSVDP_19 Reserved for future use.
18	RW	0x0	GEN3_DC_BALANCE_DISABLE DC Balance Disable. Disable DC Balance feature. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky.
17	RW	0x0	GEN3_DLLP_XMT_DELAY_DISABLE DLLP Transmission Delay Disable. Disable delay transmission of DLLPs before equalization. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
16	RW	0x0	GEN3_EQUALIZATION_DISABLE Equalization Disable. Disable equalization feature. This bit cannot be changed once the LTSSM starts link training. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky.
15:14	RO	0x0	RSVDP_14 Reserved for future use.
13	RW	0x1	RXEQ_RGRDLESS_RXTS When set to '1', the controller as Gen3 EQ master asserts RxEqEval to instruct the PHY to do Rx adaptation and evaluation after a 500ns timeout from a new preset request. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: see description Note: This register field is sticky.
12	RW	0x0	RXEQ_PH01_EN Rx Equalization Phase 0/Phase 1 Hold Enable. When this bit is set the upstream port holds phase 0 (the downstream port holds phase 1) for 10ms. Holding phase 0 or phase 1 can be used to allow sufficient time for Rx Equalization to be performed by the PHY. This bit is used during Virtex-7 Gen3 equalization. The programmable bits [RXEQ_PH01_EN, EQ_PHASE_2_3] can be used to obtain the following variations of the equalization procedure: Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: see description Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
11	RW	0x0	EQ_REDO Equalization Redo Disable. Disable autonomous mechanism for requesting to redo the equalization process. The received presets or coefficients mismatch in Recovery.RcvrLock after Recovery EQ phases causes the EQ redo requests. If the EQ redo is infinite or you do not want eq requests and redo, setting this bit to 1 will stop the EQ requests and EQ redo so that the link can go ahead to L0 state for packet trasmissions. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky.
10	RW	0x0	EQ_EIEOS_CNT Equalization EIEOS Count Reset Disable. Disable requesting reset of EIEOS count during equalization. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky.
9	RW	0x0	EQ_PHASE_2_3 Equalization Phase 2 and Phase 3 Disable. This applies to downstream ports only. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: see description Note: This register field is sticky.
8	RW	0x0	DISABLE_SCRAMBLER_GEN_3 Disable Scrambler for Gen3 and Gen4 Data Rate. The Gen3 and Gen4 scrambler/descrambler within the controller needs to be disabled when the scrambling function is implemented outside of the controller (for example within the PHY). Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky.
7:2	RO	0x00	RSVDP_2 Reserved for future use.

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Bit	Attr	Reset Value	Description
1	RW	0x0	NO_SEED_VALUE_CHANGE If this bit is set to 1, the seed value of LFSR for scrambler at Gen3 rate does not change after LinkUp = 1. This bit takes effect only when CX_AUTO_LANE_FLIP_CTRL_EN is supported. This feature requires both sides of the link support it. Note: this register is shared for Gen3 and Gen4/Gen5 data rates. Note: This register field is sticky.
0	RW	0x1	GEN3_ZRXDC_NONCOMPL Gen3 Receiver Impedance ZRX-DC Not Compliant. Receivers that operate at 8.0 GT/s with an impedance other than the range defined by the ZRX-DC parameter for 2.5 GT/s (40-60 Ohms) must meet additional behavior requirements in the following LTSSM states: Polling, Rx_L0s, L1, L2, and Disabled. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rates. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_GEN3_EQ_CONTROL_OFF

Address: Operational Base(0x00000700) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	RSVDP_27 Reserved for future use.
26	RW	0x1	GEN3_REQ_SEND_CONSEC_EIEOS_FOR_PSET_MAP Request controller to send back-to-back EIEOS in Recovery.RcvrLock state until presets to coefficients mapping is complete. Note: Gen3 and Gen4 share the same register bit and have the same feature. Note: This register field is sticky.
25	RW	0x0	GEN3_EQ_PSET_REQ_AS_COEF GEN3_EQ_PSET_REQ_AS_COEF is an internally reserved field. Do not use. Note: This register field is sticky.
24	RW	0x0	GEN3_EQ_FOM_INC_INITIAL_EVAL Include Initial FOM. Include or not the FOM feedback from the initial preset evaluation performed in the EQ Master, when finding the highest FOM among all preset evaluations. Note: - When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. - If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. - If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. - If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
23:8	RW	0x059f	GEN3_EQ_PSET_REQ_VEC Preset Request Vector. Requesting of Presets during the initial part of the EQ Master Phase. Encoding scheme is as follows: Bit [15:0] =0x0: No preset is requested and evaluated in EQ Master Phase. Bit [i] =1: "Preset=i" is requested and evaluated in EQ Master Phase. - 0000000000000000: No preset be requested and evaluated in EQ Master Phase - 000000xxxxxxxxx1: Preset 0 is requested and evaluated in EQ Master Phase - 000000xxxxxxxx1x: Preset 1 is requested and evaluated in EQ Master Phase - 000000xxxxxxx1xx: Preset 2 is requested and evaluated in EQ Master Phase - 000000xxxxxx1xxx: Preset 3 is requested and evaluated in EQ Master Phase - 000000xxxxx1xxxx: Preset 4 is requested and evaluated in EQ Master Phase - 000000xxxx1xxxxx: Preset 5 is requested and evaluated in EQ Master Phase - 000000xxx1xxxxxx: Preset 6 is requested and evaluated in EQ Master Phase - 000000xx1xxxxxxx: Preset 7 is requested and evaluated in EQ Master Phase - 000000x1xxxxxxxx: Preset 8 is requested and evaluated in EQ Master Phase - 00000x1xxxxxxxxx: Preset 9 is requested and evaluated in EQ Master Phase - 000001xxxxxxxxxx: Preset 10 is requested and evaluated in EQ Master Phase - All other encodings: Reserved Note: You must contact your PHY vendor to ensure 24 ms timeout does not occur in presets requests in EQ master phase, that is, you must set a proper value to the GEN3_EQ_PSET_REQ_VEC register so that the EQ tunning for Figure of Merit in the EQ master phase completes before 24 ms timeout. Note: - When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. - If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. - If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. - If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.
7	RO	0x0	RSVDP_7 Reserved for future use.

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Bit	Attr	Reset Value	Description
6	RW	0x1	GEN3_LOWER_RATE_EQ_REDO_ENABLE Support EQ redo and lower rate change. Note: Gen3 and Gen4 share the same register bit and have the same feature. Note: This register field is sticky.
5	RW	0x1	GEN3_EQ_EVAL_2MS_DISABLE Phase2_3 2 ms Timeout Disable. Determine behavior in Phase2 for USP (Phase3 if DSP) when the PHY does not respond within 2ms to the assertion of RxEqEval. Note: - When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. - If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. - If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. - If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
4	RW	0x0	GEN3_EQ_PHASE23_EXIT_MODE Behavior After 24 ms Timeout (when optimal settings are not found). For a USP: Determine next LTSSM state from Phase2 after 24ms Timeout - 0: Recovery.Speed - 1: Recovery.Equalization.Phase3 When optimal settings are not found then: - Equalization Phase 2 Successful status bit is not set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 0 - Equalization Phase 2 Successful status bit is set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 1 - Equalization Phase 2 Complete status bit is set in the "Link Status Register 2" For a DSP: Determine next LTSSM state from Phase3 after 24ms Timeout - 0: Recovery.Speed - 1: Recovery.Equalization.RcvrLock When optimal settings are not found then: - Equalization Phase 3 Successful status bit is not set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 0 - Equalization Phase 3 Successful status bit is set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 1 - Equalization Phase 3 Complete status bit is set in the "Link Status Register 2" Note: GEN3_EQ_PHASE23_EXIT_MODE = 1 affects Direction Change feed back mode. EQ requests for Figure Of Merit mode complete before 24 ms timeout. Please see GEN3_EQ_PSET_REQ_VEC Register for more. Note: - When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. - If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. - If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. - If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.
3:0	RW	0x1	GEN3_EQ_FB_MODE Feedback Mode. Other values are reserved. Note: - When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is a shadow register for Gen3 and Gen4/Gen5 data rate. - If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. - If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. - If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.

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PCIE_DSP_PF0_PORT_LOGIC_GEN3_EQ_FB_MODE_DIR_CHANGE_OFF

Address: Operational Base(0x00000700) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	RSVDP_18 Reserved for future use.
17:14	RW	0x0	GEN3_EQ_FMDC_MAX_POST_CUSROR_DELTA Convergence Window Aperture for C+1. Post-cursor coefficients maximum delta within the convergence window depth. Allowed range: 0,1,2,..15. Note: - When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. - If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. - If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. - If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.
13:10	RW	0x0	GEN3_EQ_FMDC_MAX_PRE_CUSROR_DELTA Convergence Window Aperture for C-1. Pre-cursor coefficients maximum delta within the convergence window depth. Allowed range: 0,1,2,..15. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.
9:5	RW	0x02	GEN3_EQ_FMDC_N_EVALS Convergence Window Depth. Number of consecutive evaluations considered in Phase 2/3 when determining if optimal coefficients have been found. Allowed range: 0,1,2,..16 up to a maximum of CX_GEN3_EQ_COEFQ_DEPTH. When set to 0, EQ Master is performed without sending any requests to the remote partner in Phase 2 for USP and Phase 3 for DSP. Therefore, the remote partner will not change its transmitter coefficients and will move to the next state. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	GEN3_EQ_FMDC_T_MIN_PHASE23 Minimum Time (in ms) To Remain in EQ Master Phase. The LTSSM stays in EQ Master phase for at least this amount of time, before starting to check for convergence of the coefficients. Allowed values 0,1,...,24. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_ORDER_RULE_CTRL_OFF

Address: Operational Base(0x00000700) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	RSVDP_16 Reserved for future use.
15:8	RW	0x00	CPL_PASS_P Completion Passing Posted Ordering Rule Control. Determines if CPL can pass halted P queue.
7:0	RW	0x00	NP_PASS_P Non-Posted Passing Posted Ordering Rule Control. Determines if NP can pass halted P queue.

PCIE_DSP_PF0_PORT_LOGIC_PIPE_LOOPBACK_CONTROL_OFF

Address: Operational Base(0x00000700) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31	RW	0x0	PIPE_LOOPBACK PIPE Loopback Enable. Indicates RMMI Loopback if M-PCIe. Note: This register field is sticky.
30:27	RO	0x0	RSVDP_27 Reserved for future use.
26:24	WO	0x0	RXSTATUS_VALUE RXSTATUS_VALUE is an internally reserved field. Do not use.
23:22	RO	0x0	RSVDP_22 Reserved for future use.
21:16	RW	0x00	RXSTATUS_LANE RXSTATUS_LANE is an internally reserved field. Do not use. Note: This register field is sticky.
15:0	RW	0x0001	LPBK_RXVALID LPBK_RXVALID is an internally reserved field. Do not use. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MISC_CONTROL_1_OFF

Address: Operational Base(0x00000700) + offset (0x01BC)

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Bit	Attr	Reset Value	Description
31:23	RO	0x000	RSVDP_23 Reserved for future use.
22	RW	0x0	PORT_LOGIC_WR_DISABLE Disable port logic register write from wire side. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
21	RW	0x0	P2P_ERR_RPT_CTRL Determines whether to enable Peer to Peer (P2P) error reporting. Note: This register field is sticky.
20	RW	0x0	P2P_TRACK_CPL_TO_REG Determines whether to track completion of transmitted Non-Posted TLPs in P2P mode. Note: This register field is sticky.
19:18	RW	0x2	TARGET_ABOVE_CONFIG_LIMIT_REG Configuration requests with an address greater than CONFIG_LIMIT_REG are directed to either ELBI or TRGT1 interface based on the setting of this field. This field can have the following values: Note: This register field is sticky.
17:8	RW	0x3ff	CONFIG_LIMIT_REG Configuration requests are directed either to CDM or ELBI/RTRGT1 based on the value of this field. - Configuration requests with an address less CONFIG_LIMIT_REG are directed to the CDM - Configuration requests with an address greater than CONFIG_LIMIT_REG are directed to either ELBI or TRGT1 interface based on the setting of TARGET_ABOVE_CONFIG_LIMIT_REG field. Your application must set a proper value for this field based on your extended configuration registers. For more details, see the "CDM/ELBI Register Space Access Through CFG Request" in "Register Module, LBC, and DBI" section in the "Controller Operations" chapter of the Databook. Note: This register field is sticky.
7	RW	0x0	CFG_TLP_BYPASS_EN_REG Setting of this field defines how to decide the destination of Configuration requests. Note: When app_req_retry_en is asserted, the setting of this field is ignored. Note: This register field is sticky.
6	RW	0x1	CPLQ_MNG_EN This field enables the Completion Queue Management feature. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
5	RW	0x0	ARI_DEVICE_NUMBER When ARI is enabled, this field enables use of the device ID. Note: This register field is sticky.
4	RW	0x0	DISABLE_AUTO_LTR_CLR_MSG Disable the autonomous generation of LTR clear message in upstream port. This field can have the following values: For more details, see "Latency Tolerance Reporting (LTR) Message Generation [EP Mode]" in "Message Generation" section of the "Controller Operations" chapter of the Databook. Note: This register field is sticky.
3	RW	0x0	SIMPLIFIED_REPLAY_TIMER Enables Simplified Replay Timer (Gen4). For more details, see "Transmit Replay" in "Transmit TLP Processing" section in the "Controller Operations" chapter of the Databook. Simplified Replay Timer can have the following Values: - A value from 24,000 to 31,000 Symbol Times when Extended Synch is 0b. - A value from 80,000 to 100,000 Symbol Times when Extended Synch is 1b. The Simplified Replay Timer value must not be changed while the link is in use. Note: This register field is sticky.
2	RW	0x0	UR_CA_MASK_4_TRGT1 When this field is set to '1', the controller suppresses error logging, error message generation, and CPL generation for non-posted requests TLPs (with UR filtering status) forwarded to your application (that is, when DEFAULT_TARGET =1). For more details, see "Advanced Error Handling For Received TLPs" chapter of the Databook. Note: This register field is sticky.
1	RW	0x0	DEFAULT_TARGET Default target for an IO or MEM request with UR/CA/CRS received. Based on the value of this field the controller either drops or forwards these requests to your application. For more details, see "ECRC Handling" and "Request TLP Routing Rules" in "Receive Routing" section of the "Controller Operations" chapter of the Databook. Note: This register field is sticky.
0	RW	0x0	DBI_RO_WR_EN Write to RO Registers Using DBI. For more details, see "Writing to Read-Only Registers" in "Register Module, LBC, and DBI" section in the "Controller Operations" chapter of the Databook. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_MULTI_LANE_CONTROL_OFF

Address: Operational Base(0x00000700) + offset (0x01C0)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	RSVDP_8 Reserved for future use.
7	RW	0x0	UPCONFIGURE_SUPPORT Upconfigure Support. The controller sends this value as the Link Upconfigure Capability in TS2 Ordered Sets in Configuration.Complete state. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
6	RW	0x0	DIRECT_LINK_WIDTH_CHANGE Directed Link Width Change. - If the upconfigure_capable variable is '1' and the PCIE_CAP_HW_AUTO_WIDTH_DISABLE bit in LINK_CONTROL_LINK_STATUS_REG is '0', the controller starts upconfigure or autonomous width downsizing (to the TARGET_LINK_WIDTH value) in the Configuration state. - If TARGET_LINK_WIDTH value is 0x0, the controller does not start upconfigure or autonomous width downsizing in the Configuration state. The controller self-clears this field when the controller accepts this request. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
5:0	RW	0x00	TARGET_LINK_WIDTH Target Link Width. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

PCIE_DSP_PF0_PORT_LOGIC_PHY_INTEROP_CTRL_OFF

Address: Operational Base(0x00000700) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	RSVDP_18 Reserved for future use.
17:12	RW	0x1e	PHY_RST_TIMER Decide how many aux clock cycles the PHY reset lasts (0 to 63 aux clock cycles). Note: This register field is sticky.
11	RO	0x0	reserved
10	RW	0x0	L1_CLK_SEL L1 Clock control bit. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
9	RO	0x1	L1_NOWAIT_P1 L1 entry control bit. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W (sticky) Note: This register field is sticky.
8	RW	0x0	L1SUB_EXIT_MODE L1 Exit Control Using phy_mac_pclkack_n. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. If PCLK as PHY input is selected, you should not write to this field and change the default value since PCLK as PHY input doesn't support any value other than the default. Note: This register field is sticky.
7	RO	0x0	RSVDP_7 Reserved for future use.
6:0	RW	0x01	RXSTANDBY_CONTROL Rxstandby Control. Bits 0..5 determine if the controller asserts the RxStandby signal (mac_phy_rxstandby) in the indicated condition. Bit 6 enables the controller to perform the RxStandby/RxStandbyStatus handshake. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. - [0]: Rx EIOS and subsequent T TX-IDLE-MIN - [1]: Rate Change - [2]: Inactive lane for upconfigure/downconfigure - [3]: PowerDown=P1orP2 - [4]: RxL0s.Idle - [5]: EI Infer in L0 - [6]: Execute RxStandby/RxStandbyStatus Handshake Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_TRGT_CPL_LUT_DELETE_ENTRY_OFF

Address: Operational Base(0x00000700) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31	WO	0x0	DELETE_EN This is a one-shot bit. This is a self-clearing register field. Reading from this register field always returns a '0'.

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Bit	Attr	Reset Value	Description
30:0	RW	0x00000000	LOOK_UP_ID This number selects one entry to delete of the TRGT_CPL_LUT.

PCIE_DSP_PF0_PORT_LOGIC_LINK_FLUSH_CONTROL_OFF

Address: Operational Base(0x00000700) + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	RSVD_I_8 This is an internally reserved field. Do not use. Note: This register field is sticky.
23:1	RO	0x000000	RSVDP_1 Reserved for future use.
0	RW	0x1	AUTO_FLUSH_EN Enables automatic flushing of pending requests before sending the reset request to the application logic to reset the PCIe controller and the AXI Bridge. The flushing process is initiated if any of the following events occur: - Hot reset request. A downstream port (DSP) can "hot reset" an upstream port (USP) by sending two consecutive TS1 ordered sets with the hot reset bit asserted. - Warm (Soft) reset request. Generated when exiting from D3 to D0 and cfg_pm_no_soft_rst=0. - Link down reset request. A high to low transition on smlh_req_rst_not indicates the link has gone down and the controller is requesting a reset. If you disable automatic flushing, your application is responsible for resetting the PCIe controller and the AXI Bridge. For more details see "Warm and Hot Resets" section in the Architecture chapter of the Databook. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_AMBA_ERROR_RESPONSE_DEFAULT_OFF

Address: Operational Base(0x00000700) + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	RSVDP_16 Reserved for future use.
15:10	RW	0x27	AMBA_ERROR_RESPONSE_MAP AXI Slave Response Error Map. Allows you to selectively map the errors received from the PCIe completion (for non-posted requests) to the AXI slave responses, slv_rresp or slv_bresp. The recommended setting is SLVERR. CRS is always mapped to OKAY. - [0] -- 0: UR (unsupported request) -> DECERR -- 1: UR (unsupported request) -> SLVERR - [1] -- 0: CRS (configuration retry status) -> DECERR -- 1: CRS (configuration retry status) -> SLVERR - [2] -- 0: CA (completer abort) -> DECERR -- 1: CA (completer abort) -> SLVERR - [3]: RESERVED (0x0) - [4]: RESERVED (0x0) - [5]

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Bit	Attr	Reset Value	Description
			-- 0: Completion Timeout -> DECERR -- 1: Completion Timeout -> SLVERR. The AXI bridge internally drops (processes internally but not passed to your application) a completion that has been marked by the Rx filter as UC or MLF, and does not pass its status directly down to the slave interface. It waits for a timeout and then signals "Completion Timeout" to the slave interface. The controller sets the AXI slave read databus to 0xFFFF for all error responses. Note: This register field is sticky.
9:5	RO	0x00	RSVDP_5 Reserved for future use.
4:3	RW	0x0	AMBA_ERROR_RESPONSE_CRS CRS Slave Error Response Mapping. Determines the AXI slave response for CRS completions. For more details see "Error Handling" in the AXI chapter of the Databook. Note: This register field is sticky.
2	RW	0x0	AMBA_ERROR_RESPONSE_VENDORID Vendor ID Non-existent Slave Error Response Mapping. Determines the AXI slave response for errors on reads to non-existent Vendor ID register. For more details see "Error Handling" in the AXI chapter of the Databook. Note: This register field is sticky.
1	RO	0x0	RSVDP_1 Reserved for future use.
0	RW	0x0	AMBA_ERROR_RESPONSE_GLOBAL Global Slave Error Response Mapping. Determines the AXI slave response for all error scenarios on non-posted requests. For more details see "Error Handling" in the AXI chapter of the Databook. The error response mapping is not applicable to Non-existent Vendor ID register reads. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_AMBA_LINK_TIMEOUT_OFF

Address: Operational Base(0x00000700) + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	RSVDP_9 Reserved for future use.
8	RW	0x0	LINK_TIMEOUT_ENABLE_DEFAULT Disable Flush. Note: This register field is sticky.
7:0	RW	0x32	LINK_TIMEOUT_PERIOD_DEFAULT Timeout Value (ms). The timer will timeout and then flush the bridge TX request queues after this amount of time. The timer counts when there are pending outbound AXI slave interface requests and the PCIe TX link is not transmitting any of these requests. The timer is clocked by core_clk. Note: This register field is sticky.

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PCIE_DSP_PF0_PORT_LOGIC_AMBA_ORDERING_CTRL_OFF

Address: Operational Base(0x00000700) + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	RSVDP_8 Reserved for future use.
7	RW	0x0	AX_MSTR_ZEROLREAD_FW AXI Master Zero Length Read Forward to the application. The DW PCIe controller AXI bridge is able to terminate in order with the Posted transactions the zero length read, implementing the PCIe express flush semantics of the Posted transactions.
6:5	RO	0x0	RSVDP_5 Reserved for future use.
4:3	RW	0x0	AX_MSTR_ORDR_P_EVENT_SEL AXI Master Posted Ordering Event Selector. This field selects how the master interface determines when a P write is completed when enforcing the PCIe ordering rule, "NP must not pass P" at the AXI Master Interface. The AXI protocol does not support ordering between channels. Therefore, NP reads can pass P on your AXI bus fabric. This can result in an ordering violation when the read overtakes a P that is going to the same address. Therefore, the bridge master does not issue any NP requests until all outstanding P writes reach their destination. It does this by waiting for the all of the write responses on the B channel. This can affect the performance of the master read channel. For scenarios where the interconnect serializes the AXI master "AW", "W" and "AR" channels,you can increase the performance by reducing the need to wait until the complete Posted transaction has effectively reached the application slave. Note: This setting will not affect: - MSI interrupt catcher and P data ordering. This is always driven by the B'last event. - DMA read engine TLP ordering. This is always driven by the B'last event. - NP write transactions which are always serialized with P write transactions.
2	RO	0x0	RSVDP_2 Reserved for future use.
1	RW	0x0	AX_SNP_EN AXI Serialize Non-Posted Requests Enable. This field enables the AXI Bridge to serialize same ID Non-Posted Read/Write Requests on the wire. Serialization implies one outstanding same ID NP Read or Write on the wire and used to avoid AXI RAR and WAW hazards at the remote link partner. For more details, see the "Optional Serialization of AXI Slave Non-posted Requests" section in the AXI chapter of the Databook.
0	RO	0x0	RSVDP_0 Reserved for future use.

PCIE_DSP_PF0_PORT_LOGIC_COHERENCY_CONTROL_1_OFF

Address: Operational Base(0x00000700) + offset (0x01E0)

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Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	CFG_MEMTYPE_BOUNDARY_LOW_ADDR Boundary Lower Address For Memory Type. Bits [31:0] of dword-aligned address of the boundary for Memory type. The two lower address LSBs are '00'. Addresses up to but not including this value are in the lower address space region; addresses equal or greater than this value are in the upper address space region. Note: This register field is sticky.
1	RO	0x0	RSVDP_1 Reserved for future use.
0	RW	0x0	CFG_MEMTYPE_VALUE Sets the memory type for the lower and upper parts of the address space: Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_COHERENCY_CONTROL_2_OFF

Address: Operational Base(0x00000700) + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CFG_MEMTYPE_BOUNDARY_HIGH_ADDR Boundary Upper Address For Memory Type. Bits [63:32] of the 64-bit dword-aligned address of the boundary for Memory type. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_COHERENCY_CONTROL_3_OFF

Address: Operational Base(0x00000700) + offset (0x01E8)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RW	0x0	CFG_MSTR_AWCACHE_VALUE Master Write CACHE Signal Value. Value of the individual bits in mstr_awcache when CFG_MSTR_AWCACHE_MODE is '1'. Note: Not applicable to message requests; for message requests the value of mstr_awcache is always '0000'. Note: This register field is sticky.
26:23	RO	0x0	reserved
22:19	RW	0x0	CFG_MSTR_ARCACHE_VALUE Master Read CACHE Signal Value. Value of the individual bits in mstr_arcache when CFG_MSTR_ARCACHE_MODE is '1'. Note: This register field is sticky.
18:15	RO	0x0	reserved
14:11	RW	0x0	CFG_MSTR_AWCACHE_MODE Master Write CACHE Signal Behavior. Defines how the individual bits in mstr_awcache are controlled. Note: for message requests the value of mstr_awcache is always "0000" regardless of the value of this bit. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
10:7	RO	0x0	reserved
6:3	RW	0x0	CFG_MSTR_ARCACHE_MODE Master Read CACHE Signal Behavior. Defines how the individual bits in mstr_arcache are controlled. Note: This register field is sticky.
2:0	RO	0x0	reserved

PCIE_DSP_PF0_PORT_LOGIC_AXI_MSTR_MSG_ADDR_LOW_OFF

Address: Operational Base(0x00000700) + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	CFG_AXIMSTR_MSG_ADDR_LOW Lower 20-bits of the programmable AXI address for Messages. Note: This register field is sticky.
11:0	RO	0x000	CFG_AXIMSTR_MSG_ADDR_LOW_RESERVED Reserved for future use. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_AXI_MSTR_MSG_ADDR_HIGH_OFF

Address: Operational Base(0x00000700) + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CFG_AXIMSTR_MSG_ADDR_HIGH Upper 32 bits of the programmable AXI address for Messages. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_PCIE_VERSION_NUMBER_OFF

Address: Operational Base(0x00000700) + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x3536302a	VERSION_NUMBER Version Number.

PCIE_DSP_PF0_PORT_LOGIC_PCIE_VERSION_TYPE_OFF

Address: Operational Base(0x00000700) + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x6c703035	VERSION_TYPE Version Type.

PCIE_DSP_PF0_PORT_LOGIC_PL_APP_BUS_DEV_NUM_STATUS_OFF

Address: Operational Base(0x00000700) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	RSVDP_16 Reserved for future use.
15:8	RO	0x00	RC_DSW_BUS_NUM This field reflects the value of bus number driven on app_bus_num input signal by your application. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
7:3	RO	0x00	RC_DSW_DEV_NUM This field reflects the value of device number driven on app_device_num input signal by your application. Note: This register field is sticky.
2:0	RO	0x0	RSVDP_0 Reserved for future use.

PCIE_DSP_PF0_PORT_LOGIC_PCIPM_TRAFFIC_CTRL_OFF

Address: Operational Base(0x00000700) + offset (0x041C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	RSVDP_8 Reserved for future use.
7:4	RO	0x0	PCIPM_RESERVED_4_7 Reserved. Note: This register field is sticky.
3	RW	0x0	PCIPM_NEW_TLP_CLIENT2_BLOCKED This field indicates that all TLPs transmitted by Client 2 interface are blocked during non-D0 states. Note: This register field is sticky.
2	RW	0x0	PCIPM_NEW_TLP_CLIENT1_BLOCKED This field indicates that all TLPs transmitted by Client 1 interface are blocked during non-D0 states. Note: This register field is sticky.
1	RW	0x0	PCIPM_NEW_TLP_CLIENT0_BLOCKED This field indicates that all TLPs transmitted by Client 0 interface are blocked during non-D0 states. Note: This register field is sticky.
0	RW	0x0	PCIPM_VDM_TRAFFIC_BLOCKED This field indicates that VDM Message TLPs are blocked during non-D0 states. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_PL_LTR_LATENCY_OFF

Address: Operational Base(0x00000700) + offset (0x0430)

Bit	Attr	Reset Value	Description
31	RW	0x0	NO_SNOOP_LATENCY_REQUIRE No Snoop Latency Requirement. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
30:29	RO	0x0	RSVDP_29 Reserved for future use.

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Bit	Attr	Reset Value	Description
28:26	RW	0x0	NO_SNOOP_LATENCY_SCALE No Snoop Latency Scale. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
25:16	RW	0x000	NO_SNOOP_LATENCY_VALUE No Snoop Latency Value. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
15	RW	0x0	SNOOP_LATENCY_REQUIRE Snoop Latency Requirement. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
14:13	RO	0x0	RSVDP_13 Reserved for future use.
12:10	RW	0x0	SNOOP_LATENCY_SCALE Snoop Latency Scale. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W
9:0	RW	0x000	SNOOP_LATENCY_VALUE Snoop Latency Value. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R/W

PCIE_DSP_PF0_PORT_LOGIC_AUX_CLK_FREQ_OFF

Address: Operational Base(0x00000700) + offset (0x0440)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	RSVDP_10 Reserved for future use.
9:0	RW	0x018	AUX_CLK_FREQ The aux_clk frequency in MHz. This value is used to provide a 1 us reference for counting time during low-power states with aux_clk when the PHY has removed the pipe_clk. Frequencies lower than 1 MHz are possible but with a loss of accuracy in the time counted. If the actual frequency (f) of aux_clk does not exactly match the programmed frequency (f_prog), then there is an error in the time counted by the controller that can be expressed in percentage as: err% = (f_prog/f-1)*100. For example if f=2.5 MHz and f_prog=3 MHz, then err% =(3/2.5-1)*100 =20%, meaning that the time counted by the controller on aux_clk will be 20% greater than the time in us programmed in the corresponding time register (for example T_POWER_ON). Note: This register field is sticky.

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PCIE_DSP_PF0_PORT_LOGIC_L1_SUBSTATES_OFF

Address: Operational Base(0x00000700) + offset (0x0444)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	RSVDP_9 Reserved for future use.
8	RW	0x0	L1SUB_LOW_POWER_CLOCK_SWITCH_MODE If the bit is set to 1'b1 the controller will delay the switching of aux_clk to the slow platform clock until it detects that the link partner has de-asserted CLKREQ#. Note: This register field is sticky.
7:6	RW	0x3	L1SUB_T_PCLKACK Max delay (in 1us units) between a MAC request to remove the clock on mac_phy_pclkreq_n and a PHY response on phy_mac_pclkack_n. If the PHY does not respond within this time the request is aborted. Range is 1..4 Note: This register field is sticky.
5:2	RW	0x4	L1SUB_T_L1_2 Duration (in 1us units) of L1.2. Range is 1..16. Note: This register field is sticky.
1:0	RW	0x2	L1SUB_T_POWER_OFF Duration (in 1us units) of L1.2.Entry. Range is 1..4. Note: This register field is sticky.

PCIE_DSP_PF0_PORT_LOGIC_POWERDOWN_CTRL_STATUS_OFF

Address: Operational Base(0x00000700) + offset (0x0448)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	RSVDP_12 Reserved for future use.
11:8	RO	0x2	POWERDOWN_PHY_POWERDOWN This field represents the Powerdown value that has been acknowledged by the PHY. It is updated with the value of Powerdown driven by the controller, when the PHY has returned the Phystatus acknowledgment for the Powerdown transition.
7:4	RO	0x2	POWERDOWN_MAC_POWERDOWN This field represents the Powerdown value driven by the controller to the PHY.
3:2	RO	0x0	RSVDP_2 Reserved for future use.
1	RW	0x0	POWERDOWN_VMAIN_ACK Set this bit to 1 if you do not want to perform the handshake with the power-switch after PERST# assertion. By default the controller will perform the handshake with the power-switch if L1 power gating is enabled Note: This register field is sticky.
0	WO	0x0	POWERDOWN_FORCE This field is a one shot field. This field could be used for debug purposes in event that the P2 Powerdown transition does not complete. It will allow the controller to proceed with the transition to the P1 Powerdown state. This field always reads back as 1'b0.

PCIE_DSP_PF0_PORT_LOGIC_PIPE_RELATED_OFF

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Address: Operational Base(0x00000700) + offset (0x0490)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	RSVDP_9 Reserved for future use.
8	RW	0x0	PIPE_GARBAGE_DATA_MODE PIPE Garbage Data Mode. - RxValid is deasserted - a valid RxStartBlock is received at 128b/130b encoding - a valid COM symbol is received at 8b/10b encoding Note: This register field is sticky.
7:0	RO	0x00	reserved

14.4.3.11 PCIE_DSP_PF0_PCIE_CAP_DBI2 Register Description

14.4.3.11.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_PCIE_CAP_DBI2_SHADOW_LINK_CAPABILITIES_REG	0x000C	W	0x0073EC13	This is a 7-bit register at the same address as LINK_CAPABILITIES_REG, and it only exists when one or more of the following expressions are true: - CX_NFTS !=CX_COMM_NFTS - DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY - DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCYThe register has only two fields in RTL. All of the other fields here do not exist in RTL and accesses to them are redirected to the corresponding fields in the parent register (LINK_CAPABILITIES_REG).They are modeled here to make the shadow register (model) 32 bits wide which is a tool requirement.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3.11.2 Detail Registers Description

PCIE_DSP_PF0_PCIE_CAP_DBI2_SHADOW_LINK_CAPABILITIES_REG

Address: Operational Base(0x00100000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	PCIE_CAP_PORT_NUM Shadow Port Number. This field indicates the PCI Express Port number for the given PCI Express Link. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R

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Bit	Attr	Reset Value	Description
23	RO	0x0	RSVDP_23 Reserved for future use.
22	RO	0x1	PCIE_CAP_ASPM_OPT_COMPLIANCE Shadow ASPM Optionality Compliance. This field must be set to 1b in all functions. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
21	RO	0x1	PCIE_CAP_LINK_BW_NOT_CAP Shadow Link Bandwidth Notification Capable. A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. This capability is required for all Root Ports and Switch Downstream Ports supporting Links wider than x1 and/or multiple Link speeds. This field is not applicable and is Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
20	RO	0x1	PCIE_CAP_DLL_ACTIVE_REP_CAP Shadow Data Link Layer Link Active Reporting Capable. For a Downstream Port, the controller hardwires this bit to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port (as indicated by the Hot-Plug Capable bit of the Slot Capabilities register) or a Downstream Port that supports Link speeds greater than 5.0 GT/s, the controller hardwires this bit to 1b. For Upstream Ports and components that do not support this optional capability, the controller hardwires this bit to 0b.
19	RO	0x0	PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP Shadow Surprise Down Error Reporting Capable. For a Downstream Port, this bit must be set if the component supports the optional capability of detecting and reporting a Surprise Down error condition. For Upstream Ports and components that do not support this optional capability, the controller hardwires this bit to 0b. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
18	RO	0x0	PCIE_CAP_CLOCK_POWER_MAN Shadow Clock Power Management. For Upstream Ports, a value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) via the "clock request" (CLKREQ#) mechanism when the Link is in the L1 and L2/L3 Ready Link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these Link states. L1 PM Substates defines other semantics for the CLKREQ# signal, which are managed independently of Clock Power Management. This Capability is applicable only in form factors that support "clock request" (CLKREQ#) capability. For a Multi-Function device associated with an Upstream Port, each Function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the Multi-Function device indicate a 1b in this bit. For ARI Devices, all Functions must indicate the same value in this bit. For Downstream Ports, the controller hardwires this bit to 0b. Note: This register field is sticky.
17:15	RO	0x7	SHADOW_PCIE_CAP_L1_EXIT_LATENCY Shadow L1 Exit Latency. There are two each of these register fields, this one and a shadow one at the same address. The Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG) determines which one is used by the controller and which one is accessed by a read request. Common Clock operation is supported (possible) in the controller when one or more of the following expressions is true: - CX_NFTS !=CX_COMM_NFTS - DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY - DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Common Clock operation is enabled in the controller when you set the Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG). The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the shadow field at this location. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R - Dbi2: R/W

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Bit	Attr	Reset Value	Description
14:12	RO	0x6	SHADOW_PCIE_CAP_L0S_EXIT_LATENCY Shadow L0s Exit Latency. There are two each of these register fields, this one and a shadow one at the same address. The Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG) determines which one is used by the controller and which one is accessed by a read request. Common Clock operation is supported (possible) in the controller when one or more of the following expressions is true: - CX_NFTS !=CX_COMM_NFTS - DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY - DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Common Clock operation is enabled in the controller when you set the Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG). The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the shadow field at this location. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R - Dbi2: R/W
11:10	RO	0x3	PCIE_CAP_ACTIVE_STATE_LINK_PM_SUPPORT Shadow Level of ASPM (Active State Power Management) Support. This field indicates the level of ASPM supported on the given PCI Express Link. For more details on ASPM support requirements, see section 5.4.1 of PCI Express Base Specification. Multi-Function devices associated with an Upstream Port must report the same value in this field for all functions. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
9:4	RO	0x01	PCIE_CAP_MAX_LINK_WIDTH Shadow Maximum Link Width. This field indicates the maximum Link width (xN - corresponding to N Lanes) implemented by the component. This value is permitted to exceed the number of Lanes routed to the slot (Downstream Port), adapter connector (Upstream Port), or in the case of component-to-component connections, the actual wired connection width. All encodings other than the defined encodings are reserved. Multi-Function devices associated with an Upstream Port must report the same value in this field for all functions. In M-PCIe mode, the reset and dynamic values of this field are calculated by the controller. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
3:0	RO	0x3	PCIE_CAP_MAX_LINK_SPEED Shadow Maximum Link Speed. This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. All encodings other than the defined encodings are reserved. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. In M-PCIe mode, the reset and dynamic values of this field are calculated by the controller. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.

14.4.3.12 PCIE_DSP_PF0_MSIX_CAP_DBI2 Register Description

14.4.3.12.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_MSIX_CAP_DBI2_SHADOW_PCI_MSIX_CAP_ID_NEXT_CTRL_REG	0x0000	W	0x00000000	This is the shadow register of the MSI-X Capability ID, Next Pointer, and Control Register.
PCIE_DSP_PF0_MSIX_CAP_DBI2_SHADOW_MSIX_TABLE_OFFSET_REG	0x0004	W	0x00000000	This register provides Table BIR and MSI-x Table offset select.
PCIE_DSP_PF0_MSIX_CAP_DBI2_SHADOW_MSIX_PBA_OFFSET_REG	0x0008	W	0x00000010	This register provides PBA Offset and PBA BIR value.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-*

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Double WORD (64 bits) access

14.4.3.12.2 Detail Registers Description

PCIE_DSP_PF0_MSIX_CAP_DBI2_SHADOW_PCI_MSIX_CAP_ID_NEXT_CTRL_REG

Address: Operational Base(0x001000B0) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	PCI_MSIX_RESERVED1 reserved field 1 in the shadow register. Note: This register field is sticky.
26:16	RO	0x000	PCI_MSIX_TABLE_SIZE MSI-X Table Size in the shadow register. Note: The access attributes of this field are as follows: - Wire: No access - Dbi: No access - Dbi2: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky.
15:0	RO	0x0000	PCI_MSIX_RESERVED0 reserved field 0 in the shadow register. Note: This register field is sticky.

PCIE_DSP_PF0_MSIX_CAP_DBI2_SHADOW_MSIX_TABLE_OFFSET_REG

Address: Operational Base(0x001000B0) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	PCI_MSIX_TABLE_OFFSET MSI-X Table Offset. Used as an offset from the address contained by one of the Function's Base Address Registers to point to the base of the MSI-X Table. The lower 3 Table BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. Note: The access attributes of this field are as follows: - Wire: No access - Dbi: No access - Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky.
2:0	RO	0x0	PCI_MSIX_BIR MSI-X Table BAR Indicator Register Field. This field indicates which one of a Function's Base Address Registers , located beginning at 10h in Configuration Space, or entry in the Enhanced Allocation capability with a matching BEI , is used to map the Function's MSI-X Table into Memory Space. All encodings other than the defined encodings are reserved. For a 64-bit Base Address Register , the Table BIR indicates the lower DWORD. For Functions with Type 1 Configuration Space headers, BIR values 2 through 5 are also Reserved. Note: The access attributes of this field are as follows: - Wire: No access - Dbi: No access - Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky.

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PCIE_DSP_PF0_MSIX_CAP_DBI2_SHADOW_MSIX_PBA_OFFSET_REG

Address: Operational Base(0x001000B0) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000002	PCI_MSIX_PBA_OFFSET MSI-X PBA Offset. Used as an offset from the address contained by one of the Function's Base Address Registers to point to the base of the MSI-X PBA. The lower 3 PBA BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. Note: The access attributes of this field are as follows: - Wire: No access - Dbi: No access - Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky.
2:0	RO	0x0	PCI_MSIX_PBA_BIR MSI-X PBA BIR. This field indicates which one of a Function's Base Address Registers , located beginning at 10h in Configuration Space, or entry in the Enhanced Allocation capability with a matching BEI, is used to map the Function's MSI-X PBA into Memory Space. The PBA BIR value definitions are identical to those for the Table BIR . Note: The access attributes of this field are as follows: - Wire: No access - Dbi: No access - Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky.

14.4.3.13 PCIE_DSP_PF0_ATU_CAP Register Description

14.4.3.13.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_0	0x0000	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_0	0x0004	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_0	0x0008	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_0	0x000C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_0	0x0010	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_0	0x0014	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_0	0x0018	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_0	0x0020	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_0	0x0100	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_0	0x0104	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_0	0x0108	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_0	0x010C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_0	0x0110	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_0	0x0114	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_0	0x0118	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_0	0x0120	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_1	0x0200	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_1	0x0204	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_1	0x0208	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_1	0x020C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_1	0x0210	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_1	0x0214	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_1	0x0218	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_1	0x0220	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_1	0x0300	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_1	0x0304	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_1	0x0308	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_1	0x030C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_1	0x0310	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_1	0x0314	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_1	0x0318	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_1	0x0320	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_2	0x0400	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_2	0x0404	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_2	0x0408	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_2	0x040C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_2	0x0410	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_2	0x0414	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_2	0x0418	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_2	0x0420	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_2	0x0500	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_2	0x0504	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_2	0x0508	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_2	0x050C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_2	0x0510	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_2	0x0514	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_2	0x0518	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_2	0x0520	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_3	0x0600	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_3	0x0604	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_3	0x0608	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_3	0x060C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_3	0x0610	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_3	0x0614	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_3	0x0618	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_3	0x0620	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_3	0x0700	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_3	0x0704	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_3	0x0708	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_3	0x070C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_3	0x0710	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_3	0x0714	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_3	0x0718	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_3	0x0720	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_4	0x0800	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_4	0x0804	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_4	0x0808	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_4	0x080C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_4	0x0810	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_4	0x0814	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_4	0x0818	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_4	0x0820	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_4	0x0900	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_4	0x0904	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_4	0x0908	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_4	0x090C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_4	0x0910	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_4	0x0914	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_4	0x0918	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_4	0x0920	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_5	0x0A00	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_5	0x0A04	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_5	0x0A08	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_5	0x0A0C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_5	0x0A10	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_5	0x0A14	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_5	0x0A18	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_5	0x0A20	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_5	0x0B00	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_5	0x0B04	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_5	0x0B08	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_5	0x0B0C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_5	0x0B10	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_5	0x0B14	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_5	0x0B18	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_5	0x0B20	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_6	0x0C00	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_6	0x0C04	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_6	0x0C08	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_6	0x0C0C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_6	0x0C10	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_6	0x0C14	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_6	0x0C18	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_6	0x0C20	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_6	0x0D00	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_6	0x0D04	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_6	0x0D08	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_6	0x0D0C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_6	0x0D10	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_6	0x0D14	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_6	0x0D18	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_6	0x0D20	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_7	0x0E00	W	0x00000000	This register controls the iATU outbound region access based on the optional iATU outbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_7	0x0E04	W	0x00000000	Using this register you can enable/disable the outbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_7	0x0E08	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_7	0x0E0C	W	0x00000000	This register holds the upper 32-bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_7	0x0E10	W	0x0000FFFF	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_7	0x0E14	W	0x00000000	This register holds the Lower Target part of the new address of the translated region, or the outbound TLP header information, depending on the setting of HEADER_SUBSTITUTE_EN field of IATU_REGION_CTRL_2_VIEWPORT_OFF_OUTBOUND_i register.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_7	0x0E18	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_7	0x0E20	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0->32, 8=1TB) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_7	0x0F00	W	0x00000000	This register controls the iATU inbound region access based on the optional iATU inbound features enabled using iATU Region Control 2 Register.
PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_7	0x0F04	W	0x00000000	Using this register you can enable/disable the inbound iATU optional features.

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Name	Offset	Size	Reset Value	Description
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_7	0x0F08	W	0x00000000	The CX_ATU_MIN_REGION_SIZE configuration parameter (Value Range: 4 kB, 8 kB, 16 kB, 32 kB, 64 kB defaults to 64 kB) specifies the minimum size of an address translation region. For example, if set to 64 kB; the lower 16 bits of the Base, Limit and Target registers are zero and all address regions are aligned on 64 kB boundaries. More precisely, the lower log2(CX_ATU_MIN_REGION_SIZE) bits are zero.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_7	0x0F0C	W	0x00000000	This register holds the upper 32 bits of the start (and end) address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_7	0x0F10	W	0x0000FFF0	This register holds the end address of the address region to be translated.
PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_7	0x0F14	W	0x00000000	This register holds the Lower Target part of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_7	0x0F18	W	0x00000000	This register holds the upper 32 bits of the start address (Upper Target part) of the new address of the translated region.
PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_7	0x0F20	W	0x00000000	The CX_MAX_ATU_REGION_SIZE configuration parameter (Value Range: 0(4GB) to 32(16 EB)) specifies the maximum region size of an address translation region. This register is only used when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3.13.2 Detail Registers Description

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_0

Address: Operational Base(0x00300000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_0

Address: Operational Base(0x00300000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space. Note: This register field is sticky.
27:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are define as above. Note: This register field is sticky.
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_0

Address: Operational Base(0x00300000) + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_0

Address: Operational Base(0x00300000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_0

Address: Operational Base(0x00300000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_0

Address: Operational Base(0x00300000) + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_0

Address: Operational Base(0x00300000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_0

Address: Operational Base(0x00300000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_0

Address: Operational Base(0x00300000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_0

Address: Operational Base(0x00300000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similarly with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_0

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Address: Operational Base(0x00300000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_0

Address: Operational Base(0x00300000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_0

Address: Operational Base(0x00300000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: - 0000b: 0 (Default; legacy Single Address Location mode) - 0001b: 4 - 0010b: 8 - 0011b: 16 - 0100b: 32 - 0101b: 64 - 0110b: 128 - 0111b: 256 - 1000b: 512 - 1001b: 1024 - 1010b: 2048 - 1011b: 4096 - 1100b: 8192 - 1101b: rsvd. - 1110b: rsvd. - 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_0

Address: Operational Base(0x00300000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_0

Address: Operational Base(0x00300000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_0

Address: Operational Base(0x00300000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_1

Address: Operational Base(0x00300000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_1

Address: Operational Base(0x00300000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space. Note: This register field is sticky.
27:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are define as above. Note: This register field is sticky.
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_1

Address: Operational Base(0x00300000) + offset (0x0208)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_1

Address: Operational Base(0x00300000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_1

Address: Operational Base(0x00300000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_1

Address: Operational Base(0x00300000) + offset (0x0214)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_1

Address: Operational Base(0x00300000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_1

Address: Operational Base(0x00300000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_1

Address: Operational Base(0x00300000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_1

Address: Operational Base(0x00300000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similarly with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_1

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Address: Operational Base(0x00300000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_1

Address: Operational Base(0x00300000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_1

Address: Operational Base(0x00300000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: - 0000b: 0 (Default; legacy Single Address Location mode) - 0001b: 4 - 0010b: 8 - 0011b: 16 - 0100b: 32 - 0101b: 64 - 0110b: 128 - 0111b: 256 - 1000b: 512 - 1001b: 1024 - 1010b: 2048 - 1011b: 4096 - 1100b: 8192 - 1101b: rsvd. - 1110b: rsvd. - 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_1

Address: Operational Base(0x00300000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_1

Address: Operational Base(0x00300000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_1

Address: Operational Base(0x00300000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_2

Address: Operational Base(0x00300000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_2

Address: Operational Base(0x00300000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space. Note: This register field is sticky.
27:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are define as above. Note: This register field is sticky.
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_2

Address: Operational Base(0x00300000) + offset (0x0408)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_2

Address: Operational Base(0x00300000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_2

Address: Operational Base(0x00300000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_2

Address: Operational Base(0x00300000) + offset (0x0414)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_2

Address: Operational Base(0x00300000) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_2

Address: Operational Base(0x00300000) + offset (0x0420)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_2

Address: Operational Base(0x00300000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_2

Address: Operational Base(0x00300000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similarly with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_2

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Address: Operational Base(0x00300000) + offset (0x0508)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_2

Address: Operational Base(0x00300000) + offset (0x050C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_2

Address: Operational Base(0x00300000) + offset (0x0510)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: - 0000b: 0 (Default; legacy Single Address Location mode) - 0001b: 4 - 0010b: 8 - 0011b: 16 - 0100b: 32 - 0101b: 64 - 0110b: 128 - 0111b: 256 - 1000b: 512 - 1001b: 1024 - 1010b: 2048 - 1011b: 4096 - 1100b: 8192 - 1101b: rsvd. - 1110b: rsvd. - 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_2

Address: Operational Base(0x00300000) + offset (0x0514)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_2

Address: Operational Base(0x00300000) + offset (0x0518)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_2

Address: Operational Base(0x00300000) + offset (0x0520)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_3

Address: Operational Base(0x00300000) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_3

Address: Operational Base(0x00300000) + offset (0x0604)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space. Note: This register field is sticky.
27:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are define as above. Note: This register field is sticky.
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_3

Address: Operational Base(0x00300000) + offset (0x0608)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_3

Address: Operational Base(0x00300000) + offset (0x060C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_3

Address: Operational Base(0x00300000) + offset (0x0610)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_3

Address: Operational Base(0x00300000) + offset (0x0614)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_3

Address: Operational Base(0x00300000) + offset (0x0618)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_3

Address: Operational Base(0x00300000) + offset (0x0620)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_3

Address: Operational Base(0x00300000) + offset (0x0700)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_3

Address: Operational Base(0x00300000) + offset (0x0704)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similarly with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_3

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Address: Operational Base(0x00300000) + offset (0x0708)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_3

Address: Operational Base(0x00300000) + offset (0x070C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_3

Address: Operational Base(0x00300000) + offset (0x0710)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: - 0000b: 0 (Default; legacy Single Address Location mode) - 0001b: 4 - 0010b: 8 - 0011b: 16 - 0100b: 32 - 0101b: 64 - 0110b: 128 - 0111b: 256 - 1000b: 512 - 1001b: 1024 - 1010b: 2048 - 1011b: 4096 - 1100b: 8192 - 1101b: rsvd. - 1110b: rsvd. - 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_3

Address: Operational Base(0x00300000) + offset (0x0714)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_3

Address: Operational Base(0x00300000) + offset (0x0718)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_3

Address: Operational Base(0x00300000) + offset (0x0720)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_4

Address: Operational Base(0x00300000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_4

Address: Operational Base(0x00300000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space. Note: This register field is sticky.
27:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are define as above. Note: This register field is sticky.
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_4

Address: Operational Base(0x00300000) + offset (0x0808)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_4

Address: Operational Base(0x00300000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_4

Address: Operational Base(0x00300000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_4

Address: Operational Base(0x00300000) + offset (0x0814)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_4

Address: Operational Base(0x00300000) + offset (0x0818)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_4

Address: Operational Base(0x00300000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_4

Address: Operational Base(0x00300000) + offset (0x0900)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_4

Address: Operational Base(0x00300000) + offset (0x0904)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similarly with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_4

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Address: Operational Base(0x00300000) + offset (0x0908)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_4

Address: Operational Base(0x00300000) + offset (0x090C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_4

Address: Operational Base(0x00300000) + offset (0x0910)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: - 0000b: 0 (Default; legacy Single Address Location mode) - 0001b: 4 - 0010b: 8 - 0011b: 16 - 0100b: 32 - 0101b: 64 - 0110b: 128 - 0111b: 256 - 1000b: 512 - 1001b: 1024 - 1010b: 2048 - 1011b: 4096 - 1100b: 8192 - 1101b: rsvd. - 1110b: rsvd. - 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_4

Address: Operational Base(0x00300000) + offset (0x0914)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_4

Address: Operational Base(0x00300000) + offset (0x0918)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_4

Address: Operational Base(0x00300000) + offset (0x0920)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_5

Address: Operational Base(0x00300000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_5

Address: Operational Base(0x00300000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space. Note: This register field is sticky.
27:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are define as above. Note: This register field is sticky.
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_5

Address: Operational Base(0x00300000) + offset (0x0A08)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_5

Address: Operational Base(0x00300000) + offset (0x0A0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_5

Address: Operational Base(0x00300000) + offset (0x0A10)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_5

Address: Operational Base(0x00300000) + offset (0x0A14)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_5

Address: Operational Base(0x00300000) + offset (0x0A18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_5

Address: Operational Base(0x00300000) + offset (0x0A20)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_5

Address: Operational Base(0x00300000) + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_5

Address: Operational Base(0x00300000) + offset (0x0B04)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.

Bit	Attr	Reset Value	Description
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similarly with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_5

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Address: Operational Base(0x00300000) + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_5

Address: Operational Base(0x00300000) + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_5

Address: Operational Base(0x00300000) + offset (0x0B10)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: - 0000b: 0 (Default; legacy Single Address Location mode) - 0001b: 4 - 0010b: 8 - 0011b: 16 - 0100b: 32 - 0101b: 64 - 0110b: 128 - 0111b: 256 - 1000b: 512 - 1001b: 1024 - 1010b: 2048 - 1011b: 4096 - 1100b: 8192 - 1101b: rsvd. - 1110b: rsvd. - 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_5

Address: Operational Base(0x00300000) + offset (0x0B14)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_5

Address: Operational Base(0x00300000) + offset (0x0B18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_5

Address: Operational Base(0x00300000) + offset (0x0B20)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_6

Address: Operational Base(0x00300000) + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_6

Address: Operational Base(0x00300000) + offset (0x0C04)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space. Note: This register field is sticky.
27:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are define as above. Note: This register field is sticky.
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_6

Address: Operational Base(0x00300000) + offset (0x0C08)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_6

Address: Operational Base(0x00300000) + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_6

Address: Operational Base(0x00300000) + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_6

Address: Operational Base(0x00300000) + offset (0x0C14)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_6

Address: Operational Base(0x00300000) + offset (0x0C18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_6

Address: Operational Base(0x00300000) + offset (0x0C20)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_6

Address: Operational Base(0x00300000) + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_6

Address: Operational Base(0x00300000) + offset (0x0D04)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similarly with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_6

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Address: Operational Base(0x00300000) + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_6

Address: Operational Base(0x00300000) + offset (0x0D0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_6

Address: Operational Base(0x00300000) + offset (0x0D10)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: - 0000b: 0 (Default; legacy Single Address Location mode) - 0001b: 4 - 0010b: 8 - 0011b: 16 - 0100b: 32 - 0101b: 64 - 0110b: 128 - 0111b: 256 - 1000b: 512 - 1001b: 1024 - 1010b: 2048 - 1011b: 4096 - 1100b: 8192 - 1101b: rsvd. - 1110b: rsvd. - 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_6

Address: Operational Base(0x00300000) + offset (0x0D14)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_6

Address: Operational Base(0x00300000) + offset (0x0D18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_6

Address: Operational Base(0x00300000) + offset (0x0D20)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_OUTBOUND_7

Address: Operational Base(0x00300000) + offset (0x0E00)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky.
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_OUTBOUND_7

Address: Operational Base(0x00300000) + offset (0x0E04)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space. Note: This register field is sticky.
27:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are define as above. Note: This register field is sticky.
21	RW	0x0	TLP_HEADER_FIELDS_BYPASS TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are - TC - PH - TH - ST - AT - Attr (IDO, RO and NS). Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_7

Address: Operational Base(0x00300000) + offset (0x0E08)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_7

Address: Operational Base(0x00300000) + offset (0x0E0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_OUTBOUND_7

Address: Operational Base(0x00300000) + offset (0x0E10)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.
3:0	RO	0xf	CBUF_INCR Circular Buffer. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_7

Address: Operational Base(0x00300000) + offset (0x0E14)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): - LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; - LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). - n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': - LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_7

Address: Operational Base(0x00300000) + offset (0x0E18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_7

Address: Operational Base(0x00300000) + offset (0x0E20)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_1_OFF_INBOUND_7

Address: Operational Base(0x00300000) + offset (0x0F00)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:20	RW	0x0	CTRL_1_FUNC_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_REGION_CTRL_2_OFF_INBOUND_7

Address: Operational Base(0x00300000) + offset (0x0F04)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky.
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that - CfgRd0 and CfgRd1 TLPs are seen as identical. Similarly with CfgWr0 and CfgWr1. - MWr, MRd, and MRdLk TLPs are seen as identical - The Routing field of Msg/MsgD TLPs is ignored - FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Reserved. You must set this bit to '0'. Note: This register field is sticky.
18:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved
10:8	RW	0x0	BAR_NUM Reserved. You must set this bit to '0' Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_BASE_ADDR_OFF_INBOUND_7

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Address: Operational Base(0x00300000) + offset (0x0F08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_BASE_ADDR_OFF_INBOUND_7

Address: Operational Base(0x00300000) + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LIMIT_ADDR_OFF_INBOUND_7

Address: Operational Base(0x00300000) + offset (0x0F10)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky.
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: - 0000b: 0 (Default; legacy Single Address Location mode) - 0001b: 4 - 0010b: 8 - 0011b: 16 - 0100b: 32 - 0101b: 64 - 0110b: 128 - 0111b: 256 - 1000b: 512 - 1001b: 1024 - 1010b: 2048 - 1011b: 4096 - 1100b: 8192 - 1101b: rsvd. - 1110b: rsvd. - 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated. Note: The access attributes of this field are as follows: - Wire: No access. - Dbi: R (sticky) Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_LWR_TARGET_ADDR_OFF_INBOUND_7

Address: Operational Base(0x00300000) + offset (0x0F14)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. - Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. - Field size depends on log2(BAR_MASK+1) in BAR match mode.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_7

Address: Operational Base(0x00300000) + offset (0x0F18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

PCIE_DSP_PF0_ATU_CAP_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_7

Address: Operational Base(0x00300000) + offset (0x0F20)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'.
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky.

14.5 Interface Description

Table 14-3 PCIe IO Usage Model

Signal name	Direction	IO Attribute
CLKREQN	I/O	Open Drain, pull up

Table 14-4 PCIe0 RC G2 Interface Description

Module Pin	Dir	Group	Pin Name	IOMUX Setting
pcie_clkreq_in/out_n	I/O	M0	VI_CIF_D11/SDMMC1_CMD_M1/ETH0_TXD3_M1/SAI0_SDI2_M0/PDM0_SDI1_M3/UART1_CTSN_M1/SPI4_CSN0_M3/PCI	TOP_IOC_GPIO2B_IOMUX_SEL_L[11:8]=4'hb

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Module Pin	Dir	Group	Pin Name	IOMUX Setting
			E0_CLKREQN_M0/GPIO2_B2_d	
		M1	ETH1_RXCLK_M1/SDMMC1_D2_M0/SAI3_SDO_M1/UART3_CTSN_M2/SPI1_MISO_M0/PCIE0_CLKREQN_M1/GPIO1_B6_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[11:8]=4'hc
		M2	SPDIF_TX0_M0/FLEXBUS0_D15_M1/UART2_TX_M1/I2C3_SCL_M0/PCIE0_CLKREQN_M2/CAN1_TX_M2/GPIO4_B5_d	TOP_IOC_GPIO4B_IOMUX_SEL_H[7:4]=4'hc
		M3	SAI4_SDI_M2/VP1_SYNC_OUT/PCIE0_CLKREQN_M3/SATA0_ACTLED_M1/I2C6_SCL_M3/SPI4_MISO_M0/CAN1_TX_M1/PWM2_CH2_M1/GPIO4_C6_d	VCCIO6_IOC_GPIO4C_IOMUX_ SEL_H[11:8]=4'h9
pcie_button_n	I		ETH1_TXD0_M1/FSPI1_D0_M1/UART4_TX_M1/UART2_RTSN_M0/SPI2_MOSI_M1/PCIE0_BUTTONRSTN/GPIO1_C4_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[3:0]=4'hc

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 14-5 PCIe1 RC G2 Interface Description

Module Pin	Dir	Group	Pin Name	IOMUX Setting
pcie_clkreq_in/out_n	I/O	M0	VI_CIF_D10/SDMMC1_CLK_M1/ETH0_TXCLK_M1/SAI0_SDO2_M0/PDM0_CLK1_M3/UART1_RTSN_M1/SPI4_CLK_M3/PCIE1_CLKREQN_M0/GPIO2_B3_d	TOP_IOC_GPIO2B_IOMUX_SEL_L[15:12]=4'hb
		M1	ETH1_RXD2_M1/SDMMC1_D0_M0/SAI3_SCLK_M1/I2C9_SDA_M1/SPI1_CLK_M0/PCIE1_CLKREQN_M1/PWM1_CH0_M1/GPIO1_B4_d	TOP_IOC_GPIO1B_IOMUX_SEL_H[3:0]=4'hc
		M2	SAI1_LRCK_M0/FLEXBUS1_D12_M1/SPI4_CSN1_M2/UART5_CTSN_M1/I2C2_SDA_M2/PCIE1_CLKREQN_M2/GPIO4_A5_d	TOP_IOC_GPIO4A_IOMUX_SEL_H[7:4]=4'hc
		M3	DSM_AUD_LN_M1/HDMI_TX_HPDIN_M0/PCIE1_CLKREQN_M3/I2C7_SDA_M3/EDP_TX_HPDIN_M0/UART11_RX_M2/PWM0_CH1_M1/GPIO4_C1_d	VCCIO6_IOC_GPIO4C_IOMUX_ SEL_L[7:4]=4'ha
pcie_button_n	I		ETH1_TXD1_M1/FSPI1_D1_M1/UART4_RX_M1/UART2_CTSN_M0/SPI2_MISO_M1/PCIE1_BUTTONRSTN/GPIO1_C5_d	TOP_IOC_GPIO1C_IOMUX_SEL_H[7:4]=4'hc

Notes: I=input, O=output, I/O=input/output, bidirectional

14.6 Application Notes

14.6.1 Clock and Reset

14.6.1.1 Clock Overview

The PCIe module uses multiple clock domains, it consists of system bus clocks (APB and AXI), Core function clock, PIPE interface clock, Power management clock, and PCIe PHY reference clock.

Table 14-6 Clock Overview

Clock Name	Note
pclk/core_clk/pipe_clk	PIPE and Core clock from PHY PLL generated
mstr_aclk	AXI master clock
slv_aclk	AXI slave clock
dbi_aclk	DBI AXI slave clock
aux_clk	Low power clock(XIN OSC clock)
apb_clk	APB slave clock for Client

The system bus clock is generated from SOC main PLL internally, please refer to the relative CRU for details. System bus clock gating is handled automatically by PCIe controller.

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Core function clock is derived from the PIPE interface clock output from the PCIe PHY. In specific low power state, core function clock is gated and switch to Power management clock automatically. After power up, if the PHY is not ready(phystatus is not de-assert), accessing the core through AXI slave will be held until it is ready.

The PHY TX PLL generates PIPE interface clock from the platform reference clock. The PCIe link Training and transaction is completely dependent upon availability of this clock. Application should not initiate transactions before ensuring that the PHY PLL is locked.

The Power management clock which should be fixed with XIN OSC clock driven by crystal input clock. The PCIe controller uses this clock for counting time during L1 substates. You must program the frequency of this clock into the L1_SUBSTATES_OFF register with a value of XIN OSC clock to count real time.

Many PCIe connections, especially backplane connections, require a synchronous reference clock between the two link partners. To achieve this a common clock source, referred to as REFCLK in the PCI Express Card Electromechanical Specification, should be used by both ends of the PCIe link.

14.6.1.2 PCIe PHY Reference Clock

The PHY usually use the external dedicated 100M differential clock as reference clock, the clock should be compatible with the CEM specification.

For low BOM cost usage, In RC mode, PCIe PHY can use internal single-ended clock which can be configured to 24Mhz(Combo PHY), 100Mhz(Combo PHY). Meanwhile, In Combo PHY mode, PCIe PHY can provide differential clock output for system application. The source of differential clock output can be select from internal single-ended clock or PHY TX PLL.

14.6.1.3 Reset Overview

14.6.1.3.1 Power-On Reset

The power-on reset is used as Cold reset of the PCIe. The entire module is reset when power-on reset is asserted and generate a phy_rst_n to reset the PHY link. After de-assertion of the power-on reset, the PCIe PHY and PCIe Core function reset keeps until the software release. Software should finish PCIe PHY initialization before de-asserting the power-on reset. The power-on reset is controlled by CRU, the power-on reset is keep asserted until the software de-assert the reset request.

14.6.1.3.2 System reset

The PCIe Controller has the following distinct resets, all of these are configurable through software driver. This section describes the function of each of the reset inputs.

- button_rst_n: Button reset from board if related IO has been used. section for more information. This reset has an equal functionality with power-on reset.
- perst_n: This reset works as Warm Reset of PCIe if related IO has been used.
- core_rst_n: This is the main reset for the PCIe Controller. It resets all the logic in the core running in the CORE_CLK(partial of PCLK) domain, except for the PMC module. It keeps reset with power-up reset by default. It also should be asserted when Hot Reset or link down reset occurs, but Application software can delay core_rst_n been asserted until system is ready to do core reset. This delayed reset operation will be discussed in next section.
- AXI Reset: All three AXI interface has its own reset input: mstr_aresetn, slv_aresetn, dbi_resetn. Each resets all logic in the specific AXI clock domain. Typically, these resets are be asserted whenever core_rst_n is asserted. Application software shall have the knowledge of choosing an appropriate time to drive this reset to avoid times when a transaction is in flight.
- non_sticky_rst_n: Resets all non-sticky bit registers in the configuration register space.
- sticky_rst_n : Resets all sticky bit registers in the configuration register space.
- pwr_rst_n: Resets the PMC module and resets all registers in the PM clock domain,

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including sticky bits. It is the power-on reset.

- phy_rst_n: output reset signal to reset the PCIe PHY. This reset asserted along with Cold Reset, Warm Reset, Hot Reset.

14.6.1.3.3 Hot Reset and Link-Down Reset

A downstream port (DSP) can hot reset an upstream port (USP) by sending two consecutive TS1 ordered sets with the hot reset bit asserted. Eventually, the DSP and USP assert link_req_rst_not to request external logic to reset them. Alternatively, during normal operation, the link might fail and go down. After this link-down event, the controller requests the reset module to hot-reset the controller. There is no difference in the handling of a link-down reset or a hot reset.

Hot Reset or Link-down reset cannot be activated before no transaction is appending on system bus. Application software must confirm that system bus is in IDLE state then let the reset operation go on.

To prevent your application from hanging when the controller is reset, the controller must cleanly terminate all transactions that are still in-progress. In AXI configurations with a segmented-buffer Rx queue architecture, the controller automatically executes this process before asserting link_req_rst_not. To disable automatic flushing, set the AUTO_FLUSH_EN field in LINK_FLUSH_CONTROL_OFF to '0'.

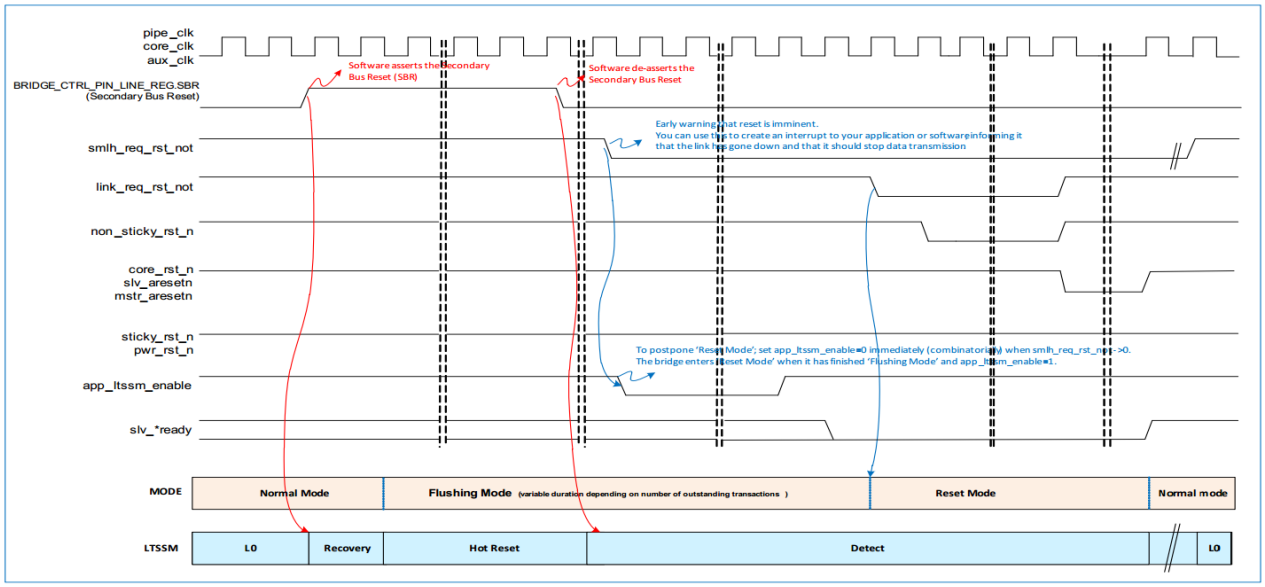


Fig. 14-3 Delaying the PCIe Hot Reset

Figure above illustrates the timing of handling Hot Reset. When Hot Reset or Link-down reset occurs, controller will assert smlh_req_rst_not as an early warning. This warning is an interrupt bit in Client Register group(link_req_rst_not_int). If you want to delay the reset of the controller so that it continues to accept and terminate slave requests, or to read out some register status through the DBI, you must set app_ltssm_enable =0 immediately (combinatorially) after smlh_req_rst_not ->0, as shown in above, this can be achieved by enable the app_dly1_en, app_ltssm_enable will be de-asserted immediately to disable the LTSSM. Then the Hot Reset process is holding on, software then should set the PCIe BIU in IDLE state. This delay will be end-up by asserting app_dly1_done.

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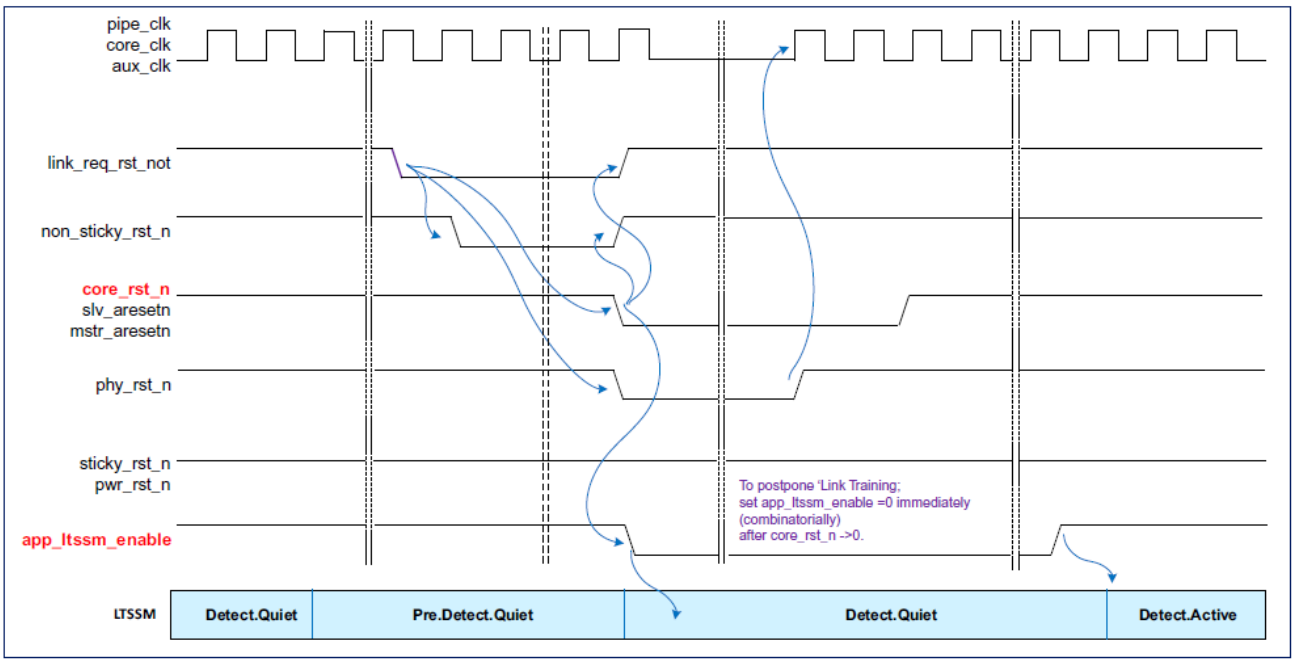


Fig. 14-4 Delaying the Link Training After Hot Reset

If you want to delay link re-establishment (after reset) so that you can reprogram some registers through DBI, you must set app_ltssm_enable =0 immediately after core_rst_n as shown in above. This can be achieved by enable the app_dly2_en, and end-up the delay by assert app_dly2_done.

To be compatible with old version client design, the app_ltssm_enable_enhance is a new way to control the glue behavior of the app_ltssm_enable. It's advised set app_ltssm_enable_enhance to "1" when the version >= 0x50600. The mechanisms of delaying the Hot reset are available only in app_ltssm_enable_enhance mode.

14.6.2 Initialization

14.6.2.1 Initialization Sequence for RC Mode

The initialization sequence for RC mode is as follows:

1. Configure the IO for CLKREQ# and WAKE# signals. Configure the optional signals button_rst_n and perst_n if they are used.
2. Configure the CRU registers to provide appropriate reference clock to PCIe PHY if internal reference used. Check all the CRU control registers, such as PLL/DIV/CKG(clock gating), to make sure the reference and other clock is working normally. Please refer to CRU Chapter for more information.
3. Configure Combo PIPE PHY General Register File, to set PHY working mode, control the unused PIPE signals and initialize the PHY, the source of the reference or output the differential reference clock.
4. Sometimes, it is also necessary to configure the PHY internal register to adjust some analog trim.
5. De-assert the power-up reset of PCIe Controller. Delay some time or wait PLL lock if the PLL lock flag is accessible.
6. Set the app_ltssm_enable_enhance to enable enhance control mode of app_ltssm_enable
7. Initialize the device_type as Root Complex. You can program Client and controller registers before Link training start if necessary. Link training can be initialed by setting ltssm_enable bit in register PCIE_CLIENT_GENERAL_CON to 1. Link training success will set phy_link_up_int to 1. And if data flow initialization success, dll_link_up_int interrupt status bit will be set to 1. These two bits can be polled in LTSSM_STATUS or GENERAL_DEBUG_INFO, besides, it can be informed by interrupt optionally. The controller tries to linkup at maximum Link width/speed, if you want to resize or change speed, please refer to internal application document about speed changing and lane resizing. It is strongly recommended that set direct_speed_change bit to 1 in

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PL_GEN2_CTRL_OFF before link training.
8. Software emulation and initialization.
9. Writes to Bus Master Enable (BME), Memory Space Enable (MSE), then application can start application traffic generation.

14.6.3 Address Translation

The controller uses the internal Address Translation Unit (iATU) to implement a local address translation scheme that replaces the TLP address and TLP header fields in the current TLP request header.

The iAUT has several inbound Address Translation regions and several outbound Address Translation regions. The minimum size of an Address Translation Region is 64k and the maximum size of an Address Translation Region is 4G.

14.6.3.1 Outbound Features

Address translation is used for mapping different address ranges to different memory spaces supported by your application. A typical example maps your application memory space to PCI memory space. The ATU also supports type translation. Without address translation, your application address is passed unmodified to the TLPs directly through the Tx application interface. You can program the iATU to implement your own outbound address translation scheme. The outbound features are as follows:

- Address Match mode operation for MEM and I/O, CFG, and MSG TLPs. No translation for completions.
- Supports type translation through TLP type header field replacement for MEM or I/O types to MSG/CFG types.
- Programmable TLP header field replacement. Including TYPE, TC, AT, ATTR, MSG-Code, TH, PH, ST.
- Multiple (up to 16) address regions programmable for location and size.
- Programmable enable/disable per region.
- Automatic FMT field translation between three DWORDs and four DWORDs for 64-bit addresses.
- Invert Address Matching mode to translate accesses outside of a successful address match.
- Configuration Shift mode. Optimizes the memory footprint of CFG accesses destined for the Rx application interface in a multifunction device.
- Response code which defines the completion status to return for accesses matching a region.
- Supports regions from 64 KB to 4 GB in size.
- Payload Inhibit marks all TLPs as having no payload data.
- Header Substitution replaces bytes 8 to 11 (for 3 DWORD header) or bytes 12 to 15 (for 4 DWORD header), inclusive, of the outbound TLP header.
- Tag Substitution of the outbound TLP tag field.
- Function number bypass mode to allow function number information to be supplied from your application transmit interface while translating the address and other attributes of the TLP.
- DMA bypass mode to allow TLPs which are initiated by the embedded DMA engine, to pass through the iATU untranslated.

14.6.3.2 Outbound Basic Operation

The address field of each request MEM and I/O TLP is checked to see if it falls into any of the enabled address regions defined by the Start and End addresses as defined in Figure below. When an address match is found, then the TLP address field is modified as follows:

Translated Address = Original Address - Base Address + Target Address

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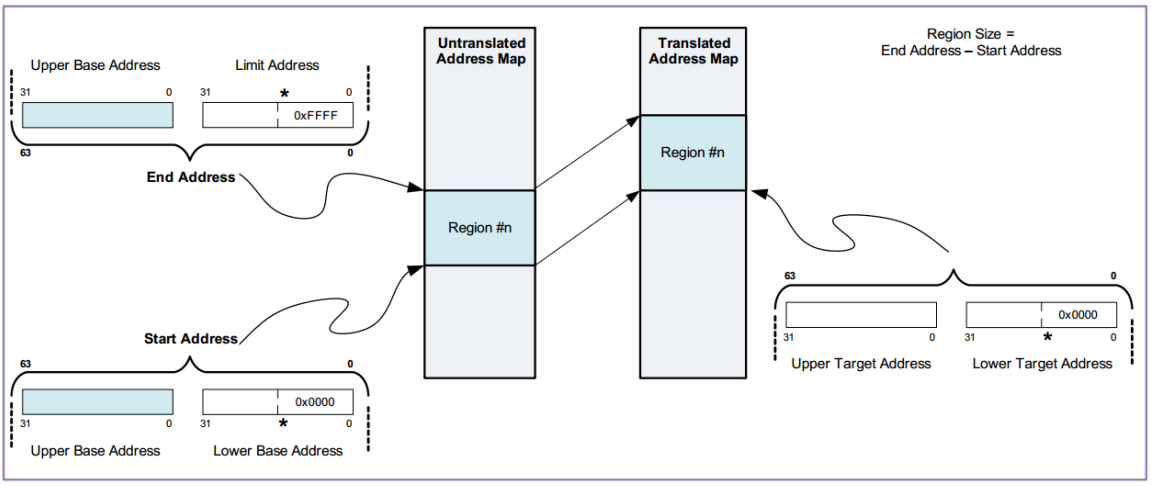


Fig. 14-5 PCIe Hot Reset Control Structure

The TYPE, TC, AT, TH, PH, ST, Function Number, and ATTR header fields are replaced with the corresponding fields in the IATU_REGION_CTRL_1_OFF_OUTBOUND_0 register. When your application address field matches more than one of the CX_ATU_NUM_OUTBOUND_REGIONS address regions, then the first (from lowest number 0) enabled region to be matched is used. For details on what happens when there is no address match, see "No Address Match Result". This operational mode (called Address Match Mode) is always used for outbound translation.

The minimum size of an address translation region is 64KB. So, the lower 16 bits of the Base, Limit, and Target registers are zero and all address regions are aligned on 64 KB boundaries.

14.6.3.3 Outbound Detailed Operation

14.6.3.3.1 RID BDF Number Replacement

When there is a successful address match on an outbound TLP, then the function number used in generating the function part of the requester ID field of the TLP is taken from the 3-bit Function Number field of the IATU_REGION_CTRL_1_OFF_OUTBOUND_iregister. The value in this field must be 0x0 unless multifunction operation in the controller is enabled. To override this behavior, use the "Function Number Translation Bypass Feature" described later.

14.6.3.3.2 iATU Outbound MSG Handling

The iATU supports TYPE translation/conversion of MEM and I/O TLPs to Msg/MsgD TLPs. This supports applications that are unable to directly generate Msg/MsgD TLPs. When there is a successful address match on an outbound MEM TLP, and the translated TLP type field is MSG (that is, the type field of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i register is 10xxx), then the message code field of the TLP is set to the value in the Message Code field of the IATU_REGION_CTRL_2_OFF_OUTBOUND_iregister.A Memory Write with an effective length of '0' is converted to Msg and all other MWr TLPs are converted to MsgD.

14.6.3.3.3 MEM-CFG Type Translation

The iATU supports translation of I/O and MEM TLPs to CFG TLPs. This is useful for applications that are unable to generate CFG TLPs. The 16-bit BDF is located at bits [31:16] of the translated address where:

Translated Address = Original Address - Base Address + Target Address

As an example:

Original Address[31:16] = {13h0,function_no[2:0]}
Base Address[31:16] = 16h0
Target Address[31:16] = {bus_no[7:0],device_no[4:0],3h0}

then:

Translated Address[31:16] = BDF ={bus_no[7:0], device_no[4:0], function_no[2:0]}

To handle eight functions (as the previous example indicates), you should use a 19-bit wide region size. For CFG transactions created directly by your application (asopposed to the iATU), you must ensure that the BDF field does not match any programmed iATU address region or else unintentional type translation could occur.

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14.6.3.3.4 CFG Shift Feature

This feature is enabled by setting the CFG_SHIFT_MODE field the IATU_REGION_CTRL_2_OFF_OUTBOUND_0 register. The iATU uses bits [27:12] of the original address to form bits [31:16] (BDF location) of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space.

14.6.3.3.5 FMT Translation

The iATU automatically sets the TLP format field for three DWORDs when it detects all zeros in the upper 32 bits of the translated address. Otherwise, it sets it to four DWORDs when it detects a 64-bit address (that is, when there is a '1' in the upper 32 bits of the translated address). When the original address and the translated address are of different format, the iATU ensures that the TLP header size matches the translated address format.

14.6.3.3.6 Invert Feature

In normal operation an address match on an outbound TLP occurs when the untranslated address is in the region bounded by the base address and limit address. When the invert feature is activated, an address match occurs when the untranslated address is not in the region bounded by the base address and limit address. This feature is activated by setting the Invert field of the IATU_REGION_CTRL_2_OFF_OUTBOUND_iregister.

14.6.3.3.7 DMA Bypass Feature

When you do not want the iATU to translate outbound requests that are generated by the DMA, you must implement one of the following approaches:

- Ensure that the combination of DMA channel address programming and iATU control register programming causes no translation of DMA traffic to be done in the iATU.
- Activate the DMA bypass mode to allow request TLPs which are initiated by the embedded DMA controller to pass through the iATU untranslated. You can activate the DMA bypass mode by setting the DMA Bypass field of the IATU_REGION_CTRL_2_OFF_OUTBOUND_i register to 1.

14.6.3.3.8 Function Number Translation Bypass Feature

In this mode the function number of the translated TLP is taken from your application transmit interface and not from the Function Number field of the REGION_CTRL_1_OFF_OUTBOUND_i register. You can activate the function number bypass mode by setting the Function Number Translation Bypass Enable field in the IATU_REGION_CTRL_2_OFF_OUTBOUND_i to '1'.

14.6.3.3.9 General Bypass

Application can program PCIE_CLIENT_AXI_SLV_ATU_BYPASS register to do general ATU bypassing. Note that you should make sure that there is no transfer pending before you program this register.

14.6.3.3.10 Header Substitution (Tx)

When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. The expected usage scenario is for Vendor Defined Msg/MsgD and ATS transactions over the AXI bridge which is normally inefficient requiring a very large iATU region. Enabled using the HEADER_SUBSTITUTE_EN field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i.

14.6.3.3.11 Tag Substitution (Tx)

When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Enabled using the TAG_SUBSTITUTE_EN field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i.

Your application must not attempt to perform TAG substitution for outgoing non-posted TLPs.

Note: If the iATU is programmed to allow a TLP to be matched to more than one iATU outbound regions, the Function Number Translation Bypass field of the

IATU_REGION_CTRL_2_OFF_OUTBOUND_i register should be same for every region where that TLP can be matched.

14.6.3.4 Outbound Programming Example

Define Outbound Region 1 as:
64 KB I/O region from 0x80000000_d000000to 0x80000000_d000ffff, to be mapped to 0x00010000in the PCIe I/O space.

1. Setup the Region Base and Limit Address Registers.
   Write 0xd0000000to Address {0x208} to set the Lower Base Address.
   Write 0x80000000to Address {0x20C} to set the Upper Base Address.
   Write 0xd000ffff to Address {0x210} to set the Limit Address.
2. Setup the Target Address Registers.
   Write 0x00010000to Address {0x214} to set the Lower Target Address.
   Write 0x00000000to Address {0x218} to set the Upper Target Address.
3. Configure the region through the Region Control 1 Register.
   Write 0x00000002to Address {0x200} to define the type of the region to be I/O.
4. Enable the region.
   Write 0x80000000to Address {0x204} to enable the region.

14.6.3.5 Inbound Features

Address translation is used for mapping different address ranges to different memory spaces supported by your application. A typical example maps your application memory space to PCI memory space. The iATU supports type translation. Without address translation, your application address is passed from the TLPs directly through the AXI application interface. You can program the iATU to implement your own inbound address translation scheme without external logic.

- Programmable Match mode operation for MEM, I/O, CFG, and MSG TLPs. No translation for completions.
- Selectable BAR Match mode operation for I/O and MEM TLPs:
  - TLPs destined for the internal CDM (or ELBI) in an upstream port are not translated.
  - TLPs that are not error-free (ECRC, malformed and so on) are not translated.
- Programmable TLP header field matching:
  - TYPE/TD/TC/AT/ATTR/MSG-Code/TH/PH/ST
  - Function Number
- Multiple address regions programmable for location and size.
- Programmable enable/disable per region.
- Automatic FMT field translation between three DWORDs and four DWORDs for 64-bit addresses.
- Invert Address Matching mode to translate accesses outside of a successful address match.
- ECAM Configuration Shift mode to allow a 256 MB CFG1 space to be located anywhere in the 64-bit address space.
- Supports regions from 64 KB to 4 GB in size.
- Single Address Location to allow all TLPs to be translated to a single address location.
- Msg Type Match Mode to allow matching of any TLP of type Message.

14.6.3.6 Inbound Basic Operation

14.6.3.6.1 Overview

The following translation rules and limitations apply:

- When there is no match, then the address is untranslated. In addition,
  - TLPs destined for the internal registers in an upstream port are not translated.
  - TLPs that are not error-free (ECRC, malformed and so on) are not translated.
- Address translation of all TLP types (MEM, I/O, CFG, and MSG) except completion is supported in Address Match mode. In BAR Match mode, only translation of I/O and MEM is supported.

The setting of the MATCH_MODE field in IATU_REGION_CTRL_2_OFF_INBOUND_0 determines how iATU inbound matching is done for each TLP type.

Table 14-7 Determination of Match Mode

TLP Type	MATCH_MODE =0	MATCH_MODE =1
MEM or I/O	Address Match Mode	BAR Match Mode
CFG0	Routing ID Match Mode	Accept Mode
MSG/MSGD	Address Match Mode	Vendor ID Match Mode

14.6.3.6.2 I/O and MEM Match Modes

Inbound address translation for I/O and MEM TLPs operates in one of two matching modes as determined by the "Inbound Match Mode" field in the IATU_REGION_CTRL_2_OFF_INBOUND_0 register.

Address Match Mode:

The operation is similar to "Outbound Basic Operation (Address Match Mode)". The address field of each request TLP is checked to see if it falls into any of the enabled address regions. When an address match is found then the TLP address field is modified as follows:

Address = Address - Base Address + Target Address

BAR Match Mode:

Looking for an address match is a two-step process.

1. The standard internal PCI Express BAR Matching Mechanism checks if the address field of any MEM and I/O request TLP falls into any address region defined by the enabled BAR addresses and masks.
2. When a matched BAR is found, then the iATU compares the BAR ID to the BAR Number field in the IATU_REGION_CTRL_2_OFF_INBOUND_0 register for all enabled regions. Figure below provides more details on inbound translation in BAR Match Mode.

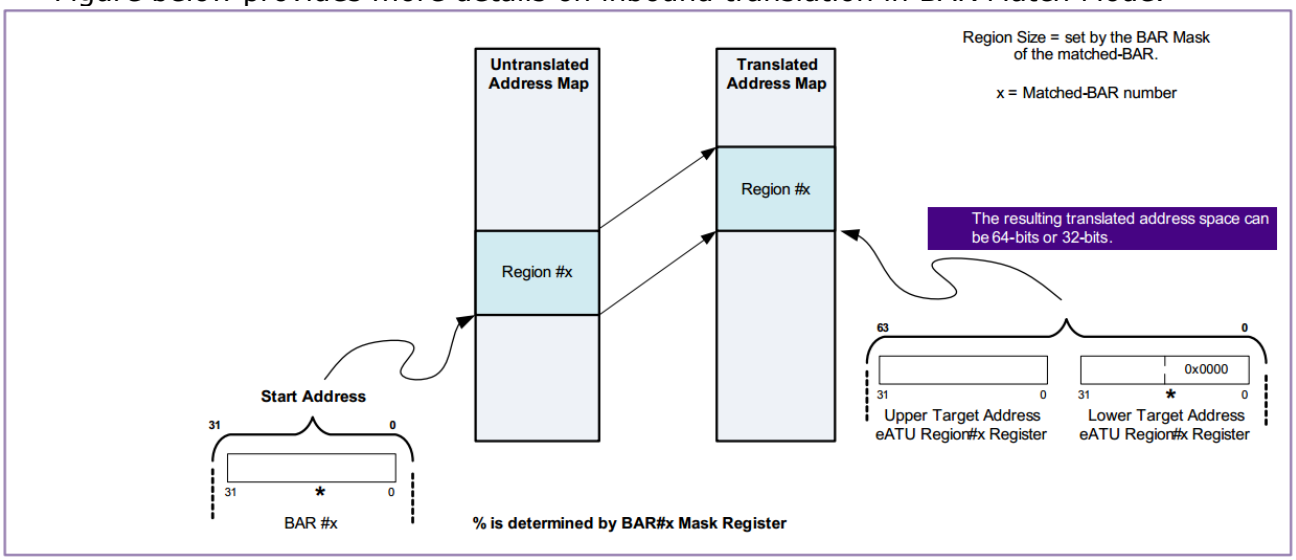


Fig. 14-6 Inbound BAR Match Mode

14.6.3.7 Inbound Detailed Operation

14.6.3.7.1 Single Address Location

When enabled and region address is matched, the TLPs can be translated to a single address location as determined by the target address register of the iATU region. This feature can be enabled using the SINGLE_ADDR_LOC_TRANS_EN field in IATU_REGION_CTRL_2_OFF_INBOUND_i. This feature is useful for translating messages on AXI bridge.

14.6.3.7.2 CFG Handling (Upstream Port)

The controller normally routes CFG TLPs (to the internal CDM or ELBI) without translation. The iATU only translates CFG0 TLPs that the controller has routed to the TRGT1. Inbound address translation for CFG0 TLPs operates in one of two matching modes as determined by the Inbound CFG0 Match Mode field in the IATU_REGION_CTRL_2_OFF_INBOUND_i register.

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Accept Mode

The controller always accepts CFG0 TLPs even when the CFG bus number does not match the current bus number of the device. This mode follows that behavior. The routing ID of received CFG0 TLPs are ignored when determining a match.

Routing ID Match Mode

The operation is similar to "Outbound Basic Operation (Address Match Mode)". The routing ID of the inbound CFG0 TLP must fall within the Base and Limit of the defined iATU region for matching to proceed. The iATU interprets the routing ID (Bytes1 8-11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM and I/O transactions.

CFG Shift Feature

Inbound CFG transactions routed to the Rx application interface can exist anywhere in address space, because the PCIe controller filter processes the routing ID (BDF) as bits [31:16] of an address. This BDF changes according on the PCIe bus topology. A compressor feature (CFG Shift Feature) can be enabled by setting the CFG Shift bit in the IATU_REGION_CTRL_2_OFF_INBOUND_i register. Bits [15:12] of the third DWORD1 of CFG TLPs are reserved. The compressor feature uses this fact to reduce the memory requirement. This shifts/maps the BDF (bits [31:16] of the third header DWORD, which would be matched against the Base and Limit addresses) of the incoming CfgRd0/CfgWr0 down to bits [27:12] of the translated address.

14.6.3.7.3 Optional Matching Fields

In address and BAR match modes, a successful address/BAR match can be optionally gated by successful matching of the following programmable TLP header fields (per region):

- TYPE/TD/TC/AT/ATTR/TH/PH/ST
- MSG Code (MSG TLPs only)
- Function number (MEM, I/O, or CFG TLPs only)
- Virtual function number (MEM or I/O TLPs only)

For each of the previous fields in the IATU_REGION_CTRL_1_OFF_INBOUND_i register, there is an associated Match Enable bit in the IATU_REGION_CTRL_2_OFF_INBOUND_i register. Address translation only proceeds when compares on all enabled field are successful.

14.6.3.7.4 Response Code Feature

When the Response Code field of the IATU_REGION_CTRL_REG_2_INBOUND_i register is set to a value other than 00, the controller uses it to determine the completion status field of completion TLPs sent in response to successfully match non-posted TLPs. This can be set to unsupported request (UR) or completer abort (CA). When the error response field is set to 2'b00, then the normal receive filter response for this TLP is used.

14.6.3.7.5 Inbound MSG Handling

Inbound message (Msg/MsgD) transactions can use one of two matching modes:

Address Match Mode

The third and fourth header DWORDs are treated as an address and are compared against the iATU Region Base and Limit Address registers. For vendor defined messages this allows specific messages to be filtered into memory at the target address. The Upper Base address should be set to BDF and Vendor ID. The Lower Base address can be used as a filter for specific messages.

Vendor ID Match Mode

This mode is relevant for ID-routed vendor defined messages. The iATU ignores the routing

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ID (BDF) in bits [31:16] of the third DWORD of the TLP header1 but compares it against the vendor ID in bits [15:0] of the third DWORD of the TLP header (bytes1 10 and 11). This allows vendor defined messages to be filtered against specific vendor IDs without needing to know the BDF number which might vary depending on the PCI topology. Bits [15:0] of the Region Upper Base register should be programmed with the required vendor ID as follows:
Region Upper Base [15:8] =byte 10
Region Upper Base [7:0] =byte 11
The lower base and limit register should be programmed to translate TLPs based on vendor-specific information in the fourth DWORD of the TLP header.

14.6.3.7.6 Msg Type Match Mode

Inbound message (Msg/MsgD) transactions can also use Msg Type Matching mode. When this mode is enabled and Single Address Location is enabled, the iATU matches Msg TLP Type field with TYPE field of IATU_REGION_CTRL_1_OFF_INBOUND_i register.

If Fuzzy Type Match Mode is also enabled, then any Msg received will be matched (that is, Msg Type's sub-field r[2:0], which specifies the Message routing mechanism, is ignored). The Message should be consumed by your application before the next message arrives as all messages go to the same address.

If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN is set for any region, then you must ensure that the same TLP cannot be matched in any other region where SINGLE_ADDRESS_LOCATION_TRANSLATE_EN is not set. If this happens radm_trgt1_hdr_uppr_bytes could have incorrect data.

14.6.3.7.7 Fuzzy Type Match Mode

When enabled, the iATU relaxes the matching of the TLP type field against the expected type field so that:

- CfgRd0 and CfgRd1 TLPs are seen as identical. Similar with CfgWr0 and CfgWr1.
- MWr, MRd and MRdLk TLPs are seen as identical.
- The routing field of MsgD TLPs is ignored.
- Atomic Ops TLPs-FetchAdd, Swap, and CAS are seen as identical.

For example, CFG0 in the type of field in the IATU_REGION_CTRL_1_OFF_INBOUND_i register matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. To enable this feature, set the Fuzzy Type Match Mode bit of the IATU_REGION_CTRL_OFF_2_INBOUND_i register.

14.6.3.7.8 FMT Translation

The iATU automatically sets the TLP format field for three DWORDs when it detects all zeroed in the upper 32 bits of the translated address. Otherwise, it sets it to four DWORDs when it detects a 64-bit address (when there is a 1 in the upper 32 bits of the translated address). When the original address and the translated address are of a different format then the iATU ensures that the TLP header size matches the translated address format.

14.6.3.7.9 Invert Feature

Normally an address match on an inbound TLP occurs when the untranslated address is in the region bounded by the Base address and Limit address. When the Invert feature is activated, an address match occurs when the untranslated address is not in the region bounded by the Base address and Limit address. This feature is activated by setting the Invert field of the IATU_REGION_CTRL_OFF_2_INBOUND_i register.

14.6.3.8 Inbound Programming Example

You must not update the iATU registers while operations are in progress on the AXI bridge slave interface.

Example 1:

Define Inbound Region 2 as: MEM region matching BAR4 (BAR match mode) mapping to 0x8000_0000_2000_0000 in your application memory space
1. Setup the Target Address Registers.
   Write 0x20000000 to Address {0x508} to set the Lower Target Address.

Write 0x80000000 to Address {0x50C} to set the Upper Target Address.
2. Configure the region through the Region Control 1 Register.
Write 0x00000000 to Address {0x500} to define the type of the region to be MEM.
3. Enable the region for BAR Match Mode.
Write 0xC0000400 to Address {0x504} to enable the region for BAR match mode for BAR#4.

Example 2:

MEM region matching TLPs with addresses in the range 0x00010000 to 0x0005ffff mapped to 0x2000_0000 - 0x2004_ffff in your application memory space.
1. Setup the Region Base and Limit Address Registers.
Write 0x00010000 to Address {0x108} to set the Lower Base Address.
Write 0x00000000 to Address {0x10C} to set the Upper Base Address.
Write 0x0005ffff to Address {0x110} to set the Limit Address.
2. Setup the Target Address Registers.
Write 0x20000000 to Address {0x114} to set the Lower Target Address.
Write 0x10000000 to Address {0x118} to set the Upper Target Address.
3. Configure the region through the Region Control 1 Register.
Write 0x00000000 to Address {0x100} to define the type of the region to be MEM.
4. Enable the region.
Write 0x80000000 to Address {0x104} to enable the region in address match mode.

14.6.4 PCIe Message Handling

This section describes the processing of messages through the controller. For a proper understanding of messages, you should be familiar with Section 2.2.8, "Message Request Rules" of the PCI Express Base Specification, Revision 3.0.

14.6.4.1 Message Generation

These are three methods to generate PCIe Messages:

- Specific MSG interface
  You can use PCIE_CLIENT_MSG_GEN_CON register to generate messages such as:
  - Vendor-Defined Message
  - Legacy PCI Interrupt Message
  - PME_Turn_Off message
  - Unlock message
  - LTR Message
  - OBFF Message

  Refer to register description for more details.
- AXI bridge
  In this method, you should program the PCIE_CLIENT_AXI_SLV_AWMISC_HDR PCIE_CLIENT_AXI_SLV_AWMISC_HDR3 and PCIE_CLIENT_AXI_SLV_AWMISC_HDR4 registers to set these parameters:
  slv_awmisc_info [4:0] =MSG
  slv_awmisc_info [20:13] = message code
  slv_awmisc_tag [5:0] = tag
  slv_awmisc_info_hdr_[3|4]dw = 3rd and 4th TLP header DWORD
  Then you can send zero length memory write (slv_awstrb=0) to generate the message. You must not program registers mentioned above when there are normal transfers pending on AXI slave interface. And should set these registers in normal value when you want to send MWr TLP. This method is not recommended because of these limitations.
- AXI bridge and iATU
  Program related client register fields as follows:
  slv_awmisc_info[4:0] =MEM
  slv_awmisc_info_hdr_[3|4]dw = 3rd and 4th TLP header DWORD
  Then iATU needs to be configured to to translate MWr to Msg TLPs. Refer to "Address Translation" for more details. This method is not recommended because that it needs

additional iATU resources.

14.6.4.2 Message Reception

PCIe controller use pcie_msg_int interrupt to indicate the reception of PCIe Message. Application can poll to PCIE_CLIENT_INTR_STATUS_MSG_RX register to check the status of Message reception. Refer to register information for details.

14.6.5 PCIe Power Management

14.6.5.1 Overview

The controller supports two categories of PM operations to control the device state (D-state) and link state. For a proper understanding of PCIe Power management you should be familiar with Section 5, "Power Management" of the PCI Express Base Specification, Revision 3.0.

Software PCI Compatible PM (PCI-PM)

- D-state PM of Function. The host software can direct the function to enter any of the D1, D2, or D3 low-power states. It does this by writing to the Power Management Control and Status Register (PMCSR) in the PCI-PM capability structure.
- D-state PM of Link. Link states are not visible to PCI-PM legacy compatible software and are derived from the power management D-states of the components connected to that link. The action of changing the D-state in the PMCSR indirectly causes a change in the link power state. The L1 state is entered whenever all functions of a USP on a link are programmed to a non-D0 state. The entry into L2 and L3 states is initiated by the DSP.

PCIe PM Mechanisms

- Active State PM (ASPM).When the USP is in L0 and detects idleness on the link for a specific amount of time, it automatically transitions the link to the L0s or L1 (optional) power state.
- L1 Substates. This is an optional PCIe feature that enables components on a link to further reduce idle power consumption while the link is in L1, including almost complete removal of power for the high speed PHY circuits.

14.6.5.2 L0s Operation

L0s is a low-power state enabled by ASPM. ASPM controls entry into L0s for the transmitter. The remote device controls entry into L0s for the receiver.

14.6.5.2.1 L0s Entry

All of these conditions must be met:

- ASPM L0s is enabled through the ASPM Control field in the Link Control register.
- L0s entry conditions as defined in Section 5.4.1.1.1, "Entry into the L0s State" of the PCI Express Base Specification, Revision 3.0, exist for a duration of time (determined by the L0S_ENTRANCE_LATENCY field in ACK_F_ASPM_CTRL_OFF).
- No higher stage of power-down requested.

14.6.5.2.2 L0s Exit

Any of these conditions can be met:

- A DLLP or TLP is pending to be sent.
- L1 entry conditions as defined in Section 5.4.1.2.1, "Entry into the L1 State" of the PCI Express Base Specification, Revision 3.0, are satisfied.
- PCIe link partner requests to enter into link recovery.

14.6.5.3 L1 Operation (Non-substates)

The following topic will be discussed in this section: L1 (ASPM/PM) Entry and Exit Conditions and L1 Clock PM (L1 with REFCLK removal/PLL Off) Entry and Exit Conditions.

14.6.5.3.1 L1 (ASPM/PM) Entry

L1 is a low-power state enabled either by ASPM (L1-ASPM) or by the software changing the D-state (L1-PM). The L1 state is a bi-directional link low-power state and both link partners must negotiate to go to this state.

The L1-ASPM entry negotiation handshake uses PM_Active_State_Request_L1 DLLPs, PM_Request_Ack DLLPs, and PM_Active_State_Nak MSG TLPs. Refer to PCIe Basic Specification for more information.

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There are three scenarios that cause the controller to enter L1 under ASPM conditions.

Scenario 1: L1 Idle Timeout In L0s

All of these conditions must be met in the USP:

- ASPM L1 and L0s are enabled through the ASPM Control field in the Link Control register.
- The ENTER_ASPMfield of ACK_F_ASPM_CTRL_OFFis set to '0' and the link state is L0s for both link partners, or the ENTER_ASPMfield of ACK_F_ASPM_CTRL_OFFis set to '1'.
- L1 entry conditions as defined in Section 5.4.1.2.1, 'Entry into the L1 State' of the PCI Express Base Specification, Revision 3.0, exist for a duration of time (determined by the L1_ENTRANCE_LATENCYfield in ACK_F_ASPM_CTRL_OFF).
- No higher stage of power-down requested.
- Your USP application is not asserting the app_xfer_pending field in PCIE_CLIENT_POWER_CON register.
- There are no in-progress transactions in the controller.
- There are no pending requests at the AXI slave interface, that is, slv_a*valid must be 0.
- There are no pending DMA transfers.

Scenario 2: L1 Idle Timeout In L0

All of these conditions must be met in the USP:

- ASPM L1 is enabled and L0s is not enabled through the ASPM Control field in the Link Control register.
- Link state is L0.
- L1 entry conditions as defined in Section 5.4.1.2.1, "Entry into the L1 State" of the PCI Express Base Specification, Revision 3.0, exist for a duration of time (determined by the L1_ENTRANCE_LATENCYfield in ACK_F_ASPM_CTRL_OFF).
- No higher stage of power down-requested.
- Your USP application is not asserting the app_xfer_pending field in PCIE_CLIENT_POWER_CON register.
- There are no in-progress transactions in the controller.
- There are no pending requests at the AXI slave interface, that is, slv_a*valid must be 0.
- There are no pending DMA transfers.

Scenario 3: Application Controlled (USP only)

All of these conditions must be met in the USP:

- ASPM L1 is enabled through the ASPM Control field in the Link Control register.
- Your application writes 1 to the app_req_entr_l1 field in PCIE_CLIENT_POWER_CON register.
- Your USP application is not asserting the app_xfer_pending field in PCIE_CLIENT_POWER_CON register.
- There are no in-progress transactions in the controller.
- There are no pending requests at the AXI slave interface, that is, slv_a*validmust be 0.
- There are no pending DMA transfers.

L1-PM Entry

The power management state of a link is determined bythe D-state of theUSP.When you change the device state of the USP to D1, D2, or D3hot by writing to the PMCSR, the controller must initiate a link state transition to L1.

An USP application asserting the app_xfer_pending field does not prevent L1-PM entry, but will cause immediate exit from L1-PM.

14.6.5.3.2 L1-PM/L1-ASPM Exit

Any of these conditions are met:

- A DLLP or TLP is pending to be sent.
- Your application asserts the app_req_exit_l1 field.
- Link partner is requesting exit from L1.
- Your application asserts the app_xfer_pending field.
- Your application asserts the app_pm_xmt_pme field.

When the USP is programmed with capability to support PME; it sends a PME message to

the RC which calls the PM software to transition the USP to the D0 state. Therefore, you should only use app_pm_xmt_pme for L1-PM exit.

- PM software (RC) requests a higher stage of power-down by writing to the PMCSR in the USP.
- Your application (USP) requests transmission of VDM, MSI/MSIX, or LTR message. Legacy interrupt is not included.
- Your application (DSP) requests transmission of Unlock message.
- Your application is requesting to send traffic by asserting or slv_a*valid.
- Your application doorbells a DMA read or write channel, or DMA controller is requesting data.
- Your application (DSP) initiates link disable, or link retrain (by setting PCIE_CAP_LINK_DISABLE or PCIE_CAP_RETRAIN_LINK field in LINK_CONTROL_LINK_STATUS_REG to 1).
- Your application (DSP) initiates hot reset by either:
  - setting RESET_ASSERT field in PORT_LINK_CTRL_OFF to 1, or
  - setting SBR field in BRIDGE_CTRL_INT_PIN_INT_LINE_REG to 1, or
  - toggling app_init_rst field in PCIE_CLIENT_GENERAL_CON.
- Your application requests a speed change (by setting DIRECT_SPEED_CHANGE field in GEN2_CTRL_OFF to 1).
- Your application requests link width change (by setting DIRECT_LINK_WIDTH_CHANGE field in MULTI_LANE_CONTROL_OFF is set to 1).

14.6.5.3.3 L1 Clock PM

For an USP, host software uses the Enable Clock Power Management bit in the Link Control register to enable this feature. For a DSP, this register bit is hard coded to '0' and cannot be used to control this behavior. Your application can use the app_clk_pm_en input to dynamically control whether to execute L1 with or without Clock PM.

- The Support Clock Power Management bit in the Link Capabilities register must be set. For downstream ports it is hardcoded to 0, for upstream ports it can be accessed through the DBI.
- The Enable Clock Power Management bit in the Link Control register must be set.
- You must set the app_clk_pm_en field to 1. The controller only samples app_clk_pm_en when L1 is entered.

L1 with Clock PM and L1 substates work orthogonal to each other. L1 with Clock PM uses the mac_phy_pclkreq_n[0]signaling, and L1 substates uses the mac_phy_pclkreq_n[1]signaling. However, L1 substates takes precedence over Clock PM within the cores PM state machine.

14.6.5.4 L1 Substate

The L1 substates are applicable in both the ASPM and PCI-PM L1 link states. L1 substates management utilizes a per-link sideband signal called CLKREQ#.

- During L1 substates it is assumed that core_clk is turned off and that aux_clk is active. It is required that your application switches aux_clk to a low frequency free running clock on entry into L1.
- The controller uses aux_clk for counting time during L1 substates. You must program the frequency of this clock into the L1_SUBSTATES_OFF register with a value in the range 1...1000MHz to count real time. Frequencies lower than 1 MHz are possible, but with a loss of accuracy in the time counted.
- When the electrical idle detection circuitry is disabled, it is assumed that the PHY holds the signal phy_mac_rxelecidle to 1.

After the link has entered L1 through the normal L1 negotiation, the USP can initiate the sequence for entering the target L1 substate (L1.1 or L1.2) by tri-stating its CLKREQ# output buffer. The entry sequence can only proceed if the DSP is also tri-stating its CLKREQ# output buffer, resulting in the bidirectional CLKREQ# signal being pulled up to 1. Otherwise CLKREQ# will remain asserted at 0 and the link state will stay in L1. The exit sequence can be initiated by either port by asserting CLKREQ# to 0. For each port there are two cases to consider, the first where the exit is initiated locally, the second where the exit is initiated remotely. L1 substates management utilizes a per-link sideband signal called CLKREQ#.

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14.6.5.4.1 L1 Substates Software Control

When the controller enters L1, the target L1 substate depends on several programming bits:

- PM Control/Status Register
  - USP: The current D-state
  - DSP: The DLLP type that was used by USP to request L1
- L1 Substates Control 1 Register
  - ASPM PM L1.1 Enabled
  - ASPM PM L1.2 Enabled
  - PCI PM L1.1 Enabled
  - PCI PM L1.2 Enabled

After the USP controller enters L1, it uses the D-state of the device to determine if L1 was entered in ASPM mode or PCI-PM mode.

After the DSP controller enters L1, it uses the USPs DLLPL1 request type to determine if L1 was entered in ASPM mode or PCI-PM mode. The next tables shows the target L1 substate as a function of the relevant programming bits.

Table 14-8 Target L1 Substate as a Function of Software Controls (USP)

D-State	ASPM L1.1 Enabled	ASPM L1.2 Enabled	LTR >= Threshold	PCI PM L1.1 Enabled	PCI PM L1.2 Enabled	Target L1 Substate
!D0	-	-	-	0	0	L1
!D0	-	-	-	1	0	L1.1
!D0	-	-	-	-	1	L1.2
D0	0	0	-	-	-	L1
D0	1	0	-	-	-	L1.1
D0	0	1	0	-	-	L1
D0	1	1	0	-	-	L1.1
D0	-	1	1	-	-	L1.2

Table 14-9 Target L1 Substate as a Function of Software Controls (DSP)

DLLP Receive	ASPM L1.1 Enabled	ASPM L1.2 Enabled	LTR >= Threshold	PCI PM L1.1 Enabled	PCI PM L1.2 Enabled	Target L1 Substate
PM_Enter_L1	-	-	-	0	0	L1
	-	-	-	1	0	L1.1
	-	-	-	-	1	L1.2
PM_Active_State_Request_L1	0	0	-	-	-	L1
	1	0	-	-	-	L1.1
	0	1	0	-	-	L1
	1	1	0	-	-	L1.1
	-	1	1	-	-	L1.2

The Reported LTR is the maximum of the snoop/no snoop latency values embedded in LTR messages transmitted by the upstream ports or received by the downstream port. The controller stores these values in the port logic LTR Latency Register (LTR_LATENCY_OFF). When the requirement bit in the message is 0, the latency value is considered infinite (that is, the check with the threshold always pass).

14.6.5.4.2 L1 Substates Entry and Exit

PCIe link entered L1 substate automatically if related enable bit is set and LTSSM already in L1 state, refer to section L1 Substates Software Control for details.

L1 substates Exit can be triggered locally or Remotely. For locally initiated exit, refer to section L1-PM/L1-ASPM Exit. Remotely initiated exit begins when CLKREQ# is asserted by

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remote PCIe partner.

14.6.5.5 L2 and L3 Power Down Entry and Exit

L2/L3 entry is initiated after the RC calls power management software to initiate the removal of power and clocks. USPs of devices in D0, D1, D2, and D3hot must respond to the receipt of a PME_Turn_Off MSG TLP by transmitting a PME_TO_Ack MSG TLP. The device must then request a link transition to L2/L3_Ready. L2/L3_Ready is a bi-directional link power down state. If your application is not ready to be shut down, it must keep the app_ready_entr_l23 field de-asserted.

L2/L3 Entry

All of these conditions must be met:

- PME_Turn_Off/PME_TO_Ack handshake has been completed.
- Your USP application is ready to be turned off; app_ready_entr_l23=1.
- After sending the PME_TO_Ack, the USP initiates the L2/L3 Ready transition protocol by sending the PM_Enter_L23 DLLP. The RC responds with the PM_Request_Ack.

L2/L3 Exit

Any of these conditions can be met:

- When the USP is programmed with capability to support PME, your application can assert the apps_pm_xmt_pme field to request the controller to wake up. The USP then sends a PM_PME MSG TLP to the RC which calls the PM software to transition the USP out of the D3 state.
- Device is programmed with capability to support PME and your application requests the controller to wake up by triggering a native hot-plug event.
- Link partner is requesting exit from L2/L3.

14.6.5.6 Dynamic Power Allocation (DPA)

The DPA capability enables software to actively manage and optimize function power usage when in the D0 state. DPA is not applicable to power states D1-D3.

For details on how your application interacts with the controller, see the description of the dpa_sub_upd_int field in PCIE_CLIENT_INTR_STATUS_MISC register.

14.6.6 PCIe Interrupt

The PCIe provides several types of interrupts to system interrupt controller. They can be divided into MSI/MSI-X, PCIe Error interrupt, PCIe Message Receive interrupt, PCIe Legacy interrupt, PCIe System interrupt and PCIe Power Management Interrupt etc. When operating as RC, the PCIe is capable of handling both MSI/MSI-X and legacy interrupts. This is because when operating as RC it should be able to service both PCIe end points as well as legacy endpoints. It is capable of generating MSI or Legacy interrupt if the PCIe is configured as EP. Notes that PCIe EP component can't generate both Legacy and MSI/MSI-X interrupt. It is either one or the other. The interrupt type an EP generates is configured during configuration time.

Interrupt status and mask bits are located in client register group, some interrupts are handled by client register directly, but some interrupts are generated by events deep into controller and software should clear the root cause to serve the interrupt events. For more information, refer to the register description.

The pcie_edma_wr/rd_int is more efficient than service by pcie_sys_int, it is available depends on Chip ID.

Table 14-10 PCIe Interrupt Table

System Interrupt Event ID	Interrupt description (level 1)	Interrupt subset (level 2)	Support mode
pcie_sys_int	PCIe System Interrupt	phy_link_up_int	RC & EP
		dll_link_up_int	RC & EP
		link_req_rst_not_int	RC & EP
		hp_pme_int	RC
		hp_int	RC

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System Interrupt Event ID	Interrupt description (level 1)	Interrupt subset (level 2)	Support mode
		hp_msi	RC
		link_auto_bw_int	RC
		link_auto_bw_msi	RC
		bw_mgt_int	RC
		bw_mgt_msi	RC
		edma_wr_int	RC & EP
		edma_rd_int	RC & EP
		dpa_sub_upd_int	EP
		rbar_updata_int	EP
		link_eq_req_int	RC & EP
		ep_elbi_app_int	EP
pcie_legacy_int	PCIe Legacy interrupt	rx_inta_int	RC
		rx_intb_int	RC
		rx_intc_int	RC
		rx_intd_int	RC
		tx_inta_int	EP
		tx_intb_int	EP
		tx_intc_int	EP
		tx_intd_int	EP
pcie_msg_rx_int	PCIe message received interrupt	ven_msg_int	RC & EP
		unlock_msg_int	EP
		ltr_msg_int	RC
		cfg_pme_int	RC
		cfg_pme_msi_int	RC
		pm_pme_int	RC
		pm_to_ack_int	RC
		pm_turnoff_int	EP
		obff_idle_int	EP
		obff_obff_int	EP
		obff_cpu_active_int	EP
pcie_err_int	PCIe Error interrupt	aer_rc_err_int	RC
		aer_rc_err_msi	RC
		rx_cpl_timeout_int	RC & EP
		tx_cpl_timeout_int	RC & EP
		cor_err_sent_int	EP
		nf_err_sent_int	EP
		f_err_sent_int	EP
		cor_err_rx_int	RC
		nf_err_rx_int	RC
		f_err_rx_int	RC
		radm_qoverflow_int	RC & EP
pcie_pmc_int	PCIe Power Management interrupt	linkst_in_l1sub_int	RC & EP
		linkst_in_l1_int	RC & EP
		linkst_in_l2_int	RC & EP
		linkst_in_l0s_int	RC & EP
		linkst_out_l1sub_int	RC & EP
		linkst_out_l1_int	RC & EP
		linkst_out_l2_int	RC & EP
		linkst_out_l0s_int	RC & EP
		pm_dstate_update_int	EP

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System Interrupt Event ID	Interrupt description (level 1)	Interrupt subset (level 2)	Support mode
pcie_msi_ctrl_int	MSI/MSI-X	message signaled interrupt	RC
pcie_msi_ctrl_int_vec[7:0]	MSI/MSI-X	message signaled interrupt	RC

14.7 Appendix

14.7.1 LTSSM Code

S_DETECT_QUIET	6'h00
S_DETECT_ACT	6'h01
S_POLL_ACTIVE	6'h02
S_POLL_COMPLIANCE	6'h03
S_POLL_CONFIG	6'h04
S_PRE_DETECT_QUIET	6'h05
S_DETECT_WAIT	6'h06
S_CFG_LINKWD_START	6'h07
S_CFG_LINKWD_ACEPT	6'h08
S_CFG_LANENUM_WAIT	6'h09
S_CFG_LANENUM_ACEPT	6'h0A
S_CFG_COMPLETE	6'h0B
S_CFG_IDLE	6'h0C
S_RCVRY_LOCK	6'h0D
S_RCVRY_SPEED	6'h0E
S_RCVRY_RCVRCFG	6'h0F
S_RCVRY_IDLE	6'h10
S_RCVRY_EQ0	6'h20
S_RCVRY_EQ1	6'h21
S_RCVRY_EQ2	6'h22
S_RCVRY_EQ3	6'h23
S_L0	6'h11
S_L0S	6'h12
S_L123_SEND_EIDLE	6'h13
S_L1_IDLE	6'h14
S_L2_IDLE	6'h15
S_L2_WAKE	6'h16
S_DISABLED_ENTRY	6'h17
S_DISABLED_IDLE	6'h18
S_DISABLED	6'h19
S_LPBK_ENTRY	6'h1A
S_LPBK_ACTIVE	6'h1B
S_LPBK_EXIT	6'h1C
S_LPBK_EXIT_TIMEOUT	6'h1D
S_HOT_RESET_ENTRY	6'h1E
S_HOT_RESET	6'h1F

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Chapter 15 USBDP COMBO PHY

15.1 Overview

This chapter describes an overview of USBDP Combo PHY (Simple writing USBDP PHY). USBDP PHY is a PMA hardmacro to support USB and DP interface. USB's PCS and DP Link must be used along with USBDP PHY for successful operation.
The supported features in USBDP PHY are:

- USB Specification 3.0 and DP Specification 1.4 compliant
- 5Gb/s Serializer/Deserializer for USB
- 1.62 Gb/s, 2.7 Gb/s, 5.4 Gb/s and 8.1 Gb/s Serializer for DP
- USB Type-C and DP Alt Mode supported

15.2 Block Diagram

The following figure illustrates a block diagram of USBDP PHY. USBDP PHY comprises one Common, two lanes of transceiver, two lanes of transmitter, one AUX channel for DP, and PMA digital.

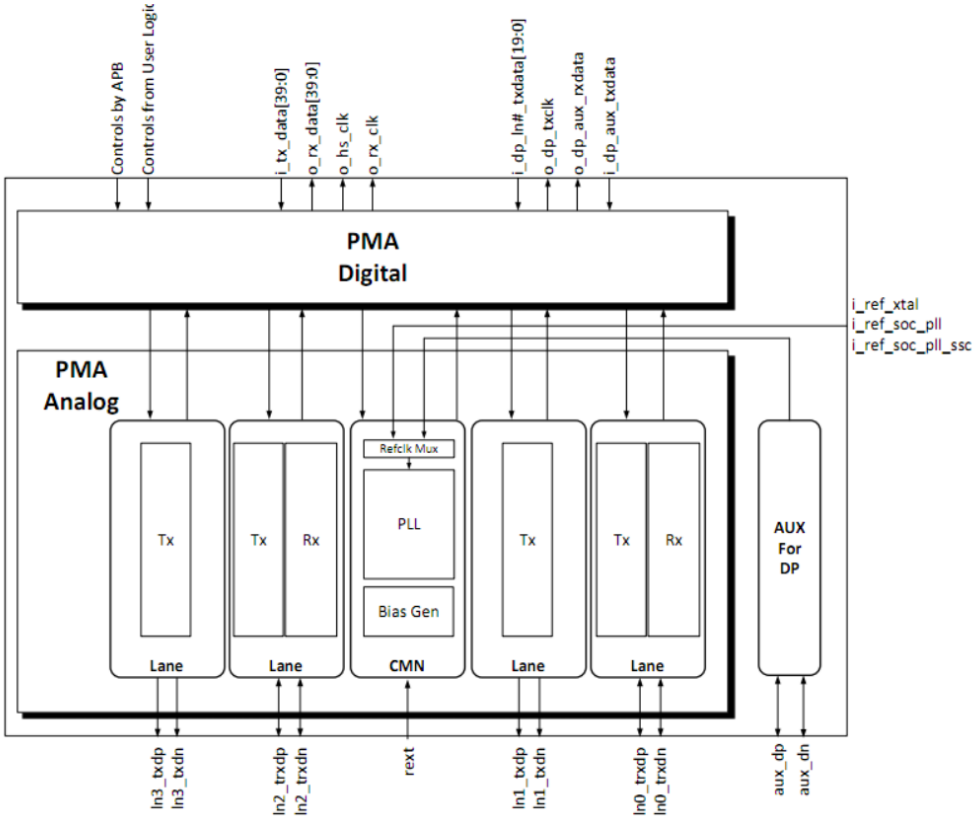


Fig. 15-1 USBDP PHY Block Diagram

The following sections describe the various blocks and their functionalities. DPTX uses a 32 bit internal data path for the main link.

15.3 Function Description

USBDP PHY is used for Universal Serial Bus (USB) and DisplayPort (DP) applications. The transceiver in the core performs these functions:

- Serializes the 8b/10b encoded data for transmission for USB Gen1 and DP RBR/HBR/HBR2/HBR3 operations
- De-serializes the received code groups Input data coming is registered once before it goes through a 3-stage pipeline. The 3-stage pipeline is required to capture the three colors components in various input video formats.

When transmitting the data, the transceiver performs these functions:

- Accepts four 10-bit 8b/10b encoded transmit characters for USB Gen1
- Attaches and serializes the data to the TXP/TXN differential outputs to a maximum value of 5.0 Gb/s for USB. Accepts two 10-bit 8b/10b encoded transmit characters for

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DP
- Attaches and serializes the data to the TXP/TXN differential outputs to a maximum value of 8.1 Gb/s for DP

When receiving the data, the transceiver performs these functions:
- Samples the received serial data on the RXP/RXN differential inputs
- De-serializes it into four 10-bit (or 8-bit) received characters

15.3.1 PMA Analog

USBDP PHY comprises of a PMA analog and PMA digital. The PMA consists of:
- One CMN block
- One AUX block for DP
- Two lanes including TX (lane1/3)
- Two lanes including TX and RX (lane0/2)
- One SSC ROPLL for DP
- One SSC LCPLL for USB

To support display alter mode, lane0 and lane2 work as TX in DP mode and as RX in USB mode. TX and RX are sharing bump in lane0 and lane2.

In the DP transmitter side, the PMA analog executes these actions:
- PMA Analog receives parallel data from PMA digital
- The data is serialized and transmitted through ln0/2_trxdp/n and ln1/3_txdp/n pads by hybrid-mode driver
- The TX driver characteristics, such as amplitude and 2-tap FIR filter, are user-controllable

In the USB transmitter side, the PMA analog executes these actions:
- PMA Analog receives parallel data from PMA digital
- The data is serialized and transmitted through ln1/3_txdp/n pads by hybrid-mode driver
- The TX driver characteristics, such as amplitude and 3-tap FIR filter, are either pre-settable or user-controllable

In the USB receiver side, the PMA analog executes these actions:
- The data is received through ln0/2_trxdp/n pads with 50Ω termination resistance
- Distortion on received signal due to channel loss is compensated by Continuous Time Linear Equalizer (CTLE) and Decision Feedback Equalizer (DFE)
- Clock and Data Recovery (CDR) generates frequency- and phase-aligned clock and equalized signal is deserialized to parallel data which is delivered to the PMA digital

15.3.2 CMN

The CMN consists of a band-gap reference (BGR), bias generator and PLL.

The BGR circuit generates high-accuracy reference voltage of 820mV across PVT variation.

A bias generator makes two kinds of current, external- and internal-resistor (RMRES)-referred current, and these currents are distributed to each block in CMN and lanes. The external resistor-referred (REXT) current is generated using an 8.2KΩ resistor which is connected between the rext pad and ground outside the chip. On the other hand, the internal resistor-referred current is generated using internally integrated replica resistor to compensate resistance error across PVT variation.

The PLL in the CMN synthesizes high-speed clock, which is used for TX serializer and RX CDR lock, from a reference clock.

The following are the main features of the PLL:
- Wide-range LC VCO from 8GHz to 10GHz
- Wide-range RO VCO from 4GHz to 8.1GHz
- Pre-defined or programmable divider setting for each USBDP Type-C specification
- Spread spectrum clocking (SSC) with sigma-delta modulated fractional divider
- Automatic Frequency Calibrated (AFC) oscillator setting for the desired frequency of operation
- Programmable charge pump current and loop filter resistance allowing for wide range of programmable loop bandwidth and peaking

15.3.3 AUX

The AUX is 1Mbps half-duplex bidirectional channel used for link management and device control. The AUX block does not support upstream detection feature.

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15.4 Register Description

15.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
USBDPPHY_CMM_REG0024	0x0090	W	0x0000003C	USBDPPHY CMN configure register
USBDPPHY_CMM_REG0025	0x0094	W	0x00000060	USBDPPHY CMN configure register
USBDPPHY_CMN_REG004A	0x0128	W	0x0000003C	USBDPPHY CMN configure register
USBDPPHY_CMN_REG004B	0x012C	W	0x000000F4	USBDPPHY CMN configure register
USBDPPHY_CMN_REG004C	0x0130	W	0x0000000F	USBDPPHY CMN configure register
USBDPPHY_CMN_REG004D	0x0134	W	0x000000F4	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0057	0x015C	W	0x0000004E	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0058	0x0160	W	0x00000034	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0059	0x0164	W	0x00000034	USBDPPHY CMN configure register
USBDPPHY_CMN_REG005A	0x0168	W	0x0000004E	USBDPPHY CMN configure register
USBDPPHY_CMN_REG005D	0x0174	W	0x0000004E	USBDPPHY CMN configure register
USBDPPHY_CMN_REG005E	0x0178	W	0x00000034	USBDPPHY CMN configure register
USBDPPHY_CMN_REG005F	0x017C	W	0x00000034	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0060	0x0180	W	0x0000004E	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0063	0x018C	W	0x00000041	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0064	0x0190	W	0x00000000	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0065	0x0194	W	0x00000005	USBDPPHY CMN configure register
USBDPPHY_CMN_REG006B	0x01AC	W	0x0000002C	USBDPPHY CMN configure register
USBDPPHY_CMN_REG006C	0x01B0	W	0x0000002C	USBDPPHY CMN configure register
USBDPPHY_CMN_REG006D	0x01B4	W	0x0000002C	USBDPPHY CMN configure register
USBDPPHY_CMN_REG006E	0x01B8	W	0x0000002C	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0072	0x01C8	W	0x00000008	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0073	0x01CC	W	0x00000008	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0074	0x01D0	W	0x00000008	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0075	0x01D4	W	0x00000008	USBDPPHY CMN configure register

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Name	Offset	Size	Reset Value	Description
USBDPPHY_CMN_REG0076	0x01D8	W	0x00000000	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0077	0x01DC	W	0x00000005	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0078	0x01E0	W	0x0000002D	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0079	0x01E4	W	0x0000000A	USBDPPHY CMN configure register
USBDPPHY_CMN_REG007C	0x01F0	W	0x00000007	USBDPPHY CMN configure register
USBDPPHY_CMN_REG007D	0x01F4	W	0x00000007	USBDPPHY CMN configure register
USBDPPHY_CMN_REG007E	0x01F8	W	0x00000007	USBDPPHY CMN configure register
USBDPPHY_CMN_REG007F	0x01FC	W	0x00000007	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0082	0x0208	W	0x00000016	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0083	0x020C	W	0x00000016	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0084	0x0210	W	0x00000016	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0085	0x0214	W	0x00000016	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0089	0x0224	W	0x00000010	USBDPPHY CMN configure register
USBDPPHY_CMN_REG00FC	0x03F0	W	0x00000019	USBDPPHY CMN configure register
USBDPPHY_CMN_REG00FD	0x03F4	W	0x00000019	USBDPPHY CMN configure register
USBDPPHY_CMN_REG00FE	0x03F8	W	0x00000019	USBDPPHY CMN configure register
USBDPPHY_CMN_REG00FF	0x03FC	W	0x00000019	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0101	0x0404	W	0x0000000F	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0102	0x0408	W	0x0000000F	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0103	0x040C	W	0x0000000F	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0104	0x0410	W	0x0000003C	USBDPPHY CMN configure register
USBDPPHY_TRSV_REG028F	0x0A3C	W	0x000000C0	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0291	0x0A44	W	0x000000C0	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0292	0x0A48	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0293	0x0A4C	W	0x000000F9	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0295	0x0A54	W	0x000000CF	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0297	0x0A5C	W	0x000000CF	USBDPPHY TRSV configure register

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Name	Offset	Size	Reset Value	Description
USBDPPHY_TRSV_REG0299	0x0A64	W	0x0000009B	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG068F	0x1A3C	W	0x000000C0	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0691	0x1A44	W	0x000000C0	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0692	0x1A48	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0693	0x1A4C	W	0x000000F9	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0695	0x1A54	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0697	0x1A5C	W	0x000000CF	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0699	0x1A64	W	0x0000009B	USBDPPHY TRSV configure register
USBDPPHY_CMN_REG00A3	0x028C	W	0x00000000	USBDPPHY CMN configure register
USBDPPHY_TRSV_REG0215	0x0854	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0415	0x1054	W	0x00000004	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0815	0x1054	W	0x00000004	USBDPPHY TRSV configure register
USBDPPHY_CMN_REG00E3	0x038C	W	0x00000002	USBDPPHY CMN configure register
USBDPPHY_CMN_REG00D5	0x0354	W	0x00000000	USBDPPHY CMN configure register
USBDPPHY_TRSV_REG02E1	0x0B84	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG06E1	0x1B84	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0204	0x0810	W	0x0000000F	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0404	0x1010	W	0x0000000F	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0604	0x1810	W	0x0000000F	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0804	0x2010	W	0x0000000F	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0205	0x0814	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0405	0x1014	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0605	0x1814	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0805	0x2014	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0206	0x0818	W	0x00000001	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0406	0x1018	W	0x00000001	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0606	0x1818	W	0x00000001	USBDPPHY TRSV configure register

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Name	Offset	Size	Reset Value	Description
USBDPPHY_TRSV_REG0806	0x2018	W	0x00000001	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0207	0x081C	W	0x000000E7	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0407	0x101C	W	0x000000E7	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0607	0x181C	W	0x000000E7	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0807	0x201C	W	0x000000E7	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG020C	0x0830	W	0x00000007	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0217	0x085C	W	0x00000080	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG040C	0x1030	W	0x00000007	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0417	0x105C	W	0x00000080	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG060C	0x1830	W	0x00000007	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0617	0x185C	W	0x00000080	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG080C	0x2030	W	0x00000007	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0817	0x205C	W	0x00000080	USBDPPHY TRSV configure register
USBDPPHY_CMN_REG008A	0x0228	W	0x00000038	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0041	0x0104	W	0x00000077	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0092	0x0248	W	0x00000077	USBDPPHY CMN configure register
USBDPPHY_TRSV_REG021E	0x0878	W	0x00000004	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG061E	0x1878	W	0x00000004	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0226	0x0898	W	0x00000077	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0626	0x189C	W	0x00000077	USBDPPHY TRSV configure register
USBDPPHY_CMN_REG0015	0x0054	W	0x00000001	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0038	0x00E0	W	0x00000038	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0018	0x0060	W	0x00000024	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0019	0x0064	W	0x000000FF	USBDPPHY CMN configure register
USBDPPHY_CMN_REG001C	0x0070	W	0x00000006	USBDPPHY CMN configure register
USBDPPHY_CMN_REG008D	0x0234	W	0x00000068	USBDPPHY CMN configure register
USBDPPHY_TRSV_REG02BD	0x0AF4	W	0x00000018	USBDPPHY TRSV configure register

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Name	Offset	Size	Reset Value	Description
USBDPPHY_TRSV_REG06BD	0x1AF4	W	0x00000018	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0267	0x099C	W	0x00000008	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0667	0x199C	W	0x00000008	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0269	0x09A4	W	0x00000007	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG026A	0x09A8	W	0x00000022	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0669	0x19A4	W	0x00000007	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG066A	0x19A8	W	0x00000022	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG026E	0x09B8	W	0x0000004E	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG066E	0x19B8	W	0x0000004E	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0279	0x09E4	W	0x00000002	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0679	0x09E8	W	0x00000002	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG028D	0x0A34	W	0x00000010	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG068D	0x1A34	W	0x00000010	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG02A6	0x0A98	W	0x0000004F	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG06A6	0x1A98	W	0x0000004F	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG030C	0x0C30	W	0x00000006	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0312	0x0C48	W	0x00000003	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG070C	0x1C3C	W	0x00000006	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0712	0x1C48	W	0x00000003	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG06BC	0x1AF0	W	0x0000001D	USBDPPHY TRSV configure register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

15.4.2 Detail Registers Description

USBDPPHY_CMM_REG0024

Address: Operational Base(0x2B018000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x3c	ana_lcpll_pms_mdiv PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMM_REG0025

Address: Operational Base(0x2B018000) + offset (0x0094)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x60	ana_lcpll_pms_mdiv PLL main divider setting for AFC counter. Divider value = Setting code.

USBDPPHY_CMN_REG004A

Address: Operational Base(0x2B018000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:3	RW	0x7	ropll_ana_cpi_ctrl_coarse PLL integral path charge-pump current contorl. 3'b0xx: half current (not used) 3'b100: 1.25uA 3'b101: 1.5625uA 3'b110: 20833uA 3'b111: 3.125uA
2:0	RW	0x4	ropll_ana_cpi_ctrl_fine PLL integral path charge-pump current contorl. 3'b0xx: half current (not used) 3'b100: 1.25uA 3'b101: 1.5625uA 3'b110: 20833uA 3'b111: 3.125uA

USBDPPHY_CMN_REG004B

Address: Operational Base(0x2B018000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0xf	ropll_ana_cpp_ctrl_coarse PLL proportional path charge-pump current contorl. 3'b000: 66.7uA 3'b001: 75uA 3'b010: 85.7uA 3'b011: 100uA 3'b100: 120uA 3'b101: 150uA 3'b110: 200uA 3'b111: 300uA
3:0	RW	0x4	ropll_ana_cpp_ctrl_fine PLL proportional path charge-pump current contorl. 3'b000: 66.7uA 3'b001: 75uA 3'b010: 85.7uA 3'b011: 100uA 3'b100: 120uA 3'b101: 150uA 3'b110: 200uA 3'b111: 300uA

USBDPPHY_CMN_REG004C

Address: Operational Base(0x2B018000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:3	RW	0x1	ropll_ana_lpf_c_sel_coarse PLL loop filter capacitor control. 3'b000: 0pF 3'b001: 1pF 3'b010: 2pF 3'b011: 3pF 3'b100: 4pF 3'b101: 5pF 3'b110: 6pF 3'b111: 7pF
2:0	RW	0x7	ropll_ana_lpf_c_sel_fine PLL loop filter capacitor control. 3'b000: 0pF 3'b001: 1pF 3'b010: 2pF 3'b011: 3pF 3'b100: 4pF 3'b101: 5pF 3'b110: 6pF 3'b111: 7pF

USBDPPHY_CMN_REG004D

Address: Operational Base(0x2B018000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0xf	ropll_ana_lpf_r_sel_coarse PLL loop filter resistor control. 4'b0000: 2K 4'b0001: 4K 4'b0010:6K ~ 4'b1111: 32K
3:0	RW	0x4	ropll_ana_lpf_r_sel_fine PLL loop filter resistor control. 4'b0000: 2K 4'b0001: 4K 4'b0010:6K 4'b1111: 32K

USBDPPHY_CMN_REG0057

Address: Operational Base(0x2B018000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x4e	ropll_pms_mdiv_rbr PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMN_REG0058

Address: Operational Base(0x2B018000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x34	ropll_pms_mdiv_hbr PLL main divider setting. Divider value = Setting code.

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USBDPPHY_CMN_REG0059

Address: Operational Base(0x2B018000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x34	ropll_pms_mdiv_hbr2 PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMN_REG005A

Address: Operational Base(0x2B018000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x4e	ropll_pms_mdiv_hbr3 PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMN_REG005D

Address: Operational Base(0x2B018000) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x4e	ropll_pms_mdiv_afc_rbr PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMN_REG005E

Address: Operational Base(0x2B018000) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x34	ropll_pms_mdiv_afc_hbr PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMN_REG005F

Address: Operational Base(0x2B018000) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x34	ropll_pms_mdiv_afc_hbr2 PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMN_REG0060

Address: Operational Base(0x2B018000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x4e	ropll_pms_mdiv_afc_hbr3 PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMN_REG0063

Address: Operational Base(0x2B018000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x4	ropll_pms_sdiv_rbr PLL post divider setting (N-1, except /7). 3'b000: /1 3'b001: /2 3'b010: /3 3'b011: /4 3'b100: /5 3'b101: /6 3'b110: X 3'b111: /8
3:0	RW	0x1	ropll_pms_sdiv_hbr PLL post divider setting (N-1, except /7). 3'b000: /1 3'b001: /2 3'b010: /3 3'b011: /4 3'b100: /5 3'b101: /6 3'b110: X 3'b111: /8

USBDPPHY_CMN_REG0064

Address: Operational Base(0x2B018000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ropll_pms_sdiv_hbr3 PLL post divider setting (N-1, except /7). 3'b000: /1 3'b001: /2 3'b010: /3 3'b011: /4 3'b100: /5 3'b101: /6 3'b110: X 3'b111: /8
3:0	RW	0x0	ropll_pms_sdiv_hbr2 PLL post divider setting (N-1, except /7). 3'b000: /1 3'b001: /2 3'b010: /3 3'b011: /4 3'b100: /5 3'b101: /6 3'b110: X 3'b111: /8

USBDPPHY_CMN_REG0065

Address: Operational Base(0x2B018000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ana_ropll_iqdiv_bypass VCO clock bypass IQ divider enable.
6	RW	0x0	ovrd_ropll_pms_iqdiv_rstn Override enable flag for ropll_pms_iqdiv_rstn
5	RW	0x0	ropll_pms_iqdiv_rstn IQ divider resetn.

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Bit	Attr	Reset Value	Description
4:3	RW	0x0	ana_ropll_ref_bypass_clk_sel PLL Bypass clock selection. 2'b00: XO 2'b01: IO 2'b10: PIXEL or LC_OUT_CLK 2'b11: System PLL clock
2	RW	0x1	ana_ropll_ref_chopper_clk_en Chopper clk enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	ovrd_ropll_ref_chopper_clk_div_rstn Override enable flag for ropll_ref_chopper_clk_div_rstn.
0	RW	0x1	ropll_ref_chopper_clk_div_rstn Chopper clk divider reset. 1'b0: Reset. 1'b1: Released.

USBDPPHY_CMN_REG006B

Address: Operational Base(0x2B018000) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x2c	ropll_sdm_denominator_rbr Denominator of SDM (Max. 255) Constraint: i_pll_sdm_lc > |signedi_pll_sdm_k-i_pll_ssc_fm_deviation-i_pll_ssc_fm_freq-1|

USBDPPHY_CMN_REG006C

Address: Operational Base(0x2B018000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x2c	ropll_sdm_denominator_hbr Denominator of SDM (Max. 255) Constraint: i_pll_sdm_lc > |signedi_pll_sdm_k-i_pll_ssc_fm_deviation-i_pll_ssc_fm_freq-1|

USBDPPHY_CMN_REG006D

Address: Operational Base(0x2B018000) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x2c	ropll_sdm_denominator_hbr2 Denominator of SDM (Max. 255) Constraint: i_pll_sdm_lc > |signedi_pll_sdm_k-i_pll_ssc_fm_deviation-i_pll_ssc_fm_freq-1|

USBDPPHY_CMN_REG006E

Address: Operational Base(0x2B018000) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x2c	ropll_sdm_denominator_hbr3 Denominator of SDM (Max. 255) Constraint: i_pll_sdm_lc > |signedi_pll_sdm_k-i_pll_ssc_fm_deviation-i_pll_ssc_fm_freq-1|

USBDPPHY_CMN_REG0072

Address: Operational Base(0x2B018000) + offset (0x01C8)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x08	ropll_sdm_numerator_rbr Numerator of SDM with i_pll_sdm_k_sign (-255~255).

USBDPPHY_CMN_REG0073

Address: Operational Base(0x2B018000) + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x08	ropll_sdm_numerator_hbr Numerator of SDM with i_pll_sdm_k_sign (-255~255).

USBDPPHY_CMN_REG0074

Address: Operational Base(0x2B018000) + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x08	ropll_sdm_numerator_hbr2 Numerator of SDM with i_pll_sdm_k_sign (-255~255).

USBDPPHY_CMN_REG0075

Address: Operational Base(0x2B018000) + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x08	ropll_sdm_numerator_hbr3 Numerator of SDM with i_pll_sdm_k_sign (-255~255).

USBDPPHY_CMN_REG0076

Address: Operational Base(0x2B018000) + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ana_ropll_sdm_ph_num_sel PLL PI input clock phase number . 1'b0: 8-phase, 1'b1: 4-phase
4:3	RW	0x0	ana_ropll_sdm_pi_step PLL phase interpolstor step. 3'b00: 1-step (16-phase) 3'b01: 2-step (8-phase) 3'b1x: 0.5-step
2:0	RW	0x0	ropll_sdc_n_sp PLL SDC divide-ratio selection (MC_val=0 N, MC_val=1 N-1) 3'b000: /4/3 3'b001: /5/4 3'b010: /6/5 3'b100: /7/6 3'b101: /8/7 3'b110: /9/8

USBDPPHY_CMN_REG0077

Address: Operational Base(0x2B018000) + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:3	RW	0x0	ropll_sdc_n_ssp PLL SDC divide-ratio selection (MC_val=0 N, MC_val=1 N-1). 3'b000: /4/3 3'b001: /5/4 3'b010: /6/5 3'b100: /7/6 3'b101: /8/7 3'b110: /9/8
2:0	RW	0x5	ropll_sdc_n_rbr PLL SDC divide-ratio selection (MC_val=0 N, MC_val=1 N-1). 3'b000: /4/3 3'b001: /5/4 3'b010: /6/5 3'b100: /7/6 3'b101: /8/7 3'b110: /9/8

USBDPPHY_CMN_REG0078

Address: Operational Base(0x2B018000) + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:3	RW	0x5	ropll_sdc_n_hbr PLL SDC divide-ratio selection (MC_val=0 N, MC_val=1 N-1) 3'b000: /4/3 3'b001: /5/4 3'b010: /6/5 3'b100: /7/6 3'b101: /8/7 3'b110: /9/8
2:0	RW	0x5	ropll_sdc_n_hbr2 PLL SDC divide-ratio selection (MC_val=0 N, MC_val=1 N-1) 3'b000: /4/3 3'b001: /5/4 3'b010: /6/5 3'b100: /7/6 3'b101: /8/7 3'b110: /9/8

USBDPPHY_CMN_REG0079

Address: Operational Base(0x2B018000) + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:1	RW	0x5	ropll_sdc_n_hbr3 PLL SDC divide-ratio selection (MC_val=0 N, MC_val=1 N-1) 3'b000: /4/3 3'b001: /5/4 3'b010: /6/5 3'b100: /7/6 3'b101: /8/7 3'b110: /9/8
0	RW	0x0	ana_ropll_sdc_n2 PLL SDC divide-ratio selection. 1'b0: No additional /2 1'b1: Additional /2

USBDPPHY_CMN_REG007C

Address: Operational Base(0x2B018000) + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	ropll_sdc_numerator_rbr Numerator of SDC (Max 65).

USBDPPHY_CMN_REG007D

Address: Operational Base(0x2B018000) + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	ropll_sdc_numerator_hbr Numerator of SDC (Max 65).

USBDPPHY_CMN_REG007E

Address: Operational Base(0x2B018000) + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	ropll_sdc_numerator_hbr2 Numerator of SDC (Max 65).

USBDPPHY_CMN_REG007F

Address: Operational Base(0x2B018000) + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x07	ropll_sdc_numerator_hbr3 Numerator of SDC (Max 65).

USBDPPHY_CMN_REG0082

Address: Operational Base(0x2B018000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x16	ropll_sdc_denominator_rbr Denominator of SDC (Max 65).

USBDPPHY_CMN_REG0083

Address: Operational Base(0x2B018000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x16	ropll_sdc_denominator_hbr Denominator of SDC (Max 65).

USBDPPHY_CMN_REG0084

Address: Operational Base(0x2B018000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x16	ropll_sdc_denominator_hbr2 Denominator of SDC (Max 65).

USBDPPHY_CMN_REG0085

Address: Operational Base(0x2B018000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x16	ropll_sdc_denominator_hbr3 Denominator of SDC (Max 65).

USBDPPHY_CMN_REG0089

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Address: Operational Base(0x2B018000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x1	ana_ropll_ssc_clk_div_sel PLL SSC clock divide ratio. 4'b0000: N/A 4'b0001: /1 4'b0010: /2 ~ 4'b1111: /15
3	RW	0x0	ovrd_ropll_cd_clk_en Override enable flag for ropll_cd_clk_en
2	RW	0x0	ropll_cd_clk_en CD enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	ovrd_ropll_cd_tx_ser_rstn Override enable flag for ropll_cd_tx_ser_rstn.
0	RW	0x0	ropll_cd_tx_ser_rstn TX_SER resetn.

USBDPPHY_CMN_REG00FC

Address: Operational Base(0x2B018000) + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x19	ana_ropll_ssc_fm_deviation_rbr PLL SSC modulation deviation.

USBDPPHY_CMN_REG00FD

Address: Operational Base(0x2B018000) + offset (0x03F4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x19	ana_ropll_ssc_fm_deviation_hbr PLL SSC modulation deviation.

USBDPPHY_CMN_REG00FE

Address: Operational Base(0x2B018000) + offset (0x03F8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x19	ana_ropll_ssc_fm_deviation_hbr2 PLL SSC modulation deviation.

USBDPPHY_CMN_REG00FF

Address: Operational Base(0x2B018000) + offset (0x03FC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x19	ana_ropll_ssc_fm_deviation_hbr3 PLL SSC modulation deviation.

USBDPPHY_CMN_REG0101

Address: Operational Base(0x2B018000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0f	ana_ropll_ssc_fm_freq_rbr PLL SSC modulation frequency.

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USBDPPHY_CMN_REG0102

Address: Operational Base(0x2B018000) + offset (0x0408)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0f	ana_ropll_ssc_fm_freq_hbr PLL SSC modulation frequency.

USBDPPHY_CMN_REG0103

Address: Operational Base(0x2B018000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0f	ana_ropll_ssc_fm_freq_hbr2 PLL SSC modulation frequency.

USBDPPHY_CMN_REG0104

Address: Operational Base(0x2B018000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:2	RW	0x0f	ana_ropll_ssc_fm_freq_hbr3 PLL SSC modulation frequency.
1	RW	0x0	lcpll_lock_done_delay_bypass Lock_done_flag_delay_bypass.
0	RW	0x0	ropll_lock_done_delay_bypass Lock_done_flag_delay_bypass.

USBDPPHY_TRSV_REG028F

Address: Operational Base(0x2B018000) + offset (0x0A3C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xc0	ln0_rx_cdr_pms_m_sp_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0291

Address: Operational Base(0x2B018000) + offset (0x0A44)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xc0	ln0_rx_cdr_pms_m_ssp_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0292

Address: Operational Base(0x2B018000) + offset (0x0A48)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ln0_rx_cdr_pms_m_rbr_8 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0293

Address: Operational Base(0x2B018000) + offset (0x0A4C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xf9	ln0_rx_cdr_pms_m_rbr_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

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USBDPPHY_TRSV_REG0295

Address: Operational Base(0x2B018000) + offset (0x0A54)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xcf	ln0_rx_cdr_pms_m_hbr_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0297

Address: Operational Base(0x2B018000) + offset (0x0A5C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xcf	ln0_rx_cdr_pms_m_hbr2_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0299

Address: Operational Base(0x2B018000) + offset (0x0A64)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x9b	ln0_rx_cdr_pms_m_hbr3_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG068F

Address: Operational Base(0x2B018000) + offset (0x1A3C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xc0	ln2_rx_cdr_pms_m_sp_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0691

Address: Operational Base(0x2B018000) + offset (0x1A44)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xc0	ln2_rx_cdr_pms_m_ssp_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0692

Address: Operational Base(0x2B018000) + offset (0x1A48)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ln2_rx_cdr_pms_m_rbr_8 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0693

Address: Operational Base(0x2B018000) + offset (0x1A4C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xf9	ln2_rx_cdr_pms_m_rbr_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

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USBDPPHY_TRSV_REG0695

Address: Operational Base(0x2B018000) + offset (0x1A54)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ln2_rx_cdr_pms_m_hbr_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0697

Address: Operational Base(0x2B018000) + offset (0x1A5C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xcf	ln2_rx_cdr_pms_m_hbr2_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0699

Address: Operational Base(0x2B018000) + offset (0x1A64)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x9b	ln2_rx_cdr_pms_m_hbr3_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_CMN_REG00A3

Address: Operational Base(0x2B018000) + offset (0x028C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RW	0x0	dp_tx_link_bw DP bandwidth 2'b00: RBR (1.62Gbps) 2'b01: HBR (2.7Gbps) 2'b10: HBR2(5.4Gbps) 2'b11: HBR3(8.1Gbps)
4:3	RO	0x0	reserved
2	RW	0x0	dp_tx_lane_swap_en DP lane swap enable. 1'b0: Lane0/1/2/3_TxData mapping to Lane0/1/2/3_TXDP/N. 1'b1: Lane0/1/2/3_TxData mapping to Lane2/3/0/1_TXDP/N.
1	RW	0x0	dp_tx_data_inv DP TX data polarity inversion enable.
0	RW	0x0	dp_tx_data_swap DP TX data bit order swap enable (MSB <-> LSB).

USBDPPHY_TRSV_REG0215

Address: Operational Base(0x2B018000) + offset (0x0854)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln0_tx_ser_rate_sel_hbr TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit

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Bit	Attr	Reset Value	Description
6	RW	0x0	ln0_tx_ser_rate_sel_hbr2 TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
5	RW	0x0	ln0_tx_ser_rate_sel_hbr3 TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
4	RW	0x0	ovrd_ln0_tx_ser_clk_rstn Override enable flag for ln0_tx_ser_clk_rstn
3	RW	0x0	ln0_tx_ser_clk_rstn TX serializer clock-path resetn. 1'b0: Reset 1'b1: Released
2	RW	0x0	ln0_ana_tx_cdr_clk_mon_en TX serializer clock selection: If default=0 then MUX will always toggle with PLL clk and 1mA power waste. CDR clock is turned off in RX therefore power will not burn. 1'b0: PLL clock 1'b1: CDR clock
1	RO	0x0	reserved
0	RW	0x0	ln0_ana_tx_lane_rstn_sel Mux select to choose lane RSTN (ser_clk_rstn) or CMN RSTN (ser_tx_clk_rstn) which resets the CMN RSTN (ser_tx_clk_rstn) which resets the divider, 1'b0: CMN RSTN 1'b1: LINE RSTN

USBDPPHY_TRSV_REG0415

Address: Operational Base(0x2B018000) + offset (0x1054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln1_tx_ser_rate_sel_hbr TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
6	RW	0x0	ln1_tx_ser_rate_sel_hbr2 TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
5	RW	0x0	ln1_tx_ser_rate_sel_hbr3 TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
4	RW	0x0	ovrd_ln1_tx_ser_clk_rstn Override enable flag for ln1_tx_ser_clk_rstn
3	RW	0x0	ln1_tx_ser_clk_rstn TX serializer clock-path resetn. 1'b0: Reset 1'b1: Released

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Bit	Attr	Reset Value	Description
2	RW	0x1	ln1_ana_tx_cdr_clk_mon_en TX serializer clock selection: If default=0 then MUX will always toggle with PLL clk and 1mA power waste. CDR clock is turned off in RX therefore power will not burn 1'b0: PLL clock 1'b1: CDR clock
1	RO	0x0	reserved
0	RW	0x0	ln1_ana_tx_lane_rstn_sel Mux select to choose lane RSTN (ser_clk_rstn) or CMN RSTN (ser_tx_clk_rstn) which resets the divider (/5/10/20). 1'b0: CMN RSTN 1'b1: LANE RSTN

USBDPPHY_TRSV_REG0815

Address: Operational Base(0x2B018000) + offset (0x1054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln3_tx_ser_rate_sel_hbr TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
6	RW	0x0	ln3_tx_ser_rate_sel_hbr2 TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
5	RW	0x0	ln3_tx_ser_rate_sel_hbr3 TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
4	RW	0x0	ovrd_ln3_tx_ser_clk_rstn Override enable flag for ln1_tx_ser_clk_rstn
3	RW	0x0	ln3_tx_ser_clk_rstn TX serializer clock-path resetn. 1'b0: Reset 1'b1: Released
2	RW	0x1	ln3_ana_tx_cdr_clk_mon_en TX serializer clock selection: If default=0 then MUX will always toggle with PLL clk and 1mA power waste. CDR clock is turned off in RX therefore power will not burn 1'b0: PLL clock 1'b1: CDR clock
1	RO	0x0	reserved
0	RW	0x0	ln3_ana_tx_lane_rstn_sel Mux select to choose lane RSTN (ser_clk_rstn) or CMN RSTN (ser_tx_clk_rstn) which resets the divider (/5/10/20). 1'b0: CMN RSTN 1'b1: LANE RSTN

USBDPPHY_CMN_REG00E3

Address: Operational Base(0x2B018000) + offset (0x038C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3	RW	0x0	dp_init_rstn DP initial reset.
2	RW	0x0	dp_cmn_rstn DP PLL reset.
1	RW	0x1	cdr_watchdog_en CDR lock watchdog enable. If CDR lock wasn't occured, toggle cdr_en signal to restart CDR.
0	RW	0x0	cdr_watchdog_mask_cdr_en Disable cdr_en toggle when CDR restart by watchdog.

USBDPPHY_CMN_REG00D5

Address: Operational Base(0x2B018000) + offset (0x0354)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:2	RO	0x0	ana_lcpll_mon_gm_code LC VCO GM code monitor.
1	RO	0x0	ana_ropll_lock_done PLL Lock Done.
0	RO	0x0	ana_ropll_afc_done PLL AFC Done.

USBDPPHY_TRSV_REG02E1

Address: Operational Base(0x2B018000) + offset (0x0B84)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	ln0_mon_rx_cdr_afc_done Monitoring SFR.
2	RO	0x0	ln0_mon_rx_cdr_cal_done Monitoring SFR.
1	RO	0x0	ln0_mon_rx_cdr_fld_pll_mode_done Monitoring SFR.
0	RO	0x0	ln0_mon_rx_cdr_lock_done Monitoring SFR.

USBDPPHY_TRSV_REG06E1

Address: Operational Base(0x2B018000) + offset (0x1B84)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ln2_mon_rx_cdr_afc_done Monitoring SFR.
2	RO	0x0	ln2_mon_rx_cdr_cal_done Monitoring SFR.
1	RO	0x0	ln2_mon_rx_cdr_fld_pll_mode_done Monitoring SFR.
0	RO	0x0	ln2_mon_rx_cdr_done Monitoring SFR.

USBDPPHY_TRSV_REG0204

Address: Operational Base(0x2B018000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ovrd_ln0_tx_drv_lvl_ctrl Override enable flag for ln0_tx_drv_lvl_ctrl

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Bit	Attr	Reset Value	Description
4:0	RW	0x0f	ln0_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap level (max swing) ~ 5'b00000: min main-tap level (min swing) Others: N/A

USBDPPHY_TRSV_REG0404

Address: Operational Base(0x2B018000) + offset (0x1010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ovrd_ln1_tx_drv_lvl_ctrl Override enable flag for ln1_tx_drv_lvl_ctrl
4:0	RW	0x0f	ln1_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap level (max swing) ~ 5'b00000: min main-tap level (min swing) Others: N/A

USBDPPHY_TRSV_REG0604

Address: Operational Base(0x2B018000) + offset (0x1810)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ovrd_ln2_tx_drv_lvl_ctrl Override enable flag for ln2_tx_drv_lvl_ctrl
4:0	RW	0x0f	ln2_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap level (max swing) ~ 5'b00000: min main-tap level (min swing) Others: N/A

USBDPPHY_TRSV_REG0804

Address: Operational Base(0x2B018000) + offset (0x2010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ovrd_ln3_tx_drv_lvl_ctrl Override enable flag for ln3_tx_drv_lvl_ctrl
4:0	RW	0x0f	ln3_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap level (max swing) ~ 5'b00000: min main-tap level (min swing) Others: N/A

USBDPPHY_TRSV_REG0205

Address: Operational Base(0x2B018000) + offset (0x0814)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ovrd_ln0_tx_drv_lvl_ctrl Override enable flag for ln0_tx_drv_post_lvl_ctrl

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	ln0_tx_drv_post_lvl_ctrl TX driver de-emphasis level (TX_DE_EMP<14:0>) 3'b0000: min de-emphasis level ~ 3'b1110: max de-emphasis level Others: N/A

USBDPPHY_TRSV_REG0405

Address: Operational Base(0x2B018000) + offset (0x1014)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ovrd_ln1_tx_drv_lvl_ctrl Override enable flag for ln1_tx_drv_post_lvl_ctrl
3:0	RW	0x0	ln1_tx_drv_post_lvl_ctrl TX driver de-emphasis level (TX_DE_EMP<14:0>) 3'b0000: min de-emphasis level ~ 3'b1110: max de-emphasis level Others: N/A

USBDPPHY_TRSV_REG0605

Address: Operational Base(0x2B018000) + offset (0x1814)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ovrd_ln2_tx_drv_lvl_ctrl Override enable flag for ln2_tx_drv_post_lvl_ctrl
3:0	RW	0x0	ln2_tx_drv_post_lvl_ctrl TX driver de-emphasis level (TX_DE_EMP<14:0>) 3'b0000: min de-emphasis level ~ 3'b1110: max de-emphasis level Others: N/A

USBDPPHY_TRSV_REG0805

Address: Operational Base(0x2B018000) + offset (0x2014)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ovrd_ln3_tx_drv_lvl_ctrl Override enable flag for ln3_tx_drv_post_lvl_ctrl
3:0	RW	0x0	ln3_tx_drv_post_lvl_ctrl TX driver de-emphasis level (TX_DE_EMP<14:0>) 3'b0000: min de-emphasis level ~ 3'b1110: max de-emphasis level Others: N/A

USBDPPHY_TRSV_REG0206

Address: Operational Base(0x2B018000) + offset (0x0818)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ovrd_ln0_tx_drv_pre_lvl_ctrl Override enable flag for ln0_tx_drv_pre_lvl_ctrl

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Bit	Attr	Reset Value	Description
5:2	RW	0x0	ln0_tx_drv_pre_lvl_ctrl TX driver pre-shoot level (TX_PRE_EMP<9:0>) 4'b0000: min pre-shoot boosting ~ 4'b1001: max pre-shoot boosting Others: N/A
1	RW	0x0	ovrd_ln0_tx_drv_idrv_en Override enable flag for ln0_tx_drv_idrv_en
0	RW	0x1	ln0_tx_drv_idrv_en TX current-driver enable 1'b0: Disable 1'b1: Enable

USBDPPHY_TRSV_REG0406

Address: Operational Base(0x2B018000) + offset (0x1018)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ovrd_ln1_tx_drv_pre_lvl_ctrl Override enable flag for ln1_tx_drv_pre_lvl_ctrl
5:2	RW	0x0	ln1_tx_drv_pre_lvl_ctrl TX driver pre-shoot level (TX_PRE_EMP<9:0>) 4'b0000: min pre-shoot boosting ~ 4'b1001: max pre-shoot boosting Others: N/A
1	RW	0x0	ovrd_ln1_tx_drv_idrv_en Override enable flag for ln1_tx_drv_idrv_en
0	RW	0x1	ln1_tx_drv_idrv_en TX current-driver enable 1'b0: Disable 1'b1: Enable

USBDPPHY_TRSV_REG0606

Address: Operational Base(0x2B018000) + offset (0x1818)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ovrd_ln2_tx_drv_pre_lvl_ctrl Override enable flag for ln2_tx_drv_pre_lvl_ctrl
5:2	RW	0x0	ln2_tx_drv_pre_lvl_ctrl TX driver pre-shoot level (TX_PRE_EMP<9:0>) 4'b0000: min pre-shoot boosting ~ 4'b1001: max pre-shoot boosting Others: N/A
1	RW	0x0	ovrd_ln2_tx_drv_idrv_en Override enable flag for ln2_tx_drv_idrv_en
0	RW	0x1	ln2_tx_drv_idrv_en TX current-driver enable 1'b0: Disable 1'b1: Enable

USBDPPHY_TRSV_REG0806

Address: Operational Base(0x2B018000) + offset (0x2018)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	ovrd_ln3_tx_drv_pre_lvl_ctrl Override enable flag for ln3_tx_drv_pre_lvl_ctrl
5:2	RW	0x0	ln3_tx_drv_pre_lvl_ctrl TX driver pre-shoot level (TX_PRE_EMP<9:0>) 4'b0000: min pre-shoot boosting ~ 4'b1001: max pre-shoot boosting Others: N/A
1	RW	0x0	ovrd_ln3_tx_drv_idrv_en Override enable flag for ln3_tx_drv_idrv_en
0	RW	0x1	ln3_tx_drv_idrv_en TX current-driver enable 1'b0: Disable 1'b1: Enable

USBDPPHY_TRSV_REG0207

Address: Operational Base(0x2B018000) + offset (0x081C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x7	ln0_ana_tx_drv_idrv_iup_ctrl TX current driver pmos current control. 3'b000: Min 3'b111: Max
4	RW	0x0	ln0_ana_tx_drv_beacon_idrv_delay_sel Retain idrv settling time margin @beacon entry. 1'b0: Select delay (default) 1'b1: Org
3:2	RW	0x1	ln0_ana_tx_drv_beacon_idrv_delay_ctrl i_tx_drv_beacon_delay_ctrl<1:0> 3'b00: 2UI delay 3'b01: 3UI delay (default) 3'b10: 4UI delay 3'b11: 5UI delay
1	RW	0x1	ln0_ana_tx_drv_accdrv_en Enable of Cap. Peaking block. 1'b0: Disable 1'b1: Enable
0	RW	0x1	ln0_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b1: polarity change, data P/N is switched (enhancement) 1'b0: polarity non-change (deenhancement)

USBDPPHY_TRSV_REG0407

Address: Operational Base(0x2B018000) + offset (0x101C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x7	ln1_ana_tx_drv_idrv_iup_ctrl TX current driver pmos current control. 3'b000: Min 3'b111: Max
4	RW	0x0	ln1_ana_tx_drv_beacon_idrv_delay_sel Retain idrv settling time margin @beacon entry. 1'b0: Select delay (default) 1'b1: Org

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Bit	Attr	Reset Value	Description
3:2	RW	0x1	ln1_ana_tx_drv_beacon_idrv_delay_ctrl i_tx_drv_beacon_delay_ctrl<1:0> 3'b00: 2UI delay 3'b01: 3UI delay (default) 3'b10: 4UI delay 3'b11: 5UI delay
1	RW	0x1	ln1_ana_tx_drv_accdrv_en Enable of Cap. Peaking block. 1'b0: Disable 1'b1: Enable
0	RW	0x1	ln1_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b1: polarity change, data P/N is switched (enhancement) 1'b0: polarity non-change (deenhancement)

USBDPPHY_TRSV_REG0607

Address: Operational Base(0x2B018000) + offset (0x181C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x7	ln2_ana_tx_drv_idrv_iup_ctrl TX current driver pmos current control. 3'b000: Min 3'b111: Max
4	RW	0x0	ln2_ana_tx_drv_beacon_idrv_delay_sel Retain idrv settling time margin @beacon entry. 1'b0: Select delay (default) 1'b1: Org
3:2	RW	0x1	ln2_ana_tx_drv_beacon_idrv_delay_ctrl i_tx_drv_beacon_delay_ctrl<1:0> 3'b00: 2UI delay 3'b01: 3UI delay (default) 3'b10: 4UI delay 3'b11: 5UI delay
1	RW	0x1	ln2_ana_tx_drv_accdrv_en Enable of Cap. Peaking block. 1'b0: Disable 1'b1: Enable
0	RW	0x1	ln2_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b1: polarity change, data P/N is switched (enhancement) 1'b0: polarity non-change (deenhancement)

USBDPPHY_TRSV_REG0807

Address: Operational Base(0x2B018000) + offset (0x201C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x7	ln3_ana_tx_drv_idrv_iup_ctrl TX current driver pmos current control. 3'b000: Min 3'b111: Max
4	RW	0x0	ln3_ana_tx_drv_beacon_idrv_delay_sel Retain idrv settling time margin @beacon entry. 1'b0: Select delay (default) 1'b1: Org

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Bit	Attr	Reset Value	Description
3:2	RW	0x1	ln3_ana_tx_drv_beacon_idrv_delay_ctrl i_tx_drv_beacon_delay_ctrl<1:0> 3'b00: 2UI delay 3'b01: 3UI delay (default) 3'b10: 4UI delay 3'b11: 5UI delay
1	RW	0x1	ln3_ana_tx_drv_accdrv_en Enable of Cap. Peaking block. 1'b0: Disable 1'b1: Enable
0	RW	0x1	ln3_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b1: polarity change, data P/N is switched (enhancement) 1'b0: polarity non-change (deenhancement)

USBDPPHY_TRSV_REG020C

Address: Operational Base(0x2B018000) + offset (0x0830)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ln0_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x7	ln0_tx_jeq_even_ctrl_sp TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on

USBDPPHY_TRSV_REG0217

Address: Operational Base(0x2B018000) + offset (0x085C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	ovrd_ln0_tx_ser_vreg_en Override enable flag for ln0_tx_ser_vreg_en
6	RW	0x0	ln0_tx_ser_vreg_en Controls Regulator Enable: 1'b0: Disable regulator (Bypass VDD PMOS switch turns ON) 1'b1: Regulator Enable (Bypass path disables)
5	RW	0x0	ln0_ana_tx_ser_vreg_bypass Force Bypass Regulator: 1'b0: Regulator mode 1'b1: Bypass Regulator and VDD is connected to Regulator node using pass gate
4	RW	0x0	ovrd_ln0_tx_ser_vreg_lpf_bypass Override enable flag for ln0_tx_ser_vreg_lpf_bypass.

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Bit	Attr	Reset Value	Description
3	RW	0x0	ln0_tx_ser_vreg_lpf_bypass Controls Regulator input voltage reference noise reduction Low pass filter (BW <5MHz) 1'b0: Regulator reference Low pass filter Mode 1'b1: Bypass Low pass filter (Fast charging)
2:0	RW	0x0	ln0_ana_tx_ser_vreg Choose vref based on VDDH ladder tap points. For VDDH=1.8, Vref=: 3'b000:0.749 3'b001:0.776 3'b010:0.804 3'b011:0.831 3'b100:0.859(default), 3'b101:0.886 3'b110:0.914 3'b111:0.941

USBDPPHY_TRSV_REG040C

Address: Operational Base(0x2B018000) + offset (0x1030)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ln1_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x7	ln1_tx_jeq_even_ctrl_sp TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on

USBDPPHY_TRSV_REG0417

Address: Operational Base(0x2B018000) + offset (0x105C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	ovrd_ln1_tx_ser_vreg_en Override enable flag for ln1_tx_ser_vreg_en
6	RW	0x0	ln1_tx_ser_vreg_en Controls Regulator Enable: 1'b0: Disable regulator (Bypass VDD PMOS switch turns ON) 1'b1: Regulator Enable (Bypass path disables)
5	RW	0x0	ln1_ana_tx_ser_vreg_bypass Force Bypass Regulator: 1'b0: Regulator mode 1'b1: Bypass Regulator and VDD is connected to Regulator node using pass gate
4	RW	0x0	ovrd_ln1_tx_ser_vreg_lpf_bypass Override enable flag for ln1_tx_ser_vreg_lpf_bypass.

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Bit	Attr	Reset Value	Description
3	RW	0x0	ln1_tx_ser_vreg_lpf_bypass Controls Regulator input voltage reference noise reduction Low pass filter (BW <5MHz) 1'b0: Regulator reference Low pass filter Mode 1'b1: Bypass Low pass filter (Fast charging)
2:0	RW	0x0	ln1_ana_tx_ser_vreg Choose vref based on VDDH ladder tap points. For VDDH=1.8, Vref=: 3'b000:0.749 3'b001:0.776 3'b010:0.804 3'b011:0.831 3'b100:0.859(default), 3'b101:0.886 3'b110:0.914 3'b111:0.941

USBDPPHY_TRSV_REG060C

Address: Operational Base(0x2B018000) + offset (0x1830)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ln2_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x7	ln2_tx_jeq_even_ctrl_sp TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on

USBDPPHY_TRSV_REG0617

Address: Operational Base(0x2B018000) + offset (0x185C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	ovrd_ln2_tx_ser_vreg_en Override enable flag for ln2_tx_ser_vreg_en
6	RW	0x0	ln2_tx_ser_vreg_en Controls Regulator Enable: 1'b0: Disable regulator (Bypass VDD PMOS switch turns ON) 1'b1: Regulator Enable (Bypass path disables)
5	RW	0x0	ln2_ana_tx_ser_vreg_bypass Force Bypass Regulator: 1'b0: Regulator mode 1'b1: Bypass Regulator and VDD is connected to Regulator node using pass gate
4	RW	0x0	ovrd_ln2_tx_ser_vreg_lpf_bypass Override enable flag for ln2_tx_ser_vreg_lpf_bypass.

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Bit	Attr	Reset Value	Description
3	RW	0x0	ln2_tx_ser_vreg_lpf_bypass Controls Regulator input voltage reference noise reduction Low pass filter (BW <5MHz) 1'b0: Regulator reference Low pass filter Mode 1'b1: Bypass Low pass filter (Fast charging)
2:0	RW	0x0	ln2_ana_tx_ser_vreg Choose vref based on VDDH ladder tap points. For VDDH=1.8, Vref=: 3'b000:0.749 3'b001:0.776 3'b010:0.804 3'b011:0.831 3'b100:0.859(default), 3'b101:0.886 3'b110:0.914 3'b111:0.941

USBDPPHY_TRSV_REG080C

Address: Operational Base(0x2B018000) + offset (0x2030)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ln3_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x7	ln3_tx_jeq_even_ctrl_sp TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on

USBDPPHY_TRSV_REG0817

Address: Operational Base(0x2B018000) + offset (0x205C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	ovrd_ln3_tx_ser_vreg_en Override enable flag for ln3_tx_ser_vreg_en
6	RW	0x0	ln3_tx_ser_vreg_en Controls Regulator Enable: 1'b0: Disable regulator (Bypass VDD PMOS switch turns ON) 1'b1: Regulator Enable (Bypass path disables)
5	RW	0x0	ln3_ana_tx_ser_vreg_bypass Force Bypass Regulator: 1'b0: Regulator mode 1'b1: Bypass Regulator and VDD is connected to Regulator node using pass gate
4	RW	0x0	ovrd_ln3_tx_ser_vreg_lpf_bypass Override enable flag for ln3_tx_ser_vreg_lpf_bypass.

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Bit	Attr	Reset Value	Description
3	RW	0x0	ln3_tx_ser_vreg_lpf_bypass Controls Regulator input voltage reference noise reduction Low pass filter (BW <5MHz) 1'b0: Regulator reference Low pass filter Mode 1'b1: Bypass Low pass filter (Fast charging)
2:0	RW	0x0	ln3_ana_tx_ser_vreg Choose vref based on VDDH ladder tap points. For VDDH=1.8, Vref=: 3'b000:0.749 3'b001:0.776 3'b010:0.804 3'b011:0.831 3'b100:0.859(default), 3'b101:0.886 3'b110:0.914 3'b111:0.941

USBDPPHY_CMN_REG008A

Address: Operational Base(0x2B018000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ana_ropll_cd_hsclk_inv CD output clock polarity inversion 1'b0: No swap 1'b1: P/N swap
5	RW	0x1	ana_ropll_cd_hsclk_west_en CD driver nmos strength control N/A
4	RW	0x1	ana_ropll_cd_hsclk_east_en CD driver pmos strength control N/A
3	RW	0x1	ovrd_ropll_cd_vreg_en Override enable flag for ropll_cd_vreg_en
2	RW	0x0	ropll_cd_vreg_en Controls Regulator Enable: 1'b0: Disable regulator (Bypass VDD PMOS switch turns ON) 1'b1: Regulator Enable (Bypass path disables)
1	RW	0x0	ovrd_ropll_cd_vreg_lpf_bypass Override enable flag for ropll_cd_vreg_lpf_bypass
0	RW	0x0	ropll_cd_vreg_lpf_bypass Controls Regulator input voltage reference noise reduction Low pass filter (BW <5MHz) 1'b0: Regulator reference Low pass filter Mode 1'b1: Bypass Low pass filter (Fast charging)

USBDPPHY_CMN_REG0041

Address: Operational Base(0x2B018000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x77	ana_lcpll_reserved USBDP [7]: i_pll_cd_div2_en_west (default: 0) [6]: i_pll_cd_rstn_sel_west (default: 1) [5:4]: i_pll_cd_hsclk_west_ctrl<1:0> (default: 3) [3]: i_pll_cd_div2_en_east (default: 0) [2]: i_pll_cd_rstn_sel_east (default: 0) [1:0]: i_pll_cd_hsclk_east_ctrl<1:0> (default: 3)

USBDPPHY_CMN_REG0092

Address: Operational Base(0x2B018000) + offset (0x0248)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x77	ana_ropll_reserved USBDP [7]: i_pll_cd_div2_en_west (default: 0) [6]: i_pll_cd_rstn_sel_west (default: 1) [5:4]: i_pll_cd_hsclk_west_ctrl<1:0> (default: 3) [3]: i_pll_cd_div2_en_east (default: 0) [2]: i_pll_cd_rstn_sel_east (default: 0) [1:0]: i_pll_cd_hsclk_east_ctrl<1:0> (default: 3)

USBDPPHY_TRSV_REG021E

Address: Operational Base(0x2B018000) + offset (0x0878)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x04	ln0_ana_tx_reserved Reserved port USBDP Lane0,2 [0] : Driver input data force sel 1'b0: Data force @ driver off state 1'b1: Data force @ srlb_en [1] : Driver input P data @ force mode [2] : Driver input N data @ force mode USBDP Lane 1,3 [0] : Driver input data force sel 1'b0: Data force @ driver off state 1'b1: Data force @ srlb_en

USBDPPHY_TRSV_REG061E

Address: Operational Base(0x2B018000) + offset (0x1878)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x04	ln2_ana_tx_reserved Reserved port USBDP Lane0,2 [0] : Driver input data force sel 1'b0: Data force @ driver off state 1'b1: Data force @ srlb_en [1] : Driver input P data @ force mode [2] : Driver input N data @ force mode USBDP Lane 1,3 [0] : Driver input data force sel 1'b0: Data force @ driver off state 1'b1: Data force @ srlb_en

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USBDPPHY_TRSV_REG0226

Address: Operational Base(0x2B018000) + offset (0x0898)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x7	ln0_rx_cdr_mdiv_sel_pll_sp CDR IQ(main) divider rate control 4'b1111: div16 4'b0111: div8 4'b0011: div4 4'b0001: div2 4'b0000: div1
3:0	RW	0x7	ln0_rx_cdr_mdiv_sel_pll_ssp CDR IQ(main) divider rate control 4'b1111: div16 4'b0111: div8 4'b0011: div4 4'b0001: div2 4'b0000: div1

USBDPPHY_TRSV_REG0626

Address: Operational Base(0x2B018000) + offset (0x189C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x7	ln2_rx_cdr_mdiv_sel_pll_sp CDR IQ(main) divider rate control 4'b1111: div16 4'b0111: div8 4'b0011: div4 4'b0001: div2 4'b0000: div1
3:0	RW	0x7	ln2_rx_cdr_mdiv_sel_pll_ssp CDR IQ(main) divider rate control 4'b1111: div16 4'b0111: div8 4'b0011: div4 4'b0001: div2 4'b0000: div1

USBDPPHY_CMN_REG0015

Address: Operational Base(0x2B018000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:2	RW	0x0	ana_lcpll_avc_cnt_wait_num Number of reference clock cycle to wait VCO clock during AFC
1	RW	0x0	ana_lcpll_avc_en AVC Enable
0	RW	0x1	ana_lcpll_avc_force_en AVC Force Enable

USBDPPHY_CMN_REG0038

Address: Operational Base(0x2B018000) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	ana_lcpll_cd_hsclk_inv CD output clock polarity inversion 1'b0: No swap 1'b1: P/N swap
5	RW	0x1	ana_lcpll_cd_hsclk_west_en CD driver enable to WEST Side clocks
4	RW	0x1	ana_lcpll_cd_hsclk_east_en CD driver enable to EAST Side clocks
3	RW	0x1	ovrd_lcpll_cd_vreg_en Override enable flag for lcpll_cd_vreg_en
2	RW	0x0	lcpll_cd_vreg_en Controls Regulator Enable: 1'b0: Disable regulator (Bypass VDD PMOS switch turns ON) 1'b1: Regulator Enable (Bypass path disables)
1	RW	0x0	ovrd_lcpll_cd_vreg_lpf_pass Override enable flag for lcpll_cd_vreg_lpf_bypass
0	RW	0x0	lcpll_cd_vreg_lpf_bypass Controls Regulator input voltage reference noise reduction Low pass filter (BW <5MHz) 1'b0: Regulator reference Low pass filter Mode 1'b1: Bypass Low pass filter (Fast charging)

USBDPPHY_CMN_REG0018

Address: Operational Base(0x2B018000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:3	RW	0x4	lcpll_ana_cpi_ctrl_coarse PLL integral path charge-pump current contorl 3'b0xx: half current (not used) 3'b100: 1.25uA 3'b101:1.5625uA 3'b110: 20833uA 3'b111: 3.125uA
2:0	RW	0x4	lcpll_ana_cpi_ctrl_fine PLL integral path charge-pump current contorl 3'b0xx: half current (not used) 3'b100: 1.25uA 3'b101:1.5625uA 3'b110: 20833uA 3'b111: 3.125uA

USBDPPHY_CMN_REG0019

Address: Operational Base(0x2B018000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0xf	lcpll_ana_cpp_ctrl_coarse PLL proportional path charge-pump current contorl 3'b000: 66.7uA 3'b001: 75uA 3'b010: 85.7uA 3'b011: 100uA 3'b100: 120uA 3'b101: 150uA 3'b110:200uA 3'b111:300uA

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Bit	Attr	Reset Value	Description
3:0	RW	0xf	lcpll_ana_cpp_ctrl_fine PLL proportional path charge-pump current contorl 3'b000: 66.7uA 3'b001: 75uA 3'b010: 85.7uA 3'b011: 100uA 3'b100: 120uA 3'b101: 150uA 3'b110:200uA 3'b111:300uA

USBDPPHY_CMN_REG001C

Address: Operational Base(0x2B018000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	lcpll_ana_lpf_c_sel_fine PLL loop filter capacitor control 3'b000: 0pF 3'b001: 1pF 3'b010: 2pF 3'b011: 3pF 3'b100: 4pF 3'b101: 5pF 3'b110: 6pF 3'b111: 7pF
3:0	RW	0x6	lcpll_ana_lpf_r_sel_coarse PLL loop filter resistor control 4'b0000: 2K 4'b0001: 4K 4'b0010:6K ~ 4'b1111: 32K

USBDPPHY_CMN_REG008D

Address: Operational Base(0x2B018000) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ropll_beacon_lfps_out_en Override enable flag for ropll_beacon_lfps_out_en
6	RW	0x1	ropll_beacon_lfps_out_en TX beacon clock enable 1'b0: Disable 1'b1: Enable
5	RW	0x1	ana_ropll_misc_clk_sync_en PLL miscellaneous clock synchronization enable If enabled, PLL misc clock output is self synchronized so that clock shape is not affedted by LFPS/beacon enable timing. 1'b0: Disable (async) 1'b1: Enalbe (sync)
4:3	RW	0x1	ana_ropll_misc_clk_sel PLL low-frequency clock output source selection 2'b00: Reference clock 2'b01: Config clock from SoC 2'b10: Internal oscillator clock 2'b11: Divided PLL clock

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Bit	Attr	Reset Value	Description
2	RW	0x0	ana_ropll_ref_clk_mon_en PLL reference clock monitor enable 1'b0: Disable 1'b: Enable
1	RW	0x0	ovrd_ropll_misc_osc_rstn Override enable flag for ropll_misc_osc_rstn
0	RW	0x0	ropll_misc_osc_rstn Self osc reset

USBDPPHY_TRSV_REG02BD

Address: Operational Base(0x2B018000) + offset (0x0AF4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln0_ovrd_rx_rcal_rstn Override enable flag for ln0_rx_rcal_rstn
6	RW	0x0	ln0_rx_rcal_rstn Signal override
5:4	RW	0x1	ln0_rx_rcal_opt_code 2'b00: o_rcal_code = tune_code 2'b01: o_rcal_code = i_sfr_rcal_code 2'b10: o_rcal_code = tune_code + i_sfr_rcal_code 2'b11: o_rcal_code = tune_code - i_sfr_rcal_code
3:0	RW	0x8	ln0_rx_rterm_ctrl Offset to tune_code at opt_code = 2or3

USBDPPHY_TRSV_REG06BD

Address: Operational Base(0x2B018000) + offset (0x1AF4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln2_ovrd_rx_rcal_rstn Override enable flag for ln0_rx_rcal_rstn
6	RW	0x0	ln2_rx_rcal_rstn Signal override
5:4	RW	0x1	ln2_rx_rcal_opt_code 2'b00: o_rcal_code = tune_code 2'b01: o_rcal_code = i_sfr_rcal_code 2'b10: o_rcal_code = tune_code + i_sfr_rcal_code 2'b11: o_rcal_code = tune_code - i_sfr_rcal_code
3:0	RW	0x8	ln2_rx_rterm_ctrl Offset to tune_code at opt_code = 2or3

USBDPPHY_TRSV_REG0267

Address: Operational Base(0x2B018000) + offset (0x099C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	ln0_rx_dfe_vga_rl_ctrl_hbr2 VGA R output value control 3'b000: 600ohm ... 3'b111: 75ohm
4:2	RW	0x2	ln0_rx_dfe_vga_rl_ctrl_hbr3 VGA R output value control 3'b000: 600ohm ... 3'b111: 75ohm

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	ln0_ana_rx_dfe_vga_pbias_ctrl_reserved VGA default current control 2'b00: 1.2mA 2'b01: 1.6mA 2'b10: 2.0mA 2'b11: 2.4mA

USBDPPHY_TRSV_REG0667

Address: Operational Base(0x2B018000) + offset (0x199C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	ln2_rx_dfe_vga_rl_ctrl_hbr2 VGA R output value control 3'b000: 600ohm ... 3'b111: 75ohm
4:2	RW	0x2	ln2_rx_dfe_vga_rl_ctrl_hbr3 VGA R output value control 3'b000: 600ohm ... 3'b111: 75ohm
1:0	RW	0x0	ln2_ana_rx_dfe_vga_pbias_ctrl_reserved VGA default current control 2'b00: 1.2mA 2'b01: 1.6mA 2'b10: 2.0mA 2'b11: 2.4mA

USBDPPHY_TRSV_REG0269

Address: Operational Base(0x2B018000) + offset (0x09A4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln0_ana_rx_rterm_ofsn_ctrl Offset code for RX RTERM N node
5	RW	0x0	ln0_ana_rx_rterm_ofsp_ctrl Offset code for RX RTERM P node 1'b0: No offset added 1'b1: +1 offset code added
4	RW	0x0	ln0_ana_rx_rterm_path_ctrl RX term sw ctrl 1'b0: rtern sw ctrl by"offset_cal_enable" 1'b1: ctrl by "offset_cal_enable" && "rterm_en" --> for DP tx mode
3:0	RW	0x7	reserved

USBDPPHY_TRSV_REG026A

Address: Operational Base(0x2B018000) + offset (0x09A8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RW	0x1	ln0_ana_rx_rterm_incm_vcm_ctrl_reserved reserved
4	RW	0x0	ovrd_ln0_rx_rterm_cm_pulldn_reserved Override enable flag for ln0_rx_rterm_cm_pulldn_reserved
3	RW	0x0	ln0_rx_rterm_cm_pulldn_reserved reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	ovrd_ln0_rx_rterm_vcm_en_reserved Override enable flag for ln0_rx_rterm_vcm_en_reserved
1	RW	0x1	ln0_rx_rterm_vcm_en_reserved reserved
0	RW	0x0	ln0_ana_rx_sq_vref_820m_lpf_bypass_reserved reserved

USBDPPHY_TRSV_REG0669

Address: Operational Base(0x2B018000) + offset (0x19A4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln2_ana_rx_rterm_ofsn_ctrl Offset code for RX RTERM N node
5	RW	0x0	ln2_ana_rx_rterm_ofsp_ctrl Offset code for RX RTERM P node 1'b0: No offset added 1'b1: +1 offset code added
4	RW	0x0	ln2_ana_rx_rterm_path_ctrl RX term sw ctrl 1'b0: rtern sw ctrl by"offset_cal_enable" 1'b1: ctrl by "offset_cal_enable" && "rterm_en" --> for DP tx mode
3:0	RW	0x7	reserved

USBDPPHY_TRSV_REG066A

Address: Operational Base(0x2B018000) + offset (0x19A8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RW	0x1	ln2_ana_rx_rterm_incm_vcm_ctrl_reserved reserved
4	RW	0x0	ovrd_ln2_rx_rterm_cm_pulldn_reserved Override enable flag for ln2_rx_rterm_cm_pulldn_reserved
3	RW	0x0	ln2_rx_rterm_cm_pulldn_reserved reserved
2	RW	0x0	ovrd_ln2_rx_rterm_vcm_en_reserved Override enable flag for ln2_rx_rterm_vcm_en_reserved
1	RW	0x1	ln2_rx_rterm_vcm_en_reserved reserved
0	RW	0x0	ln2_ana_rx_sq_vref_820m_lpf_bypass_reserved reserved

USBDPPHY_TRSV_REG026E

Address: Operational Base(0x2B018000) + offset (0x09B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	ln0_ana_rx_sqhs_th_ctrl_reserved reserved
3	RW	0x1	ln0_ana_rx_sqhs_filter_en SQHS loss detector enable
2:1	RW	0x3	ln0_ana_rx_sqhs_bw_ctrl Not used.
0	RO	0x0	reserved

USBDPPHY_TRSV_REG066E

Address: Operational Base(0x2B018000) + offset (0x19B8)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	ln2_ana_rx_sqhs_th_ctrl_reserved reserved
3	RW	0x1	ln2_ana_rx_sqhs_filter_en SQHS loss detector enable
2:1	RW	0x3	ln2_ana_rx_sqhs_bw_ctrl Not used.
0	RW	0x0	ln2_ana_rx_sqhs_vref_supply_sel Selection of supply voltage of reference voltage for threshold calibration of HS SQ 1'b0: VREG 1'b1: VDD

USBDPPHY_TRSV_REG0279

Address: Operational Base(0x2B018000) + offset (0x09E4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x02	ln0_rx_sslms_c1_init_reserved reserved

USBDPPHY_TRSV_REG0679

Address: Operational Base(0x2B018000) + offset (0x09E8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x02	ln2_rx_sslms_c1_init_reserved reserved

USBDPPHY_TRSV_REG028D

Address: Operational Base(0x2B018000) + offset (0x0A34)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x1	ln0_rx_sslms_rstn RX DFE force Reset 1'b0: Reset 1'b1: Use lane reset
3	RW	0x0	ln0_ovrd_rx_sslms_adap_en_reserved Override enable flag for ln0_rx_sslms_adap_en_reserved
2	RW	0x0	ln0_rx_sslms_adap_en_reserved reserved
1	RW	0x0	ln0_ovrd_rx_sslms_adap_hold_reserved Override enable flag for override enable flag for ln0_rx_sslms_adap_hold_reserved
0	RW	0x0	ln0_rx_sslms_adap_hold_reserved reserved

USBDPPHY_TRSV_REG068D

Address: Operational Base(0x2B018000) + offset (0x1A34)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x1	ln2_rx_sslms_rstn RX DFE force Reset 1'b0: Reset 1'b1: Use lane reset
3	RW	0x0	ln2_ovrd_rx_sslms_adap_en_reserved Override enable flag for ln2_rx_sslms_adap_en_reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	ln2_rx_sslms_adap_en_reserved reserved
1	RW	0x0	ln2_ovrd_rx_sslms_adap_hold_reserved Override enable flag for override enable flag for ln2_rx_sslms_adap_hold_reserved
0	RW	0x0	ln2_rx_sslms_adap_hold_reserved reserved

USBDPPHY_TRSV_REG02A6

Address: Operational Base(0x2B018000) + offset (0x0A98)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	ln0_rx_cdr_fbb_fine_ctrl_sp RX CDR FBB code in PLL Low-BW of CK and Data mode 4'b0000: Min FBB code ... 4'b1111: Max FBB code
3:0	RW	0xf	ln0_rx_cdr_fbb_pll_bw_diff_sp RX CDR FBB offset from FBB-calibrated code in PLL mode 4'b0000: No offset 4'b0001: +1 4'b0010: +2 ~ 4'b1111: Max FBB code

USBDPPHY_TRSV_REG06A6

Address: Operational Base(0x2B018000) + offset (0x1A98)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	ln2_rx_cdr_fbb_fine_ctrl_sp RX CDR FBB code in PLL Low-BW of CK and Data mode 4'b0000: Min FBB code ~ 4'b1111: Max FBB code
3:0	RW	0xf	ln2_rx_cdr_fbb_pll_bw_diff_sp RX CDR FBB offset from FBB-calibrated code in PLL mode 4'b0000: No offset, 4'b0001: +1, 4'b0010: +2, ~ 4'b1111: Max FBB code

USBDPPHY_TRSV_REG030C

Address: Operational Base(0x2B018000) + offset (0x0C30)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x06	ln0_rx_sslms_hf_init_rate_ssp RX DFE SSLMS init value

USBDPPHY_TRSV_REG0312

Address: Operational Base(0x2B018000) + offset (0x0C48)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x03	ln0_rx_sslms_mf_init_rate_ssp RX DFE SSLMS init value

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USBDPPHY_TRSV_REG070C

Address: Operational Base(0x2B018000) + offset (0x1C3C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x06	ln2_rx_sslms_hf_init_rate_ssp RX DFE SSLMS init value

USBDPPHY_TRSV_REG0712

Address: Operational Base(0x2B018000) + offset (0x1C48)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x03	ln2_rx_sslms_mf_init_rate_ssp RX DFE SSLMS init value

USBDPPHY_TRSV_REG06BC

Address: Operational Base(0x2B018000) + offset (0x1AF0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln2_rxd_polarity On normal path, Rx data polarity inversion
6:5	RW	0x0	ln2_rx_sigval_lpf_bypass Low pass filter for removing sigval falling glitchs. 1'b0: Filter enable 1'b1: Filter bypass
4:2	RW	0x7	ln2_tg_rx_sigval_lpf_delay_time N/A
1	RW	0x0	ln2_rx_ctle_eq_mf_man_sel N/A
0	RW	0x1	ln2_rx_ctle_eq_hf_man_sel N/A

15.5 Application Notes

15.5.1 Signal Controlled by GRF and CRU

There is one USBDP PHY in system. The signals need to be controlled by CRU or GRF are list below:

i_rx_lfps_en: USBDPPHY_GRF_CON1[14]
i_init_rstn: PMU1_CRU_SOFTRST_CON00[15]
i_apb_presetn: PMU1_CRU_SOFTRST_CON00[12]
i_pcs_apb_presetn: PMU1_CRU_SOFTRST_CON01[2]
i_cmn_rstn: PMU1_CRU_SOFTRST_CON01[0]
i_lane_rstn: PMU1_CRU_SOFTRST_CON01[1]

15.5.2 Power Sequence Guide

15.5.2.1 Power-Up Sequence

Sequential power-up of 1.8V and 0.85V must be provided to USBDP PHY for proper SerDes operation. Supply voltage of 0.85V must be ramped up first, and supply voltage of 1.8V must be started ramping up after 0.85V supply is completely settled down. Signals i_init_rstn and i_apb_presetn must be asserted after power is fully turned on. Following the release of i_init_rstn, you can access some registers through APB if need and the primary inputs i_cmn_rstn should be set low until the APB programming is finished from initial. After the APB is programmed, the i_cmn_rstn should be released. The signal i_cmn_rstn=0 will cause the PMA's COMMON to turn on. And, the primary input i_lane_rstn will be controlled by Link sub-controller and will be reset in abnormal situation like link-down. PLL locks within 60us after i_cmn_rstn is asserted and o_pll_lock_done goes to high when

the PLL achieves lock. The following figure illustrates the timing restrictions for RESET signals and the typical timing information for the related output signals.

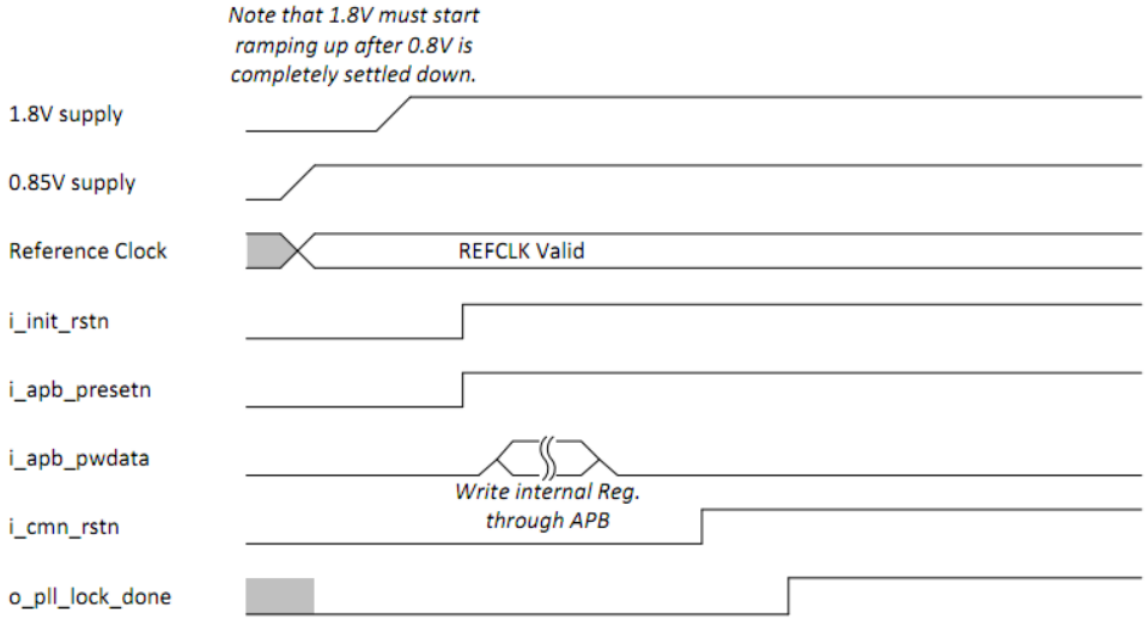


Fig. 15-2 USBDP PHY Power Up Sequence

15.5.2.2 Power-Down Sequence

During power-down (Turning-off supply voltage), supply voltage of 0.85V must start ramping down after supply voltage of 1.8V is completely discharge.

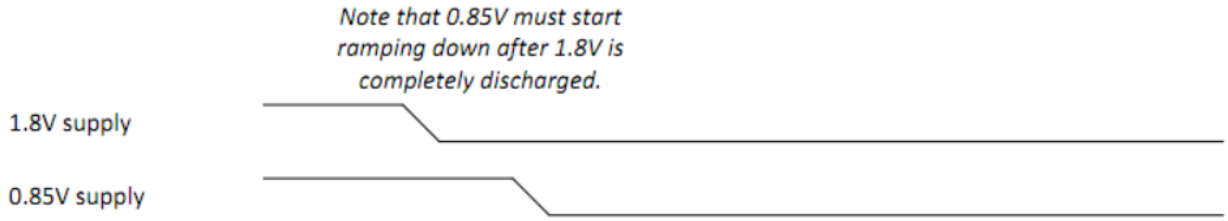


Fig. 15-3 USBDP PHY Power Down Sequence

15.5.3 PHY Initialization Guide

15.5.3.1 USBDP APB Reset Sequence

The USBDP PHY has USB part and DP part. And both parts share the APB Reset. The APB Reset sequence is needed to initialize the USBDP PHY.

Please de-assert USBDP PHY APB Reset when the USBDP PHY is needed to re-initialize like POR (Power-On-Reset, Alt-mode configuration changing).

Please do not de-assert i_apb_presetn when only USB part or DP part initialized.

15.5.3.2 USB LANE0/1, DP LANE2/3 Setting Sequence

When USBDP PHY works, some initial setting should be applicated. The following shows the initialization sequence.

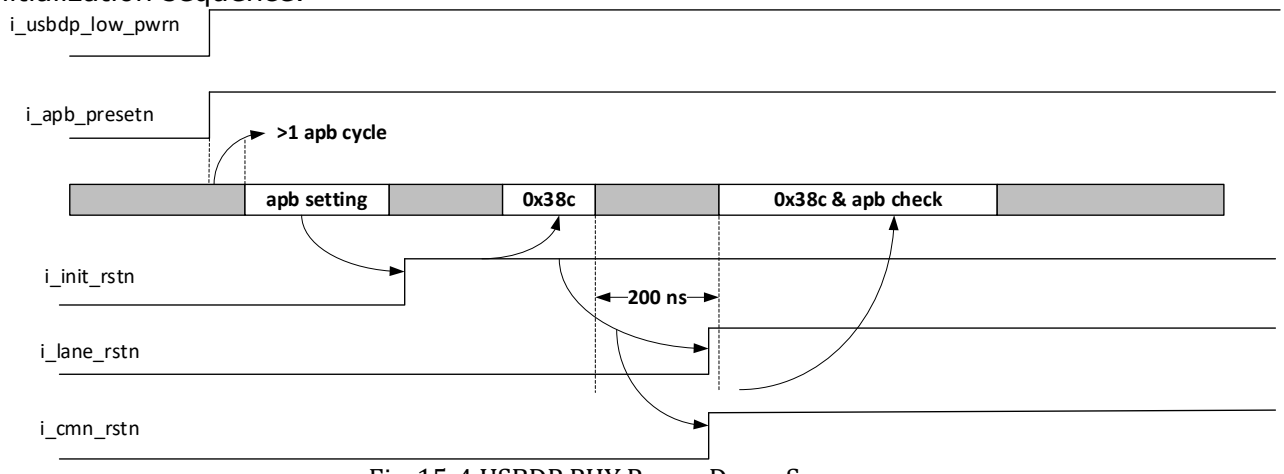


Fig. 15-4 USBDP PHY Power Down Sequence

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Table 15-1 PHY Initialization Sequence

Port / SFR Address	**Write value**			**Read value**
	USB RX0 TX1 DP TX2 TX3	DP TX0 TX1 USB RX2 TX3	DP TX0/TX1/TX2/TX3	
rext	1	1	1	
i_usbdp_low_pwrn	0	0	0	
i_apb_presetn	0	0	0	
WAIT 1 APB_CLK				
i_usbdp_low_pwrn	1	1	1	
i_apb_presetn	1	1	1	
i_lcpll_ref_clk_sel	0	0	0	
i_ropll_ref_clk_Sel	0	0	0	
i_init_rstn	0	0	0	
i_lane_rstn	0	0	0	
i_cmn_rstn	0	0	0	
24M reference clk: 0x0090 0x0094 0x0128 0x012c 0x0130 0x0134 0x015c 0x0160 0x0164 0x0168 0x0174 0x0178 0x017c 0x0180 0x018c 0x0190 0x0194 0x01ac 0x01b0 0x01b4 0x01b8 0x01c8 0x01cc 0x01d0 0x01d4 0x01d8 0x01dc 0x01e0 0x01e4 0x01f0 0x01f4 0x01f8	**24M reference clk:** 0x68 0x68 0x24 0x44 0x3f 0x44 0xa9 0x71 0x71 0xa9 0xa9 0x71 0x71 0xa9 0x41 0x00 0x05 0x2a 0x17 0x17 0x2a 0x04 0x08 0x08 0x04 0x20 0x01 0x09 0x03 0x29 0x02 0x02 0x29		

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Port / SFR Address	Write value			Read value
	USB RX0 TX1 DP TX2 TX3	DP TX0 TX1 USB RX2 TX3	DP TX0/TX1/TX2/TX3	
0x01fc	0x2a			
0x0208	0x17			
0x020c	0x17			
0x0210	0x2a			
0x0214	0x20			
0x0224	0x0d			
0x03f0	0x09			
0x03f4	0x09			
0x03f8	0x0d			
0x03fc	0x0e			
0x0404	0x14			
0x0408	0x14			
0x040c	0x3b			
0x0410	0xd0			
0x0a3c	0xd0			
0x0a44	0x01			
0x0a48	0x0d			
0x0a4c	0xe0			
0x0a54	0xe0			
0x0a5c	0xa8			
0x0a64	0xd0			
0x1a3c	0xd0			
0x1a44	0x01			
0x1a48	0x0d			
0x1a4c	0xe0			
0x1a54	0xe0			
0x1a5c	0xa8			
0x1a64	0x05			
0x0E38	**26M reference clk:**			
26M reference clk:	0x07			
0x0830	0x80			
0x085c	0x07			
0x1030	0x80			
0x105c	0x07			
0x1830	0x80			
0x185c	0x07			
0x2030	0x80			
0x205c	0x38			
0x0228	0x44			
0x0104	0x44			
0x0248	0x02			
0x038C	0x04			
0x0878	0x04			
0x1878	0x77			
0x0898	0x77			
0x1898	0x01			
0x0054	0x38			
0x00e0	0x24			
0x0060	0x77			
	0x76			

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Port / SFR Address	Write value			Read value
	USB RX0 TX1 DP TX2 TX3	DP TX0 TX1 USB RX2 TX3	DP TX0/TX1/TX2/TX3	
0x0064 0x0070 0x0234 0x0AF4 0x1AF4 0x081C 0x181C 0x099C 0x199C 0x09A4 0x09A8 0x19A4 0x19A8 0x09B8 0x19B8 0x09E4 0x19E4 0x0A34 0x1A34 0x0A98 0x1A98 0x0c30 0x0C48 0x1C30 0x1C48 0x028C 0x0AF0 0x1AF0 0x0E38	0xE8 0x15 0x15 0xE5 0xE5 0x48 0x48 0x07 0x22 0x07 0x22 0x3E 0x3E 0x02 0x02 0x1E 0x1E 0x2F 0x2F 0x0E 0x06 0x0E 0x06 0x18 0x00 0x00 0x05			
0x028C	0x14 // RBR 0x34 // HBR 0x54 // HBR2 0x74 // HBR3	0x10 // RBR 0x30 // HBR 0x50 // HBR2 0x70 // HBR3	0x10 // RBR 0x30 // HBR 0x50 // HBR2 0x70 // HBR3	
0x0854 (RBR, HBR) 0x1054 (RBR, HBR)	0x04 0x04	0x06 0x06	0x06 0x06	
0x1854 (RBR, HBR) 0x2054 (RBR,	0x06 0x06	0x04 0x04	0x06 0x06	

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Port / SFR Address	Write value			Read value
	USB RX0 TX1 DP TX2 TX3	DP TX0 TX1 USB RX2 TX3	DP TX0/TX1/TX2/TX3	
HBR)				
0x0854 (HBR2, HBR3) 0x1054 (HBR2, HBR3)	0x04 0x04	0x04 0x04	0x04 0x04	
0x1854 (HBR2, HBR3) 0x2054 (HBR2, HBR3)	0x04 0x04	0x04 0x04	0x04 0x04	
i_init_rstn (when USB used)	1	1	0	
0x038C (when DP used)	0x0A	0x0A	0x0A	
WAIT 200ns				
i_lane_rstn (when USB used)	1	1	0	
i_cmn_rstn (when USB used)	1	1	0	
0x038C (when DP used)	0x0E	0x0E	0x0E	
0x0350 (Check when USB used)			SKIP	0b_11XX_XXXX
0x0354 (Check when DP used)				0b_XXXX_XX11
0x0B84 (Check when USB used)		SKIP	SKIP	0b_XXXX_XXX1
0x1B84 (Check when USB used)	SKIP		SKIP	0b_XXXX_XXX1

15.5.4 SFR Setting for Transmitter

15.5.4.1 Amplitude

Tx amplitude is defined as a differential swing of low-frequency (DC) signal, which is less dependent on off-chip environment, at ln[N]_txdp, ln[N]_txdn, ln[N]_trxdp and ln[N]_trxdn as shown in the following figure. Tx driver amplitude is controlled by two tuning parameters; voltage-mode and current-mode driver amplitude control, respectively.

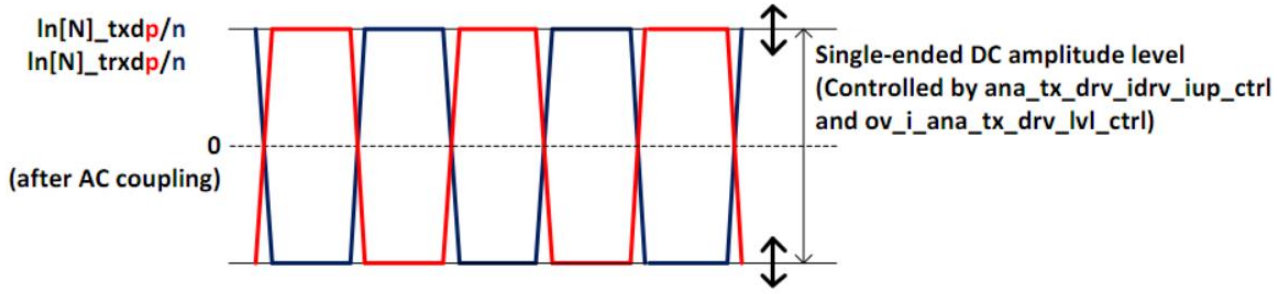


Fig. 15-5 TX DC Amplitude Control

The amplitude of voltage-mode driver can be controlled by either PCS or PMA SFR setting. SFR fields for control consist of override enable and input bits. When override enable is set to high, all following input bits for override are directly applied to Tx voltage mode driver circuit. Due to its own characteristic of voltage-mode driver, the maximum single-ended amplitude of the driver cannot exceed the supply voltage level, VDD (Assuming well-

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matched Tx impedance). Note that the register field for voltage-mode driver swing control is separated into four rate-specific registers and one matched register value is automatically applied according to the data rate under operation. A current-mode driver is implemented to achieve higher voltage swing beyond the limit of voltage-mode drive. In order to activate the current-mode driver, ln_tx_drv_idrv_en must be set to high and ana_tx_drv_idrv_iup_ctrl must be set When the current-mode driver is enabled, extra higher swing can be achieved over VDD.

Table 15-2 Amplitude Control of Voltage-Mode Driver

Name	Address	Code	Description
Override enable for TX Amplitude Contorl	0x0810 0x1010 0x1810 0x2010 Bit[5]	0x1	Override enable for tx_drv_idrv_en
TX Differential Output (TXDP/TXDN) Amplitude Control ln0/1/2/3_tx_drv_lvl_ctrl	0x0810 0x1010 0x1810 0x2010 Bit[4:0]	0xa	1200mV (Max)
		0x0	400 mV
TX Differential Output (TXDP/TXDN) Amplitude Control ln0/1/2/3_tx_drv_idrv_en	0x0818 0x1018 0x1818 0x2018 Bit[0]	0x10	Disable current driver
		0x11	enable current driver
TX Differential Output (TXDP/TXDN) Amplitude Control ln0/1/2/3_ana_tx_drv_idrv_iup_ctrl	0x081C 0x101C 0x181C 0x201C Bit[7:5]	0x0	1200mV (Max)
		0x7	850mV (Min)

15.5.4.2 Equalization

USBDP Combo PHY has 3 tap FIR filter in Tx. De-emphasis function is implemented to reduce the swing of driver when there is no transition (bit change) between current and previous data bit as shown following.

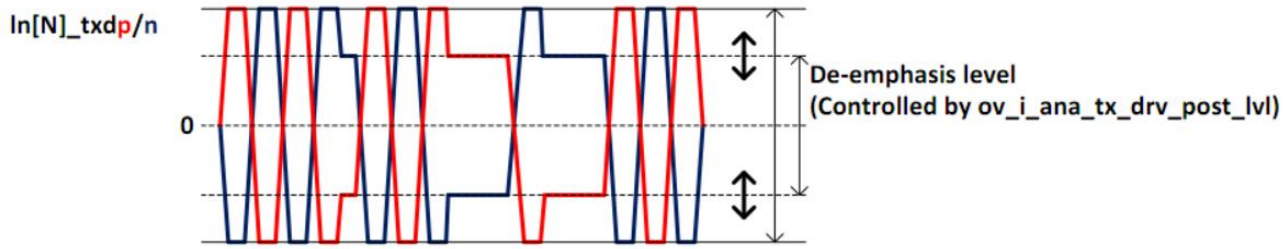


Fig. 15-6 TX De-emphasis Level Control

Table 15-3 SFR Setting for De-emphasis Level Control

Name	Address	Code	Description
TX De-Emphasis Level Control ln0/1/2/3_tx_drv_post_lvl_ctrl	0x0814 0x1014 0x1814 0x2014 Bit[4:0]	00000	-0.5 dB
		00100	– 1.5 dB.
		0100	– 2.8 dB.
		01000	– 4.2 dB.

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Preshoot function is implemented to reduce the swing of driver when there is no transition (bit change) between current and next data bit as shown following

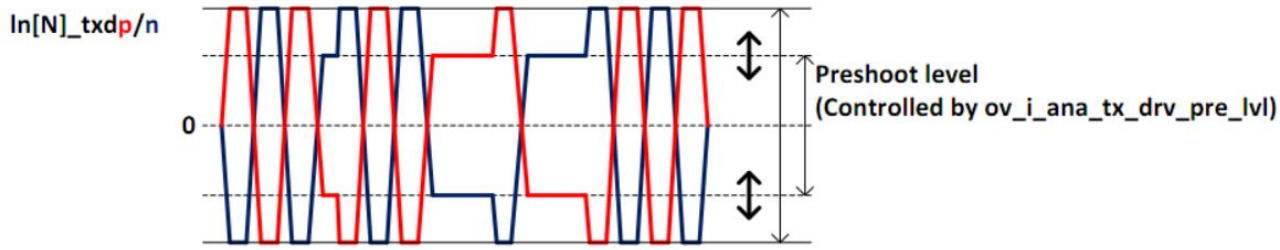


Fig. 15-7 TX Preshoot Level Control

Table 15-4 SFR Setting for Preshoot Level Control

Name	Address	Code	Description
TX Pre-shoot Level Control ln0/1/2/3_tx_drv_pre_lvl_ctrl	0x0818 0x1018 0x1818 0x2018 Bit[5:2]	0000	0 dB Recommend to use over 5 Gbps speed
		0110	– 1.6 dB. Recommend to use over 10 Gbps speed.
		1001	– 6.9 dB. Not recommend to use because main amplitude level is also aggressively reduced.

15.5.4.3 Slew Rate

Slew rate of Tx waveform is able to be controlled by SFR. In order to enable slew-rate control, ana_tx_drv_accdrv_en bit must be set to high. Polarity of slew-rate control is controlled by ana_tx_drv_accdrv_pol_sel_* for each data rate. Tx driver has faster slew rate when this bit is set to high, while slower rate when set to low. Amount of slew rate control is determined by ana_tx_drv_accdrv_ctrl_* for each data rate. Higher value makes Tx driver to have faster slope when ana_tx_drv_accdrv_pol_sel_* is set to high, while higher value makes Tx driver to have slower slope when ana_tx_drv_accdrv_pol_sel_* is set to low.

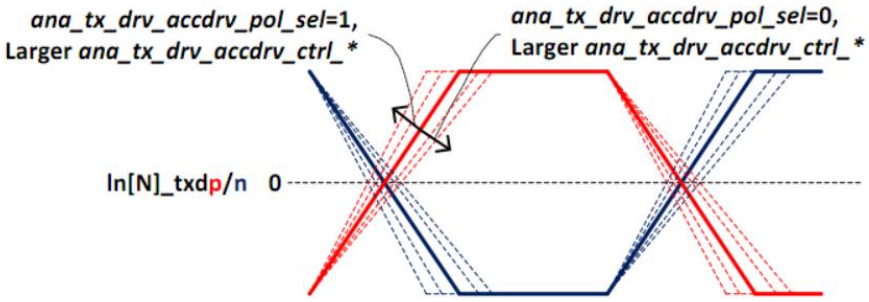


Fig. 15-8 TX Slew-Rate Control

Table 15-5 SFR Setting for Slew Rate Level Control

Name	Address	Code	Description
accdrv_en ln0/1/2/3_ana_tx_drv_accdrv_en	0x081C 0x101C 0x181C 0x201C Bit[1]	0x0	TX AC-coupled driver enable for slew rate control Disable
		0x1	TX AC-coupled driver enable for slew rate control

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Name	Address	Code	Description
			Enable
accdrv_pol_sel ln0/1/2/3_ana_tx_drv_accdrv_pol_sel	0x081C 0x101C 0x181C 0x201C Bit[0]	0x1	Faster slew rate
		0x0	Slower slew rate
drv_accdrv_ctrl ln0/1/2/3_ana_tx_ drv_accdrv_ctrl	0x0820 0x1020 0x1820 0x2020 Bit[5:3]	0x7	TX AC-coupled driver Max Strength
		0x0	TX AC-coupled driver Min Strength

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Chapter 16 SATA Host

16.1 Overview

SATA Host implements the Serial Advanced Technology Attachment (SATA) storage interface for physical storage devices.

SATA Host supports the following features:

- Include 2 controller , each controller have a port, and each port can connect up to 15 devices using PM switching
- SATA 1.5Gb/s, SATA 3.0Gb/s, SATA 6.0Gb/s speeds
- eSATA
- Compliant with Serial ATA 3.1 specifications
- Compliant with AHCI Revision 1.3.1
- OOB signaling detection and generation
- Digital support of Mechanical presence switch and cold presence detect
- Activity LED support
- Digital support of device hot-plugging
- Output port to indicate speed that is negotiated after COMRESET for power optimization
- Memory Data Protection (ECC) and Error Correction (ECC)
- Memory Data Protection Diagnostic Error Injection
- SATA 1.5Gb/s, SATA 3.0Gb/s, and SATA 6.0Gb/s speed negotiation
- Asynchronous signal recovery, including retry polling
- Power management features including automatic partial-to-slumber transition
- BIST loopback modes
- Hardware-assisted Native Command Queuing for up to 32 entries
- Port Multiplier with FIS-based switching
- Disabling RX and TX Data clocks during power down modes
- Any sector sizes
- AXI slave interface used for configuration only support single
- AXI master interface used to fetch data from memory

16.2 Block Diagram

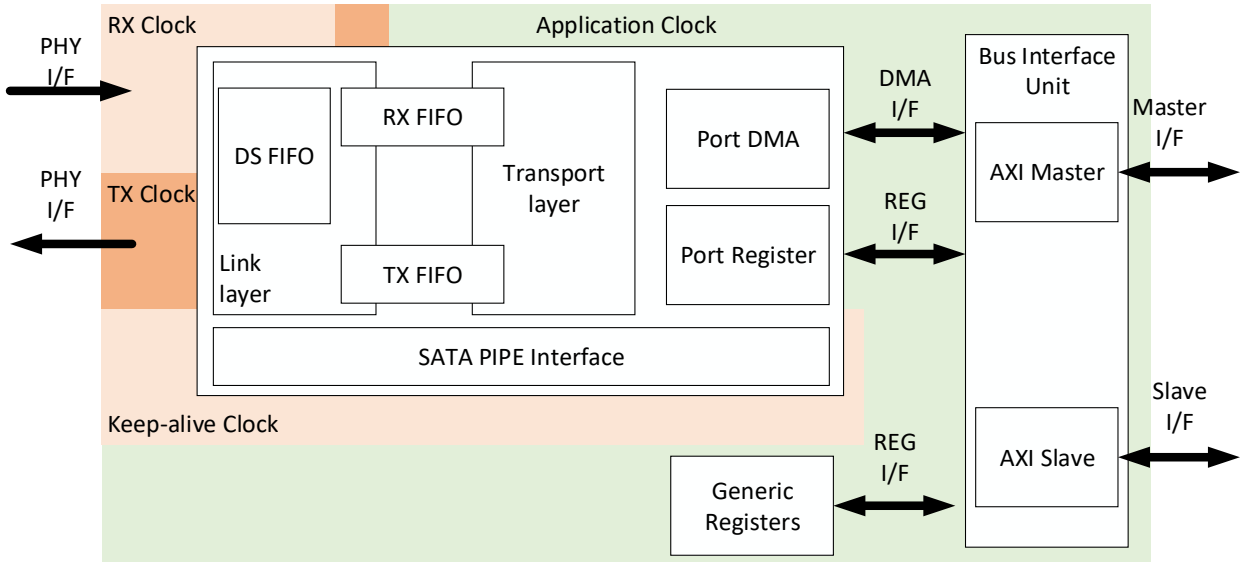


Fig. 16-1 SATA host Architecture

16.3 Function Description

16.3.1 Bus Interface Unit (BIU)

The Bus Interface Unit provides two interfaces:
AXI Master - This interface enables the SATA AHCI DMA engine to read and write to an AXI

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slave connected to AXI BIU.
AXI Slave - This interface enables an AXI master to read and write through the AXI BIU to the SATA AHCI registers.

16.3.2 Generic Registers (GCSR)

This module implements all global registers and provides the following functions:

- Generic configuration and control
- Global interrupt support
- BIST operation

16.3.3 Port Registers (PCSR)

The port registers module implements all Port-specific registers:

- Command list and FIS Based address
- Interrupt status/enable
- Port command/status
- Task file data/signature/serial ATA
- DMA status/control

16.3.4 Port DMA(PDMA)

This module performs the following functions:

- Monitors commands posted by system software using the CI register
- Control data transfer between the Transport layer FIFOs and system memory using Physical Region Descriptor Table (PRDT)
- Transfers non-Data FISes received from the device to system memory using Received FIS Structure

Most of the communication between the PDMA and software is done using two system memory descriptors that are constructed by software prior to initiating the transfer: FIS descriptor, which contains FISes received from that device; and the command list, which contains a list of 1 to 32 commands available for Port to execute and the pointers for data transfers. Some additional communication is done by registers located in the GCSR and PCSR modules.

System memory structures are described in the SATA AHCI specification and are not repeated in this document.

The PDMA module operates in the application clock(aclk) domain.

16.3.5 Port Transport layer

The transport layer block provides FIS reception and transmission functions of the SATA transport layer. It operates in two clock domains: transmit and application. During reception, the transport layer receives a new FIS from the link layer through the RX FIFO, decodes the FIS type, and instructs the PDMA to route the FIS payload data to the appropriate location in system memory. During transmission, the transport layer instructs the PDMA to construct the appropriate FIS, and then passes it to the link layer through the TX FIFO. The transport layer block receives all the PHY/Link errors from the link layer, detects transport errors and passes them to the PCSR for setting the corresponding error bits.

The transport layer processes one FIS at time on the transmit side, meaning only one FIS is allowed in the TX FIFO at a time. On the receive side, RX FIFO can potentially contain more than one FIS at a time. For example, when the device transmits several DMA data FISes back-to-back with minimal delay, the RX FIFO still has the previous Data FIS while the next FIS is being received. The transport layer also contains a small internal eight-DWORD RX FIFO1 that is used for non-data FISes and FIS "End Status."

16.3.6 Port Link layer

This module optional OOB signaling, system initialization, speed negotiation, frame negotiation and arbitration, envelope framing/de-framing, CRC calculating, insertion and checking, flow control, frame acknowledgement and status reporting, data scrambling/de-scrambling for EMI reduction, repeat primitive data transmission and reception handling, ALIGN primitive detection, dropping and data alignment and power management.

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16.4 Register Description

16.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SATA0	0x2A240000
SATA1	0x2A250000

16.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SATA_CAP	0x0000	W	0xE737FF80	This register indicates basic capabilities of the SATA Host to the software.
SATA_GHC	0x0004	W	0x80000000	This register controls various global actions of the SATA Host.
SATA_IS	0x0008	W	0x00000000	This register indicates which of the ports within the SATA Host have an interrupt pending and require service
SATA_PI	0x000C	W	0x00000000	This register indicates which ports are exposed by the SATA Host and are available for the software to use. It is loaded before OS boot.
SATA_VS	0x0010	W	0x00010300	This register indicates the major and minor version of the AHCI specification that the SATA Host implementation supports. The SATA Host supports version 1.3.0
SATA_CCC_CTL	0x0014	W	0x00010108	This register is used to configure the command completion coalescing (CCC) feature for the SATA Host.
SATA_CCC_PORTS	0x0018	W	0x00000000	This register specifies the ports that are coalesced as part of the command completion coalescing (CCC) feature.
SATA_CAP2	0x0024	W	0x00000004	This register indicates capabilities of the SATA Host to the software.
SATA_BISTAFR	0x00A0	W	0x00000000	This register contains the pattern definition and data pattern fields of the received BIST Activate FIS.

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Name	Offset	Size	Reset Value	Description
SATA_MEMEDRXFERRCNT	0x00A0	W	0x00000000	ECC/Parity RX FIFO RAM Error Count Register. To access this register for a given port, software must first select the port by writing the port number to the TESTR.PSEL field, along with setting TESTR_BSEL to 2'b01.
SATA_BISTCR	0x00A4	W	0x00007700	This register is used in BIST initiator modes and for general PHY/Link control. It is loaded by the host software prior to sending BIST Activate FIS to the device.
SATA_MEMEDRXFERRDATA	0x00A4	W	0x00000000	RX FIFO RAM Data ECC/Parity Error Location and Syndrome Register. To access this register for a given port, software must first select the port by writing the port number to the TESTR.PSEL field, along with setting TESTR_BSEL to 2'b01.
SATA_BISTFCTR	0x00A8	W	0x00000000	This register contains the received BIST FIS count in the loopback initiator Far-end Retimed, Far-end Analog and Near-end Analog modes.
SATA_MEMEDTXFERRCNT	0x00A8	W	0x00000000	ECC/Parity TX FIFO RAM Error Count Register. To access this register for a given port, software must first select the port by writing the port number to the TESTR.PSEL field, along with setting TESTR_BSEL to 2'b01.
SATA_BISTSR	0x00AC	W	0x00000000	This register contains errors detected in the received BIST FIS in the loopback initiator Far-end Retimed, Far-end Analog and Near-end Analog modes. It is updated each time a new BIST FIS is received.

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Name	Offset	Size	Reset Value	Description
SATA_MEMEDTXFERRDATA	0x00AC	W	0x00000000	TX FIFO RAM Data ECC/Parity Error Location and Syndrome Register. To access this register for a given port, software must first select the port by writing the port number to the TESTR.PSEL field, along with setting TESTR_BSEL to 2'b01.
SATA_MEMEDFBSERRCNT	0x00B0	W	0x00000000	ECC/Parity FBS RAM Data Error Count Register. To access this register for a given port, software must first select the port by writing the port number to the TESTR.PSEL field, along with setting TESTR_BSEL to 2'b01.
SATA_BISTDECR	0x00B0	W	0x00000000	This register contains the number of DWORD errors detected in the received BIST frame in the loopback initiator Far-end Retimed, Far-end Analog and Near-end Analog modes. It is updated each time a new BIST frame is received.
SATA_MEMEDFBSERRDATA	0x00B4	W	0x00000000	FBS RAM Data ECC/Parity Error Location and Syndrome Register. To access this register for a given port, software must first select the port by writing the port number to the TESTR.PSEL field, along with setting TESTR_BSEL to 2'b01.
SATA_MEMEDERRINJ	0x00B8	W	0x00000000	ECC/Parity Error Detction Status and Error Injection Register. To access this register for a given port, software must first select the port by writing the port number to the TESTR.PSEL field, along with setting TESTR_BSEL to 2'b01.

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Name	Offset	Size	Reset Value	Description
SATA_MEMEDRXFERRDATAU	0x00BC	W	0x00000000	RX FIFO RAM Data Parity Error Syndrome Upper Bits Register. To access this register for a given port, software must first select the port by writing the port number to the TESTR.PSEL field, along with setting TESTR_BSEL to 2'b01.
SATA_OOBR	0x00BC	W	0x00000000	This register controls the Link layer OOB detection counters. The default values, MIN_COMWAKE, MAX_COMWAKE, MIN_COMINIT and MAX_COMINIT are calculated based on the RXOOB_CLK_FREQ parameter and loaded on power-up or asynchronous SATA Host reset.
SATA_MEMEDTXFERRDATAU	0x00C0	W	0x00000000	TX FIFO RAM Data Parity Error Syndrome Upper Bits Register. To access this register for a given port, software must first select the port by writing the port number to the TESTR.PSEL field, along with setting TESTR_BSEL to 2'b01.
SATA_DIAGNR3	0x00C4	W	0x00000000	DIAGNR3
SATA_MEMEDFBSERRDATAU	0x00C4	W	0x00000000	FBS RAM Data Parity Error Syndrome Upper Bits Register. To access this register for a given port, software must first select the port by writing the port number to the TESTR.PSEL field, along with setting TESTR_BSEL to 2'b01.
SATA_TIMER1MS	0x00E0	W	0x000493E0	This register is used to generate a 1-ms tick for the command completion coalescing (CCC) or DevSleep logic, based on the AMBA bus clock frequency.
SATA_MEMDPCR	0x00E4	W	0x00000000	This register is used to control the various options associated with the Data protection (ECC/Parity) and Address protection (Parity) functionality.

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Name	Offset	Size	Reset Value	Description
SATA_TESTR	0x00F4	W	0x00000000	This register is used to put the SATA Host slave interface into a test mode and to select a Port for BIST operation.
SATA_VERSION	0x00F8	W	0x3530302A	This 32-bit read-only register contains hard-coded hexadecimal SATA Host component version value.
SATA_IDR	0x00FC	W	0x00000000	This register contains a hard-coded hexadecimal SATA Host identification value, as determined by the configuration parameter External User Core ID Port.
SATA_P0CLB	0x0100	W	0x00000000	Port Command List Base Address Register
SATA_P0CLBU	0x0104	W	0x00000000	Port Command List Base Address Upper 32-Bits Register
SATA_P0FB	0x0108	W	0x00000000	Port FIS Base Address Register
SATA_P0FBU	0x010C	W	0x00000000	Port FIS Base Address Upper 32-Bits Register
SATA_P0IS	0x0110	W	0x00000000	Port Interrupt Status Register.
SATA_P0IE	0x0114	W	0x00000000	Port Interrupt Enable Register.
SATA_P0CMD	0x0118	W	0x00000000	Port Command Register. This register contains bits controlling various Port functions.
SATA_P0TFD	0x0120	W	0x00007F00	Port Task File Data Register. This register contains Error and Status registers updated every time a new Register FIS, PIO Setup FIS, or Set Device Bits FIS is received from the device.
SATA_P0SIG	0x0124	W	0xFFFFFFFF	Port Signature Register
SATA_P0SSTS	0x0128	W	0x00000000	Port Serial ATA Status (SStatus) Register. This 32-bit register conveys the current state of the interface and host. The Port updates it continuously and asynchronously. When the Port transmits a COMRESET to the device, this register is updated to its reset values (such as, Global reset, Port reset, or device disconnect ('PHY Ready' negation)).

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Name	Offset	Size	Reset Value	Description
SATA_P0SCTL	0x012C	W	0x00000000	Port Serial ATA Control Register. This 32-bit read-write register is used by the software to control SATA interface capabilities. Writes to this register result in an action being taken by the Port PHY interface. Reads from the register return the last value written to it. Reset on Global reset.
SATA_P0SERR	0x0130	W	0x00000000	Port Serial ATA Error Register. This 32-bit register represents all the detected interface errors accumulated since the last time it was cleared.
SATA_P0SACT	0x0134	W	0x00000000	Port Serial ATA Active Register
SATA_P0CI	0x0138	W	0x00000000	Port Command Issue Register
SATA_P0SNTF	0x013C	W	0x00000000	Port Serial ATA Notification Register. This register is used to determine when asynchronous notification events have occurred for directly connected devices and devices connected to a Port Multiplier.
SATA_P0FBS	0x0140	W	0x00000000	Port FIS-Based Switching Control Register. This register is used to control and obtain status for Port Multiplier FIS-based switching.
SATA_P0DMACR	0x0170	W	0x00000044	Port DMA Control Register. This register contains bits for controlling the Port DMA engine. The software can change the fields of this register only when P0CMD.ST=0. This register is reset to its default value on power-up (system reset) only.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

16.4.3 Detail Registers Description

SATA_CAP

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x1	s64a Supports 64-bit addressable data structures by utilizing P0FBU and P0CLBU registers.

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Bit	Attr	Reset Value	Description
30	RO	0x1	sncq Supports SATA native command queuing by handing DMA Setup FIS natively.
29	RO	0x1	ssntf Supports P0SNTF (SNotification) register and its associated functionality.
28	RW	0x0	smps This bit is set by the system firmware/BIOS when platform supports mechanical presence for hot plug operation.
27	RW	0x0	sss This bit is set by the system firmware/BIOS to indicate platform support for staggered devices' spin-up. SATA Host supports this feature through the P0CMD.SUD bit functionality.
26	RO	0x1	salp Supports auto-generating Link Layer requests to the PARTIAL or SLUMBER power management states when there are no commands to process.
25	RO	0x1	sal Supports activity indication using signal P0_act_led.
24	RO	0x1	sclo Supports the P0CMA.CLO bit functionality for Port Multiplier devices' enumeration.
23:20	RO	0x3	iss Supports SATA 1.5Gb/s, SATA 3Gb/s, SATA 6Gb/s interface speeds.
19	RO	0x0	snzo This feature is not supported.
18	RO	0x1	sam Supports AHCI mode only and does not supports legacy, task-file based register interface.
17	RO	0x1	spm Supports command-based switching Port Multiplier on any of its ports.
16	RO	0x1	fbss FIS-Based Switching supported.
15	RO	0x1	pmd Supports multiple DRQ block data transfer for the PIO command protocol.
14	RO	0x1	ssc Supports transitions to the interface SLUMBER power management state.
13	RO	0x1	psc Supports transitions to the interface PARTIAL power management state.

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Bit	Attr	Reset Value	Description
12:8	RO	0x1f	ncs Supports 32 command slots per Port.
7	RO	0x1	cccs Command Completion Coalescing Supported
6	RO	0x0	ems SATA Host does not support enclosure management.
5	RO	0x0	sxs The options for this field are: 1'h0: Indicates that the SATA Host has no ports that have a signal only connector externally accessible; 1'h1: Indicates that the SATA Host has one or more ports that has a signal only connector (power is not part of that connector) that is externally accessible. When this bit is set to 1, the software can refer to the P0CMD.ESP bit to determine whether a specific Port has its signal connector externally accessible.
4:0	RO	0x00	np Indicating the numbers of ports supported by the SATA Host.

SATA_GHC

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RO	0x1	ae This bit is always set since SATA Host supports only AHCI mode as indicated by the CAP.SAM=1.
30:2	RO	0x00000000	reserved
1	RW	0x0	ie This global bit enables interrupts from the SATA Host. When cleared, all interrupt sources from all the ports are disabled. When set, interrupts are enabled and ant SATA Host interrupt event caused intrq assertion.
0	WO	0x0	hr When set by the software, this bit causes an internal Global reset of the SATA Host. All state machines that relate to data transfers and queuing return to and idle state, and all the ports are re-initialized by sending COMRESET when staggered spin-up is not supported. When staggered spin-up is supported, then the software must spin-up each port after this reset has complete.

SATA_IS

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	ips When set, this bit indicates that the corresponding Ports or Command Completion Coalescing logic has an interrupt pending. The software can use this information to determine which ports require service after an interrupt. The bits of this field are set by the ports that have interrupt events pending in the P0IS bits and enabled by the P0IE or CCC interrupt is generated. Set bits are cleared by the software writing 1 to all bits to clear.

SATA_PI

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	pi This register is bit significant. 1'h0: The Port is not available for the software to use; 1'h1: The corresponding Port is available for the software to use.

SATA_VS

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0001	mjr Indicates that the major AHCI version is 1.
15:0	RO	0x0300	mnr Indicates that the minor AHCI version is 30 or 31.

SATA_CCC_CTL

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0001	tv This field specifies the CCC time-out value in 1ms intervals. The software loads this value prior to enabling CCC.
15:8	RW	0x01	cc This field specifies the number of command completions that are necessary to cause a CCC interrupt. The value 8'h00 for this field disables CCC interrupts being generated based on the number of commands completed. In this case, CCC interrupts are only generated based on the timer.
7:3	RO	0x01	intr_int This field specifies the interrupt used by the ccc feature, using the number of ports configured for the core.
2:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	en The options for this field are: 1'h0: CCC feature is disabled and no CCC interrupts are generated; 1'h1: CCC feature is enabled and CCC interrupts may be generated based on the time-out or command completion conditions.

SATA_CCC_PORTS

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	prt This field is bit significant. Each bit corresponds to a particular Port, where bit 0 corresponds to Port0.The options for this field are: 1'h0: The corresponding Port is not part of the CCC feature. 1'h1: The corresponding Port is part of the CCC feature. Bits set in this register must also have the corresponding bit set in the PI (Ports Implemented Register).

SATA_CAP2

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	deso SATA Host supports DevSleep entrance from any Link state (active, Partial, or Slumber).
4	RO	0x0	sadm SATA Host supports hardware assertion of the P0_phy_devslp output after the idle timer expires.
3	RO	0x0	sds SATA Host supports hardware assertion of the P0_phy_devslp output after the idle timer expires.
2	RO	0x1	apst Automatic Partial to Slumber Transitions
1	RO	0x0	nvmp SATA Host does not support NVMHCI.
0	RO	0x0	boh SATA Host does not support BOH.

SATA_BISTAFR

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	ncp Least significant byte of the received BIST Activate FIS second DWORD (bits [7:0]). This value defines the required pattern for Far-end transmit only mode (BISTAFR.PD=0xC0 or 0xE0): 8'h4A: High frequency test pattern (HFTP); 8'h78: Mid frequency test pattern (MFTP); 8'h7E: Low frequency test pattern (LFTP); 8'h7F: Simultaneous switching outputs pattern (SSOP); 8'hAB: Low frequency spectral component pattern (LFSCP); 8'hB5: High transition density pattern (HTDP); 8'hF1: Low transition density pattern (LTDP). When none of these values is decoded, the Lone bit pattern (LBP) is transmitted by default.
7:0	RO	0x00	pd Indicates the pattern definition field of the received BIST Activate FIS - bits [23:16] of the first DWORD. It is used to put the SATA Host in one of the following BIST modes: 8'h08: Far-end Analog (when PHY supports this mode); 8'h10: Far-end Retimed; 8'hC0: Far-end Transmit only; 8'hE0: Far-end Transmit only with scrambler bypassed. All other values should not be used by the device, otherwise, the FIS is negatively acknowledged with R_ERRp. For Far-end Transmit only modes BISTAFR.NCP field contains the required data pattern.

SATA_MEMEDRXFERRCNT

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	mem_rxf_corr_err_cnt RX FIFO Corrected RAM Data Error Count.
7:0	RO	0x00	mem_rxf_uncorr_err_cnt RX FIFO Uncorrected RAM Data Error Count.

SATA_BISTCR

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x0	old_phy_ready Old phy_ready

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Bit	Attr	Reset Value	Description
24	RO	0x0	late_phy_ready When set, this bit changes monitoring of phy_ready to be the "OR" of phy_ready or phy_rx_data_vld so that a "late arriving", or even "never asserting" phy_ready. This requires that phy_rx_data_vld does not become valid until after the PHY has locked onto post OOB incoming ALIGNs, and the ALIGNs are valid from the PHY. This will not work if phy_rx_data_vld is asserted during OOB data bursts. This behavior is intended for PHYs that assert phy_ready late, but will also work if phy_ready never asserts or is not present.
23:21	RO	0x0	reserved
20	WO	0x0	ferlb When set, this bit is used to put the SATA Host Link into Far-end Retimed mode, without the BIST Activate FIS, regardless whether the device is connected or disconnected (Link in NOCOMM state). This field is one-shot type and reads returns 0.
19	RO	0x0	reserved
18	WO	0x0	txo This bit is used to initiate transmission of one of the non-compliant patterns defined by the BISTCR.PATTERN value when the device is disconnected.
17	WO	0x0	cntclr This bit clears BIST error count registers. This field is one-shot type and reads returns 0. 1'h1: Clear BISTFCTR, BISTSR, and BISTDECR registers.
16	WO	0x0	nearlb This bit places the Port PHY into Near-end Analog loopback mode. This field is one-shot type and reads returns 0. 1'h0: Near-end Analog loopback disabled; 1'h1: Near-end Analog loopback request. BISTCR.PATTERN field contains the appropriate pattern. This mode should be initiated either in the PARTIAL or SLUMBER power mode, or with the device disconnected from the Port PHY (Link NOCOMM state). BIST Activate FIS is not sent to the device in this mode.
15	RW	0x0	llb When set, masks out phy_sig_det from the OOB Detector in BIST Loopback Mode, and the only way to exit BIST Loopback mode is to clear the register bit (requires access to the Device AMBA register interface), then issue COMRESET or receive COMINIT as normal. Alternately, a power on reset will automatically clear the BIST Loopback Mode register bit.

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Bit	Attr	Reset Value	Description
14	RO	0x1	qphyinit When set, this bit enables quick PHY initialization feature. The Link does not require any ALIGNs to transition from OOB to normal operation.
13	RW	0x1	errlossen This bit is cleared until it is set via programming.
12	RW	0x1	sdfe This bit is cleared until it is set via programming. It is not affected by a Global reset or COMRESET.
11	RO	0x0	reserved
10:8	RW	0x7	llc This field controls the Port Link Layer functions: scrambler, de-scrambler, and repeat primitive drop. Note the different meanings for normal and BIST modes of operation: Bit 8 - SCRAM The options for this field are: 1'h0: Scrambler disabled in normal mode, enabled in BIST mode; 1'h1: Scrambler enabled in normal mode, disabled in BIST mode. Bit 9 - DESCRAM The options for this field are: 1'h0: Descrambler disabled in normal mode, enabled in BIST mode; 1'h1: Descrambler enabled in normal mode, disabled in BIST mode. Bit 10 - RPD The options for this field are: 1'h0: Repeat primitive drop function disabled in normal mode, NA in BIST mode; 1'h1: Repeat primitive drop function enabled in normal mode, NA in BIST mode. The SCRAM bit is cleared (enabled) by the Port when the Port enters a responder far-end transmit BIST mode with scrambling enabled (BISTAFR.PD=0xC0). In normal mode, the functions scrambler, descrambler, or RPD can be changed only during Port reset (P0SCTL.DET=0x1)
7	RO	0x0	reserved
6	RW	0x0	erren This bit is used to allow or filter (disable) PHY internal errors outside the FIS boundary to set corresponding P0SERR bits. The options for this field are: 1'h0: Filter errors outside the FIS, allow errors inside the FIS; 1'h1: Allow errors outside or inside the FIS.
5	RW	0x0	flip This bit is used to change disparity of the current test pattern to the opposite every time its state is changed by the software.

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Bit	Attr	Reset Value	Description
4	RW	0x0	pv This bit is used to select either short or long version of the SSOP, HTDP, LTDP, LFSCP, COMP patterns. The options for this field are: 1'h0: Short pattern version; 1'h1: Long pattern version.
3:0	RW	0x0	pattern This field defines one of the following SATA-compliant patterns for Far-end Retimed/Far-end Analog/Near-end Analog initiator modes, or non-compliant patterns for Transmit-only responder mode when initiated by the software writing to the BISTCR.TXO bit. The options for this field are: 4'h0: Simultaneous switching outputs pattern (SSOP); 4'h1: High transition density pattern (HTDP); 4'h2: Low transition density pattern (LTDP); 4'h3: Low frequency spectral component pattern (LFSCP); 4'h4: Composite pattern (COMP); 4'h5: Lone bit pattern (LBP); 4'h6: Mid frequency test pattern (MFTP); 4'h7: High frequency test pattern (HFTP); 4'h8: Low frequency test pattern (LFTP). All other values are reserved and should not be used. If the value is none of the listed previously, Composite pattern (COMP) is transmitted by default.

SATA_MEMEDRXFERRDATA

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	mem_rxf_err_synd This field logs the error syndrome of the RAM Data Ecc/Parity error, if the syndrome width excess the range of the filed MEMEDRXFERRDATA.mem_rxf_err_synd, extra bits is logged in another register MEMEDRXFERRDATAU.mem_rxf_err_synd_u.
11:0	RO	0x000	mem_rxf_err_addr This filed logs the error location (the address of which the RAM data Ecc/Parity error detected).

SATA_BISTFCTR

Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	count Received BIST FIS Count

SATA_MEMEDTXFERRCNT

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Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	mem_txf_corr_err_cnt TX FIFO Corrected RAM Data Error Count.
7:0	RO	0x00	mem_txf_uncorr_err_cnt TX FIFO Uncorrected RAM Data Error Count.

SATA_BISTSR

Address: **Operational Base** + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	brsterr This field contains the burst error count. It is accumulated each time a burst error condition is detected: DWORD error is detected in the received frame and 1.5 seconds (27,000 frames) passed since the previous burst error was detected.
15:0	RO	0x0000	framerr This field contains the frame error count. It is accumulated (new value is added to the old value) each time a new BIST frame with a CRC error is received.

SATA_MEMEDTXFERRDATA

Address: **Operational Base** + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	mem_txf_err_synd This field logs the error syndrome of the RAM Data Ecc/Parity error, if the syndrome width excess the range of the filed MEMEDTXFERRDATA.mem_txf_err_synd, extra bits is logged in another register MEMEDTXFERRDATAU.mem_txf_err_synd_u.
11:0	RO	0x000	mem_txf_err_addr This filed logs the error location (the address of which the RAM data Ecc/Parity error detected).

SATA_MEMEDFBSERRCNT

Address: **Operational Base** + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	mem_fbs_corr_err_cnt FBS Corrected RAM Data Error Count.
7:0	RO	0x00	mem_fbs_uncorr_err_cnt FBS Uncorrected RAM Data Error Count.

SATA_BISTDECR

Address: **Operational Base** + offset (0x00B0)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dwerr This field contains the DWORD error count. It is accumulated (new value is added to the old value) each time a new BIST frame is received.

SATA_MEMEDFBSERRDATA

Address: **Operational Base** + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	mem_fbs_err_synd This field logs the error syndrome of the RAM Data Ecc/Parity error, if the syndrome with excess the range of the filed MEMEDFBSERRDATA.mem_fbs_err_synd, extra bits is logged in another register MEMEDFBSERRDATAU.mem_fbs_err_synd_u.
11:0	RO	0x000	mem_fbs_err_addr This filed logs the error location (the address of which the RAM data Ecc/Parity error detected)

SATA_MEMEDERRINJ

Address: **Operational Base** + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	ued Indicates a single bit uncorrected, or multiple bit error was detected. Cleared by writing '1' to this field.
16	RW	0x0	ced Indicates a single bit error was corrected. Cleared by writing '1' to this field.
15:5	RO	0x000	reserved
4	RW	0x0	oneB_2B When MEM_DP_TYPE=1 (Parity), only single-bit error injection is allowed in Parity mode and hence the value programmed in this bit is 'don't care'.
3	RW	0x0	cont Selects 'one-shot' (0) or 'continuous' (1) errors
2:1	RW	0x0	mem_sel 2'h0: All three memory interfaces; 2'h1: RX FIFO Memory; 2'h2: TX FIFO Memory; 2'h3: FBS RAM.
0	RW	0x0	err_inj_valid The values in the rest of the fields of this register are valid only when this bit is set to 1.

SATA_MEMEDRXFERRDATAU

Address: **Operational Base** + offset (0x00BC)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mem_rxf_err_synd_u When the RX FIFO RAM Data parity error syndrome width excess the range of the register MEMEDRXFERRDATA.mem_rx_err_synd, extra bits is logged in this field.

SATA_OOBR

Address: **Operational Base** + offset (0x00BC)

Bit	Attr	Reset Value	Description
31	RW	0x0	we The options for this field are: 1'h0: OOBR bits [30:0] are read-only; 1'h1: OOBR bits [30:0] can be written. This bit is cleared when COMRESET is detected.
30:24	RW	0x00	cwMin This field is RW when WE=1 and RO when WE=0.
23:16	RW	0x00	cwMax This field is RW when WE=1 and RO when WE=0.
15:8	RW	0x00	ciMin This field is RW when WE=1 and RO when WE=0.
7:0	RW	0x00	ciMax This field is RW when WE=1 and RO when WE=0.

SATA_MEMEDTXFERRDATAU

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mem_txf_err_synd_u When the TX FIFO RAM Data parity error syndrome width excess the range of the register MEMEDTXFERRDATA.mem_tx_err_synd, extra bits is logged in this field.

SATA_DIAGNR3

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	fbcsw_cnt FIS-based context switching counter

SATA_MEMEDFBSERRDATAU

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mem_fbs_err_synd_u When the FBS RAM Data parity error syndrome width excess the range of the register MEMEDFBSERRDATA.mem_fbs_err_synd, extra bits is logged in this field.

SATA_TIMER1MS

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Address: **Operational Base** + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x493e0	timv This field contains the following value for the internal timer to generate 1-ms tick: Famba*1000, where Famba = AMBA clock frequency in MHz. The options for this field are: RW when CCC_CTL.EN=0 and CCC_SUPPORT = Include RO when CCC_CTL.EN=1 and CCC_SUPPORT = Include RW when CCC_SUPPORT=Exclude and DEVSLP_SUPPORT=Include

SATA_MEMDPCR

Address: **Operational Base** + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	mem_par_even This value is derived from the MEM_PAR_EVEN parameter. The options for this field are as follows: 1'h0: Generate odd type of parity for data (if parity type protection selected) and address; 1'h1: Generate even type of parity for data (if parity type protection selected) and address.
8	RW	0x0	mem_err_inj_loc The options for this field are as follows: 1'h0: Inject error on data bits; 1'h1: Inject error on data check bits.
7	RW	0x0	mem_ed_log_clr_en 1'h0: All error detection and correction logging registers are cleared by Global or COMRESET. 1'h1: All error detection and correction logging registers are cleared only when MEMDPCR.EM_ED_LOG_CLR is set.
6	WO	0x0	mem_ed_log_clr This field clears all error detection and correction logging registers when written. This bit clears itself one cycle after written.
5	RW	0x0	mem_ed_log_dis This field disables error detection and correction logging when set.
4	RW	0x0	mem_ed_ce_en This field enables correctable error detection interrupt (INFS). (For diagnostic purposes only)
3	RW	0x0	mem_ed_pdmaf_dis This field disables PDMA from entering a fatal error state when an incorrect error is detected. (For diagnostic purposes only)

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Bit	Attr	Reset Value	Description
2	RW	0x0	mem_ed_ifs_dis This field disables setting the IFS interrupt register bit (interface fatal error status interrupt) when an incorrect error is detected when MEM_DP_TYPE selects ECC, or a Parity error is detected when MEM_DP_TYPE selects Parity.
1	RW	0x0	mem_ec_dis When set, disables the single error correcting features everywhere, and all errors are reported as incorrect. This field has no effect when MEM_DP_TYPE = Parity or when MEM_DP_EN = 0.
0	RW	0x0	mem_ed_dis All ECC/Parity error detection, correction, interrupt generation and Fatal error state transitions are disabled when this bit is set to 1. This field has no effect when the hardware parameter MEM_DP_EN = 0.

SATA_TESTR

Address: **Operational Base** + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RW	0x0	bsel This field is used to select a bank for BIST or Data Protection operation or Address Protection operation. The options for this field are: 2'h0: BIST registers selected 2'h1: Data Protection registers selected 2'h2: Address Protection registers selected 2'h3: Reserved
23:19	RO	0x00	reserved
18:16	RW	0x0	psel This field is used to select a Port for BIST operation. The options for this field are: 3'h0: Port0 is selected; 3'h1: Port1 is selected; 3'h2: Port2 is selected; 3'h3: Port3 is selected; 3'h4: Port4 is selected; 3'h5: Port5 is selected; 3'h6: Port6 is selected; 3'h7: Port7 is selected.
15:1	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	test_if This bit is used to put the SATA Host slave interface into the test mode. The options for this field are: 1'h0: Normal mode: the read back value of some registers is a function of the SATA Host state and does not match the value written; 1'h1: Test mode: the read back value of the registers matches the value written. Normal operation is disabled. The following registers can be accessed in this mode: GHC register IE bit BISTAFR register NCP and PD bits become read-write BISTCR register LLC, ERREN, FLIP, PV, PATTERN BISTFCTR, BISTSR, BISTDECR become read-write P0CLB/CLBU, P0FB/FBU registers P0IS register RW1C and UFS bits become read-write P0IE register RW bits (CPDE is RO if DEV_CP_DET = Exclude, DMPE bit is RO if DEV_MP_SWITCH = Exclude) P0CMD register ASP, ALPE, DLAE, ATAPI, PMA bits P0TFD, P0SIG registers become read-write P0SCTL register RW bits [9:8], [5:4], and [2:0] (Bits [2:0] cannot be written with the 3'b001 value if P0CMD.SUD=0) P0SERR register RW1C bits become read-write bits P0SACT, P0CI, P0SNTF registers become read-write P0DMACR register P0PHYCR register P0PHYSR register becomes read-write GPSR register becomes read-write

SATA_VERSION

Address: **Operational Base** + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x3530302a	version SATA Host hard-coded hexadecimal version value.

SATA_IDR

Address: **Operational Base** + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	id Hard-coded hexadecimal identification value.

SATA_P0CLB

Address: **Operational Base** + offset (0x0100)

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Bit	Attr	Reset Value	Description
31:10	RW	0x000000	clb Indicates the 32-bit base physical address for the command list for this Port. This base is used when fetching commands to execute. The structure pointed to by this address range is 1 KB in length. This address must be 1-KB-aligned as indicated by bits [9:0] being read only.
9:0	RO	0x000	reserved

SATA_P0CLBU

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clbu Indicates the upper 32 bits for the command list base physical address for this Port. This base is used when fetching commands to execute.

SATA_P0FB

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	fb Indicates the 32-bit base physical address for received FISes. The structure pointed to by this address range is 256 bytes in length. This address must be 256byte-aligned as indicated by bits [7:0] being read only.
7:0	RO	0x00	reserved

SATA_P0FBU

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	fbu Indicates the upper 32 bits for received FIS base physical address for this Port.

SATA_P0IS

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31	RW	0x0	cpds This bit is set when the P0_cp_det input changes its state due to the insertion or removal of the device. This bit is only valid when the Port supports cold presence detect as indicated by the P0CMD.CPD set to 1.
30	RW	0x0	tfes This bit is set whenever the P0TFD.STS register is updated by the device and the error bit [0] is set.

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Bit	Attr	Reset Value	Description
29	RW	0x0	hbfs This bit is set when SATA Host AMBA Master detects an ERROR response from the slave. Port DMA transitions to a fatal state until the software clears P0CMD.ST bit or resets the interface by way of Port or Global reset.
28	RW	0x0	hbds This bit is always cleared to 0.
27	RW	0x0	ifs This bit is set when any of the following conditions are detected: SYNC escape is received from the device during non-Data or Data FIS transmission or reception (P0SERR.DIAG_S and ERR_P are set); One or more of the following errors are detected during Data FIS transfer: Protocol (P0SERR.ERR_P) CRC (P0SERR.DIAG_C) Handshake (P0SERR.DIAG_H) PHY Not Ready (P0SERR.ERR_C) Unknown FIS is received with good CRC, but the length exceeds 64 bytes; PRD table byte count is zero; DMA Setup FIS is received with a TAG corresponding to inactive (P0SACT bit is cleared) command slot; RAM address protection error detected (when hardware configuration parameter MEM_AP_SUPPORT is set to Include, and the MEM_AP_ERRFB_EN is set to Include, and the MEMDPCR.MEM_ADDR_ED_IFS_DIS register bit is set to 0); and/or Uncorrected error detected (when hardware configuration parameter MEM_DP_SUPPORT is set to Include, and the MEMDPCR.MEM_ED_IFS_DIS register bit is set to 0). Port DMA transitions to a fatal state until the software clears PCMD.ST bit or resets the interface by way of Port or Global reset.

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Bit	Attr	Reset Value	Description
26	RW	0x0	infs This bit is set when any of the following conditions are detected: One or more of the following errors are detected during non-data FIS transfer: Protocol (P0SERR.ERR_P) CRC (P0SERR.DIAG_C) Handshake (P0SERR.DIAG_H) PHY Not Ready (P0SERR.ERR_C) Command list underflow during read operation (such as, DMA read) when the software builds command table that has more total bytes than the transaction given to the device Corrected error detected (when hardware configuration parameter MEM_DP_SUPPORT is set to Include, MEM_DP_TYPE is set to ECC, and the MEMDPCR.MEM_ED_CE_EN register bit is set to 1) In both cases Port operation continues normally. When error is detected during non-data FIS transmission, this FIS is retransmitted continuously until it succeeds, or until the software times out and resets the interface.
25	RO	0x0	reserved
24	RW	0x0	ofs This bit is set when command list overflow is detected during read or write operation when the software builds command table that has fever total bytes than the transaction given to the device. Port DMA transitions to a fatal state until the software clears P0CMD.ST bit or resets the interface by way of Port or Global reset.
23	RW	0x0	ipms Indicates that the HBA received a FIS from a device whose Port Multiplier field did not match what was expected. This bit may be set during enumeration of devices on a Port Multiplier due to the normal Port Multiplier enumeration process. The software must use the IPMS bit only after enumeration is complete on the Port Multiplier.
22	RW	0x0	prcs This bit reflects the state of the P0SERR.DIAG_N bit. When set to 1, indicates the internal P0_phy_ready signal changed state. To clear this bit, the software must clear the P0SERR.DIAG_N bit to 0.
21:8	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	dmps This bit is set when the P0_mp_switch input changes its state as a result of a mechanical switch attached to this Port opening or closing. This bit is valid only when both CAP.SMPS and P0CMD.MPSP are set.
6	RO	0x0	pcs This bit reflects the state of the P0SERR.DIAG_X bit: 1'h0: No change in Current Connect Status; 1'h1: Change in Current Connect Status. This bit is cleared only when P0SERR.DIAG_X is cleared.
5	RW	0x0	dps A PRD with the I bit set has transferred all of its data.
4	RO	0x0	ufs When set to 1, indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by the software clearing the P0SERR.DIAG_F bit to 0.
3	RW	0x0	sdbs A Set Device Bits FIS has been received with the 'I' bit set and has been copied into system memory.
2	RW	0x0	dss A DMA Setup FIS has been received with the 'I' bit set and has been copied into system memory.
1	RW	0x0	pss A PIO Setup FIS has been received with the 'I' bit set, it has been copied into system memory, and the data related to that FIS has been transferred.
0	RW	0x0	dhrs A Device-to-Host Register FIS has been received with the 'I' bit set, and has been copied into system memory.

SATA_P0IE

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31	RW	0x0	cpde When the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.CPDS=1

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Bit	Attr	Reset Value	Description
30	RW	0x0	tfee when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.TFES=1
29	RW	0x0	hbfe When the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.HBFS=1
28	RW	0x0	hbde When the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.HBDS=1
27	RW	0x0	ife When the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.IFS=1
26	RW	0x0	infe When the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.INFS=1
25	RO	0x0	reserved
24	RW	0x0	ofe When the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.OFS=1
23	RW	0x0	ipme When the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.IPMS=1

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Bit	Attr	Reset Value	Description
22	RW	0x0	prce When the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.PRCS=1
21:8	RO	0x0000	reserved
7	RW	0x0	dmpe When the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.DMPS=1
6	RO	0x0	pce When the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.PCS=1
5	RW	0x0	dpe When the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.DPS=1
4	RO	0x0	ufe When the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.UFS=1
3	RW	0x0	sdbe When the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.SDBS=1
2	RW	0x0	dse When the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.DSS=1

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Bit	Attr	Reset Value	Description
1	RW	0x0	pse When the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.PSS=1
0	RW	0x0	dhre Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P0IS.DHRS=1

SATA_P0CMD

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	icc This field is used to control power management states of the interface. When the Link layer is currently in the L_IDLE state or L_NoCommPower state, writes to this field cause the Port to initiate a transition to the interface power management state requested. When the Link layer is not currently in the L_IDLE state or L_NoCommPower, writes to this field have no effect. 4'h1: Active. This causes the Port to request a transition of the interface into the active state; 4'h2: Partial. This causes the Port to request a transition of the interface to the Partial state. The SATA device can reject the request and the interface remains in its current state; 4'h6: Slumber. This causes the Port to request a transition of the interface to the Slumber state. The SATA device can reject the request and the interface remains in its current state; Else: Reserved.
27	RW	0x0	asp The options for this field are: When set to 1, and P0CMD.ALPE=1, the Port aggressively enters the SLUMBER state when one of the following conditions is true: The Port clears the P0CI and the P0SACT register is cleared. The Port clears the P0SACT register and P0CI is cleared. When cleared to 0, and P0CMD.ALPE=1, the Port aggressively enters the PARTIAL state when one of the following conditions is true: The Port clears the P0CI register and the P0SACT register is cleared. The Port clears the P0SACT register and P0CI is cleared.

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Bit	Attr	Reset Value	Description
26	RW	0x0	alpe When set to 1, the Port aggressively enters a lower link power state (PARTIAL or SLUMBER) based on the setting of the P0CMD.ASP bit. When cleared to 0, aggressive power management state transition is disabled.
25	RW	0x0	dlae When set to 1, P0CMD.ATAPI=1, and commands are active, the Port asserts P0_act_led output.
24	RW	0x0	atapi This bit is used by the Port to control whether to assert P0_act_led output when commands are active. The options for this field are: 1'h0: Non-ATAPI device; 1'h1: ATAPI device.
23	RW	0x0	apste When this bit is set and the SATA Host Link layer negotiates Partial power management state with the device, it transitions into the Slumber state directly, regardless whether it was host software-, Port (aggressive)-, or device-initiated.
22	RW	0x0	fbscp When set to 1, indicates that this Port supports Port Multiplier FIS-based switching. When cleared to 0, indicates that this Port does not support FIS-based switching.
21	RW	0x0	esp When set to 1, indicates that this Port's signal only connector is externally accessible. When set to 1, CAP.SXS is also set to 1. When cleared to 0, indicates that this Port's signal only connector is not externally accessible.
20	RW	0x0	cpd The options for this field are: 1'h0: Platform does not support cold presence detection on this Port; 1'h1: Platform supports cold presence detection on this Port. When this bit is set to 1, P0CMD.HPCP must also be set to 1.
19	RW	0x0	mpsp To enable the SATA Host mechanical presence detection feature. The options for this field are: 1'h0: Indicates the platform does not support a mechanical presence switch attached to this Port. When this bit is set to 1, P0CMD.HPCP should also be set to 1; 1'h1: Indicates the platform supports a mechanical presence switch attached to this Port.

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Bit	Attr	Reset Value	Description
18	RW	0x0	hpcp The options for this field are: 1'h0: Indicates that this Port's signal and power connectors are not externally accessible; 1'h1: Indicates that this Port's signal and power connectors are externally accessible via a joint signal-power connector for blind mate device hot plug.
17	RO	0x0	pma The software is responsible for detecting whether a Port Multiplier is present; the SATA Host Port does not auto-detect the presence of a Port Multiplier. The options for this field are: 1'h0: A Port Multiplier is not attached to this Port; 1'h1: A Port Multiplier is attached to this Port.
16	RO	0x0	cps This bit reports whether a device is currently detected on this Port as indicated by the P0_cp_det input state. The options for this field are: 1'h0: No device attached to this Port; 1'h1: Device is attached to this Port.
15	RO	0x0	cr When this bit is set to '1', the command list DMA engine for this Port is running.
14	RO	0x0	fr When set to '1', the FIS Receive DMA engine for the Port is running.
13	RO	0x0	mpss The software must use this bit only when both CAP.SMPS and P0CMD.MPSP are set. This bit reports the state of a mechanical presence switch attached to this Port as indicated by the P0_mp_switch input state. The options for this field are: 1'h0: Switch is closed; 1'h1: Switch is open. When CAP.SMPS=0 then this bit is cleared to 0.
12:8	RW	0x00	ccs This field is set to the command slot value of the command that is currently being issued by the Port. When P0CMD.ST transitions from 1 to 0, this field is cleared again to 5'h0. After P0CMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is P0CMD.CCS+1.
7:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	fre When set to 1, the Port may post received FISes into the FIS receive area pointed to by P0FB. When cleared, received FISes are not accepted by the Port, except for the first D2H register FIS after the initialization sequence, and no FISes are posted to the FIS receive area. The software must not set this bit until P0FB has been programmed with a valid pointer to the FIS receive area. When the software wishes to move the base, this bit must first be cleared, and the software must wait for the P0CMD.FR bit to be cleared.
3	RW	0x0	clo Setting this bit to 1 cause P0TFD.STS.BSY and P0TFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the P0TFD.STS register. This bit is cleared to 0 when P0TFD.STS.BSY and P0TFD.STS.DRQ have been cleared to 0. A write to this register with a value of '0' has no effect. This bit should only be set to 1 immediately prior to setting P0CMD.ST bit to 1 from a previous value of 0. Setting this bit to 1 at any other time is not supported and results in indeterminate behaviors.
2	RW	0x0	pod This bit is read/write when cold presence detection is supported on this Port as indicated by P0CMD.CPD=1. This bit is read-only 1 when cold presence detection is not supported and P0CMD.CPD=0. When set, the Port asserts the P0_cp_pod output pin so that it may be used to provide power to a cold-presence detectable Port.
1	RW	0x0	sud This bit is read/write when staggered spin-up is supported as indicated by the CAP.SSS=1. This bit is read-only 1 when staggered spin-up is not supported and CAP.SSS=0. On an edge detect from 0 to 1, the Port starts a COMRESET initialization sequence to the device. Clearing this bit causes no action on the interface.
0	RW	0x0	st When set to 1, the Port processes the command list. When cleared, the Port does not process the command list. Whenever this bit is changed from a 0 to a 1, the Port starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the P0CI register is cleared by the Port upon transition into an idle state.

SATA_P0TFD

Address: **Operational Base** + offset (0x0120)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x7f	err This field contains the latest copy of the task file error register.
7:0	RO	0x00	sts This field contains the latest copy of the task file status register. The bits that affect SATA Host operation are: Bit [7] BSY: Indicates the interface is busy; Bits [6:4] cs: Command specific; Bit [3] DRQ: Indicates a data transfer is requested; Bits [2:1] cs: Command specific; Bit [0] ERR: Indicates an error during the transfer.

SATA_P0SIG

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RO	0xffffffff	sig This field contains the signature received from a device on the first D2H Register FIS. The bit order as follows: Bits [31:24]: LBA High (Cylinder High) Register; Bits [23:16]: LBA Mid (Cylinder Low) Register; Bits [15:8]: LBA Low (Sector Number) Register; Bits [7:0]: Sector Count Register. This field is updated once after a reset sequence (cause by asynchronous, port, or soft reset). Reset on Global or Port reset.

SATA_P0SSTS

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RO	0x0	ipm Indicates the current interface state. The options for this field are: 4'h0: Device not present or communication not established; 4'h1: Interface in Active state; 4'h2: Interface in Partial power management state; 4'h6: Interface in Slumber power management state; 4'h8: Interface in DevSleep power management state.
7:4	RO	0x0	spd Indicates the negotiated interface communication speed. The options for this field are: 4'h0: Device not present or communication not established; 4'h1: 1.5 Gb/s communication rate negotiated; 4'h2: 3.0 Gb/s communication rate negotiated; 4'h3: 6.0 Gb/s communication rate negotiated.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	det Indicates the interface device detection and PHY state. The options for this field are: 4'h0: No device detected and PHY communication not established; 4'h1: Device presence detected but PHY communication not established (COMINIT is detected); 4'h3: Device presence detected and PHY communication established ('PHY Ready' is detected); 4'h4: PHY in offline mode as a result of the interface being disabled or running in a BIST loopback mode. All other values reserved.

SATA_P0SCTL

Address: **Operational Base** + offset (0x012C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	ipm This field indicates which power states the Port PHY interface is allowed to transition to. When an interface power management state is disabled, the Port does not initiate that state and any request from the device to enter that state is rejected via PMNAKp. The options for this field are: 2'h0: No interface power management state restrictions; 2'h1: Transitions to the Partial state disabled; 2'h2: Transitions to the Slumber state disabled; 2'h3: Transitions to both Partial and Slumber states disabled.
7:6	RO	0x0	reserved
5:4	RW	0x0	spd This field indicates the highest allowable speed of the Port PHY interface. The options for this field are: 2'h0: No speed negotiation restrictions 2'h1: Limit speed negotiation to SATA 1.5 Gb/s communication rate 2'h2: Limit speed negotiation to SATA 3.0 Gb/s communication rate 2'h3: Limit speed negotiation to a rate not greater than SATA 6.0 Gb/s communication rate.
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	det Controls the Port's device detection and interface initialization. The options for this field are: 3'h0: No device detection or initialization action requested 3'h1: Perform interface initialization sequence to establish communication. This results in the interface being reset and communication re initialized. The SATA Host asserts the corresponding P0_phy_reset(_n) output when DET=0x1. It negates P0_phy_reset(_n) and sends COMRESET OOB sequence when DET=0x0. 3'h4: Disable the Serial ATA interface and put the Port PHY in offline mode.

SATA_P0SERR

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	diag_x This bit is set to 1 when PHY COMINIT signal is detected. This bit is reflected in the P0IS.PCS bit.
25	RW	0x0	diag_f This bit indicates that one or more FISes were received by the Transport layer with good CRC, but had a type field that was not recognized/known and the length was less than or equal to 64 bytes.
24	RW	0x0	diag_t This bit indicates that a Transport Layer protocol violation was detected since the last time this bit was cleared.
23	RW	0x0	diag_s This bit indicates that one or more Link state machine error conditions was encountered. One of the conditions that cause this bit to be set is device doing SYNC escape during FIS transmission.
22	RW	0x0	diag_h This bit indicates that one or more R_ERRp was received in response to frame transmission. Such errors may be the result of a CRC error detected by the device, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21	RW	0x0	diag_c This bit indicates that one or more CRC errors were detected by the Link layer during FIS reception.
20	RO	0x0	diag_d This bit is always cleared to 0 since it is not used by the AHCI specification.

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Bit	Attr	Reset Value	Description
19	RW	0x0	diag_b This bit indicates errors were detected by 10b/8b decoder.
18	RW	0x0	diag_w This bit is set when PHY COMWAKE signal is detected.
17	RW	0x0	diag_i This bit is set when the PHY detects some internal error as indicated by the assertion of the P0_phy_rx_err input.
16	RW	0x0	diag_n This bit indicates that the PHY Ready signal changed state. This bit is reflected in the P0IS.PRCS bit.
15:12	RO	0x0	reserved
11	RW	0x0	err_e This bit is set to 1 when one or more AMBA bus ERROR responses are detected on the master interface.
10	RW	0x0	err_p This bit is set to 1 when any of the following conditions are detected. Transport state transition error (DIAG_T) Link sequence error (DIAG_S) RX FIFO overflow Link bad end error (WTRM instead of EOF is received).
9	RW	0x0	err_c This bit is set to 1 when PHY Ready signal is negated due to the loss of communication with the device or problems with interface, but not after transition from active to Partial or Slumber power management state.
8	RW	0x0	err_t This bit is set when any of the following P0SERR register bits are set during Data FIS transfer: ERR_P (Protocol) DIAG_C (CRC) DIAG_H (Handshake) ERR_C ('PHY Ready' negation)
7:2	RO	0x00	reserved
1	RW	0x0	err_m This bit is set to 1 when the PHY Ready condition is asserted under the following conditions: At any time except when there is a transition from power-down mode to Active state After interface initialization (after power on or COMRESET)

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Bit	Attr	Reset Value	Description
0	RW	0x0	err_i This bit is set when any of the following P0SERR register bits is set during non-Data FIS transfer: ERR_P (Protocol) DIAG_C (CRC) DIAG_H (Handshake)

SATA_P0SACT

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ds This field is bit significant. Each bit corresponds to the TAG and command slot of a native queued command, where bit 0 corresponds to TAG 0 and command slot 0. Software sets this field prior to issuing a native queued command for a particular command slot. Prior to writing P0CI[TAG] to 1, the software sets DS[TAG] to 1 to indicate that a command with that TAG is outstanding. This field is cleared to 0 when: The software writes P0CMD.ST from a 1 to a 0. The device sends a Set Device Bits FIS to the Port. The Port clears bits in this field that are set in the SActive field of the Set Device Bits FIS. The Port clears only bits that correspond to native queued commands that have completed successfully. This field is not cleared by the following: Port reset (COMRESET). Software reset.

SATA_P0CI

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ci This field is bit significant. Each bit corresponds to a command slot, where bit 0 corresponds to command slot 0. This field is set by the software to indicate to the Port that a command has been built in system memory for a command slot and may be sent to the device. When the Port receives a FIS which clears the BSY, DRQ, and ERR bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field can only be set to 1 by the software when P0CMD.ST is set to 1.

SATA_P0SNTF

Address: **Operational Base** + offset (0x013C)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	pmn This field indicates whether a particular device with the corresponding PM Port number issued a Set Device Bits FIS to the SATA Host Port with the Notification bit set: PM Port 0 sets bit 0. PM Port 1 sets bit 1. ... PM Port 15 sets bit 15. Individual bits are cleared by the software writing 1s to the corresponding bit positions. This field is reset on Global reset, but it is not reset by Port reset (COMRESET) or software reset.

SATA_P0FBS

Address: **Operational Base** + offset (0x0140)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RO	0x0	dwe This field is set by the SATA Host core to the value of the Port Multiplier port number of the device that experienced a fatal error condition. This field is only valid when P0FBS.SDE=1.
15:12	RW	0x0	ado This field is hard-wired to the FBS_PMPN_MAX value.
11:8	RW	0x0	dev Software sets this field to the Port Multiplier port value of the next command to issue. This field enables the SATA Host core to know the port the command to be issues to without fetching the command header. Software should not issue commands to multiple Port Multiplier ports on the same write of the P0CI register. This bit is reset on Global reset.
7:3	RO	0x00	reserved
2	RW	0x0	sde When this field is set to 1 and a fatal error condition has occurred, the SATA Host core believes the error is localized to one device such that software's first error recovery step should be to utilize the P0FBS.DEC functionality. When cleared to 0 and a fatal error condition has occurred, the error applies to the entire Port. To clear the error, software should clear P0CMD.ST to 0. This bit is cleared on P0FBS.DEC being set to 1 or on P0CMD.ST being cleared to 0. This bit is reset on Global reset.

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Bit	Attr	Reset Value	Description
1	RW	0x0	dec When set to 1 by software, the SATA Host core clears the device-specific error condition. It flushes any commands outstanding for the device that experienced the error, including clearing P0CI and P0SACT bits for that device to 0. The SATA Host core clears this bit to 0 when it completes error recovery actions. When software writes a 0 to this bit, there is no effect. Software should only set this bit to 1 if P0FBS.EN=1 and P0FBS.SDE=1. This bit is reset on Global reset.
0	RW	0x0	en 1'h0: FIS-based switching is not being used (command-based switching is used instead). Software should only change the value of this bit when P0CMD.ST=0; 1'h1: A Port Multiplier is attached and the SATA Host uses FIS-based switching to communicate with it. This bit is reset on Global reset.

SATA_P0DMACR

Address: **Operational Base** + offset (0x0170)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	rxts This field defines the Port DMA transaction size in FIFO words for receive (system bus write, device read) operation. The options for this field are: 4'h0: 1 4'h1: 2 4'h2: 4 4'h3: 8 4'h4: 16 4'h5: 32 4'h6: 64 4'h7: 128 4'h8: 256 4'h9: 512 4'hA: 1024 All other values are reserved and should not be used. This field is read-write when P0CMD.ST=0 and read-only when P0CMD.ST=1.

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Bit	Attr	Reset Value	Description
3:0	RW	0x4	txts This field defines the DMA transaction size in FIFO words for transmit (system bus read, device write) operation. The options for this field are: 4'h0: 1 4'h1: 2 4'h2: 4 4'h3: 8 4'h4: 16 4'h5: 32 4'h6: 64 4'h7: 128 4'h8: 256 4'h9: 512 4'hA: 1024 All other values are reserved and should not be used. This field is read-write when P0CMD.ST=0 and read-only when P0CMD.ST=1.

16.5 Interface Description

Table 16-1 SATA host interface description

Module Pin	Direction	Pad Name	IOMUX Setting
SATA0_CPDET	I	ETH1_RXD0_M1/FSPI1_D3_M1/PDM0_SDI1_M2/UART2_RX_M0/I2C8_SDA_M1/SATA_CPDET/GPIO1_C7_d	IOC_MISC_CON0[0]=1'b0; TOP_IOC_GPIO1C_IOMUX_SEL_H[15:12]=4'hc
SATA1_CPDET	I	ETH1_RXD0_M1/FSPI1_D3_M1/PDM0_SDI1_M2/UART2_RX_M0/I2C8_SDA_M1/SATA_CPDET/GPIO1_C7_d	IOC_MISC_CON0[0]=1'b1; TOP_IOC_GPIO1C_IOMUX_SEL_H[15:12]=4'hc
SATA0_MPSWITCH	I	ETH_CLK1_25M_OUT_M1/FSPI1_CLK_M1/PDM0_CLK1_M2/SPDIF_TX1_M2/UART10_CTSN_M1/I2C5_SDA_M1/SPI2_CLK_M1/SATA_MPSWIT/CLK1_32K_OUT/GPIO1_D5_d	IOC_MISC_CON0[0]=1'b0; TOP_IOC_GPIO1D_IOMUX_SEL_H[7:4]=4'hc
SATA1_MPSWITCH	I	ETH_CLK1_25M_OUT_M1/FSPI1_CLK_M1/PDM0_CLK1_M2/SPDIF_TX1_M2/UART10_CTSN_M1/I2C5_SDA_M1/SPI2_CLK_M1/SATA_MPSWIT/CLK1_32K_OUT/GPIO1_D5_d	IOC_MISC_CON0[0]=1'b1; TOP_IOC_GPIO1D_IOMUX_SEL_H[7:4]=4'hc
SATA0_CPPOD	O	ETH1_TXCTL_M1/FSPI1_D2_M1/PDM0_SDI0_M2/UART2_TX_M0/I2C8_SCL_M1/SATA_CPPOD/GPIO1_C6_d	IOC_MISC_CON0[0]=1'b0; TOP_IOC_GPIO1C_IOMUX_SEL_H[11:8]=4'hc
SATA1_CPPOD	O	ETH1_TXCTL_M1/FSPI1_D2_M1/PDM0_SDI0_M2/UART2_TX_M0/I2C8_SCL_M1/SATA_CPPOD/GPIO1_C6_d	IOC_MISC_CON0[0]=1'b1; TOP_IOC_GPIO1C_IOMUX_SEL_H[11:8]

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Module Pin	Direction	Pad Name	IOMUX Setting
			=4'hc
SATA0_ACTLED_M0	O	VI_CIF_D9/SDMMC1_PWREN_M1/ETH0_TXD2_M1/SAI0_SDI3_M0/PDM0_SDI0_M3/UART7_CTSN_M0/SPI4_MOSI_M3/SATA0_ACTLED_M0/GPIO2_B4_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[3:0]=4'hc
SATA1_ACTLED_M0	O	VI_CIF_D8/SDMMC1_DETN_M1/ETH0_RXCLK_M1/SAI0_MCLK_M0/PDM0_CLK0_M3/UART7_RTSN_M0/SPI4_MISO_M3/SATA1_ACTLED_M0/GPIO2_B5_d	TOP_IOC_GPIO2B_IOMUX_SEL_H[7:4]=4'hc
SATA0_ACTLED_M1	O	SAI4_SDI_M2/VP1_SYNC_OUT/PCIE0_CLKREQN_M3/SATA0_ACTLED_M1/I2C6_SCL_M3/SPI4_MISO_M0/CAN1_TX_M1/PWM2_CH2_M1/GPIO4_C6_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[11:8]=4'ha
SATA1_ACTLED_M1	O	ISP_FLASH_TRIGOUT_M1/SAI4_SDO_M2/VP0_SYNC_OUT/SATA1_ACTLED_M1/I2C3_SDA_M3/SPI4_MOSI_M0/UART6_RX_M3/PWM2_CH5_M1/GPIO4_C5_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[7:4]=4'ha

Notes: I=input, O=output, I/O=input/output, bidirectional

16.6 Application Notes

16.6.1 Data transfer

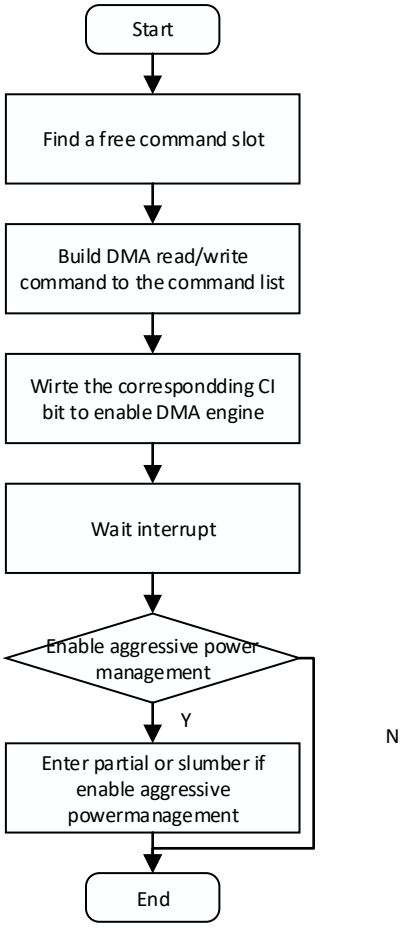


Fig. 16-2 Data transfer flow

16.6.2 Port multiple support

When a port is connected to a Port Multiplier, software must first enumerate it by issuing software reset to Port 0xF (control Port) on the Port Multiplier. When the signature returned corresponds to a Port Multiplier, then a Port Multiplier is attached. When the signature returned corresponds to another device type, then a Port Multiplier is not attached.

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The SATA host provides command list override feature via CMD.CLO to help software reliably enumerate the Port Multiplier:

- software ensures that CMD.ST bit is 0;
- software constructs the two register FISes required for a software reset in the command list, where the PM port field value in the register FIS is set to 0xF;
- software set CMD.CLO to 1 to force the BSY and DRQ bits in the TFD register to be cleared;
- software sets CMD.ST bit to 1 and set appropriate CI bits in order to begin execution of the software reset command.

16.6.3 Interrupt

The SATA host uses two-tiered interrupt structure.

First tier (GIS register)
The first tier is identified by the GIS and GHC registers. GHC.IE bit enables interrupts for the entire host: when it is cleared, interrupt output is not asserted regardless of any bits set in the GIS register. GHC.IE bit acts as a mask and does not affect the setting of any interrupt status bits.

Second tier (PIS registers)
The second tier is identified in each port through the PIS (status) and PIE (interrupt enable) register. The PIS register has various interrupt bits that can be individually enabled or disabled by setting the corresponding bit in the PIE. The status bit in the PIS is always set regardless of the setting of the corresponding PIE bit.

16.6.4 reset condition

System reset
System bus resets SATA host by asserting aresetn=0. It is usually initiated on power-up or during system bus failure. All components of the host are initialized, including ports, Generic registers, BIU.

Global reset
Software may globally reset host by setting GHC.HR to 1. When software sets the GHC.HR bit to 1, the host performs an internal reset action, then clears this bit to 0 when the reset is complete. A software writes of 0 to GHC.HR has no affect.

Port reset (COMRESET)
Software causes a Port reset by writing 1h to the SCTL.DET field to invoke COMRESET on the interface and start a re-establishment of the PHY Layer communication. Software should wait at least 1ms before clearing SCTL.DET to 0h. After clearing SCTL.DET to 0h, software should wait for communication to be re-established as indicated by 0 of SSTS.DET being set to 1. Then software should write all ones to SERR register to clear any bits that were set as part of the Port reset.

Software reset
Software builds two H2D register FISes in the command list. The first register FIS has the SRST bit set to 1 in the control field of the register FIS, the "C" bit is cleared to "0" in the register FIS, and the command table has the CH[R] (reset) and CH[C] (clear BSY ON R_OK) bits set to "1". The CH[R] bit causes the Port to perform a SYNC escape when necessary to put the device into an idle condition before sending the software reset. The CH[C] bit needs to be set for the first register FIS to clear the BSY bit and proceed to issue the next register FIS since the device does not send a response to the first register FIS in a software reset sequence. The second register FIS has SRST="0" in the control field of the register FIS, the "C" bit is cleared to "0" in the register FIS, and the command tables has the CH[R] and CH[C] bits cleared to "0". When issuing a software reset sequence, there should not be other commands in the command list. Before issuing the software reset, software must clear CMD.ST, wait for the Port to be idle, and then re-set CMD.ST. TFD.STS.BSY and TFD.STS.DRQ must be cleared prior to issuing the reset. When TFD.STS.BSY or TFD.STS.DRQ is still set based on the failed command, then a Port reset should be attempted or command list override should be used.

16.6.5 Staggered spin-up

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The CMD.SUD bit is used to manipulate the PHY behavior. SCTL.DET and CMD.SUD must be set correctly in order to avoid illegal combinations of the two values. Table 16-2 CMD.SUD and SCTL.DET interactiondescribes interaction between the CMD.SUD and SCTL.DET bits.

Table 16-2 CMD.SUD and SCTL.DET interaction

S	C	M	Behavior
0	0		Interface is in a reduced power state. When COMINIT is received then SERR.DIAG_X is set and no response is sent to the device COMWAVE is ignored. The application must place the Port into this state only when no device is detected as connected to this Port. In this mode, the Port forces the PHY into a low power state without requesting a SLUMBER transition on the link.
0	0-		Port sends COMRESET, begins initialization sequence.
0	1		Normal operating state when the Port is performing data transfer.
1	0	Il	This combination is prohibited in hardware, i.e. CMD.SUD can't be cleared when SCTL/DET=1, and SCTL.DET can't be set to 1 when CMD.SUD=0.
1	1	R	Port continuously transmits COMRESET and does not listen for COMINIT. When COMINIT is received in this state, the SERR.DIAG_X bit is set.
1-	1	I	Port stops sending COMRESET, being initialization sequence
4	N/	O	Port PHY is off.

Software must only clear CMD.SUD when it believes that no device is attached. In listen mode, the Port PHY enters a reduced power state, equivalent to the SLUMBER power management state. The Port PHY enters this state without negotiating a transition to SLUMBER on the link, as asking for a transition to SLUMBER when no device is attached fails, and therefore the PHY remains in a high power state. To avoid this software should ensure that SSTS.DET=0x0 indicating that no device is present before clearing CMD.SUD.

16.6.6 Activity LED

The CAP.SAL=1 indicates that the activity LED feature is enabled to software. Act_led outputs is used to drive an external LED based upon activity of the Port:

- 1 - LED On
- 0 - LED Off

The port drives the LED active if:

- (CI!=0 or SACT!=0) and CMD.ATAPI = 0
- (CI!=0 or SACT!=0) and CMD.ATAPI = 1 and CMD.DLAE = 1

The Port drives the LED off when CI and SACT are both cleared to 0.

16.6.7 Asynchronous notification

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The SATA host supports asynchronous notification feature as indicated by the CAP.SSNT=1. This feature allows an ATAPI device to send a signal to the host when media is inserted or removed and avoid polling the device for media changes. The signal sent to the host is Set Device Bits FIS with the "I" and "N" bits set to "1".

To use asynchronous notification, software should set the IS.SDBS bit to enable interrupt notification on a Set Device Bits FIS. When accesses to the ATAPI device are idle, software should place the device in a low power state. When the device has media change, it signals this to the host with a Set Device Bits FIS. In response to receiving a IS.SDBS interrupt on an idle Port, the software should interrogate the device to determine the cause of the interrupt.

The first DWORD of any FIS received by the host contains a 4-bit Port Multiplier field. The PM port field indicates which Port behind the Port Multiplier issued the FIS to the host. When a set device bits FIS is received by the host and "N" bit is set, the bit position in the SNTF register corresponding to the PM Port field is set. The host sets the IS.SDBS to "1" when the "I" bit is set in the set device bits FIS. This causes an interrupt to be generated when that interrupt is enabled.

16.6.8 BIST operation

1.6.8.1 Loopback responder

Software must ensure that the CMD.ST bit is set, the Port is in idle state, and there are no outstanding commands by checking CI and SACT registers are both cleared, TFD.STS register BSY, DRQ and ERR bits are all cleared.

The host enters one of the BIST loopback responder modes when a corresponding BIST Activate FIS is successfully received from the device and is supported by the host. SSTS.DET field return 4h when read. Since BIST registers' locations are shared between all the active ports, software must first select the Port for BIST operation by writing the Port number to the TESTR.PSEL field before accessing BISTAFR.

The following loopback responder modes are supported by the host:

- Far-end Retimed
  - The Port receives BIST activate FIS with pattern definition field=0x10 from the RX FIFO and stores it in the BIST AFR.PD field
  - All the data received from the device in the form of a SATA-compliant pattern is retimed in the Link Layer and transmitted back to the device.
  - Alternately, this mode can be initiated with device disconnected from the Port PHY when software writes BISTCR.FERLB=1. After the device is connected to the host, the device must transmit the number of ALIGNs required for the PHY to sync.
- Far-end Analog
  - The Port receives BIST active FIS with pattern definition field =0x08 from the RX FIFO and stores it in the BISTAFR.PD field
  - The Port asserts phy_farafelb signal to the PHY to put it to the Far-end analog loopback mode. The PHY receives and retransmits the raw data without retiming
- Far-end Transmit only
  - The Port receives BIST activate FIS with pattern definition field = 0xC0(scrambling is enabled) or 0xE0 (scrambling is bypassed) from the RX FIFO and stores it in the BISTAFR.PD field. The second DWORD of the BIST activate FIS least significant byte is stored in the BISTAFR.NCP field.
  - The Port transmits corresponding a SATA non-compliant test pattern to the device based on the BISTAFR.NCP value:
    - 0xF1: Low transition density pattern (LTDP)
    - 0xB5: High transition density pattern (HTDP)
    - 0xAB: Low frequency spectral component pattern (LFSCP)
    - 0x7F: Simultaneous switching outputs pattern (SSOP)
    - 0x78: Mid frequency test pattern (MFTP)
    - 0x4A: High frequency test pattern (HFTP)

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- 0x7E: Low frequency test pattern (LFTP)

If none of the previous pattern is decoded, the Lone bit pattern (LBP) is transmitted by default.

- Alternately, this mode can be initiated with the device disconnected from the Port PHY when software writes a one to BISTCR.TXO bit. Host transmits non-compliant BIST pattern defined by the value in the BISTCR.PATTERN field.

Loopback responder BIST modes can be exited either when the device signals COMINIT OOB condition, or when the software initiates Port reset.

1.6.8.2 Loopback initiator

The software first selects the Port for BIST operation by writing the Port number to the TESTR.PSEL field, then the required pattern by writing to the BISTCR.PATTERN field.

The software builds a BIST FIS with the required mode in the commands list and sets CTBAz[B]. Once a BIST command is placed into the list, software is not allowed to build any more commands until it clears CMD.ST. After the Port successfully transmits this FIS, it enters this mode and generates/receives the compliant test pattern selected by the BISTCR.PATTERN field.

SSTS.DET return 4h when read. BISTCR and BISTFCTR registers are updated with error/FIS count information for each received BIST FIS.

The following BIST initiator modes can be requested by the software:

- Far-end Retimed
  - The host software writes the BISTCR.PATTERN field to select one of the SATA-defined compliant patterns:
    - 0x0: Simultaneous switching outputs pattern (SSOP)
    - 0x1: High transition density pattern (HTDP)
    - 0x2: Low transition density pattern (LTDP)
    - 0x3: Low frequency spectral component pattern (LFSCP)
    - 0x4: Composite pattern (COMP)
    - 0x5: Lone bit pattern (LBP)
    - 0x6: Mid frequency test pattern (MFTP)
    - 0x7: High frequency test pattern (HFTP)
    - 0x8: Low frequency test pattern (LFTP)
  - The software prepares BIST Activate FIS with bits [23:16] = 8'h10 of the first DWORD in the command list. The Port sends this BIST Activate FIS to the device.
  - After successful transmission of the BIST Activate FIS the Port generates the requested compliant pattern in the form of BIST frames continuously and checks for errors on the receive side.
  - BISTCTR register is updated with received BIST frame count and BISTSR - with frame /burst error count. SERR register is updated with CRC, disparity and 10B8B errors for each frame. BISTFCTR, BISTSR, and BISTDECR registers can be cleared by writing 1 to the BISTCR.CNTCLR bit.
  - To change the pattern, the software issues a Port Reset, write to the BISTCR.PATTERN field to select a new pattern and re-issues the command by setting the CI bit.

- Far-end Analog
  - The software prepares BIST Activate FIS with bits [23:16] = 8'h8 of the first DWORD in the command list. The Port sends this BIST Activate FIS to the device.
  - The operation proceeds as described in the Far-end retimed test above.

- Near-end Analog
  - This mode can be initiated either in the PARTIAL power management mode or with the device disconnected from the Port PHY. The software issues a PARTIAL power

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state request to the device via CMD.ICC field and sets the BISTCR.NEALB bit. The BISTCR.PATTERN field selects the required BIST pattern.
  - The Port asserts phy_nearfelb to the PHY. The PHY loops the data from its transmitter to its receiver and ignores any data coming from the device.

- Far-end Transmit only
  - The software prepares BIST Activate FIS in the command list with the second and third DWORDs containing the required pattern, and the first DWORD - with the Pattern definition value corresponding to the required mode - Bit 23 is set, bits 20,19,17 cleared and bits 22,21 and 18 are used to enable the following options:
    - Bit 22 is set - Bypass ALIGN
    - Bit 21 is set - Bypass scrambling
    - Bit 18 is set - primitive bit
  - The Port sends this BIST Activate FIS to the device.
  - After the device acknowledges the reception of this FIS with R_OKp, the Port disables the PHY receiver and transmitter.

Loopback initiator BIST modes can be terminated either by the device when it signals COMINIT OOB condition (except the near-end analog mode), or when the software initiates Port reset.

16.6.9 command completion coalescing

A command completion coalescing (CCC) feature is used to reduce the interrupt and command completion overhead in a heavily-loaded system. The host generates an interrupt to allow software to process completed commands when either of these conditions is true:

- A software-specified number of commands have completed
- A software-specified time-out has expired

This feature applies to all ports selected to be in the CCC set by software via the CCC_PORTS register.

CCC logic used specific register TIMERIMS to generate 1ms interval based on the application clock frequency. Software must load this register with the required value before enabling the CCC feature:

Fappclk*1000, where Fappclk = aclk frequency, in MHz.

Additional Command completion coalescing details and examples can be found in the AHCI specification.

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Chapter 17 Multiple Protocol PHY

17.1 Overview

The PHY subsystem contains one types of PHY. It is a combo of multiple protocol including the PCIe 2.0/USB 3.0/SATA 3.1, 2 Combo PIPE PHYs are used.

17.1.1 Combo PIPE PHY Overview

The Combo PIPE PHY supports physical layer of multiple protocol including USB3.0 Super Speed (5GT/s), PCIe Gen1/Gen2(2.5GT/s and 5GT/s), SATA Gen1/Gen2/Gen3 (1.5GT/3GT/s /6GT/s).

The key features of the Combo PIPE PHY core include:

- Compatible with PCIe/USB3/SATA base Specification
- Fully compatible with PIPE 4.3 interface specification
- Data rate configurable to 1.25G/1.5G/2.5G/3G/5G/6G for different application
- Support 16-bit or 32-bit parallel interface when encode/decode enabled
- Support 20-bit parallel interface when encode/decode bypassed
- Support flexible reference clock frequency
- Support 100MHz differential reference clock input or output (optional with SSC) in PCIe Mode
- Support Spread-Spectrum clock (SSC) generation and receiving from -5000ppm to 0ppm
- Support programmable transmit amplitude and De-emphasis
- Support TX detect RX function in PCIe and USB3.0 Mode
- Support Beacon signal generation and detection in PCIE Mode
- Support Low Frequency Periodic Signaling (LFPS) generation and detection in USB3.0 Mode
- Support COMWAKE, COMINIT and COMRESET (OOB) generation and detection in SATA Mode
- Support L1 sub-state power management
- Support RX low latency mode in SATA operation mode
- Support Loopback BERT and Multiple Pattern BIST Mode

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17.2 Block Diagram

17.2.1 Combo PIPE PHY Function Description

17.2.1.1 Block Diagram and Description

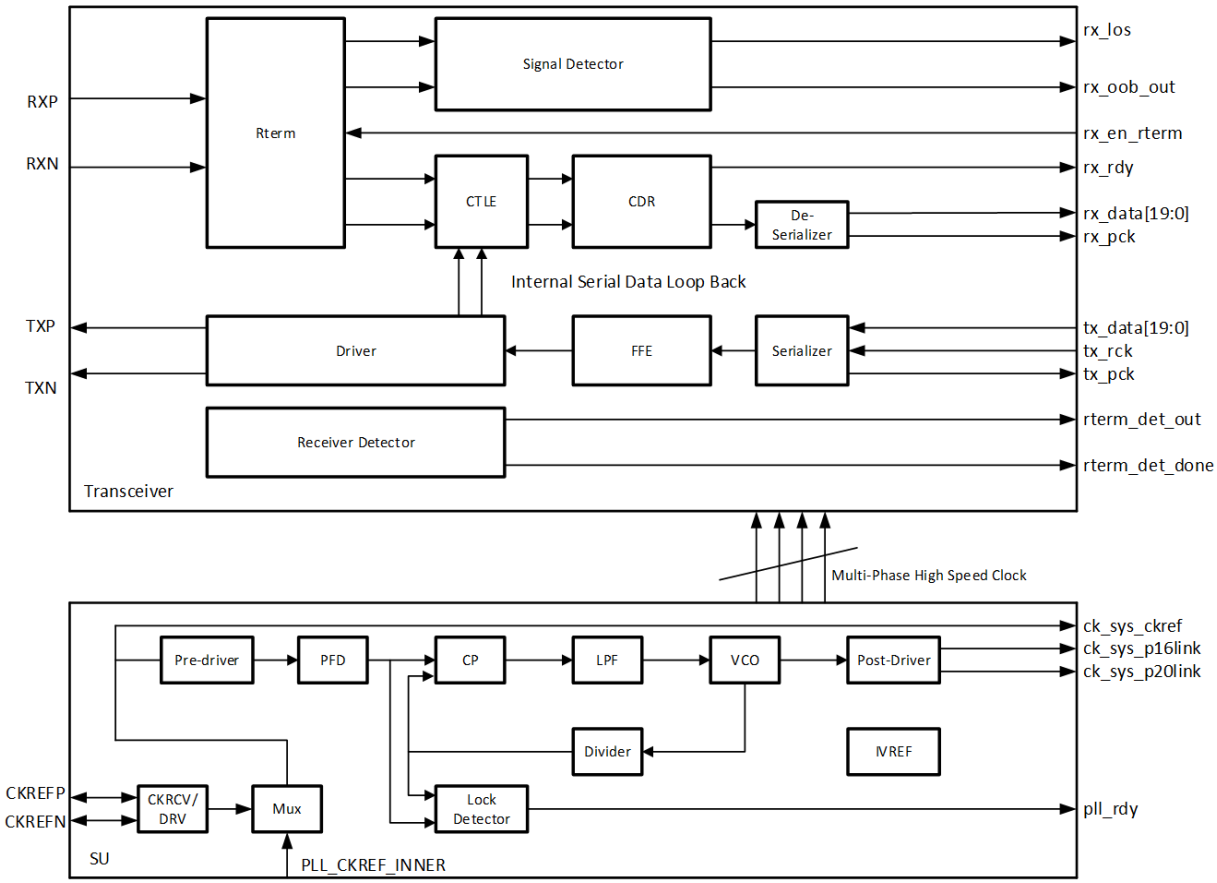


Fig. 17-1 PMA Block Diagram of Multi-PHY

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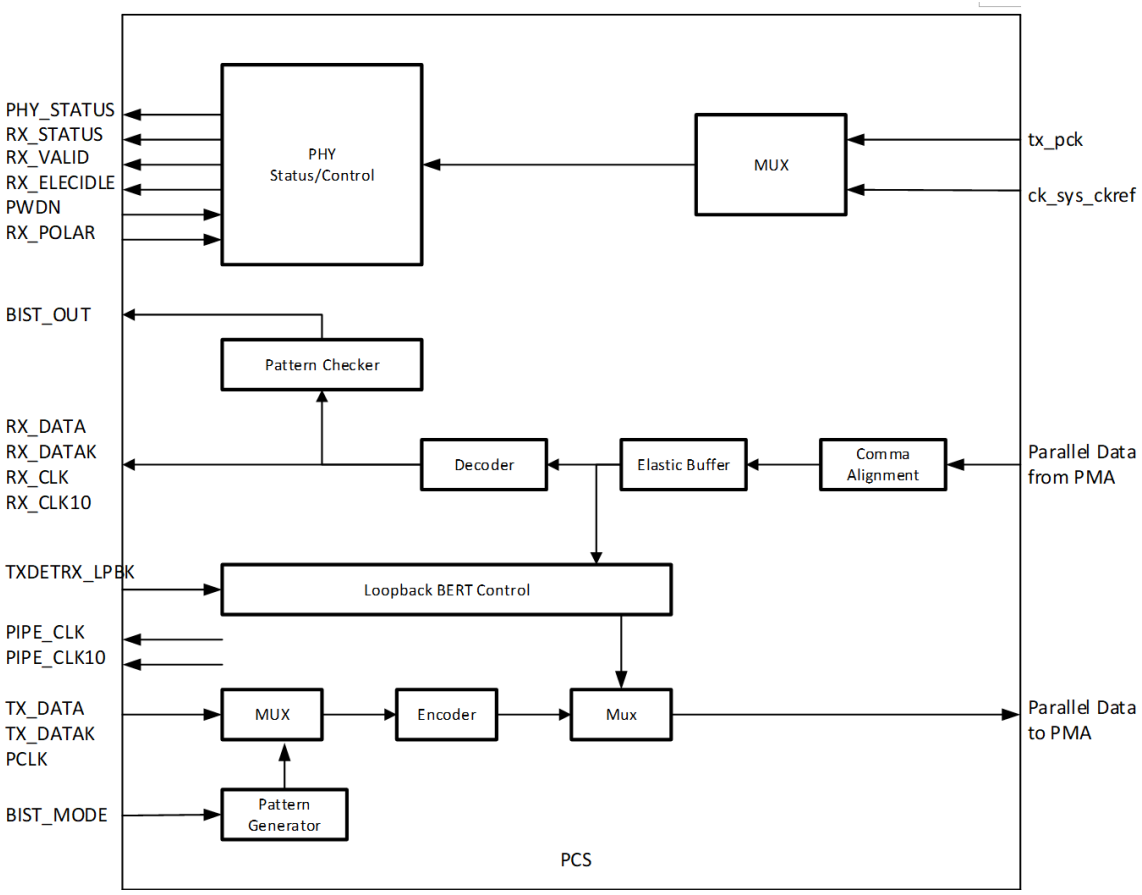


Fig. 17-2 PCS Block Diagram of Multi-PHY

Combo PIPE PHY includes two major blocks, PMA and PCS. PMA is an analog macro to perform serial to parallel and parallel to serial conversion. PMA includes three blocks, Transmitter, Receiver and SU(includes PLL, IVREF, etc.). PCS is a digital synthesis macro to perform PHY coding sub-layer function like 8bit/10bit code and decode, elastic buffer, comma alignment and BERT loopback, it also includes a register interface to access internal control registers with APB interface.

17.2.1.2 SHARED UNIT (SU)

PLL takes reference clock input from CKREFP/N and PLL_CKREF_INNER, to generate a high-speed clock for data transmission and clock data recovery. The high-speed clock generated by PLL could be SSC (spectrum spread clock) modulated if SSC mode is turned on. When SSC is enabled, the PHY is transmitting spread-spectrum serial data with frequency offset in 31.5KHz periodically.

IVREF includes a voltage and current reference generator, which comprises a Bandgap Reference and a Voltage Regulator. Reference voltage and current are generated for internal circuit usage. IVREF block is always on as long as IP power up, it will consume ~170uA static current all the time.

CKDRV is an input/output differential clock buffer, when it is used as input, it can receive a wide range differential reference clock. When used as output, CKDRV can drive a 100MHz differential clock for PCIE host application.

17.2.1.3 TRANSMITTER (TX)

The Serializer block converts parallel data from PHY PCS to high-speed serial data by using high speed clock generated by PLL. A feed forward equalizer (FFE) is implemented to compensate channel ISI.

Driver will convert the serial data to differential signal on TXP/TXM, also the driver will transmit Beacon Signal (PCIE2.0), OOB(SATA) or LFPS(USB3.0) signaling. The differential

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output amplitude and Deemphasis level can be programmed via setting PIPE3 control pins TX_SWING, TX_DEEMPH[2:0] and TX_MARGIN[2:0].

The receiver detector will be used to detect the far-end receiver present or not.

17.2.1.4 RECEIVER (RX)

The CTLE (Continuous Time Linear Equalizer) is used to compensate channel loss and cancel ISI of the input signals by boosting high frequency gain. The CTLE can be set to adaptive mode or manual setting mode.

The CDR (Clock and Data Recover) tracks input data stream and generate recovered clock for data de-serializer. De-Serializer converts incoming serial bit stream recovered by CDR into a synchronized parallel data bus and forward it to PHY PCS block.

The Signal Detector detects OOB/LFPS on the RX input pair.

17.2.1.5 PCS

PCS module is a pure digital synthesis module, it works as an interface between PMA and MAC, it accomplishes functions including comma alignment, 8bit/10bit code/decode, elastic buffer, power control and IP testing. This module also includes an APB interface for accessing PHY control registers. PCS is fully compatible with the PIPE3 interface of "PHY interface for PCI express and USB3.0 architecture by intel".

17.2.2 PHY and Controller Mapping

Combo PIPE PHY0: PCIe0/SATA0
Combo PIPE PHY1: PCIe1/SATA1/USB3_OTG1

17.3 Function Description

N/A

17.4 Register Description

17.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
COMBO_PIPE_PHY0	0x2B050000
COMBO_PIPE_PHY1	0x2B060000

17.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
COMBO_PIPE_PHY_REG_000	0x0000	W	0x00000000	Combo PHY Register 0
COMBO_PIPE_PHY_REG_001	0x0004	W	0x00000080	Combo PHY Register 1
COMBO_PIPE_PHY_REG_002	0x0008	W	0x000000FF	Combo PHY Register 2
COMBO_PIPE_PHY_REG_003	0x000C	W	0x00000000	Combo PHY Register 3
COMBO_PIPE_PHY_REG_004	0x0010	W	0x00000000	Combo PHY Register 4
COMBO_PIPE_PHY_REG_005	0x0014	W	0x00000000	Combo PHY Register 5

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Name	Offset	Size	Reset Value	Description
COMBO_PIPE_PHY_REG_006	0x0018	W	0x00000088	Combo PHY Register 6
COMBO_PIPE_PHY_REG_007	0x001C	W	0x00000008	Combo PHY Register 7
COMBO_PIPE_PHY_REG_008	0x0020	W	0x00000060	Combo PHY Register 8
COMBO_PIPE_PHY_REG_009	0x0024	W	0x00000009	Combo PHY Register 9
COMBO_PIPE_PHY_REG_010	0x0028	W	0x00000093	Combo PHY Register 10
COMBO_PIPE_PHY_REG_011	0x002C	W	0x00000002	Combo PHY Register 11
COMBO_PIPE_PHY_REG_012	0x0030	W	0x00000008	Combo PHY Register 12
COMBO_PIPE_PHY_REG_013	0x0034	W	0x00000059	Combo PHY Register 13
COMBO_PIPE_PHY_REG_014	0x0038	W	0x00000040	Combo PHY Register 14
COMBO_PIPE_PHY_REG_015	0x003C	W	0x00000063	Combo PHY Register 15
COMBO_PIPE_PHY_REG_016	0x0040	W	0x00000000	Combo PHY Register 16
COMBO_PIPE_PHY_REG_017	0x0044	W	0x00000032	Combo PHY Register 17
COMBO_PIPE_PHY_REG_018	0x0048	W	0x0000009B	Combo PHY Register 18
COMBO_PIPE_PHY_REG_019	0x004C	W	0x00000047	Combo PHY Register 19
COMBO_PIPE_PHY_REG_020	0x0050	W	0x0000000B	Combo PHY Register 20
COMBO_PIPE_PHY_REG_021	0x0054	W	0x00000041	Combo PHY Register 21
COMBO_PIPE_PHY_REG_022	0x0058	W	0x0000002C	Combo PHY Register 22
COMBO_PIPE_PHY_REG_023	0x005C	W	0x00000030	Combo PHY Register 23
COMBO_PIPE_PHY_REG_024	0x0060	W	0x00000000	Combo PHY Register 24
COMBO_PIPE_PHY_REG_025	0x0064	W	0x00000000	Combo PHY Register 25
COMBO_PIPE_PHY_REG_026	0x0068	W	0x00000014	Combo PHY Register 26
COMBO_PIPE_PHY_REG_027	0x006C	W	0x00000000	Combo PHY Register 27
COMBO_PIPE_PHY_REG_028	0x0070	W	0x00000005	Combo PHY Register 28
COMBO_PIPE_PHY_REG_029	0x0074	W	0x00000040	Combo PHY Register 29
COMBO_PIPE_PHY_REG_030	0x0078	W	0x00000000	Combo PHY Register 30
COMBO_PIPE_PHY_REG_031	0x007C	W	0x00000010	Combo PHY Register 31
COMBO_PIPE_PHY_REG_032	0x0080	W	0x00000000	Combo PHY Register 32

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Name	Offset	Size	Reset Value	Description
COMBO_PIPE_PHY_REG_033	0x0084	W	0x00000000	Combo PHY Register 33
COMBO_PIPE_PHY_REG_034	0x0088	W	0x00000000	Combo PHY Register 34
COMBO_PIPE_PHY_REG_035	0x008C	W	0x00000000	Combo PHY Register 35
COMBO_PIPE_PHY_REG_036	0x0090	W	0x00000000	Combo PHY Register 36
COMBO_PIPE_PHY_REG_037	0x0094	W	0x00000000	Combo PHY Register 37
COMBO_PIPE_PHY_REG_038	0x0098	W	0x00000000	Combo PHY Register 38
COMBO_PIPE_PHY_REG_039	0x009C	W	0x00000000	Combo PHY Register 39
COMBO_PIPE_PHY_REG_040	0x00A0	W	0x00000000	Combo PHY Register 40
COMBO_PIPE_PHY_REG_041	0x00A4	W	0x00000000	Combo PHY Register 41
COMBO_PIPE_PHY_REG_042	0x00A8	W	0x00000000	Combo PHY Register 42
COMBO_PIPE_PHY_REG_043	0x00AC	W	0x00000000	Combo PHY Register 43
COMBO_PIPE_PHY_REG_044	0x00B0	W	0x00000000	Combo PHY Register 44
COMBO_PIPE_PHY_REG_045	0x00B4	W	0x00000000	Combo PHY Register 45
COMBO_PIPE_PHY_REG_046	0x00B8	W	0x00000000	Combo PHY Register 46
COMBO_PIPE_PHY_REG_047	0x00BC	W	0x00000000	Combo PHY Register 47
COMBO_PIPE_PHY_REG_048	0x00C0	W	0x00000000	Combo PHY Register 48
COMBO_PIPE_PHY_REG_049	0x00C4	W	0x00000000	Combo PHY Register 49

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

17.4.3 Detail Registers Description

COMBO_PIPE_PHY_REG_000

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	clk_out_sel Select which internal clock connect to output test_clk 1'b0: TXPLL clock/4 1'b1: RXCDR clock/4
6	RW	0x0	inv_txpll_clk 1'b1: Invert the PLL clock from PHY to PCS in PCS
5	RW	0x0	inv_rxcdr_clk 1'b1: Invert the CDR clock from PHY to PCS in PCS
4:0	RO	0x00	reserved

COMBO_PIPE_PHY_REG_001

Address: **Operational Base** + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x2	pwdn_ctrl_l [0]: If 1, PHY block power controlled by pwon** signals instead of PIPE signals [1]: Enable IVREF in PMA when pwdn_ctrl[0]=1
5:1	RO	0x00	reserved
0	RW	0x0	custom_specific Used to select which of operation2 or operation3 L1 SSTM the PHY interface would act as

COMBO_PIPE_PHY_REG_002

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xff	pwdn_ctrl_h [2]: Enable PWON_TX_BUF to power on TX driver in PMA pwdn_ctrl[0]=1 [3]: Enable PWON_TXPLL to power on PLL in PMA pwdn_ctrl[0]=1 [4]: Enable PWON_IDLE_DET to power on PCIE EIDLE detect driver in PMA pwdn_ctrl[0]=1 [5]: Enable PWON_LFPS_DET to power on USB LFPS detect in PMA pwdn_ctr[0]=1 [6]: Enable PWON_RX_BUF to power on RX CTLE in PMA pwdn_ctrl[0]=1 [7]: Enable PWON_CDR to power on RX CDR in PMA pwdn_ctrl[0]=1 [8]: Enable PWON_OOB_DET to power on SATA OOB detect in PMA pwdn_ctr[0]=1 [9]: Enable PWON_HS_DET to power on SATA high speed data detect in PMA pwdn_ctrl[0]=1

COMBO_PIPE_PHY_REG_003

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	rx_rterm_vcom RX vcom voltage select signal 2'b00: GND 2'b01, 2'b10: Floating 2'b11: 320mV
5:3	RW	0x0	tx_rate bit[2]: PMA tx_rate source selects. 1'b0: Source from PIPE 1'b1: Source from APB bit[1:0]: tx_rate control
2:0	RW	0x0	rx_rate bit[2]: PMA rx_rate source selects. 1'b0: Source from PIPE 1'b1: Source from APB bit[1:0]: rx_rate control

COMBO_PIPE_PHY_REG_004

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6:3	RO	0x0	bist_mode IP bist mode control
2:0	RO	0x0	reserved

COMBO_PIPE_PHY_REG_005

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	pll_ckref_div PLL input clock divider, valid when su_trim[14]=1 2'b00: 1 2'b01: 1/2 2'b10: 1/3 2'b11: 1/4
5:3	RW	0x0	rate bit[2]: PMA PLL rate source selects. 1'b0: Source from PIPE 1'b1: Source from APB bit[1:0]: PLL rate control
2:0	RW	0x0	phy_mode bit[2]: PMA phy_mode source selects. 1'b0: Source from PIPE 1'b1: Source from APB bit[1:0]: Phy model control.

COMBO_PIPE_PHY_REG_006

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x8	tx_rterm TX output resister adjust signal by step about 1ohm 4'h0: 60 4'h8: 50 4'hf: 44 Others: Reserved
3:0	RW	0x8	rx_rterm RX input resister adjust signal by step about 1ohm 4'h0: 60 4'h8: 50 4'hf: 43.5 Others: Reserved

COMBO_PIPE_PHY_REG_007

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	byps_cdr_en 1'b0: CDR recovered clock will be operation while PLL is locked and CDR is operation, and rx_cdr_trim[7] only can be set to 1'b0 using reference clock for rx_rdy generation. 1'b1: CDR recovered clock will be operation while PLL is locked, and rx_cdr_trim[7] can be set to 1'b1 using recovered clock for rx_rdy generation.
6	RW	0x0	tx_swing Tx_swing control.

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Bit	Attr	Reset Value	Description
5	RW	0x0	near_end_lpk_enable PHY Near end loop back enable in BIST mode.
4	RW	0x0	ssc_en In USB3 and SATA mode, this bit= 1, set SSC on. In PCIE mode, this bit=0 set SSC off.
3:0	RW	0x8	tx_swing_com TX boost level adjust signal 3'b000: Minimum 3'b111: Maximum

COMBO_PIPE_PHY_REG_008

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	byps_cdr_fl_en 1'b0: rx_rdy is pulse signal to indicate CDR start to clock and data recovered from input serial data. 1'b1: rx_rdy is not controlled by PMA/PCS interface signal "cdr_fl_en".
6	RW	0x1	byps_cpath_limit 1'b0: CDR CPATH will be reset while CDR CPATH is overflow. 1'b1: CDR CPATH will be locked to MAX frequency offset while CDR CPATH is overflow.
5	RW	0x1	byps_capth_overflow 1'b0: CDR CPATH is controlled by CDR CPATH overflow. 1'b1: CDR CPATH is not controlled by CDR CPATH overflow.
4	RW	0x0	byps_fgain_adpt 1'b0: CDR CPATH gain is X2 while CDR recover frequency while rx_cdr_trim[6]=0. 1'b1: CDR CPATH gain is X1 while CDR recover frequency while rx_cdr_trim[6]=0.
3	RW	0x0	byps_pwon_rx_buf 1'b0: CTLE and LOS detector is controlled by PWDN[1:0]. 1'b1: CTLE and LOS detector is operation while reference clock and RX termination is present.
2	RW	0x0	byps_pown_rx_cdr 1'b0: CDR is controlled by PWDN[1:0]. 1'b1: CDR is operation after PLL is locked while reference clock and RX termination is present.
1	RW	0x0	byps_pwon_tx_buf 1'b0: TX Driver is controlled by PWDN[1:0]. 1'b1: TX Driver is operation after PLL is locked while reference clock is present, and TX detect RX is finished.
0	RW	0x0	byps_resetn 1'b0: PMA is reset by RSTN. 1'b1: PMA is not controlled by RSTN.

COMBO_PIPE_PHY_REG_009

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	byps_rterm_en 1'b0: RX termination is controlled by RTERM_EN. 1'b1: RX termination is present all the way.
6	RW	0x0	byps_rx_cdr_idle 1'b0: CDR is reset if EIDLE is detected by LOS Detect module. 1'b1: CDR is not controlled by LOS Detect module.
5	RW	0x0	byps_rx_rdy_pulse 1'b0: rx_rdy is pulse signal. 1'b1: rx_rdy is step signal while byps_cdr_fl_en=1.
4	RW	0x0	byps_tx_eidle_en 1'b0: TX EIDLE is controlled by PMA/PCS interface signal "tx_eidle_en" (SATA Mode) or "tx_lfps_beacon_en"(PCIE/USB Mode). 1'b1: TX EIDLE is disable.
3:0	RW	0x9	ssc_ppm PLL SCC ppm adjust signal by step 500ppm. 4'h0: 0ppm 4'h1: 500ppm 4'h8: 4000ppm 4'hf: 7500ppm

COMBO_PIPE_PHY_REG_010

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x93	su_trim_bank0 SU adjust signal [2:0]: PLL KVCO adjust 3'b000: Min 3'b111: Max [3]: PLL force lock [24:23], [6:4]: PLL charge pump current adjusts 5'b00000: Min 5'b11111: Max [10:7]: PLL LPF R1 adjust 3'b000: Max 3'b111: Min [11]: bypass PLL power down control [12]: bypass ref clock detect function [13]: bypass vcntl detect [14]: bypass PLL loop divider code [15]: bypass ivref power down control [16]: bypass PLL lock detect mode of always detect [17]: bypass POR function [18]: bypass ivref power down control [19]: CKRCV common voltage adjust 1'b0: floating 1'b1: GND [21:20]: CKRCV termination resister adjust 2'b00: 100ohm 2'b01: 200ohm 2'b10: 1000ohm 2'b11: Hi-Z [22]: CKRCV mode select 1'b0: difference receiver mode 1'b1: signal receiver mode (CKREFP is valid, CKREFN is disable) [24:23]: CKRCV amp input common voltage adjust 2'b00: 480 mV 2'b01: 510 mV 2'b10: 600 mV (default) 2'b11: 660 mV [28:25]: CKDRV output swing adjust, step:50 mV 4'h0: 100 mV ..... 4'hf: 860 mV [29]: CKDRV input clock select signal, 1'b0: ck100m_pcie from PLL 1'b1: ckref from CKRCV [31:30]: CKDRV output slew rate adjusts 2'b00: Fast 2'b11: Slow

COMBO_PIPE_PHY_REG_011

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x02	su_trim_bank1 SU adjust signal [2:0]: PLL KVCO adjust 3'b000: Min 3'b111: Max [3]: PLL force lock [24:23], [6:4]: PLL charge pump current adjusts 5'b00000: Min 5'b11111: Max [10:7]: PLL LPF R1 adjust 3'b000: Max 3'b111: Min [11]: bypass PLL power down control [12]: bypass ref clock detect function [13]: bypass vcntl detect [14]: bypass PLL loop divider code [15]: bypass ivref power down control [16]: bypass PLL lock detect mode of always detect [17]: bypass POR function [18]: bypass ivref power down control [19]: CKRCV common voltage adjust 1'b0: floating 1'b1: GND [21:20]: CKRCV termination resister adjust 2'b00: 100ohm 2'b01: 200ohm 2'b10: 1000ohm 2'b11: Hi-Z [22]: CKRCV mode select 1'b0: difference receiver mode 1'b1: signal receiver mode (CKREFP is valid, CKREFN is disable) [24:23]: CKRCV amp input common voltage adjust 2'b00: 480 mV 2'b01: 510 mV 2'b10: 600 mV (default) 2'b11: 660 mV [28:25]: CKDRV output swing adjust, step:50 mV 4'h0: 100 mV ..... 4'hf: 860 mV [29]: CKDRV input clock select signal, 1'b0: ck100m_pcie from PLL 1'b1: ckref from CKRCV [31:30]: CKDRV output slew rate adjusts 2'b00: Fast 2'b11: Slow

COMBO_PIPE_PHY_REG_012

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x08	su_trim_bank2 SU adjust signal [2:0]: PLL KVCO adjust 3'b000: Min 3'b111: Max [3]: PLL force lock [24:23], [6:4]: PLL charge pump current adjusts 5'b00000: Min 5'b11111: Max [10:7]: PLL LPF R1 adjust 3'b000: Max 3'b111: Min [11]: bypass PLL power down control [12]: bypass ref clock detect function [13]: bypass vcntl detect [14]: bypass PLL loop divider code [15]: bypass ivref power down control [16]: bypass PLL lock detect mode of always detect [17]: bypass POR function [18]: bypass ivref power down control [19]: CKRCV common voltage adjust 1'b0: floating 1'b1: GND [21:20]: CKRCV termination resister adjust 2'b00: 100ohm 2'b01: 200ohm 2'b10: 1000ohm 2'b11: Hi-Z [22]: CKRCV mode select 1'b0: difference receiver mode 1'b1: signal receiver mode (CKREFP is valid, CKREFN is disable) [24:23]: CKRCV amp input common voltage adjust 2'b00: 480 mV 2'b01: 510 mV 2'b10: 600 mV (default) 2'b11: 660 mV [28:25]: CKDRV output swing adjust, step:50 mV 4'h0: 100 mV ..... 4'hf: 860 mV [29]: CKDRV input clock select signal, 1'b0: ck100m_pcie from PLL 1'b1: ckref from CKRCV [31:30]: CKDRV output slew rate adjusts 2'b00: Fast 2'b11: Slow

COMBO_PIPE_PHY_REG_013

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x59	su_trim_bank3 SU adjust signal [2:0]: PLL KVCO adjust 3'b000: Min 3'b111: Max [3]: PLL force lock [24:23], [6:4]: PLL charge pump current adjusts 5'b00000: Min 5'b11111: Max [10:7]: PLL LPF R1 adjust 3'b000: Max 3'b111: Min [11]: bypass PLL power down control [12]: bypass ref clock detect function [13]: bypass vcntl detect [14]: bypass PLL loop divider code [15]: bypass ivref power down control [16]: bypass PLL lock detect mode of always detect [17]: bypass POR function [18]: bypass ivref power down control [19]: CKRCV common voltage adjust 1'b0: floating 1'b1: GND [21:20]: CKRCV termination resister adjust 2'b00: 100ohm 2'b01: 200ohm 2'b10: 1000ohm 2'b11: Hi-Z [22]: CKRCV mode select 1'b0: difference receiver mode 1'b1: signal receiver mode (CKREFP is valid, CKREFN is disable) [24:23]: CKRCV amp input common voltage adjust 2'b00: 480 mV 2'b01: 510 mV 2'b10: 600 mV (default) 2'b11: 660 mV [28:25]: CKDRV output swing adjust, step:50 mV 4'h0: 100 mV ..... 4'hf: 860 mV [29]: CKDRV input clock select signal, 1'b0: ck100m_pcie from PLL 1'b1: ckref from CKRCV [31:30]: CKDRV output slew rate adjusts 2'b00: Fast 2'b11: Slow

COMBO_PIPE_PHY_REG_014

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:6	RW	0x1	ssc_cnt_l PLL control SSC module period When the pll_ckref_inner is 100MHz/25MHz, This signal should be set to its default value unless the user want to change the 31.5KHz SSC modulation frequency. When the pll_ckref_inner is 24MHz, this signal should be set to its default value unless the user want to change the 32.8KHz SSC modulation frequency.
5:2	RW	0x0	test_sel select the digital test signal. 4'h0: Input Reference Clock 4'h1: PLL Loopback Clock 4'h2: PLL Locked 4'h3: RX PCL enable 4'h4: RX CDR enable 4'h5: RX CTLE enable 4'h6: CDR overflow 4'h7: RX ready 4'h8: RX LFPS idle detect 4'h9: RX PCIE idle detect 4'ha: RX SATA idle detect 4'hb: RX super speed detect 4'hc: Iddq_en 4'hd: Rterm detect Others: Reserved
1	RW	0x0	rx_tseq USB Mode When asserted, it is used to instruct USB3.0 PHY to bypass normal operation and do a receiver equalization training. Please refer to PIPE3 interface and USB3.0 base spec for more detail information.
0	RW	0x0	en_adpt Adaptive Continuous Time Linear Equalizer (CTLE) enable signal 1'b0: Disable adaptive CTLE 1'b1: Enable adaptive CTLE

COMBO_PIPE_PHY_REG_015

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x63	ssc_cnt_h PLL control SSC module period When the pll_ckref_inner is 100MHz/25MHz, This signal should be set to its default value unless the user want to change the 31.5KHz SSC modulation frequency. When the pll_ckref_inner is 24MHz, this signal should be set to its default value unless the user want to change the 32.8KHz SSC modulation frequency.

COMBO_PIPE_PHY_REG_016

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	pll_div_l PLL loop divider, valid when su_trim[14]=1, [14:10] is the integer number of divider factor, and [9:0] are the decimal fraction.

COMBO_PIPE_PHY_REG_017

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	frez_apt_eq 1'b0: The adaptive equalizer will be always working when the adaptive equalizer function is enabled. 1'b1: The adaptive equalizer will freeze at its final result when equalizer training pattern transmission is done. This signal is used in USB3.1 mode, when equalizer training pattern transmission is done, IP user can stop adaptive equalization and freeze the result.
6:0	RW	0x32	pll_div_h PLL loop divider, valid when su_trim[14]=1, [14:10] is the integer number of divider factor, and [9:0] are the decimal fraction.

COMBO_PIPE_PHY_REG_018

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x2	cdr_valid_sel cdr data valid counter delay in pcs select.
5:3	RW	0x3	rx_afe_trim Receiver 2nd stage equalizer res control, used to adjust pole-zero of RX eq.
2:0	RW	0x3	rx_afe_ctrim Receiver 1st stage equalizer cap control, used to adjust pole-zero of RX EQ.

COMBO_PIPE_PHY_REG_019

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	com_det_once Disable Look for the comma location multiple times 1'b0: 5 times 1'b1: 2 times
6	RW	0x1	sata_vlaid_sel SATA mode rx_valid source selects
5	RW	0x0	beacon_timeout_sel PCIe beacon timeout select
4	RW	0x0	rx_polar RX output polarity set 1'b0: No invert RX output data polarity 1'b1: Invert RX output data polarity
3:0	RW	0x7	rx_afe_rtrim Receiver 1st stage equalizer res control, used to adjust pole-zero of RX eq.

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COMBO_PIPE_PHY_REG_020

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x0b	rx_sqdet_trim_l RX squelch adjust [2:0]: squelch input filler bandwidth adjusts 3'b000: Max bandwidth 3'b111: Min bandwidth [4:3]: squelch delay adjusts 2'b00: Max delay 2'b11: Min delay [6:5]: amp bias adjusts 2'b00: Max ibias 2'b11: Min ibias [8:7]: squelch detect vth adjust 2'b00: Min vth 2'b11: Max vth

COMBO_PIPE_PHY_REG_021

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	rx_adpt_eq_trim [2:0]: adaptive equalizer detection threshold control [3]: adaptive equalizer gain control
3:0	RW	0x1	rx_sqdet_trim_h [9]: bypass rx_superspeed 1'b1: rx_superspeed=1 [10]: rx_superspeed function selects 1'b0: ~los output 1'b1: ~los output | squelch output [11]: rx_pcie_idle function selects 1'b0: ~ squelch output 1'b1: los output

COMBO_PIPE_PHY_REG_022

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x2c	rx_adpt_eq_trim_h [6:4]: adaptive equalizer bandwidth control [8:7]: adaptive output refresh bandwidth control [9]: bypass the adaptive Cj function [10]: test mode selects [11]: Reserved

COMBO_PIPE_PHY_REG_023

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x3	rx_cdr_trim_l [3]: CDR gain adjust 1'b0: 1/4([4]=1), 1/8([4]=0) 1'b1: 1/8 [2:0]: The slew rate control for PI 3'b000: Fast slew rate 3'b111: Slow slew rate
3:0	RW	0x0	rx_los_trim RX los detect adjust [1:0]: Low vth adjust [2]: Reserved [3]: Enable signal of Los eidle reseting CDR or not 1'b0: Los eidle not reset CDR 1'b1: Los eidle reset CDR

COMBO_PIPE_PHY_REG_024

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	rx_cdr_trim_h [4]: CDR gain adjust 1'b0: 1/8 1'b1: 1/4 when rx_cdr_trim[3]=1 [5]: CDR phase path gain adjust 1'b0: x1 1'b1: x2 [6]: CDR cpath bandwidth gain adjusts 1'b0: Low bandwidth 1'b1: High bandwidth [7]: rx_rdy counter clock select 1'b0: Ref clock 1'b1: CDR recovery clock [9:8]: rx_rdy delay time select 2'b00: 1.28us 2'b01: 0.64us 2'b10: 2.56us 2'b11: 5.12us [11:10]: Reserved

COMBO_PIPE_PHY_REG_025

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	tx_trim_l TX adjust [3:0]: TX FFE adjust valid when tx_trim[4]=1 [4]: Manual mode enable [5]: Force rterm detect ready 1'b1: Force rtern_det_out=1 [6]: Force eidle 1'b1: txp/txm is eidle [7]: hi-z idle enable [8]: tx_pck invert enable [9]: MSB enable [10]: Bypass low resister eidle mode 1'b0: Eidle has not hi-z mode 1'b1: Eidle has hi-z mode [11]: Bypass 0.6kohm charge resister 1'b0: 0.6kohm resister 1'b1: 1kohm resister [13:12]: Rterm detect vth adjust 2'b00: Max vth 2'b11: Min vth [14]: Bypass signal of gate_tx_pck

COMBO_PIPE_PHY_REG_026

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x14	tx_trim_h TX adjust [3:0]: TX FFE adjust valid when tx_trim[4]=1 [4]: Manual mode enable [5]: Force rterm detect ready 1'b1: Force rtern_det_out=1 [6]: Force eidle 1'b1: txp/txm is eidle [7]: hi-z idle enable [8]: tx_pck invert enable [9]: MSB enable [10]: Bypass low resister eidle mode 1'b0: Eidle has not hi-z mode 1'b1: Eidle has hi-z mode [11]: Bypass 0.6kohm charge resister 1'b0: 0.6kohm resister 1'b1: 1kohm resister [13:12]: Rterm detect vth adjust 2'b00: Max vth 2'b11: Min vth [14]: Bypass signal of gate_tx_pck

COMBO_PIPE_PHY_REG_027

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	rx_trim [0]: rx_pck invert enable [1]: RX MSB enable [3:2]: PLL LPF C1 adjust signal 2'b00: 20pf 2'b01: 40pf 2;b10: 65pf 2'b11: 85pf [5:4]: PLL loop's divider factor(pre-divider) adjust signal 2'b00, 2'b01: 1 2'b10: 2 2'b11: 4 [6]: PLL LPF R1 fine-adjust signal 1'b0: Disable(2.5kohm by step) 1'b1: Enable(1.25kohm by step) [7]: Reserved

COMBO_PIPE_PHY_REG_028

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	tx_margin Tx margin control
4:0	RW	0x05	rterm_det_trim [1:0]: rterm detect pre-charge time adjust 2'b00: 512us 2'b11: 4096us [3:2]: rterm detect post-charge time adjust 2'b00: 8us 2'b11: 64us [4]: Reserved

COMBO_PIPE_PHY_REG_029

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	unused_name1_bank0 Bit[3]: gate_tx_pck_sel length select Bit[2]: Reserved Bit[1]: Bypass idle det in PCIe P1.1 and P1.2 Bit[0]: SATA align detect logic output select
3	RW	0x0	bist_out_sel Reserved
2:0	RW	0x0	tx_deemph Tx_deemph control

COMBO_PIPE_PHY_REG_030

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	testo_sel pcs internal signal to testo io select

COMBO_PIPE_PHY_REG_031

Address: **Operational Base** + offset (0x007C)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x10	register_bank0 [0]: bypass the mode of pd_ck100m controlling CKDRV 1'b0: CKDRV is on only in PCIE mode 1'b1: CKDRV is controlled by ckref_src[1:0] [2:1]: CKDRV output slew rate adjusts 2'b00: Fast 2'b11: Slow [3]: 50ohm termination disable signal in CKREP/N TX mode 1'b0: Not disable 1'b1: Disable mode [5:4]: Select signal of SSC direction 2'b00: Up spread spectrum 2'b01: Down spread spectrum 2'b10: Illegal 2'b11: Intermediate spread spectrum [7:6]: SSC offset compensation 2'b00: 0ppm 2'b01: +500ppm 2'b10, 2'b11: -500ppm [8]: pll_rdy delay control when rate change 1'b0: Delay 3*TX_PCK relative to the falling edge of gate_tx_pck 1'b1: Delay about 20us relative to the falling edge of gate_tx_pck [9]: Select pll_lock to TX/RX 1'b0: pll_lock_txrx is same to pll_lock_pcs 1'b1: pll_lock_txrx is not controled by gate_tx_pck [12:10]: PLL KVCO fine tuning signals [13]: PLL control SSC module period [15:14]: Reserved

COMBO_PIPE_PHY_REG_032

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	register_bank1 [0]: bypass the mode of pd_ck100m controlling CKDRV 1'b0: CKDRV is on only in PCIE mode 1'b1: CKDRV is controlled by ckref_src[1:0] [2:1]: CKDRV output slew rate adjusts 2'b00: Fast 2'b11: Slow [3]: 50ohm termination disable signal in CKREP/N TX mode 1'b0: Not disable 1'b1: Disable mode [5:4]: Select signal of SSC direction 2'b00: Up spread spectrum 2'b01: Down spread spectrum 2'b10: Illegal 2'b11: Intermediate spread spectrum [7:6]: SSC offset compensation 2'b00: 0ppm 2'b01: +500ppm 2'b10, 2'b11: -500ppm [8]: pll_rdy delay control when rate change 1'b0: Delay 3*TX_PCK relative to the falling edge of gate_tx_pck 1'b1: Delay about 20us relative to the falling edge of gate_tx_pck [9]: Select pll_lock to TX/RX 1'b0: pll_lock_txrx is same to pll_lock_pcs 1'b1: pll_lock_txrx is not controled by gate_tx_pck [12:10]: PLL KVCO fine tuning signals [13]: PLL control SSC module period [15:14]: Reserved

COMBO_PIPE_PHY_REG_033

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	COMMA_DET Comma detect
5	RO	0x0	COMMA_RECEIVED Comma received
4	RO	0x0	CDR_DATA_VALID CDR data valid
3	RO	0x0	RX_SUPERSPEED RX super speed
2	RO	0x0	DET_FINISH_PUSE Detection finish
1	RO	0x0	SKP_REMOVED SKP removed
0	RO	0x0	SKP_INSERTED SKP inserted

COMBO_PIPE_PHY_REG_034

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	EB_OF Ebuffer overflow

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Bit	Attr	Reset Value	Description
6	RO	0x0	EB_UF Ebuffer underflow
5:4	RO	0x0	DISPARITY_ERR Dsiparity error
3:2	RO	0x0	INVALID_CODE Invalid code
1:0	RO	0x0	BRST_SYM BRST_SYM

COMBO_PIPE_PHY_REG_035

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	NO_ERR NO_ERR
6	RO	0x0	BIST_RESULT BIST result
5	RO	0x0	TEST_DONE Test done
4	RO	0x0	RX_ELECIDLE_O RX electrical idle
3	RO	0x0	BIST_DONE BIST done
2	RO	0x0	BIST_TIMEOUT BIST timeout
1	RO	0x0	DET_FINSH Detect finish
0	RO	0x0	DET_RESULT Detect result

COMBO_PIPE_PHY_REG_036

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	ERR_CNT Error count

COMBO_PIPE_PHY_REG_037

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:2	RO	0x00	MAX_JITTER Max jitter
1	RO	0x0	CDR_FL_EN CDR_FL_EN
0	RO	0x0	CDR_FREQ_LK CDR frequency lock

COMBO_PIPE_PHY_REG_038

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	USB3_MODE USB3_MODE

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Bit	Attr	Reset Value	Description
5	RO	0x0	SATA_MODE SATA_MODE
4	RO	0x0	PCIE_MODE PCIE_MODE
3	RO	0x0	BEACON_LFPS BEACON_LFPS
2	RO	0x0	TX_DET_RX_0 TX_DET_RX_0
1	RO	0x0	GAT_PLL_CLK GAT_PLL_CLK
0	RO	0x0	SS_MODULE SS_MODULE

COMBO_PIPE_PHY_REG_039

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	RATE_1_O RATE_1_O
6	RO	0x0	RATE_0_O RATE_0_O
5	RO	0x0	RATE_TX_1 RATE_TX_1
4	RO	0x0	RATE_TX_0 RATE_TX_0
3	RO	0x0	RATE_RX_1 RATE_RX_1
2	RO	0x0	RATE_RX_0 RATE_RX_0
1	RO	0x0	PWON_PLL_O PWON_PLL_O
0	RO	0x0	TXPLL_LOCK TX PLL lock

COMBO_PIPE_PHY_REG_040

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	PWON_IREF PWON_IREF
6	RO	0x0	PWON_LFPS_DET PWON_LFPS_DET
5	RO	0x0	PWON_IDLE_DET PWON_IDLE_DET
4	RO	0x0	PWON_OOB_DET PWON_OOB_DET
3	RO	0x0	PWON_HS_DET PWON_HS_DET
2	RO	0x0	PWON_RX_BUS PWON_TX_BUF
1	RO	0x0	PWON_TX_BUF PWON_TX_BUF
0	RO	0x0	PWON_CDR_O PWON_CDR_O

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COMBO_PIPE_PHY_REG_041

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	RX_DETECEED RX_DETECEED
5	RO	0x0	RX_LFPS_I RX_LFPS_I
4	RO	0x0	RX_SUPERSPEED RX_SUPERSPEED
3	RO	0x0	RX_SATA_IDLE RX_SATA_IDLE
2	RO	0x0	RX_PCIE_IDLE RX_PCIE_IDLE
1	RO	0x0	RX_ELECIDLE RX_ELECIDLE
0	RO	0x0	RX_VALID RX_VALID

COMBO_PIPE_PHY_REG_042

Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RO	0x0	REFCK_DET_OUT REFCK_DET_OUT
5	RO	0x0	RTERM_DET_OUT RTERM_DET_OUT
4	RO	0x0	RX_ADPE_EQ_FL RX_ADPE_EQ_FL
3:0	RO	0x0	RX_ADPT_EQ_TRIM RX_ADPT_EQ_TRIM

COMBO_PIPE_PHY_REG_043

Address: **Operational Base** + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RO	0x0	BERC_SYM BERC_SYM
4	RO	0x0	LP_RX_EN LP_RX_EN
3	RO	0x0	LP_SLAVE_EN LP_SLAVE_EN
2:0	RO	0x0	RX_ADPT_EQ_CTRIM RX_ADPT_EQ_CTRIM

COMBO_PIPE_PHY_REG_044

Address: **Operational Base** + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	RX_DEBUG_R RX_DEBUG_R

COMBO_PIPE_PHY_REG_045

Address: **Operational Base** + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	UNUSED_DEBUG RX_DEBUG_R

COMBO_PIPE_PHY_REG_046

Address: **Operational Base** + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	unused_name1_bank1 bit[5]: phy clk_src source selects 1'b0: Source from APB 1'b1: Source from SOC bit[4:3]: phy clk_src control bit[2]: IP BIST_MODE source selects 1'b0: Source from APB 1'b1: Source from SOC bit[1:0]: rx_supperspeed delay selects: 2'b00: Delay 2 reference clock cycles 2'b01: Delay 6 reference clock cycles 2'b10: Delay 8 reference clock cycles 2'b11: Delay 10 reference clock cycles

COMBO_PIPE_PHY_REG_047

Address: **Operational Base** + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	unused_name1_bank2 bit[7]: bypass PHY power down in p1.2 with PCIe mode 1'b0: Disable 1'b1: Enable bit[6]: mac_interface module data valid input source selects 1'b0: CDR lock from PMA 1'b1: Data valid generation by cdr_ctrl module bit[5]: PMA tx_deemph control source selects 1'b0: Source from PCS 1'b1: From APB config bit[4]: PMA tx_margin control source selects 1'b0: Source from PCS 1'b1: From APB config bit[3]: PMA tx_swing control source selects 1'b0: Source from PCS 1'b1: From APB config bit[2]: Reserved bit[1]: RX_STANDY_O output selects 1'b0: rx_standby_o active when rx_standby assert 1'b1: rx_standby_o normal output when rx_standby dis-assert bit[0]: Bypass com_det module sata_mode input when PHY in general serdes model 1'b0: Not SATA mode 1'b1: SATA mode

COMBO_PIPE_PHY_REG_048

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	register_bank2 Reserved

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COMBO_PIPE_PHY_REG_049

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	register_bank3 Reserved

17.5 Interface Description

Table 17-1 Combo PIPE PHY 0 Analog IO Interface Description

Module Pin	Dir	Pin Name	IOMUX Setting
AVDH	I/O	PCIE0_SATA0_AVDD1V8	N/A
AVDL	I/O	PCIE0_SATA0_AVDD0V85	N/A
CKREFN	I/O	PCIE0_REFCLKN	N/A
CKREFP	I/O	PCIE0_REFCLKN	N/A
RXN	I	PCIE0_RXN/SATA0_RXN	N/A
RXP	I	PCIE0_RXP/SATA0_RXP	N/A
TXN	O	PCIE0_TXN/SATA0_TXN	N/A
TXP	O	PCIE0_TXP/SATA0_TXP	N/A

*Notes: **I**=input, **O**=output, **I/O**=input/output, bidirectional.*

Table 17-2 Combo PIPE PHY 1 Analog IO Interface Description

Module Pin	Dir	Pin Name	IOMUX Setting
AVDH	I/O	PCIE1_SATA1_USB3_OTG1_AVDD1V8	N/A
AVDL	I/O	PCIE1_SATA1_USB3_OTG1_AVDD0V85	N/A
CKREFN	I/O	PCIE1_REFCLKN	N/A
CKREFP	I/O	PCIE1_REFCLKP	N/A
RXN	I	PCIE1_RXN/SATA1_RXN/USB3_OTG1_SSRXN	N/A
RXP	I	PCIE1_RXP/SATA1_RXP/USB3_OTG1_SSRXP	N/A
TXN	O	PCIE1_TXN/SATA1_TXN/USB3_OTG1_SSTXN	N/A
TXP	O	PCIE1_TXP/SATA1_TXP/USB3_OTG1_SSTXP	N/A

*Notes: **I**=input, **O**=output, **I/O**=input/output, bidirectional.*

17.6 Application Notes

17.6.1 Combo PHY Application Note

17.6.1.1 Operation Mode Support

The following mode are supported for IP operation, IP configuration other than this list are not supported.

Table 17-3 PHY operation mode

PHY_MODE	RATE	BUS_WIDTH	PHY Operation Mode
00	00	00	PCIe Gen1, 32bit, PCLK=62.5M
		01	N/A
	01	00	PCIe Gen2, 32bit, PCLK=125M
		01	N/A
01	00	00	USB3.0, 32bit, PCLK=125M
01	00	01	N/A
10	00	00	N/A
		01	SATA Gen1, 16bit, PCLK=75M

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PHY_MODE	RATE	BUS_WIDTH	PHY Operation Mode
	01	00	N/A
		01	SATA Gen2, 16bit, PCLK=150M
	10	00	N/A
		01	SATA Gen3, 16bit, PCLK=300M

- PHY_MODE is configured by COMBO_PIPE_PHY_GRF_PIPE_CON0.pipe_phymode
- RATE is controlled by protocol controller or can be configured COMBO_PIPE_PHY_GRF_PIPE_CON0.pipe_rate when override is enabled
- BUS_WIDTH is controlled by protocol controller or can be configured COMBO_PIPE_PHY_GRF_PIPE_CON0.pipe_databuswidth when override is enabled

17.6.1.2 Power Down Mode

Power down control signals to individual analog modules are generated based on PWDN[1:0] setting from PIPE inputs as shown in below table. An override function is provided for debug purpose, see COMBO_PIPE_PHY register list. (√ – active; ×– power down)

Table 17-4 PCIE power down mode

PWDN[3:0]	TX_ELECIDLE	TX_Buffer	RX_Buffer	CDR	TX_PLL
0000	--	√	√	√	√
0001	0(illegal)	√	√	√	√
	1	×	√	√	√
0010	0(illegal)	√	×	×	√
	1	×	×	×	√
0011	0	√	×	×	×
	1	×	×	×	×
1---	0(illegal)	√	×	×	×
	1	×	×	×	×

In PCIe mode, power for IVREF and PCIe idle detector are always on, while power for LFPS, 1.5G SATA idle and 3G/6G SATA idle detectors are always off, and power of Rx buffer is off when RX_STANDBY is high.

Note: If TX_ELECIDLE(pipe_txelecidle) and TX_COMPLIANCE(pipe_txcompliance) is both asserted, all powers are off.

Table 17-5 USB3 power down mode

PWDN[3:0]	TX_ELECIDLE	TX_Buffer	RX_Buffer	CDR	TX_PLL
0000	--	√	√	√	√
0001	0	√	√	×	√
	1	√	√	×	√
0010	0	√	√	×	√
	1	√	√	×	√
0011	0	√	√	×	×
	1	×	√	×	×

In USB3.0 mode, power for IVREF and LFPS detector are always on, while power for PCIe idle, 1.5G SATA idle and 3G/6G SATA idle detectors are always off, and power of LFPS detector and power of Rx buffer are turned off if termination is not on.

17.6.1.3 Reference Clock

Combo PIPE PHY's reference clock source can be selected from either PLL_CKREF_INNER or PCIE20_REFCLKN/P, according to the status CKREF_SRC[1:0] after the PHY de-asserted reset.

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The differential pair PCIE20_REFCLKN/P can be configured as either reference clock input or reference clock output, according to CKREF_SRC[1].

Configure the register signal su_trim[29] to select reference clock(ckref) or 100MHz clock (ck100m_pcie) from PLL to drive to PCIE20_REFCLKN/P.

The CKREF_SRC is controlled by COMBO_PIPE_PHY_GRF_PIPE_CON3.phy_clk_ref_src, and the COMBO_PIPE_PHY_GRF_PIPE_CON3.phy_clk_sel is used to set the frequency of the selected reference clock.

The PLL_CKREF_INNER is derived by SoC internal CRU, refers to CRU for detail configurations to generate the appropriate reference clock.

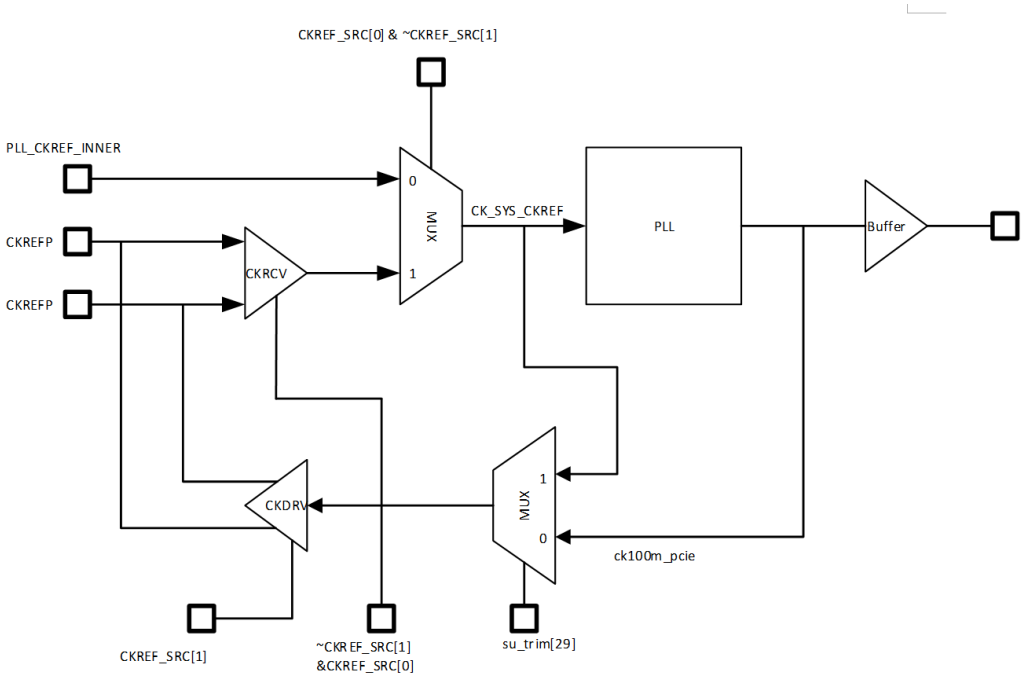


Fig. 17-3 Reference Clock Structure of Combo PIPE PHY

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Chapter 18 MIPI DSI-2 Host Controller

18.1 Overview

The Display Serial Interface 2 (DSI-2) is part of a group of communication protocols defined by the MIPI Alliance. The MIPI DSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI DSI-2 Specification.
There are one DSI2 host controller in PD_VO0 subsystem, which provide an interface between the system and MIPI D-PHY/C-PHY Combo PHY, allowing the communication with a DSI-2-compliant display.

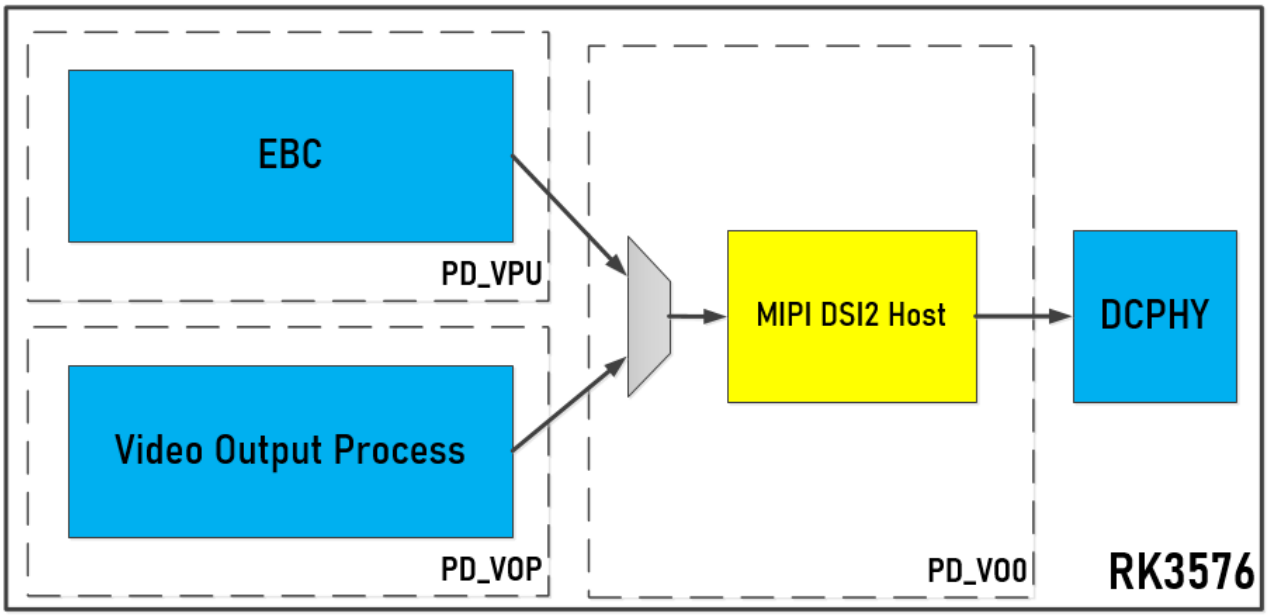


Fig. 18-1 DSI2 Host Controller In RK3576 SoC

18.2 Features

- Compliant with MIPI Alliance standards
  - MIPI® Alliance Specification for Display Serial Interface 2 (DSI-2) Version 1.1
  - MIPI® Alliance Specification for Display Command Set (DCS) Version 1.4
  - MIPI® Alliance Specification for D-PHY v2.0
  - MIPI® Alliance Specification for C-PHY v1.1
  - AMBA 3.0 Specification (APB)
- Interface with MIPI D-PHY and MIPI C-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specifications
- All commands defined in the MIPI Alliance specification for Display Command Set (DCS)
  - Request of command packets through the APB interface
  - Low-power and high-speed transmission in Video, Data Stream, and Command modes
- Up to 2.5 Gbps per lane in D-PHY
- Up to 1.7 Gsps per trio in C-PHY
- Four data lanes on D-PHY and three data trios on C-PHY
- Bidirectional communication and escape mode through data lane 0
- Continuous and non-continuous clock modes on D-PHY and non-continuous clock mode on C-PHY
- Packet header ECC/CRC and packet payload CRC Checksum capabilities
- End of Transmission packet (EoTp)
- Fault recovery schemes

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- Scrambling

18.2.1 Limitations

- The minimum region size (HAS,HBP,HACT,HFP) is 4 pixels
- HTOTAL and HACTIVE must be 4 pixel aligned
- HSYNC/HBP/HFP is suggested to be 4 pixel aligned
- When enable the EBC-DSI Host data path, only support the DSI video mode.
- The minimum value for the max_pix_pkt field of the IPI_PIX_PKT_CFG register should be 48 pixels. This applies to DataStream and Video Mode operating modes (except for Burst-Mode)
- Automatic Tear Effect is not supported, but can through I/O
- When changing from Video Mode, CRI busy must be cleared
- High-Speed clock period must be different from SYS clock period in the CPHY mode

18.2.2 Unsupported features

- Video pattern generator
- CPHY does not support the non-continuous clock mode
- EoTp is not supported in DataStream mode
- PRI calibration is not supported in CPHY
- PRI is not supported in CPHY

18.3 Function Description

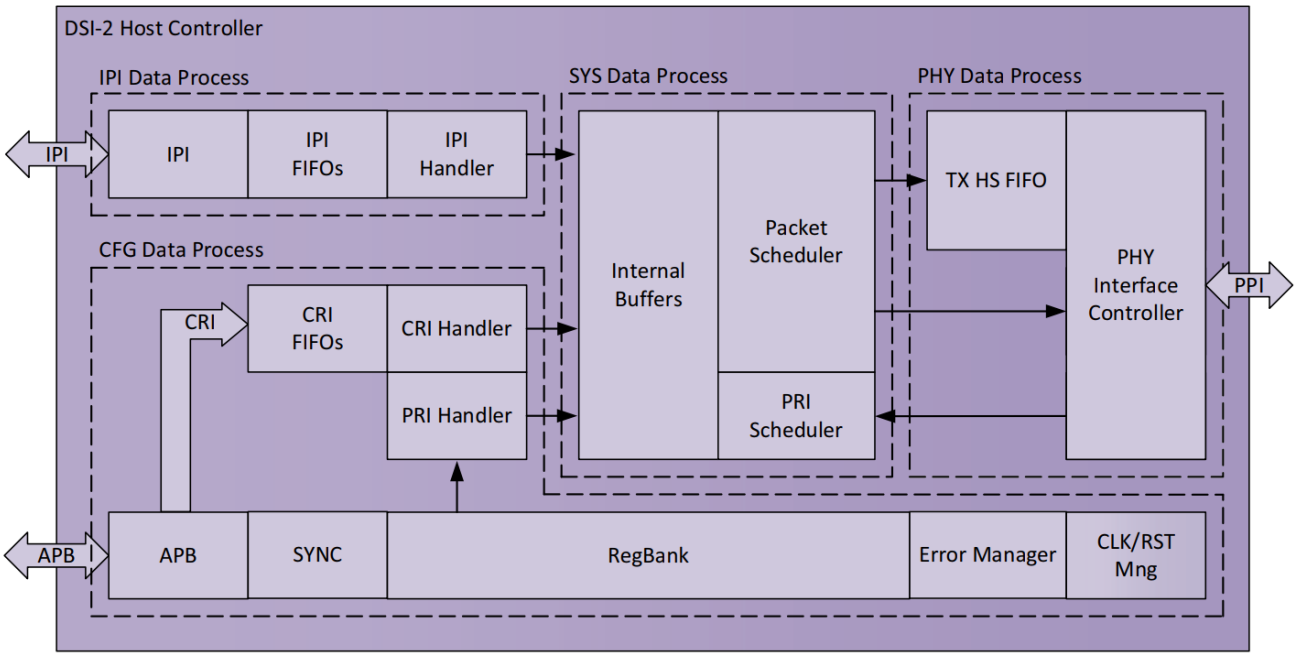


Fig. 18-2 The Architecture of MIPI DSI2 Host Controller

There are four main blocks inside MIPI DSI2 Host Controller:

- CFG Data Process
  1. Handles the AMBA APB 3 interface synchronization to sys_clk domain
  2. Stores and distributes DSI-2 Host configurations across the controller
  3. Manages clocks and resets
  4. Controls the changes between the controller operating modes and the routines for auto calculation
  5. Performs error processing

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6. Handles the CRI and PRI functional interfaces

- IPI Data Process
  1. Handles the Image Pixel Interface (IPI)
  2. Stores IPI events and IPI data into FIFOs to minimize Clock Domain Crossing (CDC) between ipi_clk and sys_clk
  3. Reorganizes IPI pixel data to DSI-2 pixel format
  4. Captures timing information
- SYS Data Process
  1. Contains the main FSMs for the different modes of operation
  2. Defines packet priorities and transmission modes
  3. Constructs the packets to be sent (header, payload, and associated ECC and CRC)
  4. Applies scrambling to the generated packets
- PHY Data Process
  1. Handles the PHY Protocol Interface (PPI)
  2. Sends high-speed data
  3. Sends and receives the low-power data
  4. Monitors PHY related timeouts

18.3.1 Controller Operating Mode

MIPI_DSI2_Host Controller has the following modes of operation:

- Idle Mode: In the Idle mode of operation
  - The controller stops data reception from the IPI, CRI, and PRI interfaces.
  - All the FIFOs are empty.
  - All the FSMs are in the INIT state.
  - There are no pending packets being transmitted or received.
- Auto-Calculation Mode: In the Auto-Calculation mode of operation, the controller
  - Stops the data reception from the IPI, CRI, and PRI interfaces.
  - Starts to calculate all the required PHY related timings.
  - Enters into the Idle mode when the procedure is complete.
- Video mode: In Video mode of operation
  - The controller accepts the IPI and CRI interfaces with IPI generating video frames.
  - The CRI interface requests are transmitted inside the video frame if there is enough time.
- Data Stream mode: In the Data Stream mode of operation, the controller
  - Accepts the IPI, CRI, and PRI interfaces with IPI generating data stream frames.
  - Prioritizes CRI over PRI and sends up to one packet from them at the end of each line from IPI.
- Command mode: In the Command mode of operation, the controller
  - Blocks the data reception from IPI.
  - Accepts CRI and PRI requests prioritizing the CRI requests

18.3.1.1 Idle Mode

Idle mode ensures that the controller is in a known and stable status with no pending packets to send, and ready to work in another operating mode. While changing the operating mode, the controller ensures that the new operating mode is preceded by the Idle mode even without explicitly requesting the Idle mode.

When an operating mode change is requested, or when Idle mode is directly requested, the controller immediately ignores any new request from the CRI and PRI interfaces, and blocks the data reception from IPI at the end of the current frame. Then, it waits until all the remaining packets from these sources are sent, and their respective FIFOs are empty. While in the Idle mode, it blocks the data reception from the IPI, CRI, and PRI interfaces,

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maintaining all controller FIFOs empty and all FSMs in an INIT state.

18.3.1.2 Video Mode

Video mode transmits the video frames received from IPI. These video frames are transformed in sync events and video packets. The controller attends requests from CRI or Display commands during BLLP (Blanking or low-power) region. MIPI DSI-2 protocol specifies the following video modes:

- Burst Mode
- on-Burst Mode with Sync Pulses
- on-Burst Mode with Sync Events

18.3.1.2.1 Burst Mode

In Burst mode, pixel transmission is time-compressed and the blanking regions are typically bigger. As the pixel transmission is time compressed, pixel data is sent in a single packet. The IPI_PIX_PKT_CFG register has no effect when the controller uses the Burst mode.

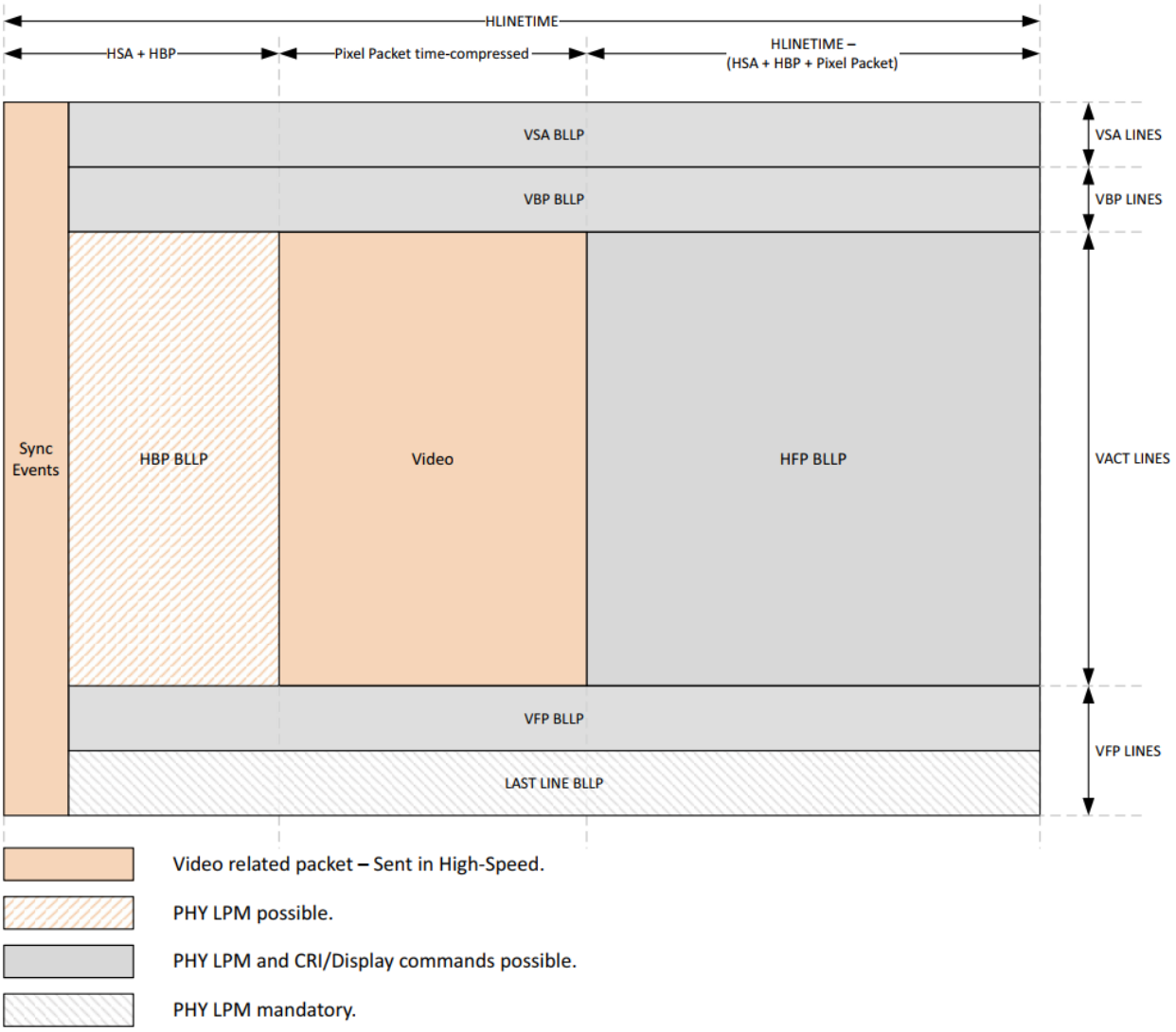


Fig. 18-3 Burst Mode Frame Behavior

18.3.1.2.2 Non-Burst Mode with Sync Pulses

Non-Burst mode with sync pulses enables the controller to accurately reconstruct original video timing and sync pulse widths. The Figure shows a DSI-2 frame transmitted in non-burst mode with sync pulses through PHY Protocol Interface (PPI).

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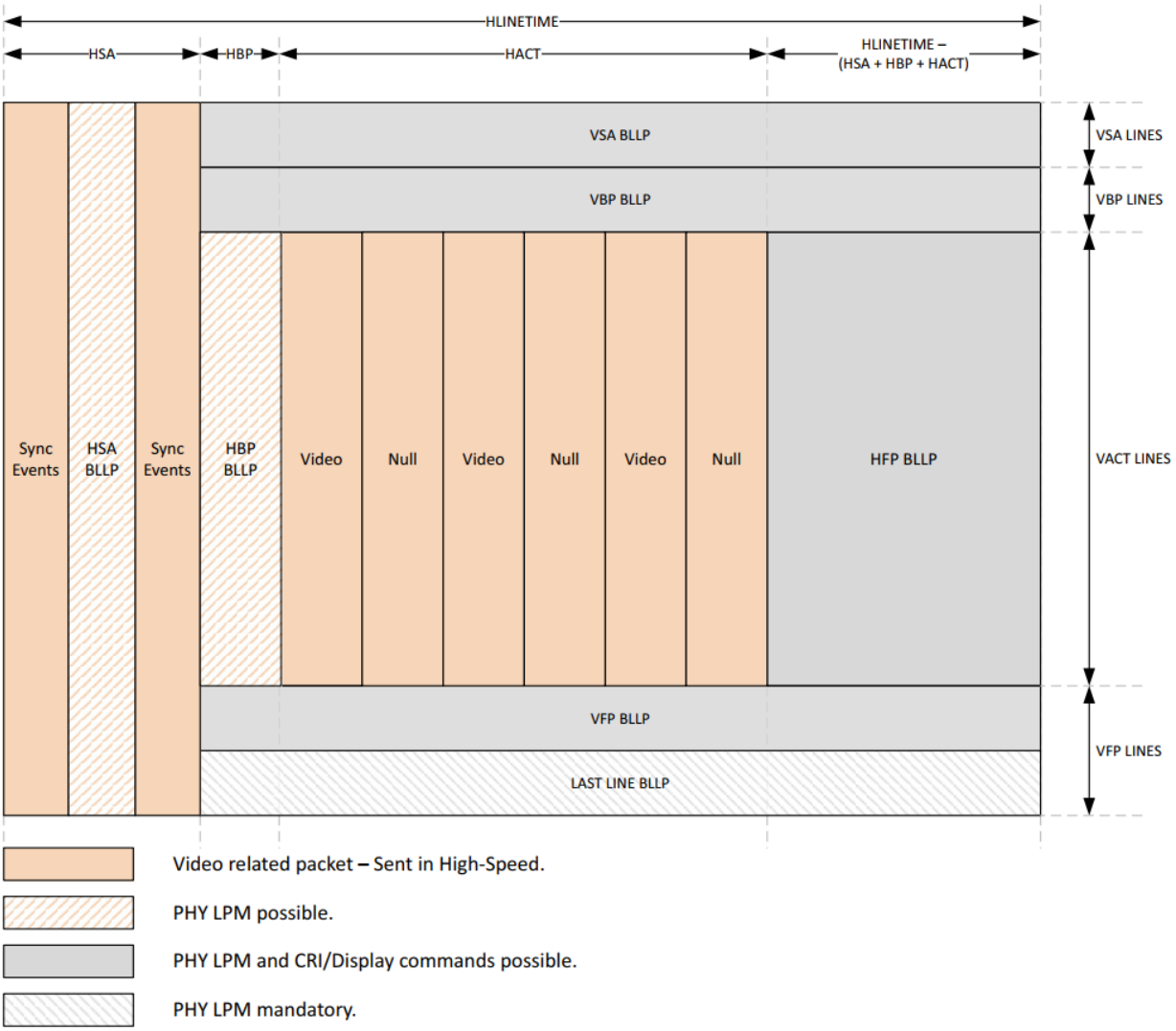


Fig. 18-4 Non-Burst With Sync Pulse Mode Frame Behavior

To adhere to the HACT timing coming from IPI interface, MIPI_DSI2_Host Controller splits the pixel stream in chunks. Each chunk is composed of a pixel packet, and an associated null packet. The number of chunks and pixel packets size depend on the programmed value in the IPI_PIX_PKT_CFG register.

18.3.1.2.3 Non-Burst Mode with Sync Events

The Non-Burst mode with sync events is similar to the Non-Burst mode with sync pulses, but accurate reconstruction of sync pulse widths is not required. The Figure shows a DSI-2 frame transmitted in non-burst mode with sync events through PHY Protocol Interface (PPI).

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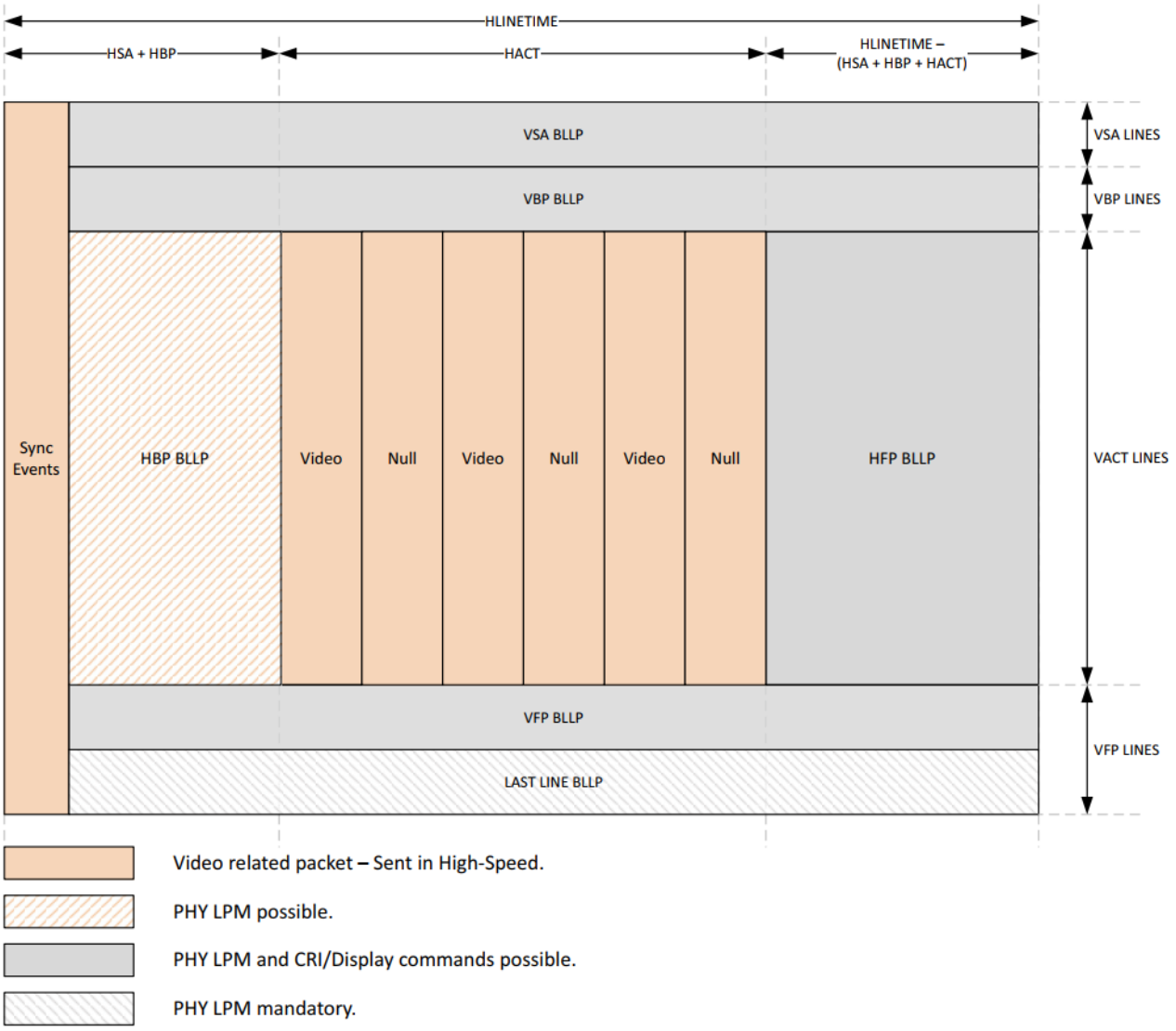


Fig. 18-5 Non-Burst With Sync Event Mode Frame Behavior

18.3.1.3 Data Stream Mode

Data Stream mode is an operating mode that transmits the data stream frames coming from IPI. These frames are transformed in DCS write packets using the Write Memory Start (WMS) and Write Memory Continue (WMC) commands, attending all pending requests from CRI or PRI after the last IPI related packet.

The controller processes the traffics in the following way:

- Start processing the IPI data stream traffic using a WMS command.
- Continue the IPI data stream traffic processing using WMC commands.
- After the last WMS/WMC command from the current frame is sent, process all pending CRI requests.
- Process all pending PRI requests

18.3.1.4 Command Mode

Command mode completely ignores IPI. The controller does not process any traffic that arrives through IPI interface. Instead, it processes requests coming from CRI or PRI interfaces on a first come, first served basis. If the requests are accumulated in the FIFOs of both interfaces, the controller prioritizes CRI traffic over PRI requests.

18.3.2 DSI-2 Options

MIPI_DSI2_Host Controller has a subset of programmable values related to the DSI-2 protocol.

MIPI_DSI2_Host Controller supports the following features:

- Virtual Channels
- Scrambling

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- Video Transmission
- Device Compliance

18.3.2.1 Virtual Channels

To be able to transmit or receive packets, MIPI_DSI2_Host controller must be programmed with the virtual channel identifier. Use the DSI_VCID_CFG register:

- To program a virtual channel identifier for all transmitted packets
- To identify the read-back packets to process
- For CRI packet transmissions, virtual channel identifier is programmed in the virtual_channel field of the CRI_TX_HDR register and virtual channel for responses is made available in the virtual_channel field of the CRI_RX_HDR register

18.3.2.2 Scrambling

Data scrambling can be used to mitigate the effects of electromagnetic interferences on the transmissions using a data randomization technique described in DSI-2 specification. Scrambling is applied only on the data payload, and the footer of long packets transmitted in high speed.

Scrambling can be enabled through the DSI_SCRAMBLING_CFG[0] bit. By default, scrambling seed is 0xFFFF as recommended in DSI-2 specification. This value can be changed using the SI_SCRAMBLING_CFG [31:16] bits.

18.3.2.3 Video Transmission

In the Video mode, the transmission of video frames and related details can be programmed through the DSI_VID_TX_CFG register. The vid_mode_type field of the DSI_VID_TX_CFG register controls the video mode transmission type, between burst, non-burst with sync pulses, and non-burst with sync events. This originates different packet sequences in PPI, as described in DSI-2 specification, to precisely replicate the characteristics of each horizontal region. With respect to the horizontal active region data and timing:

- In Burst mode, the controller creates just one video packet which is sent as soon as possible.
- In Non-burst mode, the controller creates multiple video packets, interlacing each one with a null packet as per the IPI_PIX_PKT_CFG register programming.

The size of the null packets is calculated such that the duration of the horizontal active region is preserved in PPI as well.

The controller follows the defined behavior for each video region when the controller has no packets to send. The controller tries to go in low-power (if time allows) unless the option to fill that region with Blanking packets is set.

Display commands mentioned in DSI-2 specification (Turn On, Turn Off, Color Mode On, and Color Mode Off) can be programmed to be transmitted in low-power.

18.3.2.4 Device Compliance

To match the compatibility requirements of the coupled DSI-2 Device, MIPI_DSI2_Host Controller enables or disables some general features. This ensures that both Host and Device can communicate effectively. Following are the features that can be programmed through the DSI_GENERAL_CFG register:

- BTA enable: Determines whether the controller should send Bus Turnaround requests or disable them.
- EoTp transmission: Determines whether the controller should send EoTp in high-speed or not sent at all.

18.3.2.5 DSI-2 Host Controller Timeouts

MIPI_DSI2_Host Controller allows the configuration of several configurable timeouts. All timeouts are measured using phy_lptx_clk. Because it is a clock divided from sys_clk, it is always available to the controller.

When a given timeout period is violated, an interrupt will be triggered in INT_ST_TO register to inform which timeout is breached.

The timeouts measurement on the PPI interface can be divided in three main categories:

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high-speed transmission, low-power data transmission, and Turnaround.

18.3.3 Debug Capabilities

FIFOs control and status, and FSMs control and status are available through AMBA APB 3 interface to identify the possible error scenarios.

18.3.3.1 FIFO Control and Status

The status of the various FIFOs present on MIPI_DSI2_Host Controller can be read for debug purposes through the OBS_FIFO_STATUS register. This register reports one of the following statuses:

- Empty
- Almost empty - two positions from empty
- Half full
- Almost full - two positions from full
- Full
- Current Word Count

Manual FIFO flush control is provided through the OBS_FIFO_CTRL register, and automatic FIFO flush control is provided using the OBS_FIFO_CFG register.

18.3.3.2 FSM Control and Status

The status of the main FSM present on MIPI_DSI2_Host Controller can be read for debug purposes through the OBS_FSM_STATUS register. This register reports the following statuses:

- Current state
- Previous state
- Current state counter: Counts the number of cycles in the current state

Manual FSM initialization control is provided through the OBS_FSM_CTRL register, and automatic FSM initialization control is provided through the OBS_FSM_CFG register.

18.4 Register Description

18.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

18.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DSI2_CORE_ID	0x0000	W	0x3130302A	Core identification represented in ASCII
DSI2_VERSION	0x0004	W	0x1A020100	Core version number
DSI2_PWR_UP	0x000C	W	0x00000000	Controls the power up of the core
DSI2_SOFT_RESET	0x0010	W	0x00000007	Controls the soft-reset of individual parts of the IP
DSI2_INT_ST_MAIN	0x0014	W	0x00000000	Contains the status of individual interrupt sources
DSI2_MODE_CTRL	0x0018	W	0x00000000	Controller operating mode change request
DSI2_MODE_STATUS	0x001C	W	0x00000000	Controller operating mode status
DSI2_CORE_STATUS	0x0020	W	0x00000000	Core status
DSI2_MANUAL_MODE_CFG	0x0024	W	0x00000000	Manual mode for setting all timings.
DSI2_OBS_FSM_STATUS_SEL	0x0028	W	0x00000000	FSM selection for status reporting and debug
DSI2_OBS_FSM_STATUS	0x002C	W	0x00000000	Status of the selected FSM
DSI2_OBS_FSM_CFG	0x0030	W	0x00000000	Controls automatic FSM re-initialization options

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Name	Offset	Size	Reset Value	Description
DSI2_OBS_FSM_CTRL	0x0034	W	0x00000000	Controls manual FSM re-initialization options in case of an FSM stuck.
DSI2_OBS_FIFO_STATUS_SEL	0x0038	W	0x00000000	FIFO selection for status reporting and debugging
DSI2_OBS_FIFO_STATUS	0x003C	W	0x00000000	Status of the selected FSM
DSI2_OBS_FIFO_CFG	0x0040	W	0x00000000	Controls automatic FSM re-initialization options
DSI2_OBS_FIFO_CTRL	0x0044	W	0x00000000	Manual FIFOs flush
DSI2_TIMEOUT_HSTX_CFG	0x0048	W	0x00000000	Configures the counter for high-speed TX timeout
DSI2_TIMEOUT_HSTXRDY_CFG	0x004C	W	0x00000000	Configures the counter for high-speed TX Ready timeout
DSI2_TIMEOUT_LPRX_CFG	0x0050	W	0x00000000	Configures the counter for low power RX timeout
DSI2_TIMEOUT_LPTXRDY_CFG	0x0054	W	0x00000000	Configures the counter for low-power TX DATA timeout
DSI2_TIMEOUT_LPTXTRIG_CFG	0x0058	W	0x00000000	Configures the counter for low power TX TRIGGER timeout
DSI2_TIMEOUT_LPTXULPS_CFG	0x005C	W	0x00000000	Configures the counter for low power TX ULPS timeout
DSI2_TIMEOUT_BTA_CFG	0x0060	W	0x00000000	Configures the counter for bus turnaround direction timeout
DSI2_PHY_MODE_CFG	0x0100	W	0x00000030	Configures the PHY interface
DSI2_PHY_CLK_CFG	0x0104	W	0x00000000	Configures the clock running type, and the division factor of the phy_lptx_clk clock
DSI2_PHY_STATUS	0x0108	W	0x00000000	Reports the status of PHY
DSI2_PHY_LP2HS_MAN_CFG	0x010C	W	0x00000000	Configures PHY transition time from low-power to high-speed transmission
DSI2_PHY_LP2HS_AUTO_CFG	0x0110	W	0x00000000	Reports measured value for PHY transition time from low-power to high-speed transmission
DSI2_PHY_HS2LP_MAN_CFG	0x0114	W	0x00000000	Configures PHY transition time from low-power to high-speed transmission
DSI2_PHY_HS2LP_AUTO_CFG	0x0118	W	0x00000000	Reports measured value for PHY transition time from low-power to high-speed transmission
DSI2_PHY_MAX_RD_T_MAN_CFG	0x011C	W	0x00000000	Configures the maximum read time
DSI2_PHY_MAX_RD_T_AUTO	0x0120	W	0x00000000	Reports the maximum read time, when in auto-mode
DSI2_PHY_ESC_CMD_T_MAN_CFG	0x0124	W	0x00000000	Configures PHY trigger time
DSI2_PHY_ESC_CMD_T_AUTO	0x0128	W	0x00000000	Reports PHY trigger time, when in auto-mode
DSI2_PHY_ESC_BYTE_T_MAN_CFG	0x012C	W	0x00000000	Configures PHY trigger time
DSI2_PHY_ESC_BYTE_T_AUTO	0x0130	W	0x00000000	Reports PHY trigger time, when in auto-mode

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Name	Offset	Size	Reset Value	Description
DSI2_PHY_IPI_RATIO_MAN_CFG	0x0134	W	0x00000000	Configures ratio between frequencies of HSTX clock and IPI clock
DSI2_PHY_IPI_RATIO_MAN_AUTO	0x0138	W	0x00000000	Reports the calculated ratio between frequencies of HSTX clock and IPI clock
DSI2_PHY_SYS_RATIO_MAN_CFG	0x013C	W	0x00000000	Configures ratio between frequencies of HSTX clock and SYS clock.
DSI2_PHY_SYS_RATIO_MAN_AUTO	0x0140	W	0x00000000	Reports the calculated ratio between frequencies of HSTX clock and SYS clock
DSI2_PRI_TX_CMD	0x01C0	W	0x00000000	This register is used for transmitting all available PHY requests
DSI2_PRI_RX_CMD	0x01C4	W	0x00000000	This register contains calibration required time
DSI2_PRI_CAL_CTRL	0x01C8	W	0x00000000	This register contains calibration required time
DSI2_PRI_ULPS_CTRL	0x01CC	W	0x00000000	This register defines different modes for ULPS entry and exit
DSI2_DSI_GENERAL_CFG	0x0200	W	0x00000000	Configures the general options to meet the characteristics of the peripheral.
DSI2_DSI_VCID_CFG	0x0204	W	0x00000000	Configures the virtual channel for transmission
DSI2_DSI_SCRAMBLING_CFG	0x0208	W	0xFFFF0000	Configures data scrambling
DSI2_DSI_VID_TX_CFG	0x020C	W	0x00000000	Configures the video transmission options
DSI2_DSI_MAX_RPS_CFG	0x0210	W	0x00000000	Configures the maximum payload size that a received packet can contain
DSI2_CRI_TX_HDR	0x02C0	W	0x00000000	Header for packets to be sent in command mode
DSI2_CRI_TX_PLD	0x02C4	W	0x00000000	Payload for packets to be sent in command mode
DSI2_CRI_RX_HDR	0x02C8	W	0x00000000	Header of packets received from device side
DSI2_CRI_RX_PLD	0x02CC	W	0x00000000	Payload of packets received from device side
DSI2_IPI_COLOR_MAN_CFG	0x0300	W	0x00000000	Configures the color coding for the IPI interface in manual mode
DSI2_IPI_VID_HSA_MAN_CFG	0x0304	W	0x00000000	Configures the Horizontal Sync Active period
DSI2_IPI_VID_HSA_AUTO	0x0308	W	0x00000000	Reports the Horizontal Sync Active period, when in auto-mode
DSI2_IPI_VID_HBP_MAN_CFG	0x030C	W	0x00000000	Configures the Horizontal Back Porch period
DSI2_IPI_VID_HBP_AUTO	0x0310	W	0x00000000	Reports the Horizontal back porch period, when in auto-mode
DSI2_IPI_VID_HACT_MAN_CFG	0x0314	W	0x00000000	Configures the Horizontal Active line time HACT

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Name	Offset	Size	Reset Value	Description
DSI2_IPI_VID_HACT_AUTO	0x0318	W	0x00000000	Reports the Horizontal Active period, when in auto-mode
DSI2_IPI_VID_HLINE_MAN_CFG	0x031C	W	0x00000000	Configures the total line time
DSI2_IPI_VID_HLINE_AUTO	0x0320	W	0x00000000	Reports the total line time, when in auto-mode
DSI2_IPI_VID_VSA_MAN_CFG	0x0324	W	0x00000000	Configures the Vertical Sync Active period
DSI2_IPI_VID_VSA_AUTO	0x0328	W	0x00000000	Reports the Vertical Sync Active period in auto-mode
DSI2_IPI_VID_VBP_MAN_CFG	0x032C	W	0x00000000	Configures the Vertical Back Porch period
DSI2_IPI_VID_VBP_AUTO	0x0330	W	0x00000000	Reports the Vertical Back Porch period in auto-mode
DSI2_IPI_VID_VACT_MAN_CFG	0x0334	W	0x00000000	Configures the Vertical Active region period
DSI2_IPI_VID_VACT_AUTO	0x0338	W	0x00000000	Reports the Vertical Active region period when in auto-mode
DSI2_IPI_VID_VFP_MAN_CFG	0x033C	W	0x00000000	Configures the Vertical Front Porch period
DSI2_IPI_VID_VFP_AUTO	0x0340	W	0x00000000	Reports the Vertical Front Porch period in auto-mode
DSI2_IPI_PIX_PKT_CFG	0x0344	W	0x00000000	Configures the number of pixels per packet
DSI2_INT_ST_PHY	0x0400	W	0x00000000	Groups the interrupt sources related to PHY
DSI2_INT_MASK_PHY	0x0404	W	0x00000000	Configures masks for the interrupt sources of the INT_ST_PHY register
DSI2_INT_FORCE_PHY	0x0408	W	0x00000000	Forces the interrupt sources of the INT_ST_PHY register
DSI2_INT_ST_TO	0x0410	W	0x00000000	Groups the interrupt sources related to PHY
DSI2_INT_MASK_TO	0x0414	W	0x00000000	Configures masks for the interrupt sources of the INT_ST_PHY register
DSI2_INT_FORCE_TO	0x0418	W	0x00000000	Forces the interrupt sources of the INT_ST_PHY register
DSI2_INT_ST_ACK	0x0420	W	0x00000000	Groups the interrupt sources related to Acknowledge and Error Report packet
DSI2_INT_MASK_ACK	0x0424	W	0x00000000	Configures masks for the interrupt sources of the INT_ST_ACK register
DSI2_INT_FORCE_ACK	0x0428	W	0x00000000	Forces the interrupt sources of the INT_ST_ACK register
DSI2_INT_ST_IPI	0x0430	W	0x00000000	Groups the interrupt sources related to IPI
DSI2_INT_MASK_IPI	0x0434	W	0x00000000	Configures masks for the interrupt sources of the INT_ST_PHY register
DSI2_INT_FORCE_IPI	0x0438	W	0x00000000	Forces the interrupt sources of the INT_ST_IPI register

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Name	Offset	Size	Reset Value	Description
DSI2_INT_ST_FIFO	0x0440	W	0x00000000	Groups the interrupt sources related to FIFOs
DSI2_INT_MASK_FIFO	0x0444	W	0x00000000	Configures masks for the interrupt sources of the INT_ST_FIFO register
DSI2_INT_FORCE_FIFO	0x0448	W	0x00000000	Forces the interrupt sources of the INT_ST_FIFO register
DSI2_INT_ST_PRI	0x0450	W	0x00000000	Groups the interrupt sources related to PRI
DSI2_INT_MASK_PRI	0x0454	W	0x00000000	Configures masks for the interrupt sources of the INT_ST_PHY register
DSI2_INT_FORCE_PRI	0x0458	W	0x00000000	Forces the interrupt sources of the INT_ST_PRI register
DSI2_INT_ST_CRI	0x0460	W	0x00000000	Groups the interrupt sources related to CRI
DSI2_INT_MASK_CRI	0x0464	W	0x00000000	Configures masks for the interrupt sources of the INT_ST_CRI register
DSI2_INT_FORCE_CRI	0x0468	W	0x00000000	Forces the interrupt sources of the INT_ST_CRI register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

18.4.3 Detail Registers Description

DSI2_CORE_ID

Address: Operational Base(0x27D80000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x3130302a	core_id Core identification. Byte-wise representation of ASCII characters containing the version of the IP.

DSI2_VERSION

Address: Operational Base(0x27D80000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RO	0x1a020100	core_version Core version number.

DSI2_PWR_UP

Address: Operational Base(0x27D80000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	pwr_up Configures the core either to power-up or to reset. 1'b0: Reset 1'b1: Power-up

DSI2_SOFT_RESET

Address: Operational Base(0x27D80000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x1	sys_rstn Soft-reset for SYS data process. Active low and used synchronously.

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Bit	Attr	Reset Value	Description
1	RW	0x1	phy_rstn Soft-reset for PHY data process. Active low and used synchronously.
0	RW	0x1	ipi_rstn Soft-reset for IPI data process. Active low and used synchronously.

DSI2_INT_ST_MAIN

Address: Operational Base(0x27D80000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RC	0x0	int_st_cri Status of the INT_ST_CRI register
5	RC	0x0	int_st_pri Status of the INT_ST_PRI register
4	RC	0x0	int_st_fifo Status of the INT_ST_FIFO register
3	RC	0x0	int_st_ipi Status of the INT_ST_IPI register
2	RC	0x0	int_st_ack Status of the INT_ST_DSI register
1	RC	0x0	int_st_to Status of the INT_ST_TO register
0	RC	0x0	int_st_phy Status of the INT_ST_PHY register

DSI2_MODE_CTRL

Address: Operational Base(0x27D80000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	WO	0x0	mode_ctrl Requested operating mode: 3'b000: Idle mode 3'b001: AutoCalculation mode 3'b010: Command mode 3'b011: Video mode 3'b100: Data Stream mode Others: Reserved

DSI2_MODE_STATUS

Address: Operational Base(0x27D80000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RO	0x0	mode_status Current operating mode: 3'b000: Idle mode 3'b001: AutoCalculation mode 3'b010: Command mode 3'b011: Video mode 3'b100: Data Stream mode Others: Reserved

DSI2_CORE_STATUS

Address: Operational Base(0x27D80000) + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x0	pri_rd_data_avail PRI has new read data available.
25	RO	0x0	pri_fifos_not_empty At least one PRI WR FIFO is not empty.
24	RO	0x0	pri_busy PRI interface is busy: - At least one PRI FIFO is not empty - [or] At least one PRI packet is being transmitted or processed.
23:19	RO	0x00	reserved
18	RO	0x0	cri_rd_data_avail CRI has new read data available.
17	RO	0x0	cri_fifos_not_empty At least one CRI WR FIFO is not empty.
16	RO	0x0	cri_busy Command Interface is busy: - At least one CRI FIFO (internal and external) is not empty - [or] At least one CRI packet is being transmitted or processed.
15:10	RO	0x00	reserved
9	RO	0x0	ipi_fifos_not_empty At least one IPI FIFO (internal and external) is not empty.
8	RO	0x0	ipi_busy Image Pixel Interface is busy: - At least one IPI FIFO (internal and external) is not empty - [or] At least one IPI packet is being transmitted or processed.
7:2	RO	0x00	reserved
1	RO	0x0	core_fifos_not_empty At least one FIFO (internal and external) is not empty.
0	RO	0x0	core_busy mipidsi2_host is busy: - At least one FIFO (internal and external) is not empty - [or] At least one packet is being transmitted or processed.

DSI2_MANUAL_MODE_CFG

Address: Operational Base(0x27D80000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	manual_mode_en Enables manual mode for setting all timings. When unset, timings are automatically calculated by measuring times and lines in the next frame. When set, all timing parameters need to be programmed through the register bank.

DSI2_OBS_FSM_STATUS_SEL

Address: Operational Base(0x27D80000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	fsm_selector FSM selection for reporting and debugging. Current word count of the selected FSM: 4'b0000: ipi_vid_fsm 4'b0001: ipi_auto_calc_fsm 4'b0010: sys_main_fsm 4'b0011: sys_cmd_fsm 4'b0100: sys_pkt_build_fsm 4'b0101: phy_tx_ready_fsm Others: Reserved

DSI2_OBS_FSM_STATUS

Address: Operational Base(0x27D80000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	current_state_cnt Number of clock cycles that the FSM has been in this state.
15:13	RO	0x0	reserved
12:8	RO	0x00	previous_state Previous state.
7:6	RO	0x0	reserved
5	RO	0x0	stuck Flag to indicate that the FSM is stuck.
4:0	RO	0x00	current_state Current state.

DSI2_OBS_FSM_CFG

Address: Operational Base(0x27D80000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	fsm0_auto_init Enables automatic re-initialization of FSM 0.

DSI2_OBS_FSM_CTRL

Address: Operational Base(0x27D80000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	fsm0_auto_init Manual re-initialization of FSM 0.

DSI2_OBS_FIFO_STATUS_SEL

Address: Operational Base(0x27D80000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	fsm_selector FIFO selection for reporting and debugging. Current status of the selected FIFO: 4'b0000: cmd_rd_pld_fifo 4'b0001: cmd_wr_hdr_fifo 4'b0010: cmd_wr_pld_fifo 4'b0011: ipi_data_fifo 4'b0100: ipi_event_fifo 4'b0101: phy_txhs_fifo Others: Reserved

DSI2_OBS_FIFO_STATUS

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Address: Operational Base(0x27D80000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	current_word_count Current word count of the selected FIFO.
15:5	RO	0x000	reserved
4	RO	0x0	full Indicates that the selected FIFO is full.
3	RO	0x0	almost_full Indicates that the selected FIFO is almost full
2	RO	0x0	half_full Indicates that the selected FIFO is half full.
1	RO	0x0	almost_empty Indicates that the selected FIFO is almost empty.
0	RO	0x0	empty Indicates that the selected FIFO is empty.

DSI2_OBS_FIFO_CFG

Address: Operational Base(0x27D80000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ipi_fifo_auto_flush Enables automatic flush for the IPI FIFO.
2	RW	0x0	cmd_wr_hdr_fifo_auto_flush Enables automatic flush for the cmd_wr_hdr FIFO.
1	RW	0x0	cmd_wr_pld_fifo_auto_flush Enables automatic flush for the cmd_wr_pld FIFO.
0	RW	0x0	cmd_rd_pld_fifo_auto_flush Enables automatic flush for the cmd_rd_pld FIFO.

DSI2_OBS_FIFO_CTRL

Address: Operational Base(0x27D80000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ipi_fifo_maual_flush Enables manual flush for the IPI FIFO.
2	RW	0x0	cmd_wr_hdr_fifo_maual_flush Enables manual flush for the cmd_wr_hdr FIFO.
1	RW	0x0	cmd_wr_pld_fifo_maual_flush Enables manual flush for the cmd_wr_pld FIFO.
0	RW	0x0	cmd_rd_pld_fifo_maual_flush Enables manual flush for the cmd_rd_pld FIFO.

DSI2_TIMEOUT_HSTX_CFG

Address: Operational Base(0x27D80000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	to_hstx_value Configures the counter that triggers a high-speed transmission timeout (measured in phy_lptx_clk cycles)

DSI2_TIMEOUT_HSTXRDY_CFG

Address: Operational Base(0x27D80000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	to_hstxrdy_value Configures the counter that triggers a high-speed transmission ready timeout (measured in phy_lptx_clk cycles)

DSI2_TIMEOUT_LPRX_CFG

Address: Operational Base(0x27D80000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	to_lprxrdy_value Configures the counter that triggers a low-power reception timeout (measured in phy_lptx_clk cycles).

DSI2_TIMEOUT_LPTXRDY_CFG

Address: Operational Base(0x27D80000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	to_lptxrdy_value Configures the counter that triggers a low-power data transmission timeout (measured in phy_lptx_clk cycles).

DSI2_TIMEOUT_LPTXTRIG_CFG

Address: Operational Base(0x27D80000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	to_lptxtrig_value Configures the counter that triggers a low-power trigger transmission timeout (measured in phy_lptx_clk cycles)

DSI2_TIMEOUT_LPTXULPS_CFG

Address: Operational Base(0x27D80000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	to_lptxulps_value Configures the counter that triggers a low-power ULPS entry timeout (measured in phy_lptx_clk cycles)

DSI2_TIMEOUT_BTA_CFG

Address: Operational Base(0x27D80000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	to_bta_value Configures the counter that triggers a bus turnaround direction timeout (measured in phy_lptx_clk cycles)

DSI2_PHY_MODE_CFG

Address: Operational Base(0x27D80000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	ppi_width 2'b00: 8 bits 2'b01: 16 bits 2'b10: 32 bits 2'b11: Reserved
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x3	phy_lanes Configures the number of active lanes. 2'b00: 1 lane 2'b01: 2 lanes 2'b10: 3 lanes 2'b11: 4 lanes
3:1	RO	0x0	reserved
0	RW	0x0	phy_type Configures which PHY interface to be used: 1'b0: DPHY 1'b1: CPHY

DSI2_PHY_CLK_CFG

Address: Operational Base(0x27D80000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	phy_lptx_clk_div Division factor for TX Escape clock to be generated from sys_clk. 5'b00000: phy_lptx_clk turned off 5'b00001: phy_lptx_clk = sys_clk / 2 5'b00010: phy_lptx_clk = sys_clk / 4 5'b00011: phy_lptx_clk = sys_clk / 6 ... 5'b11111: phy_lptx_clk = sys_clk / 62
7:1	RO	0x00	reserved
0	RW	0x0	clk_type Configures the behavior of the clock lane: 1'b0: Continuous clock 1'b1: Non-continuous clock

DSI2_PHY_STATUS

Address: Operational Base(0x27D80000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	phy_l3_ulpsactivenot Indicates the status of the phy_l3_ulpsactivenot signal.
19	RW	0x0	phy_l2_ulpsactivenot Indicates the status of the phy_l2_ulpsactivenot signal.
18	RW	0x0	phy_l1_ulpsactivenot Indicates the status of the phy_l1_ulpsactivenot signal.
17	RW	0x0	phy_l0_ulpsactivenot Indicates the status of the phy_l0_ulpsactivenot signal.
16	RW	0x0	phy_clk_ulpsactivenot Indicates the status of the phy_clk_ulpsactivenot signal.
15:13	RO	0x0	reserved
12	RW	0x0	phy_l3_stopstate Indicates the status of the phy_l3_stopstate signal.
11	RW	0x0	phy_l2_stopstate Indicates the status of the phy_l2_stopstate signal.
10	RW	0x0	phy_l1_stopstate Indicates the status of the phy_l1_stopstate signal.
9	RW	0x0	phy_l0_stopstate Indicates the status of the phy_l0_stopstate signal.
8	RW	0x0	phy_clk_stopstate Indicates the status of the phy_clk_stopstate signal.

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Bit	Attr	Reset Value	Description
7:1	RO	0x00	reserved
0	RW	0x0	phy_direction Indicates the status of the phy_direction signal. 1'b0: TX 1'b1: RX

DSI2_PHY_LP2HS_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	phy_lp2hs_time Configures the time measured in cycles of phy_hstx_clk that is necessary for PHY to switch any clock or data lane from low-power to high-speed transmission. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_LP2HS_AUTO_CFG

Address: Operational Base(0x27D80000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	phy_lp2hs_time_auto Indicates the time measured by the controller in cycles of phy_hstx_clk that PHY takes to switch any clock or data lane from low-power to high-speed transmission. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_HS2LP_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	phy_hs2lp_time Configures the time measured by the controller in cycles of phy_hstx_clk that PHY takes to switch any clock or data lane from high-speed to low-power transmission. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_HS2LP_AUTO_CFG

Address: Operational Base(0x27D80000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	phy_hs2lp_time_auto Indicates the time measured by the controller in cycles of phy_hstx_clk that PHY takes to switch any clock or data lane from high-speed to low-power transmission. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_MAX_RD_T_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:0	RW	0x0000000	phy_max_rd_time Configures the time measured in cycles of phy_hstx_clk that is necessary for receiving a response packet of maximum size. Note that if there is the possibility that an "Acknowledge and Error Report" and/or an EoTp come together with the packet of max size, this value need to reflect the time that is needed to receive them all. This is an integer value (no fractional bits)

DSI2_PHY_MAX_RD_T_AUTO

Address: Operational Base(0x27D80000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RO	0x0000000	phy_max_rd_time_auto Indicates the time measured in cycles of phy_hstx_clk that is necessary for receiving a response packet of maximum size. Note that if there is the possibility that an "Acknowledge and Error Report" and/or an EoTp come together with the packet of max size, this value need to reflect the time that is needed to receive them all. This is an integer value (no fractional bits)

DSI2_PHY_ESC_CMD_T_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	phy_esc_cmd_time Configures the time measured in cycles of phy_hstx_clk that is necessary for the PHY to transmit an escape mode command. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_ESC_CMD_T_AUTO

Address: Operational Base(0x27D80000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	phy_esc_cmd_time_auto Indicates the time measured in cycles of phy_hstx_clk that is necessary for the PHY to transmit an escape mode command. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_ESC_BYTE_T_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	phy_esc_byte_time Configures the time measured in cycles of phy_hstx_clk that is necessary for the PHY to transmit a byte in low-power data transmission. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_ESC_BYTE_T_AUTO

Address: Operational Base(0x27D80000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:0	RO	0x00000000	phy_esc_byte_time_auto Indicates the time measured in cycles of phy_hstx_clk that is necessary for the PHY to transmit a byte in low-power data transmission. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_IPI_RATIO_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	phy_ipi_ratio Configures the ratio calculated as HSTX clock frequency / IPI clock frequency. This is a fixed-point value with 6 integral bits and 16 fractional bits

DSI2_PHY_IPI_RATIO_MAN_AUTO

Address: Operational Base(0x27D80000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RO	0x000000	phy_ipi_ratio_auto Indicates the ratio calculated as HSTX clock frequency / IPI clock frequency. This is a fixed-point value with 6 integral bits and 16 fractional bits

DSI2_PHY_SYS_RATIO_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	phy_sys_ratio Configures Ratio calculated as HSTX clock frequency / SYS clock frequency. This is a fixed-point value with 1 integral bit and 16 fractional bits.

DSI2_PHY_SYS_RATIO_MAN_AUTO

Address: Operational Base(0x27D80000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	phy_sys_ratio_auto Ratio calculated as HSTX clock frequency / SYS clock frequency. This is a fixed-point value with 1 integral bit and 16 fractional bits.

DSI2_PRI_TX_CMD

Address: Operational Base(0x27D80000) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	W1C	0x0	phy_bta Enables PHY bus turnaround request.
15:14	RO	0x0	reserved
13	W1C	0x0	phy_ulps_exit Enables PHY ULPS exit request. Note that this request is valid only if the previous one was a phy_ulps_entry, and if it was successfully transmitted.

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Bit	Attr	Reset Value	Description
12	W1C	0x0	phy_ulps_entry Enables PHY ULPS entry request. Note that two consecutives phy_ulps_entry requests (and when first is successful sent by controller) will result in an interrupt.
11:9	RO	0x0	reserved
8	W1C	0x0	phy_cal Enables PHY calibration request
7:4	RO	0x0	reserved
3	W1C	0x0	phy_tx_trigger_3 Requests sending a trigger 3
2	W1C	0x0	phy_tx_trigger_2 Requests sending a trigger 2
1	W1C	0x0	phy_tx_trigger_1 Requests sending a trigger 1
0	W1C	0x0	phy_tx_trigger_0 Requests sending a trigger 0

DSI2_PRI_RX_CMD

Address: Operational Base(0x27D80000) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RC	0x0	phy_rx_trigger_3 This bit indicates that a trigger 3 has been received.
2	RC	0x0	phy_rx_trigger_2 This bit indicates that a trigger 2 has been received.
1	RC	0x0	phy_rx_trigger_1 This bit indicates that a trigger 1 has been received.
0	RC	0x0	phy_rx_trigger_0 This bit indicates that a trigger 0 has been received.

DSI2_PRI_CAL_CTRL

Address: Operational Base(0x27D80000) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	phy_cal_time Time needed to complete deskew calibration, given in cycles of sys_clk.

DSI2_PRI_ULPS_CTRL

Address: Operational Base(0x27D80000) + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	phy_wakeup_time Configures the PHY wakeup time that controller will consider when performing an ULPS exit request. This time is measured in cycles of phy_lptx_clk and shall represent at least 1 ms, to meet the twakeup time requirement found in D-PHY and C-PHY specifications.
15:5	RO	0x000	reserved
4	RW	0x0	phy_ulps_clk_lane ULPS request command is active for the clock lane
3:1	RO	0x0	reserved
0	RW	0x0	phy_ulps_data_lanes ULPS request command is active for all active data lanes

DSI2_DSI_GENERAL_CFG

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Address: Operational Base(0x27D80000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	bta_en Enables Bus Turn Around (BTA) procedures.
0	RW	0x0	eotp_tx_en Enables the EoTp transmission in high-speed.

DSI2_DSI_VCID_CFG

Address: Operational Base(0x27D80000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	tx_vcid Identifies virtual channel for transmitted packets.

DSI2_DSI_SCRAMBLING_CFG

Address: Operational Base(0x27D80000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:16	RW	0xffff	scrambling_seed Scrambling seed.
15:1	RO	0x0000	reserved
0	RW	0x0	scrambling_en Scrambling enable.

DSI2_DSI_VID_TX_CFG

Address: Operational Base(0x27D80000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	lpdt_display_cmd_en Enables the transmission of commands to be done only in low-power mode.
19:15	RO	0x00	reserved
14	RW	0x0	blk_vfp_hs_en Enables filling the VFP period with blanking packets. If unset and time allows, controller returns to the low-power mode
13	RW	0x0	blk_vbp_hs_en Enables filling the VBP period with blanking packets. If unset and time allows, controller returns to the low-power mode
12	RW	0x0	blk_vsa_hs_en Enables filling the VSA period with blanking packets. If unset and time allows, controller returns to the low-power mode
11:7	RO	0x00	reserved
6	RW	0x0	blk_hfp_hs_en Enables filling the HFP period with blanking packets. If unset and time allows, controller returns to the low-power mode
5	RW	0x0	blk_hbp_hs_en Enables filling the HBP period with blanking packets. If unset and time allows, controller returns to the low-power mode
4	RW	0x0	blk_hsa_hs_en Enables filling the HSA period with blanking packets. If unset and time allows, controller returns to the low-power mode
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	vid_mode_type Configures the video mode transmission type. 2'b00: Non-burst with sync pulses 2'b01: Non-burst with sync events Others: Burst mode

DSI2_DSI_MAX_RPS_CFG

Address: Operational Base(0x27D80000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	max_rt_pkt_sz Maximum payload size that a received packet can contain, in bytes.

DSI2_CRI_TX_HDR

Address: Operational Base(0x27D80000) + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	WO	0x0	cmd_hdr_long Configures the packet as a long packet. This is used only when the programmed data type is a reserved value
28	WO	0x0	cmd_hdr_rd Configures the packet as a read request command. This is used only when the programmed data type is a reserved value.
27:25	RO	0x0	reserved
24	WO	0x0	cmd_tx_mode Configures the transmission mode of the packet. 1'b0: High-speed transmission 1'b1: Low-power transmission
23:16	WO	0x00	wc_msb Configures the most significant byte for the word count field of long packets, or data 1 for short packets.
15:8	WO	0x00	wc_lsb Configures the least significant byte for the word count field of long packets, or data 0 for short packets.
7:6	WO	0x0	virtual_channel Configures the virtual channel for the packet.
5:0	WO	0x00	data_type Configures the data type for the packet.

DSI2_CRI_TX_PLD

Address: Operational Base(0x27D80000) + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:24	WO	0x00	byte_3 The fourth byte of current word of payload.
23:16	WO	0x00	byte_2 The third byte of current word of payload.
15:8	WO	0x00	byte_1 The second byte of current word of payload.
7:0	WO	0x00	byte_0 The first byte of current word of payload.

DSI2_CRI_RX_HDR

Address: Operational Base(0x27D80000) + offset (0x02C8)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RC	0x00	wc_msb The most significant byte for the word count field of long packets, or data 1 for short packets.
15:8	RC	0x00	wc_lsb The least significant byte for the word count field of long packets, or data 0 for short packets.
7:6	RC	0x0	virtual_channel The virtual channel for the packet.
5:0	RC	0x00	data_type The data type for the packet.

DSI2_CRI_RX_PLD

Address: Operational Base(0x27D80000) + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	byte_3 The fourth byte of current word of payload.
23:16	RO	0x00	byte_2 The third byte of current word of payload.
15:8	RO	0x00	byte_1 The second byte of current word of payload.
7:0	RO	0x00	byte_0 The first byte of current word of payload.

DSI2_IPI_COLOR_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ipi_depth Configures the IPI color depth. 4'b0010: 5-6-5 bits 4'b0011: 6 bits 4'b0101: 8 bits 4'b0110: 10 bits Others: Reserved
3:0	RW	0x0	ipi_format Configures the IPI pixel format. 4'b0000: RGB 4'b1011: Compressed Data Others: Reserved

DSI2_IPI_VID_HSA_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	vid_hsa_time Configures the Horizontal Sync Active period measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_IPI_VID_HSA_AUTO

Address: Operational Base(0x27D80000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:0	RO	0x00000000	vid_hsa_time_auto Horizontal Sync Active period measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_IPI_VID_HBP_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	vid_hbp_time Configures the Horizontal Back Porch period measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_IPI_VID_HBP_AUTO

Address: Operational Base(0x27D80000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	vid_hbp_time_auto Horizontal Sync Active period measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_IPI_VID_HACT_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	vid_hact_time Configures the Horizontal Active period measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_IPI_VID_HACT_AUTO

Address: Operational Base(0x27D80000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	vid_hact_time_auto Horizontal Active period measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_IPI_VID_HLINE_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x031C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vid_hline_time Configures the total line time (HSA+HBP+HACT+HFP) measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits

DSI2_IPI_VID_HLINE_AUTO

Address: Operational Base(0x27D80000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	vid_hline_time_auto Total line period measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits.

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DSI2_IPI_VID_VSA_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	vid_vsa_lines Configures the Vertical Sync Active period measured in lines.

DSI2_IPI_VID_VSA_AUTO

Address: Operational Base(0x27D80000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	vid_vsa_lines_auto Vertical Sync Active period measured in lines, as seen by the controller.

DSI2_IPI_VID_VBP_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	vid_vbp_lines Configures the Vertical Back Porch measured in lines.

DSI2_IPI_VID_VBP_AUTO

Address: Operational Base(0x27D80000) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	vid_vbp_lines_auto Vertical Back Porch period measured in lines, as seen by the controller.

DSI2_IPI_VID_VACT_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x0334)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	vid_vact_lines Configures the Vertical Active period measured in lines.

DSI2_IPI_VID_VACT_AUTO

Address: Operational Base(0x27D80000) + offset (0x0338)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	vid_vsa_lines_auto Vertical Active period measured in lines, as seen by the controller.

DSI2_IPI_VID_VFP_MAN_CFG

Address: Operational Base(0x27D80000) + offset (0x033C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	vid_vfp_lines Configures the Vertical Front Porch period measured in lines.

DSI2_IPI_VID_VFP_AUTO

Address: Operational Base(0x27D80000) + offset (0x0340)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
12:0	RO	0x0000	vid_vfp_lines_auto Vertical Front Porch period measured in lines, as seen by the controller.

DSI2_IPI_PIX_PKT_CFG

Address: Operational Base(0x27D80000) + offset (0x0344)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	max_pix_pkt Configures the number of pixels in a single video packet, used in Video mode (for non-burst modes) and Data Stream mode. A value of 0 or bigger than the HACT pixels will originate one single video packet per line, in Video mode. For RGB-10bit color coding, this value must be a multiple of 4.

DSI2_INT_ST_PHY

Address: Operational Base(0x27D80000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RC	0x0	err_phy0 Error PHY 0

DSI2_INT_MASK_PHY

Address: Operational Base(0x27D80000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RC	0x0	mask_err_phy0 Write 1 to unmask each error report.

DSI2_INT_FORCE_PHY

Address: Operational Base(0x27D80000) + offset (0x0408)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	force_err_phy0 Force Error PHY 0

DSI2_INT_ST_TO

Address: Operational Base(0x27D80000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RC	0x0	err_to_bta Indicates that a bus turnaround direction timeout has occurred.
5	RC	0x0	err_to_lptxulps Indicates that a low-power TX ULPS timeout has occurred.
4	RC	0x0	err_to_lptxtrig Indicates that a low-power TX TRIGGER timeout has occurred.
3	RC	0x0	err_to_lptxrdy Indicates that a low-power TX DATA timeout has occurred.
2	RC	0x0	err_to_lprx Indicates that a low-power RX timeout has occurred.
1	RC	0x0	err_to_hstxrdy Indicates that a high-speed TX RDY timeout has occurred.
0	RC	0x0	err_to_hstx Indicates that a high-speed TX timeout has occurred.

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DSI2_INT_MASK_TO

Address: Operational Base(0x27D80000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	mask_err_to_bta Write 1 to unmask this error report.
5	RW	0x0	mask_err_to_lptxulps Write 1 to unmask this error report.
4	RW	0x0	mask_err_to_lptxtrig Write 1 to unmask this error report.
3	RW	0x0	mask_err_to_lptxrdy Write 1 to unmask this error report.
2	RW	0x0	mask_err_to_lprx Write 1 to unmask this error report.
1	RW	0x0	mask_err_to_hstxrdy Write 1 to unmask this error report.
0	RW	0x0	mask_err_to_hstx Write 1 to unmask this error report.

DSI2_INT_FORCE_TO

Address: Operational Base(0x27D80000) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	W1C	0x0	force_err_to_bta Forces the interrupt sources
5	W1C	0x0	force_err_to_lptxulps Forces the interrupt sources
4	W1C	0x0	force_err_to_lptxtrig Forces the interrupt sources
3	W1C	0x0	force_err_to_lptxrdy Forces the interrupt sources
2	W1C	0x0	force_err_to_lprx Forces the interrupt sources
1	W1C	0x0	force_err_to_hstxrdy Forces the interrupt sources
0	W1C	0x0	force_err_to_hstx Forces the interrupt sources

DSI2_INT_ST_ACK

Address: Operational Base(0x27D80000) + offset (0x0420)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RC	0x0	err_ack_rpt_15 Retrieves the DSI Protocol Violation error bit from the Acknowledge error report.
14	RC	0x0	err_ack_rpt_14 Retrieves the Reserved (specific to device) error bit from the Acknowledge error report.
13	RC	0x0	err_ack_rpt_13 Retrieves the Invalid Transmission Length error bit from the Acknowledge error report.
12	RC	0x0	err_ack_rpt_12 Retrieves the DSI VC ID Invalid error bit from the Acknowledge error report.

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Bit	Attr	Reset Value	Description
11	RC	0x0	err_ack_rpt_11 Retrieves the DSI Data Type not recognized error bit from the Acknowledge error report.
10	RC	0x0	err_ack_rpt_10 Retrieves the Payload Checksum error bit (long packet only) from the Acknowledge error report.
9	RC	0x0	err_ack_rpt_9 Retrieves the header ECC/SSDC/Checksum multi-bit (detected, not corrected) error bit from the Acknowledge error report.
8	RC	0x0	err_ack_rpt_8 Retrieves the header ECC/SSDC/Checksum single-bit (detected and corrected) error bit from the Acknowledge error report.
7	RC	0x0	err_ack_rpt_7 Retrieves the Contention Detected error bit from the Acknowledge error report.
6	RC	0x0	err_ack_rpt_6 Retrieves the False Control error bit from the Acknowledge error report.
5	RC	0x0	err_ack_rpt_5 Retrieves the Peripheral Timeout error bit from the Acknowledge error report.
4	RC	0x0	err_ack_rpt_4 Retrieves the Low-Power Transmit Sync error bit from the Acknowledge error report.
3	RC	0x0	err_ack_rpt_3 Retrieves the Escape Mode Entry Command error bit from the Acknowledge error report.
2	RC	0x0	err_ack_rpt_2 Retrieves the EoT Sync error bit from the Acknowledge error report.
1	RC	0x0	err_ack_rpt_1 Retrieves the SoT Sync error bit from the Acknowledge error report.
0	RC	0x0	err_ack_rpt_0 Retrieves the SoT error bit from the Acknowledge error report.

DSI2_INT_MASK_ACK

Address: Operational Base(0x27D80000) + offset (0x0424)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	mask_err_ack_rpt_15 Write 1 to unmask this error report.
14	RW	0x0	mask_err_ack_rpt_14 Write 1 to unmask this error report.
13	RW	0x0	mask_err_ack_rpt_13 Write 1 to unmask this error report.
12	RW	0x0	mask_err_ack_rpt_12 Write 1 to unmask this error report.
11	RW	0x0	mask_err_ack_rpt_11 Write 1 to unmask this error report.
10	RW	0x0	mask_err_ack_rpt_10 Write 1 to unmask this error report.
9	RW	0x0	mask_err_ack_rpt_9 Write 1 to unmask this error report.

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Bit	Attr	Reset Value	Description
8	RW	0x0	mask_err_ack_rpt_8 Write 1 to unmask this error report.
7	RW	0x0	mask_err_ack_rpt_7 Write 1 to unmask this error report.
6	RW	0x0	mask_err_ack_rpt_6 Write 1 to unmask this error report.
5	RW	0x0	mask_err_ack_rpt_5 Write 1 to unmask this error report.
4	RW	0x0	mask_err_ack_rpt_4 Write 1 to unmask this error report.
3	RW	0x0	mask_err_ack_rpt_3 Write 1 to unmask this error report.
2	RW	0x0	mask_err_ack_rpt_2 Write 1 to unmask this error report.
1	RW	0x0	mask_err_ack_rpt_1 Write 1 to unmask this error report.
0	RW	0x0	mask_err_ack_rpt_0 Write 1 to unmask this error report.

DSI2_INT_FORCE_ACK

Address: Operational Base(0x27D80000) + offset (0x0428)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	W1C	0x0	force_err_ack_rpt_15 Force err_ack_rpt_015
14	W1C	0x0	force_err_ack_rpt_14 Force err_ack_rpt_14
13	W1C	0x0	force_err_ack_rpt_13 Force err_ack_rpt_13
12	W1C	0x0	force_err_ack_rpt_12 Force err_ack_rpt_12
11	W1C	0x0	force_err_ack_rpt_11 Force err_ack_rpt_11
10	W1C	0x0	force_err_ack_rpt_10 Force err_ack_rpt_10
9	W1C	0x0	force_err_ack_rpt_9 Force err_ack_rpt_9
8	W1C	0x0	force_err_ack_rpt_8 Force err_ack_rpt_8
7	W1C	0x0	force_err_ack_rpt_7 Force err_ack_rpt_7
6	W1C	0x0	force_err_ack_rpt_6 Force err_ack_rpt_6
5	W1C	0x0	force_err_ack_rpt_5 Force err_ack_rpt_5
4	W1C	0x0	force_err_ack_rpt_4 Force err_ack_rpt_4
3	W1C	0x0	force_err_ack_rpt_3 Force err_ack_rpt_3
2	W1C	0x0	force_err_ack_rpt_2 Force err_ack_rpt_2
1	W1C	0x0	force_err_ack_rpt_1 Force err_ack_rpt_1
0	W1C	0x0	force_err_ack_rpt_0 Force err_ack_rpt_0

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DSI2_INT_ST_IPI

Address: Operational Base(0x27D80000) + offset (0x0430)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RC	0x0	err_display_cmd_ovfl Display command request ignored by the controller due to internal buffer overflow.
1	RC	0x0	err_display_cmd_time Display command request ignored by the controller due to timing.
0	RC	0x0	err_ipi_dtype No DSI-2 data type is a direct match for the choice made by the pair ipi_format and ipi_depth. Data is captured and delivered as for Packed Pixel Stream, 24-bit forma.

DSI2_INT_MASK_IPI

Address: Operational Base(0x27D80000) + offset (0x0434)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	mask_err_display_cmd_ovfl Write 1 to unmask this error report.
1	RW	0x0	mask_err_display_cmd_time Write 1 to unmask this error report.
0	RW	0x0	mask_err_ipi_dtype Write 1 to unmask this error report.

DSI2_INT_FORCE_IPI

Address: Operational Base(0x27D80000) + offset (0x0438)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	W1C	0x0	force_err_display_cmd_ovfl force err_display_cmd_ovfl
1	W1C	0x0	force_err_display_cmd_time force err_display_cmd_time
0	W1C	0x0	force_err_ipi_dtype force err_ipi_dtype

DSI2_INT_ST_FIFO

Address: Operational Base(0x27D80000) + offset (0x0440)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RC	0x0	err_phy0 Groups the interrupt sources related to FIFOs.

DSI2_INT_MASK_FIFO

Address: Operational Base(0x27D80000) + offset (0x0444)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RC	0x0	mask_err_phy0 Write 1 to unmask FIFOs error report.

DSI2_INT_FORCE_FIFO

Address: Operational Base(0x27D80000) + offset (0x0448)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RC	0x0	force_err_phy0 Force FIFOs Error.

DSI2_INT_ST_PRI

Address: Operational Base(0x27D80000) + offset (0x0450)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RC	0x0	err_pri_tx_time PRI request ignored due to timing error (Video Mode only).
0	RC	0x0	err_pri_tx_cmd PHY request cannotbe attended and will be discarded.

DSI2_INT_MASK_PRI

Address: Operational Base(0x27D80000) + offset (0x0454)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RC	0x0	mask_err_pri_tx_time Write 1 to unmask FIFOs error report.
0	RC	0x0	mask_err_pri_tx_cmd Write 1 to unmask FIFOs error report.

DSI2_INT_FORCE_PRI

Address: Operational Base(0x27D80000) + offset (0x0458)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RC	0x0	force_err_pri_tx_time force err_pri_tx_time
0	RC	0x0	force_err_pri_tx_cmd force err_pri_tx_cmd

DSI2_INT_ST_CRI

Address: Operational Base(0x27D80000) + offset (0x0460)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RC	0x0	err_cri_rpt_6 CRI request ignored due to timing error (Video Mode only).
15:14	RO	0x0	reserved
13	RC	0x0	err_cri_rpt_5 CRI received packet length invalid.
12	RC	0x0	err_cri_rpt_4 CRI received packet header invalid virtual channel.
11	RC	0x0	err_cri_rpt_3 CRI received packet header invalid data type
10	RC	0x0	err_cri_rpt_2 CRI received long packet CRC error
9	RC	0x0	err_cri_rpt_1 CRI received packet header fatal ECC error
8	RC	0x0	err_cri_rpt_0 CRI received packet header single ECC error
7:0	RO	0x00	reserved

DSI2_INT_MASK_CRI

Address: Operational Base(0x27D80000) + offset (0x0464)

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Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	mask_err_cri_rpt_6 Write 1 to unmask this error report.
15:14	RO	0x0	reserved
13	RW	0x0	mask_err_cri_rpt_5 Write 1 to unmask this error report.
12	RW	0x0	mask_err_cri_rpt_4 Write 1 to unmask this error report.
11	RW	0x0	mask_err_cri_rpt_3 Write 1 to unmask this error report.
10	RW	0x0	mask_err_cri_rpt_2 Write 1 to unmask this error report.
9	RW	0x0	mask_err_cri_rpt_1 Write 1 to unmask this error report.
8	RW	0x0	mask_err_cri_rpt_0 Write 1 to unmask this error report.
7:0	RO	0x00	reserved

DSI2_INT_FORCE_CRI

Address: Operational Base(0x27D80000) + offset (0x0468)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	force_err_cri_rpt_6 Forces err_cri_cmd_time
15:14	RO	0x0	reserved
13	RW	0x0	force_err_cri_rpt_5 Forces err_cri_invalid_rx_length
12	RW	0x0	force_err_cri_rpt_4 Forces err_cri_invalid_vc
11	RW	0x0	force_err_cri_rpt_3 Forces err_cri_invalid_dt
10	RW	0x0	force_err_cri_rpt_2 Forces err_cri_crc
9	RW	0x0	force_err_cri_rpt_1 Forces err_cri_ecc_fatal
8	RW	0x0	force_err_cri_rpt_0 Forces err_cri_ecc
7:0	RO	0x00	reserved

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Chapter 19 MIPI CSI HOST

19.1 Overview

The CSI-2 Host Controller is designed to receive data from a CSI-2 compliant camera sensor. A D-PHY/C-PHY configured as a Slave acts as the physical layer.
The MIPI CSI-2 Host Controller supports the following features:

- Compliant with MIPI Alliance Specification for CSI-2, Version 1.01.00-9 November 2010
- Interface with MIPI D-PHY v1.2/D-PHY v2.0/C-PHY v1.1
- Up to four D-PHY RX data lanes or three C-PHY RX data lanes.
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets
- Several Frame formats
  - General Frame or Digital Interlaced Video with or without accurate sync timing
  - Data Type (Packet or Frame Level) and Virtual Channel interleaving
- 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification
- All primary and secondary data formats
  - RGB, YUV, and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types
- Error detection and correction
  - PHY level
  - Packet level
  - Line level
  - Frame level
- Support DSI video mode/command mode

19.2 Block Diagram

The following diagram shows the MIPI CSI-2 Host Controller architecture.

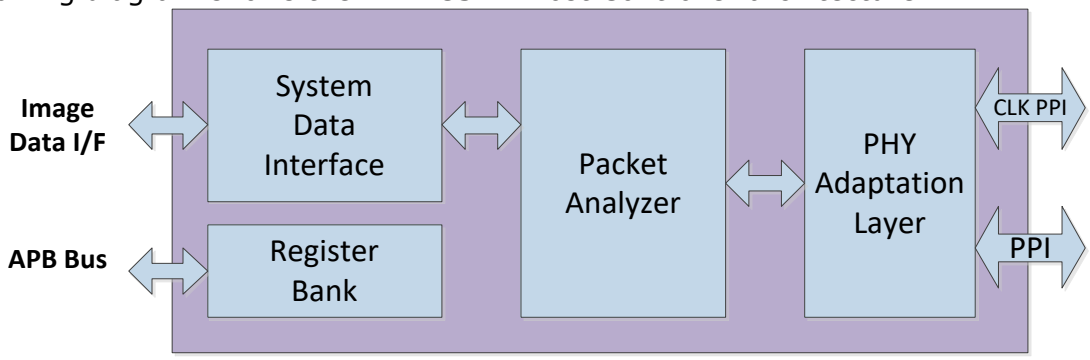


Fig. 19-1 MIPI CSI-2 Host Controller Architecture

- **PHY Adaptation Layer**: Manages the D-PHY/C-PHY PPI interface
- **Packet Analyzer**: Merges the data from the different lanes
- **Image Data Interface**: Reorders pixels into 32-bit data for memory storage and generates timing accurate video synchronization signals
- **AMBA-APB Register Bank**: Provides access to configuration and control registers

19.3 Function Description

19.3.1 Supported Resolutions and Frame Rates

The CSI-2 specification does not define the supported standard resolutions or frame rates. Camera sensor resolution, blanking periods, synchronization events, frame rates, and pixel color depth play a fundamental role in the required bandwidth. All these variables make it difficult to define a standard procedure to estimate the minimum lane rate and the

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minimum number of lanes that support a specific CSI-2 device.
Following table presents some predefined and supported camera settings, assuming the following:

- Clock lane frequency is 500 MHz or 750 MHz that results in a bandwidth of 1 Gbps or 1.5 Gbps respectively, for each data lane.
- No significant control/reserved traffic is present on the link when pixel data is being transmitted.

The last column of following table presents the minimum number of lanes required for each configuration.

Table 19-1 Supported Camera Settings

Mega Pixels	Mega Pixels with Overhead	Refresh Rate (Hz)	Color Depth (bpp)	CSI2 BW (Mbits)	D-PHY/C-PHY at 1 Gbps Number of Lanes	D-PHY/C-PHY at 1.5Gbps Number of Lanes
2MP	2560000	15	24	922	1	1
2MP	2560000	30	24	1843	2	2
3MP	3840000	15	16	922	1	1
3MP	3840000	30	16	1843	2	2
3MP	3840000	30	24	2765	3	2
5MP	6400000	15	16	1536	2	2
5MP	6400000	15	24	2304	3	2
5MP	6400000	30	16	3072	4	3
8MP	10240000	15	16	2458	3	2
8MP	10240000	15	24	3686	4	3
8MP	10240000	30	12	3686	4	3
12MP	15360000	15	12	2765	3	2
12MP	15360000	15	16	3686	4	3
14MP	17920000	15	12	3226	4	3
16MP	20480000	15	12	3686	4	3
Video Formats						
1280x720 pixels(720p)	921600	30	24	664	1	1
1280x720 pixels(720p)	921600	60	24	1327	2	1
1920x1080 pixels(1080p)	2073600	60	24	2986	3	2

19.3.2 Error Detection

The CSI-2 Host Controller analyzes the received packets and determines if there are protocol errors. It is possible to monitor the following errors:

- Frame errors such as incorrect Frame sequence, reception of a CRC error in the most recent frame, and the mismatch between Frame Start and Frame End
- Line errors such as incorrect line sequence and mismatch between Line Start and Line End
- Packet errors such as ECC or CRC mismatch
- D-PHY/C-PHY errors such as synchronization pattern mismatch

Following table shows all the errors that CSI-2 Host Controller can identify.

Table 19-2 Errors Identified by the CSI-2 Host Controller

Error	Description	Level	Action
phy_errsotsynchs_*	Start of transmission error on data lane* with no synchronization achieved	PHY	Packets with this error are not delivered in IDI interface
phy_erresc_*	Escape entry error	PHY	Informative only. Error is

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Error	Description	Level	Action
	(ULPM) on data lane*		acknowledged in the register and the interrupt pin is raised.
phy_errsoths_*	Start of transmission error on data lane* but synchronization can still be achieved	PHY	Informative only since PHY can recover from this error. Error is acknowledged in register and the interrupt pin is raised.
vc*_err_crc	Checksum error detected on virtual channel*	Packet	Informative only. Error is acknowledged in the register and Interrupt pin is raised.
vc*_err_crc	Header ECC contains one error detected on virtual channel*	Packet	Informative only since controller can recover the correct header. Error is acknowledged in the register and the interrupt pin is raised.
err_ecc_double	Header ECC contains two errors. Unrecoverable.	Packet	Packets with this error are not delivered in IDI.s
err_id_vc*	Unrecognized or unimplemented data type detected in virtual channel*	Packet	Informative only. Error is acknowledged in the register and the interrupt pin is raised
err_f_bndry_match_vc*	Error matching Frame Start with Frame End for virtual channel*	Frame	Informative only. Error is acknowledged in register and the interrupt pin is raised if not masked.
err_f_seq_vc*	Incorrect Frame Sequence detected in virtual channel*	Frame	Informative only. Error is acknowledged in register and the interrupt pin is raised if not masked.
err_frame_data_vc*	Last received frame, in virtual channel*, had at least one CRC error	Frame	Informative only. Error is acknowledged in the register and the interrupt pin is raised.

19.4 Register Description

19.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
CSIHOST0	0x27C80000
CSIHOST1	0x27C90000
CSIHOST2	0x27CA0000
CSIHOST3	0x27CB0000
CSIHOST4	0x27CC0000

19.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CSI2HOST_VERSION	0x0000	W	0x00000000	Controller version identification
CSI2HOST_N_LANES	0x0004	W	0x00000000	Number of active data lanes

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Name	Offset	Size	Reset Value	Description
CSI2HOST_CSI2_RESETN	0x0010	W	0x00000000	CSI2 controller reset
CSI2HOST_PHY_STATE	0x0014	W	0x00000000	General settings for all blocks
CSI2HOST_ERR1	0x0020	W	0x00000000	Error state register 1
CSI2HOST_ERR2	0x0024	W	0x00000000	Error state register 2
CSI2HOST_MSK1	0x0028	W	0x00000000	Masks for errors 1
CSI2HOST_MSK2	0x002C	W	0x00000000	Masks for errors 2
CSI2HOST_CONTROL	0x0040	W	0x0C204000	Control
CSI2HOST_HEADER_0	0x0050	W	0x00000000	Header 0
CSI2HOST_HEADER_1	0x0054	W	0x00000000	Header 1
CSI2HOST_HEADER_2	0x0058	W	0x00000000	Header 2
CSI2HOST_HEADER_3	0x005C	W	0x00000000	Header 3

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

19.4.3 Detail Registers Description

CSI2HOST_VERSION

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	version Version of the csi2host.

CSI2HOST_N_LANES

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	n_lanes Number of active data lanes. 2'b00: 1 data lane(lane 0) 2'b01: 2 data lanes(lane0 and 1) 2'b10: 3 data lanes(lane0,1,and 2) 2'b11: 4 data lanes(ALL) Can only be updated when the D-PHY/C-PHY lane is in the Stop state.

CSI2HOST_CSI2_RESETN

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	csi2_resetn CSI2 controller reset output. Active low.

CSI2HOST_PHY_STATE

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RW	0x0	bypass_2ecc_tst Payload Bypass test mode for double ECC errors.
30:15	RO	0x0000	reserved
14	RO	0x0	phy_rxactivehs_3 Lane3 high-speed receive active. Active high.
13	RO	0x0	phy_rxactivehs_2 Lane2 high-speed receive active. Active high.

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Bit	Attr	Reset Value	Description
12	RO	0x0	phy_rxactivehs_1 Lane1 high-speed receive active. Active high.
11	RO	0x0	phy_rxactivehs_0 Lane0 high-speed receive active. Active high.
10	RO	0x0	phy_stopstateclk Clock lane in Stop state.
9	RO	0x0	phy_rxulpsclknot This signal indicates that the clock lane module has entered the Ultra Low Power state. Active low.
8	RO	0x0	phy_rxclkactivehs Indicates that the clock lane is actively receiving a DDR clock.
7	RO	0x0	phy_stopstatedata_3 Data lane 3 in Stop state.
6	RO	0x0	phy_stopstatedata_2 Data lane 2 in Stop state.
5	RO	0x0	phy_stopstatedata_1 Data lane 1 in Stop state.
4	RO	0x0	phy_stopstatedata_0 Data lane 0 in Stop state.
3	RO	0x0	phy_rxulpsesc_3 Lane module0 has entered the Ultra Low Power mode.
2	RO	0x0	phy_rxulpsesc_2 Lane module2 has entered the Ultra Low Power mode.
1	RO	0x0	phy_rxulpsesc_1 Lane module1 has entered the Ultra Low Power mode.
0	RO	0x0	phy_rxulpsesc_0 Lane module0 has entered the Ultra Low Power mode.

CSI2HOST_ERR1

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31	RW	0x0	err_ph_crc_lane2 Packet crc error of lane2 when sw_cphy_en=1.
30	RW	0x0	err_ph_crc_lane1 Packet crc error of lane1 when sw_cphy_en=1.
29	RW	0x0	err_ph_crc_lane0 Packet crc error of lane0 when sw_cphy_en=1.
28	RO	0x0	err_ecc_double Header ECC contains 2 errors, unrecoverable.
27	RO	0x0	vc3_err_crc Checksum error detected on virtual channel 3.
26	RO	0x0	vc2_err_crc Checksum error detected on virtual channel 2.
25	RO	0x0	vc1_err_crc Checksum error detected on virtual channel 1.
24	RO	0x0	vc0_err_crc Checksum error detected on virtual channel 0.
23:16	RO	0x00	reserved
15	RO	0x0	err_frame_data_vc3 Last received frame, in virtual channel 3, had at least one CRC error.

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Bit	Attr	Reset Value	Description
14	RO	0x0	err_frame_data_vc2 Last received frame, in virtual channel 2, had at least one CRC error.
13	RO	0x0	err_frame_data_vc1 Last received frame, in virtual channel 1, had at least one CRC error.
12	RO	0x0	err_frame_data_vc0 Last received frame, in virtual channel 0, had at least one CRC error.
11	RO	0x0	err_f_seq_vc3 Incorrect frame sequence detected in virtual channel 3.
10	RO	0x0	err_f_seq_vc2 Incorrect frame sequence detected in virtual channel 2.
9	RO	0x0	err_f_seq_vc1 Incorrect frame sequence detected in virtual channel 1.
8	RO	0x0	err_f_seq_vc0 Incorrect frame sequence detected in virtual channel 0.
7	RO	0x0	err_f_bndry_match_vc3 Error matching frame start with frame end for virtual channel 3.
6	RO	0x0	err_f_bndry_match_vc2 Error matching frame start with frame end for virtual channel 2.
5	RO	0x0	err_f_bndry_match_vc1 Error matching frame start with frame end for virtual channel 1.
4	RO	0x0	err_f_bndry_match_vc0 Error matching frame start with frame end for virtual channel 0.
3	RO	0x0	phy_errsotsynchs_3 Start of transmission error on data lane 3.
2	RO	0x0	phy_errsotsynchs_2 Start of transmission error on data lane 2.
1	RO	0x0	phy_errsotsynchs_1 Start of transmission error on data lane 1.
0	RO	0x0	phy_errsotsynchs_0 Start of transmission error on data lane 0(no synchronization achieved).

CSI2HOST_ERR2

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	fifo_overflow FIFO overflow in adapter.
27	RW	0x0	cphy_errcodehs_3 Lane 3 receive invalid code whensw_cphy_en=1.
26	RW	0x0	cphy_errcodehs_2 Lane 2 receive invalid code whensw_cphy_en=1.
25	RW	0x0	cphy_errcodehs_1 Lane 1 receive invalid code whensw_cphy_en=1.
24	RW	0x0	cphy_errcodehs_0 Lane 0 receive invalid code whensw_cphy_en=1.
23:20	RO	0x0	reserved
19	RW	0x0	phy_errcontrol_3 Control error on data lane 3.
18	RW	0x0	phy_errcontrol_2 Control error on data lane 2.

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Bit	Attr	Reset Value	Description
17	RW	0x0	phy_errcontrol_1 Control error on data lane 1.
16	RW	0x0	phy_errcontrol_0 Control error on data lane 0.
15	RW	0x0	err_id_vc3 Unrecognized or unimplemented data type detected in virtual channel 3.
14	RW	0x0	err_id_vc2 Unrecognized or unimplemented data type detected in virtual channel 2.
13	RW	0x0	err_id_vc1 Unrecognized or unimplemented data type detected in virtual channel 1.
12	RW	0x0	err_id_vc0 Unrecognized or unimplemented data type detected in virtual channel 0.
11	RW	0x0	vc3_err_ecc_corrected Header error detected and corrected on virtual channel 3.
10	RW	0x0	vc2_err_ecc_corrected Header error detected and corrected on virtual channel 2.
9	RW	0x0	vc1_err_ecc_corrected Header error detected and corrected on virtual channel 1.
8	RW	0x0	vc0_err_ecc_corrected Header error detected and corrected on virtual channel 0.
7	RW	0x0	phy_errsoths_3 Start of transmission error on data lane 3(synchronization can still be achieved).
6	RW	0x0	phy_errsoths_2 Start of transmission error on data lane 2(synchronization can still be achieved).
5	RW	0x0	phy_errsoths_1 Start of transmission error on data lane 1(synchronization can still be achieved).
4	RW	0x0	phy_errsoths_0 Start of transmission error on data lane 0(synchronization can still be achieved).
3	RW	0x0	phy_erresc_3 Escape entry error(ULPM) on data lane 3.
2	RW	0x0	phy_erresc_2 Escape entry error(ULPM) on data lane 2.
1	RW	0x0	phy_erresc_1 Escape entry error(ULPM) on data lane 1.
0	RW	0x0	phy_erresc_0 Escape entry error(ULPM) on data lane 0.

CSI2HOST_MSK1

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31	RW	0x0	mask_err_ph_crc_lane2 Mask for err_ph_crc_lane2.
30	RW	0x0	mask_err_ph_crc_lane1 Mask for err_ph_crc_lane1.
29	RW	0x0	mask_err_ph_crc_lane0 Mask for err_ph_crc_lane0.

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Bit	Attr	Reset Value	Description
28	RW	0x0	mask_err_ecc_double Mask for err_ecc_double.
27	RW	0x0	mask_vc3_err_crc Mask for vc3_err_crc.
26	RW	0x0	mask_vc2_err_crc Mask for vc2_err_crc.
25	RW	0x0	mask_vc1_err_crc Mask for vc1_err_crc.
24	RW	0x0	mask_vc0_err_crc Mask for vc0_err_crc.
23:16	RO	0x00	reserved
15	RW	0x0	mask_err_frame_data_vc3 Mask for err_frame_data_vc3.
14	RW	0x0	mask_err_frame_data_vc2 Mask for err_frame_data_vc2.
13	RW	0x0	mask_err_frame_data_vc1 Mask for err_frame_data_vc1.
12	RW	0x0	mask_err_frame_data_vc0 Mask for err_frame_data_vc0.
11	RW	0x0	mask_err_f_seq_vc3 Mask for err_f_seq_vc3.
10	RW	0x0	mask_err_f_seq_vc2 Mask for err_f_seq_vc2.
9	RW	0x0	mask_err_f_seq_vc1 Mask for err_f_seq_vc1.
8	RW	0x0	mask_err_f_seq_vc0 Mask for err_f_seq_vc0.
7	RW	0x0	mask_err_f_bndry_match_vc3 Mask for err_f_bndry_match_vc3.
6	RW	0x0	mask_err_f_bndry_match_vc2 Mask for err_f_bndry_match_vc2.
5	RW	0x0	mask_err_f_bndry_match_vc1 Mask for err_f_bndry_match_vc1.
4	RW	0x0	mask_err_f_bndry_match_vc0 Mask for err_f_bndry_match_vc0.
3	RW	0x0	mask_phy_errsotsynchs_3 Mask for phy_errsotsynchs_3.
2	RW	0x0	mask_phy_errsotsynchs_2 Mask for phy_errsotsynchs_2.
1	RW	0x0	mask_phy_errsotsynchs_1 Mask for phy_errsotsynchs_1.
0	RW	0x0	mask_phy_errsotsynchs_0 Mask for phy_errsotsynchs_0.

CSI2HOST_MSK2

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	mask_fifo_overflow Mask for fifo overflow.
27	RW	0x0	mask_phy_errcodehs_3 Mask for phy_errcodehs_3.
26	RW	0x0	mask_phy_errcodehs_2 Mask for phy_errcodehs_2.

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Bit	Attr	Reset Value	Description
25	RW	0x0	mask_phy_errcodehs_1 Mask for phy_errcodehs_1.
24	RW	0x0	mask_phy_errcodehs_0 Mask for phy_errcodehs_0.
23:20	RO	0x0	reserved
19	RW	0x0	mask_phy_errcontrol_3 Mask for phy_errcontrol_3.
18	RW	0x0	mask_phy_errcontrol_2 Mask for phy_errcontrol_2.
17	RW	0x0	mask_phy_errcontrol_1 Mask for phy_errcontrol_1.
16	RW	0x0	mask_phy_errcontrol_0 Mask for phy_errcontrol_0.
15	RW	0x0	mask_err_id_vc3 Mask for err_id_vc3.
14	RW	0x0	mask_err_id_vc2 Mask for err_id_vc2.
13	RW	0x0	mask_err_id_vc1 Mask for err_id_vc1.
12	RW	0x0	mask_err_id_vc0 Mask for err_id_vc0.
11	RW	0x0	mask_vc3_err_ecc_corrected Mask for vc3_err_ecc_corrected.
10	RW	0x0	mask_vc2_err_ecc_corrected Mask for vc2_err_ecc_corrected.
9	RW	0x0	mask_vc1_err_ecc_corrected Mask for vc1_err_ecc_corrected.
8	RW	0x0	mask_vc0_err_ecc_corrected Mask for vc0_err_ecc_corrected.
7	RW	0x0	mask_phy_errsoths_3 Mask for phy_errsoths_3.
6	RW	0x0	mask_phy_errsoths_2 Mask for phy_errsoths_2.
5	RW	0x0	mask_phy_errsoths_1 Mask for phy_errsoths_1
4	RW	0x0	mask_phy_errsoths_0 Mask for phy_errsoths_0.
3	RW	0x0	mask_phy_erresc_3 Mask for phy_erresc_3.
2	RW	0x0	mask_phy_erresc_2 Mask for phy_erresc_2.
1	RW	0x0	mask_phy_erresc_1 Mask for phy_erresc_1.
0	RW	0x0	mask_phy_erresc_0 Mask for phy_erresc_0.

CSI2HOST_CONTROL

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RW	0x03	sw_datatype_le The datatype of line end.
25:20	RW	0x02	sw_datatype_ls The datatype of line start.
19:14	RW	0x01	sw_datatype_fe The datatype of frame end.

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Bit	Attr	Reset Value	Description
13:8	RW	0x00	sw_datatype_fs The datatype of frame start.
7	RO	0x0	reserved
6	RW	0x0	sw_debug_en 1'b0: Normal mode 1'b1: Debug mode
5	RW	0x0	sw_adapter_mux 1'b0: New rtl code for dphy adapter 1'b1: Old rtl code for dphy adapter
4	RW	0x0	sw_dsi_en 1'b0: For csi2 1'b1: For dsi
3:1	RO	0x0	reserved
0	RW	0x0	sw_cphy_en 1'b0: For dphy 1'b1: For cphy

CSI2HOST_HEADER_0

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ro_header_0 32bit header {2'd0,ecc,word_count,vc,data_type} ro_header_0 is latest and ro_header_3 is earliest.

CSI2HOST_HEADER_1

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ro_header_1 32bit header {2'd0,ecc,word_count,vc,data_type}

CSI2HOST_HEADER_2

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ro_header_2 32bit header {2'd0,ecc,word_count,vc,data_type}

CSI2HOST_HEADER_3

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ro_header_3 32bit header {2'd0,ecc,word_count,vc,data_type}

19.5 Application Notes

- The most important step is configuring the right CSI2HOST_N_LANES before pulling up csi_resetn. If the host is used to receive DSI data, the sw_dsi_en must be enabled, and the sw_datatype_fs, sw_datatype_fe, sw_datatype_ls, sw_datatype_le must be configured correctly. When the sw_dsi_en is enabled, those debug or error detection registers are useless.
- There are five MIPI CSI HOST in RK3576 SOC, CSI HOST0 is connected to MIPI CD Combo PHY0, CSI HOST1/2 are connected to MIPI DPHY0, CSI HOST3/4 are connected to MIPI DPHY1.
- When MIPI DPHY0 works in full mode, the SYS_GRF_SOC_CON5[1] should be set to 0, and the CSI HOST1 is connected to MIPI DPHY0 4 lanes.
- When MIPI DPHY0 works in split mode, the SYS_GRF_SOC_CON5[1] should be set to 1, and CSI HOST1 is connected to MIPI DPHY0 lane0/1, CSI HOST2 is connected to MIPI

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DPHY0 lane2/3.

- When MIPI DPHY1 works in full mode, the SYS_GRF_SOC_CON5[2] should be set to 0, and the CSI HOST3 is connected to MIPI DPHY1 4 lanes.
- When MIPI DPHY1 works in split mode, the SYS_GRF_SOC_CON5[2] should be set to 1, and CSI HOST3 is connected to MIPI DPHY1 lane0/1, CSI HOST4 is connected to MIPI DPHY1 lane2/3.

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Chapter 20 MIPI CSI DPHY

20.1 Overview

The features of MIPI CSI DPHY are as follow:

- Analog mixed-signal hard-macro LP/HS Receiver solution
- Designed to MIPI v1.2 Specifications
- Integrated PHY Protocol Interface(PPI) interfaces to DSI/CSI and UniPro MIPI protocols
- 2.5 Gbps maximum data transfer rate per lane
- Expandable to support 4 data lanes, providing up to 10 Gbps transfer rate
- HS-RX, LP-RX, LP-TX and Calibration supported
- 10Mbps per lane in low-power mode
- Unidirectional and bi-directional modes supported
- Automatic termination control for HS and LP modes
- Buffers with tunable On-Die-Termination
- Includes embedded ESD, boundary scan and BIST
- Dual clock lanes mode supported

20.2 Block Diagram

MIPI D-PHY configuration contains one Clock Lane Module and four Data Lane Modules. Each of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect. Figure below shows a Universal Lane Module Diagram with a global overview of internal functionality of the CIL function. This Universal Module can be used for all Lane types. The requirements for the 'Control and Interface Logic'(CIL) function depend on the Lane type and Lane side.

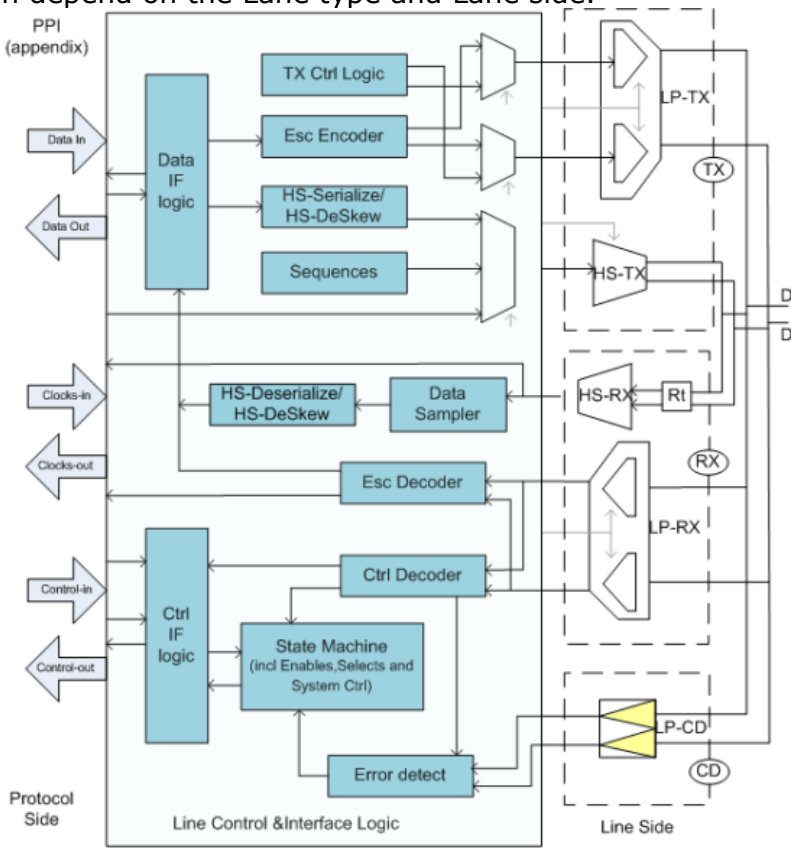


Fig. 20-1 MIPI CSI DPHY Block Diagram

20.3 Register Description

20.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

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Operational Base

Name	Base Address
CSIDPHY0	0x2B030000
CSIDPHY1	0x2B070000

20.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CSI_DPHY_LANE_EN	0x0000	W	0x00000001	Clk/data lane enable
CSI_DPHY_LANE_CK1_EN	0x002C	W	0x0000001E	Clk1 lane enable
CSI_DPHY_DIGITAL_CLK_PHASE	0x0034	W	0x000000C0	Digital clock phase
CSI_DPHY_LANE_CLK_3_PHASE	0x0038	W	0x00000036	Lane clock/3 phase
CSI_DPHY_LANE_2_1_0_PHASE	0x003C	W	0x000000DB	Data lane 2/1/0 phase
CSI_DPHY_DIGITAL_CLK_REVERSE	0x0048	W	0x00000010	Digital clock reverse
CSI_DPHY_DUAL_CLK_ENABLE	0x0080	W	0x0000001F	MIPI/LVDS enable
CSI_DPHY_LANE_CLK1_PHASE	0x00CC	W	0x00000030	Lane clock1 phase
CSI_DPHY_LANE_CK_MODE	0x0128	W	0x0000000F	Clock lane mode
CSI_DPHY_LANE_CK_MSB	0x0138	W	0x00000086	MSB enable
CSI_DPHY_LANE_CK_TTAGO	0x0140	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_CK_TTASURE	0x0144	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_CK_TTAWAIT	0x0148	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_CK_THSSETTLE	0x0160	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_CK_CAL_EN	0x0168	W	0x0000007F	Calibration reception enable
CSI_DPHY_LANE_0_MSB	0x01B8	W	0x00000086	MSB enable
CSI_DPHY_LANE_0_TTAGO	0x01C0	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_0_TTASURE	0x01C4	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_0_TTAWAIT	0x01C8	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_0_THSSETTLE	0x01E0	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_0_CAL_EN	0x01E8	W	0x00000000	Calibration reception enable
CSI_DPHY_LANE_1_MSB	0x0238	W	0x00000086	MSB enable
CSI_DPHY_LANE_1_TTAGO	0x0240	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_1_TTASURE	0x0244	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_1_TTAWAIT	0x0248	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_1_THSSETTLE	0x0260	W	0x0000001B	The count time of the THS-SETTLE by protocol

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Name	Offset	Size	Reset Value	Description
CSI_DPHY_LANE_1_CAL_EN	0x0268	W	0x0000007F	Calibration reception enable
CSI_DPHY_LANE_2_MSB	0x02B8	W	0x00000086	MSB enable
CSI_DPHY_LANE_2_TTAGO	0x02C0	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_2_TTASURE	0x02C4	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_2_TTAWAIT	0x02C8	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_2_THSSETTLE	0x02E0	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_2_CAL_EN	0x02E8	W	0x0000007F	Calibration reception enable
CSI_DPHY_LANE_3_MSB	0x0338	W	0x00000086	MSB enable
CSI_DPHY_LANE_3_TTAGO	0x0340	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_3_TTASURE	0x0344	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_3_TTAWAIT	0x0348	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_3_THSSETTLE	0x0360	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_3_CAL_EN	0x0368	W	0x0000007F	Calibration reception enable
CSI_DPHY_LANE_CK1_MODE	0x03A8	W	0x00000000	Clock lane1 mode
CSI_DPHY_LANE_CK1_MSB	0x03B8	W	0x00000086	MSB enable
CSI_DPHY_LANE_CK1_TTAGO	0x03C0	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_CK1_TTASURE	0x03C4	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_CK1_TTAWAIT	0x03C8	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_CK1_THSSETTLE	0x03E0	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_CK1_CAL_EN	0x03E8	W	0x0000007F	Calibration reception enable

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

20.3.3 Detail Registers Description

CSI_DPHY_LANE_EN

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_en_ck Enable D-PHY clock lane:active high.
5	RW	0x0	lane_en_3 Enable D-PHY lane3:active high.
4	RW	0x0	lane_en_2 Enable D-PHY lane2:active high.
3	RW	0x0	lane_en_1 Enable D-PHY lane1:active high.

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Bit	Attr	Reset Value	Description
2	RW	0x0	lane_en_0 Enable D-PHY lane0:active high.
1:0	RW	0x1	reserved Reserved

CSI_DPHY_LANE_CK1_EN

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	reserved1 Reserved
6	RW	0x0	lane_en_ck1 Enable D-PHY clock1 lane:active high.
5:0	RW	0x1e	reserved Reserved

CSI_DPHY_DIGITAL_CLK_PHASE

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:3	RW	0x18	reserved Reserved
2:0	RW	0x0	digital_clk_phase 3'b000: Phase 0(default value) 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.

CSI_DPHY_LANE_CLK_3_PHASE

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x3	lane_clk_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.

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Bit	Attr	Reset Value	Description
3:1	RW	0x3	lane_3_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
0	RW	0x0	lane_2_phase_msb See lane_2_phase for the details of the register.

CSI_DPHY_LANE_2_1_0_PHASE

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x3	lane_2_phase {lane_2_phase_msb,lane_2_phase} 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
5:3	RW	0x3	lane_1_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
2:0	RW	0x3	lane_0_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.

CSI_DPHY_DIGITAL_CLK_REVERSE

Address: **Operational Base** + offset (0x0048)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	digital_clk_reverse 1'b0: Make the digital sample clock positive(default value) 1'b1: Reverse the digital sample clock
6:0	RW	0x10	reserved Reserved

CSI_DPHY_DUAL_CLK_ENABLE

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	dual_clk_mode_en 1'b0: Enable single clock lane mode 1'b1: Enable dual clock lanes mode
5:1	RW	0x0f	reserved Reserved
0	RW	0x1	reg_dig_rstn 1'b0: Reset 1'b1: Normal

CSI_DPHY_LANE_CLK1_PHASE

Address: **Operational Base** + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x3	lane_clk1_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
3	RO	0x0	reserved
2:0	RW	0x0	digital_clk1_phase 3'b000: Phase 0(default value) 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.

CSI_DPHY_LANE_CK_MODE

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	lane_ck_mode 2'b00: Disable continuous clock mode 2'b11: Enable continuous clock mode

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Bit	Attr	Reset Value	Description
3:0	RW	0xf	reserved Reserved

CSI_DPHY_LANE_CK_MSB

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	reserved1 Reserved
6	RW	0x0	lane_ck_msb MSB enable for pin_rxdatahs_* 1'b0: Disable 1'b1: Enable
5:0	RW	0x06	reserved Reserved

CSI_DPHY_LANE_CK_TTAGO

Address: **Operational Base** + offset (0x0140)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_ck_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_CK_TTASURE

Address: **Operational Base** + offset (0x0144)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_ck_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_CK_TTAWAIT

Address: **Operational Base** + offset (0x0148)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_ck_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_CK_THSSETTLE

Address: **Operational Base** + offset (0x0160)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_ck_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06

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Bit	Attr	Reset Value	Description
			250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

CSI_DPHY_LANE_CK_CAL_EN

Address: **Operational Base** + offset (0x0168)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_ck_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RW	0x7f	reserved Reserved

CSI_DPHY_LANE_0_MSB

Address: **Operational Base** + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	reserved1 Reserved
6	RW	0x0	lane_0_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RW	0x06	reserved Reserved

CSI_DPHY_LANE_0_TTAGO

Address: **Operational Base** + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_0_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_0_TTASURE

Address: **Operational Base** + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_0_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

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CSI_DPHY_LANE_0_TTAWAIT

Address: **Operational Base** + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_0_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_0_THSSETTLE

Address: **Operational Base** + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_0_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

CSI_DPHY_LANE_0_CAL_EN

Address: **Operational Base** + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_0_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

CSI_DPHY_LANE_1_MSB

Address: **Operational Base** + offset (0x0238)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	reserved1 Reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	lane_1_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RW	0x06	reserved Reserved

CSI_DPHY_LANE_1_TTAGO

Address: **Operational Base** + offset (0x0240)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_1_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_1_TTASURE

Address: **Operational Base** + offset (0x0244)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_1_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_1_TTAWAIT

Address: **Operational Base** + offset (0x0248)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_1_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_1_THSSETTLE

Address: **Operational Base** + offset (0x0260)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_1_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23

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Bit	Attr	Reset Value	Description
			1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

CSI_DPHY_LANE_1_CAL_EN

Address: **Operational Base** + offset (0x0268)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_1_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RW	0x7f	reserved Reserved

CSI_DPHY_LANE_2_MSB

Address: **Operational Base** + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	reserved1 Reserved
6	RW	0x0	lane_2_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RW	0x06	reserved Reserved

CSI_DPHY_LANE_2_TTAGO

Address: **Operational Base** + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_2_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_2_TTASURE

Address: **Operational Base** + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_2_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_2_TTAWAIT

Address: **Operational Base** + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x32	lane_2_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_2_THSSETTLE

Address: **Operational Base** + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_2_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

CSI_DPHY_LANE_2_CAL_EN

Address: **Operational Base** + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_2_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RW	0x7f	reserved Reserved

CSI_DPHY_LANE_3_MSB

Address: **Operational Base** + offset (0x0338)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	reserved1 Reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	lane_3_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RW	0x06	reserved Reserved

CSI_DPHY_LANE_3_TTAGO

Address: **Operational Base** + offset (0x0340)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_3_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_3_TTASURE

Address: **Operational Base** + offset (0x0344)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_3_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_3_TTAWAIT

Address: **Operational Base** + offset (0x0348)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_0_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_3_THSSETTLE

Address: **Operational Base** + offset (0x0360)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_3_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23

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Bit	Attr	Reset Value	Description
			1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

CSI_DPHY_LANE_3_CAL_EN

Address: **Operational Base** + offset (0x0368)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_3_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RW	0x7f	reserved Reserved

CSI_DPHY_LANE_CK1_MODE

Address: **Operational Base** + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	lane_ck1_mode 2'b00: Disable continuous clock mode 2'b11: Enable continuous clock mode
3:0	RO	0x0	reserved

CSI_DPHY_LANE_CK1_MSB

Address: **Operational Base** + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	reserved1 Reserved
6	RW	0x0	lane_ck1_msb MSB enable for pin_rxdatahs_* 1'b0: Disable 1'b1: Enable
5:0	RW	0x06	reserved Reserved

CSI_DPHY_LANE_CK1_TTAGO

Address: **Operational Base** + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_ck1_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_CK1_TTASURE

Address: **Operational Base** + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_ck1_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

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CSI_DPHY_LANE_CK1_TTAWAIT

Address: **Operational Base** + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_ck1_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_CK1_THSSETTLE

Address: **Operational Base** + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_ck1_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

CSI_DPHY_LANE_CK1_CAL_EN

Address: **Operational Base** + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_ck1_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RW	0x7f	reserved Reserved

20.4 Application Notes

20.4.1 MIPI SINGLE CLOCK LANE Mode Application

step1: send 0x7d to register LANE_EN. Enable the D-PHY.

step2: send 0x01f001f0 to register CSIDPHY_GRF_CON0.Enable the clock lane and 4 data lanes.

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step3: According to data rate, write corresponding value to Ths-settle registers for lanes. If TX skew calibration function is on, send 0xff to register LANE_*_CAL_EN.

20.4.2 MIPI DUAL CLOCK LANES MODE Application

step1: send 0x7d to register CSI_DPHY_LANE_EN. Enable the D-PHY.
step2: send 0x5f to register CSI_DPHY_DUAL_CLK_ENABLE.Enable dual clock lanes mode.
step3: send 0x05f005f0 to register CSIDPHY_GRF_CON0.Enable 2 clock lanes and 4 data lanes.
step4: According to data rate, write corresponding value to Ths-settle registers for lanes. If TX skew calibration function is on, send 0xff to register LANE_*_CAL_EN.

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Chapter 21 MIPI D-PHY / C-PHY Combo PHY

21.1 Overview

The MIPI D-PHY / C-PHY Combo PHY is a high speed, low power, low cost PHY, especially suited for mobile applications. It is commonly used for connecting a mobile display driver or a camera sensor to a host processor according to MIPI Alliance DPHY V2.0 and C-PHY V1.1 specification.

The features of D-PHY are:

- D-PHY spec v2.0 compatible
- Supports 1 Clock lane and up to 4 data lanes scalability in TX and RX respectively
- High-Speed mode: Differential and terminated
  - TX: 80Mbps ~ 2500 Mbps
  - RX: 80Mbps ~ 4500 Mbps
- Low-Power mode: Single-ended and non-terminated, 1.2 V swing: 10 Mbps maximum
- All lanes support high-speed transmission in the forward direction.
- Bi-directional data transmission in Low-Power mode at the Master Data Lane 0 only.
- Synchronous link between Master (data source) and Slave (data sink).

The features of C-PHY are:

- C-PHY spec v1.1 compatible
- Supports up to 3 trios scalability in TX and RX respectively
- High-Speed mode: Differential and terminated
  - TX: 80Msps ~ 1700Msps
  - RX: 80Msps ~ 2500Msps
- Low-Power mode: Single-ended and non-terminated: 10Mbps maximum

Note: The TX and RX only support operate in the same PHY mode.

21.2 Block Diagram

The 4-lane D-PHY architecture including lanes and common block is shown in the below figure. IP is composed of common block (BIAS/PLL), Master clock lane, Master data 4 lanes, Slave clock lane, and Slave data 4 lanes. PLL offers the operating clock for Master block operation. Slave block uses clock from Slave clock lane input PAD at the normal operation mode. BIAS block make the analog reference voltages and currents for analog function according to MIPI specification. HS mode 0.4V voltage regulator is embedded into IP and is just used for Master blocks.

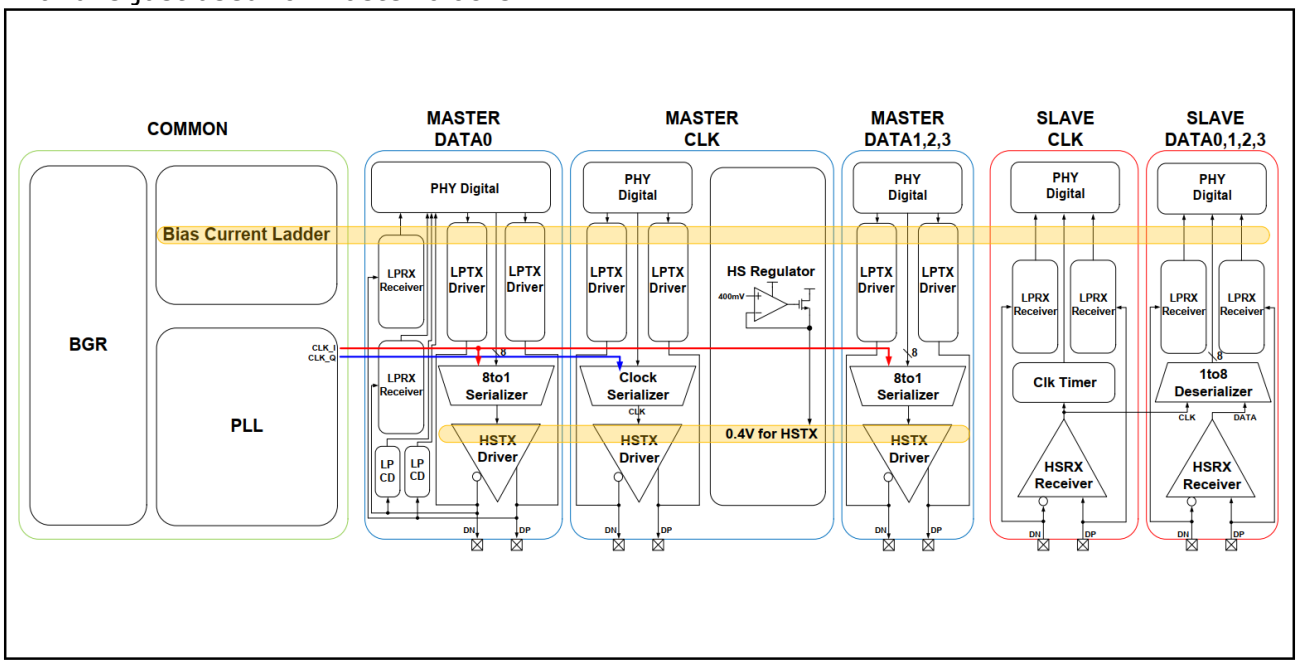


Fig. 21-1 MIPI DCPHY Block Diagram

MIPI DCPHY comprises with:

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- BGR and bias generator
- Phase Locked Loop (PLL)
- Serializer
- HS TX Driver
- LP TX Driver
- Deserializer
- HS RX Receiver
- LP RX Receiver

21.3 Function Description

21.3.1 BGR and bias generator

The BGR circuit generates high-accuracy reference voltage of 820mV across PVT variation. A bias generator makes internal-resistor (RMRES)-referred currents, and these currents are distributed to each block in Common and Lanes. The internal resistor-referred current is generated using internally integrated replica resistor to compensate resistance error across PVT variation.

21.3.2 Phase Locked Loop (PLL)

The PLL in the Common synthesizes high-speed clock, which is used for TX serializer from a reference clock. In the PHY, the high frequency clock from PLL is used in the serialization of TX data. The following are the main features of the PLL.

- Supports output frequency from 80MHz to 2.5GHz clock
- Supports pre-defined and programmable divider setting for MIPI D-PHY specification
- Supports spread spectrum clocking (SSC) with sigma-delta modulated fractional divider

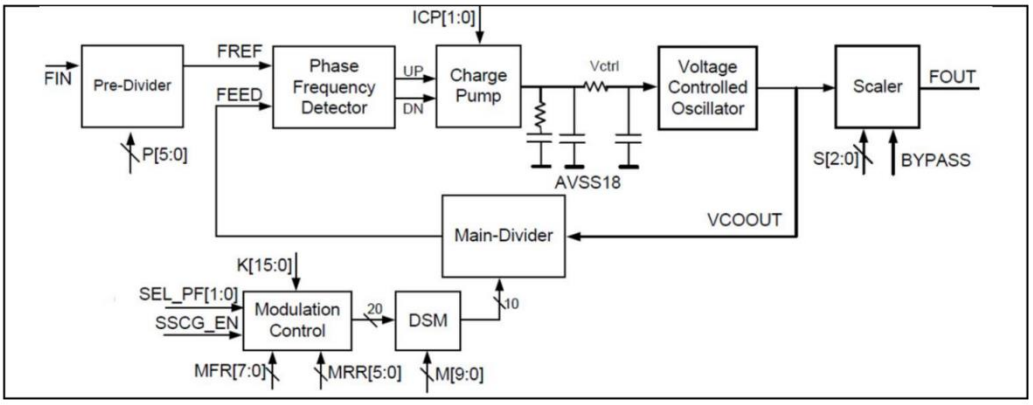


Fig. 21-2 PLL Diagram

21.3.3 Serializer

The serializer accepts 8-bit data from the PHY digital which is synchronized to TX byte clock. The parallel data is converted to the high-speed serial data. Finally, serializer transmits the serial data through the driver.

21.3.4 HS TX Driver

The driver generates baud-rate voltage waveform on TX output pads. The driver comprises of pre-driver and main-driver. The output data of serializer are delivered to the main-driver via the pre-driver. The main driver is based on voltage-mode driver to achieve a small power consumption and voltage swing.

21.3.5 LP TX Driver

In the low power mode, LP TX driver sends the low frequency data under 10Mbps. Generally, LP-11 stop state and HS enter sequence (LP-11 - LP-01 - LP-00) are used mostly.

21.3.6 Deserializer

In the BIST (Built-In Self-Test) mode, the serial data from the serializer is fed back to the de-serializer. And in the real mode, the real data from HS-RX receiver is sent to the de-serializer. De-serializer converted serial data to 8-bit parallel data and transferred them into PHY digital circuit for sending data to link or checking bit error at BIST mode.

21.3.7 HS RX Receiver

The high speed data from the MIPI D-PHY master has the MIPI D-PHY electrical

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characteristics. HS RX receiver convert it to the TTL CMOS level and send it to de-serializer for making the low parallel data.

21.3.8 LP RX Receiver

In the low power mode, LP RX receiver make esc clock from LP signal and converts the voltage level from 1.2V level to TTL CMOS logic level. And it sends them to PHY digital for command interpretation. And LP RX receiver always watches the DP/DN signal level. If DP/DN goes to LP-11, PHY recognizes Stop-state, and enters to low power mode.

21.3.9 PLL and Clock Lane Connection

The below figure illustrates the PLL and Clock Lane connection. MIPI D-PHY is source synchronous system. Master clock lane sends high speed differential clock to Slave clock lane. During LP mode (Low Power mode), LP signals are sent by master block. LP-TX sends the LP signals for changing mode between LP mode and HS mode. Slave block has the termination resistor between differential signals that is enabled during HS mode. Master PLL generates the high speed clock from input clock.

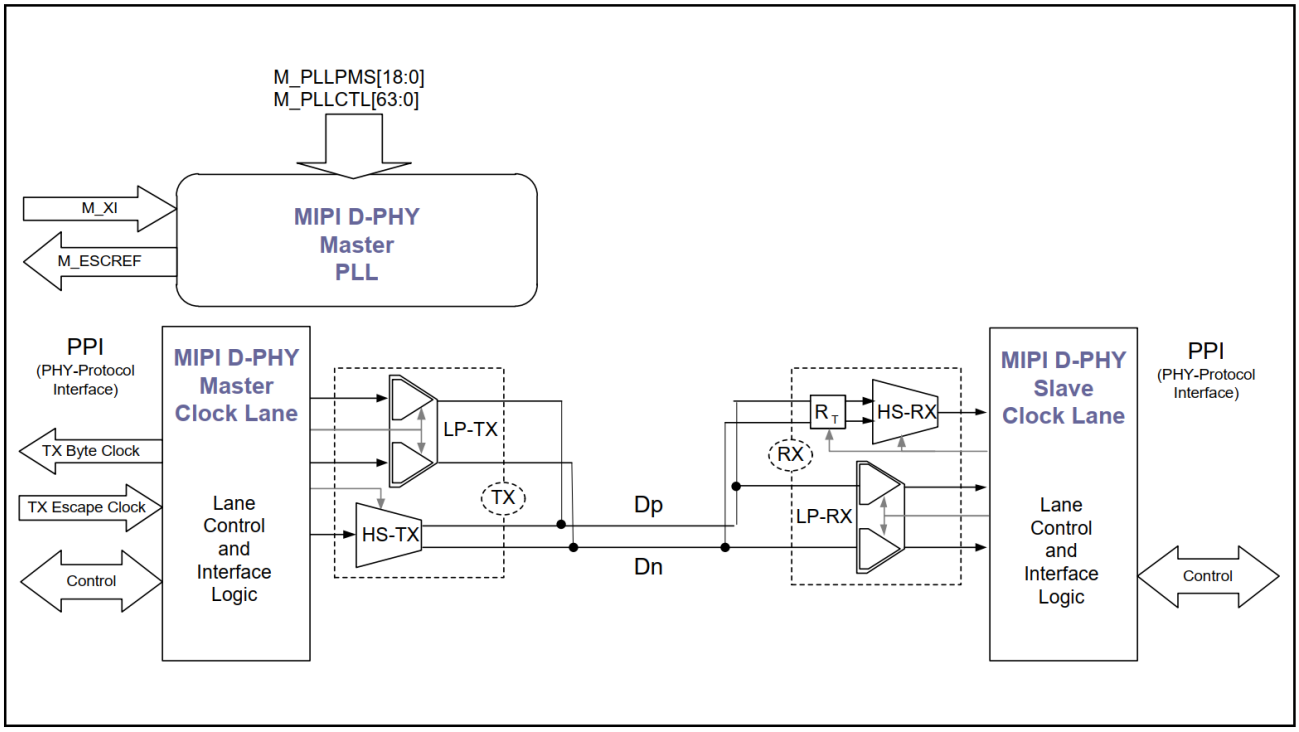


Fig. 21-3 Clock Lane Connection

21.3.10 Data Lane Connection

The below figure illustrates the Data0 Lane connection between Master and the Slave. Master Data0 lane is the special lane for DSI interface because it has LP-CD and LP-RX. LP-RX is used for Turn-Around function according to MIPI standard specification. It is used to be called as BTA (Bus Turn-Around). It is known that BTA is needed for sending the Low Power Data Transmission from Slave to Master. LP-CD (Low Power Contention Detector) is used for detecting the abnormal state when the both of Master LP-TX and Slave LP-TX at BTA mode are enabled and the output signals are conflicted.

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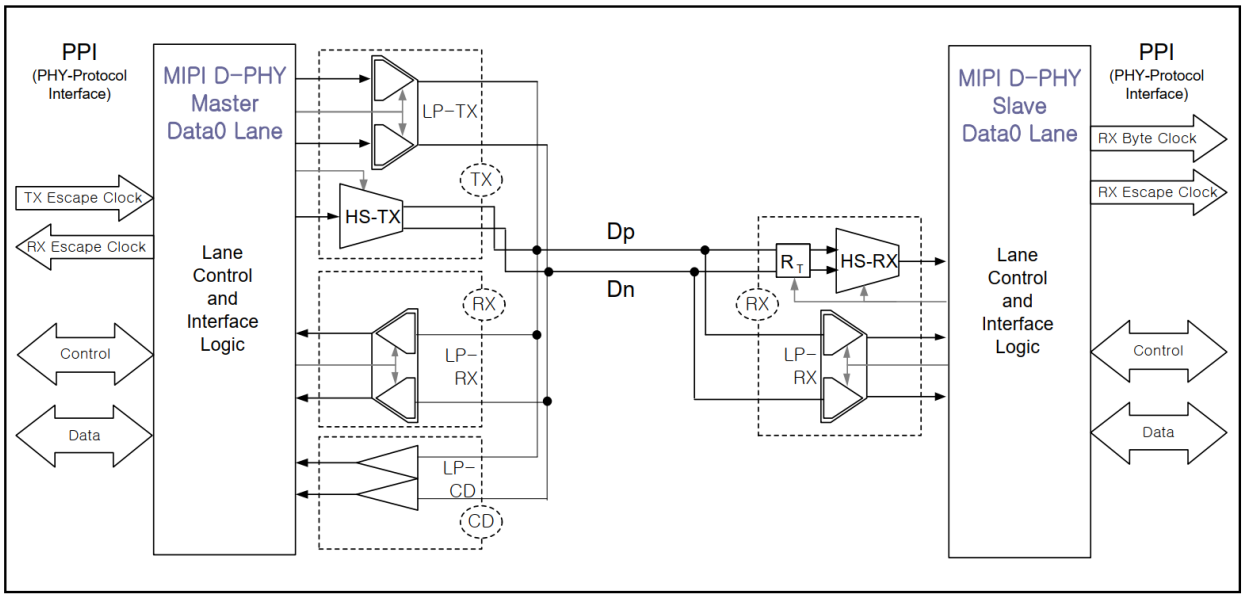


Fig. 21-4 Data 0 Lane Connection

The below figure illustrates the Data1/2/3 Lane connection between Master and the Slave. LP mode signals are used for switching mode between LP mode and HS mode. HS mode is used for interfacing high speed signals. All interface pins between PHY and protocol layer are defined at MIPI stand specification, PPI (PHY-Protocol Interface). Slave block has the termination resistor between differential signals that is enabled during HS mode.

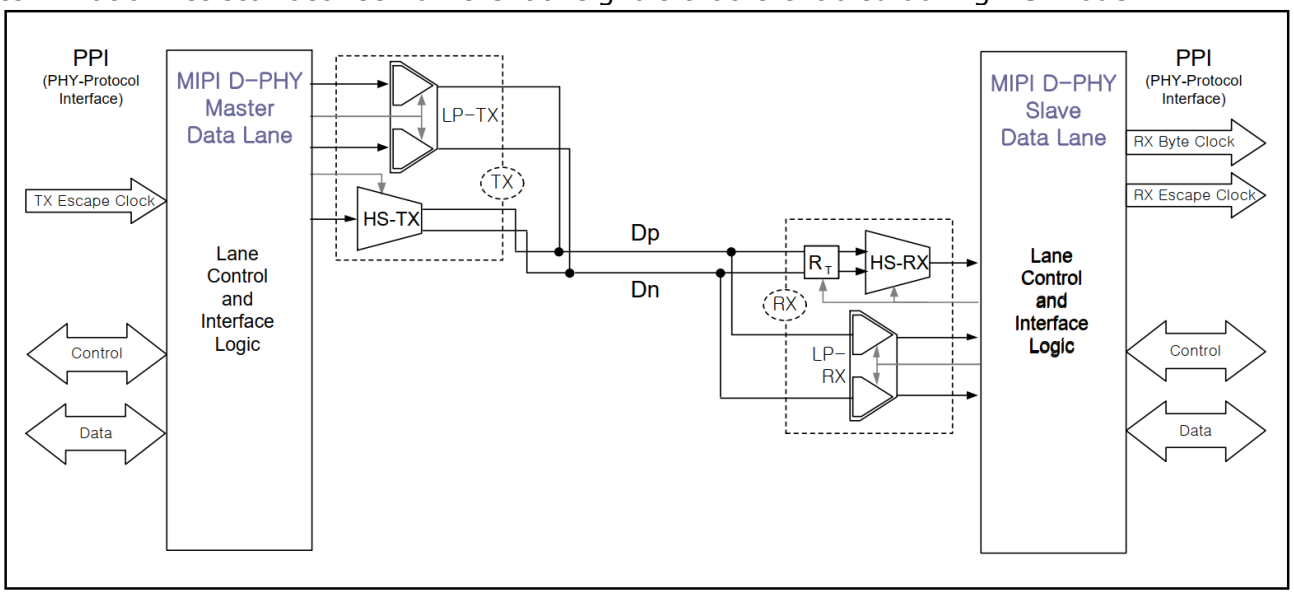


Fig. 21-5 Data 1/2/3 Lane Connection

21.4 Register Description

21.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

21.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DCPHY_M0_BIAS_CON0	0x0000	W	0x00000010	BIAS Control Register0
DCPHY_M0_BIAS_CON1	0x0004	W	0x00000110	BIAS Control Register1
DCPHY_M0_BIAS_CON2	0x0008	W	0x00003223	BIAS Control Register2
DCPHY_M0_BIAS_CON4	0x0010	W	0x00000000	BIAS Control Register4
DCPHY_M0_PLL_CON0	0x0100	W	0x00000000	PLL Control Register0
DCPHY_M0_PLL_CON1	0x0104	W	0x00000000	PLL Control Register1

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Name	Offset	Size	Reset Value	Description
DCPHY_M0_PLL_CON2	0x0108	W	0x00000000	PLL Control Register2
DCPHY_M0_PLL_CON3	0x010C	W	0x00000000	PLL Control Register3
DCPHY_M0_PLL_CON4	0x0110	W	0x00000000	PLL Control Register4
DCPHY_M0_PLL_CON5	0x0114	W	0x00000000	PLL Control Register5
DCPHY_M0_PLL_CON6	0x0118	W	0x00000000	PLL Control Register6
DCPHY_M0_PLL_CON7	0x011C	W	0x00000000	PLL Control Register7
DCPHY_M0_PLL_CON8	0x0120	W	0x00000000	PLL Control Register8
DCPHY_M0_PLL_STAT0	0x0140	W	0x00000000	PLL Status Register0
DCPHY_M0_DPHY_MC_GNR_CON0	0x0300	W	0x00000000	D-PHY Master Clock Lane General Control Register0
DCPHY_M0_DPHY_MC_GNR_CON1	0x0304	W	0x00000000	D-PHY Master Clock Lane General Control Register1
DCPHY_M0_DPHY_MC_ANA_CON0	0x0308	W	0x00007133	D-PHY Master Clock Lane Analog Block Control Register0
DCPHY_M0_DPHY_MC_ANA_CON1	0x030C	W	0x00000000	D-PHY Master Clock Lane Analog Block Control Register1
DCPHY_M0_DPHY_MC_ANA_CON2	0x0310	W	0x00000000	D-PHY Master Clock Lane Analog Block Control Register2
DCPHY_M0_DPHY_MC_ANA_CON3	0x0314	W	0x00000000	D-PHY Master Clock Lane Analog Block Control Register3
DCPHY_M0_DPHY_MC_TIME_CON0	0x0330	W	0x00000000	D-PHY Master Clock Lane Timing Control Register0
DCPHY_M0_DPHY_MC_TIME_CON1	0x0334	W	0x00000000	D-PHY Master Clock Lane Timing Control Register1
DCPHY_M0_DPHY_MC_TIME_CON2	0x0338	W	0x00000000	D-PHY Master Clock Lane Timing Control Register2
DCPHY_M0_DPHY_MC_TIME_CON3	0x033C	W	0x00000000	D-PHY Master Clock Lane Timing Control Register3
DCPHY_M0_DPHY_MC_TIME_CON4	0x0340	W	0x00000000	D-PHY Master Clock Lane Timing Control Register4
DCPHY_M0_DPHY_MC_DATA_CON0	0x0344	W	0x00000000	D-PHY Master Clock Lane Data Control Register0
DCPHY_M0_DPHY_MC_DESKEW_CON0	0x0350	W	0x00000000	D-PHY Master Clock Lane Skew Calibration Control Register0
DCPHY_M0_COMBO_MD0_GNR_CON0	0x0400	W	0x00000000	DC-PHY Combo Master Data 0 Lane General Control Register0
DCPHY_M0_COMBO_MD0_GNR_CON1	0x0404	W	0x00000000	DC-PHY Combo Master Data 0 Lane General Control Register1
DCPHY_M0_COMBO_MD0_ANA_CON0	0x0408	W	0x00007133	DC-PHY Combo Master Data 0 Lane Analog Block Control Register0
DCPHY_M0_COMBO_MD0_ANA_CON1	0x040C	W	0x00000000	DC-PHY Combo Master Data 0 Lane Analog Block Control Register1
DCPHY_M0_COMBO_MD0_ANA_CON2	0x0410	W	0x00000000	DC-PHY Combo Master Data 0 Lane Analog Block Control Register2
DCPHY_M0_COMBO_MD0_TIME_CON0	0x0430	W	0x00000000	DC-PHY Combo Master Data 0 Lane Timing Control Register0
DCPHY_M0_COMBO_MD0_TIME_CON1	0x0434	W	0x00000000	DC-PHY Combo Master Data 0 Lane Timing Control Register1
DCPHY_M0_COMBO_MD0_TIME_CON2	0x0438	W	0x00000000	DC-PHY Combo Master Data 0 Lane Timing Control Register2

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Name	Offset	Size	Reset Value	Description
DCPHY_M0_COMBO_MD0_TIME_CON3	0x043C	W	0x00000000	DC-PHY Combo Master Data 0 Lane Timing Control Register3
DCPHY_M0_COMBO_MD0_TIME_CON4	0x0440	W	0x00000000	DC-PHY Combo Master Data 0 Lane Timing Control Register4
DCPHY_M0_COMBO_MD0_DATA_CON0	0x0444	W	0x00000000	DC-PHY Combo Master Data 0 Lane Data Control Register0
DCPHY_M0_COMBO_MD0_PRGSEQ_CON0	0x0460	W	0x00000000	DC-PHY Combo Master Data 0 Lane Programmable Sequence Control Register0
DCPHY_M0_COMBO_MD0_PRGSEQ_CON1	0x0464	W	0x00000000	DC-PHY Combo Master Data 0 Lane Programmable Sequence Control Register1
DCPHY_M0_COMBO_MD0_PRGSEQ_CON2	0x0468	W	0x00000000	DC-PHY Combo Master Data 0 Lane Programmable Sequence Control Register2
DCPHY_M0_COMBO_MD0_PRGSEQ_CON3	0x046C	W	0x00000000	DC-PHY Combo Master Data 0 Lane Programmable Sequence Control Register3
DCPHY_M0_COMBO_MD1_GNR_CON0	0x0500	W	0x00000000	DC-PHY Combo Master Data 1 Lane General Control Register0
DCPHY_M0_COMBO_MD1_GNR_CON1	0x0504	W	0x00000000	DC-PHY Combo Master Data 1 Lane General Control Register1
DCPHY_M0_COMBO_MD1_ANA_CON0	0x0508	W	0x00007133	DC-PHY Combo Master Data 1 Lane Analog Block Control Register0
DCPHY_M0_COMBO_MD1_ANA_CON1	0x050C	W	0x00000000	DC-PHY Combo Master Data 1 Lane Analog Block Control Register1
DCPHY_M0_COMBO_MD1_ANA_CON2	0x0510	W	0x00000000	DC-PHY Combo Master Data 1 Lane Analog Block Control Register2
DCPHY_M0_COMBO_MD1_TIME_CON0	0x0530	W	0x00000000	DC-PHY Combo Master Data 1 Lane Timing Control Register0
DCPHY_M0_COMBO_MD1_TIME_CON1	0x0534	W	0x00000000	DC-PHY Combo Master Data 1 Lane Timing Control Register1
DCPHY_M0_COMBO_MD1_TIME_CON2	0x0538	W	0x00000000	DC-PHY Combo Master Data 1 Lane Timing Control Register2
DCPHY_M0_COMBO_MD1_TIME_CON3	0x053C	W	0x00000000	DC-PHY Combo Master Data 1 Lane Timing Control Register3
DCPHY_M0_COMBO_MD1_TIME_CON4	0x0540	W	0x00000000	DC-PHY Combo Master Data 1 Lane Timing Control Register4
DCPHY_M0_COMBO_MD1_DATA_CON0	0x0544	W	0x00000000	DC-PHY Combo Master Data 1 Lane Data Control Register0
DCPHY_M0_COMBO_MD1_PRGSEQ_CON0	0x0560	W	0x00000000	DC-PHY Combo Master Data 1 Lane Programmable Sequence Control Register0
DCPHY_M0_COMBO_MD1_PRGSEQ_CON1	0x0564	W	0x00000000	DC-PHY Combo Master Data 1 Lane Programmable Sequence Control Register1
DCPHY_M0_COMBO_MD1_PRGSEQ_CON2	0x0568	W	0x00000000	DC-PHY Combo Master Data 1 Lane Programmable Sequence Control Register2

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Name	Offset	Size	Reset Value	Description
DCPHY_M0_COMBO_MD1_PRGSEQ_CON3	0x056C	W	0x00000000	DC-PHY Combo Master Data 1 Lane Programmable Sequence Control Register3
DCPHY_M0_COMBO_MD2_GNR_CON0	0x0600	W	0x00000000	DC-PHY Combo Master Data 2 Lane General Control Register0
DCPHY_M0_COMBO_MD2_GNR_CON1	0x0604	W	0x00000000	DC-PHY Combo Master Data 2 Lane General Control Register1
DCPHY_M0_COMBO_MD2_ANA_CON0	0x0608	W	0x00007133	DC-PHY Combo Master Data 2 Lane Analog Block Control Register0
DCPHY_M0_COMBO_MD2_ANA_CON1	0x060C	W	0x00000000	DC-PHY Combo Master Data 2 Lane Analog Block Control Register1
DCPHY_M0_COMBO_MD2_ANA_CON2	0x0610	W	0x00000000	DC-PHY Combo Master Data 2 Lane Analog Block Control Register2
DCPHY_M0_COMBO_MD2_TIME_CON0	0x0630	W	0x00000000	DC-PHY Combo Master Data 2 Lane Timing Control Register0
DCPHY_M0_COMBO_MD2_TIME_CON1	0x0634	W	0x00000000	DC-PHY Combo Master Data 2 Lane Timing Control Register1
DCPHY_M0_COMBO_MD2_TIME_CON2	0x0638	W	0x00000000	DC-PHY Combo Master Data 2 Lane Timing Control Register2
DCPHY_M0_COMBO_MD2_TIME_CON3	0x063C	W	0x00000000	DC-PHY Combo Master Data 2 Lane Timing Control Register3
DCPHY_M0_COMBO_MD2_TIME_CON4	0x0640	W	0x00000000	DC-PHY Combo Master Data 2 Lane Timing Control Register4
DCPHY_M0_COMBO_MD2_DATA_CON0	0x0644	W	0x00000000	DC-PHY Combo Master Data 2 Lane Data Control Register0
DCPHY_M0_COMBO_MD2_PRGSEQ_CON0	0x0660	W	0x00000000	DC-PHY Combo Master Data 2 Lane Programmable Sequence Control Register0
DCPHY_M0_COMBO_MD2_PRGSEQ_CON1	0x0664	W	0x00000000	DC-PHY Combo Master Data 2 Lane Programmable Sequence Control Register1
DCPHY_M0_COMBO_MD2_PRGSEQ_CON2	0x0668	W	0x00000000	DC-PHY Combo Master Data 2 Lane Programmable Sequence Control Register2
DCPHY_M0_COMBO_MD2_PRGSEQ_CON3	0x066C	W	0x00000000	DC-PHY Combo Master Data 2 Lane Programmable Sequence Control Register3
DCPHY_M0_DPHY_MD3_GNR_CON0	0x0700	W	0x00000000	D-PHY Master Data 3 Lane General Control Register0
DCPHY_M0_DPHY_MD3_GNR_CON1	0x0704	W	0x00000000	D-PHY Master Data 3 Lane General Control Register1
DCPHY_M0_DPHY_MD3_ANA_CON0	0x0708	W	0x00007133	D-PHY Master Data 3 Lane Analog Block Control Register0
DCPHY_M0_DPHY_MD3_ANA_CON1	0x070C	W	0x00000000	D-PHY Master Data 3 Lane Analog Block Control Register1
DCPHY_M0_DPHY_MD3_ANA_CON2	0x0710	W	0x00000000	D-PHY Master Data 3 Lane Analog Block Control Register2
DCPHY_M0_DPHY_MD3_TIME_CON0	0x0730	W	0x00000000	D-PHY Master Data 3 Lane Timing Control Register0
DCPHY_M0_DPHY_MD3_TIME_CON1	0x0734	W	0x00000000	D-PHY Master Data 3 Lane Timing Control Register1

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Name	Offset	Size	Reset Value	Description
DCPHY_M0_DPHY_MD3_TIME_CON2	0x0738	W	0x00000000	D-PHY Master Data 3 Lane Timing Control Register2
DCPHY_M0_DPHY_MD3_TIME_CON3	0x073C	W	0x00000000	D-PHY Master Data 3 Lane Timing Control Register3
DCPHY_M0_DPHY_MD3_TIME_CON4	0x0740	W	0x00000000	D-PHY Master Data 3 Lane Timing Control Register4
DCPHY_M0_DPHY_MD3_DATA_CON0	0x0744	W	0x00000000	D-PHY Master Data 3 Lane Data Control Register0
DCPHY_M0_DPHY_SC_GNR_CON0	0x0B00	W	0x00000000	D-PHY Slave Clock Lane General Control Register0
DCPHY_M0_DPHY_SC_GNR_CON1	0x0B04	W	0x00000000	D-PHY Slave Clock Lane General Control Register1
DCPHY_M0_DPHY_SC_ANA_CON0	0x0B08	W	0x00000000	D-PHY Slave Clock Lane Analog Block Control Register0
DCPHY_M0_DPHY_SC_ANA_CON1	0x0B0C	W	0x00000000	D-PHY Slave Clock Lane Analog Block Control Register1
DCPHY_M0_DPHY_SC_ANA_CON2	0x0B10	W	0x00000000	D-PHY Slave Clock Lane Analog Block Control Register2
DCPHY_M0_DPHY_SC_ANA_CON3	0x0B14	W	0x00000000	D-PHY Slave Clock Lane Analog Block Control Register3
DCPHY_M0_DPHY_SC_ANA_CON4	0x0B18	W	0x00000000	D-PHY Slave Clock Lane Analog Block Control Register4
DCPHY_M0_DPHY_SC_ANA_CON5	0x0B1C	W	0x00000000	D-PHY Slave Clock Lane Analog Block Control Register5
DCPHY_M0_DPHY_SC_TIME_CON0	0x0B30	W	0x00000000	D-PHY Slave Clock Lane Timing Control Register0
DCPHY_M0_COMBO_SD0_GNR_CON0	0x0C00	W	0x00000000	DC-PHY Combo Slave Data 0 Lane General Control Register0
DCPHY_M0_COMBO_SD0_GNR_CON1	0x0C04	W	0x00000000	DC-PHY Combo Slave Data 0 Lane General Control Register1
DCPHY_M0_COMBO_SD0_ANA_CON0	0x0C08	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Analog Block Control Register0
DCPHY_M0_COMBO_SD0_ANA_CON1	0x0C0C	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Analog Block Control Register1
DCPHY_M0_COMBO_SD0_ANA_CON2	0x0C10	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Analog Block Control Register2
DCPHY_M0_COMBO_SD0_ANA_CON3	0x0C14	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Analog Block Control Register3
DCPHY_M0_COMBO_SD0_ANA_CON4	0x0C18	W	0x00000000	DC-PHY Combo Slave Data0 Lane Analog Block Control Register4
DCPHY_M0_COMBO_SD0_ANA_CON6	0x0C20	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Analog Block Control Register6
DCPHY_M0_COMBO_SD0_ANA_CON7	0x0C24	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Analog Block Control Register7
DCPHY_M0_COMBO_SD0_TIME_CON0	0x0C30	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Timing Control Register0
DCPHY_M0_COMBO_SD0_TIME_CON1	0x0C34	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Timing Control Register1
DCPHY_M0_COMBO_SD0_DATA_CON0	0x0C38	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Data Control Register0
DCPHY_M0_COMBO_SD0_DESKEW_CON0	0x0C40	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Skew Calibration Control Register0

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Name	Offset	Size	Reset Value	Description
DCPHY_M0_COMBO_SD0_DESKEW_CON1	0x0C44	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Skew Calibration Control Register1
DCPHY_M0_COMBO_SD0_DESKEW_CON2	0x0C48	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Skew Calibration Control Register2
DCPHY_M0_COMBO_SD0_DESKEW_CON3	0x0C4C	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Skew Calibration Control Register3
DCPHY_M0_COMBO_SD0_DESKEW_CON4	0x0C50	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Skew Calibration Control Register4
DCPHY_M0_COMBO_SD0_CRC_CON0	0x0C60	W	0x00000000	DC-PHY Combo Slave Data 0 Lane CRC Control Register0
DCPHY_M0_COMBO_SD0_CRC_CON1	0x0C64	W	0x00000000	DC-PHY Combo Slave Data 0 Lane CRC Control Register1
DCPHY_M0_COMBO_SD0_CRC_CON2	0x0C68	W	0x00000000	DC-PHY Combo Slave Data 0 Lane CRC Control Register2
DCPHY_M0_COMBO_SD1_GNR_CON0	0x0D00	W	0x00000000	DC-PHY Combo Slave Data 1 Lane General Control Register0
DCPHY_M0_COMBO_SD1_GNR_CON1	0x0D04	W	0x00000000	DC-PHY Combo Slave Data 1 Lane General Control Register1
DCPHY_M0_COMBO_SD1_ANA_CON0	0x0D08	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Analog Block Control Register0
DCPHY_M0_COMBO_SD1_ANA_CON1	0x0D0C	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Analog Block Control Register1
DCPHY_M0_COMBO_SD1_ANA_CON2	0x0D10	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Analog Block Control Register2
DCPHY_M0_COMBO_SD1_ANA_CON3	0x0D14	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Analog Block Control Register3
DCPHY_M0_COMBO_SD1_ANA_CON4	0x0D18	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Analog Block Control Register4
DCPHY_M0_COMBO_SD1_ANA_CON6	0x0D20	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Analog Block Control Register6
DCPHY_M0_COMBO_SD1_ANA_CON7	0x0D24	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Analog Block Control Register7
DCPHY_M0_COMBO_SD1_TIME_CON0	0x0D30	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Timing Control Register0
DCPHY_M0_COMBO_SD1_TIME_CON1	0x0D34	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Timing Control Register1
DCPHY_M0_COMBO_SD1_DATA_CON0	0x0D38	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Data Control Register0
DCPHY_M0_COMBO_SD1_DESKEW_CON0	0x0D40	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Skew Calibration Control Register0
DCPHY_M0_COMBO_SD1_DESKEW_CON1	0x0D44	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Skew Calibration Control Register1
DCPHY_M0_COMBO_SD1_DESKEW_CON2	0x0D48	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Skew Calibration Control Register2
DCPHY_M0_COMBO_SD1_DESKEW_CON3	0x0D4C	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Skew Calibration Control Register3

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Name	Offset	Size	Reset Value	Description
DCPHY_M0_COMBO_SD1_DESKEW_CON4	0x0D50	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Skew Calibration Control Register4
DCPHY_M0_COMBO_SD1_CRC_CON0	0x0D60	W	0x00000000	DC-PHY Combo Slave Data 1 Lane CRC Control Register0
DCPHY_M0_COMBO_SD1_CRC_CON1	0x0D64	W	0x00000000	DC-PHY Combo Slave Data 1 Lane CRC Control Register1
DCPHY_M0_COMBO_SD1_CRC_CON2	0x0D68	W	0x00000000	DC-PHY Combo Slave Data 1 Lane CRC Control Register2
DCPHY_M0_COMBO_SD2_GNR_CON0	0x0E00	W	0x00000000	DC-PHY Combo Slave Data 2 Lane General Control Register0
DCPHY_M0_COMBO_SD2_GNR_CON1	0x0E04	W	0x00000000	DC-PHY Combo Slave Data 2 Lane General Control Register1
DCPHY_M0_COMBO_SD2_ANA_CON0	0x0E08	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Analog Block Control Register0
DCPHY_M0_COMBO_SD2_ANA_CON1	0x0E0C	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Analog Block Control Register1
DCPHY_M0_COMBO_SD2_ANA_CON2	0x0E10	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Analog Block Control Register2
DCPHY_M0_COMBO_SD2_ANA_CON3	0x0E14	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Analog Block Control Register3
DCPHY_M0_COMBO_SD2_ANA_CON4	0x0E18	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Analog Block Control Register4
DCPHY_M0_COMBO_SD2_ANA_CON6	0x0E20	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Analog Block Control Register6
DCPHY_M0_COMBO_SD2_ANA_CON7	0x0E24	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Analog Block Control Register7
DCPHY_M0_COMBO_SD2_TIME_CON0	0x0E30	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Timing Control Register0
DCPHY_M0_COMBO_SD2_TIME_CON1	0x0E34	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Timing Control Register1
DCPHY_M0_COMBO_SD2_DATA_CON0	0x0E38	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Data Control Register0
DCPHY_M0_COMBO_SD2_DESKEW_CON0	0x0E40	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Skew Calibration Control Register0
DCPHY_M0_COMBO_SD2_DESKEW_CON1	0x0E44	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Skew Calibration Control Register1
DCPHY_M0_COMBO_SD2_DESKEW_CON2	0x0E48	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Skew Calibration Control Register2
DCPHY_M0_COMBO_SD2_DESKEW_CON3	0x0E4C	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Skew Calibration Control Register3
DCPHY_M0_COMBO_SD2_DESKEW_CON4	0x0E50	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Skew Calibration Control Register4
DCPHY_M0_COMBO_SD2_CRC_CON0	0x0E60	W	0x00000000	DC-PHY Combo Slave Data 2 Lane CRC Control Register0
DCPHY_M0_COMBO_SD2_CRC_CON1	0x0E64	W	0x00000000	DC-PHY Combo Slave Data 2 Lane CRC Control Register1
DCPHY_M0_COMBO_SD2_CRC_CON2	0x0E68	W	0x00000000	DC-PHY Combo Slave Data 2 Lane CRC Control Register2

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Name	Offset	Size	Reset Value	Description
DCPHY_M0_DPHY_SD3_GNR_CON0	0x0F00	W	0x00000000	D-PHY Slave Data 3 Lane General Control Register0
DCPHY_M0_DPHY_SD3_GNR_CON1	0x0F04	W	0x00000000	D-PHY Slave Data 3 Lane General Control Register1
DCPHY_M0_DPHY_SD3_ANA_CON0	0x0F08	W	0x00000000	D-PHY Slave Data 3 Lane Analog Block Control Register0
DCPHY_M0_DPHY_SD3_ANA_CON1	0x0F0C	W	0x00000000	D-PHY Slave Data 3 Lane Analog Block Control Register1
DCPHY_M0_DPHY_SD3_ANA_CON2	0x0F10	W	0x00000000	D-PHY Slave Data 3 Lane Analog Block Control Register2
DCPHY_M0_DPHY_SD3_ANA_CON3	0x0F14	W	0x00000000	D-PHY Slave Data 3 Lane Analog Block Control Register3
DCPHY_M0_DPHY_SD3_ANA_CON4	0x0F18	W	0x00000000	D-PHY Slave Data 3 Lane Analog Block Control Register4
DCPHY_M0_DPHY_SD3_ANA_CON5	0x0F1C	W	0x00000000	D-PHY Slave Data 3 Lane Analog Block Control Register5
DCPHY_M0_DPHY_SD3_TIME_CON0	0x0F30	W	0x00000000	D-PHY Slave Data 3 Lane Timing Control Register0
DCPHY_M0_DPHY_SD3_TIME_CON1	0x0F34	W	0x00000000	D-PHY Slave Data 3 Lane Timing Control Register1
DCPHY_M0_DPHY_SD3_DATA_CON0	0x0F38	W	0x00000000	D-PHY Slave Data 3 Lane Data Control Register0
DCPHY_M0_DPHY_SD3_DESKEW_CON0	0x0F40	W	0x00000000	D-PHY Slave Data 3 Lane Skew Calibration Control Register0
DCPHY_M0_DPHY_SD3_DESKEW_CON1	0x0F44	W	0x00000000	D-PHY Slave Data 3 Lane Skew Calibration Control Register1
DCPHY_M0_DPHY_SD3_DESKEW_CON2	0x0F48	W	0x00000000	D-PHY Slave Data 3 Lane Skew Calibration Control Register2
DCPHY_M0_DPHY_SD3_DESKEW_CON3	0x0F4C	W	0x00000000	D-PHY Slave Data 3 Lane Skew Calibration Control Register3
DCPHY_M0_DPHY_SD3_DESKEW_CON4	0x0F50	W	0x00000000	D-PHY Slave Data 3 Lane Skew Calibration Control Register4

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

21.4.3 Detail Registers Description

DCPHY_M0_BIAS_CON0

Address: Operational Base(0x2B020000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x1	I_RES_CNTL Bias current control 3'b000: 59.2uA 3'b001: 100.2uA 3'b010: 94.2uA 3'b011: 113.8uA 3'b100: 89.7uA 3'b101: 111.8uA 3'b110: 108.2uA 3'b111: 120.8uA
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	I_DIV_SEL BGR Chopper Clock Divider Control 2b'00: DIV 6 2b'01: DIV 12 2b'10: DIV 20 2b'11: DIV 40

DCPHY_M0_BIAS_CON1

Address: Operational Base(0x2B020000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x1	I_VBG_SEL BGR Reference Voltage 820mV Control 2b'00: vbg_780mV 2b'01: vbg_820mV 2b'10: vbg_860mV 2b'11: vbg_900mV
7:6	RO	0x0	reserved
5:4	RW	0x1	I_BGR_VREF_SEL Bias Reference Voltage 820mV Control 2b'00: S<0> 810mV 2b'01: S<1> 820mV 2b'10: S<2> 830mV 2b'11: S<3> 840mV
3	RO	0x0	reserved
2:0	RW	0x0	I_LADDER_SEL BGR Resistor Ladder Voltage Control 3'b000: 1V 3'b001: 0.96V 3'b010: 0.92V 3'b011: 0.88V 3'b100: 0.84V 3'b101: 0.8V 3'b110: 0.76V 3'b111: 0.72V

DCPHY_M0_BIAS_CON2

Address: Operational Base(0x2B020000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:12	RW	0x3	REG_325M Reference voltage-325mV for CD Function control pin 3'b000: 295mV 3'b001: 305mV 3'b010: 315mV 3'b011: 325mV 3'b100: 335mV 3'b101: 345mV 3'b110: 355mV 3'b111: 365mV
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x2	REG_LP_400M Reference voltage-400mV for LP_REG Function control pin 3'b000: 380mV 3'b001: 390mV 3'b010: 400mV 3'b011: 410mV 3'b100: 420mV 3'b101: 430mV 3'b110: 440mV 3'b111: 450mV
7	RO	0x0	reserved
6:4	RW	0x2	REG_400M Reference voltage-400mV/200mV for HS Function control pin, the left value is selected when I_MUX_SEL is set to 0x0 and the right value is selected when I_MUX_SEL is set to 0x1. 3'b000: 380mV / 230mV 3'b001: 390mV / 220mV 3'b010: 400mV / 210mV 3'b011: 410mV / 200mV 3'b100: 420mV / 190mV 3'b101: 430mV / 180mV 3'b110: 440mV / 170mV 3'b111: 450mV / 160mV
3	RO	0x0	reserved
2:0	RW	0x3	REG_645M Reference voltage-645mV for LP Function control pin 3'b000: 605mV 3'b001: 625mV 3'b010: 635mV 3'b011: 645mV 3'b100: 655mV 3'b101: 665mV 3'b110: 685mV 3'b111: 725mV

DCPHY_M0_BIAS_CON4

Address: Operational Base(0x2B020000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RW	0x0	I_MUX_SEL Output Voltage(400mV/200mV/530mV) selction pin 2b'00 : 400mV 2b'01 : 200mV 2b'10 : 530mV 2b'11 : 530mV D-PHY: 2'b00 C-PHY: 2'b10
4:0	RO	0x00	reserved

DCPHY_M0_PLL_CON0

Address: Operational Base(0x2B020000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	PLL_EN PLL Control Logic Block Enable Register. For use PLL in PHY module, user can set this register after setting registers.
11	RO	0x0	reserved
10:8	RW	0x0	S Register for Division Value of the 3-bit Programmable Scaler.
7:6	RO	0x0	reserved
5:0	RW	0x00	P Register for Division Value of the 6-bit Programmable Pre-Divider. PLL has to be reset if P value is changed.

DCPHY_M0_PLL_CON1

Address: Operational Base(0x2B020000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	K Value of 16-bit DSM.

DCPHY_M0_PLL_CON2

Address: Operational Base(0x2B020000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	USE_SDW_REG Shadow Register Enable Register. For using frequency hopping function in PHY, user can set this register before controlling the interface signal PLL_CFG_UPDT.
14	RW	0x0	M_ESCREF_EN M_ESCREF Output Enable Register. When user wants to measure the Escape Clock of Master Lanes, set this register.
13	RW	0x0	FOUT_MASK Register for Scaler's Re-initialization Time Control Pin. Default value is 1'b0.
12	RW	0x0	FEED_EN Register for Monitoring Pin. If FEED_EN is 1, FEED_OUT is enabled. Default value is 1'b0.
11:10	RO	0x0	reserved
9:0	RW	0x000	M Register for Division Value of the 10-bit Programmable Main-Divider. PLL has to be reset if M value is changed.

DCPHY_M0_PLL_CON3

Address: Operational Base(0x2B020000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x00	MRR Register for Value of 6-bit Modulation Rate Control. PLL has to be reset if MRR is changed.
7:0	RW	0x00	MFR Register for Value of 8-bit Modulation Frequency Control. PLL has to be reset if MFR is changed.

DCPHY_M0_PLL_CON4

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Address: Operational Base(0x2B020000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	SSCG_EN Register for Enable Pin for Dithered Mode(Active-high).
10	RW	0x0	FSEL Register for Monitoring Pin. If FSEL is 0, FEED_OUT is FREF If FSEL is 1, FEED_OUT is FEED Default value is 1'b0.
9	RW	0x0	BYPASS Register for Bypass Function of PLL. If BYPASS is 1, bypass mode is enabled. (FOUT: FIN) If BYPASS is 0, PLL operates normally.
8	RW	0x0	AFC_ENB Register for Monitoring Pin. If AFC_ENB is 0, AFC is enabled and VCO is calibrated automatically. If AFC_ENB is 1, AFC is disabled and VCO is calibrated manually by EXTAFC[4:0] for the test of VCO range. Default value is 1'b0.
7:5	RO	0x0	reserved
4:0	RW	0x00	EXTAFC Register for Monitoring Pin. If AFC_ENB is 1, AFC is disabled and VCO is calibrated manually by EXTAFC[4:0] for the test of VCO range. Default value is 5'b0_0000.

DCPHY_M0_PLL_CON5

Address: Operational Base(0x2B020000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	CLK_BUFF_EN_SEL Clock Buffering Enable Selection Register. 1'b0: Clock buffering is enabled when PLL_EN is set. 1'b1: Clock buffering is enabled when ENABLE(M%_DPHY_M#C_GNR_CON0) is set.
14	RW	0x0	F_OUT_EN PLL Output to External Module Enable Control Register. For sharing PLL signals of this module with other module, user can set this register before enabling the PLL.
13	RW	0x0	CAL_SEL_CK Clock I-Q Phase Change Control Register. 1'b0: Use Q Phase. 1'b1: Use I Phase. (Changed)
12	RW	0x0	CAL_SEL_DATA Data I-Q Phase Change Control Register. 1'b0: Use I Phase. 1'b1: Use Q Phase. (Changed)
11	RW	0x0	SEL_EXTCLK PLL of External Module Enable Register. For using shared clock and clock signals by PLL of external module, user can set this register without enabling the PLL in this module. 1'b0: Use Internal PLL. (Default) 1'b1: Use External PLL.

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Bit	Attr	Reset Value	Description
10	RW	0x0	RESET_N_SEL Clock Divider Reset Selection Register. 1'b0: Release clock divider reset when PLL_EN is set. 1'b1: Release clock divider reset when ENABLE(M%_DPHY_M#C_GNR_CON0) is set.
9	RW	0x0	MS_ENABLECLK_SEL PLL Buffering Enable Selection Register. 1'b0: PLL buffering is enabled when ENABLE(M%_DPHY_M#C_GNR_CON0) is set. 1'b1: PLL buffering is enabled when ENABLE(M%_DPHY_S#C_GNR_CON0) is set.
8	RW	0x0	PLL_ENABLE_SEL PLL Buffering Enable Selection Register. 1'b0: PLL buffering is enabled when PLL_EN is set. 1'b1: PLL buffering is enabled when ENABLE(M%_DPHY_M#C_GNR_CON0) is set.
7:6	RO	0x0	reserved
5:4	RW	0x0	ICP Register for Controls the Charge-Pump Current. Default value: 2'b00
3:2	RO	0x0	reserved
1:0	RW	0x0	SEL_PF Register for Value of 2-bit Modulation Method Control. 00: Down spread 01: Up spread 1x: Center spread. PLL has to be reset if SEL_PF is changed.

DCPHY_M0_PLL_CON6

Address: Operational Base(0x2B020000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	CLK_BUFF_EN_SEL Clock Gating Disable Control Register. 1'b0: Clock gating function is available. 1'b1: Clock gating function is not available when PLL_WCLK_EN is asserted.
11:8	RW	0x0	WCLK_BUF_SFT_CNT Word Clock Buffer Shift Count Control Register. Please set this register as below. Roundup((Word Clock Period) / 38.46 + 2)
7	RW	0x0	PLL_TEST_DIV_EN PLL Test Divider Enable Control Register. For measuring frequency in ATE test environment, user can set this register and measure the divided clock frequency at the port "PLL_TEST_DIV_TM."
6	RW	0x0	D2A_CLK_BUF_EN_SEL D2A_CLK_BUF_EN Enable Selection Register. 1'b0: D2A_CLK_BUF_EN 1'b1: ENABLE(M%_DPHY_M#C_GNR_CON0)
5	RW	0x0	INTERNAL_LOOPBACK_EN Internal Loopback Test Enable Register. 1'b1: Internal Loopback Test

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Bit	Attr	Reset Value	Description
4	RW	0x0	M_RESETN_IQ_SEL M_RESETN Phase Control Register. 1'b0: I Phase 1'b1: Q Phase
3	RW	0x0	BITCLKDIV2_OUT_ENB Bit Clock /2 Divider Output Enable Control Register. 1'b0: Enable 1'b1: Disable
2	RW	0x0	BITCLKDIV4_OUT_ENB Bit Clock /4 Divider Output Enable Control Register. 1'b0: Enable 1'b1: Disable
1	RW	0x0	BITCLKDIV8_OUT_ENB Bit Clock /8 Divider Output Enable Control Register. 1'b0: Enable 1'b1: Disable
0	RW	0x0	BGR_REF_CLK_EN BGR_REF_CLK Output Enable Control Register. 1'b0: Disable 1'b1: Enable

DCPHY_M0_PLL_CON7

Address: Operational Base(0x2B020000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PLL_LOCK_CNT PLL Lock Timing Control Register. This reigster is the count value of PLL lock indication. When set the PLL_EN register, PHY lock counter starts to count. And when count value reaches to the value of this register, PLL_LOCK(M%_PLL_STAT0[0]) is set to HIGH. Generally, 200us is needed for locking the PLL.

DCPHY_M0_PLL_CON8

Address: Operational Base(0x2B020000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PLL_STB_CNT PLL Stabilization Timing Control Register. This register is the count value of PLL stablization is done. When the signal PLL_CFG_UPDT is asserted for frequency hopping function, PHY stabilizing counter starts to count. And when count value reaches to the value of this register, the signal PLL_CFG_READY is set to HIGH. Generally, 100us is needed for stablizing PLL in frequency hopping.

DCPHY_M0_PLL_STAT0

Address: Operational Base(0x2B020000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RO	0x0	PLL_LOCK PLL Lock Indicate Register. This register is set when output clock of PLL is locked and ready to operate after setting PLL_EN. User can control setting timing of this register using PLL_LOCK_CNT(M0_PLL_CON7[15:0]) register. And user can control ENABLE register of each Lanes after PLL_LOCK is set.

DCPHY_M0_DPHY_MC_GNR_CON0

Address: Operational Base(0x2B020000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(DPHY_M#C_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_DPHY_MC_GNR_CON1

Address: Operational Base(0x2B020000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(DPHY_M#C_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_DPHY_MC_ANA_CON0

Address: Operational Base(0x2B020000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:12	RW	0x7	EDGE_CON Cap Peaking Control Register. Set the register as below. In case of D-PHY, 3'b111 In case of C-PHY, 3'b001
11:10	RO	0x0	reserved
9	RW	0x0	EDGE_CON_DIR Cap Peaking Direction Control Register. Set the register as below. In case of D-PHY, 1'b0 In case of C-PHY, 1'b1
8	RW	0x1	EDGE_CON_EN Cap Peaking Enable Register.

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Bit	Attr	Reset Value	Description
7:4	RW	0x3	RES_UP High-Speed Driver Up Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm
3:0	RW	0x3	RES_DN High-Speed Driver Down Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm

DCPHY_M0_DPHY_MC_ANA_CON1

Address: Operational Base(0x2B020000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	IQ_RESETN_POL_CON I-Q Clock Polarity Control Register.
14	RW	0x0	VREG12_VALID 1.2V Voltage Regulator Valid Control Register.
13	RW	0x0	VREG12_VALID_SEL 1.2V Voltage Regulator Valid Select Register.
12	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.
11	RW	0x0	ATB_SEL_GND Analog Test Bus Select for SER Ground Register.
10	RW	0x0	ATB_SEL_VDD Analog Test Bus Select for SER Power Register.

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	LPTX_SR_UP Low-Power TX Driver Slew Rate Up Enable Register. Releated with LPTX_SR_CTRL Register. 2b'1X : Max slew rate 2b'0X : Default
7:6	RO	0x0	reserved
5:4	RW	0x0	LPTX_SR_CTRL Low-Power TX Driver Slew Rate Control Register. When LPTX_SR_UP is 2b'0X, 2b'00 : Default 2b'01 or 2b'10 : Decrease slew rate by 1% 2b'11 : Decrease slew rate by 2%
3:2	RO	0x0	reserved
1:0	RW	0x0	EMP De-Emphasis Control Register. In case of D-PHY: Data Rate >=4.5Gbps: 2'b01 Data Rate < 4.5Gbps: 2'b00 2'b00: 0 dB 2'b01: -1.5 dB 2'b10: -3.5 dB 2'b11: -6.5 dB In case of C-PHY, Data Rate <= 2Gsps 2'b00: 0dB 2'b01: NA 2'b10: NA 2'b11: NA

DCPHY_M0_DPHY_MC_ANA_CON2

Address: Operational Base(0x2B020000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	HS_VREG_AMP_ICON High Speed Voltage Regulator Current Control Register 2'b00 : Clock hstx enable HS VREG after lp sequence 2'b10 : Clock bias enable HS VREG after lane enable

DCPHY_M0_DPHY_MC_ANA_CON3

Address: Operational Base(0x2B020000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	HIZ_EN Master dn/dp differential output floating mode enable register when hs_tx disable. 1b'0 = normal mode 1b'1 = hi-z mode
14:0	RO	0x0000	reserved

DCPHY_M0_DPHY_MC_TIME_CON0

Address: Operational Base(0x2B020000) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	HSTX_CLK_SEL HS-TX State Machine Clock Select Register. HS-TX Clock is used for counting some of timing speicfications. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
11:4	RW	0x00	T_LPX TLPX Timing Counter Register. This count value is specially used in High-Speed Transmit operation
3:0	RO	0x0	reserved

DCPHY_M0_DPHY_MC_TIME_CON1

Address: Operational Base(0x2B020000) + offset (0x0334)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_CLK_ZERO TCLK-ZERO Timing Counter Register. This count value is used in High-Speed Transmit operation.
7:0	RW	0x00	T_CLK_PREPARE TCLK-PREPARE Timing Counter Register. This count value is used in High-Speed Transmit operation.

DCPHY_M0_DPHY_MC_TIME_CON2

Address: Operational Base(0x2B020000) + offset (0x0338)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_EXIT THS-EXIT Timing Counter Register. This count value is used in High-Speed Transmit operation.
7:0	RW	0x00	T_CLK_TRAIL TCLK-TRAIL Timing Counter Register. This count value is used in High-Speed Transmit operation.

DCPHY_M0_DPHY_MC_TIME_CON3

Address: Operational Base(0x2B020000) + offset (0x033C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	T_CLK_POST TCLK-POST Timing Counter Register. This count value is used in High-Speed Transmit operation.

DCPHY_M0_DPHY_MC_TIME_CON4

Address: Operational Base(0x2B020000) + offset (0x0340)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	T_ULPS_EXIT Ultra-Low Power Exit Timing Counter Register. This count value is used in Ultra-Low Power operation. For exiting Ultra-Low Power State, the Link layer can set PPI signal "TXULPSEXIT" to HIGH. There are two conditions for moving the state of PHY to "TX-ULPS-Exit." One is that the Link layer control PPI signal "TXULPSCLK" to LOW. Another way is to use the counter in PHY.

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DCPHY_M0_DPHY_MC_DATA_CON0

Address: Operational Base(0x2B020000) + offset (0x0344)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	CLK_INV Clock Inversion Control Register. When this register is set to HIGH, the clock output of DP/DN will be inverted.
0	RO	0x0	reserved

DCPHY_M0_DPHY_MC_DESKEW_CON0

Address: Operational Base(0x2B020000) + offset (0x0350)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	SKEW_CAL_RUN_TIME Periodic Skew Calibration Running Time Control Register. This count value is used in Periodic Skew Calibration. If this register is set to 0, the Periodic Skew Calibration running time is same as when set this register to 4'h4.
11:8	RW	0x0	SKEW_CAL_INIT_RUN_TIME Initial Skew Calibration Running Time Control Register. This count value is used in Initial Skew Calibration. If this register is set to 0, the Initial Skew Calibration running time is same as when set this register to 4'h7.
7:4	RW	0x0	SKEW_CAL_INIT_WAIT_TIME Initial Skew Calibration Waiting Time Control Register. This count value is used in Initial Skew Calibration. After power-on sequence, count will be started. If this register is set to 0, the Initial Skew Calibration is not goint to work.
3:1	RO	0x0	reserved
0	RW	0x0	SKEW_CAL_EN Skew Calibration Enable Register. This register enables Skew Calibration logic and circuits. For using Skew Calibration function through PPI "TXSKEWCALHS," set this register before enabling the lanes. If the operating data rate is 1.5Gbps or above, the Skew Calibration is madatory function.

DCPHY_M0_COMBO_MD0_GNR_CON0

Address: Operational Base(0x2B020000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(COMBO_M#D#_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_COMBO_MD0_GNR_CON1

Address: Operational Base(0x2B020000) + offset (0x0404)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(COMBO_M#D#_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_COMBO_MD0_ANA_CON0

Address: Operational Base(0x2B020000) + offset (0x0408)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:12	RW	0x7	EDGE_CON Cap Peaking Control Register. Set the register as below. In case of D-PHY, 3'b111 In case of C-PHY, 3'b001
11:10	RO	0x0	reserved
9	RW	0x0	EDGE_CON_DIR Cap Peaking Direction Control Register. Set the register as below. In case of D-PHY, 1'b0 In case of C-PHY, 1'b1
8	RW	0x1	EDGE_CON_EN Cap Peaking Enable Register.
7:4	RW	0x3	RES_UP High-Speed Driver Up Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm

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Bit	Attr	Reset Value	Description
3:0	RW	0x3	RES_DN High-Speed Driver Down Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm

DCPHY_M0_COMBO_MD0_ANA_CON1

Address: Operational Base(0x2B020000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	IQ_RESETN_POL_CON I-Q Clock Polarity Control Register.
14	RW	0x0	VREG12_VALID 1.2V Voltage Regulator Valid Control Register.
13	RW	0x0	VREG12_VALID_SEL 1.2V Voltage Regulator Valid Select Register.
12	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.
11	RW	0x0	ATB_SEL_GND Analog Test Bus Select for SER Ground Register.
10	RW	0x0	ATB_SEL_VDD Analog Test Bus Select for SER Power Register.
9:8	RW	0x0	LPTX_SR_UP Low-Power TX Driver Slew Rate Up Enable Register. Related with LPTX_SR_CTRL Register. 2b'1X : Max slew rate 2b'0X : Default
7:6	RO	0x0	reserved
5:4	RW	0x0	LPTX_SR_CTRL Low-Power TX Driver Slew Rate Control Register. When LPTX_SR_UP is 2b'0X, 2b'00: Default 2b'01 or 2b'10: Decrease slew rate by 1% 2b'11: Decrease slew rate by 2%
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	EMP De-Emphasis Control Register. In case of D-PHY: Data Rate >=4.5Gbps: 2'b01 Data Rate < 4.5Gbps: 2'b00 2'b00: 0 dB 2'b01: -1.5 dB 2'b10: -3.5 dB 2'b11: -6.5 dB In case of C-PHY, Data Rate <= 2Gsps 2'b00: 0dB 2'b01: NA 2'b10: NA 2'b11: NA

DCPHY_M0_COMBO_MD0_ANA_CON2

Address: Operational Base(0x2B020000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	LPRX_HYS_SEL Low-Power RX Hysterisis Select Register.
11	RO	0x0	reserved
10:8	RW	0x0	DTB_SEL Digital Test Bus Select Register.
7	RW	0x0	CNT_REJECTION_PULSE Pulse Rejection Control Register.
6	RW	0x0	SEL_ESCPOL Escape Mode Clock Polarity Select Register.
5	RW	0x0	SEL_VREF Reference Voltage Select Register.
4	RW	0x0	CNT_ULPSHYS ULPS Hysterisis Control Register.
3	RW	0x0	EN_RSTN_SEL Reset Enable Select Register.
2	RW	0x0	PULSE_REJ_ENB Pulse Rejection Enable Register.
1	RW	0x0	LPCD_HYS_SEL Low-Power Contention Detect Hysterisis Select Register.
0	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.

DCPHY_M0_COMBO_MD0_TIME_CON0

Address: Operational Base(0x2B020000) + offset (0x0430)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	HSTX_CLK_SEL HS-TX State Machine Clock Select Register. HS-TX Clock is used for counting some of timing specifications. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.

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Bit	Attr	Reset Value	Description
11:4	RW	0x00	T_LPX TLPX Timing Counter Register. This count value is specially used in High-Speed Transmit operation
3:2	RW	0x0	T_LP_EXIT_SKEW High-Speed Data Transmission End-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the End-of-Transmission procedure of High-Speed Data Transmission.
1:0	RW	0x0	T_LP_ENTRY_SKEW High-Speed Data Transmission Start-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the Start-of-Transmission procedure of High-Speed Data Transmission.

DCPHY_M0_COMBO_MD0_TIME_CON1

Address: Operational Base(0x2B020000) + offset (0x0434)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_ZERO THS-ZERO (D-PHY) / T3-PREBEGIN (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.
7:0	RW	0x00	T_HS_PREPARE THS-PREPARE (D-PHY) / T3-PREPARE (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance..

DCPHY_M0_COMBO_MD0_TIME_CON2

Address: Operational Base(0x2B020000) + offset (0x0438)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_EXIT THS-EXIT Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.
7:0	RW	0x00	T_HS_TRAIL THS-TRAIL (D-PHY) / T3-POST (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.

DCPHY_M0_COMBO_MD0_TIME_CON3

Address: Operational Base(0x2B020000) + offset (0x043C)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	T_TA_GET TTA-GET Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.
3:0	RW	0x0	T_TA_GO TTA-GO Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.

DCPHY_M0_COMBO_MD0_TIME_CON4

Address: Operational Base(0x2B020000) + offset (0x0440)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	T_ULPS_EXIT Ultra-Low Power Exit Timing Counter Register. This count value is used in Ultra-Low Power operation. For exiting Ultra-Low Power State, the Link layer can set PPI signal "TXULPSEXIT" to HIGH. There are two conditions for moving the state of PHY to "TX-ULPS-Exit." One is that the Link layer control PPI signal "TXULPSCLK" to LOW. Another way is to use the counter in PHY.

DCPHY_M0_COMBO_MD0_DATA_CON0

Address: Operational Base(0x2B020000) + offset (0x0444)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	ERR_CONTENTION_DISABLE Contention Error Detect Disable Control Register. When this register is set to HIGH, the contention error will not occur through "ERRCONTENTIONLP0/1."
11:9	RO	0x0	reserved
8	RW	0x0	TRIG_EXIT_CLK_EN Trigger Mode Exit Clock Toggle Enable Register. When this register is set to HIGH, after transmitting the trigger command, DP signal is toggled as period of Escape mode clock until "TXREQUESTESC" goes to LOW.
7:6	RO	0x0	reserved
5	RW	0x0	LPTX_SWAP Low-Power Signal Swap Control Register. This register is only valid in C-PHY mode. When this register is set to HIGH, the Low-Power signal output A/C will be swapped.
4	RW	0x0	SYMBOL_SWAP Symbol Swap Control Register. When this register is set to HIGH, 7-symbol input will be swapped.
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	CLK_INV Clock Inversion Control Register. When this register is set to HIGH, the clock output of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data input will be swapped.

DCPHY_M0_COMBO_MD0_PRGSEQ_CON0

Address: Operational Base(0x2B020000) + offset (0x0460)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	PROG_SEQ_EN Programmable Sequence Enable Register. When this register is set to HIGH, Programmable Sequence of the Preamble is used as setting value in PROG_SEQ{COMBO_M#D#_PRGSEQ_CON1[9:0], COMBO_M#D#_PRGSEQ_CON2[15:0], COMBO_M#D#_PRGSEQ_CON3[15:0]}.

DCPHY_M0_COMBO_MD0_PRGSEQ_CON1

Address: Operational Base(0x2B020000) + offset (0x0464)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD0_PRGSEQ_CON2

Address: Operational Base(0x2B020000) + offset (0x0468)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD0_PRGSEQ_CON3

Address: Operational Base(0x2B020000) + offset (0x046C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD1_GNR_CON0

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Address: Operational Base(0x2B020000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(COMBO_M#D#_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_COMBO_MD1_GNR_CON1

Address: Operational Base(0x2B020000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(COMBO_M#D#_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_COMBO_MD1_ANA_CON0

Address: Operational Base(0x2B020000) + offset (0x0508)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:12	RW	0x7	EDGE_CON Cap Peaking Control Register. Set the register as below. In case of D-PHY, 3'b111 In case of C-PHY, 3'b001
11:10	RO	0x0	reserved
9	RW	0x0	EDGE_CON_DIR Cap Peaking Direction Control Register. Set the register as below. In case of D-PHY,1'b0 In case of C-PHY,1'b1
8	RW	0x1	EDGE_CON_EN Cap Peaking Enable Register.

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Bit	Attr	Reset Value	Description
7:4	RW	0x3	RES_UP High-Speed Driver Up Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm
3:0	RW	0x3	RES_DN High-Speed Driver Down Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm

DCPHY_M0_COMBO_MD1_ANA_CON1

Address: Operational Base(0x2B020000) + offset (0x050C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	IQ_RESETN_POL_CON I-Q Clock Polarity Control Register.
14	RW	0x0	VREG12_VALID 1.2V Voltage Regulator Valid Control Register.
13	RW	0x0	VREG12_VALID_SEL 1.2V Voltage Regulator Valid Select Register.
12	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.
11	RW	0x0	ATB_SEL_GND Analog Test Bus Select for SER Ground Register.
10	RW	0x0	ATB_SEL_VDD Analog Test Bus Select for SER Power Register.

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	LPTX_SR_UP Low-Power TX Driver Slew Rate Up Enable Register. Related with LPTX_SR_CTRL Register. 2b'1X : Max slew rate 2b'0X : Default
7:6	RO	0x0	reserved
5:4	RW	0x0	LPTX_SR_CTRL Low-Power TX Driver Slew Rate Control Register. When LPTX_SR_UP is 2b'0X, 2b'00 : Default 2b'01 or 2b'10 : Decrease slew rate by 1% 2b'11 : Decrease slew rate by 2%
3:2	RO	0x0	reserved
1:0	RW	0x0	EMP De-Emphasis Control Register. In case of D-PHY: Data Rate >=4.5Gbps: 2'b01 Data Rate < 4.5Gbps: 2'b00 2'b00: 0 dB 2'b01: -1.5 dB 2'b10: -3.5 dB 2'b11: -6.5 dB In case of C-PHY, Data Rate <= 2Gsps 2'b00: 0dB 2'b01: NA 2'b10: NA 2'b11: NA

DCPHY_M0_COMBO_MD1_ANA_CON2

Address: Operational Base(0x2B020000) + offset (0x0510)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	LPRX_HYS_SEL Low-Power RX Hysterisis Select Register.
11	RO	0x0	reserved
10:8	RW	0x0	DTB_SEL Digital Test Bus Select Register.
7	RW	0x0	CNT_REJECTION_PULSE Pulse Rejection Control Register.
6	RW	0x0	SEL_ESCPOL Escape Mode Clock Polarity Select Register.
5	RW	0x0	SEL_VREF Reference Voltage Select Register.
4	RW	0x0	CNT_ULPSHYS ULPS Hysterisis Control Register.
3	RW	0x0	EN_RSTN_SEL Reset Enable Select Register.
2	RW	0x0	PULSE_REJ_ENB Pulse Rejection Enable Register.
1	RW	0x0	LPCD_HYS_SEL Low-Power Contention Detect Hysterisis Select Register.
0	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.

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DCPHY_M0_COMBO_MD1_TIME_CON0

Address: Operational Base(0x2B020000) + offset (0x0530)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	HSTX_CLK_SEL HS-TX State Machine Clock Select Register. HS-TX Clock is used for counting some of timing specifications. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
11:4	RW	0x00	T_LPX TLPX Timing Counter Register. This count value is specially used in High-Speed Transmit operation
3:2	RW	0x0	T_LP_EXIT_SKEW High-Speed Data Transmission End-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the End-of-Transmission procedure of High-Speed Data Transmission.
1:0	RW	0x0	T_LP_ENTRY_SKEW High-Speed Data Transmission Start-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the Start-of-Transmission procedure of High-Speed Data Transmission.

DCPHY_M0_COMBO_MD1_TIME_CON1

Address: Operational Base(0x2B020000) + offset (0x0534)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_ZERO THS-ZERO (D-PHY) / T3-PREBEGIN (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.
7:0	RW	0x00	T_HS_PREPARE THS-PREPARE (D-PHY) / T3-PREPARE (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance..

DCPHY_M0_COMBO_MD1_TIME_CON2

Address: Operational Base(0x2B020000) + offset (0x0538)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	T_HS_EXIT THS-EXIT Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.
7:0	RW	0x00	T_HS_TRAIL THS-TRAIL (D-PHY) / T3-POST (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.

DCPHY_M0_COMBO_MD1_TIME_CON3

Address: Operational Base(0x2B020000) + offset (0x053C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	T_TA_GET TTA-GET Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.
3:0	RW	0x0	T_TA_GO TTA-GO Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.

DCPHY_M0_COMBO_MD1_TIME_CON4

Address: Operational Base(0x2B020000) + offset (0x0540)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	T_ULPS_EXIT Ultra-Low Power Exit Timing Counter Register. This count value is used in Ultra-Low Power operation. For exiting Ultra-Low Power State, the Link layer can set PPI signal "TXULPSEXIT" to HIGH. There are two conditions for moving the state of PHY to "TX-ULPS-Exit." One is that the Link layer control PPI signal "TXULPSCLK" to LOW. Another way is to use the counter in PHY.

DCPHY_M0_COMBO_MD1_DATA_CON0

Address: Operational Base(0x2B020000) + offset (0x0544)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	ERR_CONTENTION_DISABLE Contention Error Detect Disable Control Register. When this register is set to HIGH, the contention error will not occur through "ERRCONTENTIONLP0/1."
11:9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	TRIG_EXIT_CLK_EN Trigger Mode Exit Clock Toggle Enable Register. When this register is set to HIGH, after transmitting the trigger command, DP signal is toggled as period of Escape mode clock until "TXREQUESTESC" goes to LOW.
7:6	RO	0x0	reserved
5	RW	0x0	LPTX_SWAP Low-Power Signal Swap Control Register. This register is only valid in C-PHY mode. When this register is set to HIGH, the Low-Power signal output A/C will be swapped.
4	RW	0x0	SYMBOL_SWAP Symbol Swap Control Register. When this register is set to HIGH, 7-symbol input will be swapped.
3:2	RO	0x0	reserved
1	RW	0x0	CLK_INV Clock Inversion Control Register. When this register is set to HIGH, the clock output of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data input will be swapped.

DCPHY_M0_COMBO_MD1_PRGSEQ_CON0

Address: Operational Base(0x2B020000) + offset (0x0560)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	PROG_SEQ_EN Programmable Sequence Enable Register. When this register is set to HIGH, Programmable Sequence of the Preamble is used as setting value in PROG_SEQ{COMBO_M#D#_PRGSEQ_CON1[9:0], COMBO_M#D#_PRGSEQ_CON2[15:0], COMBO_M#D#_PRGSEQ_CON3[15:0]}.

DCPHY_M0_COMBO_MD1_PRGSEQ_CON1

Address: Operational Base(0x2B020000) + offset (0x0564)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD1_PRGSEQ_CON2

Address: Operational Base(0x2B020000) + offset (0x0568)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD1_PRGSEQ_CON3

Address: Operational Base(0x2B020000) + offset (0x056C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD2_GNR_CON0

Address: Operational Base(0x2B020000) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(COMBO_M#D#_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_COMBO_MD2_GNR_CON1

Address: Operational Base(0x2B020000) + offset (0x0604)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(COMBO_M#D#_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_COMBO_MD2_ANA_CON0

Address: Operational Base(0x2B020000) + offset (0x0608)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:12	RW	0x7	EDGE_CON Cap Peaking Control Register. Set the register as below. In case of D-PHY, 3'b111 In case of C-PHY, 3'b001

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Bit	Attr	Reset Value	Description
11:10	RO	0x0	reserved
9	RW	0x0	EDGE_CON_DIR Cap Peaking Direction Control Register. Set the register as below. In case of D-PHY,1'b0 In case of C-PHY,1'b1
8	RW	0x1	EDGE_CON_EN Cap Peaking Enable Register.
7:4	RW	0x3	RES_UP High-Speed Driver Up Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm
3:0	RW	0x3	RES_DN High-Speed Driver Down Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm

DCPHY_M0_COMBO_MD2_ANA_CON1

Address: Operational Base(0x2B020000) + offset (0x060C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	IQ_RESETN_POL_CON I-Q Clock Polarity Control Register.
14	RW	0x0	VREG12_VALID 1.2V Voltage Regulator Valid Control Register.
13	RW	0x0	VREG12_VALID_SEL 1.2V Voltage Regulator Valid Select Register.

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Bit	Attr	Reset Value	Description
12	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.
11	RO	0x0	ATB_SEL_GND Analog Test Bus Select for SER Ground Register.
10	RW	0x0	ATB_SEL_VDD Analog Test Bus Select for SER Power Register.
9:8	RW	0x0	LPTX_SR_UP Low-Power TX Driver Slew Rate Up Enable Register. Related with LPTX_SR_CTRL Register. 2b'1X: Max slew rate 2b'0X: Default
7:6	RO	0x0	reserved
5:4	RW	0x0	LPTX_SR_CTRL Low-Power TX Driver Slew Rate Control Register. When LPTX_SR_UP is 2b'0X, 2b'00: Default 2b'01 or 2b'10: Decrease slew rate by 1% 2b'11: Decrease slew rate by 2%
3:2	RO	0x0	reserved
1:0	RW	0x0	EMP De-Emphasis Control Register. In case of D-PHY: Data Rate >=4.5Gbps: 2'b01 Data Rate < 4.5Gbps: 2'b00 2'b00: 0 dB 2'b01: -1.5 dB 2'b10: -3.5 dB 2'b11: -6.5 dB In case of C-PHY, Data Rate <= 2Gsps 2'b00: 0dB 2'b01: NA 2'b10: NA 2'b11: NA

DCPHY_M0_COMBO_MD2_ANA_CON2

Address: Operational Base(0x2B020000) + offset (0x0610)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	LPRX_HYS_SEL Low-Power RX Hysterisis Select Register.
11	RO	0x0	reserved
10:8	RW	0x0	DTB_SEL Digital Test Bus Select Register.
7	RW	0x0	CNT_REJECTION_PULSE Pulse Rejection Control Register.
6	RW	0x0	SEL_ESCPOL Escape Mode Clock Polarity Select Register.
5	RW	0x0	SEL_VREF Reference Voltage Select Register.
4	RW	0x0	CNT_ULPSHYS ULPS Hysterisis Control Register.
3	RW	0x0	EN_RSTN_SEL Reset Enable Select Register.

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Bit	Attr	Reset Value	Description
2	RW	0x0	PULSE_REJ_ENB Pulse Rejection Enable Register.
1	RW	0x0	LPCD_HYS_SEL Low-Power Contention Detect Hysterisis Select Register.
0	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.

DCPHY_M0_COMBO_MD2_TIME_CON0

Address: Operational Base(0x2B020000) + offset (0x0630)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	HSTX_CLK_SEL HS-TX State Machine Clock Select Register. HS-TX Clock is used for counting some of timing speicfications. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
11:4	RW	0x00	T_LPX TLPX Timing Counter Register. This count value is specially used in High-Speed Transmit operation
3:2	RW	0x0	T_LP_EXIT_SKEW High-Speed Data Transmission End-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the End-of-Transmission procedure of High-Speed Data Transmission.
1:0	RW	0x0	T_LP_ENTRY_SKEW High-Speed Data Transmission Start-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the Start-of-Transmission procedure of High-Speed Data Transmission.

DCPHY_M0_COMBO_MD2_TIME_CON1

Address: Operational Base(0x2B020000) + offset (0x0634)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_ZERO THS-ZERO (D-PHY) / T3-PREBEGIN (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.
7:0	RW	0x00	T_HS_PREPARE THS-PREPARE (D-PHY) / T3-PREPARE (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance..

DCPHY_M0_COMBO_MD2_TIME_CON2

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Address: Operational Base(0x2B020000) + offset (0x0638)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_EXIT THS-EXIT Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.
7:0	RW	0x00	T_HS_TRAIL THS-TRAIL (D-PHY) / T3-POST (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.

DCPHY_M0_COMBO_MD2_TIME_CON3

Address: Operational Base(0x2B020000) + offset (0x063C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	T_TA_GET TTA-GET Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.
3:0	RW	0x0	T_TA_GO TTA-GO Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.

DCPHY_M0_COMBO_MD2_TIME_CON4

Address: Operational Base(0x2B020000) + offset (0x0640)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	T_ULPS_EXIT Ultra-Low Power Exit Timing Counter Register. This count value is used in Ultra-Low Power operation. For exiting Ultra-Low Power State, the Link layer can set PPI signal "TXULPSEXIT" to HIGH. There are two conditions for moving the state of PHY to "TX-ULPS-Exit." One is that the Link layer control PPI signal "TXULPSCLK" to LOW. Another way is to use the counter in PHY.

DCPHY_M0_COMBO_MD2_DATA_CON0

Address: Operational Base(0x2B020000) + offset (0x0644)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	ERR_CONTENTION_DISABLE Contention Error Detect Disable Control Register. When this register is set to HIGH, the contention error will not occur through "ERRCONTENTIONLP0/1."
11:9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	TRIG_EXIT_CLK_EN Trigger Mode Exit Clock Toggle Enable Register. When this register is set to HIGH, after transmitting the trigger command, DP signal is toggled as period of Escape mode clock until "TXREQUESTESC" goes to LOW.
7:6	RO	0x0	reserved
5	RW	0x0	LPTX_SWAP Low-Power Signal Swap Control Register. This register is only valid in C-PHY mode. When this register is set to HIGH, the Low-Power signal output A/C will be swapped.
4	RW	0x0	SYMBOL_SWAP Symbol Swap Control Register. When this register is set to HIGH, 7-symbol input will be swapped.
3:2	RO	0x0	reserved
1	RW	0x0	CLK_INV Clock Inversion Control Register. When this register is set to HIGH, the clock output of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data input will be swapped.

DCPHY_M0_COMBO_MD2_PRGSEQ_CON0

Address: Operational Base(0x2B020000) + offset (0x0660)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	PROG_SEQ_EN Programmable Sequence Enable Register. When this register is set to HIGH, Programmable Sequence of the Preamble is used as setting value in PROG_SEQ{COMBO_M#D#_PRGSEQ_CON1[9:0], COMBO_M#D#_PRGSEQ_CON2[15:0], COMBO_M#D#_PRGSEQ_CON3[15:0]}.

DCPHY_M0_COMBO_MD2_PRGSEQ_CON1

Address: Operational Base(0x2B020000) + offset (0x0664)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD2_PRGSEQ_CON2

Address: Operational Base(0x2B020000) + offset (0x0668)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD2_PRGSEQ_CON3

Address: Operational Base(0x2B020000) + offset (0x066C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_DPHY_MD3_GNR_CON0

Address: Operational Base(0x2B020000) + offset (0x0700)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(DPHY_M#D#_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_DPHY_MD3_GNR_CON1

Address: Operational Base(0x2B020000) + offset (0x0704)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(DPHY_M#D#_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_DPHY_MD3_ANA_CON0

Address: Operational Base(0x2B020000) + offset (0x0708)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:12	RW	0x7	EDGE_CON Cap Peaking Control Register. Set the register as below. In case of D-PHY, 3'b111 In case of C-PHY, 3'b001

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Bit	Attr	Reset Value	Description
11:10	RO	0x0	reserved
9	RW	0x0	EDGE_CON_DIR Cap Peaking Direction Control Register. Set the register as below. In case of D-PHY,1'b0 In case of C-PHY,1'b1
8	RW	0x1	EDGE_CON_EN Cap Peaking Enable Register.
7:4	RW	0x3	RES_UP High-Speed Driver Up Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm
3:0	RW	0x3	RES_DN High-Speed Driver Down Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm

DCPHY_M0_DPHY_MD3_ANA_CON1

Address: Operational Base(0x2B020000) + offset (0x070C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	IQ_RESETN_POL_CON I-Q Clock Polarity Control Register.
14	RW	0x0	VREG12_VALID 1.2V Voltage Regulator Valid Control Register.
13	RW	0x0	VREG12_VALID_SEL 1.2V Voltage Regulator Valid Select Register.

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Bit	Attr	Reset Value	Description
12	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.
11	RW	0x0	ATB_SEL_GND Analog Test Bus Select for SER Ground Register.
10	RW	0x0	ATB_SEL_VDD Analog Test Bus Select for SER Power Register.
9:8	RW	0x0	LPTX_SR_UP Low-Power TX Driver Slew Rate Up Enable Register. Releated with LPTX_SR_CTRL Register. 2b'1X: Max slew rate 2b'0X: Default
7:6	RO	0x0	reserved
5:4	RW	0x0	LPTX_SR_CTRL Low-Power TX Driver Slew Rate Control Register. When LPTX_SR_UP is 2b'0X, 2b'00: Default 2b'01 or 2b'10: Decrease slew rate by 1% 2b'11: Decrease slew rate by 2%
3:2	RO	0x0	reserved
1:0	RW	0x0	EMP De-Emphasis Control Register. In case of D-PHY: Data Rate >=4.5Gbps: 2'b01 Data Rate < 4.5Gbps: 2'b00 2'b00: 0 dB 2'b01: -1.5 dB 2'b10: -3.5 dB 2'b11: -6.5 dB In case of C-PHY, Data Rate <= 2Gsps 2'b00: 0dB 2'b01: NA 2'b10: NA 2'b11: NA

DCPHY_M0_DPHY_MD3_ANA_CON2

Address: Operational Base(0x2B020000) + offset (0x0710)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	LPRX_HYS_SEL Low-Power RX Hysterisis Select Register.
11	RO	0x0	reserved
10:8	RW	0x0	DTB_SEL Digital Test Bus Select Register.
7	RW	0x0	CNT_REJECTION_PULSE Pulse Rejection Control Register.
6	RW	0x0	SEL_ESCPOL Escape Mode Clock Polarity Select Register.
5	RW	0x0	SEL_VREF Reference Voltage Select Register.
4	RW	0x0	CNT_ULPSHYS ULPS Hysterisis Control Register.
3	RW	0x0	EN_RSTN_SEL Reset Enable Select Register.

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Bit	Attr	Reset Value	Description
2	RW	0x0	PULSE_REJ_ENB Pulse Rejection Enable Register.
1	RW	0x0	LPCD_HYS_SEL Low-Power Contention Detect Hysterisis Select Register.
0	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.

DCPHY_M0_DPHY_MD3_TIME_CON0

Address: Operational Base(0x2B020000) + offset (0x0730)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	HSTX_CLK_SEL HS-TX State Machine Clock Select Register. HS-TX Clock is used for counting some of timing specifications. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
11:4	RW	0x00	T_LPX TLPX Timing Counter Register. This count value is specially used in High-Speed Transmit operation
3:2	RW	0x0	T_LP_EXIT_SKEW High-Speed Data Transmission End-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the End-of-Transmission procedure of High-Speed Data Transmission.
1:0	RW	0x0	T_LP_ENTRY_SKEW High-Speed Data Transmission Start-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the Start-of-Transmission procedure of High-Speed Data Transmission.

DCPHY_M0_DPHY_MD3_TIME_CON1

Address: Operational Base(0x2B020000) + offset (0x0734)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_ZERO THS-ZERO (D-PHY) / T3-PREBEGIN (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.
7:0	RW	0x00	T_HS_PREPARE THS-PREPARE (D-PHY) / T3-PREPARE (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance..

DCPHY_M0_DPHY_MD3_TIME_CON2

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Address: Operational Base(0x2B020000) + offset (0x0738)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_EXIT THS-EXIT Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.
7:0	RW	0x00	T_HS_TRAIL THS-TRAIL (D-PHY) / T3-POST (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.

DCPHY_M0_DPHY_MD3_TIME_CON3

Address: Operational Base(0x2B020000) + offset (0x073C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	T_TA_GET TTA-GET Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.
3:0	RW	0x0	T_TA_GO TTA-GO Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.

DCPHY_M0_DPHY_MD3_TIME_CON4

Address: Operational Base(0x2B020000) + offset (0x0740)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	T_ULPS_EXIT Ultra-Low Power Exit Timing Counter Register. This count value is used in Ultra-Low Power operation. For exiting Ultra-Low Power State, the Link layer can set PPI signal "TXULPSEXIT" to HIGH. There are two conditions for moving the state of PHY to "TX-ULPS-Exit." One is that the Link layer control PPI signal "TXULPSCLK" to LOW. Another way is to use the counter in PHY.

DCPHY_M0_DPHY_MD3_DATA_CON0

Address: Operational Base(0x2B020000) + offset (0x0744)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	ERR_CONTENTION_DISABLE Contention Error Detect Disable Control Register. When this register is set to HIGH, the contention error will not occur through "ERRCONTENTIONLP0/1."
11:9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	TRIG_EXIT_CLK_EN Trigger Mode Exit Clock Toggle Enable Register. When this register is set to HIGH, after transmitting the trigger command, DP signal is toggled as period of Escape mode clock until "TXREQUESTESC" goes to LOW.
7:2	RO	0x00	reserved
1	RW	0x0	CLK_INV Clock Inversion Control Register. When this register is set to HIGH, the clock output of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data input will be swapped.

DCPHY_M0_DPHY_SC_GNR_CON0

Address: Operational Base(0x2B020000) + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(DPHY_S#C_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_DPHY_SC_GNR_CON1

Address: Operational Base(0x2B020000) + offset (0x0B04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(DPHY_S#C_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_DPHY_SC_ANA_CON0

Address: Operational Base(0x2B020000) + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	HS_RX_CNT_ROUT Output Resistor of HSRX AFE's 1st Stage Amp 3'b000: 282 Ohm 3'b001: 188 Ohm 3'b011: 141 Ohm 3'b100: 565 Ohm

DCPHY_M0_DPHY_SC_ANA_CON1

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Address: Operational Base(0x2B020000) + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RW	0x00	HS_RX_BIAS_CON [15]: Diff to CMOS Level shifter's current 1'b0:550uA 1'b1:650uA [14:13]: 2nd stage amp bias current 2'b00:500uA 2'b01:550uA 2'b10:600uA 2'b11:650uA [12:11]: 1st stage amp bias current 2'b00:700uA 2'b01:850uA 2'b10:350uA 2'b11:500uA
10	RO	0x0	reserved
9	RW	0x0	HS_RX_FLATBAND EQ On/Off Control Register. 1'b0: EQ off, 1'b1: EQ on
8	RO	0x0	reserved
7:4	RW	0x0	HS_RX_RSELCNT EQ Resistor Control Register. 5'b00000: forbidden (infinite resistance) 5b'00001: 330 Ohm 5b'00100: 660 Ohm 5b'01000: 1.3k Ohm 5b'01100: 440 Ohm 5b'01111: 130 Ohm (min) 5b'10000: 2.6k Ohm (max) 5b'10100: 530 Ohm 5b'10101: 200 Ohm 24d~31d: forbidden
3:0	RW	0x0	HS_RX_CAPCNT EQ Capacitor Control (Covered Freq.) Register. 4'b0000: 7.43GHz 4'b0001: 4.82GHz 4'b0010: 4.09GHz 4'b0011: 3.58GHz 4'b0100: 3.44GHz 4'b0101: 3.12GHz 4'b0110: 2.87GHz 4'b0111: 2.7GHz ** MSB[2]: gain/freq control of 2nd amp

DCPHY_M0_DPHY_SC_ANA_CON2

Address: Operational Base(0x2B020000) + offset (0x0B10)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	CLK_HSRX_ENABLE_MAN CLK_HSRX_ENABLE, Only Test mode for DPHY
14:12	RO	0x0	reserved
11	RW	0x0	CLK_TERM_EN_MAN CLK Term enable, Only Test mode for DPHY

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Bit	Attr	Reset Value	Description
10	RW	0x0	HSMODE_MAN_SEL Only Test mode for DPHY, 1'b0: Normal 1'b1: Test mode
9:8	RW	0x0	CLK_DIV1234_MC clk div 1/2/3/4 ctrl, 2'b00: Div4 2'b01: Div3 2'b10: Div2 2'b11: Div1
7	RW	0x0	SKEWCAL_CLK_SEL Skew Calibration Clock Rate Control Register. 1'b0: Fin/8 1'b1: Fin/4 Fin is input clock speed.
6	RO	0x0	reserved
5	RW	0x0	HS_UNTERM_EN Termination control pin for DPHY HS-RX, 1'b0: Term, 1'b1: Un-Term
4:3	RO	0x0	reserved
2:0	RW	0x0	HS_TERM_SW HS-RX Termination Impedance Control 3b'000: 102 Ohm 3b'001: 99.1 Ohm 3b'010: 96.6 Ohm (default) 3b'011: 94.1 Ohm 3b'100: 113 Ohm 3b'101: 110 Ohm 3b'110: 107 Ohm 3b'111: 104 Ohm

DCPHY_M0_DPHY_SC_ANA_CON3

Address: Operational Base(0x2B020000) + offset (0x0B14)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	EN_RSTN_SEL internal resetn sel. 0x0: Enable_D2A 0x1: ResetN_D2A
14	RW	0x0	DPDN_SWAP DPDN swap, 1'b0: Normal, 1'b1: Swap
13:12	RW	0x0	HS_DELAY_CON Clk delay control for loopback test at Clock lane 2'b00: 20pS 2'b01: 40pS 2'b10: 60pS 2'b11: 80pS
11	RW	0x0	SEL_ESCPOL LP ESCCLK Polarity sel 1'b0: Normal 1'b1: Swap

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	ULPS_HYS_SW_DPHY ULPS Hysterisis Level Control 3'b000: 126mV 3'b001: 135mV 3'b010: 143mV 3'b011: 150mV 3'b100: 64.6mV 3'b101: 82.2mV 3'b110: 104mV 3'b111: 117mV
7	RW	0x0	CNT_REJECT_PULSE LP Pulse Reject Time Control 1b'0: Default 1b'1: Smaller Reject Time
6	RW	0x0	LP_EN_PRECHARGE_SEL LPRX Pre-charge Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
5:4	RW	0x0	LP_HYS_SW LP-RX Hysteresis Level Control 2'b00: 45mV 2'b01: 65mV 2'b10: 85mV 2'b11: 100mV
3	RW	0x0	PULSE_REJ_ENB Pulse Rejecter Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
2	RW	0x0	CULPS_HYS Ulps vref sel, 1'b0: Self bias, 1'b1: From r-ladder
1:0	RW	0x0	LPRX_BIAS_CTRL Rx normal LP bias select, 2'b00: 25uA 2'b01: 35uA 2'b10: 20uA 2'b11: 25uA

DCPHY_M0_DPHY_SC_ANA_CON4

Address: Operational Base(0x2B020000) + offset (0x0B18)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	CLK_DBL_CTRL clk doubler pulse width ctrl, 2'b00: 1nS 2'b01: 2nS 2'b10: 3nS 2'b11: 4ns
11	RW	0x0	REG05_11 Forcing HS-RX Mode Enable/Disable Control 0x0: Disable 0x1: Enable
10:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	ATB_SEL_VREF ATB Enable, 1'b0: Switch off, 1'b1: Switch on(Vref 645MV)
6	RW	0x0	VREF_BGRVDD_SEL Slave Reference Voltage 520mV Selection Control, 1'b0: BGR, 1'b1: R-ladder
5:4	RW	0x0	LP_VREF520_SW ULPS reference voltage option selection
3:0	RW	0x0	ATB_SEL_DMY ATB Enable, 1'b0: Switch off, 1'b1: Switch on(AVSS, AVSS, AVDDL, AVSS)

DCPHY_M0_DPHY_SC_ANA_CON5

Address: Operational Base(0x2B020000) + offset (0x0B1C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	CLK_MISS_DISABLE Clock Miss Disable Control Register.
14:12	RO	0x0	reserved
11	RW	0x0	NON_MIPI_ENABLE 1'b0: Non mipi feature disable 1'b1: Non mipi feature enable
10	RO	0x0	reserved
9:0	RW	0x000	RXBIAS_CNT Slave DPHY I bias ctrl, ([1:0]-SD0, [3:2]-SD1, [5:4]-SD2, [7:6]-SD3, [9:8]-SC) 2'b00: 50uA 2'b01: 37.5uA 2'b10: 37.5uA 2'b11: 25uA

DCPHY_M0_DPHY_SC_TIME_CON0

Address: Operational Base(0x2B020000) + offset (0x0B30)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	T_CLK_MISS Clock Miss Detect Timing Control Register. This count value is used in High-Speed Transmit operation. There is a watchdog timer in Receive logic for detecting Clock Miss. If the clock is not detected in Slave Clock Lane until the watchdog timer is expired, then internal flag is set. Please refer to "Supplement Guide" for setting this register.
7:0	RW	0x00	T_CLK_SETTLE TCLK-SETTLE Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" of mipi alliance. And please refer to "Supplement Guide" for setting this register according to data rate.

DCPHY_M0_COMBO_SD0_GNR_CON0

Address: Operational Base(0x2B020000) + offset (0x0C00)

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Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(DPHY_S#D0_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_COMBO_SD0_GNR_CON1

Address: Operational Base(0x2B020000) + offset (0x0C04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(DPHY_S#D0_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_COMBO_SD0_ANA_CON0

Address: Operational Base(0x2B020000) + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	HS_RX_CNT_ROUT Output Resistor of HSRX AFE's 1st Stage Amp 3'b000: 282 Ohm 3'b001: 188 Ohm 3'b011: 141 Ohm 3'b100: 565 Ohm

DCPHY_M0_COMBO_SD0_ANA_CON1

Address: Operational Base(0x2B020000) + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RW	0x00	HS_RX_BIAS_CON [15]: Diff to CMOS Level shifter's current 1'b0: 550uA 1'b1: 650uA [14:13]: 2nd stage amp bias current 2'b00: 500uA 2'b01: 550uA 2'b10: 600uA 2'b11: 650uA [12:11]: 1st stage amp bias current 2'b00: 700uA 2'b01: 850uA 2'b10: 350uA 2'b11: 500uA
10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	HS_RX_FLATBAND EQ On/Off Control Register. 1'b0: EQ off, 1'b1: EQ on
8	RO	0x0	reserved
7:4	RW	0x0	HS_RX_RSELCNT EQ Resistor Control Register. In case of DPHY 5'b00000: Forbidden (infinite resistance) 5b'00101: 200 Ohm 5b'00001: 300 Ohm 5b'00010: 400 Ohm 5b'10100: 480 Ohm 5b'00100: 600 Ohm 5b'11000: 800 Ohm In case of CPHY 5'b00000: Forbidden (infinite resistance) 5b'01111: 220 Ohm 5b'00110: 280 Ohm 5b'10010: 430 Ohm 5b'10100: 600 Ohm 5b'00100: 700 Ohm 5b'00001: 1300 Ohm
3:0	RW	0x0	HS_RX_CAPCNT EQ Capacitor Control (Covered Freq.) Register. ** MSB[3]: gain/freq control of 2nd amp In case of DPHY 4'b0000: 7.43GHz 4'b0001: 4.82GHz 4'b0010: 4.09GHz 4'b0011: 3.58GHz 4'b0100: 3.44GHz 4'b0101: 3.12GHz 4'b0110: 2.87GHz 4'b0111: 2.7GHz In case of CPHY 4'b0000: Small capacitance 4'b0001: Large capacitance HS_RX_CAPCNT[1:0]: Reserved

DCPHY_M0_COMBO_SD0_ANA_CON2

Address: Operational Base(0x2B020000) + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	SEL_FDLY Fine delay on/off control pin for skew cal, DPHY only. 0x0: Fine delay 0x1: Bypass
13:12	RW	0x0	UDLY_SPDCNT Fine delay selection for Skew cal, DPHY only. 2'b00: 4.89ps, 2'b10: 7.72ps
11	RW	0x0	HS_TERM_EN_MAN TERM_ENABLE, Only Test mode for DPHY

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Bit	Attr	Reset Value	Description
10	RW	0x0	HSMODE_MAN_SEL Only Test mode for DPHY, 1'b0: Normal, 1'b1: Test mode
9:8	RW	0x0	SKEW_DLYSEL Set the register as below. 4.0Gbps <= Data Rate <= 6.5Gbps: 2'b00 3.0Gbps <= Data Rate < 4.0Gbps: 2'b01 2.0Gbps <= Data Rate < 3.0Gbps: 2'b10 1.5Gbps <= Data Rate < 2.0Gbps: 2'b11 2'b00 for the rest.
7	RW	0x0	RXDDRCLKHS_SEL Clock selection pin for Data patch clock 0x0: CLK1 0x1: CLK2
6	RW	0x0	SKEW_CAL_EXT_FORCE Manual Skew Calibration control 0x0: Disable 0x1: Enable
5	RW	0x0	HS_UNTERM_EN Termination control pin for DPHY HS-RX, 1'b0: Term, 1'b1: Un-Term
4:3	RO	0x0	reserved
2:0	RW	0x0	RX_TERM_SW HS-RX Termination Impedance Control 3b'000: 102 Ohm 3b'001: 99.1 Ohm 3b'010: 96.6 Ohm (default) 3b'011: 94.1 Ohm 3b'100: 113 Ohm 3b'101: 110 Ohm 3b'110: 107 Ohm 3b'111: 104 Ohm

DCPHY_M0_COMBO_SD0_ANA_CON3

Address: Operational Base(0x2B020000) + offset (0x0C14)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	EN_RSTN_SEL Internal resetn sel. 0x0: Enabel_D2A 0x1: ResetN_D2A
14	RW	0x0	DPDN_SWAP DPDN swap, 1'b0: Normal 1'b1: Swap
13:12	RW	0x0	HS_DELAY_CON Clk delay control for loopback test at Clock lane 2'b00: 20pS 2'b01: 40pS 2'b10: 60pS 2'b11: 80pS

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Bit	Attr	Reset Value	Description
11	RW	0x0	SEL_ESCPOL LP ESCCLK Polarity sel 1'b0: Normal 1'b1: Swap
10:8	RW	0x0	ULPS_HYS_SW_DPHY ULPS Hysterisis Level Control 3'b000: 126mV 3'b001: 135mV 3'b010: 143mV 3'b011: 150mV 3'b100: 64.6mV 3'b101: 82.2mV 3'b110: 104mV 3'b111: 117mV
7	RW	0x0	CNT_REJECT_PULSE LP Pulse Reject Time Control 1b'0: Default 1b'1: Smaller Reject Time
6	RW	0x0	LP_EN_PRECHARGE_SEL LPRX Pre-charge Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
5:4	RW	0x0	LP_HYS_SW LP-RX Hysteresis Level Control 2'b00: 45mV 2'b01: 65mV 2'b10: 85mV 2'b11: 100mV
3	RW	0x0	PULSE_REJ_ENB Pulse Rejecter Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
2	RW	0x0	CULPS_HYS ulps vref sel, 1'b0: Self bias, 1'b1: From r-ladder
1:0	RW	0x0	LPRX_BIAS_CTRL Rx normal LP bias sel, 2'b00: 25uA 2'b01: 35uA 2'b10: 20uA 2'b11: 25uA

DCPHY_M0_COMBO_SD0_ANA_CON4

Address: Operational Base(0x2B020000) + offset (0x0C18)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	REG05_11 Forcing HS-RX Mode Enable/Disable Control 0x0: Disable 0x1: Enable
10:0	RO	0x000	reserved

DCPHY_M0_COMBO_SD0_ANA_CON6

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Address: Operational Base(0x2B020000) + offset (0x0C20)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	DL_COMP_CTRL UI mask code output control - sec control
7:6	RO	0x0	reserved
5:4	RW	0x0	UI_MASK_CTRL UI Mask control - sec control
3	RW	0x0	EXT_DL_MUX_EN 1UI data sampling type - sec control
2:0	RO	0x0	reserved

DCPHY_M0_COMBO_SD0_ANA_CON7

Address: Operational Base(0x2B020000) + offset (0x0C24)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	CLK_DBL_CTRL XI to doubler clock delay cotrol - sec control
5:0	RO	0x00	reserved

DCPHY_M0_COMBO_SD0_TIME_CON0

Address: Operational Base(0x2B020000) + offset (0x0C30)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	SETTLE_CLK_SEL Settle Counter Clock Select Register. Settle Clock is used for counting TCLK-SETTLE. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
7:0	RW	0x00	T_HS_SETTLE TSETTLE Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" of mipi alliance. And please refer to "Supplement Guide" for setting this register according to data rate.

DCPHY_M0_COMBO_SD0_TIME_CON1

Address: Operational Base(0x2B020000) + offset (0x0C34)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	T_ERR_SOT_SYNC SoT Sync Error Detect Timing Control Register. This count value is used in High-Speed Transmit operation. There is a watchdog timer in Receive logic for detecting SoT Sync Error. If the Sync Pattern is not detected until the watchdog timer is expired, then the PPI signal "ERRSOTSYNC" goes to HIGH.

DCPHY_M0_COMBO_SD0_DATA_CON0

Address: Operational Base(0x2B020000) + offset (0x0C38)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	SYMBOL_SWAP Symbol Swap Control Register. When this register is set to HIGH, 7-symbol data will be swapped.
3:2	RO	0x0	reserved
1	RW	0x0	DATA_INV Data Inversion Control Register. When this register is set to HIGH, the data input of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data output will be swapped.

DCPHY_M0_COMBO_SD0_DESKEW_CON0

Address: Operational Base(0x2B020000) + offset (0x0C40)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SKEW_CAL_DES_SEL Skew Calibration Clock Division Ratio Control Register.
3:1	RO	0x0	reserved
0	RW	0x0	SKEW_CAL_EN Skew Calibration Enable Register.

DCPHY_M0_COMBO_SD0_DESKEW_CON1

Address: Operational Base(0x2B020000) + offset (0x0C44)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	SKEW_CAL_FINAL_COMP_TIME Skew Calibration Final Compare Time Control Register.
7:6	RW	0x0	SKEW_CAL_COMP_TOL Skew Calibration Compare Tolerance Control Register.
5:4	RW	0x0	SKEW_CAL_COMP_WAIT_TIME Skew Calibration Compare Wait Time Control Register.
3:0	RW	0x0	SKEW_CAL_COMP_RUN_TIME Skew Calibration Compare Run Time Control Register.

DCPHY_M0_COMBO_SD0_DESKEW_CON2

Address: Operational Base(0x2B020000) + offset (0x0C48)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	SKEW_CAL_DATA_COARSE_SET Skew Calibration Manual Data Coarse Delay Control Register.
7:5	RO	0x0	reserved
4:0	RW	0x00	SKEW_CAL_CLK_COARSE_SET Skew Calibration Manual Data Fine Delay Control Register.

DCPHY_M0_COMBO_SD0_DESKEW_CON3

Address: Operational Base(0x2B020000) + offset (0x0C4C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	SKEW_CAL_DATA_FINE_FALL_SET Skew Calibration Manual Data Fine Falling Delay Control Register.
11:8	RW	0x0	SKEW_CAL_DATA_FINE_RISE_SET Skew Calibration Manual Data Fine Rising Delay Control Register.

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	SKEW_CAL_CLK_FINE_FALL_SET Skew Calibration Manual Clock Fine Falling Delay Control Register.
3:0	RW	0x0	SKEW_CAL_CLK_FINE_RISE_SET Skew Calibration Manual Clock Fine Rising Delay Control Register.

DCPHY_M0_COMBO_SD0_DESKEW_CON4

Address: Operational Base(0x2B020000) + offset (0x0C50)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	SKEW_CAL_FINE_MAX_SET Skew Calibration Maximum Fine Delay Step Control Register.
7:5	RO	0x0	reserved
4:0	RW	0x00	SKEW_CAL_COARSE_MAX_SET Skew Calibration Maximum Coarse Delay Step Control Register.

DCPHY_M0_COMBO_SD0_CRC_CON0

Address: Operational Base(0x2B020000) + offset (0x0C60)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:4	RW	0x00	CRC_FORCE_CODE CRC Forcing Mode Code Control Register.
3:1	RO	0x0	reserved
0	RW	0x0	CRC_FORCE_CODE_EN CRC Forcing Mode Enable Register.

DCPHY_M0_COMBO_SD0_CRC_CON1

Address: Operational Base(0x2B020000) + offset (0x0C64)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	CRC_POST_GATING_CNT CRC Post Gating Count Register.
7	RW	0x0	CRC_POST_GATING_EN CRC Post Gating Enable Register.
6:4	RW	0x0	CRC_SETTLE_MASK_SEL CRC Clock Polarity Control Register.
3	RW	0x0	CRC_POL_SEL CRC Clock Polarity Control Register.
2	RW	0x0	CRC_SOT_SYNC_ERR_CHK CRC SoT Sync Error Check Enable Register.
1:0	RW	0x0	CRC_AVG_SEL CRC Code Average Select Register.

DCPHY_M0_COMBO_SD0_CRC_CON2

Address: Operational Base(0x2B020000) + offset (0x0C68)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	CRC_BURST_CNT CRC Multiple Burst Count for Average Code Register.
11:9	RO	0x0	reserved
8	RW	0x0	CRC_CODE_FIX CRC Code Fix Control Register.
7:4	RW	0x0	CRC_CODE_TOL CRC Code Tolerance Control Register.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	CRC_CODE_TUNE CRC Code Tuning Register.

DCPHY_M0_COMBO_SD1_GNR_CON0

Address: Operational Base(0x2B020000) + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(DPHY_S#D1_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_COMBO_SD1_GNR_CON1

Address: Operational Base(0x2B020000) + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(DPHY_S#D1_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_COMBO_SD1_ANA_CON0

Address: Operational Base(0x2B020000) + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	HS_RX_CNT_ROUT Output Resistor of HSRX AFE's 1st Stage Amp 3'b000: 282 Ohm 3'b001: 188 Ohm 3'b011: 141 Ohm 3'b100: 565 Ohm

DCPHY_M0_COMBO_SD1_ANA_CON1

Address: Operational Base(0x2B020000) + offset (0x0D0C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:11	RW	0x00	HS_RX_BIAS_CON [15]: Diff to CMOS Level shifter's current 1'b0: 550uA 1'b1: 650uA [14:13]: 2nd stage amp bias current 2'b00: 500uA 2'b01: 550uA 2'b10: 600uA 2'b11: 650uA [12:11]: 1st stage amp bias current 2'b00: 700uA 2'b01: 850uA 2'b10: 350uA 2'b11: 500uA
10	RO	0x0	reserved
9	RW	0x0	HS_RX_FLATBAND EQ On/Off Control Register. 1'b0: EQ off, 1'b1: EQ on
8	RO	0x0	reserved
7:4	RW	0x0	HS_RX_RSELCNT EQ Resistor Control Register. In case of DPHY 5'b00000: Forbidden (infinite resistance) 5b'00101: 200 Ohm 5b'00001: 300 Ohm 5b'00010: 400 Ohm 5b'10100: 480 Ohm 5b'00100: 600 Ohm 5b'11000: 800 Ohm In case of CPHY 5'b00000: Forbidden (infinite resistance) 5b'01111: 220 Ohm 5b'00110: 280 Ohm 5b'10010: 430 Ohm 5b'10100: 600 Ohm 5b'00100: 700 Ohm 5b'00001: 1300 Ohm
3:0	RW	0x0	HS_RX_CAPCNT EQ Capacitor Control (Covered Freq.) Register. ** MSB[3]: gain/freq control of 2nd amp In case of DPHY 4'b0000: 7.43GHz 4'b0001: 4.82GHz 4'b0010: 4.09GHz 4'b0011: 3.58GHz 4'b0100: 3.44GHz 4'b0101: 3.12GHz 4'b0110: 2.87GHz 4'b0111: 2.7GHz In case of CPHY 4'b0000: Small capacitance 4'b0001: Large capacitance HS_RX_CAPCNT[1:0]: Reserved

DCPHY_M0_COMBO_SD1_ANA_CON2

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Address: Operational Base(0x2B020000) + offset (0x0D10)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	SEL_FDLY Fine delay on/off control pin for skew cal, DPHY only. 0x0: Fine delay 0x1: Bypass
13:12	RW	0x0	UDLY_SPDCNT Fine delay selection for Skew cal, DPHY only. 2'b00: 4.89ps, 2'b10: 7.72ps
11	RW	0x0	HS_TERM_EN_MAN TERM_ENABLE, Only Test mode for DPHY
10	RW	0x0	HSMODE_MAN_SEL Only Test mode for DPHY, 1'b0: Normal, 1'b1: Test mode
9:8	RW	0x0	SKEW_DLYSEL Set the register as below. 4.0Gbps <= Data Rate <= 6.5Gbps: 2'b00 3.0Gbps <= Data Rate < 4.0Gbps: 2'b01 2.0Gbps <= Data Rate < 3.0Gbps: 2'b10 1.5Gbps <= Data Rate < 2.0Gbps: 2'b11 2'b00 for the rest.
7	RW	0x0	RXDDRCLKHS_SEL Clock selection pin for Data patch clock 0x0: CLK1 0x1: CLK2
6	RW	0x0	SKEW_CAL_EXT_FORCE Manual Skew Calibration control 0x0: Disable 0x1: Enable
5	RW	0x0	HS_UNTERM_EN Termination control pin for DPHY HS-RX, 1'b0: Term, 1'b1: Un-Term
4:3	RO	0x0	reserved
2:0	RW	0x0	RX_TERM_SW HS-RX Termination Impedance Control 3b'000: 102 Ohm 3b'001: 99.1 Ohm 3b'010: 96.6 Ohm (default) 3b'011: 94.1 Ohm 3b'100: 113 Ohm 3b'101: 110 Ohm 3b'110: 107 Ohm 3b'111: 104 Ohm

DCPHY_M0_COMBO_SD1_ANA_CON3

Address: Operational Base(0x2B020000) + offset (0x0D14)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	EN_RSTN_SEL Internal resetn sel. 0x0: Enabel_D2A 0x1: ResetN_D2A

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Bit	Attr	Reset Value	Description
14	RW	0x0	DPDN_SWAP DPDN swap, 1'b0: Normal 1'b1: Swap
13:12	RW	0x0	HS_DELAY_CON Clk delay control for loopback test at Clock lane 2'b00: 20pS 2'b01: 40pS 2'b10: 60pS 2'b11: 80pS
11	RW	0x0	SEL_ESCPOL LP ESCCLK Polarity sel 1'b0: Normal 1'b1: Swap
10:8	RW	0x0	ULPS_HYS_SW_DPHY ULPS Hysterisis Level Control 3'b000: 126mV 3'b001: 135mV 3'b010: 143mV 3'b011: 150mV 3'b100: 64.6mV 3'b101: 82.2mV 3'b110: 104mV 3'b111: 117mV
7	RW	0x0	CNT_REJECT_PULSE LP Pulse Reject Time Control 1b'0: Default 1b'1: Smaller Reject Time
6	RW	0x0	LP_EN_PRECHARGE_SEL LPRX Pre-charge Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
5:4	RW	0x0	LP_HYS_SW LP-RX Hysteresis Level Control 2'b00: 45mV 2'b01: 65mV 2'b10: 85mV 2'b11: 100mV
3	RW	0x0	PULSE_REJ_ENB Pulse Rejecter Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
2	RW	0x0	CULPS_HYS ulps vref sel, 1'b0: Self bias, 1'b1: From r-ladder
1:0	RW	0x0	LPRX_BIAS_CTRL Rx normal LP bias sel, 2'b00: 25uA 2'b01: 35uA 2'b10: 20uA 2'b11: 25uA

DCPHY_M0_COMBO_SD1_ANA_CON4

Address: Operational Base(0x2B020000) + offset (0x0D18)

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Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	REG05_11 Forcing HS-RX Mode Enable/Disable Control 0x0: Disable 0x1: Enable
10:0	RO	0x000	reserved

DCPHY_M0_COMBO_SD1_ANA_CON6

Address: Operational Base(0x2B020000) + offset (0x0D20)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	DL_COMP_CTRL UI mask code output control - sec control
7:6	RO	0x0	reserved
5:4	RW	0x0	UI_MASK_CTRL UI Mask control - sec control
3	RW	0x0	EXT_DL_MUX_EN 1UI data sampling type - sec control
2:0	RO	0x0	reserved

DCPHY_M0_COMBO_SD1_ANA_CON7

Address: Operational Base(0x2B020000) + offset (0x0D24)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	CLK_DBL_CTRL XI to doubler clock delay cotrol - sec control
5:0	RO	0x00	reserved

DCPHY_M0_COMBO_SD1_TIME_CON0

Address: Operational Base(0x2B020000) + offset (0x0D30)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	SETTLE_CLK_SEL Settle Counter Clock Select Register. Settle Clock is used for counting TCLK-SETTLE. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
7:0	RW	0x00	T_HS_SETTLE TSETTLE Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" of mipi alliance. And please refer to "Supplement Guide" for setting this register according to data rate.

DCPHY_M0_COMBO_SD1_TIME_CON1

Address: Operational Base(0x2B020000) + offset (0x0D34)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	T_ERR_SOT_SYNC SoT Sync Error Detect Timing Control Register. This count value is used in High-Speed Transmit operation. There is a watchdog timer in Receive logic for detecting SoT Sync Error. If the Sync Pattern is not detected until the watchdog timer is expired, then the PPI signal "ERRSOTSYNC" goes to HIGH.

DCPHY_M0_COMBO_SD1_DATA_CON0

Address: Operational Base(0x2B020000) + offset (0x0D38)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SYMBOL_SWAP Symbol Swap Control Register. When this register is set to HIGH, 7-symbol data will be swapped.
3:2	RO	0x0	reserved
1	RW	0x0	DATA_INV Data Inversion Control Register. When this register is set to HIGH, the data input of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data output will be swapped.

DCPHY_M0_COMBO_SD1_DESKEW_CON0

Address: Operational Base(0x2B020000) + offset (0x0D40)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SKEW_CAL_DES_SEL Skew Calibration Clock Division Ratio Control Register.
3:1	RO	0x0	reserved
0	RW	0x0	SKEW_CAL_EN Skew Calibration Enable Register.

DCPHY_M0_COMBO_SD1_DESKEW_CON1

Address: Operational Base(0x2B020000) + offset (0x0D44)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	SKEW_CAL_FINAL_COMP_TIME Skew Calibration Final Compare Time Control Register.
7:6	RW	0x0	SKEW_CAL_COMP_TOL Skew Calibration Compare Tolerance Control Register.
5:4	RW	0x0	SKEW_CAL_COMP_WAIT_TIME Skew Calibration Compare Wait Time Control Register.
3:0	RW	0x0	SKEW_CAL_COMP_RUN_TIME Skew Calibration Compare Run Time Control Register.

DCPHY_M0_COMBO_SD1_DESKEW_CON2

Address: Operational Base(0x2B020000) + offset (0x0D48)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	SKEW_CAL_DATA_COARSE_SET Skew Calibration Manual Data Coarse Delay Control Register.
7:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	SKEW_CAL_CLK_COARSE_SET Skew Calibration Manual Data Fine Delay Control Register.

DCPHY_M0_COMBO_SD1_DESKEW_CON3

Address: Operational Base(0x2B020000) + offset (0x0D4C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	SKEW_CAL_DATA_FINE_FALL_SET Skew Calibration Manual Data Fine Falling Delay Control Register.
11:8	RW	0x0	SKEW_CAL_DATA_FINE_RISE_SET Skew Calibration Manual Data Fine Rising Delay Control Register.
7:4	RW	0x0	SKEW_CAL_CLK_FINE_FALL_SET Skew Calibration Manual Clock Fine Falling Delay Control Register.
3:0	RW	0x0	SKEW_CAL_CLK_FINE_RISE_SET Skew Calibration Manual Clock Fine Rising Delay Control Register.

DCPHY_M0_COMBO_SD1_DESKEW_CON4

Address: Operational Base(0x2B020000) + offset (0x0D50)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	SKEW_CAL_FINE_MAX_SET Skew Calibration Maximum Fine Delay Step Control Register.
7:5	RO	0x0	reserved
4:0	RW	0x00	SKEW_CAL_COARSE_MAX_SET Skew Calibration Maximum Coarse Delay Step Control Register.

DCPHY_M0_COMBO_SD1_CRC_CON0

Address: Operational Base(0x2B020000) + offset (0x0D60)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:4	RW	0x00	CRC_FORCE_CODE CRC Forcing Mode Code Control Register.
3:1	RO	0x0	reserved
0	RW	0x0	CRC_FORCE_CODE_EN CRC Forcing Mode Enable Register.

DCPHY_M0_COMBO_SD1_CRC_CON1

Address: Operational Base(0x2B020000) + offset (0x0D64)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	CRC_POST_GATING_CNT CRC Post Gating Count Register.
7	RW	0x0	CRC_POST_GATING_EN CRC Post Gating Enable Register.
6:4	RW	0x0	CRC_SETTLE_MASK_SEL CRC Clock Polarity Control Register.
3	RW	0x0	CRC_POL_SEL CRC Clock Polarity Control Register.
2	RW	0x0	CRC_SOT_SYNC_ERR_CHK CRC SoT Sync Error Check Enable Register.
1:0	RW	0x0	CRC_AVG_SEL CRC Code Average Select Register.

DCPHY_M0_COMBO_SD1_CRC_CON2

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Address: Operational Base(0x2B020000) + offset (0x0D68)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	CRC_BURST_CNT CRC Multiple Burst Count for Average Code Register.
11:9	RO	0x0	reserved
8	RW	0x0	CRC_CODE_FIX CRC Code Fix Control Register.
7:4	RW	0x0	CRC_CODE_TOL CRC Code Tolerance Control Register.
3:0	RW	0x0	CRC_CODE_TUNE CRC Code Tuning Register.

DCPHY_M0_COMBO_SD2_GNR_CON0

Address: Operational Base(0x2B020000) + offset (0x0E00)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(DPHY_S#D2_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_COMBO_SD2_GNR_CON1

Address: Operational Base(0x2B020000) + offset (0x0E04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(DPHY_S#D2_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_COMBO_SD2_ANA_CON0

Address: Operational Base(0x2B020000) + offset (0x0E08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	HS_RX_CNT_ROUT Output Resistor of HSRX AFE's 1st Stage Amp 3'b000: 282 Ohm 3'b001: 188 Ohm 3'b011: 141 Ohm 3'b100: 565 Ohm

DCPHY_M0_COMBO_SD2_ANA_CON1

Address: Operational Base(0x2B020000) + offset (0x0E0C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:11	RW	0x00	HS_RX_BIAS_CON [15]: Diff to CMOS Level shifter's current 1'b0: 550uA 1'b1: 650uA [14:13]: 2nd stage amp bias current 2'b00: 500uA 2'b01: 550uA 2'b10: 600uA 2'b11: 650uA [12:11]: 1st stage amp bias current 2'b00: 700uA 2'b01: 850uA 2'b10: 350uA 2'b11: 500uA
10	RO	0x0	reserved
9	RW	0x0	HS_RX_FLATBAND EQ On/Off Control Register. 1'b0: EQ off, 1'b1: EQ on
8	RO	0x0	reserved
7:4	RW	0x0	HS_RX_RSELCNT EQ Resistor Control Register. In case of DPHY 5'b00000: Forbidden (infinite resistance) 5b'00101: 200 Ohm 5b'00001: 300 Ohm 5b'00010: 400 Ohm 5b'10100: 480 Ohm 5b'00100: 600 Ohm 5b'11000: 800 Ohm In case of CPHY 5'b00000: Forbidden (infinite resistance) 5b'01111: 220 Ohm 5b'00110: 280 Ohm 5b'10010: 430 Ohm 5b'10100: 600 Ohm 5b'00100: 700 Ohm 5b'00001: 1300 Ohm
3:0	RW	0x0	HS_RX_CAPCNT EQ Capacitor Control (Covered Freq.) Register. ** MSB[3]: gain/freq control of 2nd amp In case of DPHY 4'b0000: 7.43GHz 4'b0001: 4.82GHz 4'b0010: 4.09GHz 4'b0011: 3.58GHz 4'b0100: 3.44GHz 4'b0101: 3.12GHz 4'b0110: 2.87GHz 4'b0111: 2.7GHz In case of CPHY 4'b0000: Small capacitance 4'b0001: Large capacitance HS_RX_CAPCNT[1:0]: Reserved

DCPHY_M0_COMBO_SD2_ANA_CON2

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Address: Operational Base(0x2B020000) + offset (0x0E10)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	SEL_FDLY Fine delay on/off control pin for skew cal, DPHY only. 0x0: Fine delay 0x1: Bypass
13:12	RW	0x0	UDLY_SPDCNT Fine delay selection for Skew cal, DPHY only. 2'b00: 4.89ps, 2'b10: 7.72ps
11	RW	0x0	HS_TERM_EN_MAN TERM_ENABLE, Only Test mode for DPHY
10	RW	0x0	HSMODE_MAN_SEL Only Test mode for DPHY, 1'b0: Normal, 1'b1: Test mode
9:8	RW	0x0	SKEW_DLYSEL Set the register as below. 4.0Gbps <= Data Rate <= 6.5Gbps: 2'b00 3.0Gbps <= Data Rate < 4.0Gbps: 2'b01 2.0Gbps <= Data Rate < 3.0Gbps: 2'b10 1.5Gbps <= Data Rate < 2.0Gbps: 2'b11 2'b00 for the rest.
7	RW	0x0	RXDDRCLKHS_SEL Clock selection pin for Data patch clock 0x0: CLK1 0x1: CLK2
6	RW	0x0	SKEW_CAL_EXT_FORCE Manual Skew Calibration control 0x0: Disable 0x1: Enable
5	RW	0x0	HS_UNTERM_EN Termination control pin for DPHY HS-RX, 1'b0: Term, 1'b1: Un-Term
4:3	RO	0x0	reserved
2:0	RW	0x0	RX_TERM_SW HS-RX Termination Impedance Control 3b'000: 102 Ohm 3b'001: 99.1 Ohm 3b'010: 96.6 Ohm (default) 3b'011: 94.1 Ohm 3b'100: 113 Ohm 3b'101: 110 Ohm 3b'110: 107 Ohm 3b'111: 104 Ohm

DCPHY_M0_COMBO_SD2_ANA_CON3

Address: Operational Base(0x2B020000) + offset (0x0E14)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	EN_RSTN_SEL Internal resetn sel. 0x0: Enabel_D2A 0x1: ResetN_D2A

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Bit	Attr	Reset Value	Description
14	RW	0x0	DPDN_SWAP DPDN swap, 1'b0: Normal 1'b1: Swap
13:12	RW	0x0	HS_DELAY_CON Clk delay control for loopback test at Clock lane 2'b00: 20pS 2'b01: 40pS 2'b10: 60pS 2'b11: 80pS
11	RW	0x0	SEL_ESCPOL LP ESCCLK Polarity sel 1'b0: Normal 1'b1: Swap
10:8	RW	0x0	ULPS_HYS_SW_DPHY ULPS Hysterisis Level Control 3'b000: 126mV 3'b001: 135mV 3'b010: 143mV 3'b011: 150mV 3'b100: 64.6mV 3'b101: 82.2mV 3'b110: 104mV 3'b111: 117mV
7	RW	0x0	CNT_REJECT_PULSE LP Pulse Reject Time Control 1b'0: Default 1b'1: Smaller Reject Time
6	RW	0x0	LP_EN_PRECHARGE_SEL LPRX Pre-charge Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
5:4	RW	0x0	LP_HYS_SW LP-RX Hysteresis Level Control 2'b00: 45mV 2'b01: 65mV 2'b10: 85mV 2'b11: 100mV
3	RW	0x0	PULSE_REJ_ENB Pulse Rejecter Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
2	RW	0x0	CULPS_HYS ulps vref sel, 1'b0: Self bias, 1'b1: From r-ladder
1:0	RW	0x0	LPRX_BIAS_CTRL Rx normal LP bias sel, 2'b00: 25uA 2'b01: 35uA 2'b10: 20uA 2'b11: 25uA

DCPHY_M0_COMBO_SD2_ANA_CON4

Address: Operational Base(0x2B020000) + offset (0x0E18)

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Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	REG05_11 Forcing HS-RX Mode Enable/Disable Control 0x0: Disable 0x1: Enable
10:0	RO	0x000	reserved

DCPHY_M0_COMBO_SD2_ANA_CON6

Address: Operational Base(0x2B020000) + offset (0x0E20)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	DL_COMP_CTRL UI mask code output control - sec control
7:6	RO	0x0	reserved
5:4	RW	0x0	UI_MASK_CTRL UI Mask control - sec control
3	RW	0x0	EXT_DL_MUX_EN 1UI data sampling type - sec control
2:0	RO	0x0	reserved

DCPHY_M0_COMBO_SD2_ANA_CON7

Address: Operational Base(0x2B020000) + offset (0x0E24)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	CLK_DBL_CTRL XI to doubler clock delay cotrol - sec control
5:0	RO	0x00	reserved

DCPHY_M0_COMBO_SD2_TIME_CON0

Address: Operational Base(0x2B020000) + offset (0x0E30)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	SETTLE_CLK_SEL Settle Counter Clock Select Register. Settle Clock is used for counting TCLK-SETTLE. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
7:0	RW	0x00	T_HS_SETTLE TSETTLE Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" of mipi alliance. And please refer to "Supplement Guide" for setting this register according to data rate.

DCPHY_M0_COMBO_SD2_TIME_CON1

Address: Operational Base(0x2B020000) + offset (0x0E34)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	T_ERR_SOT_SYNC SoT Sync Error Detect Timing Control Register. This count value is used in High-Speed Transmit operation. There is a watchdog timer in Receive logic for detecting SoT Sync Error. If the Sync Pattern is not detected until the watchdog timer is expired, then the PPI signal "ERRSOTSYNC" goes to HIGH.

DCPHY_M0_COMBO_SD2_DATA_CON0

Address: Operational Base(0x2B020000) + offset (0x0E38)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SYMBOL_SWAP Symbol Swap Control Register. When this register is set to HIGH, 7-symbol data will be swapped.
3:2	RO	0x0	reserved
1	RW	0x0	DATA_INV Data Inversion Control Register. When this register is set to HIGH, the data input of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data output will be swapped.

DCPHY_M0_COMBO_SD2_DESKEW_CON0

Address: Operational Base(0x2B020000) + offset (0x0E40)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SKEW_CAL_DES_SEL Skew Calibration Clock Division Ratio Control Register.
3:1	RO	0x0	reserved
0	RW	0x0	SKEW_CAL_EN Skew Calibration Enable Register.

DCPHY_M0_COMBO_SD2_DESKEW_CON1

Address: Operational Base(0x2B020000) + offset (0x0E44)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	SKEW_CAL_FINAL_COMP_TIME Skew Calibration Final Compare Time Control Register.
7:6	RW	0x0	SKEW_CAL_COMP_TOL Skew Calibration Compare Tolerance Control Register.
5:4	RW	0x0	SKEW_CAL_COMP_WAIT_TIME Skew Calibration Compare Wait Time Control Register.
3:0	RW	0x0	SKEW_CAL_COMP_RUN_TIME Skew Calibration Compare Run Time Control Register.

DCPHY_M0_COMBO_SD2_DESKEW_CON2

Address: Operational Base(0x2B020000) + offset (0x0E48)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	SKEW_CAL_DATA_COARSE_SET Skew Calibration Manual Data Coarse Delay Control Register.
7:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	SKEW_CAL_CLK_COARSE_SET Skew Calibration Manual Data Fine Delay Control Register.

DCPHY_M0_COMBO_SD2_DESKEW_CON3

Address: Operational Base(0x2B020000) + offset (0x0E4C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	SKEW_CAL_DATA_FINE_FALL_SET Skew Calibration Manual Data Fine Falling Delay Control Register.
11:8	RW	0x0	SKEW_CAL_DATA_FINE_RISE_SET Skew Calibration Manual Data Fine Rising Delay Control Register.
7:4	RW	0x0	SKEW_CAL_CLK_FINE_FALL_SET Skew Calibration Manual Clock Fine Falling Delay Control Register.
3:0	RW	0x0	SKEW_CAL_CLK_FINE_RISE_SET Skew Calibration Manual Clock Fine Rising Delay Control Register.

DCPHY_M0_COMBO_SD2_DESKEW_CON4

Address: Operational Base(0x2B020000) + offset (0x0E50)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	SKEW_CAL_FINE_MAX_SET Skew Calibration Maximum Fine Delay Step Control Register.
7:5	RO	0x0	reserved
4:0	RW	0x00	SKEW_CAL_COARSE_MAX_SET Skew Calibration Maximum Coarse Delay Step Control Register.

DCPHY_M0_COMBO_SD2_CRC_CON0

Address: Operational Base(0x2B020000) + offset (0x0E60)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:4	RW	0x00	CRC_FORCE_CODE CRC Forcing Mode Code Control Register.
3:1	RO	0x0	reserved
0	RW	0x0	CRC_FORCE_CODE_EN CRC Forcing Mode Enable Register.

DCPHY_M0_COMBO_SD2_CRC_CON1

Address: Operational Base(0x2B020000) + offset (0x0E64)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	CRC_POST_GATING_CNT CRC Post Gating Count Register.
7	RW	0x0	CRC_POST_GATING_EN CRC Post Gating Enable Register.
6:4	RW	0x0	CRC_SETTLE_MASK_SEL CRC Clock Polarity Control Register.
3	RW	0x0	CRC_POL_SEL CRC Clock Polarity Control Register.
2	RW	0x0	CRC_SOT_SYNC_ERR_CHK CRC SoT Sync Error Check Enable Register.
1:0	RW	0x0	CRC_AVG_SEL CRC Code Average Select Register.

DCPHY_M0_COMBO_SD2_CRC_CON2

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Address: Operational Base(0x2B020000) + offset (0x0E68)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	CRC_BURST_CNT CRC Multiple Burst Count for Average Code Register.
11:9	RO	0x0	reserved
8	RW	0x0	CRC_CODE_FIX CRC Code Fix Control Register.
7:4	RW	0x0	CRC_CODE_TOL CRC Code Tolerance Control Register.
3:0	RW	0x0	CRC_CODE_TUNE CRC Code Tuning Register.

DCPHY_M0_DPHY_SD3_GNR_CON0

Address: Operational Base(0x2B020000) + offset (0x0F00)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(DPHY_S#D3_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_DPHY_SD3_GNR_CON1

Address: Operational Base(0x2B020000) + offset (0x0F04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(DPHY_S#D3_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_DPHY_SD3_ANA_CON0

Address: Operational Base(0x2B020000) + offset (0x0F08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	HS_RX_CNT_ROUT Output Resistor of HSRX AFE's 1st Stage Amp 3'b000: 282 Ohm 3'b001: 188 Ohm 3'b011: 141 Ohm 3'b100: 565 Ohm

DCPHY_M0_DPHY_SD3_ANA_CON1

Address: Operational Base(0x2B020000) + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:11	RW	0x00	HS_RX_BIAS_CON [15]: Diff to CMOS Level shifter's current 1'b0: 550uA 1'b1: 650uA [14:13]: 2nd stage amp bias current 2'b00: 500uA 2'b01: 550uA 2'b10: 600uA 2'b11: 650uA [12:11]: 1st stage amp bias current 2'b00: 700uA 2'b01: 850uA 2'b10: 350uA 2'b11: 500uA
10	RO	0x0	reserved
9	RW	0x0	HS_RX_FLATBAND EQ On/Off Control Register. 1'b0: EQ off, 1'b1: EQ on
8	RO	0x0	reserved
7:4	RW	0x0	HS_RX_RSELCNT EQ Resistor Control Register. 5'b00000: Forbidden (infinite resistance) 5b'00001: 330 Ohm 5b'00100: 660 Ohm 5b'01000: 1.3k Ohm 5b'01100: 440 Ohm 5b'01111: 130 Ohm (min) 5b'10000: 2.6k Ohm (max) 5b'10100: 530 Ohm 5b'10101: 200 Ohm 24d~31d: Forbidden
3:0	RW	0x0	HS_RX_CAPCNT EQ Capacitor Control (Covered Freq.) Register. 4'b0000: 7.43GHz 4'b0001: 4.82GHz 4'b0010: 4.09GHz 4'b0011: 3.58GHz 4'b0100: 3.44GHz 4'b0101: 3.12GHz 4'b0110: 2.87GHz 4'b0111: 2.7GHz ** MSB[2]: gain/freq control of 2nd amp

DCPHY_M0_DPHY_SD3_ANA_CON2

Address: Operational Base(0x2B020000) + offset (0x0F10)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	RESETN_CFG_SEL Reset Selection Register for 2+2 Configuration 1'b0: 4-Lane 1'b1: 2+2 Lane
14	RW	0x0	SEL_FDLY Fine delay on/off control pin for skew cal 0x0: Fine delay 0x1: Bypass

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	UDLY_SPDCNT Fine delay selection for Skew cal, 2'b00: 4.89ps, 2'b10: 7.72ps
11	RW	0x0	HS_TERM_EN_MAN TERM_ENABLE, Only Test mode for DPHY
10	RW	0x0	HSMODE_MAN_SEL Only Test mode for DPHY, 1'b0: Normal, 1'b1: Test mode
9:8	RW	0x0	SKEW_DLYSEL Set the register as below. 4.0Gbps <: Data Rate <: 6.5Gbps: 2'b00 3.0Gbps <: Data Rate < 4.0Gbps: 2'b01 2.0Gbps <: Data Rate < 3.0Gbps: 2'b10 1.5Gbps <: Data Rate < 2.0Gbps: 2'b11 2'b00 for the rest.
7	RW	0x0	RXDDRCLKHS_SEL Clock selection pin for Data patch clock 0x0: CLK1 0x1: CLK2
6	RW	0x0	SKEW_CAL_EXT_FORCE Manual Skew Calibration control 0x0: Disable 0x1: Enable
5	RW	0x0	HS_UNTERM_EN Termination control pin for DPHY HS-RX, 1'b0: Term, 1'b1: Un-Term
4:3	RO	0x0	reserved
2:0	RW	0x0	RX_TERM_SW HS-RX Termination Impedance Control 3b'000: 102 Ohm 3b'001: 99.1 Ohm 3b'010: 96.6 Ohm (default) 3b'011: 94.1 Ohm 3b'100: 113 Ohm 3b'101: 110 Ohm 3b'110: 107 Ohm 3b'111: 104 Ohm

DCPHY_M0_DPHY_SD3_ANA_CON3

Address: Operational Base(0x2B020000) + offset (0x0F14)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	EN_RSTN_SEL internal resetn sel. 0x0: Enabel_D2A 0x1: ResetN_D2A
14	RW	0x0	DPDN_SWAP DPDN swap, 1'b0: Normal, 1'b1: Swap

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	HS_DELAY_CON Clk delay control for loopback test at Clock lane 2'b00: 20pS 2'b01: 40pS 2'b10: 60pS 2'b11: 80pS
11	RW	0x0	SEL_ESCPOL LP ESCCLK Polarity sel 1'b0: Normal, 1'b1: Swap
10:8	RW	0x0	ULPS_HYS_SW_DPHY ULPS Hysterisis Level Control 3'b000: 126mV 3'b001: 135mV 3'b010: 143mV 3'b011: 150mV 3'b100: 64.6mV 3'b101: 82.2mV 3'b110: 104mV 3'b111: 117mV
7	RW	0x0	CNT_REJECT_PULSE LP Pulse Reject Time Control 1b'0: Default 1b'1: Smaller Reject Time
6	RW	0x0	LP_EN_PRECHARGE_SEL LPRX Pre-charge Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
5:4	RW	0x0	LP_HYS_SW LP-RX Hysteresis Level Control 2'b00: 45mV 2'b01: 65mV 2'b10: 85mV 2'b11: 100mV
3	RW	0x0	PULSE_REJ_ENB Pulse Rejecter Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
2	RW	0x0	CULPS_HYS ulps vref sel, 1'b0: Self bias, 1'b1: From r-ladder
1:0	RW	0x0	LPRX_BIAS_CTRL rx normal LP bias sel, 2'b00: 25uA 2'b01: 35uA 2'b10: 20uA 2'b11: 25uA

DCPHY_M0_DPHY_SD3_ANA_CON4

Address: Operational Base(0x2B020000) + offset (0x0F18)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x0	REG05_11 Forcing HS-RX Mode Enable/Disable Control 0x0: Disable 0x1: Enable
10:6	RO	0x00	reserved
5:4	RW	0x0	ATB_SEL_POWER_IR ULPS reference voltage option selection
3:0	RW	0x0	ATB_SEL_DMY ATB Enable, 1'b0: Switch off, 1'b1: Switch on(AVSS, AVSS, AVDDL, AVSS)

DCPHY_M0_DPHY_SD3_ANA_CON5

Address: Operational Base(0x2B020000) + offset (0x0F1C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	DESER_DELAY_ENABLE 1'b0 : Deserializer enable delay off 1'b1 : Deserializer enable delay on
11	RW	0x0	NON_MIPI_ENABLE 1'b0 : Non mipi feature disable 1'b1 : Non mipi feature enable
10:0	RO	0x000	reserved

DCPHY_M0_DPHY_SD3_TIME_CON0

Address: Operational Base(0x2B020000) + offset (0x0F30)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	SETTLE_CLK_SEL Settle Counter Clock Select Register. Settle Clock is used for counting TCLK-SETTLE. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
7:0	RW	0x00	T_HS_SETTLE TSETTLE Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" of mipi alliance. And please refer to "Supplement Guide" for setting this register according to data rate.

DCPHY_M0_DPHY_SD3_TIME_CON1

Address: Operational Base(0x2B020000) + offset (0x0F34)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	T_ERR_SOT_SYNC SoT Sync Error Detect Timing Control Register. This count value is used in High-Speed Transmit operation. There is a watchdog timer in Receive logic for detecting SoT Sync Error. If the Sync Pattern is not detected until the watchdog timer is expired, then the PPI signal "ERRSOTSYNC" goes to HIGH.

DCPHY_M0_DPHY_SD3_DATA_CON0

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Address: Operational Base(0x2B020000) + offset (0x0F38)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	DATA_INV Data Inversion Control Register. When this register is set to HIGH, the data input of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data output will be swapped.

DCPHY_M0_DPHY_SD3_DESKEW_CON0

Address: Operational Base(0x2B020000) + offset (0x0F40)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SKEW_CAL_DES_SEL Skew Calibration Clock Division Ratio Control Register.
3:1	RO	0x0	reserved
0	RW	0x0	SKEW_CAL_EN Skew Calibration Enable Register.

DCPHY_M0_DPHY_SD3_DESKEW_CON1

Address: Operational Base(0x2B020000) + offset (0x0F44)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	SKEW_CAL_FINAL_COMP_TIME Skew Calibration Final Compare Time Control Register.
7:6	RW	0x0	SKEW_CAL_COMP_TOL Skew Calibration Compare Tolerance Control Register.
5:4	RW	0x0	SKEW_CAL_COMP_WAIT_TIME Skew Calibration Compare Wait Time Control Register.
3:0	RW	0x0	SKEW_CAL_COMP_RUN_TIME Skew Calibration Compare Run Time Control Register.

DCPHY_M0_DPHY_SD3_DESKEW_CON2

Address: Operational Base(0x2B020000) + offset (0x0F48)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	SKEW_CAL_DATA_COARSE_SET Skew Calibration Manual Data Coarse Delay Control Register.
7:5	RO	0x0	reserved
4:0	RW	0x00	SKEW_CAL_CLK_COARSE_SET Skew Calibration Manual Data Fine Delay Control Register.

DCPHY_M0_DPHY_SD3_DESKEW_CON3

Address: Operational Base(0x2B020000) + offset (0x0F4C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	SKEW_CAL_DATA_FINE_FALL_SET Skew Calibration Manual Data Fine Falling Delay Control Register.
11:8	RW	0x0	SKEW_CAL_DATA_FINE_RISE_SET Skew Calibration Manual Data Fine Rising Delay Control Register.
7:4	RW	0x0	SKEW_CAL_CLK_FINE_FALL_SET Skew Calibration Manual Clock Fine Falling Delay Control Register.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	SKEW_CAL_CLK_FINE_RISE_SET Skew Calibration Manual Clock Fine Rising Delay Control Register.

DCPHY_M0_DPHY_SD3_DESKEW_CON4

Address: Operational Base(0x2B020000) + offset (0x0F50)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	SKEW_CAL_FINE_MAX_SET Skew Calibration Maximum Fine Delay Step Control Register.
7:5	RO	0x0	reserved
4:0	RW	0x00	SKEW_CAL_COARSE_MAX_SET Skew Calibration Maximum Coarse Delay Step Control Register.

21.5 Interface Description

Table 21-1 MIPI DCPHY Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
MS_VDD0P85	I/O	MIPI_DCPHY_AVDD	N/A
MS_VDD18	I/O	MIPI_DCPHY_AVDD1V8	N/A
M_VDD12	I/O	MIPI_DCPHY_AVDD1V2	N/A
M_VREG_0P4V	I/O	MIPI_D/C_PHY0_VREG	N/A
M_DNCLK_B1	I/O	MIPI_DPHY_DSI_TX_CLKN/MIPI_CPHY_DSI_TX_TRIO1_B	N/A
M_DNDATA0_A0	I/O	MIPI_DPHY_DSI_TX_D0N/MIPI_CPHY_DSI_TX_TRIO0_A	N/A
M_DNDATA1_C0	I/O	MIPI_DPHY_DSI_TX_D1N/MIPI_CPHY_DSI_TX_TRIO0_C	N/A
M_DNDATA2_A2	I/O	MIPI_DPHY_DSI_TX_D2N/MIPI_CPHY_DSI_TX_TRIO2_A	N/A
M_DNDATA3_C2	I/O	MIPI_DPHY_DSI_TX_D3N/MIPI_CPHY_DSI_TX_TRIO2_C	N/A
M_DPCLK_C1	I/O	MIPI_DPHY_DSI_TX_CLKP/MIPI_CPHY_DSI_TX_TRIO1_C	N/A
M_DPDATA0_B0	I/O	MIPI_DPHY_DSI_TX_D0P/MIPI_CPHY_DSI_TX_TRIO0_B	N/A
M_DPDATA1_A1	I/O	MIPI_DPHY_DSI_TX_D1P/MIPI_CPHY_DSI_TX_TRIO1_A	N/A
M_DPDATA2_B2	I/O	MIPI_DPHY_DSI_TX_D2P/MIPI_CPHY_DSI_TX_TRIO2_B	N/A
M_DPDATA3	I/O	MIPI_DPHY_DSI_TX_D3P/NO_USE	N/A
S_DNCLK_B1	I/O	MIPI_DPHY_CSI0_RX_CLKN/MIPI_CPHY_CSI_RX_TRIO1_B	N/A
S_DNDATA0_A0	I/O	MIPI_DPHY_CSI0_RX_D0N/MIPI_CPHY_CSI_RX_TRIO0_A	N/A
S_DNDATA1_C0	I/O	MIPI_DPHY_CSI0_RX_D1N/MIPI_CPHY_CSI_RX_TRIO0_C	N/A
S_DNDATA2_A2	I/O	MIPI_DPHY_CSI0_RX_D2N/MIPI_CPHY_CSI_RX_TRIO2_A	N/A
S_DNDATA3_C2	I/O	MIPI_DPHY_CSI0_RX_D3N/MIPI_CPHY_CSI_RX_TRIO2_C	N/A
S_DPCLK_C1	I/O	MIPI_DPHY_CSI0_RX_CLKP/MIPI_CPHY_CSI_RX_TRIO1_C	N/A
S_DPDATA0_B0	I/O	MIPI_DPHY_CSI0_RX_D0P/MIPI_CPHY_CSI_RX_	N/A

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Module Pin	Dir	Pad Name	IOMUX Setting
		TRIO0_B	
S_DPDATA1_A1	I/O	MIPI_DPHY_CSI0_RX_D1P/MIPI_CPHY_CSI_RX_TRIO1_A	N/A
S_DPDATA2_B2	I/O	MIPI_DPHY_CSI0_RX_D2P/MIPI_CPHY_CSI_RX_TRIO2_B	N/A
S_DPDATA3	I/O	MIPI_DPHY_CSI0_RX_D3P/NO_USE	N/A

Notes: I=input, O=output, I/O=input/output, bidirectional

21.6 Application Notes

21.6.1 System-level Interaction

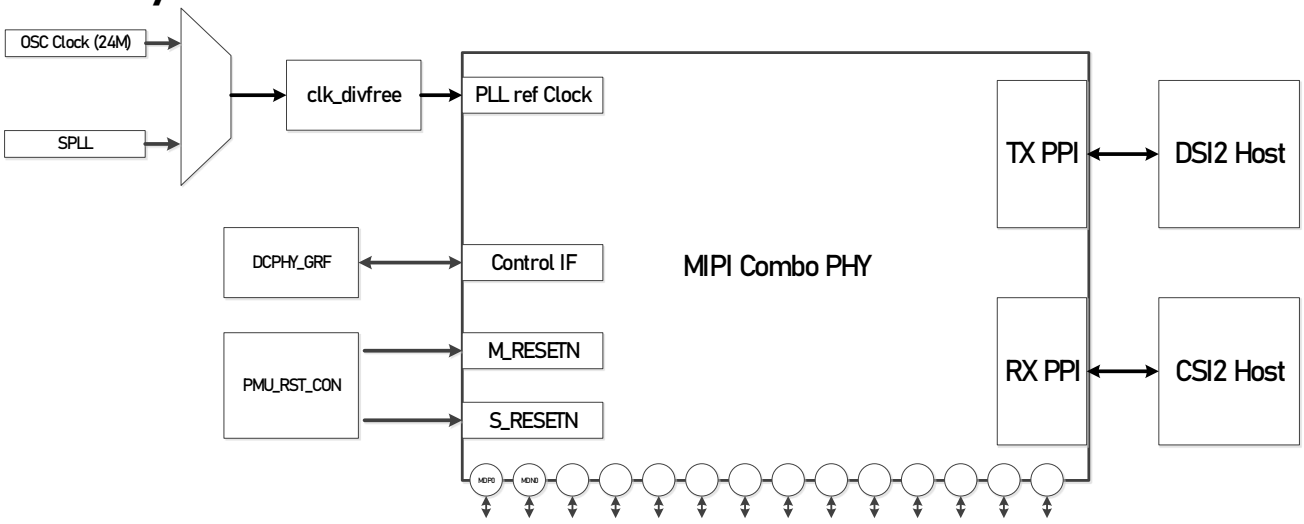


Fig. 21-6 DCPHY System Level Interaction

21.6.1.1 Clock

- **pll_ref_clk**: MIPI DCPHY PLL reference clock could be configured to choose the source from external oscillator 24Mhz clock or system PLL clock. The default setting is oscillator 24Mhz clock for clock quality consideration.

21.6.1.2 Reset

- **M_RESETN**: reset to PLL block, TX Clock lane block and data lane 0/1/2/3 block.
- **S_RESETN**: reset to RX Clock lane block and data lane 0/1/2/3 block.

M_RESETN and S_RESETN are programmed in *PMU1CRU_SOFTRST_CON01 register.*

21.6.1.3 AMBA APB 3 Interface

MIPI D-PHY/C-PHY combo PHY has internal registers to control the PHY itself and to debug. These internal registers are accessible through the APB interface, and each register is a maximum of 16bits wide. The APB slave in the PHY is completely compatible with AMBA 3.0 APB specification.

Table 21-2 DCPHY APB Base Address

IP	Base Address
DCPHY	0x2B020000

21.6.1.4 System Control Signals

MIPI DCPHY mode and some debug status are interacted with their corresponding GRF.

Table 21-3 DCPHY GRF Base Address

IP	Base Address
DCPHY_GRF	0x26034000

M/S_CPHY_MODE: D-PHY / C-PHY mode select signal of bias / DTB / PLL / TX / RX block.

21.6.2 PLL Programmability

PLL in MIPI DCPHY is a 1.8V/0.75V dual supply-voltage phase locked loop (PLL) with a wide-output-frequency-range for frequency synthesis. It consists of a phase frequency detector (PFD), a charge pump, a voltage-controlled oscillator (VCO), a 6-bit predivider, a

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10-bit main-divider, a 3-bit scaler, a delta-sigma modulator (DSM) and an automatic frequency control (AFC).
The output frequency (Fout) is related to the input frequency (Fin) using the following equation.

$$Fvco = \frac{((M + \frac{K}{65536}) \times 2 \times Fin)}{P}$$

$$Fout = \frac{((M + \frac{K}{65536}) \times 2 \times Fin)}{(P \times 2^{s})}$$

where p, m, s, and k are the division values in decimal numbers for pre-divider, main-divider, scaler, and DSM, respectively.
Frequency of VCO's output: 2600MHz ⩽ F_{vco} ⩽ 6600MHz
P[5:0], M[9:0] and S[2:0] are unsigned integers. K[15:0] is a two's complement integer.

- 6'b000001 ⩽ P[5:0] ⩽ 6'b11 1111 and 6MHz ⩽ FFREF(FFIN / p) ⩽ 30MHz
- 10'b00_0100_0000 ⩽ M[9:0] ⩽ 10'b11_1111_1111
- 3'b000 ⩽ S[2:0] ⩽ 3'b110
- 16'b1000_0000_0000_0000 ⩽ K[15:0] ⩽ 16'b0111_1111_1111_1111

21.6.3 Start-up Sequence

The below figure illustrates the initialization sequence.

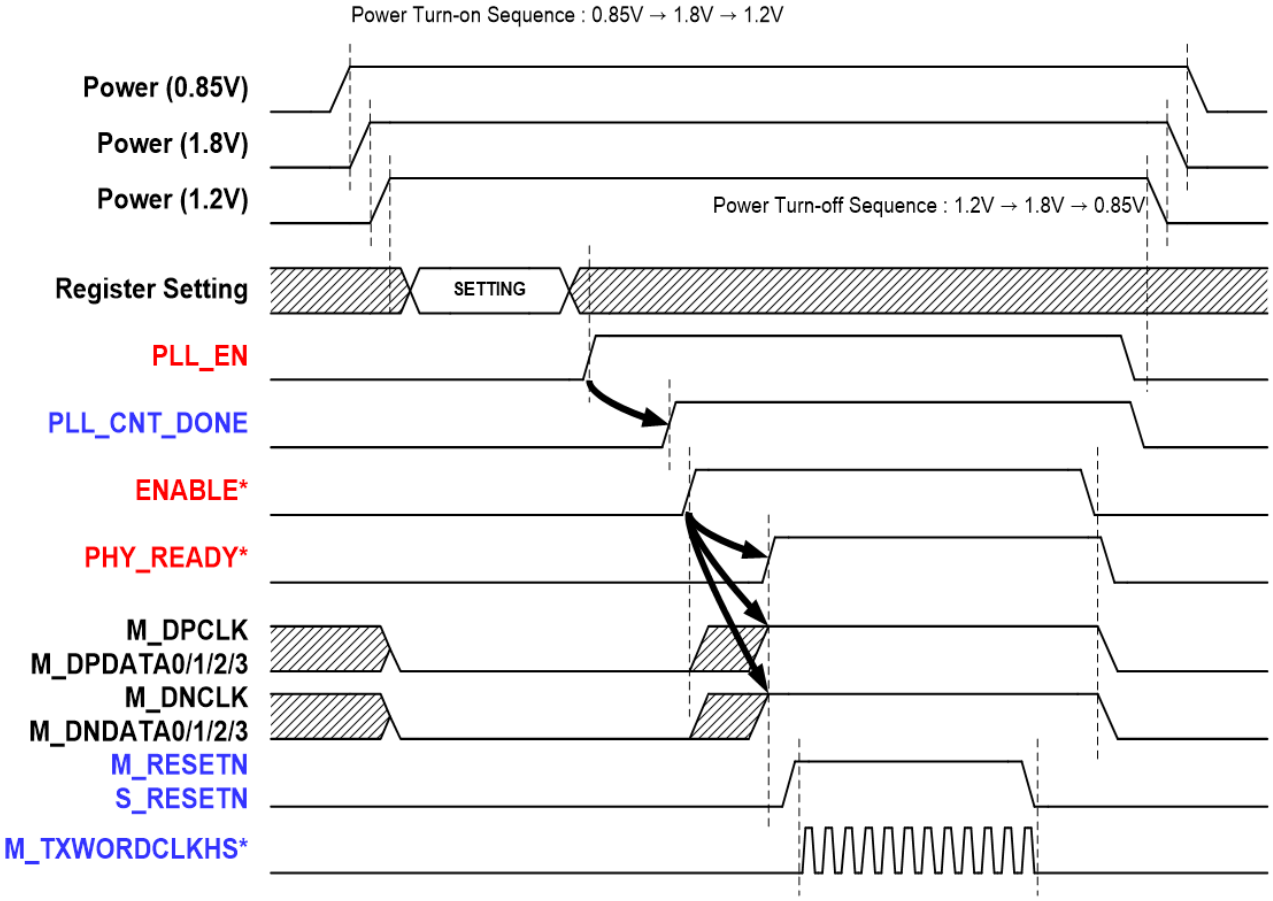


Fig. 21-7 DCPHY Start Up Sequence

(1) Turn the powers on by the sequence according to the initialization sequence figure. After power sequence is done, drivers in PHY are stabilized and DP/DN pad outputs of each Lane become LP-00 state.
(2) Set the special function registers through APB interface including the registers of PLL. DO NOT set PLL_EN and ENABLE register in this time.
   - PLL_EN: PLL_CON0[12]
   - ENABLE: DPHY_M0C_GNR_CON0[0] / DPHY_M0D#_GNR_CON0[0] / COMBO_M0D#_GNR_CON[0] / DPHY_S0C_GNR_CON0[0] /

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DPHY_S0D#_GNR_CON0[0] / COMBO_S0D#_GNR_CON[0]

(3) Enable PLL by set PLL_EN register to HIGH. If Slave Lanes are only used, then PLL sequence can be skipped at the real set.

(4) When PLL_EN is set to HIGH, PLL lock counter is started for getting stabilized clock. The lock counter is expired when the count value is reached to the value set as REG_PLL_LOCK_CNT (PLL_CON7[15:0]). And then, the interface signal PLL_CNT_DONE is asserted.

(5) Through ENABLE registers, the Lanes are enabled (# = 0/1/2/3).
- ENABLE: DPHY_M0C_GNR_CON0[0] / DPHY_M0D#_GNR_CON0[0] / COMBO_M0D#_GNR_CON[0] / DPHY_S0C_GNR_CON0[0] / DPHY_S0D#_GNR_CON0[0] / COMBO_S0D#_GNR_CON[0]

(6) When ENABLE is set to HIGH, the circuits need 200us for initializing Low-Power regulator and stabilizing bias block. For this, there are PHY ready counter in each Lanes. The counter is expired when the count value is reached to the value set as T_PHY_READY (GNR_CON1[15:0]). And then, PHY_READY (GNR_CON0[1]) register is set to HIGH.
- T_PHY_READY : DPHY_M0C_GNR_CON1[15:0] / DPHY_M0D#_GNR_CON1[15:0] / COMBO_M0D#_GNR_CON1[15:0] / DPHY_S0C_GNR_CON1[15:0] / DPHY_S0D#_GNR_CON1[15:0] / COMBO_S0D#_GNR_CON1[15:0]
- PHY_READY: DPHY_M0C_GNR_CON0[1] / DPHY_M0D#_GNR_CON0[1] / COMBO_M0D#_GNR_CON0[1] / DPHY_S0C_GNR_CON0[1] / DPHY_S0D#_GNR_CON0[1] / COMBO_S0D#_GNR_CON0[1]

(7) After PHY_READY is set to HIGH, the pad outputs DP/DN are stabilized to LP-11 state.

(8) After all of PHY_READY of each Lane, user can release reset of PHY "M_RESETN" or "S_RESETN".

(9) M_TXWORDCLKHS* are toggled after releasing the reset.

21.6.4 Configuration examples

21.6.4.1 **Case 1** (TX operate at 2.5Gbps DPHY Mode, Ref_Clk = 24Mhz)

Configuration Sequence:

① set PMU1CRU_SOFTRST_CON01[3] = 1 to assert M_RESETN

② set BIAS block
- BIAS_CON0 = 0x0010
- BIAS_CON1 = 0x0110
- BIAS_CON2 = 0x3223

③ set TX PLL
- PLL_CON0 = 0x0101 (P = 1, S = 1)
- PLL_CON1 = 0x2762 (K = 0x2762)
- PLL_CON2 = 0x0068 (M = 0x68)

④ set TX clock lane
1) set MC_GNR_CON0 = 0xf000
2) set MC_ANA_CON0 = 0x7133
3) set MC_ANA_CON1 = 0x0001
4) set timing parameters through MC_TIME_CON0/MC_TIME_CON1/MC_TIME_CON2/MC_TIME_CON3 refer to the Supplement Guide Timing Table.
5) set DPHY_MC_DESKEW_CON0 = 0x9cb1 to enable deskew calibration function.

⑤ set TX data lane (* = 0,1,2,3)
1) set COMBO_MD*_GNR_CON1 = 0x2000
2) set COMBO_MD*_ANA_CON0 = 0x7133
3) set COMBO_MD*_ANA_CON0 = 0x0001
4) set timing parameters through COMBO_MD*_TIME_CON0/COMBO_MD*_TIME_CON1/COMBO_MD*_TIME_CON2/COMBO_MD*_TIME_CON3/COMBO_MD*_TIME_CON4 refer to the Supplement Guide Timing Table.

⑥ set PLL_EN = 1(PLL_CON0[0])

⑦ wait PLL is locked (read the PLL_STAT0[0])

⑧ set

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DPHY_MC_GNR_CON0[0]/COMBO_MD0_GNR_CON0[0]/COMBO_MD1_GNR_CON0[0]/COMBO_MD2_GNR_CON0[0]/COMBO_MD3_GNR_CON0[0] = 0x1 to enable lanes.

⑨ wait clock lane and data lanes' PHY_READY (GNR_CON0[1]) register is set to HIGH

⑩ set PMU1CRU_SOFTRST_CON01[3] = 0 to deassert M_RESETN

21.6.4.2 **Case 2** (TX operate at 1.5Gbps CPHY Mode, Ref_Clk = 24Mhz)

Configuration Sequence:

① set MIPI_DCPHY_GRF_CON0 = 0x9 (M_CPHY_MODE = 1)

② set PMU1CRU_SOFTRST_CON01[3] = 1 to assert M_RESETN

③ set BIAS block
- BIAS_CON0 = 0x0010
- BIAS_CON1 = 0x0110
- BIAS_CON2 = 0x3223
- BIAS_CON4.I_MUX_SEL = 0x2
- DPHY_MC_ANA_CON2.HS_VREG_AMP_ICON = 0x2

④ set TX PLL
- PLL_CON0 = 0x0103 (P = 3, S = 1)
- PLL_CON1 = 0x8000 (K = 32767)
- PLL_CON2 = 0x00BB (M = 0xBB)

⑤ set TX data lane (* = 0,1,2)
1) set COMBO_MD*_GNR_CON1 = 0x2000
2) set timing parameters through COMBO_MD*_TIME_CON0/COMBO_MD*_TIME_CON1/COMBO_MD*_TIME_CON2/COMBO_MD*_TIME_CON3/COMBO_MD*_TIME_CON4 refer to the Supplement Guide Timing Table.

⑥ set PLL_EN = 1 (PLL_CON0[0])

⑦ wait PLL is locked (read the PLL_STAT0[0])

⑧ set COMBO_MD0_GNR_CON0[0]/COMBO_MD1_GNR_CON0[0]/COMBO_MD2_GNR_CON0[0] = 0x1 to enable lanes.

⑨ wait data lanes' PHY_READY (GNR_CON0[1]) register is set to HIGH

⑩ set PMU1CRU_SOFTRST_CON01[3] = 0 to deassert M_RESETN

21.6.4.3 **Case 3** (RX operate at 2.5Gbps DPHY Mode)

Configuration Sequence:

① set PMU1CRU_SOFTRST_CON01[4] = 1 to assert S_RESETN

② set BIAS block
set BIAS_CON0 = 0x0010
set BIAS_CON1 = 0x0110
set BIAS_CON2 = 0x3223

③ set RX clock/data lane ANA control parameter
set SC_ANA_CON1 = 0x8000
set SC_ANA_CON2 = 0x2
set SC_ANA_CON3 = 0x600

set SD*_ANA_CON1 = 0x8000
set SD*_ANA_CON2 = 0x202
set SD*_ANA_CON3 = 0x600
set SD*_ANA_CON7 = 0x40

④ set RX clock/data lane ready timing parameter
set SC_GNR_CON1 = 0x12c0
set SD*_GNR_CON1 = 0x12c0

⑤ set RX clock lane timing parameter
set SC_TIME_CON0 = 0x301.

⑥ set RX data lane timing parameter (refer to the Supplement Guide Timing Table)
set SD*_TIME_CON0 = 0xd.
set SD*_TIME_CON1 = 0x3.

⑦ set RX data lane deskew control parameter

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set SD*_DESKEW_CON0 = 0x1
set SD*_DESKEW_CON4 = 0x81a

⑧ set RX clock/data lane enable
set SC_GNR_CON0 = 0x1

set SD*_GNR_CON0 = 0x1

⑨ wait clock lane and data lanes' PHY_READY (SD*_GNR_CON0[1]) register is set to HIGH

⑩ set PMU1CRU_SOFTRST_CON01[4] = 0 to deassert S_RESETN

21.6.4.4 **Case 4** (RX operate at 2.5Gsps CPHY Mode)

Configuration Sequence:

① set MIPI_DCPHY_GRF_CON0 = 0x9 (CPHY_MODE = 1)
② set PMU1CRU_SOFTRST_CON01[4] = 1 to assert S_RESETN
③ set BIAS block
set BIAS_CON0 = 0x0010
set BIAS_CON1 = 0x0110
set BIAS_CON2 = 0x3223
set BIAS_CON4 = 0x40
④ set RX data lane ANA control parameter
set SD*_ANA_CON1 = 0x8000
set SD*_ANA_CON2 = 0x5
set SD*_ANA_CON3 = 0x600
set SD*_ANA_CON6 = 0x608
set SD*_ANA_CON7 = 0x40
⑤ set RX data lane ready timing parameter
set SD*_GNR_CON1 = 0x12c0
⑥ set RX data lane timing parameter (refer to the Supplement Guide Timing Table)
set SD*_TIME_CON0 = 0x1.
set SD*_TIME_CON1 = 0x32.
⑦ set RX data lane crc control parameter
set SD*_CRC_CON1 = 0x1500
set SD*_CRC_CON2 = 0x30
⑧ set RX data lane enable
set SD*_GNR_CON0 = 0x1
⑨ wait data lanes' PHY_READY (SD*_GNR_CON0[1]) register is set to HIGH
⑩ set PMU1CRU_SOFTRST_CON04[4] = 0 to deassert S_RESETN

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Chapter 22 DisplayPort Transmitter Controller (DPTX)

22.1 Overview

The DisplayPort Transmitter Controller (DPTX), which provides support for next generation video display interface technology. The Video Electronics Standards Association (VESA) defines the DisplayPort standard as an open digital communications interface for use in internal as well as external connections, such as:

- Interfaces within a PC or monitor (internal)
- External display connections, including interfaces between a PC and monitor or projector, between a PC and TV, or between a device such as a DVD player and TV display.

DPTX is compliant with the DisplayPort Specification Version 1.4 and supports both HDCP 1.3 and HDCP 2.2 standards. The DPTX digital controller interfaces with the DisplayPort/USB Type-C combo PHY, enabling the integration of a complete DisplayPort Interface in a USB Type-C environment.

22.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

DPTX supports the following features:

- General Features
  - DisplayPort 1.4
  - Main Link: 1/2/4 lanes
  - Main Link: RBR/HBR/HBR2/HBR3
  - 1Mbps AUX channel
  - Single Stream Transport (SST)
  - Multistream Transport (MST)
  - Type-C support (alternate mode)
  - HDCP 2.2, HDCP 1.3
  - Dual Pixel Mode
  - YCrCb (3 formats), RGB support
  - Up to 48 bits per pixel
  - Support for Register based SDP (Secondary Data Packets)
  - Native AUX, I2C over AUX
  - AMBA APB Interface for internal register access and AUX access
- Video-Related Features
  - Video formats
    - CEA-861-F
    - VESA DMT
    - VESA CVT
  - Colorimetry
    - Supports up to 8/10 bits per color component
    - Supports RGB, YCbCr4:4:4, YCbCr4:2:2, YCbCr4:2:0
- Audio-Related Features
  - Up to 192 KHz, 24 bits per sample LPCM
  - Up to 8 audio channels
  - I2S, S/PDIF interface supported
  - High Bit-Rate audio @768 KHz
- DPTX are not support the following features:
  - DSC(Display Stream Compression)
  - Dual Mode Support
- Requirement of interface video timing
  - Suggest follow CTA-861 standard
  - When the video timing is not standard, the min value of HSYNC/HBP/HFP is 16 pixel

22.3 Function Description

22.3.1 Architecture Overview

The figure below shows the architecture overview of DPTX.

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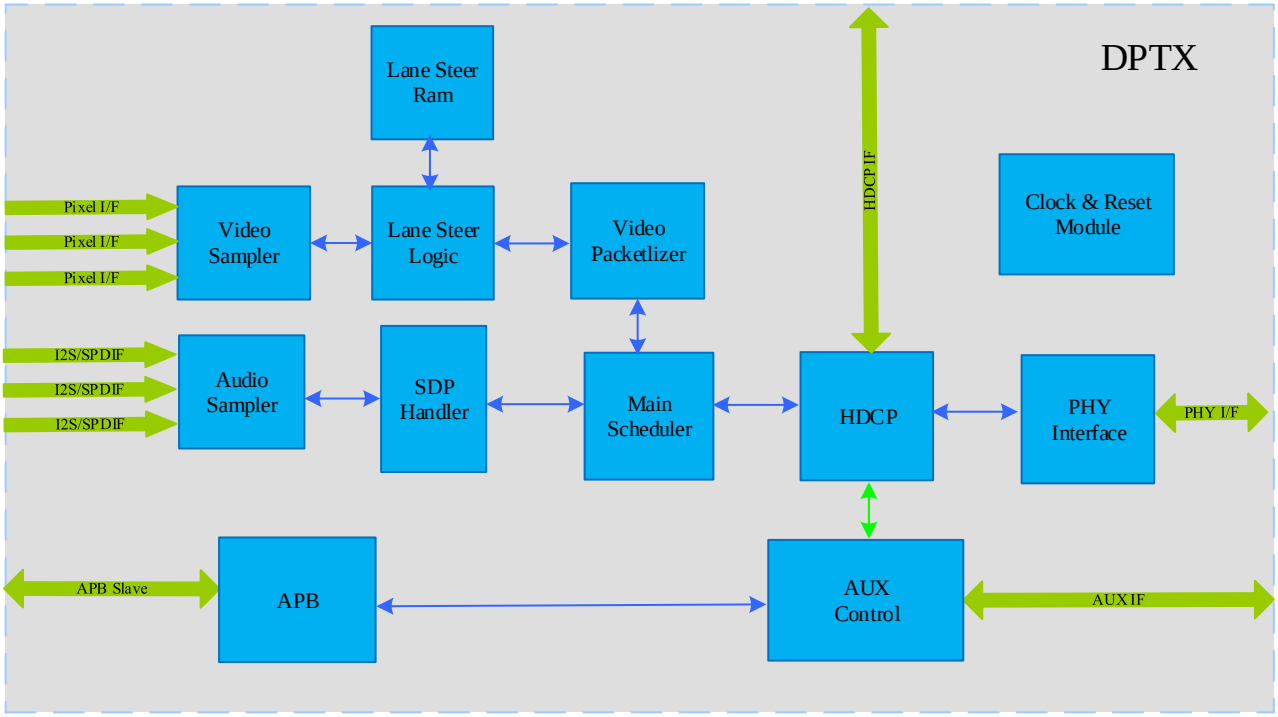


Fig. 22-1 DPTX Architecture Overview

The following sections describe the various blocks and their functionalities. DPTX uses a 32 bits internal data path for the main link.

22.3.2 Video Pixel Sampler

The video pixel sampler captures video pixel data on the video interface based on the various video formats, deep color modes. It outputs the captured video pixel data to the Video lane steering module as three separate color components.

Input data coming is registered once before it goes through a 3-stage pipeline. The 3-stage pipeline is required to capture the three-color components in various input video formats. The default delay in the video sampler is 4 cycles, which includes 3 stage pipeline and 1 stage input registering.

The video pixel sampler also gives the hsync and vsync to the lane steering logic based on what is presented on the video interface. To maintain the same pipeline delay, the hsync and vsync signals also go through the lane steering FIFO. On the rising edge and on the falling edge of the hsync and vsync a separate entry is pushed into the lane steering FIFO. When the packetizer pops out the hsync/vsync entry, it generates the hsync/vsync signals to the main scheduler.

The video is input on a 48-bit interface for supporting up to 16 bits per component mode. The data inputs are MSB aligned and for 6 bits per component mode; only the MSB 6 bits are valid for each component. The input video is sampled by the video sampler. The video sampler manipulates the video format that is input to the core, and then presents the data to the lane steering logic. The video sampler has pipelines to assemble the data and present to the lane steering logic.

22.3.3 Lane Steering Logic

The lane steering logic interfaces between the video pixel sampler and the Video packetizer. The lane steering logic takes three pixel components from the video pixel sampler and splits it into 32/64/128-bit data for each of up to four lanes in single/dual/quad pixel modes and sends it to the video Packetizer module.

The lane steering logic contains internal pipelines to assemble the data coming in from the video pixel sampler and push this data into the lane steering FIFOs in a 32/64/128-bit format. The lane steering FIFO is a 2-clock FIFO, with the pixel_clk being the write clock and the link clock being the read clock. The 32/64/128-bit data is pushed in simultaneously for all lanes. There is separate lane steering logic modules to take care of different video modes like RGB,YCbCr etc.

In the lane steering logic, the video data crosses the clock domains, from the pixel clock (pixel_clk) domain to the link clock (link_clk) domain.

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This module contains a dual clock FIFO per lane which is 39-bit wide. The lane steering FIFO is popped out by the video packetizer. The packetizer and the downstream logics run on the link clock. When the PHY interface is operating at 40 bits, then the link clock is the same as the phy_clk. But if the PHY interface is running at 20bits, then the link clock is half of the phy_clk. The video packetizer is instantiated per lane.
The lane_steer_fsm state machine in this module controls the data packing. This state machine looks at the input pixel pipeline and packs the data into 32 bits of data for each lane and pushes them into a 2-clock FIFO. The FIFO is written by the video packetizer on the pixel clock and read on the link clock. On seeing the lane steering FIFO being non empty, the video packetizer waits for threshold amount of link clock. By default, it waits for 16 clocks which is equivalent to 64 symbols (since the data width is 32), where 64 is the Transfer unit size. This threshold value could be changed by reprogramming VIDEO_CONFIG5 register. After waiting for the threshold number of link clocks, the packetizer pops out the data and send to the main scheduler. The packetizer keeps track of the transfer unit count. If the symbols transmitted is greater than the average number of symbols that is define for a particular video format (defined in VIDOE_CONFIG5.AVERAGE_SYMBOLS_PER_TU) and link rate, or if the FIFO is empty, it inserts fillers into the transfer unit until the transfer unit size of 64 is reached. During this filling time, data gets accumulated in the lane steering FIFO. During the transmission of the valid symbols, data gets filled into the FIFO and also gets popped out. The rate at which the push/pop happens varies.
The lane steering logic uses 12-stage pipelining. Each of the color components (R/G/B) go through the 12-stage pipelining. The 12 stages are required only for 6bpp mode with 4 lanes. Because this is not a configurable option, these pipeline stages are always present. If the number of lanes configured is less than 4, only a 5-stage pipeline is required.

22.3.4 Video Packetizer

The video packetizer takes data from the Video Lane Splitter to form packets based on the Tranfer Unit. The Transfer Unit Size is fixed to 64 bytes and internal data width is 32 bytes. The number of valid bytes to pack in a Transfer Unit is governed by the register fields AVERGAE_BYTES_PER_TU and AVERAGE_BYTES_PER_TU_FRAC in the VIDEO_CONFIG5 register. The software calculates this value based on the pixel rate for a given video format and the link rates, and then programs the value into the register.
The video packetizer acts on each lane. A 4-lane configuration contains four instances of the packetizer. Each instance of the packetizer must also know the total number of lanes for the packetizing logic.
The video packetizer works on a single clock domain, the link clock (link_clk).
When the lane steering FIFO goes non-empty, the packetizer waits for threshold amount of link clocks which is equivalent to a Transfer Unit. The threshold accumulates pixels in the lane steering FIFO. After threshold amounts of clocks, the packetizer transmits the pixels until the FIFO becomes empty. After average_bytes_per_tu bytes has been transmitted, based on Valid symbols per TU and TU size, video packetizer module inserts dummy data symbols and the corresponding framing symbols if required. For the following TU, it does not wait for 16 clocks, and transmits the available data in the FIFO. When the dummy data symbols are being inserted the video packetizer stops reading the lane steering FIFO.
When the Lane steering logic FIFO has a threshold amount of data, it starts reading data and transmits to the Link. The threshold is controlled by the VIDEO_CONFIG5.INIT_THRESHOLD. The FIFO must not get empty while active video is being transmitted. When the packetizer sees that the FIFO is almost empty or when average_bytes_per_tu bytes have been transmitted, it starts to insert fillers until the end of transfer unit. It also adds zero padding towards the end of active video period. The data output from the Video packetizer is multiplexed with SDP data from the SDP packetizer inside the main scheduler.
The packetizer works in the single stream mode. The data from the lane steering FIFO directly go to the scheduler. In SST mode, the lane steering FIFO is popped by the SST packetizer. But in MST mode this pop function needs to be handled by the Rate governor module through the scheduler.
When a stream is enabled but there is no pixel data on the pixel interface OR stream is not

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enabled in MST mode, the stream symbol sequence generator generates the SF symbols in its VC payload timeslot and every 1024 time slot VB-ID should be inserted. This is done by the scheduler. Scheduler is in the VBLANK state during this time. In SST mode, this functionality is handled by the scheduler.

22.3.5 Main Scheduler

The main scheduler multiplexes the data coming from the video and the secondary data packets (SDP) stream. It also inserts the blanking-start and blanking-end symbols. The main scheduler maintains a timer module that tracks the start and end of each horizontal and vertical blanking.

When the data valid goes low, indicating the end of active pixels, the main scheduler inserts blanking-start control symbol and follows it up with the VB-ID information. When the data valid goes high, indicating valid pixels, the main scheduler inserts blanking-start control symbol and follows it up with the pixel transmission.

The main scheduler

- Keeps track of active video period and the blanking intervals
- Multiplexes the data from the video stream and the SDP stream to the link based on blanking intervals.
- Uses video_daten and various programmed timing parameters to derive the horizontal and vertical intervals.
- Is responsible for transmitting the blanking start (BS) and blanking end (BE) control symbols at the blanking boundary.
- Gives control to the SDP scheduler for scheduling the SDP streams at the blanking intervals.
- Transmits VB-ID, Mvid and Mauid at the start of the blanking intervals
- Gives arbitration to SDP streams, in the absence of video stream, so that dummy symbols are inserted from the SDP packetizer (Figure 2-11 of DP 1.3 spec).
- The main scheduler module also takes care of generating the video timestamp values Mvid and Nvid.

With the fixed priority arbitration, the lower numbered register sets get priority over higher numbered register sets. The SDP module frames the SDP packet based on the information programmed in the SDP register set, and also calculates the ECC for the SDP.

22.3.6 Audio Sampler

The audio sampler is responsible for capturing the audio input received, and writing it into the audio FIFO for processing by the SDP module.

22.3.6.1 I2S Interface

I2S is one of the interfaces available in the DPTX for interfacing the audio stream.

The width of the audio samples is programmable through audio register AUD_CONFIG1. I2s_data_width, to be 16 to 24 bits.

The following control bits are to be transmitted in the audio stream as per IEC specification:

- P - Parity bit
- C - Channel Status
- U - User Data
- V – Validity
- PR - Start of Block Preamble (2 bits used to indicate Preamble for start of block. The PR bit in the audio stream SDP is encoded using this bit).
  - 00: Subframe 1 and start of audio block
  - 01: Subframe 1
  - 10: Subframe 2

Each I2S data supports two audio channels. For DPTX, there are 4 I2S data signals for supporting up to 8 audio channels, with a maximum sample frequency of 192Khz (non HBR).

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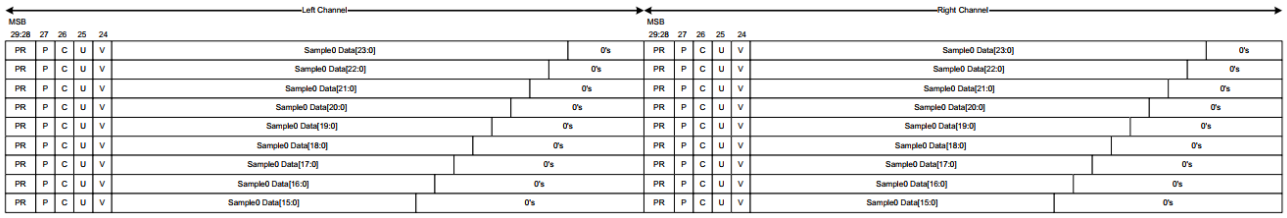


Fig. 22-2 i2s Data Input Format

Each audio sample per channel is 22 to 30 bits including preamble, control bits (auxiliary bits) and the sample data itself 16-24 bits). In one sampling frequency period, 2 sub-frames are provided or 2 samples (for the left and right channels). Since the input clock is 512 *fs, the remaining data in the subframe is ignored by the core.

High Bit Rate (HBR) Audio Support over I2S Interface

For supporting HBR audio over the I2S interface, perform the following steps:

1. Split the stream in four sub-streams by sending the stream to a FIFO with four outputs each. Each sub stream consists of a pair of samples.
2. Apply the i2sclk clock to the I2S interface with a frequency of 512*fs/4 (for example, 98.3 MHz for a 768 kHz input).
3. Set the I2S sample width to 22 bits by using the AUD_CONFIG1. I2s_data_width field register.
4. Configure the I2S interface by using the AUD_CONFIG1.audio_inf_select register. Enable all the four channels so that each channel carries a pair of samples using AUD_CONFIG1. i2s_in_en.
5. Map the I2S data sample, sampleI2S[21:0], in the following way: data[21:0] = {PR,P,C,U,V,dataHBR[15:0]} (Where PR,P,C,U,V are IEC61937 parameters, PR is the encoded preamble, and data[15:0] is the actual HBR sample data.)
6. The I2S data must be driven according to the following table.

22.3.6.2 SPDIF Interface

The SPDIF interface uses a clock (spdifclk_i) and serial data (spdifdata_i]) to transfer audio samples / audio stream into the DPTX. Each bits of the ispdif[3:0] data corresponds to a pair of channels. Data input on the SPDIF must be BMC coded. The spdifclk_i must be synchronous to the spdifdata_i and the frequency must be 512*fs, where fs is the original audio sampling frequency.

Each audio sample per channel is 32 bits including preamble, control bits (auxiliary bits) and the sample data itself 16-24 bits). In one sampling frequency period, 2 sub-frames are provided or 2 samples (for the left and right channels) or 64 bits. Since the SPDIF data input is BMC (Bi-Phase mark coding) coded, it takes 2 input clocks to represent a bit. So, one frame (or 2 sub frames) are represented in 128 clocks. Since the input clock is 512 *fs, the remaining data is zero coded.

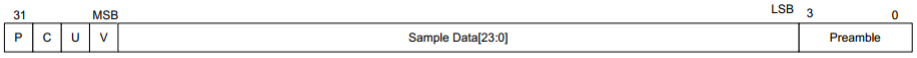


Fig. 22-3 SPDIF Data Input Format

The High Bit Rate Audio is fed on the SPDIF interface in the standard 2-channel format, with ispdifdata[0] only used for data transmission.

22.3.7 PHY Interface Layer

The controller supports Pipe complaint interface which can be used for interfacing with Synopsys PHY with the PCC logic inside the PHY.

The behavior of phy_powerdown, phy_laneX_phystatus, and phy_rate is similar to the signals in the PIPE 3.0 Spec with some minor modifications. The controller supports both 20- and 40-bit wide data interface to the PHY. The output from the main scheduler goes to the PHY interface unit. The PHY interface unit has the scrambler, the 8b/10 encoder and the training pattern generator unit. The training pattern generator is responsible for generating the patterns during link training at the request of the software. The link training is driven by the software. The software instructs the PHY interface unit and sequences it through each step of the link training. The PHY interface unit also has PCC (Power and clock control) module which is specific to interfacing with Synopsys PHY. This module is responsible for taking care of the power down changes and the clock multiplexing based on the data rate of the link. The PHY interface unit also has a Rocket IO wrapper which is used for

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interfacing to the rocket IO for prototyping.

22.3.8 AUX Channel Interface

The AUX channel interface is used by the DPTX controller for AUX transfers.
The AUX module uses a 16 MHz input AUX clock for oversampling and regenerating the AUX data from the serial interface in AUX Rx. The AUX module also has the Manchester encoder and decoder. Various registers are provided for the software to get notification on aux transaction completion or error status.
The AUX channel is responsible for executing the AUX transfers as requested by the software driver, via the APB interface, or by internal modules via a dedicated internal interface. The request by the software is initiated by programming the AUX registers which are implemented in the APB clock domain. Once a write to the AUX_CMD register is detected, the AUX channel initiates an AUX transfer and sets the AUX_REPLY_RECEIVED bit in the AUX_STATUS register. The transmitted data is encoded using a Manchester-II encoder. When the encoder is not driving the bus, then the transmit enable for the bidirectional AUX is not asserted. This interface runs at a nominal 1MHz (1Mbps). For a 16MHz clock for AUX is used, then each UI requires 16 clock periods to generate. The encoder generates the following sequence before any data stream is to be transmitted:

- Pre-charge: 16 zeros
- Pre-amble: 16 zeros
- AUX_SYNC_END: 2 High periods followed by 2 Low periods
- Data to be transmitted
- AUX_STOP: 2 High periods followed by 2 Low periods

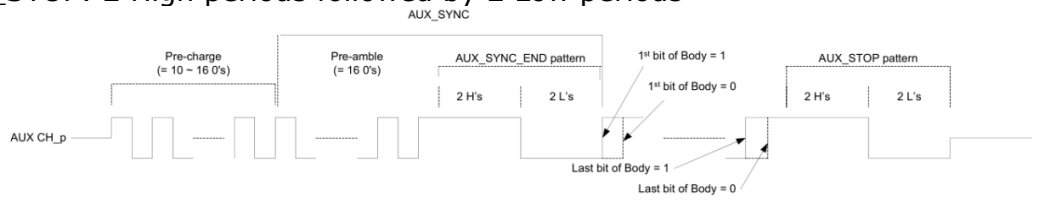


Fig. 22-4 AUX sequence

When all the data is transmitted, the AUX channel waits for a response. A 400uSec timer starts to limit the reply wait time. The Sink reply is captured & latched into the AUX status and data registers implemented in the APB block but also available on the internal bus to be consumed by the internal requesters. It's the SW responsibility to interpret the status and decide about the next transfer. The internal requests from the HDCP modules are limited to Native AUX. The internal requesters are expected to interpret correctly the ACK/NACK/DEFER responses, then decide how to proceed. The AUX_REPLY_RECEIVED bit is reset after the reply is received or timeout occurred.
Once the SW initiates an AUX request, some checks are performed to make sure its a legal request. The AUX_CMD.AUX_CMD_TYPE setting are compared with the 8 possible legal commands and the AUX_CMD.AUX_Byte_Length is checked so that:

- Read request is 1 byte
- Write does not exceed 16 bytes (1 + N, where N is 1-16)

22.3.9 Secondary Data Packet (SDP)

This section explains the how SDPs other than the Audio Stream SDPs are handled by the DPTX.
The DPTX controller has various software programmable registers through which the driver programs the header and the payload of the various SDPs, then programs the SDP Vertical/Horizontal & Manual control registers to enable specific SDP transmission and set whether the SDP is transmitted in the vertical, horizontal or both blanking intervals. The Manual control is used to control whether a SDP is transmitted once or continuously in the specified intervals.
DPTX always transmits the SDP as size of 32 bytes. Payloads less than this size are padded with zeros to make it 32 bytes.

- **Vendor Specific Infoframe Scheduling**

According to DP spec 1.3, section 2.2.5.1, the source should comply with the CEA861-F spec for transmission of any Infoframe. As per CEA861-F, a source should support transmission of more than one VSIFs in a vertical blanking interval. DPTX SDP register banks allows transmission of more than one VSIFs in a vertical blanking interval. CEA861-F

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also talks about transmitting the version1/version2, where version2 used to indicate a change in the payload of the VSIF. This is also supported by the controller. The driver has to make sure that the multiple VSIFs to be transmitted in a vertical interval has to be programmed from a lower to higher continuously in the SDP register bank. For example if there are 4 VSIFs to be transmitted in an interval, then the 1 to 4 VSIFs should be programmed in SDP register bank N to N+4, where the first VSIF should be programmed in register bank N and fourth VSIF should be programmed in register bank N+4.
Either auto or manual mode can be used to transmit the VSIFs. If not using manual mode, then the specific register banks should be disabled before making a change and re enabling.

- **Audio Timestamp SDP**

Audio Timestamp SDP payload, which has the Maud and Naud values are generated by the hardware. There is no separate register for programming the payload for Audio Timestamp SPDs. The software still needs to set the corresponding auto enable bit in the Replace this with SDP_VERTICAL/HORIZONTAL_CTRL register for enabling the transmission of the Audio Timestamp SDP.
In the absence of Main video stream, controller makes sure that the Audio Timestamp SDP is transmitted once every 512th BS symbol set.

- **Audio Stream SDPs**

The audio samples are packed into the audio stream SDP in a 2-channel format or an 8-channel format. 2 channel mode is only used when only channel 1 /2 are active. In this case the AUD_CONFIG1.num_channels should be set to 2, and AUD_CONFIG1.audio_data_in_en should have a value of only 1. 8 channel mode is used whenever audio samples are available for channels 3-8. In this case AUD_CONFIG1.num_channels should be set to 8 and the AUD_CONFIG1.audio_data_in_en can be set to any value based on which channels the samples are available on.
In an 8 channel operation if only 4 channels have samples active (AUD_CONFIG1.audio_data_in_en[3:0] == 4'b1001), then the audio stream SDPs are transmitted in an 8-channel mode and data for channels 3,4,5,6 are zeroed out. The sample present bit for these channels are still set.
Zero padding of sample data at the audio interface is required in case the number of transmitted audio channels is odd. No zero padding is required if the corresponding AUD_CONFIG1.AUDIO_DATA_IN_EN is set to 1'b0.
In the absence of Main video stream, controller makes sure that the Audio Infoframe SDP if enabled, is transmitted once every 512th BS symbol set.

22.3.10 High-Bandwidth Digital Content Protection (HDCP)

The DPTX core can be configured to support HDCP. When HDCP is enabled, it can be programmed to support HDCP 2.2 or HDCP 1.3 authentication protocols.
The HDCP 2.2 core contains a processor to fetch the instructions and data from the system memory. So, the HDCP core has a DMA master AXI interface.
This module is responsible for reading the ciphers and using them to encrypt the data. When encryption is enabled, this module reads cipher from HDCP1.3 or HDCP2.2 block based on the mode of operation and XORs the cipher with data; control symbols are bypassed.
It also maintains the Link verification pattern. Link verification pattern is shifted by one on every blanking interval and reset when encryption is disabled.
There is also a debug option to bypass encryption by not XORing the data with cipher with encryption enabled. This is only for debug purpose and must be locked using the HDCPCFG.HDCP_LOCK bit

22.3.10.1 Overview of HDCP 2.2

On NACK, DEFER response or ACK response with fewer bytes from sink, the ESM retries the entire AUX transaction — but not the full HDCP transaction. For example, when the ESM reads 522-byte Rx certificate and has successfully read the first 128 bytes, then it does a 16-byte read request for bytes 129-144 and gets a NACK, DEFER, or ACK with fewer than 16 bytes. It then re-attempts from byte 129, not from byte 1 (and not from byte (129 + # of bytes received)).
The SHALE hardware can be programmed to break up transfers into chunks of 4, 8 or 16

bytes but this is a static configuration parameter and cannot be adjusted on the fly. Re-attempts are always done with the same transaction size.
Retrying authentication is the responsibility of the application software controlling the ESM. When it has been determined that the Rx is 2.2 capable, the Tx retries infinitely until the device is disconnected or HDCP is wiggled. Retries are done at the rate of the send cert timeout (100 ms), so it is effective immediately.

22.3.10.2 Overview of HDCP 1.3

All AUX transfer requests from authentication and revocation state machine are handled in this module. It is responsible for forming the aux transfer commands and holding the values read in internal registers for use by authentication and revocation state machine (KSV list read is stored in the revocation RAM).
On NACK, DEFER response or ACK response with fewer bytes from sink, the transfer is retried
automatically from the point where the transfer stopped. For example, if HDCP1.3 reads 16 bytes, but sinks return 1byte with NAK response, HDCP1.3 retries only for the remaining 15bytes.
When seven consecutive NACK or DEFER response is received, HDCP interrupt event is generated.

- HDCP1.3 Encryption Signaling block implements the display port encryption signaling defined in HDCP1.3 spec.
- HDCP API Interface register Bank contains registers related to KSVs, AN, DPK programming, SHA calculation and GPIO status.
- HDCP SFR register Bank contains HDCP configuration register, HDCP observation register, HDCP interrupt related registers.
- HDCP1.3 DPK registers are used when ROM less configuration is chosen. DPKs are programmed by software and are stored in this module. It is used by cipher module for the keys.

Controller retries authentication indefinitely until the HDCP enable bit is reset by the application.

22.3.11 Multistream Transport (MST)

The DWC_dptx controller supports up to 3 video streams and their corresponding audio streams and secondary data packets. The maximum number of supported streams can be configured while configuring the controller.
Note:
1. DP interface support MST to 3 channels.
2. MST_DP0/1/2 source is from VP0/1/2, maximum resolution depends on each VP. And DPTX controller's MST_DP's maximum frame rate has following limits:
MST_DP0: 4096x2160@yuv422-120Hz
MST_DP1: 2560x1440@60Hz
MST_DP2: 2560x1440@60Hz
3. The DP interface maximum bandwidth is 25.92Gbps. The total bandwidth (MST_DP0+MST_DP1+MST_DP0) can not beyond this.

22.4 Register Description

22.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

22.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DPTX_VERSION_NUMBER	0x0000	W	0x3231312A	Version Number Register
DPTX_VERSION_TYPE	0x0004	W	0x65613038	Version Type Register
DPTX_CONFIG_REG1	0x0100	W	0x02212D0D	RTL Configuration Parameter Register 1
DPTX_CONFIG_REG2	0x0104	W	0x08001000	RTL Configuration Parameter Register 2

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Name	Offset	Size	Reset Value	Description
DPTX_CONFIG_REG3	0x0108	W	0x0000016C	RTL Configuration Parameter Register 3
DPTX_CCTL	0x0200	W	0x00000004	Global Control Register
DPTX_SOFT_RESET_CTRL	0x0204	W	0x00000000	Software Initiated Reset Register
DPTX_MST_VCP_TABLE_REG_0	0x0208	W	0x00000000	Program the Virtual Channel Payload allocation table maintained by the Payload Bandwidth manager
DPTX_MST_VCP_TABLE_REG_1	0x020C	W	0x00000000	Program the Virtual Channel Payload allocation table maintained by the Payload Bandwidth manager
DPTX_MST_VCP_TABLE_REG_2	0x0210	W	0x00000000	Program the Virtual Channel Payload allocation table maintained by the Payload Bandwidth manager
DPTX_MST_VCP_TABLE_REG_3	0x0214	W	0x00000000	Program the Virtual Channel Payload allocation table maintained by the Payload Bandwidth manager
DPTX_MST_VCP_TABLE_REG_4	0x0218	W	0x00000000	Program the Virtual Channel Payload allocation table maintained by the Payload Bandwidth manager
DPTX_MST_VCP_TABLE_REG_5	0x021C	W	0x00000000	Program the Virtual Channel Payload allocation table maintained by the Payload Bandwidth manager
DPTX_MST_VCP_TABLE_REG_6	0x0220	W	0x00000000	Program the Virtual Channel Payload allocation table maintained by the Payload Bandwidth manager
DPTX_MST_VCP_TABLE_REG_7	0x0224	W	0x00000000	Program the Virtual Channel Payload allocation table maintained by the Payload Bandwidth manager
DPTX_VSAMPLE_CTRL_STREAM0	0x0300	W	0x00000000	Video Sampler Control Register
DPTX_VSAMPLE_STUFF_CTRL1_STREAM0	0x0304	W	0x00000000	Video Sampler Data Stuff Control Register
DPTX_VSAMPLE_STUFF_CTRL2_STREAM0	0x0308	W	0x00000000	Stuff Control for RCR/GY Data Register
DPTX_VINPUT_POLARITY_CTRL_STREAM0	0x030C	W	0x00000000	Video Input Polarity Control Register
DPTX_VIDEO_CONFIG1_STREAM0	0x0310	W	0x02800280	Video Configuration Register1
DPTX_VIDEO_CONFIG2_STREAM0	0x0314	W	0x002D01E0	Video Configuration Register2
DPTX_VIDEO_CONFIG3_STREAM0	0x0318	W	0x00600010	Video Configuration Register3
DPTX_VIDEO_CONFIG4_STREAM0	0x031C	W	0x0002000A	Video Configuration Register4
DPTX_VIDEO_CONFIG5_STREAM0	0x0320	W	0x00030796	Video Configuration Register5

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Name	Offset	Size	Reset Value	Description
DPTX_VIDEO_MSA1_STREAM0	0x0324	W	0x00230090	Main Stream Attribute Register 1
DPTX_VIDEO_MSA2_STREAM0	0x0328	W	0x00000000	Main Stream Attribute Register 2
DPTX_VIDEO_MSA3_STREAM0	0x032C	W	0x00000000	Main Stream Attribute Register 3
DPTX_VIDEO_HBLANK_INTERVAL_STREAM0	0x0330	W	0x00000000	Hblank Interval Symbol Register
DPTX_AUD_CONFIG1_STREAM0	0x0400	W	0x12001202	Audio Input Control Register
DPTX_SDP_VERTICAL_CTRL_STREAM0	0x0500	W	0x00000000	Secondary Data Packets Vertical Blanking Register
DPTX_SDP_HORIZONTAL_CTRL_STREAM0	0x0504	W	0x00000000	Secondary Data Packets Horizontal Blanking Register
DPTX_SDP_STATUS_REGISTER_STREAM0	0x0508	W	0x00000000	Secondary Data Packets Status Register
DPTX_SDP_MANUAL_CTRL_STREAM0	0x050C	W	0x00000000	Manual Controlled Transmit of SDP
DPTX_SDP_STATUS_EN_STREAM0	0x0510	W	0x00000000	SDP Status Interrupt Enable Register
DPTX_SDP_REGISTER_BANK_STREAM0	0x0600	W	0x00000000	SDP Register bank
DPTX_PHYIF_CTRL	0x0A00	W	0x00060000	PHY Interface Control Register
DPTX_PHY_TX_EQ	0x0A04	W	0x00000000	PHY Pre-emphasis and Voltage Swing Control Register
DPTX_CUSTOMPAT0	0x0A08	W	0x00000000	Custom 80-bit pattern Position Register 0
DPTX_CUSTOMPAT1	0x0A0C	W	0x00000000	Custom 80-bit pattern Position Register 1
DPTX_CUSTOMPAT2	0x0A10	W	0x00000000	Highest 20-bits of the 80-bit pattern.
DPTX_HBR2_COMPLIANCE_SCRAMBLER_RESET	0x0A14	W	0x000000FC	CP2520 Pattern Length
DPTX_PHYIF_PWRDOWN_CTRL	0x0A18	W	0x00000000	Lane Powerdown Control
DPTX_AUX_CMD	0x0B00	W	0x00000000	AUX Configuration Register
DPTX_AUX_STATUS	0x0B04	W	0x00000000	AUX Status Register
DPTX_AUX_DATA0	0x0B08	W	0x00000000	AUX Data- First 4 bytes
DPTX_AUX_DATA1	0x0B0C	W	0x00000000	AUX Data Second 4 bytes
DPTX_AUX_DATA2	0x0B10	W	0x00000000	AUX Data Third 4 bytes
DPTX_AUX_DATA3	0x0B14	W	0x00000000	AUX Data Fourth 4 bytes
DPTX_PHYREG_CMDADDR	0x0C00	W	0x00000000	PHY Address Register
DPTX_PHYREG_DATA	0x0C04	W	0x00000000	PHY Write and Read DATA
DPTX_TYPEC_CTRL	0x0C08	W	0x00000000	Type-C Control Register
DPTX_GENERAL_INTERRUPT	0x0D00	W	0x00000000	General Interrupt Register
DPTX_GENERAL_INTERRUPT_ENABLE	0x0D04	W	0x00000000	General Interrupt Enable Register
DPTX_HPD_STATUS	0x0D08	W	0x00000000	HPD Interrupt Status Register
DPTX_HPD_INTERRUPT_ENABLE	0x0D0C	W	0x00000000	HPD Interrupt Enable Register
DPTX_HDCPCFG	0x0E00	W	0x00000000	HDCP Config Register
DPTX_HDCPOBS	0x0E04	W	0x00000000	HDCP Observation Register

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Name	Offset	Size	Reset Value	Description
DPTX_HDCPAPIINTCLR	0x0E08	W	0x00000000	HDCP Interrupt Clear Register
DPTX_HDCPAPIINTSTAT	0x0E0C	W	0x00000000	HDCP Interrupt Status Register
DPTX_HDCPAPIINTMSK	0x0E10	W	0x00000000	HDCP Interrupt Mask Register
DPTX_HDCPKSVMEMCTRL	0x0E18	W	0x00000000	HDCP KSV Memory Controller Register
DPTX_HDCP_REVOC_RAM_i	0x0E20	W	0xFFFFFFFF	HDCP Revocation RAM space
DPTX_HDCPREG_BKSV0	0x3600	W	0x00000000	HDCP BKSV Status Register 0
DPTX_HDCPREG_BKSV1	0x3604	W	0x00000000	HDCP BKSV Status Register 1
DPTX_HDCPREG_ANCONF	0x3608	W	0x00000000	HDCP AN Bypass Control Register
DPTX_HDCPREG_AN0	0x360C	W	0x00000000	HDCP Forced AN Register 0
DPTX_HDCPREG_AN1	0x3610	W	0x00000000	HDCP Forced AN Register 1
DPTX_HDCPREG_RMLCTL	0x3614	W	0x00000000	HDCP Encrypted Device Private Keys Control Register
DPTX_HDCPREG_RMLSTS	0x3618	W	0x00000000	HDCP Encrypted DPK Status Register
DPTX_HDCPREG_SEED	0x361C	W	0x00000000	HDCP Encrypted DPK Seed Register 0
DPTX_HDCPREG_DPK0	0x3620	W	0x00000000	HDCP Encrypted DPK Data Register 0
DPTX_HDCPREG_DPK1	0x3624	W	0x00000000	HDCP Encrypted DPK Data Register 1
DPTX_HDCP22GPIOSTS	0x3628	W	0x00000000	HDCP22 controller GPIO output status
DPTX_HDCP22GPIOCHNGSTS	0x362C	W	0x00000000	HDCP22 controller GPIO output change status
DPTX_HDCPREG_DPK_CRC	0x3630	W	0x00000000	HDCP Encrypted DPK Data CRC Register
DPTX_VSAMPLE_CTRL_STREAM1	0x10300	W	0x00000000	Video Sampler Control Register
DPTX_VSAMPLE_STUFF_CTRL1_STREAM1	0x10304	W	0x00000000	Video Sampler Data Stuff Control Register
DPTX_VSAMPLE_STUFF_CTRL2_STREAM1	0x10308	W	0x00000000	Stuff Control for RCR/GY Data Register
DPTX_VINPUT_POLARITY_CTRL_STREAM1	0x1030C	W	0x00000000	Video Input Polarity Control Register
DPTX_VIDEO_CONFIG1_STREAM1	0x10310	W	0x02800280	Video Configuration Register1
DPTX_VIDEO_CONFIG2_STREAM1	0x10314	W	0x002D01E0	Video Configuration Register2
DPTX_VIDEO_CONFIG3_STREAM1	0x10318	W	0x00600010	Video Configuration Register3
DPTX_VIDEO_CONFIG4_STREAM1	0x1031C	W	0x0002000A	Video Configuration Register4
DPTX_VIDEO_CONFIG5_STREAM1	0x10320	W	0x00030796	Video Configuration Register5
DPTX_VIDEO_MSA1_STREAM1	0x10324	W	0x00230090	Main Stream Attribute Register 1
DPTX_VIDEO_MSA2_STREAM1	0x10328	W	0x00000000	Main Stream Attribute Register 2
DPTX_VIDEO_MSA3_STREAM1	0x1032C	W	0x00000000	Main Stream Attribute Register 3
DPTX_VIDEO_HBLANK_INTERVAL_STREAM1	0x10330	W	0x00000000	Hblank Interval Symbol Register

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Name	Offset	Size	Reset Value	Description
DPTX_AUD_CONFIG1_STREAM1	0x10400	W	0x12001202	Audio Input Control Register
DPTX_SDP_VERTICAL_CTRL_STREAM1	0x10500	W	0x00000000	Secondary Data Packets Vertical Blanking Register
DPTX_SDP_HORIZONTAL_CTRL_STREAM1	0x10504	W	0x00000000	Secondary Data Packets Horizontal Blanking Register
DPTX_SDP_STATUS_REGISTER_STREAM1	0x10508	W	0x00000000	Secondary Data Packets Status Register
DPTX_SDP_MANUAL_CTRL_STREAM1	0x1050C	W	0x00000000	Manual Controlled Transmit of SDP
DPTX_SDP_STATUS_EN_STREAM1	0x10510	W	0x00000000	SDP Status Interrupt Enable Register
DPTX_SDP_REGISTER_BANK_STREAM1	0x10600	W	0x00000000	SDP Register bank
DPTX_VSAMPLE_CTRL_STREAM2	0x20300	W	0x00000000	Video Sampler Control Register
DPTX_VSAMPLE_STUFF_CTRL1_STREAM2	0x20304	W	0x00000000	Video Sampler Data Stuff Control Register
DPTX_VSAMPLE_STUFF_CTRL2_STREAM2	0x20308	W	0x00000000	Stuff Control for RCR/GY Data Register
DPTX_VINPUT_POLARITY_CTRL_STREAM2	0x2030C	W	0x00000000	Video Input Polarity Control Register
DPTX_VIDEO_CONFIG1_STREAM2	0x20310	W	0x02800280	Video Configuration Register1
DPTX_VIDEO_CONFIG2_STREAM2	0x20314	W	0x002D01E0	Video Configuration Register2
DPTX_VIDEO_CONFIG3_STREAM2	0x20318	W	0x00600010	Video Configuration Register3
DPTX_VIDEO_CONFIG4_STREAM2	0x2031C	W	0x0002000A	Video Configuration Register4
DPTX_VIDEO_CONFIG5_STREAM2	0x20320	W	0x00030796	Video Configuration Register5
DPTX_VIDEO_MSA1_STREAM2	0x20324	W	0x00230090	Main Stream Attribute Register 1
DPTX_VIDEO_MSA2_STREAM2	0x20328	W	0x00000000	Main Stream Attribute Register 2
DPTX_VIDEO_MSA3_STREAM2	0x2032C	W	0x00000000	Main Stream Attribute Register 3
DPTX_VIDEO_HBLANK_INTERVAL_STREAM2	0x20330	W	0x00000000	Hblank Interval Symbol Register
DPTX_AUD_CONFIG1_STREAM2	0x20400	W	0x12001202	Audio Input Control Register
DPTX_SDP_VERTICAL_CTRL_STREAM2	0x20500	W	0x00000000	Secondary Data Packets Vertical Blanking Register
DPTX_SDP_HORIZONTAL_CTRL_STREAM2	0x20504	W	0x00000000	Secondary Data Packets Horizontal Blanking Register
DPTX_SDP_STATUS_REGISTER_STREAM2	0x20508	W	0x00000000	Secondary Data Packets Status Register
DPTX_SDP_MANUAL_CTRL_STREAM2	0x2050C	W	0x00000000	Manual Controlled Transmit of SDP
DPTX_SDP_STATUS_EN_STREAM2	0x20510	W	0x00000000	SDP Status Interrupt Enable Register
DPTX_SDP_REGISTER_BANK_STREAM2	0x20600	W	0x00000000	SDP Register bank

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*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

22.4.3 Detail Registers Description

DPTX_VERSION_NUMBER

Address: Operational Base(0x27E40000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x3231312a	VERSION_NUMBER Version Number of the DPTX

DPTX_VERSION_TYPE

Address: Operational Base(0x27E40000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RO	0x65613038	VERSION_TYPE Version type of the DPTX

DPTX_CONFIG_REG1

Address: Operational Base(0x27E40000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	DSC The value of the parameter DPTX_DSC_EN
29	RO	0x0	GEN2_PHY The value of the parameter DPTX_COMBO_PHY_C10_GEN2.
28:25	RO	0x1	NUM_DSC_ENC The value of the parameter DPTX_NUM_DSC_ENC.
24	RO	0x0	FEC_EN The value of the parameter DPTX_FEC_EN
23	RO	0x0	EDP_EN The value of the parameter DPTX_EDP_EN.
22	RO	0x0	DSC_EN Indicates if Internal DSC is enabled or not
21:19	RO	0x4	MP_MODE 3'b001: Single Pixel Mode. 3'b010: Dual Pixel Mode. 3'b100: Quad Pixel Mode.
18:16	RO	0x1	NUM_STREAMS 3'h1: SST Mode. 3'h2: Two Streams 3'h3: Three Streams 3'h4: Four Streams
15:14	RO	0x0	reserved_15_14 Reserved
13:12	RO	0x2	SYNC_DEPTH 2'b10: Indicates that 2 stage synchronizers being used 2'b11: Indicates that 3 stage synchronizers being used
11	RO	0x1	DPK_8BIT 1'b1: ROM width is 8 bits 1'b0: ROM width is 56bits
10	RO	0x1	DPK_ROMLESS When 1, disables the use of External ROM for storing Device Private Keys
9	RO	0x0	FPGA_EN When enabled, configures the core to have the audio and video generators instantiated inside the DWC_dptx top level.

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Bit	Attr	Reset Value	Description
8:4	RO	0x10	SDP_REG_BANK_SIZE Specifies the number of SDP register banks supported. Enabling each register bank instantiates nine 32-bit registers for the transmission of 32Byte SDP packet.
3	RO	0x1	PHY_USED The value of the parameter DPTX_PHYIF_TYPE 1'b0: Vendor PHY 1'b1: PIPE Compliant PHY
2:1	RO	0x2	AUDIO_SELECT The value of parameter audio_select 2'b00: I2S Interface 2'b01: SPDIF Interface 2'b10: I2S and SPDIF Interface 2'b11: None
0	RO	0x1	HDCP_SELECT Reflects the hardware parameter hdcp_en 1'b0: No 1'b1: Yes

DPTX_CONFIG_REG2

Address: Operational Base(0x27E40000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RO	0x0800	DSC_MAX_NUM_LINES The value of the parameter DSC_MAX_NUM_LINES
15:0	RO	0x1000	DSC_MAX_PIXS_PER_LINE The value of the parameter DSC_MAX_PIXS_PER_LINE

DPTX_CONFIG_REG3

Address: Operational Base(0x27E40000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved_31_9 Reserved
8:7	RO	0x2	PHY_TYPE 2'b00: Vendor PHY 2'b01: RocketIO FPGA Only 2'b10: Pipe Compliant PHY 2'b11: Reseved
6	RO	0x1	DSC_NATIVE_422_EN The value of the parameter DSC_NATIVE_422_EN
5	RO	0x1	DSC_NATIVE_420_EN The value of the parameter DSC_NATIVE_420_EN
4:0	RO	0x0c	DSC_MAX_BPC The value of the parameter DSC_MAX_BPC

DPTX_CCTL

Address: Operational Base(0x27E40000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	ENHANCE_FRAMING_WITH_FE When set controller follows enhanced framing with FEC as specified in section 3.5.1.1 of the DP1.4 spec. Configure this bit when enabling FEC on sink ie before setting FEC_READY bit in sink

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Bit	Attr	Reset Value	Description
28	RW	0x0	INITIATE_MST_ACT_SEQ Only used in MST mode and should be programmed to trigger the link to start an ACT sequence with the DPRX of the branch device immediately connected to the DPTX.
27	RW	0x0	ENABLE_eDP This bit is used to control the operation of the controller as an Embedded DisplayPort controller (eDP) or a standard DisplayPort Controller compliant with the DisplayPort Spec Ver 1.4. 1'b1: Controller operates in eDP mode 1'b0: Controller operates in standard DisplayPort mode eDP features are disabled by default. Program this bit only if you have chosen to enable eDP features by seeing the parameter DPTX_EDP_EN = 1. When eDP is enabled FEC should not be enabled (ENABLE_FEC should be 0).
26	RW	0x0	ENABLE_FEC This bit is used to enable the FEC feature. Set this bit to 1 to enable the FEC functionality. If FEC is disabled during core configuration (DWC_DPTX_FEC_EN=0), then writing to this bit has no effect.
25	RW	0x0	ENABLE_MST_MODE This bit is used for enabling the MST mode of operation.
24:17	RW	0x00	BS_512_SCALE_DOWN When SR_SCALE_DOWN is set, this controls the 512 scale down count.
16	RW	0x0	SR_SCALE_DOWN "Every 512th BS symbol must be replaced with an SR symbol by a DPTX to reset the LFSR of the scrambler". For simulation, a scale down factor has been added and this bit controls the scaledown. When set to 1 the scrambler reset replaces Blanking Start after CCTL.BS_512_SCALE_DOWN value. When set to 0 scrambler reset replaces Blanking Start after 512 Blanking Starts
15:12	RO	0x0	reserved
11:8	RW	0x0	DEBUG_CONTROL Used for controlling the debug bus output. By configuring this register different signals selected to the output 64bits debug bus. No signal is selected and the output is '0' when the register is in its default state. 4'b0000: No signal is selected. 4'b0001: AUX 4'b0010: AUDIO 4'b0011: VIDEO 4'b0100: LINK 4'b0101: HDCP1.3 4'b0110: HDCP2.2 4'b0111: SDP 4'b1XXX: reserved
7	RO	0x0	reserved
6	RW	0x0	SEL_AUX_TIMEOUT_32MS When set to 1 the Aux timeout value is 3.2ms instead of 400us
5	RW	0x0	DISABLE_INTERLEAVING When set to 1 the nibble interleaving logic implemented as part of SDP packets generation is disabled.

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Bit	Attr	Reset Value	Description
4	RW	0x0	FORCE_HPD Used for testing only. It allows software to force the HPD value to 1 when writing 1. Otherwise does not impact the external HPD input.
3	RW	0x0	SCALE_DOWN_MODE When programmed to 1 the debounce filter on the HPD input is reduced from 100mSec in normal operation to 10uSec. This bit does not have any impact on the IRQ generation timing.
2	RW	0x1	DEFAULT_FAST_LINK_TRAIN_E When set after coming out of power on reset the controller starts fast link training for 1lane RBR rate without the driver intervention. The default video timings are set for 640x480 timing format 6bpc.
1	RW	0x0	ENHANCE_FRAMING_EN When set, controller follows enhanced framing. Configure this bit based on enhanced framing support of sink
0	RW	0x0	SCRAMBLE_DIS 1'b1: Disable scramble. 1'b0: Scramble enabled (default). When set, DWC_dptx link does not scramble data on the main link. Enabling or disabling this bit resets the scrambler.

DPTX_SOFT_RESET_CTRL

Address: Operational Base(0x27E40000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	AUDIO_SAMPLER_RESET_STREAM3 Software sets this bit to start the audio sampler reset. This also clears the audio FIFOs. This field is valid only for MST mode and is used for the reset of audio streams 3.
10	RW	0x0	AUDIO_SAMPLER_RESET_STREAM2 Software sets this bit to start the audio sampler reset. This also clears the audio FIFOs. This field is valid only for MST mode and is used for the reset of audio streams 2.
9	RW	0x0	AUDIO_SAMPLER_RESET_STREAM1 Software sets this bit to start the audio sampler reset. This also clears the audio FIFOs. This field is valid only for MST mode and is used for the reset of audio streams 1.
8:5	RW	0x0	VIDEO_RESET Software sets this bit to reset the video logic. In MST mode each bit controls the reset of a specific Video Stream. Bit5-8 controls the soft reset of Video stream-0 to 3.
4	RW	0x0	AUX_RESET Software sets this bit to start the aux channel reset.
3	RW	0x0	AUDIO_SAMPLER_RESET Software sets this bit to start the audio sampler reset. This also clears the audio FIFOs. In MST mode, this bit is used for Stream0.
2	RW	0x0	HDCP_MODULE_RESET Software sets this bit to start the HDCP module reset
1	RW	0x0	PHY_SOFT_RESET Software sets this bit to start the PHY reset process.
0	RW	0x0	CONTROLLER_RESET Software sets this bit to start the controller reset process. This also initiates a PHY reset.

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DPTX_MST_VCP_TABLE_REG_0

Address: Operational Base(0x27E40000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	STREAM_ID_SLOT_7 Stream ID Slot 7 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
27:24	RW	0x0	STREAM_ID_SLOT_6 Stream ID Slot 6 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
23:20	RW	0x0	STREAM_ID_SLOT_5 Stream ID Slot 5 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
19:16	RW	0x0	STREAM_ID_SLOT_4 Stream ID Slot 4 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
15:12	RW	0x0	STREAM_ID_SLOT_3 Stream ID Slot 3 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
11:8	RW	0x0	STREAM_ID_SLOT_2 Stream ID Slot 2 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
7:4	RW	0x0	STREAM_ID_SLOT_1 Stream ID Slot 1 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
3:0	RW	0x0	STREAM_ID_SLOT_0 Stream ID Slot 0 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3

DPTX_MST_VCP_TABLE_REG_1

Address: Operational Base(0x27E40000) + offset (0x020C)

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	STREAM_ID_SLOT_7 Stream ID Slot 7 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
27:24	RW	0x0	STREAM_ID_SLOT_6 Stream ID Slot 6 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
23:20	RW	0x0	STREAM_ID_SLOT_5 Stream ID Slot 5 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
19:16	RW	0x0	STREAM_ID_SLOT_4 Stream ID Slot 4 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
15:12	RW	0x0	STREAM_ID_SLOT_3 Stream ID Slot 3 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
11:8	RW	0x0	STREAM_ID_SLOT_2 Stream ID Slot 2 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
7:4	RW	0x0	STREAM_ID_SLOT_1 Stream ID Slot 1 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
3:0	RW	0x0	STREAM_ID_SLOT_0 Stream ID Slot 0 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3

DPTX_MST_VCP_TABLE_REG_2

Address: Operational Base(0x27E40000) + offset (0x0210)

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	STREAM_ID_SLOT_7 Stream ID Slot 7 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
27:24	RW	0x0	STREAM_ID_SLOT_6 Stream ID Slot 6 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
23:20	RW	0x0	STREAM_ID_SLOT_5 Stream ID Slot 5 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
19:16	RW	0x0	STREAM_ID_SLOT_4 Stream ID Slot 4 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
15:12	RW	0x0	STREAM_ID_SLOT_3 Stream ID Slot 3 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
11:8	RW	0x0	STREAM_ID_SLOT_2 Stream ID Slot 2 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
7:4	RW	0x0	STREAM_ID_SLOT_1 Stream ID Slot 1 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
3:0	RW	0x0	STREAM_ID_SLOT_0 Stream ID Slot 0 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3

DPTX_MST_VCP_TABLE_REG_3

Address: Operational Base(0x27E40000) + offset (0x0214)

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	STREAM_ID_SLOT_7 Stream ID Slot 7 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
27:24	RW	0x0	STREAM_ID_SLOT_6 Stream ID Slot 6 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
23:20	RW	0x0	STREAM_ID_SLOT_5 Stream ID Slot 5 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
19:16	RW	0x0	STREAM_ID_SLOT_4 Stream ID Slot 4 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
15:12	RW	0x0	STREAM_ID_SLOT_3 Stream ID Slot 3 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
11:8	RW	0x0	STREAM_ID_SLOT_2 Stream ID Slot 2 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
7:4	RW	0x0	STREAM_ID_SLOT_1 Stream ID Slot 1 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
3:0	RW	0x0	STREAM_ID_SLOT_0 Stream ID Slot 0 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3

DPTX_MST_VCP_TABLE_REG_4

Address: Operational Base(0x27E40000) + offset (0x0218)

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	STREAM_ID_SLOT_7 Stream ID Slot 7 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
27:24	RW	0x0	STREAM_ID_SLOT_6 Stream ID Slot 6 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
23:20	RW	0x0	STREAM_ID_SLOT_5 Stream ID Slot 5 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
19:16	RW	0x0	STREAM_ID_SLOT_4 Stream ID Slot 4 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
15:12	RW	0x0	STREAM_ID_SLOT_3 Stream ID Slot 3 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
11:8	RW	0x0	STREAM_ID_SLOT_2 Stream ID Slot 2 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
7:4	RW	0x0	STREAM_ID_SLOT_1 Stream ID Slot 1 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
3:0	RW	0x0	STREAM_ID_SLOT_0 Stream ID Slot 0 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3

DPTX_MST_VCP_TABLE_REG_5

Address: Operational Base(0x27E40000) + offset (0x021C)

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	STREAM_ID_SLOT_7 Stream ID Slot 7 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
27:24	RW	0x0	STREAM_ID_SLOT_6 Stream ID Slot 6 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
23:20	RW	0x0	STREAM_ID_SLOT_5 Stream ID Slot 5 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
19:16	RW	0x0	STREAM_ID_SLOT_4 Stream ID Slot 4 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
15:12	RW	0x0	STREAM_ID_SLOT_3 Stream ID Slot 3 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
11:8	RW	0x0	STREAM_ID_SLOT_2 Stream ID Slot 2 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
7:4	RW	0x0	STREAM_ID_SLOT_1 Stream ID Slot 1 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
3:0	RW	0x0	STREAM_ID_SLOT_0 Stream ID Slot 0 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3

DPTX_MST_VCP_TABLE_REG_6

Address: Operational Base(0x27E40000) + offset (0x0220)

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	STREAM_ID_SLOT_7 Stream ID Slot 7 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
27:24	RW	0x0	STREAM_ID_SLOT_6 Stream ID Slot 6 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
23:20	RW	0x0	STREAM_ID_SLOT_5 Stream ID Slot 5 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
19:16	RW	0x0	STREAM_ID_SLOT_4 Stream ID Slot 4 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
15:12	RW	0x0	STREAM_ID_SLOT_3 Stream ID Slot 3 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
11:8	RW	0x0	STREAM_ID_SLOT_2 Stream ID Slot 2 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
7:4	RW	0x0	STREAM_ID_SLOT_1 Stream ID Slot 1 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
3:0	RW	0x0	STREAM_ID_SLOT_0 Stream ID Slot 0 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3

DPTX_MST_VCP_TABLE_REG_7

Address: Operational Base(0x27E40000) + offset (0x0224)

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	STREAM_ID_SLOT_7 Stream ID Slot 7 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
27:24	RW	0x0	STREAM_ID_SLOT_6 Stream ID Slot 6 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
23:20	RW	0x0	STREAM_ID_SLOT_5 Stream ID Slot 5 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
19:16	RW	0x0	STREAM_ID_SLOT_4 Stream ID Slot 4 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
15:12	RW	0x0	STREAM_ID_SLOT_3 Stream ID Slot 3 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
11:8	RW	0x0	STREAM_ID_SLOT_2 Stream ID Slot 2 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
7:4	RW	0x0	STREAM_ID_SLOT_1 Stream ID Slot 1 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3
3:0	RW	0x0	STREAM_ID_SLOT_0 Stream ID Slot 0 for register 0 4'h0: Not allocated 4'h1: Stream1 4'h2: Stream2 4'h3: Stream3

DPTX_VSAMPLE_CTRL_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25	RW	0x0	STREAM_TYPE This is a per stream control defining the stream type. RepeaterAuth_Stream_Manage of HDCP2.2 specification. This field is valid only when HDCP MST are enabled.
24	RW	0x0	ENCRYPTION_ENABLE This is a per stream control to enable encryption. Setting ofthis bit has significance only when operating in MST mode or eDP. In non eDP SST operation, this bit has no significance. In MST mode or when eDP is enabled, this bit control the encryption to be used. In MST mode, this bit control HDCP encryption for a specific stream. HDCPCFG register controls the global enable of HDCP. In eDP mode this bit controls the enabling of ASSR feature as specified in section 3.5 of eDP1.4b spec and Section 2.10 of DP1.4 spec. When eDP is enabled, HDCP should be disabled and HDCPCFG[1] should not be set.
23	RW	0x0	ENABLE_DSC Set this bit to 1 to enable Display Stream Compression (DSC) on this specific stream. The software driver can set this bit only if DSC is enabled during configuration (DWC_DPTX_DSC_EN = 1 or 2). Otherwise writing 1 1 to this bit does not take effect.
22:21	RW	0x0	PIXEL_MODE_SELECT This field is used to select the single/dual/quad pixel mode of operation. 2'b00: Single pixel mode (default) 2'b01: Dual pixel mode 2'b10: Quad pixel mode. 2'b11: Reserved.

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Bit	Attr	Reset Value	Description
20:16	RW	0x00	VIDEO_MAPPING Video input mapping color space/depth Video Input mapping (color space/color depth) with DSC disabled/enabled(VSAMPLE_CTRL.ENABLE_DSC=0/1): 0: RGB 6bits (Reserved) 1: RGB 8bits (RGB 8bits) 2: RGB 10bits (RGB 10bits) 3: RGB 12bits (RGB 12bits) 4: RGB 16bits (Reserved) 5: YCbCR4:4:4 8bits (YCbCr4:4:4 8bits) 6: YCbCr4:4:4 10bits (YCbCr4:4:4 10bits) 7: YCbCr4:4:4 12bits (YCbCr4:4:4 12bits) 8: YCbCr4:4:4 16bits (Reserved) 9: YCbCR4:2:2 8bits (Simple YCbCr4:2:2 8bits) 10: YCbCr4:2:2 10bits (Simple YCbCr4:2:2 10bits) 11: YCbCr4:2:2 12bits (Simple YCbCr4:2:2 12bits) 12: YCbCr4:2:2 16bits (Reserved) 13: YCbCR4:2:0 8bits (YCbCR4:2:0 8bits) 14: YCbCr4:2:0 10bits (YCbCR4:2:0 10bits) 15: YCbCr4:2:0 12bits (YCbCR4:2:0 12bits) 16: YCbCr4:2:0 16bits (Reserved) 17: YOnly 8bits (native YCbCr4:2:2 8bits) 18: YOnly 10bits (native YCbCr4:2:2 10bits) 19: YOnly 12bits (native YCbCr4:2:2 12bits) 20: YOnly 16bits (Reserved) 23: RAW 8bits. (Reserved) 24: RAW 10bits (Reserved) 25: RAW 12bits (Reserved) 27: RAW 16bits (Reserved) Others: Reserved.
15:6	RO	0x000	reserved
5	RW	0x0	VIDEO_STREAM_ENABLE 1'b0: Video stream Disable 1'b1: Video stream Enable When set to 0, no video stream is transmitted. Video inputs are ignored and NoVideoStream_flag in the VB-ID is set.
4	RW	0x0	INTERNAL_DE_GENERATOR 1'b1: Enable internal data generator 1'b0: Data enable signal available at the input. When the external logic which drives the pixel data does not generate the video data enable, then enabling this bit forces the controller to generate the video enable internally. Note: This feature is currently not supported and therefore should not be used.
3:0	RO	0x0	reserved

DPTX_VSAMPLE_STUFF_CTRL1_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	BCB_STUFF_DATA Data to be stuffed on B/Cb data path.
15:3	RO	0x0000	reserved
2	RW	0x0	GY_DATA_STUFFING_EN Enable stuffing on internal G/Y data lines.
1	RW	0x0	RCR_DATA_STUFFING_EN Enable stuffing on internal R/Cr data lines.

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Bit	Attr	Reset Value	Description
0	RW	0x0	BCB_DATA_STUFFING_EN Enable stuffing on internal B/Cb data lines

DPTX_VSAMPLE_STUFF_CTRL2_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	GY_STUFF_DATA Data to be stuffed on G/Y data path.
15:0	RW	0x0000	RCR_STUFF_DATA Data to be stuffed on R/Cr data path.

DPTX_VINPUT_POLARITY_CTRL_STREAM0

Address: Operational Base(0x27E40000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	DE_IN_POLARITY de input polarity 1'b1: Active low 1'b0: Active high
1	RW	0x0	HSYNC_IN_POLARITY Hsync input polarity 1'b1: Active high 1'b0: Active low
0	RW	0x0	VSYNC_IN_POLARITY Vsync input polarity 1'b1: Active high 1'b0: Active low

DPTX_VIDEO_CONFIG1_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	RW	0x0280	HACTIVE Input video Horizontal active pixel region width. Number of Horizontal active pixels [0...8191].
15:2	RW	0x00a0	HBLANK Input video Horizontal blanking pixel region width. Number of Horizontal blanking pixels [0...4095].
1	RW	0x0	I_P Input video mode 1b: Interlaced 0b: Progressive
0	RW	0x0	R_V_BLANK_IN_OSC Used for CEA861-D modes with fractional Vblank (for example, modes 5, 6, 7, 10, 11, 20, 21, and 22). For more modes, see the CEA861-D specification. Note: Set this field to 1 for video mode 39, although there is no Vblank oscillation. 1b: Active high

DPTX_VIDEO_CONFIG2_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	RW	0x002d	VBLANK Input video Vertical blanking pixel region width. Number of Vertical blanking lines.

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Bit	Attr	Reset Value	Description
15:0	RW	0x01e0	VACTIVE Input video Vertical active pixel region width. This bit field holds bits 15:0 of number of Vertical active pixels.

DPTX_VIDEO_CONFIG3_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:16	RW	0x0060	H_SYNC_WIDTH Input video Hsync active pulse width. Integer number of pixel clock cycles [0...511].
15:0	RW	0x0010	H_FRONT_PORCH Input video Hsync active edge delay. Integer number of pixel clock cycles from "de" non active edge of the last "de" valid period [0...4095].

DPTX_VIDEO_CONFIG4_STREAM0

Address: Operational Base(0x27E40000) + offset (0x031C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0002	V_SYNC_WIDTH Input video Vsync active pulse width. Integer number of video lines [0...63].
15:0	RW	0x000a	V_FRONT_PORCH Input video Vsync active edge delay. Integer number of hsync pulses from "de" non active edge of the last "de" valid period. [0...255]. Specified in terms of number of lines. Value After Reset: 0

DPTX_VIDEO_CONFIG5_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:21	RW	0x0	INIT_THRESHOLD_HI Most Significant two bits of INT_THRESHOLD.
20	RW	0x0	ENABLE_3D_FRAME_FIELD_SE Set this bit to 1 if the video format being transmitted is 3D video format and Frame/Filed sequential 3D mode is used. Set this bit to 0 (default) if no 3D video is being transmitted, or Frame/Filed sequential 3D format is not being used. Refer to section "3D Stereo Mode Support" for more details.

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Bit	Attr	Reset Value	Description
19:14	RW	0x0c	AVERAGE_BYTES_PER_TU_FR This is the fractional portion of the value calculated in the average bytes per TU. The first decimal value in the fractional part should be programmed here. For example, if the average bytes per TU is 24.34, then this field should be programmed to a value of 3. In SST mode only bits 19:16 is used. In MST mode, this field should be programmed with the fractional value of the VC payload size calculated by the Payload bandwidth manager. as specified in Section 2.6.4.3 of DisplayPort 1.4 Spec. The fractional value calculated times 64 should be programmed in this field. For example if the vc_payload_size calculated is 34.23, a value of 0.23*64 = 15 (14.72 rounded to the nearest integer) should be programmed here. For over 64 MTPs controller transmits AVERAGE_BYTES_PER_TU+1 timeslots with valid symbols for average_bytes_per_tu MTPs for this streams and for 64-average_bytes_per_tu MTPS AVERAGE_BYTES_PER_TU timeslots will have valid symbols. Here is an example for calculating the average_bytes_per_tu_frac in MST mode for the video format VIC-1 (640x480) RGB, 8bpc, at a frame rate of 60Hz. The Link is assumed to be HBR 4 lanes. Peak_stream_bandwidth = Pixel_clock_frequency*bytes_per_pixel = 25.175*3 = 75.52MBps Link Bandwidth = link_rate * 100 * number_of_lanes .= 2.7 * 100 *4 = 1080MBps Average_bytes_per_tu_frac = frac((peak_stream_bandwidth/link_bandwidth)*64))*64 = frac(4.475) *64= 0.47*64 = 30.08 . Program the frac value rounded to the nearest integer which is 30.

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Bit	Attr	Reset Value	Description
13:7	RW	0x0f	INIT_THRESHOLD This is the number of clock cycles the link should wait for the pixels to accumulate at the beginning of every video line before it starts transmitting. This threshold influences the link capability to maintain the avarge valid symbols per TU. For Non-DSC Mode: If the calculated average bytes per tu value is less than 6 then the threshold value should be programmed to 32. For RGB or YCbCr444 modes if the hblank is less than or equal to 80pixels, then a value of 12 should be used. For 4:2:0 mode if the hblank is less than 40, then a value of 3 should be used. For dual and quad pixel modes a value of 64 should be used. In all other cases the default value of 16 is sufficient. The link has a 32 bit data path and the 16 clocks is to wait for TU size clocks which is 16*4 = 64 (TU size) symbols. For DSC Mode: INIT_THRESHOLD = pixel_push_rate * link_pixel_clock_ratio * slot_count where Pixel Push rate = (8/bpp)*lane_count. slot_count for sst =average_bytes_per_tu + FEC symbols inserted per lane(13 in 1-lane and 7 in 2/4lane if fec is enabled, 0 if fec is disabled) slot count is rounded to nearest multiples of 4(ceiling). If slot count calculated is greater than 64, then slot count is fixed to 64. slot_count for mst = (32/lane_count) + average_bytes_per_tu + FEC symbols inserted per lane(13 in 1-lane and 7 in 2/4lane if fec is enabled, 0 if fec is disabled). Slot count is rounded to nearest multiples of 4(ceiling). If slot count calculated is greater than 64, then slot count is fixed to 64. bpp = PPS.bits_per_pixel in simple modes and PPS.bits_per_pixel/2 in native modes link_pixel_clock_ratio = link clock frequency in Mhz/ pixel clock frequency in Mhz.
6:0	RW	0x16	AVERAGE_BYTES_PER_TU This is the average number of valid bytes in a transfer Unit. Driver should program this register based on the video format being transmitted and the link rate and lane configuration being used. Section 2.2.1.4 of the DP 1.43 spec give details on how this average symbol count should be calculated. In MST mode, this register is programmed with the calculated TS_INT as specified in Section 2.6.4.3 of DisplayPort 1.4 Spec. In MST mode, The driver programs the avarege_bytes_per_tu using the following equation. Average_bytes_per_tu= floor((Peak_stream_bandiwth/Link_bandwidth*64) Here is an example for calculating the Average_bytes_per_tu in MST mode for the video format VIC-1 (640x480) RGB, 8bpc, at a frame rate of 60Hz. The Link is assumed to be HBR 4 lanes. Peak_stream_bandwidth = Pixel_clock_frequency*bytes_per_pixel = 25.175*3 = 75.52MBps Link Bandwidth = link_rate * 100 * number_of_lanes .= 2.7 * 100 *4 = 1080MBps Average_bytes_per_tu = floor((peak_stream_bandwidth/link_bandwidth)*64) = floor((75.52/1080)*64)) = floor(4.475) = 4.

DPTX_VIDEO_MSA1_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0324)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0023	VSTART Vertical start from the leading edge of Vsync, measured in line count. This is the vstart value that is specified in the MSA.This is same as vsync width + Vertical back porch.
15:0	RW	0x0090	HSTART Horizontal active start from leading edge of Hsync, measured in pixel count. This is the hstart value that is specified in the MSA. This is same as hsync width + Horizontal back porch.

DPTX_VIDEO_MSA2_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	MISC0 Bit 24: Synchronous mode of operation. Pixel source reference clock and link reference clock are the same. 1'b0: Asynchronous mode 1'b1: Synchronous mode Bits 31:25: Colorimetry indicator field.
23:0	RW	0x000000	MVID MVID value to be used in case of synchronous mode of operation (pixel source reference clock and link reference clock are the same). See section 2.2.3 of the DisplayPort 1.3 spec. This value goes in the MSA. If the clocks are asynchronous, controller internally calculates this value

DPTX_VIDEO_MSA3_STREAM0

Address: Operational Base(0x27E40000) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	MISC1 24-Interlaced Vertical Total Even 26:25 Stereo Video Attribute 31:30-Pixel Encoding/colorimetry Format indicator field
23:0	RW	0x000000	NVID NVID value to be used in case of synchronous mode of operation (pixel source reference clock and link reference clock are the same). See section 2.2.3 of the DisplayPort 1.3 spec. This value goes in the MSA. If the clocks are asynchronous, controller internally calculates this value.

DPTX_VIDEO_HBLANK_INTERVAL_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	HBLANK_INTERVAL For MST mode the programmed value should be (Hblank/16 *average_bytes_per_tu*link_clk/pixel_clk. Link_clk and pixel_clk are in Mhz. The link clock is based on the internal 32 bit datapath. In SST mode, it should be hblank *link_clk/pixel_lk.

DPTX_AUD_CONFIG1_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:24	RW	0x12	AUDIO_TIMESTAMP_VERSION_ Audio timestamp version number.This is used as HB3[7:2] of Audio Timestamp SDP. As per DP 1.3 Spec, this should be h'12 .Some compliance testers still look for old values, and therefore added this register field.
23:16	RW	0x00	AUDIO_PACKET_ID Defines the first byte of the audio SDP and the audio time stamp SDP header. Used for associating the audio sdp to the timestamp with multiple audio streams.
15	RW	0x0	AUDIO_MUTE Controls the AudioMute_Flag in the VB-ID. 1'b1: Sets the AudioMute_Flag in VB-ID 1'b0: Clears the AudioMute_Flag in VB-ID.
14:12	RW	0x1	NUM_CHANNELS Number of audio channels 1'b0: 1channel 1'b1: 2channels others: 8channels.
11	RO	0x0	reserved
10	RW	0x0	HBR_MODE_ENABLE Audio input is operating in HBR mode if set to '1'. When audio_if_select is 1 (S/PDIF), 768kHz x 2 Channels x 16 bits is delivered to controller. When '0' (I2s) 192kHz x 8 x 16 bits in 8-channel is delivered to controller.
9:5	RW	0x10	AUDIO_DATA_WIDTH Audio input data width audio_data_width4:0 Action 5'b00000-5'b01111: Not used 5'b10000: 16 bit data samples at input 5'b10001: 17 bit data samples at input 5'b10010: 18 bit data samples at input 5'b10011: 19: bit data samples at input 5'b10100: 20: bit data samples at input 5'b10101: 21: bit data samples at input 5'b10110: 22: bit data samples at input 5'b10111: 23: bit data samples at input 5'b11000: 24: bit data samples at input 5'b11001-5'b11111: Not Used
4:1	RW	0x1	AUDIO_DATA_IN_EN Specifies which of the audio data inputs are active. Used to control I2sSPDIF input data. audio_data_in_en0 and ispdfidata0i2sdata_i0 enabled indicates channels12 is active audio_data_in_en1, ispdfidata1, and i2sdata_i1 enabled indicates channels3 and channels4 are active. audio_data_in_en2, ispdfidata2, and i2sdata_i2 enabled indicates channels5 and channels6 are active. audio_data_in_en3, ispdfidata3, and i2sdata_i3 enabled indicates that channels7 and channels8 are active. Value of 0 is invalid.
0	RW	0x0	AUDIO_INF_SELECT 1'b0: I2S is the selected audio input interface (Default). 1'b1: SPDIF is the selected audio input interface.

DPTX_SDP_VERTICAL_CTRL_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0500)

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Bit	Attr	Reset Value	Description
31	RW	0x0	FIXED_PRIORITY_ARBITRATIO When this bit is set then the scheduler searches for the next SDP to transmit based on fixed priority, otherwise it uses Round-Robin arbitration. Fixed priority means that lower numbered register sets has higher priority than higher numbered register sets.
30	RW	0x0	DISABLE_EXT_SDP When set the external SDP interface is disabled. No external SDPs are transmitted. This bit is applicable for both the vertical and horizontal blanking.
29:25	RO	0x00	reserved
24	RW	0x0	EN_128BYTES_SDP_1 When set, register bank 1, 2, 3 and 4 are used to form a 128bytes SDP. The SW should program a single 4bytes header followed by 128bytes of data and set a single enable bit that corresponds to bank 1.
23:20	RO	0x0	reserved
19:2	RW	0x00000	EN_VERTICAL_SDP_N When set, DWC_dptx sends out SDP during the vertical intervals, using the information provided in the SDP_REGISTER BANK[n*9-1:n*9]
1	RW	0x0	EN_AUDIO_STREAM_SDP When cleared, no Audio stream is sent during the vertical blanking period. When '1' audio stream is transmitted during vertical blanking period.
0	RW	0x0	EN_AUDIO_TIMESTAMP_SDP When set, DWC_dptx sends out audio timestamp SDP once every video frame during the vertical blanking period. This SDP is always transmitted as the first SDP in the blanking period. Payload for the audio timestamp SDP and the header are internally generated by the controller.

DPTX_SDP_HORIZONTAL_CTRL_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31	RW	0x0	FIXED_PRIORITY_ARBITRATION When this bit is set then the scheduler searches for the next SDP to transmit based on fixed priority, otherwise it uses Round-Robin arbitration. Fixed priority means that lower numbered register sets has higher priority than higher numbered register sets.
30:20	RO	0x000	reserved
19:2	RW	0x00000	EN_HORIZONTAL_SDP_N When set, DWC_dptx sends out SDP during the horizontal intervals, using the information provided in the SDP_REGISTER BANK[n*9-1:n*9]
1	RW	0x0	EN_AUDIO_STREAM_SDP When cleared, no Audio stream is sent during horizontal blanking. When '1' audio stream is transmitted during horizontal blanking period.
0	RW	0x0	EN_AUDIO_TIMESTAMP_SDP When set, DWC_dptx sends out audio timestamp SDP once every horizontal blanking. Payload for the audio timestamp SDP and the header are internally generated by the controller.

DPTX_SDP_STATUS_REGISTER_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0508)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:2	W1C	0x00000	SDP_N_TX_STATUS Status indicating the transmission of corresponding Nth SDP. Set to 1 by the hardware in both Auto and Manual modes. Software writes a 1 to clear this bit.
1	W1C	0x0	AUDIO_STREAM_SDP_STATUS Status indicating the transmission of a audio SDP. Set to 1 by the hardware in both Auto and Manual modes. Software writes a 1 to clear this bit.
0	W1C	0x0	AUDIO_TIMESTAMP_SDP_STAT Status indicating the transmission of an audio timestamp SDP. Set to 1 by the hardware in both Auto and Manual modes. Software writes a 1 to clear this bit.

DPTX_SDP_MANUAL_CTRL_STREAM0

Address: Operational Base(0x27E40000) + offset (0x050C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	MANUAL_MODE_SDP Setting this bit when the corresponding bit in the SDP_VERTICAL_CTRL/SDP_HORIZONTAL_CTRL registers causes the corresponding SDP to be transmitted once. After the transmission, both corresponding enable bits are reset. If the transmission done during the Vertical or the Horizontal blanking period then the enable bit in both the SDP_VERTICAL_CTRL and SDP_HORIZONTAL_CTRL registers are reset.This provides the Software the ability to decide whether a SDP is transmitted once during the Vertical period, or Horizontal period or which ever comes first.

DPTX_SDP_STATUS_EN_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0510)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:2	RW	0x00000	SDP_STATUS_EN Setting this bit to 1 enables interrupt generation due to transmission of the corresponding SDP
1	RW	0x0	AUDIO_STREAM_SDP_STATUS Setting this bit to 1 enables interrupt generation due to transmission of an audio SPD
0	RW	0x0	AUDIO_TIMESTAMP_SDP_STAT Setting this bit to 1 enables interrupt generation due to transmission of a audio timestamp SPD

DPTX_SDP_REGISTER_BANK_STREAM0

Address: Operational Base(0x27E40000) + offset (0x0600)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SDP_REGS The register bank is split to SDPs where each SDP is the size of nine 32bits registers. The first register contains the SDP header and the other eight the data payload. For example, if DWC_DPTX_NUM_SDP_REGISTER_BANKS is 10, then 90 32bits registers are defined. The register set [8:0] specifies s SDP which is transmitted if the corresponding bit in SDP_AUTOEN_CTRL is set, whether the corresponding bit located at [2]. The next SDP, registers [17:9] are enabled by bit [3] in SDP_AUTOEN_CTRL.

DPTX_PHYIF_CTRL

Address: Operational Base(0x27E40000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:26	RW	0x0	EDP_PHY_RATE Support for the eDP rates. 3'b000: PHY rates as defined by bits 5:4 of this register (PHYRATE) are used. 3'b001: R216(2.16Gbps) 3'b010: R243(2.43Gbps) 3'b011: R324(3.24Gbps) 3'b100: R432(4.32Gbps)
25	RW	0x0	PHY_WIDTH This bit is used to configure the data width of the main link interface to the PHY. 1'b0: 20-bit interface 1'b1: 40-bit interface The power-on reset value of this bit can be configured by parameter.
24:21	RO	0x0	reserved
20:17	RW	0x3	PHY_POWERDOWN PHY power-down control.The value written in this field controls the Powerdown on all the lanes. x0: Powered on x2: Intermediate P2 power state for switching rates. x3: PHY is powered down phy_clk might stop xC: P4 Power state. PHY is powered down, reference clock can be stopped. Others: Reserved.
16	RW	0x0	SSC_DIS Disable SSC on the PHY.

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	PHY_BUSY Status from the PHY per lane: Bit 12: Lane 0 Bit 13: Lane 1 Bit 14: Lane 2 Bit 15: Lane 3 This bit for each lane is set when a power state change or rate change is requested and cleared when the PHY sends a phy_laneX_phystatus pulse. This bit is also be set when phy_reset is asserted and cleared when phy_laneX_phystatus drops to 0 after reset finishes. No changes to PHY_RATE or PHY_POWERDOWN are to occur when PHY_BUSY is high. PHY_BUSY only go high in response to PHY_RATE PHY_POWERDOWN or a reset. PHY_BUSY must go high if phy_laneX_phystatus is set. The time between when this signal asserts till deassertion is specific to PHY implementation. Software can implement a timeout that is appropriate to the PHY. Generally this is 100ms.
11:8	RW	0x0	XMIT_ENABLE Enable transmitter on the PHY per lane. If TPS_SEL is 0 then main link provides the data to be transmitted. If PHY_POWERDOWN is not 0 then the transmitter is not enabled on the PHY interface. Bit 8: Lane 0 Bit 9: Lane 1 Bit 10: Lane 2 Bit 11: Lane 3
7:6	RW	0x0	PHY_LANES Number of lanes active: 2'b00: 1 Lane 2'b01: 2 Lanes 2'b10: 4 Lanes
5:4	RW	0x0	PHYRATE Rate setting for the PHY. If the Synopsys Combo PHY is used, the software must first program PHY_POWERDOWN to 2 or 3 first and waiting for PHYBUSY to clear. Afterwards, rate can be changed along with PHY_POWERDOWN. 2'b00: RBR 1.62 Gbs 2'b01: HBR 2.7 Gbs 2'b10: HBR2 5.4 Gbs 2'b11: HBR3 8.1 Gbs

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	TPS_SEL Selects the training pattern to be transmitted to the PHY: 0: No training pattern is transmitted. Main link data is transmitted instead. 1: TPS1, D10.2 2: TPS2 3: TPS3 4: TPS4, CP2520 Pattern 3 5: Symbol Error Rate Measurement pattern 6: PRBS7 7: Custom 80-bit pattern. CUSTOMPAT0, CUSTOMPAT1, and CUSTOMPAT2 must be set to a valid pattern before this select is programmed 8: CP2520 Pattern 1 - As defined by PHY CTS 1.2b 9: CP2520 Pattern 2- - As defined by

DPTX_PHY_TX_EQ

Address: Operational Base(0x27E40000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	LANE3_TX_POST_CUR2 Lane 3 Pre-emphasis Post Cursor2 Level. Controls the phy_lane0_tx_post_cur21:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2
21:20	RW	0x0	LANE3_TX_VSWING Lane 3 Voltage Swing Level. Controls the phy_lane0_tx_vswing1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
19:18	RW	0x0	LANE3_TX_PREEMP Lane 3 Pre-emphasis Level. Directly controls the phy_lane0_tx_pre_emp1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
17:16	RW	0x0	LANE2_TX_POST_CUR2 Lane 2 Pre-emphasis Post Cursor2 Level. Controls the phy_lane0_tx_post_cur21:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2
15:14	RW	0x0	LANE2_TX_VSWING Lane 2 Voltage Swing Level. Controls the phy_lane0_tx_vswing1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	LANE2_TX_PREEMP Lane 2 Pre-emphasis Level. Directly controls the phy_lane0_tx_pre_emp1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	LANE1_TX_POST_CUR2 Lane 1 Pre-emphasis Post Cursor2 Level. Controls the phy_lane0_tx_post_cur21:0 output. 2'b00: Level 0 2'b10: Level 1 2'b10: Level 2
9:8	RW	0x0	LANE1_TX_VSWING Lane 1 Voltage Swing Level. Controls the phy_lane0_tx_vswing1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	LANE1_TX_PREEMP Lane 1 Pre-emphasis Level. Directly controls the phy_lane0_tx_pre_emp1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	LANE0_TX_POST_CUR2 Lane 0 Pre-emphasis Post Cursor2 Level. Controls the phy_lane0_tx_post_cur21:0 output. 2'b00: Level 0 2'b10: Level 1 2'b10: Level 2
3:2	RW	0x0	LANE0_TX_VSWING Lane 0 Voltage Swing Level. Controls the phy_lane0_tx_vswing1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	LANE0_TX_PREEMP Lane 0 Pre-emphasis Level. Directly controls the phy_lane0_tx_pre_emp1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

DPTX_CUSTOMPAT0

Address: Operational Base(0x27E40000) + offset (0x0A08)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:0	RW	0x00000000	CUSTOM80B_0 Lower 30-bits of the 80-bit pattern. This corresponds to 29:0 of the 80-bit pattern. Note: All 80-bits of CUSTOMPAT0 CUSTOMPAT1 and CUSTOMPAT2 must be programmed. The symbol at 9:0 is transmitted first.

DPTX_CUSTOMPAT1

Address: Operational Base(0x27E40000) + offset (0x0A0C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	CUSTOM80B_1 Next 30-bits of the 80-bit pattern. This corresponds to 59:30 of the 80-bit pattern. Note: All 80-bits of CUSTOMPAT0 CUSTOMPAT1 and CUSTOMPAT2 must be programmed.

DPTX_CUSTOMPAT2

Address: Operational Base(0x27E40000) + offset (0x0A10)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	CUSTOM80B_2 Highest 20-bits of the 80-bit pattern. This corresponds to 79:60 of the 80-bit pattern. Note: All 80-bits of CUSTOMPAT0 CUSTOMPAT1 and CUSTOMPAT2 must be programmed.

DPTX_HBR2_COMPLIANCE_SCRAMBLER_RESET

Address: Operational Base(0x27E40000) + offset (0x0A14)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x00fc	NUM_SR_ZEROS Number of scrambled 0 symbols to be output for every Enhanced Framing Scrambler Reset sequence SR-BF-BFSR when CP2520 Pattern 1, 2, or 3 is transmitted. Count includes the reset sequence. Value less than four causes scrambled 0 symbols to be output with no scrambler reset sequence. Default value is required for PHY CTS is 16'd252 = SR sequence 4 + 248 zeros

DPTX_PHYIF_PWRDOWN_CTRL

Address: Operational Base(0x27E40000) + offset (0x0A18)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	PER_LANE_PWRDOWN_CTL_E Per lane power-down control enable
15:12	RW	0x0	POWER_DOWN_CTRL_LANE3 PowerDown control for Lane-3. x0: Powered on x2: Intermediate P2 power state for switching rates. x3: PHY is powered down phy_clk might stop xC: P4 Power state. PHY is powered down, reference clock can be stopped. Others: Reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	POWER_DOWN_CTRL_LANE2 PowerDown control for Lane-2. x0: Powered on x2: Intermediate P2 power state for switching rates. x3: PHY is powered down phy_clk might stop xC: P4 Power state. PHY is powered down, reference clock can be stopped. Others: Reserved
7:4	RW	0x0	POWER_DOWN_CTRL_LANE1 PowerDown control for Lane-1. x0: Powered on x2: Intermediate P2 power state for switching rates. x3: PHY is powered down phy_clk might stop xC: P4 Power state. PHY is powered down, reference clock can be stopped. Others: Reserved
3:0	RW	0x0	POWER_DOWN_CTRL_LANE0 PowerDown control for Lane-0. x0: Powered on x2: Intermediate P2 power state for switching rates. x3: PHY is powered down phy_clk might stop xC: P4 Power state. PHY is powered down, reference clock can be stopped. Others: Reserved

DPTX_AUX_CMD

Address: Operational Base(0x27E40000) + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	AUX_CMD_TYPE AUX Channel Command: 4'b1000: Native Write 4'b1001: Native Read 4'b0100: I2C MOT Write 4'b0101: I2C MOT Read 4'b0000: I2C Write 4'b0001: I2C Read 4'b0010: I2C Write Status update 4'b0110: I2C MOT Write Status update All other values are reserved and triggers an interrupt, INTERRUPTS.AUX_CMD_INVALID
27:8	RW	0x00000	AUX_ADDR AUX Address
7:5	RO	0x0	reserved
4	RW	0x0	I2C_ADDR_ONLY A value of '1' indicates an I2C over aux address only transfer.
3:0	RW	0x0	AUX_LEN_REQ AUX Length Number of bytes to transmit. 0-15 indicating between 1 to 16 bytes of data. A value of '0' should be programmed for an I2C over aux address only

DPTX_AUX_STATUS

Address: Operational Base(0x27E40000) + offset (0x0B04)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	AUX_STATE Reflects the current state of the AUX state machine. Used for hardware debug only.
27:25	RO	0x0	AUX_REPLY_ERR_CODE Error code. Valid when sink aux reply error is detected. Used for hardware debug purpose only.
24	RW	0x0	SINK_DISCONNECT_WHILE_AC The bit is set to 1 if the SINK disconnect was detected while active AUX transfer
23:19	RO	0x00	AUX_BYTES_READ The number of valid bytes received as a reply from the SINK
18	RW	0x0	AUX_REPLY_ERR The bit is set to 1 if a reply error is detected. An error could be an illegal Manchester code, or if the source and sink are out of sync. The specific error code is in bits 27:25 of this register.
17	RO	0x0	AUX_TIMEOUT The bit is set to 1 if no reply is received within 400us after a request has been sent on the AUX channel.
16	RO	0x0	AUX_REPLY_RECEIVED If '1' then Indicates an active AUX transfer. When '0' indicates that an AUX_REPLY has been received and the AUX status/data registers are valid. Note: If the AUX transfer was not successful such that the AUX transfer timed out or an error detected then the Status & Data registers might not have valid values.
15:8	RO	0x00	AUX_M The second byte received from the Sink as a reply to an AUX transfer. This value is the number of bytes written.
7:0	RO	0x00	AUX_STATUS The first byte received from the Sink as a reply to an AUX transfer. The higher 4-bits are the actual reply: 4'b0000: AUX/I2C ACK 4'b0001: AUX NACK 4'b0010: AUX Defer 4'b0100: I2C NACK 4'b1000: I2C DEFER

DPTX_AUX_DATA0

Address: Operational Base(0x27E40000) + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUX_DATA0 AUX Data - First 4 bytes. If only 1 byte is to be written in the transaction, then only 3:0 has valid data

DPTX_AUX_DATA1

Address: Operational Base(0x27E40000) + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUX_DATA1 AUX Data Second 4 bytes

DPTX_AUX_DATA2

Address: Operational Base(0x27E40000) + offset (0x0B10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUX_DATA2 AUX Data Third 4 bytes

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DPTX_AUX_DATA3

Address: Operational Base(0x27E40000) + offset (0x0B14)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	AUX_DATA3 AUX Data Fourth 4 bytes

DPTX_PHYREG_CMDADDR

Address: Operational Base(0x27E40000) + offset (0x0C00)

Bit	Attr	Reset Value	Description
31	RW	0x0	PHY_READ Initiate the read into the PHY register. This bit self-clears when the read completes and PHYREG_DATA contains valid read data.
30	RW	0x0	PHY_WRITE Initiate the write into the PHY register. This bit self-clears when the write completes in the hardware.
29:16	RO	0x0000	reserved
15:0	RW	0x0000	PHY_ADDRESS Address bus for the PHY register interface

DPTX_PHYREG_DATA

Address: Operational Base(0x27E40000) + offset (0x0C04)

Bit	Attr	Reset Value	Description
31	RW	0x0	PHY_DONE Indicates that the data is ready to be read from the PHYREG_DATA register if a read was initiated or that a write was completed
30:16	RO	0x0000	reserved
15:0	RW	0x0000	PHY_DATA Address bus for the PHY register interface

DPTX_TYPEC_CTRL

Address: Operational Base(0x27E40000) + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	W1C	0x0	TYPEC_INTERRUPT_STATUS This is the interrupt status pin for TYPE-C. On a type-C interrupt software reads this register to confirm a Type-C binterrupt. Writing 1 by the software clears the TYPE-C interrupt.
1	RO	0x0	TYPEC_DISABLE_STATUS This is a read only register bit which directly reflects the status of the primary input pin tca_disable_i.After receiving a TYPE_C interrupt, software reads this register bit to get the status of the tca_disable.
0	RW	0x0	TYPEC_DISABLE_ACK This register bit controls the primary output pin tca_disable_ack_o.The value in this register is directly reflected on the output. Software sets or clears this bit based on the Type-C interrupt.

DPTX_GENERAL_INTERRUPT

Address: Operational Base(0x27E40000) + offset (0x0D00)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30	RO	0x0	DSC_EVENT An DSC event has occurred. Please read DSC register DSCINTSTAT to see the cause of the event. To reset the bit software need to clear the status at the source, in the DSCINTSTAT by writing to DSCINTSTAT register
29:27	RO	0x0	reserved
26	W1C	0x0	VIDEO_FIFO_OVERFLOW_STREAM3 Indicates that the video lane steering FIFO for stream2 gets an overflow. The likely cause is that the bytes_per TU programmed in the VIDEO_CONFIG5.AVERAGE_BYTES_PER_TU is wrong or the lane/rate chosen for the video format is not correct for stream2. This bit is used for debug only
25	RW	0x0	AUDIO_FIFO_OVERFLOW_STREAM3 Indicates that one or more of the audio sampler FIFOs are getting into overflow condition for stream3. This is an vindication that the audio samples are not getting drained out and is an indication that the bandwidth of the selected audio does not match with the video format being used for stream3.
24	RW	0x0	SDP_EVENT_STREAM3 An event indicating the completion of transmission of an SDP for stream3. For details on the specific SDPs that got transmitted refer to SDP Status register for stream3. To reset the bit the SW needs to clear the status at the source, in the SDP status register for stream3.
23:21	RO	0x0	reserved
20	W1C	0x0	VIDEO_FIFO_OVERFLOW_STREAM2 Indicates that the video lane steering FIFO for stream2 gets an overflow. The likely cause is that the bytes_per TU programmed in the VIDEO_CONFIG5.AVERAGE_BYTES_PER_TU is wrong or the lane/rate chosen for the video format is not correct for stream2. This bit is used for debug only
19	RW	0x0	AUDIO_FIFO_OVERFLOW_STREAM2 Indicates that one or more of the audio sampler FIFOs are getting into overflow condition for stream2. This is an indication that the audio samples are not getting drained out and is an indication that the bandwidth of the selected audio does not match with the video format being used for stream2.
18	RO	0x0	SDP_EVENT_STREAM2 An event indicating the completion of transmission of an SDP for stream2. For details on the specific SDPs that got transmitted refer to SDP Status register for stream2. To reset the bit the SW needs to clear the status at the source, in the SDP status register for stream2.
17:15	RO	0x0	reserved
14	W1C	0x0	VIDEO_FIFO_OVERFLOW_STREAM1 Indicates that the video lane steering FIFO for stream1 gets an overflow. The likely cause is that the bytes_per TU programmed in the VIDEO_CONFIG5.AVERAGE_BYTES_PER_TU is wrong or the lane/rate chosen for the video format is not correct for stream1. This bit is used for debug only
13	RW	0x0	AUDIO_FIFO_OVERFLOW_STREAM1 Indicates that one or more of the audio sampler FIFOs are getting into overflow condition for stream1. This is an indication that the audio samples are not getting drained out and is an indication that the bandwidth of the selected audio does not match with the video format being used for stream1.

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Bit	Attr	Reset Value	Description
12	RO	0x0	SDP_EVENT_STREAM1 An event indicating the completion of transmission of an SDP for stream1. For details on the specific SDPs that got transmitted refer to SDP Status register for stream1. To reset the bit the SW needs to clear the status at the source, in the SDP status register for stream1.
11:8	RO	0x0	reserved
7	RO	0x0	TYPE_C_EVENT Indicates an event related to Type-C assit block. This could be an indication that the Type-C assit input pin tca_disable has changed. Read TYPE-C_CTRL register for more details.To reset this bit software need to clear the status in TYPEC_CTRL register by writing 1 to TYPEC_INTERRUPT_STATUS bit.
6	W1C	0x0	VIDEO_FIFO_OVERFLOW_STREAM0 Indicates that the video lane steering FIFO for stream0 gets an overflow. The likely cause is that the bytes_per TU programmed in the VIDEO_CONFIG5.AVERAGE_BYTES_PER_TU is wrong or the lane/rate chosen for the video format is not correct for stream0. This bit is used for debug only
5	RW	0x0	AUDIO_FIFO_OVERFLOW_STREAM0 Indicates that one or more of the audio sampler FIFOs are getting into overflow condition for stream0. This is an indication that the audio samples are not getting drained out and is an indication that the bandwidth of the selected audio does not match with the video format being used for stream0.
4	RO	0x0	SDP_EVENT_STREAM0 An event indicating the completion of transmission of an SDP for stream0. For details on the specific SDPs that got transmitted refer to SDP Status register for stream0. To reset the bit the SW needs to clear the status at the source, in the SDP status register for stream0.
3	W1C	0x0	AUX_CMD_INVALID After initiating an AUX request, this bit is set to 1, if the command or length was invalid. The AUX request is not sent out on the AUX Channel if this bit is set
2	RO	0x0	HDCP_EVENT An HDCP event has occurred. Please read HDCP register HDCPAPIINTSTAT to see the cause of the event. To reset the bit software need to clear the status at the source, in the HDCPAPIINTSTAT by writing to HDCPAPIINTCLR register.
1	W1C	0x0	AUX_REPLY_EVENT After initiating an AUX request this bit is set to 1 after receiving a reply.
0	RO	0x0	HPD_EVENT This bit indicates that an HPD event is captured in the HPD status register. To reset the bit the SW needs to clear the status at the source in the HPD status register.

DPTX_GENERAL_INTERRUPT_ENABLE

Address: Operational Base(0x27E40000) + offset (0x0D04)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	DSC_EVENT_EN Enable for DSC event. Set to 1 to enable events related to DSC.

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Bit	Attr	Reset Value	Description
29:27	RO	0x0	reserved
26	RW	0x0	VIDEO_FIFO_OVERFLOW_EN_STREAM3 Enable for VIDEO_FIFO_OVERFLOW for stream3. Set 1 to mask this event.
25	RW	0x0	AUDIO_FIFO_OVERFLOW_EN_STREAM3 Enable for AUDIO_FIFO_OVERFLOW for stream23. Set 1 to enable this event.
24	RW	0x0	SDP_EVENT_EN_STREAM3 Global enable for SDP event for stream3. Set 1 to enable the SDP event.
23:21	RO	0x0	reserved
20	RW	0x0	VIDEO_FIFO_OVERFLOW_EN_STREAM2 Enable for VIDEO_FIFO_OVERFLOW for stream2. Set 1 to mask this event.
19	RW	0x0	AUDIO_FIFO_OVERFLOW_EN_STREAM2 Enable for AUDIO_FIFO_OVERFLOW for stream2. Set 1 to enable this event.
18	RW	0x0	SDP_EVENT_EN_STREAM2 Global enable for SDP event for stream2. Set 1 to enable the SDP event.
17:15	RO	0x0	reserved
14	RW	0x0	VIDEO_FIFO_OVERFLOW_EN_STREAM1 Enable for VIDEO_FIFO_OVERFLOW for stream1. Set 1 to mask this event.
13	RW	0x0	AUDIO_FIFO_OVERFLOW_EN_STREAM1 Enable for AUDIO_FIFO_OVERFLOW for stream1. Set 1 to enable this event.
12	RW	0x0	SDP_EVENT_EN_STREAM1 Global enable for SDP event for stream1. Set 1 to enable the SDP event.
11:8	RO	0x0	reserved
7	RW	0x0	TYPE_C_EVENT_EN Enable for TYPE_C_EVENT Set to 1 to enable this event.
6	RW	0x0	VIDEO_FIFO_OVERFLOW_EN_STREAM0 Enable for VIDEO_FIFO_OVERFLOW for stream0. Set 1 to mask this event.
5	RW	0x0	AUDIO_FIFO_OVERFLOW_EN_STREAM0 Enable for AUDIO_FIFO_OVERFLOW for stream0. Set 1 to enable this event.
4	RW	0x0	SDP_EVENT_EN_STREAM0 Global enable for SDP event for stream0. Set 1 to enable the SDP event.
3	RW	0x0	AUX_CMD_INVALID_EN Enable for AUX_CMD_INVALID. Set to 1 to enable this event.
2	RW	0x0	HDCP_EVENT_EN Enable for HDCP event. Set to 1 to enable events related to HDCP.
1	RW	0x0	AUX_REPLY_EVENT_EN Enable for Set to 1 to enable this event.
0	RW	0x0	HPD_EVENT_EN Enable for HPD_EVENT. Set to 1 to enable this event.

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DPTX_HPD_STATUS

Address: Operational Base(0x27E40000) + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	HPD_TIMER This field is the raw HPD timer value. Resets to 0 whenever HPD toggles and starts counting afterwards. If no other event occurs this timer increments until a plugunplug event is detected. The unit of measure is in microseconds. This value is used for debugging.
11:9	RO	0x0	HPD_STATE The HPD state machine state. Used for debug but SW can also use the info to determine the status after receiving an interrupt. SOURCE_STATE_IDLE= 3'd0 Sink is not connected SOURCE_STATE_UNPLUG= 3'd1 HPD gets deasserted after being in the plugged state. In this state for 2mSec. SOURCE_STATE_HPD_TIMEOUT= 3'd4 The HPD is deasserted for more than 2mSec but less than 100mSec SOURCE_STATE_PLUG = 3'd7 HPD is high, the Sink is connected
8	RO	0x0	HPD_STATUS Current status of the HPD input. This value must be qualified with the HPD_TIMER.
7:4	RO	0x0	reserved
3	W1C	0x0	HPD_UNPLUG_ERR Unplug detected. This bit is set to 1 after the HPD is deasserted for less than 250uSec.
2	W1C	0x0	HPD_HOT_UNPLUG Unplug detected. This bit is set to 1 after the HPD is deasserted for at least 2mSec.
1	W1C	0x0	HPD_HOT_PLUG Hot plug detected. This bit is asserted after the sink is plugged and asserts HPD for at least 100mSec. It is also asserted If the sink was plugged then deasserts HPD for more then 2mSec but less than 100mSec. In this case this bit is set as soon as HPD is asserted by the sink. No debounce time is implemented.
0	W1C	0x0	HPD_IRQ IRQ from the HPD. This bit is set to 1 after a low pulse on HPD has been detected between 0.25-2.0 ms

DPTX_HPD_INTERRUPT_ENABLE

Address: Operational Base(0x27E40000) + offset (0x0D0C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	HPD_UNPLUG_ERR_EN Enable for HPD_UNPLUG_ERR. Setting to 1 enables this event to assert the interrupt output.
2	RW	0x0	HPD_UNPLUG_EN Enable for HPD_UNPLUG. Setting to 1 enables this event to assert the interrupt output.
1	RW	0x0	HPD_PLUG_EN Enable for HPD_PLUG. Setting to 1 enables this event to assert the interrupt output.
0	RW	0x0	HPD_IRQ_EN Enable for IRQ_HPD. Setting to 1 enables this event to assert the interrupt output.

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DPTX_HDCPCFG

Address: Operational Base(0x27E40000) + offset (0x0E00)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	DPCD12PLUS DPCD revision of Sink is 1.2 or higher. Updated by software after reading the DPCD revision
6	RW	0x0	CP_IRQ CP_IRQ indication to HDCP controller. Software sets this bit on CP_IRQ interrupt
5	RW	0x0	BYPENCRYPTION Bypasses all the data encryption stages.
4	RW	0x0	HDCP_LOCK Lock the HDCP bypass and encryption disable mechanisms: 1b0: The default 1b0 value enables you to bypass HDCP through bit 5 bypencryption of the HDCPCFG register or to disable the encryption through bit 3 encryptiondisable of HDCPCFG register. 1b1: You can still write to the bit bypencryption of HDCPCFG or encryptiondisable bit of HDCPCFG but you cannot enable the bypass or disable encryption. Once you set the value to 1b1 you can change the value back to 1b0 only by issuing a master reset to the DWC_dptx.
3	RW	0x0	ENCRYPTIONDISABLE Disable encryption without losing authentication
2	RW	0x0	ENABLE_HDCP_13 1'b0: Default HDCP 2.2 is enabled 1'b1: HDCP 1.3 is enabled
1	RW	0x0	ENABLE_HDCP Enable HDCP functionality. This signal is tied to I_px_gpio_in[0] of HDCP2.2 Controller clears this bit under the following condition Re-authentication request from the sink.
0	RO	0x0	reserved

DPTX_HDCPOBS

Address: Operational Base(0x27E40000) + offset (0x0E04)

Bit	Attr	Reset Value	Description
31	W1C	0x0	HDCP22_RE_AUTHENTICATION_REQ Indicates that the Sink has requested a re-authentication. Cleared when software writes a 1 to this bit.
30	W1C	0x0	HDCP22_AUTHENTICATION_FAILED Set to 1 when by the hardware when the authentication is failed. Cleared when software writes a 1.
29	W1C	0x0	HDCP22_AUTHENTICATION_SUCCESS Set to 1 when by the hardware when the authentication is succeeded. Cleared when software writes a 1.
28	RO	0x0	HDCP22_CAPABLE_SINK 1'b1: HDCP 22 sink 1'b0: Sink not HDCP22 capable. If enable_hdcp_13 is set and this bit is already set then controller clears it. Re-authentication request also clears this bit.
27	W1C	0x0	HDCP22_SINK_CAP_CHECK_C Sets when the capability check is complete. Cleared when software writes a 1 to this bit.

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Bit	Attr	Reset Value	Description
26:24	RO	0x0	HDCP22_STATE Status of HDCP operation 3'B001: Initializing 3'B010: Authenticating 3'B011: Authenticated 3'B100: not Authenticated
23	W1C	0x0	HDCP22_BOOTED Status indicting the HDCP22 has booted. Cleared when software writes a 1 to this bit.
22:19	RO	0x0	HDCP13_BSTATUS Status indicting the HDCP22 has booted. Cleared when software writes a 1 to this bit.
18	RO	0x0	REPEATER Register read from attached sink device: Bcap bit 1
17	RO	0x0	HDCP_CAPABLE Register read from attached sink device: Bcap bit 0
16:14	RO	0x0	STATEE Observability register informs in which state the cipher machine is on.
13:11	RO	0x0	STATEOEG Observability register informs in which state the DPES machine is on.
10:8	RO	0x0	STATER Observability register informs in which state the revocation machine is on.
7:4	RO	0x0	STATEA Observability register informs in which state the authentication machine is on.
3:1	RO	0x0	SUBSTATEA Observability register informs in which sub-state the authentication is on
0	RO	0x0	HDCPENGAGED Informs that the current DP link has the HDCP protocol fully engaged.

DPTX_HDCPAPIINTCLR

Address: Operational Base(0x27E40000) + offset (0x0E08)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	WO	0x0	HDCP22_GPIOINT Clears the interruption related to HDCP22 GPIO output status change.
7	WO	0x0	HDCP_ENGAGED Clears the interruption related to HDCP authentication process successful.
6	WO	0x0	HDCP_FAILED Clears the interruption related to HDCP authentication process failed.
5	WO	0x0	KSVSHA1CALCDONEINT Clears the interruption related to SHA1 verification has been done.
4	WO	0x0	AUXRESPNACK7TIMES Clears the interrupt related to aux transfer Nak response for 7 times.

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Bit	Attr	Reset Value	Description
3	WO	0x0	AUXRESPTIMEOUT Clears the interrupt related to aux transfer response timeout.
2	WO	0x0	AUXRESPDEFER7TIMES Clears the interrupt related to aux transfer defer response for 7 times.
1	RO	0x0	reserved
0	WO	0x0	KSVACCESSINT Clears the interrupt related to KSV memory access grant for Read-Write access.

DPTX_HDCPAPIINTSTAT

Address: Operational Base(0x27E40000) + offset (0x0E0C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	HDCP22_GPIOINT Notifies a change in HDCP22 GPIO Output status.
7	RO	0x0	HDCP_ENGAGED Notifies that the HDCP authentication process was successful.
6	RO	0x0	HDCP_FAILED Notifies that the HDCP authentication process was failed.
5	RO	0x0	KSVSHA1CALCDONEINT Notifies that the HDCP13TCTRL controller SHA1 verification has been done. The status ready to be read.
4	RO	0x0	AUXRESPNACK7TIMES Notifies that the aux transfer initiated by HDCP13TCTRL received nack response continuously for 7 times.
3	RO	0x0	AUXRESPTIMEOUT Notifies that the aux transfer initiated by HDCP13TCTRL did not receive a response and timedout.
2	RO	0x0	AUXRESPDEFER7TIMES Notifies that the aux transfer initiated by HDCP13TCTRL received defer response continuously for 7 times
1	RO	0x0	reserved
0	RO	0x0	KSVACCESSINT Notifies that the KSV memory access as been guaranteed for Read-Write access.

DPTX_HDCPAPIINTMSK

Address: Operational Base(0x27E40000) + offset (0x0E10)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	HDCP22_GPIOINT Masks the interruption related to HDCP22 GPIO output status change.
7	RW	0x0	HDCP_ENGAGED Masks the interruption related to HDCP authentication process successful.
6	RW	0x0	HDCP_FAILED Masks the interruption related to HDCP authentication process failed.
5	RW	0x0	KSVSHA1CALCDONEINT Masks the interruption related to SHA1 verification has been done.

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Bit	Attr	Reset Value	Description
4	RW	0x0	AUXRESPNACK7TIMES Masks the interrupt related to aux transfer nack response for 7 times.
3	RW	0x0	AUXRESPTIMEOUT Masks the interrupt related to aux transfer defer response for 7 times.
2	RW	0x0	AUXRESPDEFER7TIMES Masks the interrupt related to aux transfer defer response for 7 times.
1	RO	0x0	reserved
0	RW	0x0	KSVACCESSINT Masks the interrupt related to KSV memory access grant for Read-Write access.

DPTX_HDCPKSVMEMCTRL

Address: Operational Base(0x27E40000) + offset (0x0E18)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	KSVSHA1STATUS Notification whether the KSV list message digest is correct from the controller: 1b1: if digest message verification failed 1b0: if digest message verification succeeded.
3:2	RO	0x0	reserved
1	RO	0x0	KSVMEMACCESS Notification that the KSV memory access has been guaranteed.
0	RW	0x0	KSVMEMREQUEST Request access to the KSV memory; must be de-asserted after the access is completed by the system.

DPTX_HDCP_REVOC_RAM_i

Address: Operational Base(0x27E40000) + offset (0x0E20)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	REVOC_RAM_BYTE3 Byte 3 of HDCP revocation ram dword If memory access has not been granted (see register a_ksvmemctrl) the value read is 8hff
23:16	RW	0xff	REVOC_RAM_BYTE2 Byte 2 of HDCP revocation ram dword If memory access has not been granted (see register a_ksvmemctrl) the value read is 8hff
15:8	RW	0xff	REVOC_RAM_BYTE1 Byte 1 of HDCP revocation ram dword If memory access has not been granted (see register a_ksvmemctrl) the value read is 8hff
7:0	RW	0xff	REVOC_RAM_BYTE0 Byte 0 of HDCP revocation ram dword If memory access has not been granted (see register a_ksvmemctrl) the value read is 8hff

DPTX_HDCPREG_BKSV0

Address: Operational Base(0x27E40000) + offset (0x3600)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HDCPREG_BKSV0 Contains the value of BKSV[31:0].

DPTX_HDCPREG_BKSV1

Address: Operational Base(0x27E40000) + offset (0x3604)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	HDCPREG_BKSV1 Contains the value of BKSV[39:32].

DPTX_HDCPREG_ANCONF

Address: Operational Base(0x27E40000) + offset (0x3608)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	OANBYPASS 1'b1: The value of AN used in the HDCP engine comes from the hdcpreg_an0 to hdcpreg_an7 registers. 1'b0: The value of AN used in the HDCP engine comes from the random number input.

DPTX_HDCPREG_AN0

Address: Operational Base(0x27E40000) + offset (0x360C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HDCPREG_AN0 Contains the value of AN[31:0]

DPTX_HDCPREG_AN1

Address: Operational Base(0x27E40000) + offset (0x3610)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HDCPREG_AN1 Contains the value of AN[63:32]

DPTX_HDCPREG_RMLCTL

Address: Operational Base(0x27E40000) + offset (0x3614)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ODPK_DECRYPT_ENABLE When set 1b1 this bit activates the decryption of the Device Private keys.

DPTX_HDCPREG_RMLSTS

Address: Operational Base(0x27E40000) + offset (0x3618)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	IDPK_WR_OK_STS When high 1b1 it indicates that a DPK write is allowed.
5:0	RO	0x00	IDPK_DATA_INDEX Current Device Private Key being written plus one. Position 0 is occupied by the AKSV.

DPTX_HDCPREG_SEED

Address: Operational Base(0x27E40000) + offset (0x361C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	WO	0x0000	HDCPREG_SEED Decryption seed value

DPTX_HDCPREG_DPK0

Address: Operational Base(0x27E40000) + offset (0x3620)

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Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DPK_DATA Encrypted DPK value. dpk[31:0] When this byte is written, a strobe signal is generated that triggers the decryption and/or storage of the DPK word on the DPK internal RAM memory.

DPTX_HDCPREG_DPK1

Address: Operational Base(0x27E40000) + offset (0x3624)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	WO	0x000000	DPK_DATA encrypted DPK value. dpk[55:32]

DPTX_HDCP22GPIOSTS

Address: Operational Base(0x27E40000) + offset (0x3628)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	HDCP22GPIOOUTSTS HDCP22 GPIO OUT Status

DPTX_HDCP22GPIOCHNGSTS

Address: Operational Base(0x27E40000) + offset (0x362C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	HDCP22GPIOOUTCHNGSTS HDCP22 GPIO OUT change status. If set indicates a change in HDCP22 GPIO output status. Write 1 to clear it

DPTX_HDCPREG_DPK_CRC

Address: Operational Base(0x27E40000) + offset (0x3630)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DPK_CRC CRC32 value calculated over encrypted DPK. Application can read this value, compare it against the CRC calculated in application to confirm that the DPK write to controller was successful without any errors.

DPTX_VSAMPLE_CTRL_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10300)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	STREAM_TYPE This is a per stream control defining the stream type. RepeaterAuth_Stream_Manage of HDCP2.2 specification. This field is valid only when HDCP MST are enabled.

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Bit	Attr	Reset Value	Description
24	RW	0x0	ENCRYPTION_ENABLE This is a per stream control to enable encryption. Setting ofthis bit has significance only when operating in MST mode or eDP. In non eDP SST operation, this bit has no significance. In MST mode or when eDP is enabled, this bit control the encryption to be used. In MST mode, this bit control HDCP encryption for a specific stream. HDCPCFG register controls the global enable of HDCP. In eDP mode this bit controls the enabling of ASSR feature as specified in section 3.5 of eDP1.4b spec and Section 2.10 of DP1.4 spec. When eDP is enabled, HDCP should be disabled and HDCPCFG[1] should not be set.
23	RW	0x0	ENABLE_DSC Set this bit to 1 to enable Display Stream Compression (DSC) on this specific stream. The software driver can set this bit only if DSC is enabled during configuration (DWC_DPTX_DSC_EN = 1 or 2). Otherwise writing 1 1 to this bit does not take effect.
22:21	RW	0x0	PIXEL_MODE_SELECT This field is used to select the single/dual/quad pixel mode of operation. 2'b00: Single pixel mode (default) 2'b01: Dual pixel mode 2'b10: Quad pixel mode. 2'b11: Reserved.
20:16	RW	0x00	VIDEO_MAPPING Video input mapping color space/depth Video Input mapping (color space/color depth) with DSC disabled/enabled(VSAMPLE_CTRL.ENABLE_DSC=0/1): 0: RGB 6bits (Reserved) 1: RGB 8bits (RGB 8bits) 2: RGB 10bits (RGB 10bits) 3: RGB 12bits (RGB 12bits) 4: RGB 16bits (Reserved) 5: YCbCR4:4:4 8bits (YCbCr4:4:4 8bits) 6: YCbCr4:4:4 10bits (YCbCr4:4:4 10bits) 7: YCbCr4:4:4 12bits (YCbCr4:4:4 12bits) 8: YCbCr4:4:4 16bits (Reserved) 9: YCbCR4:2:2 8bits (Simple YCbCr4:2:2 8bits) 10: YCbCr4:2:2 10bits (Simple YCbCr4:2:2 10bits) 11: YCbCr4:2:2 12bits (Simple YCbCr4:2:2 12bits) 12: YCbCr4:2:2 16bits (Reserved) 13: YCbCR4:2:0 8bits (YCbCR4:2:0 8bits) 14: YCbCr4:2:0 10bits (YCbCR4:2:0 10bits) 15: YCbCr4:2:0 12bits (YCbCR4:2:0 12bits) 16: YCbCr4:2:0 16bits (Reserved) 17: YOnly 8bits (native YCbCr4:2:2 8bits) 18: YOnly 10bits (native YCbCr4:2:2 10bits) 19: YOnly 12bits (native YCbCr4:2:2 12bits) 20: YOnly 16bits (Reserved) 23: RAW 8bits. (Reserved) 24: RAW 10bits (Reserved) 25: RAW 12bits (Reserved) 27: RAW 16bits (Reserved) Others: Reserved.
15:6	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x0	VIDEO_STREAM_ENABLE 1'b0: Video stream Disable 1'b1: Video stream Enable When set to 0, no video stream is transmitted. Video inputs are ignored and NoVideoStream_flag in the VB-ID is set.
4	RW	0x0	INTERNAL_DE_GENERATOR 1'b1: Enable internal data generator 1'b0: Data enable signal available at the input. When the external logic which drives the pixel data does not generate the video data enable, then enabling this bit forces the controller to generate the video enable internally. Note: This feature is currently not supported and therefore should not be used.
3:0	RO	0x0	reserved

DPTX_VSAMPLE_STUFF_CTRL1_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10304)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	BCB_STUFF_DATA Data to be stuffed on B/Cb data path.
15:3	RO	0x0000	reserved
2	RW	0x0	GY_DATA_STUFFING_EN Enable stuffing on internal G/Y data lines.
1	RW	0x0	RCR_DATA_STUFFING_EN Enable stuffing on internal R/Cr data lines.
0	RW	0x0	BCB_DATA_STUFFING_EN Enable stuffing on internal B/Cb data lines

DPTX_VSAMPLE_STUFF_CTRL2_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10308)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	GY_STUFF_DATA Data to be stuffed on G/Y data path.
15:0	RW	0x0000	RCR_STUFF_DATA Data to be stuffed on R/Cr data path.

DPTX_VINPUT_POLARITY_CTRL_STREAM1

Address: Operational Base(0x27E40000) + offset (0x1030C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	DE_IN_POLARITY de input polarity 1'b1: Active low 1'b0: Active high
1	RW	0x0	HSYNC_IN_POLARITY Hsync input polarity 1'b1: Active high 1'b0: Active low
0	RW	0x0	VSYNC_IN_POLARITY Vsync input polarity 1'b1: Active high 1'b0: Active low

DPTX_VIDEO_CONFIG1_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10310)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0280	HACTIVE Input video Horizontal active pixel region width. Number of Horizontal active pixels [0...8191].
15:2	RW	0x00a0	HBLANK Input video Horizontal blanking pixel region width. Number of Horizontal blanking pixels [0...4095].
1	RW	0x0	I_P Input video mode 1b: Interlaced 0b: Progressive
0	RW	0x0	R_V_BLANK_IN_OSC Used for CEA861-D modes with fractional Vblank (for example, modes 5, 6, 7, 10, 11, 20, 21, and 22). For more modes, see the CEA861-D specification. Note: Set this field to 1 for video mode 39, although there is no Vblank oscillation. 1b: Active high

DPTX_VIDEO_CONFIG2_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10314)

Bit	Attr	Reset Value	Description
31:16	RW	0x002d	VBLANK Input video Vertical blanking pixel region width. Number of Vertical blanking lines.
15:0	RW	0x01e0	VACTIVE Input video Vertical active pixel region width. This bit field holds bits 15:0 of number of Vertical active pixels.

DPTX_VIDEO_CONFIG3_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10318)

Bit	Attr	Reset Value	Description
31:16	RW	0x0060	H_SYNC_WIDTH Input video Hsync active pulse width. Integer number of pixel clock cycles [0...511].
15:0	RW	0x0010	H_FRONT_PORCH Input video Hsync active edge delay. Integer number of pixel clock cycles from "de" non active edge of the last "de" valid period [0...4095].

DPTX_VIDEO_CONFIG4_STREAM1

Address: Operational Base(0x27E40000) + offset (0x1031C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0002	V_SYNC_WIDTH Input video Vsync active pulse width. Integer number of video lines [0...63].
15:0	RW	0x000a	V_FRONT_PORCH Input video Vsync active edge delay. Integer number of hsync pulses from "de" non active edge of the last "de" valid period. [0...255]. Specified in terms of number of lines. Value After Reset: 0

DPTX_VIDEO_CONFIG5_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10320)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:21	RW	0x0	INIT_THRESHOLD_HI Most Significant two bits of INT_THRESHOLD.
20	RW	0x0	ENABLE_3D_FRAME_FIELD_SE Set this bit to 1 if the video format being transmitted is 3D video format and Frame/Filed sequential 3D mode is used. Set this bit to 0 (default) if no 3D video is being transmitted, or Frame/Filed sequential 3D format is not being used. Refer to section "3D Stereo Mode Support" for more details.
19:14	RW	0x0c	AVERAGE_BYTES_PER_TU_FR This is the fractional portion of the value calculated in the average bytes per TU. The first decimal value in the fractional part should be programmed here. For example, if the average bytes per TU is 24.34, then this field should be programmed to a value of 3. In SST mode only bits 19:16 is used. In MST mode, this field should be programmed with the fractional value of the VC payload size calculated by the Payload bandwidth manager. as specified in Section 2.6.4.3 of DisplayPort 1.4 Spec. The fractional value calculated times 64 should be programmed in this field. For example if the vc_payload_size calculated is 34.23, a value of 0.23*64 = 15 (14.72 rounded to the nearest integer) should be programmed here. For over 64 MTPs controller transmits AVERAGE_BYTES_PER_TU+1 timeslots with valid symbols for average_bytes_per_tu MTPs for this streams and for 64-average_bytes_per_tu MTPS AVERAGE_BYTES_PER_TU timeslots will have valid symbols. Here is an example for calculating the average_bytes_per_tu_frac in MST mode for the video format VIC-1 (640x480) RGB, 8bpc, at a frame rate of 60Hz. The Link is assumed to be HBR 4 lanes. Peak_stream_bandwidth = Pixel_clock_frequency*bytes_per_pixel = 25.175*3 = 75.52MBps Link Bandwidth = link_rate * 100 * number_of_lanes .= 2.7 * 100 *4 = 1080MBps Average_bytes_per_tu_frac = frac((peak_stream_bandwidth/link_bandwidth)*64))*64 = frac(4.475) *64= 0.47*64 = 30.08 . Program the frac value rounded to the nearest integer which is 30.

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Bit	Attr	Reset Value	Description
13:7	RW	0x0f	INIT_THRESHOLD This is the number of clock cycles the link should wait for the pixels to accumulate at the beginning of every video line before it starts transmitting. This threshold influences the link capability to maintain the avarge valid symbols per TU. For Non-DSC Mode: If the calculated average bytes per tu value is less than 6 then the threshold value should be programmed to 32. For RGB or YCbCr444 modes if the hblank is less than or equal to 80pixels, then a value of 12 should be used. For 4:2:0 mode if the hblank is less than 40, then a value of 3 should be used. For dual and quad pixel modes a value of 64 should be used. In all other cases the default value of 16 is sufficient. The link has a 32 bit data path and the 16 clocks is to wait for TU size clocks which is 16*4 = 64 (TU size) symbols. For DSC Mode: INIT_THRESHOLD = pixel_push_rate * link_pixel_clock_ratio * slot_count where Pixel Push rate = (8/bpp)*lane_count. slot_count for sst =average_bytes_per_tu + FEC symbols inserted per lane(13 in 1-lane and 7 in 2/4lane if fec is enabled, 0 if fec is disabled) slot count is rounded to nearest multiples of 4(ceiling). If slot count calculated is greater than 64, then slot count is fixed to 64. slot_count for mst = (32/lane_count) + average_bytes_per_tu + FEC symbols inserted per lane(13 in 1-lane and 7 in 2/4lane if fec is enabled, 0 if fec is disabled). Slot count is rounded to nearest multiples of 4(ceiling). If slot count calculated is greater than 64, then slot count is fixed to 64. bpp = PPS.bits_per_pixel in simple modes and PPS.bits_per_pixel/2 in native modes link_pixel_clock_ratio = link clock frequency in Mhz/ pixel clock frequency in Mhz.
6:0	RW	0x16	AVERAGE_BYTES_PER_TU This is the average number of valid bytes in a transfer Unit. Driver should program this register based on the video format being transmitted and the link rate and lane configuration being used. Section 2.2.1.4 of the DP 1.43 spec give details on how this average symbol count should be calculated. In MST mode, this register is programmed with the calculated TS_INT as specified in Section 2.6.4.3 of DisplayPort 1.4 Spec. In MST mode, The driver programs the avarege_bytes_per_tu using the following equation. Average_bytes_per_tu= floor((Peak_stream_bandiwth/Link_bandwidth*64) Here is an example for calculating the Average_bytes_per_tu in MST mode for the video format VIC-1 (640x480) RGB, 8bpc, at a frame rate of 60Hz. The Link is assumed to be HBR 4 lanes. Peak_stream_bandwidth = Pixel_clock_frequency*bytes_per_pixel = 25.175*3 = 75.52MBps Link Bandwidth = link_rate * 100 * number_of_lanes .= 2.7 * 100 *4 = 1080MBps Average_bytes_per_tu = floor((peak_stream_bandwidth/link_bandwidth)*64) = floor((75.52/1080)*64)) = floor(4.475) = 4.

DPTX_VIDEO_MSA1_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10324)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0023	VSTART Vertical start from the leading edge of Vsync, measured in line count. This is the vstart value that is specified in the MSA.This is same as vsync width + Vertical back porch.
15:0	RW	0x0090	HSTART Horizontal active start from leading edge of Hsync, measured in pixel count. This is the hstart value that is specified in the MSA. This is same as hsync width + Horizontal back porch.

DPTX_VIDEO_MSA2_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10328)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	MISC0 Bit 24: Synchronous mode of operation. Pixel source reference clock and link reference clock are the same. 1'b0: Asynchronous mode 1'b1: Synchronous mode Bits 31:25: Colorimetry indicator field.
23:0	RW	0x000000	MVID MVID value to be used in case of synchronous mode of operation (pixel source reference clock and link reference clock are the same). See section 2.2.3 of the DisplayPort 1.3 spec. This value goes in the MSA. If the clocks are asynchronous, controller internally calculates this value

DPTX_VIDEO_MSA3_STREAM1

Address: Operational Base(0x27E40000) + offset (0x1032C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	MISC1 24-Interlaced Vertical Total Even 26:25 Stereo Video Attribute 31:30-Pixel Encoding/colorimetry Format indicator field
23:0	RW	0x000000	NVID NVID value to be used in case of synchronous mode of operation (pixel source reference clock and link reference clock are the same). See section 2.2.3 of the DisplayPort 1.3 spec. This value goes in the MSA. If the clocks are asynchronous, controller internally calculates this value.

DPTX_VIDEO_HBLANK_INTERVAL_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10330)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	HBLANK_INTERVAL For MST mode the programmed value should be (Hblank/16 *average_bytes_per_tu*link_clk/pixel_clk. Link_clk and pixel_clk are in Mhz. The link clock is based on the internal 32 bit datapath. In SST mode, it should be hblank *link_clk/pixel_lk.

DPTX_AUD_CONFIG1_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10400)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:24	RW	0x12	AUDIO_TIMESTAMP_VERSION_ Audio timestamp version number.This is used as HB3[7:2] of Audio Timestamp SDP. As per DP 1.3 Spec, this should be h'12 .Some compliance testers still look for old values, and therefore added this register field.
23:16	RW	0x00	AUDIO_PACKET_ID Defines the first byte of the audio SDP and the audio time stamp SDP header. Used for associating the audio sdp to the timestamp with multiple audio streams.
15	RW	0x0	AUDIO_MUTE Controls the AudioMute_Flag in the VB-ID. 1'b1: Sets the AudioMute_Flag in VB-ID 1'b0: Clears the AudioMute_Flag in VB-ID.
14:12	RW	0x1	NUM_CHANNELS Number of audio channels 1'b0: 1channel 1'b1: 2channels others: 8channels.
11	RO	0x0	reserved
10	RW	0x0	HBR_MODE_ENABLE Audio input is operating in HBR mode if set to '1'. When audio_if_select is 1 (S/PDIF), 768kHz x 2 Channels x 16 bits is delivered to controller. When '0' (I2s) 192kHz x 8 x 16 bits in 8-channel is delivered to controller.
9:5	RW	0x10	AUDIO_DATA_WIDTH Audio input data width audio_data_width4:0 Action 5'b00000-5'b01111: Not used 5'b10000: 16 bit data samples at input 5'b10001: 17 bit data samples at input 5'b10010: 18 bit data samples at input 5'b10011: 19: bit data samples at input 5'b10100: 20: bit data samples at input 5'b10101: 21: bit data samples at input 5'b10110: 22: bit data samples at input 5'b10111: 23: bit data samples at input 5'b11000: 24: bit data samples at input 5'b11001-5'b11111: Not Used
4:1	RW	0x1	AUDIO_DATA_IN_EN Specifies which of the audio data inputs are active. Used to control I2sSPDIF input data. audio_data_in_en0 and ispdfidata0i2sdata_i0 enabled indicates channels12 is active audio_data_in_en1, ispdfidata1, and i2sdata_i1 enabled indicates channels3 and channels4 are active. audio_data_in_en2, ispdfidata2, and i2sdata_i2 enabled indicates channels5 and channels6 are active. audio_data_in_en3, ispdfidata3, and i2sdata_i3 enabled indicates that channels7 and channels8 are active. Value of 0 is invalid.
0	RW	0x0	AUDIO_INF_SELECT 1'b0: I2S is the selected audio input interface (Default). 1'b1: SPDIF is the selected audio input interface.

DPTX_SDP_VERTICAL_CTRL_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10500)

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Bit	Attr	Reset Value	Description
31	RW	0x0	FIXED_PRIORITY_ARBITRATIO When this bit is set then the scheduler searches for the next SDP to transmit based on fixed priority, otherwise it uses Round-Robin arbitration. Fixed priority means that lower numbered register sets has higher priority than higher numbered register sets.
30	RW	0x0	DISABLE_EXT_SDP When set the external SDP interface is disabled. No external SDPs are transmitted. This bit is applicable for both the vertical and horizontal blanking.
29:25	RO	0x00	reserved
24	RW	0x0	EN_128BYTES_SDP_1 When set, register bank 1, 2, 3 and 4 are used to form a 128bytes SDP. The SW should program a single 4bytes header followed by 128bytes of data and set a single enable bit that corresponds to bank 1.
23:20	RO	0x0	reserved
19:2	RW	0x00000	EN_VERTICAL_SDP_N When set, DWC_dptx sends out SDP during the vertical intervals, using the information provided in the SDP_REGISTER BANK[n*9-1:n*9]
1	RW	0x0	EN_AUDIO_STREAM_SDP When cleared, no Audio stream is sent during the vertical blanking period. When '1' audio stream is transmitted during vertical blanking period.
0	RW	0x0	EN_AUDIO_TIMESTAMP_SDP When set, DWC_dptx sends out audio timestamp SDP once every video frame during the vertical blanking period. This SDP is always transmitted as the first SDP in the blanking period. Payload for the audio timestamp SDP and the header are internally generated by the controller.

DPTX_SDP_HORIZONTAL_CTRL_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10504)

Bit	Attr	Reset Value	Description
31	RW	0x0	FIXED_PRIORITY_ARBITRATION When this bit is set then the scheduler searches for the next SDP to transmit based on fixed priority, otherwise it uses Round-Robin arbitration. Fixed priority means that lower numbered register sets has higher priority than higher numbered register sets.
30:20	RO	0x000	reserved
19:2	RW	0x00000	EN_HORIZONTAL_SDP_N When set, DWC_dptx sends out SDP during the horizontal intervals, using the information provided in the SDP_REGISTER BANK[n*9-1:n*9]
1	RW	0x0	EN_AUDIO_STREAM_SDP When cleared, no Audio stream is sent during horizontal blanking. When '1' audio stream is transmitted during horizontal blanking period.
0	RW	0x0	EN_AUDIO_TIMESTAMP_SDP When set, DWC_dptx sends out audio timestamp SDP once every horizontal blanking. Payload for the audio timestamp SDP and the header are internally generated by the controller.

DPTX_SDP_STATUS_REGISTER_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10508)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:2	W1C	0x00000	SDP_N_TX_STATUS Status indicating the transmission of corresponding Nth SDP. Set to 1 by the hardware in both Auto and Manual modes. Software writes a 1 to clear this bit.
1	W1C	0x0	AUDIO_STREAM_SDP_STATUS Status indicating the transmission of a audio SDP. Set to 1 by the hardware in both Auto and Manual modes. Software writes a 1 to clear this bit.
0	W1C	0x0	AUDIO_TIMESTAMP_SDP_STAT Status indicating the transmission of an audio timestamp SDP. Set to 1 by the hardware in both Auto and Manual modes. Software writes a 1 to clear this bit.

DPTX_SDP_MANUAL_CTRL_STREAM1

Address: Operational Base(0x27E40000) + offset (0x1050C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	MANUAL_MODE_SDP Setting this bit when the corresponding bit in the SDP_VERTICAL_CTRL/SDP_HORIZONTAL_CTRL registers causes the corresponding SDP to be transmitted once. After the transmission, both corresponding enable bits are reset. If the transmission done during the Vertical or the Horizontal blanking period then the enable bit in both the SDP_VERTICAL_CTRL and SDP_HORIZONTAL_CTRL registers are reset.This provides the Software the ability to decide whether a SDP is transmitted once during the Vertical period, or Horizontal period or which ever comes first.

DPTX_SDP_STATUS_EN_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10510)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:2	RW	0x00000	SDP_STATUS_EN Setting this bit to 1 enables interrupt generation due to transmission of the corresponding SDP
1	RW	0x0	AUDIO_STREAM_SDP_STATUS Setting this bit to 1 enables interrupt generation due to transmission of an audio SPD
0	RW	0x0	AUDIO_TIMESTAMP_SDP_STAT Setting this bit to 1 enables interrupt generation due to transmission of a audio timestamp SPD

DPTX_SDP_REGISTER_BANK_STREAM1

Address: Operational Base(0x27E40000) + offset (0x10600)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SDP_REGS The register bank is split to SDPs where each SDP is the size of nine 32bits registers. The first register contains the SDP header and the other eight the data payload. For example, if DWC_DPTX_NUM_SDP_REGISTER_BANKS is 10, then 90 32bits registers are defined. The register set [8:0] specifies s SDP which is transmitted if the corresponding bit in SDP_AUTOEN_CTRL is set, whether the corresponding bit located at [2]. The next SDP, registers [17:9] are enabled by bit [3] in SDP_AUTOEN_CTRL.

DPTX_VSAMPLE_CTRL_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20300)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	STREAM_TYPE This is a per stream control defining the stream type. RepeaterAuth_Stream_Manage of HDCP2.2 specification. This field is valid only when HDCP MST are enabled.
24	RW	0x0	ENCRYPTION_ENABLE This is a per stream control to enable encryption. Setting ofthis bit has significance only when operating in MST mode or eDP. In non eDP SST operation, this bit has no significance. In MST mode or when eDP is enabled, this bit control the encryption to be used. In MST mode, this bit control HDCP encryption for a specific stream. HDCPCFG register controls the global enable of HDCP. In eDP mode this bit controls the enabling of ASSR feature as specified in section 3.5 of eDP1.4b spec and Section 2.10 of DP1.4 spec. When eDP is enabled, HDCP should be disabled and HDCPCFG[1] should not be set.
23	RW	0x0	ENABLE_DSC Set this bit to 1 to enable Display Stream Compression (DSC) on this specific stream. The software driver can set this bit only if DSC is enabled during configuration (DWC_DPTX_DSC_EN = 1 or 2). Otherwise writing 1 1 to this bit does not take effect.
22:21	RW	0x0	PIXEL_MODE_SELECT This field is used to select the single/dual/quad pixel mode of operation. 2'b00: Single pixel mode (default) 2'b01: Dual pixel mode 2'b10: Quad pixel mode. 2'b11: Reserved.

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Bit	Attr	Reset Value	Description
20:16	RW	0x00	VIDEO_MAPPING Video input mapping color space/depth Video Input mapping (color space/color depth) with DSC disabled/enabled(VSAMPLE_CTRL.ENABLE_DSC=0/1): 0: RGB 6bits (Reserved) 1: RGB 8bits (RGB 8bits) 2: RGB 10bits (RGB 10bits) 3: RGB 12bits (RGB 12bits) 4: RGB 16bits (Reserved) 5: YCbCR4:4:4 8bits (YCbCr4:4:4 8bits) 6: YCbCr4:4:4 10bits (YCbCr4:4:4 10bits) 7: YCbCr4:4:4 12bits (YCbCr4:4:4 12bits) 8: YCbCr4:4:4 16bits (Reserved) 9: YCbCR4:2:2 8bits (Simple YCbCr4:2:2 8bits) 10: YCbCr4:2:2 10bits (Simple YCbCr4:2:2 10bits) 11: YCbCr4:2:2 12bits (Simple YCbCr4:2:2 12bits) 12: YCbCr4:2:2 16bits (Reserved) 13: YCbCR4:2:0 8bits (YCbCR4:2:0 8bits) 14: YCbCr4:2:0 10bits (YCbCR4:2:0 10bits) 15: YCbCr4:2:0 12bits (YCbCR4:2:0 12bits) 16: YCbCr4:2:0 16bits (Reserved) 17: YOnly 8bits (native YCbCr4:2:2 8bits) 18: YOnly 10bits (native YCbCr4:2:2 10bits) 19: YOnly 12bits (native YCbCr4:2:2 12bits) 20: YOnly 16bits (Reserved) 23: RAW 8bits. (Reserved) 24: RAW 10bits (Reserved) 25: RAW 12bits (Reserved) 27: RAW 16bits (Reserved) Others: Reserved.
15:6	RO	0x000	reserved
5	RW	0x0	VIDEO_STREAM_ENABLE 1'b0: Video stream Disable 1'b1: Video stream Enable When set to 0, no video stream is transmitted. Video inputs are ignored and NoVideoStream_flag in the VB-ID is set.
4	RW	0x0	INTERNAL_DE_GENERATOR 1'b1: Enable internal data generator 1'b0: Data enable signal available at the input. When the external logic which drives the pixel data does not generate the video data enable, then enabling this bit forces the controller to generate the video enable internally. Note: This feature is currently not supported and therefore should not be used.
3:0	RO	0x0	reserved

DPTX_VSAMPLE_STUFF_CTRL1_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20304)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	BCB_STUFF_DATA Data to be stuffed on B/Cb data path.
15:3	RO	0x0000	reserved
2	RW	0x0	GY_DATA_STUFFING_EN Enable stuffing on internal G/Y data lines.
1	RW	0x0	RCR_DATA_STUFFING_EN Enable stuffing on internal R/Cr data lines.

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Bit	Attr	Reset Value	Description
0	RW	0x0	BCB_DATA_STUFFING_EN Enable stuffing on internal B/Cb data lines

DPTX_VSAMPLE_STUFF_CTRL2_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20308)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	GY_STUFF_DATA Data to be stuffed on G/Y data path.
15:0	RW	0x0000	RCR_STUFF_DATA Data to be stuffed on R/Cr data path.

DPTX_VINPUT_POLARITY_CTRL_STREAM2

Address: Operational Base(0x27E40000) + offset (0x2030C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	DE_IN_POLARITY de input polarity 1'b1: Active low 1'b0: Active high
1	RW	0x0	HSYNC_IN_POLARITY Hsync input polarity 1'b1: Active high 1'b0: Active low
0	RW	0x0	VSYNC_IN_POLARITY Vsync input polarity 1'b1: Active high 1'b0: Active low

DPTX_VIDEO_CONFIG1_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20310)

Bit	Attr	Reset Value	Description
31:16	RW	0x0280	HACTIVE Input video Horizontal active pixel region width. Number of Horizontal active pixels [0...8191].
15:2	RW	0x00a0	HBLANK Input video Horizontal blanking pixel region width. Number of Horizontal blanking pixels [0...4095].
1	RW	0x0	I_P Input video mode 1b: Interlaced 0b: Progressive
0	RW	0x0	R_V_BLANK_IN_OSC Used for CEA861-D modes with fractional Vblank (for example, modes 5, 6, 7, 10, 11, 20, 21, and 22). For more modes, see the CEA861-D specification. Note: Set this field to 1 for video mode 39, although there is no Vblank oscillation. 1b: Active high

DPTX_VIDEO_CONFIG2_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20314)

Bit	Attr	Reset Value	Description
31:16	RW	0x002d	VBLANK Input video Vertical blanking pixel region width. Number of Vertical blanking lines.

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Bit	Attr	Reset Value	Description
15:0	RW	0x01e0	VACTIVE Input video Vertical active pixel region width. This bit field holds bits 15:0 of number of Vertical active pixels.

DPTX_VIDEO_CONFIG3_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20318)

Bit	Attr	Reset Value	Description
31:16	RW	0x0060	H_SYNC_WIDTH Input video Hsync active pulse width. Integer number of pixel clock cycles [0...511].
15:0	RW	0x0010	H_FRONT_PORCH Input video Hsync active edge delay. Integer number of pixel clock cycles from "de" non active edge of the last "de" valid period [0...4095].

DPTX_VIDEO_CONFIG4_STREAM2

Address: Operational Base(0x27E40000) + offset (0x2031C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0002	V_SYNC_WIDTH Input video Vsync active pulse width. Integer number of video lines [0...63].
15:0	RW	0x000a	V_FRONT_PORCH Input video Vsync active edge delay. Integer number of hsync pulses from "de" non active edge of the last "de" valid period. [0...255]. Specified in terms of number of lines. Value After Reset: 0

DPTX_VIDEO_CONFIG5_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20320)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:21	RW	0x0	INIT_THRESHOLD_HI Most Significant two bits of INT_THRESHOLD.
20	RW	0x0	ENABLE_3D_FRAME_FIELD_SE Set this bit to 1 if the video format being transmitted is 3D video format and Frame/Filed sequential 3D mode is used. Set this bit to 0 (default) if no 3D video is being transmitted, or Frame/Filed sequential 3D format is not being used. Refer to section "3D Stereo Mode Support" for more details.

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Bit	Attr	Reset Value	Description
19:14	RW	0x0c	AVERAGE_BYTES_PER_TU_FR This is the fractional portion of the value calculated in the average bytes per TU. The first decimal value in the fractional part should be programmed here. For example, if the average bytes per TU is 24.34, then this field should be programmed to a value of 3. In SST mode only bits 19:16 is used. In MST mode, this field should be programmed with the fractional value of the VC payload size calculated by the Payload bandwidth manager. as specified in Section 2.6.4.3 of DisplayPort 1.4 Spec. The fractional value calculated times 64 should be programmed in this field. For example if the vc_payload_size calculated is 34.23, a value of 0.23*64 = 15 (14.72 rounded to the nearest integer) should be programmed here. For over 64 MTPs controller transmits AVERAGE_BYTES_PER_TU+1 timeslots with valid symbols for average_bytes_per_tu MTPs for this streams and for 64-average_bytes_per_tu MTPS AVERAGE_BYTES_PER_TU timeslots will have valid symbols. Here is an example for calculating the average_bytes_per_tu_frac in MST mode for the video format VIC-1 (640x480) RGB, 8bpc, at a frame rate of 60Hz. The Link is assumed to be HBR 4 lanes. Peak_stream_bandwidth = Pixel_clock_frequency*bytes_per_pixel = 25.175*3 = 75.52MBps Link Bandwidth = link_rate * 100 * number_of_lanes .= 2.7 * 100 *4 = 1080MBps Average_bytes_per_tu_frac = frac((peak_stream_bandwidth/link_bandwidth)*64))*64 = frac(4.475) *64= 0.47*64 = 30.08 . Program the frac value rounded to the nearest integer which is 30.

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Bit	Attr	Reset Value	Description
13:7	RW	0x0f	INIT_THRESHOLD This is the number of clock cycles the link should wait for the pixels to accumulate at the beginning of every video line before it starts transmitting. This threshold influences the link capability to maintain the avarge valid symbols per TU. For Non-DSC Mode: If the calculated average bytes per tu value is less than 6 then the threshold value should be programmed to 32. For RGB or YCbCr444 modes if the hblank is less than or equal to 80pixels, then a value of 12 should be used. For 4:2:0 mode if the hblank is less than 40, then a value of 3 should be used. For dual and quad pixel modes a value of 64 should be used. In all other cases the default value of 16 is sufficient. The link has a 32 bit data path and the 16 clocks is to wait for TU size clocks which is 16*4 = 64 (TU size) symbols. For DSC Mode: INIT_THRESHOLD = pixel_push_rate * link_pixel_clock_ratio * slot_count where Pixel Push rate = (8/bpp)*lane_count. slot_count for sst =average_bytes_per_tu + FEC symbols inserted per lane(13 in 1-lane and 7 in 2/4lane if fec is enabled, 0 if fec is disabled) slot count is rounded to nearest multiples of 4(ceiling). If slot count calculated is greater than 64, then slot count is fixed to 64. slot_count for mst = (32/lane_count) + average_bytes_per_tu + FEC symbols inserted per lane(13 in 1-lane and 7 in 2/4lane if fec is enabled, 0 if fec is disabled). Slot count is rounded to nearest multiples of 4(ceiling). If slot count calculated is greater than 64, then slot count is fixed to 64. bpp = PPS.bits_per_pixel in simple modes and PPS.bits_per_pixel/2 in native modes link_pixel_clock_ratio = link clock frequency in Mhz/ pixel clock frequency in Mhz.
6:0	RW	0x16	AVERAGE_BYTES_PER_TU This is the average number of valid bytes in a transfer Unit. Driver should program this register based on the video format being transmitted and the link rate and lane configuration being used. Section 2.2.1.4 of the DP 1.43 spec give details on how this average symbol count should be calculated. In MST mode, this register is programmed with the calculated TS_INT as specified in Section 2.6.4.3 of DisplayPort 1.4 Spec. In MST mode, The driver programs the avarege_bytes_per_tu using the following equation. Average_bytes_per_tu= floor((Peak_stream_bandiwth/Link_bandwidth*64) Here is an example for calculating the Average_bytes_per_tu in MST mode for the video format VIC-1 (640x480) RGB, 8bpc, at a frame rate of 60Hz. The Link is assumed to be HBR 4 lanes. Peak_stream_bandwidth = Pixel_clock_frequency*bytes_per_pixel = 25.175*3 = 75.52MBps Link Bandwidth = link_rate * 100 * number_of_lanes .= 2.7 * 100 *4 = 1080MBps Average_bytes_per_tu = floor((peak_stream_bandwidth/link_bandwidth)*64) = floor((75.52/1080)*64)) = floor(4.475) = 4.

DPTX_VIDEO_MSA1_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20324)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0023	VSTART Vertical start from the leading edge of Vsync, measured in line count. This is the vstart value that is specified in the MSA.This is same as vsync width + Vertical back porch.
15:0	RW	0x0090	HSTART Horizontal active start from leading edge of Hsync, measured in pixel count. This is the hstart value that is specified in the MSA. This is same as hsync width + Horizontal back porch.

DPTX_VIDEO_MSA2_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20328)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	MISC0 Bit 24: Synchronous mode of operation. Pixel source reference clock and link reference clock are the same. 1'b0: Asynchronous mode 1'b1: Synchronous mode Bits 31:25: Colorimetry indicator field.
23:0	RW	0x000000	MVID MVID value to be used in case of synchronous mode of operation (pixel source reference clock and link reference clock are the same). See section 2.2.3 of the DisplayPort 1.3 spec. This value goes in the MSA. If the clocks are asynchronous, controller internally calculates this value

DPTX_VIDEO_MSA3_STREAM2

Address: Operational Base(0x27E40000) + offset (0x2032C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	MISC1 24-Interlaced Vertical Total Even 26:25 Stereo Video Attribute 31:30-Pixel Encoding/colorimetry Format indicator field
23:0	RW	0x000000	NVID NVID value to be used in case of synchronous mode of operation (pixel source reference clock and link reference clock are the same). See section 2.2.3 of the DisplayPort 1.3 spec. This value goes in the MSA. If the clocks are asynchronous, controller internally calculates this value.

DPTX_VIDEO_HBLANK_INTERVAL_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20330)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	HBLANK_INTERVAL For MST mode the programmed value should be (Hblank/16 *average_bytes_per_tu*link_clk/pixel_clk. Link_clk and pixel_clk are in Mhz. The link clock is based on the internal 32 bit datapath. In SST mode, it should be hblank *link_clk/pixel_lk.

DPTX_AUD_CONFIG1_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20400)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:24	RW	0x12	AUDIO_TIMESTAMP_VERSION_ Audio timestamp version number.This is used as HB3[7:2] of Audio Timestamp SDP. As per DP 1.3 Spec, this should be h'12 .Some compliance testers still look for old values, and therefore added this register field.
23:16	RW	0x00	AUDIO_PACKET_ID Defines the first byte of the audio SDP and the audio time stamp SDP header. Used for associating the audio sdp to the timestamp with multiple audio streams.
15	RW	0x0	AUDIO_MUTE Controls the AudioMute_Flag in the VB-ID. 1'b1: Sets the AudioMute_Flag in VB-ID 1'b0: Clears the AudioMute_Flag in VB-ID.
14:12	RW	0x1	NUM_CHANNELS Number of audio channels 1'b0: 1channel 1'b1: 2channels others: 8channels.
11	RO	0x0	reserved
10	RW	0x0	HBR_MODE_ENABLE Audio input is operating in HBR mode if set to '1'. When audio_if_select is 1 (S/PDIF), 768kHz x 2 Channels x 16 bits is delivered to controller. When '0' (I2s) 192kHz x 8 x 16 bits in 8-channel is delivered to controller.
9:5	RW	0x10	AUDIO_DATA_WIDTH Audio input data width audio_data_width4:0 Action 5'b00000-5'b01111: Not used 5'b10000: 16 bit data samples at input 5'b10001: 17 bit data samples at input 5'b10010: 18 bit data samples at input 5'b10011: 19: bit data samples at input 5'b10100: 20: bit data samples at input 5'b10101: 21: bit data samples at input 5'b10110: 22: bit data samples at input 5'b10111: 23: bit data samples at input 5'b11000: 24: bit data samples at input 5'b11001-5'b11111: Not Used
4:1	RW	0x1	AUDIO_DATA_IN_EN Specifies which of the audio data inputs are active. Used to control I2sSPDIF input data. audio_data_in_en0 and ispdfidata0i2sdata_i0 enabled indicates channels12 is active audio_data_in_en1, ispdfidata1, and i2sdata_i1 enabled indicates channels3 and channels4 are active. audio_data_in_en2, ispdfidata2, and i2sdata_i2 enabled indicates channels5 and channels6 are active. audio_data_in_en3, ispdfidata3, and i2sdata_i3 enabled indicates that channels7 and channels8 are active. Value of 0 is invalid.
0	RW	0x0	AUDIO_INF_SELECT 1'b0: I2S is the selected audio input interface (Default). 1'b1: SPDIF is the selected audio input interface.

DPTX_SDP_VERTICAL_CTRL_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20500)

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Bit	Attr	Reset Value	Description
31	RW	0x0	FIXED_PRIORITY_ARBITRATIO When this bit is set then the scheduler searches for the next SDP to transmit based on fixed priority, otherwise it uses Round-Robin arbitration. Fixed priority means that lower numbered register sets has higher priority than higher numbered register sets.
30	RW	0x0	DISABLE_EXT_SDP When set the external SDP interface is disabled. No external SDPs are transmitted. This bit is applicable for both the vertical and horizontal blanking.
29:25	RO	0x00	reserved
24	RW	0x0	EN_128BYTES_SDP_1 When set, register bank 1, 2, 3 and 4 are used to form a 128bytes SDP. The SW should program a single 4bytes header followed by 128bytes of data and set a single enable bit that corresponds to bank 1.
23:20	RO	0x0	reserved
19:2	RW	0x00000	EN_VERTICAL_SDP_N When set, DWC_dptx sends out SDP during the vertical intervals, using the information provided in the SDP_REGISTER BANK[n*9-1:n*9]
1	RW	0x0	EN_AUDIO_STREAM_SDP When cleared, no Audio stream is sent during the vertical blanking period. When '1' audio stream is transmitted during vertical blanking period.
0	RW	0x0	EN_AUDIO_TIMESTAMP_SDP When set, DWC_dptx sends out audio timestamp SDP once every video frame during the vertical blanking period. This SDP is always transmitted as the first SDP in the blanking period. Payload for the audio timestamp SDP and the header are internally generated by the controller.

DPTX_SDP_HORIZONTAL_CTRL_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20504)

Bit	Attr	Reset Value	Description
31	RW	0x0	FIXED_PRIORITY_ARBITRATION When this bit is set then the scheduler searches for the next SDP to transmit based on fixed priority, otherwise it uses Round-Robin arbitration. Fixed priority means that lower numbered register sets has higher priority than higher numbered register sets.
30:20	RO	0x000	reserved
19:2	RW	0x00000	EN_HORIZONTAL_SDP_N When set, DWC_dptx sends out SDP during the horizontal intervals, using the information provided in the SDP_REGISTER BANK[n*9-1:n*9]
1	RW	0x0	EN_AUDIO_STREAM_SDP When cleared, no Audio stream is sent during horizontal blanking. When '1' audio stream is transmitted during horizontal blanking period.
0	RW	0x0	EN_AUDIO_TIMESTAMP_SDP When set, DWC_dptx sends out audio timestamp SDP once every horizontal blanking. Payload for the audio timestamp SDP and the header are internally generated by the controller.

DPTX_SDP_STATUS_REGISTER_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20508)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:2	W1C	0x00000	SDP_N_TX_STATUS Status indicating the transmission of corresponding Nth SDP. Set to 1 by the hardware in both Auto and Manual modes. Software writes a 1 to clear this bit.
1	W1C	0x0	AUDIO_STREAM_SDP_STATUS Status indicating the transmission of a audio SDP. Set to 1 by the hardware in both Auto and Manual modes. Software writes a 1 to clear this bit.
0	W1C	0x0	AUDIO_TIMESTAMP_SDP_STAT Status indicating the transmission of an audio timestamp SDP. Set to 1 by the hardware in both Auto and Manual modes. Software writes a 1 to clear this bit.

DPTX_SDP_MANUAL_CTRL_STREAM2

Address: Operational Base(0x27E40000) + offset (0x2050C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	MANUAL_MODE_SDP Setting this bit when the corresponding bit in the SDP_VERTICAL_CTRL/SDP_HORIZONTAL_CTRL registers causes the corresponding SDP to be transmitted once. After the transmission, both corresponding enable bits are reset. If the transmission done during the Vertical or the Horizontal blanking period then the enable bit in both the SDP_VERTICAL_CTRL and SDP_HORIZONTAL_CTRL registers are reset.This provides the Software the ability to decide whether a SDP is transmitted once during the Vertical period, or Horizontal period or which ever comes first.

DPTX_SDP_STATUS_EN_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20510)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:2	RW	0x00000	SDP_STATUS_EN Setting this bit to 1 enables interrupt generation due to transmission of the corresponding SDP
1	RW	0x0	AUDIO_STREAM_SDP_STATUS Setting this bit to 1 enables interrupt generation due to transmission of an audio SPD
0	RW	0x0	AUDIO_TIMESTAMP_SDP_STAT Setting this bit to 1 enables interrupt generation due to transmission of a audio timestamp SPD

DPTX_SDP_REGISTER_BANK_STREAM2

Address: Operational Base(0x27E40000) + offset (0x20600)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SDP_REGS The register bank is split to SDPs where each SDP is the size of nine 32bits registers. The first register contains the SDP header and the other eight the data payload. For example, if DWC_DPTX_NUM_SDP_REGISTER_BANKS is 10, then 90 32bits registers are defined. The register set [8:0] specifies s SDP which is transmitted if the corresponding bit in SDP_AUTOEN_CTRL is set, whether the corresponding bit located at [2]. The next SDP, registers [17:9] are enabled by bit [3] in SDP_AUTOEN_CTRL.

22.5 Interface Description

Table 22-1 EDP TX Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
dptx_ln0_txdp	O	USB3_OTG0_SSRX1P/DP_TX_D0P	NS
dptx_ln0_txdn	O	USB3_OTG0_SSRX1N/DP_TX_D0N	NS
dptx_ln1_txdp	O	USB3_OTG0_SSTX1P/DP_TX_D1P	NS
dptx_ln1_txdn	O	USB3_OTG0_SSTX1N/DP_TX_D1N	NS
dptx_ln2_txdp	O	USB3_OTG0_SSRX2P/DP_TX_D2P	NS
dptx_ln2_txdn	O	USB3_OTG0_SSRX2N/DP_TX_D2N	NS
dptx_ln3_txdp	O	USB3_OTG0_SSTX2P/DP_TX_D3P	NS
dptx_ln3_txdn	O	USB3_OTG0_SSTX2N/DP_TX_D3N	NS
dptx_auxp	I/O	DP_TX_AUXP	NS
dptx_auxn	I/O	DP_TX_AUXN	NS
dptx_hpd_m0	I	ISP_PRELIGHT_TRIG_M1/SAI4_LRCK_M2/DP_HPDIN_M0/I2C3_SCL_M3/SPI4_CSN0_M0/UART6_TX_M3/PWM2_CH6_M1/GPIO4_C4_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_H[3:0]=4'hA
dptx_hpd_m1	I	SAI0_SDO0_M1/DP_HPDIN_M1/UART10_RX_M2/I3C0_SDA_PU_M0/GPIO0_C5_d	PMU1_IOC_GPIO0C_IOMUX_SEL_H[7:4]=4'h9

Notes: I=input, O=output, I/O=input/output, bidirectional, NS=Not Set

22.6 Application Notes

22.6.1 Programming Flow After POR

The driver performs the following steps after power-on reset:

22.6.1.1 Assert PHY Reset

1. Set the PHY soft reset by setting the PMU1CRU_RESET_CON00[12] register.
2. Refer the PHY document to know if anything else need to be reset at this time.
3. Wait for 5us to make sure that the soft reset takes effect and then clear the PHY soft reset bit by writing a 0 to this bit.
4. Wait for the PHYIF_CTRL.PHY_BUSY register to be 0.
5. Ensure that GENERAL_INTERRUPT_ENABLE.HPD_EVENT are cleared.

22.6.1.2 Wait for HPD (Hot Plug Detect) interrupt

Interrupt is asserted and when driver reads the GENERAL_INTERRUPT register, finds HPD_EVENT bit set. This interrupt is generated when the Sink is disconnected and with an

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HPD transition from 0 to 1 and has stayed at 1 for greater than 0.25ms. This section indicates how the software should handle the interrupt.
1. Software receives an interrupt and reads the GENERAL_INTERRUPT register. GENERAL_INTERRUPTS.HPD_EVENT is set. It should also see that HPD_STATUS.HPD_STATUS
is 1.
2. The software should set PHYIF_CTRL.PHY_LANEX_POWERDOWN to 0 to power on the PHY for all enabled lanes.
3. Software clears the interrupt by writing 1 to GENERAL_INTERRUPTS.HPD_EVENT

22.6.1.3 Read Hardware Parameter

Read the DPTX_CONFIG_REG1, DPTX_CONFIG_REG2, DPTX_CONFIG_REG3 register to get the DPTX configuration parameters.

22.6.1.4 Read EDID of the Sink

EDID reads are done using I2C over AUX transactions. See I2C AUX Channel Read/Write for details about initiating I2C over AUX read.

22.6.1.5 Read Sink DPCD registers

Read the sink DPCD register to get at least the following sink information. DPCD registers are read using Native AUX transactions. See NATIVE AUX Channel Read/Write for details about using the Aux channel to read the DPCD.

- Read Sink Rceiver Capability (DPCD address 000000 – 000FF)

This gives the sink supported link rate, lane count, enhance_frame_cap, extended_receiver_capability_present, and so on.

- Read Sink Extended Reciver Capability (DPCD address 02200 – 022FF)

Extended Receiver capability is read only if the sink supports it. Link rate, lane count, enhance_frame_cap.

22.6.1.6 Program Sink DPCD Link Configuration registers

Link configuration registers are programmed based on the Sink setting read during Step-5, and the Video format being transmitted. It also depends on the source configs (Step-3).

22.6.1.7 Initiate link training

- Disable the fast link training if enabled. Fast link training is enabled by default.
- Follow the steps specified in "Full Link Bringup Sequence,"for initiating link training.

22.6.1.8 Configure Video mode

After reading and having parsed the EDID data (step 4), program the controller with the video
timings based on the video mode the sink supports and the trained link is able to support. In the single stream (SST) mode, use only stream-0, and program only the corresponding registers. If there is no video stream to transmit, then this setup is not required. Set VSAMPLE_CTRL.video_stream_enable bit to 0 forces the controller to send IDLE patterns. Follow these steps for every active stream:

1. Program the VSAMPLE_CTRL.video_mapping bit to set the video_mapping input mode (RGB/YCbCr), based on what is supported by the sink.
2. Program the video timing information. In MST mode, follow these steps for every active stream.
   a. Set the Hsync/vsync polarity by programming VINPUT_POLARITY_CTRL register.
   b. Program the VIDEO_CONFIG1 register by specifying the following
      - R_v_blank_in_osc – Fractional vblank.
      - I_P – Interlaced/Progressive
      - Hblank – Horizontal blanking period in pixels.
      - Hactive – Horizontal active video period in pixels.
   c. Program the VIDEO_CONFIG2 register by specifying the following
      - Vactive – Vertical active video period in terms of pixels.
      - Vblank – Vertical blanking period in terms of vertical blanking lines.
   d. Program the VIDEO_CONFIG3 register by specifying the following
      - H_front_porch – The horizontal front porch in terms of pixels.
      - H_sync_width – hsync active pulse width in terms of pixels.

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e. Program the VIDEO_CONFIG4 register by specifying the following
   - V_front_porch – The vertical front porch in terms of number of lines.
   - V_sync_width – vsync active pulse width in terms of number of lines.

f. In SST mode, program the VIDEO_CONFIG5 register by specifying the following
   Specify the Average number of symbols per TU, and average bytes per TU fractional values. Driver should program this register field based on the video format being transmitted and the link rate and lane configuration being used. Section 2.2.1.4 of the DP 1.4 spec gives details about how this average symbol count should be calculated.

3. Program the core for Main Stream Attribute parameters
   a. Program the Stream_N.VIDEO_MSA1 register with the following values
      - Hstart – Horizontal active start from the leading edge of hsync.
      - Vstart – Vertical active start from the leading edge of vsync.
   b. Program the Stream_N.VIDEO_MSA2 register with the following values
      - Mvid – MVID value to be transmitted in the synchronous mode of operation.
      - MISC0 – Specifies synchronous/asynchronous mode of operation and other colormetry values to be transmitted in the MSA.
   c. Program the Stream_N.VIDEO_MSA3 register with the following values
      - Nvid – MVID value to be transmitted in the synchronous mode of operation.
      - MISC1 – Specifies synchronous/asynchronous mode of operation and other colormetry values to be transmitted in the MSA.
4. Program MSA mode
   a. Calculate the VC_payload_size_N of the video format that it is driving as specified in section.2.6.4.3 of DP1.4 spec using the formula, VC_payload_size=(Peak_stream_bandiwth_N/Link_bandwidth*64).Where Link_bandwidth is the bandwidth of the link DPTX is driving. Peak_stream_bandiwdth_N is the bandwidth of stream_N.
   b. Program the VC Payload allocation table MST_VCP_TABLE_N with the virtual channel payload size for the video stream. VC payload size slots should be programmed with the stream ID corresponding to the stream.The controller switches to the allocation based on the updated table only after the completion of the ACT sequence (after the software driver sets CCTL.INITIATE_ACT_SEQUENCE).
   c. Program the Stream_N.VIDEO_CONFIG5 register specific to this stream by writing the AVERAGE_BYTES_PER_TU with the integer value of the VC_payload_size.
   Average_bytes_per_tu= floor((Peak_stream_bandiwth/Link_bandwidth*64)
   d. Program the Stream_N.VIDEO_CONFIG5 register specific to this stream by writing the AVERAGE_BYTES_PET_TU_FRAC with the fractional value of VC_payload_size *100.
   Average_bytes_per_tu_frac = frac (Peak_stream_bandiwth/Link_bandwidth*64) *100.
   For every 100 MTPs, controller transmits average_bytes_per_tu symbols +1 for average_bytes_per_tu_frac MTPs and average_bytes_per_tu symbols for 100-average_bytes_per_tu_frac MTPs.
   e. If the sink supports enhance_frame_cap, set CCTL.Enhance_framing_en.
   Follow these steps only in the MST mode
   f. Using Native Aux transaction, update the VC payload ID table of the branch device. Use the DPCD registers 1C0'h to 2C0'h. See table 2-138 of DP1.4 Specification for more details.
   g. Using Native Aux, read the PAYLOAD_TABLE_UPDATE_STATUS DPCD register (2C0'h) bit VC payload ID table updated in the branch device, to check for the payload ID table to be updated. Wait for this bit to be set.
   h. Set CCTL.INITIATE_ACT_SEQUENCE to trigger the ACT sequence (VC payload allocation over main link) between the DPTX and the DPRX of the immediate branch device connected to the DPTX.
   i. Using Native Aux, read the PAYLOAD_TABLE_UPDATE_STATUS DPCD register (2C0'h) bit ACT_handled, to check the successful handling of the ACT trigger sequence. Wait for this bit to be set. This is to make sure that the ACT trigger sequence has been successfully handled by the branch DPRX.

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j. If content protection is not required, then enable video stream by setting the VSAMPLE_CTRL.video_stream_enable bit. At this time, the video sampler is enabled, and the data is sampled into the fifos. The pixel interface could have the video input active at this time. The controller transmits Blanking End (BE) only after video is enabled (either through fast link training which is enabled by default or by the setting of VSAMPLE_CTRL.video_stream_enable).In MST mode, after setting the video_stream_enable bit, controller waits for 16 MTPs before starting stream symbol sequence insertion for this particular stream. Until this time, DPTX sends VCPF symbol sequence in the time-slot for this video stream.
k. If content protection is required, then enable video after configure HDCP.

22.6.1.9 Configure Audio mode

From step 4, the audio configuration of the Sink are read and the controller is configured to set up the audio mode accordingly by the following steps.

- Program the AUDIO_CONFIG1 register specifying the audio configuration controls
  - audio_inf_select – Select the primary Audio interface option, I2S or SPDIF.
  - audio_data_in_en – Specify which of the data input pins are active. For example for the i2s interface if all 8 channels are supported then all 4 data inputs must be enabled by writing h'F to this field.
  - Audio_data_width – Specify the audio sample data width (16 to 24 bits).
  - hbr_mode_enable – Specify if High Bit Rate audio is to be enabled or not
- Enable transmission of Audio Stream SDP by setting the SDP_VERTICAL_CTRL/SDP_HORIZONTAL_CTRL register bits 1 and 0. From this time, the audio sampler is enabled and the audio samples presented at the I2S/SPDIF inputs are sampled in to the audio FIFOs. Before the audio stream is enabled, the I2S or SPDIF data could be active. But these samples are not transmitted on the main link by the controller.

22.6.1.10 Configure SDPs (Secondary Data Packets)

- Program the SDP_REGISTER_BANK registers with the header and payload of the SPD that are required to be transmitted.
- Program the SDP_VERTICAL_CTRL and SDP_HORIZONTAL_CTRL registers to indicate when the specific SDP register set need to be transmitted. Also specify the priority by using Bit 31 of these registers.
- If Manual control is required, then program the SDP_MANUAL_CTRL register.

22.6.1.11 Configure HDCP2.2

The following steps must be followed for configuring the HDCP.

1. Program the Synopsys HDCP2.2 controller for the HDCP2.2 initialization. Check the Synopsys HDCP2.2 controller for details.
2. After booting the HDCP2.2 controller, Enable HDCP by setting the HDCPCFG[1] register.
3. Wait for HDCP22 GPIO status change interrupt and check HDCP sink capability by checking the HDCPOBS[28:27] bits.
4. If the sink is not HDCP2.2, go to Step12. If the sink is HDCP2.2 then Call the HL_tx_authenticate() function in the HDCP2.2 library to start the authentication process.
5. Wait for HDCP interrupt and check the authentication status by reading the HDCPOBS register bits 29 and 30.
6. If the authentication is successful, then mainstream are encrypted after this. If authentication is not successful, then it is up to the driver to take the next action.

22.6.1.12 Configure HDCP1.3

1. Configure device private keys when DPTX_HDCP_DPK_ROMLESS configuration parameter is set to true.ie Go to step 13 and return
2. Set HDCPCFG. DPCD12PLUS to 1 if the DPCD revision is 1.2 or higher
3. Write the revocation list to memory.ie Go to step 14 and return
4. Write HDCP_CONFIG [2] to enable HDCP1.3 functionality.
5. Wait for HDCP interrupt indicating authentication success/failure (HDCPAPIINTSTAT.HDCPENGAGED)
6. If authentication is successful, mainstream is encrypted after this. If authentication is not successful, then it is up to the driver to take the next action.

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22.6.1.13 Configure Device private keys

1. Disable decryption logic HDCPREG_RMLCTL.ODPK_DECRYPT_ENABLE=0
2. Poll for HDCPREG_RMLSTS. IDPK_WR_OK_STS=1
3. Write unencrypted AKSV[39:32] in HDCPREG_DPK1
4. Write unencrypted AKSV[31:0] in HDCPREG_DPK0
5. Poll for HDCPREG_RMLSTS. IDPK_WR_OK_STS=1 and HDCPREG_RMLSTS. IDPK_DATA_INDEX=1
6. Enable decryption logic HDCPREG_RMLCTL.ODPK_DECRYPT_ENABLE=1
7. Write encryption seed ENC_KEY[15:0] in HDCPREG_SEED
8. Set DPK index value = 1
9. Write DPK[DPK Index value][55:32] to HDCPREG_DPK1
10. Write DPK[DPK Index value][31:0] to HDCPREG_DPK0
11. Poll for HDCPREG_RMLSTS. IDPK_WR_OK_STS=1 and HDCPREG_RMLSTS. IDPK_DATA_INDEX= (DPK Index value+1)
12. Increment DPK Index value by 1
13. Repeat step h to step m till DPK index value reaches 40
14. Read CRC32 value calculated by controller over unencrypted DPKs in HDCPREG_DPK_CRC register
15. Compare the CRC from controller with the original CRC to check for DPK programming result.

22.6.1.14 Program Revocation list

Revocation list is stored in a 8-bit data width SPRAM, though the memory data width is 8-bis, it can only be accessed through 32-bit register read writes so the 8-bit values need to accumulated and written as 32-bit values, do read modify writes if the address does not start at a dword boundary.

Following steps illustrate how it is done.

1. Read HDCP_REVOC_LIST[0]|HDCP_REVOC_SIZE[0:1]|HDCP_VH[19] values by doing a 32-bit register read to address 0x10B8. Keep HDCP_VH[19] unmodified, update HDCP_REVOC_LIST[0]|HDCP_REVOC_SIZE[0:1] and write back the values to the same 32-bit register
2. Set revocation list loop count to 0
3. Write HDCP_REVOC_LIST[2+revocation list loop count: 5+revocation list loop count] by doing a 32-bit register write to address 0x10BC+(revocaltion list loop count*4)
4. Increment revocation list loop count
5. If (revocation list loop count *4+2) is greater than HDCP_REVOC_SIZE repeat steps step b through step e, else exit

22.6.2 Programming Flow After Re-Authentication Request/Link Integrity Failure from Sink Application

The re-authentication/Link Integrity Failure condition is detected by the driver under the following condition.

- HPD Interrupt is generated. After an interrupt is received, read the INTERRUPTS and see if HPD_EVENT is set. Then check that HPD_STATUS is 1. Clear the HPD_STATUS
- Read the DPCD register and check DPCD.CP_IRQ bit to be set. Write 1 to DPCD.CP_IRQ register field to clear the interrupt. If CP_IRQ is set proceed to next step
- Set the HDCPCFG.CPIRQ bit and clear it after 10 clock cycles.

Controller internally reads Bstatus and checks for Link Integrity failure or re-authentication request and initiates authentication if any of the bits are set. Controller stops encryption at the next CPSR boundary.

22.6.3 Programming Flow After a Hot Unplug Event

This interrupt is generated when the Sink is connected and HPD transition from 1 to 0 staying at 0 for greater than 2 ms. This section indicates how the software handles the interrupt.

1. Software receives an interrupt and reads the GENERAL_INTERRUPT register. GENERAL_INTERRUPT.HPD_EVENT is set. It should also see that HPD_STATUS.HPD_STATUS is 0.

2. The software clears PHYIF_CTRL.XMIT_ENABLE on all lanes to turn off the transmitter. Optionally, PHYIF_CTRL.PHY_LANEX_POWERDOWN can be set to 3 for all enabled lanes to

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save power.

3. Software clears the interrupt by writing 1 to GENERAL_INTERRUPT.HPD_EVENT.

22.6.4 Programming Flow After a Hot Unplug Event

Follow these steps for Hot plug event after an unplug event:

- Program HDCP soft reset and release it (SOFT_RESET_CTRL.HDCP_MODULE_RESET=1). This step is needed as the HDCP controller is unaware of the unplug event and needs to be reset.
- If audio is enabled, then it should be disabled along with the audio timestamp SDPs by clearing bits 0 and 1 of SDP_VERTICAL_CTRL and SDP_HORIZONTAL_CTRL registers. In addition, the audio sampler should be reset by writing to SOFT_RESET_CTRL. AUDIO_SAMPLER_RESET.
- Follow steps 4 to steps 7. This includes the EDID and DPCP reads.
- steps 8 to steps 11 might be required based on the previous steps.

22.6.5 Programming Flow Sequence for HDCP

The figure below shows the programming flow sequence for HDCP.

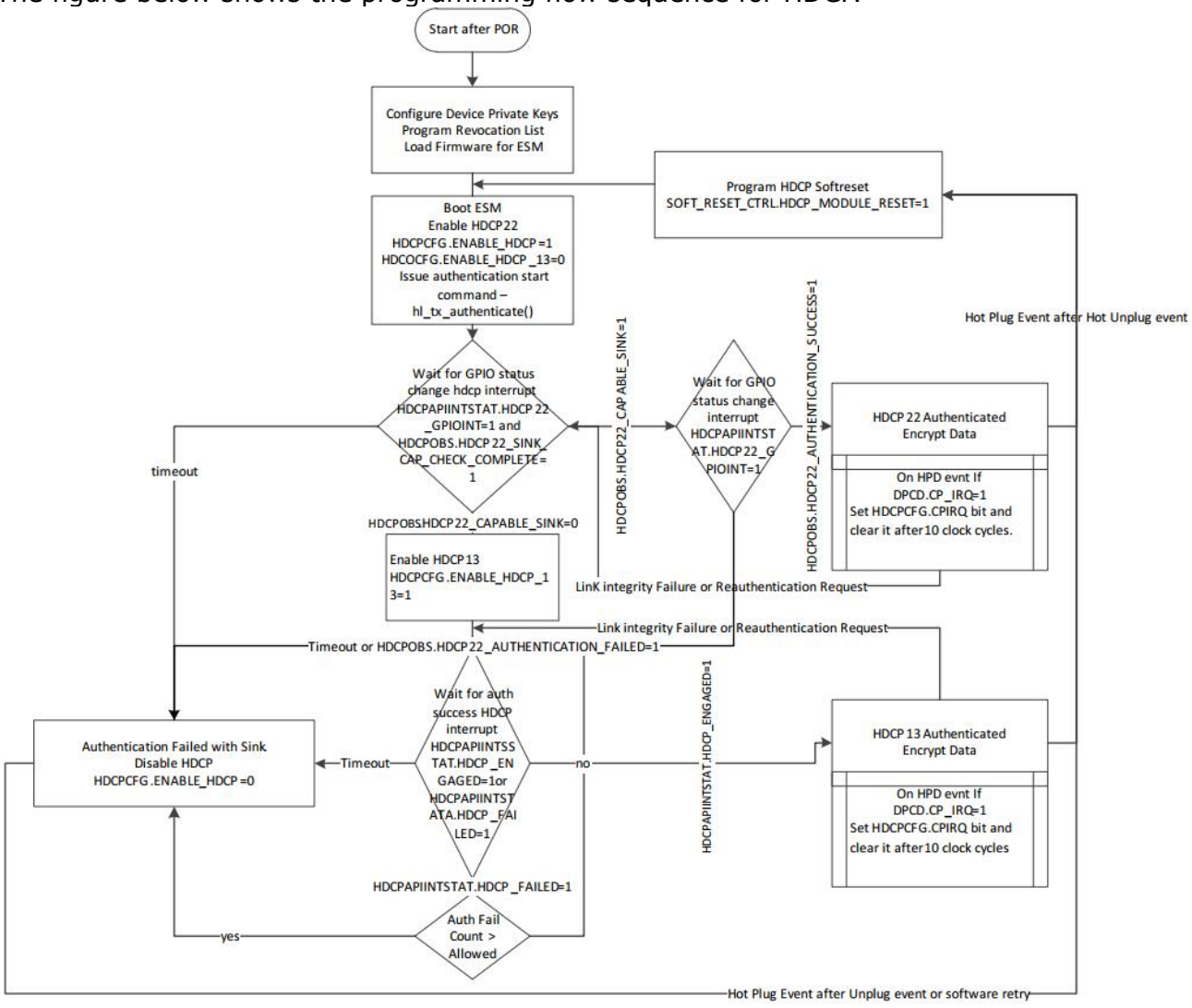


Fig. 22-5 Programming Flow Sequence for HDCP

22.6.6 Link training Sequence

22.6.6.1 Initialization Without Link Training

This initialization sequence assumes that the PHY does not need to go through the link training sequence. This is used to speed up RTL simulation or if the DP Sink Device is capable of receiving Main-Link signal without link training.

1. Set the PHY soft reset. Clear after 5us.
2. Ensure that PHYIF_CTRL.PHY_LANEX_POWERDOWN=0 for all enabled lanes.
3. Set PHYIF_CTRL.PHY_LANES to the desired number of lanes and PHYIF_CTRL.PHY_RATE to the desired rate.

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4. Wait until PHYIF_CTRL.PHY_BUSY is cleared for the desired lanes that have been enabled. For example, if 4 lanes are enabled, then wait until PHYIF_CTRL.PHY_BUSY[3:0]=4'h0. If only 1 lane enabled, then wait until PHYIF_CTRL.PHY_BUSY[0]=0
5. Program the predetermined pre-emphasis and voltage swing values into the PHY_TX_EQ registers if required.
6. Enable the transmitter by setting PHYIF_CTRL.XMIT_EN for each enabled lane.

22.6.6.2 Basic Link Bring up Sequence with Fast Link Training

This sequence is applicable if the PHY is to use predetermined pre-emphasis and swing values. This sequence occurs if the Sink DPCD 00003h NO_AUX_TRANSACTION_LINK_TRAINING is read to be 1 and if the source policy is to initiate TPS1 and TPS2/3/4 for 500us each.

1. Set the PHY soft reset. Wait for the read to return 0.
2. Ensure that GENERAL_INTERRUPT_ENABLE.HPD_EVENT is cleared.
3. Wait for the sink to be connected
   a. After an interrupt is received, read the INTERRUPTS and see if HPD_EVENT is set. Then check that HPD_STATUS.HPD_STATUS is 1. This indicates that the Sink has been connected.
   b. If IRQ_HPD is received instead of HPD_EVENT and DPCD Revision is 1.2 or greater, then check LINK_SERVICE_IRQ_VECTOR_ESI0.RX_CAP_CHANGED bit. This also indicates that the Sink has been connected. Also recheck if NO_AUX_TRANSACTION_LINK_TRAINING is still set. If it is cleared, then do a full link training process.
4. Ensure that PHYIF_CTRL.PHY_LANEX_POWERDOWN=0 for all enabled lanes.
5. Based on the highest link rate, highest number of lanes supported, and Source policy, set
   PHYIF_CTRL.PHY_LANES, and PHYIF_CTRL.PH_YRATE.
6. Wait until PHYIF_CTRL.PHY_BUSY is cleared for the desired lanes that have been enabled. For example, if 4 lanes are enabled, then wait until PHYIF_CTRL.PHY_BUSY[3:0]=4'h0. If only 1 lane enabled, then wait until PHYIF_CTRL.PHY_BUSY[0]=0
7. Program the predetermined pre-emphasis and voltage swing values into the PHY_TX_EQ registers if required.
8. Set PHYIF_CTRL.TPS_SEL=1 to send TPS1
9. Enable the transmitter by setting PHYIF_CTRL.XMIT_EN for each enabled lane.
10. Wait for 500us.
11. Set PHYIF_CTRL.TPS_SEL to the following:
    a. 2 if HBR is the highest desired rate
    b. 3 if HBR2 is the highest desired rate
    c. 4 if HBR3 is the highest desired rate
12. Wait for 500us.
13. Set PHYIF_CTRL.TPS_SEL to 0

22.6.6.3 Full Link Bring up Sequence

By default, fast link training is enabled, which allows the controller to transmit fail safe video format, as specified in section "Fast Link Training". This feature should be disabled by clearing the CCTL.DEFAULT_FAST_LINK_TRAIN_EN register bit.

The default value of PHY power state from the controller is P3. For any PHY rate change operation, the power state must be P3 or P2.

1. Based on the highest link rate, highest number of lanes supported, and Source policy, set PHYIF_CTRL.PHY_LANES, and PHYIF_CTRL.PHY_RATE. If Rocket IO PHY is used, set PHYIF_CTRL.SSC_DIS=1.
2. Wait until PHYIF_CTRL.PHY_BUSY is cleared for the desired lanes that have been enabled. For example, if 4 lanes are enabled, then wait until PHYIF_CTRL.PHY_BUSY[3:0]=4'h0. If only 1 lane enabled, then wait until PHYIF_CTRL.PHY_BUSY[0]=0.
3. Set PHYIF_CTRL.TPS_SEL=0 to force the transmitted pattern to none.
   While using a PHY with Pipe Interface (DPTX_PHYIF_TYPE=2), transition the unused

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lanes to P3 before going to step 4. For example, if the number of lanes programmed in step 1 is 1, then the lanes 2, 3, and 4 should be transitioned to P3. Use the PHYIF_POWERDOWN_CTRL[0] register at offset 0xA18 for this. The PHYIF_PWRDOWN_CTRL[0].PER_LANE_PWRDOWN_CTL_EN register should be set to 1. The PHYIF_CTRL.PHY_POWERDOWN register is not used for controlling individual lanes powerdown.

4. Program the pre-emphasis and voltage swing values into the PHY_TX_EQ registers corresponding to voltage swing level 0 and pre-emphasis level 0 for all enabled lanes.
5. Set PHYIF_CTRL.TPS_SEL=1 to send TPS1.
6. Enable the transmitter by setting PHYIF_CTRL.XMIT_EN for each enabled lane.
7. Set the following DPCD registers on the Sink – using AUX Channel Interface Registers:
   a. LINK_BW_SET register (DPCD Address 00100h) to the desired rate.
   b. LANE_COUNT_SET field in the LANE_COUNT_SET register (DPCD Address 00101h, bits 4:0) to the desired # of lanes.
   c. DOWNSPREAD_CTRL register (DPCD Address 00107h), SPREAD_AMP must be set to 1 for a regular PHY and 0 for Rocket IO.
   d. MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) to 01h.
   e. TRAINING_PATTERN_SET register (DPCD Address 00102h) to 21h.
   f. TRAINING_LANEx_SET register (DPCD Addresses 00103h through 00106h) for each lane to voltage swing level 0 and pre-emphasis level 0.
   g. Note that TRAINING_PATTERN_SET and TRAINING_LANEx_SET registers must be written in one AUX CH burst write transaction.
8. Read the DPCD Sink TRAINING_AUX_RD_INTERVAL field in the TRAINING_AUX_RD_INTERVAL register (DPCD Address 0000Eh, bits 6:0) and wait the specified time period before reading the LANEx_CR_DONE bit of the lane in the LANEx_y_STATUS register (DPCD Address 00202h, bits 0 and 4, and DPCD Address 00203h, bits 0 and 4, for Lanes 0, 1, 2, and 3, respectively, as appropriate).
   a. If LANEx_CR_DONE is not set for all enabled lane, then read for ADJUST_REQUEST_LANEx_y register (DPCD Address(es) 00206h and 00207h) for all enabled lanes, then set the local register PHY_TX_EQ to the requested level. Wait TRAINING_AUX_RD_INTERVAL and then re-read LANEx_CR_DONE.
   b. if LANEx_CR_DONE is still not set and the same voltage and swing levels have been tried 5times, then reduce the link rate by one level. Set PHYIF_CTRL.PHY_RATE accordingly. Wait until PHYIF_CTRL.PHY_BUSY is cleared for the desired lanes that have been enabled. Repeat <XREF>.
   c. If the rate is already reduced to RBR, but LANEx_CR_DONE is only set for 1 or 2 lanes, then set PHYIF_CTRL.PHY_LANES to match, and PHYIF_CTRL.PHY_RATE to the high supported rate. Repeat <XREF>. Training fails if LANEx_CR_DONE is never set for any lane.
   d. If LANEx_CR_DONE is set for all enabled lanes, then move on to the next step.
9. Set PHYIF_CTRL.TPS_SEL to the following
   - if HBR is the highest desired rate
   - 3 if HBR2 is the highest desired rate
   - 4 if HBR3 is the highest desired rate
10. Write the following to the DPCD sink registers: 22h for TPS2, 23h for TPS3, or 07h for TPS4 to the TRAINING_PATTERN_SET register (DPCD Address 00102h) and the current drive setting to the TRAINING_LANEx_SET register (DPCD Addresses 00103h through 00106h). Ensure that scrambling (CCTL.SCRAMBLE_DISABLE = 0) is enabled if TPS4 is transmitted.
11. Wait TRAINING_AUX_RD_INTERVAL, and then read the following:
    - LANEx_CR_DONE
    - LANEx_CHANNEL_EQ_DONE bit in the LANEx_y_STATUS register (DPCD Address 00202h, bits 1 and 5, and DPCD Address 00203h, bits 1 and 5, for Lanes 0, 1, 2, and 3, respectively, as appropriate)
    - LANEx_SYMBOL_LOCKED bit in the LANEx_y_STATUS register (DPCD Address 00202h, bits 2 and 6, and DPCD Address 00203h, bits 2 and 6, for Lanes 0, 1, 2, and 3, respectively, as appropriate)

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- INTERLANE_ALIGN_DONE bits in the LANE_ALIGN__STATUS_UPDATED and LANE_ALIGN__STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, bit 0, respectively)

12. Wait TRAINING_AUX_RD_INTERVAL, and then read the following:
    - If some of the register values are still 0, then ADJUST_REQUEST_LANEx_y register (DPCD Address(es) 00206h and 00207h) and adjust PHY_TX_EQ according the requested drive level settings. Repeat step 9.
    - If after 5 iterations, the EQ bits are not set, then reduce rate. Set PHYIF_CTRL.PHY_RATE accordingly. Wait until PHYIF_CTRL.PHY_BUSY is cleared for the desired lanes that have been enabled. Repeat step 9.
    - If the rate is already reduced to RBR, then do the following:
      Clear the TRAINING_PATTERN_SET register (DPCD Address 00102h).
      Set PHYIF_CTRL.TPS_SEL =1 and set PHY_TX_EQ to default voltage swing and pre-emphasis (400mV, no pre-emphasis).
      Write 21h to the TRAINING_PATTERN_SET register (and appropriate values to the TRAINING_LANEx_SET register (DPCD Addresses 00103h through 00106h)) to initiate
      training
13. Set PHYIF_CTRL.TPS_SEL to 0 when finished. Set DPCD Sink TRAINING_PATTERN_SET register to 00h.

22.6.6.4 Combo PHY

- For rate changes, PHYIF_CTRL.PHY_LANE0_POWERDOWN must be set to 2 or 3 and PHYIF_CTRL.PHY_BUSY must be low before PHYIF_CTRL.PHY_RATE is changed. P2 can be used to change rates more quickly than P3.
- Only PHYIF_CTRL.PHY_LANE0_POWERDOWN is used for the Combo PHY. PHYIF_CTRL.PHY_LANE{1,2,3}_POWERDOWN have no effect.
- Every bit of PHYIF_CTRL.PHY_BUSY[15:13] is the same as PHYIF_CTRL.PHY_BUSY[12].

22.6.7 AUX Channel Access

1. If write set AUX_DATA 0/1/2/3 first. Then write the CMD register with the desired CMD_TYPE, ADDR and LENGTH. Note the CMD register is transmitted as-is over the AUX channel so make sure unused bits are '0'.
2. Once the write to the CMD register is done, the request is queued for execution and additional writes to the data/cmd registers are disabled. The register bit AUX_STATUS.AUX_REPLY_RECEIVED is set to indicate the AUX channel is ACTIVE/BUSY.
3. Wait for an interrupt, and check to see if GENERAL_INTERRUPT.AUX_REPLY_EVENT is set.
   Alternatively, if INTERRUPT_ENABLE.AUX_REPLY_EVENT_EN is reset, software can poll AUX_STATUS.AUX_REPLY_RECEIVED to see if a response has been received. This bit resets to '0' when the AUX transfer completes.
4. If GENERAL_INTERRUPT.AUX_REPLY_EVENT=1, then software can read AUX_STATUS to find the outcome of the AUX transfer.
   - If the AUX_STATUS.AUX_STATUS is AUX ACK then the AUX request is fully executed and read data is available in AUX_DATA0/1/2/3.
   - If it is AUX WRITE NACK, then the software can read AUX_STATUS.AUX_M indicates the number of bytes that are written.
5. If AUX_STATUS.AUX_TIMEOUT is set or the AUX_STATUS.AUX_STATUS is AUX NACK or AUX DEFER, then AUX_DATA0/1/2/3 are not valid.
6. Clear GENERAL_INTERRUPT.AUX_REPLY_EVENT.
7. If the SINK response is other than ACK, it is the SW responsibility to follow the DP spec and continue with the appropriate AUX request.

22.6.8 Test 80-bit Custom Pattern Programming

1. Read DPCD TEST_80BIT_CUSTOM_PATTERN (00250h to 025Bh)
2. Program CUSTOMPAT0/1/2 according to the TEST_80BIT_CUSTOM_PATTERN[79:0] read from the DPCD.
3. Based on the desired link rate, highest number of lanes supported, and Source policy, set PHYIF_CTRL.PHY_LANES and PHYIF_CTRL.PHY_RATE.
4. Wait until PHYIF_CTRL.PHY_BUSY is cleared for the desired lanes that have been

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enabled. For example, if 4 lanes are enabled, then wait until PHYIF_CTRL.PHY_BUSY[3:0]=4'h0. If only 1 lane enabled, then wait until PHYIF_CTRL.PHY_BUSY[0]=0

5. Set PHYIF_CTRL.XMIT_ENABLE for each enabled lane to enable the transmission.
6. You can check the CONTINUOUS_80BIT_PATTERN_FROM_DPRX_AUX_CH_CAP is supported and set CONTINUOUS_80BIT_PATTERN_FROM_DPRX_AUX_CH_EN=1 along with the DURATION_CTRL=1. (DPCD 0025Bh). This step can be omitted for standalone testing with an oscilloscope.

22.6.9 INIT_THRESHOLD Value Calculation

The INIT_THRESHOLD determines how many clock cycles the link packetizer logic should wait after the pixel data is available in the lane steering FIFO, before reading it and transmitting it on the link. Based on the lane steering logic push rate and the link rate, this value changes for various modes of operations. The calculated value should be programmed into the INIT_THRESHOLD, and INIT_THRESHOLD_HI fields of the VIDEO_CONFIG5 register.

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Chapter 23 EDP TX Controller

23.1 Overview

This eDP TX is compliant with DisplayPort standard 1.2a and standard eDP 1.3. DisplayPort is an industry standard to accommodate the growing broad adoption of digital display technology within the PC and consumer electronics (CE) industries. It consolidates the internal and external connection methods to reduce device complexity and cost, supports necessary features for key cross industry applications, and provides performance scalability to enable the next generation of displays featuring higher color depths, refresh rates, and display resolutions.

EDP TX Controller supports the following features:

- Compliant with DisplayPort™ Specification, Version 1.2
- Compliant with eDP™ Specification, Version 1.3
- Main link containing 4 physical lanes of 5.4/2.7/1.62 Gbps/lane
- Bi-directional auxiliary link with up to 1Mbps speed
- Support RGB, YCbCr 4:4:4, YCbCr 4:2:2 and 8/10 bit per component video format
- Support HDCP v1.3, integrated HDCP encryption engine for transmitting protected audio and video content
- Support PSR
- Support I2S audio interface, the maximum number of channels is 8
- Support S/PDIF audio interface
- 24/26 MHz crystal clock
- PRBS or programmable transmitter pattern for main link quality test
- Hot plug and unplug detection and link status monitor
- Supports reading of the display EDID

23.2 Block Diagram

EDP TX Controller comprises with:

- Video Data Capture
- Audio Data Capture
- EDP Transmitter
- APB Slave Interface
- EDPTX PHY

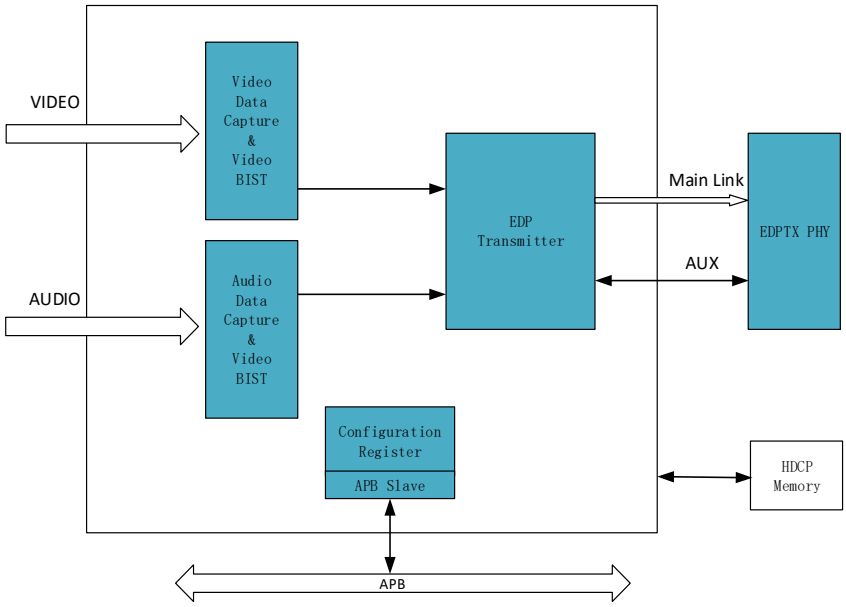


Fig. 23-1 EDP TX Controller Block Diagram

23.3 Function Description

23.3.1 Video Data Capture

The video data comes from VOP or EBC. The eDP TX receives signals and stores the video

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signals into the buffer. Afterward, the DP transmitter reads data from the buffer.

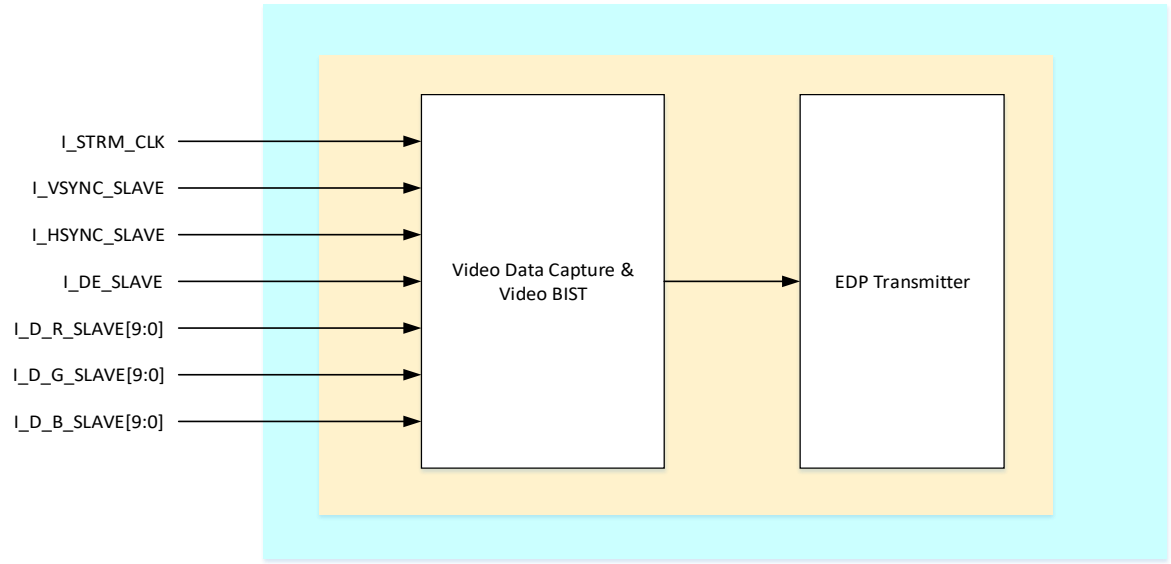


Fig. 23-2 Block diagram of Video Interface

23.3.2 Audio Data Capture

The audio data comes from I2S or S/PDIF. For audio, there are two interface: S/PDIF slave and I2S slave. In S/PDIF slave mode, the audio stream is sent from the S/PDIF input. In I2S slave mode, the audio stream is sent from the I2S S/PDIF input.

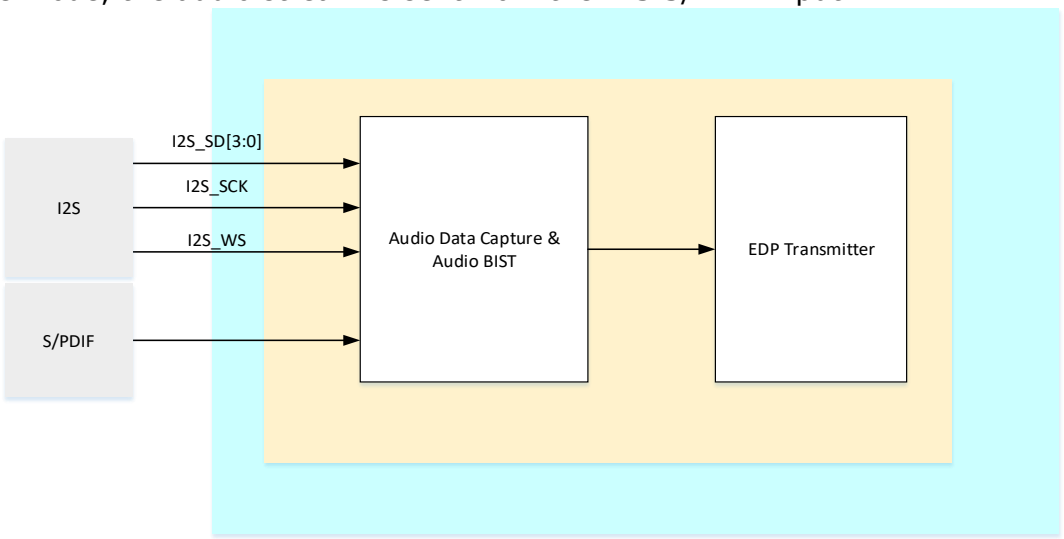


Fig. 23-3 Audio data interface block diagram

23.3.3 EDP Transmitter

The EDP_TX gets the video data from the Video FIFO module. Then the video data will be packed into TU (Transfer Unit). The Info Frame is passed directly through the APB interface. Some main link attributes data come from APB interface, but the information of input video timing of main link attribute come from Video Capture module.

23.3.4 APB Slave Interface

The APB slave interface is used at the configuration registers interface. Configure eDP TX and get its status. HDCP key memory is whiten by the APB slave interface, too.

23.3.5 EDPTX PHY

The eDP TX PHY is combo transmit eDP and HDMI. In eDP mode, it can support 4 physical lanes of 5.4/2.7/1.62 Gbps/lane and bi-directional auxiliary link with up to 1Mbps speed.

23.4 Register Description

23.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

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23.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
EDPTX_DP_TX_VERSION	0x0010	W	0x00000060	DPTX Version
EDPTX_FUNC_EN_1	0x0018	W	0x0000007D	Function Enable Register 1
EDPTX_FUNC_EN_2	0x001C	W	0x00000087	Function Enable Register 2
EDPTX_VIDEO_CTL_1	0x0020	W	0x00000000	Video Control Register 1
EDPTX_VIDEO_CTL_2	0x0024	W	0x00000010	Video Control Register 2
EDPTX_VIDEO_CTL_3	0x0028	W	0x00000000	Video Control Register 3
EDPTX_VIDEO_CTL_4	0x002C	W	0x00000000	Video Control Register 4
EDPTX_VIDEO_CTL_8	0x003C	W	0x00000020	Video Control Register 8
EDPTX_VIDEO_CTL_10	0x0044	W	0x00000000	Video Control Register 10
EDPTX_TOTAL_LINE_CFG_L	0x0048	W	0x00000000	Total Line Byte Configure Register
EDPTX_TOTAL_LINE_CFG_H	0x004C	W	0x00000000	Total Line High Byte Configure Register
EDPTX_ACTIVE_LINE_CFG_L	0x0050	W	0x00000000	Active Line Low Byte Configure Register
EDPTX_ACTIVE_LINE_CFG_H	0x0054	W	0x00000000	Active Line High Byte Configure Register
EDPTX_V_F_PORCH_CFG	0x0058	W	0x00000000	Vertical Front Porch Configure Register
EDPTX_V_SYNC_WIDTH_CFG	0x005C	W	0x00000000	Vertical Sync Width Configure Register
EDPTX_V_B_PORCH_CFG	0x0060	W	0x00000000	Vertical Back Porch Configure Register
EDPTX_TOTAL_PIXEL_CFG_L	0x0064	W	0x00000000	Total Pixel Low Byte Configure Register
EDPTX_TOTAL_PIXEL_CFG_H	0x0068	W	0x00000000	Total Pixel High Byte Configure Register
EDPTX_ACTIVE_PIXEL_CFG_L	0x006C	W	0x00000000	Active Pixel Low Byte Configure Register
EDPTX_ACTIVE_PIXEL_CFG_H	0x0070	W	0x00000000	Active Pixel High Byte Configure Register
EDPTX_H_F_PORCH_CFG_L	0x0074	W	0x00000000	Horizon Front Porch Low Byte Configure Register
EDPTX_H_F_PORCH_CFG_H	0x0078	W	0x00000000	Horizon Front Porch High Byte Configure Register
EDPTX_H_SYNC_CFG_L	0x007C	W	0x00000000	Horizon Sync Width Low Byte Configure Register
EDPTX_H_SYNC_CFG_H	0x0080	W	0x00000000	Horizon Sync Width High Byte Configure Register
EDPTX_H_B_PORCH_CFG_L	0x0084	W	0x00000000	Horizon Back Porch Low Byte Configure Register
EDPTX_H_B_PORCH_CFG_H	0x0088	W	0x00000000	Horizon Back Porch High Byte Configure Register
EDPTX_VIDEO_STATUS	0x008C	W	0x00000000	Input Video Status Register
EDPTX_TOTAL_LINE_STA_L	0x0090	W	0x00000000	Total Line Status Low Byte Register
EDPTX_TOTAL_LINE_STA_H	0x0094	W	0x00000000	Total Line Status High Byte Register
EDPTX_ACTIVE_LINE_STA_L	0x0098	W	0x00000000	Active Line Status Low Byte Register
EDPTX_ACTIVE_LINE_STA_H	0x009C	W	0x00000000	Active Line Status High Byte Register

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Name	Offset	Size	Reset Value	Description
EDPTX_V_F_PORCH_STA	0x00A0	W	0x00000001	Vertical Front Porch Status Register
EDPTX_V_SYNC_STA	0x00A4	W	0x00000000	Vertical Sync Width Status Register
EDPTX_V_B_PORCH_STA	0x00A8	W	0x00000000	Vertical Back Porch Status Register
EDPTX_TOTAL_PIXEL_STA_L	0x00AC	W	0x00000000	Total Pixel Status Low Byte Register
EDPTX_TOTAL_PIXEL_STA_H	0x00B0	W	0x00000000	Total Pixel Status High Byte Register
EDPTX_ACTIVE_PIXEL_STA_L	0x00B4	W	0x00000000	Active Pixel Status Low Byte Register
EDPTX_ACTIVE_PIXEL_STA_H	0x00B8	W	0x00000000	Active Pixel Status High Byte Register
EDPTX_H_F_PORCH_STA_L	0x00BC	W	0x00000000	Horizon Front Porch Status Low Byte Register
EDPTX_H_F_PORCH_STA_H	0x00C0	W	0x00000000	Horizon Front Porch Status High Byte Register
EDPTX_H_SYNC_STA_L	0x00C4	W	0x00000000	Horizon Sync Width Status Low Byte Register
EDPTX_H_SYNC_STA_H	0x00C8	W	0x00000000	Horizon Sync Width Status High Byte Register
EDPTX_H_B_PORCH_STA_L	0x00CC	W	0x00000000	Horizon Back Porch Status Low Byte Register
EDPTX_H_B_PORCH_STA_H	0x00D0	W	0x00000000	Horizon Back Porch Status High Byte Register
EDPTX_SPDIF_AUDIO_CTL_0	0x00D8	W	0x00000000	SPDIF Audio Control Register 0
EDPTX_DP_AUDIO_CTL_1	0x00DC	W	0x00000000	DP Audio Control Register 1
EDPTX_SPDIF_AUDIO_STA_0	0x00E0	W	0x00000000	SPDIF Audio Status Register 0
EDPTX_SPDIF_AUDIO_STA_1	0x00E4	W	0x00000000	Audio SPDIF Status Register 1
EDPTX_SPDIF_ERR_THRD	0x00E8	W	0x00000001	SPDIF Error Threshold Register
EDPTX_SPDIF_ERR_CNT	0x00EC	W	0x00000000	SPDIF Error Counter Register
EDPTX_AUDIO_BIST_CTL	0x00F0	W	0x00000000	Audio BIST Control Register
EDPTX_AUD_FREQ_CNT_1	0x00F4	W	0x00000000	Audio Input Clock Frequency Counter Register 1
EDPTX_AUD_FREQ_CNT_2	0x00F8	W	0x00000000	Audio Input Clock Frequency Counter Register 2
EDPTX_AVI_DB	0x01D0	W	0x00000000	AVI InfoFrame Packet Data Byte, address is Base + 0x01D0 ~ Base + 0x0200, AVI_DB1 ~ AVI_DB13
EDPTX_AUDIO_DB	0x021C	W	0x00000000	Audio InfoFrame Packet Data Byte, address is Base + 0x021C ~ Base + 0x0240, AUDIO_DB1 ~ AUDIO_DB10
EDPTX_IF_TYPE	0x0244	W	0x00000000	InfoFrame Packet Type Code.
EDPTX_IF_PKT_DB	0x0254	W	0x00000000	InfoFrame Packet Data Byte, address is Base + 0x0254 ~ Base + 0x02B4, IF_PKT_DB1 ~ IF_PKT_DB25

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Name	Offset	Size	Reset Value	Description
EDPTX_MPEG_DB	0x02D0	W	0x00000000	MPEG Source InfoFrame Packet Data Byte, address is Base + 0x02D0 ~ Base + 0x02F4, MPEG_DB1 ~ MPEG_DB10
EDPTX_REUSE_SPD_HB	0x02F8	W	0x00000000	Reuse SPD HB0 ~ HB3, address is Base + 0x02F8 ~ Base + 0x0304
EDPTX_REUSE_SPD_PB	0x0308	W	0x00000000	Reuse SPD PB0 ~ PB3, address is Base + 0x0308 ~ Base + 0x0314
EDPTX_PSR_FRAME_UPDATA_CTRL	0x0318	W	0x00000000	PSR frame update control
EDPTX_VSC_SHADOW_DB	0x031C	W	0x00000000	VSC shadow data bytes 0 ~ 7, address is Base+ 0x031C ~ Base+ 0x0338, VSC_SHADOW_DB0 ~ VSC_SHADOW_DB7
EDPTX_VSC_SHADOW_PB	0x033C	W	0x00000000	VSC shadow parity bytes 0 ~ 1, address is Base+ 0x033C ~ Base+ 0x0340, VSC_SHADOW_PB0 ~ VSC_SHADOW_PB1
EDPTX_AUDIO_I2S_CH_STA1	0x0344	W	0x00000000	Audio I2S Channel Status Register 1
EDPTX_AUDIO_I2S_CH_STA2	0x0348	W	0x00000000	Audio I2S Channel Status Register 2
EDPTX_AUDIO_I2S_CH_STA3	0x034C	W	0x00000000	Audio I2S Channel Status Register 3
EDPTX_AUDIO_I2S_CH_STA4	0x0350	W	0x00000000	I2S Channel Status Register 4
EDPTX_AUDIO_I2S_CH_STA5	0x0354	W	0x00000000	Audio Channel Status Register 5
EDPTX_LANE_MAP	0x035C	W	0x00000055	Lane Map Register
EDPTX_INT_STATE	0x03C0	W	0x00000000	Interrupt Status Register
EDPTX_COMMON_INT_STA_1	0x03C4	W	0x00000000	Common Interrupt Status Register 1
EDPTX_COMMON_INT_STA_2	0x03C8	W	0x00000000	Common Interrupt Status Register 2
EDPTX_COMMON_INT_STA_3	0x03CC	W	0x00000000	Common Interrupt Status Register 3
EDPTX_COMMON_INT_STA_4	0x03D0	W	0x00000000	Common Interrupt Status Register 4
EDPTX_SPDIF_BIPHASE_INT_STA	0x03D4	W	0x00000000	SPDIF Biphase Interrupt Status Register
EDPTX_DP_INT_STA	0x03DC	W	0x00000000	DisplayPort Interrupt Status Register
EDPTX_COMMON_INT_MASK_1	0x03E0	W	0x00000000	Interrupt Mask Register
EDPTX_COMMON_INT_MASK_2	0x03E4	W	0x00000000	Interrupt Mask Register
EDPTX_COMMON_INT_MASK_3	0x03E8	W	0x00000000	Interrupt Mask Register
EDPTX_COMMON_INT_MASK_4	0x03EC	W	0x00000000	Interrupt Mask Register
EDPTX_DP_INT_STA_MASK	0x03F8	W	0x00000000	Interrupt enable Register

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Name	Offset	Size	Reset Value	Description
EDPTX_INT_CTL	0x03FC	W	0x00000001	Interrupt Control Register
EDPTX_SYS_CTL_1	0x0600	W	0x00000000	System Control Register 1
EDPTX_SYS_CTL_2	0x0604	W	0x00000000	System Control Register 2
EDPTX_SYS_CTL_3	0x0608	W	0x00000000	System Control Register 3
EDPTX_SYS_CTL_4	0x060C	W	0x00000000	System Control Register 4
EDPTX_DP_VID_CTL	0x0610	W	0x00000000	DP Video Control Register
EDPTX_PKT_SEND_CTL	0x0640	W	0x00000000	Packet Send Control Register.
EDPTX_DP_HDCP_CTL	0x0648	W	0x00000000	DisplayPort HDCP Control Register.
EDPTX_SPDIF_PHASE1_CTL_0	0x0650	W	0x00000000	This register control SPDIF 1 cycle phase counter value [7:0]
EDPTX_SPDIF_PHASE1_CTL_1	0x0654	W	0x00000000	This register enables force of the 1 cycle phase counter value [8]
EDPTX_SPDIF_PHASE2_CTL_0	0x0658	W	0x00000000	This register control SPDIF 2 cycle phase counter value [7:0]
EDPTX_SPDIF_PHASE2_CTL_1	0x065C	W	0x00000000	This register control SPDIF 2 cycle phase counter value [8]
EDPTX_SPDIF_PHASE3_CTL_0	0x0660	W	0x00000000	This register control SPDIF 3 cycle phase counter value [7:0]
EDPTX_SPDIF_PHASE3_CTL_1	0x0664	W	0x00000000	This register control SPDIF 3 cycle phase counter value [8]
EDPTX_LINK_BW_SET	0x0680	W	0x0000000A	Main link bandwidth setting
EDPTX_LANE_COUNT_SET	0x0684	W	0x00000000	Main link lane count
EDPTX_DP_TRAINING_PTN_SET	0x0688	W	0x00000000	DP Training Pattern Set Register
EDPTX_DP_LN0_LINK_TRAINING_CTL	0x068C	W	0x00000000	DP Lane 0 Link Training Control Register.
EDPTX_DP_LN1_LINK_TRAINING_CTL	0x0690	W	0x00000000	DP Lane 1 Link Training Control Register.
EDPTX_DP_LN2_LINK_TRAINING_CTL	0x0694	W	0x00000000	DP Lane 2 Link Training Control Register.
EDPTX_DP_LN3_LINK_TRAINING_CTL	0x0698	W	0x00000000	DP Lane 3 Link Training Control Register.
EDPTX_DP_HW_LINK_TRAINING_CTL	0x06A0	W	0x00000000	DP hardware training control registers.
EDPTX_HPD_DEGLITCH_L	0x06C4	W	0x0000005E	HPD_DEGLITCH is used to de-glitch the HPD signal.
EDPTX_HPD_DEGLITCH_H	0x06C8	W	0x0000001A	HPD_DEGLITCH is used to de-glitch the HPD signal.
EDPTX_POLLING_PERIOD	0x06CC	W	0x0000000E	POLLING_PERIOD
EDPTX_DP_LINK_DEBUG_CTL	0x06E0	W	0x00000000	DP Link Debug Control Register
EDPTX_DP_SINK_COUNT	0x06E4	W	0x00000000	SINK_COUNT
EDPTX_DP_IRD_VECTOR	0x06E8	W	0x00000000	IRQ_VECTOR
EDPTX_DP_LINK_STATUS0	0x06EC	W	0x00000000	DP_LINK_STATUS0
EDPTX_DP_LINK_STATUS1	0x06F0	W	0x00000000	DP_LINK_STATUS1
EDPTX_DP_ALIGN_STATUS	0x06F4	W	0x00000000	ALIGN_STATUS
EDPTX_M_VID_0	0x0700	W	0x00000000	M_VID[7:0]
EDPTX_M_VID_1	0x0704	W	0x00000000	M_VID[15:8]
EDPTX_M_VID_2	0x0708	W	0x00000000	M_VID[23:16]

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Name	Offset	Size	Reset Value	Description
EDPTX_N_VID_0	0x070C	W	0x00000000	N_VID[7:0]
EDPTX_N_VID_1	0x0710	W	0x00000000	N_VID[15:8]
EDPTX_N_VID_2	0x0714	W	0x00000000	N_VID[23:16]
EDPTX_M_VID_MON	0x0718	W	0x00000000	M_VID value monitoring register
EDPTX_DP_VIDEO_FIFO_THRD	0x0730	W	0x00000000	DP Video Data FIFO Threshold Register
EDPTX_DP_GNS_CTRL	0x0734	W	0x00000000	DP GNS CONTROL REGISTER
EDPTX_DP_AUDIO_MARGIN	0x073C	W	0x00000000	DP Audio Margin Register
EDPTX_M_AUD_MON	0x0740	W	0x00000000	M_AUD value monitoring register
EDPTX_M_AUD_0	0x0748	W	0x00000000	M_AUD[7:0]
EDPTX_M_AUD_1	0x074C	W	0x00000000	M_AUD[15:8]
EDPTX_M_AUD_2	0x0750	W	0x00000000	M_AUD[23:16]
EDPTX_N_AUD_0	0x0754	W	0x00000000	N_AUD[7:0]
EDPTX_N_AUD_1	0x0758	W	0x00000000	N_AUD[15:8]
EDPTX_N_AUD_2	0x075C	W	0x00000000	N_AUD[23:16]
EDPTX_DP_M_CAL_CTL	0x0760	W	0x00000000	DP M Value Calculation Control Register
EDPTX_M_VID_GEN_FILTER_TH	0x0764	W	0x00000004	The threshold of M_VID generation filter
EDPTX_M_AUD_GEN_FILTER_TH	0x0778	W	0x00000002	The threshold of M_AUD generation filter
EDPTX_AUX_CH_STA	0x0780	W	0x00000000	AUX Channel Access Status Register
EDPTX_AUX_ERR_NUM	0x0784	W	0x00000000	AUX Channel Access Error Code Register
EDPTX_AUX_CH_DEFER_CTL	0x0788	W	0x0000007F	DP AUX CH DEFER Control Register
EDPTX_AUX_RX_COMM	0x078C	W	0x00000000	AUX CH received command
EDPTX_BUFFER_DATA_CTL	0x0790	W	0x00000000	DP Buffer Data Count Register
EDPTX_AUX_CH_CTL_1	0x0794	W	0x00000000	DP AUX Channel Control Register 1
EDPTX_AUX_ADDR_7_0	0x0798	W	0x00000000	AUX_ADDR[7:0]
EDPTX_AUX_ADDR_15_8	0x079C	W	0x00000000	AUX_ADDR[15:8]
EDPTX_AUX_ADDR_19_16	0x07A0	W	0x00000000	AUX_ADDR[19:16]
EDPTX_AUX_CH_CTL_2	0x07A4	W	0x00000000	DP AUX CH Control Register 2
EDPTX_BUF_DATA	0x07C0	W	0x000000FF	AUX CH buffer data 0 ~ 15, address is Base + 0x07C0 ~ Base+0x07FC
EDPTX_SOC_GENERAL_CTL	0x0800	W	0x00000000	General control register
EDPTX_DP_TEST_80B_PATTERN0	0x081C	W	0x00000000	DP test 80bit pattern0
EDPTX_DP_TEST_80B_PATTERN1	0x0820	W	0x00000000	DP test 80bit pattern1
EDPTX_DP_TEST_80B_PATTERN2	0x0824	W	0x00000000	DP test 80bit pattern2
EDPTX_AUD_CTL	0x0834	W	0x00000000	Audio Control register
EDPTX_CRC_CON	0x0890	W	0x00000000	CRC check control
EDPTX_CRC_RESULT	0x0894	W	0x00000000	CRC result
EDPTX_I2S_CTRL	0x09C8	W	0x00000000	I2S_CTRL

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Name	Offset	Size	Reset Value	Description
EDPTX_I2S_CH_SWAP	0x09CC	W	0x0000000B	I2S channel swap
EDPTX_I2S_CH_CTRL	0x09D0	W	0x000000E4	I2S channel control
EDPTX_I2S_CH_CTRL1	0x09D4	W	0x00000000	I2S channel control 1
EDPTX_LINK_POLICY	0x09D8	W	0x00000050	Link_Policy

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

23.4.3 Detail Register Description

EDPTX_DP_TX_VERSION

Address: Operational Base(0x27DC0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x60	dp_tx_version DPTX Version

EDPTX_FUNC_EN_1

Address: Operational Base(0x27DC0000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x1	vid_cap_func_en_n Video capture functions enable. 1'b0: Normal operation 1'b1: Disable video capture
5	RW	0x1	vid_fifo_func_en_n Video FIFO functions enable. 1'b0: Normal operation 1'b1: Disable video FIFO
4	RW	0x1	aud_fifo_func_en_n Audio FIFO functions enable. 1'b0: Normal operation. 1'b1: Disable audio FIFO.
3	RW	0x1	aud_func_en_n Audio FIFO and capture module function enable. 1'b0: Normal operation 1'b1: Disable audio FIFO and capture module If audio data (DMA or SPDIF) should be transmitted, AUD_FUNC_EN_N and AUD_FIFO_FUNC_EN_N should be set to 0 (enable).
2	RW	0x1	hdcp_func_en_n HDCP module functions enable. 1'b0: Normal operation 1'b1: Disable HDCP logic By disabling and enabling HDCP, all of registers in HDCP are cleared, except for the HDCP key inside of SPSRAM. Therefore, as an easy way to prepare re-authentication, firmware can disable and enable again to clear all HDCP registers.
1	RO	0x0	reserved
0	RW	0x1	sw_func_en_n Software defined function enable. 1'b0: Normal operation 1'b1: Disable all the function modules The bit has the highest priority, if the bit is 1, other function enable bits does not work.

EDPTX_FUNC_EN_2

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Address: Operational Base(0x27DC0000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	ssc_func_en_n SSC module enable. 1'b0: Normal mode 1'b1: Disable SSC module To apply updated SSC parameters into SSC operation, firmware must disable and enable this bit.
6:3	RO	0x0	reserved
2	RW	0x1	aux_func_en_n AUX channel module function enable. 1'b0: Normal operation 1'b1: Disable AUX channel module
1	RW	0x1	serdes_fifo_func_en_n Serdes FIFO function enable. 1'b0: Normal mode 1'b1: Disable Serdes FIFO To reset the serdes fifo, firmware must disable and enable this bit.
0	RW	0x1	ls_clk_domain_func_en_n Link symbol clock domain modules functions enable. 1'b0: Normal mode 1'b1: Disable the modules in link symbol clock domain. To reset the modules in link symbol clock domain, firmware must disable and enable this bit.

EDPTX_VIDEO_CTL_1

Address: Operational Base(0x27DC0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	video_en Video data input enable. 1'b0: Disable video data input 1'b1: Enable video data input It takes effect at next video frame.
6	RW	0x0	video_mute Video mute enable. In video mute mode, the solid color, specified in Base + 0x04A8 ~ Base + 0x04B0, is displayed. 1'b0: Disable 1'b1: Enable Output video data is changed properly as soon as this bit is configured.
5:0	RO	0x00	reserved

EDPTX_VIDEO_CTL_2

Address: Operational Base(0x27DC0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	in_d_range Dynamic range. This bit field is used to specify video data format in main stream attribute data. 1'b1: CEA range (16 ~ 235) 1'b0: VESA range (0 ~ 255)

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Bit	Attr	Reset Value	Description
6:4	RW	0x1	in_bpc Video input bit per color/ component (bpc). This bit field is used to specify video data format in main stream attribute data. Note that 6 bpc mode is invalid in YCbCr 422 mode. 3'b011: 12 bits 3'b010: 10 bits 3'b001: 8 bits 3'b000: 6 bits Other: Reserved
3:2	RO	0x0	reserved
1:0	RW	0x0	in_color_f Colorimetric format of input video. This is used to specify video data format in main stream attribute data. 2'b11: Reserved 2'b10: YCbCr444 2'b01: YcbCr422 2'b00: RGB

EDPTX_VIDEO_CTL_3

Address: Operational Base(0x27DC0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	in_yc_coeffi YCbCr Coefficients of input video. This is used to specify video data format in main stream attribute data. 1'b1: ITU709 1'b0: ITU601
6:5	RO	0x0	reserved
4	RW	0x0	vid_chk_update_type Select video format stability check method in video capture block. 1'b1: Check stability with the difference between adjacent frames. 1'b0: Check stability with the difference of differences between adjacent frames. Compares difference of 1st and 2nd to difference of 3rd and 4th frame.
3:0	RO	0x0	reserved

EDPTX_VIDEO_CTL_4

Address: Operational Base(0x27DC0000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	bist_en Video BIST enable. 1'b1: Enable video BIST 1'b0: Normal operation mode
2	RW	0x0	bist_width Control display BIST color bar width. 1'b1: Each bar is 64 pixel width. 1'b0: Each bar is 32 pixel width.
1:0	RW	0x0	bist_type Display BIST type. 2'b00: Color bar 2'b01: White, gray and black bar 2'b10: Mobile white bar 2'b11: Reserved

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EDPTX_VIDEO_CTL_8

Address: Operational Base(0x27DC0000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x2	vid_hres_th Video Frame Horizontal Resolution variation threshold for video capture block. This bit field is used by CAPTURE block to determine whether STRM_VALID should be asserted.
3:0	RW	0x0	vid_vres_th Video Frame Vertical Resolution variation threshold for video capture block. This bit field is used by CAPTURE block to determine whether STRM_VALID should be asserted.

EDPTX_VIDEO_CTL_10

Address: Operational Base(0x27DC0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	f_sel Video format select. 1'b1: Video format information from register 1'b0: Video format information from video_capture module According to the configuration of this bit field, the values of video format status registers in Base + 0x008C~ 0x00D0 are determined, which are transferred as main stream attribute packet. Note that if BIST_EN is set to 1, F_SEL must be cleared to 0 although video format information comes from registers set by user.
3	RO	0x0	reserved
2	RW	0x0	slave_i_scan_cfg Interlace scan mode configuration. 1'b0: Progressive 1'b1: Interlace When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.
1	RW	0x0	slave_vsync_p_cfg Slave mode VSYNC polarity configuration. 1'b1: Low is active. 1'b0: High is active. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.
0	RW	0x0	slave_hsync_p_cfg Slave mode HSYNC polarity configuration. 1'b1: Low is active. 1'b0: High is active. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_TOTAL_LINE_CFG_L

Address: Operational Base(0x27DC0000) + offset (0x0048)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	total_line_cfg_l TOTAL_LINE_CFG is used to specify the number of lines in each frame. This register is TOTAL_LINE_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_TOTAL_LINE_CFG_H

Address: Operational Base(0x27DC0000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	total_line_cfg_h TOTAL_LINE_CFG is used to specify the number of lines in each frame. This register is TOTAL_LINE_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When Video BIST_EN is enabled, this bit must be configured right to generate right video format.

EDPTX_ACTIVE_LINE_CFG_L

Address: Operational Base(0x27DC0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	active_line_cfg_l ACTIVE_LINE_CFG is used to specify the number of active lines in each frame. This register is ACTIVE_LINE_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_ACTIVE_LINE_CFG_H

Address: Operational Base(0x27DC0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	active_line_cfg_h ACTIVE_LINE_CFG is used to specify the number of active lines in each frame. This register is ACTIVE_LINE_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_V_F_PORCH_CFG

Address: Operational Base(0x27DC0000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	v_f_porch_cfg This is used to specify the number of lines in vertical front porch part. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_V_SYNC_WIDTH_CFG

Address: Operational Base(0x27DC0000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	v_sync_width_cfg This is used to specify the number of lines in VSYNC period. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_V_B_PORCH_CFG

Address: Operational Base(0x27DC0000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	v_b_porch_cfg This is used to specify the number of lines in frame back porch part. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_TOTAL_PIXEL_CFG_L

Address: Operational Base(0x27DC0000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	total_pixel_cfg_l TOTAL_PIXEL_CFG is used to specify the number of pixels in each line. This register is TOTAL_PIXEL_CFG[7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_TOTAL_PIXEL_CFG_H

Address: Operational Base(0x27DC0000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	total_pixel_cfg_h TOTAL_PIXEL_CFG is used to specify the number of pixels in each line. This register is TOTAL_PIXEL_CFG [13:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

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EDPTX_ACTIVE_PIXEL_CFG_L

Address: Operational Base(0x27DC0000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	active_pixel_cfg_l ACTIVE_PIXEL_CFG is used to specify the number of active pixels in each line. This register is ACTIVE_PIXEL_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_ACTIVE_PIXEL_CFG_H

Address: Operational Base(0x27DC0000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	active_pixel_cfg_h ACTIVE_PIXEL_CFG is used to specify the number of active pixels in each line. This register is ACTIVE_PIXEL_CFG [13:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_H_F_PORCH_CFG_L

Address: Operational Base(0x27DC0000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	h_f_porch_cfg_l H_F_PORCH_CFG is used to specify the number of pixels in frame horizon front porch part. This register is H_F_PORCH_CFG[7:0] When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_H_F_PORCH_CFG_H

Address: Operational Base(0x27DC0000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	h_f_porch_cfg_h H_F_PORCH_CFG is used to specify the number of pixels in frame horizon front porch part. This register is H_F_PORCH_CFG [11:8] When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_H_SYNC_CFG_L

Address: Operational Base(0x27DC0000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	h_sync_cfg_l H_SYNC_CFG is used to specify the number of pixels in HSYNC period. This register is H_SYNC_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_H_SYNC_CFG_H

Address: Operational Base(0x27DC0000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	h_sync_cfg_h H_SYNC_CFG is used to specify the number of pixels in HSYNC period. This register is H_SYNC_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_H_B_PORCH_CFG_L

Address: Operational Base(0x27DC0000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	h_b_porch_cfg_l H_B_PORCH_CFG is used to specify the number of pixel in frame horizon back porch part. This register is H_B_PORCH_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_H_B_PORCH_CFG_H

Address: Operational Base(0x27DC0000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	h_b_porch_cfg_h H_B_PORCH_CFG is used to specify the number of pixel in frame horizon back porch part. This register is H_B_PORCH_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_VIDEO_STATUS

Address: Operational Base(0x27DC0000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	field_s Interlace scan field status. 1'b1: Second field. 1'b0: First field. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

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Bit	Attr	Reset Value	Description
2	RW	0x0	i_scan_s Auto-detect interlace or progressive scan status: 1'b1: Interlace scan. 1'b0: Progressive scan. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.
1	RW	0x0	vsync_p_s Auto-detect VSYNC polarity: 1'b1: Low is active. 1'b0: High is active. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.
0	RW	0x0	hsync_p_s Auto-detect HSYNC polarity: 1'b1: Low is active. 1'b0: High is active. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_TOTAL_LINE_STA_L

Address: Operational Base(0x27DC0000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	total_line_sta_l TOTAL_LINE [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_TOTAL_LINE_STA_H

Address: Operational Base(0x27DC0000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	total_line_sta_h TOTAL_LINE [11:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_ACTIVE_LINE_STA_L

Address: Operational Base(0x27DC0000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	active_line_sta_l ACTIVE_LINE [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_ACTIVE_LINE_STA_H

Address: Operational Base(0x27DC0000) + offset (0x009C)

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Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	active_line_sta_h ACTIVE_LINE [11:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_V_F_PORCH_STA

Address: Operational Base(0x27DC0000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x01	v_f_porch_sta V_F_PORCH (vertical front porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_V_SYNC_STA

Address: Operational Base(0x27DC0000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	v_sync_sta V_SYNC_WIDTH (vertical sync width) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_V_B_PORCH_STA

Address: Operational Base(0x27DC0000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	v_b_porch_sta V_B_PORCH (vertical back porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_TOTAL_PIXEL_STA_L

Address: Operational Base(0x27DC0000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	total_pixel_sta_l TOTAL_PIXEL [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_TOTAL_PIXEL_STA_H

Address: Operational Base(0x27DC0000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x00	total_pixel_sta_h TOTAL_PIXEL [13:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_ACTIVE_PIXEL_STA_L

Address: Operational Base(0x27DC0000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	active_pixel_sta_l ACTIVE_PIXEL [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_ACTIVE_PIXEL_STA_H

Address: Operational Base(0x27DC0000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	active_pixel_sta_h ACTIVE_PIXEL [13:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_H_F_PORCH_STA_L

Address: Operational Base(0x27DC0000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	h_f_porch_sta_l H_F_PORCH [7:0] (horizon front porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_H_F_PORCH_STA_H

Address: Operational Base(0x27DC0000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	h_f_porch_sta_h H_F_PORCH [11:8] (horizon front porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_H_SYNC_STA_L

Address: Operational Base(0x27DC0000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	h_sync_sta_l H_SYNC [7:0] (horizon sync width) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_H_SYNC_STA_H

Address: Operational Base(0x27DC0000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	h_sync_sta_h H_SYNC [11:8] (horizon sync width) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_H_B_PORCH_STA_L

Address: Operational Base(0x27DC0000) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	h_b_porch_sta_l H_B_PORCH [7:0] (horizon back porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_H_B_PORCH_STA_H

Address: Operational Base(0x27DC0000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	h_b_porch_sta_h H_B_PORCH [11:8] (horizon back porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_SPDIF_AUDIO_CTL_0

Address: Operational Base(0x27DC0000) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	aud_spdif_en Set SPDIF audio stream input enable. 1'b0: Disable 1'b1: Enable
6:4	RO	0x0	reserved
3	RW	0x0	reuse_spd_en Reuse spd inforframe registers.

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Bit	Attr	Reset Value	Description
2	RW	0x0	force_spdif_det Force SPDIF_STREAM_DET, which is SPDIF detect status, to 1. (Test purpose only) 1'b1: Force SPDIF_STREAM_DET to 1. 1'b0: SPDIF_STREAM_DET is set by hardware detector.
1	RW	0x0	spdif_parity_ctrl Control the SPDIF parity generation scheme. In the IEC-60958, audio packet is 28-bit. But in the DP standard v1.1, the audio packet is 32-bit, 4 more control bits have been added. The control bit selects the parity scheme of original 28 bit defined in IEC-60958 or parity scheme of 32 bit defined in DP standard v1.1. 1'b1: Parity of DP link audio sample 32 bit. 1'b0: Parity of SPDIF audio sample 28 bit.
0	RW	0x0	spdif_clk_det_reset_bypass Bypass SPDIF clock detect auto reset: 1'b1: Bypass SPDIF clock detect auto reset, SPDIF module will not be reset even SPDIF clock is not detected. 1'b0: If SPDIF clock is not detected, SPDIF module is reset automatically.

EDPTX_DP_AUDIO_CTL_1

Address: Operational Base(0x27DC0000) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	aud_mute_en4 Audio data auto mute control enable for audio FIFO under run interrupt. 1'b1: Enable 1'b0: Disable
4	RW	0x0	aud_mute_en3 Audio data auto mute control enable for audio FIFO overrun interrupt. 1'b1: Enable 1'b0: Disable
3	RW	0x0	aud_mute_en2 Audio data auto mute control enable for HDCP failed interrupt. 1'b1: Enable 1'b0: Disable
2	RW	0x0	aud_mute_en1 Audio data auto mute control enable for SPDIF unstable interrupt. 1'b1: Enable 1'b0: Disable
1	RW	0x0	aud_mute_en0 Audio data auto mute control enable for Audio clock change interrupt. 1'b1: Enable 1'b0: Disable
0	RO	0x0	reserved

EDPTX_SPDIF_AUDIO_STA_0

Address: Operational Base(0x27DC0000) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	spdif_clk_det SPDIF audio clock detected flag. 1'b1: Clock detected 1'b0: Clock not detected
6:1	RO	0x00	reserved
0	RW	0x0	spdif_stream_det SPDIF audio stream detected flag. 1'b1: Input detected 1'b0: No input detected

EDPTX_SPDIF_AUDIO_STA_1

Address: Operational Base(0x27DC0000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	spdif_fs_freq Sampling clock frequency (corresponding to channel status bits [27:24]). 4'b0000: 44.1 KHz 4'b0010: 48 KHz 4'b0011: 32 KHz 4'b1000: 88.2 KHz 4'b1010: 96 KHz 4'b1110: 192 KHz Others: Reserved SPDIF_FS_FREQ can be read when SPDIF_STREAM_DET and VSYNC_DET are high.
3:0	RW	0x0	spdif_word_len Audio word length (corresponding to channel status bits [35:32]). 4'b0010: 16 bits 4'b0011: 20 bits 4'b0100: 18 bits 4'b0101: 22 bits 4'b1000: 19 bits 4'b1001: 23 bits 4'b1010: 20 bits 4'b1011: 24 bits 4'b1100: 17 bits 4'b1101: 21 bits SPDIF_WORD_LEN can be read when SPDIF_STREAM_DET and VSYNC_SET are high.

EDPTX_SPDIF_ERR_THRD

Address: Operational Base(0x27DC0000) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x01	spdif_err_thrd SPDIF parity error threshold for the SPDIF_ERR interrupt. When SPDIF stream data parity error occurs, the SPDIF_ERR_CNT will increase by 1. And when SPDIF_ERR_CNT equals to SPDIF_ERR_THRD, SPDIF_ERR interrupt happens.

EDPTX_SPDIF_ERR_CNT

Address: Operational Base(0x27DC0000) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	spdif_err_cnt SPDIF parity errors counter. Write any value to clear.

EDPTX_AUDIO_BIST_CTL

Address: Operational Base(0x27DC0000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	sin_ampl Set the Sin wave amplitude for audio BIST data. 4'b0000: 255 4'b0001: 510 4'b0010: 1020 4'b0011: 2040 4'b0100: 4080 4'b0101: 8160 4'b0110: 16320 4'b0111: 32640 4'b1000: 65280 4'b1001: 130560 4'b1010: 261120 4'b1011: 522240 4'b1100: 1044480 4'b1101: 2088960 4'b1110: 4177920 4'b1111: 8355840
3:1	RO	0x0	reserved
0	RW	0x0	aud_bist_en Audio BIST enable. 1'b1: Enable 1'b0: Disable

EDPTX_AUD_FREQ_CNT_1

Address: Operational Base(0x27DC0000) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	aud_freq_cnt_l Audio input clock frequency counter register. For test purpose only.

EDPTX_AUD_FREQ_CNT_2

Address: Operational Base(0x27DC0000) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	aud_freq_cnt_h Audio input clock frequency counter register. For test purpose only.

EDPTX_AVI_DB

Address: Operational Base(0x27DC0000) + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	avi_db AVI InfoFrame Packet Data Byte 1 ~ 13

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EDPTX_AUDIO_DB

Address: Operational Base(0x27DC0000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	audio_db Audio InfoFrame Packet Data Byte 1 ~ 10

EDPTX_IF_TYPE

Address: Operational Base(0x27DC0000) + offset (0x0244)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	if_type InfoFrame Packet Type Code. It can be set as (0x80 + InfoFrame Type Code) and send any type of infoframe defined in CEA-861C. Commonly, we set it as 0x83(0x80 + 0x03, 0x03 is the type code of SPD InfoFrame) and send SPD infoframe.

EDPTX_IF_PKT_DB

Address: Operational Base(0x27DC0000) + offset (0x0254)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	if_pkt_db InfoFrame Packet Data Byte 1 ~ 25. The registers define the data in the InfoFrame and the InfoFrame type is defined by IF_TYPE.

EDPTX_MPEG_DB

Address: Operational Base(0x27DC0000) + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	mpeg_db MPEG Source InfoFrame Packet Data Byte 1 ~ 10

EDPTX_REUSE_SPD_HB

Address: Operational Base(0x27DC0000) + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	reuse_spd_hb Reuse SPD HB0 ~ HB3

EDPTX_REUSE_SPD_PB

Address: Operational Base(0x27DC0000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	reuse_spd_pb Reuse SPD PB0 ~ PB3

EDPTX_PSR_FRAME_UPDATA_CTRL

Address: Operational Base(0x27DC0000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	psr_frame_up_type Select PSR Frame Update type. 1'b1: Burst single frame update 1'b0: Single frame update

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Bit	Attr	Reset Value	Description
0	RW	0x0	psr_frame_update Enable PSR Frame Update

EDPTX_VSC_SHADOW_DB

Address: Operational Base(0x27DC0000) + offset (0x031C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	vsc_shadow_db VSC shadow data bytes 0 ~ 7

EDPTX_VSC_SHADOW_PB

Address: Operational Base(0x27DC0000) + offset (0x033C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	vsc_shadow_pb VSC shadow parity bytes 0 ~ 1

EDPTX_AUDIO_I2S_CH_STA1

Address: Operational Base(0x27DC0000) + offset (0x0344)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	audio_mode 2'b00: PCM Audio Others: No PCM Audio stream
5:3	RW	0x0	pcm_mode 3'b000: 2 audio channels without pre-emphasis 3'b001: 2 audio channels with 50/15 pre-emphasis
2	RW	0x0	sw_cprgt 1'b0: Software for which copyright is asserted 1'b1: Software for which no copyright is asserted
1	RW	0x0	non_pcm 1'b0: Audio sample word represents linear PCM samples 1'b1: Audio sample word used for other purposes
0	RW	0x0	audio_i2s_ch_sta1 1'b0: Consumer applications 1'b1: Professional applications

EDPTX_AUDIO_I2S_CH_STA2

Address: Operational Base(0x27DC0000) + offset (0x0348)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	cat_code Category code (corresponding to channel status bits [15:8])

EDPTX_AUDIO_I2S_CH_STA3

Address: Operational Base(0x27DC0000) + offset (0x034C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ch_num Channel number (corresponding to channel status bits [23:20]). Only 2_channel is supported in BIST mode.
3:0	RW	0x0	source_num Source number (corresponding to channel status bits [19:16]). Only 2_channel is supported in BIST mode.

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EDPTX_AUDIO_I2S_CH_STA4

Address: Operational Base(0x27DC0000) + offset (0x0350)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	chnl_bit1 Corresponding to channels status bits [31:30].
5:4	RW	0x0	clk_accur Clock accuracy (corresponding to channels status bits [29:28]). These two bits define the sampling frequency tolerance. The bits are set in the transmitter.
3:0	RW	0x0	fs_freq Sampling clock frequency (corresponding to channel status bits [27:24]). 4'b0000: 44.1 KHz 4'b0010: 48 KHz 4'b0011: 32 KHz 4'b1000: 88.2 KHz 4'b1010: 96 KHz 4'b1110: 192 KHz Others: Reserved When set SPDIF_FS_OVRWR to "1", the four bits sample clock frequency in channel status is replaced by this register setting. Note that the audio sine wave frequency equals to Audio Sample Frequency/128. For example, if the sampling clock frequency is 44.1K, the sine wave frequency is 44,100/128 = 344.6Hz.

EDPTX_AUDIO_I2S_CH_STA5

Address: Operational Base(0x27DC0000) + offset (0x0354)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	chnl_bit2 Corresponding to channels status bits [39:36].
3:1	RW	0x0	word_length Audio word length (corresponding to channel status bits [35:33]). When WORD_MAX: 0, 3'b001: 16 bits 3'b010: 18 bits 3'b100: 19 bits 3'b101: 20 bits 3'b110: 17 bits When WORD_MAX: 1, 3'b001: 20 bits 3'b010: 22 bits 3'b100: 23 bits 3'b101: 24 bits 3'b110: 21 bits
0	RW	0x0	word_max Audio word length Max (corresponding to channel status bits 32). 1'b0: Maximal word length is 20 bits. 1'b1: Maximal word length is 24 bits.

EDPTX_LANE_MAP

Address: Operational Base(0x27DC0000) + offset (0x035C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:6	RW	0x1	lane3_map Control physical lane 3 will map to which logic lane: 2'b11: Logic lane 3 2'b10: Logic lane 2 2'b01: Logic lane 1 2'b00: Logic lane 0
5:4	RW	0x1	lane2_map Control physical lane 2 will map to which logic lane: 2'b11: Logic lane 3 2'b10: Logic lane 2 2'b01: Logic lane 1 2'b00: Logic lane 0
3:2	RW	0x1	lane1_map Control physical lane 1 will map to which logic lane: 2'b11: Logic lane 3 2'b10: Logic lane 2 2'b01: Logic lane 1 2'b00: Logic lane 0
1:0	RW	0x1	lane0_map Control physical lane 0 will map to which logic lane: 2'b11: Logic lane 3 2'b10: Logic lane 2 2'b01: Logic lane 1 2'b00: Logic lane 0

EDPTX_INT_STATE

Address: Operational Base(0x27DC0000) + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	int_state Interrupt request status 1'b1: Interrupt service is requested. 1'b0: No interrupt service is requested.

EDPTX_COMMON_INT_STA_1

Address: Operational Base(0x27DC0000) + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	vsync_det 1'b1: VSYNC active edge has been detected.
6	RW	0x0	pll_lock_chg 1'b1: PLL lock state is changed. Check PLL_LOCK of register DP_DEBUG_CTL for PLL lock status.
5	RW	0x0	spdif_err 1'b1: SPDIF parity errors Write 1 to clear. Software can change this interrupt generation by setting the register SPDIF_ERR_THRD. When SPDIF_ERR, software shall check SPDIF status on register SPDIF_AUDIO_STA_0.
4	RW	0x0	spdif_unstbl 1'b1: Not find expected preamble for SPDIF input.
3	RW	0x0	vid_format_chg 1'b1: Video input format change is detected.
2	RW	0x0	aud_clk_chg 1'b1: Audio input clock change is detected.

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Bit	Attr	Reset Value	Description
1	RW	0x0	vid_clk_chg 1'b1: Video input clock change is detected.
0	RW	0x0	sw_int 1'b1: Software-induced interrupt.

EDPTX_COMMON_INT_STA_2

Address: Operational Base(0x27DC0000) + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	enc_en_chg 1'b1: HDCP_ENC_EN changed detected. Write 1 to clear. ENC_EN_CHG happens whenever HDCP_ENC_EN is changed from 1 to 0 or form 0 to 1. This interrupt is generated when the internal HDCP cipher module find out that encryption status is changed. Software can check encryption status on bit ENCRYPT of register HDCP_STA.
5:4	RO	0x0	reserved
3	RW	0x0	hw_bksv_rdy 1'b1: BKSV is ready. Write 1 to clear. It is for H/W HDCP.
2	RW	0x0	hw_sha_done 1'b1: HDCP hardware computing V has ended. Write 1 to clear. During H/W HDCP authentication, it is generated after calculating V.
1	RW	0x0	hw_auth_state_chg 1'b1: H/W HDCP authentication state has changed. HW_AUTH_STATE_CHG happens after H/W HDCP is enabled. Software can check hardware authentication status on bit HW_AUTHEN_PASS of register HDCP_STA. This bit is set only when authentication success or failure status is changed. So, successive authentication failure does not set this bit.
0	RW	0x0	hw_auth_done 1'b1: H/W HDCP authentication has ended. This bit is set when H/W HDCP authentication is finished regardless of success or failure. Software can check hardware authentication status on bit HW_AUTHEN_PASS of register HDCP_STA.

EDPTX_COMMON_INT_STA_3

Address: Operational Base(0x27DC0000) + offset (0x03CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	afifo_under 1'b1: Audio FIFO is under run. Write 1 to clear.
6	RW	0x0	afifo_over 1'b1: Audio FIFO is overrun. Write 1 to clear.

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Bit	Attr	Reset Value	Description
5	RW	0x0	r0_chk_flag For hardware authentication (with HDCP repeater): 1'b1: R0 check is finished. For software authentication: 1'b1: R0 is ready for software check. Write 1 to clear. If H/W re-authentication is needed and this bit is set to 1, then this bit must be cleared before H/W re-authentication.
4	RW	0x0	dpcd_specific_irq 1'b1: Sink specific interrupt in DPCD is detected. Write 1 to clear
3	RW	0x0	mydp_plug_in 1'b1: MYDP plug out event is detected. Write 1 to clear
2	RW	0x0	mydp_plug_out 1'b1: MYDP plug out event is detected. Write 1 to clear
1	RW	0x0	mydp_hpd_irq 1'b1: MYDP HPD interrupt is detected. Write 1 to clear
0	RW	0x0	hdcp_link_check_fail 1'b1: HDCP link check failure is detected. Write 1 to clear.

EDPTX_COMMON_INT_STA_4

Address: Operational Base(0x27DC0000) + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	spdif_bi_phase_err 1'b1: SPDIF bi-phase error has occurred. Write 1 to clear. Software reset will not clear this interrupt.
4:3	RO	0x0	reserved
2	RW	0x0	hotplug_chg 1'b1: Hot plug change detected. Write 1 to clear. HOTPLUG_CHG happens whenever the pin I_DP_HDP changes and the change remains for at least hot plug deglitch time. And the hot plug deglitch time is defined in HPD_DEGLITCH_L and HPD_DEGLITCH_H. When HOTPLUG_CHG is high, software shall check the status of HPD signal on register HPD_STATUS.
1	RW	0x0	hpd_lost Hot plug detect signal lost timer larger than 2ms, that means cable is plugged out: 1'b1: Interrupt assert 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
0	RW	0x0	plug Hot plug detect signal lost time is larger than 2ms before cable plugged, it means cable is plugged in: 1'b1: Interrupt assert 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.

EDPTX_SPDIF_BIPHASE_INT_STA

Address: Operational Base(0x27DC0000) + offset (0x03D4)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	spdif_biphase_err_clr SPDIF biphase error
6:0	RO	0x00	reserved

EDPTX_DP_INT_STA

Address: Operational Base(0x27DC0000) + offset (0x03DC)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	int_hpd IRQ (HPD de-asserted less than 2ms) detect interrupt: 1'b1: IRQ interrupt assert 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
5	RW	0x0	hw_training_finish Training FSM module finish link training procedure: 1'b1: Hardware link training finished 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
4	RO	0x0	reserved
3	RW	0x0	sink_lost Sink lost interrupt 1'b1: Sink lost occurred 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
2	RW	0x0	link_lost Link lost interrupt 1'b1: Link lost occurred 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
1	RW	0x0	rply_receiv AUX channel command reply is received: 1'b1: Interrupt assert 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
0	RW	0x0	aux_err AUX channel access error interrupt: 1'b1: Interrupt assert 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.

EDPTX_COMMON_INT_MASK_1

Address: Operational Base(0x27DC0000) + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	common_int_mask_1 Each bit corresponds to the same bit in Common Interrupt Status Register 1. 1'b0: Mask interrupt 1'b1: Enable interrupt

EDPTX_COMMON_INT_MASK_2

Address: Operational Base(0x27DC0000) + offset (0x03E4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	common_int_mask_2 Each bit corresponds to the same bit in Common Interrupt Status Register 2. 1'b0: Mask interrupt 1'b1: Enable interrupt

EDPTX_COMMON_INT_MASK_3

Address: Operational Base(0x27DC0000) + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	common_int_mask_3 Each bit corresponds to the same bit in Common Interrupt Status Register 3. 1'b0: Mask interrupt 1'b1: Enable interrupt

EDPTX_COMMON_INT_MASK_4

Address: Operational Base(0x27DC0000) + offset (0x03EC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	common_int_mask_4 Each bit corresponds to the same bit in Common Interrupt Status Register 3. 1'b0: Mask interrupt 1'b1: Enable interrupt

EDPTX_DP_INT_STA_MASK

Address: Operational Base(0x27DC0000) + offset (0x03F8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	dp_int_sta_mask Each bit corresponds to the same bit in DisplayPort Interrupt Status Register (DP_INT_STA). 1'b1: Enable interrupt 1'b0: Mask interrupt

EDPTX_INT_CTL

Address: Operational Base(0x27DC0000) + offset (0x03FC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	serdes_overflow_clear 1'b1: Clear SerDes FIFO overflow flag
4	RW	0x0	serdes_underflow_clear 1'b1: Clear SerDes FIFO underflow flag
3	RO	0x0	reserved
2	RW	0x0	soft_int_ctrl Set Software Interrupt: 1'b1: Set interrupt 1'b0: Do not set interrupt
1	RO	0x0	reserved
0	RW	0x1	int_pol INT pin assertion polarity: 1'b1: Assert high 1'b0: Assert low

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EDPTX_SYS_CTL_1

Address: Operational Base(0x27DC0000) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:3	RW	0x0	hbr2_eye_sy_ctrl HBR2 pattern control
2	RW	0x0	det_sta Video stream clock detect status, It will not affect video output. 1'b1: Stream clock detected 1'b0: Stream clock not detected Write any value to update the current status.
1	RW	0x0	force_det Force video stream clock detect, this bit is only active when DET_CTRL is 1 1'b1: Force video stream clock detected 1'b0: Force video stream clock not detected This bit's type is R/W.
0	RW	0x0	det_ctrl Video stream clock detect status control: 1'b1: Use force detect status 1'b0: Use auto-detected status This bit's type is R/W.

EDPTX_SYS_CTL_2

Address: Operational Base(0x27DC0000) + offset (0x0604)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	cha_cri Pixel clock change detection threshold. The incoming pixel clock input is counted continuously by the 24Mhz reference clock. This register defines a number, if the counter number change is more than this value for 2 pixel clock edges, the CHA_STA bit is asserted. This bit's type is R/W.
3	RO	0x0	reserved
2	RW	0x0	cha_sta Video stream clock change status, It will not affect video output 1'b1: Clock frequency changed. 1'b0: Clock frequency not changed. Write any value to update the current status.
1	RW	0x0	force_cha Force stream clock change status, this bit only active when CHA_CTRL is 1. 1'b1: Force clock change. When asserted, CHA_STA is '1'. 1'b0: Force clock not change. This bit's type is R/W.
0	RW	0x0	cha_ctrl Pixel clock frequency change status control 1'b1: Use force change status 1'b0: Use auto-detected status This bit's type is R/W.

EDPTX_SYS_CTL_3

Address: Operational Base(0x27DC0000) + offset (0x0608)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6	RO	0x0	hpd_status Hot plug detect status. 1'b1: HPD is 1. 1'b0: HPD is 0. This bit's type is RO. When this bit is 0, AUX CH will not work. Note that the HPD_STATUS is only changed after the change of the pin I_DP_HPD remains for no less than hot plug deglitch time. And the hot plug deglitch time is defined in HPD_DEGLITCH_L and HPD_DEGLITCH_H.
5	RW	0x0	f_hpd Force hot plug detect. 1'b1: Force HPD 1. 1'b0: Force HPD 0. This bit's type is R/W.
4	RW	0x0	hpd_ctrl Hot plug detect manual control. 1'b1: Force HPD with F_HPD. 1'b0: Use PIN_HPD state. This bit's type is R/W.
3	RO	0x0	hdcp_rdy HDCP ready status. 1'b1: HDCP is ready. 1'b0: HDCP is not ready. This bit's type is RO. This bit is an indicator of whether HDCP is ready to perform. Usually, it is set as soon as HPD signal is detected as plugged.
2	RW	0x0	strm_valid Input stream have constant video format, and this stream is valid to send out through link. 1'b1: Input stream is valid. 1'b0: Input stream is not valid. Write any value to update the current status. Hardware will not send out video through link when this bit is 0.
1	RW	0x0	f_valid Force stream valid, this bit only active when VALID_CTRL is 1. 1'b1: Force input video stream valid. 1'b0: Force input video stream not valid. This bit's type is R/W.
0	RW	0x0	valid_ctrl Stream valid control. 1'b1: Use F_VALID bit to control video stream valid status 1'b0: Use video stream valid auto-detect This bit's type is R/W.

EDPTX_SYS_CTL_4

Address: Operational Base(0x27DC0000) + offset (0x060C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	fix_m_aud Fix M_AUD value 1'b1: Use register M_AUD value to be sent out. 1'b0: Use calculates M_AUD value to be sent out.

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Bit	Attr	Reset Value	Description
3	RW	0x0	enhanced DisplayPort Enhanced mode enable 1'b1: Enhanced mode 1'b0: Normal mode
2	RW	0x0	fix_m_vid Fix M_VID value 1'b1: Use register M_VID value to be sent out. 1'b0: Use calculates M_VID value to be sent out.
1:0	RW	0x0	m_vid_update_ctrl Control M_VID update frequency 2'b11: 1/8 X update rate 2'b10: 1/4 X update rate 2'b01: 1/2 X update rate 2'b00: Normal rate

EDPTX_DP_VID_CTL

Address: Operational Base(0x27DC0000) + offset (0x0610)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	bpc Bit per color/ component with video which transferred via DP main link 3'b011: 12 bits 3'b010: 10 bits 3'b001: 8 bits 3'b000: 6 bits Other: Reserved
4	RW	0x0	yc_coeff YCbCr Coefficients with video which transferred via DP main link 1'b1: ITU709 1'b0: ITU601
3	RW	0x0	d_range Dynamic range 1'b1: CEA range 1'b0: VESA range (from 0 to the maximum)
2:1	RW	0x0	color_f Colorimetric format with video which transferred via DP main link 2'b11: Reserved 2'b10: YcbCr444 2'b01: YcbCr422 2'b00: RGB
0	RO	0x0	reserved

EDPTX_PKT_SEND_CTL

Address: Operational Base(0x27DC0000) + offset (0x0640)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	audio_info_up Audio InfoFrame content has been updated. 1'b1: Updated 1'b0: Don't care Write 1 to this bit after Audio Packet Content Registers have been configured as Audio InfoFrame content has been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.

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Bit	Attr	Reset Value	Description
6	RW	0x0	avi_info_up AVI InfoFrame content has been updated. 1'b1: Updated 1'b0: Don't care Write 1 to this bit after AVI Packet Content Registers have been configured as AVI InfoFrame content has been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.
5	RW	0x0	mpeg_info_up MPEG InfoFrame content has been updated. 1'b1: Updated 1'b0: Don't care Write 1 to this bit after MPEG Packet Content Registers have been configured as MPEG InfoFrame content has been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.
4	RW	0x0	if_up Configurable InfoFrame content has been updated. 1'b1: Updated 1'b0: Don't care Write 1 to this bit after IF_TYPE and IF_PKT_DB1~25 Registers have been configured as configurable InfoFrame content have been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.
3	RW	0x0	audio_info_en Audio InfoFrame send enable. 1'b1: Send Audio InfoFrame 1'b0: Don't send Audio InfoFrame Make sure that the Audio Packet Content Registers had been configured correctly and the AUDIO_INFO_UP had been written with 1. This bit's type is R/W.
2	RW	0x0	avi_info_en AVI InfoFrame send enable. 1'b1: Send AVI InfoFrame 1'b0: Don't send AVI InfoFrame Make sure that the AVI Packet Content Registers had been configured correctly and the AVI_INFO_UP had been written with 1. This bit's type is R/W.
1	RW	0x0	mpeg_info_en MPEG InfoFrame send enable. 1'b1: Send MPEG InfoFrame 1'b0: Don't send MPEG InfoFrame Make sure that the MPEG Packet Content Registers had been configured correctly and the MPEG_INFO_UP had been written with 1. This bit's type is R/W.
0	RW	0x0	pkt_send_ctl Configurable InfoFrame send enable. 1'b1: Send InfoFrame defined in IF_TYPE and IF_PKT_DB1~25. 1'b0: Don't send InfoFrame. Make sure that the IF_TYPE and IF_PKT_DB1~25 Registers had been configured correctly and the IF_UP had been written with 1. This bit's type is R/W.

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EDPTX_DP_HDCP_CTL

Address: Operational Base(0x27DC0000) + offset (0x0648)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	hdcp_hpd_rst HDCP block reset control. 1'b0: No reset for HDCP block when HPD is low. 1'b1: Reset HDCP when HPD is low.
5:2	RO	0x0	reserved
1	RW	0x0	link_check_mode HDCP link integrity check mode: 1'b1: HDCP polling link integrity check status, and re-start HDCP Authentication automatically when detected link integrity check fail. 1'b0: HDCP don't polling link integrity check status.
0	RW	0x0	hw_hdcp_int The DP receiver initiates a HDCP interrupt through Hot Plug Detect Pin to DP transmitter whenever DP receiver finds R0' calculation done, downstream KSV list is ready and V' calculation done, or HDCP link integrity check failure. A firmware on DP transmitter must set this bit to 1 in order to make H/W HDCP authentication module do some proper action when firmware of DP transmitter find it out that the interrupt about HDCP. This bit is self cleared.

EDPTX_SPDIF_PHASE1_CTL_0

Address: Operational Base(0x27DC0000) + offset (0x0650)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	spdif_phase1_ctl_0 This register control SPDIF 1 cycle phase counter value [7:0], if bit SPDIF_PHASE1_CTL_EN is 0, the 1 cycle phase counter value [7:0] is read out. If the register SPDIF_PHASE1_CTL_EN is 1, firmware can force this value by writing data to this register. The bits can be read only when SPDIF_STREAM_DET is one. SPDIF_PHASE1_CTL should be set as Fls_clk / (32*Faudio_frequency * AudioChannelNum * 2). Here 2 are for biphase encoding and 32 is for each sub frame. For example if audio_frequency is 44.1KHz, Audio Channel Number is 2 and ls_clk frequency is 135M Hz. 135,000,000/ (32*44,100*2*2) = 23.9. SPDIF_PHASE1_CTL should set to 24.

EDPTX_SPDIF_PHASE1_CTL_1

Address: Operational Base(0x27DC0000) + offset (0x0654)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	spdif_phase1_ctl_en This register enables force of the 1 cycle phase counter value function. 1'b0: SPDIF 1 cycle phase counter value use chip counted value. 1'b1: SPDIF 1 cycle phase counter value use the data written to register SPDIF_PHASE1_CTL_0 and SPDIF_PHASE1_CTL_1.
6:1	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	spdif_phase1_ctl_1 This register control SPDIF 1 cycle phase counter value [8], if bit PHASE_1_CONTROL_EN is 0, the 1 cycle phase counter value [8] is read out. If the register SPDIF_PHASE1_CTL_EN is 1, firmware can force this value by writing data to this register.

EDPTX_SPDIF_PHASE2_CTL_0

Address: Operational Base(0x27DC0000) + offset (0x0658)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	spdif_phase2_ctl_0 This register control SPDIF 2 cycle phase counter value [7:0], if bit SPDIF_PHASE2_CTL_EN is 0, the 2 cycle phase counter value [7:0] is read out. If the register SPDIF_PHASE2_CTL_EN is 1, firmware can force this value by writing data to this register. The bits can be read only when SPDIF_STREAM_DET is one. SPDIF_PHASE2_CTL should be set as 2*Fls_clk / (32*Faudio_frequency * AudioChannelNum * 2). Here 2 are for biphase encoding and 32 is for each sub frame. For example if audio_frequency is 44.1KHz, Audio Channel Number is 2 and ls_clk frequency is 135M Hz. 2*135,000,000/ (32*44,100*2*2) = 47.8. SPDIF_PHASE2_CTL should set to 48.

EDPTX_SPDIF_PHASE2_CTL_1

Address: Operational Base(0x27DC0000) + offset (0x065C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	spdif_phase2_ctl_en This register enables force of the 2 cycle phase counter value function. 1'b0: SPDIF 2 cycle phase counter value use chip counted value. 1'b1: SPDIF 2 cycle phase counter value use the data written to register SPDIF_PHASE2_CTL_0 and SPDIF_PHASE2_CTL_1.
6:1	RO	0x00	reserved
0	RW	0x0	spdif_phase2_ctl_1 This register control SPDIF 2 cycle phase counter value [8], if bit SPDIF_PHASE2_CTL_EN is 0, the 2 cycle phase counter value [8] is read out. If the register SPDIF_PHASE2_CTL_EN is 1, firmware can force this value by writing data to this register.

EDPTX_SPDIF_PHASE3_CTL_0

Address: Operational Base(0x27DC0000) + offset (0x0660)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	spdif_phase3_ctl_0 This register control SPDIF 3 cycle phase counter value [7:0], if bit SPDIF_PHASE3_CTL_EN is 0, the 3 cycle phase counter value [7:0] is read out. If the register SPDIF_PHASE3_CTL_EN is 1, firmware can force this value by writing data to this register. The bits can be read only when SPDIF_STREAM_DET is one. SPDIF_PHASE3_CTL should be set as 3*Fls_clk / (32*Faudio_frequency * AudioChannelNum * 2). Here 2 are for biphase encoding and 32 is for each sub frame. For example if audio_frequency is 44.1KHz, Audio Channel Number is 2 and ls_clk frequency is 135M Hz. 3*135,000,000/ (32*44,100*2*2) = 71.7. SPDIF_PHASE3_CTL should set to 72.

EDPTX_SPDIF_PHASE3_CTL_1

Address: Operational Base(0x27DC0000) + offset (0x0664)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	spdif_phase3_ctl_en This register enables force of the 3 cycle phase counter value function. 1'b0: SPDIF 3 cycle phase counter value use chip counted value. 1'b1: SPDIF 3 cycle phase counter value use the data written to register SPDIF_PHASE3_CTL_0 and SPDIF_PHASE3_CTL_1.
6:1	RO	0x00	reserved
0	RW	0x0	spdif_phase3_ctl_1 This register control SPDIF 3 cycle phase counter value [8], if bit SPDIF_PHASE3_CTL_EN is 0, the 3 cycle phase counter value [8] is read out. If the register SPDIF_PHASE3_CTL_EN is 1, firmware can force this value by writing data to this register.

EDPTX_LINK_BW_SET

Address: Operational Base(0x27DC0000) + offset (0x0680)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0xa	link_bw_set Main link bandwidth setting: 4'b0110: 1.62Gpbs per lane 4'b1010: 2.7Gpbs per lane Other: Reserved

EDPTX_LANE_COUNT_SET

Address: Operational Base(0x27DC0000) + offset (0x0684)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	lane_count_set Main link lane count 3'b001: one lane 3'b010: two lanes 3'b100: four lanes Other: Reserved

EDPTX_DP_TRAINING_PTN_SET

Address: Operational Base(0x27DC0000) + offset (0x0688)

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Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	scrambling_disable Disable scramble 1'b1: Disable 1'b0: Normal operation
4:2	RW	0x0	link_qual_pattern_set Link quality pattern setting. 3'b101: HBR2 Compliance 3'b100: 80 bit test pattern 3'b011: PRBS 7 bit 3'b010: symbol error rate measurement pattern is sent 3'b001: D10.2 test pattern is sent 3'b000: link quality test pattern not sent
1:0	RW	0x0	sw_training_pattern_set Link training pattern setting. SW_TRAINING_PATTERN_SET has higher priority than LINK_QUAL_PATTER_SET. 2'b11: Reserved 2'b10: Sending training pattern 2 2'b01: Sending training pattern 1 2'b00: Training pattern not sent

EDPTX_DP_LN0_LINK_TRAINING_CTL

Address: Operational Base(0x27DC0000) + offset (0x068C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	max_pre_reach_0 This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached.
4:3	RW	0x0	pre_emphasis_set_0 Lane 0 pre-emphasis level setting 2'b11: 9.5 dB 2'b10: 6.0 dB 2'b01: 3.5 dB 2'b00: 0 dB (No pre-emphasis) This bit's type is R/W.
2	RW	0x0	max_drive_reach_0 This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For test purpose only. This bit's type is RO. For more information, refer to MAX_PRE_REACH_0.
1:0	RW	0x0	drive_current_set_0 Lane 0 output amplitude setting 2'b11: 1200 mV 2'b10: 800 mV 2'b01: 600 mV 2'b00: 400 mV This bit's type is R/W.

EDPTX_DP_LN1_LINK_TRAINING_CTL

Address: Operational Base(0x27DC0000) + offset (0x0690)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	max_pre_reach_1 This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached.

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Bit	Attr	Reset Value	Description
4:3	RW	0x0	pre_emphasis_set_1 Lane 1 pre-emphasis level setting 2'b11: 9.5 dB 2'b10: 6.0 dB 2'b01: 3.5 dB 2'b00: 0 dB (No pre-emphasis) This bit's type is R/W.
2	RW	0x0	max_drive_reach_1 This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For more information, refer to MAX_PRE_REACH_1. For test purpose only. This bit's type is RO.
1:0	RW	0x0	drive_current_set_1 Lane 1 output amplitude setting 2'b11: 1200 mV 2'b10: 800 mV 2'b01: 600 mV 2'b00: 400 mV This bit's type is R/W.

EDPTX_DP_LN2_LINK_TRAINING_CTL

Address: Operational Base(0x27DC0000) + offset (0x0694)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	max_pre_reach_2 This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached.
4:3	RW	0x0	pre_emphasis_set_2 Lane 2 pre-emphasis level setting 2'b11: 9.5 dB 2'b10: 6.0 dB 2'b01: 3.5 dB 2'b00: 0 dB (No pre-emphasis) This bit's type is R/W.
2	RW	0x0	max_drive_reach_2 This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For more information, refer to MAX_PRE_REACH_2. For test purpose only. This bit's type is RO.
1:0	RW	0x0	drive_current_set_2 Lane 2 output amplitude setting 2'b11: 1200 mV 2'b10: 800 mV 2'b01: 600 mV 2'b00: 400 mV This bit's type is R/W.

EDPTX_DP_LN3_LINK_TRAINING_CTL

Address: Operational Base(0x27DC0000) + offset (0x0698)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	max_pre_reach_3 This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached.

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Bit	Attr	Reset Value	Description
4:3	RW	0x0	pre_emphasis_set_3 Lane 3 pre-emphasis level setting 2'b11: 9.5 dB 2'b10: 6.0 dB 2'b01: 3.5 dB 2'b00: 0 dB (No pre-emphasis) This bit's type is R/W.
2	RO	0x0	max_drive_reach_3 This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For more information, refer to MAX_PRE_REACH_3. For test purpose only. This bit's type is RO.
1:0	RW	0x0	drive_current_set_3 Lane 3 output amplitude setting 2'b11: 1200 mV 2'b10: 800 mV 2'b01: 600 mV 2'b00: 400 mV This bit's type is R/W.

EDPTX_DP_HW_LINK_TRAINING_CTL

Address: Operational Base(0x27DC0000) + offset (0x06A0)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	hw_training_error_code Training error code 3'b000: OK 3'b001: AUX_WRITE_ERROR 3'b010: MAX_DRIVE_REACHED 3'b011: WRONG_LANE_COUNT_SETTING 3'b100: LOOP_SAME_5_TIME 3'b101: CR_FAIL_IN_EQ 3'b110: EQ_LOOP_5_TIME
3:1	RO	0x0	reserved
0	RW	0x0	hw_training_en Link training sequence enable Write 1 to enable training sequence, write 0 to force training sequence stop, this bit will self-clear when training done.

EDPTX_HPD_DEGLITCH_L

Address: Operational Base(0x27DC0000) + offset (0x06C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x5e	hpd_deglitch_l HPD_DEGLITCH, which is counted at 24 MHz, is used to de-glitch the HPD signal This register is HPD_DEGLITCH [7:0]. The default value is 0x5E for 280.75 us deglitch time.

EDPTX_HPD_DEGLITCH_H

Address: Operational Base(0x27DC0000) + offset (0x06C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1a	hpd_deglitch_h HPD_DEGLITCH, which is counted at 24 MHz, is used to de-glitch the HPD signal. This register is HPD_DEGLITCH [13:8]. The default value is 0x1A for 280.75 us deglitch time.

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EDPTX_POLLING_PERIOD

Address: Operational Base(0x27DC0000) + offset (0x06CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x0e	polling_period This register controls the interval between each time of polling operation. Interval time = POLLING_PERIOD * 2^16 * Period of 24M clock.

EDPTX_DP_LINK_DEBUG_CTL

Address: Operational Base(0x27DC0000) + offset (0x06E0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	new_prbs7 Control the PRBS 7 formula. 1'b1: Use new PRBS7 formula in DP 1.1 version 1'b0: Use old PRBS7 formula in DP 1.0 version
3	RW	0x0	dis_fifo_rst Disable video FIFO reset every line 1'b1: Disable 1'b0: Reset video FIFO every line
2	RW	0x0	disable_auto_reset_encoder Disable 8b/10 encoder auto reset 1'b1: Disabled auto reset 8b/10 encode before sending Link Training Pattern 2 1'b0: Auto reset 8b/10 encode before sending Link Training Pattern 2
1	RO	0x0	reserved
0	RW	0x0	prbs31_en Enable DisplayPort PRBS 31. 1'b1: Enabled 1'b0: Normal mode

EDPTX_DP_SINK_COUNT

Address: Operational Base(0x27DC0000) + offset (0x06E4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dp_sink_count Sink Count

EDPTX_DP_IRD_VECTOR

Address: Operational Base(0x27DC0000) + offset (0x06E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dp_ird_vector Irq_vector

EDPTX_DP_LINK_STATUS0

Address: Operational Base(0x27DC0000) + offset (0x06EC)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln1_sybol_lock Lane1 symbol lock
5	RW	0x0	ln1_eq_done Lane1 EQ done

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Bit	Attr	Reset Value	Description
4	RW	0x0	ln1_cr_done Lane1 CR done
3	RO	0x0	reserved
2	RW	0x0	ln0_sybol_lock Lane0 symbol lock
1	RW	0x0	ln0_eq_done Lane0 EQ done
0	RW	0x0	ln0_cr_done Lane0 CR done

EDPTX_DP_LINK_STATUS1

Address: Operational Base(0x27DC0000) + offset (0x06F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	inter_ln_align Interlace align
6	RW	0x0	ln3_sybol_lock Lane3 symbol lock
5	RW	0x0	ln3_eq_done Lane3 EQ done
4	RW	0x0	ln3_cr_done Lane3 CR done
3	RO	0x0	reserved
2	RW	0x0	ln2_sybol_lock Lane2 symbol lock
1	RW	0x0	ln2_eq_done Lane2 EQ done
0	RW	0x0	ln2_cr_done Lane2 CR done

EDPTX_DP_ALIGN_STATUS

Address: Operational Base(0x27DC0000) + offset (0x06F4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dp_align_status ALIGN_STATUS

EDPTX_M_VID_0

Address: Operational Base(0x27DC0000) + offset (0x0700)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	m_vid_0 M_VID [7:0]. If FIX_M_VID is 1, this M_VID is used. Otherwise the M_VID value which chip calculated is used.

EDPTX_M_VID_1

Address: Operational Base(0x27DC0000) + offset (0x0704)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	m_vid_1 M_VID [15:8]. If FIX_M_VID is 1, this M_VID is used. Otherwise the M_VID value which chip calculated is used.

EDPTX_M_VID_2

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Address: Operational Base(0x27DC0000) + offset (0x0708)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	m_vid_2 M_VID [23:16]. If FIX_M_VID is 1, this M_VID is used. Otherwise the M_VID value which chip calculated is used.

EDPTX_N_VID_0

Address: Operational Base(0x27DC0000) + offset (0x070C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_vid_0 N_VID[7:0] The maximum value of M_VID is 0xFFFF in ASYNC mode.

EDPTX_N_VID_1

Address: Operational Base(0x27DC0000) + offset (0x0710)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_vid_1 N_VID[15:8]

EDPTX_N_VID_2

Address: Operational Base(0x27DC0000) + offset (0x0714)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_vid_2 N_VID[23:16]

EDPTX_M_VID_MON

Address: Operational Base(0x27DC0000) + offset (0x0718)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	m_vid_mon This register shows M_VID value which is actually transmitted to Rx for monitoring purpose.

EDPTX_DP_VIDEO_FIFO_THRD

Address: Operational Base(0x27DC0000) + offset (0x0730)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	video_th_ctrl Video Data FIFO threshold control enables. 1'b1: Video Data FIFO threshold uses VIDEO_TH_VALUE. 1'b0: Video Data FIFO threshold uses internal calculate value automatically.
3:0	RW	0x0	video_th_value Video Data FIFO threshold value. If VIDEO_TH_CTRL is 1, and data count in video data FIFO have reached FIFO threshold value, video data is read out from FIFO.

EDPTX_DP_GNS_CTRL

Address: Operational Base(0x27DC0000) + offset (0x0734)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	eq_training_loop_control 1'b1: Enable 1'b0: Disable
5	RO	0x0	reserved
4	RW	0x0	scramble_ctrl Scramble formula control: 1'b1: New formula 1'b0: Old formula
3	RW	0x0	in_ex Control scrambler structure: 1'b1: Internal type 1'b0: External type
2	RW	0x0	disable_serdes_fifo_rset 1'b1: Disable serdes FIFO auto reset. 1'b0: Enable serdes FIFO auto reset.
1	RW	0x0	video_map_ctrl Control use or not the video data map in YCbCr 4:2:2 mode: 1'b1: Use video data map in YCbCr 4:2:2 mode 1'b0: Don't use
0	RW	0x0	rs_ctrl Control RS parameter: 1'b1: Parameter define by V1.0 1'b0: Parameter in GNS

EDPTX_DP_AUDIO_MARGIN

Address: Operational Base(0x27DC0000) + offset (0x073C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	force_audio_margin Force audio margin 1'b1: Audio margin use register value AUDIO_MARGIN. 1'b0: Audio margin use hardware calculation. It is the default setting.
6:0	RW	0x00	audio_margin Audio packet is sent out during vertical blank or horizontal blank. This register is used to specify minimum stream clock cycles to transfer audio stream packet. If current remaining stream clock cycles before sending active video data is less than the value, DP postpone sending audio stream packets to the next video blank interval. AUDIO_MARGIN only takes effect when FORCE_AUDIO_MARGIN is set 1.

EDPTX_M_AUD_MON

Address: Operational Base(0x27DC0000) + offset (0x0740)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	m_aud_mon This register shows M_AUD value which is actually transmitted to Rx for monitoring purpose.

EDPTX_M_AUD_0

Address: Operational Base(0x27DC0000) + offset (0x0748)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	m_aud_0 M_AUD [7:0]. If FIX_M_AUD is 1, this M_AUD is used. Otherwise the calculated M_AUD value is used.

EDPTX_M_AUD_1

Address: Operational Base(0x27DC0000) + offset (0x074C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	m_aud_1 M_AUD [15:8]. If FIX_M_AUD is 1, this M_AUD is used. Otherwise the calculated M_AUD value is used.

EDPTX_M_AUD_2

Address: Operational Base(0x27DC0000) + offset (0x0750)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	m_aud_2 M_AUD [23:16]. If FIX_M_AUD is 1, this M_AUD is used. Otherwise the calculated M_AUD value is used.

EDPTX_N_AUD_0

Address: Operational Base(0x27DC0000) + offset (0x0754)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_aud_0 N_AUD[7:0]

EDPTX_N_AUD_1

Address: Operational Base(0x27DC0000) + offset (0x0758)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_aud_1 N_AUD[15:8]

EDPTX_N_AUD_2

Address: Operational Base(0x27DC0000) + offset (0x075C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_aud_2 N_AUD[23:16]

EDPTX_DP_M_CAL_CTL

Address: Operational Base(0x27DC0000) + offset (0x0760)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	m_aud_gen_filter_en Enable M_AUD value generation filter to reduce the variation of M_AUD value. This filter is a low-pass filter to smooth out the M_AUD variation 1'b1: Enable the filter 1'b0: Disable the filter

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Bit	Attr	Reset Value	Description
2	RW	0x0	m_vid_gen_filter_en Enable M_VID value generation filter to reduce the variation of M_VID value. This filter is a low-pass filter to smooth out the M_VID variation 1'b1: Enable the filter 1'b0: Disable the filter
1	RO	0x0	reserved
0	RW	0x0	m_gen_clk_sel Select which link clock is used to generate the M value 1'b1: Clock with down spreading is used 1'b0: Clock without down spreading is used

EDPTX_M_VID_GEN_FILTER_TH

Address: Operational Base(0x27DC0000) + offset (0x0764)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x04	m_vid_gen_filter_th The threshold of M_VID generation filter. It only takes effect when M_VID_GEN_FILTER_EN is set to 1

EDPTX_M_AUD_GEN_FILTER_TH

Address: Operational Base(0x27DC0000) + offset (0x0778)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x02	m_aud_gen_filter_th The threshold of M_AUD generation filter. It only takes effect when M_AUD_GEN_FILTER_EN is set to 1

EDPTX_AUX_CH_STA

Address: Operational Base(0x27DC0000) + offset (0x0780)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	aux_busy AUX channel status bit. If this bit is read as 1, AUX channel access should be halted. 1'b1: AUX CH is busy 1'b0: AUX CH is idle
3:0	RW	0x0	aux_status This register indicate the AUX channel access status 4'b0000: OK 4'b0001: NACK_ERROR 4'b0010: TIMEOUT_ERROR 4'b0011: UNKNOWN_ERROR 4'b0100: MUCH_DEFER_ERROR 4'b0101: TX_SHORT_ERROR 4'b0110: RX_SHORT_ERROR 4'b0111: NACK_WITHOUT_M_ERROR 4'b1000: I2C_NACK_ERROR Other: Reserved

EDPTX_AUX_ERR_NUM

Address: Operational Base(0x27DC0000) + offset (0x0784)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	aux_err_num The error number counter of AUX channel counts when AUX channel access failed. In AUX CH reading, this number indicates the number of read back byte. In AUX CH writing, this number indicates the number of reply command.

EDPTX_AUX_CH_DEFER_CTL

Address: Operational Base(0x27DC0000) + offset (0x0788)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	defer_ctrl_en AUX CH received DEFER command count control enable 1'b1: If the count that AUX CH receive DEFER command equal to (DEFER_COUNT * 64), the AUX CH transaction is terminated, and the AUX_STATUS is 0100 1'b0: The count that AUX CH receive DEFER command is unlimited
6:0	RW	0x7f	defer_count The count is defined to limit the max count AUX CH receive DEFER command. When DEFER_CTRL_EN is 1 and AUX CH received (DEFER_COUNT * 64) DEFER command, the AUX CH will terminate the transaction

EDPTX_AUX_RX_COMM

Address: Operational Base(0x27DC0000) + offset (0x078C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	aux_rx_comm AUX CH received command

EDPTX_BUFFER_DATA_CTL

Address: Operational Base(0x27DC0000) + offset (0x0790)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	buf_clr Write 1 to this bit to clear AUX CH data buffer (BUF_DATA_0 ~ BUF_DATA_15). Always read back 0 from this bit. This bit's type is R/W. This bit is self cleared. Note: For the write operation, set this bit to 1 before writing data to BUF_DATA_0~15. And for READ operation, this bit has only to be set before starting data transfer by setting AUX_EN.
6:5	RO	0x0	reserved
4	RW	0x0	buf_have_data 1'b0: Buffer have data 1'b1: Buffer have not data
3:0	RW	0x0	buffer_data_count The counts of data AUX CH buffer have.

EDPTX_AUX_CH_CTL_1

Address: Operational Base(0x27DC0000) + offset (0x0794)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	aux_length Register control AUX CH transaction length.
3:0	RW	0x0	aux_tx_comm Register control AUX CH transaction command.

EDPTX_AUX_ADDR_7_0

Address: Operational Base(0x27DC0000) + offset (0x0798)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	aux_addr_7_0 AUX_ADDR[7:0], Register control AUX CH address.

EDPTX_AUX_ADDR_15_8

Address: Operational Base(0x27DC0000) + offset (0x079C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	aux_addr_15_8 AUX_ADDR[15:8], Register control AUX CH address

EDPTX_AUX_ADDR_19_16

Address: Operational Base(0x27DC0000) + offset (0x07A0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	aux_addr_19_16 AUX_ADDR[7:0], Register control AUX CH address.

EDPTX_AUX_CH_CTL_2

Address: Operational Base(0x27DC0000) + offset (0x07A4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	pd_aux_idle Power down AUX CH when AUX CH is in idle state. 1'b1: Power down AUX CH in idle state. 1'b0: Keep AUX CH power up in idle state.
2	RW	0x0	aux_pn_inv Invert AUX CH PN 1'b1: Invert PN 1'b0: Normal mode
1	RW	0x0	addr_only AUX CH issue "address only" command 1'b1: Issue "address only" command 1'b0: Normal AUX CH command
0	RW	0x0	aux_en Register control AUX CH operation enable Write 1 to this bit to enable AUX CH operation This bit will self-clear when AUX CH operation is finished. This bit is self cleared.

EDPTX_BUF_DATA

Address: Operational Base(0x27DC0000) + offset (0x07C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xff	buf_data AUX CH buffer data 0 ~ 15

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EDPTX_SOC_GENERAL_CTL

Address: Operational Base(0x27DC0000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	audio_bit_mapping_type Audio bit mapping type in 16bit audio mode 2'b00: Type 0 2'b01: Type 1 2'b10: Type 2 2'b11: Reserved
15	RO	0x0	reserved
14:13	RW	0x0	pcm_size PCM data bit size 2'b00: 16 bit 2'b01: 20 bit 2'b10: 24 bit 2'b11: Reserved
12:5	RO	0x00	reserved
4:0	RW	0x00	audio_ch_status_same Select the channel status bits for audio channel 3~8. 1'b1: Use the same data channel status bits from AUDIO_GP0_STATUS_n registers. 1'b0: Use each channel status bits from the corresponding AUDIO_GPx_STATUS_n registers.

EDPTX_DP_TEST_80B_PATTERN0

Address: Operational Base(0x27DC0000) + offset (0x081C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dp_test_80b_pattern0 DP test 80bit pattern0[29:0]

EDPTX_DP_TEST_80B_PATTERN1

Address: Operational Base(0x27DC0000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dp_test_80b_pattern1 DP test 80bit pattern0[59:30]

EDPTX_DP_TEST_80B_PATTERN2

Address: Operational Base(0x27DC0000) + offset (0x0824)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	dp_test_80b_pattern2 DP test 80bit pattern0[79:60]

EDPTX_AUD_CTL

Address: Operational Base(0x27DC0000) + offset (0x0834)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	aud_channel_count Audio Channel Number 3'b001: 2 channel 3'b011: 4 channel 3'b101: 6 channel 3'b111: 8 channel

EDPTX_CRC_CON

Address: Operational Base(0x27DC0000) + offset (0x0890)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	vid_crc_flush Video CRC flush enable. The video CRC value is initialized at every v-sync.
1	RO	0x0	reserved
0	RW	0x0	vid_crc_enable Video CRC enable. 1'b0: Disable 1'b1: Enable

EDPTX_CRC_RESULT

Address: Operational Base(0x27DC0000) + offset (0x0894)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	aud_crc_result Audio CRC result
15:0	RW	0x0000	vid_crc_result Video CRC result

EDPTX_I2S_CTRL

Address: Operational Base(0x27DC0000) + offset (0x09C8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	i2s_en I2S enable
3:0	RW	0x0	i2s_fmt_ctrl I2S Format Control

EDPTX_I2S_CH_SWAP

Address: Operational Base(0x27DC0000) + offset (0x09CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	i2s_ch_swap I2S channel swap
3:0	RW	0xb	i2s_wd_len I2S word length

EDPTX_I2S_CH_CTRL

Address: Operational Base(0x27DC0000) + offset (0x09D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xe4	i2s_ch_ctrl I2S channel control

EDPTX_I2S_CH_CTRL1

Address: Operational Base(0x27DC0000) + offset (0x09D4)

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Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	i2s_aud_layout Audio layout
1	RW	0x0	i2s_aud_v_bit Audio v_bit
0	RW	0x0	i2s_aut_ext_sta Audio ext channel status

EDPTX_LINK_POLICY

Address: Operational Base(0x27DC0000) + offset (0x09D8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	alternate_sr_en Alternate SR enable
6:4	RW	0x5	link_train_cr_lp_in Link training CR loop in
3	RW	0x0	link_train_wr_en Training first write en
2	RO	0x0	reserved
1	RW	0x0	link_train_inv Invert training bit enable
0	RW	0x0	frame_change_en Framing change enable

23.5 Interface Description

Table 23-1 EDP TX Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
edptx_ln0_txdp	O	HDMI_TX_D0P/EDP_TX_D0P	NS
edptx_ln0_txdn	O	HDMI_TX_D0N/EDP_TX_D0N	NS
edptx_ln1_txdp	O	HDMI_TX_D1P/EDP_TX_D1P	NS
edptx_ln1_txdn	O	HDMI_TX_D1N/EDP_TX_D1N	NS
edptx_ln2_txdp	O	HDMI_TX_D2P/EDP_TX_D2P	NS
edptx_ln2_txdn	O	HDMI_TX_D2N/EDP_TX_D2N	NS
edptx_ln3_txdp	O	HDMI_TX_D3P/EDP_TX_D3P	NS
edptx_ln3_txdn	O	HDMI_TX_D3N/EDP_TX_D3N	NS
edptx_sbdp	I/O	HDMI_TX_SBDP/EDP_TX_AUXP	NS
edptx_sbdn	I/O	HDMI_TX_SBDN/EDP_TX_AUXN	NS
edptx_hpd_m0	I	DSM_AUD_LN_M1/HDMI_TX_HPDIN_M0/PCIE1_CLKREQN_M3/I2C7_SDA_M3/EDP_TX_HPDIN_M0/UART11_RX_M2/PWM0_CH1_M1/GPIO4_C1_d	VCCIO6_IOC_GPIO4A_IOMUX_SEL_L[7:4]=4'hC
edptx_hpd_m1	I	SDMMC0_PWREN/SDMMC1_DETN_M2/HDMI_TX_HPDIN_M1/EDP_TX_HPDIN_M1/PWM1_CH2_M0/GPIO0_B6_d	PMU1_IOC_GPIO3D_IOMUX_SEL_H[11:8]=4'hA

Notes: I=input, O=output, I/O=input/output, bidirectional, NS=Not Set

23.6 Application Notes

23.6.1 EDP TX Clock Domain Overview

The eDP TX clock domain can be seen in the figure below. The clock frequency of

"o_tx_link_sym_clk" and "o_tx_hs_clk" should be set according to PHY registers. From the figure, can get this frequency relation,
o_tx_link_sym_clk = I_CH_TXD_CLK = I_CLK_DIV2 = i_tx_data_clk
o_tx_hs_clk = I_LINK_CLK
o_tx_hs_clk = 2 * o_tx_link_sym_clk
The clock o_tx_hs_clk has twice the frequency of o_tx_link_sym_clk. For example, link rate is 2.7Gbps, o_tx_hs_clk should be 270M and o_tx_link_sym_clk should be 135M.

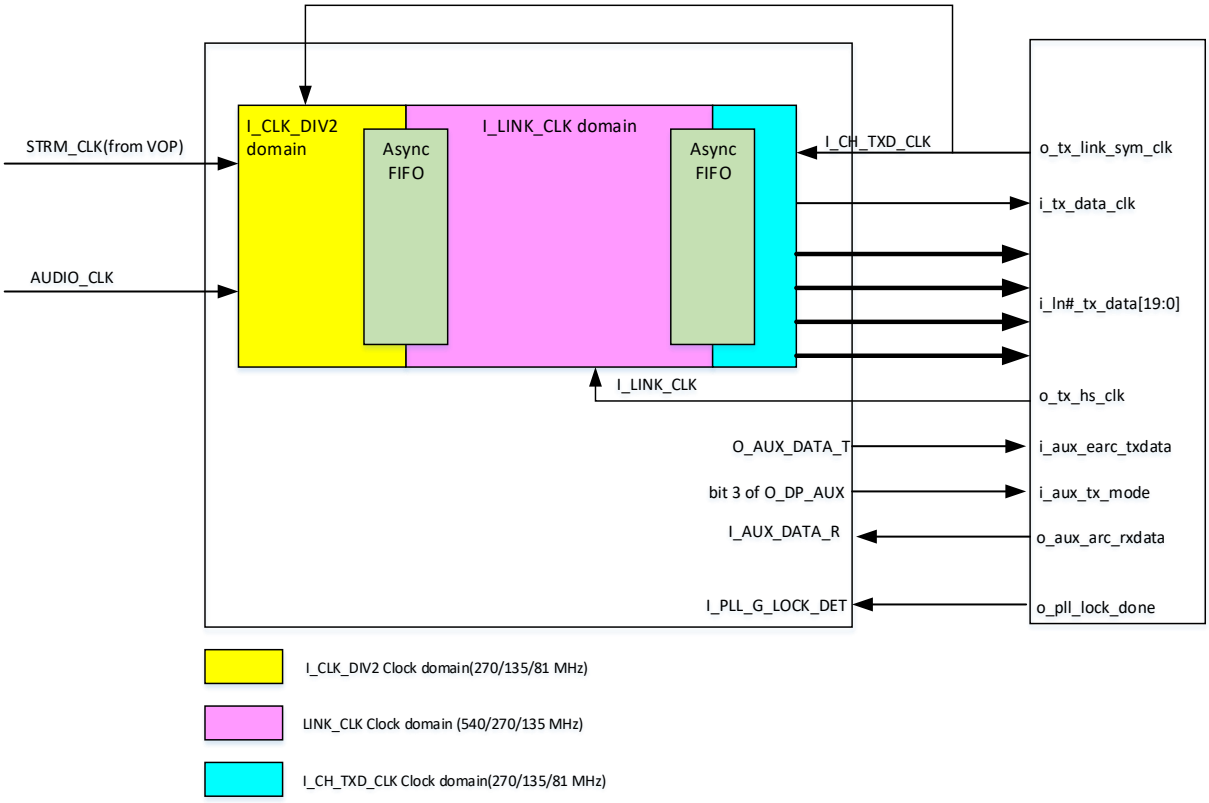


Fig. 23-4 DP Clock Domain

23.6.2 EDP TX Controller Programming Guide

After PHY is ready, the eDP TX controller can begin to work.

23.6.2.1 How to Initialize DP

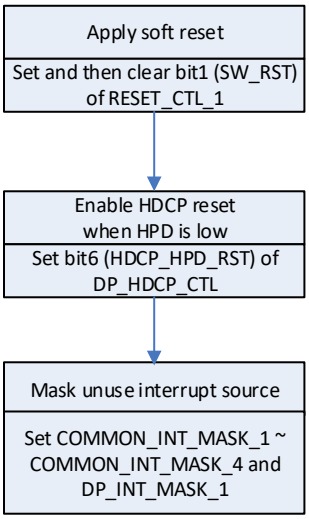


Fig. 23-5 DP controller Initial

23.6.2.2 How to Detect Hot Plug Insertion

In Wait Hot Plug state, chip is in power down status. System only responses to hot plug change interrupt. When a hot plug interrupt is detected, in the interrupt routine, firmware

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will judge whether it is a receiver plug-in or un-plug or link training request. If plug-in, chip will be powered on and system state will be set to Read and Parse EDID.

23.6.2.3 How to Access DPCD Space in DP Rx

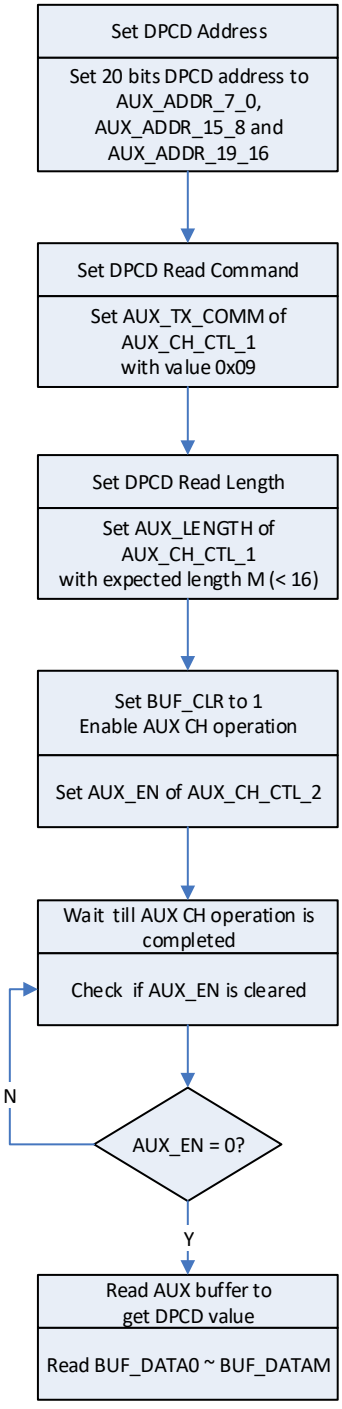


Fig. 23-6 DP DPCD Read

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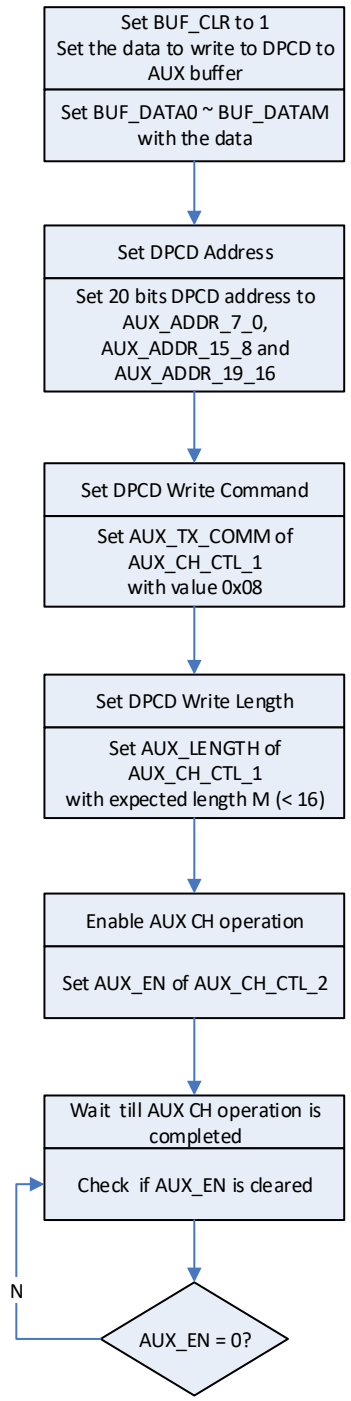


Fig. 23-7 DP DPCD Write

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23.6.2.4 How to Write into EDID space in DP Rx

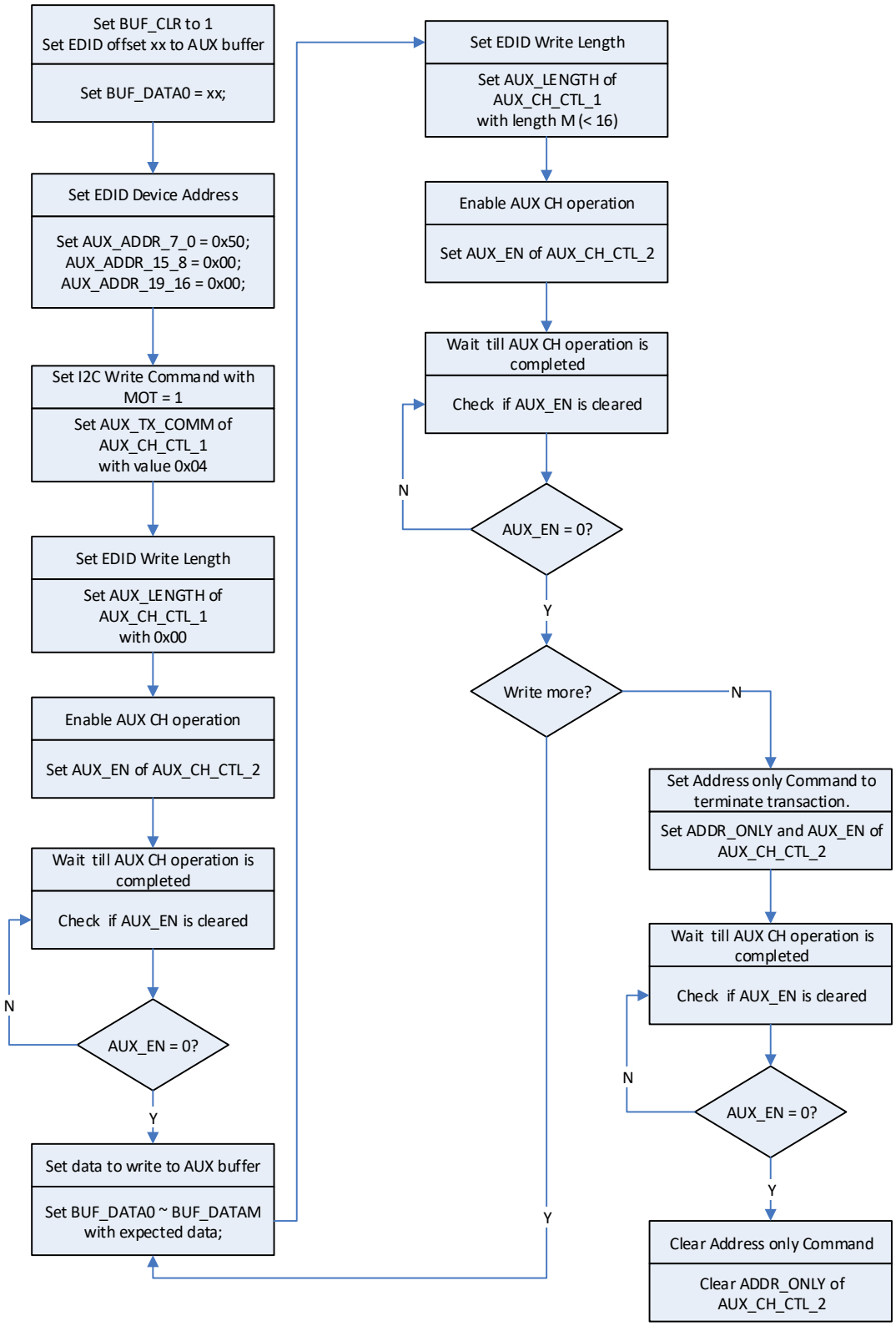


Fig. 23-8 Write into EDID space in DP Rx

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23.6.2.5 How to READ From EDID Space in DP Rx

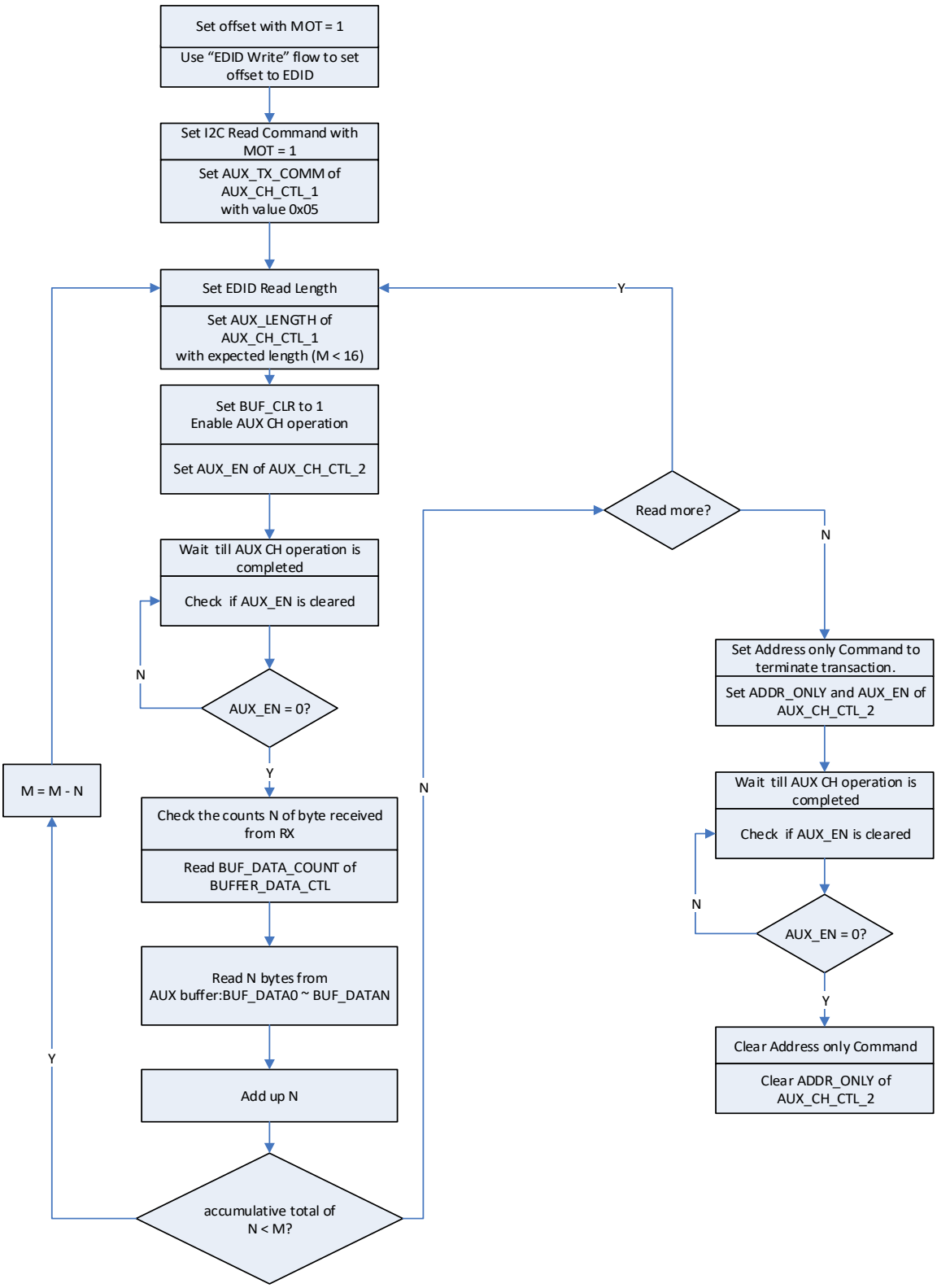


Fig. 23-9 Read from EDID space in DP Rx

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23.6.2.6 How to do SW Link Training

23.6.2.6.1 State Machine of SW Link Training

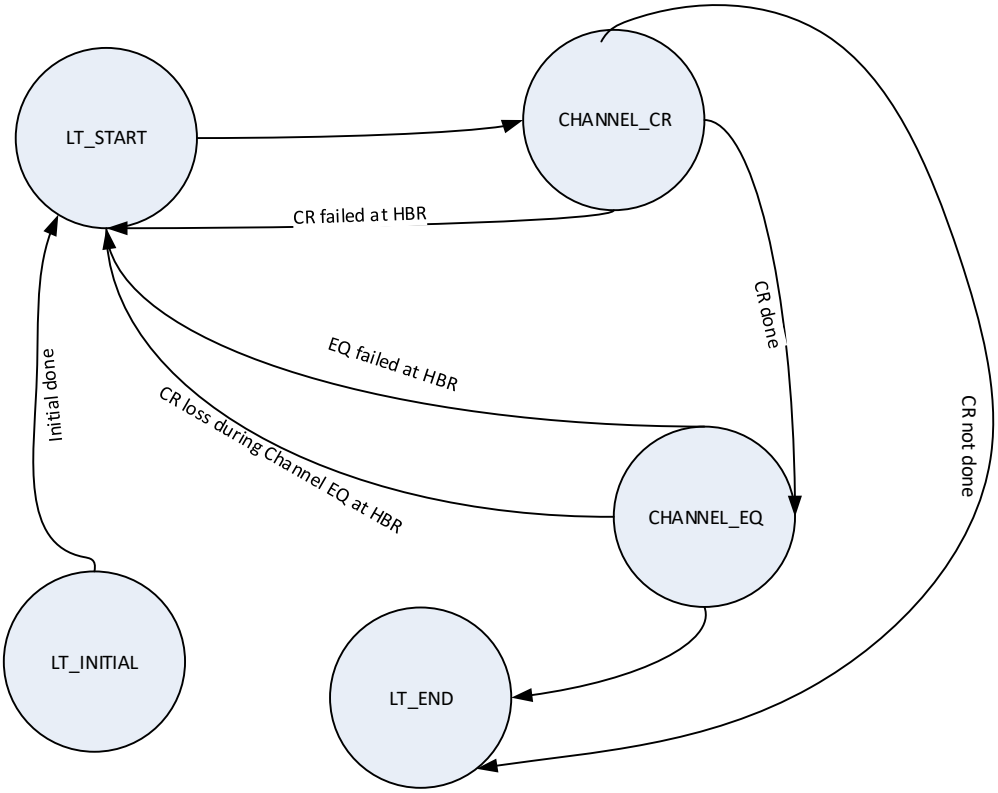


Fig. 23-10 State Machine of SW Link Training

23.6.2.6.2 State LT_INITIAL

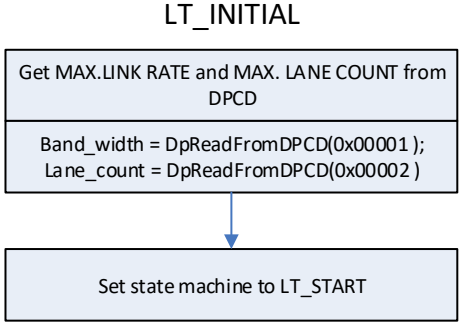


Fig. 23-11 State LT_INITIAL

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23.6.2.6.3 State LT_START

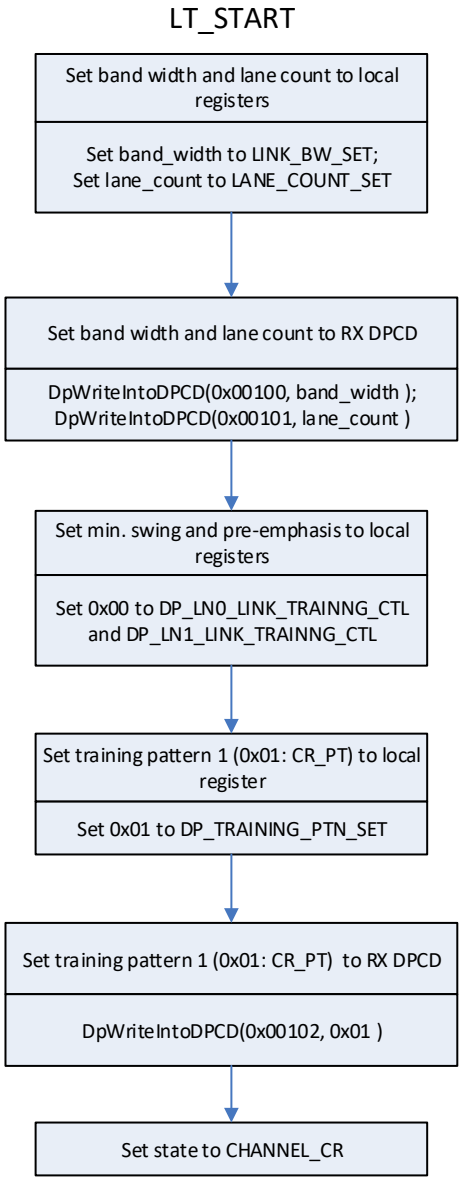


Fig. 23-12 State LT_START

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23.6.2.6.4 State CHANNEL_CR

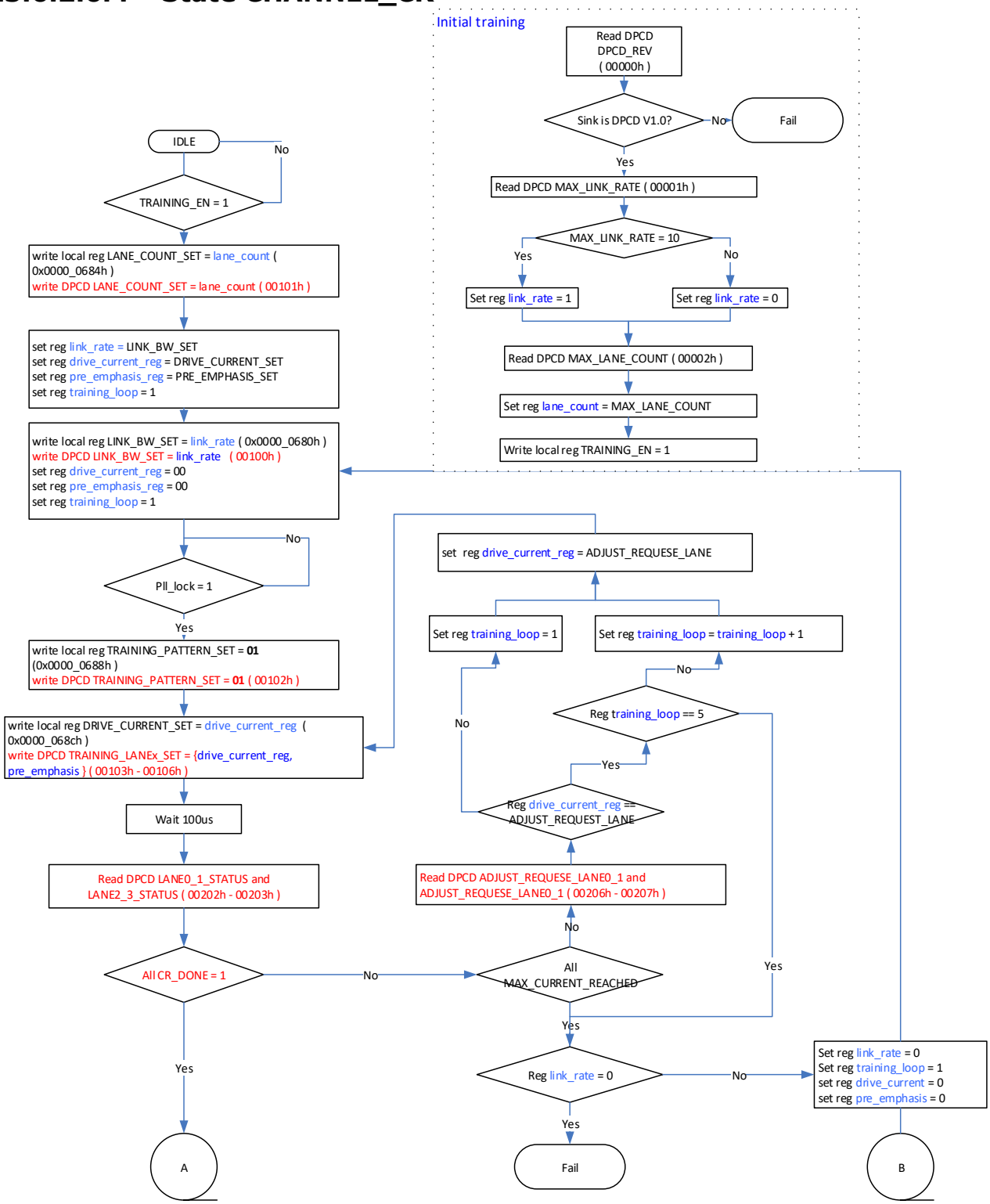
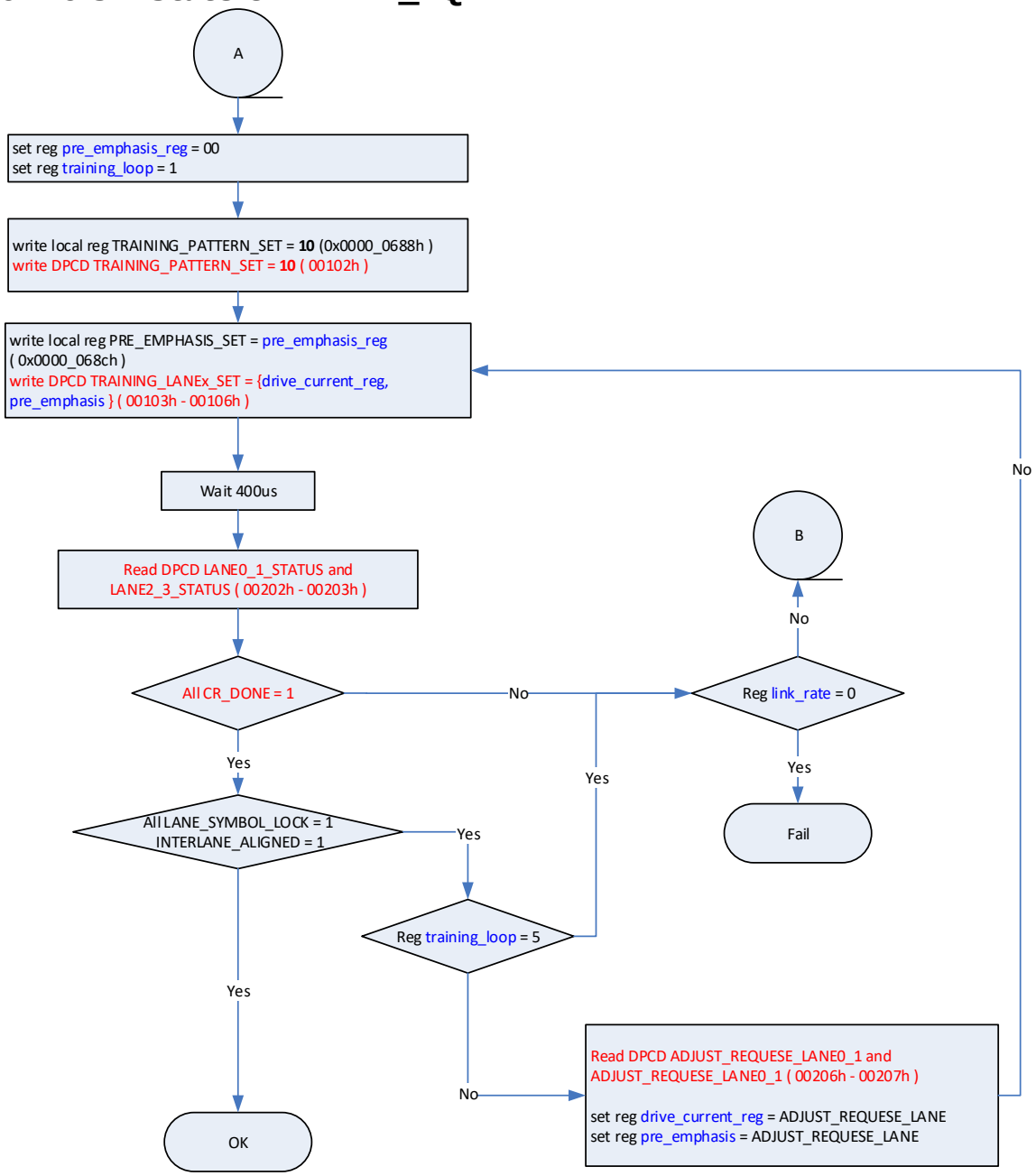


Fig. 23-13 Link Training Initial and Clock Recovery Training

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23.6.2.6.5 State CHANNEL_EQ



Note : link_rate, lane_count, drive_current_reg, pre_emphasis_reg and training_loop are temporary variables.

Fig. 23-14 Equalizer Training

23.6.2.7 How to Setup Main Stream Attribute Data

23.6.2.7.1 Attribute of Video timing

Chip hardware setups attribute of video timing automatically.

23.6.2.7.2 Attribute of Color Depth

Set IN_BPC of VIDEO_CTL_2 with correct value.

23.6.2.7.3 Attribute of Color Space

Set IN_COLOR_F of VIDEO_CTL_2 [1:0] with correct value.
IN_YC_COEFFI of VIDEO_CTL_3 [7] also must be set.

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23.6.2.8 How to do HDCP Authentication and Encryption

23.6.2.8.1 Initialize HDCP Key

Taking eDP0 as an example, the configuration process is as follows.
<Step 1>Set HDCP Key write enable. <BUS_SGRF_SOC_CON21>[12] = 1'b0
<Step 2>Write HDCP Key into memory. The base HDCP key address for eDP0 is 0xFDF18000.
<Step 3>Set HDCP Key access by controller. <BUS_SGRF_SOC_CON21>[12] = 1'b1

For eDP1
<Step 1>Set HDCP Key write enable. <BUS_SGRF_SOC_CON21>[13] = 1'b0
<Step 2>Write HDCP Key into memory. The base HDCP key address for eDP1 is 0xFDF1C000.
<Step 3>Set HDCP Key access by controller. <BUS_SGRF_SOC_CON21>[13] = 1'b1

23.6.2.8.2 SW HDCP State Machine

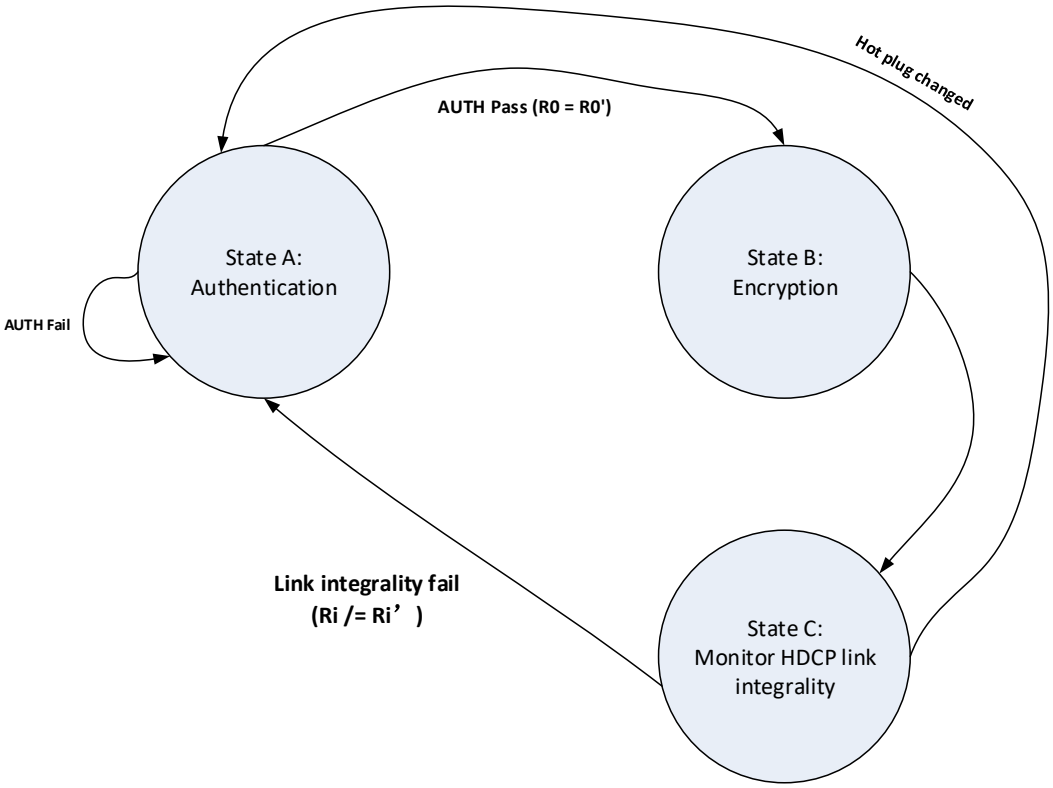


Fig. 23-15 SW HDCP State Machine

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23.6.2.8.3 SW HDCP Flowchart

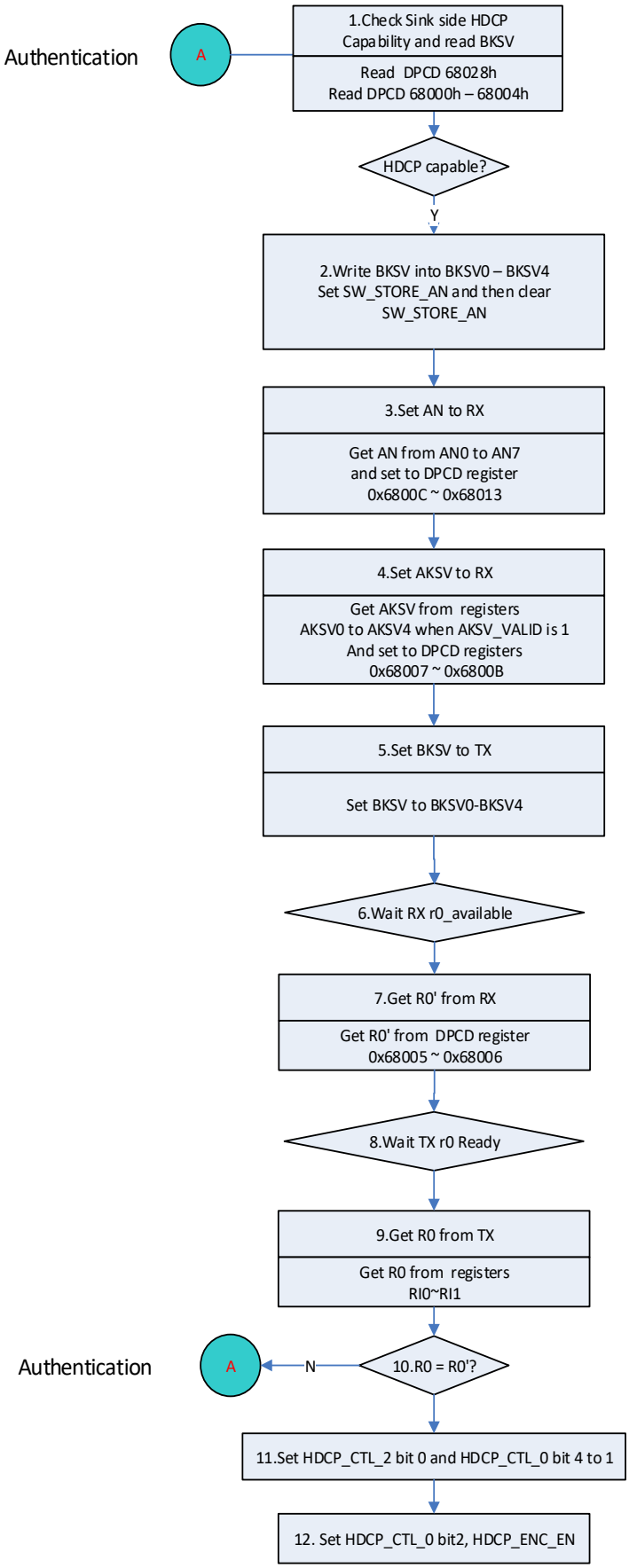


Fig. 23-16 SW HDCP Flowchart A

Note that BKSV to BKSV0~BKSV4 are loaded two times in step2 and in step5. With the first BKSV writing, AKSV starts to be loaded and SW_STORE_AN function is enabled. As another function, validity of BKSV is possible by the bit filed, BKSV_VALID. In the other hand, the

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second BKSV writing starts the R0 calculation.

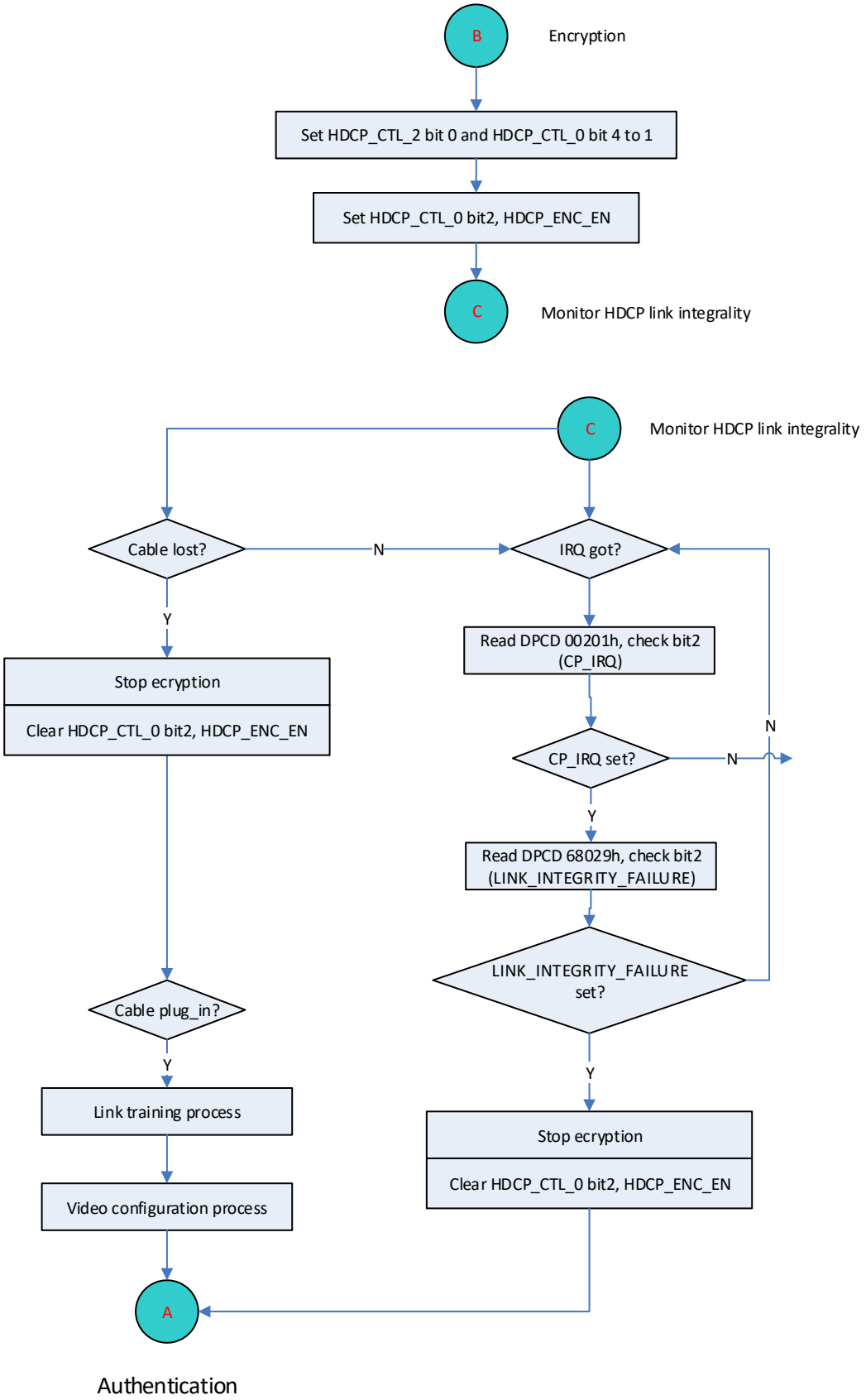


Fig. 23-17 SW HDCP Flowchart B

23.6.2.9 How to Configure Video

We suggest using M value auto-generated mode.

Slave mode video configuration process (M value auto-generated)

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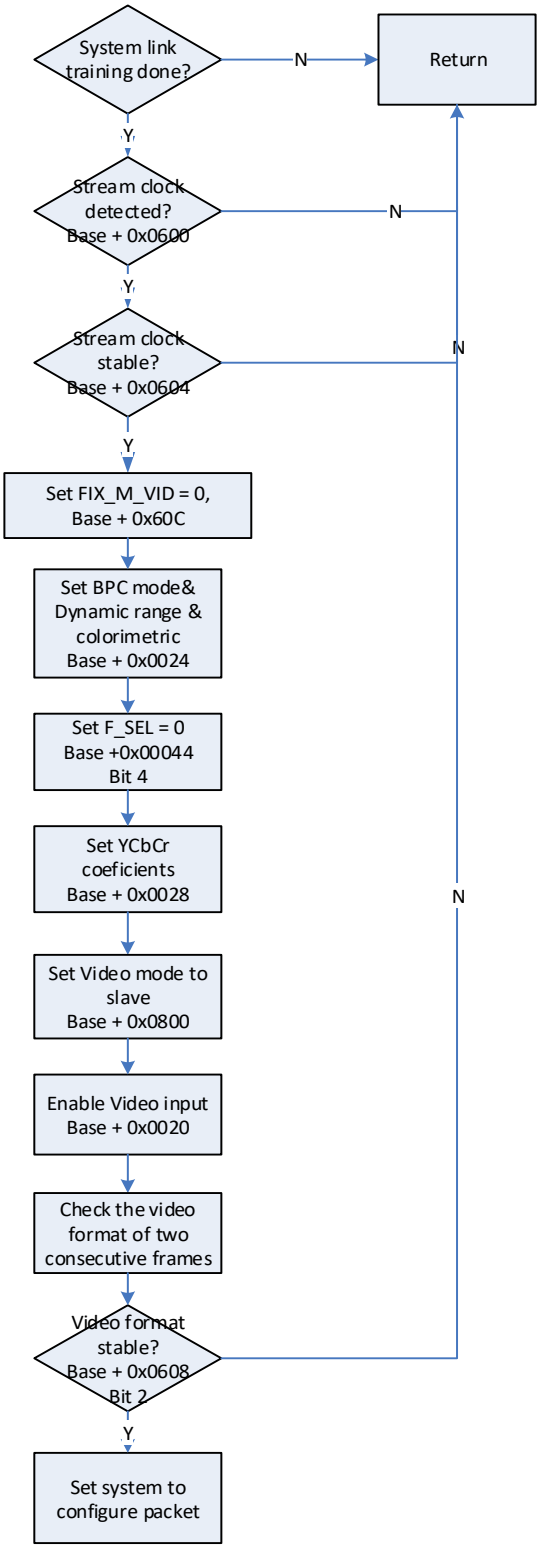


Fig. 23-18 Slave mode video configuration process (M value auto-generated)

Slave mode video configuration process (M value register defined 1400x1050/108M, RGB888, 2.7G)

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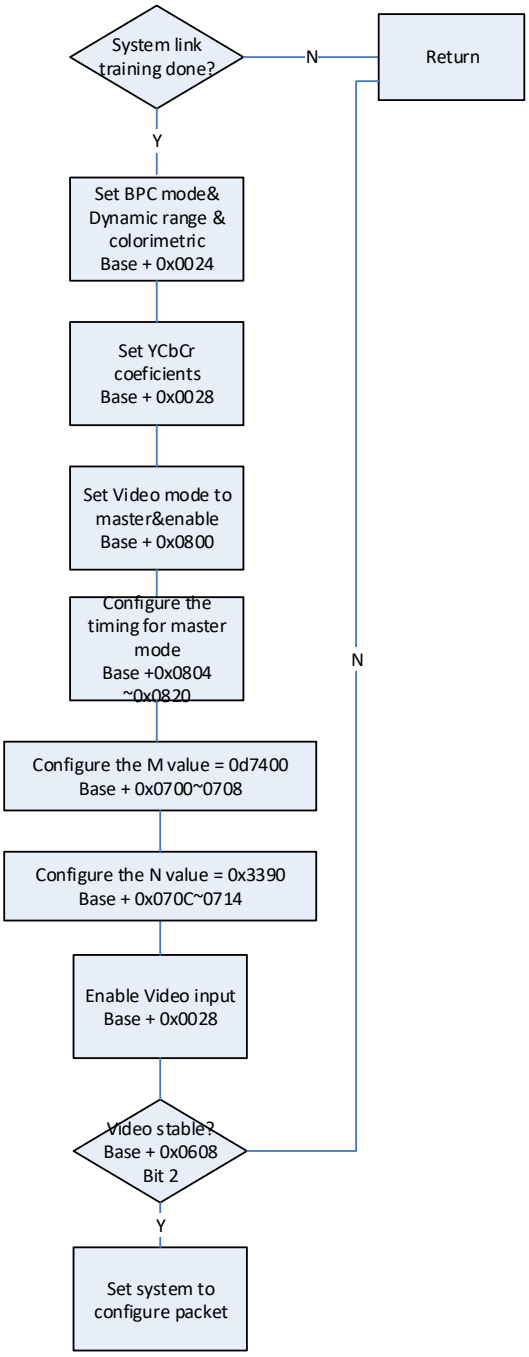


Fig. 23-19 Slave mode video configuration process (M value register defined)

Notes: Usually, you do not need to set FIX_M_VID to 1. We suggest that set FIX_M_VID to 0.

If FIX_M_VID is 0, then the hardware calculated M_VID value is used. But, if FIX_M_VID must be set to 1 by any reason, then M_VID_0, M_VID_1 and M_VID_2 should be set by using following formula.

M_VID = F_STRM_CLK * N_VID / FDIV2_CLK

Notes: F_STRM_CLK means the frequency of STRM_CLK, FDIV2_CLK means the frequency of I_CLK_DIV2. STRM_CLK and I_CLK_DIV2 can be found in figure DP Clock Domain.

N_VID must be choose let the result of this equation is an integer, for example N_VID is 13500 (0x34bc) in 2.7G and 8100 (0x1fa4) in 1.62G.

2.7G: M_VID = F_STRM_CLK*0x34BC/135M

1.62G: M_VID = F_STRM_CLK*0x1FA4/81M

For example, if input is 1400x1050/108M, RGB888, 2.7G,

M_VID = 108*0x34BC/135= 0x2A30,

set M_VID_0 = 0x30, set M_VID_1 = 0x2A, set M_VID_2 = 0.

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23.6.2.10 How to Configure Audio

If want to transfer S/PDIF or I2S by eDP TX, please set these GRF registers first.
<GRF_VO0_CON0>[0] = 1'b1 //eDP I2S
<GRF_VO0_CON0>[1] = 1'b1 //eDP S/PDIF
The controller should be set as below. We suggest using M value auto-generated mode.
Slave mode audio configuration process (M value auto-generated)

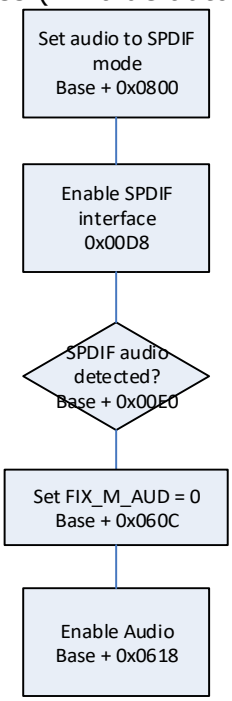


Fig. 23-20 Slave mode audio configuration process (M value auto-generated)

For example audio type is I2S, which is 2CH, 44.1kHz, 16 bits sample, setting as below

```
<EDPTX_DP_AUD_CTL>       = 0x11
<EDPTX_FUNC_EN_1>        = 0x04
<EDPTX_AUD_CTL>          = 0x01
<EDPTX_I2S_CTRL>         = 0x10
<EDPTX_I2S_CH_SWAP>      = 0x02
<EDPTX_DP_AUD_CTL>       = 0x15
<EDPTX_I2S_CH_CTRL1>     = 0x00

//I2S STA
<EDPTX_AUDIO_I2S_CH_STA1>       = 0x00
<EDPTX_AUDIO_I2S_CH_STA2>       = 0x00
<EDPTX_AUDIO_I2S_CH_STA3>       = 0x21
<EDPTX_AUDIO_I2S_CH_STA4>       = 0x10
<EDPTX_AUDIO_I2S_CH_STA5>       = 0x01
```

For other sample_rate, channel number and bits_per_sample, change the setting value.
If I2S is 8CH, <EDPTX_I2S_CH_CTRL1> bit2 should be 1'b1.
Slave mode audio configuration process (Register defined M value, 48 KHz, 2.7 G)

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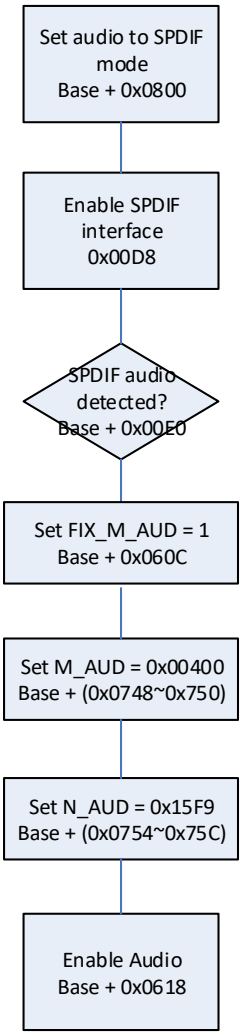


Fig. 23-21 Slave mode audio configuration process (Register defined M value)

Notes: Usually, you do not need to set FIX_M_AUD to 1. We suggest that set FIX_M_AUD to 0.

If FIX_M_AUD is 0, then the hardware calculated M_AUD value is used. But, if FIX_M_AUD must be set to 1 by any reason, then M_AUD_0, M_AUD_1, M_AUD_2 and N_AUD_0, N_AUD_1, N_AUD_2 should be set by using following formula.

M_AUD = 512*Faud_sample* N_AUD / 2 * FLS_CLK

Notes: Faud_sample is the sampling frequency of the audio stream being transported. FLS_CLK is the frequency of I_LINK_CLK. I_LINK_CLK can be found in figure 1-4 DP Clock Domain.

For example,

2.7G M_AUD = 512*Faud_sample *N_AUD/270,000,000

1.62G M_AUD = 512*Faud_sample*N_AUD/162,000,000

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23.6.2.11 How to PROCESS interrupt

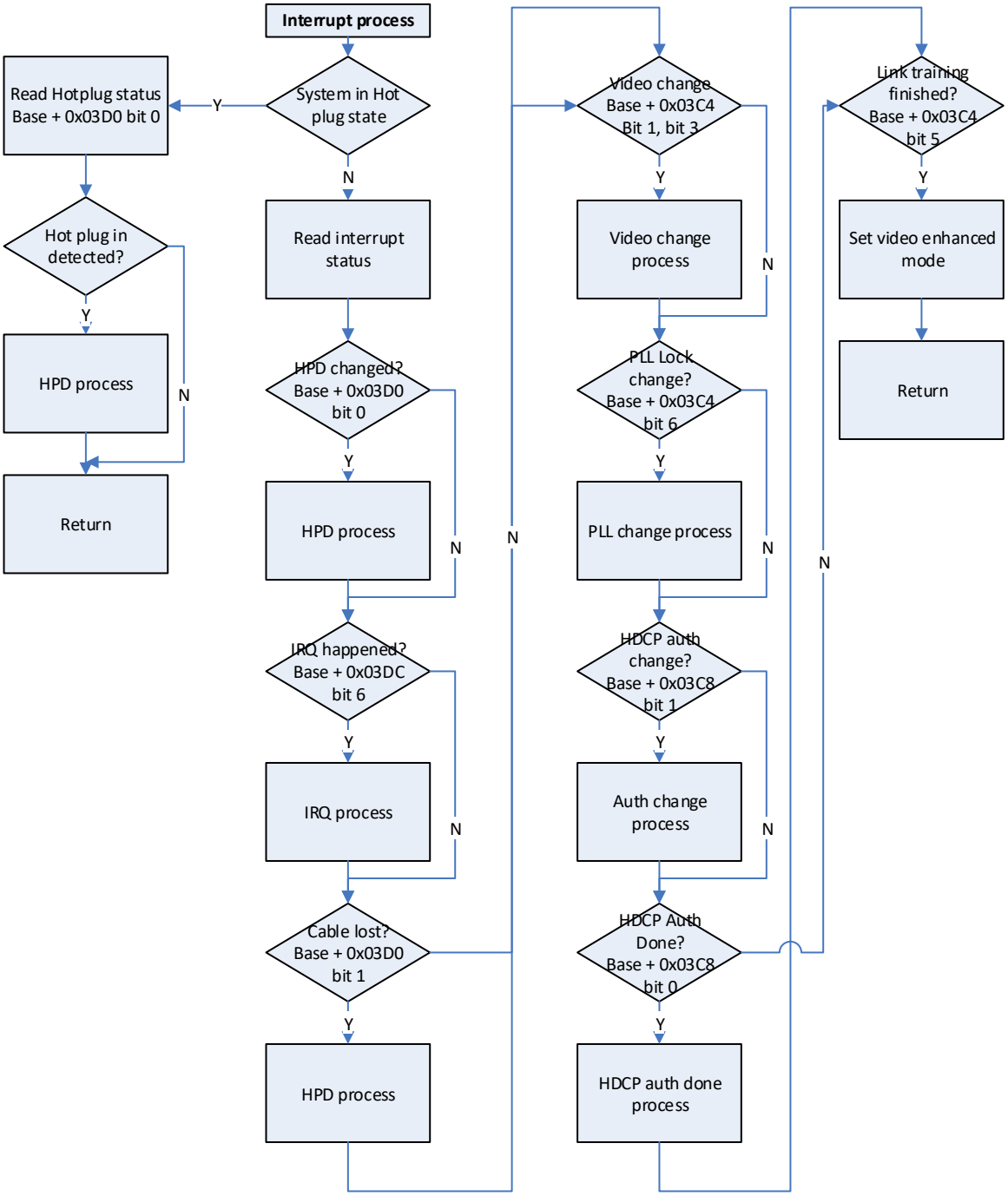


Fig. 23-22 Interrupt process

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23.6.2.12 How to Send Auxiliary Information Packets

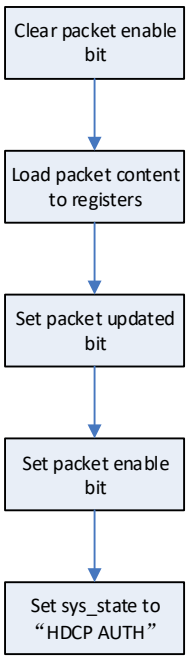


Fig. 23-23 Send Auxiliary Information Packets

23.6.3 GRF Setting for EDP TX

<GRF_HDPTX_CON0> [0] = 1'b1 //PHY EDP mode
If want to transfer S/PDIF or I2S, please set these registers:
<GRF_VO0_CON0>[0] = 1'b1 //eDP I2S
<GRF_VO0_CON0>[1] = 1'b1 //eDP S/PDIF
If want to select video path from EBC, please set the register:
<GRF_VO0_CON9>[10] = 1'b1

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Chapter 24 HDMI TX Controller

24.1 Overview

The HDMI TX Controller supports the following features:
HDMI 2.1 Compliance
- Fixed Rate Link (FRL) stream
- Support for 4K@120 Hz video modes
- Extended Metadata Packets
- Variable Refresh Rate (VRR) including Quick Media Switching (QMS) which is also known as Cinema VRR)
- Reed-Solomon Forward Error Correction (RSFEC)
- SCDC I2C DDC access
- TMDS Scrambler to enable support for 4K@60 Hz with RGB/YCbCr 4:4:4/YCbCr 4:2:2
- Character Error Detection
- Multi-stream Audio Support (Multi-stream Audio Sample)
- Audio Return Channel (ARC)

HDCP 1.4 Compliance
- According to HDMI 2.1 Specification, support for this HDCP encryption/decryption method is not available when operating in Fixed Rate Link mode
- For HDMI 2.0 and lower version specifications, HDCP 1.4 content protection engine is available

HDCP 2.3 Compliance
- External HDCP 2 interface is provided, which allows connecting HDCP 2 Embedded Security Module IP that can be licensed separately

Single-channel DVI 1.0 backward compatibility (dual-link DVI is not supported) All HDMI sources are compatible with all DVI-compliant sinks and all HDMI sinks are compatible with DVI-compliant sources. All HDMI devices are compatible to the DVI 1.0 Specification, except some rules. For more information on these rules, see the *HDMI 1.4b Specification*.
Supports the following video formats:
- RGB 4:4:4 8-bit normal color mode
- RGB 4:4:4 10-bit deep color mode
- YCBCR 4:4:4 8-bit normal color mode
- YCBCR 4:4:4 10-bit deep color mode
- YCBCR 4:2:2 10-bit deep color mode
- YCBCR 4:2:0 8-bit normal color mode
- YCBCR 4:2:0 10-bit deep color mode
- Up to 4K x 2K video format (HDMI 1.4b)
- CEA-861-F video format (HDMI 2.0)
- CTA-861-G video format (HDMI 2.1)

Supports encoded audio data:
- L-PCM
- L-PCM multi-channel
- High Bit-Rate audio

Supports CEC function. CEC is a protocol that provides high-level control functions between all of the various audiovisual products in your environment. The CEC bus allows all products in the system to potentially discover and communicate with each other.
Support ARC function. The ARC TX uses the HPD and utility lines of the HDMI connector to receive audio samples from HDMI sink to HDMI source, along with bidirectional control data packets.
The supported audio formats include:
- L-PCM (up to 32 channels)

Requirement of interface video timing
- Suggest follow CTA-861 and VESA standard
- When the video timing is not standard, HSYNC/HBP/HFP is suggested 4 pixel aligned

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24.2 Block Diagram

HDMI TX CONTROLLER comprises with:

- MM: Main Module
- APB: APB Interface Module
- AVP: Audio Video Packet Module
- ARC: Audio Return Channel Receiver (ARC Rx) Controller
- CEC Module: Consumer Electronics Control Module
- HDCP 2.x Encoder (External)
- IPI: Image Pixel Interface
- STI: SPDIF Tx Interface
- ITI: I2S Tx Interface
- SRI: S/PDIF Rx Interface
- IRI: I2S Rx Interface

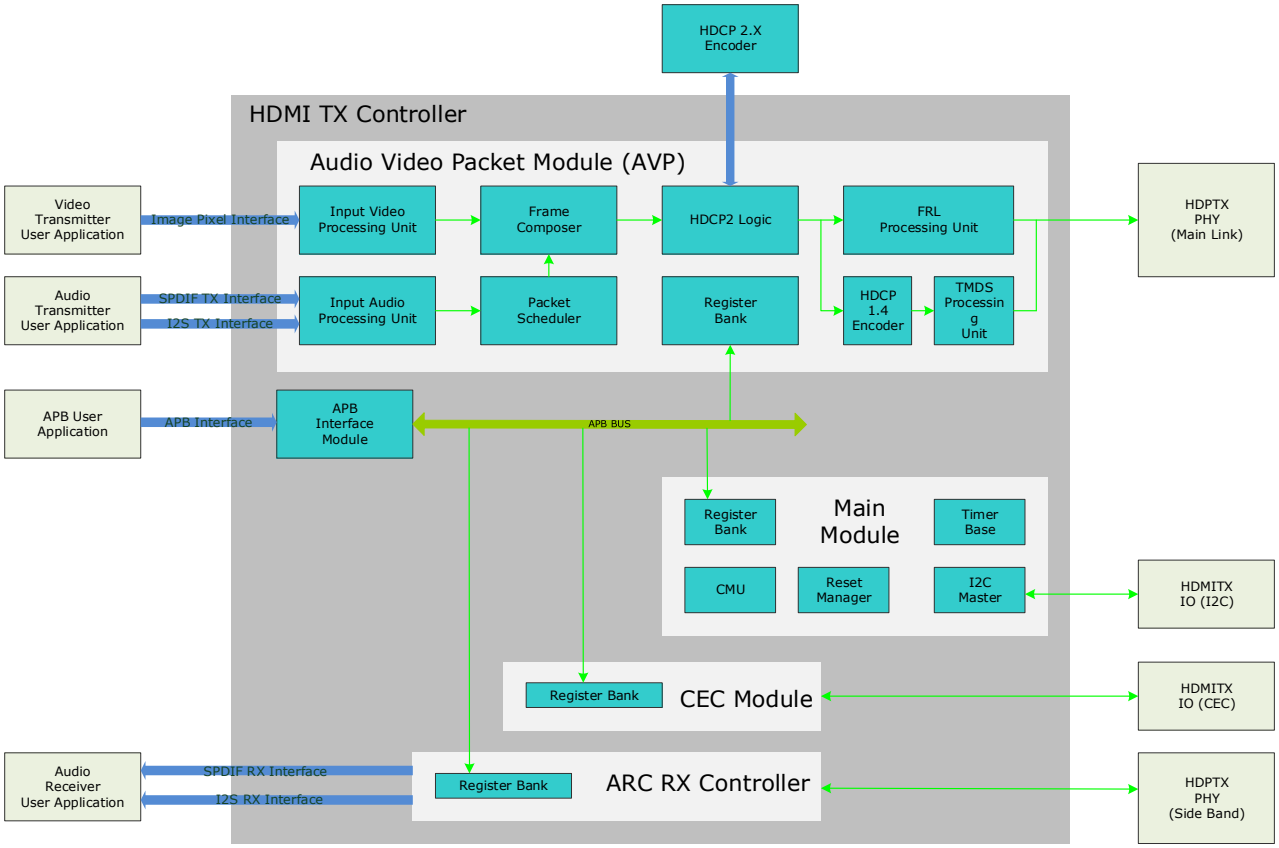


Fig. 24-1 HDMI TX Controller Block Diagram

24.3 Function Description

24.3.1 Main Module

This includes the following sub modules which can be common or completely independent of the remaining macro blocks.

- Reset Manager Module
- Timer Base Module
- Control Measurement Unit
- Status and Control Data Channel Module
- Display Data Channel
- I2C Master Module

24.3.1.1 Reset Manager Module

The Reset Manager module, generates all reset and initial signals required by the other functional modules; Synchronizes the resets to different clock domains; Guarantees that the resets from different clock domains to the same functional modules; Overlap when asserted the reset architecture of the HDMI TX Controller comprises of three types of

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clearing logic: the asynchronous reset, software initials, and software disables.

24.3.1.2 Timer Base Module

The Timer Base module generates timer bases for the reference counters of the different timers. The timer bases are calculated based on the timer_reference_base (frequency of the reference clock - refclk) field of the timer_base_config0 registers.

24.3.1.3 Control Measurement Unit

The Control Measurement Unit (CMU) measures the frequency and provides watchdog of imeasclk signal (frequency greater than 2 KHz). Frequency= ocfgr_clk_freq[19:0]/base time signal or evaluation period.

24.3.1.4 Status and Control Data Channel Module

The Status and Data Control Channel (SCDC) operates as a point-to-point communication protocol to exchange data between the HDMI Source and the HDMI Sink. It is an I2C-based system and makes use of the same I2C interface used for E-EDID (DDC) accesses and for HDCP (I2C Bus) accesses. This protocol extends the I2C standard by providing a mechanism for the Sink device (I2C Slave) to request a Source device (I2C Master) to initiate a status check read. The SCDC access is used for Read/Write operations into the SCDC registers for retrieving information about the actual status of the controller.

24.3.1.5 Display Data Channel

The Display Data Channel (DDC) reads E-EDID and SCDC structure to determine the capabilities and characteristics of the Sink. DDC implements the I2C Master for DDC/E-DDC channel in HDMI TX controller.

The DDC Controls all I2C transactions Interfaces with HDCP 1.4, HDCP 2.x, SCDC, and software The I2C Master complies with the *I2C Bus Specification, Version 2.1*.

24.3.1.6 I2C Master Module

The I2C Master module implements the I2C Master for E-DDC channel in HDMI TX Controller. It is responsible for all I2C transactions and it can interface with HDCP 1.4, HDCP 2.x, SCDC, and software (SW). The software interface allows reading the Sink's E-EDID based on system needs. The I2C Master complies with the *I2C Bus Specification 2.1*.

24.3.2 AMBA APB Interface Module

The APB Interface communicates between the AMBA 3 APB Slave Interface module and the HDMI TX Register Bank. The AMBA APB Interface module. Receives the APB Master's Read/Write operations and translates them into the internal Register Bank Access (RBK) protocol; Multiplexes the Register Bank access to the several domains based on the APB address; Synchronizes the Register Bank access protocol into/from the corresponding clock domain For more information, see *AMBA 3 APB Protocol*.

24.3.3 Audio Video Packets (AVP) Module

The Audio Video Packets (AVP) module packages the input audio, video, and packet information into a TMDS stream and prepares it for transmission in to the FRL or TMDS stream. This stream can be redirected for encryption to an external HDCP 2.x encoder. An HDCP 1.4 encoder is used internally for the TMDS stream. AVP module consists of the following modules: "Video Processing Unit","FRL Processing Unit","TDMS Processing Unit" ,"Audio Processing Unit".

24.3.3.1 Video Processing Unit

The Video Processing Unit receives the video stream from the user application side to transmit into the HDMI stream. The Video Processing Unit of the AVP module consists of the components shown in the figure below.

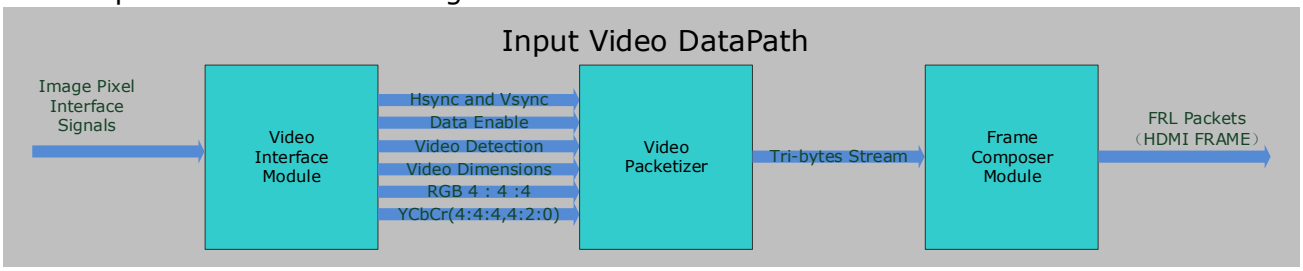


Fig. 24-2 Input Video Data Path

The Video Interface module detects and measures the video parameters and characteristics of the input video stream (IPI). The Video Interface module also samples the Image Pixel

Interface (IPI) and maps the correspondent video data to the internal blocks. The measured video parameters are: Hfront, Hback, Hblank, Hactive, Htotal, Hsync Width, Vsync Width, Vback, Vblank, Vactive, Vtotal.
The measured video characteristics are Vsync polarity, Hsync polarity, Alternative video detection, Field detection, Progressive or Interlaced video detection.

24.3.3.2 FRL Processing Unit

The FRL Processing Unit of the AVP module consists of the components shown in the figure below.

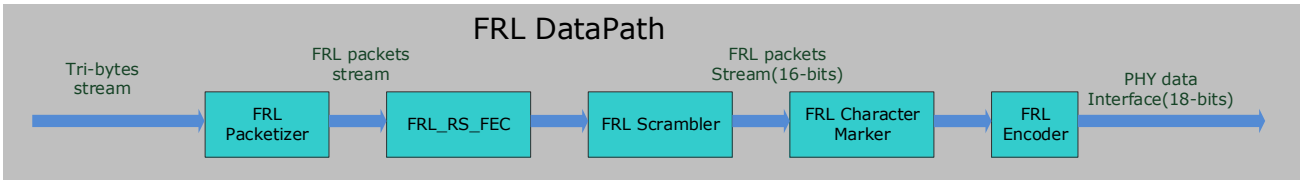


Fig. 24-3 FRL Data Path

24.3.3.3 TMDS Processing Unit

The TMDS Processing Unit processes the TMDS stream which includes audio, video, and auxiliary data stream. The TMDS Processing Unit of the AVP module consists of the components shown in the figure below.

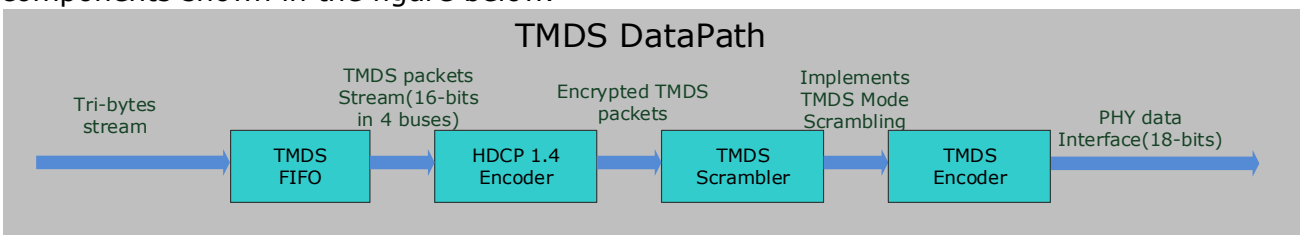


Fig. 24-4 TMDS Data Path

24.3.3.4 HDCP 1.4 Encoder

The HDCP 1.4 Encoder module receives the data from the TMDS Datapath from the four buses (a, b, c and d). This data includes the following: Video, Data Island, Control Period, HSYNC and VSYNC Indication, Data Enable This module encrypts the TMDS Stream. HDCP 1.4 uses an custom cipher for data encoding, a Finite State Machine to control the encryption operation and a dedicated access to the I2C Master present in the HDMI TX controller. For more information about the HDCP protocol, see the *HDCP 1.4 Specification*.

24.3.3.5 Audio Processing Unit

The Input Audio Processing Unit receives the audio data-Inter-IC Sound (I2S) Interface, and Sony/Philips Digital Interface (S/PDIF), from the application side to transmit into the HDMI stream. The Input Audio Processing Unit of the AVP module consists of the components shown in Figure 67-5.

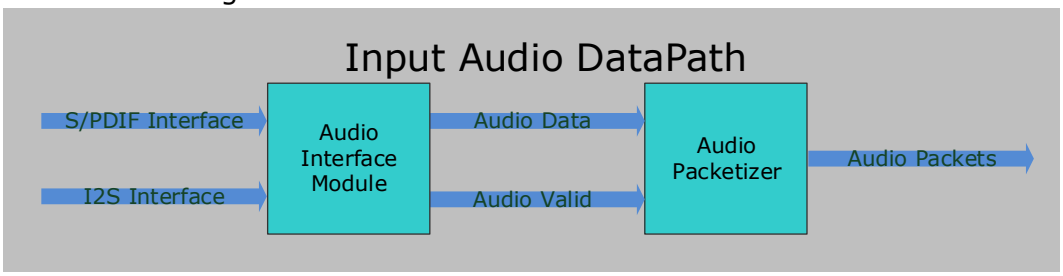


Fig. 24-5 Input Audio Data Path

24.3.3.6 Packet Scheduler

The Packet Scheduler schedules enabled packets and transfers it to the Frame Composer module. You can configure the priorities of the packets.

24.3.4 Audio Return Channel Receiver (ARC Rx) Controller

The ARC Rx controller Uses the HPD and Utility lines to receive audio samples from the ARC Rx sink. Supports bi-directional communication of data packets. The data packets are read and written through the register bank. The following are the audio output selectable interfaces: Sony/Philips Digital Interface (S/PDIF) (up to 8 audio channels);

24.3.5 Consumer Electronics Control Module

The Consumer Electronics Control (CEC) module Provides high-level control functions for all

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the various audio-visual products connected to the HDMI. Uses a single bidirectional line for transmission and reception of messages. The following terms are commonly used for CEC module: Message–The information (payload data) received by CEC application/software level. Frame–A frame is one burst of a data flow (including payload and overhead data) received by the CEC controller after triggered by the CEC software. The maximum size of a frame is 16 data blocks (including a header block). Data/Header block–One data/header block consists of 10-bits, in which 8-bits are payload data and 2-bits are overhead. There are two operation modes for a CEC module. Initiator mode–In this mode, the CEC module sends out messages and waits for a follower for feed-back. CEC module works in this mode when it sends a frame. After the transmission is complete, it reverts to the follower mode automatically. Follower mode–In this mode, the CEC module receives messages and sends appropriate acknowledgment to the initiator. The CEC module always works in the follower mode whenever it does not transmit any data. There can be more than one followers.

24.3.6 HDCP 2.x Encoder(External)

The HDCP 2.x Encoder encrypts the Tri-bytes stream using the HDCP 2.x encryption protocol. The HDCP 2.x specification includes a more powerful authentication protocol and a locality check that ensures the sink and source are close together. HDCP 2.x is not backward compatible with HDCP 1.4, so both protection systems co-exist in the HDMI TX controller. The controller provides support for HDCP 2.x, through external HDCP 2.x encoder. HDCP 2.x Encoder (HDCP2 ESM) can be automatically configured and integrated with the controller. The verification environment also supports this encryption engine.

24.3.7 Register Bank

The register bank comprises of 32-bit registers that can be seen from the software side, as read-only, write-only, read-write. The configuration shell module placed per clock domain and functional area reduces the number of synchronizations. Synchronization is done at the APB level instead at the bit field or signal levels. The Register Bank of the HDMI TX controller is divided into four regions that is placed within the functional domain, AVP, MAIN, CEC

24.4 Register Description

24.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

24.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_CORE_ID	0x0000	W	0x48515458	IP Identification Register
HDMI TX Controller_VER_NUMBER	0x0004	W	0x30313030	IP Version Number Register
HDMI TX Controller_VER_TYPE	0x0008	W	0x6C753030	IP Version Type Register
HDMI TX Controller_CONFIG_REG	0x000C	W	0x11E0D501	IP Configuration Identification Register
HDMI TX Controller_CORE_TIMESTAMP_HHMM	0x0014	W	0x31373336	IP Timestamp HHMM Register
HDMI TX Controller_CORE_TIMESTAMP_MMDD	0x0018	W	0x30333131	IP Timestamp MMDD Register
HDMI TX Controller_CORE_TIMESTAMP_YYYY	0x001C	W	0x32303231	IP Timestamp YYYY Register
HDMI TX Controller_GLOBAL_SWRESET_REQUEST	0x0040	W	0x00000000	Main Controller Software Reset Register

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_GLOBAL_SWDISABLE	0x0044	W	0x00000000	Main Controller Synchronous Disable Register
HDMI TX Controller_RESET_MANAGER_CONFIG0	0x0048	W	0x00000000	Main Controller Software Configuration Register 0
HDMI TX Controller_RESET_MANAGER_STATUS0	0x0050	W	0x00000000	Main Controller Software Status Register 0
HDMI TX Controller_RESET_MANAGER_STATUS1	0x0054	W	0x00000000	Main Controller Software Status Register 1
HDMI TX Controller_RESET_MANAGER_STATUS2	0x0058	W	0x00000000	Main Controller Software Status Register 2
HDMI TX Controller_TIMER_BASE_CONFIG0	0x0080	W	0x179A7B00	Timer Base Configuration Register 0
HDMI TX Controller_TIMER_BASE_STATUS0	0x0084	W	0x00000000	Timer Base Status Register 0
HDMI TX Controller_I2CM_SM_SCL_CONFIG0	0x00E0	W	0x085E085E	I2C Master Standard-mode SCL configuration 0
HDMI TX Controller_I2CM_FM_SCL_CONFIG0	0x00E4	W	0x02170217	I2C Master Fast-mode SCL configuration 0
HDMI TX Controller_I2CM_CONFIG0	0x00E8	W	0x00000000	I2C Master configuration 0
HDMI TX Controller_I2CM_CONTROL0	0x00EC	W	0x00000000	I2C Master control 0
HDMI TX Controller_I2CM_STATUS0	0x00F0	W	0x00000000	I2C Master status 0
HDMI TX Controller_I2CM_INTERFACE_CONTROL0	0x00F4	W	0x00000000	I2C Master Interface SW access control 0
HDMI TX Controller_I2CM_INTERFACE_CONTROL1	0x00F8	W	0x00000000	I2C Master Interface SW access control 1
HDMI TX Controller_I2CM_INTERFACE_WRDATA_0_3	0x00FC	W	0x00000000	I2C Master Interface SW write data, byte 0 to 3
HDMI TX Controller_I2CM_INTERFACE_WRDATA_4_7	0x0100	W	0x00000000	I2C Master Interface SW write data, byte 4 to 7
HDMI TX Controller_I2CM_INTERFACE_WRDATA_8_11	0x0104	W	0x00000000	I2C Master Interface SW write data, byte 8 to 11
HDMI TX Controller_I2CM_INTERFACE_WRDATA_12_15	0x0108	W	0x00000000	I2C Master Interface SW write data, byte 12 to 15

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_I2CM_INTERFACE_RDDATA_0_3	0x010C	W	0x00000000	I2C Master Interface SW read data, byte 0 to 3
HDMI TX Controller_I2CM_INTERFACE_RDDATA_4_7	0x0110	W	0x00000000	I2C Master Interface SW read data, byte 4 to 7
HDMI TX Controller_I2CM_INTERFACE_RDDATA_8_11	0x0114	W	0x00000000	I2C Master Interface SW read data, byte 8 to 11
HDMI TX Controller_I2CM_INTERFACE_RDDATA_12_15	0x0118	W	0x00000000	I2C Master Interface SW read data, byte 12 to 15
HDMI TX Controller_SCDC_CONFIG0	0x0140	W	0x00000080	SCDC configuration 0
HDMI TX Controller_SCDC_CONTROL0	0x0148	W	0x00000000	SCDC control 0
HDMI TX Controller_SCDC_STATUS0	0x0150	W	0x00000000	SCDC status 0
HDMI TX Controller_FLT_CONFIG0	0x0160	W	0x00000000	FRL Link Training configuration 0
HDMI TX Controller_FLT_CONFIG1	0x0164	W	0x00000000	FRL Link Training configuration 1
HDMI TX Controller_FLT_CONFIG2	0x0168	W	0x00000000	FRL Link Training configuration 2
HDMI TX Controller_FLT_CONTROL0	0x0170	W	0x00000000	FRL Link Training control 0
HDMI TX Controller_MAINUNIT_STATUS0	0x0180	W	0x00000000	Main Unit Status Register 0
HDMI TX Controller_VIDEO_INTERFACE_CONFIG0	0x0800	W	0x00000000	Video Interface configuration Register 0
HDMI TX Controller_VIDEO_INTERFACE_CONFIG2	0x0808	W	0x00000000	Video Interface configuration Register 2
HDMI TX Controller_VIDEO_INTERFACE_CONTROL0	0x080C	W	0x00000000	Video Interface control Register 0
HDMI TX Controller_VIDEO_INTERFACE_STATUS0	0x0814	W	0x00000000	Video Interface status Register 0
HDMI TX Controller_VIDEO_PACKING_CONFIG0	0x081C	W	0x00000000	Video Packing configuration Register 0
HDMI TX Controller_AUDIO_INTERFACE_CONFIG0	0x0820	W	0x00000000	Audio Interface configuration Register 0
HDMI TX Controller_AUDIO_INTERFACE_CONFIG1	0x0824	W	0x00000000	Audio Interface configuration Register 1

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_AUDIO_INTERFACE_CONTROL0	0x082C	W	0x00000000	Audio Interface control Register 0
HDMI TX Controller_AUDIO_INTERFACE_STATUS0	0x0834	W	0x00000000	Audio Interface status Register 0
HDMI TX Controller_FRAME_COMPOSER_CONFIG0	0x0840	W	0x42000000	Frame Composer configuration Register 0
HDMI TX Controller_FRAME_COMPOSER_CONFIG1	0x0844	W	0xFFF0FF00	Frame Composer configuration Register 1
HDMI TX Controller_FRAME_COMPOSER_CONFIG2	0x0848	W	0x00000000	Frame Composer configuration Register 2
HDMI TX Controller_FRAME_COMPOSER_CONFIG3	0x084C	W	0x00000000	Frame Composer configuration Register 3
HDMI TX Controller_FRAME_COMPOSER_CONFIG4	0x0850	W	0x00000000	Frame Composer configuration Register 4
HDMI TX Controller_FRAME_COMPOSER_CONFIG5	0x0854	W	0x00000000	Frame Composer configuration Register 5
HDMI TX Controller_FRAME_COMPOSER_CONFIG6	0x0858	W	0x00000000	Frame Composer configuration Register 6
HDMI TX Controller_FRAME_COMPOSER_CONFIG7	0x085C	W	0x00000000	Frame Composer configuration Register 7
HDMI TX Controller_FRAME_COMPOSER_CONFIG8	0x0860	W	0x00010000	Frame Composer configuration Register 8
HDMI TX Controller_FRAME_COMPOSER_CONFIG9	0x0864	W	0x00000100	Frame Composer configuration Register 9
HDMI TX Controller_FRAME_COMPOSER_CONTROL0	0x086C	W	0x00000000	Frame Composer control Register 0
HDMI TX Controller_VIDEO_MONITOR_CONFIG0	0x0880	W	0x00000000	Video Monitor configuration Register 0
HDMI TX Controller_VIDEO_MONITOR_STATUS0	0x0884	W	0x00000000	Video Monitor status Register 0
HDMI TX Controller_VIDEO_MONITOR_STATUS1	0x0888	W	0x00000000	Video Monitor status Register 1
HDMI TX Controller_VIDEO_MONITOR_STATUS2	0x088C	W	0x00000000	Video Monitor status Register 2
HDMI TX Controller_VIDEO_MONITOR_STATUS3	0x0890	W	0x00000000	Video Monitor status Register 3

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_VIDEO_MONITOR_STATUS4	0x0894	W	0x00000000	Video Monitor status Register 4
HDMI TX Controller_VIDEO_MONITOR_STATUS5	0x0898	W	0x00000000	Video Monitor status Register 5
HDMI TX Controller_VIDEO_MONITOR_STATUS6	0x089C	W	0x00000000	Video Monitor status Register 6
HDMI TX Controller_HDCP2LOGIC_CONFIG0	0x08E0	W	0x00000000	HDCP 2 Logic Configuration Register 0
HDMI TX Controller_HDCP2LOGIC_ESM_GPIO_IN	0x08E4	W	0x00000000	HDCP 2 Logic GPIO Inputs
HDMI TX Controller_HDCP2LOGIC_ESM_GPIO_OUT	0x08E8	W	0x00000000	HDCP 2 Logic GPIO Outputs
HDMI TX Controller_HDCP14_CONFIG0	0x0900	W	0x00010000	HDCP 1.4 Configuration Register 0
HDMI TX Controller_HDCP14_CONTROL0	0x0904	W	0x00000000	HDCP 1.4 Configuration Register 1
HDMI TX Controller_HDCP14_CONFIG1	0x0908	W	0x00000000	HDCP 1.4 Configuration Register 2
HDMI TX Controller_HDCP14_CONFIG2	0x090C	W	0x00000000	HDCP 1.4 Configuration Register 3
HDMI TX Controller_HDCP14_KEY_SEED	0x0914	W	0x00000000	HDCP 1.4 Key Decryption Seed Register
HDMI TX Controller_HDCP14_KEY_H	0x0918	W	0x00000000	HDCP 1.4 Key High Configuration Register
HDMI TX Controller_HDCP14_KEY_L	0x091C	W	0x00000000	HDCP 1.4 Key Low Configuration Register
HDMI TX Controller_HDCP14_KEY_STATUS	0x0920	W	0x00000000	HDCP 1.4 Key Status Register
HDMI TX Controller_HDCP14_AKSV_H	0x0924	W	0x00000000	HDCP 1.4 AKSV High Configuration Register
HDMI TX Controller_HDCP14_AKSV_L	0x0928	W	0x00000000	HDCP 1.4 AKSV Low Configuration Register
HDMI TX Controller_HDCP14_AN_H	0x092C	W	0x00000000	HDCP 1.4 An High Configuration Register
HDMI TX Controller_HDCP14_AN_L	0x0930	W	0x00000000	HDCP 1.4 An Low Configuration Register

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_HDCP14_STATUS0	0x0934	W	0x00000000	HDCP 1.4 Status Register 0
HDMI TX Controller_HDCP14_STATUS1	0x0938	W	0x00000000	HDCP 1.4 Status Register 1
HDMI TX Controller_SCRAMB_CONFIG0	0x0960	W	0x00000000	Scrambler config register 0
HDMI TX Controller_LINK_CONFIG0	0x0968	W	0x00000010	Link config register 0
HDMI TX Controller_TMDS_FIFO_CONFIG0	0x0970	W	0x00000001	TMDS FIFO Configuration Register 0
HDMI TX Controller_TMDS_FIFO_CONTROL0	0x0974	W	0x00000000	TMDS FIFO Control Register 0
HDMI TX Controller_FRL_RSFEC_CONFIG0	0x0A20	W	0x00000000	FRL Reed-Solomon FEC Configuration Register 0
HDMI TX Controller_FRL_RSFEC_STATUS0	0x0A30	W	0x00000000	FRL Reed-Solomon FEC Status Register 0
HDMI TX Controller_FRL_PKTZ_CONFIG0	0x0A40	W	0x00000000	FRL Packetizer Configuration Register 0
HDMI TX Controller_FRL_PKTZ_CONTROL0	0x0A44	W	0x00000000	FRL Packetizer Control Register 0
HDMI TX Controller_FRL_PKTZ_CONTROL1	0x0A50	W	0x00000000	FRL Packetizer Control Register 1
HDMI TX Controller_FRL_PKTZ_STATUS1	0x0A54	W	0x00000000	FRL Packetizer Status Register 1
HDMI TX Controller_PKTSCHED_CONFIG0	0x0A80	W	0x00000006	Packet Scheduler Configuration Register 0
HDMI TX Controller_PKTSCHED_PRQUEUE0_CONFIG0	0x0A84	W	0x00030201	Packet Scheduler Priority Queue 0 Configuration Register 0
HDMI TX Controller_PKTSCHED_PRQUEUE1_CONFIG0	0x0A88	W	0x09070D08	Packet Scheduler Priority Queue 1 Configuration Register 0
HDMI TX Controller_PKTSCHED_PRQUEUE2_CONFIG0	0x0A8C	W	0x06050C04	Packet Scheduler Priority Queue 2 Configuration Register 0
HDMI TX Controller_PKTSCHED_PRQUEUE2_CONFIG1	0x0A90	W	0x0E0F0B0A	Packet Scheduler Priority Queue 2 Configuration Register 1
HDMI TX Controller_PKTSCHED_PRQUEUE2_CONFIG2	0x0A94	W	0x00001110	Packet Scheduler Priority Queue 2 Configuration Register 2

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKTSCHED_PKT_CONFIG0	0x0A98	W	0x00764807	Packet Scheduler - Packet Configuration Register 0
HDMI TX Controller_PKTSCHED_PKT_CONFIG1	0x0A9C	W	0x00007F00	Packet Scheduler - Packet Configuration Register 1
HDMI TX Controller_PKTSCHED_PKT_CONFIG2	0x0AA0	W	0x11001000	Packet Scheduler - Packet Configuration Register 2
HDMI TX Controller_PKTSCHED_PKT_CONFIG3	0x0AA4	W	0x00000000	Packet Scheduler - Packet Configuration Register 3
HDMI TX Controller_PKTSCHED_PKT_EN	0x0AA8	W	0x00000000	Packet Scheduler - Packet Enable Control Register
HDMI TX Controller_PKTSCHED_PKT_CONTROL0	0x0AAC	W	0x00000000	Packet Scheduler - Packet Control Register 0
HDMI TX Controller_PKTSCHED_PKT_SEND	0x0AB0	W	0x00000000	Packet Scheduler - Packet Send Request
HDMI TX Controller_PKTSCHED_PKT_STATUS0	0x0AB4	W	0x00000000	Packet Scheduler - Status Register 0
HDMI TX Controller_PKTSCHED_PKT_STATUS1	0x0AB8	W	0x00000000	Packet Scheduler - Status Register 1
HDMI TX Controller_PKT_NULL_CONTENTS0	0x0B00	W	0x00000000	NULL - Null - Packet contents register 0
HDMI TX Controller_PKT_NULL_CONTENTS1	0x0B04	W	0x00000000	NULL - Null - Packet contents register 1
HDMI TX Controller_PKT_NULL_CONTENTS2	0x0B08	W	0x00000000	NULL - Null - Packet contents register 2
HDMI TX Controller_PKT_NULL_CONTENTS3	0x0B0C	W	0x00000000	NULL - Null - Packet contents register 3
HDMI TX Controller_PKT_NULL_CONTENTS4	0x0B10	W	0x00000000	NULL - Null - Packet contents register 4
HDMI TX Controller_PKT_NULL_CONTENTS5	0x0B14	W	0x00000000	NULL - Null - Packet contents register 5
HDMI TX Controller_PKT_NULL_CONTENTS6	0x0B18	W	0x00000000	NULL - Null - Packet contents register 6
HDMI TX Controller_PKT_NULL_CONTENTS7	0x0B1C	W	0x00000000	NULL - Null - Packet contents register 7
HDMI TX Controller_PKT_ACP_CONTENTS0	0x0B20	W	0x00000000	ACP - Audio Content Protection - Packet contents register 0

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKT_ACP_CONTENTS1	0x0B24	W	0x00000000	ACP - Audio Content Protection - Packet contents register 1
HDMI TX Controller_PKT_ACP_CONTENTS2	0x0B28	W	0x00000000	ACP - Audio Content Protection - Packet contents register 2
HDMI TX Controller_PKT_ACP_CONTENTS3	0x0B2C	W	0x00000000	ACP - Audio Content Protection - Packet contents register 3
HDMI TX Controller_PKT_ACP_CONTENTS4	0x0B30	W	0x00000000	ACP - Audio Content Protection - Packet contents register 4
HDMI TX Controller_PKT_ACP_CONTENTS5	0x0B34	W	0x00000000	ACP - Audio Content Protection - Packet contents register 5
HDMI TX Controller_PKT_ACP_CONTENTS6	0x0B38	W	0x00000000	ACP - Audio Content Protection - Packet contents register 6
HDMI TX Controller_PKT_ACP_CONTENTS7	0x0B3C	W	0x00000000	ACP - Audio Content Protection - Packet contents register 7
HDMI TX Controller_PKT_ISRC1_CONTENTS0	0x0B40	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 0
HDMI TX Controller_PKT_ISRC1_CONTENTS1	0x0B44	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 1
HDMI TX Controller_PKT_ISRC1_CONTENTS2	0x0B48	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 2
HDMI TX Controller_PKT_ISRC1_CONTENTS3	0x0B4C	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 3
HDMI TX Controller_PKT_ISRC1_CONTENTS4	0x0B50	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 4
HDMI TX Controller_PKT_ISRC1_CONTENTS5	0x0B54	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 5
HDMI TX Controller_PKT_ISRC1_CONTENTS6	0x0B58	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 6
HDMI TX Controller_PKT_ISRC1_CONTENTS7	0x0B5C	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 7
HDMI TX Controller_PKT_ISRC2_CONTENTS0	0x0B60	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 0
HDMI TX Controller_PKT_ISRC2_CONTENTS1	0x0B64	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 1
HDMI TX Controller_PKT_ISRC2_CONTENTS2	0x0B68	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 2

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller PKT ISRC2 CONTENTS3	0x0B6C	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 3
HDMI TX Controller PKT ISRC2 CONTENTS4	0x0B70	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 4
HDMI TX Controller PKT ISRC2 CONTENTS5	0x0B74	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 5
HDMI TX Controller PKT ISRC2 CONTENTS6	0x0B78	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 6
HDMI TX Controller PKT ISRC2 CONTENTS7	0x0B7C	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 7
HDMI TX Controller PKT GMD CONTENTS0	0x0B80	W	0x00000000	GMD - Gamut Metadata - Packet contents register 0
HDMI TX Controller PKT GMD CONTENTS1	0x0B84	W	0x00000000	GMD - Gamut Metadata - Packet contents register 1
HDMI TX Controller PKT GMD CONTENTS2	0x0B88	W	0x00000000	GMD - Gamut Metadata - Packet contents register 2
HDMI TX Controller PKT GMD CONTENTS3	0x0B8C	W	0x00000000	GMD - Gamut Metadata - Packet contents register 3
HDMI TX Controller PKT GMD CONTENTS4	0x0B90	W	0x00000000	GMD - Gamut Metadata - Packet contents register 4
HDMI TX Controller PKT GMD CONTENTS5	0x0B94	W	0x00000000	GMD - Gamut Metadata - Packet contents register 5
HDMI TX Controller PKT GMD CONTENTS6	0x0B98	W	0x00000000	GMD - Gamut Metadata - Packet contents register 6
HDMI TX Controller PKT GMD CONTENTS7	0x0B9C	W	0x00000000	GMD - Gamut Metadata - Packet contents register 7
HDMI TX Controller PKT AMD CONTENTS0	0x0BA0	W	0x00000000	AMD - Audio Metadata - Packet contents register 0
HDMI TX Controller PKT AMD CONTENTS1	0x0BA4	W	0x00000000	AMD - Audio Metadata - Packet contents register 1
HDMI TX Controller PKT AMD CONTENTS2	0x0BA8	W	0x00000000	AMD - Audio Metadata - Packet contents register 2
HDMI TX Controller PKT AMD CONTENTS3	0x0BAC	W	0x00000000	AMD - Audio Metadata - Packet contents register 3
HDMI TX Controller PKT AMD CONTENTS4	0x0BB0	W	0x00000000	AMD - Audio Metadata - Packet contents register 4

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKT_AMD_CONTENTS5	0x0BB4	W	0x00000000	AMD - Audio Metadata - Packet contents register 5
HDMI TX Controller_PKT_AMD_CONTENTS6	0x0BB8	W	0x00000000	AMD - Audio Metadata - Packet contents register 6
HDMI TX Controller_PKT_AMD_CONTENTS7	0x0BBC	W	0x00000000	AMD - Audio Metadata - Packet contents register 7
HDMI TX Controller_PKT_VSI_CONTENTS0	0x0BC0	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 0
HDMI TX Controller_PKT_VSI_CONTENTS1	0x0BC4	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 1
HDMI TX Controller_PKT_VSI_CONTENTS2	0x0BC8	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 2
HDMI TX Controller_PKT_VSI_CONTENTS3	0x0BCC	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 3
HDMI TX Controller_PKT_VSI_CONTENTS4	0x0BD0	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 4
HDMI TX Controller_PKT_VSI_CONTENTS5	0x0BD4	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 5
HDMI TX Controller_PKT_VSI_CONTENTS6	0x0BD8	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 6
HDMI TX Controller_PKT_VSI_CONTENTS7	0x0BDC	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 7
HDMI TX Controller_PKT_AVI_CONTENTS0	0x0BE0	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 0
HDMI TX Controller_PKT_AVI_CONTENTS1	0x0BE4	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 1
HDMI TX Controller_PKT_AVI_CONTENTS2	0x0BE8	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 2
HDMI TX Controller_PKT_AVI_CONTENTS3	0x0BEC	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 3
HDMI TX Controller_PKT_AVI_CONTENTS4	0x0BF0	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 4
HDMI TX Controller_PKT_AVI_CONTENTS5	0x0BF4	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 5
HDMI TX Controller_PKT_AVI_CONTENTS6	0x0BF8	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 6

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller PKT AVI CONTENTS7	0x0BFC	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 7
HDMI TX Controller PKT SPDI CONTENTS0	0x0C00	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 0
HDMI TX Controller PKT SPDI CONTENTS1	0x0C04	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 1
HDMI TX Controller PKT SPDI CONTENTS2	0x0C08	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 2
HDMI TX Controller PKT SPDI CONTENTS3	0x0C0C	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 3
HDMI TX Controller PKT SPDI CONTENTS4	0x0C10	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 4
HDMI TX Controller PKT SPDI CONTENTS5	0x0C14	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 5
HDMI TX Controller PKT SPDI CONTENTS6	0x0C18	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 6
HDMI TX Controller PKT SPDI CONTENTS7	0x0C1C	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 7
HDMI TX Controller PKT AUDI CONTENTS0	0x0C20	W	0x000A0100	AUDI - Audio InfoFrame - Packet contents register 0
HDMI TX Controller PKT AUDI CONTENTS1	0x0C24	W	0x00000000	AUDI - Audio InfoFrame - Packet contents register 1
HDMI TX Controller PKT AUDI CONTENTS2	0x0C28	W	0x00000000	AUDI - Audio InfoFrame - Packet contents register 2
HDMI TX Controller PKT AUDI CONTENTS3	0x0C2C	W	0x00000000	AUDI - Audio InfoFrame - Packet contents register 3
HDMI TX Controller PKT AUDI CONTENTS4	0x0C30	W	0x00000000	AUDI - Audio InfoFrame - Packet contents register 4
HDMI TX Controller PKT AUDI CONTENTS5	0x0C34	W	0x00000000	AUDI - Audio InfoFrame - Packet contents register 5
HDMI TX Controller PKT AUDI CONTENTS6	0x0C38	W	0x00000000	AUDI - Audio InfoFrame - Packet contents register 6
HDMI TX Controller PKT AUDI CONTENTS7	0x0C3C	W	0x00000000	AUDI - Audio InfoFrame - Packet contents register 7
HDMI TX Controller PKT NVI CONTENTS0	0x0C40	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 0

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKT_NVI_CONTENTS1	0x0C44	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 1
HDMI TX Controller_PKT_NVI_CONTENTS2	0x0C48	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 2
HDMI TX Controller_PKT_NVI_CONTENTS3	0x0C4C	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 3
HDMI TX Controller_PKT_NVI_CONTENTS4	0x0C50	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 4
HDMI TX Controller_PKT_NVI_CONTENTS5	0x0C54	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 5
HDMI TX Controller_PKT_NVI_CONTENTS6	0x0C58	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 6
HDMI TX Controller_PKT_NVI_CONTENTS7	0x0C5C	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 7
HDMI TX Controller_PKT_DRMI_CONTENTS0	0x0C60	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 0
HDMI TX Controller_PKT_DRMI_CONTENTS1	0x0C64	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 1
HDMI TX Controller_PKT_DRMI_CONTENTS2	0x0C68	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 2
HDMI TX Controller_PKT_DRMI_CONTENTS3	0x0C6C	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 3
HDMI TX Controller_PKT_DRMI_CONTENTS4	0x0C70	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 4
HDMI TX Controller_PKT_DRMI_CONTENTS5	0x0C74	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 5
HDMI TX Controller_PKT_DRMI_CONTENTS6	0x0C78	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 6
HDMI TX Controller_PKT_DRMI_CONTENTS7	0x0C7C	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 7
HDMI TX Controller_PKT_GHDMI1_CONTENTS0	0x0C80	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 0
HDMI TX Controller_PKT_GHDMI1_CONTENTS1	0x0C84	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 1
HDMI TX Controller_PKT_GHDMI1_CONTENTS2	0x0C88	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 2

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKT_GHDMI1_CONTENTS3	0x0C8C	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 3
HDMI TX Controller_PKT_GHDMI1_CONTENTS4	0x0C90	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 4
HDMI TX Controller_PKT_GHDMI1_CONTENTS5	0x0C94	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 5
HDMI TX Controller_PKT_GHDMI1_CONTENTS6	0x0C98	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 6
HDMI TX Controller_PKT_GHDMI1_CONTENTS7	0x0C9C	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 7
HDMI TX Controller_PKT_GHDMI2_CONTENTS0	0x0CA0	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 0
HDMI TX Controller_PKT_GHDMI2_CONTENTS1	0x0CA4	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 1
HDMI TX Controller_PKT_GHDMI2_CONTENTS2	0x0CA8	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 2
HDMI TX Controller_PKT_GHDMI2_CONTENTS3	0x0CAC	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 3
HDMI TX Controller_PKT_GHDMI2_CONTENTS4	0x0CB0	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 4
HDMI TX Controller_PKT_GHDMI2_CONTENTS5	0x0CB4	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 5
HDMI TX Controller_PKT_GHDMI2_CONTENTS6	0x0CB8	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 6
HDMI TX Controller_PKT_GHDMI2_CONTENTS7	0x0CBC	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 7
HDMI TX Controller_PKT_EMP_CONFIG0	0x0CE0	W	0x00000000	EMP Packetizer Config Register 0
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS0	0x0D00	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 0
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS1	0x0D04	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 1
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS2	0x0D08	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 2
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS3	0x0D0C	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 3

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS4	0x0D10	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 4
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS5	0x0D14	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 5
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS6	0x0D18	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 6
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS7	0x0D1C	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 7
HDMI TX Controller_AUDPKT_CONTROL0	0x0E20	W	0x00000000	Audio Packetizer Control Register 0
HDMI TX Controller_AUDPKT_CONTROL1	0x0E24	W	0x00000000	Audio Packetizer Control Register 1
HDMI TX Controller_AUDPKT_ACR_CONTROL0	0x0E40	W	0x00000000	Audio Packetizer ACR Control Register 0
HDMI TX Controller_AUDPKT_ACR_CONTROL1	0x0E44	W	0x00000000	Audio Packetizer ACR Control Register 1
HDMI TX Controller_AUDPKT_ACR_STATUS0	0x0E4C	W	0x00000000	Audio Packetizer ACR Status Register 0
HDMI TX Controller_AUDPKT_CHSTATUS_OVR0	0x0E60	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 0
HDMI TX Controller_AUDPKT_CHSTATUS_OVR1	0x0E64	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 1
HDMI TX Controller_AUDPKT_CHSTATUS_OVR2	0x0E68	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 2
HDMI TX Controller_AUDPKT_CHSTATUS_OVR3	0x0E6C	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 3
HDMI TX Controller_AUDPKT_CHSTATUS_OVR4	0x0E70	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 4
HDMI TX Controller_AUDPKT_CHSTATUS_OVR5	0x0E74	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 5
HDMI TX Controller_AUDPKT_CHSTATUS_OVR6	0x0E78	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 6
HDMI TX Controller_AUDPKT_CHSTATUS_OVR7	0x0E7C	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 7
HDMI TX Controller_AUDPKT_CHSTATUS_OVR8	0x0E80	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 8

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC0	0x0EA0	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 0
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC1	0x0EA4	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 1
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC2	0x0EA8	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 2
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC3	0x0EAC	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 3
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC4	0x0EB0	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 4
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC5	0x0EB4	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 5
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC6	0x0EB8	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 6
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC7	0x0EBC	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 7
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC8	0x0EC0	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 8
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC9	0x0EC4	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 9
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC10	0x0EC8	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 10
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC11	0x0ECC	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 11
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC12	0x0ED0	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 12

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC13	0x0ED4	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 13
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC14	0x0ED8	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 14
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC15	0x0EDC	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 15
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC16	0x0EE0	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 16
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC17	0x0EE4	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 17
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC18	0x0EE8	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 18
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC19	0x0EEC	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 19
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC20	0x0EF0	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 20
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC21	0x0EF4	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 21
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC22	0x0EF8	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 22
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC23	0x0EFC	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 23
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC24	0x0F00	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 24
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC25	0x0F04	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 25

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC26	0x0F08	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 26
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC27	0x0F0C	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 27
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC28	0x0F10	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 28
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC29	0x0F14	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 29
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC30	0x0F18	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 30
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC31	0x0F1C	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 31
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC32	0x0F20	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 32
HDMI TX Controller_AUDPKT_VBIT_OVR0	0x0F24	W	0x00000000	Audio Packetizer - Validity Bit Override Register 0
HDMI TX Controller_CEC_TX_CONTROL	0x1000	W	0x00000000	CEC Transmit Control Register
HDMI TX Controller_CEC_STATUS	0x1004	W	0x00000000	CEC Status Register
HDMI TX Controller_CEC_CONFIG	0x1008	W	0x00000110	CEC Configuration Register
HDMI TX Controller_CEC_ADDR	0x100C	W	0x00000000	CEC Logical Address Register
HDMI TX Controller_CEC_TX_COUNT	0x1020	W	0x00000000	CEC Transmitter Buffer Counter Register
HDMI TX Controller_CEC_TX_DATA3_0	0x1024	W	0x00000000	CEC Byte 0-3 Transmitter Data Buffer Register
HDMI TX Controller_CEC_TX_DATA7_4	0x1028	W	0x00000000	CEC Byte 4-7 Transmitter Data Buffer Register
HDMI TX Controller_CEC_TX_DATA11_8	0x102C	W	0x00000000	CEC Byte 8-11 Transmitter Data Buffer Register

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_CEC_TX_DATA_15_12	0x1030	W	0x00000000	CEC Byte 12-15 Transmitter Data Buffer Register
HDMI TX Controller_CEC_RX_COUNT_STATUS	0x1040	W	0x00000000	CEC Receiver Buffer Counter and Lock Status Register
HDMI TX Controller_CEC_RX_DATA_3_0	0x1044	W	0x00000000	CEC Byte 0-3 Receiver Data Buffer Register
HDMI TX Controller_CEC_RX_DATA_7_4	0x1048	W	0x00000000	CEC Byte 4-7 Receiver Data Buffer Register
HDMI TX Controller_CEC_RX_DATA_11_8	0x104C	W	0x00000000	CEC Byte 8-11 Receiver Data Buffer Register
HDMI TX Controller_CEC_RX_DATA_15_12	0x1050	W	0x00000000	CEC Byte 12-15 Receiver Data Buffer Register
HDMI TX Controller_CEC_LOCK_CONTROL	0x1054	W	0x00000000	CEC Lock Control Register
HDMI TX Controller_CEC_RXQUAL_BITTIME_CONFIG	0x1060	W	0x00033333	CEC RX Bit Qualifier Timings
HDMI TX Controller_CEC_RX_BITTIME_CONFIG	0x1064	W	0x00333333	CEC RX Bit Qualifier Timings
HDMI TX Controller_CEC_TX_BITTIME_CONFIG	0x1068	W	0x63444444	CEC TX Bit Qualifier Timings
HDMI TX Controller_MAIN_INTVEC_INDEX	0x3000	W	0x00000000	Main Unit Interrupt Vector Table Register
HDMI TX Controller_MAINUNIT_0_INT_STATUS	0x3010	W	0x00000000	Main Unit 0 Interrupt Status Register
HDMI TX Controller_MAINUNIT_0_INT_MASK_N	0x3014	W	0x80000000	Main Unit 0 Interrupt Mask Register
HDMI TX Controller_MAINUNIT_0_INT_CLEAR	0x3018	W	0x00000000	Main Unit 0 Interrupt Clear Register
HDMI TX Controller_MAINUNIT_0_INT_FORCE	0x301C	W	0x00000000	Main Unit 0 Interrupt Force Register
HDMI TX Controller_MAINUNIT_1_INT_STATUS	0x3020	W	0x00000000	Main Unit 1 Interrupt Status Register
HDMI TX Controller_MAINUNIT_1_INT_MASK_N	0x3024	W	0x00000000	Main Unit 1 Interrupt Mask Register
HDMI TX Controller_MAINUNIT_1_INT_CLEAR	0x3028	W	0x00000000	Main Unit 1 Interrupt Clear Register

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_MAINUNIT_1_INT_FORCE	0x302C	W	0x00000000	Main Unit 1 Interrupt Force Register
HDMI TX Controller_AVP_INTVEC_INDEX	0x3800	W	0x00000000	AVP Interrupt Vector Table Register
HDMI TX Controller_AVP_0_INT_STATUS	0x3810	W	0x00000000	AVPUNIT 0 Interrupt Status Register
HDMI TX Controller_AVP_0_INT_MASK_N	0x3814	W	0x00000000	AVPUNIT 0 Interrupt Mask Register
HDMI TX Controller_AVP_0_INT_CLEAR	0x3818	W	0x00000000	AVPUNIT 0 Interrupt Clear Register
HDMI TX Controller_AVP_0_INT_FORCE	0x381C	W	0x00000000	AVPUNIT 0 Interrupt Force Register
HDMI TX Controller_AVP_1_INT_STATUS	0x3820	W	0x00000000	AVPUNIT 1 Interrupt Status Register
HDMI TX Controller_AVP_1_INT_MASK_N	0x3824	W	0x00000000	AVPUNIT 1 Interrupt Mask Register
HDMI TX Controller_AVP_1_INT_CLEAR	0x3828	W	0x00000000	AVPUNIT 1 Interrupt Clear Register
HDMI TX Controller_AVP_1_INT_FORCE	0x382C	W	0x00000000	AVPUNIT 1 Interrupt Force Register
HDMI TX Controller_AVP_2_INT_STATUS	0x3830	W	0x00000000	AVPUNIT 2 Interrupt Status Register
HDMI TX Controller_AVP_2_INT_MASK_N	0x3834	W	0x00000000	AVPUNIT 2 Interrupt Mask Register
HDMI TX Controller_AVP_2_INT_CLEAR	0x3838	W	0x00000000	AVPUNIT 2 Interrupt Clear Register
HDMI TX Controller_AVP_2_INT_FORCE	0x383C	W	0x00000000	AVPUNIT 2 Interrupt Force Register
HDMI TX Controller_AVP_3_INT_STATUS	0x3840	W	0x00000000	AVPUNIT 3 Interrupt Status Register
HDMI TX Controller_AVP_3_INT_MASK_N	0x3844	W	0x00000000	AVPUNIT 3 Interrupt Mask Register
HDMI TX Controller_AVP_3_INT_CLEAR	0x3848	W	0x00000000	AVPUNIT 3 Interrupt Clear Register
HDMI TX Controller_AVP_3_INT_FORCE	0x384C	W	0x00000000	AVPUNIT 3 Interrupt Force Register

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Name	Offset	Size	Reset Value	Description
HDMI TX Controller_AVP_4_INT_STATUS	0x3850	W	0x00000000	AVPUNIT 4 Interrupt Status Register
HDMI TX Controller_AVP_4_INT_MASK_N	0x3854	W	0x00000000	AVPUNIT 4 Interrupt Mask Register
HDMI TX Controller_AVP_4_INT_CLEAR	0x3858	W	0x00000000	AVPUNIT 4 Interrupt Clear Register
HDMI TX Controller_AVP_4_INT_FORCE	0x385C	W	0x00000000	AVPUNIT 4 Interrupt Force Register
HDMI TX Controller_AVP_5_INT_STATUS	0x3860	W	0x00000000	AVPUNIT 5 Interrupt Status Register
HDMI TX Controller_AVP_5_INT_MASK_N	0x3864	W	0x00000000	AVPUNIT 5 Interrupt Mask Register
HDMI TX Controller_AVP_5_INT_CLEAR	0x3868	W	0x00000000	AVPUNIT 5 Interrupt Clear Register
HDMI TX Controller_AVP_5_INT_FORCE	0x386C	W	0x00000000	AVPUNIT 5 Interrupt Force Register
HDMI TX Controller_AVP_6_INT_STATUS	0x3870	W	0x00000000	AVPUNIT 6 Interrupt Status Register
HDMI TX Controller_AVP_6_INT_MASK_N	0x3874	W	0x00000000	AVPUNIT 6 Interrupt Mask Register
HDMI TX Controller_AVP_6_INT_CLEAR	0x3878	W	0x00000000	AVPUNIT 6 Interrupt Clear Register
HDMI TX Controller_AVP_6_INT_FORCE	0x387C	W	0x00000000	AVPUNIT 6 Interrupt Force Register
HDMI TX Controller_CEC_INT_STATUS	0x4000	W	0x00000000	CEC Interrupt Status Register
HDMI TX Controller_CEC_INT_MASK_N	0x4004	W	0x00000000	CEC Interrupt Mask Register
HDMI TX Controller_CEC_INT_CLEAR	0x4008	W	0x00000000	CEC Interrupt Clear Register
HDMI TX Controller_CEC_INT_FORCE	0x400C	W	0x00000000	CEC Interrupt Force Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

24.4.3 Detail Registers Description

HDMI TX Controller_CORE_ID

Address: Operational Base(0x27DA0000) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:24	RO	0x48	CORE_ID_ASCII3 ASCII encoded value of the first character of the IP identification code. Values: 0x48 (ASCII_H): H ASCII Character Value After Reset:0x48
23:16	RO	0x51	CORE_ID_ASCII2 ASCII encoded value of the second character of the IP identification code. Values: 0x51 (ASCII_Q): Q ASCII Character Value After Reset:0x51
15:8	RO	0x54	CORE_ID_ASCII1 ASCII encoded value of the third character of the IP identification code. Values: 0x54 (ASCII_T): T ASCII Character Value After Reset:0x54
7:0	RO	0x58	CORE_ID_ASCII0 ASCII encoded value of the fourth character of the IP identification code. Values: 0x58 (ASCII_X): X ASCII Character Value After Reset:0x58

HDMI TX Controller_VER_NUMBER

Address: Operational Base(0x27DA0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x30	VER_NUMBER_ASCII3 ASCII encoded value of the first character of the IP version. Value After Reset:0x30
23:16	RO	0x31	VER_NUMBER_ASCII2 ASCII encoded value of the second character of the IP version. Value After Reset:0x31
15:8	RO	0x30	VER_NUMBER_ASCII1 ASCII encoded value of the third character of the IP version. Value After Reset:0x30
7:0	RO	0x30	VER_NUMBER_ASCII0 ASCII encoded value of the fourth character of the IP version. Value After Reset:0x30

HDMI TX Controller_VER_TYPE

Address: Operational Base(0x27DA0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x6c	VER_TYPE_ASCII3 ASCII encoded value of the first character of the IP release type. Value After Reset:0x6c
23:16	RO	0x75	VER_TYPE_ASCII2 ASCII encoded value of the second character of the IP release type. Value After Reset:0x75
15:8	RO	0x30	VER_TYPE_ASCII1 ASCII encoded value of the third character of the IP release type. Value After Reset:0x30

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Bit	Attr	Reset Value	Description
7:0	RO	0x30	VER_TYPE_ASCII0 ASCII encoded value of the fourth character of the IP release type. Value After Reset:0x30

HDMI TX Controller_CONFIG_REG

Address: Operational Base(0x27DA0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved5 Reserved Field:Yes
28	RO	0x1	CEC The CEC interface is present in the generated controller RTL. Value After Reset:0x1
27:25	RW	0x0	Reserved4 Reserved Field:Yes
24	RO	0x1	ARCRX Enhanced Audio Return Channel (ARC) RX interface is present in the generated controller RTL. Value After Reset:0x1
23	RO	0x1	AUD_UD Support for IEC 60958 User Data channel is present in the generated controller RTL. Value After Reset:0x1
22	RO	0x1	AUD_MS Support for Multi-Stream Audio is present in the generated controller RTL. Value After Reset:0x1
21	RO	0x1	AUD_HBR Support for High Bit Rate Audio is present in the generated controller RTL. Value After Reset:0x1
20	RO	0x0	AUD_3D Support for 3D Audio is present in the generated controller RTL. Value After Reset:0x0
19:16	RW	0x0	Reserved3 Reserved Field:Yes
15	RO	0x1	CVTEM Support for Compressed Video Timing Extended Metadata (CVTEM) Packets is present in the generated controller RTL. Value After Reset:0x1
14	RO	0x1	VTEM Support for Video Timing Extended Metadata (VTEM) Packets is present in the generated controller RTL. Value After Reset:0x1
13	RO	0x0	EEMP Support for External Extended Metadata Packets (EEMP) is present in the generated controller RTL. Value After Reset:0x0
12	RO	0x1	FRL The Fixed Rate Link (FRL) feature is present in the generated controller RTL. Value After Reset:0x1
11	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
10	RO	0x1	HDCP14_SW_SHA1CALC The hardware for the SHA-1 calculation for HDCP 1.4 Protocol is not present in the generated controller RTL and the software calculates the SHA-1. Value After Reset:0x1
9	RO	0x0	HDCP14_DKSET_EXTERNAL The Device Key Set from the HDCP 1.4 Protocol is stored in the external memory. Value After Reset:0x0
8	RO	0x1	HDCP14 Support for HDCP1.4 Encryption is present in the generated controller RTL. Value After Reset:0x1
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	RO	0x0	PR Support for Pixel Repetition is present in the generated controller RTL. Value After Reset:0x0
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RO	0x1	AVP The HDMI TX Audio, Video, and Packet (AVP) processing is present in the generated controller RTL. Value After Reset:0x1

HDMI TX Controller_CORE_TIMESTAMP_HHMM

Address: Operational Base(0x27DA0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RO	0x31	CORE_TIMESTAMP_HHMM_ASCII3 ASCII value of the tens digit of the hour. Values: 0x30 (TENS_OF_HOURS_0): 0 is the tens digit of the hours 0x31 (TENS_OF_HOURS_1): 1 is the tens digit of the hours 0x32 (TENS_OF_HOURS_2): 2 is the tens digit of the hours Value After Reset:0x31
23:16	RO	0x37	CORE_TIMESTAMP_HHMM_ASCII2 ASCII value of the units digit of the hour. Values: 0x30 (HOUR_0): 0 is the units digit of the hours 0x31 (HOUR_1): 1 is the units digit of the hours 0x32 (HOUR_2): 2 is the units digit of the hours 0x33 (HOUR_3): 3 is the units digit of the hours 0x34 (HOUR_4): 4 is the units digit of the hours 0x35 (HOUR_5): 5 is the units digit of the hours 0x36 (HOUR_6): 6 is the units digit of the hours 0x37 (HOUR_7): 7 is the units digit of the hours 0x38 (HOUR_8): 8 is the units digit of the hours 0x39 (HOUR_9): 9 is the units digit of the hours Value After Reset:0x37

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Bit	Attr	Reset Value	Description
15:8	RO	0x33	CORE_TIMESTAMP_HHMM_ASCII1 ASCII value of the tens digit of the minute. Values: 0x30 (TENS_OF_MINUTES_0): 0 is the tens digit of the minutes 0x31 (TENS_OF_MINUTES_1): 1 is the tens digit of the minutes 0x32 (TENS_OF_MINUTES_2): 2 is the tens digit of the minutes 0x33 (TENS_OF_MINUTES_3): 3 is the tens digit of the minutes 0x34 (TENS_OF_MINUTES_4): 4 is the tens digit of the minutes 0x35 (TENS_OF_MINUTES_5): 5 is the tens digit of the minutes Value After Reset:0x33
7:0	RO	0x36	CORE_TIMESTAMP_HHMM_ASCII0 ASCII value of the units digit of the minute. Values: 0x30 (MINUTE_0): 0 is the units digit of the minutes 0x31 (MINUTE_1): 1 is the units digit of the minutes 0x32 (MINUTE_2): 2 is the units digit of the minutes 0x33 (MINUTE_3): 3 is the units digit of the minutes 0x34 (MINUTE_4): 4 is the units digit of the minutes 0x35 (MINUTE_5): 5 is the units digit of the minutes 0x36 (MINUTE_6): 6 is the units digit of the minutes 0x37 (MINUTE_7): 7 is the units digit of the minutes 0x38 (MINUTE_8): 8 is the units digit of the minutes 0x39 (MINUTE_9): 9 is the units digit of the minutes Value After Reset:0x36

HDMI TX Controller_CORE_TIMESTAMP_MMDD

Address: Operational Base(0x27DA0000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x3033	CORE_TIMESTAMP_MM ASCII value of the month (in numerical format) Values: 0x3031 (MONTH_01): Month 1 of the year 0x3032 (MONTH_02): Month 2 of the year 0x3033 (MONTH_03): Month 3 of the year 0x3034 (MONTH_04): Month 4 of the year 0x3035 (MONTH_05): Month 5 of the year 0x3036 (MONTH_06): Month 6 of the year 0x3037 (MONTH_07): Month 7 of the year 0x3038 (MONTH_08): Month 8 of the year 0x3039 (MONTH_09): Month 9 of the year 0x3130 (MONTH_10): Month 10 of the year 0x3131 (MONTH_11): Month 11 of the year 0x3132 (MONTH_12): Month 12 of the year Value After Reset:0x3036

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Bit	Attr	Reset Value	Description
15:0	RO	0x3131	CORE_TIMESTAMP_DD ASCII value of the day Values: 0x3031 (DAY_01): Day 1 of the month 0x3032 (DAY_02): Day 2 of the month 0x3033 (DAY_03): Day 3 of the month 0x3034 (DAY_04): Day 4 of the month 0x3035 (DAY_05): Day 5 of the month 0x3036 (DAY_06): Day 6 of the month 0x3037 (DAY_07): Day 7 of the month 0x3038 (DAY_08): Day 8 of the month 0x3039 (DAY_09): Day 9 of the month 0x3130 (DAY_10): Day 10 of the month 0x3131 (DAY_11): Day 11 of the month 0x3132 (DAY_12): Day 12 of the month 0x3133 (DAY_13): Day 13 of the month 0x3134 (DAY_14): Day 14 of the month 0x3135 (DAY_15): Day 15 of the month 0x3136 (DAY_16): Day 16 of the month 0x3137 (DAY_17): Day 17 of the month 0x3138 (DAY_18): Day 18 of the month 0x3139 (DAY_19): Day 19 of the month 0x3230 (DAY_20): Day 20 of the month 0x3231 (DAY_21): Day 21 of the month 0x3232 (DAY_22): Day 22 of the month 0x3233 (DAY_23): Day 23 of the month 0x3234 (DAY_24): Day 24 of the month 0x3235 (DAY_25): Day 25 of the month 0x3236 (DAY_26): Day 26 of the month 0x3237 (DAY_27): Day 27 of the month 0x3238 (DAY_28): Day 28 of the month 0x3239 (DAY_29): Day 29 of the month 0x3330 (DAY_30): Day 30 of the month 0x3331 (DAY_31): Day 31 of the month Value After Reset:0x3136

HDMI TX Controller_CORE_TIMESTAMP_YYYY

Address: Operational Base(0x27DA0000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x32	CORE_TIMESTAMP_YYYY_ASCII3 ASCII value of the thousands digit of the year Values: 0x31 (YEAR_THOUSANDS_1): 1 is the thousands digit of the year 0x32 (YEAR_THOUSANDS_2): 2 is the thousands digit of the year Value After Reset:0x32
23:16	RO	0x30	CORE_TIMESTAMP_YYYY_ASCII2 ASCII value of the hundreds digit of the year Values: 0x30 (YEAR_HUNDREDS_0): 0 is the hundreds digit of the year 0x39 (YEAR_HUNDREDS_9): 9 is the hundreds digit of the year Value After Reset:0x30

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Bit	Attr	Reset Value	Description
15:8	RO	0x32	CORE_TIMESTAMP_YYYY_ASCII1 ASCII value of the tens digit of the year Values: 0x30 (YEAR_TENS_0): 0 is the tens digit of the year 0x31 (YEAR_TENS_1): 1 is the tens digit of the year 0x32 (YEAR_TENS_2): 2 is the tens digit of the year 0x33 (YEAR_TENS_3): 3 is the tens digit of the year 0x34 (YEAR_TENS_4): 4 is the tens digit of the year 0x35 (YEAR_TENS_5): 5 is the tens digit of the year 0x36 (YEAR_TENS_6): 6 is the tens digit of the year 0x37 (YEAR_TENS_7): 7 is the tens digit of the year 0x38 (YEAR_TENS_8): 8 is the tens digit of the year 0x39 (YEAR_TENS_9): 9 is the tens digit of the year Value After Reset:0x32
7:0	RO	0x31	CORE_TIMESTAMP_YYYY_ASCII0 ASCII value of the units digit of the year. Values: 0x30 (YEAR_UNITS_0): 0 is the units digit of the year 0x31 (YEAR_UNITS_1): 1 is the units digit of the year 0x32 (YEAR_UNITS_2): 2 is the units digit of the year 0x33 (YEAR_UNITS_3): 3 is the units digit of the year 0x34 (YEAR_UNITS_4): 4 is the units digit of the year 0x35 (YEAR_UNITS_5): 5 is the units digit of the year 0x36 (YEAR_UNITS_6): 6 is the units digit of the year 0x37 (YEAR_UNITS_7): 7 is the units digit of the year 0x38 (YEAR_UNITS_8): 8 is the units digit of the year 0x39 (YEAR_UNITS_9): 9 is the units digit of the year Value After Reset:0x31

HDMI TX Controller_GLOBAL_SWRESET_REQUEST

Address: Operational Base(0x27DA0000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved3 Reserved Field:Yes
27	WO	0x0	ARCRX_CMDC_SWINIT_P Reset control field that when activated resets the CMDC controller in the ARCRX functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
26	WO	0x0	ARCRX_DMAC_SWINIT_P Reset control field that when activated resets the DMAC controller in the ARCRX functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0

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Bit	Attr	Reset Value	Description
25	WO	0x0	ARCRX_SWINIT_P Reset control field that when activated resets the ARCRX functional unit, including all configuration and status bits. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
24:19	RW	0x00	Reserved2 Reserved Field:Yes
18	WO	0x0	CEC_CTRL_SWINIT_P Reset control field that when activated resets the controller in the CEC functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
17	WO	0x0	CEC_SWINIT_P Reset control field that when activated resets the CEC functional unit, including all configuration and status bits. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
16	WO	0x0	I2C_SWINIT_P Reset control field that when activated resets the I2C Master in the MAIN functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
15:12	RW	0x0	Reserved1 Reserved Field:Yes
11	WO	0x0	AVP_DATAPATH_PACKET_METADATA_SWINIT_P Reset control field that when activated resets the Extended Metadata Packets data path of the AVP functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
10	WO	0x0	AVP_DATAPATH_PACKET_AUDIO_SWINIT_P Reset control field that when activated resets the audio data path of the AVP functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0

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Bit	Attr	Reset Value	Description
9	WO	0x0	AVP_DATAPATH_PACKET_SWINIT_P Reset control field that when activated resets the packet data path of the AVP functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
8	WO	0x0	AVP_DATAPATH_HDCP_KEYS_SWINIT_P Reset control field that when activated resets the HDCP keys used in the data path of the AVP functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
7	WO	0x0	AVP_DATAPATH_VIDEO_SWINIT_P Reset control field that when activated resets the video data path of the AVP functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
6	WO	0x0	AVP_DATAPATH_SWINIT_P Reset control field that when activated resets the data path of the AVP functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
5	WO	0x0	AVP_SWINIT_P Reset control field that when activated resets the AVP functional unit, including all configuration and status bits. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
4:2	RW	0x0	Reserved0 Reserved Field:Yes
1	WO	0x0	MASTER_NOMAINRB_SWINIT_P Main reset control field that when activated resets all functional units. Also resets all configuration and status bits except those that are part of the MAIN unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0

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Bit	Attr	Reset Value	Description
0	WO	0x0	MASTER_SWINIT_P Main reset control field that when activated resets all functional units and all configuration registers. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0

HDMI TX Controller_GLOBAL_SWDISABLE

Address: Operational Base(0x27DA0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved3 Reserved Field:Yes
26	RW	0x0	ARCRX_CTRL_SWDISABLE Disable control field that when activated disables the controllers in the ARCRX functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_ARCRX_CTRL): disable affected units Value After Reset:0x0
25	RW	0x0	ARCRX_SWDISABLE Disable control field that when activated disables the ARCRX functional unit. Also reset all contained configuration and status bits. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_ARCRX): disable affected units Value After Reset:0x0
24:19	RW	0x00	Reserved2 Reserved Field:Yes
18	RW	0x0	CEC_CTRL_SWDISABLE Disable control field that when activated disables the controller in the CEC functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_CEC_CTRL): disable affected units Value After Reset:0x0
17	RW	0x0	CEC_SWDISABLE Disable control field that when activated disables the CEC functional unit. Also reset all contained configuration and status bits. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_CEC): disable affected units Value After Reset:0x0
16	RW	0x0	I2C_SWDISABLE Disable control field that when activated disables the I2C Master in the MAIN functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_I2C): disable affected units Value After Reset:0x0
15:12	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
11	RW	0x0	AVP_DATAPATH_PACKET_METADATA_SWDISABLE Disable control field that when activated disables the Extended Metadata Packet data path of the AVP functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP_DATAPATH_PACKET_METADATA): disable affected units Value After Reset:0x0
10	RW	0x0	AVP_DATAPATH_PACKET_AUDIO_SWDISABLE Disable control field that when activated disables the audio data path of the AVP functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP_DATAPATH_PACKET_AUDIO): disable affected units Value After Reset:0x0
9	RW	0x0	AVP_DATAPATH_PACKET_SWDISABLE Disable control field that when activated disables the packet data path of the AVP functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP_DATAPATH_PACKET): disable affected units Value After Reset:0x0
8	RW	0x0	AVP_DATAPATH_TMDS_SWDISABLE Disable control field that when activated disables the TMDS data path of the AVP functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP_DATAPATH_TMDS): disable affected units Value After Reset:0x0
7	RW	0x0	AVP_DATAPATH_FRL_SWDISABLE Disable control field that when activated disables the FRL data path of the AVP functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP_DATAPATH_FRL): disable affected units Value After Reset:0x0
6	RW	0x0	AVP_DATAPATH_VIDEO_SWDISABLE Disable control field that when activated disables the video data path of the AVP functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP_DATAPATH_VIDEO): disable affected units Value After Reset:0x0
5	RW	0x0	AVP_DATAPATH_SWDISABLE Disable control field that when activated disables the data path of the AVP functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP_DATAPATH): disable affected units Value After Reset:0x0

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Bit	Attr	Reset Value	Description
4	RW	0x0	AVP_SWDISABLE Disable control field that when activated disables the AVP functional unit. Also reset all contained configuration and status bits. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP): disable affected units Value After Reset:0x0
3:0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller_RESET_MANAGER_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes
12	RW	0x0	RESET_MANAGER_ARC_BPCLK_OVR_VALUE Influence of ARC_bpclk in Reset Manager Override Value. Values: 0x0 (CLK_OFF): Indicates that ARC_bpclk is in a OFF state. The Reset Manager does not overlap other domains with the ARC_bpclk. 0x1 (CLK_ON): Indicates that ARC_bpclk is in a ON state. The Reset Manager overlaps other domains with the ARC_bpclk. Value After Reset:0x0
11	RW	0x0	RESET_MANAGER_AUDCLK_OVR_VALUE Influence of audclk in Reset Manager Override Value. Values: 0x0 (CLK_OFF): Indicates that audclk is in a OFF state. The Reset Manager does not overlap other domains with the audclk. 0x1 (CLK_ON): Indicates that audclk is in a ON state. The Reset Manager overlaps other domains with the audclk. Value After Reset:0x0
10	RW	0x0	RESET_MANAGER_LINKQPCLK_OVR_VALUE Influence of linkqpclk in Reset Manager Override Value. Values: 0x0 (CLK_OFF): Indicates that linkqpclk is in a OFF state. The Reset Manager does not overlap other domains with the linkqpclk. 0x1 (CLK_ON): Indicates that linkqpclk is in a ON state. The Reset Manager overlaps other domains with the linkqpclk. Value After Reset:0x0
9	RW	0x0	RESET_MANAGER_VIDQPCLK_OVR_VALUE Influence of vidqpclk in Reset Manager Override Value. Values: 0x0 (CLK_OFF): Indicates that vidqpclk is in a OFF state. The Reset Manager does not overlap other domains with the vidqpclk. 0x1 (CLK_ON): Indicates that vidqpclk is in a ON state. The Reset Manager overlaps other domains with the vidqpclk. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
8	RW	0x0	RESET_MANAGER_IPI_CLK_OVR_VALUE Influence of ipi_clk in Reset Manager Override Value. Values: 0x0 (CLK_OFF): Indicates that ipi_clk is in a OFF state. The Reset Manager does not overlap other domains with the ipi_clk. 0x1 (CLK_ON): Indicates that ipi_clk is in a ON state. The Reset Manager overlaps other domains with the ipi_clk. Value After Reset:0x0
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4	RW	0x0	RESET_MANAGER_ARC_BPCLK_OVR_EN Influence of ARC_bpclk in Reset Manager Override Enable. Values: 0x0 (OVERRIDE_DISABLE): Override Disable. Value of cmu_status.ARC_bpclk_off_st used. 0x1 (OVERRIDE_ENABLE): Override Enable. Value of reset_manager_config0.reset_manager_ARC_bpclk_value used. Value After Reset:0x0
3	RW	0x0	RESET_MANAGER_AUDCLK_OVR_EN Influence of audclk in Reset Manager Override Enable. Values: 0x0 (OVERRIDE_DISABLE): Override Disable. Value of cmu_status.audclk_off_st used. 0x1 (OVERRIDE_ENABLE): Override Enable. Value of reset_manager_config0.reset_manager_audclk_value used. Value After Reset:0x0
2	RW	0x0	RESET_MANAGER_LINKQPCLK_OVR_EN Influence of linkqpclk in Reset Manager Override Enable. Values: 0x0 (OVERRIDE_DISABLE): Override Disable. Value of cmu_status.linkqpclk_off_st used. 0x1 (OVERRIDE_ENABLE): Override Enable. Value of reset_manager_config0.reset_manager_linkqpclk_value used. Value After Reset:0x0
1	RW	0x0	RESET_MANAGER_VIDQPCLK_OVR_EN Influence of vidqpclkclk in Reset Manager Override Enable. Values: 0x0 (OVERRIDE_DISABLE): Override Disable. Value of cmu_status.vidqpclkclk_off_st used. 0x1 (OVERRIDE_ENABLE): Override Enable. Value of reset_manager_config0.reset_manager_vidqpclk_value used. Value After Reset:0x0
0	RW	0x0	RESET_MANAGER_IPI_CLK_OVR_EN Influence of ipi_clk in Reset Manager Override Enable. Values: 0x0 (OVERRIDE_DISABLE): Override Disable. Value of cmu_status.ipi_clk_off_st used. 0x1 (OVERRIDE_ENABLE): Override Enable. Value of reset_manager_config0.reset_manager_ipi_clk_value used. Value After Reset:0x0

HDMI TX Controller_RESET_MANAGER_STATUS0

Address: Operational Base(0x27DA0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
29	RO	0x0	AVP_DATAPATH_VIDEO_AUDCLK_STATUS Status of the Video Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
28	RO	0x0	AVP_DATAPATH_VIDEO_LINKQPCLK_STATUS Status of the Video Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
27	RO	0x0	AVP_DATAPATH_VIDEO_VIDQPCLK_STATUS Status of the Video Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
26	RO	0x0	AVP_DATAPATH_VIDEO_IPI_CLK_STATUS Status of the Video Functional Group Init at ipi_clk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
25	RO	0x0	AVP_DATAPATH_VIDEO_REFCLK_STATUS Status of the Video Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
24	RO	0x0	AVP_DATAPATH_AUDCLK_STATUS Status of the DATAPATH Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
23	RO	0x0	AVP_DATAPATH_LINKQPCLK_STATUS Status of the DATAPATH Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
22	RO	0x0	AVP_DATAPATH_VIDQPCLK_STATUS Status of the DATAPATH Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
21	RO	0x0	AVP_DATAPATH_IPI_CLK_STATUS Status of the DATAPATH Functional Group Init at ipi_clk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
20	RO	0x0	AVP_DATAPATH_REFCLK_STATUS Status of the DATAPATH Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
19	RO	0x0	AVP_APB_PCLK_STATUS Status of the AVP Functional Group Init at apb_pclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
18	RO	0x0	AVP_AUDCLK_STATUS Status of the AVP Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
17	RO	0x0	AVP_LINKQPCLK_STATUS Status of the AVP Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
16	RO	0x0	AVP_VIDQPCLK_STATUS Status of the AVP Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
15	RO	0x0	AVP_IPI_CLK_STATUS Status of the AVP Functional Group Init at ipi_clk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
14	RO	0x0	AVP_REFCLK_STATUS Status of the AVP Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
13	RO	0x0	MASTER_NOMAINRB_APB_PCLK_STATUS Status of the MASTER_NOMAINRB Functional Group Init at apb_pclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
12	RO	0x0	MASTER_NOMAINRB_ARC_BPCLK_STATUS Status of the MASTER_NOMAINRB Functional Group Init at ARC_bpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
11	RO	0x0	MASTER_NOMAINRB_AUDCLK_STATUS Status of the MASTER_NOMAINRB Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
10	RO	0x0	MASTER_NOMAINRB_LINKQPCLK_STATUS Status of the MASTER_NOMAINRB Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
9	RO	0x0	MASTER_NOMAINRB_VIDQPCLK_STATUS Status of the MASTER_NOMAINRB Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
8	RO	0x0	MASTER_NOMAINRB_IPI_CLK_STATUS Status of the MASTER_NOMAINRB Functional Group Init at ipi_pclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
7	RO	0x0	MASTER_NOMAINRB_REFCLK_STATUS Status of the MASTER_NOMAINRB Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
6	RO	0x0	MASTER_APB_PCLK_STATUS Status of the MASTER Functional Group Init at apb_pclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
5	RO	0x0	MASTER_ARC_BPCLK_STATUS Status of the MASTER Functional Group Init at ARC_bpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
4	RO	0x0	MASTER_AUDCLK_STATUS Status of the MASTER Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
3	RO	0x0	MASTER_LINKQPCLK_STATUS Status of the MASTER Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
2	RO	0x0	MASTER_VIDQPCLK_STATUS Status of the MASTER Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
1	RO	0x0	MASTER_IPI_CLK_STATUS Status of the MASTER Functional Group Init at ipi_clk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
0	RO	0x0	MASTER_REFCLK_STATUS Status of the MASTER Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

HDMI TX Controller_RESET_MANAGER_STATUS1

Address: Operational Base(0x27DA0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved0 Reserved Field:Yes
28	RO	0x0	APB_REFCLK_STATUS Status of the APB Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
27	RO	0x0	APB_ARC_BPCLK_STATUS Status of the APB Functional Group Init at ARC_bpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
26	RO	0x0	APB_AUDCLK_STATUS Status of the APB Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
25	RO	0x0	APB_LINKQPCLK_STATUS Status of the APB Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
24	RO	0x0	APB_VIDQPCLK_STATUS Status of the APB Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
23	RO	0x0	APB_IPI_CLK_STATUS Status of the APB Functional Group Init at ipi_clk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
22	RO	0x0	APB_APB_PCLK_STATUS Status of the APB Functional Group Init at apb_pclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
21	RO	0x0	ARCRX_CMDC_REFCLK_STATUS Status of the ARCRX_CMDC Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
20	RO	0x0	ARCRX_DMAC_ARC_BPCLK_STATUS Status of the ARCRX_DMAC Functional Group Init at ARC_bpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
19	RO	0x0	ARCRX_CTRL_REFCLK_STATUS Status of the ARCRX_CTRL Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
18	RO	0x0	ARCRX_CTRL_ARC_BPCLK_STATUS Status of the ARCRX_CTRL Functional Group Init at ARC_bpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
17	RO	0x0	ARCRX_APB_PCLK_STATUS Status of the ARCRX Functional Group Init at apb_pclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
16	RO	0x0	ARCRX_REFCLK_STATUS Status of the ARCRX Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
15	RO	0x0	ARCRX_ARC_BPCLK_STATUS Status of the ARCRX Functional Group Init at ARC_bpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
14	RO	0x0	CEC_CTRL_REFCLK_STATUS Status of the CEC_CTRL Functional Group Init at refclk: Values: 0x0 (ASSERT): Init_n is asserted. 0x1 (NOT_ASSERT): Init_n is not asserted. Value After Reset:0x0
13	RO	0x0	CEC_REFCLK_STATUS Status of the CEC Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
12	RO	0x0	I2C_LINKQPCLK_STATUS Status of the I2C Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
11	RO	0x0	I2C_REFCLK_STATUS Status of the I2C Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
10	RO	0x0	AVP_DATAPATH_PACKET_METADATA_VIDQPCLK_STATUS Status of the METADATA Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
9	RO	0x0	AVP_DATAPATH_PACKET_AUDIO_VIDQPCLK_STATUS Status of the AUDIO Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
8	RO	0x0	AVP_DATAPATH_PACKET_AUDIO_AUDCLK_STATUS Status of the AUDIO Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
7	RO	0x0	AVP_DATAPATH_PACKET_LINKQPCLK_STATUS Status of the PACKET Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
6	RO	0x0	AVP_DATAPATH_PACKET_AUDCLK_STATUS Status of the PACKET Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
5	RO	0x0	AVP_DATAPATH_PACKET_VIDQPCLK_STATUS Status of the PACKET Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
4	RO	0x0	AVP_DATAPATH_HDCP_LINKQPCLK_STATUS Status of the HDCP Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
3	RO	0x0	AVP_DATAPATH_TMDS_LINKQPCLK_STATUS Status of the TMDS Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
2	RO	0x0	AVP_DATAPATH_TMDS_VIDQPCLK_STATUS Status of the TMDS Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
1	RO	0x0	AVP_DATAPATH_FRL_LINKQPCLK_STATUS Status of the FRL Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
0	RO	0x0	AVP_DATAPATH_FRL_VIDQPCLK_STATUS Status of the FRL Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

HDMI TX Controller_RESET_MANAGER_STATUS2

Address: Operational Base(0x27DA0000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved0 Reserved Field:Yes
4	RO	0x0	RESET_MANAGER_ARC_BPCLK_ON_STATUS Influence of ARC_bpclk in Reset Manager: Values: 0x0 (CLK_OFF): The ARC_bpclk is not used in Reset Manager. The logic at ARC_bpclk is not affected by any init_n/disable. 0x1 (CLK_ON): The ARC_bpclk is used in Reset Manager overlap function. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
3	RO	0x0	RESET_MANAGER_AUDCLK_ON_STATUS Influence of audclk in Reset Manager: Values: 0x0 (CLK_OFF): The audclk is not used in Reset Manager. The logic at audclk is not affected by any init_n/disable. 0x1 (CLK_ON): The audclk is used in Reset Manager overlap function. Value After Reset:0x0
2	RO	0x0	RESET_MANAGER_LINKQPCLK_ON_STATUS Influence of linkqpclk in Reset Manager: Values: 0x0 (CLK_OFF): The linkqpclk is not used in Reset Manager. The logic at linkqpclk is not affected by any init_n/disable. 0x1 (CLK_ON): The linkqpclk is used in Reset Manager overlap function. Value After Reset:0x0
1	RO	0x0	RESET_MANAGER_VIDQPCLK_ON_STATUS Influence of vidqpclk in Reset Manager: Values: 0x0 (CLK_OFF): The vidqpclk is not used in Reset Manager. The logic at vidqpclk is not affected by any init_n/disable. 0x1 (CLK_ON): The vidqpclk is used in Reset Manager overlap function. Value After Reset:0x0
0	RO	0x0	RESET_MANAGER_IPI_CLK_ON_STATUS Influence of ipi_clk in Reset Manager: Values: 0x0 (CLK_OFF): The ipi_clk is not used in Reset Manager. The logic at ipi_clk is not affected by any init_n/disable. 0x1 (CLK_ON): The ipi_clk is used in Reset Manager overlap function. Value After Reset:0x0

HDMI TX Controller_TIMER_BASE_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved0 Reserved Field:Yes
28:0	RW	0x179a7b00	TIMER_REFERENCE_BASE Timer Reference Base, this represents the number of irefclk cycles in 1 second. This is the frequency of the refclk. Attention: This register is always consistent with input irefclk clock frequency. Example of configured value for irefclk of 396.0000 MHz is 29'd396000000. Value After Reset:0x179A7B00

HDMI TX Controller_TIMER_BASE_STATUS0

Address: Operational Base(0x27DA0000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
0	RO	0x0	TIMER_BASE_LOCKED_ST Timer base locked status flag. Note: Writing a new Timer Reference Base to the register global_timer_ref_base initiates new Timer Base calculations. While these are in progress, this status is expected to fall momentaneously and when the calculations are finally done it is expected to rise, together with corresponding interrupt request timer_base_locked_irq. Values: 0x0 (NOT_LOCKED): Timer Base calculations in progress and not locked. 0x1 (LOCKED): Timer Base calculations completed and locked. Value After Reset:0x0

HDMI TX Controller_I2CM_SM_SCL_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x085e	I2CM_SM_SCL_HIGH_CNT I2C Master Standard-mode SCL High Control Value After Reset:0x85e
15:0	RW	0x085e	I2CM_SM_SCL_LOW_CNT I2C Master Standard-mode SCL Low Control Value After Reset:0x85e

HDMI TX Controller_I2CM_FM_SCL_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0217	I2CM_FM_SCL_HIGH_CNT I2C Master Fast-mode SCL High Control Value After Reset:0x217
15:0	RW	0x0217	I2CM_FM_SCL_LOW_CNT I2C Master Fast-mode SCL Low Control Value After Reset:0x217

HDMI TX Controller_I2CM_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved1 Reserved Field:Yes
15:8	RW	0x00	I2CM_SDA_HOLD I2C Master SDA hold time Value After Reset:0x0
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x00	I2CM_RXFILTER_PULSE_WIDTH I2C Master Rx filter pulse width Value After Reset:0x0

HDMI TX Controller_I2CM_CONTROL0

Address: Operational Base(0x27DA0000) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
0	WO	0x0	I2CM_BUS_CLEAR_P I2C Master Bus Clear Value After Reset:0x0

HDMI TX Controller_I2CM_STATUS0

Address: Operational Base(0x27DA0000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x0	I2CM_ARB_LOST I2C Master arbitration lost Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_CONTROL0

Address: Operational Base(0x27DA0000) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:20	RW	0x0	I2CM_NBYTES I2C Master Interface number of bytes minus 1 to read/write: Values: 0x0 (BYTES1): 1 byte to read/write 0x1 (BYTES2): 2 bytes to read/write 0x2 (BYTES3): 3 bytes to read/write 0x3 (BYTES4): 4 bytes to read/write 0x4 (BYTES5): 5 bytes to read/write 0x5 (BYTES6): 6 bytes to read/write 0x6 (BYTES7): 7 bytes to read/write 0x7 (BYTES8): 8 bytes to read/write 0x8 (BYTES9): 9 bytes to read/write 0x9 (BYTES10): 10 bytes to read/write 0xa (BYTES11): 11 bytes to read/write 0xb (BYTES12): 12 bytes to read/write 0xc (BYTES13): 13 bytes to read/write 0xd (BYTES14): 14 bytes to read/write 0xe (BYTES15): 15 bytes to read/write 0xf (BYTES16): 16 bytes to read/write Value After Reset:0x0
19:12	RW	0x00	I2CM_ADDR I2C Master Interface read/write address Value After Reset:0x0
11:5	RW	0x00	I2CM_SLVADDR I2C Master Interface slave address Value After Reset:0x0
4	RW	0x0	I2CM_EXT_READ I2C Master Interface extended read operation Value After Reset:0x0
3	RW	0x0	I2CM_SHORT_READ I2C Master Interface short read operation Value After Reset:0x0
2	RW	0x0	I2CM_READ I2C Master Interface read operation Value After Reset:0x0

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Bit	Attr	Reset Value	Description
1	RW	0x0	I2CM_WRITE I2C Master Interface write operation Value After Reset:0x0
0	RW	0x0	I2CM_FM_EN I2C Master Interface Fast-mode enable Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_CONTROL1

Address: Operational Base(0x27DA0000) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved0 Reserved Field:Yes
14:7	RW	0x00	I2CM_SEG_PTR I2C Master Interface extended read access segment pointer Value After Reset:0x0
6:0	RW	0x00	I2CM_SEG_ADDR I2C Master Interface extended read access segment address Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_WRDATA_0_3

Address: Operational Base(0x27DA0000) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	I2CM_WRDATA_3 I2C Master Interface SW write data, byte 3 Value After Reset:0x0
23:16	RW	0x00	I2CM_WRDATA_2 I2C Master Interface SW write data, byte 2 Value After Reset:0x0
15:8	RW	0x00	I2CM_WRDATA_1 I2C Master Interface SW write data, byte 1 Value After Reset:0x0
7:0	RW	0x00	I2CM_WRDATA_0 I2C Master Interface SW write data, byte 0 Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_WRDATA_4_7

Address: Operational Base(0x27DA0000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	I2CM_WRDATA_7 I2C Master Interface SW write data, byte 7 Value After Reset:0x0
23:16	RW	0x00	I2CM_WRDATA_6 I2C Master Interface SW write data, byte 6 Value After Reset:0x0
15:8	RW	0x00	I2CM_WRDATA_5 I2C Master Interface SW write data, byte 5 Value After Reset:0x0
7:0	RW	0x00	I2CM_WRDATA_4 I2C Master Interface SW write data, byte 4 Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_WRDATA_8_11

Address: Operational Base(0x27DA0000) + offset (0x0104)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	I2CM_WRDATA_11 I2C Master Interface SW write data, byte 11 Value After Reset:0x0
23:16	RW	0x00	I2CM_WRDATA_10 I2C Master Interface SW write data, byte 10 Value After Reset:0x0
15:8	RW	0x00	I2CM_WRDATA_9 I2C Master Interface SW write data, byte 9 Value After Reset:0x0
7:0	RW	0x00	I2CM_WRDATA_8 I2C Master Interface SW write data, byte 8 Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_WRDATA_12_15

Address: Operational Base(0x27DA0000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	I2CM_WRDATA_15 I2C Master Interface SW write data, byte 15 Value After Reset:0x0
23:16	RW	0x00	I2CM_WRDATA_14 I2C Master Interface SW write data, byte 14 Value After Reset:0x0
15:8	RW	0x00	I2CM_WRDATA_13 I2C Master Interface SW write data, byte 13 Value After Reset:0x0
7:0	RW	0x00	I2CM_WRDATA_12 I2C Master Interface SW write data, byte 12 Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_RDDATA_0_3

Address: Operational Base(0x27DA0000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	I2CM_RDDATA_3 I2C Master Interface SW read data, byte 3 Value After Reset:0x0
23:16	RO	0x00	I2CM_RDDATA_2 I2C Master Interface SW read data, byte 2 Value After Reset:0x0
15:8	RO	0x00	I2CM_RDDATA_1 I2C Master Interface SW read data, byte 1 Value After Reset:0x0
7:0	RO	0x00	I2CM_RDDATA_0 I2C Master Interface SW read data, byte 0 Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_RDDATA_4_7

Address: Operational Base(0x27DA0000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	I2CM_RDDATA_7 I2C Master Interface SW read data, byte 7 Value After Reset:0x0
23:16	RO	0x00	I2CM_RDDATA_6 I2C Master Interface SW read data, byte 6 Value After Reset:0x0

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	I2CM_RDDATA_5 I2C Master Interface SW read data, byte 5 Value After Reset:0x0
7:0	RO	0x00	I2CM_RDDATA_4 I2C Master Interface SW read data, byte 4 Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_RDDATA_8_11

Address: Operational Base(0x27DA0000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	I2CM_RDDATA_11 I2C Master Interface SW read data, byte 11 Value After Reset:0x0
23:16	RO	0x00	I2CM_RDDATA_10 I2C Master Interface SW read data, byte 10 Value After Reset:0x0
15:8	RO	0x00	I2CM_RDDATA_9 I2C Master Interface SW read data, byte 9 Value After Reset:0x0
7:0	RO	0x00	I2CM_RDDATA_8 I2C Master Interface SW read data, byte 8 Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_RDDATA_12_15

Address: Operational Base(0x27DA0000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	I2CM_RDDATA_15 I2C Master Interface SW read data, byte 15 Value After Reset:0x0
23:16	RO	0x00	I2CM_RDDATA_14 I2C Master Interface SW read data, byte 14 Value After Reset:0x0
15:8	RO	0x00	I2CM_RDDATA_13 I2C Master Interface SW read data, byte 13 Value After Reset:0x0
7:0	RO	0x00	I2CM_RDDATA_12 I2C Master Interface SW read data, byte 12 Value After Reset:0x0

HDMI TX Controller_SCDC_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved2 Reserved Field:Yes
12	RW	0x0	SCDC_I2C_FM_EN SCDC I2C Fast-mode enable Value After Reset:0x0
11:8	RW	0x0	Reserved1 Reserved Field:Yes
7	RW	0x1	SCDC_UPD_FLAGS_RD_CLR_NBYTES SCDC Update Flags number of bytes minus 1 to read/clear: Values: 0x0 (BYTES1): 1 byte to read/clear 0x1 (BYTES2): 2 bytes to read/clear Value After Reset:0x1

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Bit	Attr	Reset Value	Description
6	RW	0x0	SCDC_UPD_FLAGS_AUTO_CLR SCDC Update Flags auto clear on read Value After Reset:0x0
5	RW	0x0	SCDC_UPD_FLAGS_POLL_CONT SCDC Update Flags Polling continuously Value After Reset:0x0
4	RW	0x0	SCDC_UPD_FLAGS_POLL_EN SCDC Update Flags Polling enable Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RW	0x0	SCDC_RR_REPLY_STOP SCDC Read Request reply with STOP Value After Reset:0x0
0	RW	0x0	SCDC_RR_EN SCDC Read Request enable Value After Reset:0x0

HDMI TX Controller_SCDC_CONTROL0

Address: Operational Base(0x27DA0000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	WO	0x0	SCDC_UPD_FLAGS_CLR_P SCDC Update Flags clear request Value After Reset:0x0
0	WO	0x0	SCDC_UPD_FLAGS_RD_P SCDC Update Flags read request Value After Reset:0x0

HDMI TX Controller_SCDC_STATUS0

Address: Operational Base(0x27DA0000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15:8	RO	0x00	SCDC_UPD_FLAGS_1 SCDC Update Flags 1 Value After Reset:0x0
7:0	RO	0x00	SCDC_UPD_FLAGS_0 SCDC Update Flags 0 Value After Reset:0x0

HDMI TX Controller_FLT_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved1 Reserved Field:Yes
8	RW	0x0	FLT_NO_TIMEOUT FRL Link Training FLT_no_timeout Source Test Configuration Register Value After Reset:0x0
7:4	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	FLT_FFE_LEVELS FRL Link Training FFE Levels Value After Reset:0x0

HDMI TX Controller_FLT_CONFIG1

Address: Operational Base(0x27DA0000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes
19:16	RW	0x0	FLT_LTP_LANE3_OVR_VALUE Link Training Pattern to apply on Lane 3 override value Value After Reset:0x0
15:12	RW	0x0	FLT_LTP_LANE2_OVR_VALUE Link Training Pattern to apply on Lane 2 override value Value After Reset:0x0
11:8	RW	0x0	FLT_LTP_LANE1_OVR_VALUE Link Training Pattern to apply on Lane 1 override value Value After Reset:0x0
7:4	RW	0x0	FLT_LTP_LANE0_OVR_VALUE Link Training Pattern to apply on Lane 0 override value Value After Reset:0x0
3	RW	0x0	FLT_LTP_LANE3_OVR_EN Link Training Pattern to apply on Lane 3 override enable Value After Reset:0x0
2	RW	0x0	FLT_LTP_LANE2_OVR_EN Link Training Pattern to apply on Lane 2 override enable Value After Reset:0x0
1	RW	0x0	FLT_LTP_LANE1_OVR_EN Link Training Pattern to apply on Lane 1 override enable Value After Reset:0x0
0	RW	0x0	FLT_LTP_LANE0_OVR_EN Link Training Pattern to apply on Lane 0 override enable Value After Reset:0x0

HDMI TX Controller_FLT_CONFIG2

Address: Operational Base(0x27DA0000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes
19:16	RW	0x0	FLT_TXFFE_LANE3_OVR_VALUE Link Training TxFFE setting to apply on Lane 3 override value Value After Reset:0x0
15:12	RW	0x0	FLT_TXFFE_LANE2_OVR_VALUE Link Training TxFFE setting to apply on Lane 2 override value Value After Reset:0x0
11:8	RW	0x0	FLT_TXFFE_LANE1_OVR_VALUE Link Training TxFFE setting to apply on Lane 1 override value Value After Reset:0x0
7:4	RW	0x0	FLT_TXFFE_LANE0_OVR_VALUE Link Training TxFFE setting to apply on Lane 0 override value Value After Reset:0x0
3	RW	0x0	FLT_TXFFE_LANE3_OVR_EN Link Training TxFFE setting to apply on Lane 3 override enable Value After Reset:0x0

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Bit	Attr	Reset Value	Description
2	RW	0x0	FLT_TXFFE_LANE2_OVR_EN Link Training TxFFE setting to apply on Lane 2 override enable Value After Reset:0x0
1	RW	0x0	FLT_TXFFE_LANE1_OVR_EN Link Training TxFFE setting to apply on Lane 1 override enable Value After Reset:0x0
0	RW	0x0	FLT_TXFFE_LANE0_OVR_EN Link Training TxFFE setting to apply on Lane 0 override enable Value After Reset:0x0

HDMI TX Controller_FLT_CONTROL0

Address: Operational Base(0x27DA0000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	FLT_START_P FRL Link Training LTS:3 start Value After Reset:0x0

HDMI TX Controller_MAINUNIT_STATUS0

Address: Operational Base(0x27DA0000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x0	ARC_BPCLK_VALID_STABLE_ST ARC RX Biphase clock valid change interrupt status. Value After Reset:0x0

HDMI TX Controller_VIDEO_INTERFACE_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved0 Reserved Field:Yes
28	RW	0x0	VESA_DSC_48BITS_OVR_VALUE VESA DSC 48bits override value Value After Reset:0x0
27	RW	0x0	VESA_DSC_24BITS_OVR_VALUE VESA DSC 24bits override value Value After Reset:0x0
26:24	RW	0x0	HDMI_VIDEO_FORMAT_OVR_VALUE Video Format override value Value After Reset:0x0
23:20	RW	0x0	HDMI_COLOR_DEPTH_OVR_VALUE Color depth override value Value After Reset:0x0
19	RW	0x0	IPI_MAP_ENDIANNESS_OVR_VALUE Bit endianness of each mapped byte Values: 0x0 (LITTLE_ENDIAN): little-endian 0x1 (BIG_ENDIAN): big-endian Value After Reset:0x0
18:16	RW	0x0	IPI_MAP_BYTE5_OVR_VALUE Internal video vector where IPI byte 5 is mapped Value After Reset:0x0

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Bit	Attr	Reset Value	Description
15:13	RW	0x0	IPI_MAP_BYTE4_OVR_VALUE Internal video vector where IPI byte 4 is mapped Value After Reset:0x0
12:10	RW	0x0	IPI_MAP_BYTE3_OVR_VALUE Internal video vector where IPI byte 3 is mapped Value After Reset:0x0
9:7	RW	0x0	IPI_MAP_BYTE2_OVR_VALUE Internal video vector where IPI byte 2 is mapped Value After Reset:0x0
6:4	RW	0x0	IPI_MAP_BYTE1_OVR_VALUE Internal video vector where IPI byte 1 is mapped Value After Reset:0x0
3:1	RW	0x0	IPI_MAP_BYTE0_OVR_VALUE Internal video vector where IPI byte 0 is mapped Value After Reset:0x0
0	RW	0x0	IPI_MAP_OVR_EN IPI mapping override mechanism enable Values: 0x0 (OVERRIDE_OFF): No override mechanism 0x1 (OVERRIDE_ON): Override mechanism enabled Value After Reset:0x0

HDMI TX Controller_VIDEO_INTERFACE_CONFIG2

Address: Operational Base(0x27DA0000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved1 Reserved Field:Yes
4	RW	0x0	IPI_DESERIALIZER_EN IPI Deserializer configuration Values: 0x0 (DISABLE): IPI Data received in 4 buses (deserialization disabled) 0x1 (ENABLE): IPI Data Serialized and received only in interface 0 Value After Reset:0x0
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	VID_FIFO_INIT_ON_OVF Video Interface FIFO Init on overflow configuration Value After Reset:0x0

HDMI TX Controller_VIDEO_INTERFACE_CONTROL0

Address: Operational Base(0x27DA0000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	VID_FIFO_CLR_P Video Interface FIFO clear Value After Reset:0x0

HDMI TX Controller_VIDEO_INTERFACE_STATUS0

Address: Operational Base(0x27DA0000) + offset (0x0814)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
18	RO	0x0	HSYNC_POLARITY Detected Hsync polarity status Values: 0x0 (HSYNC_NEG): Hsync pulse is active low 0x1 (HSYNC_POS): Hsync pulse is active high Value After Reset:0x0
17	RO	0x0	VSYNC_POLARITY Detected Vsync polarity status Values: 0x0 (VSYNC_NEG): Vsync pulse is active low 0x1 (VSYNC_POS): Vsync pulse is active high Value After Reset:0x0
16	RO	0x0	VESA_DSC_48BIT VESA DSC 48bit video mode Values: 0x0 (VESADSC48_NOT): VESA DSC 48bit video mode not in use 0x1 (VESADSC48_DET): VESA DSC 48bit video mode detected Value After Reset:0x0
15	RO	0x0	VESA_DSC_24BIT VESA DSC 24bit video mode Values: 0x0 (VESADSC24_NOT): VESA DSC 24bit video mode not in use 0x1 (VESADSC24_DET): VESA DSC 24bit video mode detected Value After Reset:0x0
14:12	RO	0x0	HDMI_VIDEO_FORMAT Video Format status Value After Reset:0x0
11:8	RO	0x0	HDMI_COLOR_DEPTH Color depth in use in HDMI Value After Reset:0x0
7:4	RO	0x0	IPI_COLOR_DEPTH Detected IPI color depth Value After Reset:0x0
3:0	RO	0x0	IPI_FORMAT IPI format Value After Reset:0x0

HDMI TX Controller_VIDEO_PACKING_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x081C)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	GCP_DEFAULT_PHASE GCP Default_Phase selector (only applicable for 30bits or 36 bits) Values: 0x0 (DP0): Default Phase 0 0x1 (DP1): Default Phase 1 Value After Reset:0x0

HDMI TX Controller_AUDIO_INTERFACE_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved4 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
28	RW	0x0	PAI_DISABLE_SAMPLE_PRESENT_LEFT PAI interface disable automatic sample present assertion for left-only channels Values: 0x0 (SP_PAI_LEFT_EN): Sample present is asserted for PAI Interface when left-only channel is received 0x1 (SP_PAI_LEFT_DIS): Sample present is not asserted for PAI Interface when left-only channel is received Value After Reset:0x0
27	RW	0x0	PAI_FORMAT_OVR_EN PAI interface format override enable Values: 0x0 (PAI_FRMT_OVR_DIS): PAI interface input audio format is used 0x1 (PAI_FRMT_OVR_EN): PAI interface input audio format is overriden to follow the value of 'aud_format' field Value After Reset:0x0
26:24	RW	0x0	AUD_FORMAT Audio Format: Values: 0x0 (AUD_ASP): Audio Sample (L-PCM and IEC 61937 compressed formats) 0x1 (AUD_OBA): One Bit Audio Sample Packet 0x2 (AUD_DST): DST Audio Packet 0x3 (AUD_HBR): High Bitrate (HBR) Audio Stream Packet (IEC 61937) - only valid when the configuration parameter HDMI_QP_TX_AUD_HBR is set 0x4 (AUD_MSASP): Multi-Stream Audio Sample Packet (L-PCM and IEC 61937 compressed formats) - only valid when the configuration parameter HDMI_QP_TX_AUD_MS is set 0x5 (AUD_MSOBA): One-Bit Multi-Stream Audio Sample Packet - only valid when the configuration parameter HDMI_QP_TX_AUD_MS is set 0x6 (AUD_3DASP): 3D Audio Sample Packet (L-PCM format only) - only valid when the configuration parameter HDMI_QP_TX_AUD_3D is set 0x7 (AUD_3DOBA): One Bit 3D Audio Sample Packet - only valid when the configuration parameter HDMI_QP_TX_AUD_3D is set Value After Reset:0x0
23:22	RW	0x0	Reserved3 Reserved Field:Yes
21:20	RW	0x0	SPDIF_PAIR_SEL SPDIF interface pair used to sample data Value After Reset:0x0
19:16	RW	0x0	SPDIF_LINES_EN SPDIF interface lines enable. Value After Reset:0x0
15:14	RW	0x0	Reserved2 Reserved Field:Yes
13	RW	0x0	I2S_BBIT_RIGHT I2S interface B bit selection Values: 0x0 (BBIT_L): B bit taken from left channel 0x1 (BBIT_R): B bit taken from right channel Value After Reset:0x0

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Bit	Attr	Reset Value	Description
12	RW	0x0	I2S_BPCUV_EN I2S interface BPCUV insertion enable Values: 0x0 (BPCUV_RCV_DIS): BPCUV bits not received through the interface 0x1 (BPCUV_RCV_EN): BPCUV bits received through the interface Value After Reset:0x0
11:8	RW	0x0	Reserved1 Reserved Field:Yes
7:4	RW	0x0	I2S_LINES_EN I2S interface lines enable. Value After Reset:0x0
3	RW	0x0	Reserved0 Reserved Field:Yes
2	RW	0x0	AUDFIFO_INIT_ON_OVF Audio FIFO init on overflow Value After Reset:0x0
1:0	RW	0x0	AUD_IF_SEL Audio Interface selection Note 1: Others values not listed default to 0 Values: 0x0 (PAI): PAI interface selection 0x1 (I2S): I2S interface selection 0x2 (SPDIF): SPDIF interface selection Value After Reset:0x0

HDMI TX Controller_AUDIO_INTERFACE_CONFIG1

Address: Operational Base(0x27DA0000) + offset (0x0824)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved1 Reserved Field:Yes
28	RW	0x0	PAI_CHANNELSPREAD_THRESHOLD_OVR_EN PAI Interface channel spread threshold override enable Values: 0x0 (PAI_CHTHR_OVR_DIS): Uses PAI interface threshold configuration 0x1 (PAI_CHTHR_OVR_EN): Channel Spread Threshold override enabled, value from 'pai_channelspread_threshold_ovr_value' is used Value After Reset:0x0
27:20	RW	0x00	PAI_CHANNELSPREAD_THRESHOLD_OVR_VALUE PAI Interface channel threshold value override Value After Reset:0x0
19	RW	0x0	PAI_CHANNELSPREAD_DETECTED_OVR_EN PAI Interface channel spread detection override enable Values: 0x0 (PAI_CHSPREAD_OVR_DIS): Channel spread detected by PAI interface 0x1 (PAI_CHSPREAD_OVR_EN): Channel spread override enabled, value from 'pai_channelspread_detected_ovr_value' is used Value After Reset:0x0

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Bit	Attr	Reset Value	Description
18	RW	0x0	PAI_CHANNELSPREAD_DETECTED_OVR_VALUE PAI Interface channel spread detection override Values: 0x0 (PAI_CHSPREAD_DIS): Channel spread disabled 0x1 (PAI_CHSPREAD_EN): Channel spread enabled Value After Reset:0x0
17	RW	0x0	Reserved0 Reserved Field:Yes
16	RW	0x0	PAI_PAIR_LAYOUT_OVR_EN PAI Interface pair layout override enable Values: 0x0 (PAI_PAIR_LAY_OVR_DIS): Pair layout determined by received pairs 0x1 (PAI_PAIR_LAY_OVR_EN): Pair layout override enabled, value from 'pai_pair_layout_ovr_value' is used Value After Reset:0x0
15:0	RW	0x0000	PAI_PAIR_LAYOUT_OVR_VALUE PAI Interface pair layout override Value After Reset:0x0

HDMI TX Controller_AUDIO_INTERFACE_CONTROL0

Address: Operational Base(0x27DA0000) + offset (0x082C)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	AUDFIFO_CLR_P Audio FIFO clear Value After Reset:0x0

HDMI TX Controller_AUDIO_INTERFACE_STATUS0

Address: Operational Base(0x27DA0000) + offset (0x0834)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23	RO	0x0	SPDIF_LINE3_LOCK S/PDIF Line 3 audio lock Values: 0x0 (SPDIF_LINE3_AUD_NOK): Lane not receiving audio correctly 0x1 (SPDIF_LINE3_AUD_OK): Lane receiving audio correctly Value After Reset:0x0
22	RO	0x0	SPDIF_LINE2_LOCK S/PDIF Line 2 audio lock Values: 0x0 (SPDIF_LINE2_AUD_NOK): Lane not receiving audio correctly 0x1 (SPDIF_LINE2_AUD_OK): Lane receiving audio correctly Value After Reset:0x0
21	RO	0x0	SPDIF_LINE1_LOCK S/PDIF Line 1 audio lock Values: 0x0 (SPDIF_LINE1_AUD_NOK): Lane not receiving audio correctly 0x1 (SPDIF_LINE1_AUD_OK): Lane receiving audio correctly Value After Reset:0x0

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Bit	Attr	Reset Value	Description
20	RO	0x0	SPDIF_LINE0_LOCK S/PDIF Line 0 audio lock Values: 0x0 (SPDIF_LINE0_AUD_NOK): Lane not receiving audio correctly 0x1 (SPDIF_LINE0_AUD_OK): Lane receiving audio correctly Value After Reset:0x0
19	RO	0x0	PAI_CHANNELSPREAD_DETECTED PAI channel spread detection: Values: 0x0 (PAI_CHSPREAD_DET_DIS): Channel spread disabled 0x1 (PAI_CHSPREAD_DET_EN): Channel spread enabled Value After Reset:0x0
18:16	RO	0x0	PAI_FORMAT PAI format status: Values: 0x0 (AUDPKT_TYPE_0X02): Audio sample 0x1 (AUDPKT_TYPE_0X07): One bit audio 0x2 (AUDPKT_TYPE_0X08): DST audio 0x3 (AUDPKT_TYPE_0X09): HBR audio (only valid when the configuration parameter HDMI_QP_TX_AUD_HBR is set) 0x4 (AUDPKT_TYPE_0X0e): MSA audio (only valid when the configuration parameter HDMI_QP_TX_AUD_MS is set) 0x5 (AUDPKT_TYPE_0X0f): OBM audio (only valid when the configuration parameter HDMI_QP_TX_AUD_MS is set) 0x6 (AUDPKT_TYPE_0X0b): 3D audio sample (only valid when the configuration parameter HDMI_QP_TX_AUD_3D is set) 0x7 (AUDPKT_TYPE_0X0c): 3D One bit audio (only valid when the configuration parameter HDMI_QP_TX_AUD_3D is set) Value After Reset:0x0
15:0	RO	0x0000	PAIR_LAYOUT Audio pair layout status Note: This register field only takes values greater than 15 when Audio 3D features are present in the configuration (HDMI_QP_TX_AUD_3D == 1) Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0840)

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Bit	Attr	Reset Value	Description
31:28	RW	0x4	EXTCTL_SPACING_SEL Maximum spacing between Extended Control Periods, set in ms. Note: The HDMI specification defines a maximum spacing (tEXTS,max_delay) of 50ms between Extended Control Periods. Values: 0x0 (ECP5ms): 5ms 0x1 (ECP10ms): 10ms 0x2 (ECP15ms): 15ms 0x3 (ECP20ms): 20ms 0x4 (ECP25ms): 25ms 0x5 (ECP30ms): 30ms 0x6 (ECP35ms): 35ms 0x7 (ECP40ms): 40ms 0x8 (ECP42ms): 42ms 0x9 (ECP45ms): 45ms 0xa (ECP46ms): 46ms 0xb (ECP47ms): 47ms 0xc (ECP48ms): 48ms 0xd (ECP49ms): 49ms 0xe (ECP50ms): 50ms 0xf (ECP55ms): 55ms Value After Reset:0x4
27	RW	0x0	Reserved2 Reserved Field:Yes
26:20	RW	0x20	EXTCTL_DURATION Extended Control Period duration, set in TMDS clock cycles (nominal pixels) This field can be set from 0 (disabled) to 127 clock cycles. Note: The HDMI specification defines a minimum (tEXTS,min) of 32 clock cycles for Extended Control Period duration. Value After Reset:0x20
19:6	RW	0x0000	Reserved1 Reserved Field:Yes
5:4	RW	0x0	MTW_FREQ_CFG Metadata Transmission Window - MTW Frequency configuration Values: 0x0 (MTW_FRAME): MTW is repeated every Frame 0x1 (MTW_FIELD): MTW is repeated every Field 0x2 (MTW_VBLANK): MTW is repeated every Vertical Blanking 0x3 (MTW_RES): Reserved Value After Reset:0x0

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Bit	Attr	Reset Value	Description
3	RW	0x0	VIDEO_MEAS_OVR_EN Video Measures Override enable The following fields are used when the override mode is enabled: video_hfront_ovr_value video_hsyncwidth_ovr_value video_hback_ovr_value video_hblank_ovr_value video_hactive_ovr_value video_htotal_ovr_value video_vfront_ovr_value video_vsyncwidth_ovr_value video_vback_ovr_value video_vblank_ovr_value video_vactive_ovr_value video_vtotal_ovr_value Values: 0x0 (VIDMEAS_OVR_DIS): Video measures are performed by the internal Video Monitor block 0x1 (VIDMEAS_OVR_EN): Video measures are set by the fields video_*_ovr_value of registers frame_composer_config* Value After Reset:0x0
2	RW	0x0	SCRAMBLER_UCP_LINE Scrambler Unscrambled Control Period per line enable. This is a debug feature for testing proposes only. In normal operation it shall always be disabled. Values: 0x0 (NORMAL_UCP): Unscrambled Control Period per video field 0x1 (LINE_UCP): Unscrabled Control Period per line Value After Reset:0x0
1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	FAPA_START_LOCATION FAPA_start_location value from E-EDID HF-VSDB This field shall be set from SW when it reads the E-EDID from the Sink device, with the value of bit 'FAPA_start_location' in HF-VSDB byte 8, bit 0. The FAPA region is the only allowed frame region for transmission of EMP - Extended Metadata Packets belonging to a Data Set with Sync=1. Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONFIG1

Address: Operational Base(0x27DA0000) + offset (0x0844)

Bit	Attr	Reset Value	Description
31:20	RW	0xfff	MAX_PACKETS_BLANK Maximum number of Data Island packets in a non-active video line (video blanking line) - 0 : No packets are transmitted - 1 : Number of packets limited to 1 - ... - 4094 : Number of packets limited to 4094 - 4095 : Unlimited number of packets, when configured value has all bits set (=1) Value After Reset:0xfff
19:16	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
15:8	RW	0xff	MAX_PACKETS_ACTIVE Maximum number of Data Island packets in an active video line - 0 : No packets are transmitted - 1 : Number of packets limited to 1 - ... - 254 : Number of packets limited to 254 - 255 : Unlimited number of packets, when configured value has all bits set (=1) Value After Reset:0xff
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_FRAME_COMPOSER_CONFIG2

Address: Operational Base(0x27DA0000) + offset (0x0848)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VIDEO_HSYNCWIDTH_OVR_VALUE Video Hsync width override value Only used when video_meas_ovr_en=1 Value After Reset:0x0
15:0	RW	0x0000	VIDEO_HFRONT_OVR_VALUE Video Hfront override value Only used when video_meas_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONFIG3

Address: Operational Base(0x27DA0000) + offset (0x084C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VIDEO_HBLANK_OVR_VALUE Video Hblank override value Only used when video_meas_ovr_en=1 Value After Reset:0x0
15:0	RW	0x0000	VIDEO_HBACK_OVR_VALUE Video Hback override value Only used when video_meas_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONFIG4

Address: Operational Base(0x27DA0000) + offset (0x0850)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VIDEO_HTOTAL_OVR_VALUE Video Htotal override value Only used when video_meas_ovr_en=1 Value After Reset:0x0
15:0	RW	0x0000	VIDEO_HACTIVE_OVR_VALUE Video Hactive override value Only used when video_meas_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONFIG5

Address: Operational Base(0x27DA0000) + offset (0x0854)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VIDEO_VSYNCWIDTH_OVR_VALUE Video Vsync width override value Only used when video_meas_ovr_en=1 Value After Reset:0x0

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	VIDEO_VFRONT_OVR_VALUE Video Vfront override value Only used when video_meas_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONFIG6

Address: Operational Base(0x27DA0000) + offset (0x0858)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VIDEO_VBLANK_OVR_VALUE Video Vblank override value Only used when video_meas_ovr_en=1 Value After Reset:0x0
15:0	RW	0x0000	VIDEO_VBACK_OVR_VALUE Video Vback override value Only used when video_meas_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONFIG7

Address: Operational Base(0x27DA0000) + offset (0x085C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VIDEO_VTOTAL_OVR_VALUE Video Vtotal override value Only used when video_meas_ovr_en=1 Value After Reset:0x0
15:0	RW	0x0000	VIDEO_VACTIVE_OVR_VALUE Video Vactive override value Only used when video_meas_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONFIG8

Address: Operational Base(0x27DA0000) + offset (0x0860)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	Reserved0 Reserved Field:Yes
17:16	RW	0x1	KEEPOUT_WOO_CFG Configure when to enable the Keepout period for the HDCP Window of Opportunity. The start and end time for the keepout period are the same for all Enabled configurations. Note: When keepout_hdcp_authenticated_ovr_en=1, the HDCP Authenticated state is given by field keepout_hdcp_authenticated_ovr_val Values: 0x0 (KEEPOUT_WOO_DIS): Keepout period disabled. 0x1 (KEEPOUT_WOO_AUTH_FRL): Keepout period enabled when in FRL mode or HDCP is authenticated. 0x2 (KEEPOUT_WOO_ALWAYS): Keepout period always enabled. 0x3 (KEEPOUT_WOO_RSV): Reserved, don't use. Value After Reset:0x1
15:8	RW	0x00	KEEPOUT_WOO_END_MARGIN Keepout period for the HDCP Window of Opportunity - End margin The keepout period end shall be (650 + keepout_woo_end_margin) tribytes from the active edge of Vsync Value After Reset:0x0

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	KEEPOUT_WOO_START_MARGIN Keepout period for the HDCP Window of Opportunity - Start margin The keepout period start shall be (508 - keepout_woo_start_margin) tribytes from the active edge of Vsync Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONFIG9

Address: Operational Base(0x27DA0000) + offset (0x0864)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	Reserved0 Reserved Field:Yes
9:8	RW	0x1	KEEPOUT_REKEY_CFG Configure when to enable the Keepout period for the HDCP14 hdcpRekeyCipher operation. The start and end time for the keepout period are the same for all Enabled configurations. Note: When keepout_hdcp_authenticated_ovr_en=1, the HDCP Authenticated state is given by field keepout_hdcp_authenticated_ovr_val Values: 0x0 (KEEPOUT_REKEY_DIS): Keepout period disabled. 0x1 (KEEPOUT_REKEY_AUTH): Keepout period enabled when HDCP is authenticated. 0x2 (KEEPOUT_REKEY_ALWAYS): Keepout period always enabled. 0x3 (KEEPOUT_REKEY_RSV): Reserved, don't use. Value After Reset:0x1
7:0	RW	0x00	KEEPOUT_REKEY_END_MARGIN Keepout period for the HDCP14 hdcpRekeyCipher operation - End margin The keepout period end shall be (58 + keepout_rekey_end_margin) tribytes from the end of each active video period Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONTROL0

Address: Operational Base(0x27DA0000) + offset (0x086C)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	RW	0x0	KEEPOUT_HDCP_AUTH_OVR_VALUE Override Value for the HDCP authenticated state, used only for controlling Keepout periods Values: 0x0 (KEEPOUT_NOTAUTH): HDCP Not Authenticated 0x1 (KEEPOUT_AUTH): HDCP Authenticated Value After Reset:0x0
0	RW	0x0	KEEPOUT_HDCP_AUTH_OVR_EN Override Enable for the HDCP authenticated state, used only for controlling Keepout periods Values: 0x0 (KEEPOUT_AUTH_OVR_DIS): Disabled 0x1 (KEEPOUT_AUTH_OVR_EN): Enabled Value After Reset:0x0

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HDMI TX Controller_VIDEO_MONITOR_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0880)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	Reserved0 Reserved Field:Yes
9	RW	0x0	VMON_IRQ_VACTIVE_EN Video monitor interrupt on Vactive change enable Value After Reset:0x0
8	RW	0x0	VMON_IRQ_VBACK_EN Video monitor interrupt on Vback change enable Value After Reset:0x0
7	RW	0x0	VMON_IRQ_VSYNCWIDTH_EN Video monitor interrupt on Vsync width change enable Value After Reset:0x0
6	RW	0x0	VMON_IRQ_VFRONT_EN Video monitor interrupt on Vfront change enable Value After Reset:0x0
5	RW	0x0	VMON_IRQ_VTOTAL_EN Video monitor interrupt on Vtotal change enable Value After Reset:0x0
4	RW	0x0	VMON_IRQ_HACTIVE_EN Video monitor interrupt on Hactive change enable Value After Reset:0x0
3	RW	0x0	VMON_IRQ_HBACK_EN Video monitor interrupt on Hback change enable Value After Reset:0x0
2	RW	0x0	VMON_IRQ_HSYNCWIDTH_EN Video monitor interrupt on Hsync width change enable Value After Reset:0x0
1	RW	0x0	VMON_IRQ_HFRONT_EN Video monitor interrupt on Hfront change enable Value After Reset:0x0
0	RW	0x0	VMON_IRQ_HTOTAL_EN Video monitor interrupt on Htotal change enable Value After Reset:0x0

HDMI TX Controller_VIDEO_MONITOR_STATUS0

Address: Operational Base(0x27DA0000) + offset (0x0884)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	VMON_HSYNCWIDTH Video monitor measured Hsync width Value After Reset:0x0
15:0	RO	0x0000	VMON_HFRONT Video monitor measured Hfront Value After Reset:0x0

HDMI TX Controller_VIDEO_MONITOR_STATUS1

Address: Operational Base(0x27DA0000) + offset (0x0888)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	VMON_HBLANK Video monitor measured Hblank Value After Reset:0x0
15:0	RO	0x0000	VMON_HBACK Video monitor measured Hback Value After Reset:0x0

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HDMI TX Controller_VIDEO_MONITOR_STATUS2

Address: Operational Base(0x27DA0000) + offset (0x088C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	VMON_HTOTAL Video monitor measured Htotal Value After Reset:0x0
15:0	RO	0x0000	VMON_HACTIVE Video monitor measured Hactive Value After Reset:0x0

HDMI TX Controller_VIDEO_MONITOR_STATUS3

Address: Operational Base(0x27DA0000) + offset (0x0890)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	VMON_VSYNCWIDTH Video monitor measured Vsync width Value After Reset:0x0
15:0	RO	0x0000	VMON_VFRONT Video monitor measured Vfront Value After Reset:0x0

HDMI TX Controller_VIDEO_MONITOR_STATUS4

Address: Operational Base(0x27DA0000) + offset (0x0894)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	VMON_VBLANK Video monitor measured Vblank Value After Reset:0x0
15:0	RO	0x0000	VMON_VBACK Video monitor measured Vback Value After Reset:0x0

HDMI TX Controller_VIDEO_MONITOR_STATUS5

Address: Operational Base(0x27DA0000) + offset (0x0898)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	VMON_VTOTAL Video monitor measured Vtotal Value After Reset:0x0
15:0	RO	0x0000	VMON_VACTIVE Video monitor measured Vactive Value After Reset:0x0

HDMI TX Controller_VIDEO_MONITOR_STATUS6

Address: Operational Base(0x27DA0000) + offset (0x089C)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	RO	0x0	VMON_ILACE_DETECT Video Monitor - Interlaced Video mode detected Value After Reset:0x0
0	RO	0x0	VMON_ALT_DETECT Video Monitor - Field Alternative video mode detected Value After Reset:0x0

HDMI TX Controller_HDCP2LOGIC_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x08E0)

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Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved0 Reserved Field:Yes
4	RW	0x0	HDCP2_OPMODE_OVR_VALUE OPMODE Override Value Values: 0x0 (OPMODE_TMDS): The OPMODE indication is set to 1'b0, meaning the TMDS Mode. 0x1 (OPMODE_FRL): The AVMUTE indication is set to 1'b1, meaning the FRL Mode. Value After Reset:0x0
3	RW	0x0	HDCP2_OPMODE_OVR_EN OPMODE Override Enable Values: 0x0 (OVERRIDE_OFF): The OPMODE indication is defined internaly. 0x1 (OVERRIDE_ON): The OPMODE indication is overriden by the hdcp2_opmode_ovr_value field. Value After Reset:0x0
2	RW	0x0	HDCP2_AVMUTE_OVR_VALUE AVMUTE Override Value Values: 0x0 (AVMUTE_OFF): The AVMUTE indication is set to 1'b0. 0x1 (AVMUTE_ON): The AVMUTE indication is set to 1'b1. Value After Reset:0x0
1	RW	0x0	HDCP2_AVMUTE_OVR_EN AVMUTE Override Enable Values: 0x0 (OVERRIDE_OFF): The AVMUTE indication is defined internaly. 0x1 (OVERRIDE_ON): The AVMUTE indication is overriden by the hdcp2_avmute_ovr_value field. Value After Reset:0x0
0	RW	0x0	HDCP2_BYPASS Internal Bypass of HDCP2. Values: 0x0 (BYPASS_OFF): The video datapath goes through the External HDCP2 Module. 0x1 (BYPASS_ON): The video datapath bypasses the External HDCP2 Module. Value After Reset:0x0

HDMI TX Controller_HDCP2LOGIC_ESM_GPIO_IN

Address: Operational Base(0x27DA0000) + offset (0x08E4)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:4	RW	0x0	HDCP2_ESM_P0_GPIO_IN Port 0 General-Purpose inputs to the HDCP2 ESM block - For more information, see the ESM Databook. The bit mapping is equivalent to the ESM Databook definition. Value After Reset:0x0
3:0	RW	0x0	HDCP2_ESM_GLOBAL_GPIO_IN Global General-Purpose inputs to the HDCP2 ESM block - For more information, see the ESM Databook. The bit mapping is equivalent to the ESM Databook definition. Value After Reset:0x0

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HDMI TX Controller_HDCP2LOGIC_ESM_GPIO_OUT

Address: Operational Base(0x27DA0000) + offset (0x08E8)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes
19:4	RO	0x0000	HDCP2_ESM_P0_GPIO_OUT Port 0 General-Purpose outputs to the HDCP2 ESM block - For more information, see the ESM Databook. The bit mapping is equivalent to the ESM Databook definition. Value After Reset:0x0
3:0	RO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT Global General-Purpose outputs to the HDCP2 ESM block - For more information, see the ESM Databook. The bit mapping is equivalent to the ESM Databook definition. Value After Reset:0x0

HDMI TX Controller_HDCP14_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0900)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved1 Reserved Field:Yes
30:23	RW	0x00	HDCP14_PREWOO_OVR_VALUE Number of clock cycles between the VSYNC active edge and the start of Window of Opportunity (Divided by 4) Needs the hdcp14_prewoo_ovr_en active. Value After Reset:0x0
22	RW	0x0	HDCP14_PREWOO_OVR_EN Window of Oportunity Start Override Enable Value After Reset:0x0
21:19	RW	0x0	Reserved0 Reserved Field:Yes
18	RW	0x0	HDCP14_RI_READ_MODE Ri Read Mode: Values: 0x0 (RI_RDMODE_128_FRAMES): Trigered every 128 Frames. 0x1 (RI_RDMODE_2_SECONDS): Trigered every 2 seconds. Value After Reset:0x0
17:15	RW	0x2	HDCP14_OESS_CTL3_PULSE_SIZE Duration of the CTL3 bit definition when in OESS mode. Note 1: The value must be devided by 4. Value After Reset:0x2
14	RW	0x0	HDCP14_OESS_ESSS_OVR_VALUE EESS/OESS Override Value: Values: 0x0 (OESS): OESS 0x1 (EESS): EESS Value After Reset:0x0
13	RW	0x0	HDCP14_OESS_ESSS_OVR_EN EESS/OESS Override Enable Value After Reset:0x0

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Bit	Attr	Reset Value	Description
12	RW	0x0	HDCP14_AN_BYPASS An value definition: Values: 0x0 (AN_VALUE_HW): The An value is retrieved from the HDCP14 Cipher. 0x1 (AN_VALUE_SW): The An value is defined by the an_value register. Value After Reset:0x0
11	RW	0x0	HDCP14_AN_CIPHER_INPUT Chipher Input for An value calculation: Values: 0x0 (AN_CIPHER_HW): The Input of HDCP14 Cipher is connected directly from his outputs. 0x1 (AN_CIPHER_SW): The Input of HDCP14 Cipher is connected to an_value register. Value After Reset:0x0
10	RW	0x0	HDCP14_KEY_DECRYPT_EN HDCP Key Encryption enable: Values: 0x0 (HDCP_KEY_NONENC): HDCP Key is not encrypted. 0x1 (HDCP_KEY_ENC): HDCP Key is encrypted. Value After Reset:0x0
9	RW	0x0	HDCP14_FEATURES11_ENABLE Enable 1.1 Features for HDCP14. This option will only be applied if the connected HDCP Receiver also has the 1.1 Features Enabled. Value After Reset:0x0
8:5	RW	0x0	HDCP14_I2C_NACK_THRESHOLD Number of received I2C NACKs until the HDCP Transmitter became unauthenticated. If set to 4'b0, this check is disabled and the HDCP Transmitter never gets unauthenticated by the I2C NACK. Value After Reset:0x0
4	RW	0x0	HDCP14_I2C_SHORT_READ_DISABLE Disable I2C Short Read for HDCP14 Operations. Value After Reset:0x0
3	RW	0x0	HDCP14_I2C_FASTMODE Enable I2C Fast Mode for HDCP14 Operations. This option will only be applied if the connected HDCP Receiver also has the I2C Fast Mode Enabled. Value After Reset:0x0
2	RW	0x0	HDCP14_ENCRYPTION_ENABLE Encryption Enable Value After Reset:0x0
1	RW	0x0	HDCP14_BYPASS HDCP 14 Bypass Value After Reset:0x0
0	RW	0x0	HDCP14_HPD HDCP 14 HDP Value After Reset:0x0

HDMI TX Controller_HDCP14_CONTROL0

Address: Operational Base(0x27DA0000) + offset (0x0904)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
4	WO	0x0	HDCP14_SHA1_MSG_FAIL_P Software Indication that the SHA-1 Message failed. Value After Reset:0x0
3	WO	0x0	HDCP14_SHA1_MSG_CORRECT_P Software Indication that the SHA-1 Message was correctly digested. Value After Reset:0x0
2	RW	0x0	Reserved0 Reserved Field:Yes
1	WO	0x0	HDCP14_KSV_LIST_REVOCATED_P Software Indication that the KSV List was revocated. Value After Reset:0x0
0	WO	0x0	HDCP14_RESTART_P Restart HDCP14 Value After Reset:0x0

HDMI TX Controller_HDCP14_CONFIG1

Address: Operational Base(0x27DA0000) + offset (0x0908)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2 Reserved Field:Yes
27:19	RW	0x000	HDCP14_READY_TIMER_OVR_VALUE READY bit Timer Limit Limit Override Value The defined override value is in an 10ms timebase. Value After Reset:0x0
18	RW	0x0	HDCP14_READY_TIMER_OVR_EN READY bit Timer Limit Override Enable Value After Reset:0x0
17:16	RW	0x0	Reserved1 Reserved Field:Yes
15:8	RW	0x00	HDCP14_RI_TIMER_OVR_VALUE Ri Verification Timer Limit Override Value The defined override value is in an 10ms timebase. Value After Reset:0x0
7	RW	0x0	HDCP14_RI_TIMER_OVR_EN Ri Verification Timer Limit Override Enable Value After Reset:0x0
6:5	RW	0x0	Reserved0 Reserved Field:Yes
4:1	RW	0x0	HDCP14_R0_TIMER_OVR_VALUE R0 waiting Timer Limit Override Value The defined override value is in a 10ms base. Value After Reset:0x0
0	RW	0x0	HDCP14_R0_TIMER_OVR_EN R0 waiting Timer Limit Override Enable Value After Reset:0x0

HDMI TX Controller_HDCP14_CONFIG2

Address: Operational Base(0x27DA0000) + offset (0x090C)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
14:1	RW	0x0000	HDCP14_I2C_TIMER_OVR_VALUE I2C operation watchdog Timer Limit Override Value The defined override value is in an 10ms timebase. Value After Reset:0x0
0	RW	0x0	HDCP14_I2C_TIMER_OVR_EN I2C operation watchdog Timer Limit Override Enable Value After Reset:0x0

HDMI TX Controller_HDCP14_KEY_SEED

Address: Operational Base(0x27DA0000) + offset (0x0914)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15:0	WO	0x0000	HDCP14_KEY_DECRYPT_SEED HDCP Key Decryption seed. 16-bit seed used in HDCP Key Decryption. Value After Reset:0x0

HDMI TX Controller_HDCP14_KEY_H

Address: Operational Base(0x27DA0000) + offset (0x0918)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:0	WO	0x000000	HDCP14_KEY_HIGH HDCP Encrypted Key [55:32] portion. Encrypted secret key, only for external storage of encrypted HDCP keys. A key is written by first writing the high part of hdcpkey[55:32] in hdcp14_key_high register and then the low hdcpkey[31:0] to hdcp14_key_low register. Writing hdcp14_key_low triggers decryption and storage in the key table, as well as auto incrementing of the hdcp14_key_index. Value After Reset:0x0

HDMI TX Controller_HDCP14_KEY_L

Address: Operational Base(0x27DA0000) + offset (0x091C)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	HDCP14_KEY_LOW HDCP Encrypted Key [31:0] portion. Encrypted secret key, only for external storage of encrypted HDCP keys. A key is written by first writing the high part of hdcpkey[55:32] in hdcp14_key_high register and then the low hdcpkey[31:0] to hdcp14_key_low register. Writing hdcp14_key_low triggers decryption and storage in the key table, as well as auto incrementing of the hdcp14_key_index. Value After Reset:0x0

HDMI TX Controller_HDCP14_KEY_STATUS

Address: Operational Base(0x27DA0000) + offset (0x0920)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
8	RO	0x0	HDCP14_KEY_WR_OK HDCP Key write OK. Value After Reset:0x0
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RO	0x00	HDCP14_KEY_INDEX HDCP Key index. Valid range is 00h ... 27h. Value After Reset:0x0

HDMI TX Controller_HDCP14_AKSV_H

Address: Operational Base(0x27DA0000) + offset (0x0924)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x00	HDCP14_AKSV_HIGH DDC AKSV register content (bits 39:32). Value After Reset:0x0

HDMI TX Controller_HDCP14_AKSV_L

Address: Operational Base(0x27DA0000) + offset (0x0928)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HDCP14_AKSV_LOW DDC AKSV register content (bits 31:0). Value After Reset:0x0

HDMI TX Controller_HDCP14_AN_H

Address: Operational Base(0x27DA0000) + offset (0x092C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HDCP14_AN_VALUE_HIGH An value register content (bits 63:32). Value After Reset:0x0

HDMI TX Controller_HDCP14_AN_L

Address: Operational Base(0x27DA0000) + offset (0x0930)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HDCP14_AN_VALUE_LOW An value register content (bits 31:0). Value After Reset:0x0

HDMI TX Controller_HDCP14_STATUS0

Address: Operational Base(0x27DA0000) + offset (0x0934)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved2 Reserved Field:Yes
23:20	RO	0x0	HDCP14_I2C_NACK_CNT HDCP 1.4 Total of I2C NACK Received. Cleared when hdcp14_restart_p is set to 1 or the number of received I2C NACK reaches the value defined in hdcp14_i2c_nack_threshold. Value After Reset:0x0
19:17	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
16	RO	0x0	HDCP14_BKSV_REVOC_FAIL_ST HDCP 1.4 BKSV Revocation status. When changed, it triggers the bksv_revoc_fail_irq interrupt. Value After Reset:0x0
15:9	RO	0x00	HDCP14_RPT_DEVICE_COUNT HDCP 1.4 Receiver/Repeater DEVICE_COUNT. Total number of attached downstream devices. Always zero for HDCP Receivers. This count does not include the HDCP Repeater itself, but only downstream devices downstream from the HDCP Repeater Value After Reset:0x0
8	RO	0x0	HDCP14_RPT_MAX_DEVS_EXCEEDED HDCP 1.4 Receiver/Repeater MAX_DEVS_EXCEEDED. Topology error indicator. When set to one, more than 127 downstream devices, or the capacity of the KSV Fifo, are attached. Value After Reset:0x0
7:5	RO	0x0	HDCP14_RPT_DEPTH HDCP 1.4 Receiver/Repeater DEPTH. Three-bit repeater cascade depth. This value gives the number of attached levels through the connection topology. Value After Reset:0x0
4	RO	0x0	HDCP14_RPT_MAX_CASCADE_EXCEEDED HDCP 1.4 Receiver/Repeater MAX_CASCADE_EXCEEDED. Topology error indicator. When set to one, more than seven levels of video repeater have been cascaded together. Value After Reset:0x0
3	RO	0x0	HDCP14_RCV_HDMI_MODE HDCP 1.4 Receiver HDMI_MODE: Values: 0x0 (DVI_MODE): DVI Mode. 0x1 (HDMI_MODE): HDMI Mode. Value After Reset:0x0
2	RO	0x0	HDCP14_AUTH_ST HDCP 1.4 Authentication State: Values: 0x0 (NON_AUTHENTICATED): Not Authenticated 0x1 (AUTHENTICATED): Authenticated Value After Reset:0x0
1	RW	0x0	Reserved0 Reserved Field:Yes
0	RO	0x0	HDCP14_OESS_ESSS HDCP 1.4 Encryption Status Signaling status: Values: 0x0 (OESS): OESS 0x1 (EESS): EESS Value After Reset:0x0

HDMI TX Controller_HDCP14_STATUS1

Address: Operational Base(0x27DA0000) + offset (0x0938)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	Reserved1 Reserved Field:Yes
6	RO	0x0	HDCP14_RCV_REPEATER HDCP 1.4 Receiver Bstatus - REPEATER Value After Reset:0x0

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Bit	Attr	Reset Value	Description
5	RO	0x0	HDCP14_RCV_KSV_FIFO_READY HDCP 1.4 Receiver Bstatus - READY bit Value After Reset:0x0
4	RO	0x0	HDCP14_RCV_FASTMODE HDCP 1.4 Receiver Bstatus - FAST Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RO	0x0	HDCP14_RCV_1_1_FEATURES HDCP 1.4 Receiver Bstatus - 1.1_FEATURES Value After Reset:0x0
0	RO	0x0	HDCP14_RCV_FAST_REAUTHENTICATION HDCP 1.4 Receiver Bstatus - FAST_REAUTHENTICATION Value After Reset:0x0

HDMI TX Controller_SCRAMB_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0960)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	TMDS_SCRAMB_ENABLE TMDS scrambling enable Value After Reset:0x0

HDMI TX Controller_LINK_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0968)

Bit	Attr	Reset Value	Description
31:17	RW	0x0000	Reserved4 Reserved Field:Yes
16	RW	0x0	PHY_WORD_REVERSE Output bit reverse Values: 0x0 (NOT_REVERSED): word order is not reversed for the output 0x1 (REVERSED): word order is reversed for the output Value After Reset:0x0
15:13	RW	0x0	Reserved3 Reserved Field:Yes
12	RW	0x0	BIT_REVERSE Output bit reverse Values: 0x0 (NOT_REVERSED): Bit order is not reversed for the output 0x1 (REVERSED): Bit order is reversed for the output Value After Reset:0x0
11:9	RW	0x0	Reserved2 Reserved Field:Yes
8	RW	0x0	OPMODE_FRL_4LANES FRL number of active lanes Values: 0x0 (THREE_LANES): 3 lanes 0x1 (FOUR_LANES): 4 lanes Value After Reset:0x0
7:5	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
4	RW	0x1	OPMODE_DVI HDMI / DVI configuration bit Values: 0x0 (HDMI): HDMI mode 0x1 (DVI): DVI mode Value After Reset:0x1
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	OPMODE_FRL TMDS / FRL configuration bit Values: 0x0 (TMDS): TMDS mode 0x1 (FRL): FRL mode Value After Reset:0x0

HDMI TX Controller_TMDS_FIFO_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0970)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x1	TMDSFIFO_INIT_ON_OVF TMDS FIFO Init on overflow configuration. Value After Reset:0x1

HDMI TX Controller_TMDS_FIFO_CONTROL0

Address: Operational Base(0x27DA0000) + offset (0x0974)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	TMDSFIFO_CLR_P TMDS FIFO clear Value After Reset:0x0

HDMI TX Controller_FRL_RSFEC_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0A20)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	FRL_RSFEC_ENC_BYP FRL Reed-Solomon FEC calculation bypass enable: Values: 0x0 (NORMAL_MODE): RS FEC block calculate RS parity data to be included in the FRL stream 0x1 (BYPASS_MODE): RS FEC block does not calculate RS parity data to be included in the FRL stream Value After Reset:0x0

HDMI TX Controller_FRL_RSFEC_STATUS0

Address: Operational Base(0x27DA0000) + offset (0x0A30)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
0	RO	0x0	FRL_RSFEC_ALIGN_BUFFER_FULL_ST FRL Reed-Solomon FEC Aligner Buffer Full Status. Values: 0x0 (NOT_FULL): RS FEC Aligner Buffer is in normal operation 0x1 (FULL): RS FEC Aligner Buffer is full Value After Reset:0x0

HDMI TX Controller_FRL_PKTZ_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0A40)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	PKTZ_FRLCHAR_FIFO_INIT_ON_OVF FRL Packetizer FIFO Init on Overflow control Value After Reset:0x0

HDMI TX Controller_FRL_PKTZ_CONTROL0

Address: Operational Base(0x27DA0000) + offset (0x0A44)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	PKTZ_FRLCHAR_FIFO_CLR_P FRL Packetizer FIFO clear Value After Reset:0x0

HDMI TX Controller_FRL_PKTZ_CONTROL1

Address: Operational Base(0x27DA0000) + offset (0x0A50)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	PKTZ_FRLCHAR_FIFO_MAX_FILL_LEVEL_CLR_P FRL Packetizer FIFO max level clear Value After Reset:0x0

HDMI TX Controller_FRL_PKTZ_STATUS1

Address: Operational Base(0x27DA0000) + offset (0x0A54)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	Reserved0 Reserved Field:Yes
6:0	RO	0x00	PKTZ_FRLCHAR_FIFO_MAX_FILL_LEVEL FRL Packetizer FIFO maximum fill level reached This value is cleared with the frl_pktz_control1.pktz_frlchar_fifo_max_fill_level_clr_p bit field Value After Reset:0x0

HDMI TX Controller_PKTSCHED_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0A80)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
2	RW	0x1	PKTSCHED_PRQUEUE2_EXEC_TYPE Packet Priority Queue 2 - Execution type Values: 0x0 (PRIORITY): Priority List 0x1 (RROBIN): Round-Robin Value After Reset:0x1
1	RW	0x1	PKTSCHED_PRQUEUE1_EXEC_TYPE Packet Priority Queue 1 - Execution type Values: 0x0 (PRIORITY): Priority List 0x1 (RROBIN): Round-Robin Value After Reset:0x1
0	RW	0x0	PKTSCHED_PRQUEUE0_EXEC_TYPE Packet Priority Queue 0 - Execution type Values: 0x0 (PRIORITY): Priority List 0x1 (RROBIN): Round-Robin Value After Reset:0x0

HDMI TX Controller_PKTSCHED_PRQUEUE0_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0A84)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved2 Reserved Field:Yes
20:16	RW	0x03	PKTSCHED_PRQUEUE0_P2 Priority queue 0, priority position 2 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x3
15:13	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
12:8	RW	0x02	PKTSCHED_PRQUEUE0_P1 Priority queue 0, priority position 1 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x2
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x01	PKTSCHED_PRQUEUE0_P0 Priority queue 0, priority position 0 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x1

HDMI TX Controller_PKTSCHED_PRQUEUE1_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0A88)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
28:24	RW	0x09	PKTSCHED_PRQUEUE1_P3 Priority queue 1, priority position 3 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x9
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20:16	RW	0x07	PKTSCHED_PRQUEUE1_P2 Priority queue 1, priority position 2 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x7
15:13	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
12:8	RW	0x0d	PKTSCHED_PRQUEUE1_P1 Priority queue 1, priority position 1 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0xd
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x08	PKTSCHED_PRQUEUE1_P0 Priority queue 1, priority position 0 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x8

HDMI TX Controller_PKTSCHED_PRQUEUE2_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0A8C)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
28:24	RW	0x06	PKTSCHED_PRQUEUE2_P3 Priority queue 2, priority position 3 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x6
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20:16	RW	0x05	PKTSCHED_PRQUEUE2_P2 Priority queue 2, priority position 2 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x5
15:13	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
12:8	RW	0x0c	PKTSCHED_PRQUEUE2_P1 Priority queue 2, priority position 1 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0xc
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x04	PKTSCHED_PRQUEUE2_P0 Priority queue 2, priority position 0 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x4

HDMI TX Controller_PKTSCHED_PRQUEUE2_CONFIG1

Address: Operational Base(0x27DA0000) + offset (0x0A90)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
28:24	RW	0x0e	PKTSCHED_PRQUEUE2_P7 Priority queue 2, priority position 7 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0xe
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20:16	RW	0x0f	PKTSCHED_PRQUEUE2_P6 Priority queue 2, priority position 6 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0xf
15:13	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
12:8	RW	0x0b	PKTSCHED_PRQUEUE2_P5 Priority queue 2, priority position 5 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0xb
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x0a	PKTSCHED_PRQUEUE2_P4 Priority queue 2, priority position 4 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0xa

HDMI TX Controller_PKTSCHED_PRQUEUE2_CONFIG2

Address: Operational Base(0x27DA0000) + offset (0x0A94)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
12:8	RW	0x11	PKTSCHED_PRQUEUE2_P9 Priority queue 2, priority position 9 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x11
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x10	PKTSCHED_PRQUEUE2_P8 Priority queue 2, priority position 8 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x10

HDMI TX Controller_PKTSCHED_PKT_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0A98)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
29:22	RW	0x01	PKTSCHED_ISRC_TIMER Packet Type ISRC 1/2 (International Standard Recording Code) Schedule Timer The ISRC 1/2 packets shall be sent once every time interval set in this field. The timer base increment is defined in the register field pktsched_isrc_timer_base. Settings 0 and 1 have the same value; - 0 : 1 time the configured timer base - 1 : 1 time the configured timer base - 2 : 2 times the configured timer base - ... - 255 : 255 times the configured timer base Note: There may be some uncertainty in the real time interval due to Data Island location within a frame and overall packet type priority settings. Value After Reset:0x1
21:20	RW	0x3	PKTSCHED_ISRC_TIMER_BASE Packet Type ISRC 1/2 (International Standard Recording Code) Schedule Timer Base Values: 0x0 (ONE_US): Timer base of 1 microsecond (1 us) 0x1 (ONE_HUNDRED_US): Timer base of 100 microseconds (100 us) 0x2 (TEN_MS): Timer base of 10 miliseconds (10 ms) 0x3 (VSYNC): Timer base corresponding to the Vertical frequency of the Video Mode being sent Value After Reset:0x3
19:12	RW	0x64	PKTSCHED_SPDI_TIMER Packet Type SPDI (Source Product Descriptor InfoFrame) Schedule Timer The SPDI packet shall be sent once every time interval set in this field. The timer base increment is defined in the register field pktsched_spdi_timer_base. Settings 0 and 1 have the same value; The recommended interval between SPDI packets per CTA-861-G specification is 1s; SPDI packets shall not be sent more than once per Video Frame, although it is possible for debug or custom usage. - 0 : 1 time the configured timer base - 1 : 1 time the configured timer base - 2 : 2 times the configured timer base - ... - 255 : 255 times the configured timer base Note: There may be some uncertainty in the real time interval due to Data Island location within a frame and overall packet type priority settings. Value After Reset:0x64

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Bit	Attr	Reset Value	Description
11:10	RW	0x2	PKTSCHED_SPDI_TIMER_BASE Packet Type SPDI (Source Product Descriptor InfoFrame) Schedule Timer Base Values: 0x0 (ONE_US): Timer base of 1 microsecond (1 us) 0x1 (ONE_HUNDRED_US): Timer base of 100 microseconds (100 us) 0x2 (TEN_MS): Timer base of 10 miliseconds (10 ms) 0x3 (VSYNC): Timer base corresponding to the Vertical frequency of the Video Mode being sent Value After Reset:0x2
9:2	RW	0x01	PKTSCHED_ACP_TIMER Packet Type ACP (Audio Content Protection) Schedule Timer The ACP packet shall be sent once every time interval set in this field. The timer base increment is defined in the register field pktsched_acp_timer_base. Settings 0 and 1 have the same value; The maximum interval between ACP packets per HDMI2.1 specification is 300ms; Larger values may be used for debug or custom usage. - 0 : 1 time the configured timer base - 1 : 1 time the configured timer base - 2 : 2 times the configured timer base - ... - 255 : 255 times the configured timer base Note: There may be some uncertainty in the real time interval due to Data Island location within a frame and overall packet type priority settings. Value After Reset:0x1
1:0	RW	0x3	PKTSCHED_ACP_TIMER_BASE Packet Type ACP (Audio Content Protection) Schedule Timer Base Values: 0x0 (ONE_US): Timer base of 1 microsecond (1 us) 0x1 (ONE_HUNDRED_US): Timer base of 100 microseconds (100 us) 0x2 (TEN_MS): Timer base of 10 miliseconds (10 ms) 0x3 (VSYNC): Timer base corresponding to the Vertical frequency of the Video Mode being sent Value After Reset:0x3

HDMI TX Controller_PKTSCHED_PKT_CONFIG1

Address: Operational Base(0x27DA0000) + offset (0x0A9C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
15	RW	0x0	PKTSCHED_EMPFAPA_NOINTERLEAVE Packet Type EMP (Extended Metadata) Block interleaving other packets with SYNC=1 EMP packets during FAPA EMP packets with SYNC=1 bit setting within its contents shall be sent during the FAPA region of the frame. This field blocks any other packet types to be interleaved between SYNC=1 EMP packets during the FAPA region, except for packets that always take precedence per HDMI2.1 specification: ACR, AUDS, GCP. Values: 0x0 (INTERLEAVE): Other packet types can be interleaved with SYNC=1 EMP packet during FAPA region. 0x1 (NOINTERLEAVE): Other packet types are blocked from being interleaved with SYNC=1 EMP packet during FAPA region. Value After Reset:0x0
14	RW	0x1	PKTSCHED_VSI_FIELDRATE Packet type VSI (Vendor Specific InfoFrame) Send Rate Values: 0x0 (ONEFIELD): VSI packet sent once per One Video Field 0x1 (TWOFIELDS): VSI packet sent once per Two Video Fields Value After Reset:0x1
13	RW	0x1	PKTSCHED_DRMI_FIELDRATE Packet type DRMI (Dynamic Range and Mastering InfoFrame) Send Rate Values: 0x0 (ONEFIELD): DRMI packet sent once per One Video Field 0x1 (TWOFIELDS): DRMI packet sent once per Two Video Fields Value After Reset:0x1
12	RW	0x1	PKTSCHED_AVI_FIELDRATE Packet type AVI (Auxiliary Video InfoFrame) Send Rate Values: 0x0 (ONEFIELD): AVI packet sent once per One Video Field 0x1 (TWOFIELDS): AVI packet sent once per Two Video Fields Value After Reset:0x1
11	RW	0x1	PKTSCHED_AUDI_BEFORE_NEW_AUDS Packet type AUDI (Audio InfoFrame) Send Before First New Audio Sample Packet When a new Audio Format is configured, and a new Audio stream is enabled to be sent (change 'pktsched_auds_tx_en' from 0 to 1), an AUDI packet shell be sent before the first Audio Sample packet Values: 0x0 (DISABLED): AUDS Audio Sample packets sent immediately 0x1 (ENABLED): AUDI packet sent before first new AUDS Audio Sample packet Value After Reset:0x1

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Bit	Attr	Reset Value	Description
10	RW	0x1	PKTSCHED_AMD_BEFORE_NEW_AUDS Packet type AMD (Audio Metadata) Send Before First New Audio Sample Packet When a new Audio Format is configured, and a new Audio stream is enabled to be sent (change 'pktsched_auds_tx_en' from 0 to 1), an AMD packet shell be sent before the first Audio Sample packet Values: 0x0 (DISABLED): AUDS Audio Sample packets sent immediately 0x1 (ENABLED): AMD packet sent before first new AUDS Audio Sample packet Value After Reset:0x1
9	RW	0x1	PKTSCHED_AUDI_FIELD_FORCE_SCHED Packet type AUDI (Audio Infoframe) Force Schedule In regular schedule, AUDI packets are sent once per video field. Per HDMI2.1 specificattion, when there is any change to the AUDI packet contents, or a new Audio stream is started, the AUDI packet should be sent before any new audio sample (AUDS packets) If a previous AUDI packet has already been sent in the current video frame, this bit forces the packet schedule to allow a new content AUDI packet to be sent as soon as it is available, instead of waiting for a new video frame. Values: 0x0 (AUDIFORCEEN): AUDI Force Schedule Disabled 0x1 (AUDIFORCEDIS): AUDI Force Schedule Enabled Value After Reset:0x1
8	RW	0x1	PKTSCHED_AMD_FIELD_FORCE_SCHED Packet type AMD (Audio Metadata) Force Schedule In regular schedule, AMD packets are sent once per video field. Per HDMI2.1 specificattion, when there is any change to the AMD packet contents, or a new Audio stream is started, the AMD packet should be sent before any new audio sample (AUDS packets) If a previous AMD packet has already been sent in the current video frame, this bit forces the packet schedule to allow a new content AMD packet to be sent as soon as it is available, instead of waiting for a new video frame. Values: 0x0 (AMDFORCEEN): AMD Force Schedule Disabled 0x1 (AMDFORCEDIS): AMD Force Schedule Enabled Value After Reset:0x1
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKTSCHED_PKT_CONFIG2

Address: Operational Base(0x27DA0000) + offset (0x0AA0)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
28:24	RW	0x11	PKTSCHED_GHDMI2_PKT_OVR_VALUE Packet type GHDMI2 (Generic HDMI 2) override to replace other packet type's content If this field is set to any value different from GHDMI2, the contents register fields (pkt_ghdmi2_contents[0-7]) will replace the selected packet type contents. The packet enable and schedule configuration for the overriden packet type are still controlled by that type's respective register fields and hardware behavior. Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x11
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20	RW	0x0	PKTSCHED_GHDMI2_UNIT Packet type GHDMI2 (Generic HDMI 2) Send Unit Set the send unit for the number defined in pktsched_ghdmi2_rate. Note: This field is not used if pktsched_ghdmi2_pkt_ovr_value is set to any value different from GHDMI2; Values: 0x0 (FRAME): Packets per Video Frame 0x1 (FIELD): Packets per Video Field Value After Reset:0x0

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Bit	Attr	Reset Value	Description
19:16	RW	0x0	PKTSCHED_GHDMI2_RATE Packet type GHDMI2 (Generic HDMI 2) Send Rate Set the send rate for GHDMI2 packets, in number of packets per field or frame (depending on the setting of pktsched_ghdmi2_unit). Note: This field is not used if pktsched_ghdmi2_pkt_ovr_value is set to any value different from GHDMI2; Values: 0x0 (DISABLED): Send disabled 0x1 (SEND1): Send 1 packet per field/frame 0x2 (SEND2): Send 2 packets per field/frame 0x3 (SEND3): Send 3 packets per field/frame 0x4 (SEND4): Send 4 packets per field/frame 0x5 (SEND5): Send 5 packets per field/frame 0x6 (SEND6): Send 6 packets per field/frame 0x7 (SEND7): Send 7 packets per field/frame 0x8 (SEND8): Send 8 packets per field/frame 0x9 (SEND9): Send 9 packets per field/frame 0xa (SEND10): Send 10 packets per field/frame 0xb (SEND11): Send 11 packets per field/frame 0xc (SEND12): Send 12 packets per field/frame 0xd (SEND13): Send 13 packets per field/frame 0xe (SEND14): Send 14 packets per field/frame 0xf (SEND15): Send 15 packets per field/frame Value After Reset:0x0
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x10	PKTSCHED_GHDMI1_PKT_OVR_VALUE Packet type GHDMI1 (Generic HDMI 1) override to replace other packet type's content If this field is set to any value different from GHDMI1, the contents register fields (pkt_ghdmi1_contents[0-7]) will replace the selected packet type contents. The packet enable and schedule configuration for the overriden packet type are still controlled by that type's respective register fields and hardware behavior. Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x10

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4	RW	0x0	PKTSCHED_GHDMI1_UNIT Packet type GHDMI1 (Generic HDMI 1) Send Unit Set the send unit for the number defined in pktsched_ghdmi1_rate. Note: Note: This field is not used if pktsched_ghdmi1_pkt_ovr_value is set to any value different from GHDMI1; Values: 0x0 (FRAME): Packets per Video Frame 0x1 (FIELD): Packets per Video Field Value After Reset:0x0
3:0	RW	0x0	PKTSCHED_GHDMI1_RATE Packet type GHDMI1 (Generic HDMI 1) Send Rate Set the send rate for GHDMI1 packets, in number of packets per field or frame (depending on the setting of pktsched_ghdmi1_unit). Note: Note: This field is not used if pktsched_ghdmi1_pkt_ovr_value is set to any value different from GHDMI1; Values: 0x0 (DISABLED): Send disabled 0x1 (SEND1): Send 1 packet per field/frame 0x2 (SEND2): Send 2 packets per field/frame 0x3 (SEND3): Send 3 packets per field/frame 0x4 (SEND4): Send 4 packets per field/frame 0x5 (SEND5): Send 5 packets per field/frame 0x6 (SEND6): Send 6 packets per field/frame 0x7 (SEND7): Send 7 packets per field/frame 0x8 (SEND8): Send 8 packets per field/frame 0x9 (SEND9): Send 9 packets per field/frame 0xa (SEND10): Send 10 packets per field/frame 0xb (SEND11): Send 11 packets per field/frame 0xc (SEND12): Send 12 packets per field/frame 0xd (SEND13): Send 13 packets per field/frame 0xe (SEND14): Send 14 packets per field/frame 0xf (SEND15): Send 15 packets per field/frame Value After Reset:0x0

HDMI TX Controller_PKTSCHED_PKT_CONFIG3

Address: Operational Base(0x27DA0000) + offset (0x0AA4)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved3 Reserved Field:Yes
19	RW	0x0	PKTSCHED_GHDMI2_TX_ONCE GHDMI2 - Generic HDMI 2 packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0

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Bit	Attr	Reset Value	Description
18	RW	0x0	PKTSCHED_GHDMI1_TX_ONCE GHDMI1 - Generic HDMI 1 packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
17	RW	0x0	PKTSCHED_DRMI_TX_ONCE DRMI - Dynamic Range and Mastering InfoFrame packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
16	RW	0x0	PKTSCHED_NVI_TX_ONCE NVI - NTSC VBI InfoFrame packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
15	RW	0x0	PKTSCHED_AUDI_TX_ONCE AUDI - Audio InfoFrame packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
14	RW	0x0	PKTSCHED_SPDI_TX_ONCE SPDI - Source Product Descriptor InfoFrame packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
13	RW	0x0	PKTSCHED_AVI_TX_ONCE AVI - Auxiliary Video InfoFrame packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0

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Bit	Attr	Reset Value	Description
12	RW	0x0	PKTSCHED_VSI_TX_ONCE VSI - Vendor Specific InfoFrame packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
11:8	RW	0x0	Reserved2 Reserved Field:Yes
7	RW	0x0	PKTSCHED_GMD_TX_ONCE GMD - Gamut Metadata packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
6	RW	0x0	Reserved1 Reserved Field:Yes
5	RW	0x0	PKTSCHED_ISRC_TX_ONCE ISRC - Intl Std Recording Code packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
4	RW	0x0	PKTSCHED_ACP_TX_ONCE ACP - Audio Content Protection packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
3:0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKTSCHED_PKT_EN

Address: Operational Base(0x27DA0000) + offset (0x0AA8)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved1 Reserved Field:Yes
19	RW	0x0	PKTSCHED_GHDMI2_TX_EN GHDMI2 - Generic HDMI 2 packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0

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Bit	Attr	Reset Value	Description
18	RW	0x0	PKTSCHED_GHDMI1_TX_EN GHDMI1 - Generic HDMI 1 packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
17	RW	0x0	PKTSCHED_DRMI_TX_EN DRMI - Dynamic Range and Mastering InfoFrame packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
16	RW	0x0	PKTSCHED_NVI_TX_EN NVI - NTSC VBI InfoFrame packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
15	RW	0x0	PKTSCHED_AUDI_TX_EN AUDI - Audio InfoFrame packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
14	RW	0x0	PKTSCHED_SPDI_TX_EN SPDI - Source Product Descriptor InfoFrame packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
13	RW	0x0	PKTSCHED_AVI_TX_EN AVI - Auxiliary Video InfoFrame packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
12	RW	0x0	PKTSCHED_VSI_TX_EN VSI - Vendor Specific InfoFrame packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
11	RW	0x0	Reserved0 Reserved Field:Yes
10	RW	0x0	PKTSCHED_EMP_CVTEM_TX_EN CVTEM - Compressed Video Timing Extended Metadata packet transmission control: Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0

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Bit	Attr	Reset Value	Description
9	RW	0x0	PKTSCHED_EMP_VTEM_TX_EN VTEM - Video Timing Extended Metadata packet transmission control: Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
8	RW	0x0	PKTSCHED_AMD_TX_EN AMD - Audio Metadata packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
7	RW	0x0	PKTSCHED_GMD_TX_EN GMD - Gamut Metadata packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
6	RW	0x0	PKTSCHED_ISRC2_TX_EN ISRC2 - Intl Std Recording Code 2 packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
5	RW	0x0	PKTSCHED_ISRC1_TX_EN ISRC1 - Intl Std Recording Code 1 packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
4	RW	0x0	PKTSCHED_ACP_TX_EN ACP - Audio Content Protection packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
3	RW	0x0	PKTSCHED_GCP_TX_EN GCP - General Control packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
2	RW	0x0	PKTSCHED_AUDS_TX_EN AUDS - Audio Sample packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
1	RW	0x0	PKTSCHED_ACR_TX_EN ACR - Audio Clock Regeneration packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0

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Bit	Attr	Reset Value	Description
0	RW	0x0	PKTSCHED_NULL_TX_EN NULL - Null packet transmission control; This packet type is a filler for Data Island periods, when all other packet types are either not enabled or waiting for their respective scheduled slot. If disabled, when no other packets types are ready to be sent, the HDMI stream will be kept in Control Period, and no Data Island period is used. Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0

HDMI TX Controller_PKTSCHED_PKT_CONTROL0

Address: Operational Base(0x27DA0000) + offset (0x0AAC)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	RW	0x0	PKTSCHED_GCP_CLEAR_AVMUTE GCP - General Control - Define the value of the Clear_AVMUTE field in GCP packets. If this field is set to '1', field 'pktsched_gcp_set_avmute' must be 0. Values: 0x0 (CLEAR_AVMUTE0): Clear_AVMUTE=0 0x1 (CLEAR_AVMUTE1): Clear_AVMUTE=1 Value After Reset:0x0
0	RW	0x0	PKTSCHED_GCP_SET_AVMUTE GCP - General Control - Define the value of the Set_AVMUTE field in GCP packets. If this field is set to '1', field 'pktsched_gcp_clear_avmute' must be 0. Values: 0x0 (SET_AVMUTE0): Set_AVMUTE=0 0x1 (SET_AVMUTE1): Set_AVMUTE=1 Value After Reset:0x0

HDMI TX Controller_PKTSCHED_PKT_SEND

Address: Operational Base(0x27DA0000) + offset (0x0AB0)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved2 Reserved Field:Yes
19	WO	0x0	PKTSCHED_GHDMI2_TX_SEND_P GHDMI2 - Generic HDMI 2 packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
18	WO	0x0	PKTSCHED_GHDMI1_TX_SEND_P GHDMI1 - Generic HDMI 1 packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
17	WO	0x0	PKTSCHED_DRMI_TX_SEND_P DRMI - Dynamic Range and Mastering InfoFrame packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
16	WO	0x0	PKTSCHED_NVI_TX_SEND_P NVI - NTSC VBI InfoFrame packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
15	WO	0x0	PKTSCHED_AUDI_TX_SEND_P AUDI - Audio InfoFrame packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
14	WO	0x0	PKTSCHED_SPDI_TX_SEND_P SPDI - Source Product Descriptor InfoFrame packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
13	WO	0x0	PKTSCHED_AVI_TX_SEND_P AVI - Auxiliary Video InfoFrame packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
12	WO	0x0	PKTSCHED_VSI_TX_SEND_P VSI - Vendor Specific InfoFrame packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
11:8	RW	0x0	Reserved1 Reserved Field:Yes
7	WO	0x0	PKTSCHED_GMD_TX_SEND_P GMD - Gamut Metadata packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
6	WO	0x0	PKTSCHED_ISRC2_TX_SEND_P ISRC2 - Intl Std Recording Code 2 packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
5	WO	0x0	PKTSCHED_ISRC1_TX_SEND_P ISRC1 - Intl Std Recording Code 1 packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
4	WO	0x0	PKTSCHED_ACP_TX_SEND_P ACP - Audio Content Protection packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
3:0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKTSCHED_PKT_STATUS0

Address: Operational Base(0x27DA0000) + offset (0x0AB4)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved2 Reserved Field:Yes
19	RO	0x0	PKTSCHED_GHDMI2_TX_STATUS GHDMI2 - Generic HDMI 2 packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0

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Bit	Attr	Reset Value	Description
18	RO	0x0	PKTSCHED_GHDMI1_TX_STATUS GHDMI1 - Generic HDMI 1 packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
17	RO	0x0	PKTSCHED_DRMI_TX_STATUS DRMI - Dynamic Range and Mastering InfoFrame packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
16	RO	0x0	PKTSCHED_NVI_TX_STATUS NVI - NTSC VBI InfoFrame packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
15	RO	0x0	PKTSCHED_AUDI_TX_STATUS AUDI - Audio InfoFrame packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
14	RO	0x0	PKTSCHED_SPDI_TX_STATUS SPDI - Source Product Descriptor InfoFrame packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
13	RO	0x0	PKTSCHED_AVI_TX_STATUS AVI - Auxiliary Video InfoFrame packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
12	RO	0x0	PKTSCHED_VSI_TX_STATUS VSI - Vendor Specific InfoFrame packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
11:8	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
7	RO	0x0	PKTSCHED_GMD_TX_STATUS GMD - Gamut Metadata packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
6	RO	0x0	PKTSCHED_ISRC2_TX_STATUS ISRC2 - Intl Std Recording Code 2 packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
5	RO	0x0	PKTSCHED_ISRC1_TX_STATUS ISRC1 - Intl Std Recording Code 1 packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
4	RO	0x0	PKTSCHED_ACP_TX_STATUS ACP - Audio Content Protection packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
3:0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKTSCHED_PKT_STATUS1

Address: Operational Base(0x27DA0000) + offset (0x0AB8)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x0	PKTSCHED_GCP_AVMUTE_SENT_STS Currently active AVMUTE status; i.e. last AVMUTE state sent to HDMI Sink in a GCP Packet Value After Reset:0x0

HDMI TX Controller_PKT_NULL_CONTENTS0

Address: Operational Base(0x27DA0000) + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_NULL_HEADER_HB2 NULL - Null - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_NULL_HEADER_HB1 NULL - Null - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

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HDMI TX Controller_PKT_NULL_CONTENTS1

Address: Operational Base(0x27DA0000) + offset (0x0B04)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NULL_BODY_PB3_0 NULL - Null - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_NULL_CONTENTS2

Address: Operational Base(0x27DA0000) + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NULL_BODY_PB7_4 NULL - Null - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_NULL_CONTENTS3

Address: Operational Base(0x27DA0000) + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NULL_BODY_PB11_8 NULL - Null - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_NULL_CONTENTS4

Address: Operational Base(0x27DA0000) + offset (0x0B10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NULL_BODY_PB15_12 NULL - Null - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_NULL_CONTENTS5

Address: Operational Base(0x27DA0000) + offset (0x0B14)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NULL_BODY_PB19_16 NULL - Null - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_NULL_CONTENTS6

Address: Operational Base(0x27DA0000) + offset (0x0B18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NULL_BODY_PB23_20 NULL - Null - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_NULL_CONTENTS7

Address: Operational Base(0x27DA0000) + offset (0x0B1C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NULL_BODY_PB27_24 NULL - Null - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_ACP_CONTENTS0

Address: Operational Base(0x27DA0000) + offset (0x0B20)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	PKT_ACP_HEADER_HB2 ACP - Audio Content Protection - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_ACP_HEADER_HB1 ACP - Audio Content Protection - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_ACP_CONTENTS1

Address: Operational Base(0x27DA0000) + offset (0x0B24)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ACP_BODY_PB3_0 ACP - Audio Content Protection - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_ACP_CONTENTS2

Address: Operational Base(0x27DA0000) + offset (0x0B28)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ACP_BODY_PB7_4 ACP - Audio Content Protection - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_ACP_CONTENTS3

Address: Operational Base(0x27DA0000) + offset (0x0B2C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ACP_BODY_PB11_8 ACP - Audio Content Protection - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_ACP_CONTENTS4

Address: Operational Base(0x27DA0000) + offset (0x0B30)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ACP_BODY_PB15_12 ACP - Audio Content Protection - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_ACP_CONTENTS5

Address: Operational Base(0x27DA0000) + offset (0x0B34)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ACP_BODY_PB19_16 ACP - Audio Content Protection - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_ACP_CONTENTS6

Address: Operational Base(0x27DA0000) + offset (0x0B38)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ACP_BODY_PB23_20 ACP - Audio Content Protection - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_ACP_CONTENTS7

Address: Operational Base(0x27DA0000) + offset (0x0B3C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ACP_BODY_PB27_24 ACP - Audio Content Protection - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC1_CONTENTS0

Address: Operational Base(0x27DA0000) + offset (0x0B40)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_ISRC1_HEADER_HB2 ISRC1 - Intl Std Recording Code 1 - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_ISRC1_HEADER_HB1 ISRC1 - Intl Std Recording Code 1 - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_ISRC1_CONTENTS1

Address: Operational Base(0x27DA0000) + offset (0x0B44)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC1_BODY_PB3_0 ISRC1 - Intl Std Recording Code 1 - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC1_CONTENTS2

Address: Operational Base(0x27DA0000) + offset (0x0B48)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC1_BODY_PB7_4 ISRC1 - Intl Std Recording Code 1 - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC1_CONTENTS3

Address: Operational Base(0x27DA0000) + offset (0x0B4C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC1_BODY_PB11_8 ISRC1 - Intl Std Recording Code 1 - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC1_CONTENTS4

Address: Operational Base(0x27DA0000) + offset (0x0B50)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC1_BODY_PB15_12 ISRC1 - Intl Std Recording Code 1 - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC1_CONTENTS5

Address: Operational Base(0x27DA0000) + offset (0x0B54)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC1_BODY_PB19_16 ISRC1 - Intl Std Recording Code 1 - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC1_CONTENTS6

Address: Operational Base(0x27DA0000) + offset (0x0B58)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC1_BODY_PB23_20 ISRC1 - Intl Std Recording Code 1 - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC1_CONTENTS7

Address: Operational Base(0x27DA0000) + offset (0x0B5C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC1_BODY_PB27_24 ISRC1 - Intl Std Recording Code 1 - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC2_CONTENTS0

Address: Operational Base(0x27DA0000) + offset (0x0B60)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_ISRC2_HEADER_HB2 ISRC2 - Intl Std Recording Code 2 - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_ISRC2_HEADER_HB1 ISRC2 - Intl Std Recording Code 2 - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_ISRC2_CONTENTS1

Address: Operational Base(0x27DA0000) + offset (0x0B64)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC2_BODY_PB3_0 ISRC2 - Intl Std Recording Code 2 - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC2_CONTENTS2

Address: Operational Base(0x27DA0000) + offset (0x0B68)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC2_BODY_PB7_4 ISRC2 - Intl Std Recording Code 2 - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC2_CONTENTS3

Address: Operational Base(0x27DA0000) + offset (0x0B6C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC2_BODY_PB11_8 ISRC2 - Intl Std Recording Code 2 - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC2_CONTENTS4

Address: Operational Base(0x27DA0000) + offset (0x0B70)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC2_BODY_PB15_12 ISRC2 - Intl Std Recording Code 2 - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC2_CONTENTS5

Address: Operational Base(0x27DA0000) + offset (0x0B74)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC2_BODY_PB19_16 ISRC2 - Intl Std Recording Code 2 - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC2_CONTENTS6

Address: Operational Base(0x27DA0000) + offset (0x0B78)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC2_BODY_PB23_20 ISRC2 - Intl Std Recording Code 2 - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC2_CONTENTS7

Address: Operational Base(0x27DA0000) + offset (0x0B7C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC2_BODY_PB27_24 ISRC2 - Intl Std Recording Code 2 - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_GMD_CONTENTS0

Address: Operational Base(0x27DA0000) + offset (0x0B80)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_GMD_HEADER_HB2 GMD - Gamut Metadata - Packet Header (byte HB2) Value After Reset:0x0

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	PKT_GMD_HEADER_HB1 GMD - Gamut Metadata - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_GMD_CONTENTS1

Address: Operational Base(0x27DA0000) + offset (0x0B84)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GMD_BODY_PB3_0 GMD - Gamut Metadata - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_GMD_CONTENTS2

Address: Operational Base(0x27DA0000) + offset (0x0B88)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GMD_BODY_PB7_4 GMD - Gamut Metadata - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_GMD_CONTENTS3

Address: Operational Base(0x27DA0000) + offset (0x0B8C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GMD_BODY_PB11_8 GMD - Gamut Metadata - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_GMD_CONTENTS4

Address: Operational Base(0x27DA0000) + offset (0x0B90)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GMD_BODY_PB15_12 GMD - Gamut Metadata - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_GMD_CONTENTS5

Address: Operational Base(0x27DA0000) + offset (0x0B94)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GMD_BODY_PB19_16 GMD - Gamut Metadata - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_GMD_CONTENTS6

Address: Operational Base(0x27DA0000) + offset (0x0B98)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GMD_BODY_PB23_20 GMD - Gamut Metadata - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_GMD_CONTENTS7

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Address: Operational Base(0x27DA0000) + offset (0x0B9C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GMD_BODY_PB27_24 GMD - Gamut Metadata - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_AMD_CONTENTS0

Address: Operational Base(0x27DA0000) + offset (0x0BA0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_AMD_HEADER_HB2 AMD - Audio Metadata - Packet Header (byte HB2 - 'NUM_AUDIO_STR' and 'NUM_VIEWS' defaul values defined by HDMI specification) Value After Reset:0x0
15:8	RW	0x00	PKT_AMD_HEADER_HB1 AMD - Audio Metadata - Packet Header (byte HB1 - 'HDMI_3D_Audio' default value defined by HDMI specification) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_AMD_CONTENTS1

Address: Operational Base(0x27DA0000) + offset (0x0BA4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AMD_BODY_PB3_0 AMD - Audio Metadata - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_AMD_CONTENTS2

Address: Operational Base(0x27DA0000) + offset (0x0BA8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AMD_BODY_PB7_4 AMD - Audio Metadata - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_AMD_CONTENTS3

Address: Operational Base(0x27DA0000) + offset (0x0BAC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AMD_BODY_PB11_8 AMD - Audio Metadata - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_AMD_CONTENTS4

Address: Operational Base(0x27DA0000) + offset (0x0BB0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AMD_BODY_PB15_12 AMD - Audio Metadata - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_AMD_CONTENTS5

Address: Operational Base(0x27DA0000) + offset (0x0BB4)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AMD_BODY_PB19_16 AMD - Audio Metadata - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_AMD_CONTENTS6

Address: Operational Base(0x27DA0000) + offset (0x0BB8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AMD_BODY_PB23_20 AMD - Audio Metadata - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_AMD_CONTENTS7

Address: Operational Base(0x27DA0000) + offset (0x0BBC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AMD_BODY_PB27_24 AMD - Audio Metadata - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_VSI_CONTENTS0

Address: Operational Base(0x27DA0000) + offset (0x0BC0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_VSI_HEADER_HB2 VSI - Vendor Specific InfoFrame - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_VSI_HEADER_HB1 VSI - Vendor Specific InfoFrame - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_VSI_CONTENTS1

Address: Operational Base(0x27DA0000) + offset (0x0BC4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_VSI_BODY_PB3_0 VSI - Vendor Specific InfoFrame - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_VSI_CONTENTS2

Address: Operational Base(0x27DA0000) + offset (0x0BC8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_VSI_BODY_PB7_4 VSI - Vendor Specific InfoFrame - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_VSI_CONTENTS3

Address: Operational Base(0x27DA0000) + offset (0x0BCC)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_VSI_BODY_PB11_8 VSI - Vendor Specific InfoFrame - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_VSI_CONTENTS4

Address: Operational Base(0x27DA0000) + offset (0x0BD0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_VSI_BODY_PB15_12 VSI - Vendor Specific InfoFrame - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_VSI_CONTENTS5

Address: Operational Base(0x27DA0000) + offset (0x0BD4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_VSI_BODY_PB19_16 VSI - Vendor Specific InfoFrame - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_VSI_CONTENTS6

Address: Operational Base(0x27DA0000) + offset (0x0BD8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_VSI_BODY_PB23_20 VSI - Vendor Specific InfoFrame - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_VSI_CONTENTS7

Address: Operational Base(0x27DA0000) + offset (0x0BDC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_VSI_BODY_PB27_24 VSI - Vendor Specific InfoFrame - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_AVI_CONTENTS0

Address: Operational Base(0x27DA0000) + offset (0x0BE0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_AVI_HEADER_HB2 AVI - Auxiliary Video InfoFrame - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_AVI_HEADER_HB1 AVI - Auxiliary Video InfoFrame - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_AVI_CONTENTS1

Address: Operational Base(0x27DA0000) + offset (0x0BE4)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AVI_BODY_PB3_0 AVI - Auxiliary Video InfoFrame - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_AVI_CONTENTS2

Address: Operational Base(0x27DA0000) + offset (0x0BE8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AVI_BODY_PB7_4 AVI - Auxiliary Video InfoFrame - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_AVI_CONTENTS3

Address: Operational Base(0x27DA0000) + offset (0x0BEC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AVI_BODY_PB11_8 AVI - Auxiliary Video InfoFrame - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_AVI_CONTENTS4

Address: Operational Base(0x27DA0000) + offset (0x0BF0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AVI_BODY_PB15_12 AVI - Auxiliary Video InfoFrame - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_AVI_CONTENTS5

Address: Operational Base(0x27DA0000) + offset (0x0BF4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AVI_BODY_PB19_16 AVI - Auxiliary Video InfoFrame - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_AVI_CONTENTS6

Address: Operational Base(0x27DA0000) + offset (0x0BF8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AVI_BODY_PB23_20 AVI - Auxiliary Video InfoFrame - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_AVI_CONTENTS7

Address: Operational Base(0x27DA0000) + offset (0x0BFC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AVI_BODY_PB27_24 AVI - Auxiliary Video InfoFrame - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_SPDI_CONTENTS0

Address: Operational Base(0x27DA0000) + offset (0x0C00)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_SPDI_HEADER_HB2 SPDI - Source Product Descriptor InfoFrame - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_SPDI_HEADER_HB1 SPDI - Source Product Descriptor InfoFrame - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_SPDI_CONTENTS1

Address: Operational Base(0x27DA0000) + offset (0x0C04)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_SPDI_BODY_PB3_0 SPDI - Source Product Descriptor InfoFrame - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_SPDI_CONTENTS2

Address: Operational Base(0x27DA0000) + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_SPDI_BODY_PB7_4 SPDI - Source Product Descriptor InfoFrame - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_SPDI_CONTENTS3

Address: Operational Base(0x27DA0000) + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_SPDI_BODY_PB11_8 SPDI - Source Product Descriptor InfoFrame - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_SPDI_CONTENTS4

Address: Operational Base(0x27DA0000) + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_SPDI_BODY_PB15_12 SPDI - Source Product Descriptor InfoFrame - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_SPDI_CONTENTS5

Address: Operational Base(0x27DA0000) + offset (0x0C14)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_SPDI_BODY_PB19_16 SPDI - Source Product Descriptor InfoFrame - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_SPDI_CONTENTS6

Address: Operational Base(0x27DA0000) + offset (0x0C18)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_SPDI_BODY_PB23_20 SPDI - Source Product Descriptor InfoFrame - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_SPDI_CONTENTS7

Address: Operational Base(0x27DA0000) + offset (0x0C1C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_SPDI_BODY_PB27_24 SPDI - Source Product Descriptor InfoFrame - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_AUDI_CONTENTS0

Address: Operational Base(0x27DA0000) + offset (0x0C20)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x0a	PKT_AUDI_HEADER_HB2 AUDI - Audio InfoFrame - Packet Header (byte HB2 - 'Length' default value defined by HDMI specification, shall only be changed for debug purposes) Value After Reset:0xa
15:8	RW	0x01	PKT_AUDI_HEADER_HB1 AUDI - Audio InfoFrame - Packet Header (byte HB1 - 'Version Number' value defined by HDMI specification, shall only be changed for debug purposes) Value After Reset:0x1
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_AUDI_CONTENTS1

Address: Operational Base(0x27DA0000) + offset (0x0C24)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AUDI_BODY_PB3_0 AUDI - Audio InfoFrame - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_AUDI_CONTENTS2

Address: Operational Base(0x27DA0000) + offset (0x0C28)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AUDI_BODY_PB7_4 AUDI - Audio InfoFrame - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_AUDI_CONTENTS3

Address: Operational Base(0x27DA0000) + offset (0x0C2C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AUDI_BODY_PB11_8 AUDI - Audio InfoFrame - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

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HDMI TX Controller_PKT_AUDI_CONTENTS4

Address: Operational Base(0x27DA0000) + offset (0x0C30)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AUDI_BODY_PB15_12 AUDI - Audio InfoFrame - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_AUDI_CONTENTS5

Address: Operational Base(0x27DA0000) + offset (0x0C34)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AUDI_BODY_PB19_16 AUDI - Audio InfoFrame - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_AUDI_CONTENTS6

Address: Operational Base(0x27DA0000) + offset (0x0C38)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AUDI_BODY_PB23_20 AUDI - Audio InfoFrame - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_AUDI_CONTENTS7

Address: Operational Base(0x27DA0000) + offset (0x0C3C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AUDI_BODY_PB27_24 AUDI - Audio InfoFrame - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_NVI_CONTENTS0

Address: Operational Base(0x27DA0000) + offset (0x0C40)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_NVI_HEADER_HB2 NVI - NTSC VBI InfoFrame - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_NVI_HEADER_HB1 NVI - NTSC VBI InfoFrame - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_NVI_CONTENTS1

Address: Operational Base(0x27DA0000) + offset (0x0C44)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NVI_BODY_PB3_0 NVI - NTSC VBI InfoFrame - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_NVI_CONTENTS2

Address: Operational Base(0x27DA0000) + offset (0x0C48)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NVI_BODY_PB7_4 NVI - NTSC VBI InfoFrame - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_NVI_CONTENTS3

Address: Operational Base(0x27DA0000) + offset (0x0C4C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NVI_BODY_PB11_8 NVI - NTSC VBI InfoFrame - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_NVI_CONTENTS4

Address: Operational Base(0x27DA0000) + offset (0x0C50)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NVI_BODY_PB15_12 NVI - NTSC VBI InfoFrame - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_NVI_CONTENTS5

Address: Operational Base(0x27DA0000) + offset (0x0C54)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NVI_BODY_PB19_16 NVI - NTSC VBI InfoFrame - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_NVI_CONTENTS6

Address: Operational Base(0x27DA0000) + offset (0x0C58)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NVI_BODY_PB23_20 NVI - NTSC VBI InfoFrame - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_NVI_CONTENTS7

Address: Operational Base(0x27DA0000) + offset (0x0C5C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NVI_BODY_PB27_24 NVI - NTSC VBI InfoFrame - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_DRMI_CONTENTS0

Address: Operational Base(0x27DA0000) + offset (0x0C60)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_DRMI_HEADER_HB2 DRMI - Dynamic Range and Mastering InfoFrame - Packet Header (byte HB2) Value After Reset:0x0

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	PKT_DRMI_HEADER_HB1 DRMI - Dynamic Range and Mastering InfoFrame - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_DRMI_CONTENTS1

Address: Operational Base(0x27DA0000) + offset (0x0C64)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_DRMI_BODY_PB3_0 DRMI - Dynamic Range and Mastering InfoFrame - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_DRMI_CONTENTS2

Address: Operational Base(0x27DA0000) + offset (0x0C68)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_DRMI_BODY_PB7_4 DRMI - Dynamic Range and Mastering InfoFrame - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_DRMI_CONTENTS3

Address: Operational Base(0x27DA0000) + offset (0x0C6C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_DRMI_BODY_PB11_8 DRMI - Dynamic Range and Mastering InfoFrame - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_DRMI_CONTENTS4

Address: Operational Base(0x27DA0000) + offset (0x0C70)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_DRMI_BODY_PB15_12 DRMI - Dynamic Range and Mastering InfoFrame - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_DRMI_CONTENTS5

Address: Operational Base(0x27DA0000) + offset (0x0C74)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_DRMI_BODY_PB19_16 DRMI - Dynamic Range and Mastering InfoFrame - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_DRMI_CONTENTS6

Address: Operational Base(0x27DA0000) + offset (0x0C78)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_DRMI_BODY_PB23_20 DRMI - Dynamic Range and Mastering InfoFrame - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

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HDMI TX Controller_PKT_DRMI_CONTENTS7

Address: Operational Base(0x27DA0000) + offset (0x0C7C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_DRMI_BODY_PB27_24 DRMI - Dynamic Range and Mastering InfoFrame - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS0

Address: Operational Base(0x27DA0000) + offset (0x0C80)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:16	RW	0x00	PKT_GHDMI1_HEADER_HB2 GHDMI1 - Generic HDMI 1 - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_GHDMI1_HEADER_HB1 GHDMI1 - Generic HDMI 1 - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	PKT_GHDMI1_HEADER_HB0 GHDMI1 - Generic HDMI 1 - Packet Header (byte HB0) Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS1

Address: Operational Base(0x27DA0000) + offset (0x0C84)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI1_BODY_PB3_0 GHDMI1 - Generic HDMI 1 - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS2

Address: Operational Base(0x27DA0000) + offset (0x0C88)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI1_BODY_PB7_4 GHDMI1 - Generic HDMI 1 - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS3

Address: Operational Base(0x27DA0000) + offset (0x0C8C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI1_BODY_PB11_8 GHDMI1 - Generic HDMI 1 - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS4

Address: Operational Base(0x27DA0000) + offset (0x0C90)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI1_BODY_PB15_12 GHDMI1 - Generic HDMI 1 - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS5

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Address: Operational Base(0x27DA0000) + offset (0x0C94)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI1_BODY_PB19_16 GHDMI1 - Generic HDMI 1 - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS6

Address: Operational Base(0x27DA0000) + offset (0x0C98)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI1_BODY_PB23_20 GHDMI1 - Generic HDMI 1 - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS7

Address: Operational Base(0x27DA0000) + offset (0x0C9C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI1_BODY_PB27_24 GHDMI1 - Generic HDMI 1 - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS0

Address: Operational Base(0x27DA0000) + offset (0x0CA0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:16	RW	0x00	PKT_GHDMI2_HEADER_HB2 GHDMI2 - Generic HDMI 2 - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_GHDMI2_HEADER_HB1 GHDMI2 - Generic HDMI 2 - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	PKT_GHDMI2_HEADER_HB0 GHDMI2 - Generic HDMI 2 - Packet Header (byte HB0) Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS1

Address: Operational Base(0x27DA0000) + offset (0x0CA4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI2_BODY_PB3_0 GHDMI2 - Generic HDMI 2 - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS2

Address: Operational Base(0x27DA0000) + offset (0x0CA8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI2_BODY_PB7_4 GHDMI2 - Generic HDMI 2 - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS3

Address: Operational Base(0x27DA0000) + offset (0x0CAC)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI2_BODY_PB11_8 GHDMI2 - Generic HDMI 2 - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS4

Address: Operational Base(0x27DA0000) + offset (0x0CB0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI2_BODY_PB15_12 GHDMI2 - Generic HDMI 2 - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS5

Address: Operational Base(0x27DA0000) + offset (0x0CB4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI2_BODY_PB19_16 GHDMI2 - Generic HDMI 2 - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS6

Address: Operational Base(0x27DA0000) + offset (0x0CB8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI2_BODY_PB23_20 GHDMI2 - Generic HDMI 2 - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS7

Address: Operational Base(0x27DA0000) + offset (0x0CBC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI2_BODY_PB27_24 GHDMI2 - Generic HDMI 2 - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_EMP_CONFIG0

Address: Operational Base(0x27DA0000) + offset (0x0CE0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Reserved0 Reserved Field:Yes
3:1	RW	0x0	EMP_TX_ORDER Extended Metadata Packets transmission order (from left to right): Note 1: Others values not listed are reserved Values: 0x0 (VCX): VTEM, CVTEM, EMP_EXTMEM 0x1 (VXC): VTEM, EMP_EXTMEM, CVTEM 0x2 (CXV): CVTEM, EMP_EXTMEM,VTEM 0x3 (CVX): CVTEM, VTEM, EMP_EXTMEM 0x4 (XVC): EMP_EXTMEM, VTEM, CVTEM 0x5 (XCV): EMP_EXTMEM, CVTEM, VTEM Value After Reset:0x0

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Bit	Attr	Reset Value	Description
0	RW	0x0	EMP_TX_MTW_VIOLATION_EN Extended Metadata Packets transmission control when new MTW begins: Values: 0x0 (EMP_NSTOP_TX): continue to transmit EMPs until the end of the Data Sets loaded by SW for transmission 0x1 (EMP_STOP_TX): stop transmission when the new MTW begins Value After Reset:0x0

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS0

Address: Operational Base(0x27DA0000) + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_EMP_VTEM_HEADER_HB2 VTEM - Video Timing Extended Metadata - Packet Header (byte HB2) Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0
15:8	RW	0x00	PKT_EMP_VTEM_HEADER_HB1 VTEM - Video Timing Extended Metadata - Packet Header (byte HB1) Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS1

Address: Operational Base(0x27DA0000) + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15:0	RW	0x0000	PKT_EMP_VTEM_BODY_PB1_0 VTEM - Video Timing Extended Metadata - Packet Body - bytes {PB1,PB0} Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS2

Address: Operational Base(0x27DA0000) + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	PKT_EMP_VTEM_BODY_PB7_5 VTEM - Video Timing Extended Metadata - Packet Body - bytes {PB7,PB6,PB5} Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS3

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Address: Operational Base(0x27DA0000) + offset (0x0D0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_EMP_VTEM_BODY_PB11_8 VTEM - Video Timing Extended Metadata - Packet Body - bytes {PB11,PB10,PB9,PB8} Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS4

Address: Operational Base(0x27DA0000) + offset (0x0D10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_EMP_VTEM_BODY_PB15_12 VTEM - Video Timing Extended Metadata - Packet Body - bytes {PB15,PB14,PB13,PB12} Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS5

Address: Operational Base(0x27DA0000) + offset (0x0D14)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_EMP_VTEM_BODY_PB19_16 VTEM - Video Timing Extended Metadata - Packet Body - bytes {PB19,PB18,PB17,PB16} Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS6

Address: Operational Base(0x27DA0000) + offset (0x0D18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_EMP_VTEM_BODY_PB23_20 VTEM - Video Timing Extended Metadata - Packet Body - bytes {PB23,PB22,PB21,PB20} Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS7

Address: Operational Base(0x27DA0000) + offset (0x0D1C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_EMP_VTEM_BODY_PB27_24 VTEM - Video Timing Extended Metadata - Packet Body - bytes {PB27,PB26,PB25,PB24} Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_AUDPKT_CONTROL0

Address: Operational Base(0x27DA0000) + offset (0x0E20)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved4 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
20	RW	0x0	AUDPKT_SAMPLE_FLAT_OVR_EN Audio flat / sample invalid bits override enable Values: 0x0 (FLAT_OVR_DIS): Flat bits from audio interface 0x1 (FLAT_OVR_EN): Flat bits override Value After Reset:0x0
19:17	RW	0x0	Reserved3 Reserved Field:Yes
16	RW	0x0	AUDPKT_SAMPLE_PRESENT_OVR_EN Audio sample present bits override enable Values: 0x0 (SPL_PRST_OVR_DIS): Sample present bits from audio interface 0x1 (SPL_PRST_OVR_EN): Sample present bits override Value After Reset:0x0
15:13	RW	0x0	Reserved2 Reserved Field:Yes
12	RW	0x0	AUDPKT_PBIT_FORCE_EN Audio parity bit force enable Values: 0x0 (PARITY_FORCE_DIS): Parity bit from audio interface 0x1 (PARITY_FORCE_EN): Parity bit calculated internally Value After Reset:0x0
11:10	RW	0x0	Reserved1 Reserved Field:Yes
9	RW	0x0	AUDPKT_LAYOUT_OVR_EN Audio Layout bit override enable Values: 0x0 (LAYOUT_OVR_DIS): ENLayout bit estimated in audio interface 0x1 (LAYOUT_OVR_EN): Layout bit override Value After Reset:0x0
8	RW	0x0	AUDPKT_LAYOUT_OVR_VALUE Audio Layout bit override value Value After Reset:0x0
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5	RW	0x0	AUDPKT_DBL_DST_OVR_EN Audio DBL bit override enable Values: 0x0 (DBL_OVR_DIS): DBL bit from audio interface 0x1 (DBL_OVR_EN): DBL bit override Value After Reset:0x0
4	RW	0x0	AUDPKT_DBL_DST_OVR_VALUE Audio DBL bit override value Value After Reset:0x0
3	RW	0x0	AUDPKT_VBIT_OVR_EN Audio Packetizer IEC 60958 Validity bit override enable Note: This field should only be set after the Audio Packetizer Validity bit override registers (audpkt_vbit_ovr*) are configured. Values: 0x0 (VBIT_OVR_DIS): Validity bit from audio interface 0x1 (VBIT_OVR_EN): Validity bit override Value After Reset:0x0

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Bit	Attr	Reset Value	Description
2	RW	0x0	AUDPKT_USRDATA_SPREAD_EN_OVR_VALUE Audio Packetizer IEC 60958 User Data override spread enable when override values are used Note: This field should only be set after the Audio Packetizer User Data override registers (audpkt_usrdata_ovr*) are configured and enabled (audpkt_usrdata_ovr_en=1) Values: 0x0 (USRDATA_OVR_SPREAD_DIS): User Data spread accross the different audio pairs of an audio packet 0x1 (USRDATA_OVR_SPREAD_EN): Same User Data used for all audio pairs of an audio packet Value After Reset:0x0
1	RW	0x0	AUDPKT_USRDATA_OVR_EN Audio Packetizer IEC 60958 User Data override enable Note: This field should only be set after the Audio Packetizer User Data override registers (audpkt_usrdata_ovr*) are configured Values: 0x0 (USRDATA_OVR_DIS): User Data from audio interface 0x1 (USRDATA_OVR_EN): User Data override Value After Reset:0x0
0	RW	0x0	AUDPKT_CHSTATUS_OVR_EN Audio Packetizer IEC 60958 Channel Status override enable Note: This field should only be set after the Audio Packetizer Channel Status override registers (audpkt_chstatus_ovr*) are configured. Values: 0x0 (CHSTATUS_OVR_DIS): Channel status from audio interface 0x1 (CHSTATUS_OVR_EN): Channel status override Value After Reset:0x0

HDMI TX Controller_AUDPKT_CONTROL1

Address: Operational Base(0x27DA0000) + offset (0x0E24)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	AUDPKT_SAMPLE_FLAT_OVR_VALUE Audio flat / sample invalid bits override values Note 1: This register field only takes values greater than 15 when Audio 3D features are present in the configuration (HDMI_QP_TX_AUD_3D == 1) Value After Reset:0x0
15:0	RW	0x0000	AUDPKT_SAMPLE_PRESENT_OVR_VALUE Audio sample present bits override values Note 1: This register field only takes values greater than 15 when Audio 3D features are present in the configuration (HDMI_QP_TX_AUD_3D == 1) Value After Reset:0x0

HDMI TX Controller_AUDPKT_ACR_CONTROL0

Address: Operational Base(0x27DA0000) + offset (0x0E40)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
25	RW	0x0	AUDPKT_ACR_PLL4X_OVR_VALUE Audio Clock Regeneration (ACR) PLL 4x multiplication override value Values: 0x0 (PLL1X_OVR_VAL): PLL 1x 0x1 (PLL4X_OVR_VAL): PLL 4x Value After Reset:0x0
24	RW	0x0	AUDPKT_ACR_PLL4X_OVR_EN Audio Clock Regeneration (ACR) PLL 4x multiplication override enable Values: 0x0 (PLL4X_OVR_DIS): PLL 4x override disabled 0x1 (PLL4X_OVR_EN): PLL 4x override enabled Value After Reset:0x0
23:20	RW	0x0	Reserved0 Reserved Field:Yes
19:0	RW	0x00000	AUDPKT_ACR_N_VALUE Audio Clock Regeneration (ACR) packet N value Note 1: This value is used in the calculation of ACR CTS value and in the composition of the ACR packet. Value After Reset:0x0

HDMI TX Controller_AUDPKT_ACR_CONTROL1

Address: Operational Base(0x27DA0000) + offset (0x0E44)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	AUDPKT_ACR_CTS_OFFSET_VALUE Audio Clock Regeneration (ACR) CTS offset value. This register field can be configured with a positive or negative value that is added to the CTS received in the ACR packet. Note 1: The register must be configured with a value represented in 2's complement Value After Reset:0x0
23:4	RW	0x00000	AUDPKT_ACR_CTS_OVR_VALUE Audio Clock Regeneration (ACR) CTS override value Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RW	0x0	AUDPKT_ACR_CTS_OVR_EN Audio Clock Regeneration (ACR) CTS override enable Values: 0x0 (CTS_OVR_DIS): CTS override disabled 0x1 (CTS_OVR_EN): CTS overrride enabled Value After Reset:0x0
0	RW	0x0	AUDPKT_ACR_CTS_ZERO_NOCHG Audio Clock Regeneration (ACR) CTS send mode Values: 0x0 (CTS_CALC): Sending ACR CTS calculated value, even if no change in relation to the previous CTS sent 0x1 (CTS_ZERO): Sending ACR CTS values of zero to indicate no new value of CTS Value After Reset:0x0

HDMI TX Controller_AUDPKT_ACR_STATUS0

Address: Operational Base(0x27DA0000) + offset (0x0E4C)

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Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes
19:0	RO	0x00000	AUDPKT_ACR_CTS_VALUE Audio Clock Regeneration (ACR) packet CTS calculated value Note: This value is calculated from the ACR N value and used in the composition of the ACR packet. Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR0

Address: Operational Base(0x27DA0000) + offset (0x0E60)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15:0	RW	0x0000	AUDPKT_CHSTATUS_COMMON_BYTES1_0_OVR_VALUE Common Audio Channel Status payload bytes 0 (LSB byte) to 1 Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR1

Address: Operational Base(0x27DA0000) + offset (0x0E64)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_CHSTATUS_COMMON_BYTES6_3_OVR_VALUE Common Audio Channel Status payload bytes 3 (LSB byte) to 6 (MSB byte) Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR2

Address: Operational Base(0x27DA0000) + offset (0x0E68)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_CHSTATUS_COMMON_BYTES10_7_OVR_VALUE Common Audio Channel Status payload bytes 7 (LSB byte) to 10 (MSB byte) Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR3

Address: Operational Base(0x27DA0000) + offset (0x0E6C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_CHSTATUS_COMMON_BYTES14_11_OVR_VALUE Common Audio Channel Status payload bytes 11 (LSB byte) to 14 (MSB byte) Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR4

Address: Operational Base(0x27DA0000) + offset (0x0E70)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_CHSTATUS_COMMON_BYTES18_15_OVR_VALUE Common Audio Channel Status payload bytes 15 (LSB byte) to 18 (MSB byte) Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR5

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Address: Operational Base(0x27DA0000) + offset (0x0E74)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_CHSTATUS_COMMON_BYTES22_19_OVR_VALUE Common Audio Channel Status payload bytes 19 (LSB byte) to 22 (MSB byte) Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR6

Address: Operational Base(0x27DA0000) + offset (0x0E78)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x00	AUDPKT_CHSTATUS_COMMON_BYTE23_OVR_VALUE Common Audio Channel Status payload byte 23 (LSB byte) Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR7

Address: Operational Base(0x27DA0000) + offset (0x0E7C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_CHSTATUS_CHANNELS4_1_BYTE2_OVR_VALUE Channels 1 (LSB byte) to 4 (MSB byte) - Audio Channel Status block payload byte 2 {Source Number, Channel Number} Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR8

Address: Operational Base(0x27DA0000) + offset (0x0E80)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_CHSTATUS_CHANNELS8_5_BYTE2_OVR_VALUE Channels 5 (LSB byte) to 8 (MSB byte) - Audio Channel Status block payload byte 2 {Source Number, Channel Number} Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC0

Address: Operational Base(0x27DA0000) + offset (0x0EA0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_4_1_OVR_VALUE User Data Generic message payload IUs 4 to 1 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 1, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 4. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC1

Address: Operational Base(0x27DA0000) + offset (0x0EA4)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_8_5_OVR_VALUE User Data Generic message payload IUs 8 to 5 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 5, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 8. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC2

Address: Operational Base(0x27DA0000) + offset (0x0EA8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_12_9_OVR_VALUE User Data Generic message payload IUs 12 to 9 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 9, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 12. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC3

Address: Operational Base(0x27DA0000) + offset (0x0EAC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_16_13_OVR_VALUE User Data Generic message payload IUs 16 to 13 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 13, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 16. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC4

Address: Operational Base(0x27DA0000) + offset (0x0EB0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_20_17_OVR_VALUE User Data Generic message payload IUs 20 to 17 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 17, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 20. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC5

Address: Operational Base(0x27DA0000) + offset (0x0EB4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_24_21_OVR_VALUE User Data Generic message payload IUs 24 to 21 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 21, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 24. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC6

Address: Operational Base(0x27DA0000) + offset (0x0EB8)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_28_25_OVR_VALUE User Data Generic message payload IUs 28 to 25 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 25, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 28. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC7

Address: Operational Base(0x27DA0000) + offset (0x0EBC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_32_29_OVR_VALUE User Data Generic message payload IUs 32 to 29 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 29, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 32. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC8

Address: Operational Base(0x27DA0000) + offset (0x0EC0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_36_33_OVR_VALUE User Data Generic message payload IUs 36 to 33 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 33, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 36. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC9

Address: Operational Base(0x27DA0000) + offset (0x0EC4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_40_37_OVR_VALUE User Data Generic message payload IUs 40 to 37 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 37, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 40. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC10

Address: Operational Base(0x27DA0000) + offset (0x0EC8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_44_41_OVR_VALUE User Data Generic message payload IUs 44 to 41 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 41, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 44. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC11

Address: Operational Base(0x27DA0000) + offset (0x0ECC)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_48_45_OVR_VALUE User Data Generic message payload IUs 48 to 45 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 45, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 48. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC12

Address: Operational Base(0x27DA0000) + offset (0x0ED0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_52_49_OVR_VALUE User Data Generic message payload IUs 52 to 49 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 49, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 52. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC13

Address: Operational Base(0x27DA0000) + offset (0x0ED4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_56_53_OVR_VALUE User Data Generic message payload IUs 56 to 53 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 53, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 56. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC14

Address: Operational Base(0x27DA0000) + offset (0x0ED8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_60_57_OVR_VALUE User Data Generic message payload IUs 60 to 57 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 57, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 60. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC15

Address: Operational Base(0x27DA0000) + offset (0x0EDC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_64_61_OVR_VALUE User Data Generic message payload IUs 64 to 61 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 61, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 64. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC16

Address: Operational Base(0x27DA0000) + offset (0x0EE0)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_68_65_OVR_VALUE User Data Generic message payload IUs 68 to 65 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 65, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 68. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC17

Address: Operational Base(0x27DA0000) + offset (0x0EE4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_72_69_OVR_VALUE User Data Generic message payload IUs 72 to 69 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 69, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 72. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC18

Address: Operational Base(0x27DA0000) + offset (0x0EE8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_76_73_OVR_VALUE User Data Generic message payload IUs 76 to 73 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 73, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 76. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC19

Address: Operational Base(0x27DA0000) + offset (0x0EEC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_80_77_OVR_VALUE User Data Generic message payload IUs 80 to 77 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 77, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 80. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC20

Address: Operational Base(0x27DA0000) + offset (0x0EF0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_84_81_OVR_VALUE User Data Generic message payload IUs 84 to 81 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 81, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 84. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC21

Address: Operational Base(0x27DA0000) + offset (0x0EF4)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_88_85_OVR_VALUE User Data Generic message payload IUs 88 to 85 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 85, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 88. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC22

Address: Operational Base(0x27DA0000) + offset (0x0EF8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_92_89_OVR_VALUE User Data Generic message payload IUs 92 to 89 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 89, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 92. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC23

Address: Operational Base(0x27DA0000) + offset (0x0EFC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_96_93_OVR_VALUE User Data Generic message payload IUs 96 to 93 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 93, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 96. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC24

Address: Operational Base(0x27DA0000) + offset (0x0F00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_100_97_OVR_VALUE User Data Generic message payload IUs 100 to 97 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 97, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 100. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC25

Address: Operational Base(0x27DA0000) + offset (0x0F04)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_104_101_OVR_VALUE User Data Generic message payload IUs 104 to 101 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 101, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 104. Only used when audpkt_usrdata_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC26

Address: Operational Base(0x27DA0000) + offset (0x0F08)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_108_105_OVR_VALUE User Data Generic message payload IUs 108 to 105 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 105, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 108. Only used when audpkt_usrdata_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC27

Address: Operational Base(0x27DA0000) + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_112_109_OVR_VALUE User Data Generic message payload IUs 112 to 109 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 109, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 112. Only used when audpkt_usrdata_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC28

Address: Operational Base(0x27DA0000) + offset (0x0F10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_116_113_OVR_VALUE User Data Generic message payload IUs 116 to 113 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 113, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 116. Only used when audpkt_usrdata_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC29

Address: Operational Base(0x27DA0000) + offset (0x0F14)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_120_117_OVR_VALUE User Data Generic message payload IUs 120 to 117 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 117, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 120. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC30

Address: Operational Base(0x27DA0000) + offset (0x0F18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_124_121_OVR_VALUE User Data Generic message payload IUs 124 to 121 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 121, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 124. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC31

Address: Operational Base(0x27DA0000) + offset (0x0F1C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_128_125_OVR_VALUE User Data Generic message payload IUs 128 to 125 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 125, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 128. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC32

Address: Operational Base(0x27DA0000) + offset (0x0F20)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x00	AUDPKT_USRDATA_MSG_GENERIC_IU_129_OVR_VALUE User Data Generic message payload IUs 129 Only used when audpkt_usrdata_ovr_en=1 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 129, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 129. Value After Reset:0x0

HDMI TX Controller_AUDPKT_VBIT_OVR0

Address: Operational Base(0x27DA0000) + offset (0x0F24)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x00	AUDPKT_VBIT_CHANNEL8_1_OVR_VALUE IEC 60958 Validity override value - Channels 1-8 Only used when audpkt_vbit_ovr_en=1 Note: The LSB (bit) of the field corresponds to channel 1 and the MSB (bit) to channel 8. Value After Reset:0x0

HDMI TX Controller_CEC_TX_CONTROL

Address: Operational Base(0x27DA0000) + offset (0x1000)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	WO	0x0	FRAME_SEND_CLR_P Prevents further re-transmissions. If the transmission is ongoing, it is attempted to completion. Value After Reset:0x0
0	WO	0x0	FRAME_SEND_SET_P Set by software to trigger CEC sending a frame as an initiator. If cec_cfg.txreq_discad_ifrxbusy==0, the frame is transmitted even after receiving a frame in between. Otherwise, the frame to be sent is discarded as soon as a new incoming frame arrives (before being able to transmit). Value After Reset:0x0

HDMI TX Controller_CEC_STATUS

Address: Operational Base(0x27DA0000) + offset (0x1004)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
8	RO	0x0	CECTX_BUSY_ST Hardware is busy transmitting a frame. When this bit changes, it generates the cectx_busy_irq interrupt. Value After Reset:0x0
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	RO	0x0	CECRX_BUSY_ST Hardware is busy receiving a message frame. If 'send' is asserted for a new TX message to be sent, it is delayed until the ongoing RX message is done. When this bit changes, it generates the cecrx_busy_irq interrupt. Value After Reset:0x0
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RO	0x0	FRAME_SEND_PENDING_ST Frame send pending status: Values: 0x1 (FRAME_PENDING): A frame is set to be transmitted (waiting for the end of an incoming message or to have access to the line). This bit keeps at 1 while the transmission is going on. 0x0 (NO_FRAME_PENDING): CEC transmission is done (no matter successful or failed). Value After Reset:0x0

HDMI TX Controller_CEC_CONFIG

Address: Operational Base(0x27DA0000) + offset (0x1008)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved3 Reserved Field:Yes
13:12	RW	0x0	SIGNAL_FREE_TIME Selects the Signal Free Time period that is to be respected before attempting to transmit or re-transmit a frame. If 0 is selected then the core follows the HDMI specification in CEC 9.1 Signal free time. Values: 0x0 (AUTO): Follows HDMI specification 0x1 (THREE_BIT_PERIOD): Waits for 3-bit periods before attempt transmission 0x2 (FIVE_BIT_PERIOD): Waits for 5-bit periods before attempt transmission 0x3 (SEVEN_BIT_PERIOD): Waits for 7-bit periods before attempt transmission Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	RW	0x0	RX_AUTOMATIC_DRIVE_ACKNOWLEDGE RX automatic drive acknowledge. Values: 0x0 (WAIT_FOR_INITIATOR_ACK): Wait for initiator to drive logic '1' at ACK/NACK bit position for follower to reply with ACK/NACK bit. 0x1 (DRIVE_ACK): Automatically drive ACK/NACK bit at 2.65 ms of EOM initiator bit. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
8	RW	0x1	CECFILTER Filter enable. Active high. Values: 0x1 (FILTER_ACTIVE): CEC filter is active and filters spurious signals in the CEC line (filter pulses <0.1ms) 0x0 (NO_FILTER): CEC filter inactive Value After Reset:0x1
7:6	RW	0x0	Reserved1 Reserved Field:Yes
5:4	RW	0x1	FRAME_NRETRANS Select number of re-transmission the hardware attempts as initiator after an arbitration loss (cectx_arblost_irq) or line error detection (cectx_lineerror_irq) Values: 0x0 (NO_RETRANS): Re-transmission is not attempt 0x1 (RETRANS_1): Re-transmit one time 0x2 (RETRANS_2): Re-transmit two times 0x3 (RETRANS_3): Re-transmit three times Value After Reset:0x1
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RW	0x0	BROADCAST_NACK Broadcast State. Values: 0x1 (BROADCAST_NACK): Respond with Negative ACK to any received broadcast message. Message not stored in RX registers. 0x0 (RECEIVE_BROADCAST): Receive broadcast messages. Value After Reset:0x0
0	RW	0x0	TXREQ_DISCARD_IF_RXBUSY Transmit request (cec_ctrl.send = 1) is discarded if a RX transfer is ongoing. Values: 0x1 (DISCARD_IF_BUSY): The transmit request is cancelled if there is an ongoing RX transfer on the CEC line, raising the RX busy interrupt. 0x0 (WAIT_TO_TRANSMIT): The transmit request is always recorded by the TX FIFO for immediate or later transmission, depending on the CEC line status. For instance, the transmit is performed as soon as possible. Value After Reset:0x0

HDMI TX Controller_CEC_ADDR

Address: Operational Base(0x27DA0000) + offset (0x100C)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved0 Reserved Field:Yes
14	RW	0x0	CEC_FOLLOWER_ADDR_14 Allocated to the CEC device the Logical address 14 (Specific use) Values: 0x1 (LOGICAL_ADDRESS_14): Logical address 14 - Specific use 0x0 (ADDRESS_NOT_SELECTED): Logical address 14 not allocated Value After Reset:0x0

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Bit	Attr	Reset Value	Description
13	RW	0x0	CEC_FOLLOWER_ADDR_13 Allocated to the CEC device the Logical address 13 (Backup 2) Values: 0x1 (LOGICAL_ADDRESS_13): Logical address 13 - Backup 2 0x0 (ADDRESS_NOT_SELECTED): Logical address 13 not allocated Value After Reset:0x0
12	RW	0x0	CEC_FOLLOWER_ADDR_12 Allocated to the CEC device the Logical address 12 (Backup 1) Values: 0x1 (LOGICAL_ADDRESS_12): Logical address 12 - Backup 1 0x0 (ADDRESS_NOT_SELECTED): Logical address 12 not allocated Value After Reset:0x0
11	RW	0x0	CEC_FOLLOWER_ADDR_11 Allocated to the CEC device the Logical address 11 (Playback Device 3) Values: 0x1 (LOGICAL_ADDRESS_11): Logical address 11 - Playback Device 3 0x0 (ADDRESS_NOT_SELECTED): Logical address 11 not allocated Value After Reset:0x0
10	RW	0x0	CEC_FOLLOWER_ADDR_10 Allocated to the CEC device the Logical address 10 (Tuner 4) Values: 0x1 (LOGICAL_ADDRESS_10): Logical address 10 - Tuner 4 0x0 (ADDRESS_NOT_SELECTED): Logical address 10 not allocated Value After Reset:0x0
9	RW	0x0	CEC_FOLLOWER_ADDR_09 Allocated to the CEC device the Logical address 9 (Recording Device 3) Values: 0x1 (LOGICAL_ADDRESS_09): Logical address 9 - Recording Device 3 0x0 (ADDRESS_NOT_SELECTED): Logical address 9 not allocated Value After Reset:0x0
8	RW	0x0	CEC_FOLLOWER_ADDR_08 Allocated to the CEC device the Logical address 8 (Playback Device 2) Values: 0x1 (LOGICAL_ADDRESS_08): Logical address 8 - Playback Device 2 0x0 (ADDRESS_NOT_SELECTED): Logical address 8 not allocated Value After Reset:0x0
7	RW	0x0	CEC_FOLLOWER_ADDR_07 Allocated to the CEC device the Logical address 7 (Tuner 3) Values: 0x1 (LOGICAL_ADDRESS_07): Logical address 7 - Tuner 3 0x0 (ADDRESS_NOT_SELECTED): Logical address 7 not allocated Value After Reset:0x0

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Bit	Attr	Reset Value	Description
6	RW	0x0	CEC_FOLLOWER_ADDR_06 Allocated to the CEC device the Logical address 6 (Tuner 2) Values: 0x1 (LOGICAL_ADDRESS_06): Logical address 6 - Tuner 2 0x0 (ADDRESS_NOT_SELECTED): Logical address 6 not allocated Value After Reset:0x0
5	RW	0x0	CEC_FOLLOWER_ADDR_05 Allocated to the CEC device the Logical address 5 (Audio System) Values: 0x1 (LOGICAL_ADDRESS_05): Logical address 5 - Audio System 0x0 (ADDRESS_NOT_SELECTED): Logical address 5 not allocated Value After Reset:0x0
4	RW	0x0	CEC_FOLLOWER_ADDR_04 Allocated to the CEC device the Logical address 4 (Playback Device 1) Values: 0x1 (LOGICAL_ADDRESS_04): Logical address 4 - Playback Device 1 0x0 (ADDRESS_NOT_SELECTED): Logical address 4 not allocated Value After Reset:0x0
3	RW	0x0	CEC_FOLLOWER_ADDR_03 Allocated to the CEC device the Logical address 3 (Tuner 1) Values: 0x1 (LOGICAL_ADDRESS_03): Logical address 3 - Tuner 1 0x0 (ADDRESS_NOT_SELECTED): Logical address 3 not allocated Value After Reset:0x0
2	RW	0x0	CEC_FOLLOWER_ADDR_02 Allocated to the CEC device the Logical address 2 (Recording Device 2) Values: 0x1 (LOGICAL_ADDRESS_02): Logical address 2 - Recording Device 2 0x0 (ADDRESS_NOT_SELECTED): Logical address 2 not allocated Value After Reset:0x0
1	RW	0x0	CEC_FOLLOWER_ADDR_01 Allocated to the CEC device the Logical address 1 (Recording Device 1) Values: 0x1 (LOGICAL_ADDRESS_01): Logical address 1 - Recording Device 1 0x0 (ADDRESS_NOT_SELECTED): Logical address 1 not allocated Value After Reset:0x0
0	RW	0x0	CEC_FOLLOWER_ADDR_00 Allocated to the CEC device the Logical address 0 (Device TV) Values: 0x1 (LOGICAL_ADDRESS_00): Logical address 0 - Device TV 0x0 (ADDRESS_NOT_SELECTED): Logical address 0 not allocated Value After Reset:0x0

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HDMI TX Controller_CEC_TX_COUNT

Address: Operational Base(0x27DA0000) + offset (0x1020)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Reserved0 Reserved Field:Yes
3:0	RW	0x0	CEC_TXBUFFER_CNT Frame message size in bytes to be transmitted, including Header and Data blocks. Values: 0x0 (SEND_1_BYTE): Send 1 byte 0x1 (SEND_2_BYTES): Send 2 bytes 0x2 (SEND_3_BYTES): Send 3 bytes 0x3 (SEND_4_BYTES): Send 4 bytes 0x4 (SEND_5_BYTES): Send 5 bytes 0x5 (SEND_6_BYTES): Send 6 bytes 0x6 (SEND_7_BYTES): Send 7 bytes 0x7 (SEND_8_BYTES): Send 8 bytes 0x8 (SEND_9_BYTES): Send 9 bytes 0x9 (SEND_10_BYTES): Send 10 bytes 0xa (SEND_11_BYTES): Send 11 bytes 0xb (SEND_12_BYTES): Send 12 bytes 0xc (SEND_13_BYTES): Send 13 bytes 0xd (SEND_14_BYTES): Send 14 bytes 0xe (SEND_15_BYTES): Send 15 bytes 0xf (SEND_16_BYTES): Send 16 bytes Value After Reset:0x0

HDMI TX Controller_CEC_TX_DATA3_0

Address: Operational Base(0x27DA0000) + offset (0x1024)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	CEC_TXBUFFER_DATA_3 CEC Transmitter Buffer - Byte 3 Value After Reset:0x0
23:16	RW	0x00	CEC_TXBUFFER_DATA_2 CEC Transmitter Buffer - Byte 2 Value After Reset:0x0
15:8	RW	0x00	CEC_TXBUFFER_DATA_1 CEC Transmitter Buffer - Byte 1 Value After Reset:0x0
7:0	RW	0x00	CEC_TXBUFFER_DATA_0 CEC Transmitter Buffer - Byte 0 Value After Reset:0x0

HDMI TX Controller_CEC_TX_DATA7_4

Address: Operational Base(0x27DA0000) + offset (0x1028)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	CEC_TXBUFFER_DATA_7 CEC Transmitter Buffer - Byte 7 Value After Reset:0x0
23:16	RW	0x00	CEC_TXBUFFER_DATA_6 CEC Transmitter Buffer - Byte 6 Value After Reset:0x0
15:8	RW	0x00	CEC_TXBUFFER_DATA_5 CEC Transmitter Buffer - Byte 5 Value After Reset:0x0

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	CEC_TXBUFFER_DATA_4 CEC Transmitter Buffer - Byte 4 Value After Reset:0x0

HDMI TX Controller_CEC_TX_DATA11_8

Address: Operational Base(0x27DA0000) + offset (0x102C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	CEC_TXBUFFER_DATA_11 CEC Transmitter Buffer - Byte 11 Value After Reset:0x0
23:16	RW	0x00	CEC_TXBUFFER_DATA_10 CEC Transmitter Buffer - Byte 10 Value After Reset:0x0
15:8	RW	0x00	CEC_TXBUFFER_DATA_9 CEC Transmitter Buffer - Byte 9 Value After Reset:0x0
7:0	RW	0x00	CEC_TXBUFFER_DATA_8 CEC Transmitter Buffer - Byte 8 Value After Reset:0x0

HDMI TX Controller_CEC_TX_DATA15_12

Address: Operational Base(0x27DA0000) + offset (0x1030)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	CEC_TXBUFFER_DATA_15 CEC Transmitter Buffer - Byte 15 Value After Reset:0x0
23:16	RW	0x00	CEC_TXBUFFER_DATA_14 CEC Transmitter Buffer - Byte 14 Value After Reset:0x0
15:8	RW	0x00	CEC_TXBUFFER_DATA_13 CEC Transmitter Buffer - Byte 13 Value After Reset:0x0
7:0	RW	0x00	CEC_TXBUFFER_DATA_12 CEC Transmitter Buffer - Byte 12 Value After Reset:0x0

HDMI TX Controller_CEC_RX_COUNT_STATUS

Address: Operational Base(0x27DA0000) + offset (0x1040)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved1 Reserved Field:Yes
8	RO	0x0	LOCKED_RXBUFFER_ST Status: Values: 0x1 (MSG_RECEIVED_RXBUFFER_LOCKED): Message is received as follower and is available to be read at cec_rx_cnt /cec_rx_data_XX. Further received messages are NACKed. 0x0 (NEW_MSG_WILL_BE_RECEIVED): A new message can be received. This bit goes to zero, the software writes (cec_lock_ctrl.locked_rxbuffer_clear =1). Value After Reset:0x0
7:4	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	CEC_RXBUFFER_CNT Received frame message size in bytes, including Header and Data blocks: Values: 0x0 (RECEIVED_1_BYTE): 1 byte received 0x1 (RECEIVED_2_BYTES): 2 bytes received 0x2 (RECEIVED_3_BYTES): 3 bytes received 0x3 (RECEIVED_4_BYTES): 4 bytes received 0x4 (RECEIVED_5_BYTES): 5 bytes received 0x5 (RECEIVED_6_BYTES): 6 bytes received 0x6 (RECEIVED_7_BYTES): 7 bytes received 0x7 (RECEIVED_8_BYTES): 8 bytes received 0x8 (RECEIVED_9_BYTES): 9 bytes received 0x9 (RECEIVED_10_BYTES): 10 bytes received 0xa (RECEIVED_11_BYTES): 11 bytes received 0xb (RECEIVED_12_BYTES): 12 bytes received 0xc (RECEIVED_13_BYTES): 13 bytes received 0xd (RECEIVED_14_BYTES): 14 bytes received 0xe (RECEIVED_15_BYTES): 15 bytes received 0xf (RECEIVED_16_BYTES): 16 bytes received Value After Reset:0x0

HDMI TX Controller_CEC_RX_DATA3_0

Address: Operational Base(0x27DA0000) + offset (0x1044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CEC_RXBUFFER_DATA_3 CEC Receiver Buffer - Byte 3 Value After Reset:0x0
23:16	RO	0x00	CEC_RXBUFFER_DATA_2 CEC Receiver Buffer - Byte 2 Value After Reset:0x0
15:8	RO	0x00	CEC_RXBUFFER_DATA_1 CEC Receiver Buffer - Byte 1 Value After Reset:0x0
7:0	RO	0x00	CEC_RXBUFFER_DATA_0 CEC Receiver Buffer - Byte 0 Value After Reset:0x0

HDMI TX Controller_CEC_RX_DATA7_4

Address: Operational Base(0x27DA0000) + offset (0x1048)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CEC_RXBUFFER_DATA_7 CEC Receiver Buffer - Byte 7 Value After Reset:0x0
23:16	RO	0x00	CEC_RXBUFFER_DATA_6 CEC Receiver Buffer - Byte 6 Value After Reset:0x0
15:8	RO	0x00	CEC_RXBUFFER_DATA_5 CEC Receiver Buffer - Byte 5 Value After Reset:0x0
7:0	RO	0x00	CEC_RXBUFFER_DATA_4 CEC Receiver Buffer - Byte 4 Value After Reset:0x0

HDMI TX Controller_CEC_RX_DATA11_8

Address: Operational Base(0x27DA0000) + offset (0x104C)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	CEC_RXBUFFER_DATA_11 CEC Receiver Buffer - Byte 11 Value After Reset:0x0
23:16	RO	0x00	CEC_RXBUFFER_DATA_10 CEC Receiver Buffer - Byte 10 Value After Reset:0x0
15:8	RO	0x00	CEC_RXBUFFER_DATA_9 CEC Receiver Buffer - Byte 9 Value After Reset:0x0
7:0	RO	0x00	CEC_RXBUFFER_DATA_8 CEC Receiver Buffer - Byte 8 Value After Reset:0x0

HDMI TX Controller_CEC_RX_DATA15_12

Address: Operational Base(0x27DA0000) + offset (0x1050)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CEC_RXBUFFER_DATA_15 CEC Receiver Buffer - Byte 15 Value After Reset:0x0
23:16	RO	0x00	CEC_RXBUFFER_DATA_14 CEC Receiver Buffer - Byte 14 Value After Reset:0x0
15:8	RO	0x00	CEC_RXBUFFER_DATA_13 CEC Receiver Buffer - Byte 13 Value After Reset:0x0
7:0	RO	0x00	CEC_RXBUFFER_DATA_12 CEC Receiver Buffer - Byte 12 Value After Reset:0x0

HDMI TX Controller_CEC_LOCK_CONTROL

Address: Operational Base(0x27DA0000) + offset (0x1054)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	LOCKED_RXBUFFER_CLR_P Write 1 to this bit to unlock the RX buffer and allow the controller to receive a new incoming message Value After Reset:0x0

HDMI TX Controller_CEC_RXQUAL_BITTIME_CONFIG

Address: Operational Base(0x27DA0000) + offset (0x1060)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved4 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
18:16	RW	0x3	RXQUAL_FOLLBIT_TIMET8_EARLSTART RX qualifier bit time for T8, the earliest time of the start of a new bit. Any fall edge before this time puts the bit qualifier fsm in abort state. Values: 0x0 (T8_1.90ms): 1.90 ms 0x1 (T8_1.95ms): 1.95 ms 0x2 (T8_2.00ms): 2.00 ms 0x3 (T8_2.04ms): 2.04 ms 0x4 (T8_2.10ms): 2.10 ms 0x5 (T8_2.15ms): 2.15 ms 0x6 (T8_2.20ms): 2.20 ms 0x7 (T8_2.25ms): 2.25 ms Value After Reset:0x3
15	RW	0x0	Reserved3 Reserved Field:Yes
14:12	RW	0x3	RXQUAL_FOLLBIT_TIMET7_LATERETHIGH RX qualifier bit time for T7, the latest return to high time. Any edge after this time puts the bit qualifier fsm in abort state. Values: 0x0 (T7_1.55ms): 1.55 ms 0x1 (T7_1.60ms): 1.60 ms 0x2 (T7_1.65ms): 1.65 ms 0x3 (T7_1.71ms): 1.71 ms 0x4 (T7_1.75ms): 1.75 ms 0x5 (T7_1.80ms): 1.80 ms 0x6 (T7_1.85ms): 1.85 ms 0x7 (T7_1.90ms): 1.90 ms Value After Reset:0x3
11	RW	0x0	Reserved2 Reserved Field:Yes
10:8	RW	0x3	RXQUAL_FOLLBIT_TIMET6_EARLRETHIGH RX qualifier bit time for T6, the earliest return to high time. Any edge before this time puts the bit qualifier fsm in abort state. Values: 0x0 (T6_1.15ms): 1.15 ms 0x1 (T6_1.20ms): 1.20 ms 0x2 (T6_1.25ms): 1.25 ms 0x3 (T6_1.29ms): 1.29 ms 0x4 (T6_1.35ms): 1.35 ms 0x5 (T6_1.40ms): 1.40 ms 0x6 (T6_1.45ms): 1.45 ms 0x7 (T6_1.50ms): 1.50 ms Value After Reset:0x3
7	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
6:4	RW	0x3	RXQUAL_FOLLBIT_TIMET3_LATERETHIGH RX qualifier bit time for T3, the latest return to high time. Any edge after this time puts the bit qualifier fsm in abort state. Values: 0x0 (T3_0.65ms): 0.65 ms 0x1 (T3_0.70ms): 0.70 ms 0x2 (T3_0.75ms): 0.75 ms 0x3 (T3_0.81ms): 0.81 ms 0x4 (T3_0.85ms): 0.85 ms 0x5 (T3_0.90ms): 0.90 ms 0x6 (T3_0.95ms): 0.95 ms 0x7 (T3_1.00ms): 1.00 ms Value After Reset:0x3
3	RW	0x0	Reserved0 Reserved Field:Yes
2:0	RW	0x3	RXQUAL_FOLLBIT_TIMET2_EARLRETHIGH RX qualifier bit time for T2, the earliest return to high time. Any edge before this time puts the bit qualifier fsm in abort state. Values: 0x0 (T2_0.25ms): 0.25 ms 0x1 (T2_0.30ms): 0.30 ms 0x2 (T2_0.35ms): 0.35 ms 0x3 (T2_0.39ms): 0.39 ms 0x4 (T2_0.45ms): 0.45 ms 0x5 (T2_0.50ms): 0.50 ms 0x6 (T2_0.55ms): 0.55 ms 0x7 (T2_0.60ms): 0.60 ms Value After Reset:0x3

HDMI TX Controller_CEC_RX_BITTIME_CONFIG

Address: Operational Base(0x27DA0000) + offset (0x1064)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Reserved5 Reserved Field:Yes
22:20	RW	0x3	RX_FOLLBIT_TIMET9_AUTO_ACK When RX automatic ACK bit is enabled (rx_automatic_drive_acknowledge = 1) and current bit is EOM, the follower drives CEC line to zero thus starting the NACK/ACK bit time. This correspond to the end of a bit (time T9). Note: When RX automatic ACK bit is disabled (rx_automatic_drive_acknowledge = 0), the maximum bit time is defined by rx_follbit_timet9_endframe field register. Values: 0x0 (AUTOACK_T9_2.50ms): 2.50 ms 0x1 (AUTOACK_T9_2.55ms): 2.55 ms 0x2 (AUTOACK_T9_2.60ms): 2.60 ms 0x3 (AUTOACK_T9_2.65ms): 2.65 ms 0x4 (AUTOACK_T9_2.70ms): 2.70 ms 0x5 (AUTOACK_T9_2.75ms): 2.75 ms 0x6 (AUTOACK_T9_2.80ms): 2.80 ms 0x7 (AUTOACK_T9_2.85ms): 2.85 ms Value After Reset:0x3
19	RW	0x0	Reserved4 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
18:16	RW	0x3	RX_STARTBIT_TIMET4_LATEND RX start bit time for T4, the latest time of the start of a new bit. If a fall edge is not detected before this time, the maximum width of a start bit has been exceeded and so the start bit is aborted. Values: 0x0 (T4_4.55ms): 4.55 ms 0x1 (T4_4.60ms): 4.60 ms 0x2 (T4_4.65ms): 4.65 ms 0x3 (T4_4.71ms): 4.71 ms 0x4 (T4_4.75ms): 4.75 ms 0x5 (T4_4.80ms): 4.80 ms 0x6 (T4_4.85ms): 4.85 ms 0x7 (T4_4.90ms): 4.90 ms Value After Reset:0x3
15	RW	0x0	Reserved3 Reserved Field:Yes
14:12	RW	0x3	RX_STARTBIT_TIMET3_EARLEND RX start bit time for T3, the earliest end of a start bit. Any edge before this time aborts the start bit. Values: 0x0 (T3_4.15ms): 4.15 ms 0x1 (T3_4.20ms): 4.20 ms 0x2 (T3_4.25ms): 4.25 ms 0x3 (T3_4.29ms): 4.29 ms 0x4 (T3_4.35ms): 4.35 ms 0x5 (T3_4.40ms): 4.40 ms 0x6 (T3_4.45ms): 4.45 ms 0x7 (T3_4.50ms): 4.50 ms Value After Reset:0x3
11	RW	0x0	Reserved2 Reserved Field:Yes
10:8	RW	0x3	RX_STARTBIT_TIMET2_LATERETHIGH RX start bit time for T2, the earliest return to high time. A fall edge after this time aborts the start bit. Values: 0x0 (T2_3.75ms): 3.75 ms 0x1 (T2_3.80ms): 3.80 ms 0x2 (T2_3.85ms): 3.85 ms 0x3 (T2_3.91ms): 3.91 ms 0x4 (T2_3.95ms): 3.95 ms 0x5 (T2_4.00ms): 4.00 ms 0x6 (T2_4.05ms): 4.05 ms 0x7 (T2_4.10ms): 4.10 ms Value After Reset:0x3
7	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
6:4	RW	0x3	RX_STARTBIT_TIMET1_EARLRETHIGH RX start bit time for T1, the earliest return to high time. Any edge before this time aborts the start bit. Values: 0x0 (T1_3.35ms): 3.35 ms 0x1 (T1_3.40ms): 3.40 ms 0x2 (T1_3.45ms): 3.45 ms 0x3 (T1_3.49ms): 3.49 ms 0x4 (T1_3.55ms): 3.55 ms 0x5 (T1_3.60ms): 3.60 ms 0x6 (T1_3.65ms): 3.65 ms 0x7 (T1_3.70ms): 3.70 ms Value After Reset:0x3
3	RW	0x0	Reserved0 Reserved Field:Yes
2:0	RW	0x3	RX_FOLLBIT_TIMET9_ENDFRAME RX follower bit time for T9, the end of a frame. An edge after this time is considered as part of a new frame. Values: 0x0 (T9_2.60ms): 2.60 ms 0x1 (T9_2.65ms): 2.65 ms 0x2 (T9_2.70ms): 2.70 ms 0x3 (T9_2.76ms): 2.76 ms 0x4 (T9_2.80ms): 2.80 ms 0x5 (T9_2.85ms): 2.85 ms 0x6 (T9_2.90ms): 2.90 ms 0x7 (T9_2.95ms): 2.95 ms Value After Reset:0x3

HDMI TX Controller_CEC_TX_BITTIME_CONFIG

Address: Operational Base(0x27DA0000) + offset (0x1068)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved7 Reserved Field:Yes
30:28	RW	0x6	TX_ROUND_TRIP_DELAY TX round trip delay. The CEC input line is sampled after this delay to check if the drive zero of the CEC output is in fact in the line. This value is greater than the fall edge output delay of the CEC line output. Note: With the filter ON, the values below 0.1 ms works as the interrupt, drive_err_irq triggers since the delay caused by the filter is already greater than the specified value. Values: 0x0 (ROUND_TRIP_DELAY_0.02ms): 0.02 ms 0x1 (ROUND_TRIP_DELAY_0.04ms): 0.04 ms 0x2 (ROUND_TRIP_DELAY_0.06ms): 0.06 ms 0x3 (ROUND_TRIP_DELAY_0.08ms): 0.08 ms 0x4 (ROUND_TRIP_DELAY_0.10ms): 0.10 ms 0x5 (ROUND_TRIP_DELAY_0.13ms): 0.13 ms 0x6 (ROUND_TRIP_DELAY_0.16ms): 0.16 ms 0x7 (ROUND_TRIP_DELAY_0.20ms): 0.20 ms Value After Reset:0x6
27	RW	0x0	Reserved6 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
26:24	RW	0x3	TX_STARTBIT_TIME_RISESAMPLE TX start bit rise sample. This is the time (counted from the fall edge of the startbit) when the CEC input line is sampled to check if the line is zero. Note: From this time on (and until the next bit fall edge), if the CEC line is zero the arbitration lost interrupt is triggered. Values: 0x0 (START_BIT_RISE_SAMPLE_3.75ms): 3.75 ms 0x1 (START_BIT_RISE_SAMPLE_3.80ms): 3.80 ms 0x2 (START_BIT_RISE_SAMPLE_3.85ms): 3.85 ms 0x3 (START_BIT_RISE_SAMPLE_3.91ms): 3.91 ms 0x4 (START_BIT_RISE_SAMPLE_3.95ms): 3.95 ms 0x5 (START_BIT_RISE_SAMPLE_4.00ms): 4.00 ms 0x6 (START_BIT_RISE_SAMPLE_4.05ms): 4.05 ms 0x7 (START_BIT_RISE_SAMPLE_4.10ms): 4.10 ms Value After Reset:0x3
23	RW	0x0	Reserved5 Reserved Field:Yes
22:20	RW	0x4	TX_STARTBIT_TIME_TOTALDURATION TX start bit total duration. This is the time when the next bit starts: Note: When the CEC Filter is enabled, both options 0 and 1, produces a start bit total duration of 4.40 ms, due to the delay added by the filter (0.1 ms). Values: 0x0 (START_BIT_TOTAL_DURATION_4.30ms): 4.30 ms (or 4.40 ms when CEC Filter is enabled) 0x1 (START_BIT_TOTAL_DURATION_4.35ms): 4.35 ms (or 4.40 ms when CEC Filter is enabled) 0x2 (START_BIT_TOTAL_DURATION_4.40ms): 4.40 ms 0x3 (START_BIT_TOTAL_DURATION_4.45ms): 4.45 ms 0x4 (START_BIT_TOTAL_DURATION_4.50ms): 4.50 ms 0x5 (START_BIT_TOTAL_DURATION_4.55ms): 4.55 ms 0x6 (START_BIT_TOTAL_DURATION_4.60ms): 4.60 ms 0x7 (START_BIT_TOTAL_DURATION_4.65ms): 4.65 ms Value After Reset:0x4
19	RW	0x0	Reserved4 Reserved Field:Yes
18:16	RW	0x4	TX_STARTBIT_TIME_LH_TRANS TX start bit low to high transition time. This is the duration of the low period of the start bit. Values: 0x0 (START_BIT_LH_TRANS_3.50ms): 3.50 ms 0x1 (START_BIT_LH_TRANS_3.55ms): 3.55 ms 0x2 (START_BIT_LH_TRANS_3.60ms): 3.60 ms 0x3 (START_BIT_LH_TRANS_3.65ms): 3.65 ms 0x4 (START_BIT_LH_TRANS_3.70ms): 3.70 ms 0x5 (START_BIT_LH_TRANS_3.75ms): 3.75 ms 0x6 (START_BIT_LH_TRANS_3.80ms): 3.80 ms 0x7 (START_BIT_LH_TRANS_3.85ms): 3.85 ms Value After Reset:0x4
15	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
14:12	RW	0x4	TX_ERR_NOTIFY_TIME TX error notify time. This is the duration of the low logic value of the CEC line for an error notification. Values: 0x0 (ERR_NOTIFY_3.40ms): 3.40 ms 0x1 (ERR_NOTIFY_3.45ms): 3.45 ms 0x2 (ERR_NOTIFY_3.50ms): 3.50 ms 0x3 (ERR_NOTIFY_3.55ms): 3.55 ms 0x4 (ERR_NOTIFY_3.60ms): 3.60 ms 0x5 (ERR_NOTIFY_3.65ms): 3.65 ms 0x6 (ERR_NOTIFY_3.70ms): 3.70 ms 0x7 (ERR_NOTIFY_3.75ms): 3.75 ms Value After Reset:0x4
11	RW	0x0	Reserved2 Reserved Field:Yes
10:8	RW	0x4	TX_BIT_TIME_PERIOD TX initiator data bit period. The time when a new consecutive bit starts. Values: 0x0 (BIT_PERIOD_2.20ms): 2.20 ms 0x1 (BIT_PERIOD_2.25ms): 2.25 ms 0x2 (BIT_PERIOD_2.30ms): 2.30 ms 0x3 (BIT_PERIOD_2.35ms): 2.35 ms 0x4 (BIT_PERIOD_2.40ms): 2.40 ms 0x5 (BIT_PERIOD_2.45ms): 2.45 ms 0x6 (BIT_PERIOD_2.50ms): 2.50 ms 0x7 (BIT_PERIOD_2.55ms): 2.55 ms Value After Reset:0x4
7	RW	0x0	Reserved1 Reserved Field:Yes
6:4	RW	0x4	TX_BIT_TIME_RETHIGH TX initiator return to high data bit time when indicating a logic bit 0 (zero). Values: 0x0 (RETHIGH_1.30ms): 1.30 ms 0x1 (RETHIGH_1.35ms): 1.35 ms 0x2 (RETHIGH_1.40ms): 1.40 ms 0x3 (RETHIGH_1.45ms): 1.45 ms 0x4 (RETHIGH_1.50ms): 1.50 ms 0x5 (RETHIGH_1.55ms): 1.55 ms 0x6 (RETHIGH_1.60ms): 1.60 ms 0x7 (RETHIGH_1.65ms): 1.65 ms Value After Reset:0x4
3	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
2:0	RW	0x4	TX_BIT_TIME_LH_TRANS TX initiator low to high data bit transition time when indicating a logical 1 (one). Values: 0x0 (LH_TRANS_0.40ms): 0.40 ms 0x1 (LH_TRANS_0.45ms): 0.45 ms 0x2 (LH_TRANS_0.50ms): 0.50 ms 0x3 (LH_TRANS_0.55ms): 0.55 ms 0x4 (LH_TRANS_0.60ms): 0.60 ms 0x5 (LH_TRANS_0.65ms): 0.65 ms 0x6 (LH_TRANS_0.70ms): 0.70 ms 0x7 (LH_TRANS_0.75ms): 0.75 ms Value After Reset:0x4

HDMI TX Controller_MAIN_INTVEC_INDEX

Address: Operational Base(0x27DA0000) + offset (0x3000)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	RO	0x0	MAINUNIT_1_INTVEC Main unit 1 Interrupt Vector triggered Value After Reset:0x0
0	RO	0x0	MAINUNIT_0_INTVEC Main unit 0 Interrupt Vector triggered Value After Reset:0x0

HDMI TX Controller_MAINUNIT_0_INT_STATUS

Address: Operational Base(0x27DA0000) + offset (0x3010)

Bit	Attr	Reset Value	Description
31	RO	0x0	APB_REGBANK_READY_IRQ Register Bank ready interrupt. Indicates all non-powered off units between AVPUNIT, PKTFIFO, and CEC (HDMI_QP_TX_CEC configs only) are ready. Value After Reset:0x0
30	RW	0x0	Reserved3 Reserved Field:Yes
29	RO	0x0	RESET_MANAGER_STATUS_END_IRQ Reset Manager Init_n/Disable end interrupt Value After Reset:0x0
28:25	RW	0x0	Reserved2 Reserved Field:Yes
24	RO	0x0	TIMER_BASE_LOCKED_IRQ Timer Base locked interrupt Value After Reset:0x0
23	RW	0x0	Reserved1 Reserved Field:Yes
22	RO	0x0	ARC_BPCLK_VALID_STABLE_CHG_IRQ ARC RX Biphase Clock (ARC_bpclk) valid change interrupt. Value After Reset:0x0
21	RO	0x0	ARC_BPCLK_OFF_CHG_IRQ ARC RX Biphase Clock (ARC_bpclk) is off (not running) change interrupt. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
20	RO	0x0	ARC_BPCLK_LOCKED_CHG_IRQ ARC RX Biphase Clock (ARC_bpclk) locked change interrupt. Value After Reset:0x0
19:8	RW	0x000	Reserved0 Reserved Field:Yes
7	RO	0x0	AUDCLK_OFF_CHG_IRQ Audio Clock (audclk) is off (not running) change interrupt. Value After Reset:0x0
6	RO	0x0	AUDCLK_LOCKED_CHG_IRQ Audio Clock (audclk) locked change interrupt. Value After Reset:0x0
5	RO	0x0	LINKQPCLK_OFF_CHG_IRQ Link QP Clock (linkqpclk) is off (not running) change interrupt. Value After Reset:0x0
4	RO	0x0	LINKQPCLK_LOCKED_CHG_IRQ Link QP Clock (linkqpclk) locked change interrupt. Value After Reset:0x0
3	RO	0x0	VIDQPCLK_OFF_CHG_IRQ Video QP Clock (vidqpclk) is off (not running) change interrupt. Value After Reset:0x0
2	RO	0x0	VIDQPCLK_LOCKED_CHG_IRQ Video QP Clock (vidqpclk) locked change interrupt. Value After Reset:0x0
1	RO	0x0	IPI_CLK_OFF_CHG_IRQ IPI Clock (ipi_clk) is off (not running) change interrupt. Value After Reset:0x0
0	RO	0x0	IPI_CLK_LOCKED_CHG_IRQ IPI Clock (ipi_clk) locked change interrupt. Value After Reset:0x0

HDMI TX Controller_MAINUNIT_0_INT_MASK_N

Address: Operational Base(0x27DA0000) + offset (0x3014)

Bit	Attr	Reset Value	Description
31	RW	0x1	APB_REGBANK_READY_MASK_N Mask for apb_regbank_ready_irq. Values: 0x0 (MASK): Write 0 to mask apb_regbank_ready_irq. 0x1 (UNMASK): Write 1 to unmask apb_regbank_ready_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x1
30	RW	0x0	Reserved3 Reserved Field:Yes
29	RW	0x0	RESET_MANAGER_STATUS_END_MASK_N Mask for reset_manager_status_end_irq. Values: 0x0 (MASK): Write 0 to mask reset_manager_status_end_irq. 0x1 (UNMASK): Write 1 to unmask reset_manager_status_end_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
28:25	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
24	RW	0x0	TIMER_BASE_LOCKED_MASK_N Mask for timer_base_locked_irq. Values: 0x0 (MASK): Write 0 to mask timer_base_locked_irq. 0x1 (UNMASK): Write 1 to unmask timer_base_locked_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
23	RW	0x0	Reserved1 Reserved Field:Yes
22	RW	0x0	ARC_BPCLK_VALID_STABLE_CHG_MASK_N Mask for ARC_bpclk_valid_stable_chg_irq. Values: 0x0 (MASK): Write 0 to mask ARC_bpclk_valid_stable_chg_irq. 0x1 (UNMASK): Write 1 to unmask ARC_bpclk_valid_stable_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
21	RW	0x0	ARC_BPCLK_OFF_CHG_MASK_N Mask for ARC_bpclk_off_chg_irq. Values: 0x0 (MASK): Write 0 to mask ARC_bpclk_off_chg_irq. 0x1 (UNMASK): Write 1 to unmask ARC_bpclk_off_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
20	RW	0x0	ARC_BPCLK_LOCKED_CHG_MASK_N Mask for ARC_bpclk_locked_chg_irq. Values: 0x0 (MASK): Write 0 to mask ARC_bpclk_locked_chg_irq. 0x1 (UNMASK): Write 1 to unmask ARC_bpclk_locked_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
19:8	RW	0x000	Reserved0 Reserved Field:Yes
7	RW	0x0	AUDCLK_OFF_CHG_MASK_N Mask for audclk_off_chg_irq. Values: 0x0 (MASK): Write 0 to mask audclk_off_chg_irq. 0x1 (UNMASK): Write 1 to unmask audclk_off_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
6	RW	0x0	AUDCLK_LOCKED_CHG_MASK_N Mask for audclk_locked_chg_irq. Values: 0x0 (MASK): Write 0 to mask audclk_locked_chg_irq. 0x1 (UNMASK): Write 1 to unmask audclk_locked_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
5	RW	0x0	LINKQPCLK_OFF_CHG_MASK_N Mask for linkqpclk_off_chg_irq. Values: 0x0 (MASK): Write 0 to mask linkqpclk_off_chg_irq. 0x1 (UNMASK): Write 1 to unmask linkqpclk_off_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
4	RW	0x0	LINKQPCLK_LOCKED_CHG_MASK_N Mask for linkqpclk_locked_chg_irq. Values: 0x0 (MASK): Write 0 to mask linkqpclk_locked_chg_irq. 0x1 (UNMASK): Write 1 to unmask linkqpclk_locked_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3	RW	0x0	VIDQPCLK_OFF_CHG_MASK_N Mask for vidqpclk_off_chg_irq. Values: 0x0 (MASK): Write 0 to mask vidqpclk_off_chg_irq. 0x1 (UNMASK): Write 1 to unmask vidqpclk_off_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
2	RW	0x0	VIDQPCLK_LOCKED_CHG_MASK_N Mask for vidqpclk_locked_chg_irq. Values: 0x0 (MASK): Write 0 to mask vidqpclk_locked_chg_irq. 0x1 (UNMASK): Write 1 to unmask vidqpclk_locked_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
1	RW	0x0	IPI_CLK_OFF_CHG_MASK_N Mask for ipi_clk_off_chg_irq. Values: 0x0 (MASK): Write 0 to mask ipi_clk_off_chg_irq. 0x1 (UNMASK): Write 1 to unmask ipi_clk_off_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	IPI_CLK_LOCKED_CHG_MASK_N Mask for ipi_clk_locked_chg_irq. Values: 0x0 (MASK): Write 0 to mask ipi_clk_locked_chg_irq. 0x1 (UNMASK): Write 1 to unmask ipi_clk_locked_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_MAINUNIT_0_INT_CLEAR

Address: Operational Base(0x27DA0000) + offset (0x3018)

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Bit	Attr	Reset Value	Description
31	WO	0x0	APB_REGBANK_READY_CLEAR Clear for apb_regbank_ready_irq Values: 0x1 (CLEAR): Write 1 to clear apb_regbank_ready_irq Value After Reset:0x0
30	RW	0x0	Reserved3 Reserved Field:Yes
29	WO	0x0	RESET_MANAGER_STATUS_END_CLEAR Clear for reset_manager_status_end_irq Values: 0x1 (CLEAR): Write 1 to clear reset_manager_status_end_irq Value After Reset:0x0
28:25	RW	0x0	Reserved2 Reserved Field:Yes
24	WO	0x0	TIMER_BASE_LOCKED_CLEAR Clear for timer_base_locked_irq Values: 0x1 (CLEAR): Write 1 to clear timer_base_locked_irq Value After Reset:0x0
23	RW	0x0	Reserved1 Reserved Field:Yes
22	WO	0x0	ARC_BPCLK_VALID_STABLE_CHG_CLEAR Clear for ARC_bpclk_valid_stable_chg_irq Values: 0x1 (CLEAR): Write 1 to clear ARC_bpclk_valid_stable_chg_irq Value After Reset:0x0
21	WO	0x0	ARC_BPCLK_OFF_CHG_CLEAR Clear for ARC_bpclk_off_chg_irq Values: 0x1 (CLEAR): Write 1 to clear ARC_bpclk_off_chg_irq Value After Reset:0x0
20	WO	0x0	ARC_BPCLK_LOCKED_CHG_CLEAR Clear for ARC_bpclk_locked_chg_irq Values: 0x1 (CLEAR): Write 1 to clear ARC_bpclk_locked_chg_irq Value After Reset:0x0
19:8	RW	0x000	Reserved0 Reserved Field:Yes
7	WO	0x0	AUDCLK_OFF_CHG_CLEAR Clear for audclk_off_chg_irq Values: 0x1 (CLEAR): Write 1 to clear audclk_off_chg_irq Value After Reset:0x0
6	WO	0x0	AUDCLK_LOCKED_CHG_CLEAR Clear for audclk_locked_chg_irq Values: 0x1 (CLEAR): Write 1 to clear audclk_locked_chg_irq Value After Reset:0x0
5	WO	0x0	LINKQPCLK_OFF_CHG_CLEAR Clear for linkqpclk_off_chg_irq Values: 0x1 (CLEAR): Write 1 to clear linkqpclk_off_chg_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
4	WO	0x0	LINKQPCLK_LOCKED_CHG_CLEAR Clear for linkqpclk_locked_chg_irq Values: 0x1 (CLEAR): Write 1 to clear linkqpclk_locked_chg_irq Value After Reset:0x0
3	WO	0x0	VIDQPCLK_OFF_CHG_CLEAR Clear for vidqpclk_off_chg_irq Values: 0x1 (CLEAR): Write 1 to clear vidqpclk_off_chg_irq Value After Reset:0x0
2	WO	0x0	VIDQPCLK_LOCKED_CHG_CLEAR Clear for vidqpclk_locked_chg_irq Values: 0x1 (CLEAR): Write 1 to clear vidqpclk_locked_chg_irq Value After Reset:0x0
1	WO	0x0	IPI_CLK_OFF_CHG_CLEAR Clear for ipi_clk_off_chg_irq Values: 0x1 (CLEAR): Write 1 to clear ipi_clk_off_chg_irq Value After Reset:0x0
0	WO	0x0	IPI_CLK_LOCKED_CHG_CLEAR Clear for ipi_clk_locked_chg_irq Values: 0x1 (CLEAR): Write 1 to clear ipi_clk_locked_chg_irq Value After Reset:0x0

HDMI TX Controller_MAINUNIT_0_INT_FORCE

Address: Operational Base(0x27DA0000) + offset (0x301C)

Bit	Attr	Reset Value	Description
31	WO	0x0	APB_REGBANK_READY_FORCE Force for apb_regbank_ready_irq Values: 0x1 (FORCE): Write 1 to trigger apb_regbank_ready_irq Value After Reset:0x0
30	RW	0x0	Reserved3 Reserved Field:Yes
29	WO	0x0	RESET_MANAGER_STATUS_END_FORCE Force for reset_manager_status_end_irq Values: 0x1 (FORCE): Write 1 to trigger reset_manager_status_end_irq Value After Reset:0x0
28:25	RW	0x0	Reserved2 Reserved Field:Yes
24	WO	0x0	TIMER_BASE_LOCKED_FORCE Force for timer_base_locked_irq Values: 0x1 (FORCE): Write 1 to trigger timer_base_locked_irq Value After Reset:0x0
23	RW	0x0	Reserved1 Reserved Field:Yes
22	WO	0x0	ARC_BPCLK_VALID_STABLE_CHG_FORCE Force for ARC_bpclk_valid_stable_chg_irq Values: 0x1 (FORCE): Write 1 to trigger ARC_bpclk_valid_stable_chg_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
21	WO	0x0	ARC_BPCLK_OFF_CHG_FORCE Force for ARC_bpclk_off_chg_irq Values: 0x1 (FORCE): Write 1 to trigger ARC_bpclk_off_chg_irq Value After Reset:0x0
20	WO	0x0	ARC_BPCLK_LOCKED_CHG_FORCE Force for ARC_bpclk_locked_chg_irq Values: 0x1 (FORCE): Write 1 to trigger ARC_bpclk_locked_chg_irq Value After Reset:0x0
19:8	RW	0x000	Reserved0 Reserved Field:Yes
7	WO	0x0	AUDCLK_OFF_CHG_FORCE Force for audclk_off_chg_irq Values: 0x1 (FORCE): Write 1 to trigger audclk_off_chg_irq Value After Reset:0x0
6	WO	0x0	AUDCLK_LOCKED_CHG_FORCE Force for audclk_locked_chg_irq Values: 0x1 (FORCE): Write 1 to trigger audclk_locked_chg_irq Value After Reset:0x0
5	WO	0x0	LINKQPCLK_OFF_CHG_FORCE Force for linkqpclk_off_chg_irq Values: 0x1 (FORCE): Write 1 to trigger linkqpclk_off_chg_irq Value After Reset:0x0
4	WO	0x0	LINKQPCLK_LOCKED_CHG_FORCE Force for linkqpclk_locked_chg_irq Values: 0x1 (FORCE): Write 1 to trigger linkqpclk_locked_chg_irq Value After Reset:0x0
3	WO	0x0	VIDQPCLK_OFF_CHG_FORCE Force for vidqpclk_off_chg_irq Values: 0x1 (FORCE): Write 1 to trigger vidqpclk_off_chg_irq Value After Reset:0x0
2	WO	0x0	VIDQPCLK_LOCKED_CHG_FORCE Force for vidqpclk_locked_chg_irq Values: 0x1 (FORCE): Write 1 to trigger vidqpclk_locked_chg_irq Value After Reset:0x0
1	WO	0x0	IPI_CLK_OFF_CHG_FORCE Force for ipi_clk_off_chg_irq Values: 0x1 (FORCE): Write 1 to trigger ipi_clk_off_chg_irq Value After Reset:0x0
0	WO	0x0	IPI_CLK_LOCKED_CHG_FORCE Force for ipi_clk_locked_chg_irq Values: 0x1 (FORCE): Write 1 to trigger ipi_clk_locked_chg_irq Value After Reset:0x0

HDMI TX Controller_MAINUNIT_1_INT_STATUS

Address: Operational Base(0x27DA0000) + offset (0x3020)

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Bit	Attr	Reset Value	Description
31:23	RW	0x000	Reserved2 Reserved Field:Yes
22	RO	0x0	FLT_EXIT_TO_LTSL_IRQ Indicates a transition from FRL Link Training LTS:3 to LTS:L Value After Reset:0x0
21	RO	0x0	FLT_EXIT_TO_LTS4_IRQ Indicates a transition from FRL Link Training LTS:3 to LTS:4 Value After Reset:0x0
20	RO	0x0	FLT_EXIT_TO_LTSP_IRQ Indicates a transition from FRL Link Training LTS:3 to LTS:P Value After Reset:0x0
19:13	RW	0x00	Reserved1 Reserved Field:Yes
12	RO	0x0	SCDC_NACK_RCVD_IRQ Indicates that SCDC has received a NACK from I2C Master Value After Reset:0x0
11	RO	0x0	SCDC_RR_REPLY_STOP_IRQ Indicates that Source has replied with STOP to a Read Request Value After Reset:0x0
10	RO	0x0	SCDC_UPD_FLAGS_CLR_IRQ Indicates that Update Flags were cleared Value After Reset:0x0
9	RO	0x0	SCDC_UPD_FLAGS_CHG_IRQ Indicates that Update Flags have changed Value After Reset:0x0
8	RO	0x0	SCDC_UPD_FLAGS_RD_IRQ Indicates that Update Flags were read Value After Reset:0x0
7:3	RW	0x00	Reserved0 Reserved Field:Yes
2	RO	0x0	I2CM_NACK_RCVD_IRQ Indicates that I2C Master has received a NACK Value After Reset:0x0
1	RO	0x0	I2CM_READ_REQUEST_IRQ Indicates that I2C Master has received an SCDC Read Request Value After Reset:0x0
0	RO	0x0	I2CM_OP_DONE_IRQ Indicates that I2C Master operation has finished Value After Reset:0x0

HDMI TX Controller_MAINUNIT_1_INT_MASK_N

Address: Operational Base(0x27DA0000) + offset (0x3024)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Reserved2 Reserved Field:Yes
22	RW	0x0	FLT_EXIT_TO_LTSL_MASK_N Mask for flt_exit_to_ltsl_irq. Values: 0x0 (MASK): Write 0 to mask flt_exit_to_ltsl_irq. 0x1 (UNMASK): Write 1 to unmask flt_exit_to_ltsl_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
21	RW	0x0	FLT_EXIT_TO_LTS4_MASK_N Mask for flt_exit_to_lts4_irq. Values: 0x0 (MASK): Write 0 to mask flt_exit_to_lts4_irq. 0x1 (UNMASK): Write 1 to unmask flt_exit_to_lts4_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
20	RW	0x0	FLT_EXIT_TO_LTSP_MASK_N Mask for flt_exit_to_ltsp_irq. Values: 0x0 (MASK): Write 0 to mask flt_exit_to_ltsp_irq. 0x1 (UNMASK): Write 1 to unmask flt_exit_to_ltsp_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
19:13	RW	0x00	Reserved1 Reserved Field:Yes
12	RW	0x0	SCDC_NACK_RCVD_MASK_N Mask for scdc_nack_rcvd_irq. Values: 0x0 (MASK): Write 0 to mask scdc_nack_rcvd_irq. 0x1 (UNMASK): Write 1 to unmask scdc_nack_rcvd_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
11	RW	0x0	SCDC_RR_REPLY_STOP_MASK_N Mask for scdc_rr_reply_stop_irq. Values: 0x0 (MASK): Write 0 to mask scdc_rr_reply_stop_irq. 0x1 (UNMASK): Write 1 to unmask scdc_rr_reply_stop_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
10	RW	0x0	SCDC_UPD_FLAGS_CLR_MASK_N Mask for scdc_upd_flags_clr_irq. Values: 0x0 (MASK): Write 0 to mask scdc_upd_flags_clr_irq. 0x1 (UNMASK): Write 1 to unmask scdc_upd_flags_clr_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
9	RW	0x0	SCDC_UPD_FLAGS_CHG_MASK_N Mask for scdc_upd_flags_chg_irq. Values: 0x0 (MASK): Write 0 to mask scdc_upd_flags_chg_irq. 0x1 (UNMASK): Write 1 to unmask scdc_upd_flags_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
8	RW	0x0	SCDC_UPD_FLAGS_RD_MASK_N Mask for scdc_upd_flags_rd_irq. Values: 0x0 (MASK): Write 0 to mask scdc_upd_flags_rd_irq. 0x1 (UNMASK): Write 1 to unmask scdc_upd_flags_rd_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
7:3	RW	0x00	Reserved0 Reserved Field:Yes
2	RW	0x0	I2CM_NACK_RCVD_MASK_N Mask for i2cm_nack_rcvd_irq. Values: 0x0 (MASK): Write 0 to mask i2cm_nack_rcvd_irq. 0x1 (UNMASK): Write 1 to unmask i2cm_nack_rcvd_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
1	RW	0x0	I2CM_READ_REQUEST_MASK_N Mask for i2cm_read_request_irq. Values: 0x0 (MASK): Write 0 to mask i2cm_read_request_irq. 0x1 (UNMASK): Write 1 to unmask i2cm_read_request_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	I2CM_OP_DONE_MASK_N Mask for i2cm_op_done_irq. Values: 0x0 (MASK): Write 0 to mask i2cm_op_done_irq. 0x1 (UNMASK): Write 1 to unmask i2cm_op_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_MAINUNIT_1_INT_CLEAR

Address: Operational Base(0x27DA0000) + offset (0x3028)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Reserved2 Reserved Field:Yes
22	WO	0x0	FLT_EXIT_TO_LTSL_CLEAR Clear for flt_exit_to_ltsl_irq Values: 0x1 (CLEAR): Write 1 to clear flt_exit_to_ltsl_irq Value After Reset:0x0
21	WO	0x0	FLT_EXIT_TO_LTS4_CLEAR Clear for flt_exit_to_lts4_irq Values: 0x1 (CLEAR): Write 1 to clear flt_exit_to_lts4_irq Value After Reset:0x0
20	WO	0x0	FLT_EXIT_TO_LTSP_CLEAR Clear for flt_exit_to_ltsp_irq Values: 0x1 (CLEAR): Write 1 to clear flt_exit_to_ltsp_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
19:13	RW	0x00	Reserved1 Reserved Field:Yes
12	WO	0x0	SCDC_NACK_RCVD_CLEAR Clear for scdc_nack_rcvd_irq Values: 0x1 (CLEAR): Write 1 to clear scdc_nack_rcvd_irq Value After Reset:0x0
11	WO	0x0	SCDC_RR_REPLY_STOP_CLEAR Clear for scdc_rr_reply_stop_irq Values: 0x1 (CLEAR): Write 1 to clear scdc_rr_reply_stop_irq Value After Reset:0x0
10	WO	0x0	SCDC_UPD_FLAGS_CLR_CLEAR Clear for scdc_upd_flags_clr_irq Values: 0x1 (CLEAR): Write 1 to clear scdc_upd_flags_clr_irq Value After Reset:0x0
9	WO	0x0	SCDC_UPD_FLAGS_CHG_CLEAR Clear for scdc_upd_flags_chg_irq Values: 0x1 (CLEAR): Write 1 to clear scdc_upd_flags_chg_irq Value After Reset:0x0
8	WO	0x0	SCDC_UPD_FLAGS_RD_CLEAR Clear for scdc_upd_flags_rd_irq Values: 0x1 (CLEAR): Write 1 to clear scdc_upd_flags_rd_irq Value After Reset:0x0
7:3	RW	0x00	Reserved0 Reserved Field:Yes
2	WO	0x0	I2CM_NACK_RCVD_CLEAR Clear for i2cm_nack_rcvd_irq Values: 0x1 (CLEAR): Write 1 to clear i2cm_nack_rcvd_irq Value After Reset:0x0
1	WO	0x0	I2CM_READ_REQUEST_CLEAR Clear for i2cm_read_request_irq Values: 0x1 (CLEAR): Write 1 to clear i2cm_read_request_irq Value After Reset:0x0
0	WO	0x0	I2CM_OP_DONE_CLEAR Clear for i2cm_op_done_irq Values: 0x1 (CLEAR): Write 1 to clear i2cm_op_done_irq Value After Reset:0x0

HDMI TX Controller_MAINUNIT_1_INT_FORCE

Address: Operational Base(0x27DA0000) + offset (0x302C)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Reserved2 Reserved Field:Yes
22	WO	0x0	FLT_EXIT_TO_LTSL_FORCE Force for flt_exit_to_ltsl_irq Values: 0x1 (FORCE): Write 1 to trigger flt_exit_to_ltsl_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
21	WO	0x0	FLT_EXIT_TO_LTS4_FORCE Force for flt_exit_to_lts4_irq Values: 0x1 (FORCE): Write 1 to trigger flt_exit_to_lts4_irq Value After Reset:0x0
20	WO	0x0	FLT_EXIT_TO_LTSP_FORCE Force for flt_exit_to_ltsp_irq Values: 0x1 (FORCE): Write 1 to trigger flt_exit_to_ltsp_irq Value After Reset:0x0
19:13	RW	0x00	Reserved1 Reserved Field:Yes
12	WO	0x0	SCDC_NACK_RCVD_FORCE Force for scdc_nack_rcvd_irq Values: 0x1 (FORCE): Write 1 to trigger scdc_nack_rcvd_irq Value After Reset:0x0
11	WO	0x0	SCDC_RR_REPLY_STOP_FORCE Force for scdc_rr_reply_stop_irq Values: 0x1 (FORCE): Write 1 to trigger scdc_rr_reply_stop_irq Value After Reset:0x0
10	WO	0x0	SCDC_UPD_FLAGS_CLR_FORCE Force for scdc_upd_flags_clr_irq Values: 0x1 (FORCE): Write 1 to trigger scdc_upd_flags_clr_irq Value After Reset:0x0
9	WO	0x0	SCDC_UPD_FLAGS_CHG_FORCE Force for scdc_upd_flags_chg_irq Values: 0x1 (FORCE): Write 1 to trigger scdc_upd_flags_chg_irq Value After Reset:0x0
8	WO	0x0	SCDC_UPD_FLAGS_RD_FORCE Force for scdc_upd_flags_rd_irq Values: 0x1 (FORCE): Write 1 to trigger scdc_upd_flags_rd_irq Value After Reset:0x0
7:3	RW	0x00	Reserved0 Reserved Field:Yes
2	WO	0x0	I2CM_NACK_RCVD_FORCE Force for i2cm_nack_rcvd_irq Values: 0x1 (FORCE): Write 1 to trigger i2cm_nack_rcvd_irq Value After Reset:0x0
1	WO	0x0	I2CM_READ_REQUEST_FORCE Force for i2cm_read_request_irq Values: 0x1 (FORCE): Write 1 to trigger i2cm_read_request_irq Value After Reset:0x0
0	WO	0x0	I2CM_OP_DONE_FORCE Force for i2cm_op_done_irq Values: 0x1 (FORCE): Write 1 to trigger i2cm_op_done_irq Value After Reset:0x0

HDMI TX Controller_AVP_INTVEC_INDEX

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Address: Operational Base(0x27DA0000) + offset (0x3800)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	Reserved0 Reserved Field:Yes
6	RO	0x0	AVP_6_INTVEC AVP 6 Interrupt Vector triggered Value After Reset:0x0
5	RO	0x0	AVP_5_INTVEC AVP 5 Interrupt Vector triggered Value After Reset:0x0
4	RO	0x0	AVP_4_INTVEC AVP 4 Interrupt Vector triggered Value After Reset:0x0
3	RO	0x0	AVP_3_INTVEC AVP 3 Interrupt Vector triggered Value After Reset:0x0
2	RO	0x0	AVP_2_INTVEC AVP 2 Interrupt Vector triggered Value After Reset:0x0
1	RO	0x0	AVP_1_INTVEC AVP 1 Interrupt Vector triggered Value After Reset:0x0
0	RO	0x0	AVP_0_INTVEC AVP 0 Interrupt Vector triggered Value After Reset:0x0

HDMI TX Controller_AVP_0_INT_STATUS

Address: Operational Base(0x27DA0000) + offset (0x3810)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved6 Reserved Field:Yes
24	RO	0x0	AUDPKT_INVALID_SAMPLE_PRESENT_IRQ Audio Packetizer Invalid Sample_Present bits configuration interrupt Value After Reset:0x0
23:21	RW	0x0	Reserved5 Reserved Field:Yes
20	RO	0x0	PKTZ_FRLCHAR_FIFO_OVF_IRQ Packetizer FIFO Overflow interrupt. Value After Reset:0x0
19:17	RW	0x0	Reserved4 Reserved Field:Yes
16	RO	0x0	AUDFIFO_UDF_IRQ Audio Interface FIFO Underflow interrupt. Value After Reset:0x0
15:13	RW	0x0	Reserved3 Reserved Field:Yes
12	RO	0x0	TMDSFIFO_OVF_IRQ Detected TMDS FIFO Overflow interrupt. Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
9	RO	0x0	EMP_TX_MTW_VIOLATION_IRQ Extended Metada Packets loaded by software were not all transmitted within a single MTW. If emp_tx_mtw_violation_en=1, the EMP Packet Scheduler continues to send the EMP packets until transmission is complete. Value After Reset:0x0
8	RO	0x0	EMP_TX_DONE_IRQ All Extended Metada Packets loaded by software were successfully transmitted. Value After Reset:0x0
7	RW	0x0	Reserved1 Reserved Field:Yes
6	RO	0x0	EMP_CVTEM_TX_DONE_IRQ CVTEM were successfully transmitted. Value After Reset:0x0
5	RO	0x0	EMP_VTEM_TX_DONE_IRQ VTEM were successfully transmitted. Value After Reset:0x0
4	RO	0x0	DEFAULT_PHASE_VIO_IRQ Default Phase rule violation Value After Reset:0x0
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RO	0x0	IPI_NOT_SUPPORTED_IRQ Detected IPI format and/or color depth not supported interrupt Note: Interrupt only active when ipi_override_map=0 Value After Reset:0x0

HDMI TX Controller_AVP_0_INT_MASK_N

Address: Operational Base(0x27DA0000) + offset (0x3814)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved6 Reserved Field:Yes
24	RW	0x0	AUDPKT_INVALID_SAMPLE_PRESENT_MASK_N Mask for audpkt_invalid_sample_present_irq. Values: 0x0 (MASK): Write 0 to mask audpkt_invalid_sample_present_irq. 0x1 (UNMASK): Write 1 to unmask audpkt_invalid_sample_present_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
23:21	RW	0x0	Reserved5 Reserved Field:Yes
20	RW	0x0	PKTZ_FRLCHAR_FIFO_OVF_MASK_N Mask for pktz_frlchar_fifo_ovf_irq. Values: 0x0 (MASK): Write 0 to mask pktz_frlchar_fifo_ovf_irq. 0x1 (UNMASK): Write 1 to unmask pktz_frlchar_fifo_ovf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
19:17	RW	0x0	Reserved4 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
16	RW	0x0	AUDFIFO_UDF_MASK_N Mask for audfifo_udf_irq. Values: 0x0 (MASK): Write 0 to mask audfifo_udf_irq. 0x1 (UNMASK): Write 1 to unmask audfifo_udf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
15:13	RW	0x0	Reserved3 Reserved Field:Yes
12	RW	0x0	TMDSFIFO_OVF_MASK_N Mask for tmdsfifo_ovf_irq. Values: 0x0 (MASK): Write 0 to mask tmdsfifo_ovf_irq. 0x1 (UNMASK): Write 1 to unmask tmdsfifo_ovf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	RW	0x0	EMP_TX_MTW_VIOLATION_MASK_N Mask for emp_tx_mtw_violation_irq. Values: 0x0 (MASK): Write 0 to mask emp_tx_mtw_violation_irq. 0x1 (UNMASK): Write 1 to unmask emp_tx_mtw_violation_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
8	RW	0x0	EMP_TX_DONE_MASK_N Mask for emp_tx_done_irq. Values: 0x0 (MASK): Write 0 to mask emp_tx_done_irq. 0x1 (UNMASK): Write 1 to unmask emp_tx_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
7	RW	0x0	Reserved1 Reserved Field:Yes
6	RW	0x0	EMP_CVTEM_TX_DONE_MASK_N Mask for emp_cvtem_tx_done_irq. Values: 0x0 (MASK): Write 0 to mask emp_cvtem_tx_done_irq. 0x1 (UNMASK): Write 1 to unmask emp_cvtem_tx_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
5	RW	0x0	EMP_VTEM_TX_DONE_MASK_N Mask for emp_vtem_tx_done_irq. Values: 0x0 (MASK): Write 0 to mask emp_vtem_tx_done_irq. 0x1 (UNMASK): Write 1 to unmask emp_vtem_tx_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
4	RW	0x0	DEFAULT_PHASE_VIO_MASK_N Mask for default_phase_vio_irq. Values: 0x0 (MASK): Write 0 to mask default_phase_vio_irq. 0x1 (UNMASK): Write 1 to unmask default_phase_vio_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	IPI_NOT_SUPPORTED_MASK_N Mask for ipi_not_supported_irq. Values: 0x0 (MASK): Write 0 to mask ipi_not_supported_irq. 0x1 (UNMASK): Write 1 to unmask ipi_not_supported_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_AVP_0_INT_CLEAR

Address: Operational Base(0x27DA0000) + offset (0x3818)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved6 Reserved Field:Yes
24	WO	0x0	AUDPKT_INVALID_SAMPLE_PRESENT_CLEAR Clear for audpkt_invalid_sample_present_irq Values: 0x1 (CLEAR): Write 1 to clear audpkt_invalid_sample_present_irq Value After Reset:0x0
23:21	RW	0x0	Reserved5 Reserved Field:Yes
20	WO	0x0	PKTZ_FRLCHAR_FIFO_OVF_CLEAR Clear for pktz_frlchar_fifo_ovf_irq Values: 0x1 (CLEAR): Write 1 to clear pktz_frlchar_fifo_ovf_irq Value After Reset:0x0
19:17	RW	0x0	Reserved4 Reserved Field:Yes
16	WO	0x0	AUDFIFO_UDF_CLEAR Clear for audfifo_udf_irq Values: 0x1 (CLEAR): Write 1 to clear audfifo_udf_irq Value After Reset:0x0
15:13	RW	0x0	Reserved3 Reserved Field:Yes
12	WO	0x0	TMDSFIFO_OVF_CLEAR Clear for tmdsfifo_ovf_irq Values: 0x1 (CLEAR): Write 1 to clear tmdsfifo_ovf_irq Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
9	WO	0x0	EMP_TX_MTW_VIOLATION_CLEAR Clear for emp_tx_mtw_violation_irq Values: 0x1 (CLEAR): Write 1 to clear emp_tx_mtw_violation_irq Value After Reset:0x0
8	WO	0x0	EMP_TX_DONE_CLEAR Clear for emp_tx_done_irq Values: 0x1 (CLEAR): Write 1 to clear emp_tx_done_irq Value After Reset:0x0
7	RW	0x0	Reserved1 Reserved Field:Yes
6	WO	0x0	EMP_CVTEM_TX_DONE_CLEAR Clear for emp_cvtem_tx_done_irq Values: 0x1 (CLEAR): Write 1 to clear emp_cvtem_tx_done_irq Value After Reset:0x0
5	WO	0x0	EMP_VTEM_TX_DONE_CLEAR Clear for emp_vtem_tx_done_irq Values: 0x1 (CLEAR): Write 1 to clear emp_vtem_tx_done_irq Value After Reset:0x0
4	WO	0x0	DEFAULT_PHASE_VIO_CLEAR Clear for default_phase_vio_irq Values: 0x1 (CLEAR): Write 1 to clear default_phase_vio_irq Value After Reset:0x0
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	WO	0x0	IPI_NOT_SUPPORTED_CLEAR Clear for ipi_not_supported_irq Values: 0x1 (CLEAR): Write 1 to clear ipi_not_supported_irq Value After Reset:0x0

HDMI TX Controller_AVP_0_INT_FORCE

Address: Operational Base(0x27DA0000) + offset (0x381C)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved6 Reserved Field:Yes
24	WO	0x0	AUDPKT_INVALID_SAMPLE_PRESENT_FORCE Force for audpkt_invalid_sample_present_irq Values: 0x1 (FORCE): Write 1 to trigger audpkt_invalid_sample_present_irq Value After Reset:0x0
23:21	RW	0x0	Reserved5 Reserved Field:Yes
20	WO	0x0	PKTZ_FRLCHAR_FIFO_OVF_FORCE Force for pktz_frlchar_fifo_ovf_irq Values: 0x1 (FORCE): Write 1 to trigger pktz_frlchar_fifo_ovf_irq Value After Reset:0x0
19:17	RW	0x0	Reserved4 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
16	WO	0x0	AUDFIFO_UDF_FORCE Force for audfifo_udf_irq Values: 0x1 (FORCE): Write 1 to trigger audfifo_udf_irq Value After Reset:0x0
15:13	RW	0x0	Reserved3 Reserved Field:Yes
12	WO	0x0	TMDSFIFO_OVF_FORCE Force for tmdsfifo_ovf_irq Values: 0x1 (FORCE): Write 1 to trigger tmdsfifo_ovf_irq Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	WO	0x0	EMP_TX_MTW_VIOLATION_FORCE Force for emp_tx_mtw_violation_irq Values: 0x1 (FORCE): Write 1 to trigger emp_tx_mtw_violation_irq Value After Reset:0x0
8	WO	0x0	EMP_TX_DONE_FORCE Force for emp_tx_done_irq Values: 0x1 (FORCE): Write 1 to trigger emp_tx_done_irq Value After Reset:0x0
7	RW	0x0	Reserved1 Reserved Field:Yes
6	WO	0x0	EMP_CVTEM_TX_DONE_FORCE Force for emp_cvtem_tx_done_irq Values: 0x1 (FORCE): Write 1 to trigger emp_cvtem_tx_done_irq Value After Reset:0x0
5	WO	0x0	EMP_VTEM_TX_DONE_FORCE Force for emp_vtem_tx_done_irq Values: 0x1 (FORCE): Write 1 to trigger emp_vtem_tx_done_irq Value After Reset:0x0
4	WO	0x0	DEFAULT_PHASE_VIO_FORCE Force for default_phase_vio_irq Values: 0x1 (FORCE): Write 1 to trigger default_phase_vio_irq Value After Reset:0x0
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	WO	0x0	IPI_NOT_SUPPORTED_FORCE Force for ipi_not_supported_irq Values: 0x1 (FORCE): Write 1 to trigger ipi_not_supported_irq Value After Reset:0x0

HDMI TX Controller_AVP_1_INT_STATUS

Address: Operational Base(0x27DA0000) + offset (0x3820)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved6 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
20	RO	0x0	PKTZ_FRLCHAR_FIFO_UDF_IRQ Packetizer FIFO Underflow interrupt. Value After Reset:0x0
19:17	RW	0x0	Reserved5 Reserved Field:Yes
16	RO	0x0	TMDSFIFO_UDF_IRQ Detected TMDS FIFO Underflow interrupt. Value After Reset:0x0
15:13	RW	0x0	Reserved4 Reserved Field:Yes
12	RO	0x0	FRL_RSFEC_ALIGN_BUFFER_FULL_IRQ Indicates that the buffer on the FRL RSFEC Aligner has became full. For more information about the state of the buffer, refer to frl_rsfec_config0.frl_rsfec_align_buffer_full_st Value After Reset:0x0
11:9	RW	0x0	Reserved3 Reserved Field:Yes
8	RO	0x0	AUDPKT_ACR_CTS_CALC_IRQ Audio Clock Regeneration (ACR) CTS calculation done interrupt event Value After Reset:0x0
7	RW	0x0	Reserved2 Reserved Field:Yes
6	RO	0x0	HDCP14_AUTH_CHG_IRQ HDCP 1.4 Authenticated State Change. Check field hdcp14_auth_st for more information. Value After Reset:0x0
5	RW	0x0	Reserved1 Reserved Field:Yes
4	RO	0x0	HDCP14_BKSV_REVOC_FAIL_IRQ HDCP 1.4 BKSV is in Revocation List Value After Reset:0x0
3	RO	0x0	HDCP14_I2C_NACK_RCV_IRQ HDCP 1.4 I2C NACK Received Value After Reset:0x0
2	RO	0x0	HDCP14_I2C_TIMEOUT_IRQ HDCP 1.4 I2C Operation Timeout Value After Reset:0x0
1	RO	0x0	HDCP14_KSV_LIST_DONE_IRQ HDCP 1.4 KSV List Write in Revocation Memory Done Value After Reset:0x0
0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller_AVP_1_INT_MASK_N

Address: Operational Base(0x27DA0000) + offset (0x3824)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved6 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
20	RW	0x0	PKTZ_FRLCHAR_FIFO_UDF_MASK_N Mask for pktz_frlchar_fifo_udf_irq. Values: 0x0 (MASK): Write 0 to mask pktz_frlchar_fifo_udf_irq. 0x1 (UNMASK): Write 1 to unmask pktz_frlchar_fifo_udf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
19:17	RW	0x0	Reserved5 Reserved Field:Yes
16	RW	0x0	TMDSFIFO_UDF_MASK_N Mask for tmdsfifo_udf_irq. Values: 0x0 (MASK): Write 0 to mask tmdsfifo_udf_irq. 0x1 (UNMASK): Write 1 to unmask tmdsfifo_udf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
15:13	RW	0x0	Reserved4 Reserved Field:Yes
12	RW	0x0	FRL_RSFEC_ALIGN_BUFFER_FULL_MASK_N Mask for frl_rsfec_align_buffer_full_irq. Values: 0x0 (MASK): Write 0 to mask frl_rsfec_align_buffer_full_irq. 0x1 (UNMASK): Write 1 to unmask frl_rsfec_align_buffer_full_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
11:9	RW	0x0	Reserved3 Reserved Field:Yes
8	RW	0x0	AUDPKT_ACR_CTS_CALC_MASK_N Mask for audpkt_acr_cts_calc_irq. Values: 0x0 (MASK): Write 0 to mask audpkt_acr_cts_calc_irq. 0x1 (UNMASK): Write 1 to unmask audpkt_acr_cts_calc_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
7	RW	0x0	Reserved2 Reserved Field:Yes
6	RW	0x0	HDCP14_AUTH_CHG_MASK_N Mask for hdcp14_auth_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp14_auth_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp14_auth_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
5	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
4	RW	0x0	HDCP14_BKSV_REVOC_FAIL_MASK_N Mask for hdcp14_bksv_revoc_fail_irq. Values: 0x0 (MASK): Write 0 to mask hdcp14_bksv_revoc_fail_irq. 0x1 (UNMASK): Write 1 to unmask hdcp14_bksv_revoc_fail_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3	RW	0x0	HDCP14_I2C_NACK_RCV_MASK_N Mask for hdcp14_i2c_nack_rcv_irq. Values: 0x0 (MASK): Write 0 to mask hdcp14_i2c_nack_rcv_irq. 0x1 (UNMASK): Write 1 to unmask hdcp14_i2c_nack_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
2	RW	0x0	HDCP14_I2C_TIMEOUT_MASK_N Mask for hdcp14_i2c_timeout_irq. Values: 0x0 (MASK): Write 0 to mask hdcp14_i2c_timeout_irq. 0x1 (UNMASK): Write 1 to unmask hdcp14_i2c_timeout_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
1	RW	0x0	HDCP14_KSV_LIST_DONE_MASK_N Mask for hdcp14_ksv_list_done_irq. Values: 0x0 (MASK): Write 0 to mask hdcp14_ksv_list_done_irq. 0x1 (UNMASK): Write 1 to unmask hdcp14_ksv_list_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller_AVP_1_INT_CLEAR

Address: Operational Base(0x27DA0000) + offset (0x3828)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved6 Reserved Field:Yes
20	WO	0x0	PKTZ_FRLCHAR_FIFO_UDF_CLEAR Clear for pktz_frlchar_fifo_udf_irq Values: 0x1 (CLEAR): Write 1 to clear pktz_frlchar_fifo_udf_irq Value After Reset:0x0
19:17	RW	0x0	Reserved5 Reserved Field:Yes
16	WO	0x0	TMDSFIFO_UDF_CLEAR Clear for tmdsfifo_udf_irq Values: 0x1 (CLEAR): Write 1 to clear tmdsfifo_udf_irq Value After Reset:0x0
15:13	RW	0x0	Reserved4 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
12	WO	0x0	FRL_RSFEC_ALIGN_BUFFER_FULL_CLEAR Clear for frl_rsfec_align_buffer_full_irq Values: 0x1 (CLEAR): Write 1 to clear frl_rsfec_align_buffer_full_irq Value After Reset:0x0
11:9	RW	0x0	Reserved3 Reserved Field:Yes
8	WO	0x0	AUDPKT_ACR_CTS_CALC_CLEAR Clear for audpkt_acr_cts_calc_irq Values: 0x1 (CLEAR): Write 1 to clear audpkt_acr_cts_calc_irq Value After Reset:0x0
7	RW	0x0	Reserved2 Reserved Field:Yes
6	WO	0x0	HDCP14_AUTH_CHG_CLEAR Clear for hdcp14_auth_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp14_auth_chg_irq Value After Reset:0x0
5	RW	0x0	Reserved1 Reserved Field:Yes
4	WO	0x0	HDCP14_BKSV_REVOC_FAIL_CLEAR Clear for hdcp14_bksv_revoc_fail_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp14_bksv_revoc_fail_irq Value After Reset:0x0
3	WO	0x0	HDCP14_I2C_NACK_RCV_CLEAR Clear for hdcp14_i2c_nack_rcv_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp14_i2c_nack_rcv_irq Value After Reset:0x0
2	WO	0x0	HDCP14_I2C_TIMEOUT_CLEAR Clear for hdcp14_i2c_timeout_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp14_i2c_timeout_irq Value After Reset:0x0
1	WO	0x0	HDCP14_KSV_LIST_DONE_CLEAR Clear for hdcp14_ksv_list_done_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp14_ksv_list_done_irq Value After Reset:0x0
0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller_AVP_1_INT_FORCE

Address: Operational Base(0x27DA0000) + offset (0x382C)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved6 Reserved Field:Yes
20	WO	0x0	PKTZ_FRLCHAR_FIFO_UDF_FORCE Force for pktz_frlchar_fifo_udf_irq Values: 0x1 (FORCE): Write 1 to trigger pktz_frlchar_fifo_udf_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
19:17	RW	0x0	Reserved5 Reserved Field:Yes
16	WO	0x0	TMDSFIFO_UDF_FORCE Force for tmdsfifo_udf_irq Values: 0x1 (FORCE): Write 1 to trigger tmdsfifo_udf_irq Value After Reset:0x0
15:13	RW	0x0	Reserved4 Reserved Field:Yes
12	WO	0x0	FRL_RSFEC_ALIGN_BUFFER_FULL_FORCE Force for frl_rsfec_align_buffer_full_irq Values: 0x1 (FORCE): Write 1 to trigger frl_rsfec_align_buffer_full_irq Value After Reset:0x0
11:9	RW	0x0	Reserved3 Reserved Field:Yes
8	WO	0x0	AUDPKT_ACR_CTS_CALC_FORCE Force for audpkt_acr_cts_calc_irq Values: 0x1 (FORCE): Write 1 to trigger audpkt_acr_cts_calc_irq Value After Reset:0x0
7	RW	0x0	Reserved2 Reserved Field:Yes
6	WO	0x0	HDCP14_AUTH_CHG_FORCE Force for hdcp14_auth_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp14_auth_chg_irq Value After Reset:0x0
5	RW	0x0	Reserved1 Reserved Field:Yes
4	WO	0x0	HDCP14_BKSV_REVOC_FAIL_FORCE Force for hdcp14_bksv_revoc_fail_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp14_bksv_revoc_fail_irq Value After Reset:0x0
3	WO	0x0	HDCP14_I2C_NACK_RCV_FORCE Force for hdcp14_i2c_nack_rcv_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp14_i2c_nack_rcv_irq Value After Reset:0x0
2	WO	0x0	HDCP14_I2C_TIMEOUT_FORCE Force for hdcp14_i2c_timeout_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp14_i2c_timeout_irq Value After Reset:0x0
1	WO	0x0	HDCP14_KSV_LIST_DONE_FORCE Force for hdcp14_ksv_list_done_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp14_ksv_list_done_irq Value After Reset:0x0
0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller_AVP_2_INT_STATUS

Address: Operational Base(0x27DA0000) + offset (0x3830)

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Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved0 Reserved Field:Yes
24	RO	0x0	PKTSCHED_GMD_P0PKT_UNSENT_VB_IRQ GMD - Gamut Metadata - P0 profile packet was ready but was not sent within first VBLANK period in a frame Value After Reset:0x0
23	RO	0x0	PKTSCHED_GHDMI2_UNSENT_IRQ GHDMI2 - Generic HDMI 2 - Programmed number of packets per field/frame not fully sent Value After Reset:0x0
22	RO	0x0	PKTSCHED_GHDMI1_UNSENT_IRQ GHDMI1 - Generic HDMI 1 - Programmed number of packets per field/frame not fully sent Value After Reset:0x0
21	RO	0x0	PKTSCHED_ACR_TIMEOUT_IRQ ACR - Audio Clock Recovery - Packet not sent within a 128fs/N period Value After Reset:0x0
20	RO	0x0	PKTSCHED_ISRC_TIMEOUT_IRQ ISRC - International Standard Recording Code - Packet not sent within configured period Value After Reset:0x0
19	RO	0x0	PKTSCHED_SPDI_TIMEOUT_IRQ SPDI - Source Product Descriptor InfoFrame - Packet not sent within configured period Value After Reset:0x0
18	RO	0x0	PKTSCHED_ACP_TIMEOUT_IRQ ACP - Audio Content Protection - Packet not sent within configured period Value After Reset:0x0
17	RO	0x0	PKTSCHED_GHDMI2_SENT_IRQ GHDMI2 - Generic HDMI 2 - Packet has been sent Value After Reset:0x0
16	RO	0x0	PKTSCHED_GHDMI1_SENT_IRQ GHDMI1 - Generic HDMI 1 - Packet has been sent Value After Reset:0x0
15	RO	0x0	PKTSCHED_DRMI_SENT_IRQ DRMI - Dynamic Range and Mastering InfoFrame - Packet has been sent Value After Reset:0x0
14	RO	0x0	PKTSCHED_NVI_SENT_IRQ NVI - NTSC VBI InfoFrame - Packet has been sent Value After Reset:0x0
13	RO	0x0	PKTSCHED_AUDI_SENT_IRQ AUDI - Audio InfoFrame - Packet has been sent Value After Reset:0x0
12	RO	0x0	PKTSCHED_SPDI_SENT_IRQ SPDI - Source Product Descriptor InfoFrame - Packet has been sent Value After Reset:0x0
11	RO	0x0	PKTSCHED_AVI_SENT_IRQ AVI - Auxiliary Video InfoFrame - Packet has been sent Value After Reset:0x0

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Bit	Attr	Reset Value	Description
10	RO	0x0	PKTSCHED_VSI_SENT_IRQ VSI - Vendor Specific InfoFrame - Packet has been sent Value After Reset:0x0
9	RO	0x0	PKTSCHED_EMP_SENT_IRQ EMP - Extended Metadata - Packet has been sent Value After Reset:0x0
8	RO	0x0	PKTSCHED_AMD_SENT_IRQ AMD - Audio Metadata - Packet has been sent Value After Reset:0x0
7	RO	0x0	PKTSCHED_GMD_SENT_IRQ GMD - Gamut Metadata - Packet has been sent Value After Reset:0x0
6	RO	0x0	PKTSCHED_ISRC2_SENT_IRQ ISRC2 - Intl Std Recording Code 2 - Packet has been sent Value After Reset:0x0
5	RO	0x0	PKTSCHED_ISRC1_SENT_IRQ ISRC1 - Intl Std Recording Code 1 - Packet has been sent Value After Reset:0x0
4	RO	0x0	PKTSCHED_ACP_SENT_IRQ ACP - Audio Content Protection - Packet has been sent Value After Reset:0x0
3	RO	0x0	PKTSCHED_GCP_SENT_IRQ GCP - General Control - Packet has been sent Value After Reset:0x0
2	RO	0x0	PKTSCHED_AUDS_SENT_IRQ AUDS - Audio Sample - Packet has been sent Value After Reset:0x0
1	RO	0x0	PKTSCHED_ACR_SENT_IRQ ACR - Audio Clock Recovery - Packet has been sent Value After Reset:0x0
0	RO	0x0	PKTSCHED_NULL_SENT_IRQ NULL - Null - Packet has been sent Value After Reset:0x0

HDMI TX Controller_AVP_2_INT_MASK_N

Address: Operational Base(0x27DA0000) + offset (0x3834)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved0 Reserved Field:Yes
24	RW	0x0	PKTSCHED_GMD_P0PKT_UNSENT_VB_MASK_N Mask for pktsched_gmd_p0pkt_unsent_vb_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_gmd_p0pkt_unsent_vb_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_gmd_p0pkt_unsent_vb_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
23	RW	0x0	PKTSCHED_GHDMI2_UNSENT_MASK_N Mask for pktsched_ghdmi2_unsent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_ghdmi2_unsent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_ghdmi2_unsent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
22	RW	0x0	PKTSCHED_GHDMI1_UNSENT_MASK_N Mask for pktsched_ghdmi1_unsent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_ghdmi1_unsent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_ghdmi1_unsent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
21	RW	0x0	PKTSCHED_ACR_TIMEOUT_MASK_N Mask for pktsched_acr_timeout_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_acr_timeout_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_acr_timeout_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
20	RW	0x0	PKTSCHED_ISRC_TIMEOUT_MASK_N Mask for pktsched_isrc_timeout_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_isrc_timeout_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_isrc_timeout_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
19	RW	0x0	PKTSCHED_SPDI_TIMEOUT_MASK_N Mask for pktsched_spdi_timeout_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_spdi_timeout_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_spdi_timeout_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
18	RW	0x0	PKTSCHED_ACP_TIMEOUT_MASK_N Mask for pktsched_acp_timeout_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_acp_timeout_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_acp_timeout_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
17	RW	0x0	PKTSCHED_GHDMI2_SENT_MASK_N Mask for pktsched_ghdmi2_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_ghdmi2_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_ghdmi2_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
16	RW	0x0	PKTSCHED_GHDMI1_SENT_MASK_N Mask for pktsched_ghdmi1_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_ghdmi1_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_ghdmi1_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
15	RW	0x0	PKTSCHED_DRMI_SENT_MASK_N Mask for pktsched_drmi_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_drmi_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_drmi_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
14	RW	0x0	PKTSCHED_NVI_SENT_MASK_N Mask for pktsched_nvi_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_nvi_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_nvi_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
13	RW	0x0	PKTSCHED_AUDI_SENT_MASK_N Mask for pktsched_audi_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_audi_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_audi_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
12	RW	0x0	PKTSCHED_SPDI_SENT_MASK_N Mask for pktsched_spdi_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_spdi_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_spdi_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
11	RW	0x0	PKTSCHED_AVI_SENT_MASK_N Mask for pktsched_avi_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_avi_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_avi_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
10	RW	0x0	PKTSCHED_VSI_SENT_MASK_N Mask for pktsched_vsi_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_vsi_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_vsi_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
9	RW	0x0	PKTSCHED_EMP_SENT_MASK_N Mask for pktsched_emp_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_emp_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_emp_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
8	RW	0x0	PKTSCHED_AMD_SENT_MASK_N Mask for pktsched_amd_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_amd_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_amd_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
7	RW	0x0	PKTSCHED_GMD_SENT_MASK_N Mask for pktsched_gmd_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_gmd_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_gmd_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
6	RW	0x0	PKTSCHED_ISRC2_SENT_MASK_N Mask for pktsched_isrc2_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_isrc2_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_isrc2_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
5	RW	0x0	PKTSCHED_ISRC1_SENT_MASK_N Mask for pktsched_isrc1_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_isrc1_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_isrc1_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
4	RW	0x0	PKTSCHED_ACP_SENT_MASK_N Mask for pktsched_acp_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_acp_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_acp_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3	RW	0x0	PKTSCHED_GCP_SENT_MASK_N Mask for pktsched_gcp_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_gcp_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_gcp_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
2	RW	0x0	PKTSCHED_AUDS_SENT_MASK_N Mask for pktsched_auds_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_auds_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_auds_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
1	RW	0x0	PKTSCHED_ACR_SENT_MASK_N Mask for pktsched_acr_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_acr_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_acr_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	PKTSCHED_NULL_SENT_MASK_N Mask for pktsched_null_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_null_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_null_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_AVP_2_INT_CLEAR

Address: Operational Base(0x27DA0000) + offset (0x3838)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved0 Reserved Field:Yes
24	WO	0x0	PKTSCHED_GMD_P0PKT_UNSENT_VB_CLEAR Clear for pktsched_gmd_p0pkt_unsent_vb_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_gmd_p0pkt_unsent_vb_irq Value After Reset:0x0
23	WO	0x0	PKTSCHED_GHDMI2_UNSENT_CLEAR Clear for pktsched_ghdmi2_unsent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_ghdmi2_unsent_irq Value After Reset:0x0
22	WO	0x0	PKTSCHED_GHDMI1_UNSENT_CLEAR Clear for pktsched_ghdmi1_unsent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_ghdmi1_unsent_irq Value After Reset:0x0
21	WO	0x0	PKTSCHED_ACR_TIMEOUT_CLEAR Clear for pktsched_acr_timeout_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_acr_timeout_irq Value After Reset:0x0
20	WO	0x0	PKTSCHED_ISRC_TIMEOUT_CLEAR Clear for pktsched_isrc_timeout_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_isrc_timeout_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
19	WO	0x0	PKTSCHED_SPDI_TIMEOUT_CLEAR Clear for pktsched_spdi_timeout_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_spdi_timeout_irq Value After Reset:0x0
18	WO	0x0	PKTSCHED_ACP_TIMEOUT_CLEAR Clear for pktsched_acp_timeout_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_acp_timeout_irq Value After Reset:0x0
17	WO	0x0	PKTSCHED_GHDMI2_SENT_CLEAR Clear for pktsched_ghdmi2_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_ghdmi2_sent_irq Value After Reset:0x0
16	WO	0x0	PKTSCHED_GHDMI1_SENT_CLEAR Clear for pktsched_ghdmi1_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_ghdmi1_sent_irq Value After Reset:0x0
15	WO	0x0	PKTSCHED_DRMI_SENT_CLEAR Clear for pktsched_drmi_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_drmi_sent_irq Value After Reset:0x0
14	WO	0x0	PKTSCHED_NVI_SENT_CLEAR Clear for pktsched_nvi_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_nvi_sent_irq Value After Reset:0x0
13	WO	0x0	PKTSCHED_AUDI_SENT_CLEAR Clear for pktsched_audi_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_audi_sent_irq Value After Reset:0x0
12	WO	0x0	PKTSCHED_SPDI_SENT_CLEAR Clear for pktsched_spdi_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_spdi_sent_irq Value After Reset:0x0
11	WO	0x0	PKTSCHED_AVI_SENT_CLEAR Clear for pktsched_avi_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_avi_sent_irq Value After Reset:0x0
10	WO	0x0	PKTSCHED_VSI_SENT_CLEAR Clear for pktsched_vsi_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_vsi_sent_irq Value After Reset:0x0
9	WO	0x0	PKTSCHED_EMP_SENT_CLEAR Clear for pktsched_emp_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_emp_sent_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
8	WO	0x0	PKTSCHED_AMD_SENT_CLEAR Clear for pktsched_amd_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_amd_sent_irq Value After Reset:0x0
7	WO	0x0	PKTSCHED_GMD_SENT_CLEAR Clear for pktsched_gmd_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_gmd_sent_irq Value After Reset:0x0
6	WO	0x0	PKTSCHED_ISRC2_SENT_CLEAR Clear for pktsched_isrc2_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_isrc2_sent_irq Value After Reset:0x0
5	WO	0x0	PKTSCHED_ISRC1_SENT_CLEAR Clear for pktsched_isrc1_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_isrc1_sent_irq Value After Reset:0x0
4	WO	0x0	PKTSCHED_ACP_SENT_CLEAR Clear for pktsched_acp_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_acp_sent_irq Value After Reset:0x0
3	WO	0x0	PKTSCHED_GCP_SENT_CLEAR Clear for pktsched_gcp_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_gcp_sent_irq Value After Reset:0x0
2	WO	0x0	PKTSCHED_AUDS_SENT_CLEAR Clear for pktsched_auds_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_auds_sent_irq Value After Reset:0x0
1	WO	0x0	PKTSCHED_ACR_SENT_CLEAR Clear for pktsched_acr_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_acr_sent_irq Value After Reset:0x0
0	WO	0x0	PKTSCHED_NULL_SENT_CLEAR Clear for pktsched_null_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_null_sent_irq Value After Reset:0x0

HDMI TX Controller_AVP_2_INT_FORCE

Address: Operational Base(0x27DA0000) + offset (0x383C)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
24	WO	0x0	PKTSCHED_GMD_P0PKT_UNSENT_VB_FORCE Force for pktsched_gmd_p0pkt_unsent_vb_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_gmd_p0pkt_unsent_vb_irq Value After Reset:0x0
23	WO	0x0	PKTSCHED_GHDMI2_UNSENT_FORCE Force for pktsched_ghdmi2_unsent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_ghdmi2_unsent_irq Value After Reset:0x0
22	WO	0x0	PKTSCHED_GHDMI1_UNSENT_FORCE Force for pktsched_ghdmi1_unsent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_ghdmi1_unsent_irq Value After Reset:0x0
21	WO	0x0	PKTSCHED_ACR_TIMEOUT_FORCE Force for pktsched_acr_timeout_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_acr_timeout_irq Value After Reset:0x0
20	WO	0x0	PKTSCHED_ISRC_TIMEOUT_FORCE Force for pktsched_isrc_timeout_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_isrc_timeout_irq Value After Reset:0x0
19	WO	0x0	PKTSCHED_SPDI_TIMEOUT_FORCE Force for pktsched_spdi_timeout_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_spdi_timeout_irq Value After Reset:0x0
18	WO	0x0	PKTSCHED_ACP_TIMEOUT_FORCE Force for pktsched_acp_timeout_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_acp_timeout_irq Value After Reset:0x0
17	WO	0x0	PKTSCHED_GHDMI2_SENT_FORCE Force for pktsched_ghdmi2_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_ghdmi2_sent_irq Value After Reset:0x0
16	WO	0x0	PKTSCHED_GHDMI1_SENT_FORCE Force for pktsched_ghdmi1_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_ghdmi1_sent_irq Value After Reset:0x0
15	WO	0x0	PKTSCHED_DRMI_SENT_FORCE Force for pktsched_drmi_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_drmi_sent_irq Value After Reset:0x0
14	WO	0x0	PKTSCHED_NVI_SENT_FORCE Force for pktsched_nvi_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_nvi_sent_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
13	WO	0x0	PKTSCHED_AUDI_SENT_FORCE Force for pktsched_audi_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_audi_sent_irq Value After Reset:0x0
12	WO	0x0	PKTSCHED_SPDI_SENT_FORCE Force for pktsched_spdi_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_spdi_sent_irq Value After Reset:0x0
11	WO	0x0	PKTSCHED_AVI_SENT_FORCE Force for pktsched_avi_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_avi_sent_irq Value After Reset:0x0
10	WO	0x0	PKTSCHED_VSI_SENT_FORCE Force for pktsched_vsi_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_vsi_sent_irq Value After Reset:0x0
9	WO	0x0	PKTSCHED_EMP_SENT_FORCE Force for pktsched_emp_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_emp_sent_irq Value After Reset:0x0
8	WO	0x0	PKTSCHED_AMD_SENT_FORCE Force for pktsched_amd_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_amd_sent_irq Value After Reset:0x0
7	WO	0x0	PKTSCHED_GMD_SENT_FORCE Force for pktsched_gmd_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_gmd_sent_irq Value After Reset:0x0
6	WO	0x0	PKTSCHED_ISRC2_SENT_FORCE Force for pktsched_isrc2_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_isrc2_sent_irq Value After Reset:0x0
5	WO	0x0	PKTSCHED_ISRC1_SENT_FORCE Force for pktsched_isrc1_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_isrc1_sent_irq Value After Reset:0x0
4	WO	0x0	PKTSCHED_ACP_SENT_FORCE Force for pktsched_acp_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_acp_sent_irq Value After Reset:0x0
3	WO	0x0	PKTSCHED_GCP_SENT_FORCE Force for pktsched_gcp_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_gcp_sent_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
2	WO	0x0	PKTSCHED_AUDS_SENT_FORCE Force for pktsched_auds_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_auds_sent_irq Value After Reset:0x0
1	WO	0x0	PKTSCHED_ACR_SENT_FORCE Force for pktsched_acr_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_acr_sent_irq Value After Reset:0x0
0	WO	0x0	PKTSCHED_NULL_SENT_FORCE Force for pktsched_null_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_null_sent_irq Value After Reset:0x0

HDMI TX Controller_AVP_3_INT_STATUS

Address: Operational Base(0x27DA0000) + offset (0x3840)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes
19	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_0_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[0] from ESM Module Value After Reset:0x0
18	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_1_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[1] from ESM Module Value After Reset:0x0
17	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_2_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[2] from ESM Module Value After Reset:0x0
16	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_3_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[3] from ESM Module Value After Reset:0x0
15	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_4_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[4] from ESM Module Value After Reset:0x0
14	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_5_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[5] from ESM Module Value After Reset:0x0
13	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_6_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[6] from ESM Module Value After Reset:0x0
12	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_7_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[7] from ESM Module Value After Reset:0x0

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Bit	Attr	Reset Value	Description
11	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_8_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[8] from ESM Module Value After Reset:0x0
10	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_9_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[9] from ESM Module Value After Reset:0x0
9	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_10_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[10] from ESM Module Value After Reset:0x0
8	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_11_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[11] from ESM Module Value After Reset:0x0
7	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_12_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[12] from ESM Module Value After Reset:0x0
6	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_13_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[13] from ESM Module Value After Reset:0x0
5	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_14_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[14] from ESM Module Value After Reset:0x0
4	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_15_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[15] from ESM Module Value After Reset:0x0
3	RO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_0_CHG_IRQ HDCP 2 Logic Global Change interrupt for bit hdcp2_esm_global_gpio_out[0] from ESM Module Value After Reset:0x0
2	RO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_1_CHG_IRQ HDCP 2 Logic Global Change interrupt for bit hdcp2_esm_global_gpio_out[1] from ESM Module Value After Reset:0x0
1	RO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_2_CHG_IRQ HDCP 2 Logic Global Change interrupt for bit hdcp2_esm_global_gpio_out[2] from ESM Module Value After Reset:0x0
0	RO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_3_CHG_IRQ HDCP 2 Logic Global Change interrupt for bit hdcp2_esm_global_gpio_out[3] from ESM Module Value After Reset:0x0

HDMI TX Controller_AVP_3_INT_MASK_N

Address: Operational Base(0x27DA0000) + offset (0x3844)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
19	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_0_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_0_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_0_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_0_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
18	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_1_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_1_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_1_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_1_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
17	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_2_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_2_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_2_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_2_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
16	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_3_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_3_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_3_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_3_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
15	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_4_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_4_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_4_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_4_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
14	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_5_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_5_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_5_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_5_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
13	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_6_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_6_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_6_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_6_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
12	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_7_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_7_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_7_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_7_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
11	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_8_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_8_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_8_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_8_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
10	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_9_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_9_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_9_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_9_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
9	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_10_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_10_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_10_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_10_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
8	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_11_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_11_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_11_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_11_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
7	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_12_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_12_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_12_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_12_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
6	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_13_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_13_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_13_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_13_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
5	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_14_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_14_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_14_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_14_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
4	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_15_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_15_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_15_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_15_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3	RW	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_0_CHG_MASK_N Mask for hdcp2_esm_global_gpio_out_0_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_global_gpio_out_0_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_global_gpio_out_0_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
2	RW	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_1_CHG_MASK_N Mask for hdcp2_esm_global_gpio_out_1_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_global_gpio_out_1_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_global_gpio_out_1_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
1	RW	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_2_CHG_MASK_N Mask for hdcp2_esm_global_gpio_out_2_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_global_gpio_out_2_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_global_gpio_out_2_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_3_CHG_MASK_N Mask for hdcp2_esm_global_gpio_out_3_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_global_gpio_out_3_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_global_gpio_out_3_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_AVP_3_INT_CLEAR

Address: Operational Base(0x27DA0000) + offset (0x3848)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes
19	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_0_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_0_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_0_chg_irq Value After Reset:0x0
18	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_1_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_1_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_1_chg_irq Value After Reset:0x0
17	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_2_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_2_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_2_chg_irq Value After Reset:0x0
16	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_3_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_3_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_3_chg_irq Value After Reset:0x0
15	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_4_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_4_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_4_chg_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
14	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_5_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_5_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_5_chg_irq Value After Reset:0x0
13	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_6_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_6_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_6_chg_irq Value After Reset:0x0
12	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_7_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_7_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_7_chg_irq Value After Reset:0x0
11	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_8_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_8_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_8_chg_irq Value After Reset:0x0
10	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_9_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_9_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_9_chg_irq Value After Reset:0x0
9	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_10_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_10_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_10_chg_irq Value After Reset:0x0
8	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_11_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_11_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_11_chg_irq Value After Reset:0x0
7	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_12_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_12_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_12_chg_irq Value After Reset:0x0
6	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_13_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_13_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_13_chg_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
5	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_14_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_14_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_14_chg_irq Value After Reset:0x0
4	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_15_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_15_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_15_chg_irq Value After Reset:0x0
3	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_0_CHG_CLEAR Clear for hdcp2_esm_global_gpio_out_0_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_global_gpio_out_0_chg_irq Value After Reset:0x0
2	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_1_CHG_CLEAR Clear for hdcp2_esm_global_gpio_out_1_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_global_gpio_out_1_chg_irq Value After Reset:0x0
1	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_2_CHG_CLEAR Clear for hdcp2_esm_global_gpio_out_2_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_global_gpio_out_2_chg_irq Value After Reset:0x0
0	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_3_CHG_CLEAR Clear for hdcp2_esm_global_gpio_out_3_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_global_gpio_out_3_chg_irq Value After Reset:0x0

HDMI TX Controller_AVP_3_INT_FORCE

Address: Operational Base(0x27DA0000) + offset (0x384C)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes
19	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_0_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_0_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_0_chg_irq Value After Reset:0x0
18	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_1_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_1_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_1_chg_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
17	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_2_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_2_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_2_chg_irq Value After Reset:0x0
16	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_3_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_3_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_3_chg_irq Value After Reset:0x0
15	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_4_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_4_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_4_chg_irq Value After Reset:0x0
14	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_5_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_5_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_5_chg_irq Value After Reset:0x0
13	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_6_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_6_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_6_chg_irq Value After Reset:0x0
12	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_7_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_7_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_7_chg_irq Value After Reset:0x0
11	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_8_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_8_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_8_chg_irq Value After Reset:0x0
10	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_9_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_9_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_9_chg_irq Value After Reset:0x0
9	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_10_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_10_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_10_chg_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
8	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_11_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_11_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_11_chg_irq Value After Reset:0x0
7	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_12_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_12_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_12_chg_irq Value After Reset:0x0
6	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_13_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_13_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_13_chg_irq Value After Reset:0x0
5	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_14_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_14_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_14_chg_irq Value After Reset:0x0
4	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_15_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_15_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_15_chg_irq Value After Reset:0x0
3	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_0_CHG_FORCE Force for hdcp2_esm_global_gpio_out_0_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_global_gpio_out_0_chg_irq Value After Reset:0x0
2	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_1_CHG_FORCE Force for hdcp2_esm_global_gpio_out_1_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_global_gpio_out_1_chg_irq Value After Reset:0x0
1	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_2_CHG_FORCE Force for hdcp2_esm_global_gpio_out_2_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_global_gpio_out_2_chg_irq Value After Reset:0x0
0	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_3_CHG_FORCE Force for hdcp2_esm_global_gpio_out_3_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_global_gpio_out_3_chg_irq Value After Reset:0x0

HDMI TX Controller_AVP_4_INT_STATUS

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Address: Operational Base(0x27DA0000) + offset (0x3850)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved3 Reserved Field:Yes
19	RO	0x0	SPDIF_LINE3_PROTOCOL_ERR_IRQ Audio SPDIF Protocol error in Lane 3 interrupt Value After Reset:0x0
18	RO	0x0	SPDIF_LINE2_PROTOCOL_ERR_IRQ Audio SPDIF Protocol error in Lane 2 interrupt Value After Reset:0x0
17	RO	0x0	SPDIF_LINE1_PROTOCOL_ERR_IRQ Audio SPDIF Protocol error in Lane 1 interrupt Value After Reset:0x0
16	RO	0x0	SPDIF_LINE0_PROTOCOL_ERR_IRQ Audio SPDIF Protocol error in Lane 0 interrupt Value After Reset:0x0
15	RO	0x0	SPDIF_LINE3_PARITY_ERR_IRQ Audio SPDIF parity bit received incorrectly in Lane 3 interrupt Value After Reset:0x0
14	RO	0x0	SPDIF_LINE2_PARITY_ERR_IRQ Audio SPDIF parity bit received incorrectly in Lane 2 nterrupt Value After Reset:0x0
13	RO	0x0	SPDIF_LINE1_PARITY_ERR_IRQ Audio SPDIF parity bit received incorrectly in Lane 1 interrupt Value After Reset:0x0
12	RO	0x0	SPDIF_LINE0_PARITY_ERR_IRQ Audio SPDIF parity bit received incorrectly in Lane 0 interrupt Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	RO	0x0	I2S_BBIT_ERR_IRQ Audio I2S error: disparity on received B bits interrupt Value After Reset:0x0
8	RO	0x0	I2S_WS_ERR_IRQ Audio I2S protocol error interrupt Value After Reset:0x0
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	RO	0x0	AUDFIFO_OVF_IRQ Audio interface FIFO Overflow interrupt Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RO	0x0	PAI_FORMAT_CHG_IRQ Audio PAI interface format change interrupt Value After Reset:0x0
0	RO	0x0	PAI_PAIR_LAYOUT_CHG_IRQ Audio PAI pair layout chage interrupt Value After Reset:0x0

HDMI TX Controller_AVP_4_INT_MASK_N

Address: Operational Base(0x27DA0000) + offset (0x3854)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
19	RW	0x0	SPDIF_LINE3_PROTOCOL_ERR_MASK_N Mask for spdif_line3_protocol_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line3_protocol_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line3_protocol_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
18	RW	0x0	SPDIF_LINE2_PROTOCOL_ERR_MASK_N Mask for spdif_line2_protocol_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line2_protocol_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line2_protocol_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
17	RW	0x0	SPDIF_LINE1_PROTOCOL_ERR_MASK_N Mask for spdif_line1_protocol_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line1_protocol_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line1_protocol_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
16	RW	0x0	SPDIF_LINE0_PROTOCOL_ERR_MASK_N Mask for spdif_line0_protocol_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line0_protocol_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line0_protocol_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
15	RW	0x0	SPDIF_LINE3_PARITY_ERR_MASK_N Mask for spdif_line3_parity_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line3_parity_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line3_parity_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
14	RW	0x0	SPDIF_LINE2_PARITY_ERR_MASK_N Mask for spdif_line2_parity_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line2_parity_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line2_parity_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
13	RW	0x0	SPDIF_LINE1_PARITY_ERR_MASK_N Mask for spdif_line1_parity_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line1_parity_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line1_parity_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
12	RW	0x0	SPDIF_LINE0_PARITY_ERR_MASK_N Mask for spdif_line0_parity_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line0_parity_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line0_parity_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	RW	0x0	I2S_BBIT_ERR_MASK_N Mask for i2s_bbit_err_irq. Values: 0x0 (MASK): Write 0 to mask i2s_bbit_err_irq. 0x1 (UNMASK): Write 1 to unmask i2s_bbit_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
8	RW	0x0	I2S_WS_ERR_MASK_N Mask for i2s_ws_err_irq. Values: 0x0 (MASK): Write 0 to mask i2s_ws_err_irq. 0x1 (UNMASK): Write 1 to unmask i2s_ws_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	RW	0x0	AUDFIFO_OVF_MASK_N Mask for audfifo_ovf_irq. Values: 0x0 (MASK): Write 0 to mask audfifo_ovf_irq. 0x1 (UNMASK): Write 1 to unmask audfifo_ovf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RW	0x0	PAI_FORMAT_CHG_MASK_N Mask for pai_format_chg_irq. Values: 0x0 (MASK): Write 0 to mask pai_format_chg_irq. 0x1 (UNMASK): Write 1 to unmask pai_format_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	PAI_PAIR_LAYOUT_CHG_MASK_N Mask for pai_pair_layout_chg_irq. Values: 0x0 (MASK): Write 0 to mask pai_pair_layout_chg_irq. 0x1 (UNMASK): Write 1 to unmask pai_pair_layout_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_AVP_4_INT_CLEAR

Address: Operational Base(0x27DA0000) + offset (0x3858)

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Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved3 Reserved Field:Yes
19	WO	0x0	SPDIF_LINE3_PROTOCOL_ERR_CLEAR Clear for spdif_line3_protocol_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line3_protocol_err_irq Value After Reset:0x0
18	WO	0x0	SPDIF_LINE2_PROTOCOL_ERR_CLEAR Clear for spdif_line2_protocol_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line2_protocol_err_irq Value After Reset:0x0
17	WO	0x0	SPDIF_LINE1_PROTOCOL_ERR_CLEAR Clear for spdif_line1_protocol_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line1_protocol_err_irq Value After Reset:0x0
16	WO	0x0	SPDIF_LINE0_PROTOCOL_ERR_CLEAR Clear for spdif_line0_protocol_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line0_protocol_err_irq Value After Reset:0x0
15	WO	0x0	SPDIF_LINE3_PARITY_ERR_CLEAR Clear for spdif_line3_parity_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line3_parity_err_irq Value After Reset:0x0
14	WO	0x0	SPDIF_LINE2_PARITY_ERR_CLEAR Clear for spdif_line2_parity_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line2_parity_err_irq Value After Reset:0x0
13	WO	0x0	SPDIF_LINE1_PARITY_ERR_CLEAR Clear for spdif_line1_parity_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line1_parity_err_irq Value After Reset:0x0
12	WO	0x0	SPDIF_LINE0_PARITY_ERR_CLEAR Clear for spdif_line0_parity_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line0_parity_err_irq Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	WO	0x0	I2S_BBIT_ERR_CLEAR Clear for i2s_bbit_err_irq Values: 0x1 (CLEAR): Write 1 to clear i2s_bbit_err_irq Value After Reset:0x0
8	WO	0x0	I2S_WS_ERR_CLEAR Clear for i2s_ws_err_irq Values: 0x1 (CLEAR): Write 1 to clear i2s_ws_err_irq Value After Reset:0x0
7:5	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
4	WO	0x0	AUDFIFO_OVF_CLEAR Clear for audfifo_ovf_irq Values: 0x1 (CLEAR): Write 1 to clear audfifo_ovf_irq Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	WO	0x0	PAI_FORMAT_CHG_CLEAR Clear for pai_format_chg_irq Values: 0x1 (CLEAR): Write 1 to clear pai_format_chg_irq Value After Reset:0x0
0	WO	0x0	PAI_PAIR_LAYOUT_CHG_CLEAR Clear for pai_pair_layout_chg_irq Values: 0x1 (CLEAR): Write 1 to clear pai_pair_layout_chg_irq Value After Reset:0x0

HDMI TX Controller_AVP_4_INT_FORCE

Address: Operational Base(0x27DA0000) + offset (0x385C)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved3 Reserved Field:Yes
19	WO	0x0	SPDIF_LINE3_PROTOCOL_ERR_FORCE Force for spdif_line3_protocol_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line3_protocol_err_irq Value After Reset:0x0
18	WO	0x0	SPDIF_LINE2_PROTOCOL_ERR_FORCE Force for spdif_line2_protocol_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line2_protocol_err_irq Value After Reset:0x0
17	WO	0x0	SPDIF_LINE1_PROTOCOL_ERR_FORCE Force for spdif_line1_protocol_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line1_protocol_err_irq Value After Reset:0x0
16	WO	0x0	SPDIF_LINE0_PROTOCOL_ERR_FORCE Force for spdif_line0_protocol_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line0_protocol_err_irq Value After Reset:0x0
15	WO	0x0	SPDIF_LINE3_PARITY_ERR_FORCE Force for spdif_line3_parity_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line3_parity_err_irq Value After Reset:0x0
14	WO	0x0	SPDIF_LINE2_PARITY_ERR_FORCE Force for spdif_line2_parity_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line2_parity_err_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
13	WO	0x0	SPDIF_LINE1_PARITY_ERR_FORCE Force for spdif_line1_parity_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line1_parity_err_irq Value After Reset:0x0
12	WO	0x0	SPDIF_LINE0_PARITY_ERR_FORCE Force for spdif_line0_parity_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line0_parity_err_irq Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	WO	0x0	I2S_BBIT_ERR_FORCE Force for i2s_bbit_err_irq Values: 0x1 (FORCE): Write 1 to trigger i2s_bbit_err_irq Value After Reset:0x0
8	WO	0x0	I2S_WS_ERR_FORCE Force for i2s_ws_err_irq Values: 0x1 (FORCE): Write 1 to trigger i2s_ws_err_irq Value After Reset:0x0
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	WO	0x0	AUDFIFO_OVF_FORCE Force for audfifo_ovf_irq Values: 0x1 (FORCE): Write 1 to trigger audfifo_ovf_irq Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	WO	0x0	PAI_FORMAT_CHG_FORCE Force for pai_format_chg_irq Values: 0x1 (FORCE): Write 1 to trigger pai_format_chg_irq Value After Reset:0x0
0	WO	0x0	PAI_PAIR_LAYOUT_CHG_FORCE Force for pai_pair_layout_chg_irq Values: 0x1 (FORCE): Write 1 to trigger pai_pair_layout_chg_irq Value After Reset:0x0

HDMI TX Controller_AVP_5_INT_STATUS

Address: Operational Base(0x27DA0000) + offset (0x3860)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved1 Reserved Field:Yes
4	RO	0x0	VID_FIFO_UDF_IRQ Video Interface FIFO Underflow Interrupt Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RO	0x0	VIDIF_VMON_VMEAS_IRQ Video Monitor vertical measures update interrupt Value After Reset:0x0

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Bit	Attr	Reset Value	Description
0	RO	0x0	VIDIF_VMON_HMEAS_IRQ Video Monitor horizontal measures update interrupt Value After Reset:0x0

HDMI TX Controller_AVP_5_INT_MASK_N

Address: Operational Base(0x27DA0000) + offset (0x3864)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved1 Reserved Field:Yes
4	RW	0x0	VID_FIFO_UDF_MASK_N Mask for vid_fifo_udf_irq. Values: 0x0 (MASK): Write 0 to mask vid_fifo_udf_irq. 0x1 (UNMASK): Write 1 to unmask vid_fifo_udf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RW	0x0	VIDIF_VMON_VMEAS_MASK_N Mask for vidif_vmon_vmeas_irq. Values: 0x0 (MASK): Write 0 to mask vidif_vmon_vmeas_irq. 0x1 (UNMASK): Write 1 to unmask vidif_vmon_vmeas_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	VIDIF_VMON_HMEAS_MASK_N Mask for vidif_vmon_hmeas_irq. Values: 0x0 (MASK): Write 0 to mask vidif_vmon_hmeas_irq. 0x1 (UNMASK): Write 1 to unmask vidif_vmon_hmeas_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_AVP_5_INT_CLEAR

Address: Operational Base(0x27DA0000) + offset (0x3868)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved1 Reserved Field:Yes
4	WO	0x0	VID_FIFO_UDF_CLEAR Clear for vid_fifo_udf_irq Values: 0x1 (CLEAR): Write 1 to clear vid_fifo_udf_irq Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	WO	0x0	VIDIF_VMON_VMEAS_CLEAR Clear for vidif_vmon_vmeas_irq Values: 0x1 (CLEAR): Write 1 to clear vidif_vmon_vmeas_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
0	WO	0x0	VIDIF_VMON_HMEAS_CLEAR Clear for vidif_vmon_hmeas_irq Values: 0x1 (CLEAR): Write 1 to clear vidif_vmon_hmeas_irq Value After Reset:0x0

HDMI TX Controller_AVP_5_INT_FORCE

Address: Operational Base(0x27DA0000) + offset (0x386C)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved1 Reserved Field:Yes
4	WO	0x0	VID_FIFO_UDF_FORCE Force for vid_fifo_udf_irq Values: 0x1 (FORCE): Write 1 to trigger vid_fifo_udf_irq Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	WO	0x0	VIDIF_VMON_VMEAS_FORCE Force for vidif_vmon_vmeas_irq Values: 0x1 (FORCE): Write 1 to trigger vidif_vmon_vmeas_irq Value After Reset:0x0
0	WO	0x0	VIDIF_VMON_HMEAS_FORCE Force for vidif_vmon_hmeas_irq Values: 0x1 (FORCE): Write 1 to trigger vidif_vmon_hmeas_irq Value After Reset:0x0

HDMI TX Controller_AVP_6_INT_STATUS

Address: Operational Base(0x27DA0000) + offset (0x3870)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x0	VID_FIFO_OVF_IRQ Video Interface FIFO Overflow Interrupt Value After Reset:0x0

HDMI TX Controller_AVP_6_INT_MASK_N

Address: Operational Base(0x27DA0000) + offset (0x3874)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	VID_FIFO_OVF_MASK_N Mask for vid_fifo_ovf_irq. Values: 0x0 (MASK): Write 0 to mask vid_fifo_ovf_irq. 0x1 (UNMASK): Write 1 to unmask vid_fifo_ovf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_AVP_6_INT_CLEAR

Address: Operational Base(0x27DA0000) + offset (0x3878)

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Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	VID_FIFO_OVF_CLEAR Clear for vid_fifo_ovf_irq Values: 0x1 (CLEAR): Write 1 to clear vid_fifo_ovf_irq Value After Reset:0x0

HDMI TX Controller_AVP_6_INT_FORCE

Address: Operational Base(0x27DA0000) + offset (0x387C)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	VID_FIFO_OVF_FORCE Force for vid_fifo_ovf_irq Values: 0x1 (FORCE): Write 1 to trigger vid_fifo_ovf_irq Value After Reset:0x0

HDMI TX Controller_CEC_INT_STATUS

Address: Operational Base(0x27DA0000) + offset (0x4000)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes
12	RO	0x0	CECRX_NOTIFY_ERR_IRQ Follower - Bit timing error detected, Error Notification is being sent to Initiator, while rxbusy is set (for follower). Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
11	RO	0x0	CECRX_EOM_IRQ Follower - Frame fully received after last data block with EOM=1 (for follower only). Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
10	RO	0x0	CECTX_DRIVE_ERR_IRQ Drive 0 in the CEC output has not been seen in the CEC input interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
9	RO	0x0	CECRX_BUSY_IRQ Status bit cecrx_busy_st has changed value. Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0

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Bit	Attr	Reset Value	Description
8	RO	0x0	CECTX_BUSY_IRQ Status bit cectx_busy_st has changed value. Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5	RO	0x0	CECTX_FRAME_DISCARDED_IRQ Message to be sent has been discarded, since a new message has been received before the message is sent. Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
4	RO	0x0	CECTX_NRETRANSMIT_FAIL_IRQ Last re- transmission fail. Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
3	RO	0x0	CECTX_LINE_ERR_IRQ Initiator - Line Error detected while transmitting a Frame (for initiator only). Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
2	RO	0x0	CECTX_ARBLOST_IRQ Initiator - CEC line arbitration lost to a different Initiator when starting to transmit a Frame. (specification CEC 9). Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
1	RO	0x0	CECTX_NACK_IRQ Initiator - Frame transmission stopped due to received NACK (direct address) or Negative ACK (broadcast) (for initiator only). Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
0	RO	0x0	CECTX_DONE_IRQ Initiator - Frame transmission is done successfully. (initiator only). interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0

HDMI TX Controller_CEC_INT_MASK_N

Address: Operational Base(0x27DA0000) + offset (0x4004)

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Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes
12	RW	0x0	CECRX_NOTIFY_ERR_MASK_N Mask for cecrx_notify_err_irq. Values: 0x0 (MASK): Write 0 to mask cecrx_notify_err_irq. 0x1 (UNMASK): Write 1 to unmask cecrx_notify_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
11	RW	0x0	CECRX_EOM_MASK_N Mask for cecrx_eom_irq. Values: 0x0 (MASK): Write 0 to mask cecrx_eom_irq. 0x1 (UNMASK): Write 1 to unmask cecrx_eom_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
10	RW	0x0	CECTX_DRIVE_ERR_MASK_N Mask for cectx_drive_err_irq. Values: 0x0 (MASK): Write 0 to mask cectx_drive_err_irq. 0x1 (UNMASK): Write 1 to unmask cectx_drive_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
9	RW	0x0	CECRX_BUSY_MASK_N Mask for cecrx_busy_irq. Values: 0x0 (MASK): Write 0 to mask cecrx_busy_irq. 0x1 (UNMASK): Write 1 to unmask cecrx_busy_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
8	RW	0x0	CECTX_BUSY_MASK_N Mask for cectx_busy_irq. Values: 0x0 (MASK): Write 0 to mask cectx_busy_irq. 0x1 (UNMASK): Write 1 to unmask cectx_busy_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5	RW	0x0	CECTX_FRAME_DISCARDED_MASK_N Mask for cectx_frame_discarded_irq. Values: 0x0 (MASK): Write 0 to mask cectx_frame_discarded_irq. 0x1 (UNMASK): Write 1 to unmask cectx_frame_discarded_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
4	RW	0x0	CECTX_NRETRANSMIT_FAIL_MASK_N Mask for cectx_nretransmit_fail_irq. Values: 0x0 (MASK): Write 0 to mask cectx_nretransmit_fail_irq. 0x1 (UNMASK): Write 1 to unmask cectx_nretransmit_fail_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3	RW	0x0	CECTX_LINE_ERR_MASK_N Mask for cectx_line_err_irq. Values: 0x0 (MASK): Write 0 to mask cectx_line_err_irq. 0x1 (UNMASK): Write 1 to unmask cectx_line_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
2	RW	0x0	CECTX_ARBLOST_MASK_N Mask for cectx_arblost_irq. Values: 0x0 (MASK): Write 0 to mask cectx_arblost_irq. 0x1 (UNMASK): Write 1 to unmask cectx_arblost_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
1	RW	0x0	CECTX_NACK_MASK_N Mask for cectx_nack_irq. Values: 0x0 (MASK): Write 0 to mask cectx_nack_irq. 0x1 (UNMASK): Write 1 to unmask cectx_nack_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	CECTX_DONE_MASK_N Mask for cectx_done_irq. Values: 0x0 (MASK): Write 0 to mask cectx_done_irq. 0x1 (UNMASK): Write 1 to unmask cectx_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_CEC_INT_CLEAR

Address: Operational Base(0x27DA0000) + offset (0x4008)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes
12	WO	0x0	CECRX_NOTIFY_ERR_CLEAR Clear for cecrx_notify_err_irq Values: 0x1 (CLEAR): Write 1 to clear cecrx_notify_err_irq Value After Reset:0x0
11	WO	0x0	CECRX_EOM_CLEAR Clear for cecrx_eom_irq Values: 0x1 (CLEAR): Write 1 to clear cecrx_eom_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
10	WO	0x0	CECTX_DRIVE_ERR_CLEAR Clear for cectx_drive_err_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_drive_err_irq Value After Reset:0x0
9	WO	0x0	CECRX_BUSY_CLEAR Clear for cecrx_busy_irq Values: 0x1 (CLEAR): Write 1 to clear cecrx_busy_irq Value After Reset:0x0
8	WO	0x0	CECTX_BUSY_CLEAR Clear for cectx_busy_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_busy_irq Value After Reset:0x0
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5	WO	0x0	CECTX_FRAME_DISCARDED_CLEAR Clear for cectx_frame_discarded_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_frame_discarded_irq Value After Reset:0x0
4	WO	0x0	CECTX_NRETRANSMIT_FAIL_CLEAR Clear for cectx_nretransmit_fail_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_nretransmit_fail_irq Value After Reset:0x0
3	WO	0x0	CECTX_LINE_ERR_CLEAR Clear for cectx_line_err_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_line_err_irq Value After Reset:0x0
2	WO	0x0	CECTX_ARBLOST_CLEAR Clear for cectx_arblost_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_arblost_irq Value After Reset:0x0
1	WO	0x0	CECTX_NACK_CLEAR Clear for cectx_nack_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_nack_irq Value After Reset:0x0
0	WO	0x0	CECTX_DONE_CLEAR Clear for cectx_done_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_done_irq Value After Reset:0x0

HDMI TX Controller_CEC_INT_FORCE

Address: Operational Base(0x27DA0000) + offset (0x400C)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
12	WO	0x0	CECRX_NOTIFY_ERR_FORCE Force for cecrx_notify_err_irq Values: 0x1 (FORCE): Write 1 to trigger cecrx_notify_err_irq Value After Reset:0x0
11	WO	0x0	CECRX_EOM_FORCE Force for cecrx_eom_irq Values: 0x1 (FORCE): Write 1 to trigger cecrx_eom_irq Value After Reset:0x0
10	WO	0x0	CECTX_DRIVE_ERR_FORCE Force for cectx_drive_err_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_drive_err_irq Value After Reset:0x0
9	WO	0x0	CECRX_BUSY_FORCE Force for cecrx_busy_irq Values: 0x1 (FORCE): Write 1 to trigger cecrx_busy_irq Value After Reset:0x0
8	WO	0x0	CECTX_BUSY_FORCE Force for cectx_busy_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_busy_irq Value After Reset:0x0
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5	WO	0x0	CECTX_FRAME_DISCARDED_FORCE Force for cectx_frame_discarded_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_frame_discarded_irq Value After Reset:0x0
4	WO	0x0	CECTX_NRETRANSMIT_FAIL_FORCE Force for cectx_nretransmit_fail_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_nretransmit_fail_irq Value After Reset:0x0
3	WO	0x0	CECTX_LINE_ERR_FORCE Force for cectx_line_err_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_line_err_irq Value After Reset:0x0
2	WO	0x0	CECTX_ARBLOST_FORCE Force for cectx_arblost_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_arblost_irq Value After Reset:0x0
1	WO	0x0	CECTX_NACK_FORCE Force for cectx_nack_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_nack_irq Value After Reset:0x0

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Bit	Attr	Reset Value	Description
0	WO	0x0	CECTX_DONE_FORCE Force for cectx_done_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_done_irq Value After Reset:0x0

24.5 Interface Description

Table 24-1 HDMI TX PHY Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
hdmitx_ln0_txdp	O	HDMI_TX_D0P/EDP_TX_D0P	NS
hdmitx_ln0_txdn	O	HDMI_TX_D0N/EDP_TX_D0N	NS
hdmitx_ln1_txdp	O	HDMI_TX_D1P/EDP_TX_D1P	NS
hdmitx_ln1_txdn	O	HDMI_TX_D1N/EDP_TX_D1N	NS
hdmitx_ln2_txdp	O	HDMI_TX_D2P/EDP_TX_D2P	NS
hdmitx_ln2_txdn	O	HDMI_TX_D2N/EDP_TX_D2N	NS
hdmitx_ln3_txdp	O	HDMI_TX_D3P/EDP_TX_D3P	NS
hdmitx_ln3_txdn	O	HDMI_TX_D3N/EDP_TX_D3N	NS
hdmitx_sbdp	I/O	HDMI_TX_SBDP/EDP_TX_AUXP	NS
hdmitx_sbdn	I/O	HDMI_TX_SBDN/EDP_TX_AUXN	NS
hdmitx_cec_m0	I/O	DSM_AUD_LP_M1/SAI4_MCLK_M2/HDMI_TX_CEC_M0/I2C7_SCL_M3/SPI4_CSN1_M0/UART11_TX_M2/PWM1_CH5_M1/GPIO4_C0_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[3:0]==0x9
hdmitx_cec_m1	I/O	PDM0_CLK1_M0/HDMI_TX_CEC_M1/SPI0_CSN1_M0/PWM0_CH1_M0/GPIO0_C3_d	PMUIO1_IOC_GPIO0C_IOMUX_SEL_L[15:12]==0x9
hdmitx_hpd_m0	I/O	DSM_AUD_LN_M1/HDMI_TX_HPDIN_M0/PCIE1_CLKREQN_M3/I2C7_SDA_M3/EDP_TX_HPDIN_M0/UART11_RX_M2/PWM0_CH1_M1/GPIO4_C1_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[7:4]==0x9
hdmitx_hpd_m1	I/O	SDMMC0_PWREN/SDMMC1_DETN_M2/HDMI_TX_HPDIN_M1/EDP_TX_HPDIN_M1/PWM1_CH2_M0/GPIO0_B6_d	PMUIO1_IOC_GPIO0B_IOMUX_SEL_L[11:8]==0x9
hdmitx_scl	I/O	DSM_AUD_RP_M1/HDMI_TX_SCL/I2C2_SCL_M3/CAN0_TX_M1/UART9_TX_M2/PWM2_CH0_M1/GPIO4_C2_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[11:8]==0x9
hdmitx_sda	I/O	DSM_AUD_RN_M1/HDMI_TX_SDA/I2C2_SDA_M3/CAN0_RX_M1/UART9_RX_M2/PWM2_CH1_M1/GPIO4_C3_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[15:12]==0x9

Notes: I=input, O=output, I/O=input/output, bidirectional

24.6 Application Notes

24.6.1 Controller Programming Model

The figure below shows the recommended programming sequence to build an HDMI-compliant system. The main operation mode is the HDMI TX Controller’s configuration.

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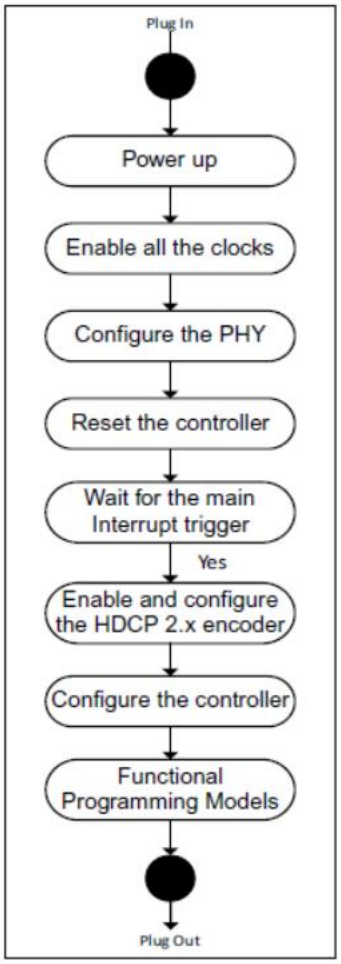


Fig. 24-6 Programming Sequence

24.6.1.1 Enabling the clocks

Enable all the clocks. The different clocks and their functions are the lists.

- apb_pclk: APB system interface clock.
- audclk: Audio interface clock.
- ARC_bpclk: ARC RX audio interface biphase clock.
- ipi_clk: IPI interface clock.
- linkqpclk: Link quad-pixel clock.linkqpclk acts as TDMS clock in HDMI mode and as FRL clock in FRL mode. Synchronous to HDCP14 Encoder.
- refclk: Reference clock. Generates timer bases of different frequencies which can be used by counters of different timers. Synchronous to I2C master.
- vidqpclk: Video datapath clock.

24.6.1.2 Configuring the PHY

Configure the PHY as the HDMI eDP Combo PHY user guide (if applicable). Drive the required system and configuration clocks and pins with the required clock frequency.

24.6.1.3 Resetting the Controller

Reset the controller using the imainrst_n signal.

24.6.1.4 Triggering the Main Interrupt

Wait for the main interrupt line omain_int to be triggered. The apb_regbank_ready_irq is unmasked by default and notifies the software that the reset operation is complete and APB interface is online.

24.6.1.5 Configuring the HDCP 2.x Encoder

Enable and configure the HDCP2.x as per the HDCP2.x user guide (if applicable).

24.6.1.6 Configuring the Controller

This section describes the steps involved in configuring the HDMI TX Controller. Configure the timer_reference_base field of the timer_base_config0 register and wait for the timer_base_locked_irq interrupt to be triggered.

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24.6.1.6.1 Configuring the Link

Configure the following components using the link_config0 register, DVI or HDMI, TMDS or FRL, FRL 3L or FRL 4L.

24.6.1.6.2 Configuring the Packets

Configure the following packet properties using the pktsched_* and pkt_<packet_type>* registers (if applicable), Packet contents - Register Writes, Scheduling options for the different packets.

24.6.1.6.3 Configuring the HDCP 1.4 Encoder

Configure the HDCP 1.4 using the hdcp14_* registers.

1. Write the hdcp14_an_value_high/low fields of the hdcp14_key_h/l registers.
2. Set HDCP 14 key encryption enable using the hdcp14_key_decrypt_en field of the hdcp14_config* registers if necessary.
3. Configure the decryption SEED using the hdcp14_key_decrypt_seed field of the hdcp14_key_seed register. Configure the HDCP An value, using the hdcp14_an_value_high/low fields of the hdcp14_an_h/l registers.
4. If the DKSET is stored in the register bank-(HDMI_QP_TX_HDCP14_DKSET_EXTERNAL=0) Write the HDCP keys in order, using the hdcp14_key_high/low fields of the hdcp14_key_h/l registers. For each HDCP Key, the MSB part (hdcp14_key_high), should be written first. Write the hdcp_aksv_high/low fields of the hdcp_aksv_h/l (40-bits for the hdcp_aksv_high) registers.
5. Initialize the HDCP Memories. Write the HDCP 1.4 KSV list in the revocation memory.
6. Update the HDCP HPD status using the hdcp14_hpd field of the hdcp14_config* registers.

24.6.1.6.4 Configuring the Audio Settings

Configure the audio settings, enable the interfaces, format status, pair layout, and so on using the audio_interface_[config/control/status]0 registers. Configuration of the number of active lanes and audio formats for the Serial Audio interface. Configure the related audio packet types-ACR, AMD, AUDI, ACP, ISRC BPCUV, user data, and others that can be overridden if they are not provided at audio interface input.

24.6.1.6.5 Configuring the Video Settings

Configure the pixel repetition factor using the vid_pr_factor [3:0] field of the video_interface_config1 register if required.

24.6.1.6.6 Configuring the SCDC

Configure the SCDC using the scdc_* and i2cm_* registers. You can configure the Scrambling, TMDS clock ratio, RR enable, FRL Rate, FFE levels, and so on.

24.6.1.6.7 Enabling Audio and Video Inputs

Provide data at the audio and video inputs.

24.6.1.6.8 Link Training

The Link Training procedure described in this section, requires the HDMI 2.1 TX Support parameter to be enabled. Otherwise, you should skip the Step 1.

1. Disable the video datapath of the AVP module by setting the avp_datapath_video_swdisable field of the global_swdisable register. This enables the generation of GAPs only.
2. Update the scdc_config0 register to choose between. Polling by setting the scdc_upd_flags_poll_en field, or read request by setting the scdc_rr_en field. If you want to set an automatic clear after a read operation, set the scdc_upd_flags_audo_clr field.
3. Check if the update flag scdc_upd_flags_1/0 (Polling FLT_ready) has been changed by reading scdc_status0 register when the scdc_upd_flags_rd_irq interrupt of the mainunit_1_int_status register is triggered.
4. When the the FLT_ready is set, configure the FRL rate and the FFE levels on the Sink. To perform this write operation using the I2C, set the I2CM_write field of the I2CM_interface_control0 register. The FFE levels should also be set using the flt_ffe_levels field of the flt_config0 register.
5. Set the flt_start_p field of the flt_control0 register to start LTS:3. Hardware triggers the flt_exit_to_ltsp_irq interrupt of the mainunit_1_int_status register, after LTS:3 is complete. The hardware automatically completes all the LTS:3 operations.

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6. Clear FLT_Update and monitor the scdc_upd_flags_clr_irq field of the mainunit_1_int_status register or the scdc_upd_flags_rd_p fields of the scdc_control0 register. Set the scdc_upd_flags_rd_p field of the scdc_control0 register to trigger an automatic read operation.
7. Check if the update flag scdc_upd_flags_1/0 has been set (Polling FRL_start) by reading the scdc_status0 register, when the scdc_upd_flags_rd_irq interrupt of the mainunit_1_int_status register is triggered. If scdc_upd_flags_* is set Link Training is complete.
8. Unset the avp_datapath_video_swdisable field of the global_swdisable register.

24.6.2 HDMI Audio and Video Programming Model

24.6.2.1 Audio Interface Programming Model

24.6.2.1.1 Audio Interfaces Configurations

The audio interface configurations can be performed using the audio_interface_config0 and audio_interface_config1 registers. Monitoring the audio interfaces can be performed using the audio_interface_status0 register and other interrupts. The required system configurations for the different audio interfaces are described in the following sections.

24.6.2.1.1.1 I2S Interface

The following section describes the system configurations for the I2S audio interface.
1. Select the I2S interface as the audio source, by setting the aud_if_sel[1:0] field of the audio_in-terface_config0 register to 2'h1.
2. Enable the active I2S lanes by configuring i2s_lines_en[3:0] field of the audio_interface_con-fig0 register. Each bit enables the respective data lane, i2s_lines_en[0] enables lane 0, i2s_lines_en[1] enables lane 1, i2s_lines_en[2] enables lane 2, i2s_lines_en[3] enables lane 3.
3. Enable the reception of the BPCUV bits (when transmitted), by setting i2s_bpcuv_en field of the audio_interface_config0 register to 1’b1.
4. Configure the audio format that is being received by writing the desired value to aud_format[2:0] field of the audio_interface_config0 register as shown in the list.
Audio Sample is Packet Type. Packet Type Value is 0x2, aud_format is 0x0.
HBR Audio Sample is Packet Type. Packet Type Value is 0x9, aud_format is 0x3.
Multi-Stream Audio Sample is Packet Type. Packet Type Value is 0xe, aud_format is 0x4.
5. When BPCUV bits reception is enabled, by default the B bit is extracted from the information received in the left channel. It is possible to force the receiver to extract the B bit from the right channel by setting the i2s_bbit_right field of the audio_interface_config0 register to 1’b1.
6. I2S operation can be monitored through the following interrupts, i2s_ws_err_irq interrupt indicates an illegal variation detected on iws_ws signal, i2s_bbit_err_irq interrupt indicates a mismatch between the B bits received in the left and right channels.

24.6.2.1.1.2 S/PDIF Interface

The following section describes the system configurations for the S/PDIF audio interface. 1. Select the S/PDIF interface as the audio source, by setting aud_if_sel[1:0] field of the audio_interface_config0 register to 2'h2.
2. Enable the active S/PDIF lanes by configuring spdif_lines_en[3:0] field of the audio_interface_config0 register. Each bit enables the respective data lane, spdif_lines_en[0] enables lane 0, spdif_lines_en[1] enables lane 1, spdif_lines_en[2] enables lane 2, spdif_lines_en[3] enables lane 3.
3. Configure the audio format that is being received by writing the appropriate value to aud- format[2:0] field of the audio_interface_config0 register.
4. Data reception is done independently for each lane since there are four S/PDIF lanes.
5. It is possible to have a timing mismatch in the reception of the two different channels. By default, S/PDIF data is sampled using the timing of S/PDIF lane 0. This can be changed by configuring a different lane in spdif_pair_sel[1:0] field of the audio_interface_config0 register, 2’h0 selects lane 0, 2’h1 selects lane 1, 2’h2 selects lane 2, 2’h3 selects lane 3.
6. Monitor the S/PDIF reception through the following register bank entries. a. When data is being received correctly on the S/PDIF lines, the corresponding entries within the {spdif_line0_lock spdif_line1_lock spdif_line2_lock spdif_line3_lock} fields are enabled (set to 1’b1) b. Parity errors in the received data are signaled for the different S/PDIF lines

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through the spdif_line0_parity_err, spdif_line1_parity_err, spdif_line2_parity_err, and spdif_line3_parity_err interrupts c. Encoding errors in the received information are signaled for the different S/PDIF lines through the spdif_line0_protocol_err, spdif_line1_protocol_err, spdif_line2_proto-col_err, and spdif_line3_protocol_err interrupts.

24.6.2.1.2 Audio Storage

The received audio data may need to be stored before being transmitted; for example, audio received during an active video line can only be transmitted in the next blanking period. The audio storage can be configured and monitored through the following fields.
1. Overflows and underflows are signaled by the audfifo_ovf_irq and audfifo_udf_irq interrupts, respectively.
2. Audio FIFO can be cleared by setting the audfifo_clr_p field of the audio_interface_control0 register to 1’b1.
3. Audio FIFO can be configured to automatically clear itself, when an overflow occurs by setting the audfifo_init_on_ovf field of the audio_interface_config0 register to 1’b1.

24.6.2.2 Audio Packetizer Programming Model

24.6.2.2.1 Configure Audio Transmission

You should perform this process only if the HDMI TX Controller is configured in HDMI mode. In DVI mode, audio is not transmitted. The selected audio mode should be supported by the source (transmitter) and the sink (receiver) of the audio. The audio capabilities of the receiver are extracted from the E-EDID information. The steps to configure audio transmission are as follows.
1. Disable all audio sources.
2. Enable the audio data path of the AVP module by writing 1'b0 to the avp_datapath_packet_audio_swdisable field of the global_swdisable register.
3. Perform the reset of the audio data path of the AVP module by writing 1'b1 to the avp_datapath_packet_audio_swinit_p field of the global_swreset_request register.
4. Disable the transmission of the AUDS, ACR, AUDI, and AMD packets by writing 1'b0 to their corresponding fields as shown, AUDS: pktsched_auds_tx_en, ACR: pktsched_acr_tx_en. AUDI: pktsched_audi_tx_en, AMD: pktsched_amd_tx_en.
5. Select and configure the audio interfaces I2S, S/PDIF.
6. Configure the audio parameters. a. Audio Clock Regeneration.
i. Fix the audio at N factor for Audio Clock Regeneration. This factor depends on the audio sampling rate and video mode. For more information, see the *HDMI 2.1 Specification*.
ii. Write the audpkt_acr_n_value field of the audpkt_acr_control0 register.
iii. Set audio CTS factor for Audio Clock Regeneration.
7. Enable the transmission of the ACR, AUDI, and AMD packets by writing 1'b1 to their corresponding bit fields as shown, ACR: pktsched_acr_tx_en, AUDI: pktsched_audi_tx_en, AMD: pktsched_amd_tx_en.
8. Enable the transmission of the AUDS packet by writing 1'b1 to the pktsched_auds_tx_en field of the pktsched_pkt_en register.
9. Enable the audio sources according to the selected interface.
10.At this step, the software can continue to transmit the audio that it configured in the frames, or go back to Step 1 to reconfigure a new audio setup.

24.6.3 CEC Programming Model

24.6.3.1 Sending a Frame

The steps to send a CEC frame are as follows. 1. Write the frame message size (in bytes), to the cec_rxbuffer_cnt field of the cec_rx_count register.
2. Write the data to be transmitted, to the cec_rxbuffer_data_## (## represents 0 to 15).
a. The first cec_rxbuffer_data_0 byte is the header block and is mapped as cec_rxbuffer_data_0[7:0]={Initiator_address[3:0], Destination_address[3:0]}.
b. Fill the rest of the cec_rxbuffer_data_[15:1] fields with the data bytes to be transmitted (if necessary).
3. Order the CEC to send the frame by writing 1 to the frame_send_set_p field of the cec_tx_control register.
4. If the frame is: Successfully sent, then the cectx_done_irq field of the cec_int_status register is asserted. Not sent successfully, then one or more of the following interrupts can be triggered: cectx_nack_irq field of the cec_int_status register; cectx_arblost_irq field of

the cec_int_status register; cectx_line_err_irq field of the cec_int_status register; cectx_nretransmit_fail_irq field of the cec_int_status register; cectx_frame_discarded_irq field of the cec_int_status register.

24.6.3.2 Read a Received Frame

The steps to read a received frame are as follows:

1. The software is informed that a frame is received successfully when the cecrx_eom_irq field of the cec_int_status register is triggered.
2. Read the cec_tx_count register to obtain information about: a. cec_txbuffer_cnt–number of bytes received (including header).
3. Read the necessary bytes from the TX buffer registers cec_txbuffer_data_## (0-15) accordingly with the information obtained in the cec_rx_count_status bit field.

24.6.3.3 Initial CEC Configuration

To use the CEC module, you must set up the following configuration registers.

24.6.3.3.1 CEC Configuration Register

The table shows the CEC configuration register cec_config and the different fields associated with the initial configuration.

Table 24-2 CEC Configuration Register

Field Name	Functionality
txreq_discard_if_rxbusy	Discards a transmit request (cec_ctrl.send=1) if receiver is busy
broadcast_nack	NACK to any received broadcast message by the CEC module. Message is not stored in the receiver registers.
cecfilter	Enable the CEC input filter.
frame_nretrans	Enable the CEC input filter.
rx_automatic_drive_acknowledge	Receiver automatic drive acknowledge.
signal_free_time	Selects the Signal Free time period that is to be respected before attempting to transmit or re-transmit a frame. If 0 is selected then the controller follows the HDMI specification in CEC 9.1 Signal free time.

24.6.3.3.2 CEC Address Register

The CEC address register-cec_addr should be set when the logical allocation is completed. You can define multiple addresses.

24.6.3.4 Cancel a TX Frame

You can cancel a TX frame by writing 1’b1 to the frame_send_clr field of the cec_tx_control register, if the frame to be transmitted is waiting for the end of an incoming frame (RX busy); the frame is set to be re-transmitted.

If the TX frame is already under transmission, then it is pushed to completion and not cancelled.

24.6.3.5 Status Fields

The table shows the CEC status register cec_status and the different fields associated with the initial configuration.

Table 24-3 Status Fields

Field Name	Functionality
frame_send_pending_st	Frame is set to be transmitted. It is 1’b1 while a transmission is ongoing.
cecrx_busy_st	The CEC module is busy receiving a frame.
cectx_busy_st	The CEC module is busy transmitting a frame.

24.6.3.6 Interrupts

The table shows the CEC interrupts available in the cec_int_status register and conditions under which it is triggered.

Table 24-4 CEC Interrupts

Field Name	Functionality
cectx_done_irq	Frame transmission is completed successfully
cectx_nack_irq	NACK for direct address or broadcast is received

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	while transmitting a frame
cectx_arblost_irq	CEC line arbitration is lost to another initiator
cectx_line_err_irq	Line error while transmitting a frame (detected a 0 instead of a 1)
cectx_nretransmit_fail_irq	All re-transmission attempts failed.
cectx_frame_discarded_irq	Frame to be sent was discarded since a new frame was received. Happens only when txreq_discard_if_rxbusy==1'b1.
cectx_busy_irq	The CEC TX FSM changes its busy state.
cecrx_busy_irq	The CEC RX FSM changes its busy state.
cectx_drive_err_irq	Drive zero in the CEC output is not seen in the CEC input.
cecrx_eom_irq	Frame is fully received with EOM after the last data block.
cecrx_notify_err_irq	Bit timing error is detected while cecrx_busy_irq is set. Error notification is sent to initiator.

24.6.3.7 CEC Bit Timing Fine Tuning

This is a debug-only feature that allows out-of-spec timings to be defined; to debug the CEC module. You can configure this feature by using the cec_rxqual_bittime_config register.

24.6.4 GRF Setting for HDMITX

24.6.4.1 GRF Setting for hpd func

IF you want to use the HPD func. Pls check below this register.

a. Register Name MISC_CON0 (offset addr 0x400 in VCCIO6_IOC domain)

HDMITX HDP control bits

Bit7-0: store the hpd low level keep time.

For example: if we set the value is 120 and also we set bit13-8 (any bit is 1) . If the iopad hpd keep low time large than 120ms , then the internal hpd port from high to low. if the iopad hpd keep low time smaller than 120ms, then we think th einternal hpd port is keep high.

Bit13-8: if any bit set to 1, then enable the low level keep func.

Bit15-14:

2'b01: The hpd irq internal port use the iopad hpd port.

2'b10 or 2'b11: The hpd irq internal port use the register port ,This mean use the after meta state port . it is better.

2'b00: The hpd irq internal port use the glitch free port . This is the very stable port . it is best and also the default configuration.

b. Register Name HDMITX_HPD_STATUS （offset addr is 0x440, in VCCIO6_IOC domain）

HDMITX HDP status

Bit7: 1'b0: means the hpd keep low more than the set Xms. (X value range from 1 to 250). 1'b1 means not keep low more than the set Xms.

Bit6: 1'b0: means the internal hpd port is 0. 1'b1: means the internal hpd port is 1.

Bit 5: 1'b0: means the external iopad hpd port is 0. 1'b1: means theexternal iopad hpd port is 1.

Bit 4: 1'b1: means the irq is active. 1'b0: means irq is not avtive.

Bit 3: 1'b1: means the internal hpd level is 1. 1'b0:mean it is 0.

Bit 2-0: stor the ihpd port change times.

24.6.4.2 GRF Setting for ebc_vop func

IF you want to enable the ebc vop lite path to hdmi tx controller .

Use the below setting for it.

Step1: GRF_V00_CON13 [4] = 1'b1 ; // it enable the grf_sw_hdmi_1to4 with hdmi mode.

Step2: GRF_VO0_CON09 [9] = 1'b1 ; // it enable the hdmi controller data source com from

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ebc.

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Chapter 25 HDMI TX/eDP Combo PHY

25.1 Overview

This chapter describes an overview of HDMI TX/eDP Combo PHY. HDMI TX/eDP Combo PHY is a PHY hard macro to support HDMI TX and eDP interfaces. Combo transmit-PHY for HDMI2.1 TMDS Link, FRL Link, eDP Link.Maximum data rate of 12Gbps (HDMI2.1 FRL) and minimum data rate of 250Mbps (HDMI2.1 TMDS). For the convenience of writing, we also name HDMI TX/eDP Combo PHY as HDPTX PHY.

- HDMI2.1
  - AC coupled voltage mode drivers for HDMI2.1 TMDS links
  - Supports all the data rates in FRL: 3, 6, 8, 10 and 12Gbps
  - Supports Single Ref-clock input and multiple TMDS/Pixel clock frequencies
  - Supports Pixel clock input (25MHz to 594MHz) with TMDS multiplication
  - Supports 3 TAP FFE support for FRL mode
  - Single ended and common mode ARC support
  - Supports 20/40 bits parallel data interface for HDMI 2.0 operation
  - Supports 18/36 bits parallel data interface for HDMI 2.1 operation
  - Supports symbol clock output with configurable divider option for link operation
  - Supports Pixel clock output for link operation
  - Supports 4 lane Fixed Rate Link operation with 3Gbps, 6Gbps, 8Gbps, 10Gbps and 12Gbps rates
  - Supports 24MHz reference clock
  - Supports channel swap function for HDMI 2.0 back compatible operation
- eDP
  - Supports RBR (1.62Gbps per lane), HBR (2.7Gbps per lane) and HBR2 (5.4Gbps per lane) data rates
  - Supports training table with swing-level 0-3 and pre-emphasis-level 0-3
  - Supports AUX function as required by DP PHY implementing TX main link
  - Supports x1, x2 and x4 configurations
  - Supports 24MHz reference clock

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25.2 Block Diagram

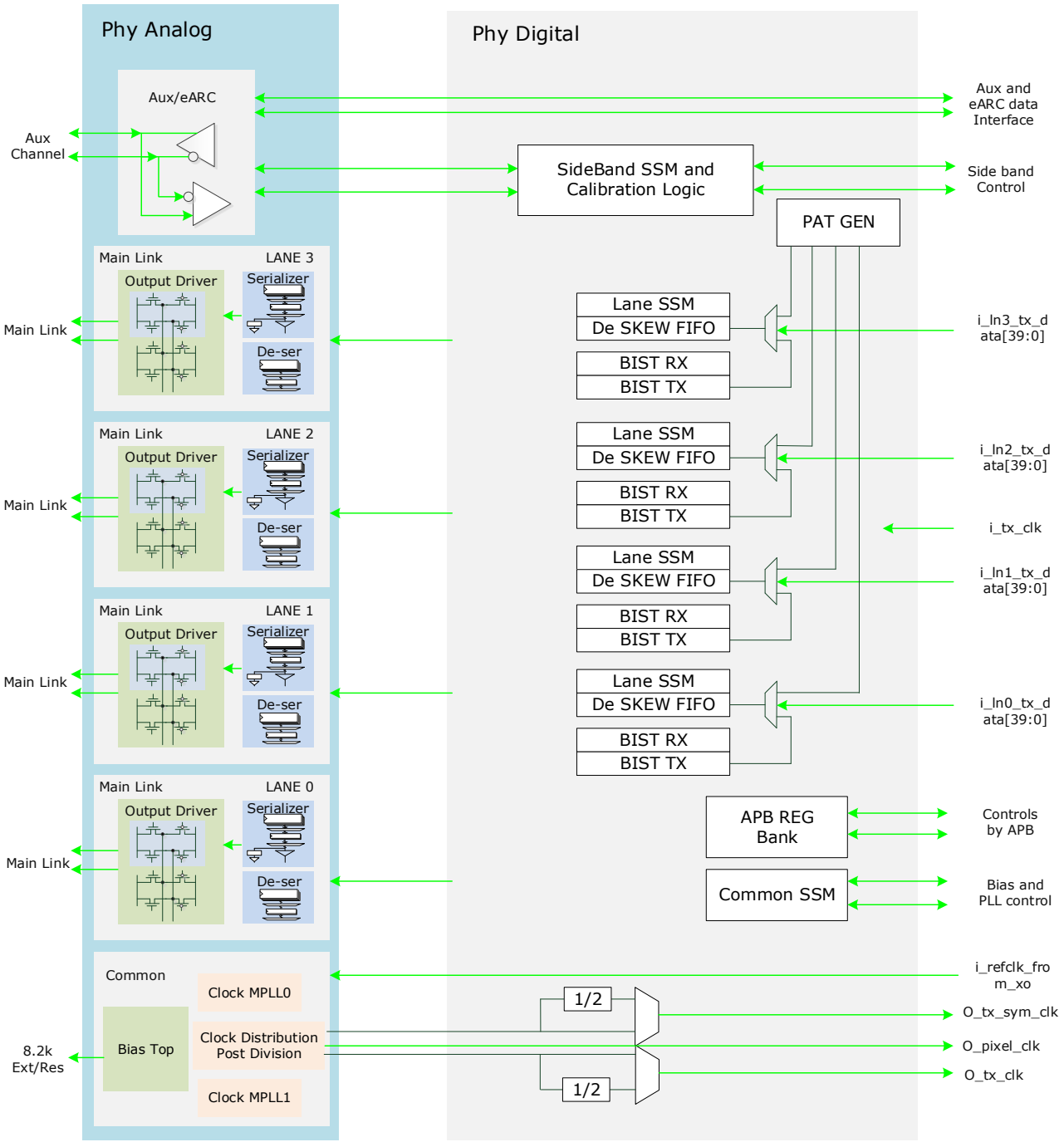


Fig. 25-1 Block Diagram of HDMI TX/eDP Combo PHY

Above figure shows the block diagram of HDMI TX/eDP Combo PHY. It comprises of one CMN, four lanes of transmitter, one sideband that supports AUX channel for eDP and one PHY digital. The common block consists of one Band Gap, one Bias generation block and one PLL.

25.3 Function Description

25.3.1 PHY Analog

HDMI TX/eDP Combo PHY comprises of a PHY analog and PHY digital. The PHY consists of: One CMN block, a sideband block to support AUX for DP and ARC HDMI and Four Transmit lanes.

25.3.1.1 CMN

The CMN consists of a band-gap reference (BGR), bias generator and PLL. The BGR circuit generates high-accuracy reference voltage of 820mV across PVT variation. A bias generator

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makes two kinds of current, external-and internal-resistor (RMRES)-referred current, and these currents are distributed to each block in CMN and lanes. The external resistor-referred (REXT) current is generated using an 8.2KΩ resistor which is connected between the rext pad and ground outside the chip. On the other hand, the internal resistor-referred current is generated using internally integrated replica resistor to compensate resistance error across PVT variation. The PLL in the CMN synthesizes high-speed clock, which is used for TX serializer, from a reference clock. The reference clock can be selected from three clock sources; crystal oscillator, SoC PLL's output reference clock.
The following are the main features of the PLL:
Supports LC PLL for 5 ~ 6GHz clock.
Supports sigma-delta modulated fractional divider.
Automatic Frequency Calibrated (AFC) oscillator setting for the desired frequency of operation Programmable charge pump current and loop filter resistance allowing for wide range of programmable loop bandwidth and peaking.

25.3.1.2 TRANSMITTER

The TX comprises serializer, driver, common-mode (CM). The driver generates baud-rate voltage waveform on TX output pads, ln01/1/2/3_txdp/n, with 3-tap FIR filter function. The main driver has hybrid structure, by combining voltage-and current-mode driver in parallel, to achieve both a small power consumption and large voltage swing. The voltage-mode driver is activated in default, but the current mode driver is optional to improve the TX output swing.
The driver also supports 3-tap FIR filter to suppress one pre and one post-cursor according to the HDMI2.1 FRL specification. The driver has the resolution of 1/36 in controlling amplitude and filter ratio, and maximum ratio of pre-shoot and de-emphasis are 15/36 and 8/36, respectively.

25.3.1.3 Side Band block

The side block consists of a termination block, a push-pull voltage buffer, a lower speed receiver and a PWM receiver. These blocks work in AC coupled AUX-RXTX.

25.3.1.3.1 Push Pull Voltage buffer (AUX Driver)

A push voltage buffer has been used to have very slow slew (5 to 30ns) on the line during transmission. The transmitter can be configured to drive wither common mode data or differential mode data on the line. During reception mode the buffer hold the line in common mode. This driver is also responsible for boundary scan driver.

25.3.1.3.2 Termination

The side-band is always terminated to 50 Ohms internally. The common mode of the termination is set by the push-pull voltage buffer described above. The termination block is designed such that same calibration code of main link transmitter can be used.

25.3.1.3.3 A lower speed receiver (AUX Receiver)

The lower speed receiver is responsible to receive 1Mbps differential AUX data. In ARC mode this listens to only sbdp line. This receiver has a pad interface which practically works as differential line to common mode voltage generation just by adding the voltage waveforms at sbdp and sbdn line. The following figure depicts the usage of pad interface and data multiplexing.

25.3.2 HDMI/eDP Combo PHY Source Power States

This section describes the PHY power states. It describes the four power states for PHY. ON state is the normal operational state or mission mode for the PHY. The allowed power state transitions are described in the following figure. For all power state transitions, ensure that the MAC/SoC does not initiate any operational sequence or further power state transition until the PHY indicates that the initial state transition is completed.

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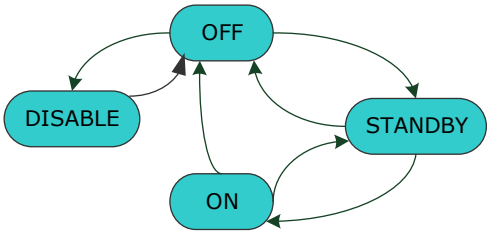


Fig. 25-2 PHY Power state transition flow diagram

Table 25-1 HDMI TX/eDP Combo PHY Power States

State	Description	Exit Latency Duration
OFF	***Reset state of PHY. All the blocks will be in power down mode.*** This is PHY reset mode but serial lines are weakly held to common mode to provide a current path during transient if SINK is connected to high voltage termination (HDMI) or board pull up (eDP) supply is coming up. Reference clock supplied to PHY may be turned off.	-
DISABLE	***Low power saving mode with low recovery time latency*** This is lowest power modes of PHY-Analog. When reduced or no lanes are used by SoC by APB configuration the PHY-Analog can be set to.	-
STANDBY	***Clock ready state*** The common block is brought and calibration for all required analog blocks are completed in this state. Some LANES can be in DISABLE state. Remaining active LANES are waiting for the LINK Layer/SoC to send parallel data. All the interface clock is ready and o_phy_rdy, o_phy_clk_rdy and o_sb_rdy is asserted high. The serial lines are held in common mode. This state is very important for the AC coupled system to charge the common mode of the line.	>200us
ON	***Normal operation mode***	-

25.4 Register Description

25.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

25.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
HDPTXPHY_CMN_REG0000	0x0000	W	0x00000004	CMN Register
HDPTXPHY_CMN_REG0008	0x0020	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0009	0x0024	W	0x0000000C	CMN Register
HDPTXPHY_CMN_REG000A	0x0028	W	0x00000083	CMN Register

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Name	Offset	Size	Reset Value	Description
HDPTXPHY_CMN_REG000B	0x002C	W	0x00000006	CMN Register
HDPTXPHY_CMN_REG0020	0x0080	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0021	0x0084	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0025	0x0094	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0028	0x00A0	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG002D	0x00B4	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG002E	0x00B8	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG002F	0x00BC	W	0x00000004	CMN Register
HDPTXPHY_CMN_REG003C	0x00F0	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG003D	0x00F4	W	0x00000040	CMN Register
HDPTXPHY_CMN_REG004E	0x0138	W	0x00000034	CMN Register
HDPTXPHY_CMN_REG0051	0x0144	W	0x0000007D	CMN Register
HDPTXPHY_CMN_REG0053	0x014C	W	0x0000007D	CMN Register
HDPTXPHY_CMN_REG0055	0x0154	W	0x0000007D	CMN Register
HDPTXPHY_CMN_REG005A	0x0168	W	0x00000033	CMN Register
HDPTXPHY_CMN_REG005C	0x0170	W	0x00000025	CMN Register
HDPTXPHY_CMN_REG005E	0x0178	W	0x0000004F	CMN Register
HDPTXPHY_CMN_REG0060	0x0180	W	0x0000004E	CMN Register
HDPTXPHY_CMN_REG0063	0x018C	W	0x0000004E	CMN Register
HDPTXPHY_CMN_REG0064	0x0190	W	0x0000000F	CMN Register
HDPTXPHY_CMN_REG0065	0x0194	W	0x00000014	CMN Register
HDPTXPHY_CMN_REG0069	0x01A4	W	0x00000002	CMN Register
HDPTXPHY_CMN_REG006C	0x01B0	W	0x00000013	CMN Register
HDPTXPHY_CMN_REG0070	0x01C0	W	0x00000018	CMN Register
HDPTXPHY_CMN_REG0074	0x01D0	W	0x00000005	CMN Register
HDPTXPHY_CMN_REG0081	0x0204	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0082	0x0208	W	0x00000000	CMN Register

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Name	Offset	Size	Reset Value	Description
HDPTXPHY_CMN_REG0083	0x020C	W	0x00000024	CMN Register
HDPTXPHY_CMN_REG0084	0x0210	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0085	0x0214	W	0x00000002	CMN Register
HDPTXPHY_CMN_REG0086	0x0218	W	0x00000010	CMN Register
HDPTXPHY_CMN_REG0087	0x021C	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0089	0x0224	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0095	0x0254	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0097	0x025C	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0099	0x0264	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG009A	0x0268	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG009B	0x026C	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG009E	0x0278	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG009F	0x027C	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG00A0	0x0280	W	0x00000000	CMN Register
HDPTXPHY_SB_REG0102	0x0408	W	0x00000003	Sideband Register
HDPTXPHY_SB_REG0103	0x040C	W	0x00000018	Sideband Register
HDPTXPHY_SB_REG0104	0x0410	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0105	0x0414	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0106	0x0418	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0109	0x0424	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG010D	0x0434	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG010F	0x043C	W	0x00000001	Sideband Register
HDPTXPHY_SB_REG0110	0x0440	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0113	0x044C	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0114	0x0450	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0115	0x0454	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0116	0x0458	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0117	0x045C	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0118	0x0460	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0119	0x0464	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG011A	0x0468	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG011B	0x046C	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG011C	0x0470	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG011D	0x0474	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG011E	0x0478	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG011F	0x047C	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0120	0x0480	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0123	0x048C	W	0x00000000	Sideband Register

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Name	Offset	Size	Reset Value	Description
HDPTXPHY_INTOP_REG0200	0x0800	W	0x00000000	Lane Top Register
HDPTXPHY_INTOP_REG0201	0x0804	W	0x00000000	Lane Top Register
HDPTXPHY_INTOP_REG0203	0x080C	W	0x00000000	Lane Top Register
HDPTXPHY_INTOP_REG0204	0x0810	W	0x00000000	Lane Top Register
HDPTXPHY_INTOP_REG0205	0x0814	W	0x00000000	Lane Top Register
HDPTXPHY_INTOP_REG0206	0x0818	W	0x00000000	Lane Top Register
HDPTXPHY_INTOP_REG0207	0x081C	W	0x00000000	Lane Top Register
HDPTXPHY_LANE_REG0303	0x0C0C	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG0307	0x0C1C	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG030A	0x0C28	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG030B	0x0C2C	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG030C	0x0C30	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG030D	0x0C34	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG030E	0x0C38	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG030F	0x0C3C	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG0310	0x0C40	W	0x00000002	Lane 0 Register
HDPTXPHY_LANE_REG0311	0x0C44	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG0312	0x0C48	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG0316	0x0C58	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG031B	0x0C6C	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG031F	0x0C7C	W	0x00000014	Lane 0 Register
HDPTXPHY_LANE_REG0320	0x0C80	W	0x000000A0	Lane 0 Register
HDPTXPHY_LANE_REG0403	0x100C	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG0407	0x101C	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG040A	0x1028	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG040B	0x102C	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG040C	0x1030	W	0x00000000	Lane 1 Register

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Name	Offset	Size	Reset Value	Description
HDPTXPHY_LANE_REG040D	0x1034	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG040E	0x1038	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG0410	0x1040	W	0x00000002	Lane 1 Register
HDPTXPHY_LANE_REG0411	0x1044	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG0412	0x1048	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG0416	0x1058	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG041B	0x106C	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG041F	0x107C	W	0x00000014	Lane 1 Register
HDPTXPHY_LANE_REG0503	0x140C	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG0507	0x141C	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG050A	0x1428	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG050B	0x142C	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG050C	0x1430	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG050D	0x1434	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG050E	0x1438	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG0510	0x1440	W	0x00000002	Lane 2 Register
HDPTXPHY_LANE_REG0511	0x1444	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG0512	0x1448	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG0516	0x1458	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG051B	0x146C	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG051F	0x147C	W	0x00000014	Lane 2 Register
HDPTXPHY_LANE_REG0520	0x1480	W	0x000000A0	Lane 2 Register
HDPTXPHY_LANE_REG0521	0x1484	W	0x00000014	Lane 2 Register
HDPTXPHY_LANE_REG0603	0x180C	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG0607	0x181C	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG060A	0x1828	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG060B	0x182C	W	0x00000000	Lane 3 Register

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Name	Offset	Size	Reset Value	Description
HDPTXPHY_LANE_REG060C	0x1830	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG060D	0x1834	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG060E	0x1838	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG0610	0x1840	W	0x00000002	Lane 3 Register
HDPTXPHY_LANE_REG0611	0x1844	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG0612	0x1848	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG0616	0x1858	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG061B	0x186C	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG061E	0x1878	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG061F	0x187C	W	0x00000014	Lane 3 Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

25.4.3 Detail Registers Description

HDPTXPHY_CMN_REG0000

Address: Operational Base(0x2B000000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_bgr_en Override enable for bgr_en.
6	RW	0x0	bgr_en BGR enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	ovrd_bgr_lpf_bypass Override enable for bgr_lpf_bypass.
4	RW	0x0	bgr_lpf_bypass BGR LPF bypass to reduce BGR settle time 1'b0: LPF enable 1'b1: LPF bypass
3:2	RW	0x1	ana_bgr_820m_sel BGR 820mV selection (for current bias) 2'b00: 780mV 2'b01: 820mV 2'b10: 860mV 2'b11: 900mV
1	RW	0x0	ana_bgr_clk_en BGR chopper clock enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	ana_bgr_ladder_en BGR output voltage selection 1'b0: BGR output 1'b1: Resistor ladder output

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HDPTXPHY_CMN_REG0008

Address: Operational Base(0x2B000000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_lcpll_en Override enable for lcpll_en.
6	RW	0x0	lcpll_en LC PLL enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	ana_lcpll_bea_con_clk_out_en Enable LCPLL beacon clock output
4	RW	0x0	ana_lcpll_lcv_co_mode_en Enable LCVCO mode
3	RW	0x0	ovrd_lcpll_afc_init_rstn Override enable for lcpll_afc_init_rstn
2	RW	0x0	lcpll_afc_init_rstn PLL AFC initial reset. When initial reset is asserted, the previous AFC result is reset. When initial reset is released, AFC starts from the initial AFC code given in i_rx_cdr_afc_sel_logic[3:0]. 1'b0: Reset 1'b1: Released
1	RW	0x0	ovrd_lcpll_afc_rstn Override enable for lcpll_afc_rstn
0	RW	0x0	lcpll_afc_rstn PLL AFC reset. When AFC reset is asserted, the previous AFC result is held. When AFC reset is released, AFC starts from the previous AFC code stored in internal memory. 1'b0: Reset 1'b1: Released

HDPTXPHY_CMN_REG0009

Address: Operational Base(0x2B000000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ana_lcpll_pi_afc_clk_div2_en PLL AFC clock frequency selection 1'b0: fVCO 1'b1: fVCO/2
4	RW	0x0	ana_lcpll_afc_bsel PLL AFC code manual selection enable 1'b0: AFC result 1'b1: Manual selection
3	RW	0x1	ana_lcpll_afc_en PLL AFC enable; if enabled, VCO frequency is automatically calibrated. If disabled, VCO starts to oscillate with fixed AFC code of i_pll_man_bsel_m and _l. 1'b0: Disable 1'b1: Enable
2	RW	0x1	ana_lcpll_afc_from_pre_code PLL AFC option in restart case 1'b0: Restart from initial AFC code 1'b1: Restart from previous AFC code

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	ana_lcpll_afc_man_bsel_l Manual PLL AFC code selection (LSB)

HDPTXPHY_CMN_REG000A

Address: Operational Base(0x2B000000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x8	ana_lcpll_afc_man_bsel_m Manual PLL AFC code selection (MSB)
3:0	RW	0x3	ana_lcpll_afc_stb_num Number of reference clock cycle to check VCO stabilization during PLL AFC start

HDPTXPHY_CMN_REG000B

Address: Operational Base(0x2B000000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:1	RW	0x3	ana_lcpll_afc_tol_num PLL VCO stabilization tolerance; VCO is considered as settled-down if |counter difference|<i_pll_afc_tol during i_pll_afc_stb_num
0	RW	0x0	ana_lcpll_afc_vci_force PLL control voltage force for open-loop test purpose 1'b0: Released 1'b1: Forced

HDPTXPHY_CMN_REG0020

Address: Operational Base(0x2B000000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	ana_lcpll_pms_mdiv PLL main divider setting Divider value = Setting code

HDPTXPHY_CMN_REG0021

Address: Operational Base(0x2B000000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	ana_lcpll_pms_mdiv_afc PLL main divider setting for AFC counter Divider value = Setting code

HDPTXPHY_CMN_REG0025

Address: Operational Base(0x2B000000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ana_lcpll_iqdiv_bypass VCO clock bypass IQ divider enable.
5	RW	0x0	ovrd_lcpll_pms_iqdiv_rstn Override enable for lcpll_pms_iqdiv_rstn
4	RW	0x0	lcpll_pms_iqdiv_rstn IQ divider resetn
3	RW	0x0	ovrd_lcpll_ref_chopper_clk_div_rstn Override enable for lcpll_ref_chopper_clk_div_rstn

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Bit	Attr	Reset Value	Description
2	RW	0x0	lcpll_ref_chopper_clk_div_rstn Chopper clk divider reset 1'b0: Reset 1'b1: Released
1:0	RW	0x0	ana_lcpll_ref_bypass_clk_sel PLL Bypass clock selection 2'b00: XO 2'b01: IO 2'b10: PIXEL or LC_OUT_CLK 2'b11: System PLL clock

HDPTXPHY_CMN_REG0028

Address: Operational Base(0x2B000000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ovrd_lcpll_sdm_rstn ovrd_lcpll_sdm_rstn
3	RW	0x0	lcpll_sdm_rstn PLL SDM reset 1'b0: Reset 1'b1: Released
2	RW	0x0	ana_lcpll_sdc_fractional_en Fractional clock divide in SDM clock generation 1'b0: Integer division 1'b1: Fractional division
1	RW	0x0	ovrd_lcpll_sdc_rstn Override enable for lcpll_sdc_rstn
0	RW	0x0	lcpll_sdc_rstn PLL SDM clock generation (SDC) reset 1'b0: Reset 1'b1: Release

HDPTXPHY_CMN_REG002D

Address: Operational Base(0x2B000000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ana_lcpll_sdm_ph_num_sel PLL PI input clock phase number 1'b0: 8-phase 1'b1: 4-phase
5:4	RW	0x0	ana_lcpll_sdm_pi_step PLL phase interpolstor step 2'b00: 1-step (16-phase) 2'b01: 2-step (8-phase) 2'b1x: 0.5-step
3:1	RW	0x0	ana_lcpll_sdc_n PLL SDC divide-ratio selection (MC_val=0 N, MC_val=1 N-1) 3'b000: /4/3 3'b001: /5/4 3'b010: /6/5 3'b100: /7/6 3'b101: /8/7 3'b110: /9/8

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Bit	Attr	Reset Value	Description
0	RW	0x0	ana_lcpll_sdc_n2 PLL SDC divide-ratio selection 1'b0: No additional/2 1'b1: Additional/2

HDPTXPHY_CMN_REG002E

Address: Operational Base(0x2B000000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	ana_lcpll_sdc_numerator Numerator of SDC (Max 65)

HDPTXPHY_CMN_REG002F

Address: Operational Base(0x2B000000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:2	RW	0x01	ana_lcpll_sdc_denominator Denominator of SDC (Max 65)
1	RW	0x0	ovrd_lcpll_sdc_ndiv_rstn Override enable for lcpll_sdc_ndiv_rstn
0	RW	0x0	lcpll_sdc_ndiv_rstn SDC NDIV Resetn.

HDPTXPHY_CMN_REG003C

Address: Operational Base(0x2B000000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	ana_lcpll_reserved PLL Reserved pins

HDPTXPHY_CMN_REG003D

Address: Operational Base(0x2B000000) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ropll_en Override enable for ropll_en.
6	RW	0x1	ropll_en RO PLL enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	ana_ropll_beacon_clk_out_en Enable ROPLL beacon clock output.
4	RW	0x0	ana_ropll_lcvco_mode_en Enable LCVCO mode.
3	RW	0x0	ovrd_ropll_afc_init_rstn Override enable for ropll_afc_init_rstn.
2	RW	0x0	ropll_afc_init_rstn PLL AFC initial reset. When initial reset is asserted, the previous AFC result is reset. When initial reset is released. AFC starts from the initial AFC code given in i_rx_cdr_afc_sel_logic[3:0]. 1'b0: Reset 1'b1: Released
1	RW	0x0	ovrd_ropll_afc_rstn Override enable for ropll_afc_rstn.

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Bit	Attr	Reset Value	Description
0	RW	0x0	ropll_afc_rstn PLL AFC reset. When AFC reset is asserted, the previous AFC result is held. When AFC reset is released, AFC starts from the previous AFC code stored in internal memory. 1'b0: Reset 1'b1: Released

HDPTXPHY_CMN_REG004E

Address: Operational Base(0x2B000000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ana_ropll_fld_non_continuous_mode Check frequency lock detection of PLL 1'b0: Once 1'b1: Continuously
6	RW	0x0	ana_ropll_fld_slow_bypass PLL slow frequency lock detection bypass 1'b0: No bypass 1'b1: Bypass
5	RW	0x1	ana_ropll_pi_en PLL phase interpolator enable 1'b0: Disable 1'b1: Enable
4:1	RW	0xa	ana_ropll_pi_str PLL phase interpolator input buffer strength control for Gen3 and Gen4 (for 8GHz VCO) 4'b0000: Min. strength .... 4'b1111: Max. strength
0	RW	0x0	ana_ropll_100m_clk_en Enable 100M clock.

HDPTXPHY_CMN_REG0051

Address: Operational Base(0x2B000000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x7d	ropll_pms_mdiv_rbr [rbr] PLL main divider setting Divider value = Setting code

HDPTXPHY_CMN_REG0053

Address: Operational Base(0x2B000000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x7d	ropll_pms_mdiv_hbr2 [hbr2] PLL main divider setting Divider value = Setting code

HDPTXPHY_CMN_REG0055

Address: Operational Base(0x2B000000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x7d	ropll_pms_mdiv_afc_rbr [rbr] PLL main divider setting for AFC counter Divider value = Setting code

HDPTXPHY_CMN_REG005A

Address: Operational Base(0x2B000000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x3	ropll_pms_sdiv_rbr [rbr] PLL post divider setting (N-1, except /7) 3'b000: /1 3'b001: /2 3'b010: /3 3'b011: /4 3'b100: /5 3'b101: /6 3'b110: X 3'b111: /8
3:0	RW	0x3	ropll_pms_sdiv_hbr [hbr]PLL post divider setting (N-1, except /7) 3'b000: /1 3'b001: /2 3'b010: /3 3'b011: /4 3'b100: /5 3'b101: /6 3'b110: X 3'b111: /8

HDPTXPHY_CMN_REG005C

Address: Operational Base(0x2B000000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ana_ropll_iqdiv_bypass VCO clock bypass IQ divider enable.
6	RW	0x0	ovrd_ropll_pms_iqdiv_rstn Override enable for ropll_pms_iqdiv_rstn.
5	RW	0x1	ropll_pms_iqdiv_rstn IO divider resetn.
4:3	RW	0x0	ana_ropll_ref_bypass_clk_sel PLL Bypass clock selection. 2'b00: X0 2'b01: IO 2'b10: PIXEL or LC_OUT_CLK 2'b11: System PLL clock
2	RW	0x1	ana_ropll_ref_chopper_clk_en Chopper clk enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	ovrd_ropll_ref_chopper_clk_div_rstn Override enable for ropll_ref_chopper_clk_div_rstn.
0	RW	0x1	ropll_ref_chopper_clk_div_rstn Chopper clk divider reset 1'b0: Reset 1'b1: Released

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HDPTXPHY_CMN_REG005E

Address: Operational Base(0x2B000000) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x1	ana_ropll_sdm_en PLL SDM enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	ovrd_ropll_sdm_rstn Override enable for ropll_sdm_rstn.
4	RW	0x0	ropll_sdm_rstn PLL SDM reset 1'b0: Reset 1'b1: Released
3	RW	0x1	ropll_sdc_fractional_en_rbr [rbr]Fractional clock divide in SDM clock generation 1'b0: Integer division 1'b1: Fractional division
2	RW	0x1	ropll_sdc_fractional_en_hbr [hbr]Fractional clock divide in SDM clock generation 1'b0: Integer division 1'b1: Fractional division
1	RW	0x1	ropll_sdc_fractional_en_hbr2 [hbr2] Fractional clock divide in SDM clock generation 1'b0: Integer division 1'b1: Fractional division
0	RW	0x1	ropll_sdc_fractional_en_hbr3 [hbr3] Fractional clock divide in SDM clock generation 1'b0: Integer division 1'b1: Fractional division

HDPTXPHY_CMN_REG0060

Address: Operational Base(0x2B000000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x4e	ropll_sdm_denominator_rbr [rbr] Denominator of SDM (Max. 255) Constraint: i_pll_sdm_lc > |signed i_pll_sdm_ki_pll_ssc_fm_deviationi_pll_ssc_fm_freq-14

HDPTXPHY_CMN_REG0063

Address: Operational Base(0x2B000000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x4e	ropll_sdm_denominator_hbr3 [hbr3] Denominator of SDM (Max. 255) Constraint: i_pll_sdm_lc > |signed i_pll_sdm_ki_pll_ssc_fm_deviation - i_pll_ssc_fm_freq-1|

HDPTXPHY_CMN_REG0064

Address: Operational Base(0x2B000000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3	RW	0x1	ropll_sdm_numerator_sign_rbr [rbr] Sign of SDM numerator 1'b0: Positive 1'b1: Negative
2	RW	0x1	ropll_sdm_numerator_sign_hbr [hbr]Sign of SDM numerator 1'b0: Positive 1'b1: Negative
1	RW	0x1	ropll_sdm_numerator_sign_hbr2 [hbr2] Sign of SDM numerator 1'b0: Positive 1'b1: Negative
0	RW	0x1	ropll_sdm_numerator_sign_hbr3 [hbr3] Sign of SDM numerator 1'b0: Positive 1'b1: Negative

HDPTXPHY_CMN_REG0065

Address: Operational Base(0x2B000000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x14	ropll_sdm_numerator_rbr [rbr] Numerator of SDM with i_pll_sdm_k_sign (-255~255).

HDPTXPHY_CMN_REG0069

Address: Operational Base(0x2B000000) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ana_ropll_sdm_ph_num_sel PLL PI input clock phase number 1'b0: 8-phase 1'b1: 4-phase
4:3	RW	0x0	ana_ropll_sdm_pi_step PLL phase interpolstor step 2'b00: 1-step (16-phase) 2'b01: 2-step (8-phase) 2'b1x: 0.5-step
2:0	RW	0x2	ropll_sdc_n_rbr [rbr] PLL SDC divide-ratio selection 3'b000: /3 3'b001: /4 3'b010: /5 3'b011: /6 3'b100: /7 3'b101: /8

HDPTXPHY_CMN_REG006C

Address: Operational Base(0x2B000000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x13	ropll_sdc_numerator_rbr [rbr] Numerator of SDC (Max 65)

HDPTXPHY_CMN_REG0070

Address: Operational Base(0x2B000000) + offset (0x01C0)

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Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x18	ropll_sdc_denominator_rbr [rbr] Denominator of SDC (Max 65)

HDPTXPHY_CMN_REG0074

Address: Operational Base(0x2B000000) + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ovrd_ropll_sdc_ndiv_rstn Override enable for ropll_sdc_ndiv_rstn
2	RW	0x1	ropll_sdc_ndiv_rstn ROPLL SDC ndiv reset
1	RW	0x0	ovrd_ropll_ssc_en Override enable for ropll_ssc_en
0	RW	0x1	ropll_ssc_en PLL SSC enable 1'b0: Disable 1'b1: Enable

HDPTXPHY_CMN_REG0081

Address: Operational Base(0x2B000000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_pll_cd_clk_en Override enable for pll_cd_clk_en
6	RW	0x0	pll_cd_clk_en CD enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	ovrd_pll_cd_tx_ser_rstn Override enable for pll_cd_tx_ser_rstn
4	RW	0x0	pll_cd_tx_ser_rstn TX_SER resetn
3	RW	0x0	ana_pll_cd_tx_ser_rate_sel NA
2	RW	0x0	ana_pll_cd_hsclk_inv CD output clock polarity inversion 1'b0: No swap 1'b1: P/N swap
1	RW	0x0	ana_pll_cd_hsclk_west_en CD driver nmos strength control N/A
0	RW	0x0	ana_pll_cd_hsclk_east_en CD driver pmos strength control N/A

HDPTXPHY_CMN_REG0082

Address: Operational Base(0x2B000000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_pll_cd_vreg_en Override enable for pll_cd_vreg_en
6	RW	0x0	pll_cd_vreg_en Controls Regulator Enable 1'b0: Disable regulator (Bypass VDD PMOS switch turns ON) 1'b1: Regulator Enable (Bypass path disables)

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Bit	Attr	Reset Value	Description
5	RW	0x0	ovrd_pll_cd_vreg_lpf_bypass Override enable for pll_cd_vreg_lpf_bypass
4	RW	0x0	pll_cd_vreg_lpf_bypass Controls Regulator input voltage reference noise reduction Low pass filter (BW <5MHz) 1'b0: Regulator reference Low pass filter Mode 1'b1: Bypass Low pass filter (Fast charging)
3:0	RW	0x0	ana_pll_cd_vreg_gain_ctrl Control regulator feedback gain--> <3>:No connect, <2:0>: Gain--> 3'b000: 1 3'b001: 1.03 3'b010: 1.035 3'b011: 1.043 3'b100: 1.059 3'b101: 1.094 3'b110: 1.118 3'b111: 1.155 Output regulator voltage: Gain*VDD

HDPTXPHY_CMN_REG0083

Address: Operational Base(0x2B000000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RW	0x1	ana_pll_cd_vreg_ictrl Regulator Opamp tail current control 2'b00: -25% 2'b01: Default 2'b10: +50% 2'b11: +100%
4	RW	0x0	ana_pll_cd_vreg_out_sel Force Bypass Regulator.Regulator and VDD is connected to Regulator node using pass gate 1'b0: Regulator mode 1'b1: Bypass
3	RW	0x0	ana_pll_cd_vreg_ref_sel Regulator Opamp Reference voltage selection 1'b0: VDD (as reference) 1'b1: VDDH Ladder as reference
2:0	RW	0x4	ana_pll_cd_vreg_ladder_sel Choose vref based on VDDH ladder tap points. For VDDH=1.8, Vref= 3'b000: 0.749 3'b001: 0.776 3'b010: 0.804 3'b011: 0.831 3'b100: 0.859 3'b101: 0.886 3'b110: 0.914 3'b111: 0.941

HDPTXPHY_CMN_REG0084

Address: Operational Base(0x2B000000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	ovrd_pll_lcro_clk_sel Override enable for pll_lcro_clk_sel
5	RW	0x0	pll_lcro_clk_sel Slects between LC vs RO PLL clock.
4	RW	0x0	ana_pll_bist_en Enables the BIST clock path in BIST mode.
3	RW	0x0	ana_pll_cd_bistclk_west_en Enables the BIST clock path twoards Lane2 and Lane 3
2	RW	0x0	ana_pll_cd_bistclk_east_en Enables the BIST clock path twoards Lane0 and Lane 1
1:0	RW	0x0	ana_pll_bist_clk_sel Selects BIST clock among 1, IB, Q and QB phases.

HDPTXPHY_CMN_REG0085

Address: Operational Base(0x2B000000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ovrd_pll_sync_loss_det_en Override enable for pll_sync_loss_det_en
4	RW	0x0	pll_sync_loss_det_en Enables the sync loss detection pulse generator.
3	RW	0x0	ovrd_pll_sync_loss_det_clk_en Override enable for pll_sync_loss_det_clk_en
2	RW	0x0	pll_sync_loss_det_clk_en Enables the clock for the sync loss detection pulse generator.
1:0	RW	0x2	ana_pll_sync_loss_det_mode Slects the sync loss detection mode from the followin table: 2'b00: 2UI pulse from div10 clock 2'b01: 4UI pulse from div10 clock 2'b10: 2UI pulse from div40 clock 2'b11: 4UI pulse from div40 clock

HDPTXPHY_CMN_REG0086

Address: Operational Base(0x2B000000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x1	ana_pll_pcg_postdiv_sel Same as output divider settings of the PLL
3:1	RW	0x0	ana_pll_pcg_clk_sel 3'b000: 8-bit color depth 3'b001: 10-bit color depth 3'b010: 12-bit color depth 3'b100: 16-bit color depth
0	RW	0x0	ana_pll_pcg_clk_en Enables the Pixel clock generator.

HDPTXPHY_CMN_REG0087

Address: Operational Base(0x2B000000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ana_pll_frl_mode_en FRL Mode enable = 1 for HDMI 2.1 mode
2	RW	0x0	ana_pll_tx_hs_clk_en Enables the DP mode symbol clock for PMA_D

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	ana_pll_atb_sel ATB select lines for CD.

HDPTXPHY_CMN_REG0089

Address: Operational Base(0x2B000000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ovrd_lcpll_fine_tune_start Override enable for lcpll_fine_tune_start
4	RW	0x0	lcpll_fine_tune_start LCPLL fine tune start override value
3	RW	0x0	ovrd_ropll_fine_tune_start Override enable for ropll_fine_tune_start
2	RW	0x0	ropll_fine_tune_start ROPLL fine tune start override value
1	RW	0x0	cmn_lcpll_alone_mode LCPLL alone mode.
0	RW	0x0	cmn_timer_sel CMN timer selection

HDPTXPHY_CMN_REG0095

Address: Operational Base(0x2B000000) + offset (0x0254)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:2	RW	0x0	lane_mux_sel_dp TX Lane LC/RO Clock Select Bit 0: Lane 0, ... , Bit3: Lane 3
1:0	RW	0x0	dp_tx_link_bw 2'b00: Picks PLL setting from RBR register set 2'b01: Picks PLL setting from HBR register set 2'b10: Picks PLL setting from HBR2 register set 2'b11: Picks PLL setting from HBR3 register set

HDPTXPHY_CMN_REG0097

Address: Operational Base(0x2B000000) + offset (0x025C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:2	RW	0x00	aux_dtb_out_en Used to select one of the DTB signals from lane CMN and SB module to drive sbp and sbn line at top
1	RW	0x0	dig_clk_sel 1'b1: Selects the LCPLL output reference clock for refence clock of PMA digital and o_dig_ref_clk 1'b0: Selects the ROPLL output reference clock for refence clock of PMA digital and o_dig_ref_clk
0	RW	0x0	hs_clk_mask_en Unused

HDPTXPHY_CMN_REG0099

Address: Operational Base(0x2B000000) + offset (0x0264)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	ssc_en Synchronize SSC enable Bit 0: LCPLL SSC Enable Bit 1: ROPLL SSC Enable
5:3	RW	0x0	vcoclk_mon_sel Tx monitor clock select 3'b000: clk/4 3'b001: clk/2 3'b100: Lane 0 read pointer clk 3'b101: Lane 1 read pointer clk 3'b110: Lane 2 read pointer clk 3'b111: Lane 3 read pointer clk
2	RW	0x0	cmn_ropll_alone_mode 1'b0: Cascaded PLL operation 1'b1: ROPLL alone operation
1:0	RW	0x0	ovrd_pcs_rate Override enable for pcs_rate

HDPTXPHY_CMN_REG009A

Address: Operational Base(0x2B000000) + offset (0x0268)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	pcs_rate Not used.
5	RW	0x0	bypass_sync_loss_det Bypass sync loss detection
4:2	RW	0x0	tg_sync_loss_mon_time Programmable delay for sync
1	RW	0x0	mon_afc_code_sel Monitor AFC code
0	RW	0x0	hs_speed_sel Tx high speed clock speed select 1'b0: Scan Tx clock / 2 1'b1: Scan Tx clock

HDPTXPHY_CMN_REG009B

Address: Operational Base(0x2B000000) + offset (0x026C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ls_speed_sel Link symbol clock select 1'b0: Link symbol clock /2 1'b1: Link symbol clock
3	RW	0x0	phy_ready Indicates the PHY is ready for transmission
2	RW	0x0	phy_clk_ready Indicates the PHY output clocks are stable
1	RW	0x0	aux_tx_data_inv Inverts auxiliary transmission data when set to 1
0	RW	0x0	aux_rx_data_inv Inverts auxiliary reception data when set to 1

HDPTXPHY_CMN_REG009E

Address: Operational Base(0x2B000000) + offset (0x0278)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:2	RW	0x00	cmn_dtb_digout_sel Select one of the digout in CMN module
1	RW	0x0	ovrd_pcs_bgr_en Override enable for pcs_bgr_en RW
0	RW	0x0	pcs_bgr_en Enable Bandgap reference.

HDPTXPHY_CMN_REG009F

Address: Operational Base(0x2B000000) + offset (0x027C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_pcs_bias_en Override enable for pcs_bias_en
6	RW	0x0	pcs_bias_en Enable biases.
5	RW	0x0	ovrd_pcs_cmn_rstn Override enable for pcs_cmn_rstn
4	RW	0x0	pcs_cmn_rstn Reset for common logics
3	RW	0x0	ovrd_pcs_init_rstn Override enable for pcs_init_rstn
2	RW	0x0	pcs_init_rstn Initial POR reset
1	RW	0x0	ovrd_pcs_lane_rstn Override enable for pcs_lane_rstn
0	RW	0x0	pcs_lane_rstn Lane reset

HDPTXPHY_CMN_REG00A0

Address: Operational Base(0x2B000000) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ovrd_pcs_pll_en Override enable for pcs_pll_en
5	RW	0x0	pcs_pll_en Enable PLL.
4:2	RW	0x0	pcs_ref_freq_sel Reference clock selection 2'b00: Ref clk from XO 2'b01: Ref clk from IO 2'b10: Ref clk from Pixel clk in 2'b11: Ref clk from Sys pll
1	RW	0x0	ovrd_pcs_dp_pll_lock_done Override enable for pcs_dp_pll_lock_done
0	RW	0x0	pcs_dp_pll_lock_done PLL lock completion indicator

HDPTXPHY_SB_REG0102

Address: Operational Base(0x2B000000) + offset (0x0408)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	ana_sb_mon_tx_ref_clk_sel Not used for HDPTX

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Bit	Attr	Reset Value	Description
5	RW	0x0	ovrd_sb_rxterm_en Override enable for sb_rxterm_en
4	RW	0x0	sb_rxterm_en Enable rx termination or source termination; this should go high after bias enable and calibration sequence in functional protocols.
3:0	RW	0x3	ana_sb_rxterm_offsp For i_sb_rescal_tune<2:0> = 3, the table for both Offset P and N looks like 4'b0000: 50 Ohms 4'b0001: 48.4 Ohms 4'b0011: 46.9 Ohms 4'b0111: 45.5 Ohms 4'b1111: 44.2 Ohms

HDPTXPHY_SB_REG0103

Address: Operational Base(0x2B000000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:3	RW	0x3	ana_sb_rxterm_offsn For i_sb_rescal_tune<2:0> = 3, the table for both Offset P and N looks like 4'b0000: 50 Ohms 4'b0001: 48.4 Ohms 4'b0011: 46.9 Ohms 4'b0111: 45.5 Ohms 4'b1111: 44.2 Ohms
2	RW	0x0	ana_sb_rx_term_gnd_en External reference clock I/O termination to ground 1'b0: Disable termination to GND 1'b1: Enable termination to GND
1	RW	0x0	ovrd_sb_rx_rescal_done Override enable for sb_rx_rescal_done
0	RW	0x0	sb_rx_rescal_done Not used for HDPTX

HDPTXPHY_SB_REG0104

Address: Operational Base(0x2B000000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_sb_rx_rescal_en Override enable for sb_rx_rescal_en
6	RW	0x0	sb_rx_rescal_en Not used for HDPTX
5	RW	0x0	ovrd_sb_en Override enable for sb_en
4	RW	0x0	sb_en Enables the common bias block for side band. This needs to be enabled only after BG_OK.
3	RW	0x0	ovrd_sb_arc_en Override enable for sb_arc_en
2	RW	0x0	sb_arc_en ARC Enable
1	RW	0x0	ovrd_sb_aux_en Override enable for sb_aux_en

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Bit	Attr	Reset Value	Description
0	RW	0x0	sb_aux_en AUX Enable 1'b0: Disable 1'b1: Enable

HDPTXPHY_SB_REG0105

Address: Operational Base(0x2B000000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ovrd_sb_earc_cmdc_en Override enable for sb_earc_cmdc_en
5	RW	0x0	sb_earc_cmdc_en External reference clock I/O AC-coupling capacitor bypass enable 1'b0: Use AC coupling cap 1'b1: Bypass AC coupling cap
4	RW	0x0	ovrd_sb_earc_cmtx_en Override enable for sb_earc_cmtx_en
3	RW	0x0	sb_earc_cmtx_en Enables the voltage buffers for slewing rate controlled transmission.
2:0	RW	0x0	ana_sb_tx_hlvl_prog This controls the voltage buffer in/out high value. 3'b000: 480mV 3'b001: 490mV 3'b010: 515mV 3'b011: 535mV 3'b100: 560mV 3'b101: 580mV 3'b110: 600mV 3'b111: 623mV

HDPTXPHY_SB_REG0106

Address: Operational Base(0x2B000000) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	ana_sb_tx_llvl_prog This controls the voltage buffer in/out low value. 3'b000: 320mV 3'b001: 310mV 3'b010: 285mV 3'b011: 260mV 3'b100: 240mV 3'b101: 220mV 3'b110: 200mV 3'b111: 180mV

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	ana_sb_tx_bias_ctrl <1:0> controls the slew Rate and <3:2> controls output stage current of buffer. Slew rate current 2'b00: (75uA) 2'b01: (100uA) 2'b10: (150uA) 2'b11: (200uA) Output stage current 2'b00: 8.0mA 2'b01: 4.0mA 2'b10: 4.0mA 2'b11: 2.0mA

HDPTXPHY_SB_REG0109

Address: Operational Base(0x2B000000) + offset (0x0424)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	ana_sb_rx_vcm_n_ctrl SB RX VCM control
5	RW	0x0	ana_sb_aux_rx_vcm_sel Not used for HDPTX
4	RW	0x0	ovrd_sb_earc_dmrx_afc_done Override enable for sb_earc_dmrx_afc_done
3	RW	0x0	sb_earc_dmrx_afc_done After AFC calibration of PWM sampling oscillator this signal goes high. Using this AFC related signals are shut down.
2:0	RW	0x0	ana_sb_dmrx_afc_div_ratio This controls the post division after oscillator. 0, 6 and 7 are not valid codes. 3'b001: divide by 16 3'b010: divide by 8 3'b011: divide by 4 3'b100: divide by 2 3'b101: divide by 1 (default)

HDPTXPHY_SB_REG010D

Address: Operational Base(0x2B000000) + offset (0x0434)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ana_sb_dmrx_lpbk_en This enables the loopback path for PWM detector; it bypasses the sampler.
4	RW	0x0	ana_sb_dmrx_lpbk_data The loopback data from register; the duty cycle of the data has to be more than 53% or less than 47%.
3:2	RW	0x0	ana_sb_dmrx_ref_prog SB DMRX reference programming
1:0	RW	0x0	ana_sb_dmrx_hyst_prog SB DMRX hysteresis programming

HDPTXPHY_SB_REG010F

Address: Operational Base(0x2B000000) + offset (0x043C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	ovrd_sb_vreg_en Override enable for sb_vreg_en
6	RW	0x0	sb_vreg_en Enables Regulator for PWM Detector.
5	RW	0x0	ovrd_sb_vreg_lpf_bypass Override enable for sb_vreg_lpf_bypass
4	RW	0x0	sb_vreg_lpf_bypass Bypasses the LPF during LDO bring up
3:0	RW	0x1	ana_sb_vreg_gain_ctrl Controls the feedback gain of the LDO. 4'b0000: 1.00 4'b0001: 1.03 4'b0010: 1.04 4'b0011: 1.05 4'b0100: 1.06 4'b0101: 1.09 4'b0110: 1.12 4'b0111: 1.15

HDPTXPHY_SB_REG0110

Address: Operational Base(0x2B000000) + offset (0x0440)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RW	0x0	ana_sb_vreg_ictrl Controls the error amplifier tail current 0: 250uA 1: 500uA 2: 750uA 3: 1.00mA RW 0x0 4:2 ana_sb_vreg_ladder_sel Controls the regulated
4:2	RW	0x0	ana_sb_vreg_ladder_sel Controls the regulated output voltage. 3'b000: 700mV 3'b001: 725mV 3'b010: 750mV 3'b011: 775mV 3'b100: 800mV 3'b101: 825mV 3'b110: 850mV 3'b111: 875mV
1	RW	0x0	ana_sb_vreg_out_sel It bypasses the LDO with VDD.
0	RW	0x0	ana_sb_vreg_ref_sel Used as power saving mode.

HDPTXPHY_SB_REG0113

Address: Operational Base(0x2B000000) + offset (0x044C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	sb_rx_rcal_opt_code This is use to select finale rcal code after rcal enable goes low and rcal done goes high 2'b00: o_rcal_code = tune_code 2'b01: o_rcal_code = i_sfr_rcal_code 2'b10: o_rcal_code = tune_code + i_sfr_rcal_code(i_sfr_sb_rx_rterm_ctrl) 2'b11: o_rcal_code = tune_code - i_sfr_rcal_code(i_sfr_sb_rx_rterm_ctrl)
3:0	RW	0x0	sb_rx_rterm_ctrl This is the code to be added in the tune code to generate finale rcal code depends on the value of i_sfr_sb_rx_rcal_opt_code

HDPTXPHY_SB_REG0114

Address: Operational Base(0x2B000000) + offset (0x0450)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

5:3	RW	0x0	sb_tg_sb_en_delay_time
			This sfr is the select line to set count wrt refclock cycle to set sb enable after rcal done goes high
			3'b000: delay_time = 9'd0; // 0
			3'b001: delay_time = 9'd13; // 0.5us for 25MHz refclk
			3'b010: delay_time = 9'd25; // 1us for 25MHz refclk
			3'b011: delay_time = 9'd50; // 2us for 25MHz refclk
			3'b100: delay_time = 9'd75; // 3us for 25MHz refclk
			3'b101: delay_time = 9'd125; // 5us for 25MHz refclk
			3'b110: delay_time = 9'd250; // 10us for 25MHz refclk
			3'b111: delay_time = 9'd500; // 20us for 25MHz refclk
			default: delay_time = 9'd25; // 1us for 25MHz refclk

2:0	RW	0x0	sb_tg_rxterm_en_delay_time
			This sfr is the select line to set count wrt refclock cycle to set sb rxterm enable signal after sb en goes high
			3'b000: delay_time = 9'd0; // 0
			3'b001: delay_time = 9'd13; // 0.5us for 25MHz refclk
			3'b010: delay_time = 9'd25; // 1us for 25MHz refclk
			3'b011: delay_time = 9'd50; // 2us for 25MHz refclk
			3'b100: delay_time = 9'd75; // 3us for 25MHz refclk
			3'b101: delay_time = 9'd125; // 5us for 25MHz refclk
			3'b110: delay_time = 9'd250; // 10us for 25MHz refclk
			3'b111: delay_time = 9'd500; // 20us for 25MHz refclk
			default: delay_time = 9'd25; // 1us for 25MHz refclk

HDPTXPHY_SB_REG0115

Address: Operational Base(0x2B000000) + offset (0x0454)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description

5:3	RW	0x0	sb_ready_delay_time
			This sfr is the select line to set count count wrt refclock cycle to set sb ready signal after all calibration completed
			3'b000: delay_time = 9'd0; // 0
			3'b001: delay_time = 9'd13; // 0.5us for 25MHz refclk
			3'b010: delay_time = 9'd25; // 1us for 25MHz refclk
			3'b011: delay_time = 9'd50; // 2us for 25MHz refclk
			3'b100: delay_time = 9'd75; // 3us for 25MHz refclk
			3'b101: delay_time = 9'd125; // 5us for 25MHz refclk
			3'b110: delay_time = 9'd250; // 10us for 25MHz refclk
			3'b111: delay_time = 9'd500; // 20us for 25MHz refclk
			default: delay_time = 9'd25; // 1us for 25MHz refclk

2:0	RW	0x0	sb_tg_osc_en_delay_time
			This sfr is the select line to set count count wrt refclock cycle to set oscillator enable after vreg sequence completed
			3'b000: delay_time = 9'd0; // 0
			3'b001: delay_time = 9'd13; // 0.5us for 25MHz refclk
			3'b010: delay_time = 9'd25; // 1us for 25MHz refclk
			3'b011: delay_time = 9'd50; // 2us for 25MHz refclk
			3'b100: delay_time = 9'd75; // 3us for 25MHz refclk
			3'b101: delay_time = 9'd125; // 5us for 25MHz refclk
			3'b110: delay_time = 9'd250; // 10us for 25MHz refclk
			3'b111: delay_time = 9'd500; // 20us for 25MHz refclk
			default: delay_time = 9'd25; // 1us for 25MHz refclk

HDPTXPHY_SB_REG0116

Address: Operational Base(0x2B000000) + offset (0x0458)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

6:4	RW	0x0	sb_tg_osc_en_to_afc_rstn_delay_time
			This sfr is the select line to set count wrt refclock cycle to release reset to afc calibration module after oscillator osc enable signal set.
			3'b000: delay_time = 9'd0; // 0
			3'b001: delay_time = 9'd13; // 0.5us for 25MHz refclk
			3'b010: delay_time = 9'd25; // 1us for 25MHz refclk
			3'b011: delay_time = 9'd50; // 2us for 25MHz refclk
			3'b100: delay_time = 9'd75; // 3us for 25MHz refclk
			3'b101: delay_time = 9'd125; // 5us for 25MHz refclk
			3'b110: delay_time = 9'd250; // 10us for 25MHz refclk
			3'b111: delay_time = 9'd500; // 20us for 25MHz refclk
			default: delay_time = 9'd25; // 1us for 25MHz refclk

3:2	RW	0x0	sb_pwm_start_code
			This is the sfr select line to set initial pwm code to start pwm calibration
			2'b00: pwm_start_code = 5'b0_1111; //-15
			2'b01: pwm_start_code = 5'b0_1010; //-10
			2'b10: pwm_start_code = 5'b0_0101; //-5
			2'b11: pwm_start_code = 5'b0_0000; // 0
			default: pwm_start_code = 5'b0_1111; //-15

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	sb_oc_settle_time This is the count which is use to select refclock cycle count to settle comparator output for latest calibration code 2'b00: settle_time = 5'd6 ; 2'b01: settle_time = 5'd12; 2'b10: settle_time = 5'd18; 2'b11: settle_time = 5'd24; default: settle_time = 5'd6 ;

HDPTXPHY_SB_REG0117

Address: Operational Base(0x2B000000) + offset (0x045C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	sb_oc_num_of_sample This is use to select number of times oc comparator output to be sampled for applied cal code to make sure cal code matches reuired specifiction 2'b00: sample_cnt = 4'd2 ; 2'b01: sample_cnt = 4'd6 ; 2'b10: sample_cnt = 4'd10; 2'b11: sample_cnt = 4'd14; default: sample_cnt = 4'd2 ;
5	RW	0x0	sb_oc_en This sfr enable offset calibration
4	RW	0x0	sb_oc_bypass_pwm Bypass enable for PWM

3:0	RW	0x0	sb_tg_pll_cd_vreg_fast_pulse_time
			This sfr is the select line to set number of clock cycle for which vreg bypass signal go high
			4'b0000: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd25;//1us
			4'b0001: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd50;//2us
			4'b0010: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd75;//3us
			4'b0011: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd100;//4us
			4'b0100: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd125;//5us
			4'b0101: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd250;//10us
			4'b0110: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd500;//20us
			4'b0111: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd750;//30us
			4'b1000: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd1000;//40us
			4'b1001: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd1250;//50us
			4'b1010: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd2500;//100us
			4'b1011: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd3750;//150us
			4'b1100: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd5000;//200us
			4'b1101: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd7500;//300us
			4'b1110: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd10000;//400us
			4'b1111: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd12500;//500us
			default: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd250;

HDPTXPHY_SB_REG0118

Address: Operational Base(0x2B000000) + offset (0x0460)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	sb_tg_earc_dmrx_recvrd_clk_cnt This is the target count the rec clk should give for specifide refclock cycle This count should be 10, 20 or 40 (i_sfr_sb_tg_cnt_run_no * reference clock cycle period) <= (i_sfr_sb_tg_earc_dmrx_recvrd_clk_cnt* recover clock period)

HDPTXPHY_SB_REG0119

Address: Operational Base(0x2B000000) + offset (0x0464)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	sb_tg_cnt_run_no__9_8 This is the refclock count cycle during which rec clock counter run. This count should be such that time duration with refclock good enough to get requird rec clock count (i_sfr_sb_tg_cnt_run_no * reference clock cycle period) <= (i_sfr_sb_tg_earc_dmrx_recvrd_clk_cnt* recover clock period)

HDPTXPHY_SB_REG011A

Address: Operational Base(0x2B000000) + offset (0x0468)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	sb_tg_cnt_run_no__7_0 This is the refclock count cycle during which rec clock counter run This count should be such that time duration with refclock good enough to get requird rec clock count (i_sfr_sb_tg_cnt_run_no * reference clock cycle period) <= (i_sfr_sb_tg_earc_dmrx_recvrd_clk_cnt* recover clock period)

HDPTXPHY_SB_REG011B

Address: Operational Base(0x2B000000) + offset (0x046C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	sb_earc_sig_det_bypass This sfr use to bypass signal detect logic
3:0	RW	0x0	sb_afc_tol OSC stable tolerance. This is the tolarance for vco count that can be taken to make sure vco generating stable frequency

HDPTXPHY_SB_REG011C

Address: Operational Base(0x2B000000) + offset (0x0470)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	sb_afc_stb_num OSC stable number for initial time. it use to configure number of time vco generate stable count to go for stable frequency comparison state

HDPTXPHY_SB_REG011D

Address: Operational Base(0x2B000000) + offset (0x0474)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	sb_tg_osc_cnt_min This is the minimum target count from vco to be received for one ref clock cycle to to get 2.5GHz pll clock. Refclock: count required 24MHz: 103 25MHz: 99 26MHz: 95 27MHz: 92 45MHz: 55 54MHz: 46

HDPTXPHY_SB_REG011E

Address: Operational Base(0x2B000000) + offset (0x0478)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	sb_tg_osc_cnt_max This is the maximum target count from vco to be received for one ref clock cycle to to get 2.5GHz pll clock. Refclock : count required 24MHz: 106 25MHz: 101 26MHz: 98 27MHz: 94 45MHz: 57 54MHz: 48

HDPTXPHY_SB_REG011F

Address: Operational Base(0x2B000000) + offset (0x047C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	sb_pwm_afc_ctrl This is the sfr which use for selecting pwm afc calibration code depending on its MSB MSB = 1 then MSB from -1 to 0 bit value taken as calibration code for pwm afc MSB = 0 then afc code is internally generated from afc module logic if AFC _EN =1
5:2	RO	0x0	reserved
1	RW	0x0	sb_rcal_rstn Sideband resister calibration enable signal 1'b0: Resister calibration disable 1'b1: Resister calibration enable
0	RW	0x0	sb_arc_en_in Sideband arc enable signal 1'b0: ARC disable 1'b1: ARC enable

HDPTXPHY_SB_REG0120

Address: Operational Base(0x2B000000) + offset (0x0480)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	sb_aux_en_in Sideband aux enable signal 1'b0: AUX disable 1'b1: AUX enable
6	RW	0x0	sb_rx_term_sel Sideband rx term sel 1'b1: Code taken from lane rcal 1'b0: Code taken from rcal module in sideband
5:4	RW	0x0	sb_rcal_term_sel Not used
3:2	RW	0x0	sb_rcal_lane_sel Select rcal code to sideband from lane 0,1,2,3. 2'b00: Lane0 code to sideband from lane 2'b01: Lane1 code to sideband from lane 2'b10: Lane2 code to sideband from lane 2'b11: Lane3 code to sideband from lane
1	RW	0x0	sb_eARC_en Enable eARC mode for HDMI
0	RW	0x0	sb_eARC_afc_en 1'b0: AFC disable 1'b1: AFC enable

HDPTXPHY_SB_REG0123

Address: Operational Base(0x2B000000) + offset (0x048C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_sb_earc_rx_mode Override enable for sb_earc_rx_mode
6	RW	0x0	sb_earc_rx_mode PHY input to eARC in cmrx mode
5	RW	0x0	ovrd_sb_ready Override enable for sb_ready
4	RW	0x0	sb_ready Showing sideband ready signal to analog
3	RW	0x0	ovrd_sb_sig_det_done Override enable for sb_sig_det_done
2	RW	0x0	sb_sig_det_done Show signal detect done in dmac rx mode
1	RW	0x0	ovrd_sb_earc_dmac_en Override enable for sb_earc_dmac_en
0	RW	0x0	sb_earc_dmac_en Input enabling from digital module for signal detect module

HDPTXPHY_INTOP_REG0200

Address: Operational Base(0x2B000000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RW	0x0	dck_master_lane Select master read pointer clock source 2'b00: Lane 0 2'b01: Lane 1 2'b10: Lane 2 2'b11: Lane 3

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Bit	Attr	Reset Value	Description
4:3	RW	0x0	master_lane_sel TX control interface of one source lane is driven to all lanes in align mode. Sources - 2'b00: Lane 0 2'b01: Lane 1 2'b10: Lane 2 2'b11: Lane 3
2	RW	0x0	protocol_sel Mux select on input data to data path CTS pattern generator gives 20 bit which the data path converts to 40 bits. In all other cases, input data connects to data path
1	RW	0x0	hdmi_tmds_frl_sel Mux selects on input data to data path In HDMI TMDS mode, one of the lanes needs to generate clock which is achieved using SFR clock user pattern. In all other cases, input data connects to data path
0	RW	0x0	cts_mode Transmits 20-bit CTS data when set to 1

HDPTXPHY_INTOP_REG0201

Address: Operational Base(0x2B000000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	clk_user_pat__39_32 40-bit clock signal generated for HDMI TMDS mode

HDPTXPHY_INTOP_REG0203

Address: Operational Base(0x2B000000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	clk_user_pat__23_16 40-bit clock signal generated for HDMI TMDS mode

HDPTXPHY_INTOP_REG0204

Address: Operational Base(0x2B000000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	clk_user_pat__15_8 40-bit clock signal generated for HDMI TMDS mode

HDPTXPHY_INTOP_REG0205

Address: Operational Base(0x2B000000) + offset (0x0814)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	clk_user_pat__7_0 40-bit clock signal generated for HDMI TMDS mode

HDPTXPHY_INTOP_REG0206

Address: Operational Base(0x2B000000) + offset (0x0818)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ctrl_align_mode TX control interface mux based on master lane selection is valid only if ctrl_align_mode is set to 1

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Bit	Attr	Reset Value	Description
6:5	RW	0x0	deskew_ptr_master_lane_sel Deskew pointer control based on master lane
4:3	RW	0x0	lane_swap_sel Selects one of four lane swap combinations (xx: o/p lane - i/p lane) 2'b00: 0 - 0, 1 - 1, 2 - 2, 3 - 3 2'b01: 0 - 1, 1 - 0, 2 - 2, 3 - 3 2'b10: 0 - 0, 1 -1 , 2 - 3, 3 - 2 2'b11: 0 - 3, 1 - 2, 2 - 1, 3 - 0
2:1	RW	0x0	data_bus_width Used for data bus width conversion 1'b0: Converts the 20-bit data in 20b clock domain to 40-bit data in tbc domain 1'b1: Conversion happends based on CTS mode value
0	RW	0x0	bus_width_sel 1'b1: Sets 36/40 bits data bus operation 1'b0: Sets 18/20 bits data bus operation

HDPTXPHY_INTOP_REG0207

Address: Operational Base(0x2B000000) + offset (0x081C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	lane_en Lane enabling for sync pulse and sync loss signals

HDPTXPHY_LANE_REG0303

Address: Operational Base(0x2B000000) + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln0_ana_tx_drv_eien_fb_en tx common mode feedback when eien is enable 1'b0: Disable 1'b1: Enable (feedback is enable)
5	RW	0x0	ovrd_ln0_tx_drv_lvl_ctrl Override enable for ln0_tx_drv_lvl_ctrl
4:0	RW	0x00	ln0_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap-level (max swing) ... 5'b00000: min main-tap-level (min swing) Others: N/A

HDPTXPHY_LANE_REG0307

Address: Operational Base(0x2B000000) + offset (0x0C1C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln0_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b0: Polarity change, data P/N is switched (deenhancement) 1'b1: Polarity non-change(enhancement)
5:3	RW	0x0	ln0_ana_tx_drv_accdrv_ctrl TX edge-enhancement AC coupled driver strength control 3'b000: No enhancement ... 3'b111: Max enhancement

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Bit	Attr	Reset Value	Description
2	RW	0x0	ln0_ana_tx_drv_hsclk_mon_en Enable of high-speed clock monitor through Tx driver 1'b0: Disable 1'b1: Enable
1	RW	0x0	ln0_ana_tx_d ln0_ana_tx_drv_pll_ref_mon_en Enable of PLL reference clock monitor through Tx driver 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln0_ana_tx_drv_pll_ref_mon_sel Select PLL reference clock monitor through Tx driver 1'b0: LCPLL 1'b1: ROPLL (MPHY do not need this pin, always LCPLL)

HDPTXPHY_LANE_REG030A

Address: Operational Base(0x2B000000) + offset (0x0C28)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ln0_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x0	ln0_tx_jeq_even_ctrl_rbr [rbr] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG030B

Address: Operational Base(0x2B000000) + offset (0x0C2C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	ln0_tx_jeq_even_ctrl_hbr [hbr]TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on
3:0	RW	0x0	ln0_tx_jeq_even_ctrl_hbr2 [hbr2] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG030C

Address: Operational Base(0x2B000000) + offset (0x0C30)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	ln0_tx_jeq_even_ctrl_hbr3 [hbr3] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on
3:0	RW	0x0	ln0_tx_jeq_odd_ctrl_rbr [rbr] TX jitter EQ driver (odd) strength control same as even control

HDPTXPHY_LANE_REG030D

Address: Operational Base(0x2B000000) + offset (0x0C34)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ln0_tx_jeq_odd_ctrl_hbr [hbr]TX jitter EQ driver (odd) strength control same as even control
3:0	RW	0x0	ln0_tx_jeq_odd_ctrl_hbr2 [hbr2] TX jitter EQ driver (odd) strength control same as even control

HDPTXPHY_LANE_REG030E

Address: Operational Base(0x2B000000) + offset (0x0C38)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:3	RW	0x0	ln0_tx_jeq_odd_ctrl_hbr3 [hbr3] TX jitter EQ driver (odd) strength control same as even control
2	RW	0x0	ovrd_ln0_tx_rcal_en Override enable for ln0_tx_rcal_en
1	RW	0x0	ln0_tx_rcal_en TX RCAL enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln0_ana_tx_rterm_42p5_en TX 42.5 ohms termination enable 1'b0: Disable (50 ohm) 1'b1: Enable (42.5 ohm)

HDPTXPHY_LANE_REG030F

Address: Operational Base(0x2B000000) + offset (0x0C3C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	ovrd_ln0_tx_rxd_comp_en Override enable for ln0_tx_rxd_comp_en
6	RW	0x0	ln0_tx_rxd_comp_en TX receiver detector comparator enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	ovrd_ln0_tx_rxd_en Override enable for ln0_tx_rxd_en
4	RW	0x0	ln0_tx_rxd_en TX receiver detector enable. Drives a transition on the serial data and measures the charge time of the line in order to determine whether a receiver is connected. 1'b0: normal operation 1'b1: initiate a receiver detect sequence
3	RW	0x0	ln0_ana_tx_rxd_comp_i_ctrl TX receiver detector comparator bias control 1'b0: 1x 1'b1: 3x
2	RW	0x0	ln0_ana_tx_bist_en Enables BIST for serial nodes.
1:0	RW	0x0	ln0_ana_tx_bist_clkdel_prog Phase shifting delay in BIST clock path.

HDPTXPHY_LANE_REG0310

Address: Operational Base(0x2B000000) + offset (0x0C40)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:2	RW	0x00	ln0_ana_tx_bist_mode This defines the BIST paths and modes as follows: <0> enables the serializer data output. <1> flips the serializer data output <3:2> defines the line sampling input 2'b00: txp-txn 2'b01: txn-vdd/2 2'b10: txp-vdd/2 2'b11: off <4> inverts the byte clock <5> enables the SA bist clock in LANE CD
1:0	RW	0x2	ln0_ana_tx_sync_loss_det_mode Selects the sync loss detection mode from the following table: 2'b00: 2UI pulse from div10 clock 2'b01: 4UI pulse from div10 clock 2'b10: 2UI pulse from div40 clock 2'b11: 4UI pulse from div40 clock

HDPTXPHY_LANE_REG0311

Address: Operational Base(0x2B000000) + offset (0x0C44)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln0_tx_sync_pulse_det_clk_en Override enable for ln0_tx_sync_pulse_det_clk_en
6	RW	0x0	ln0_tx_sync_pulse_det_clk_en Enables the clock path for sync loss detector.
5	RW	0x0	ovrd_ln0_tx_sync_pulse_det_en Override enable for ln0_tx_sync_pulse_det_en

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Bit	Attr	Reset Value	Description
4	RW	0x0	ln0_tx_sync_pulse_det_en Enables the sync loss detector
3	RW	0x0	ln0_tx_ser_40bit_en_rbr [rbr] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
2	RW	0x0	ln0_tx_ser_40bit_en_hbr [hbr]TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
1	RW	0x0	ln0_tx_ser_40bit_en_hbr2 [hbr2] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
0	RW	0x0	ln0_tx_ser_40bit_en_hbr3 [hbr3] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit

HDPTXPHY_LANE_REG0312

Address: Operational Base(0x2B000000) + offset (0x0C48)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln0_tx_ser_data_rstn Override enable for ln0_tx_ser_data_rstn
6	RW	0x0	ln0_tx_ser_data_rstn TX serializer data-path resetn 1'b0: Reset 1'b1: Released
5	RW	0x0	ln0_tx_ser_rate_sel_rbr [rbr] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
4	RW	0x0	ln0_tx_ser_rate_sel_hbr [hbr]TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
3	RW	0x0	ln0_tx_ser_rate_sel_hbr2 [hbr2] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
2	RW	0x0	ln0_tx_ser_rate_sel_hbr3 [hbr3] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
1	RW	0x0	ovrd_ln0_tx_ser_clk_rstn Override enable for ln0_tx_ser_clk_rstn
0	RW	0x0	ln0_tx_ser_clk_rstn TX serializer clock-path resetn 1'b0: Reset 1'b1: Released

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HDPTXPHY_LANE_REG0316

Address: Operational Base(0x2B000000) + offset (0x0C58)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	ln0_ana_tx_ser_vreg_gain_ctrl Control regulator feedback gain--> <3>: No connect, <2:0>: Gain--> 3'b000: 1 3'b001: 1.03 3'b010: 1.035 3'b011: 1.043 3'b100: 1.059 3'b101: 1.094 3'b110: 1.118 3'b111: 1.155 Output regulator voltage: Gain*VDD

HDPTXPHY_LANE_REG031B

Address: Operational Base(0x2B000000) + offset (0x0C6C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	ln0_ana_tx_reserved Reserved port

HDPTXPHY_LANE_REG031F

Address: Operational Base(0x2B000000) + offset (0x0C7C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ln0_rx_clk_inv 1'b1: Inverts the BIST recovered clock before feeding to PMA digital BIST RX path 1'b0: Passes the BIST recovered clock to PMA digital BIST RX path without inversion
4:2	RW	0x5	ln0_tg_rcal_rstn_delay_time Rx Rcal reset delay time after PLL AFC done 3'b000: 0 3'b001: 0.5us 3'b010: 1us 3'b011: 2us 3'b100: 3us 3'b101: 5us 3'b110: 10us 3'b111: 20us
1:0	RW	0x0	ln0_tg_tx_dcc_en_delay_time 2'b00: 3'd4 2'b01: 3'd5 2'b10: 3'd6 2'b11: 3'd7

HDPTXPHY_LANE_REG0320

Address: Operational Base(0x2B000000) + offset (0x0C80)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:5	RW	0x5	ln0_tg_ser_vreg_fast_pulse_time 3'b000: 1us 3'b001: 2us 3'b010: 3us 3'b011: 4us 3'b100: 5us 3'b101: 10us 3'b110: 20us 3'b111: 30us
4	RW	0x0	ln0_ovrd_txd_deskew_rstn Override enable for ln0_txd_deskew_rstn
3	RW	0x0	ln0_txd_deskew_rstn Active low reset for the lane data path
2	RW	0x0	ln0_txd_deskew_bypass_err_chk Counter relation check bypass
1	RW	0x0	ln0_txd_deskew_fix_da Fix the latch phase
0	RW	0x0	ln0_txd_deskew_fix_db Fix the latch phase

HDPTXPHY_LANE_REG0403

Address: Operational Base(0x2B000000) + offset (0x100C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln1_ana_tx_drv_eien_fb_en Tx common mode feedback when EIEN is enable 1'b0: Disable 1'b1: Enable (feedback is enable)
5	RW	0x0	ovrd_ln1_tx_drv_lvl_ctrl Override enable for ln1_tx_drv_lvl_ctrl
4:0	RW	0x00	ln1_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap-level (max swing) ... 5'b00000: min main-tap-level (min swing) Others: N/A

HDPTXPHY_LANE_REG0407

Address: Operational Base(0x2B000000) + offset (0x101C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln1_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b0: Polarity change, data P/N is switched (deenhancement) 1'b1: Polarity non-change(enhancement)
5:3	RW	0x0	ln1_ana_tx_drv_accdrv_ctrl TX edge-enhancement AC coupled driver strength control 3'b000: No enhancement ... 3'b111: Max enhancement
2	RW	0x0	ln1_ana_tx_drv_hsclk_mon_en Enable of high-speed clock monitor through Tx driver 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	ln1_ana_tx_drv_pll_ref_mon_en Enable of PLL reference clock monitor through Tx driver 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln1_ana_tx_drv_pll_ref_mon_sel Select PLL reference clock monitor through Tx driver 1'b0: LCPLL 1'b1: ROPLL (MPHY do not need this pin, always LCPLL)

HDPTXPHY_LANE_REG040A

Address: Operational Base(0x2B000000) + offset (0x1028)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ln1_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x0	ln1_tx_jeq_even_ctrl_rbr [rbr] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG040B

Address: Operational Base(0x2B000000) + offset (0x102C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	ln1_tx_jeq_even_ctrl_hbr [hbr]TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on
3:0	RW	0x0	ln1_tx_jeq_even_ctrl_hbr2 [hbr2] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG040C

Address: Operational Base(0x2B000000) + offset (0x1030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	ln1_tx_jeq_even_ctrl_hbr3 [hbr3] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on
3:0	RW	0x0	ln1_tx_jeq_odd_ctrl_rbr [rbr] TX jitter EQ driver (odd) strength control same as even control

HDPTXPHY_LANE_REG040D

Address: Operational Base(0x2B000000) + offset (0x1034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ln1_tx_jeq_odd_ctrl_hbr [hbr] TX jitter EQ driver (odd) strength control same as even control
3:0	RW	0x0	ln1_tx_jeq_odd_ctrl_hbr2 [hbr2] TX jitter EQ driver (odd) strength control same as even control

HDPTXPHY_LANE_REG040E

Address: Operational Base(0x2B000000) + offset (0x1038)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:3	RW	0x0	ln1_tx_jeq_odd_ctrl_hbr3 [hbr3] TX jitter EQ driver (odd) strength control same as even control
2	RW	0x0	ovrd_ln1_tx_rcal_en Override enable for ln1_tx_rcal_en
1	RW	0x0	ln1_tx_rcal_en TX RCAL enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln1_ana_tx_rterm_42p5_en TX 42.5 ohms termination enable 1'b0: Disable (50 ohm) 1'b1: Enable (42.5 ohm)

HDPTXPHY_LANE_REG0410

Address: Operational Base(0x2B000000) + offset (0x1040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:2	RW	0x00	ln1_ana_tx_bist_mode This defines the BIST paths and modes as follows: <0> enables the serializer data output. <1> flips the serializer data output <3:2> defines the line sampling input 2'b00: txp-txn 2'b01: txn-vdd/2 2'b10: txp-vdd/2 2'b11: off <4> inverts the byte clock <5> enables the SA bist clock in LANE CD
1:0	RW	0x2	ln1_ana_tx_sync_loss_det_mode Slects the sync loss detection mode from the followin table: 2'b00: 2UI pulse from div10 clock 2'b01: 4UI pulse from div10 clock 2'b10: 2UI pulse from div40 clock 2'b11: 4UI pulse from div40 clock

HDPTXPHY_LANE_REG0411

Address: Operational Base(0x2B000000) + offset (0x1044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln1_tx_sync_pulse_det_clk_en Override enable for ln1_tx_sync_pulse_det_clk_en
6	RW	0x0	ln1_tx_sync_pulse_det_clk_en Enables the clock path for sync loss detector.
5	RW	0x0	ovrd_ln1_tx_sync_pulse_det_en Override enable for ln1_tx_sync_pulse_det_en
4	RW	0x0	ln1_tx_sync_pulse_det_en Enables the sync loss detector.
3	RW	0x0	ln1_tx_ser_40bit_en_rbr [rbr] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
2	RW	0x0	ln1_tx_ser_40bit_en_hbr [hbr]TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
1	RW	0x0	ln1_tx_ser_40bit_en_hbr2 [hbr2] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
0	RW	0x0	ln1_tx_ser_40bit_en_hbr3 [hbr3] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit

HDPTXPHY_LANE_REG0412

Address: Operational Base(0x2B000000) + offset (0x1048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln1_tx_ser_data_rstn Override enable for ln1_tx_ser_data_rstn

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Bit	Attr	Reset Value	Description
6	RW	0x0	ln1_tx_ser_data_rstn TX serializer data-path resetn 1'b0: Reset 1'b1: Released
5	RW	0x0	ln1_tx_ser_rate_sel_rbr [rbr] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
4	RW	0x0	ln1_tx_ser_rate_sel_hbr [hbr]TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
3	RW	0x0	ln1_tx_ser_rate_sel_hbr2 [hbr2] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
2	RW	0x0	ln1_tx_ser_rate_sel_hbr3 [hbr3] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
1	RW	0x0	ovrd_ln1_tx_ser_clk_rstn Override enable for ln1_tx_ser_clk_rstn
0	RW	0x0	ln1_tx_ser_clk_rstn TX serializer clock-path resetn 1'b0: Reset 1'b1: Released

HDPTXPHY_LANE_REG0416

Address: Operational Base(0x2B000000) + offset (0x1058)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	ln1_ana_tx_ser_vreg_gain_ctrl Control regulator feedback gain--> <3>: No connect, <2:0>: Gain--> 3'b000: 1 3'b001: 1.03 3'b010: 1.035 3'b011: 1.043 3'b100: 1.059 3'b101: 1.094 3'b110: 1.118 3'b111: 1.155 Output regulator voltage: Gain*VDD

HDPTXPHY_LANE_REG041B

Address: Operational Base(0x2B000000) + offset (0x106C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	ln1_ana_tx_reserved Reserved port

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HDPTXPHY_LANE_REG041F

Address: Operational Base(0x2B000000) + offset (0x107C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ln1_rx_clk_inv 1'b1: Inverts the BIST recovered clock before feeding to PMA digital BIST RX path 1'b0: Passes the BIST recovered clock to PMA digital BIST RX path without inversion
4:2	RW	0x5	ln1_tg_rcal_rstn_delay_time Rx Rcal reset delay time after PLL AFC done 3'b000: 0 3'b001: 0.5us 3'b010: 1us 3'b011: 2us 3'b100: 3us 3'b101: 5us 3'b110: 10us 3'b111: 20us
1:0	RW	0x0	ln1_tg_tx_dcc_en_delay_time 2'b00: 3'd4 2'b01: 3'd5 2'b10: 3'd6 2'b11: 3'd7

HDPTXPHY_LANE_REG0503

Address: Operational Base(0x2B000000) + offset (0x140C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln2_ana_tx_drv_eien_fb_en Tx common mode feedback when eien is enable 1'b0: Disable 1'b1: Enable (feedback is enable)
5	RW	0x0	ovrd_ln2_tx_drv_lvl_ctrl Override enable for ln2_tx_drv_lvl_ctrl
4:0	RW	0x00	ln2_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap level(max swing) ... 5'b00000: min main-tap level(min swing) Others: N/A

HDPTXPHY_LANE_REG0507

Address: Operational Base(0x2B000000) + offset (0x141C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln2_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b0: Polarity change, data P/N is switched (deenhancement), 1'b1: Polarity non-change(enhancement)
5:3	RW	0x0	ln2_ana_tx_drv_accdrv_ctrl TX edge-enhancement AC coupled driver strength control 3'b000: No enhancement ... 3'b111: Max enhancement

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Bit	Attr	Reset Value	Description
2	RW	0x0	ln2_ana_tx_drv_hsclk_mon_en Enable of high-speed clock monitor through Tx driver 1'b0: Disable 1'b1: Enable
1	RW	0x0	ln2_ana_tx_drv_pll_ref_mon_en Enable of PLL reference clock monitor through Tx driver 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln2_ana_tx_drv_pll_ref_mon_sel Select PLL reference clock monitor through Tx driver 1'b0: LCPLL 1'b1: ROPLL (MPHY do not need this pin, always LCPLL)

HDPTXPHY_LANE_REG050A

Address: Operational Base(0x2B000000) + offset (0x1428)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ln2_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x0	ln2_tx_jeq_even_ctrl_rbr [rbr] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG050B

Address: Operational Base(0x2B000000) + offset (0x142C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	ln2_tx_jeq_even_ctrl_hbr [hbr] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on
3:0	RW	0x0	ln2_tx_jeq_even_ctrl_hbr2 [hbr2] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG050C

Address: Operational Base(0x2B000000) + offset (0x1430)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	ln2_tx_jeq_even_ctrl_hbr3 [hbr3] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on
3:0	RW	0x0	ln2_tx_jeq_odd_ctrl_rbr [rbr] TX jitter EQ driver (odd) strength control same as even control

HDPTXPHY_LANE_REG050D

Address: Operational Base(0x2B000000) + offset (0x1434)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ln2_tx_jeq_odd_ctrl_hbr [hbr] TX jitter EQ driver (odd) strength control same as even control
3:0	RW	0x0	ln2_tx_jeq_odd_ctrl_hbr2 [hbr2] TX jitter EQ driver (odd) strength control same as even control

HDPTXPHY_LANE_REG050E

Address: Operational Base(0x2B000000) + offset (0x1438)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:3	RW	0x0	ln2_tx_jeq_odd_ctrl_hbr3 [hbr3]TX jitter EQ driver (odd) strength control same as even control
2	RW	0x0	ovrd_ln2_tx_rcal_en Override enable for ln2_tx_rcal_en
1	RW	0x0	ln2_tx_rcal_en TX RCAL enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln2_ana_tx_rterm_42p5_en TX 42.5 ohm termination enable 1'b0: Disable(50 ohm) 1'b1: Enable (42.5 ohm)

HDPTXPHY_LANE_REG0510

Address: Operational Base(0x2B000000) + offset (0x1440)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:2	RW	0x00	ln2_ana_tx_bist_mode This defines the BIST paths and modes as follows: <0> enables the serializer data output. <1> flips the serializer data output <3:2> defines the line sampling input 2'b00: txp-txn 2'b01: txn-vdd/2 2'b10: txp-vdd/2 2'b11: off <4> inverts the byte clock <5> enables the SA bist clock in LANE CD
1:0	RW	0x2	ln2_ana_tx_sync_loss_det_mode Selects the sync loss detection mode from the following table: 2'b00: 2UI pulse from div10 clock 2'b01: 4UI pulse from div10 clock 2'b10: 2UI pulse from div40 clock 2'b11: 4UI pulse from div40 clock

HDPTXPHY_LANE_REG0511

Address: Operational Base(0x2B000000) + offset (0x1444)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln2_tx_sync_pulse_det_clk_en Override enable for ln2_tx_sync_pulse_det_clk_en
6	RW	0x0	ln2_tx_sync_pulse_det_clk_en Enables the clock path for sync loss detector.
5	RW	0x0	ovrd_ln2_tx_sync_pulse_det_en Override enable for ln2_tx_sync_pulse_det_en
4	RW	0x0	ln2_tx_sync_pulse_det_en Enables the sync loss detector.
3	RW	0x0	ln2_tx_ser_40bit_en_rbr [rbr] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
2	RW	0x0	ln2_tx_ser_40bit_en_hbr [hbr]TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
1	RW	0x0	ln2_tx_ser_40bit_en_hbr2 [hbr2] TX serializer data width
0	RW	0x0	ln2_tx_ser_40bit_en_hbr3 [hbr3] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit

HDPTXPHY_LANE_REG0512

Address: Operational Base(0x2B000000) + offset (0x1448)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln2_tx_ser_data_rstn Override enable for ln2_tx_ser_data_rstn
6	RW	0x0	ln2_tx_ser_data_rstn TX serializer data-path resetn 1'b0: Reset 1'b1: Released

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Bit	Attr	Reset Value	Description
5	RW	0x0	ln2_tx_ser_rate_sel_rbr [rbr] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
4	RW	0x0	ln2_tx_ser_rate_sel_hbr [hbr]TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
3	RW	0x0	ln2_tx_ser_rate_sel_hbr2 [hbr2] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
2	RW	0x0	ln2_tx_ser_rate_sel_hbr3 [hbr3] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
1	RW	0x0	ovrd_ln2_tx_ser_clk_rstn Override enable for ln2_tx_ser_clk_rstn
0	RW	0x0	ln2_tx_ser_clk_rstn TX serializer clock-path resetn 1'b0: Reset 1'b1: Released

HDPTXPHY_LANE_REG0516

Address: Operational Base(0x2B000000) + offset (0x1458)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	ln2_ana_tx_ser_vreg_gain_ctrl Control regulator feedback gain--> <3>: No connect, <2:0>: Gain--> 3'b000: 1 3'b001: 1.03 3'b010: 1.035 3'b011: 1.043 3'b100: 1.059 3'b101: 1.094 3'b110: 1.118 3'b111: 1.155 Output regulator voltage: Gain*VDD

HDPTXPHY_LANE_REG051B

Address: Operational Base(0x2B000000) + offset (0x146C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ln2_ana_tx_reserved Reserved port

HDPTXPHY_LANE_REG051F

Address: Operational Base(0x2B000000) + offset (0x147C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x0	ln2_rx_clk_inv 1'b1: Inverts the BIST recovered clock before feeding to PMA digital BIST RX path 1'b0: Passes the BIST recovered clock to PMA digital BIST RX path without inversion
4:2	RW	0x5	ln2_tg_rcal_rstn_delay_time Rx Rcal reset delay time after PLL AFC done 3'b000: 0 3'b001: 0.5us 3'b010: 1us 3'b011: 2us 3'b100: 3us 3'b101: 5us 3'b110: 10us 3'b111: 20us
1:0	RW	0x0	ln2_tg_tx_dcc_en_delay_time 2'b00: 3'd4 2'b01: 3'd5 2'b10: 3'd6 2'b11: 3'd7

HDPTXPHY_LANE_REG0520

Address: Operational Base(0x2B000000) + offset (0x1480)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x5	ln2_tg_ser_vreg_fast_pulse_time 3'b000: 1us 3'b001: 2us 3'b010: 3us 3'b011: 4us 3'b100: 5us 3'b101: 10us 3'b110: 20us 3'b111: 30us
4	RW	0x0	ln2_ovrd_txd_deskew_rstn Override enable for ln2_txd_deskew_rstn
3	RW	0x0	ln2_txd_deskew_rstn Active low reset for the lane data path
2	RW	0x0	ln2_txd_deskew_bypass_err_chk Counter relation check bypass
1	RW	0x0	ln2_txd_deskew_fix_da Fix the latch phase
0	RW	0x0	ln2_txd_deskew_fix_db Fix the latch phase

HDPTXPHY_LANE_REG0521

Address: Operational Base(0x2B000000) + offset (0x1484)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln2_txd_deskew_bypass Enable Tx data bypass
6	RW	0x0	ln2_txd_data_clk_type_man_en Unused
5:4	RW	0x1	ln2_txd_clk_type Unused

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Bit	Attr	Reset Value	Description
3:2	RW	0x1	ln2_txd_data_type Unused
1	RW	0x0	ln2_nearlb_en 1'b1: Enables nearend loopback mode 1'b0: Disables nearend loopback mode
0	RW	0x0	ln2_bist_auto_run Auto BIST start and errinj

HDPTXPHY_LANE_REG0603

Address: Operational Base(0x2B000000) + offset (0x180C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln3_ana_tx_drv_eien_fb_en tx common mode feedback when eien is enable 1'b0: Disable 1'b1: Enable(feedback is enable)
5	RW	0x0	ovrd_ln3_tx_drv_lvl_ctrl Override enable for ln3_tx_drv_lvl_ctrl
4:0	RW	0x00	ln3_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap-level (max swing) ... 5'b00000: min main-tap-level (min swing) Others: N/A

HDPTXPHY_LANE_REG0607

Address: Operational Base(0x2B000000) + offset (0x181C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln3_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b0: Polarity change, data P/N is switched (deenhancement) 1'b1: Polarity non-change(enhancement)
5:3	RW	0x0	ln3_ana_tx_drv_accdrv_ctrl TX edge-enhancement AC coupled driver strength control 3'b000: No enhancement ... 3'b111: Max enhancement
2	RW	0x0	ln3_ana_tx_drv_hsclk_mon_en Enable of high-speed clock monitor through Tx driver 1'b0: Disable 1'b1: Enable
1	RW	0x0	ln3_ana_tx_drv_pll_ref_mon_en Enable of PLL reference clock monitor through Tx driver 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln3_ana_tx_drv_pll_ref_mon_sel Select PLL reference clock monitor through Tx driver 1'b0: LCPLL 1'b1: ROPLL (MPHY do not need this pin, always LCPLL)

HDPTXPHY_LANE_REG060A

Address: Operational Base(0x2B000000) + offset (0x1828)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	ln3_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x0	ln3_tx_jeq_even_ctrl_rbr [rbr] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG060B

Address: Operational Base(0x2B000000) + offset (0x182C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ln3_tx_jeq_even_ctrl_hbr [hbr]TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	ln3_tx_jeq_even_ctrl_hbr2 [hbr2] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG060C

Address: Operational Base(0x2B000000) + offset (0x1830)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ln3_tx_jeq_even_ctrl_hbr3 [hbr3] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on
3:0	RW	0x0	ln3_tx_jeq_odd_ctrl_rbr [rbr] TX jitter EQ driver (odd) strength control same as even control

HDPTXPHY_LANE_REG060D

Address: Operational Base(0x2B000000) + offset (0x1834)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ln3_tx_jeq_odd_ctrl_hbr [hbr] TX jitter EQ driver (odd) strength control same as even control
3:0	RW	0x0	ln3_tx_jeq_odd_ctrl_hbr2 [hbr2] TX jitter EQ driver (odd) strength control same as even control

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HDPTXPHY_LANE_REG060E

Address: Operational Base(0x2B000000) + offset (0x1838)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:3	RW	0x0	ln3_tx_jeq_odd_ctrl_hbr3 [hbr3] TX jitter EQ driver (odd) strength control Same as even control
2	RW	0x0	ovrd_ln3_tx_rcal_en Override enable for ln3_tx_rcal_en
1	RW	0x0	ln3_tx_rcal_en TX RCAL enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln3_ana_tx_rterm_42p5_en TX 42.5 ohms termination enable 1'b0: Disable (50 ohm) 1'b1: Enable (42.5 ohm)

HDPTXPHY_LANE_REG0610

Address: Operational Base(0x2B000000) + offset (0x1840)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:2	RW	0x00	ln3_ana_tx_bist_mode This defines the BIST paths and modes as follows: <0> enables the serializer data output. <1> flips the serializer data output <3:2> defines the line sampling input 2'b00: txp-txn 2'b01: txn-vdd/2 2'b10: txp-vdd/2 2'b11: off <4> inverts the byte clock <5> enables the SA bist clock in LANE CD
1:0	RW	0x2	ln3_ana_tx_sync_loss_det_mode Slects the sync loss detection mode from the followin table: 2'b00: 2UI pulse from div10 clock 2'b01: 4UI pulse from div10 clock 2'b10: 2UI pulse from div40 clock 2'b11: 4UI pulse from div40 clock

HDPTXPHY_LANE_REG0611

Address: Operational Base(0x2B000000) + offset (0x1844)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln3_tx_sync_pulse_det_clk_en Override enable for ln3_tx_sync_pulse_det_clk_en
6	RW	0x0	ln3_tx_sync_pulse_det_clk_en Enables the clock path for sync loss detector.
5	RW	0x0	ovrd_ln3_tx_sync_pulse_det_en Override enable for ln3_tx_sync_pulse_det_en.
4	RW	0x0	ln3_tx_sync_pulse_det_en Enables the sync loss detector.
3	RW	0x0	ln3_tx_ser_40bit_en_rbr [rbr] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit

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Bit	Attr	Reset Value	Description
2	RW	0x0	ln3_tx_ser_40bit_en_hbr [hbr] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
1	RW	0x0	ln3_tx_ser_40bit_en_hbr2 [hbr2] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
0	RW	0x0	ln3_tx_ser_40bit_en_hbr3 [hbr3] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit

HDPTXPHY_LANE_REG0612

Address: Operational Base(0x2B000000) + offset (0x1848)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln3_tx_ser_data_rstn Override enable for ln3_tx_ser_data_rstn
6	RW	0x0	ln3_tx_ser_data_rstn TX serializer data-path resetn 1'b0: Reset 1'b1: Released
5	RW	0x0	ln3_tx_ser_rate_sel_rbr [rbr] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
4	RW	0x0	ln3_tx_ser_rate_sel_hbr [hbr]TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
3	RW	0x0	ln3_tx_ser_rate_sel_hbr2 [hbr2] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
2	RW	0x0	ln3_tx_ser_rate_sel_hbr3 [hbr3] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
1	RW	0x0	ovrd_ln3_tx_ser_clk_rstn Override enable for ln3_tx_ser_clk_rstn
0	RW	0x0	ln3_tx_ser_clk_rstn TX serializer clock-path resetn 1'b0: Reset 1'b1: Released

HDPTXPHY_LANE_REG0616

Address: Operational Base(0x2B000000) + offset (0x1858)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	ln3_ana_tx_ser_vreg_gain_ctrl Control regulator feedback gain--> <3>: No connect, <2:0>: Gain--> 3'b000: 1 3'b001: 1.03 3'b010: 1.035 3'b011: 1.043 3'b100: 1.059 3'b101: 1.094 3'b110: 1.118 3'b111: 1.155 Output regulator voltage: Gain*VDD

HDPTXPHY_LANE_REG061B

Address: Operational Base(0x2B000000) + offset (0x186C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	ln3_ana_tx_reserved Reserved port

HDPTXPHY_LANE_REG061E

Address: Operational Base(0x2B000000) + offset (0x1878)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln3_ovrd_tx_rcal_done Override enable for ln3_tx_rcal_done
6	RW	0x0	ln3_tx_rcal_done Monitoring for TX RCAL done
5	RW	0x0	ln3_drv_lvl_deskew_bypass Unused
4	RW	0x0	ln3_eien_deskew_bypass Unused
3	RW	0x0	ln3_hdmi_tmds_clk_lane_sel Selects clock user pattern or 40-bit tx data depending on protocol select and HDMI TMDS FRL select signals
2	RW	0x0	ln3_polarity_inv Polarity inversion of data when set to 1
1	RW	0x0	ln3_lane_mode 1'b1: The deskew FIFO works on shared pointer 1'b0: The deskew FIFO works on its own pointers
0	RW	0x0	ln3_lane_timer_sel 1'b1: Updates the lane timer value on monitoring interface even if Lane SSM did not complete 1'b0: Lets the lane timer updated on monitoring interface only when Lane SSM completes

HDPTXPHY_LANE_REG061F

Address: Operational Base(0x2B000000) + offset (0x187C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ln3_rx_clk_inv 1'b1: Inverts the BIST recovered clock before feeding to PMA digital BIST RX path 1'b0: Passes the BIST recovered clock to PMA digital BIST RX path without inversion

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Bit	Attr	Reset Value	Description
4:2	RW	0x5	ln3_tg_rcal_rstn_delay_time Rx Rcal reset delay time after PLL AFC done 3'b000: 0 3'b001: 0.5us 3'b010: 1us 3'b011: 2us 3'b100: 3us 3'b101: 5us 3'b110: 10us 3'b111: 20us
1:0	RW	0x0	ln3_tg_tx_dcc_en_delay_time 2'b00: 3'd4 2'b01: 3'd5 2'b10: 3'd6 2'b11: 3'd7

25.5 Interface Description

25.5.1 Using as HDMI TX PHY

Table 25-2 HDMI TX PHY Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
hdmitx_ln0_txdp	O	HDMI_TX_D0P/EDP_TX_D0P	NS
hdmitx_ln0_txdn	O	HDMI_TX_D0N/EDP_TX_D0N	NS
hdmitx_ln1_txdp	O	HDMI_TX_D1P/EDP_TX_D1P	NS
hdmitx_ln1_txdn	O	HDMI_TX_D1N/EDP_TX_D1N	NS
hdmitx_ln2_txdp	O	HDMI_TX_D2P/EDP_TX_D2P	NS
hdmitx_ln2_txdn	O	HDMI_TX_D2N/EDP_TX_D2N	NS
hdmitx_ln3_txdp	O	HDMI_TX_D3P/EDP_TX_D3P	NS
hdmitx_ln3_txdn	O	HDMI_TX_D3N/EDP_TX_D3N	NS
hdmitx_sbdp	I/O	HDMI_TX_SBDP/EDP_TX_AUXP	NS
hdmitx_sbdn	I/O	HDMI_TX_SBDN/EDP_TX_AUXN	NS
hdmitx_cec_m0	I/O	DSM_AUD_LP_M1/SAI4_MCLK_M2/HDMI_TX_CEC_M0/I2C7_SCL_M3/SPI4_CSN1_M0/UART11_TX_M2/PWM1_CH5_M1/GPIO4_C0_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[3:0]==0x9
hdmitx_cec_m1	I/O	PDM0_CLK1_M0/HDMI_TX_CEC_M1/SPI0_CSN1_M0/PWM0_CH1_M0/GPIO0_C3_d	PMUIO1_IOC_GPIO0C_IOMUX_SEL_L[15:12]==0x9
hdmitx_hpd_m0	I/O	DSM_AUD_LN_M1/HDMI_TX_HPDIN_M0/PCIE1_CLKREQN_M3/I2C7_SDA_M3/EDP_TX_HPDIN_M0/UART11_RX_M2/PWM0_CH1_M1/GPIO4_C1_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[7:4]==0x9
hdmitx_hpd_m1	I/O	SDMMC0_PWREN/SDMMC1_DETN_M2/HDMI_TX_HPDIN_M1/EDP_TX_HPDIN_M1/PWM1_CH2_M0/GPIO0_B6_d	PMUIO1_IOC_GPIO0B_IOMUX_SEL_L[11:8]==0x9
hdmitx_scl	I/O	DSM_AUD_RP_M1/HDMI_TX_SCL/I2C2_SCL_M3/CAN0_TX_M1/UART9_TX_M2/PWM2_C	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[11:8]==0x9

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Module Pin	Direction	Pad Name	IOMUX Setting
		H0_M1/GPIO4_C2_d	
hdmitx_sda	I/O	DSM_AUD_RN_M1/HDMI_TX_SDA/I2C2_SDA_M3/CAN0_RX_M1/UART9_RX_M2/PWM2_CH1_M1/GPIO4_C3_d	VCCIO6_IOC_GPIO4C_IOMUX_SEL_L[15:12]==0x9

Notes: I=input, O=output, I/O=input/output, bidirectional

25.5.2 Using as EDP TX PHY

Module Pin	Direction	Pad Name	IOMUX Setting
edptx_ln0_txdp	O	HDMI_TX_D0P/EDP_TX_D0P	NS
edptx_ln0_txdn	O	HDMI_TX_D0N/EDP_TX_D0N	NS
edptx_ln1_txdp	O	HDMI_TX_D1P/EDP_TX_D1P	NS
edptx_ln1_txdn	O	HDMI_TX_D1N/EDP_TX_D1N	NS
edptx_ln2_txdp	O	HDMI_TX_D2P/EDP_TX_D2P	NS
edptx_ln2_txdn	O	HDMI_TX_D2N/EDP_TX_D2N	NS
edptx_ln3_txdp	O	HDMI_TX_D3P/EDP_TX_D3P	NS
edptx_ln3_txdn	O	HDMI_TX_D3N/EDP_TX_D3N	NS
edptx_sbdp	I/O	HDMI_TX_SBDP/EDP_TX_AUXP	NS
edptx_sbdn	I/O	HDMI_TX_SBDN/EDP_TX_AUXN	NS
edptx_hpd_m0	I	DSM_AUD_LN_M1/HDMI_TX_HPDIN_M0/PCIE1_CLKREQN_M3/I2C7_SDA_M3/EDP_TX_HPDIN_M0/UART11_RX_M2/PWM0_CH1_M1/GPIO4_C1_d	VCCIO6_IOC_GPIO4A_IOMUX_SEL_L[7:4]=4'hC
edptx_hpd_m1	I	SDMMC0_PWREN/SDMMC1_DETN_M2/HDMI_TX_HPDIN_M1/EDP_TX_HPDIN_M1/PWM1_CH2_M0/GPIO0_B6_d	PMU1_IOC_GPIO3D_IOMUX_SEL_H[11:8]=4'hA

Notes: I=input, O=output, I/O=input/output, bidirectional, NS=Not Set

25.6 Application Notes

25.6.1 SFR Settings for HDMI mode

This table shows how to set SFR in HDMI mode. The "Setting Value" column has settings for TMDS 40 bits mode with lane 3 as clock lane. Please follow the description column to set for 18/20/36 bits mode, FRL mode and clock lane change.

Table 25-3 DP 40bit mode with RBR rate SFR Setting

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0800[2]	protocol_sel	0x0	0x1	0: DP mode 1: HDMI mode
0x025C[1]	dig_clk_sel	0x0	0x1	1'b0: Select LCPLL reference clock mux output (LCPLL alone mode and Cascade mode) 1'b1: Select ROPLL reference clock mux output (ROPLL alone mode)
0x0C28[4]	ln0_ana_tx_jeq_en	0x0	0x1	Transmitter setting
0x1028[4]	ln1_ana_tx_jeq_en	0x0	0x1	Transmitter setting
0x1428[4]	ln2_ana_tx_jeq_en	0x0	0x1	Transmitter setting

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0x1828[4]	ln3_ana_tx_jeq_en	0x0	0x1	Transmitter setting
0x0C28[3:0]	ln0_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter setting
0x0C2C[7:4]	ln0_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter setting
0x0C2C[3:0]	ln0_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter setting
0x0C30[7:4]	ln0_tx_jeq_even_ctrl_hbr3	0x0	0x7	Transmitter setting
0x1028[3:0]	ln1_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter setting
0x102C[7:4]	ln1_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter setting
0x102C[3:0]	ln1_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter setting
0x130C[7:4]	ln1_tx_jeq_even_ctrl_hbr3	0x0	0x7	Transmitter setting
0x1428[3:0]	ln2_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter setting
0x142C[7:4]	ln2_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter setting
0x142C[3:0]	ln2_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter setting
0x1430[7:4]	ln2_tx_jeq_even_ctrl_hbr3	0x0	0x7	Transmitter setting
0x1828[3:0]	ln3_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter setting
0x182C[7:4]	ln3_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter setting
0x182C[3:0]	ln3_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter setting
0x1830[7:4]	ln3_tx_jeq_even_ctrl_hbr3	0x0	0x7	Transmitter setting
0x0C30[3:0]	ln0_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter setting
0x0C34[7:4]	ln0_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter setting

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0x0C34[3:0]	ln0_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter setting
0x0C38[7:4]	ln0_tx_jeq_odd_ctrl_hbr3	0x0	0x7	Transmitter setting
0x1030[3:0]	ln1_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter setting
0x1034[7:4]	ln1_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter setting
0x1034[3:0]	ln1_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter setting
0x1038[7:4]	ln1_tx_jeq_odd_ctrl_hbr3	0x0	0x7	Transmitter setting
0x1430[3:0]	ln2_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter setting
0x1434[7:4]	ln2_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter setting
0x1434[3:0]	ln2_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter setting
0x1438[7:4]	ln2_tx_jeq_odd_ctrl_hbr3	0x0	0x7	Transmitter setting
0x1830[3:0]	ln3_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter setting
0x1834[7:4]	ln3_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter setting
0x1834[3:0]	ln3_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter setting
0x1838[3:0]	ln3_tx_jeq_odd_ctrl_hbr3	0x0	0x7	Transmitter setting
0x0C0C[4:0]	ln0_tx_drv_lvl_ctrl	0x0	0xC	Transmitter setting
0x100C[4:0]	ln1_tx_drv_lvl_ctrl	0x0	0xC	Transmitter setting
0x140C[4:0]	ln2_tx_drv_lvl_ctrl	0x0	0xC	Transmitter setting
0x180C[4:0]	ln3_tx_drv_lvl_ctrl	0x0	0xC	Transmitter setting
0x0C1C[6]	ln0_ana_tx_drv_accdrv_pol_sel	0x0	0x0	Transmitter setting
0x101C[6]	ln1_ana_tx_drv_accdrv_pol_sel	0x0	0x0	Transmitter setting
0x141C[6]	ln2_ana_tx_drv_accdrv_pol_sel	0x0	0x0	Transmitter setting

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0x181C[6]	ln3_ana_tx_drv_accdrv_pol_sel	0x0	0x0	Transmitter setting
0x0C1C[5:3]	ln0_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter setting
0x101C[5:3]	ln1_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter setting
0x141C[5:3]	ln2_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter setting
0x181C[5:3]	ln3_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter setting
0x021C[2]	ana_pll_tx_hs_clk_en	0x0	0x1	PLL setting
0x0204[0]	ana_pll_cd_hsclk_east_en	0x0	0x1	PLL setting
0x0204[1]	ana_pll_cd_hsclk_west_en	0x0	0x0	PLL setting
0x0818[2:1]	data_bus_width	0x0	0x3	0x0: 18 bits data bus (for HDMI FRL mode only) 0x1: 20 bits data bus 0x2: 36 bits data bus (for HDMI FRL mode only) 0x3: 40 bits data bus
0x0818[0]	bus_width_sel	0x0	0x1	0x0: 18/20 bits data bus 0x1: 36/40 bits data bus
0x0254[1:0]	dp_tx_link_bw	0x0	0x0	Multiplexes the register settings for analog blocks. 0x0: RBR register settings applied to analog (*_rbr registers) 0x1: HBR register settings applied to analog (*_hbr registers) 0x2: HBR2 register settings applied to analog (*_hbr2 registers) 0x3: HBR3 register settings applied to analog (*_hbr3 registers)
0x0264[2]	cmn_ropll_alone_mode	0x0	0x1	0x0: Cascade mode/LCPLL mode 0x1: ROPLL alone mode. For HDMI TMDS rates ROPLL alone mode should be used.

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				For FRL 8Gbps rate, cascade mode needs to be used.
0x0224[1]	cmn_lcpll_alone_mode	0x0	0x0	0x0: Cascade mode/ROPLL mode 0x1: LCPLL alone mode. For FRL 8Gbps rate, cascade mode needs to be used. For FRL 10Gbps and 12Gbps, LCPLL alone mode should be used.
0x0204[3]	ana_pll_cd_tx_ser_rate_sel	0x0	0x0	0x0: For TMDS mode 0x1: For FRL mode
0x021C[3]	ana_pll_frl_mode_en	0x0	0x0	0x0: For TMDS mode 0x1: For FRL mode
0x0C6C[7:0]	ln0_ana_tx_reserved	0x0	0x1	Transmitter setting
0x106C[7:0]	ln1_ana_tx_reserved	0x0	0x1	Transmitter setting
0x014C[7:0]	ln2_ana_tx_reserved	0x0	0x1	Transmitter setting
0x018C[7:0]	ln3_ana_tx_reserved	0x0	0x1	Transmitter setting
0x0C58[3:0]	ln0_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting
0x1058[3:0]	ln1_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting
0x1458[3:0]	ln2_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting
0x1858[3:0]	ln3_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting
0x0C40[1:0]	ln0_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting
0x1040[1:0]	ln1_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting
0x1440[1:0]	ln2_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting
0x1840[1:0]	ln3_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting

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0x0208[3:0]	ana_pll_cd_vreg_gain_ctrl	0x0	0x4	PLL setting
0x00F0[7]	ana_lcpll_reserved[7]	0x0	0x1	PLL setting
0x020C[6:5]	ana_pll_cd_vreg_ictrl	0x1	0x1	PLL setting
0x0214[1:0]	ana_pll_sync_loss_det_mode	0x0	0x3	PLL setting
0x0210[5]	pll_lcro_clk_sel	0x0	0x1	PLL setting
0x0268[0]	hs_speed_sel	0x0	0x1	Clock setting of o_tx_hs_clk 0x0: Div20 clock output 0x1: Div10 clock output
0x026C[4]	ls_speed_sel	0x0	0x0	Clock setting of o_tx_link_sym_clk 0x0: Div40/Div36 clock output 0x1: Div20/Div18 clock output
0x0C44[3]	ln0_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x0C44[2]	ln0_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting
0x0C44[1]	ln0_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x0C44[0]	ln0_tx_ser_40bit_en_hbr3	0x0	0x1	Transmitter setting
0x1044[3]	ln1_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x1044[2]	ln1_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting
0x1044[1]	ln1_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x1044[0]	ln1_tx_ser_40bit_en_hbr3	0x0	0x1	Transmitter setting
0x1444[3]	ln2_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x1444[2]	ln2_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting
0x1444[1]	ln2_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x1444[0]	ln2_tx_ser_40bit_en_hbr3	0x0	0x1	Transmitter setting
0x1844[3]	ln3_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x1844[2]	ln3_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting

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0x1844[1]	ln3_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x1844[0]	ln3_tx_ser_40bit_en_hbr3	0x0	0x1	Transmitter setting
0x0C48[5]	ln0_tx_ser_rate_sel_rbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x0C48[4]	ln0_tx_ser_rate_sel_hbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x0C48[3]	ln0_tx_ser_rate_sel_hbr2	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x0C48[2]	ln0_tx_ser_rate_sel_hbr3	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1048[5]	ln1_tx_ser_rate_sel_rbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1048[4]	ln1_tx_ser_rate_sel_hbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1048[3]	ln1_tx_ser_rate_sel_hbr2	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1048[2]	ln1_tx_ser_rate_sel_hbr3	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1448[5]	ln2_tx_ser_rate_sel_rbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1448[4]	ln2_tx_ser_rate_sel_hbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1448[3]	ln2_tx_ser_rate_sel_hbr2	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1448[2]	ln2_tx_ser_rate_sel_hbr3	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1848[5]	ln3_tx_ser_rate_sel_rbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1848[4]	ln3_tx_ser_rate_sel_hbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1848[3]	ln3_tx_ser_rate_sel_hbr2	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1848[2]	ln3_tx_ser_rate_sel_hbr3	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x0804[7:0]	clk_user_pat_39_32	0x0	0x0	Clock pattern to be driven on the clock serial lanes. Bit 40 to 32.
0x0808[7:0]	clk_user_pat_31_24	0x0	0x0	Clock pattern to be driven on the clock serial lanes. Bit 31 to 24.
0x080C[7:0]	clk_user_pat_23_16	0x0	0x0F	Clock pattern to be driven on the clock serial lanes. Bit 23 to 16.

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0x0810[7:0]	clk_user_pat_15_8	0x0	0xFF	Clock pattern to be driven on the clock serial lanes. Bit 15 to 8.
0x0814[7:0]	clk_user_pat_7_0	0x0	0xFF	Clock pattern to be driven on the clock serial lanes. Bit 7 to 0.
0x0C78[3]	ln0_hdmi_tmds_clk_lane_sel	0x0	0x0	0x0: Lane 0 drives the serial data 0x1: Lane 0 drives the clock pattern on serial lanes This register should be set for only HDMI TMDS mode basing clock lane requirement.
0x1078[3]	ln1_hdmi_tmds_clk_lane_sel	0x0	0x0	0x0: Lane 1 drives the serial data 0x1: Lane 1 drives the clock pattern on serial lanes. This register should be set for only HDMI TMDS mode basing clock lane requirement.
0x1478[3]	ln2_hdmi_tmds_clk_lane_sel	0x0	0x0	0x0: Lane 2 drives the serial data 0x1: Lane 2 drives the clock pattern on serial lanes This register should be set for only HDMI TMDS mode basing clock lane requirement.
0x1878[3]	ln3_hdmi_tmds_clk_lane_sel	0x0	0x1	0x0: Lane 3 drives the serial data 0x1: Lane 3 drives the clock pattern on serial lanes This register should be set for only HDMI TMDS mode basing clock lane requirement.
0x0800[1]	hdmi_tmds_frl_sel	0x0	0x1	0x0: HDMI FRL mode 0x1: HDMI TMDS mode
0x0218[7:4]	ana_pll_pcg_postdiv_sel	0x1	0x1	PLL Setting
0x0218[3:1]	ana_pll_pcg_clk_sel	0x0	0x0	PLL Setting
0x0218[0]	ana_pll_pcg_clk_en	0x0	0x1	0x0: Disables pixel clock generation 0x1: Enables pixel clock generation
0x081C[3:0]	lane_en	0x0	0xF	lane_en bit0: 0x0 – Disables the lane 0 0x1 – Enables the lane 0 lane_en bit1: 0x0 – Disables the lane 1 0x1 – Enables the lane 1 lane_en bit2: 0x0 – Disables the lane 2 0x1 – Enables the lane 2

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				lane_en bit3: 0x0 – Disables the lane 3 0x1 – Enables the lane 3 Only one lane can be disabled based on HDMI protocol, that too in FRL 3Gbps and 6Gbps rates only.

25.6.2 EDP TX PHY Application

"SFR Address" in the tables below means that Comb TX PHY's address.

25.6.2.1 Start-Up Sequence for PHY

The Power-Up sequence as the table below.

Table 25-4 Programming Sequence for DP Start-Up operation

Power-Up Sequence
Power up and clock is valid
Reset PHY and reset init_rstn, cmn_rstn and lane_rstn by writing PMU1CRU_SOFTRST_CON01[9]=1'b1, PMU1CRU_SOFTRST_CON01[10]=1'b1, PMU1CRU_SOFTRST_CON01[11]=1'b1
Release APB reset of PHY
Write internal registers thought APB. Configure AUX and Main Link register in this stage. Detail configuration can be found in the following chapters.
Write HDPTXPHY_GRF_CON0[6:5]=2'b11, bias_en=1, bgr_en=1
Wait 10us
Write PMU1CRU_SOFTRST_CON01[9]=1'b0, release init_rstn
Wait 10us
Write HDPTXPHY_GRF_CON0[7]=1'b1, pll_en=1
Wait 10us
PMU1CRU_SOFTRST_CON01[10]=1'b0, release cmn_rstn
Wait o_pll_lock_done, read <HDPTXPHY_GRF_STATUS> (Please see HDPTXPHY_GRF for base and offset address) until bit3 o_pll_lock_done=1.
Wait 10us
PMU1CRU_SOFTRST_CON01[11]=1'b0, release lane_rstn
Wait o_phy_rdy, read <HDPTXPHY_GRF_STATUS> until bit1 o_phy_rdy=1.
The PHY's configuration is ready, the controller can send data.

25.6.2.2 PHY AUX Setting

Below are the registers to be configured to bring up sideband in aux mode. Please set AUX as the sequence in the table below.

Table 25-5 Programming Sequence for DP AUX mode operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x044C[5:4]	sb_rx_rcal_opt_code	0x0	0x1	This is use to select finale rcal code after rcal enable goes low and rcal done goes high 2'b00: o_rcal_code = tune_code 2'b01: o_rcal_code = i_sfr_rcal_code 2'b10: o_rcal_code = tune_code +

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SFR Address	SFR Name	Default Value	Setting Value	Description
				i_sfr_rcal_code (i_sfr_sb_rx_rterm_ctrl) 2'b11: o_rcal_code = tune_code - i_sfr_rcal_code (i_sfr_sb_rx_rterm_ctrl)
0x044C[3:0]	sb_rx_rterm_ctrl	0x0	0x3	This is the code to be added in the tune code to generate finale rcal code depends on the value of i_sfr_sb_rx_rcal_opt_code
0x0450[5:3]	sb_tg_sb_en_delay_time	0x0	0x2	This sfr is the select line to set count wrt refclock cycle to set sb enable after rcal done goes high 3'b000: delay_time = 9'd0; 0us for 25MHz refclk 3'b001: delay_time = 9'd13; 0.5us for 25MHz refclk 3'b010: delay_time = 9'd25; 1us for 25MHz refclk 3'b011: delay_time = 9'd50; 2us for 25MHz refclk 3'b100: delay_time = 9'd75; 3us for 25MHz refclk 3'b101: delay_time = 9'd125; 5us for 25MHz refclk 3'b110: delay_time = 9'd250; 10us for 25MHz refclk 3'b111: delay_time = 9'd500; 20us for 25MHz refclk default: delay_time = 9'd25; 1us for 25MHz refclk
0x0450[2:0]	sb_tg_rxterm_en_delay_time	0x0	0x2	This sfr is the select line to set count wrt refclock cycle to set rxterm enable after sb enable goes high 3'b000: delay_time = 9'd0; 0us for 25MHz refclk 3'b001: delay_time = 9'd13; 0.5us for 25MHz refclk 3'b010: delay_time = 9'd25; 1us for 25MHz refclk 3'b011: delay_time = 9'd50; 2us for 25MHz refclk 3'b100: delay_time = 9'd75; 3us for 25MHz refclk 3'b101: delay_time = 9'd125;

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SFR Address	SFR Name	Default Value	Setting Value	Description
				5us for 25MHz refclk 3'b110: delay_time = 9'd250; 10us for 25MHz refclk 3'b111: delay_time = 9'd500; 20us for 25MHz refclk default: delay_time = 9'd25; 1us for 25MHz refclk
0x0454[5:3]	sb_ready_delay_time	0x0	0x2	This sfr is the select line to set count count wrt refclock cycle to set sb ready signal after all calibration completed 3'b000: delay_time = 9'd0; 0us for 25MHz refclk 3'b001: delay_time = 9'd13; 0.5us for 25MHz refclk 3'b010: delay_time = 9'd25; 1us for 25MHz refclk 3'b011: delay_time = 9'd50; 2us for 25MHz refclk 3'b100: delay_time = 9'd75; 3us for 25MHz refclk 3'b101: delay_time = 9'd125; 5us for 25MHz refclk 3'b110: delay_time = 9'd250; 10us for 25MHz refclk 3'b111: delay_time = 9'd500; 20us for 25MHz refclk default: delay_time = 9'd25; 1us for 25MHz refclk
0x0454[2:0]	sb_tg_osc_en_delay_time	0x0	0x2	This sfr is the select line to set count count wrt refclock cycle to set oscillator enable after vreg sequence completed 3'b000: delay_time = 9'd0; 0us for 25MHz refclk 3'b001: delay_time = 9'd13; 0.5us for 25MHz refclk 3'b010: delay_time = 9'd25; 1us for 25MHz refclk 3'b011: delay_time = 9'd50; 2us for 25MHz refclk 3'b100: delay_time = 9'd75; 3us for 25MHz refclk 3'b101: delay_time = 9'd125; 5us for 25MHz refclk

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SFR Address	SFR Name	Default Value	Setting Value	Description
				3'b110: delay_time = 9'd250; 10us for 25MHz refclk 3'b111: delay_time = 9'd500; 20us for 25MHz refclk default: delay_time = 9'd25; 1us for 25MHz refclk
0x0458[6:4]	sb_tg_osc_en_to_afc_rstn_delay_time	0x0	0x2	This sfr is the select line to set count wrt refclock cycle to release reset to afc calibration module after oscillator osc enable signal set. 3'b000: delay_time = 9'd0; 0us for 25MHz refclk 3'b001: delay_time = 9'd13; 0.5us for 25MHz refclk 3'b010: delay_time = 9'd25; 1us for 25MHz refclk 3'b011: delay_time = 9'd50; 2us for 25MHz refclk 3'b100: delay_time = 9'd75; 3us for 25MHz refclk 3'b101: delay_time = 9'd125; 5us for 25MHz refclk 3'b110: delay_time = 9'd250; 10us for 25MHz refclk 3'b111: delay_time = 9'd500; 20us for 25MHz refclk default: delay_time = 9'd25; 1us for 25MHz refclk
0x045C[3:0]	sb_tg_pll_cd_vreg_fast_pulse_time	0x0	0x4	This sfr is the select line to set number of clock cycle for which vreg bypass signal go high 4'b0000: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd25; 1us for 25MHz refclk 4'b0001: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd50; 2us for 25MHz refclk 4'b0010: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd75; 3us for 25MHz refclk

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SFR Address	SFR Name	Default Value	Setting Value	Description

				4'b0011:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd100;
				4us for 25MHz refclk
				4'b0100:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd125;
				5us for 25MHz refclk
				4'b0101:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd250;
				10us for 25MHz refclk
				4'b0110:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd500;
				20us for 25MHz refclk
				4'b0111:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd750;
				30us for 25MHz refclk
				4'b1000:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd1000;
				40us for 25MHz refclk
				4'b1001:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd1250;
				50us for 25MHz refclk
				4'b1010:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd2500;
				100us for 25MHz refclk
				4'b1011:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd3750;
				150us for 25MHz refclk
				4'b1100:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd5000;
				200us for 25MHz refclk
				4'b1101:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd7500;
				300us for 25MHz refclk
				4'b1110:

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SFR Address	SFR Name	Default Value	Setting Value	Description

				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd10000;
				400us for 25MHz refclk
				4'b1111:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd12500;
				500us for 25MHz refclk
				default:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd250;

0x0460[7:0]	sb_tg_earc_dmrx_recvrd_clk_cnt	0x0	0xA	This is the target count the rec clk should give for specifide refclock cycle This count should be 10, 20 or 40 (i_sfr_sb_tg_cnt_run_no * reference clock cycle period) <= (i_sfr_sb_tg_earc_dmrx_recvrd_clk_cnt* recover clock period
0x0464[7:0]	sb_tg_cnt_run_no_7_0	0x0	0x3	This is the refclock count cycle during which rec clock counter run This count should be such that time duration with refclock good enough to get requird rec clock count (i_sfr_sb_tg_cnt_run_no * reference clock cycle period) <= (i_sfr_sb_tg_earc_dmrx_recvrd_clk_cnt* recover clock period)
0x046C[4]	sb_earc_sig_det_bypass	0x0	0x1	This sfr use to bypass signal detect logic
0x046C[3:0]	sb_afc_tol	0x0	0x3	OSC stable tolerance. This is the tolarance for vco count that can be taken to make sure vco generating stable frequency
0x0470[3:0]	sb_afc_stb_num	0x0	0x4	OSC stable number for initial time.it use to configure number of times vco generate stable count to go for stable frequency comparison state
0x0474[7:0]	sb_tg_osc_cnt_min	0x0	0x67	This is the minimum target count from vco to be received for one ref clock

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SFR Address	SFR Name	Default Value	Setting Value	Description
				cycle to to get 2.5GHz PLL clock Refclock: count required 24MHz: 8'd103 25MHz: 8'd99 26MHz: 8'd95 27MHz: 8'd92 45MHz: 8'd55 54MHz: 8'd46
0x0478[7:0]	sb_tg_osc_cnt_max	0x0	0x6A	This is the maximum target count from vco to be received for one ref clock cycle to to get 2.5GHz pll clock Refclock: count required 24MHz: 8'd106 25MHz: 8'd101 26MHz: 8'd98 27MHz: 8'd94 45MHz: 8'd57 54MHz: 8'd48
0x047C[7:2]	sb_pwm_afc_ctrl	0x0	0x5	This is the sfr which use for selecting pwm afc calibration code depending on its MSB MSB = 1 then MSB-1 to 0 bits value taken as calibration code for pwm afc MSB = 0 then afc code is internally generated from afc module logic if AFC _EN =1
0x0434[4]	ana_sb_dmrx_lpbk_data	0x0	0x1	The loopback data from register; the duty cycle of the data have to be more than 53% or less than 47%.
0x0440[1]	ana_sb_vreg_out_sel	0x0	0x1	It bypasses the LDO with VDD.
0x0440[0]	ana_sb_vreg_ref_sel	0x0	0x1	Used as power saving mode
0x043C[3:0]	ana_sb_vreg_gain_ctrl	0x1	0x0	Controls the feedback gain of the LDO. 4'b0000: 1.00 4'b0001: 1.03 4'b0010: 1.04 4'b0011: 1.05 4'b0100: 1.06 4'b0101: 1.09 4'b0110: 1.12

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SFR Address	SFR Name	Default Value	Setting Value	Description
				4’b0111: 1.15
0x0408[3:0]	ana_sb_rxterm_offsp	0x0	0x3	For i_sb_rescal_tune<2:0> = 3, the table for both OffsetP and N looks like 4’b0000: 50 Ohms 4’b0001: 48.4 Ohms 4’b0011: 46.9 Ohms 4’b0111: 45.5 Ohms 4’b1111: 44.2 Ohms
0x040C[6:3]	ana_sb_rxterm_offsn	0x0	0x3	For i_sb_rescal_tune<2:0> = 3, the table for both OffsetP and N looks like 4’b0000: 50 Ohms 4’b0001: 48.4 Ohms 4’b0011: 46.9 Ohms 4’b0111: 45.5 Ohms 4’b1111: 44.2 Ohms
0x047C[1]	sb_rcal_rstn	0x0	0x1	Sideband resister calibration enable signal If 1'b0 resister calibration disable If 1'b1 resister calibration enable
0x0410[0]	sb_aux_en	0x0	0x1	AUX Enable This is ovrd for sb_aux_en_in 1’b0: Disable 1’b1: Enable
0x0480[7]	sb_aux_en_in	0x0	0x1	AUX Enable 1’b0: Disable 1’b1: Enable
0x040C[1]	ovrd_sb_rx_rescal_done	0x0	0x1	Enable SFR override for rescal done
0x0410[5]	ovrd_sb_en	0x0	0x1	Enable SFR override for sideband enable
0x0408[5]	ovrd_sb_rxterm_en	0x0	0x1	Enable SFR override for sideband rx termination enable
0x043C[7]	ovrd_sb_vreg_en	0x0	0x1	Enable SFR override for sideband vreg enable
0x0410[1]	ovrd_sb_aux_en	0x0	0x1	Enable SFR override for sideband aux enable
0x048C[5]	ovrd_sb_ready	0x0	0x1	Enable SFR override for sideband ready
Bring up Bias/BGR, deassert init_rstn, cmn_rstn if not done already and wait for 1000us				
0x040C[0]	sb_rx_rescal_done	0x0	0x1	SFR override value for rescal done
Wat for 100us				

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SFR Address	SFR Name	Default Value	Setting Value	Description
0x0410[4]	sb_en	0x0	0x1	SFR override value for sideband enable
Wait for 100us				
0x0408[4]	sb_rxterm_en	0x0	0x1	SFR override value for sideband rx termination enable
Wait for 10us				
0x043C[6]	sb_vreg_en	0x0	0x1	SFR override value for sideband vreg enable
Wait for 10us				
0x0410[0]	sb_aux_en	0x0	0x1	SFR override value for sideband aux enable
Wait for 100us				
0x048C[4]	sb_ready	0x0	0x1	

25.6.2.3 PHY Main Link Setting

Below are the registers to be configured to set RBR/HBR/HBR2 rates. Please set link rate as the sequence in the table below. For the different setting of RBR/HBR/HBR2 rates and 1/2/4 lane, please see the table below.

Table 25-6 DP mode Setting

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0800[2]	protocol_sel	0x0	0x0	DP mode
0x025C[1]	dig_clk_sel	0x0	0x1	1'b0: Select LCPLL reference clock mux output (LCPLL alone mode and Cascade mode) 1'b1: Select ROPLL reference clock mux output (ROPLL alone mode)

if RBR:
<0x0144> = 0x87, <0x0154>=0x87, <0x0168>=0x33
<0x0180> = 0x21, <0x0190>=0x07, <0x0194> = 0x00
<0x01b0> = 0x03, <0x01c0>=0x08
else if HBR:
<0x0148> = 0x71, <0x0158>=0x71, <0x0168> = 0x31
<0x0184> = 0x27, <0x0190>=0x0f, <0x0198> = 0x0d
<0x01b4> = 0x07, <0x01c4>=0x18
else if HBR2:
<0x014c> = 0x71, <0x015c> = 0x71, <0x016c> = 0x03
<0x0188> = 0x27, <0x0190> = 0x0f, <0x019c> = 0x0d
<0x01b8> = 0x07, <0x01c8> = 0x18				

0x0C28[4]	ln0_ana_tx_jeq_en	0x0	0x1	Transmitter Setting
0x1028[4]	ln1_ana_tx_jeq_en	0x0	0x1	Transmitter Setting
0x1428[4]	ln2_ana_tx_jeq_en	0x0	0x1	Transmitter Setting

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SFR Address	SFR Name	Default Value	Setting Value	Description
0x1828[4]	ln3_ana_tx_jeq_en	0x0	0x1	Transmitter Setting
0x0C28[3:0]	ln0_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter Setting
0x0C2C[7:4]	ln0_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter Setting
0x0C2C[3:0]	ln0_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x1028[3:0]	ln1_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter Setting
0x102C[7:4]	ln1_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter Setting
0x102C[3:0]	ln1_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x1428[3:0]	ln2_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter Setting
0x142C[7:4]	ln2_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter Setting
0x142C[3:0]	ln2_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x1828[3:0]	ln3_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter Setting
0x182C[7:4]	ln3_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter Setting
0x182C[3:0]	ln3_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x0C30[3:0]	ln0_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter Setting
0x0C34[7:4]	ln0_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter Setting
0x0C34[3:0]	ln0_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x1030[3:0]	ln1_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter Setting
0x1034[7:4]	ln1_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter Setting
0x1034[3:0]	ln1_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x1430[3:0]	ln2_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter Setting

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SFR Address	SFR Name	Default Value	Setting Value	Description
0x1434[7:4]	ln2_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter Setting
0x1434[3:0]	ln2_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x1830[3:0]	ln3_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter Setting
0x1834[7:4]	ln3_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter Setting
0x1834[3:0]	ln3_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x0C0C[4:0]	ln0_tx_drv_lvl_ctrl	0x0	0xC	Transmitter Setting
0x100C[4:0]	ln1_tx_drv_lvl_ctrl	0x0	0xC	Transmitter Setting
0x140C[4:0]	ln2_tx_drv_lvl_ctrl	0x0	0xC	Transmitter Setting
0x180C[4:0]	ln3_tx_drv_lvl_ctrl	0x0	0xC	Transmitter Setting
0x0C1C[6]	ln0_ana_tx_drv_accdrv_pol_sel	0x0	0x1	Transmitter Setting
0x101C[6]	ln1_ana_tx_drv_accdrv_pol_sel	0x0	0x1	Transmitter Setting
0x141C[6]	ln2_ana_tx_drv_accdrv_pol_sel	0x0	0x1	Transmitter Setting
0x181C[6]	ln3_ana_tx_drv_accdrv_pol_sel	0x0	0x1	Transmitter Setting
0x0C1C[5:3]	ln0_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter Setting
0x101C[5:3]	ln1_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter Setting
0x141C[5:3]	ln2_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter Setting
0x181C[5:3]	ln3_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter Setting
0x021C[2]	ana_pll_tx_hs_clk_en	0x0	0x1	PLL setting

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SFR Address	SFR Name	Default Value	Setting Value	Description
0x0204[0]	ana_pll_cd_hsclk_east_en	0x0	0x1	PLL setting
0x0204[1]	ana_pll_cd_hsclk_west_en	0x0	0x0	PLL setting
0x0818[2:1]	data_bus_width	0x0	0x1	2'b00: 18 bit data bus (for HDMI FRL mode only) 2'b01: 20 bit data bus 2'b10: 36 bit data bus (for HDMI FRL mode only) 2'b11: 40 bit data bus
0x0818[0]	bus_width_sel	0x0	0x0	1'b0: 20 bit data bus 1'b1: 40 bit data bus
0x0254[1:0]	dp_tx_link_bw	0x0	0x0 or 0x1 or 0x2	Multiplexes the register settings for analog blocks. 2'b00: RBR register settings applied to analog (*_rbr registers) 2'b01: HBR register settings applied to analog (*_hbr registers) 2'b10: HBR2 register settings applied to analog (*_hbr2 registers) This register is set differently when work in different rates.
0x0264[2]	cmn_ropll_alone_mode	0x0	0x1	1'b0: Cascade mode/LCPLL mode 1'b1: ROPLL alone mode ROPLL alone mode should be used for RBR, HBR and HBR2 modes.
0x0C6C[7:0]	ln0_ana_tx_reserved	0x0	0x1	Transmitter setting
0x106C[7:0]	ln1_ana_tx_reserved	0x0	0x1	Transmitter setting
0x014C[7:0]	ln2_ana_tx_reserved	0x0	0x1	Transmitter setting
0x018C[7:0]	ln3_ana_tx_reserved	0x0	0x1	Transmitter setting
0x0C58[3:0]	ln0_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting
0x1058[3:0]	ln1_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting

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SFR Address	SFR Name	Default Value	Setting Value	Description
0x1458[3:0]	ln2_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting
0x1858[3:0]	ln3_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting
0x0C40[1:0]	ln0_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting
0x1040[1:0]	ln1_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting
0x1440[1:0]	ln2_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting
0x1840[1:0]	ln3_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting
0x0208[3:0]	ana_pll_cd_vreg_gain_ctrl	0x0	0x4	PLL setting
0x00F0[7]	ana_lcpll_reserved[7]	0x0	0x1	PLL setting
0x020C[6:5]	ana_pll_cd_vreg_ictrl	0x1	0x1	PLL setting
0x0214[1:0]	ana_pll_sync_loss_det_mode	0x0	0x3	PLL setting
0x0210[5]	pll_lcro_clk_sel	0x0	0x1	PLL setting
0x0268[0]	hs_speed_sel	0x0	0x1	Clock setting of o_tx_hs_clk 1'b0: Div20 clock output 1'b1: Div10 clock output
0x026C[4]	ls_speed_sel	0x0	0x1	Clock setting of o_tx_link_sym_clk 1'b0: Div40/Div36 clock output 1'b1: Div20/Div18 clock output
0x0C44[3]	ln0_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x0C44[2]	ln0_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting
0x0C44[1]	ln0_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x1044[3]	ln1_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x1044[2]	ln1_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting

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SFR Address	SFR Name	Default Value	Setting Value	Description
0x1044[1]	ln1_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x1444[3]	ln2_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x1444[2]	ln2_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting
0x1444[1]	ln2_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x1844[3]	ln3_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x1844[2]	ln3_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting
0x1844[1]	ln3_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x0264[7:6]	ssc_en	0x0	0x2	PLL Setting
0x081C[3:0]	lane_en	0x0	0xF or 0x3 or 0x1	lane_en[0]: 1'b0: Disables lane 0 1'b1: Enables lane 0 lane_en[1]: 1'b0: Disables lane 1 1'b1: Enables lane 1 lane_en[2]: 1'b0: Disables lane 2 1'b1: Enables lane 2 lane_en[3]: 1'b0: Disables lane 3 1'b1: Enables lane 3

25.6.2.4 PHY Power-Off Setting

Bring down all the PHY enables and assert the PHY resets.

Table 25-7 Power-Off setting

SFR Address	SFR Name	Default Value	Setting Value	Description
0x081C[3:0]	lane_en	0x0	0x0	lane_en[0]: 1'b0: Disables lane 0 1'b1: Enables lane 0 lane_en[1]: 1'b0: Disables lane 1 1'b1: Enables lane 1 lane_en[2]: 1'b0: Disables lane 2 1'b1: Enables lane 2 lane_en[3]: 1'b0: Disables lane 3 1'b1: Enables lane 3
0x027C[7:6]	pcs_bias_en	0x0	0xaa	Disable bias, init, cmn and lane rstn

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SFR Address	SFR Name	Default Value	Setting Value	Description
	pcs_init_rstn pcs_cmn_rstn pcs_lane_rstn			
0x0280[6:5]	pcs_pll_en	0x0	0x2	Disable PLL
Assert APB reset				

25.6.2.5 PHY Change Setting Flow

For RBR/HBR/HBR2 rates, the registers 0x0254[1:0], 0x0144, 0x0148, 0x014c, 0x0154, 0x0158, 0x015c, 0x0168, 0x016c, 0x0180, 0x0184, 0x0188, 0x0190, 0x0194, 0x0198, 0x019c, 0x01b0, 0x01b4, 0x01b8, 0x01c0, 0x01c4, 0x01c8 should be set correctly. For 1/2/4 lane, the registers 0x081C[3:0] should be set correctly. All the register above can be seen in chapter PHY Main Link Setting. Please look for it for the details.

If want to change PHY's setting, please power down the PHY according to chapter PHY Power-Off Setting. After PHY is power-off, change the SFR settings and bring up PHY as chapter Start-Up Sequence for PHY.

25.6.2.6 PHY Voltage-Swing and Pre-Emphasis setting

The Voltage-Swing and Pre-Emphasis can be adjusted in this table.

Table 25-8 Voltage Swing and Pre-emphasis Level

	Pre-emphasis level 0	**Pre-emphasis level1**	**Pre-emphasis level 2**	**Pre-emphasis level 3**
Voltage swing level 0	lane_reg0303 =0x22 lane_reg0304 =0x10	lane_reg0303 =0x25 lane_reg0304 =0x13	lane_reg0303 =0x29 lane_reg0304 =0x17	lane_reg0303 =0x2d lane_reg0304 =0x1c
Voltage swing level 1	lane_reg0303 =0x25 lane_reg0304 =0x10	lane_reg0303 =0x2a lane_reg0304 =0x15	lane_reg0303 =0x2d lane_reg0304 =0x19	Not supported
Voltage swing level 2	lane_reg0303 =0x28 lane_reg0304 =0x10	lane_reg0303 =0x2d lane_reg0304 =0x16	Not supported	Not supported
Voltage swing level 3	lane_reg0303 =0x2d lane_reg0304 =0x10	Not supported	Not supported	Not supported

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Chapter 26 UFS

26.1 Overview

UFS Host implements the Universal Flash Storage(UFS) interface for physical storage devices.

UFS Host supports the following features:

- Supports the following UFS2.0 features
- Higher speed up to HS-G3 (High-Speed Gear 3)
- Symmetric 2RX-2TX lanes
- Auto-hibernate entry and exit sequence
- 32-bit AXI slave interface for system host programming access
- 64-bit AXI master interface for DMA controlled data transfer

26.2 Block Diagram

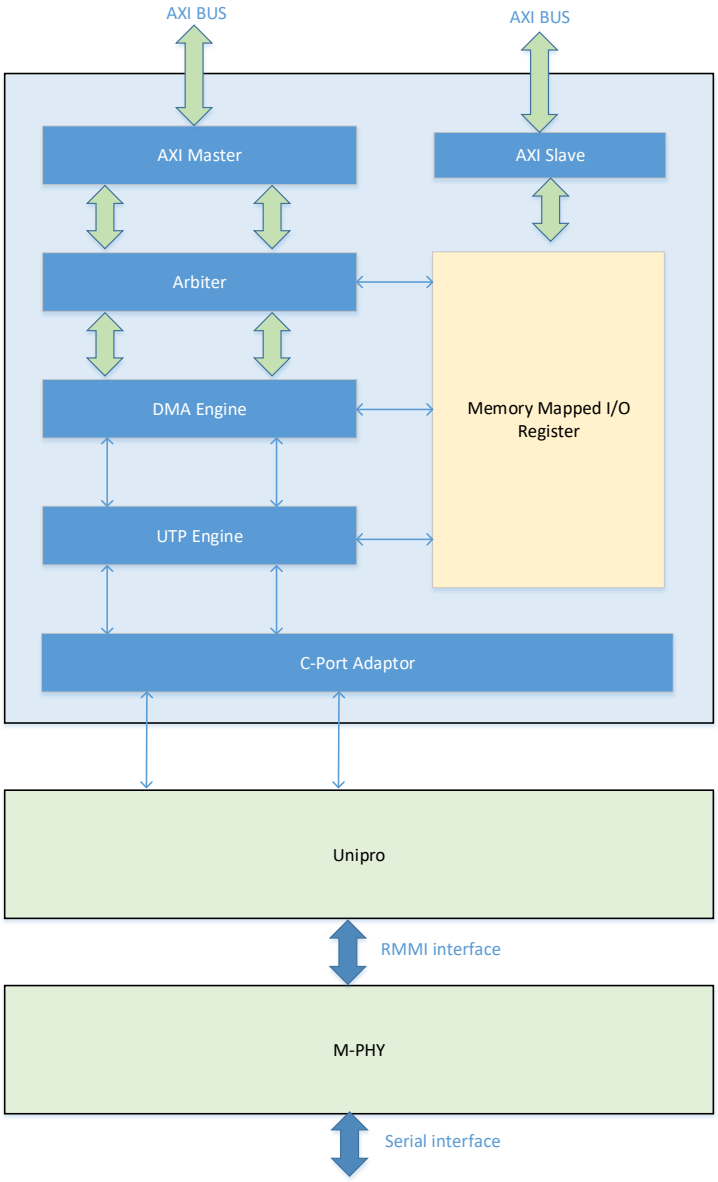


Fig. 26-1 UFS Block Diagram

26.3 Function Description

26.3.1 Memory Mapped I/O Register

The Memory Mapped I/O (MMIO) registers holds all the configuration data and provides a register layout which is compliant to the UFS Host Controller Specification [UFSHCI]. The

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registers are connected by a native bus interface to the AXI Slave Interface and can be programmed with single beat access, or for consecutive addresses with bursts.

26.3.2 AXI Interface

There are two AXI interfaces:

- AXI Master - This interface enables the DMA engine to read and write to an AXI slave connected to AXI BIU.
- AXI Slave - This interface enables an AXI master to read and write through the AXI BIU to the UFS registers.

26.3.3 DMA Engine

The DMA Engine is responsible for moving data between two entities without any interaction with the system host. It also requests AXI bus access to the Arbiter module. The DMA Engine itself is like a resource that can be requested using a semaphore by the following modules:

- AXI Master interface
- UTP Engine
- C-Port Adaptor

These modules are also possible sources or sinks for data exchange.

26.3.4 UTP Engine

The UTP Engine is responsible for managing the UFS protocol between the UFS host controller and the external UFS device.

While UFS requests are sent to the UFS host controller core in a single command, they may trigger a series of UFS packets transferred between the host and external device. The UTP Engine provides several different functions:

- Managing low level UFS protocol between device and host
- Managing the response from the device and store the appropriate information in system memory for the driver level
- Triggering the DMA engine to fetch/store data
- Managing scatter/gather table and set up DMA engine accordingly
- Maximize throughput by intelligent pre-fetching, buffering and pre-configuration
- Minimize required bus bandwidth by reducing unnecessary bus activities

26.3.5 C-Port Adaptor

The C-Port Adapter interfaces to the C-Port interface of the UniPro stack and handles the C-Port protocol. It also performs the following functions:

- UPIU Encapsulation and Decapsulation in Mission Mode
- C-Port Debug Access
- Loopback Mode

26.3.6 Arbit

To deliver optimal performance, the host controller’s initiator interface needs to perform transactions on the system bus without adding additional delays. While the specific implementation of the AXI protocol mainly determine the available bandwidth on the system bus, the arbiter determines the order in which requests are being executed. Although not directly protocol related, the order also has impact on the available bandwidth of the system – especially in systems with a high latency to access the system memory. In those systems it is important to hide the latency introduced by the access time behind a series of similar requests. Those could be a block of read or write requests, or a request stream with alternating types, for example, read followed by write, followed by read, and so on.

While on one side the arbiter is connected to the initiator interface, on the other side the interface is connected to five different internal clients. The arbiter manages based on priority and bandwidth requirements on the access to the system bus. Additionally there is one high priority request coming from one of the clients. The internal clients and the resulting requests are based on the internal architecture and the functionality the IP needs to perform.

26.3.7 UniPro

UniPro is for JEDEC UFS host/device application. lt is compliant with MIPI UniPro v1 .61 standard specification.

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The UniPro supports the following features:

- PMC
- PA_INIT(auto recovery sequence)
- Hibernate
- TX/RX preemption
- PEER_GET/PEER_SET
- Multilane up to two lanes for each direction
- LLM
- Data scrambling
- Skip symbol insertion/removal
- PHY test mode
- UniPro test feature
- Register configuration through APB3 slave
- Compatible with RMMI in MIPI M-PHY standard specification
- Compatible with CPort interface in MIPI UniPro specification
- Compliant with MIPI UniPro v1.61 standard specification
- PMC up to HS-G3

26.4 Register Description

26.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

26.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
UFSHC_CAP	0x0000	W	0x0187011F	Host Controller Capabilities. This register describes the basic capabilities of the ufshc core.
UFSHC_VER	0x0008	W	0x00000200	UFS Version. This register indicates the major and minor version of the UFSHCI specification that the ufshc implementation supports. The upper two bytes represent the major version number, and the lower two bytes represent the minor version number.
UFSHC_HCPID	0x0010	W	0x00000000	Host Controller Identification Descriptor - Product ID.
UFSHC_HCMID	0x0014	W	0x000005E6	Host Controller Identification Descriptor - Manufacturer ID.
UFSHC_AHIT	0x0018	W	0x00000000	Auto-Hibernate Idle Timer.
UFSHC_IS	0x0020	W	0x00000000	Interrupt Status. This register indicates pending interrupts that require service by the low-level driver firmware.

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Name	Offset	Size	Reset Value	Description
UFSHC_IE	0x0024	W	0x00000000	Interrupt Enable. This register enables and disables the reporting of the corresponding interrupt to host software. When a bit is set ('1') and the corresponding interrupt condition is active, then an interrupt is generated. Interrupt sources that are disabled ('0') are still indicated in the IS register. The register bit assignment matches with the IS register.
UFSHC_HCS	0x0030	W	0x00000000	Host Controller Status.
UFSHC_HCE	0x0034	W	0x00000000	Host controller enable.
UFSHC_UECPA	0x0038	W	0x00000000	Host Controller UIC Error Code PHY Adapter Layer. Register content is automatically cleared after reading.
UFSHC_UECDL	0x003C	W	0x00000000	Host UIC Error Code Data Link Layer. Register content is automatically cleared after reading.
UFSHC_UECN	0x0040	W	0x00000000	Host UIC Error Code Network Layer. Register content is automatically cleared after reading.
UFSHC_UECT	0x0044	W	0x00000000	Host UIC Error Code Transport Layer. Register content is automatically cleared after reading.
UFSHC_UECDME	0x0048	W	0x00000000	Host UIC Error Code DME. The UECDME register is reserved for future use and is fixed to 00000000h. Register content is automatically cleared after reading.
UFSHC_UTRIACR	0x004C	W	0x00000000	UTP Transfer Request Interrupt Aggregation Control Register.
UFSHC_UTRLBA	0x0050	W	0x00000000	UTP transfer request list base address.
UFSHC_UTRLBAU	0x0054	W	0x00000000	UTP Transfer Request List Base Address Upper 32-bits. This register controls the basic actions of the ufshc core. If the Master Address Width is 32, then the upper 32-bits of the base address are ignored and this register will be Read Only.
UFSHC_UTRLDBR	0x0058	W	0x00000000	UTP Transfer Request List Door Bell Register.
UFSHC_UTRLCLR	0x005C	W	0x00000000	UTP Transfer Request List Clear Register.

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Name	Offset	Size	Reset Value	Description
UFSHC_UTRLRSR	0x0060	W	0x00000000	UTP Transfer Request List Run Stop Register. This register controls the command processing of the ufshc core.
UFSHC_UTMRLBA	0x0070	W	0x00000000	UTP Task Management Request List Base Address.
UFSHC_UTMRLBAU	0x0074	W	0x00000000	UTP Task Management Request List Base Address Upper 32-Bits. If the Master Address Width is 32, then the upper 32-bits of the base address are ignored and this register will be Read Only.
UFSHC_UTMRLDBR	0x0078	W	0x00000000	UTP Task Management Request List Door Bell Register.
UFSHC_UTMRLCLR	0x007C	W	0x00000000	UTP Task Management Request List Clear Register.
UFSHC_UTMRLRSR	0x0080	W	0x00000000	UTP Task Management Request List Run Stop Register.
UFSHC_UICCMD	0x0090	W	0x00000000	UIC Command. Sending the DME_ENABLE UIC command is not allowed because this is done automatically during the ufshc initialization. See the HCS register for prerequisites to send UIC commands.
UFSHC_UICCMDARG1	0x0094	W	0x00000000	UIC Command Argument 1.
UFSHC_UICCMDARG2	0x0098	W	0x00000000	UIC Command Argument 2.
UFSHC_UICCMDARG3	0x009C	W	0x00000000	UIC Command Argument 3.
UFSHC_BUSTHRTL	0x00C0	W	0x002D7000	Bus Throttling. If there is heavy data traffic, the ufshc core may not leave sufficient bandwidth of the system bus for another peripheral. This register allows you to throttle the ufshc core either by limiting the number of outstanding read requests on the system bus or by specifying a minimum delay between two consecutive system bus accesses.
UFSHC_OOCPR	0x00C4	W	0x00000000	Outstanding OCP Requests. This register is not supported and is reserved in AXI configurations.
UFSHC_FEIE	0x00C8	W	0x00000000	Fatal Error Interrupt Enable. This register enables and disables the reporting of the corresponding Fatal interrupt to host software. When a bit is set ('1') and the corresponding Fatal Error interrupt condition is active, then Fatal interrupt is generated. Interrupt sources that are disabled ('0') are still indicated in the IS register. The register bit assignment matches with the IE register.

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Name	Offset	Size	Reset Value	Description
UFSHC_CDACFG	0x00D0	W	0x00000000	C-Port Direct Access Configuration register. This register configures and manages the basic functionality of the C-Port direct access configuration feature.
UFSHC_CDATX1	0x00D4	W	0x00000000	C-Port Direct Access Transmit 1 (D4h) register. This register takes the lower 32 bit of the 64-bit data word to be transferred. Because the UIC layer follows big endian byte order, CDATX1 and CDATX2 also follow big endian byte order.
UFSHC_CDATX2	0x00D8	W	0x00000000	C-Port Direct Access Transmit 2 (D8h) Register. This register takes the upper 32 bit of the 64-bit data word to be transferred. Writing to this address pushes the data to the UniPro adapter. Because the UIC layer follows big endian byte order, CDATX1 and CDATX2 also follow big endian byte order.
UFSHC_CDARX1	0x00DC	W	0x00000000	C-Port Direct Access Receive 1 (DCh) register. This register takes the lower 32 bit of the received 64-bit data word. Because the UIC layer follows big endian byte order, CDARX1 and CDARX2 also follow big endian byte order.
UFSHC_CDARX2	0x00E0	W	0x00000000	C-Port Direct Access Receive 2 (E0h) register. This register takes the upper 32 bit of the received 64-bit data word. Because the UIC layer follows big endian byte order, CDARX1 and CDARX2 also follow big endian byte order.
UFSHC_CDASTA	0x00E4	W	0x00000000	C-Port Direct Access Status (E4h) register. This register contains status information related to the last transfer.
UFSHC_LBMCFG	0x00F0	W	0x00000800	UPIU Loopback Configuration (F0h) register. Default: 00000800h
UFSHC_LBMSTA	0x00F4	W	0x00000000	UPIU Loopback Status. Default: 00000000h
UFSHC_DBG	0x00F8	W	0x00000000	Debug register.
UFSHC_HCLKDIV	0x00FC	W	0x000000C8	HClk Divider register. Default: UFS_P_P_CLKDIV

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

26.4.3 Detail Registers Description

UFSHC_CAP

Address: Operational Base(0x2A2D0000) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	CAP_RSVD_31_29 CAP_RSVD_31_29 reserved for future use Value After Reset:0x0
28	RW	0x0	Reserved0 Reserved Field: Yes
27	RO	0x0	CAP_RSVD_27 CAP_RSVD_27 reserved for future use Value After Reset:0x0
26	RO	0x0	UICDMETMS UIC DME_TEST_MODE command supported (UICDMETMS). Indicates whether the host controller supports the UniProSM DME_TEST_MODE.req SAP primitive. Value After Reset:0x0
25	RO	0x0	OODDS Out of order data delivery supported (OODDS). Indicates whether the ufshc core supports out of order data delivery for UTP data transfer. 1: The ufshc core supports out of order data delivery from the target device. 0: The ufshc core does not support out of order data delivery from the target device. Value After Reset:0x0
24	RO	0x1	AS64 64-bit addressing supported (64AS). Indicates whether the host controller can access 64-bit data structures. 1: The ufshc core makes the 32-bit upper bits of the UTP Transfer Request List Base Address Upper 32-bit and UTP Task Management Request List Base Address Upper 32-bit, the PRD Base, and each PRD entry read/write. 0: These bits are read-only. The ufshc core treats these bits as 0. If UFSHC_MADDR_WIDTH = 32, then this field is set to 0. If UFSHC_MADDR_WIDTH = 64, then this field is set to 1. Value After Reset:0x1
23	RO	0x1	AUTOH8 Auto-hibernation support (AUTOH8). Indicates whether ufshc controller supports auto-hibernation. 0: Host controller does not support auto-hibernation. 1: Host controller supports auto-hibernation. Value After Reset:0x1
22:19	RO	0x0	CAP_RSVD_22_19 CAP_RSVD_22_19 reserved for future use Value After Reset:0x0
18:16	RO	0x7	NUTMRS Number of UTP Task Management Request Slots (NUTMRS). Zero-based value indicating the number of slots provided by the UTP Task Management Request List. A minimum of 1 and maximum of 8 slots may be supported. Value After Reset:0x7

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Bit	Attr	Reset Value	Description
15:8	RO	0x01	NORTTS Number of outstanding READY TO TRANSFER (RTT) requests supported (NORTT). Indicates the maximum number of outstanding RTTs which are supported by the host controller. Zero-based value indicates the maximum number of RTTs that can be outstanding on the host at a particular instance. A minimum of two RTTs are supported and maximum is implementation specific. Value After Reset:0x1
7:5	RO	0x0	CAP_RSVD_7_5 CAP_RSVD_7_5 reserved for future use Value After Reset:0x0
4:0	RO	0x1f	NUTRS Number of UTP Transfer Request Slots (NUTRS). Zero-based value indicating the number of slots provided by the UTP Transfer Request List. A minimum of 1 and maximum of 32 slots may be supported. Value After Reset:0x1f

UFSHC_VER

Address: Operational Base(0x2A2D0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	VER_RSVD_31_16 VER_RSVD_31_16 reserved for future use Value After Reset:0x0
15:8	RO	0x02	MJR Major Version Number (MJR): Major version in BCD format. Value After Reset:0x2
7:4	RO	0x0	MNR Minor Version Number (MNR): Minor version in BCD format. Value After Reset:0x0
3:0	RO	0x0	VS Version Suffix (VS): Version suffix in BCD format. Value After Reset:0x0

UFSHC_HCPID

Address: Operational Base(0x2A2D0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PID Product ID (PID). Product ID that the host controller manufacturer assigns for the host controller. PID is defined by the UFS_P_P_HCPID parameter. Value After Reset:0x0

UFSHC_HCMID

Address: Operational Base(0x2A2D0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	HCMID_RSVD_31_16 HCMID_RSVD_31_16 reserved for future use Value After Reset:0x0

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Bit	Attr	Reset Value	Description
15:8	RO	0x05	BI Bank index. This field contains an index value of the bank that contains the Manufacturer Identification Code. The BI value is equal to the number of the continuation fields that precede the MIC. BI is defined by the UFS_P_P_HCMID_BI parameter. Value After Reset:0x5
7:0	RO	0xe6	MIC Manufacturer ID Code. Manufacturer Identification code of the host controller. MIC is defined by the UFS_P_P_HCMID_MIC parameter. Value After Reset:0xe6

UFSHC_AHIT

Address: Operational Base(0x2A2D0000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	AHIT_RSVD_31_13 AHIT_RSVD_31_13 reserved for future use Value After Reset:0x0
12:10	RW	0x0	TS Timer scale (TS). 000: Value times 1 us 001: Value times 10 us 010: Value times 100 us 011: Value times 1 ms 100: Value times 10 ms 101: Value times 100 ms 110 - 111: reserved Value After Reset:0x0
9:0	RW	0x000	AH8ITV Auto-Hibern8 Idle Timer Value (AH8ITV). This is the timer for which the UFS subsystem must be idle before the UFS host controller may put the UniPro link into hibernate state autonomously. The idle timer value is multiplied by the indicated timer scale to yield an absolute timer value. The idle timer starts decrementing when all of the following conditions are satisfied: UTRLDBR=0 UTMRLDBR=0 No UIC command is outstanding The idle timer continues to decrement until it reaches zero or it is reloaded as a result of software access to one of host controller interface registers. When idle timer changes a non-zero to zero, the host controller puts the UniPro link into the hibernate state. The host controller reloads this value each time the UniPro link transitions out of the hibernate state. The software writes 0 to disable the auto-hibernate idle timer. Any non-zero value enables the auto-hibernate idle timer. The software access to any one of host controller interface registers automatically puts the UniPro link out of hibernate state. Value After Reset:0x0

UFSHC_IS

Address: Operational Base(0x2A2D0000) + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:18	RO	0x0000	IS_RSVD_31_18 IS_RSVD_31_18 reserved for future use Value After Reset:0x0
17	RW	0x0	SBFES System Bus Fatal Error Status (SBFES). Indicates that the ufshc core encountered a system bus error that it cannot recover from (such as a bad software pointer). When the error occurs, the ufshc core is stopped and both UTRRSR and UTMRRSR registers are cleared to 0 by the ufshc core. Value After Reset:0x0
16	RW	0x0	HCFES Host Controller Fatal Error Status (HCFES). Indicates that the ufshc core encountered a fatal error that it cannot recover from. When the error occurs, the ufshc core is stopped and both UTRRSR and UTMRRSR are cleared to 0 by the ufshc. If the error occurs, the host application must reset the ufshc core. Value After Reset:0x0
15:13	RO	0x0	IS_RSVD_15_13 IS_RSVD_15_13 reserved for future use Value After Reset:0x0
12	RW	0x0	UTPES UTP Error Status (UTPES). Indicates that the ufshc core encountered an error at UTP layer that it cannot recover from. When the error occurs, the ufshc core updates the UTP error code field within the Host Controller Status register. The host application must then handle the error condition. Value After Reset:0x0
11	RW	0x0	DFES Device Fatal Error Status (DFES). Indicates that the ufshc core encountered a fatal error from the device that it cannot recover from. When the error occurs, the ufshc core is stopped and both UTRLRSR and UTMRLRSR bits are cleared to 0 by the ufshc core. If the error occurs, the host application must reset the ufshc. Value After Reset:0x0
10	RW	0x0	UCCS UIC Command Completion Status (UCCS). The ufshc core sets this bit to 1 after completing a UIC command. Value After Reset:0x0
9	RW	0x0	UTMRCS UTP Task Management Request Completion Status (UTMRCS). The ufshc core sets this bit to 1 after completing a task management function. Value After Reset:0x0
8	RW	0x0	ULSS UIC Link Startup Status (ULSS). Indicates that Link start-up process has been initiated by the remote end of the Link. This bit corresponds to the UniPro DME_LINKSTARTUP.ind SAP primitive. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
7	RW	0x0	ULLS UIC Link Lost Status (ULLS). This indicates a condition where remote end is trying to re-establish a link and the link is lost. This bit corresponds to the UniPro DME_LINKLOST.ind SAP primitive. Value After Reset:0x0
6	RW	0x0	UHES UIC Hibernate Enter Status (UHES). Indicates that UniPro hibernate entering process is complete and the Link state is changed to the Hibernate state if the process is successful. The HCS.UPMCRS register bit indicates if the entry process is not successful. This bit corresponds to the UniPro DME_HIBERNATE_ENTER.ind SAP primitive. Value After Reset:0x0
5	RW	0x0	UHXS UIC Hibernate Exit Status (UHXS). Indicates that the Link has exited UniPro Hibernate state. The HCS.UPMCRS register bit indicates if the exit process is not successful. This bit corresponds to the UniPro DME_HIBERNATE_EXIT.ind SAP primitive. Value After Reset:0x0
4	RW	0x0	UPMS UIC Power Mode Status (UPMS). Indicates that the UniPro/PA/DL part of the power mode change is complete. The HCS.UPMCRS register bit indicates the power mode change status. This bit corresponds to the UniPro DME_POWERMODE.ind SAP primitive. Value After Reset:0x0
3	RW	0x0	UTMS UIC Test Mode Status (UTMS). Indicates that the peer UniPro stack has been set to a given UniPro test mode. This bit corresponds to the UniPro DME_TEST_MODE.ind SAP primitive. Value After Reset:0x0
2	RW	0x0	UE UIC Error (UE). Indicates that a layer in the UniPro stack has encountered an error condition. Register bit HCS.UEC indicates the error code for the condition. This bit corresponds to the UniPro DME_ERROR.ind SAP primitive. Value After Reset:0x0
1	RW	0x0	UDEPRI UIC DME_ENDPOINTRESET Indication (UDEPRI). Indicates that the attached device has issued an DME_ENDPOINTRESET indication which is not allowed. Value After Reset:0x0
0	RW	0x0	UTRCS UTP Transfer Request Completion Status (UTRCS). The ufshc core sets this bit to when one of the following events occur: Completion of a UTP transfer request with its UTRD Interrupt bit set to 1. Interrupt caused by the UTR interrupt aggregation logic. Value After Reset:0x0

UFSHC_IE

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Address: Operational Base(0x2A2D0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	IE_RSVD_31_18 IE_RSVD_31_18 reserved for future use Value After Reset:0x0
17	RW	0x0	SBFEE System Bus Fatal Error Enable (SBFEE). When set and IS.SBFES is set, the ufshc core generates an interrupt. Value After Reset:0x0
16	RW	0x0	HCFEE Host Controller Fatal Error Enable (HCFEE). When set and IS.HCFES is set, the ufshc core generates an interrupt. Value After Reset:0x0
15:13	RO	0x0	IE_RSVD_15_13 IE_RSVD_15_13 reserved for future use Value After Reset:0x0
12	RW	0x0	UTPEE UTP Error Enable (UTPEE). When set and IS.UTPES is set, the ufshc core generates an interrupt. Value After Reset:0x0
11	RW	0x0	DFEE Device Fatal Error Enable (DFEE). When set and IS.DFES is set, the ufshc core generates an interrupt. Value After Reset:0x0
10	RW	0x0	UCCE UIC COMMAND Completion Enable (UCCE). When set and IS.UCCS is set, the ufshc core generates an interrupt. Value After Reset:0x0
9	RW	0x0	UTMRCE UTP Task Management Request Completion Enable (UTMRCE). When set and IS.UTMRCS is set, the ufshc core generates an interrupt. Value After Reset:0x0
8	RW	0x0	ULSSE UIC Link Startup Status Enable (ULSSE). When set and IS.ULSS is set, the ufshc core generates an interrupt. Value After Reset:0x0
7	RW	0x0	ULLSE UIC Link Lost Status Enable (ULLSE). When set and IS.ULLS is set, the ufshc core generates an interrupt. Value After Reset:0x0
6	RW	0x0	UHESE UIC Hibernate Enter Status Enable (UHESE). When set and IS.UHES is set, the ufshc core generates an interrupt. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
5	RW	0x0	UHXSE UIC Hibernate Exit Status Enable (UHXSE). When set and IS.UHXS is set, the ufshc core generates an interrupt. Value After Reset:0x0
4	RW	0x0	UPMSE UIC Power Mode Status Enable (UPMSE). When set and IS.UPMS is set, the ufshc core generates an interrupt. Value After Reset:0x0
3	RW	0x0	UTMSE UIC Test Mode Status Enable (UTMSE). When set and IS.UTMS is set, the ufshc core generates an interrupt. Value After Reset:0x0
2	RW	0x0	UEE UIC Error Enable (UEE). When set and IS.UEE is set, the ufshc core generates an interrupt. Value After Reset:0x0
1	RW	0x0	UDEPRIE UIC DME_ENDPOINTRESET (UDEPRIE). When set and IS. UDEPRI is set, the ufshc core generates an interrupt. Value After Reset:0x0
0	RW	0x0	UTRCE UTP Transfer Request Completion Enable (UTRCE). When set and IS.UTRCS is set, the ufshc core generates an interrupt. Value After Reset:0x0

UFSHC_HCS

Address: Operational Base(0x2A2D0000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	TLUNUTPE Target LUN of UTP error (TLUNUTPE). The LUN of the command that a UTP error occurs during execution of the command. This field is valid only when UTPES is set. The ufshc core automatically resets this bit when UTPES is cleared. Value After Reset:0x0
23:16	RO	0x00	TTAGUTPE Task Tag of UTP error (TTAGUTPE). The Task Tag of the command that a UTP error occurs during execution of the command. This field is valid only when UTPES is set. The ufshc core automatically resets this bit when UTPES is cleared. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
15:12	RO	0x0	UTPEC UTP Error Code (UTPEC). Indicates the error code of a UTP layer error. This field is valid only when UTPES is set. The ufshc core automatically resets this bit when UTPES is cleared. Value Description: 0h: Reserved 1h: Invalid transaction type 2h-Fh: Reserved Value After Reset:0x0
11	RO	0x0	HCS_RSVD_11 HCS_RSVD_11 reserved for future use Value After Reset:0x0
10:8	RO	0x0	UPMCRS UIC Power Mode Change Request Status (UPMCRS). Indicates the status of a UIC layer request for power mode change. Value Description 0h: PWR_OK. The request is accepted. 1h: PWR_LOCAL. The local request is successfully applied. 2h: PWR_REMOTE. The remote request is successfully applied. Not used because this is associated with a UIC power mode change request from the UFS Device, which is not permitted. 3h: PWR_BUSY. The request is aborted because of concurrent requests. Not used because this is associated with a UIC power mode change request from the UFS Device, which is not permitted. 4h: PWR_ERROR_CAP. The request is rejected because the requested configuration exceeded the Link's capabilities. 5h: PWR_FATAL_ERROR. The request is aborted because of a communication problem. The Link may not be operable. 6h - 7h: Reserved Value After Reset:0x0
7:4	RO	0x0	HCS_RSVD_7_4 HCS_RSVD_7_4 reserved for future use Value After Reset:0x0
3	RO	0x0	UCRDY UIC COMMAND Ready (UCRDY). Indicates whether the ufshc core is ready to process the UIC COMMAND. The host application must only set UICCMD if HCS.UCRDY is set to 1. This field is set to 1 if all the following conditions are true: IS.DFES == 0 IS.HCFES == 0 No UIC command is issued or the outstanding UIC command is complete (IS.UCCS == 1). The ufshc core clears this field to 0 when one of the following conditions occur: IS.DFES == 1 IS.HCFES == 1 A write access to the UICCMD register Value After Reset:0x0

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Bit	Attr	Reset Value	Description
2	RO	0x0	UTMRLRDY UTP Task Management Request List Ready (UTMRLRDY). This field is set to '1' if all of the following conditions are true: HCS.DP == 1 UTMRLDBR < FFh IS.DFES == 0 IS.HCFES == 0 The ufshc core clears this field to 0 when one of the following conditions occur: HCS.DP == 0 UTMRLDBR == FFh IS.DFES == 1 IS.HCFES == 1 The host application must only set the UTMRLRSR bit if HCS.UTMRLRDY is set to 1. Value After Reset:0x0
1	RO	0x0	UTRLRDY UTP Transfer Request List Ready (UTRLRDY). This field is set to '1' if all of the following conditions are true: HCS.DP == 1 UTRLDBR < FFFF_FFFFh IS.DFES == 0 IS.HCFES == 0 This field is cleared to '0' by the host controller when one of the following conditions occur: HCS.DP == 0 UTRLDBR == FFFF_FFFFh IS.DFES == 1 IS.HCFES == 1 The host application must only set the UTRLRSR bit to '1' if HCS.UTRLRDY is set to '1'. Value After Reset:0x0
0	RO	0x0	DP Device Present (DP). 1: A UFS device is attached to the ufshc core. 0: Non-volatile memory is not attached to the ufshc core. DP is set to 1 if the UIC layer is in the LinkUp power state. Value After Reset:0x0

UFSHC_HCE

Address: Operational Base(0x2A2D0000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	HCE_RSVD_31_1 HCE_RSVD_31_1 reserved for future use Value After Reset:0x0

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Bit	Attr	Reset Value	Description
0	RW	0x0	HCE Host Controller Enable (HCE). When set to 1, the ufshc core autonomously goes through the following initialization sequence: Warm hardware reset of the ufshc core DME_RESET DME_ENABLE The HCE bit stays 0 during the initialization sequence. If DME_ENABLE is not successful, HCE stays 0. If the initialization sequence is successful, HCE becomes 1. When HCE is cleared to 0, the ufshc core is disabled and register values except for the ufshc_map/ufshc_block/CAP are volatile and may lose their content. If HCE is 1 and a 0 is written to the HCE register, the HCE bit stays 1 until all outstanding OCP read requests are completed. Note : When UFSHC_STANDALONE is '1', BUSTHRTL.DME_CTRL_LOGIC_EN must be programmed to '1' for automatic issue of DME_RESET and DME_ENABLE. Value After Reset:0x0

UFSHC_UECPA

Address: Operational Base(0x2A2D0000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31	RO	0x0	ERR UIC PHY Adapter Layer Error (ERR). Indicates whether an error was generated by the PHY Adapter Layer Value After Reset:0x0
30:5	RO	0x0000000	UECPA_RSVD_30_5 UECPA_RSVD_30_5 reserved for future use Value After Reset:0x0
4:0	RO	0x00	EC UIC Adapter Layer Error (EC). Error code generated when IS.UE and UECPA.ERR are set to '1'. Bit Description: 00: PHY error on Lane 0 01: PHY error on Lane 1 02: PHY error on Lane 2 03: PHY error on Lane 3 04: Generic PHY Adapter error is flagged if there is a line reset that is initiated by either the local or the peer device. Value After Reset:0x0

UFSHC_UECDL

Address: Operational Base(0x2A2D0000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31	RO	0x0	ERR UIC Data Link Layer Error (ERR). Indicates whether an error is generated by the Data Link Layer. Value After Reset:0x0
30:15	RO	0x0000	UECDL_RSVD_30_15 UECDL_RSVD_30_15 reserved for future use Value After Reset:0x0

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Bit	Attr	Reset Value	Description
14:0	RO	0x0000	EC UIC Data Link Layer Error (EC). Error code generated when IS.UE and UECDL.ERR are set to '1'. For more information on the definitions of the error codes, see the UniPro Specification [UNIPRO]. Bit Description: 00: NAC_RECEIVED 01: TCx_REPLAY_TIMER_EXPIRED 02: AFCx_REQUEST_TIMER_EXPIRED 03: FCx_PROTECTION_TIMER_EXPIRED 04: CRC_ERROR 05: RX_BUFFER_OVERFLOW 06: MAX_FRAME_LENGTH_EXCEEDED 07: WRONG_SEQUENCE_NUMBER 08: AFC_FRAME_SYNTAX_ERROR 09: NAC_FRAME_SYNTAX_ERROR 10: EOF_SYNTAX_ERROR 11: FRAME_SYNTAX_ERROR 12: BAD_CTRL_SYMBOL_TYPE 13: PA_INIT_ERROR 14: PA_ERROR_IND_RECEIVED Value After Reset:0x0

UFSHC_UECN

Address: Operational Base(0x2A2D0000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31	RO	0x0	ERR UIC Network Layer Error (ERR). Indicates whether an error was generated by the Network Layer. Value After Reset:0x0
30:3	RO	0x0000000	UECN_RSVD_30_3 UECN_RSVD_30_3 reserved for future use Value After Reset:0x0
2:0	RO	0x0	EC UIC Network Layer Error Code (EC). Error code generated when IS.UE and UECN.ERR are set to '1'. For more information on the definitions of the error codes, see the UniPro Specification [UNIPRO]. Bit Description: 00: UNSUPPORTED_HEADER_TYPE 01: BAD_DEVICEID_ENC 02: LHDR_TRAP_PACKET_DROPPING Value After Reset:0x0

UFSHC_UECT

Address: Operational Base(0x2A2D0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31	RO	0x0	ERR UIC Transport Layer Error (ERR). Indicates whether an error was generated by the Transport Layer. Value After Reset:0x0
30:7	RO	0x000000	UECT_RSVD_30_7 UECT_RSVD_30_7 reserved for future use Value After Reset:0x0

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Bit	Attr	Reset Value	Description
6:0	RO	0x00	EC UIC Transport Layer Error Code (EC). Error code generated when IS.UE and UECT.ERR are set to '1'. For more information on the definitions of the error codes, see the UniPro Specification [UNIPRO]. Bit Description: 00: UNSUPPORTED_HEADER_TYPE 01: UNKNOWN_CPORTID 02: NO_CONNECTION_RX 03: CONTROLLED_SEGMENT_DROPPING 04: BAD_TC 05: E2E_CREDIT_OVERFLOW 06: SAFETY_VALVE_DROPPING Value After Reset:0x0

UFSHC_UECDME

Address: Operational Base(0x2A2D0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31	RO	0x0	ERR UIC DME Error (ERR). Indicates whether an error was generated by the DME Value After Reset:0x0
30:1	RO	0x00000000	UECDME_RSVD_30_1 UECDME_RSVD_30_1 reserved for future use Value After Reset:0x0
0	RO	0x0	EC UIC DME Error Code (EC). Error code generated when IS.UE and UECDME.ERR are set to '1'. Bit Description: 00: Generic DME error Value After Reset:0x0

UFSHC_UTRIACR

Address: Operational Base(0x2A2D0000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31	RW	0x0	IAEN Interrupt Aggregation Enable/Disable:. When set to '0' by the host application, command responses are not counted nor timed. Interrupts are still triggered by responses where the interrupt bit is set in the UTRD. When set to '1', the interrupt aggregation mechanism is enabled and aggregation-based interrupts are generated. Bit Description: 00: Disabled 01: Enabled Value After Reset:0x0
30:25	RO	0x00	UTRIACR_RSVD_30_25 UTRIACR_RSVD_30_25 reserved for future use Value After Reset:0x0

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Bit	Attr	Reset Value	Description
24	WO	0x0	IAPWEN Interrupt aggregation parameter write enable (IAPWEN). When the host application writes '1', the values in IACTH and IATOVAL are updated with the contents written at the same cycle. When the host application writes '0', the values in IACTH and IATOVAL are not updated. Note: Write operations to IACTH and IATOVAL are only allowed when no commands are outstanding. Value After Reset:0x0
23:21	RO	0x0	UTRIACR_RSVD_23_21 UTRIACR_RSVD_23_21 reserved for future use Value After Reset:0x0
20	RO	0x0	IASB Interrupt aggregation status bit (IASB). This bit indicates to the host application whether any responses have been received and counted towards interrupt aggregation (that is, IASB is set if IA counter is greater than 0). Bit Value Description: 0: No commands are received since the last counter reset (IA counter==0) 1: At least one command has been received and counted (IA counter >0) Value After Reset:0x0
19:17	RO	0x0	UTRIACR_RSVD_19_17 UTRIACR_RSVD_19_17 reserved for future use Value After Reset:0x0
16	WO	0x0	CTR Counter and Timer Reset (CTR). When the host application writes '1', the interrupt aggregation timer and counter are reset. It is recommended that the host application use this field to reset the timer and counter every time it services newly received UTP responses. Value After Reset:0x0
15:13	RO	0x0	UTRIACR_RSVD_15_13 UTRIACR_RSVD_15_13 reserved for future use Value After Reset:0x0
12:8	RW	0x00	IACTH Interrupt aggregation counter threshold (IACTH). The host application uses this field to configure the number of responses that are required to generate an interrupt. As UTP responses are received by the ufshc core, they are counted. When the count reaches the value configured in this field, an interrupt is generated (IS.UTRCS bit is set). The maximum allowed value is 31. When IACTH is 0, responses are not counted, and counting-based interrupts are not generated. In order to write to this field, the IAPWEN bit must be set at the same write operation. QUERY RESPONSE UPIUs and NOP IN UPIUs are not counted by the Interrupt Aggregation logic. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	IATOVAL Interrupt aggregation timeout value (IATOVAL). The host application uses this field to configure the maximum time allowed between a response arrival to the ufshc core and the generation of an interrupt. Timer Operation: The timer is reset by the application during the interrupt service routine. It starts running when the ufshc core receives the first response to a Regular Command, after the timer is reset. The timer stops when it reaches the value configured in IATOVAL field, and IS.UTRCS bit is set. When IATOVAL is 0, the timer does not run, and timer-based interrupts are not generated. The Time units in this field are 40 us. Therefore, writing 0x01 represents a time-out value of 40 us, and writing 0xFF represents a time-out value of 10.2 ms. QUERY RESPONSE UPIUs and NOP IN UPIUs are not counted by the Interrupt Aggregation logic. Value After Reset:0x0

UFSHC_UTRLBA

Address: Operational Base(0x2A2D0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	UTRLBA UTP Transfer Request List Base Address (UTRLBA). Indicates the 32-bit base physical address for the UTP Transfer Request list. This base is used when fetching commands for execution. The structure pointed to by this address range is 1KB in length. This address is 1KB aligned as indicated by bits 9:0 being read only. Value After Reset:0x0
9:0	RO	0x000	UTRLBA_RSVD_9_0 UTRLBA_RSVD_9_0 reserved for future use Value After Reset:0x0

UFSHC_UTRLBAU

Address: Operational Base(0x2A2D0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UTRLBAU UTP Transfer Request List Base Address Upper (UTRLBAU). Indicates the upper 32-bits for the UTP Transfer Request list base physical address. This base is used when fetching commands for execution. Value After Reset:0x0

UFSHC_UTRLDBR

Address: Operational Base(0x2A2D0000) + offset (0x0058)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UTRLDBR UTP Transfer Request List Door bell Register (UTRLDBR). This field is bit significant. Each bit corresponds to a slot in the UTP Transfer Request List, where bit 0 corresponds to request slot 0. A bit in this field is set to 1 by the host application to indicate to the ufshc core that a transfer request has been built in system memory for the associated transfer request slot and may be ready for execution. The host application indicates no change to request slots by setting the associated bits in this filed to '0'. Bits in this field must be set to 1 or 0 by the host application when UTRLRSR is set to '1'. When a transfer request is completed (with success or error), the corresponding bit is cleared to 0 by the ufshc core. The ufshc core always processes transfer requests in-order according to the order submitted to the list. If there are multiple commands with single door bell register ringing (batch mode), The dispatch order for these transfer requests by host controller will base on their index in the List. A transfer request with lower index value will be executed before a transfer request with higher index value. This field is also cleared when UTRLRSR is written from a '1' to a '0' by the host application. Value After Reset:0x0

UFSHC_UTRLCLR

Address: Operational Base(0x2A2D0000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	UTRLCLR UTP Transfer Request List CLear Register (UTRLCLR). This field is bit significant. Each bit corresponds to a slot in the UTP Transfer Request List, where bit 0 corresponds to request slot 0. A bit in this field is set to 0 by the host application to indicate to the ufshc core that a transfer request slot is cleared. The ufshc core frees up any resources associated to the request slot immediately, and sets the associated bit in UTRLDBR to 0. The host application indicates no change to request slots by setting the associated bits in this field to 1. Bits in this field must be set to '1' or 0 by the host application when UTRLRSR is set to 1. The host application must use this field only when a UTP Transfer Request is not expected to complete, for example, when a Transfer Request is aborted, or in case of a system bus error, such as an invalid UTRD. Value After Reset:0x0

UFSHC_UTRLRSR

Address: Operational Base(0x2A2D0000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UTRLRSR_RSVD_31_1 UTRLRSR_RSVD_31_1 reserved for future use Value After Reset:0x0

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Bit	Attr	Reset Value	Description
0	RW	0x0	UTRLRSR UTP Transfer Request List Run-Stop Register (UTRLRSR). When set to 1, the ufshc core may process the list. The ufshc core starts processing the list at entry 0. The ufshc core continues to process the list as long as this bit is set to 1. When cleared to 0, the ufshc core continues to complete all the outstanding transfer requests in the list and then stops. When cleared to 0, the ufshc core clears UTRLRDY to 0. This bit must be set to 1 when HCS.UCRDY and HCS.UTRLRDY and HCS.UTMRLRDY is set to 1. Value After Reset:0x0

UFSHC_UTMRLBA

Address: Operational Base(0x2A2D0000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	UTMRLBA UTP Task Management Request List Base Address (UTMRLBA). Indicates the 32-bit base physical address for the list. This base is used when fetching Task Management Functions for execution. The structure pointed to by this address range is 1KB in length. This address shall be 1KB aligned as indicated by bits 9:0 being read only. Value After Reset:0x0
9:0	RO	0x000	UTMRLBA_RSVD_9_0 UTMRLBA_RSVD_9_0 reserved for future use Value After Reset:0x0

UFSHC_UTMRLBAU

Address: Operational Base(0x2A2D0000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UTMRLBAU UTP Task Management Request List Base Address (UTMRLBAU). Indicates the upper 32-bits for the list base physical address. This base is used when fetching task management functions for execution. Value After Reset:0x0

UFSHC_UTMRLDBR

Address: Operational Base(0x2A2D0000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	UTMRLDBR_RSVD_31_8 UTMRLDBR_RSVD_31_8 reserved for future use Value After Reset:0x0

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	UTMRLDBR UTP Task Management Request List Door bell Register (UTMRLDBR). This field is bit significant. Each bit corresponds to a task management request slot in the List, where bit 0 corresponds to slot 0. The host application sets this field to indicate to the ufshc core that a task management request is built in system memory and may be ready for execution. When a task management request is completed (with success or error), the ufshc core clears the corresponding bit to 0. Bits in this field are only set to 1 by the host application when UTMRLRSR is set to 1. The ufshc core always processes task management request in order according to the order submitted to the list. If there are multiple requests with single door bell register ringing (batch mode), the dispatch order for these requests by ufshc core are based on their index in the List. A task management with lower index value is executed before a task management request with a higher index value. This bit is cleared when UTMRLRSR is written from '1' to '0' by the host application. Value After Reset:0x0

UFSHC_UTMRLCLR

Address: Operational Base(0x2A2D0000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	UTMRLCLR_RSVD_31_8 UTMRLCLR_RSVD_31_8 reserved for future use Value After Reset:0x0
7:0	WO	0x00	UTMRLCLR UTP Task Management List CLear Register (UTRLCLR). This field is bit significant. Each bit corresponds to a slot in the task management request List, where bit 0 corresponds to slot 0. A bit in this field is set to 0 by the host application to indicate to the ufshc core that a task management request slot is cleared. The ufshc core immediately frees up any resources associated to the task management request slot and sets the associated bit in UTMRLDBR to 0. The host application indicates no change to task management request slots by setting the associated bits in this field to 1. Bits in this field are only set to 1 or 0 by the host application when UTRLRSR is set to 1. The host application uses this field only when a UTP Task Management Request is not expected to complete (for example, if there is a system bus error, such as an invalid UTMRD). Value After Reset:0x0

UFSHC_UTMRLRSR

Address: Operational Base(0x2A2D0000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UTMRLRSR_RSVD_31_1 UTMRLRSR_RSVD_31_1 reserved for future use Value After Reset:0x0

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Bit	Attr	Reset Value	Description
0	RW	0x0	UTMRLRSR UTP Task Management Request List Run-Stop Register (UTMRLRSR). When set to 1, the ufshc core may process the list. The ufshc core starts processing the list at entry 0. The ufshc core continues to process the list as long as this bit is set to 1. When cleared to 0, the ufshc core continues to complete all outstanding task management requests in the list and then stops. When cleared to 0, the ufshc core clears UTMRLRDY to 0. This bit is only set to 1 when HCS.UTMRLRDY is set to 1. Value After Reset:0x0

UFSHC_UICCMD

Address: Operational Base(0x2A2D0000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	UICCMD_RSVD_31_8 UICCMD_RSVD_31_8 reserved for future use Value After Reset:0x0
7:0	RW	0x00	CMDOP Command Opcode (CMDOP). Indicates the Opcode of a UIC command to be dispatched to the local UIC layer. When this register is set, the ufshc core takes the values of UICCMDARGx as the corresponding parameters (input and output) that are a part of the UIC Command. Opcode UIC Commands Configuration: 01h: DME_GET 02h: DME_SET 03h: DME_PEER_GET 04h: DME_PEER_SET 05h - 0Fh: Reserved Control: 10h -11h: Reserved 12h: DME_ENABLE (not permitted) 13h: Reserved 14h: DME_RESET 15h: DME_ENDPOINTRESET 16h: DME_LINKSTARTUP 17h: DME_HIBERNATE_ENTER 18h: DME_HIBERNATE_EXIT 19h - FFh: Reserved Value After Reset:0x0

UFSHC_UICCMDARG1

Address: Operational Base(0x2A2D0000) + offset (0x0094)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ARG1 Argument 1(ARG1). This contains the value for the first argument of the UIC command if applicable. The contents of this field vary depending on the UIC Command (UICCMD). UIC Command = { Bit[31:24]/Bit[23:16], Bit[15:8]/Bit[7:0] } DME_GET = { MIBattribute, GenSelectorIndex} DME_SET = { MIBattribute, GenSelectorIndex } DME_PEER_GET = { MIBattribute, GenSelectorIndex } DME_PEER_SET = { MIBattribute, GenSelectorIndex } DME_ENABLE = { Reserved, N/A } DME_RESET = { Reserved, Reserved/ResetLevel } DME_ENDPOIBNTRESET = { Reserved, N/A } DME_LINKSTARTUP = { Reserved, N/A } DME_HIBERNATE_ENTER = { Reserved, N/A } DME_HIBERNATE_EXIT = { Reserved, N/A } MIBattribute: Indicates the ID of the attribute of the requested. For more information on the MIBattribute parameter, see the MIPI UniPro Specification version 1.40.00. GenSelectorIndex: Indicates the targeted M-PHY data lane or CPort or Test Feature when relevant. For more information on the GenSelectorIndex parameter see the MIPI UniPro Specification version 1.40.00. L1.5: Valid range is 0 to 2*PA_MaxDataLanes - 1 L4 / CPort: Valid range is 0 to T_NumCPorts - 1 L4 / Test Feature: Valid range is 0 to T_NumTestFeatures - 1 ResetLevel: Indicates the reset type. For more information on the ResetLevel parameter see the MIPI UniPro Specification version 1.40.00. 00h: Cold Reset 01h: Warm reset 02h-FFh: Reserved Value After Reset:0x0

UFSHC_UICCMDARG2

Address: Operational Base(0x2A2D0000) + offset (0x0098)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ARG2 Argument 2 (ARG2). This register contains the value for the second argument of the UIC command if applicable. The contents of this field vary depending on the UIC Command. UIC Command = { Bit[31:24], Bit[23:16], Bit[15:8 , Bit[7:0]} DME_GET = { Reserved, Reserved, Reserved, ConfigResultCode } DME_SET = { Reserved, AttrSetType, Reserved, ConfigResultCode } DME_PEER_GET = { Reserved, Reserved, Reserved, ConfigResultCode } DME_PEER_SET = { Reserved, AttrSetType, Reserved, ConfigResultCode } DME_ENABLE = { Reserved, GenericErrorCode } DME_RESET = { Reserved } DME_ENDPOIBNTRESET = { Reserved,,, GenericErrorCode } DME_LINKSTARTUP = { Reserved,,, GenericErrorCode } DME_HIBERNATE_ENTER = { Reserved,,, GenericErrorCode } DME_HIBERNATE_EXIT = { Reserved,,, GenericErrorCode } AttrSetType: Indicates whether the attribute value (AttrSet = NORMAL) or the attribute non-volatile reset value (STATIC) setting is requested. For more information on the AttrSetType parameter see the MIPI UniPro Specification version 1.40.00. ConfigResultCode: Indicates the result of the UIC configuration command request. It is valid after the ufshc core has set the IS.UCCS bit to 1. For more information on the ConfigResultCode parameter, see the MIPI UniPro Specification version 1.40.00. 00h: SUCCESS 01h: INVALID_MIB_ATTRIBUTE 02h: INVALID_MIB_ATTRIBUTE_VALUE 03h: READ_ONLY_MIB_ATTRIBUTE 04h: WRITE_ONLY_MIB_ATTRIBUTE 05h: BAD_INDEX 06h: LOCKED_MIB_ATTRIBUTE 07h: BAD_TEST_FEATURE_INDEX 08h: PEER_COMMUNICATION_FAILURE 09h: BUSY 0Ah: DME_FAILURE 0Bh-FFh: Reserved GenericErrorCode: Indicates the result of the UIC control command request. It is valid after the ufshc core sets the IS.UCCS bit to 1. For more information on the GenericErrorCode parameter, see the MIPI UniPro Specification version 1.40.00. 00h: SUCCESS 01h: FAILURE 02h-FFh: Reserved Value After Reset:0x0

UFSHC_UICCMDARG3

Address: Operational Base(0x2A2D0000) + offset (0x009C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ARG3 Argument 3 (ARG3). This register contains the value for the third argument of the UIC command if applicable. The contents of this field vary depending on the UIC Command. UIC Command = { Bit[31:24], Bit[23:16], Bit[15:8], Bit[7:0] } DME_GET = { MIBvalue_R } DME_SET = { MIBvalue_W } DME_PEER_GET = { MIBvalue_R } DME_PEER_SET = { MIBvalue_W } DME_ENABLE = { Reserved } DME_RESET = { Reserved } DME_ENDPOIBNTRESET = { Reserved } DME_LINKSTARTUP = { Reserved } DME_HIBERNATE_ENTER = { Reserved } DME_HIBERNATE_EXIT = { Reserved } MIBvalue_R: Indicates the value of the attribute as returned by the UIC command. It is valid after the ufshc core sets IS.UCCS to 1. For more information on the MIBvalue parameter, see the MIPI UniPro Specification version 1.40.00. MIBvalue_W: Indicates the value of the attribute to be set. For more information on the MIBvalue parameter, see the MIPI UniPro Specification version 1.40.00. Value After Reset:0x0

UFSHC_BUSTHRTL

Address: Operational Base(0x2A2D0000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	BUSTHRTL_RSVD_31_29 BUSTHRTL_RSVD_31_29 reserved for future use Value After Reset:0x0
28	RW	0x0	DME_CTRL_LOGIC_EN DME Control Logic Enable. Automatic issue of DME_RESET and DME_ENABLE during HCI initialization is - Disabled, when set to '0' - Enabled, when set to '1' Note 1: When UFSHC_STANDALONE = 0, this bit is fixed to '1' and cannot be modified by SW Note 2: Setting this bit to '1' in Standalone mode requires that all necessary DME Control Interface ports (LA_*Req, LA_*Cnf) are appropriately connected with the external Unipro module. Value After Reset:0x0
27:24	RO	0x0	BUSTHRTL_RSVD_27_24 BUSTHRTL_RSVD_27_24 reserved for future use Value After Reset:0x0

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Bit	Attr	Reset Value	Description
23:18	RW	0x0b	MAXOBUSR Maximum Outstanding Native Read Requests to System Bus Interface:. Actual limit of outstanding native read requests. This register value cannot be higher than the value specified by the P_P_WDP_MAX_OUTSTANDING parameter. Writing of illegal values is not checked or prohibited by the hardware. The default value is defined by the P_P_WDP_MAX_OUTSTANDING parameter, so that the application knows the maximum allowed value by reading this register. Value After Reset:0xb
17	RW	0x0	LP_AH8_PGE Low Power - AH8 Power Gating Enable. If this bit is set, all AH8 will be power gated. The default value of this bit is 1'b1. Value After Reset:0x0
16	RW	0x1	LP_PGE Low-Power Power Gating Enable. This bit should be set to enable power gated hibernates. Before programming Hibernate Entry, application should set this bit to enable power gating. If this bit is set, all application programmed Hibernates are power gated. The default value of this bit is 1'b1. Value After Reset:0x1
15:13	RW	0x3	MBL Maximum Burst Length Value. This register bits configures the maximum burst length value to the internal DMAs and the encoding is as follows: 3'b000 - Reserved 3'b001 - Maximum 4 beat burst 3'b010 - Maximum 8 beat burst 3'b011 - Maximum 16 beat burst 3'b100 - Maximum 32 beat burst 3'b101 - Maximum 64 beat burst 3'b110 - Maximum 128 beat burst 3'b111 - Maximum 256 beat burst The default value of this bit is 3'b011. Value After Reset:0x3
12	RW	0x1	CGE Clock Gating Enable. When set to '1' this bit enables the core to generate the ufs_idle_ind signal internally. The ufs_idle_ind port can be used to externally clock gate UFS host controller clock. The default value of this bit is 1'b1. Value After Reset:0x1
11:8	RW	0x0	Reserved0 Reserved Field: Yes
7:0	RW	0x00	BUSDLY Bus Delay. This register defines the minimum delay in HClk cycles between two requests to system bus from the native interface. Value After Reset:0x0

UFSHC_OOCPR

Address: Operational Base(0x2A2D0000) + offset (0x00C4)

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Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	OOCPR_RSVD_31_6 OOCPR_RSVD_31_6 reserved for future use Value After Reset:0x0
5:0	RO	0x00	OORR Outstanding OCP Requests. This register gives the number of outstanding OCP requests. If the system host writes a 0 to the HCE register, the ufshc core stays enabled (HCE=0) until all outstanding OCP requests are complete (OORR=0). Value After Reset:0x0

UFSHC_FEIE

Address: Operational Base(0x2A2D0000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	FEIE_RSVD_31_18 FEIE_RSVD_31_18 reserved for future use Value After Reset:0x0
17	RW	0x0	VSSBFEE Vendor Specific System Bus Fatal Error Enable (SBFEE). When set and IS.SBFES is set, the ufshc core generates UFSHC Fatal interrupt. Value After Reset:0x0
16	RW	0x0	VSHCFEE Vendor Specific Host Controller Fatal Error Enable (HCFEE). When set and IS.HCFES is set, the ufshc core generates UFSHC Fatal interrupt. Value After Reset:0x0
15:13	RO	0x0	FEIE_RSVD_15_13 FEIE_RSVD_15_13 reserved for future use Value After Reset:0x0
12	RW	0x0	VSUTPEE Vendor Specific UTP Error Enable (UTPEE). When set and IS.UTPES is set, the ufshc core does not generate UFSHC Fatal interrupt. Value After Reset:0x0
11	RW	0x0	VSDFEE Vendor Specific Device Fatal Error Enable (DFEE). When set and IS.DFES is set, the ufshc core generates UFSHC Fatal interrupt. Value After Reset:0x0
10	RW	0x0	VSUCCE Vendor Specific UIC COMMAND Completion Enable (UCCE). When set and IS.UCCS is set, the ufshc core does not generate UFSHC Fatal interrupt. Value After Reset:0x0
9	RW	0x0	VSUTMRCE Vendor Specific UTP Task Management Request Completion Enable (UTMRCE). When set and IS.UTMRCS is set, the ufshc core does not generate UFSHC Fatal interrupt. Value After Reset:0x0
8	RW	0x0	VSULSSE Vendor Specific UIC Link Startup Status Enable (ULSSE). When set and IS.ULSS is set, the ufshc core does not generate UFSHC Fatal interrupt. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
7	RW	0x0	VSULLSE Vendor Specific UIC Link Lost Status Enable (ULLSE). When set and IS.ULLS is set, the ufshc core does not generate UFSHC Fatal interrupt. Value After Reset:0x0
6	RW	0x0	VSUHESE Vendor Specific UIC Hibernate Enter Status Enable (UHESE). When set and IS.UHES is set, the ufshc core does not generate UFSHC Fatal interrupt. Value After Reset:0x0
5	RW	0x0	VSUHXSE Vendor Specific UIC Hibernate Exit Status Enable (UHXSE). When set and IS.UHXS is set, the ufshc core does not generate UFSHC Fatal interrupt. Value After Reset:0x0
4	RW	0x0	VSUPMSE Vendor Specific UIC Power Mode Status Enable (UPMSE). When set and IS.UPMS is set, the ufshc core does not generate UFSHC Fatal interrupt. Value After Reset:0x0
3	RW	0x0	VSUTMSE Vendor Specific UIC Test Mode Status Enable (UTMSE). When set and IS.UTMS is set, the ufshc core does not generate UFSHC Fatal interrupt. Value After Reset:0x0
2	RW	0x0	VSUEE Vendor Specific UIC Error Enable (UEE). When set and IS.UEE is set, the ufshc core does not generate UFSHC Fatal interrupt. Value After Reset:0x0
1	RW	0x0	VSUDEPRIE Vendor Specific UIC DME_ENDPOINTRESET (UDEPRIE). When set and IS. UDEPRI is set, the ufshc core does not generate UFSHC Fatal interrupt. Value After Reset:0x0
0	RW	0x0	VSUTRCE Vendor Specific UTP Transfer Request Completion Enable (VSUTRCE). When set and IS.UTRCS is set, the ufshc core does not generate UFSHC Fatal interrupt. Value After Reset:0x0

UFSHC_CDACFG

Address: Operational Base(0x2A2D0000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	CDACFG_RSVD_31_29 CDACFG_RSVD_31_29 reserved for future use Value After Reset:0x0
28	RW	0x0	CDAEN C-Port Direct Access Enable. This bit enables the direct access feature. Value After Reset:0x0
27:17	RO	0x000	CDACFG_RSVD_27_17 CDACFG_RSVD_27_17 reserved for future use Value After Reset:0x0

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Bit	Attr	Reset Value	Description
16	RW	0x0	CDAEOM C-Port Direct Access EOM. End of message indicator. Setting this bit forces the Host UniPro adapter to flush the message. Value After Reset:0x0
15:8	RW	0x00	CDABE C-Port Direct Access Byte Enables. Byte enables for the transmit data. Bit 15: CDATXB0 Bit 14: CDATXB1 Bit 13: CDATXB2 Bit 12: CDATXB3 Bit 11: CDATXB4 Bit 10: CDATXB5 Bit 9: CDATXB6 Bit 8: CDATXB7 If not all bytes carry valid payload, valid bytes must use the lower CDATXx byte fields. For example: Supported: CDABE = FCh Not supported: CDABE = CFh Value After Reset:0x0
7:0	RO	0x00	CDACFG_RSVD_7_0 CDACFG_RSVD_7_0 reserved for future use Value After Reset:0x0

UFSHC_CDATX1

Address: Operational Base(0x2A2D0000) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	CDATXB4 Write Data Byte 4 Value After Reset:0x0
23:16	RW	0x00	CDATXB5 Write Data Byte 5 Value After Reset:0x0
15:8	RW	0x00	CDATXB6 Write Data Byte 6 Value After Reset:0x0
7:0	RW	0x00	CDATXB7 Write Data Byte 7 Value After Reset:0x0

UFSHC_CDATX2

Address: Operational Base(0x2A2D0000) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	CDATXB0 Write Data Byte 0 Value After Reset:0x0
23:16	RW	0x00	CDATXB1 Write Data Byte 1 Value After Reset:0x0
15:8	RW	0x00	CDATXB2 Write Data Byte 2 Value After Reset:0x0

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	CDATXB3 Write Data Byte 3 Value After Reset:0x0

UFSHC_CDARX1

Address: Operational Base(0x2A2D0000) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	CDARXB4 Read Data Byte 4 Value After Reset:0x0
23:16	RW	0x00	CDARXB5 Read Data Byte 5 Value After Reset:0x0
15:8	RW	0x00	CDARXB6 Read Data Byte 6 Value After Reset:0x0
7:0	RW	0x00	CDARXB7 Read Data Byte 7 Value After Reset:0x0

UFSHC_CDARX2

Address: Operational Base(0x2A2D0000) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	CDARXB0 Read Data Byte 0 Value After Reset:0x0
23:16	RW	0x00	CDARXB1 Read Data Byte 1 Value After Reset:0x0
15:8	RW	0x00	CDARXB2 Read Data Byte 2 Value After Reset:0x0
7:0	RW	0x00	CDARXB3 Read Data Byte 3 Value After Reset:0x0

UFSHC_CDASTA

Address: Operational Base(0x2A2D0000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	CDASTA_RSVD_31_23 CDASTA_RSVD_31_23 reserved for future use Value After Reset:0x0
22:20	RO	0x0	CDARES C-Port Direct Access Result. Transmit result code. This field stores the result information from the last transmit operation. This field carries the TxResultCode from the UIC layer. It becomes valid one HClk cycle after the transfer is complete. 0: Access successful 1: Local CPort is not connected 2: Reserved. Not used for data transmission 3: Local CPort is not available 6: Peer device does not support selected TC 7: Message of 0 size rejected (EOM false) Value After Reset:0x0

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Bit	Attr	Reset Value	Description
19	RO	0x0	CDABUSY C-Port Direct Access Busy. This bit indicates whether the C-Port is busy. The application must poll this bit and make sure that the C-Port is available before any write access to the CDATX1 or CDATX2 registers. During data transmission, this bit is set to 1 until the transfer is completed. 0: C-Port available 1: C-Port busy Value After Reset:0x0
18	RO	0x0	CDASTA C-Port Direct Access Status. The status bit indicates if there is new data in the buffer. Value After Reset:0x0
17	RO	0x0	CDAEOM C-Port Direct Access EOM. End of message indicator. Value After Reset:0x0
16	RO	0x0	CDASOM C-Port Direct Access SOM. Start of message indicator. Value After Reset:0x0
15:8	RO	0x00	CDABE C-Port Direct Access Byte Enable. Byte enable settings for the received data. Value After Reset:0x0
7:0	RO	0x00	CDASTA_RSVD_7_0 CDASTA_RSVD_7_0 reserved for future use Value After Reset:0x0

UFSHC_LBMCFG

Address: Operational Base(0x2A2D0000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	LBMCFG_RSVD_31_20 LBMCFG_RSVD_31_20 reserved for future use Value After Reset:0x0
19:16	RW	0x0	BEP Byte Enable Pattern. This field defines the number of valid byte enables. The byte enables are filled up from MSB to LSB. This is for test mode only. For normal operation this field must be kept at the default value. 1: Byte 7 enabled 2: Byte 7:6 enabled 3: Byte 7:5 enabled 4: Byte 7:4 enabled 5: Byte 7:3 enabled 6: Byte 7:2 enabled 7: Byte 7:1 enabled Others: Byte 7:0 enabled Value After Reset:0x0

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Bit	Attr	Reset Value	Description
15	RW	0x0	BEPS Byte Enable Pattern Selection. This bit selects between a random byte enable pattern and a fixed byte enable pattern in 'read only' mode (LUN 0). In 'write only' and 'loopback mode' this field is ignored. The fixed byte enable pattern is taken from the BEP field of the LBMCFG register. This is for test mode only. For normal operation this field must be kept at the default value. 0b: Fixed byte enable pattern taken from BEP field 1b: Random byte enable pattern Value After Reset:0x0
14:11	RW	0x1	TRTLDV Throttle Divider Ratio. Because the bandwidth on the system bus may be much higher than actually supported by the UniPro link, this value allows to throttle the bandwidth in order to better mimic a real UFS Device. However, this causes some inaccuracy in performance measurement because the time to fill or empty the OCP buffer changes, which in turn influences the rate in which OCP requests to the bus fabric are issued. 0: Reserved 1-15: Divide the frequency in which data is requested from the OCP RX buffer and or stored in the OCP TX buffer. Value After Reset:0x1
10	RW	0x0	MRTTE Enable Multiple RTT Feature. Here multiple RTT will be submitted by the loopback logic. This feature tests the performance of back to back DATAOUT UPIUs. It provides feedback about the capabilities of the ufshc's RTT management capabilities. If DATAOUT UPIUs exceed a certain size (size depends on the access latency to the system memory), a second outstanding RTT may help reduce the latency between two consecutive DATAOUT UPIUs. This feature requires that a second RTT is sent to the ufshc core ahead of time. This enables the data management to fetch the data for the second RTT, while the data for the first RTT is still being sent over the UniPro link. Note: Data transfer happens in order, thus sending of data which belongs to the second RTT does not start before the first RTT is completely handled. The maximum number of outstanding RTT is two. Once the DATAOUT UPIUs for both RTTs have been transmitted, the next RTTs (2 or less) are issued until all data requested by the SCSI command are transferred. 0: Only one RTT 1: Up to two outstanding RTTs Value After Reset:0x0
9	RW	0x0	LBME Enable bit. Setting this bit decouples the UniPro layer from the ufshc logic and switches the input data stream to take packets from the loopback logic. If LBME=0, the UPIU loopback circuit is in reset. Inputs to the UniPro layer are assigned to fixed values. Value After Reset:0x0

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Bit	Attr	Reset Value	Description
8:5	RW	0x0	PDSIZE RTT Request Size. This value is a 4 bit field. It defines the amount of the data that is requested by the RTT. This mimics the ability of the UFS Device to limit the size of a DATAOUT UPIU. This field must be interpreted as the exponent of the function pow(2, PDSIZE+1). This allows sizes from 16 to 32768 bytes. Value After Reset:0x0
4	RW	0x0	USDLY Delay Period. This one bit field defines whether there is a delay before every RTT or DATAIN packet or just before the first one. Value After Reset:0x0
3:0	RW	0x0	UDLY Delay Length. This value is a 4 bit field and defines the delay (in clock cycles) from receiving the command till the response is sent back to the ufshc core. The response can either be an RTT UPIU or a DATAIN UPIU. This allows the ufshc core to fetch the required PRD entries and immediately continue processing the RTT or DATAIN UPIU. This field must be interpreted as the exponent of the function pow(2, UDLY+4). This allows delays from 16 to 524288 clock cycles ' which is approximately from 80ns to 2.6ms with a 200MHz clock. These large numbers mimic the real behavior of current devices. A value of zero will disable this feature meaning there is no delay. The USDLY field controls whether or not this delay is used for every return packet or just for the first one. Value After Reset:0x0

UFSHC_LBMSTA

Address: Operational Base(0x2A2D0000) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	LBMSTA_RSVD_31_1 LBMSTA_RSVD_31_1 reserved for future use Value After Reset:0x0
0	RW	0x0	ERR Indicates that there is general error. ERR=1 indicates that an error condition has been detected. Once an error condition is detected, the UPIU loopback circuit must be disabled and enabled again using the LBME bit. By this, the ERR register is cleared. Detectable error conditions: Command sent to unsupported LUN Unsupported command (Transaction Type) Value After Reset:0x0

UFSHC_DBG

Address: Operational Base(0x2A2D0000) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DBG Internal debug. This register is intended for Synopsys internal use only. 0: No error occurred Others: An error occurred Value After Reset:0x0

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UFSHC_HCLKDIV

Address: Operational Base(0x2A2D0000) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	HCLKDIV_RSVD_31_16 HCLKDIV_RSVD_31_16 reserved for future use Value After Reset:0x0
15:0	RW	0x00c8	HCLKDIV HCLKFrequency in MHz. HCLKDIV is used to generate 1usec tick signal used by Unipro. A maximum of +-10% variation is acceptable on this signal. 1uS = HCLKDIV * HCLK_Period For example, when HClk=200MHz then HCLKDIV=200. Value After Reset:0xc8

26.5 UFS_GRF Register Description

26.5.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

26.5.2 Registers Summary

Name	Offset	Size	Reset Value	Description
UFS_GRF_CLK_CTRL	0x0000	W	0x00000000	Clock Gate Logic Control
UFS_GRF_UIC_SRC_SEL	0x0004	W	0x00000000	UIC Command Source select
UFS_GRF_UFS_STATE_IE	0x0008	W	0x00000000	UFS_STATE Interrupt Enable
UFS_GRF_UFS_STATE_IS	0x000C	W	0x00000000	UFS_STATE Interrupt Enable
UFS_GRF_UFS_STATE	0x0010	W	0x00000000	ufs_idle_ind State

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

26.5.3 Detail Registers Description

UFS_GRF_CLK_CTRL

Address: Operational Base(0x2601F000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	WO	0x0	write_enable Write enable for lower 4 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	Hclk_CTRL Hclk Clock Gate Control. 1'b0: Auto gate the clock if no use 1'b1: Clock always on
2	RW	0x0	CG_Clk_CTRL CG_Clk Clock Gate Control. 1'b0: Auto gate the clock if no use 1'b1: Clock always on
1	RW	0x0	CG_pclk_CTRL CG_pclk Clock Gate Control. 1'b0: Auto gate the clock if no use 1'b1: Clock always on

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Bit	Attr	Reset Value	Description
0	RW	0x0	LP_Clk_T_CTRL LP_Clk_T Clock Gate Control. 1'b0: Auto gate the clock if no use 1'b1: Clock always on

UFS_GRF_UIC_SRC_SEL

Address: Operational Base(0x2601F000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	WO	0x0	write_enable Write enable for lower 1 bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	uic_src_sel UIC Command Source select. 1'b0: Use UFSHC Channel 1'b1: Use UNIPRO Channel

UFS_GRF_UFS_STATE_IE

Address: Operational Base(0x2601F000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	WO	0x0	write_enable Write enable for lower 2 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	idle_neg_dect_en UFSHC.idle_ind Negedge Detection Interrupt Enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_pos_dect_en UFSHC.idle_ind Posedge Detection Interrupt Enable. 1'b0: Disable 1'b1: Enable

UFS_GRF_UFS_STATE_IS

Address: Operational Base(0x2601F000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	WO	0x0	write_enable Write enable for lower 2 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	W1C	0x0	idle_neg_dect_is UFSHC.idle_ind Negedge Detection Interrupt.
0	W1C	0x0	idle_pos_dect_is UFSHC.idle_ind Posedge Detection Interrupt.

UFS_GRF_UFS_STATE

Address: Operational Base(0x2601F000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RO	0x0	ufs_state UFSHC.idle_ind State. 1'b0: Controller is Active 1'b1: Controller is Idle

26.6 Interface Description

Table 26-1 UFS Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
UFS_rstn	O	UFS_RSTN/GPIO4_D0_d	VCCIO7_IOC_GPIO4D_IOMUX_SEL_L[3:0]=1'b1
UFS_ref_clk	O	UFS_REFCLK/GPIO4_D1_d	VCCIO7_IOC_GPIO4D_IOMUX_SEL_L[7:4]=1'b1
UFS_rext	I/O	UFS_TX_REXT	
UFS_rx_d0n	I	UFS_RX_D0N	
UFS_rx_d1n	I	UFS_RX_D1N	
UFS_rx_d0p	I	UFS_RX_D0P	
UFS_rx_d1p	I	UFS_RX_D1P	
UFS_tx_d0n	O	UFS_TX_D0N	
UFS_tx_d1n	O	UFS_TX_D1N	
UFS_tx_d0p	O	UFS_TX_D0P	
UFS_tx_d1p	O	UFS_TX_D1P	

Notes: I=input, O=output, I/O=input/output, bidirectional

26.7 Application Notes

26.7.1 Software Model

This section provides details on the transactions, protocol elements and data structures that are used to control the UFSHC core, MIPI UniPro stack and external device. The transactions are built by the system hosts and send to UFSHC core through the UTP Transfer Request List, the UTP Task Management Request List, and the UTP Command Descriptors.

While some transactions are already prepared as UPIU packets by the host software, for some other transactions (mainly the transfer of the raw data), the UPIU packet need to be constructed first. The construction takes place on the fly in the UFSHC. The table below lists the UFSHC commands.

Table 26-2 UFSHC Commands

Command	Format	Action
UTP Command	UTP Transfer Request List	Send to device
DME Command	Register Access	Access UniPro Stack
Task Manager Command	UTP Task Management Request List	Send to device

To send commands to the UFSHC core, UniPro stack and UFS device, the system host must perform a serious of setup and configurations steps. The following list gives a brief summary on the necessary sequence.

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- Find an empty UTP Command Descriptors slot by reading the UTP Transfer Request Doorbell Register.
- Program the required transactions in the UTP Transfer Request List and depending on the transfer setup a UTP Command Descriptors entry.
- Now set up the appropriate bit in the Command and Service Issue Register.
- Start the UFSHC core by asserting the start bit in the Door Bell Register.

Now the UFSHC core starts processing the UTP Transfer Request List.

After the UFSHC core completes processing a command, it updates the status field in the UTP Transfer Request List or UTP Command Descriptors respectively.

UFS Transport Protocol (UTP) commands are commands based on UPIU packets. To set up the communication, both the transaction list as well as the command descriptors need to be programmed. UTP transactions come in the following flavors:
- Native UTP commands.
- SCSI-over-UFS commands.

26.7.2 UTP SCSI Transactions

This section provides a detailed overview of the SCSI commands implemented in the UTP protocol. To keep the implementation simple, the UFS Architecture Specification [UFS] has made only a subset of the SCSI commands available. Table below gives a brief overview about some of the implemented SCSI commands.

Table 26-3 Implemented SCSI Commands

Command	Description	Opcode
Inquiry	Report device information	12h
Mode Select	Set parameters, modes, and other such functions	55h
Mode Sense	Report parameter and other device information	5Ah
Read	Transfer data from host to device	28h
Read Capacity	Report medium capacity and block size	25h
Report LUNs	Report the accessible LUNs	5Ah
Start Stop Unit	Change power condition and load or eject	1Bh
Test Unit Ready	Test if device is ready	00h
Verify	Verify the medium	2Fh
Write	Transfer data to device	2Ah
Synchronize Cache	Store most recent device data to medium	35h

For the detailed list of commands, refer to Section 11.3 Universal Flash Storage SCSI Commands, in JESD220B specification.

26.7.3 Theory of Operation

The host application presents a list of commands to the UFSHC core. Independent from the system host, this list is then being processed by the host controller and the controller asserts an interrupt line in case a command finishes.

In order to post new commands to the UFSHC core, the system host needs to find empty slots in the command list. In case no empty slot is available, the host thread needs to wait until a command finishes and the driver software has made a new slot available.

Nevertheless, the UFSHC core monitors the UTRLDBR and UTMRLDBR registers to determine if there are commands ready to be processed. The processing order depends on the following factors:
- Time at which bits inside the UTRLDBR and UTMRLDBR registers have been asserted
- Index inside the UTRLDBR and UTMRLDBR registers
- Command type (UTP or Task Management)

The processing rules are as follows:
- Task Management commands have higher priority than UTP commands

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- Commands with lower time stamp have higher priority than commands with higher time stamps
- Within the same time stamp, commands with lower doorbell register index have higher priority than commands with a higher doorbell register index

While there is no indicator about active commands, it is not possible to know in advance when a particular command is being processed, or how the command will remain in the command list respectively.

To add an additional level of uncertainty, any UFS device is allowed to accept more than one command and is allowed to process those commands out-of-order. As a consequence, commands placed in the command list need to be robust enough to get arbitrarily re-ordered. In cases where this may cause problems, only one command at a time may be placed into the command list.

The following sections provide more detail around the low level driver to explain how the communication and data transfer is handled between the System Host, UFSHC core, and UFS Device.

26.7.3.1 Building a UTP Transaction

A command for the UFSHC core typically consists of a UTP Transfer Request List entry and a command table element. Thus, the host application needs to start by finding an empty slot inside the UTP Transfer Request List first.

Following are the basic steps for setting up the command list:

- Find an empty command list slot by reading the UTRLDBR, if there are no empty slots, wait and try again.
- If there is at least one empty slot, start setting up the UTP Transfer Request Descriptor.
  - Write CT: Define command type
  - Write DD: Define data direction
  - Write I: Define whether or not an interrupt has to be generated
  - Initialize OCS with the value 0Fh
- Allocate space inside the system memory for an UTP Command Descriptor
- Initialize Command UPIU field of the UTP Command Descriptor
  - Write TTY: Transaction type, here 01h
  - Write FL: Specific flags for this command
  - Write LUN: the SCSI address this command is directed to
  - Write TT: Task tag, a unique number to identify the task.
  - Write CST: Command set type, 0h for SCSI commands
  - Write TEL: Total EHS Length, always 0h
  - Write DSL: Data segment length, always 0h.
  - Write EDTL: Expected data transfer length. This field indicates the amount of data to be transferred between the initiator and target (read or write). Data is stored in system memory.
  - Write CDB: Write the SCSI command into the following 16bytes
- Initialize Response UPIU field of the UTP Command Descriptor with zero
- Initialize PRD field of the UTP Command Descriptor with the required data scatter/gather buffer information. The UTP Command Descriptor is now set up.
- Set up the UTP Transfer Request List Descriptor:
  - Write UCDBA: Base address of the UTP Command Descriptor
  - Write UCDBAU: Upper 32bit of the UCDBA, always 0h
  - Program field RUO with the offset (from the starting address of UCD) of Response UPIU within UCD.
  - Program field RUL with the length of Response UPIU.
  - Program field PRDTO with the offset (from the starting address of UCD) of the PRD table within UCD if required.
  - Program field PRDTL with the length of the PRD table if required.
- Repeat this procedure for all commands which need to be set up

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- Check the UTRLRSR register and make sure it is read '1' before continuing.
- Set UTP Transfer Request Interrupt Aggregation Control Register (UTRIACR) enable bit to '1' to enable the interrupt.
- Set Counter and Timer Reset (CTR) bit to '1' to reset the counter and timer associated with the interrupt.
- Program field Interrupt aggregation counter threshold (IACTH) with the number of command completions that are required to generate an interrupt.
- Program field Interrupt aggregation timeout value (IATOVAL) with the maximum time allowed between a response arrival to the host controller and the generation of an interrupt.
- Set UTRLDBR to ring the doorbell register to indicate to the host controller that one or more transfer requests are ready to be sent to the attached device. The host application must only write a '1' to the bit position that corresponding to the new command; All other bit positions within UTRLDBR should be written with a '0', which indicates no change to their current values.

The UFSHC core takes over and process the command list without further application interaction.

26.7.3.2 Processing Completed Transactions

Control is given back to the application by asserting the IS.UTRSC interrupt. This bit is set when at least one of the following conditions are met:

- The UTRD.I bit is set (Interrupt Command)
- The counter, after incrementing, reaches the value configured in IACTH
- The IA timer reaches the value configured in IATOVAL (this event may occur at any time, not necessarily coupled with request completion).

An interrupt is generated by the write operation if the completion interrupt is not masked (disabled) by the IE.UTRCE bit.

The host application processes the interrupt generated by the ufshc core for command completion. In the interrupt service routine, host software checks the IS register to determine if there is an interrupt pending. If the ufshc core has an interrupt pending:

- The host application determines the cause of the interrupt by reading the IS register. It is possible for multiple bits to be set.
- The host application clears appropriate bits in the IS register corresponding to the cause of the interrupt.
- The host application reads the UTRLDBR register, and compares the current value to the list of commands previously issued by host software that are still outstanding. Host software completes any outstanding command whose corresponding bit has been cleared in the respective register. UTRLDBR is a volatile register; software should only use its value to determine commands that have completed, not to determine which commands have previously been issued.
- If there are errors, noted in the IS register, the host application performs error recovery actions.

26.7.3.3 UFS Host Processing

Host processing of the commands initiated by the system host is done independent of the system host and software. The exact steps performed by the ufshc core can vary, but the baseline steps for a read/write operation are given below:

- The ufshc core reads the selected command list entry with one 4 beat burst.
- Depending on the command type, further actions are taken. In case the command is read/write:
  - The ufshc core fetches the first part of the UPIU (till the data segment) in 4 beat bursts. This brings the header information and the SCSI command into the controller.
  - The ufshc core reads the first PRD entry with a 2 beat burst.
  - Now the ufshc core sets up its internal data structure and variables.
  - To start the device communication, the ufshc core sends the already fetched UPIU

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packet to the device.

Now the device will initiate the data transfer phase by sending Ready-To-Transfer UPIUs to the host controller.

- The device either sends a RTT UPIU (in case of a write) or directly a Data-In UPIU (in case of a read). The size of the Data-In UPIU is not predefined.
- The host either sends back the requested data with a Data-Out UPIU, or takes the data and stores it in an internal buffer.

The above transactions between the host and the device are executed until all data is transferred or an error occurred.

In parallel to the transactions between the host and device, the data is transferred between the host controller and system memory.

- On receiving the Response UPIU, the ufshc core updates the Transfer Response field of the UTP Command Descriptor with the received UPIU.
- Once a command has been completed, an interrupt may be asserted to signal the system host that the transfer is done.

26.7.3.4 Response Management and Command Completion

Although not a command, the management of command completion, response management and error handling and can be considered to be related to the command interface.

There are essentially three steps to perform when a response UPIU arrives:

- Analyzing the packet
- Storing of the sense data which might be part of the response packet.
- Modifying the Response UPIU field in the related UPIU command table entry.

As a last step and depending on the command setup, the ufshc core sets the interrupt flag.

26.7.4 Command and Data Flow

This section provides detailed information about command data flow for every command supported by the UFSHC core.

26.7.4.1 Write Command

The figure provides an overview of a write operation.

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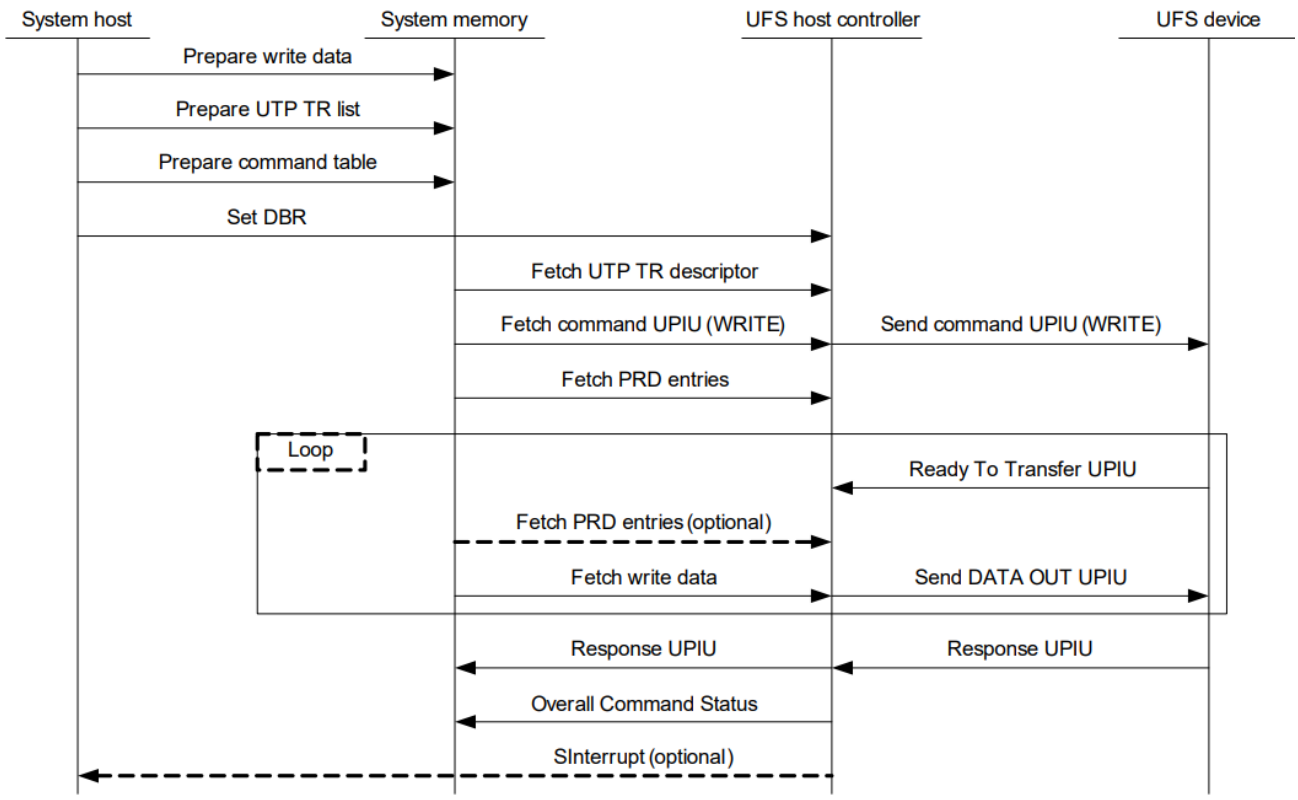


Fig. 26-2 Write Command Flow

26.7.4.2 Read Command

The figure provides an overview of a read operation.

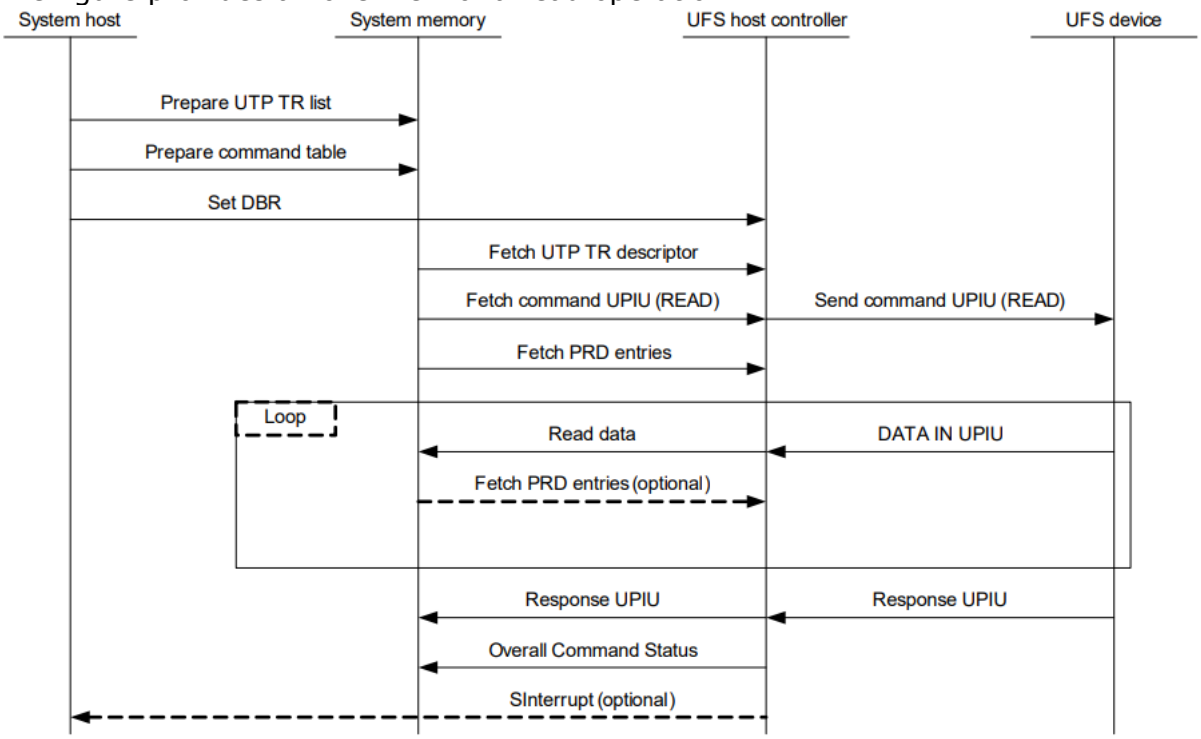


Fig. 26-3 Read Command Flow

26.7.4.3 Task Management

The figure provides an overview of a task management operation.

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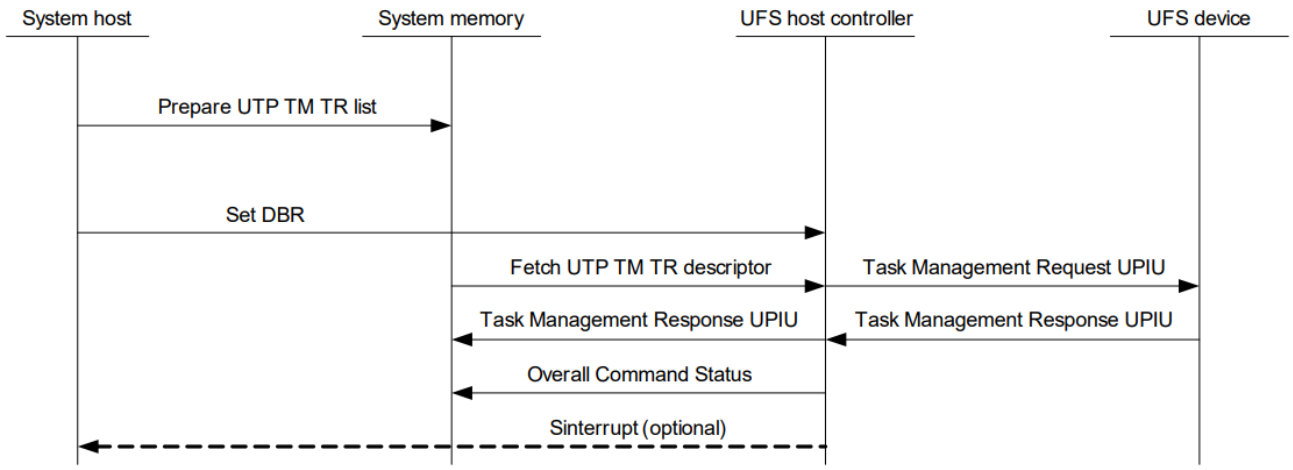


Fig. 26-4 Task Management Flow

26.7.4.4 Device Management

The figure provides an overview of a device management operation.

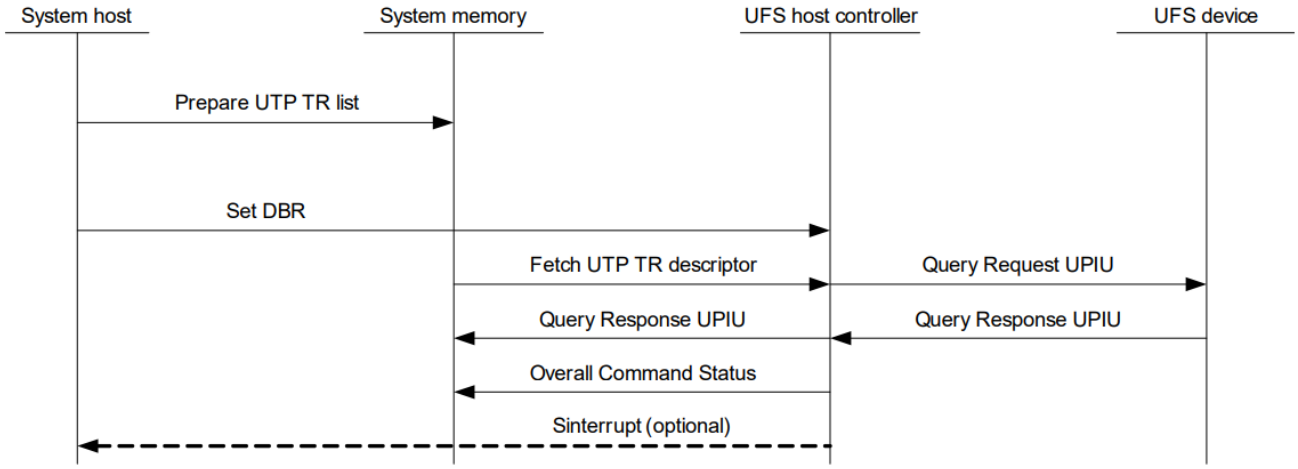


Fig. 26-5 Device Management Flow

26.7.4.5 UIC Command

The figure provides an overview of a UIC command operation.

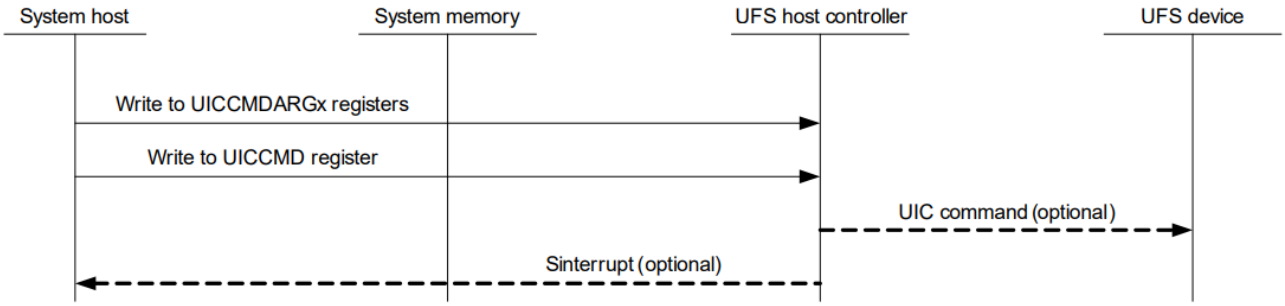


Fig. 26-6 UIC Command Flow

26.7.5 Initializing the UFSHC Core

Before using UFS, it needs to be initialized, so some configurations for Unipro and M-PHY need to be done through DME_SET.

- Assert Reset_n
- De-assert Reset_n and wait for at least 4 HClk cycles.
- Write 1 to the HCE register in order to enable the ufshc core. This triggers an autonomous basic initialization of the local UIC layer. The initialization sequence consists of a DME_RESET and a DME_ENABLE command. Further commands, such as DME_SET commands may be added, depending on the implementation needs. During the basic initialization sequence, the HCE is read as 0.
- Wait until HCE is read as '1' before continuing. This indicates that the basic initialization sequence is complete.
- DME_RESET()

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- DME_ENABLE()
- Initial Settings
  //DME_SET(MIB_ADDR, DATA, GEN_SEL)
  - DME_SET(0x155e, 0x0,0x0) // PA_Local_TX_LCC_Enable
  - DME_SET(0x200, 0x40,0x0) //Enable M-PHY DME_SET CFG
  - DME_SET(0xaa,0x6,0x0)
  - DME_SET(0xa9,0x6,0x0)
  - DME_SET(0xad,0x6,0x0)
  - DME_SET(0xac,0x6,0x0)
  - DME_SET(0xab,0x6,0x0)
  - DME_SET(0x94,0x6,0x0)
  - DME_SET(0x93,0x6,0x0)
  - DME_SET(0x7f,0x6,0x0)
  - DME_SET(0x12,0x6,0x4)
  - DME_SET(0x11,0x0,0x4)
  - DME_SET(0x1d,0x58,0x4)
  - DME_SET(0x1c,0x8c,0x4)
  - DME_SET(0x1b,0x2,0x4)
  - DME_SET(0x25,0xf6,0x4)
  - DME_SET(0x2f,0x69,0x4)
  - DME_SET(0xaa,0x6,0x1)
  - DME_SET(0xa9,0x6,0x1)
  - DME_SET(0xad,0x6,0x1)
  - DME_SET(0xac,0x6,0x1)
  - DME_SET(0xab,0x6,0x1)
  - DME_SET(0x94,0x6,0x1)
  - DME_SET(0x93,0x6,0x1)
  - DME_SET(0x7f,0x6,0x1)
  - DME_SET(0x12,0x6,0x5)
  - DME_SET(0x11,0x0,0x5)
  - DME_SET(0x1d,0x58,0x5)
  - DME_SET(0x1c,0x8c,0x5)
  - DME_SET(0x1b,0x2,0x5)
  - DME_SET(0x25,0xf6,0x5)
  - DME_SET(0x2f,0x69,0x5)
  - DME_SET(0x200, 0x0,0x0) //Disable M-PHY DME_SET CFG
- Initial Configuration Before Data Transfer
  - DME_SET(0xc022, 0x0,0x0) //T_DBG_CPORT_TX_ENDIAN
  - DME_SET(0xc023, 0x0,0x0) //T_DBG_CPORT_RX_ENDIAN
  - DME_SET(0x3000, 0x0,0x0) //N_DiviceID
  - DME_SET(0x3001, 0x1,0x0) //N_DiviceID_valid
  - DME_SET(0x4021, 0x1,0x0) //T_PeerDeviceID
  - DME_SET(0x4020, 0x1,0x0) //T_ConnectionState

26.7.6 Power Mode Change Trigger

Power mode change has a dedicated REQ register(DME_POWERMODE_REQ). After configuring the registers required for power mode change, this register needs to be configured to trigger the power mode change process.

- POWER_MODE_CHANGE Configuration
- DME_SET(0xd020,0x1,0x0) //DME_POWERMODE_REQ

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