



DATA SHEET

(DOC No. HX8399-C-DS)

HX8399-C_ GP

1080RGB x 2400 dot, 16.7M
color, LTPS Mobile Single Chip
Driver

Version 01 October, 2017

>> HX8399-C

1080RGB x 2400 dot, 16.7M color, LTPS
Mobile Single Chip Driver



Himax Technologies, Inc.
<http://www.himax.com.tw>

Revision History

October, 2017

Version	Date	Description of changes
01	2017/10/25	New Setup

Himax Confidential
Do Not Copy

» HX8399-C

1080RGB x 2400 dot, 16.7M color, LTPS
Mobile Single Chip Driver



Himax Technologies, Inc.
<http://www.himax.com.tw>

List of Contents

October, 2017

1. General Description	11
2. Features	12
2.1 Display	12
2.2 Display module	12
2.3 Support Power Mode	13
2.4 Display / Control interface	13
2.5 Input power	13
2.6 Miscellaneous	13
3. Device Overview	14
3.1 Block diagram	14
3.2 Pin description	15
4. Interface	19
4.1 System interface	19
4.2 Serial data transfer interface (MIPI DBI Type-C)	20
4.2.1 Serial data write mode	20
4.2.2 Serial data read mode	22
4.3 I2C interface	23
4.3.1 I2C protocol	23
4.3.2 I2C slave address	24
4.3.3 I2C interface write mode	25
4.3.4 I2C interface read mode	26
4.4 DSI system interface	27
4.4.1 DSI layer definitions	28
4.4.2 DSI protocol	39
4.4.3 Processor to peripheral direction packets data types	42
4.4.4 Peripheral to processor (reverse direction)	49
5. Function Description	51
5.1 Tearing effect output line	51
5.1.1 Tearing effect line timing	53
5.2 Oscillator	54
5.3 Source driver	55
5.4 LCD power generation scheme	60
5.5 DC/DC converter circuit	62
5.5.1 Charge pump and step up circuit mode	62
5.5.2 Use HX5186- C	63
5.5.3 Use PFM DC/DC converter	64
5.5.4 Use external VSP and VSN circuit	67
5.5.5 Use external VSP and VSN and VDD3 circuit	68
5.5.6 Use external VSP, VSN, VGH and VGL circuit	69
5.6 Idle display	70
5.7 Gamma characteristic correction function	71
5.7.1 Gamma characteristics adjustment register	73
5.8 Gray voltage generator for digital gamma correction	89
5.9 Characteristics of I/O	91
5.9.1 Output or bi-directional (I/O) pins	91
5.9.2 Input pins	91
5.10 Sleep Out-command and self-diagnostic functions of the display module	92
5.10.1 Register loading detection	92
5.10.2 Functionality detection	93
5.11 Power on/off sequence	94
5.11.1 VDD3/VDD1 input power (PCCS[2:0]=000, 001, 101)	95
5.11.2 VSP/VDD1 input power (PCCS[2:0]=010)	96
5.11.3 VSP/VSN/VDD1 input power (PCCS[2:0]=011)	97
5.11.4 VDD3/VSP/VSN/VDD1 input power (PCCS[2:0]=111)	98
5.11.5 VSP/VSN/VGH/VGL/VDD1 input power (PCCS[2:0]=100)	99

List of Contents

October, 2017

5.12	Uncontrolled power off	101
5.13	Content adaptive brightness control (CABC) function	102
5.13.1	Module architectures	103
5.13.2	Brightness control block	104
5.13.3	Minimum brightness setting of CABC function.....	105
5.14	FRM (Free running mode)	106
5.15	OTP programming.....	107
5.15.1	OTP table	107
5.15.2	OTP programming flow	119
5.15.3	OTP programming sequence	120
5.15.4	OTP programming example of VCOM setting VCMC	121
5.15.5	OTP programming example of ID1, ID2, ID3 and ID4	122
5.15.6	OTP Programming all OTP Index(000h~366h except 02Eh~044h)	123
5.15.7	Flexible OTP Index(370h~3FFh) Programming	124
5.15.8	Flexible OTP Index(370h~3FFh) Continuous Programming.....	125
5.15.9	OTP read example of OTP Index 00h (ID1).....	126
6.	Command.....	127
6.1	Command list	127
6.1.1	Standard command	127
6.1.2	User define command list table.....	129
6.2	Command description	141
6.2.1	NOP: No operation (00h)	141
6.2.2	SWRESET: Software reset (01h)	142
6.2.3	RDDIDIF: Read display identification information (04h)	143
6.2.4	RDNUMPE: Read number of the errors on DSI (05h)	144
6.2.5	Get_red_channel (06h)	145
6.2.6	Get_green_channel (07h)	146
6.2.7	Get_blue_channel (08h).....	147
6.2.8	RDDST: Read display status (09h)	148
6.2.9	RDDPM: Read display power mode (0Ah)	151
6.2.10	RDDMADCTL: Read display MADCTL (0Bh)	152
6.2.11	RDDCOLMOD: Read display COLMOD (0Ch).....	154
6.2.12	RDDIM: Read display image mode (0Dh).....	155
6.2.13	RDDSM: Read display signal mode (0Eh).....	156
6.2.14	RDDSDR: Read display self-diagnostic result) (0Fh)	157
6.2.15	SLPIN: Sleep in (10h)	158
6.2.16	SLPOUT: Sleep out (11h)	159
6.2.17	NORON: Normal display mode on (13h)	160
6.2.18	INVOFF: Display inversion off (20h)	161
6.2.19	INVON: Display inversion on (21h)	162
6.2.20	ALLPOFF: All pixel off (22h).....	163
6.2.21	ALLPON: All pixel on (23h)	164
6.2.22	GAMSET: Gamma set (26h)	165
6.2.23	DISPOFF: Display off (28h)	166
6.2.24	DISPON: Display on (29h)	167
6.2.25	TEOFF: Tearing effect line off (34h).....	168
6.2.26	TEON: Tearing effect line on (35h).....	169
6.2.27	MADCTL: Memory access control (36h)	170
6.2.28	IDMOFF: Idle mode off (38h)	173
6.2.29	IDMON: Idle mode on (39h).....	174
6.2.30	COLMOD: Interface pixel format 3Ah).....	175
6.2.31	TESL: Tear effect scan lines (44h)	176
6.2.32	GETSCAN: Get the current scanline (45h)	177
6.2.33	WRDISBV: Write display brightness (51h).....	178
6.2.34	RDDISBV: Read display brightness value (52h).....	179

» HX8399-C

1080RGB x 2400 dot, 16.7M color, LTPS
Mobile Single Chip Driver



Himax Technologies, Inc.
<http://www.himax.com.tw>

List of Contents

October, 2017

6.2.35	WRCTRLD: Write control display (53h)	180
6.2.36	RDCTRLD: Read control value display (54h)	181
6.2.37	WRCABC: Write content adaptive brightness control (55h)	182
6.2.38	RDCABC: Read content adaptive brightness control (56h)	183
6.2.39	WRCABCMB: Write CABC minimum brightness (5Eh)	184
6.2.40	RDCABCMB: Read CABC minimum brightness (5Fh)	185
6.2.41	RDABCSDR: Read automatic brightness control self-diagnostic result (68h)	186
6.2.42	Read_DDB_start (A1h)	187
6.2.43	Read_DDB_continue (A8h)	189
6.2.44	RDID1: Read ID1 (DAh)	190
6.2.45	RDID2: Read ID2 (DBh)	191
6.2.46	RDID3: Read ID3 (DCh)	192
6.3	User define command description	193
6.3.1	SETSEQUENCE: Set Sequence (B0h)	193
6.3.2	SETPOWER: Set power related register (B1h)	194
6.3.3	SETDISP: Set display related register (B2h)	203
6.3.4	SETCYC: Set display waveform cycles (B4h)	207
6.3.5	SETVCOM: Set VCOM voltage (B6h)	213
6.3.6	SETTE: Set internal TE function (B7h)	215
6.3.7	SETEXTC: Set extension command (B9h)	216
6.3.8	SETMIPI: Set MIPI control (BAh)	217
6.3.9	SETOTP: Set OTP (BBh)	218
6.3.10	SET_BANK: Set register bank (BDh)	220
6.3.11	SETDGCLUT_P: Set DGC LUT_P (C1h)	221
6.3.12	SETID: Set ID (C3h)	225
6.3.13	SETDDB: Set DDB (C4h)	226
6.3.14	SETCABC: Set CABC control (C9h)	227
6.3.15	SETCLOCK (CBh)	229
6.3.16	SETPANEL: Set panel related register (CCh)	230
6.3.17	SETCRC (D0h)	231
6.3.18	SETOFFSET (D2h)	232
6.3.19	SETGIP0: Set GIP Option0 (D3h)	233
6.3.20	SETGIP1: Set GIP Option1 (D5h)	239
6.3.21	SETGIP2: Set GIP Option2 (D6h)	242
6.3.22	SETGIP3: Set GIP Option3 (D8h)	245
6.3.23	SETGPO (D9h)	248
6.3.24	SETSCALING (DDh)	249
6.3.25	SETDGCLUT_N: Set DGC LUT_N (DEh)	250
6.3.26	SETIDLE (DFh)	254
6.3.27	SETGAMMA: Set gamma curve related setting (E0h)	258
6.3.28	SETCHEMODE_DYN (E4h)	260
6.3.29	SET_I2C_SA: Set I2C slave address (E8h)	262
6.3.30	SET_SP_CMD (E9h)	263
6.3.31	SETCNCD/GETCNCD (FDh)	264
6.3.32	SETREADINDEX: Set SPI Read Index (FEh)	265
6.3.33	GETSPIREAD: SPI Read Command Data (FFh)	266
7.	Layout Recommendation	267
7.1	Maximum layout resistance	267
7.2	External Components Connection	268
7.2.1	HX5186–A/B/C mode	268
7.2.2	PFM Type–A mode	269
7.2.3	PFM Type–D mode	270
7.2.4	PFM Type–C mode	271
7.2.5	External VSP/VSN mode	272
7.2.6	External VDD3/VSP/VSN mode	272

» HX8399-C

1080RGB x 2400 dot, 16.7M color, LTPS
Mobile Single Chip Driver



Himax Technologies, Inc.
<http://www.himax.com.tw>

List of Contents

October, 2017

7.2.7 External VSP/VSN/VGH/VGL mode	273
8. Electrical Characteristics	274
8.1 Absolute maximum ratings.....	274
8.2 DC characteristics.....	275
8.3 AC characteristics	276
8.3.1 I2C AC characteristics.....	276
8.3.2 DBI Type-C interface characteristics.....	277
8.3.3 DSI D-PHY electrical characteristics.....	278
8.3.4 Timings for DSI video mode.....	286
8.3.5 Reset input timing.....	288
9. Ordering Information	289

Himax Confidential
Do Not Copy

List of Figures

October, 2017

Figure 4.1: Serial data stream, write mode	20
Figure 4.2: DBI Type-C casoria interface protocol 3-wire/4-wire read mode	21
Figure 4.3: Type C:Serial interface protocol 3-wire/4-wire read mode	22
Figure 4.4: Display module data transfer recovery	22
Figure 4.5: I2C connection diagram	23
Figure 4.6: I ² C Signal timing	23
Figure 4.7: I ² C START/STOP	24
Figure 4.8: I ² C data transfer	24
Figure 4.9: I ² C interface register write flow	25
Figure 4.10: I ² C interface register read flow	26
Figure 4.11: DSI transmitter and receiver interface	27
Figure 4.12: DSI transmitter and receiver interface	28
Figure 4.13: Clock Lane Mode State diagram	30
Figure 4.14: Data Lane Mode State diagram	32
Figure 4.15: Escape Mode State Machine	33
Figure 4.16: Escape Mode timing sequence	34
Figure 4.17: High Speed Data Transmission State Machine	35
Figure 4.18: High Speed Data Transmission timing sequence	35
Figure 4.19: Switching the clock lane between clock transmission and LP mode	36
Figure 4.20: Turnaround State Machine	38
Figure 4.21: Turnaround timing sequence	38
Figure 4.22: Multiple HS transmission packets	39
Figure 4.23: Structure of the short packet	39
Figure 4.24: Structure of the long packet	40
Figure 4.25: The format of data ID	40
Figure 4.26: show Short- / Long-packet transmission command sequence	41
Figure 5.1: Tearing effect output signal mode 1	51
Figure 5.2: TE delay output	51
Figure 5.3: Tearing effect output signal mode 2	52
Figure 5.4: TE output for TELINE setting	52
Figure 5.5: Tearing effect output signal	52
Figure 5.6: Tearing effect output line-tearing effect line timing	53
Figure 5.7: Tearing effect output line-definition of tf, tr	53
Figure 5.8: OSC aritecture	54
Figure 5.9 Inversion mode (MUX_SEL=0)	56
Figure 5.10: Inversion mode 2:6 (MUX_SEL=1)	57
Figure 5.11: Zig-Zag Inversion mode(ZZ_EO=0)	58
Figure 5.12: Zig-Zag Inversion mode(ZZ_EO=1)	59
Figure 5.13: LCD power generation scheme for HX5186 and FPM mode	60
Figure 5.14: LCD power generation scheme for external power mode	60
Figure 5.15: DC/DC converter circuit of HX5186- C	63
Figure 5.16: DC/DC converter circuit (PFM Type-A)	64
Figure 5.17: DC/DC converter circuit (PFM Type-D)	65
Figure 5.18: DC/DC converter circuit (PFM Type-C)	66
Figure 5.19: DC/DC converter circuit of external VSP/VSN	67
Figure 5.20: DC/DC converter circuit of external VDD3/VSP/VSN	68
Figure 5.21: DC/DC converter circuit of external VSP/VSN/VGH/VGL	69
Figure 5.22: Idle mode grayscale control	70
Figure 5.23: Gamma adjustments different of source driver with digital gamma correction	71
Figure 5.24: Grayscale control	72
Figure 5.25: Gamma resister stream and gamma reference voltage	75
Figure 5.26: Block diagram of digital gamma correction	89
Figure 5.27: Sleep out flow chart-command and self-diagnostic functions	92
Figure 5.28: Sleep out flow chart internal function detection	93
Figure 5.29: Power on/off sequence	94

List of Figures

October, 2017

Figure 5.30: VDD3/VDD1 input power on sequence (PCCS[2:0]=000/001/101)	95
Figure 5.31: VDD3/VDD1 input power off sequence (PCCS[2:0] =000/001/101)	95
Figure 5.32: VSP/VDD1 input power on sequence (PCCS[2:0] =010)	96
Figure 5.33: VSP/VDD1 input power off sequence (PCCS[2:0] =010)	96
Figure 5.34: VSP/VSN/VDD1 input power on sequence (PCCS[2:0]=011).....	97
Figure 5.35: VSP/VSN/VDD1 input power off sequence (PCCS[2:0]=011).....	97
Figure 5.36: VDD3/VSP/VSN/VDD1 input power on sequence (PCCS[2:0]=111)	98
Figure 5.37: VDD3/VSP/VSN/VDD1 input power off sequence.....	98
Figure 5.38: VSP/VSN/VGH/VGL/VDD1 input power on sequence	99
Figure 5.39: VSP/VSN/VGH/VGL/VDD1 input power off sequence	100
Figure 5.40: CABC block diagram	102
Figure 5.41: Module architecture	103
Figure 5.42: CABC_PWM_OUT output duty	104
Figure 5.43: FRM power on sequence	106
Figure 5.44: OTP programming sequence.....	119
Figure 5.45: OTP programming sequence example 1	121
Figure 5.46: OTP programming sequence example 2	122
Figure 5.47: OTP programming all Index sequence	123
Figure 5.48: Flexible OTP programming sequence	124
Figure 5.49: Flexible OTP continuous programming sequence	125
Figure 5.50: OTP read sequence flow of Index 00h	126
Figure 8.1: I2C timing.....	276
Figure 8.2: DBI Type-C interface characteristics	277
Figure 8.3: Electrical functions of a fully D-PHY transceiver	278
Figure 8.4: Shows both the HS and LP signal levels.....	278
Figure 8.5: Differential HS signals for HS receive	280
Figure 8.6: Input glitch rejections of low-power receivers.....	281
Figure 8.7: DDR clock definition	283
Figure 8.8: Data to clock timing definitions	284
Figure 8.9: Skew window of transmitter and receiver	285
Figure 8.10: Vertical timings for DSI I/F	286
Figure 8.11: Horizontal timing for DSI video mode I/F	287
Figure 8.12: Reset input timing	288

» HX8399-C

1080RGB x 2400 dot, 16.7M color, LTPS Mobile
Single Chip Driver



Himax Technologies, Inc.
<http://www.himax.com.tw>

List of Tables

October, 2017

Table 4.1: Interface selection	19
Table 4.2: Pin connection based on different interface	19
Table 4.3: I ² C slave address table	24
Table 4.4: Global operation timing parameters for data lane	36
Table 4.5: Global operation timing parameters for clock lane	37
Table 4.6: Data types for processor-sourced packets.....	42
Table 4.7: Shows the error report bit definitions	50
Table 4.8: The complete set of peripheral-to-processor data types.....	50
Table 5.1: AC characteristics of tearing effect signal	53
Table 5.2: Voltage configuration.....	61
Table 5.3: Power mode setting.....	62
Table 5.4: Gamma-Adjustment registers for normally black panel	73
Table 5.5: Gamma-Adjustment registers for normally white panel	74
Table 5.6: Offset adjustment 0~5	76
Table 5.7: Center adjustment	76
Table 5.8: VinP/N0	77
Table 5.9: VinP/N4	77
Table 5.10: VinP/N8	77
Table 5.11: VinP/N12	78
Table 5.12: VinP/N20	78
Table 5.13: VinP/N28	78
Table 5.14: VinP/N40	79
Table 5.15: VinP/N52	79
Table 5.16: VinP/N64	79
Table 5.17: VinP/N76	80
Table 5.18: VinP/N88	80
Table 5.19: VinP/N100	80
Table 5.20: VinP/N112	81
Table 5.21: VinP/N128	81
Table 5.22: VinP/N144	81
Table 5.23: VinP/N156	82
Table 5.24: VinP/N168	82
Table 5.25: VinP/N180	82
Table 5.26: VinP/N192	83
Table 5.27: VinP/N204	83
Table 5.28: VinP/N216	83
Table 5.29: VinP/N228	84
Table 5.30: VinP/N236	84
Table 5.31: VinP/N243	84
Table 5.32: VinP/N247	85
Table 5.33: VinP/N251	85
Table 5.34: VinP/N255	85
Table 5.35: Voltage calculation formula of 256-grayscale voltage (positive/negative polarity)	88
Table 5.36: DGC look-up table	90
Table 5.37: Characteristics of output or bi-directional (I/O) pins	91
Table 5.38: Characteristics of input pins	91
Table 5.39: CABC timing table	104
Table 5.40: OTP table	118
Table 5.41: OTP programming sequence	120
Table 7.1: Maximum Layout Resistance(include IC and FPC bonding)	267
Table 7.2: HX5186-C mode external components	268
Table 7.3: PFM Type A mode external components.....	269
Table 7.4: PFM Type D mode external components.....	270
Table 7.5: PFM Type C mode external components.....	271
Table 7.6: External VSP/VSN mode external components.....	272

» HX8399-C

1080RGB x 2400 dot, 16.7M color, LTPS Mobile
Single Chip Driver



Himax Technologies, Inc.
<http://www.himax.com.tw>

List of Tables

October, 2017

Table 7.7: External VDD3/VSP/VSN mode external components	272
Table 7.8: External VSP/VSN mode external components	273
Table 8.1: Absolute maximum rating	274
Table 8.2: DC characteristic	275
Table 8.3 I2C timing spec.....	276
Table 8.4: DBI Type-C interface characteristics	277
Table 8.5: LP transmitter DC specifications	279
Table 8.6: LP transmitter AC specifications	279
Table 8.7: HS receiver DC specifications.....	280
Table 8.8: HS receiver AC specifications.....	280
Table 8.9: LP receiver DC specifications	281
Table 8.10: LP receiver AC specifications	281
Table 8.11: Contention detector DC specifications	282
Table 8.12: Reverse HS data transmission timing parameters.....	284
Table 8.13: Data to clock timing specifications	285
Table 8.14: Vertical timings for DSI I/F.....	286
Table 8.15: Horizontal timings for DSI video mode I/F.....	287
Table 8.16: Reset timing	288

Himax Confidential
Do Not Copy

>> **HX8399-C**

1080RGB x 2400 dot, 16.7M color, LTPS Mobile
Single Chip Driver



Himax Technologies, Inc.
<http://www.himax.com.tw>

Version 01

October, 2017

1. General Description

This document describes Himax's HX8399-C supports Full HD resolution driving controller. The HX8399-C is designed to provide a single-chip solution that combines a source driver, gate driver control, power supply circuit to drive a LTPS dot matrix LCD with 1080RGBx2400 dots at maximum.

The HX8399-C can be operated in low-voltage condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8399-C also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8399-C supports MIPI DSI (Display Serial Interface) interface mode, I2C and SPI. The interface mode is selected by the external hardware pins IM2~0.

The HX8399-C is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

Himax Confidential
Do Not Copy

2.Features

2.1 Display

- Single chip solution for a Full HD LTPS type LCD display
- Resolution:
 - 1080RGB x (528+8 x NL), NL=0~234
- Display color modes
 - Full color mode:
 - ◆ 16.7M colours (24-bit, 8(R):8(G):8(B))
 - Reduce color mode:
 - ◆ 262K colours (18-bit, 6(R):6(G):6(B))
 - ◆ 65K colours (16-bit, 5(R):6(G):5(B))
 - ◆ 8 colors (Idle mode on): 8 colors (3-bit binary mode)

2.2 Display module

- Support 1082 source channel outputs
- Internal level shifter for Gate Driver control
- Supports 1-dot / 2-dot / 4-dot / 8-dot / column / pixel column and Zig-Zag inversion
- Gamma correction
- On module VCOM control (-3 to +1V common electrode output voltage range)
- On module DC/DC converter
 - Positive source output voltage level: VSPR=3.1V to 5.8V
 - Negative source output voltage level: VSNR=-3.1V to -5.8V
 - VCL=-2.5V~-3.1V
 - Positive gate driver output voltage level: VGH=6.7V to 13.0V
 - Negative gate driver output voltage level: VGL=-5.7V to -12.0V
 - Common electrode voltage level: VCOM=-3V to +1V, a step=10mV

2.3 Support Power Mode

- External Charge Pump: Support HX5186-C mode
- PFM booster: Support Type A/C/D
- External Power mode support:
 - VSP + VSN + VDD1
 - VSP + VSN + VDD3 + VDD1
 - VSP + VSN + VGH + VGL + VDD1

2.4 Display / Control interface

- Display interface types supported
 - MIPI-DSI (Display Serial Interface) interface
 - ◆ Support DSI Version 1.1
 - ◆ Support D-PHY Version 1.1
 - MIPI-DSI + I2C interface
 - MIPI-DSI + DBI TypeC(Option1/Option3) interface

2.5 Input power

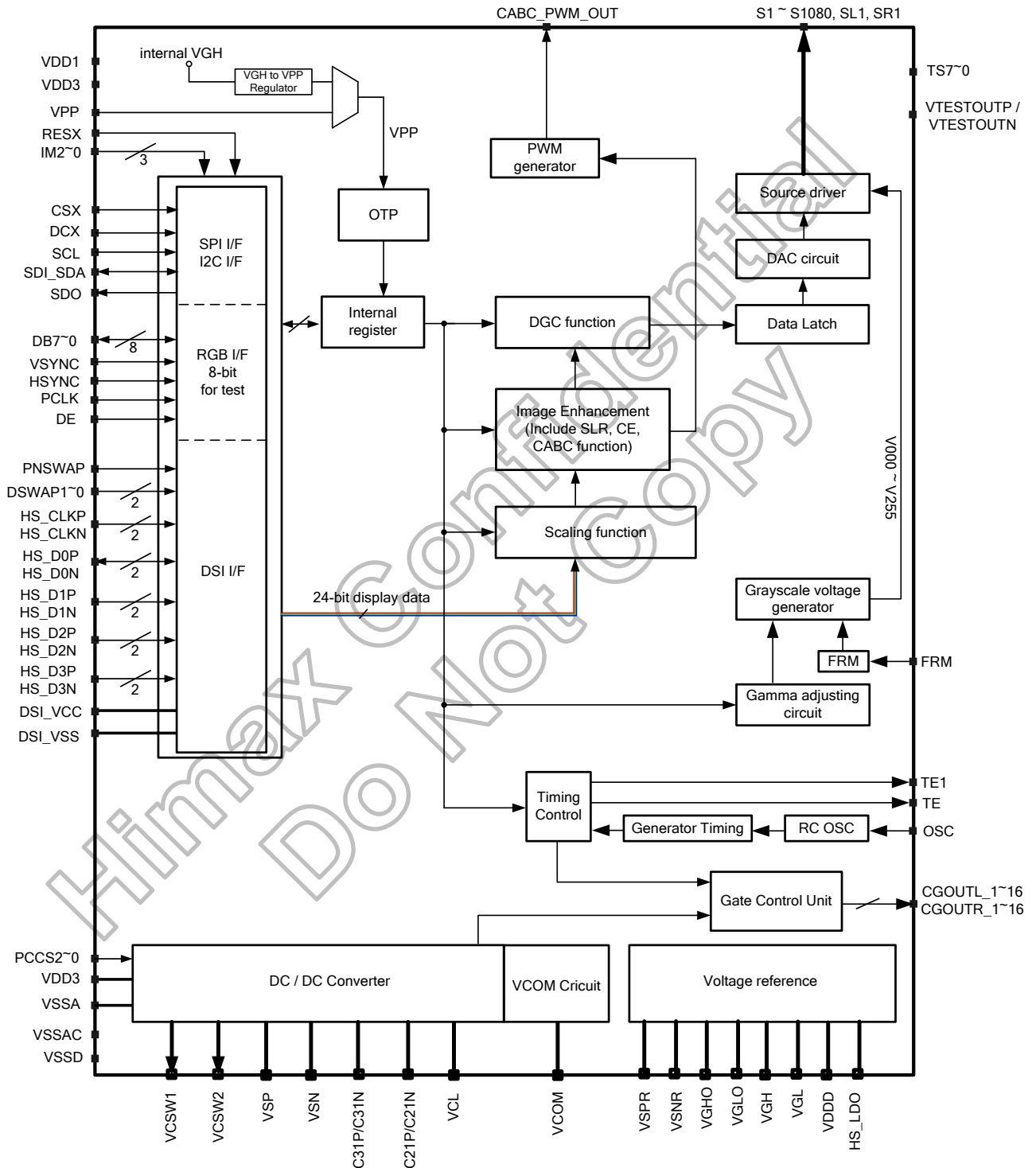
- I/O and Logic power supply (VDD1): 1.65V to 3.3V
- Analog power supply (VDD3): 2.5V to 3.6V
- High speed interface power supply (HS_VCC): 1.65V to 3.3V
- OTP programming voltage (VPP): 8.5V \pm 0.2V
- Positive source driver power (External input mode VSP): 4.8 to 6V
- Negative source driver power (External input mode VSN): -4.8 to -6V

2.6 Miscellaneous

- Software programmable color depth mode
- Oscillator for display clock generation
- GAS function for preventing image sticking when abnormal power off
- Support DC COM driving
- On-chip OTP program voltage generator
- OTP memory to store initialization register settings
- 3 times MTP for VCOM and ID setting
- Support CABC (Content Adaptive Brightness Control) function
- Support Color Enhancement function
- Support DGC (Digital Gamma Correction) function
- Support Scaling function
- Support Free Running mode(Internal BIST pattern generator)
- Support SLR(Sun Light Readability)
- Operation temperature range: -40 to +85 °C

3. Device Overview

3.1 Block diagram



3.2 Pin description

Host interface pin																																																																																																
Signals	I/O	Pin no.	Connected with	Description																																																																																												
IM2 ~ IM0	I	3	VDD1 / VSSD	These pins must be connected to VDD1 or VSSD. Interface mode is selected as listed below: <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>IM2</th> <th>IM1</th> <th>IM0</th> <th>interface mode</th> <th>DB pins</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>DSI Video mode + I2C</td> <td>HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N, SDI_SDA</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Reserved</td> <td>Reserved</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>DSI Video mode + DBI TypeC Option1</td> <td>HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N, SDI_SDA, SDO</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>DSI Video mode + DBI TypeC Option3</td> <td>HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N, SDI_SDA, SDO</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Reserved</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Reserved</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>DSI Video mode</td> <td>HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	IM2	IM1	IM0	interface mode	DB pins	0	0	0	DSI Video mode + I2C	HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N, SDI_SDA	0	0	1	Reserved	Reserved	0	1	0	DSI Video mode + DBI TypeC Option1	HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N, SDI_SDA, SDO	0	1	1	DSI Video mode + DBI TypeC Option3	HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N, SDI_SDA, SDO	1	0	0	Reserved	Reserved	1	0	1	Reserved	Reserved	1	1	0	DSI Video mode	HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N	1	1	1	Reserved	Reserved																																															
				IM2	IM1	IM0	interface mode	DB pins																																																																																								
				0	0	0	DSI Video mode + I2C	HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N, SDI_SDA																																																																																								
				0	0	1	Reserved	Reserved																																																																																								
				0	1	0	DSI Video mode + DBI TypeC Option1	HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N, SDI_SDA, SDO																																																																																								
				0	1	1	DSI Video mode + DBI TypeC Option3	HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N, SDI_SDA, SDO																																																																																								
				1	0	0	Reserved	Reserved																																																																																								
				1	0	1	Reserved	Reserved																																																																																								
				1	1	0	DSI Video mode	HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N																																																																																								
				1	1	1	Reserved	Reserved																																																																																								
Pixel format (RGB565 / RGB666 / RGB888) is selected by DCS command (0x3Ah).																																																																																																
PNSWAP, DSWAP[1:0]	I	3	VDD1 / VSSD	These pins must be connected to VDD1 or VSSD to set 1 or 0. PNSWAP and DSWAP1~0 are used for the combination of polarity swap and data lane swap of DSI. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>PNSWAP</th> <th>DSWAP [1:0]</th> <th>HS_D2P</th> <th>HS_D2N</th> <th>HS_D1P</th> <th>HS_D1N</th> <th>HS_CKP</th> <th>HS_CKN</th> <th>HS_D0P</th> <th>HS_D0N</th> <th>HS_D3P</th> <th>HS_D3N</th> </tr> </thead> <tbody> <tr> <td rowspan="3">0</td> <td>00</td> <td>D3-</td> <td>D3+</td> <td>D2-</td> <td>D2+</td> <td>CLK-</td> <td>CLK+</td> <td>D1-</td> <td>D1+</td> <td>D0-</td> <td>D0+</td> </tr> <tr> <td>01</td> <td>D3-</td> <td>D3+</td> <td>D0-</td> <td>D0+</td> <td>CLK-</td> <td>CLK+</td> <td>D1-</td> <td>D1+</td> <td>D2-</td> <td>D2+</td> </tr> <tr> <td>10</td> <td>D0-</td> <td>D0+</td> <td>D1-</td> <td>D1+</td> <td>CLK-</td> <td>CLK+</td> <td>D2-</td> <td>D2+</td> <td>D3-</td> <td>D3+</td> </tr> <tr> <td rowspan="3">1</td> <td>00</td> <td>D3+</td> <td>D3-</td> <td>D2+</td> <td>D2-</td> <td>CLK+</td> <td>CLK-</td> <td>D1+</td> <td>D1-</td> <td>D0+</td> <td>D0-</td> </tr> <tr> <td>01</td> <td>D3+</td> <td>D3-</td> <td>D0+</td> <td>D0-</td> <td>CLK+</td> <td>CLK-</td> <td>D1+</td> <td>D1-</td> <td>D2+</td> <td>D2-</td> </tr> <tr> <td>10</td> <td>D0+</td> <td>D0-</td> <td>D1+</td> <td>D1-</td> <td>CLK+</td> <td>CLK-</td> <td>D2+</td> <td>D2-</td> <td>D3+</td> <td>D3-</td> </tr> <tr> <td></td> <td>11</td> <td>D2+</td> <td>D2-</td> <td>D1+</td> <td>D1-</td> <td>CLK+</td> <td>CLK-</td> <td>D0+</td> <td>D0-</td> <td>D3+</td> <td>D3-</td> </tr> </tbody> </table>	PNSWAP	DSWAP [1:0]	HS_D2P	HS_D2N	HS_D1P	HS_D1N	HS_CKP	HS_CKN	HS_D0P	HS_D0N	HS_D3P	HS_D3N	0	00	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+	01	D3-	D3+	D0-	D0+	CLK-	CLK+	D1-	D1+	D2-	D2+	10	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+	1	00	D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-	D0+	D0-	01	D3+	D3-	D0+	D0-	CLK+	CLK-	D1+	D1-	D2+	D2-	10	D0+	D0-	D1+	D1-	CLK+	CLK-	D2+	D2-	D3+	D3-		11	D2+	D2-	D1+	D1-	CLK+	CLK-	D0+	D0-	D3+	D3-
				PNSWAP	DSWAP [1:0]	HS_D2P	HS_D2N	HS_D1P	HS_D1N	HS_CKP	HS_CKN	HS_D0P	HS_D0N	HS_D3P	HS_D3N																																																																																	
				0	00	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+																																																																																	
					01	D3-	D3+	D0-	D0+	CLK-	CLK+	D1-	D1+	D2-	D2+																																																																																	
					10	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+																																																																																	
				1	00	D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-	D0+	D0-																																																																																	
					01	D3+	D3-	D0+	D0-	CLK+	CLK-	D1+	D1-	D2+	D2-																																																																																	
					10	D0+	D0-	D1+	D1-	CLK+	CLK-	D2+	D2-	D3+	D3-																																																																																	
					11	D2+	D2-	D1+	D1-	CLK+	CLK-	D0+	D0-	D3+	D3-																																																																																	
				CSX	I	1	MPU	Chip select pin. Low: Chip can be accessed. High: Chip can not be accessed. If not use, please connect it to VSSD or VDD1.																																																																																								
RESX	I	1	MPU or reset circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied (Must be connected to VSSD or VDD1).																																																																																												
DCX	I	1	MPU	Command/parameter selection for DBI Type-C Option3. If not use, please connect it to VSSD or VDD1.																																																																																												
SCL	I	1	MPU	Serves as serial clock in DBI Type-C interface. Serves as serial clock in I2C interface. If not use, please connect it to VSSD or VDD1.																																																																																												
DB[7:0]	I/O	8	MPU	Only for internal test. Let the unused pins open or connect it to VSSD or VDD1.																																																																																												
SDO	O	1	MPU	Serial data output pin. If not used, let it open.																																																																																												
SDI_SDA	I	3	MPU	SDI: Serial data input pin in DBI Type-C interface. SDA: Serial input/output data in I2C bus interface. If not use, please connect it to VSSD or VDD1.																																																																																												
HSYNC	I	1	MPU	Only for internal test. Let the unused pins open or connect it to VSSD or VDD1																																																																																												
DE	I	1	MPU	Only for internal test. Let the unused pins open or connect it to VSSD or VDD1																																																																																												
VSYNC	I	1	MPU	Only for internal test. Let the unused pins open or connect it to VSSD or VDD1																																																																																												
PCLK	I	1	MPU	Only for internal test. Let the unused pins open or connect it to VSSD or VDD1																																																																																												

Source driver output pin				
S1 to S1200	O	1200	LCD	Output voltages applied to the liquid crystal.
				<table border="1"> <thead> <tr> <th>Resolution</th> <th>Source channels</th> </tr> </thead> <tbody> <tr> <td>1080RGBX(528+8xNL)</td> <td>S1 ~ S540, S661 ~ S1200</td> </tr> </tbody> </table>
Resolution	Source channels			
1080RGBX(528+8xNL)	S1 ~ S540, S661 ~ S1200			
SL1, SR1	-	2	Open	These pins are for Zig-Zag inversion used. If not used, please let it open.
Gate Driver control signal				
CGOUTL_1~16, CGOUTR_1~16	O	64	LCD	These are pins are LTPS control signal; the function can be selected by register setting. CGOUT/LR_1~10 output high/low level VGH/VGL. CGOUT/LR_11~16 output high/low level VSP/VSN or VGH/VGL.
Power supply pin				
VDD1	I	21	Power supply	A power supply for the I/O circuit and logic power. VDD1=1.65 to 3.3V
VDD3	I	30	Power supply	A power supply for the analog power. VDD3=2.5V to 3.6V
VSSA	P	48	Power supply	Analog ground. VSSA=0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
VSSAC	P	6	Power supply	Analog ground. Must connect to VSSA on the FPC.
VSSD	P	63	Power supply	Logic Ground. VSSD=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
Power supply pin				
VSP	I	45	Stabilizing capacitor	Input voltage generated from HX5186, PFM or external (4.8V to 6V) .
VSN	I	45	Stabilizing capacitor	Input voltage generated from HX5186, PFM or external (-4.8V to -6V) .
VCL	O	24	Stabilizing capacitor	Output voltage from the set-up circuit. it is generated from VSN.
VSPR	O	1	-	Positive regulated voltage output (3.1V to 5.8V) for Gamma.
VSNR	O	1	-	Negative regulated voltage output (-3.1V to -5.8V) for Gamma.
VDDD	O	12	Stabilizing capacitor	Internal logic voltage output
VGH	O	15	Stabilizing capacitor	Output voltage from the set-up circuit. Connect to a stabilizing capacitor between VSSA and VGH.
VGL	O	15	Stabilizing capacitor	Output voltage from the set-up circuit. Connect to a stabilizing capacitor between VSSA and VGL.
VGHO	O	9	Stabilizing capacitor	Output regulated voltage for panel voltage. It is generated from VGH. Connect to VGHO on FPC and with a stabilizing capacitor between VSSA and VGHO.
VGLO	O	9	Stabilizing capacitor	Output regulated voltage for panel voltage. It is generated from VGL. Connect VGLO on FPC and with a stabilizing capacitor between VSSA and VGLO.
VCOM	O	45	Stabilizing capacitor	The power supply of common voltage in DC com driving. The voltage range is set between -3V to +1V. It must be connected with a stabilizing capacitor 2.2μF to VSSD.

DC/DC pumping																												
PCCS2/ PCCS1/ PCCS0	I	1/2/2	VDD1 / VSP/ VSSD	These pins are for analog power source mode selection.																								
				<table border="1"> <thead> <tr> <th>PCCS[2:0]</th> <th>Power Source</th> <th>Driving Mode</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>VDD3 / VDD1</td> <td>PFM Type-C</td> </tr> <tr> <td>001</td> <td>VDD3 / VDD1</td> <td>HX5186- C</td> </tr> <tr> <td>010</td> <td>VSP / VDD1</td> <td>PFM Type-D (for VSN)</td> </tr> <tr> <td>011</td> <td>VSP / VSN / VDD1</td> <td>External-1</td> </tr> <tr> <td>100</td> <td>VGH/VGL/VSP/VSN /VDD1</td> <td>External-3</td> </tr> <tr> <td>101</td> <td>VDD3 /VDD1</td> <td>PFM Type-A</td> </tr> <tr> <td>111</td> <td>VDD3 / VSP / VSN / VDD1</td> <td>External-2</td> </tr> </tbody> </table>	PCCS[2:0]	Power Source	Driving Mode	000	VDD3 / VDD1	PFM Type-C	001	VDD3 / VDD1	HX5186- C	010	VSP / VDD1	PFM Type-D (for VSN)	011	VSP / VSN / VDD1	External-1	100	VGH/VGL/VSP/VSN /VDD1	External-3	101	VDD3 /VDD1	PFM Type-A	111	VDD3 / VSP / VSN / VDD1	External-2
				PCCS[2:0]	Power Source	Driving Mode																						
				000	VDD3 / VDD1	PFM Type-C																						
				001	VDD3 / VDD1	HX5186- C																						
				010	VSP / VDD1	PFM Type-D (for VSN)																						
				011	VSP / VSN / VDD1	External-1																						
				100	VGH/VGL/VSP/VSN /VDD1	External-3																						
101	VDD3 /VDD1	PFM Type-A																										
111	VDD3 / VSP / VSN / VDD1	External-2																										
Note: PCCS2 high level is VDD1; PCCS1 & PCCS0 high level is VSP.																												
C31P/ C31N	I/O	9/9	Step-up Capacitor	Connect to the step-up capacitor according to the DC/DC pumping factor by pumping the VGL voltage.																								
C21P/ C21N	I/O	9/8	Step-up Capacitor	Connect to the step-up capacitor according to the DC/DC pumping factor by pumping the VGH voltage.																								
VCSW1/ VCSW2	O	3/2	-	In external input power mode: Not used, Please open these pin. In HX5186 mode: VCSW1 and VCSW2 connect to HX5186- C. In PFM mode: VCSW1 and VCSW2 connect to external MOS. Detail connection, please refer to DC/DC converter circuit																								
CABC & ABC & Ambient light sensor (general purpose input and output)																												
CABC_PWM_OUT	O	1	LED driver	Backlight on/off control pin. If use CABC function, the pin can connect to external LED driver IC. The output voltage range=0 to VDD1.																								
TE	O	1	-	Serves TE (Tearing Effect) output pin. Output signal can be selected by register setting, please refer to SETGPO.																								
TE1	O	1	-	Serves TE (Tearing Effect) pin of each scan line. Output signal can be selected by register setting, please refer to SETGPO.																								
High speed interface part																												
HS_D0P/ HS_D0N	I/O	6/6	DSI Host	MIPI-DSI Data differential signal input pins. (Data lane 0) If not used, Please connect to VSSD or open.																								
HS_CLKP/ HS_CLKN	I	6/6	DSI Host	MIPI-DSI CLOCK differential signal input pins. If not used, Please connect to VSSD or open.																								
HS_D1P/ HS_D1N	I	6/6	DSI Host	MIPI-DSI Data differential signal input pins. (Data lane 1) If not used, Please connect to VSSD or open.																								
HS_D2P/ HS_D2N	I	6/6	DSI Host	MIPI-DSI Data differential signal input pins. (Data lane 2) If not used, Please connect to VSSD or open.																								
HS_D3P/ HS_D3N	I	6/6	DSI Host	MIPI-DSI Data differential signal input pins. (Data lane 3) If not used, Please connect to VSSD or open.																								
HS_VCC	P	9	Power Supply	Power supply for the MIPI DSI analog power. HS_VCC=1.65V to 3.3V																								
HS_VSS	P	21	Ground	MIPI DSI analog ground. HS_VSS=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.																								
HS_LDO	O	6	Capacitor	DSI I/F: DSI regulator output pin. Connect to a stabilizing capacitor between HS_LDO and HS_VSS If not used, please open these pins.																								
Test Pin																												
OSC	I	1	Open	Oscillator input for test purpose. If not used, please let it open or connected to VSSD. (weak pull low)																								
TEST2~0	I	3	Open	Test pins. These pins are for internal logic function test. These pins can output on FPC. If not used, let it open or connected to VSSD. (weak pull low)																								

TS7-0	O	8	Open	Test pins. Disconnect these pins.
FRM	I	1	Open	This pin can output on FPC. When connected to VDD1, FRM function is enabling. If not used, please open or connect it to VSSD (weak pull low).
VTESTOUT_P	O	1	Open	A test pin. Disconnect it. This pin can output on FPC.
VTESTOUT_N	O	1	Open	A test pin. Disconnect it. This pin can output on FPC.
DUMMYR1 DUMMYR2	-	2	Open	Dummy pads. Available for measuring the COG contact resistance. They are short-circuited within the chip.
DUMMY	-	218	Open	Not used. Let it open.

Himax Confidential
Do Not Copy

4. Interface

4.1 System interface

The HX8399-C supports I2C interface and MIPI interfaces: DBI (Display Bus Interface), DSI (Display Serial Interface). Where DBI supports serial interface (Type-C Option1 and Option3). The interface mode can be selected by IM2-0 pins setting as show in Table 4.1.

IM2	IM1	IM0	interface mode	DB pins	Note
0	0	0	DSI Video mode + I2C	SDA, HS_D0P/N~HS_D3P/N	-
0	1	0	DSI Video mode + DBI TypeC Option1	SDI, SDO, HS_D0P/N~HS_D3P/N	-
0	1	1	DSI Video mode + DBI TypeC Option3	SDI, SDO, HS_D0P/N~HS_D3P/N	-
1	1	0	DSI Video mode	HS_D0P/N~HS_D3P/N	-
Other setting			Reserved	Reserved	-

Table 4.1: Interface selection

Interface	CSX	SCL	DCX	Input/Output pin
MIPI DSI + I2C	CSX	SCL	Unused	SDA, HS_CLKP, HS_CLKN, HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N
MIPI DSI + DBI Type-C Option1	CSX	SCL	Unused	SDI, SDO, HS_CLKP, HS_CLKN, HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N
MIPI DSI + DBI Type-C Option3	CSX	SCL	DCX	SDI, SDO, HS_CLKP, HS_CLKN, HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N
MIPI DSI mode	Unused	Unused	Unused	HS_CLKP, HS_CLKN, HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N

Table 4.2: Pin connection based on different interface

4.2 Serial data transfer interface (MIPI DBI Type-C)

The HX8399-C supports two type serial data transfer interface, the interface selection by setting IM2-0 pins. The IM2-0 set “010” is select 3-wire Option1 serial bus. The IM2-0 is set “011” when select 4-wire Option3 serial bus.

The 3-wire serial bus is use: chip select line (CSX), serial input/output data (SDI and SDO) and the serial transfer clock line (SCL).The 4-wire serial bus is use: chip select line (CSX), data/command select (DCX), serial input/output data (SDI and SDO) and the serial transfer clock line (SCL).

4.2.1 Serial data write mode

The 3-pin serial data packet contains a control bit D/CX and a transmission byte and in 4-pin serial case, data packet contains just transmission byte and control signal D/CX is transferred by DCX pin. If DCX is low, the transmission byte is command byte. If D/CX is high, the transmission byte is stored in to command register. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or serial input/output data (SDI and SDO) have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

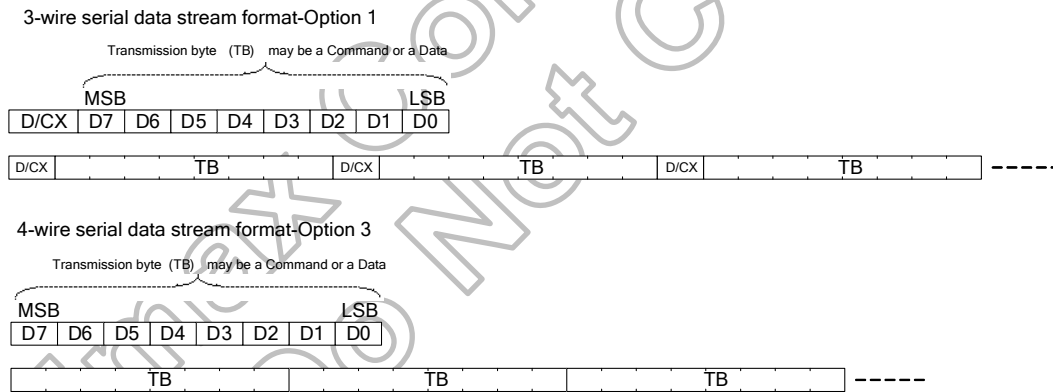
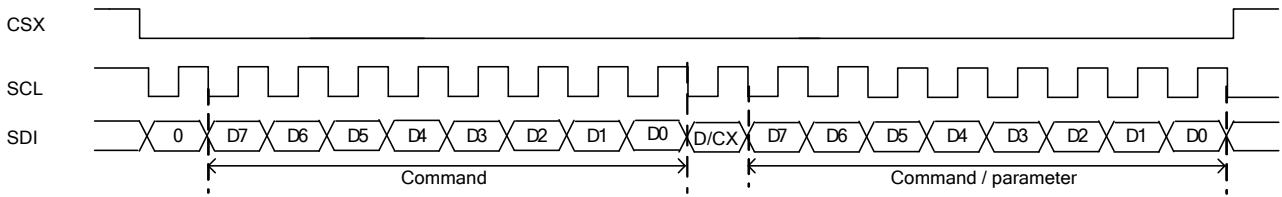


Figure 4.1: Serial data stream, write mode

DBI Type C: Interface protocol-Option 1 (3-wire)



DBI Type C: Interface protocol Option 3 (4-wire)

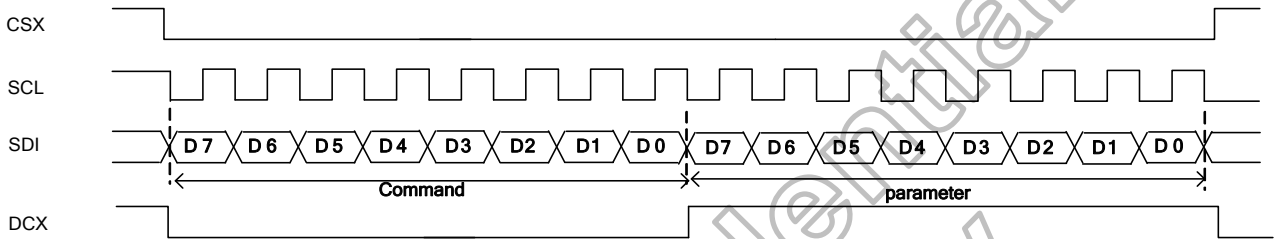


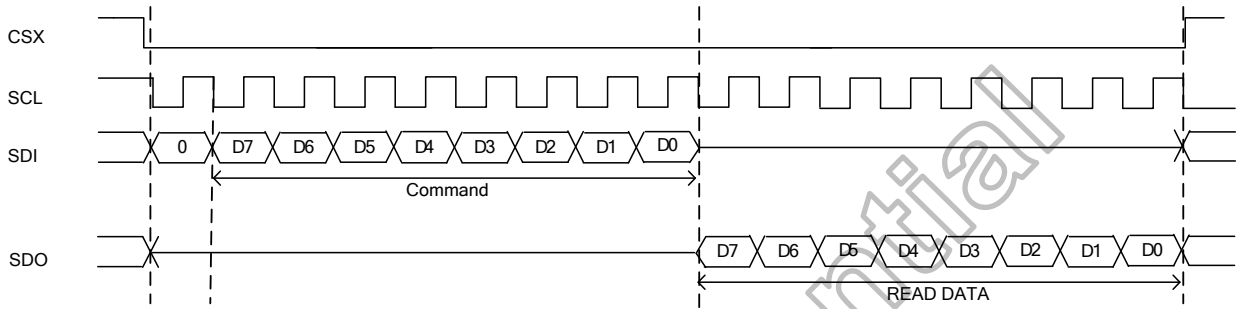
Figure 4.2: DBI Type-C casoria interface protocol 3-wire/4-wire read mode

Himax Confidential
Do Not Copy

4.2.2 Serial data read mode

The micro-controller first has to send a command and then the following byte is transmitted in the opposite direction. The 3-wire serial read data format which just needs 8-bit.

DBI Type C: Interface protocol-Option 1 (3-wire)



DBI Type-C Interface Protocol - Option 3 (4 wire)

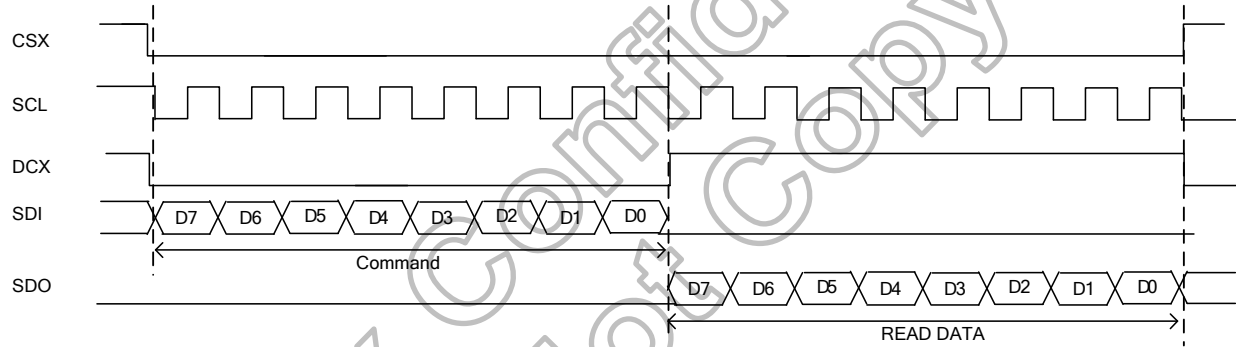


Figure 4.3: Type C:Serial interface protocol 3-wire/4-wire read mode

If there is a break on data transmission when transmit a command before a whole byte has been completed, then the display module will have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following figure.

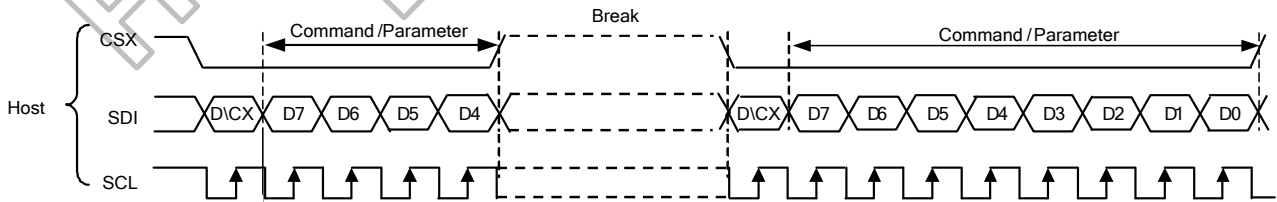


Figure 4.4: Display module data transfer recovery

4.3 I2C interface

The HX8399-C supports I2C interface to access command. The interface selection is by setting IM[2:0] pins to “000”.

2 hardware pins in I2C interface – serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognized by a unique address — whether it’s a microcontroller, LCD driver, memory or keyboard interface — and can operate as either a transmitter or receiver, depending on the function of the device. Both SDA and SCL are needed connected to a positive supply voltage via a pull-up resistor. The pull-up resistor should connect to VDD1. When the bus is free, both lines are HIGH.

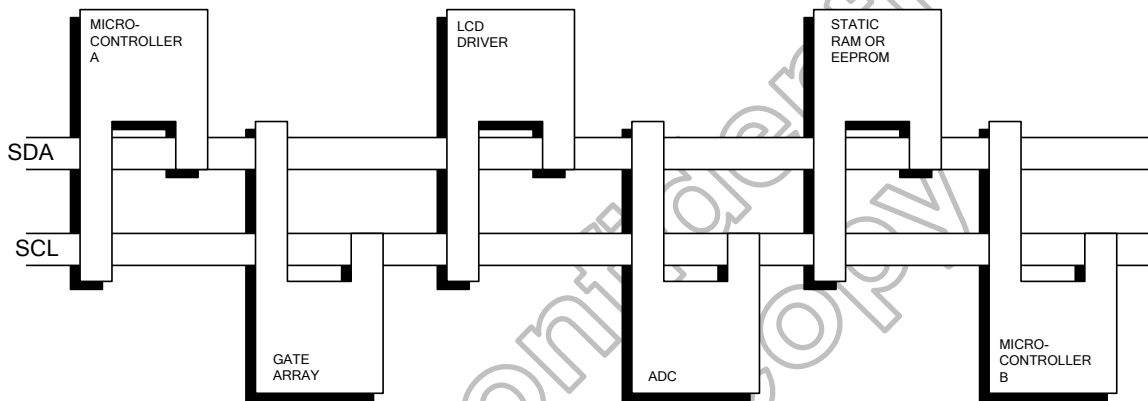


Figure 4.5: I2C connection diagram

4.3.1 I2C protocol

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

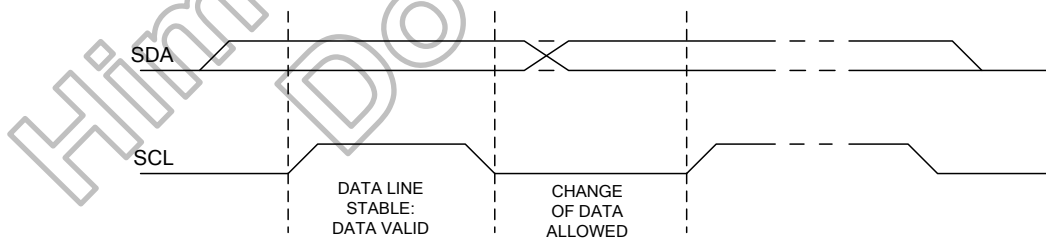


Figure 4.6: I²C Signal timing

Within the procedure of the I²C-bus, unique situations arise which are defined as START and STOP conditions. A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The I²C bus is considered to be busy after the START condition. The I²C bus is considered to be free again a certain time after the STOP condition.

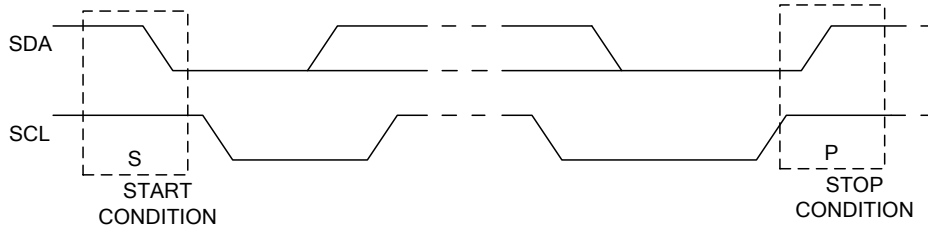


Figure 4.7: I²C START/STOP

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.

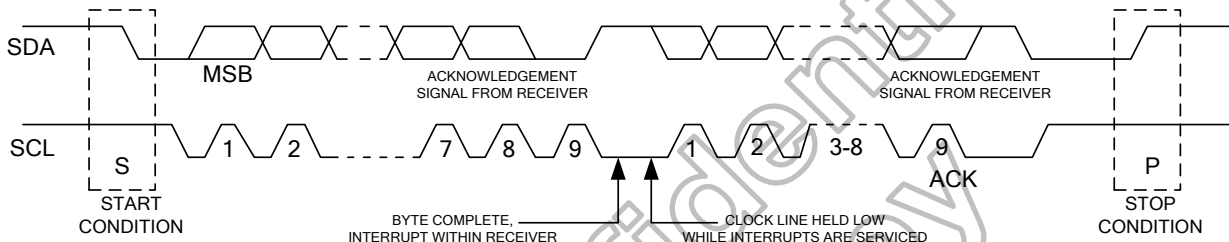


Figure 4.8: I²C data transfer

4.3.2 I2C slave address

HX8399-C support many slave addresses could be selected by register setting in command E8h. The slave address is defined a follow table.

I2C_SA[6:0]	Slave address (A6-A0)
000_0000	000_0000
000_0001~000_0111	Reserved
000_1000	000_1000
:	:
111_0110	111_0110
111_0111	111_0111
111_1xxx	Reserved

Table 4.3: I²C slave address table

4.3.3 I2C interface write mode

- HX8399-C support I2C to write data to register. The write flow is described as below
- Send Start condition followed by I2C 7 bits slave address and 1 bit '0'(write flag)
 - Send High byte of 16-bit address, then IC feedback Ack.
 - Send Low byte of 16-bit address, then IC feedback Ack.
 - Send 8-bit register data, MSB first , ADD[7] send first, the IC feedback Ack
 - Send Stop condition



[6..0] '0'(Write)

- From master to slaver
- From slaver to master

Master ex: MPU,DSP...control chip

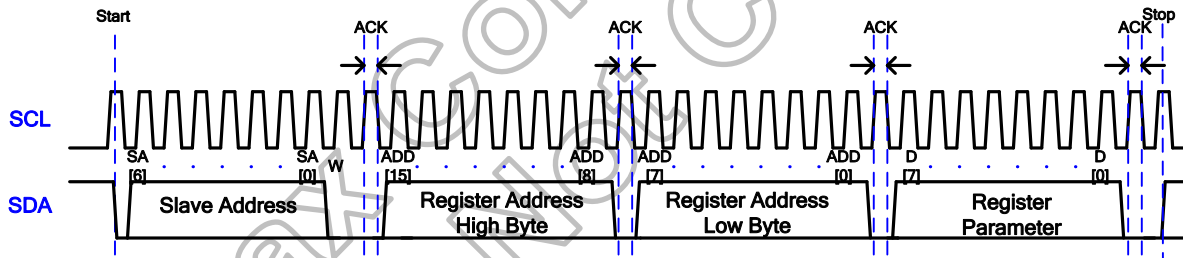
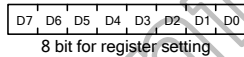
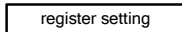
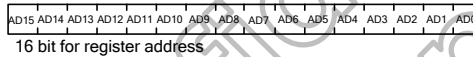
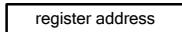
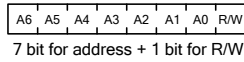
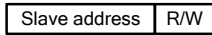


Figure 4.9: I²C interface register write flow

4.3.4 I2C interface read mode

HX8399-C also supports I2C to read data from register. The write flow is described as below:

- A. Send Start condition followed by I2C 7-bit slave address and 1 bit '0'(write flag)
- B. Send High byte of 16-bit address, then IC feedback Ack.
- C. Send Low byte of 16-bit address, then IC feedback Ack.
- D. Send restart condition followed by I2C 7-bit slave address and 1 bit '1'(read flag)
- E. Send register data to baseband, and followed by a non-ack.
- F. Send Stop condition

S	Slave Address	0	A	ADD[15]... ADD[8]	A	ADD[7]... ADD[0]	A	Sr	Slave Address	1	A	Read Data	\bar{A}	P
---	---------------	---	---	----------------------	---	---------------------	---	----	---------------	---	---	-----------	-----------	---

- From master to slaver
- From slaver to master

Master ? ex: MPU,DSP...control chip

Sr = ReStart

Slave address	R/W
---------------	-----

register address

A = Acknowledge (SDA =Low)
 A = Not acknowledge (SDA =High)
 S = Start condition
 P = Stop condition

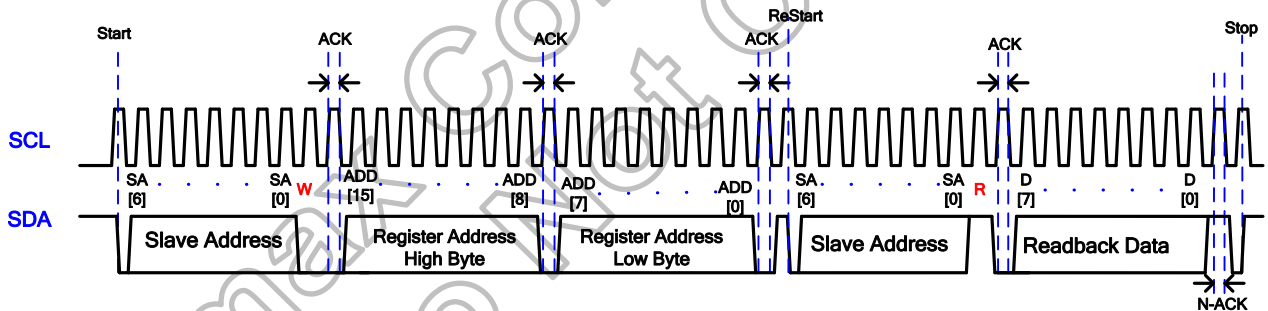
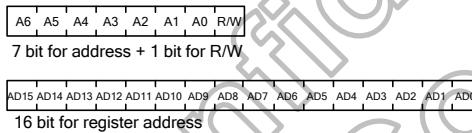


Figure 4.10: I²C interface register read flow

4.4 DSI system interface

The DSI specifies the interface between a host processor and a peripheral such as a display module. Figure 4.11 shows a simplified DSI interface. From a conceptual viewpoint, a DSI-compliant interface also sends pixels or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events. DSI-compliant peripherals support Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

Command Mode refers to operation in which transactions primarily take the form of sending Commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

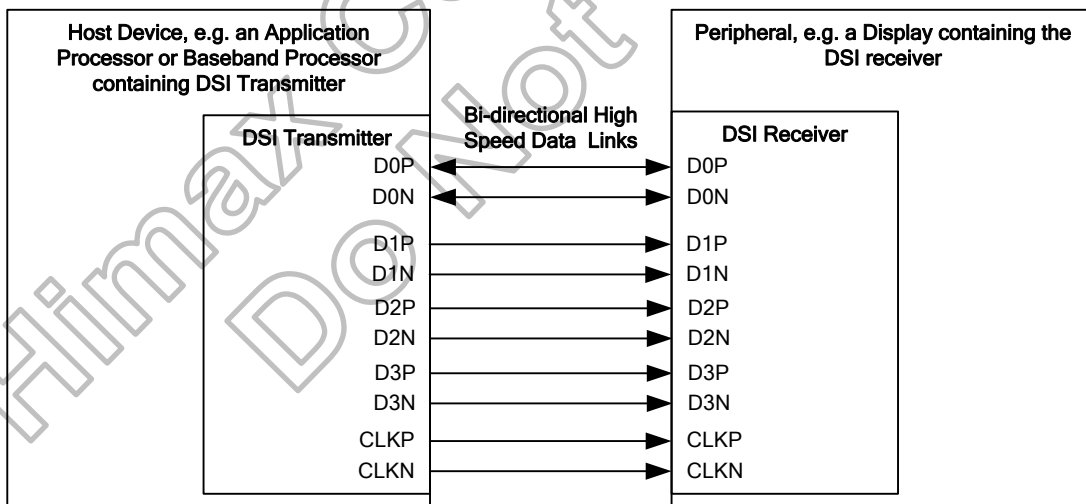


Figure 4.11: DSI transmitter and receiver interface

Please refer to Display Serial Interface Specification which is defined by MIPI Alliance for detail descriptions.

The data lane number is selected by command BAh.

4.4.1 DSI layer definitions

Figure 4.12 is DSI transmitter and Receiver block diagram which includes four parts: PHY Layer, Lane Management Layer, Low level protocol and Application Layer.

The PHY Layer specifies the characteristics of transmission medium and electrical parameters for signaling the timing relationship between clock and Data Lanes.

The Lane Management Layer specifies DSI is Lane-scalable for increased performance. The data signals maybe transmission through one or more channel depending on the bandwidth requirements of the application.

The Protocol Layer specifies at the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets.

The Application Layer describes higher-level encoding and interpretation of data contained in the data stream. The DSI specification describes the mapping of pixel values, commands and command’s parameters to bytes in the packet assembly.

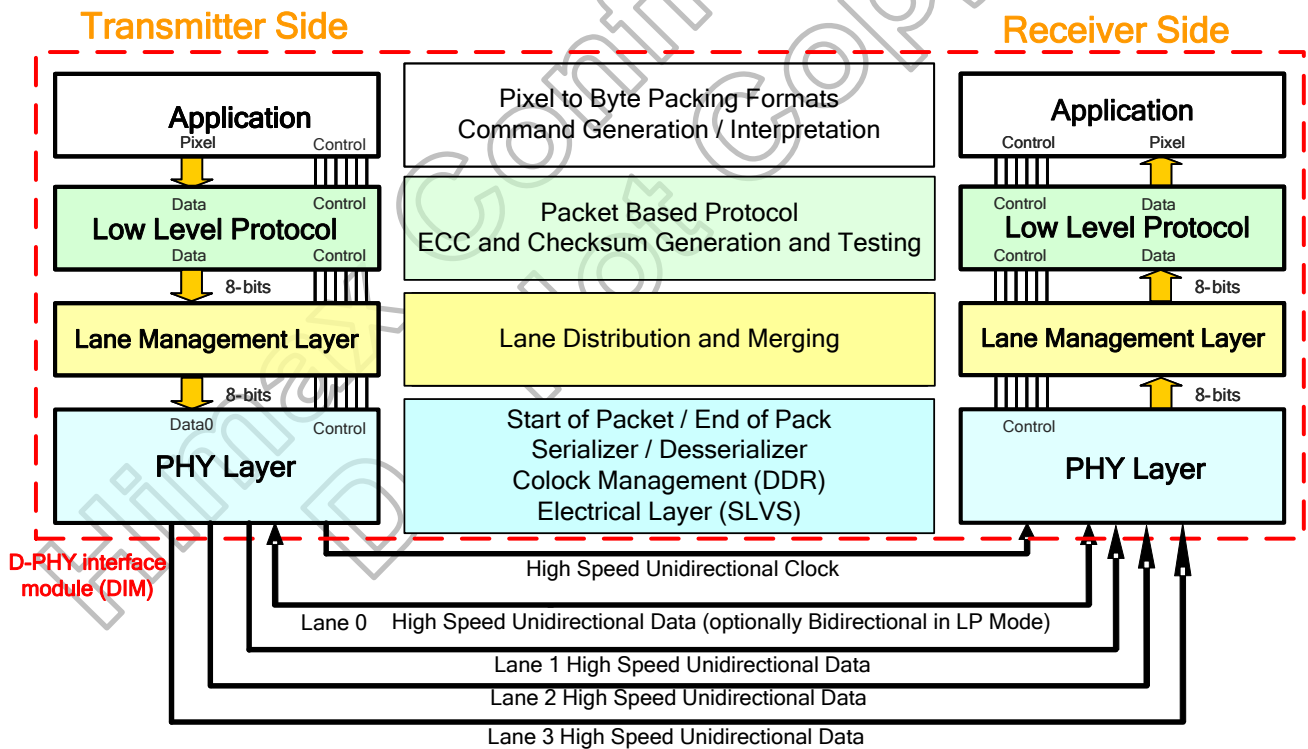


Figure 4.12: DSI transmitter and receiver interface

4.4.1.1 Lane States

The HX8399-C uses Data Lane and Clock Lane differential pairs for DSI. Both differential lane pairs can be driven LP (Low Power) or HS (High Speed) mode.

LP mode means each line of the differential pairs are used in independently and single-ended. In LP mode differential receiver is disable (termination resistor of the receiver is disable). In LP mode there are four possible Low-Power Lane states (LP-00, LP-01, LP-10, LP-11).

HS mode means the differential pairs are not used in single-end and termination resistor of the receiver is enabling. There are different modes and protocol in each mode when transfer display data from MCU to the display module.

The state code of HS and LP Lane pair are defined as below:

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	Note ⁽¹⁾	Note ⁽¹⁾
HS-1	HS High	HS Low	Differential-1	Note ⁽¹⁾	Note ⁽¹⁾
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	Note ⁽²⁾

Note1: During High-Speed transmission the Low-Power Receivers observe LP-00 on the Lines.

Note2: If LP-11 occurs during Escape mode the Lane returns to Stop state (Control Mode LP-11)

4.4.1.2 Clock Lane Mode

Figure 4.13 shows the state diagram for Clock Lane Mode. The Clock Lane has three different power modes: Low Power Stop State, Ultra Low Power State (ULPS) and High Speed clock transmission.

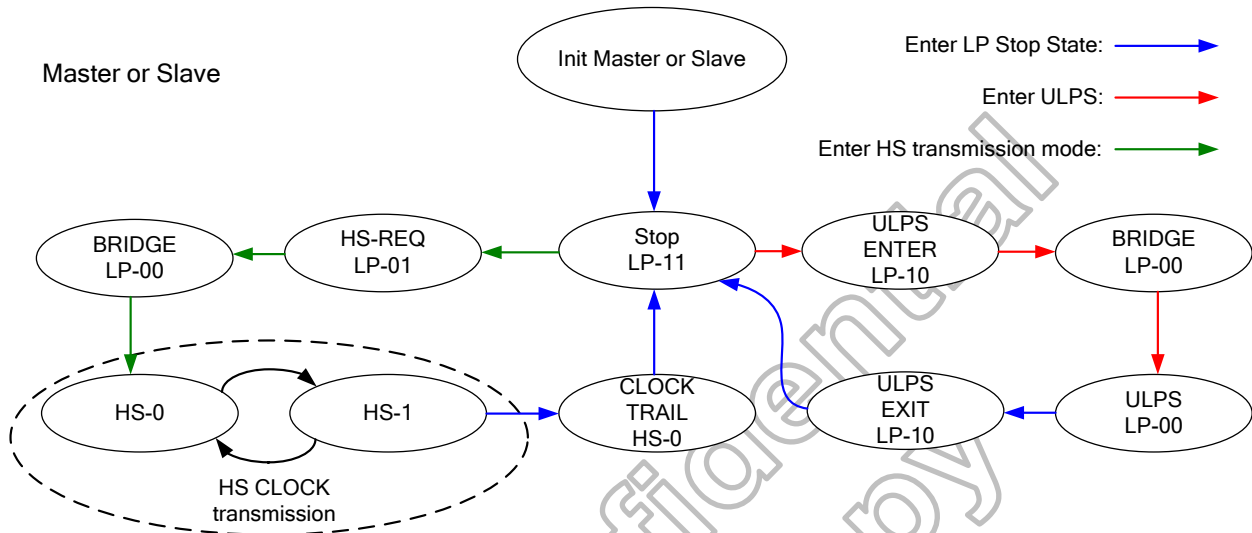
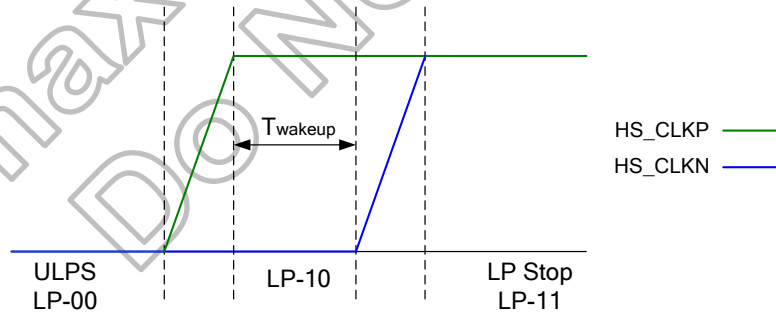


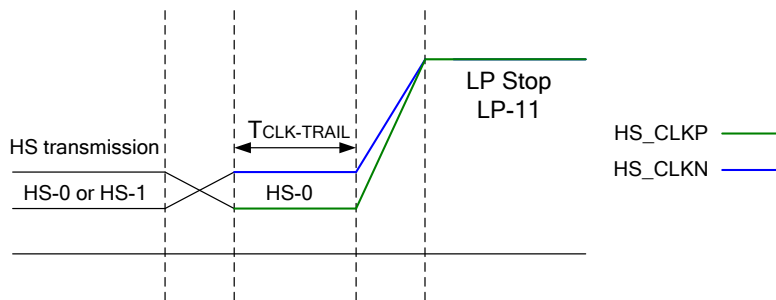
Figure 4.13: Clock Lane Mode State diagram

Clock Lane can be driven LP-11 to enter Low Power Stop State. There are three ways to enter Lower Power Stop State:

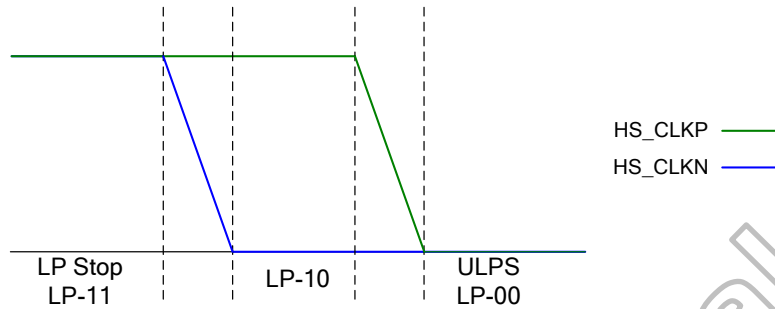
- A. After Initial state (HW reset, SW reset, Power on sequence).
- B. Leaving ULPS: ULPS LP-00 → LP-10 → Low Power Stop State LP-11.



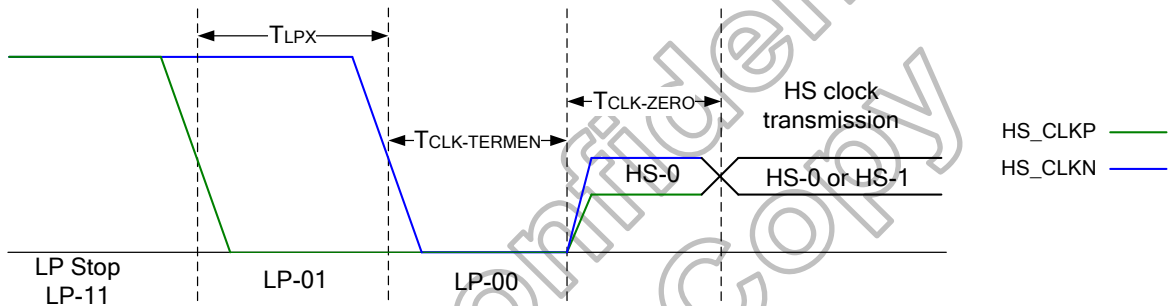
- C. Leaving HS clock transmission mode: HS mode (HS-0 or HS-1) → HS-0 → Low Power Stop State LP-11.



Clock lane can be driven LP-00 to enter ultra low power state from low power stop state. The flow is low power stop state LP-11 → LP-10 → ULPS LP-00.



Clock lane can be high speed clock transmission state from low power stop state. The flow is low power stop state LP-11 → LP-01 → LP-00 → HS-0/1.



4.4.1.3 Data Lane Mode

Figure 4.14 shows the operational flow diagram for Data Lane Mode. There are three operating modes in Data Lane: Escape mode, High-Speed transmission mode and Turnaround.

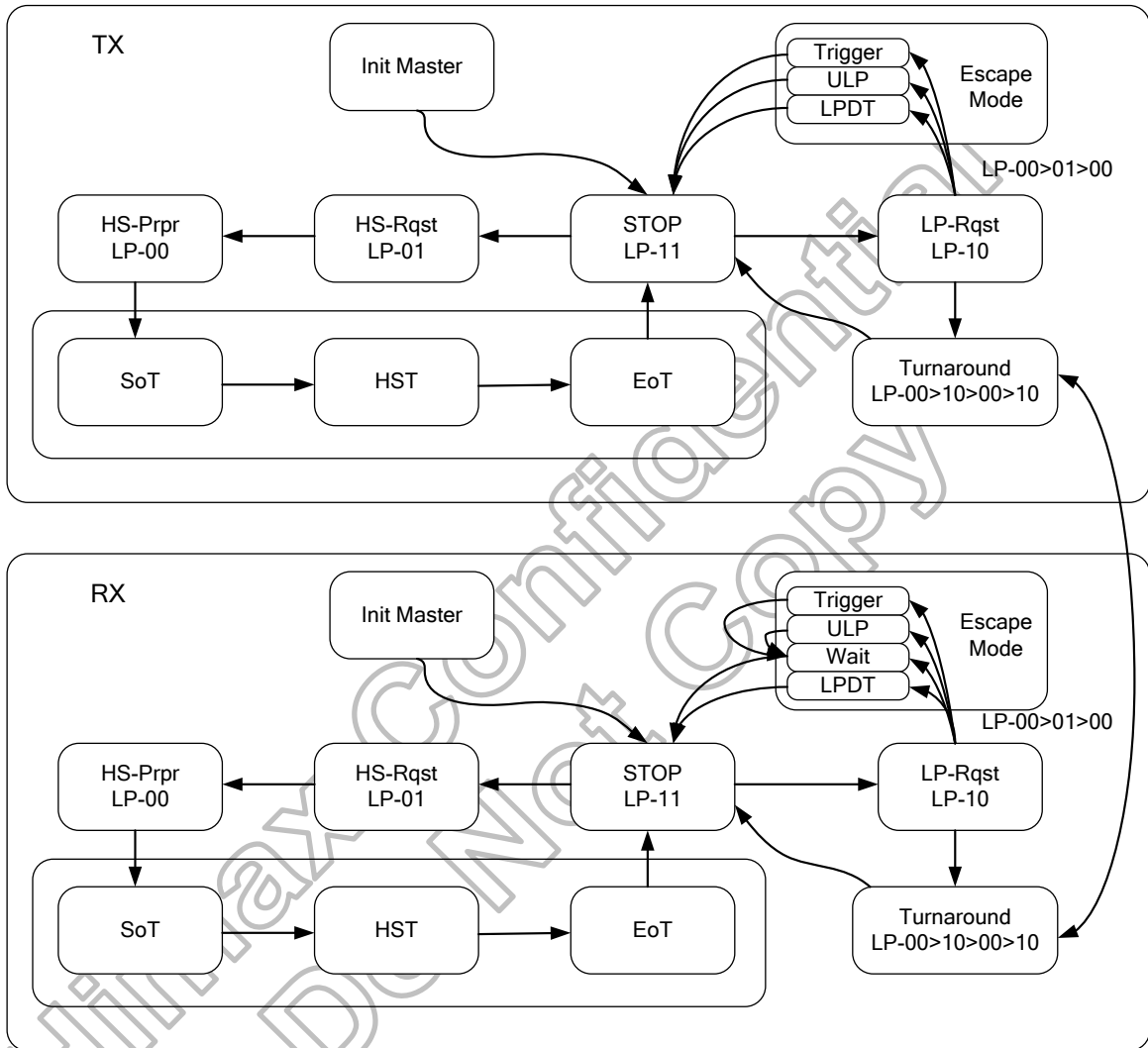


Figure 4.14: Data Lane Mode State diagram

4.4.1.3.1 Escape Mode

Data Lane0 is used in Escape Mode when data lane in LP mode. Data Lane shall enter Escape mode via LP-11 → LP-10 → LP-00 → LP-01 → LP-00 and exit Escape mode via LP-10 → LP-11.

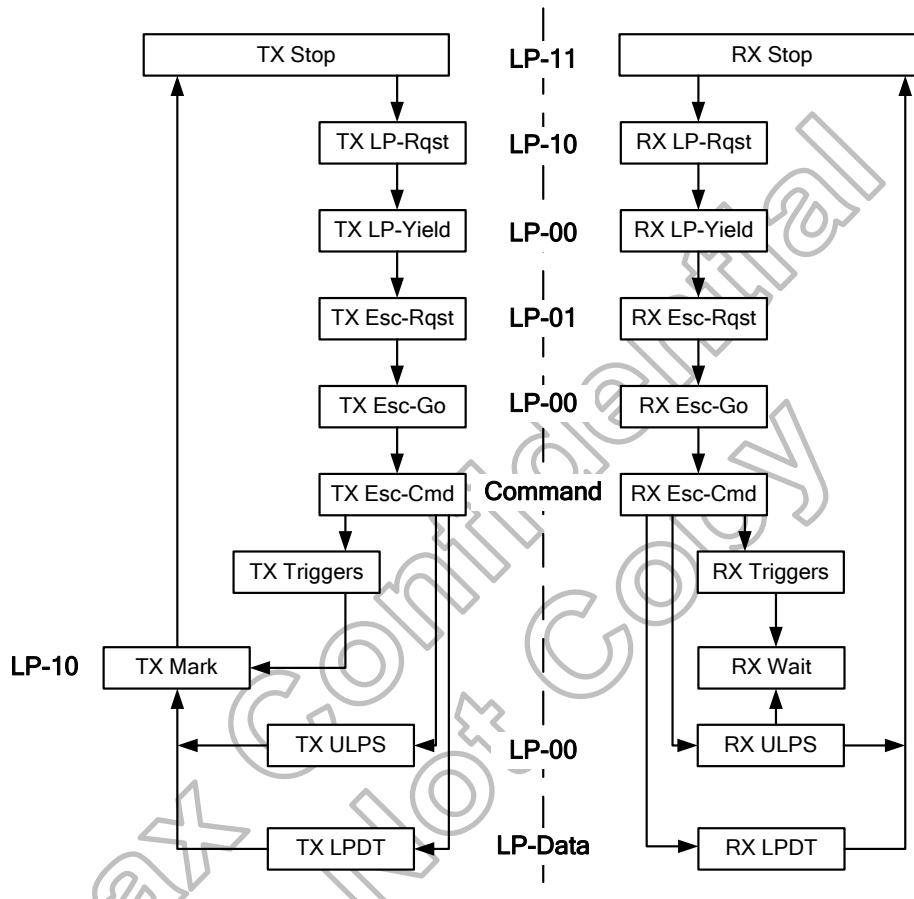


Figure 4.15: Escape Mode State Machine

Once Escape mode is entered, the transmitter shall send an 8-bit entry code to indicate the requested action. The Entry Code as follows:

- A. Trigger (Reset-Trigger(46h), Tearing effect(BAh), Acknowledge(84h))
- B. Drive Data Lane to Ultra Low Power State (78h)
- C. Send Low Power Data Transmission (87h)

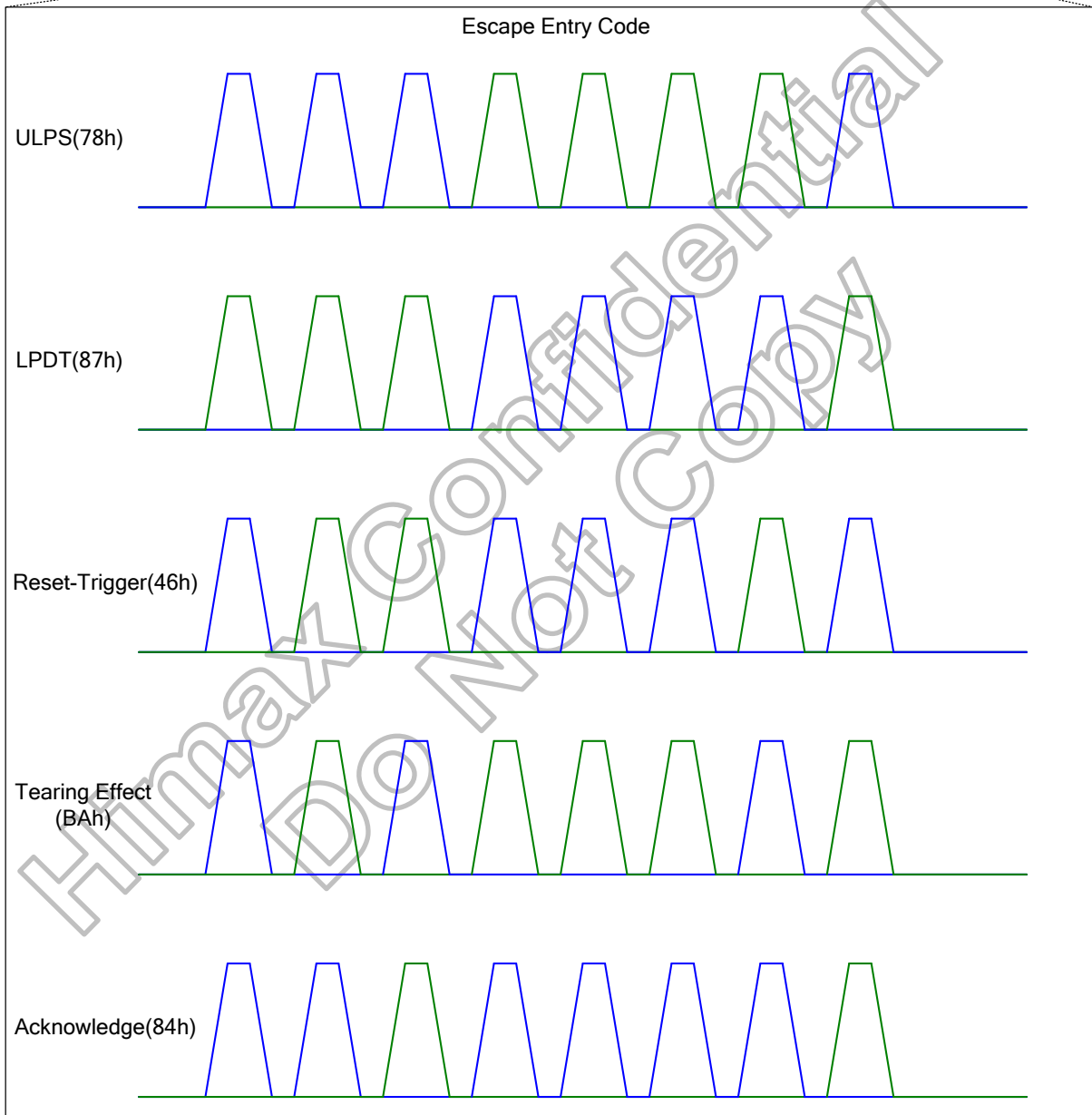
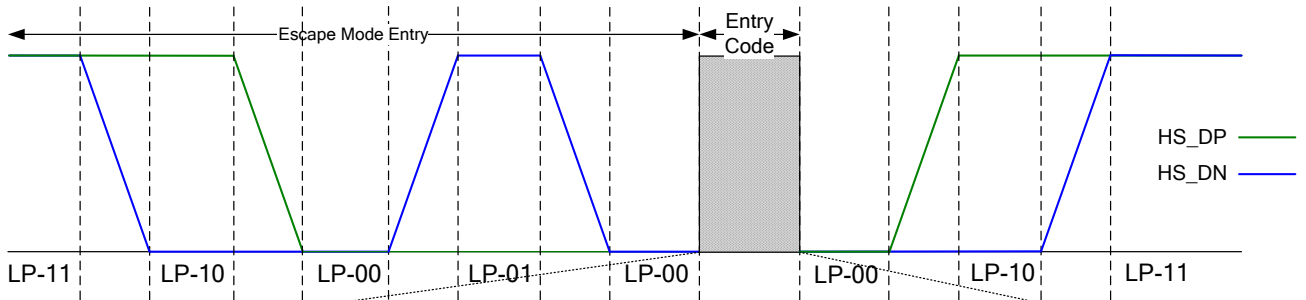


Figure 4.16: Escape Mode timing sequence

4.4.1.3.2 High speed data transmission

The display module can enter High Speed Data Transmission when Clock Lane in the High Speed Clock Mode. All Data Lane enter High Speed Data Transmission synchronously but may end at different time. Data Lane enters High Speed Data Transmission by the flow: LP-11 → LP-01 → LP-00 → SoT(HS-00011101). And exit High Speed Data Transmission flow: Toggles differential state immediately after last payload data bit and keeps that state for a time $T_{HS-TRAIL}$.

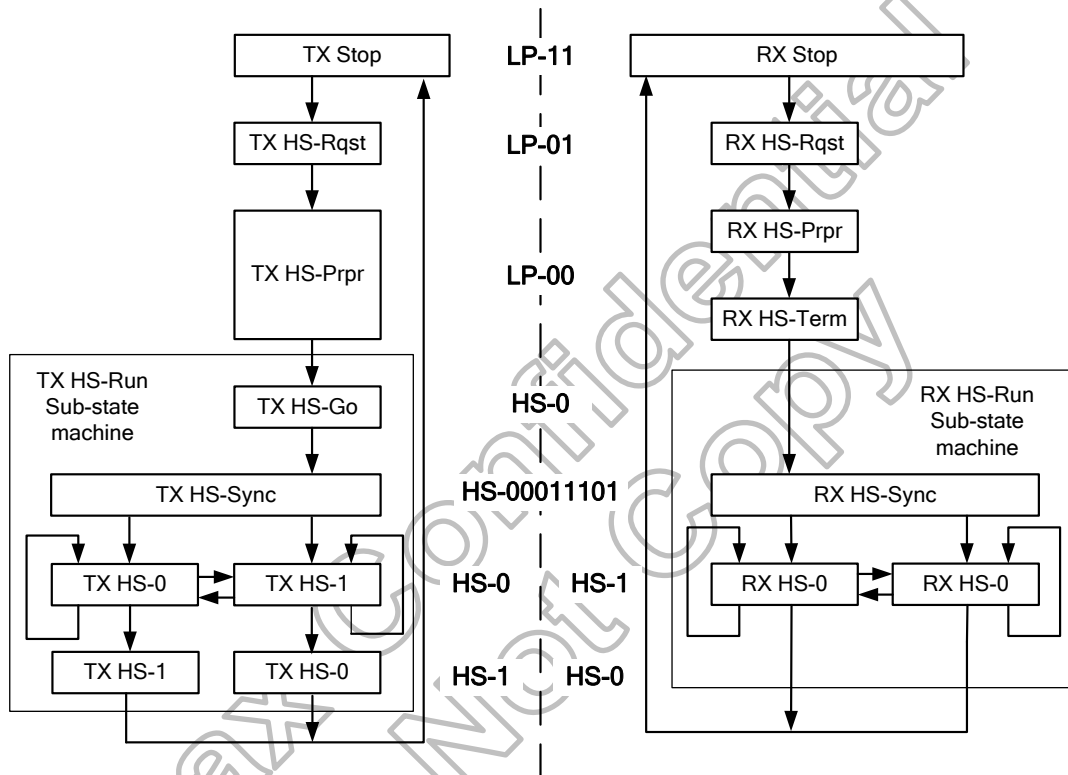


Figure 4.17: High Speed Data Transmission State Machine

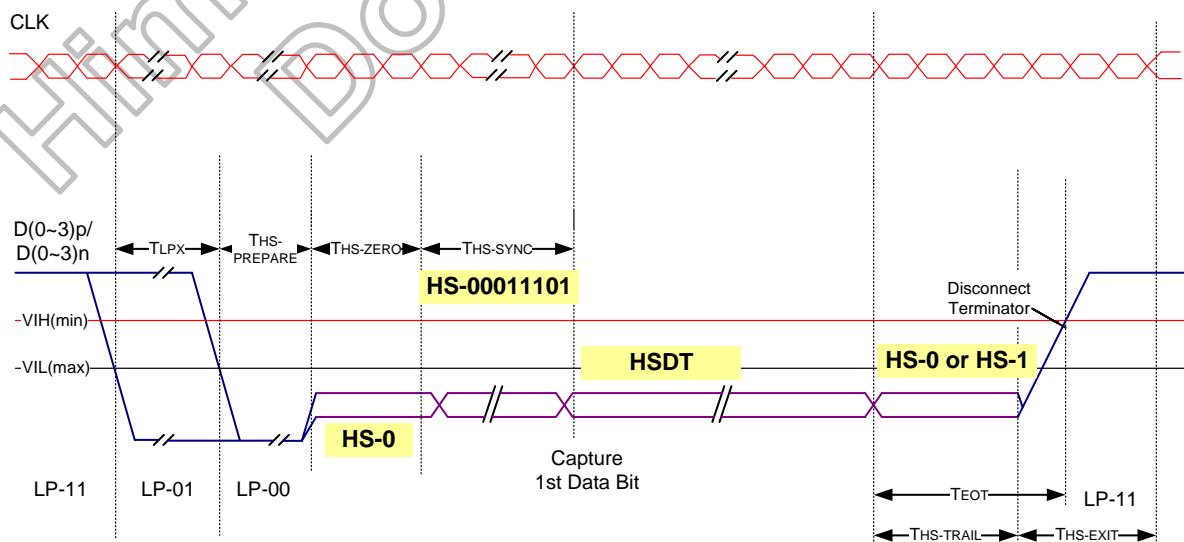


Figure 4.18: High Speed Data Transmission timing sequence

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	$40+4*UI$	-	$85+6*UI$	ns
$T_{HS-PREPARE}^+$ $T_{HS-ZERO}$	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	$145+10*UI$	-	-	ns
T_{EOT}	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst.	-	-	$105ns+12*UI$	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	$60ns+4*UI$	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

Table 4.4: Global operation timing parameters for data lane

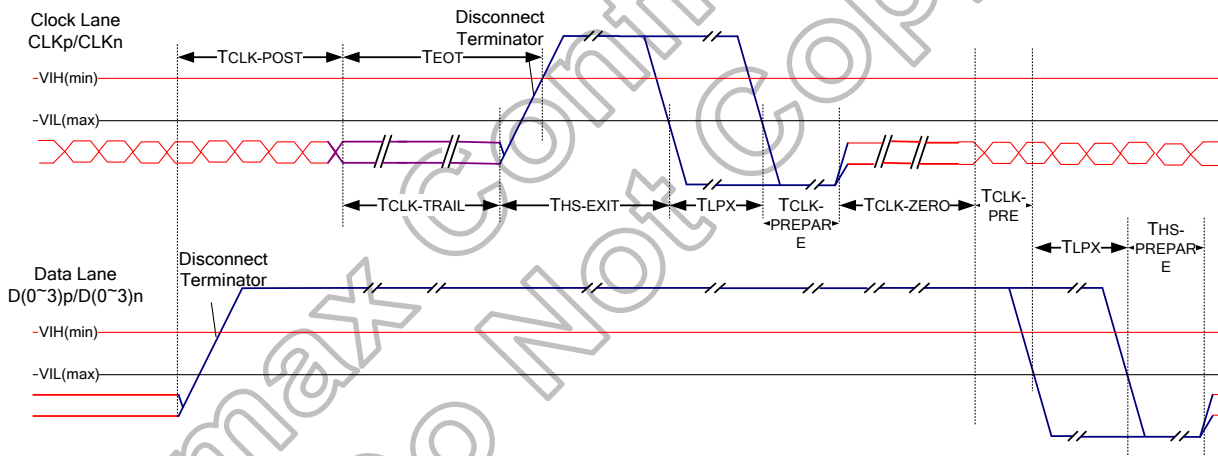


Figure 4.19: Switching the clock lane between clock transmission and LP mode

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
T _{CLK-POST}	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60+52*UI	-	-	ns
T _{CLK-TRAIL}	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	60	-	-	ns
T _{CLK-PREPARE}	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	38	-	95	ns
T _{CLK-PREPARE+CLK-ZERO}	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
T _{CLK-PRE}	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns

Table 4.5: Global operation timing parameters for clock lane

4.4.1.3.3 Bi-directional data lane turnaround

The transmission direction OD a bi-directional data Lane can be swapped by means of a link turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction.

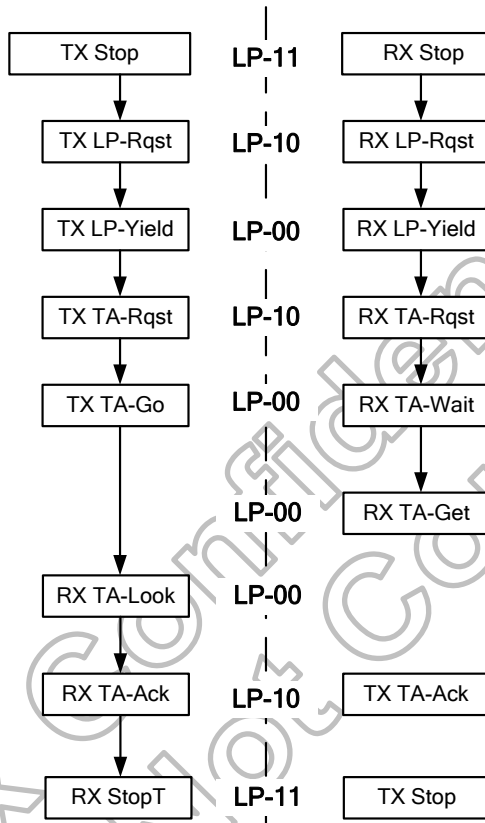


Figure 4.20: Turnaround State Machine

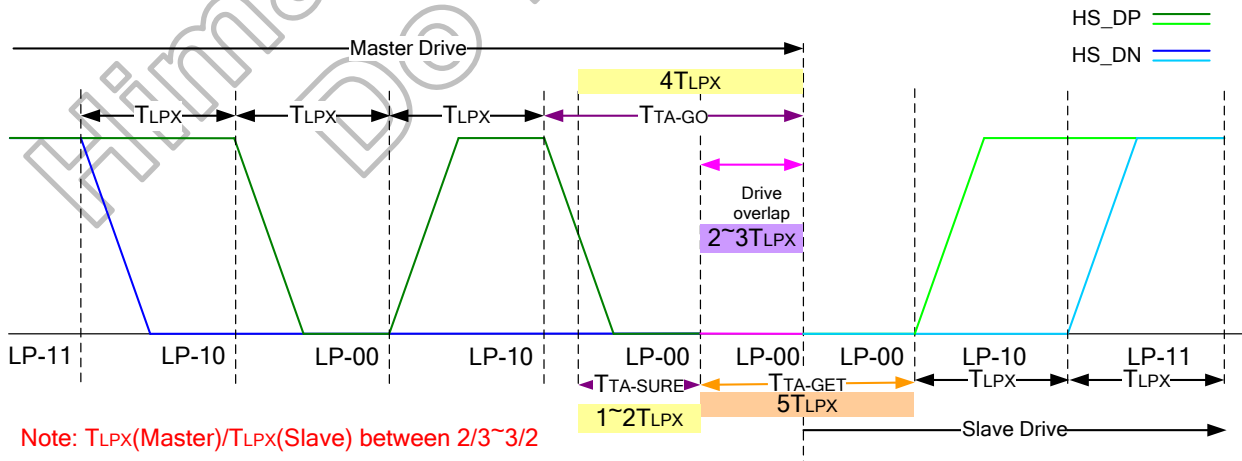
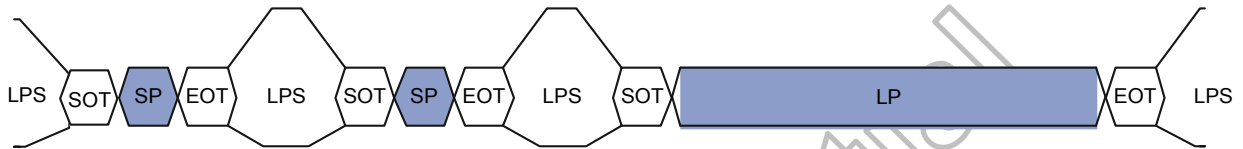


Figure 4.21: Turnaround timing sequence

4.4.2 DSI protocol

The protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded with separate write commands at system startup. Figure 4.22 illustrates multiple HS Transmission packets.

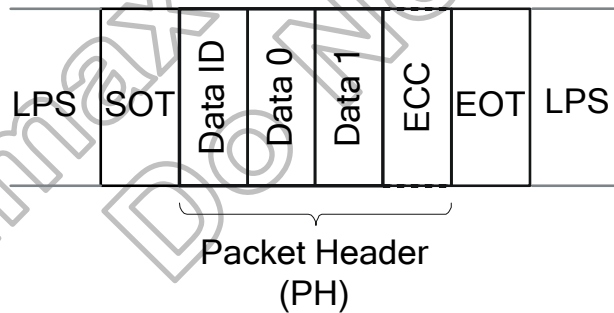


- Note:** (1) a. LPS : Low power state
 b. SOT : Start of Transmission
 c. SP : Short Packet
 d. LP : Long Packet
 e. EOT : End of Transmission

Figure 4.22: Multiple HS transmission packets

The packet includes two types which are Long packet and short packet. The first byte of the packet, the Data Identifier (DI), includes information specifying the length of the packet.

Short packets shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length. Figure 4.23 shows the structure of the Short packet.

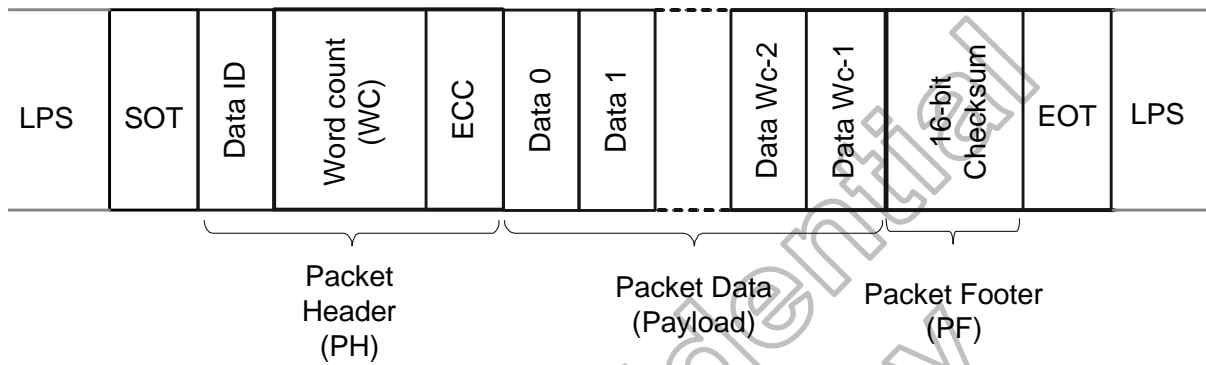


- Note:** (1) a. DI (**Data ID**) : Contain Virtual Channel Identifier and Data Type.
 b. ECC (**Error Correction Code**) : The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

Figure 4.23: Structure of the short packet

Long packets specify the payload length using a two-byte Word Count Field and then the payload maybe from 0 to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data. Figure 4.24 shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

Where 65,541 bytes = $(2^{16}-1) + 4$ bytes PH + 2 bytes PF



- Note:** (1) a. DI (**Data ID**) : Contain Virtual Channel Identifier and Data Type.
 b. WC (**Word Count**) : The receiver use WC to define packet end.
 c. ECC (Error Correction Code) : The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.
 d. PF (**Packet Footer**) : Mean 16-bit Checksum.

Figure 4.24: Structure of the long packet

According to packet form, basic elements include DI and ECC. Figure 4.25 the shows format of Data ID.

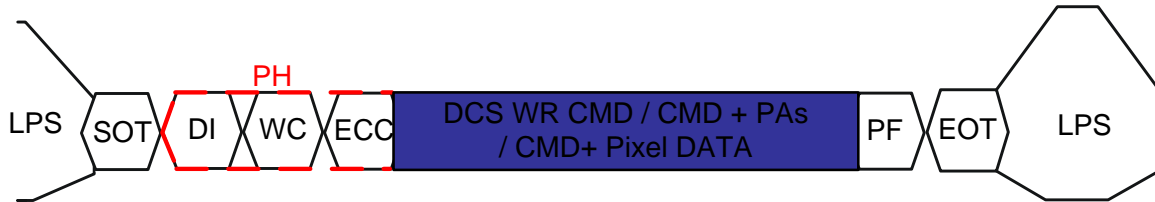
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC (Virtual Channel)		DT (Data Type)					

- Note:** (1) a. DI[7:6]: These two bits identify the data as directed to one of four virtual channels.
 b. DI[5:0]: These six bits specify the Data Type, which specifies the size, format and, in some cases, the interpretation of the packet contents.

Figure 4.25: The format of data ID.

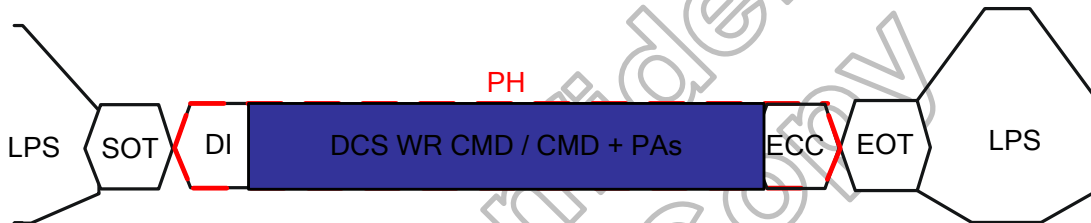
Figure 4.26 show short/long–packet transmission command sequence.

Long packet writes Command / Parameters / Pixel data



- DI → Write suitable Data type.
- WC → Write number of Payload Data.
- Ex: One CMD write, WC setting as 1.
- CMD + PAs write, WC setting as number of (CMD+PAs).
- CMD + DATA write, WC setting as number of (CMD + Pixel DATA).

Short packet writes Command / Parameters



- DI → Write suitable Data type.
- Ex: One CMD write, DI + DCS WR CMD
- CMD + PAs write, DI + DCS WR CMD + PAs

Figure 4.26: show Short- / Long-packet transmission command sequence

4.4.3 Processor to peripheral direction packets data types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 4.6 Data Types for Processor-sourced Packets.

Data type, hex	Data type, binary	Description packet	Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
05h	00 0101	DCS WRITE, no parameter	Short
15h	01 0101	DCS WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
X0h and XFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	-

Table 4.6: Data types for processor-sourced packets

Under tables list all detail function of all data types

Sync event (H start, H end, V start, V end), data type=xx 0001 (x1h)		
Data type, hex	Function description	Number of bytes
01h	V Sync start, Start of VSA pulse.	4 bytes (DI+Data0+Data1+ECC)
11h	V Sync End, End of VSA pulse.	
21h	H Sync Start, Start of HSA pulse.	
31h	H Sync End, End of HSA pulse.	

Note: (1) V Sync Start and V Sync End event represents the start and end of the VSA, respectively. Similarly H Sync Start and H Sync End event represents the start and end of the HSA, respectively.

EoT Packet		
Data type, hex	Function description	Number of bytes
08h	End of Transmission Packet (EoTp) (08,0F,0F,01)	4 bytes (DI+Data0+Data1+ECC)

Note: (1) The main objective of the EoTp is to enhance overall robustness of the system during HS transmission mode. Therefore, DSI transmitters should not generate an EoTp when transmitting in LP mode.

Color Mode Off /On Command		
Data type, hex	Function description	Number of bytes
02h	Color Mode Off Packet (02,00,00,0B)	4 bytes (DI+Data0+Data1+ECC)
12h	Color Mode On Packet (12,00,00,18)	

Note: (1) Color Mode Off is a Short packet command that returns a Video Mode display module from low-color mode to normal display operation. Color Mode On is a Short packet command that switches a Video Mode display module to a low-color mode for power saving.

Display Status (shutdown command, turn-on command)		
Data type, hex	Function description	Number of bytes
22h	Shutdown Peripheral Packet (22,00,00,1E)	4 bytes (DI+Data0+Data1+ECC)
32h	Turn On Peripheral Packet (32,00,00,0D)	

Note: (1) Shutdown Peripheral command that turns off the display in a Video Mode display for power saving. Turn On Peripheral command that turns on the display in Video Mode display for normal display.

DCS Short Write Packet (0,1 parameter)		
Data type, hex	Function description	Number of bytes
05h and 15h	DCS Short Write command, 0 or 1 parameter, Data Types=000101(05h), 010101(15h), Respectively.	4 bytes (DI+Data0+Data1+ECC)

Note: (1) For write part, If DCS Short Write command, followed by BTA (Bus Turn-Around), the peripheral shall respond with ACK when without error was detected in the transmission (Host → Slave). Unless an error was detected, the peripheral shall respond with Acknowledge with Error Report.

For example: 05h DCS WRITE for no parameter command set.

05h	CMD	0	ECC
-----	-----	---	-----

Ex. 05h, 29h, 00, 1Ch || Display On(29h)

For example: 15h DCS WRITE for only one parameter command set.

15h	CMD	Par	ECC
-----	-----	-----	-----

Ex. 15h, 36h, 08h, 11h || MADCTL(36h)-BGR bit=1

DCS Read Request, No Parameter		
Data type, hex	Function description	Number of bytes
06h	DCS Read Request, the returned data may be of Short or Long packet format.	4 bytes (DI+Data0+Data1+ECC)

- Note:** (1) When use DCS Read Command, the **Set Max Return Packet Size** command will limit the size of returning packets.
 (2) The peripheral shall respond to DCS Read Command Request in one of the following ways:
- If an error was detected by the peripheral, it shall send *Acknowledge with Error Report*. So the peripheral shall transmit the requested READ data packet with suitable ECC in the same transmission.
 - If no error was detected by the peripheral, it shall send the requested READ packet (**Short or Long**) with appropriate ECC and Checksum, if either or both features are enabled.
- (3) **One byte <= Length of payload DATA <= 2^{WC}-1**

Return Packet Size Setting		
Data type, hex	Function description	Number of bytes
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.	4 bytes (DI + WC + ECC)

- Note:** (1) The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.

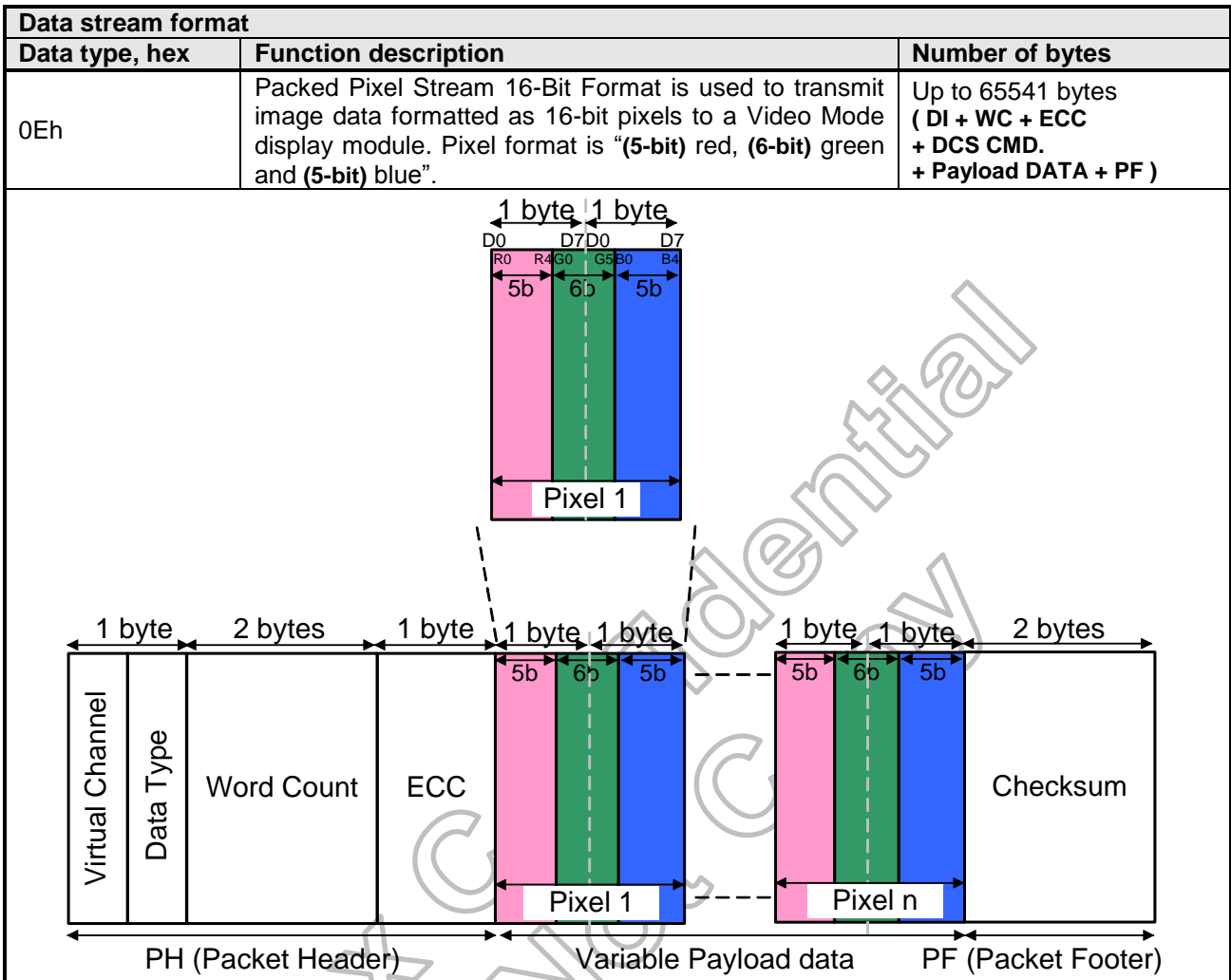
Null Packet and Blanking packet		
Data type, hex	Function description	Number of bytes
09h	Null Packet is a mechanism for keeping the serial Data Lane(s) in High-Speed mode while sending dummy data.	Up to 65541 bytes (DI + WC + ECC + DCS CMD.+ Payload DATA + PF)
19h	Blanking packet is used to convey blanking timing information in a Long packet.	

- Note:** (1) When **Null Packet**, the Payload Data belong "null" Data, actual data values sent are irrelevant because the peripheral does not capture or store the data.
 (2) When **Blanking packet**, the packet represents a period between active scan lines of a Video Mode display.

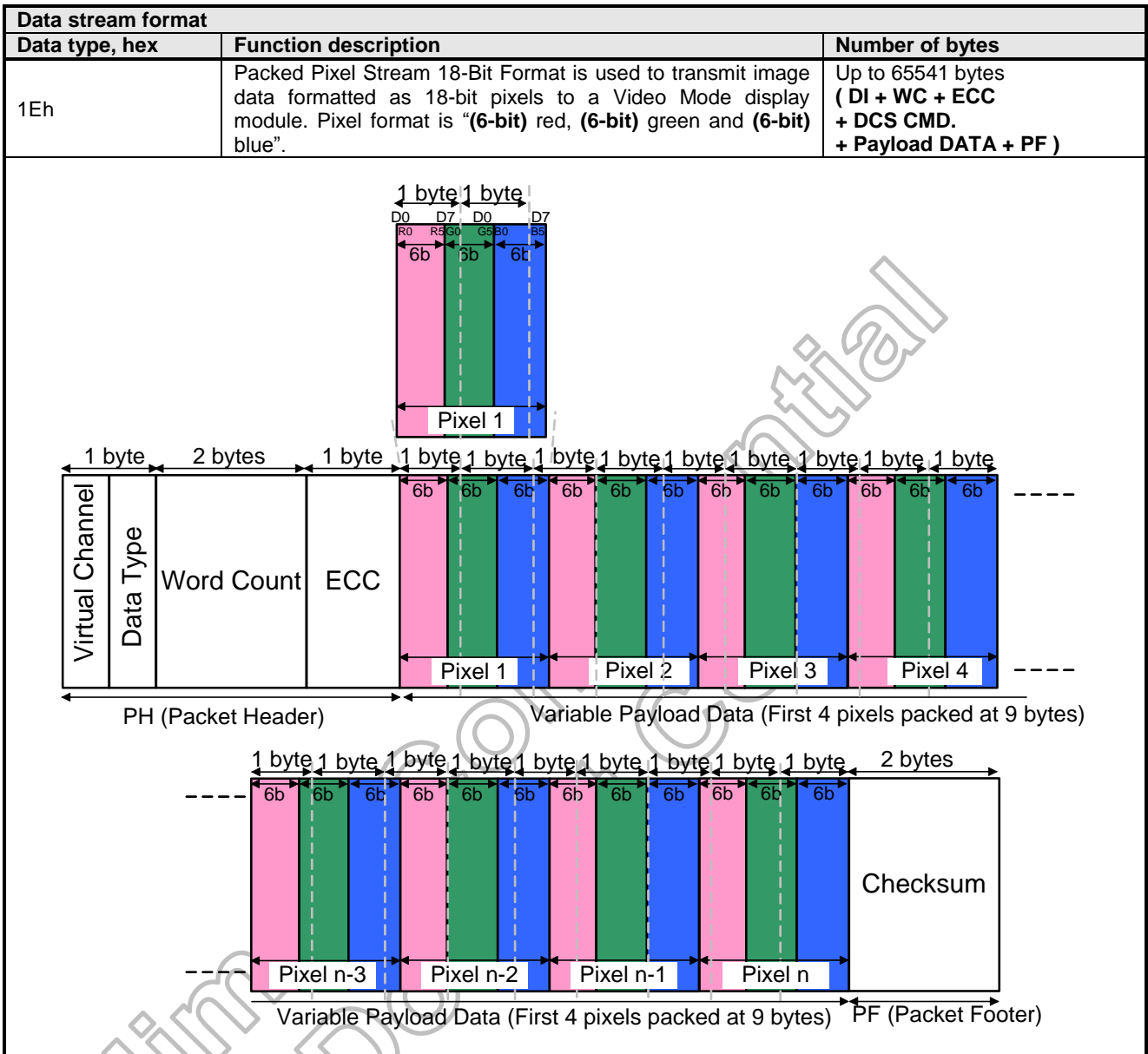
DCS Long Write packet		
Data type, hex	Function description	Number of bytes
39h	DCS Long Write/ Write - LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

Generic Long Write packet		
Data type, hex	Function description	Number of bytes
29h	A: Same as DCS Long Write (39h) B:Continuous Write Function , could be used after 29h / 39h	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

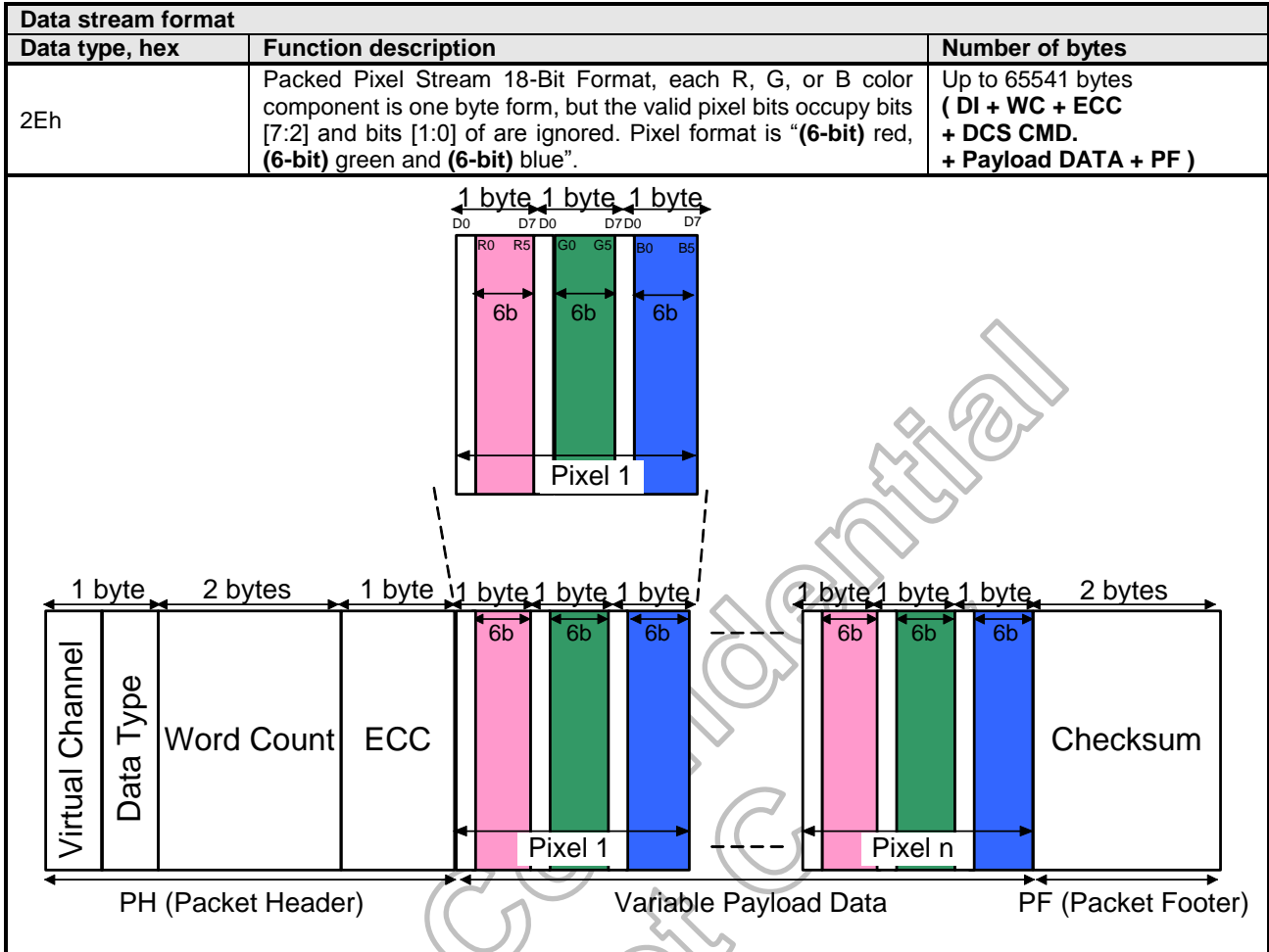
- Note:** (1) For DCS Long Write: Send a NOP or NULL packet in front of 29h to avoid Continuous Write Function beginning.
 (2) For Continuous Write: WC should be 4N+1 and the times of continuous write cannot be over 3 times.



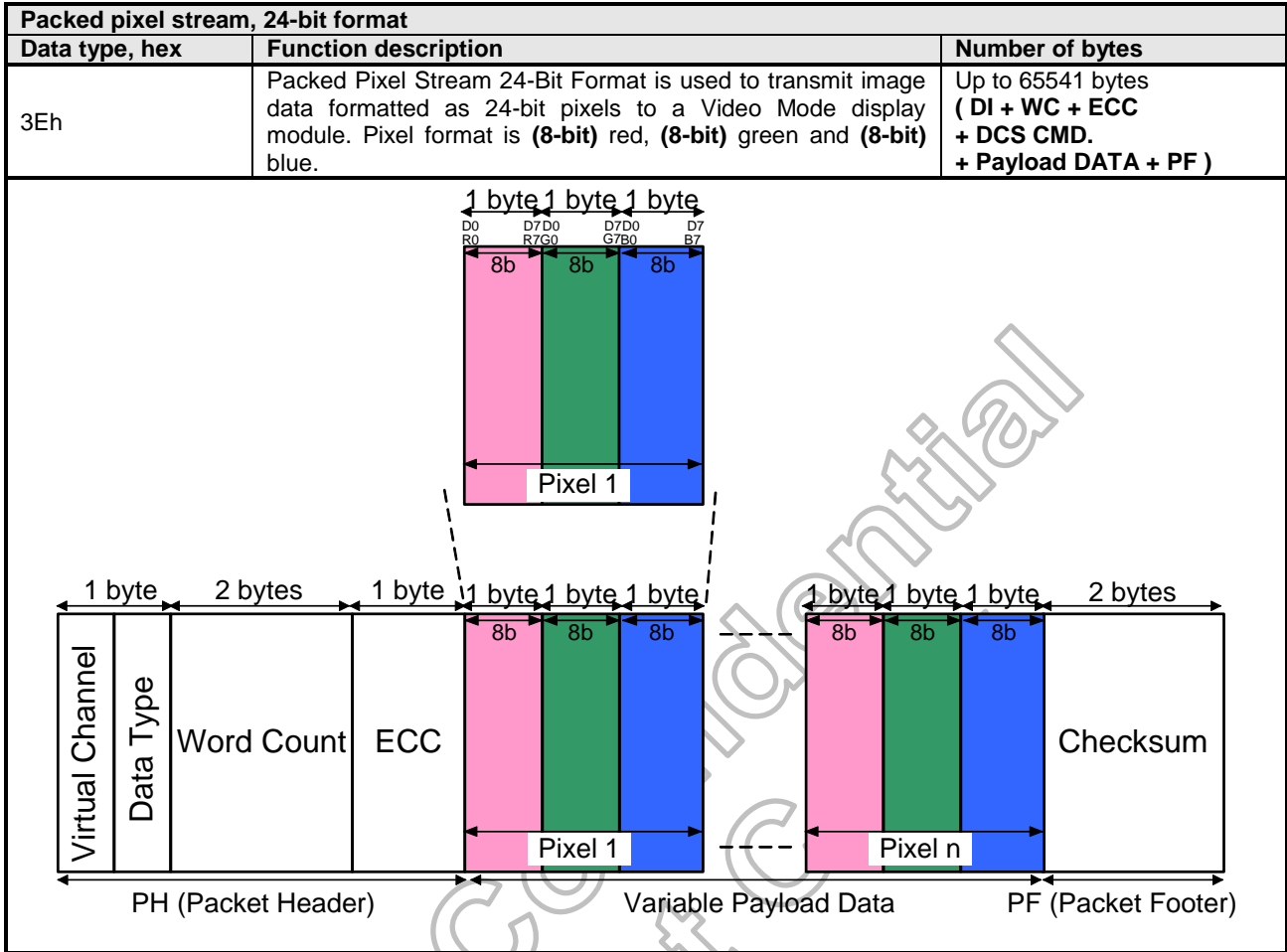
Note: (1) Within a color component, the "LSB is sent first, the MSB last".



Note: (1) Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels (9-byte). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a "clean start" for the next line.



Note: (1) Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.



Note: (1) Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

4.4.4 Peripheral to processor (reverse direction)

All Command Mode systems require bidirectional capability for returning READ data, ACK or error information to the host processor. Command Mode that use DCS shall have a bidirectional data path. Short packets and the header of Long packets may use ECC and Checksum to provide a higher level of data integrity. The Checksum feature enables detection of errors in the payload of Long packets. The packet structure for peripheral-to-processor transactions is the same as for the processor-to-peripheral direction.

Peripheral-to-processor transactions are of four basic types:

- A. *Tearing Effect*: a Trigger message sent to convey display timing information to the host processor.
- B. *Acknowledge*: a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.
- C. *Acknowledge and Error Report*: a Short packet sent if any errors were detected in preceding transmission from the host processor. Once reported, accumulated errors in the error register are cleared.
- D. *Response to Read Request* may be short or Long packet that returns data requested by the preceding READ command from the processor.

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or other error information back to the host processor.

The processor-to-peripheral transactions with BTA asserted, can contain under form.

- A. Following a **non-Read command** in which no error was detected, the peripheral shall respond with Acknowledge.
- B. Following a **Read request** in which no error was detected, the peripheral shall send the requested READ data.
- C. Following a **Read request in which the ECC error** was detected and corrected, the Peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte (**Acknowledge with Error Report**) packet in the same LP transmission. The Error Report shall have the ECC Error flag set.
- D. Following a **non-Read command in which the ECC error** was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte (**Acknowledge with Error Report**) packet, the Error Report shall have the ECC Error flag set.
- E. Following any command in which **SoT Error, SoT Sync Error, EoT Sync Error, LP Transmit Sync Error, checksum error or DSI VC ID Invalid** was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge with Error Report response, with the appropriate error flags set in the two-byte error field. Only the ACK/Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

An error report is comprised of two bytes following the DI byte, with an ECC byte following the error report bytes. Table 4.7 shows the Error Report Bit Definitions. And Table 4.8 list complete set of peripheral-to-processor Data Types.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	reserved
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	LP-TX Timeout Error
6	reserved
7	reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	reserved
14	reserved
15	DSI Protocol Violation

Table 4.7: Shows the error report bit definitions

Data type, hex	Data type, binary	Description packet	Size
02h	00 0010	Acknowledge with Error Report	Short
1Ch	01 1100	DCS Long READ Response	Long
Others (00h→3Fh)	-	Reserved	-

Table 4.8: The complete set of peripheral-to-processor data types

Acknowledge types		
Data type, hex	Function description	Number of bytes
02	Get Acknowledge with Error report when Error occurs from processor transmission.	4 bytes

Note: (1) When processor transmits complete Payload, following signal by BTA, peripheral must respond to processor. With error → Acknowledge with error report, Without error → Acknowledge.

DCS Read types		
Data type, hex	Function description	Number of bytes
1Ch	This is the long-packet response to DCS Long Read Request.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

Note: (1) If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h. If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet be sent.

5. Function Description

5.1 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize frame memory writing when displaying video images.

Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

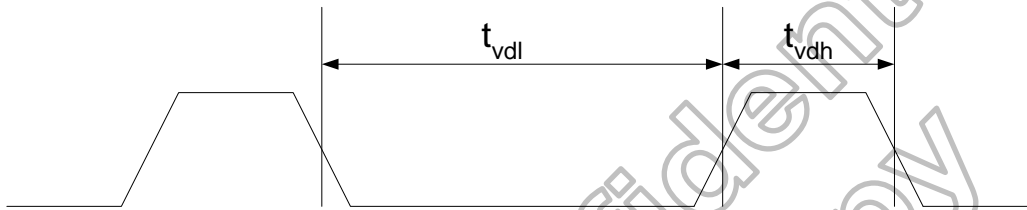


Figure 5.1: Tearing effect output signal mode 1

tvdh= The LCD display is not updated from the Frame Memory

tvdL= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Under Mode1, the TE output timing will be defined by TEP[10:0] setting.

Ex: 1. VFB + VS + VBP = 6 line.

TEP[10:0] = 0, then TE signal will output after last line finished.

TEP[10:0] = 7, then TE signal will output at second line start.

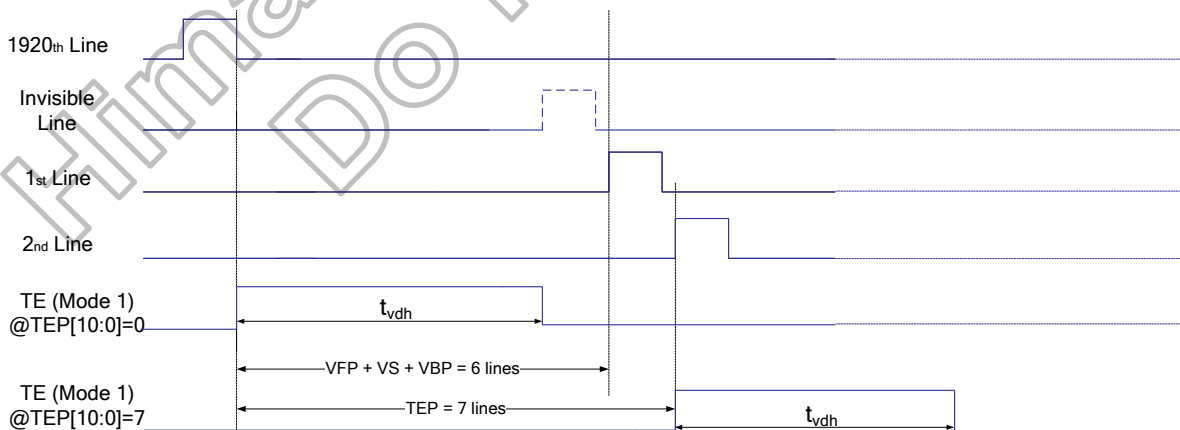


Figure 5.2: TE delay output

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and N H-sync pulses per field.

N: The resolution is 1080 RGB X 1920, the N=1920.

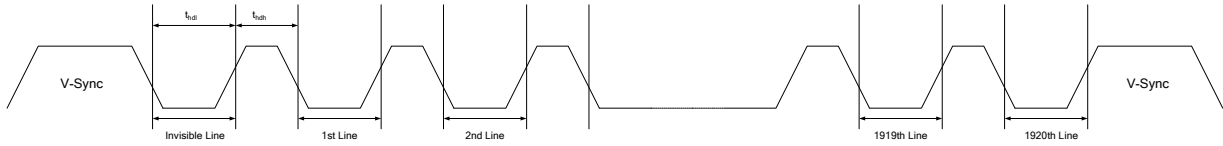


Figure 5.3: Tearing effect output signal mode 2

t_{vdh}= The LCD display is not updated from the Frame Memory

t_{hdl}= The LCD display is updated from the Frame Memory (**except Invisible Line – see above**)

Under Mode2, the H-sync pulses output amount will be defined by TESL[15:0] setting.

Ex: 1. TESL[15:0] =0, then TE signal will like TE mode 1.

TESL[15:0] =1, then TE signal will output 1920 H-sync.

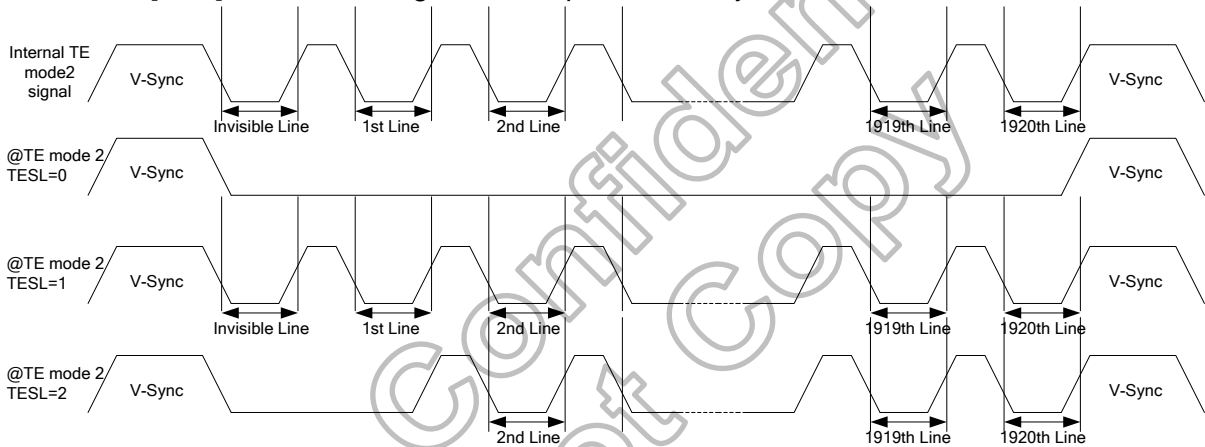
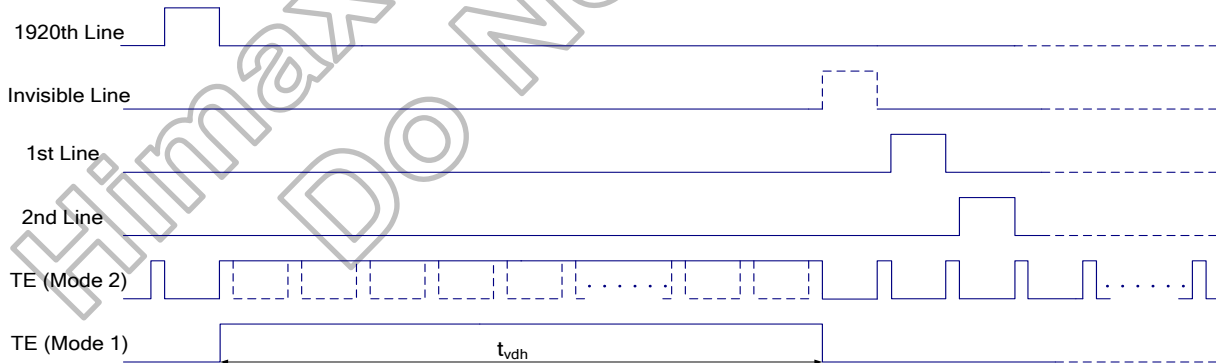


Figure 5.4: TE output for TELINE setting



Note: (1) During Sleep in Mode, the Tearing Output Pin is active Low

Figure 5.5: Tearing effect output signal

5.1.1 Tearing effect line timing

The Tearing Effect signal is described below:

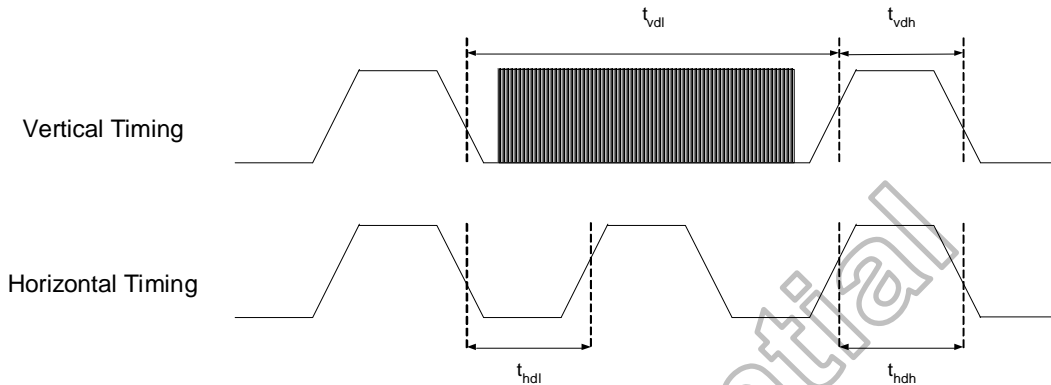


Figure 5.6: Tearing effect output line-tearing effect line timing

Idle Mode off (Resolution 1080x1920 RGB, Frame Rate=60Hz)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Rise time	t_r	-	-	15	ns
Fall time	t_f	-	-	15	ns

Table 5.1: AC characteristics of tearing effect signal

The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.

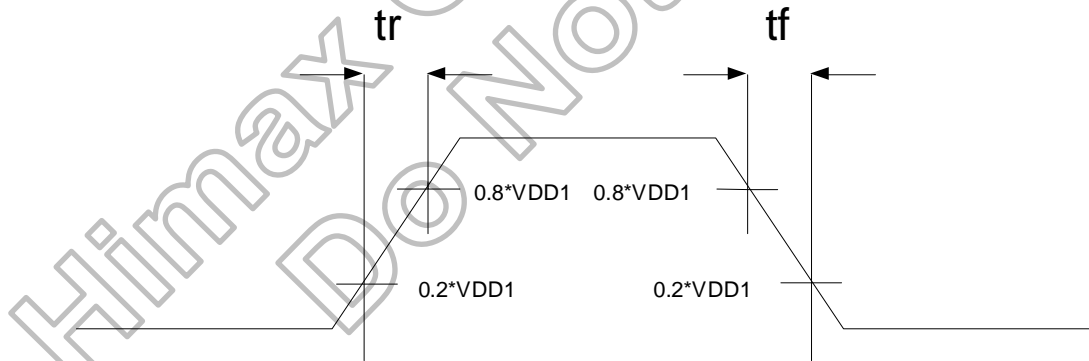


Figure 5.7: Tearing effect output line-definition of t_f , t_r

5.2 Oscillator

The HX8399-C can oscillate an internal R-C oscillator with an internal oscillation resistor (**Rf**). The oscillation frequency is changed according to the UADJ[4:0] internal register. Please refer to OSC control register. The default frequency is 100 MHz.

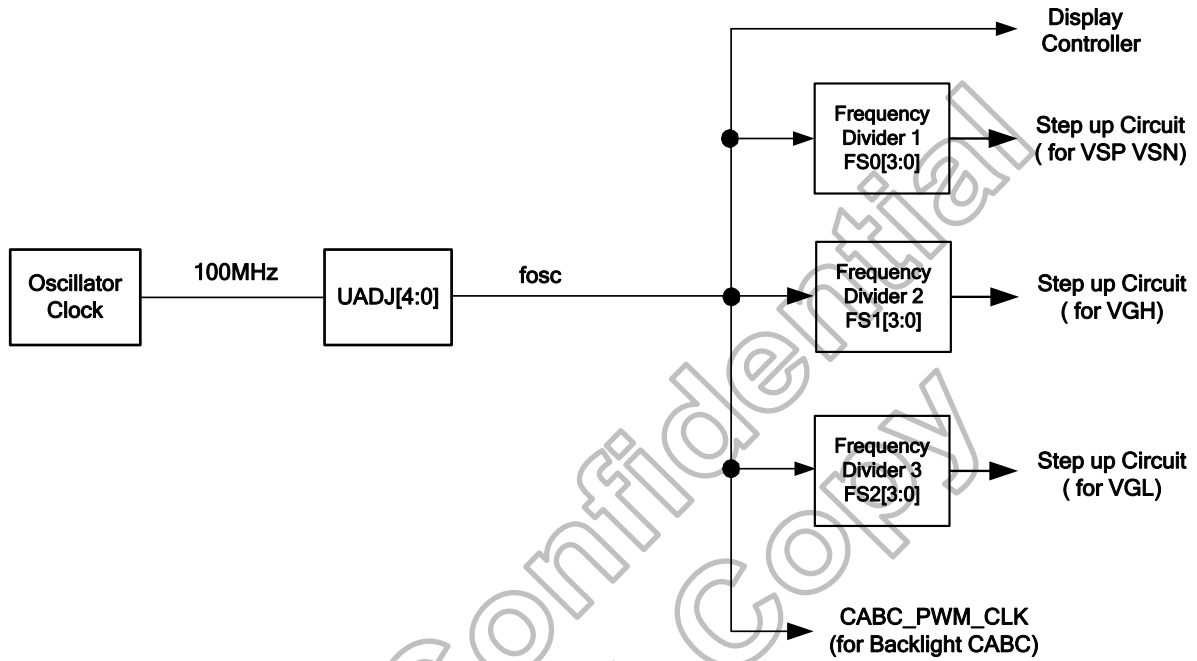


Figure 5.8: OSC aritecture

5.3 Source driver

The HX8399-C contains 1202 channels of source driver which is used for driving the source line of TFT LCD panel. The source driver converts the input digital data into the analog voltage for 1202 channels and generates corresponding gray scale voltage output, which can realize a 16.7M colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

Himax Confidential
Do Not Copy

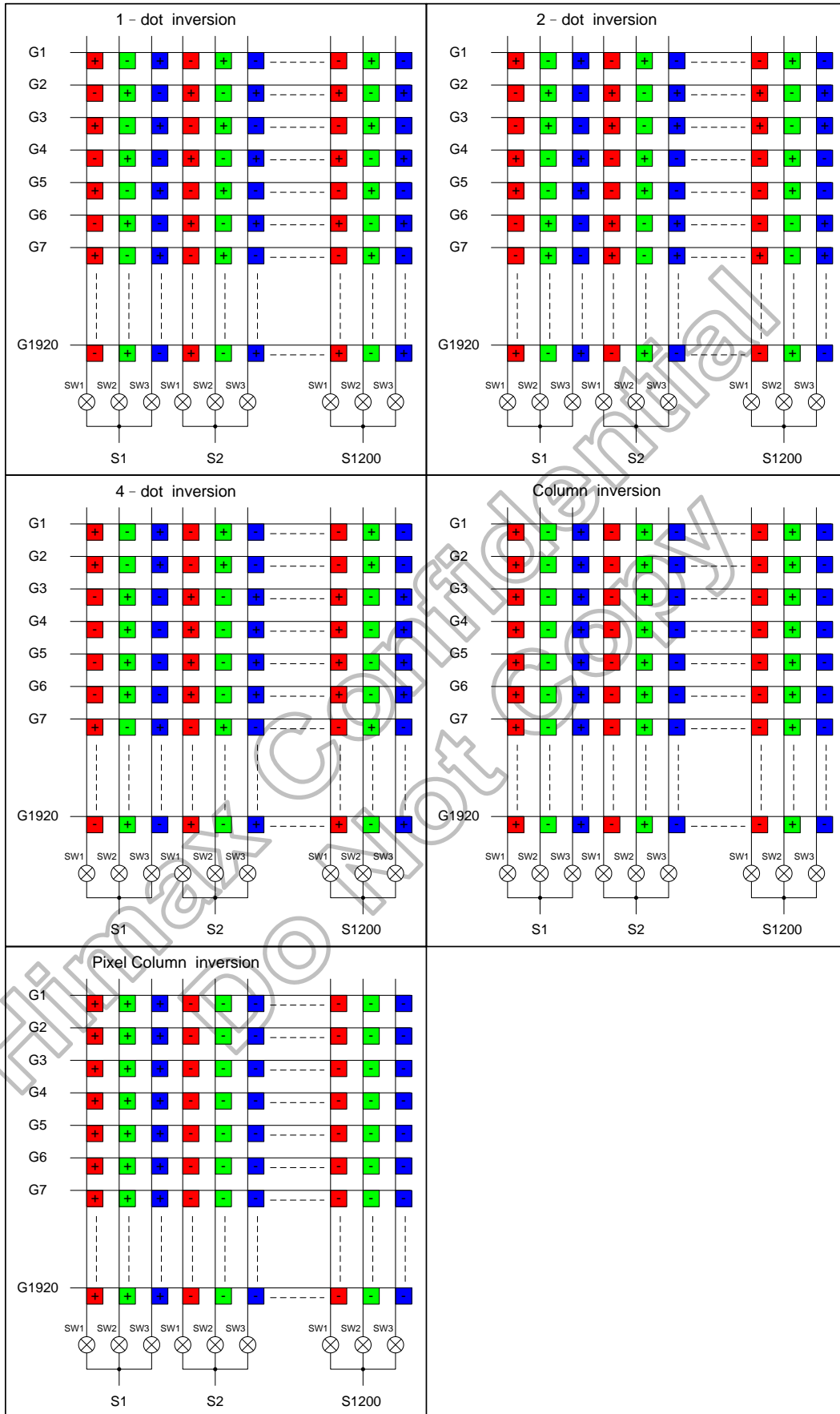


Figure 5.9 Inversion mode (MUX_SEL=0)

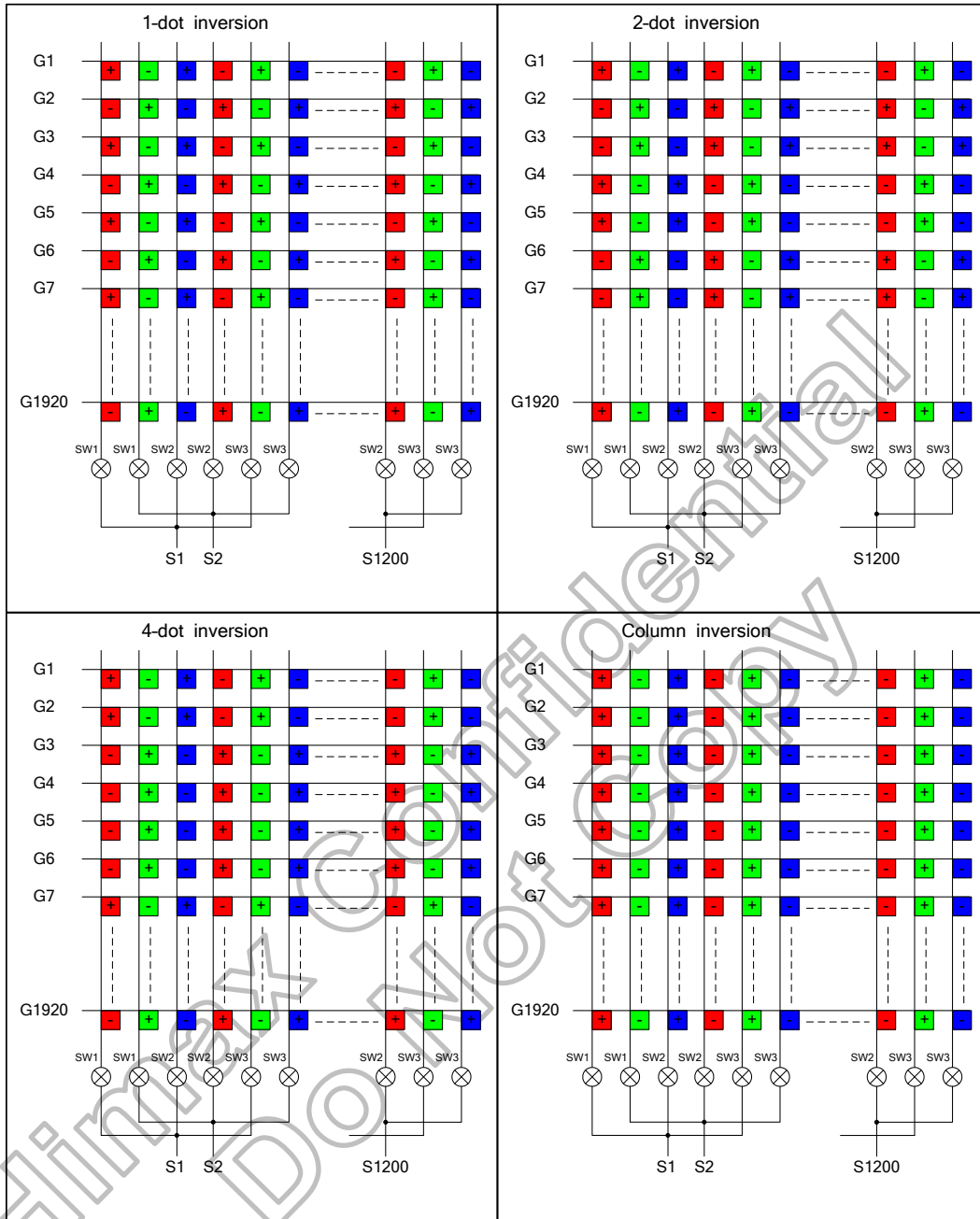


Figure 5.10: Inversion mode 2:6 (MUX_SEL=1)

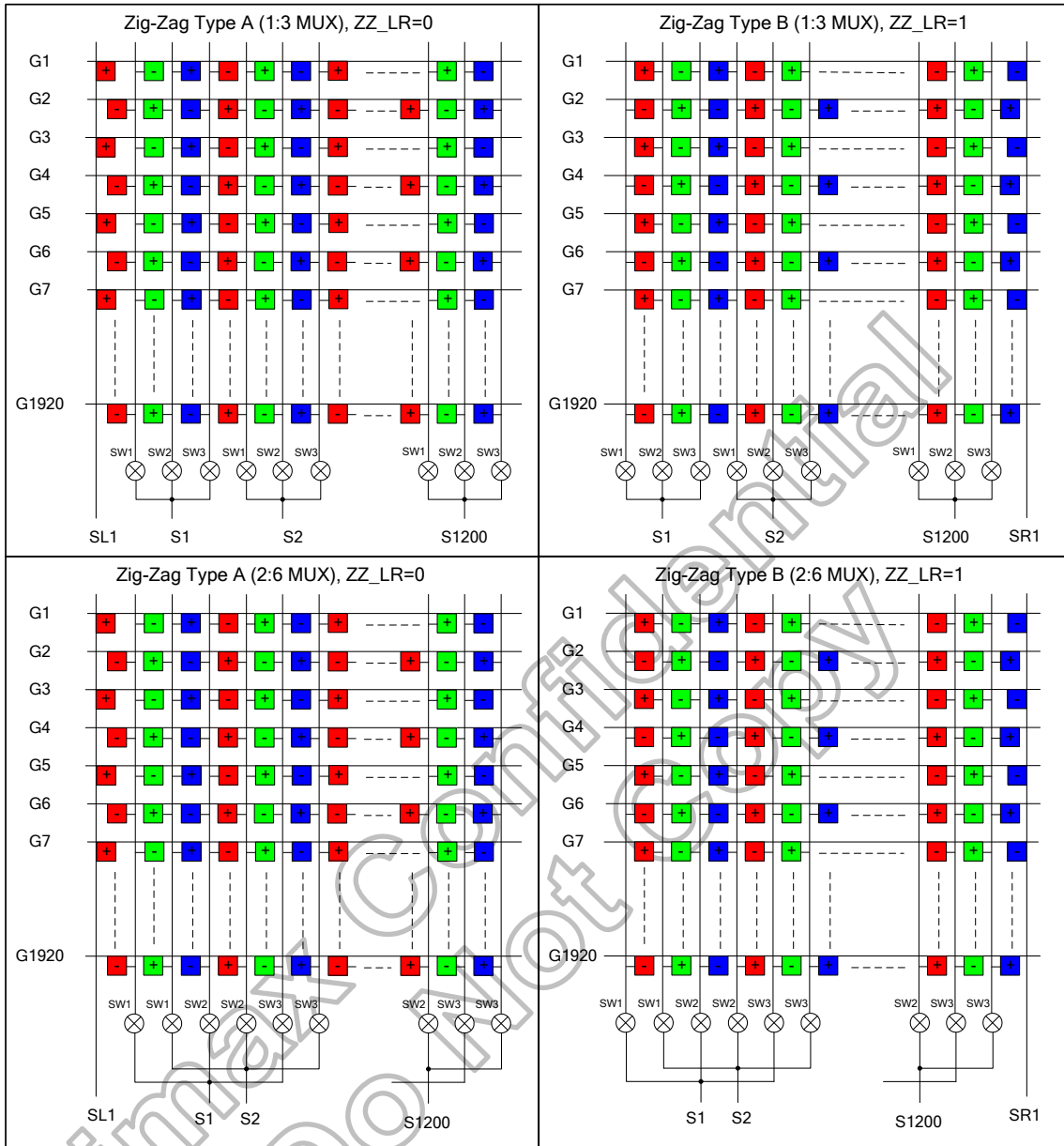


Figure 5.11: Zig-Zag Inversion mode(ZZ_EO=0)

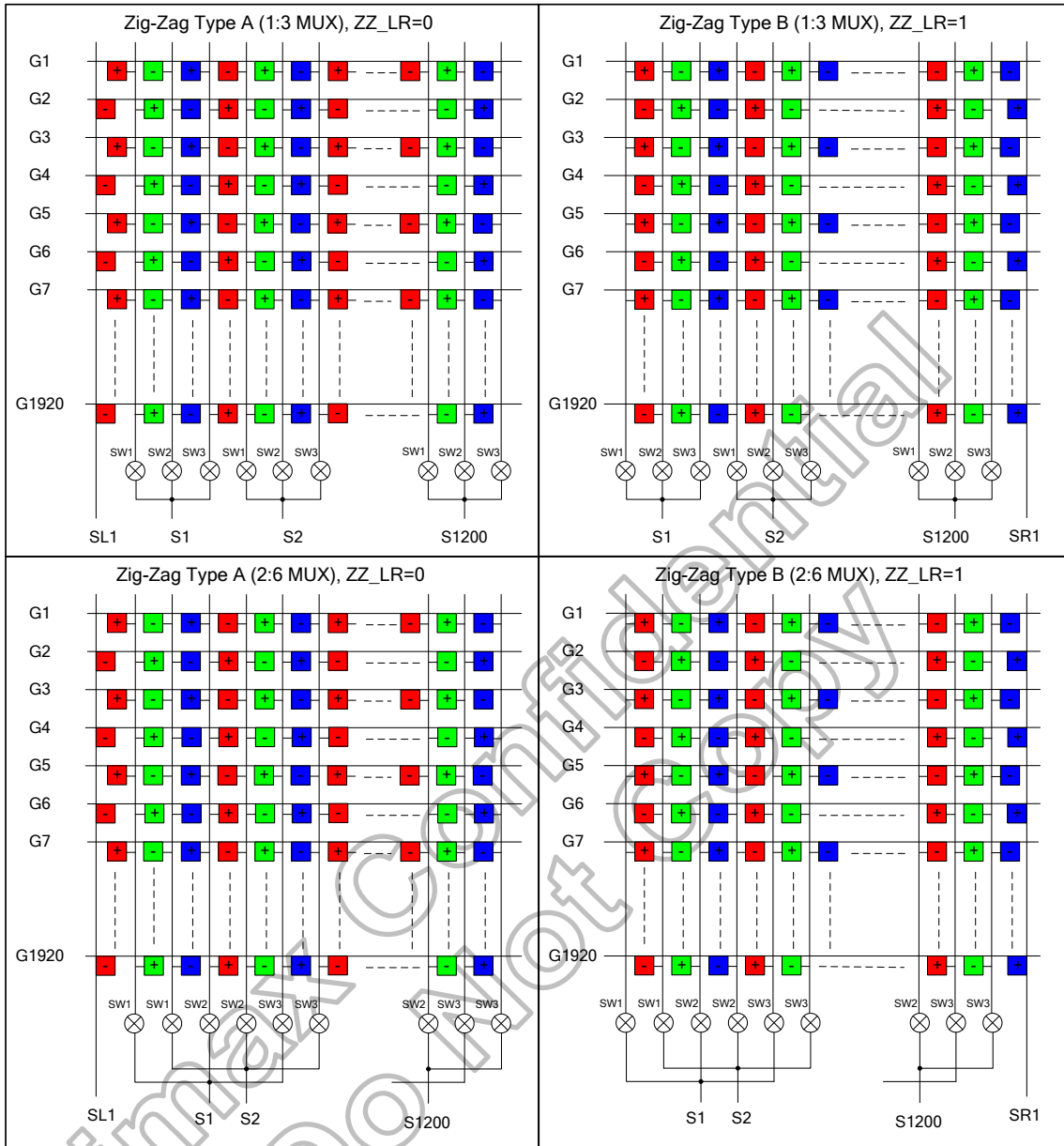


Figure 5.12: Zig-Zag Inversion mode(ZZ_EO=1)

5.4 LCD power generation scheme

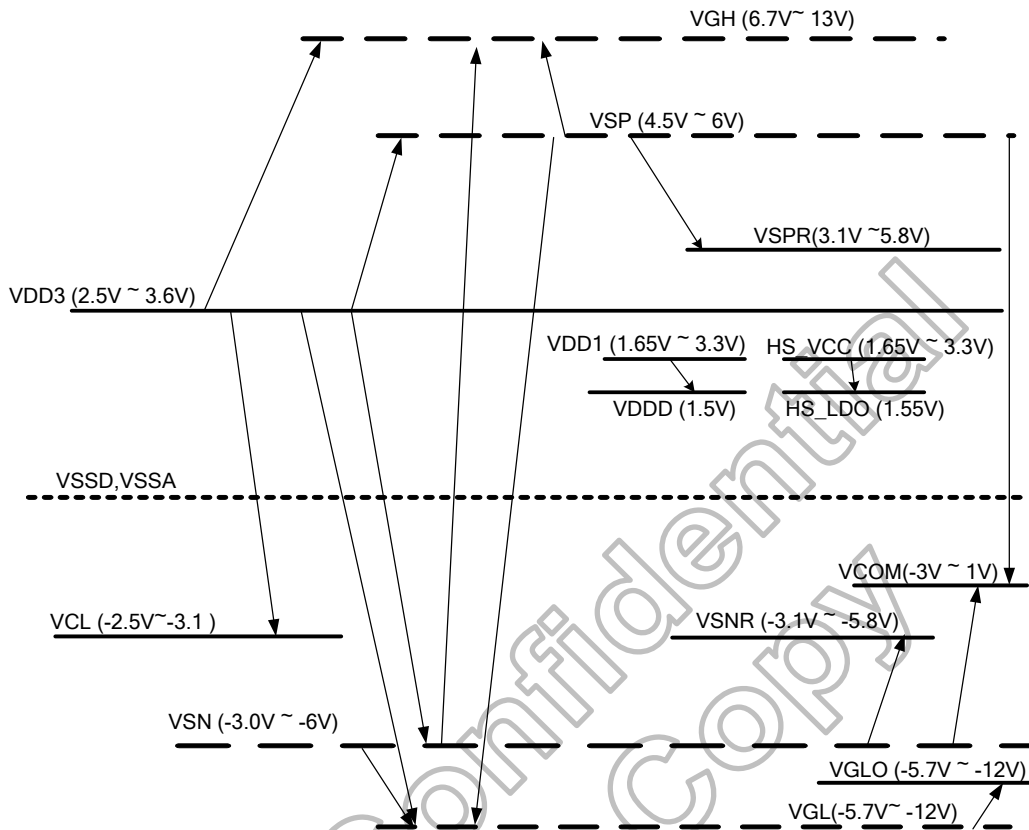


Figure 5.13: LCD power generation scheme for HX5186 and FPM mode

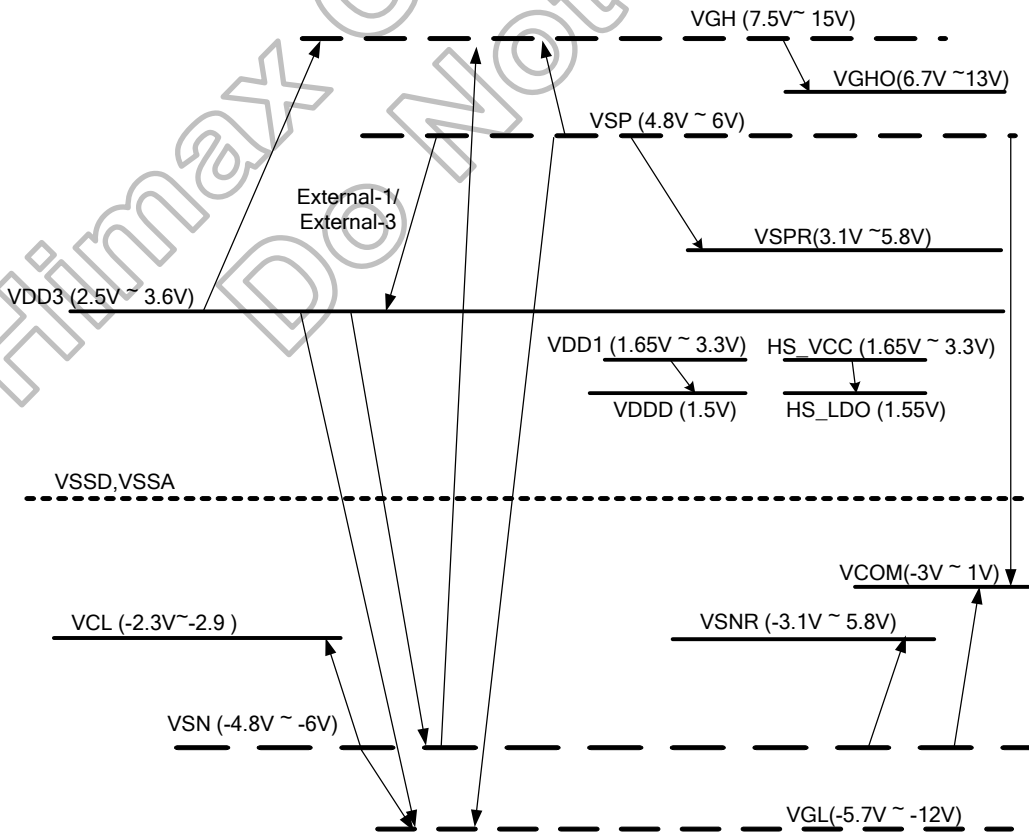


Figure 5.14: LCD power generation scheme for external power mode

HX8399-C has an internal power supply circuit to drive LTPS LCD panel. Please set up each voltage output according to the LCD panel.

Name	Function	Set up value	Note
VSPR	Reference voltage for gamma circuit	3.1V ~ 5.8V	-
VSNR	Reference voltage for gamma circuit	-3.1V ~ -5.8V	-
VDDD	Logic power supply	1.5V	-
VGH	Positive gate driver output voltage level	6.7V ~13.0V	-
VGL	Negative gate driver output voltage level	-5.7V ~ -12.0V	-
VCL	DC/DC converter circuit output	-2.3V~-3.1	-
VCOM	VCOM DC voltage	-3V ~ 1V	-
HS_LDO	Analog power for High speed interface circuit	1.55V	Depend on DSI I/F

Table 5.2: Voltage configuration

Himax Confidential
Do Not Copy

5.5 DC/DC converter circuit

5.5.1 Charge pump and step up circuit mode

HX8399-C supports various kinds of power generation mode, including PFM Type A, PFM Type D, PFM Type C and external HX5186 and external VSP & VSN and external VSP&VSN&VDD3. All power power mode can be set by hardware pins PCCS[2:0] as below:

PCCS2	PCCS1	PCCS0	Power source	Driving Mode
0	0	0	VDD3 / VDD1	PFM Type C
0	0	1	VDD3 /VDD1	HX5186-C
0	1	0	VSP /VDD1	PFM Type D(for VSN)
0	1	1	VSP / VSN / VDD1	External-1
1	0	0	VSP / VSN / VGH / VGL / VDD1	External-3
1	0	1	VDD3/ VDD1	PFM Type A
1	1	1	VDD3 / VSP / VSN / VDD1	External-2

Table 5.3: Power mode setting

Himax Confidential
Do Not Copy

5.5.2 Use HX5186- C

The HX5186-C is highly efficient switching voltage generator circuits that generate the high voltage level VSP/VSN required for source drivers. HX8399-C contains Charge Pump Controller for HX5186-C, including a comparator for VSP/VSN feedback control. HX5186-C can provide maximum efficiency and use minimum number of external components. The output voltage of the boost converter can be set from 3.0V to 6.0V (VSP) and -3.0V to -6.0V (VSN)

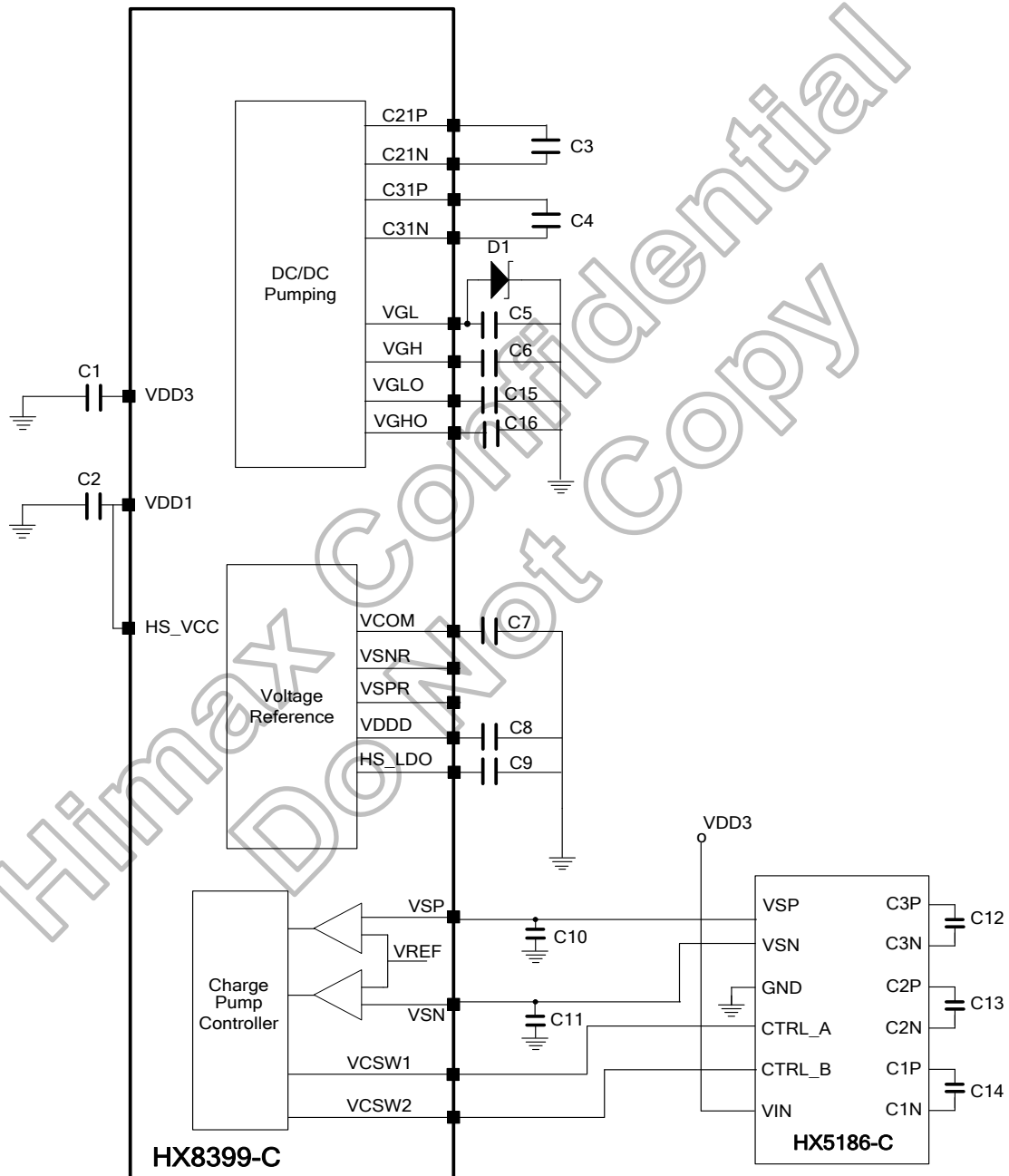


Figure 5.15: DC/DC converter circuit of HX5186- C

5.5.3 Use PFM DC/DC converter

The PFM DC-DC converter generates the high voltage level VSP/VSN required for source drivers. HX8399-C contains sub-circuits of the PFM boost converter, including a precision 1.8V reference voltage, comparator, PFM controlling logic, and the output buffer. The boost converter uses a external power transistor to provide maximum efficiency and to minimize the number of external components. The output voltage of the boost converter can be set from 3.0V to 6V (VSP) and -3.0 to -6V (VSN)

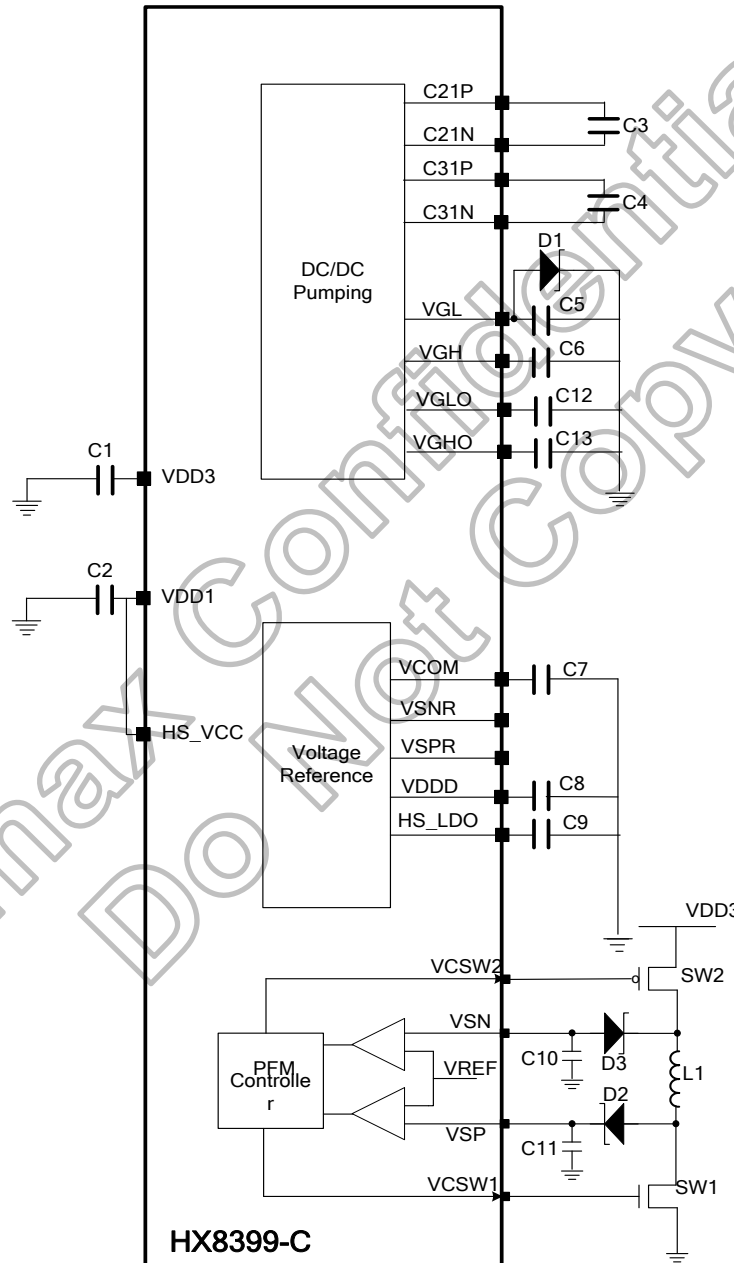


Figure 5.16: DC/DC converter circuit (PFM Type-A)

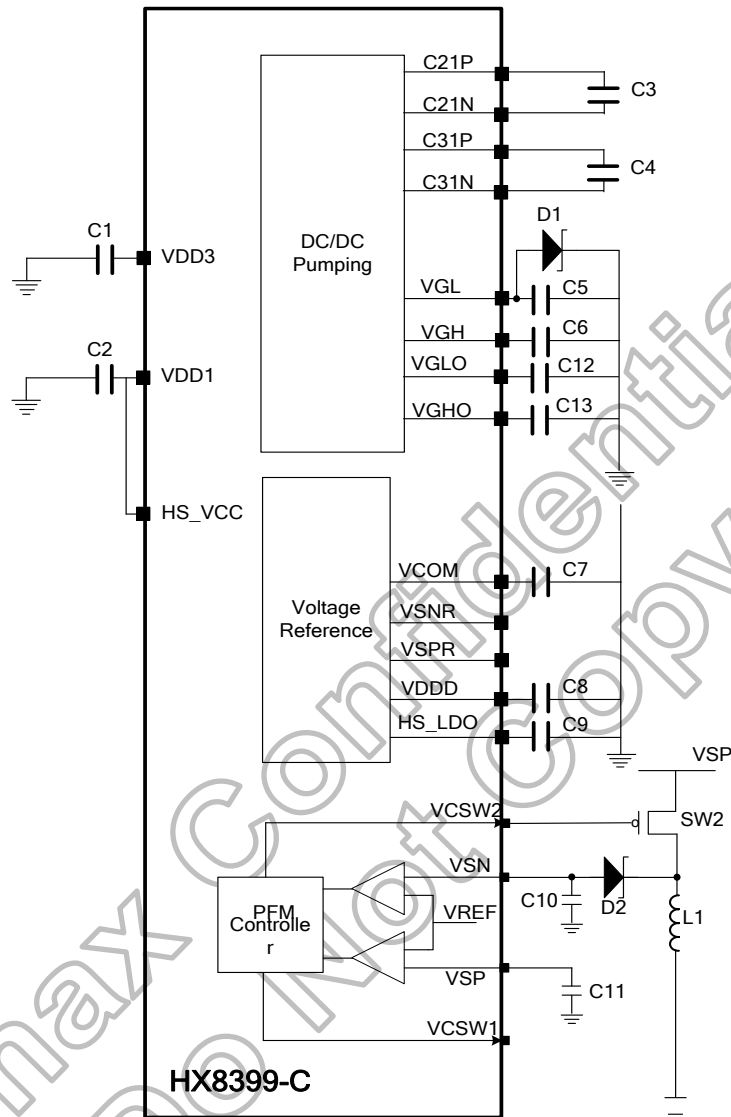


Figure 5.17: DC/DC converter circuit (PFM Type-D)

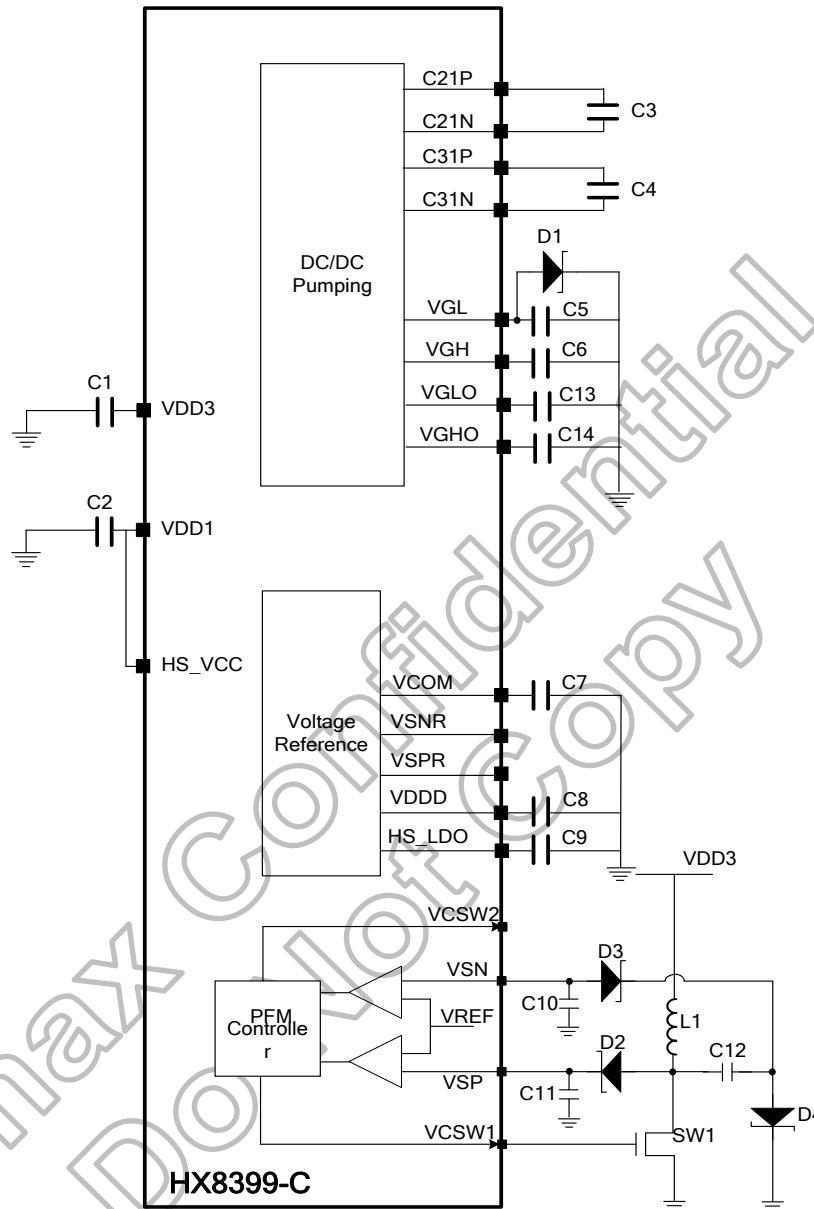


Figure 5.18: DC/DC converter circuit (PFM Type-C)

5.5.4 Use external VSP and VSN circuit

VDD3 is generated from VSP by regulator. The input voltage range of VSP is 4.8V ~ 6.0V. The input voltage range of VSN is -4.8V ~ -6.0V.

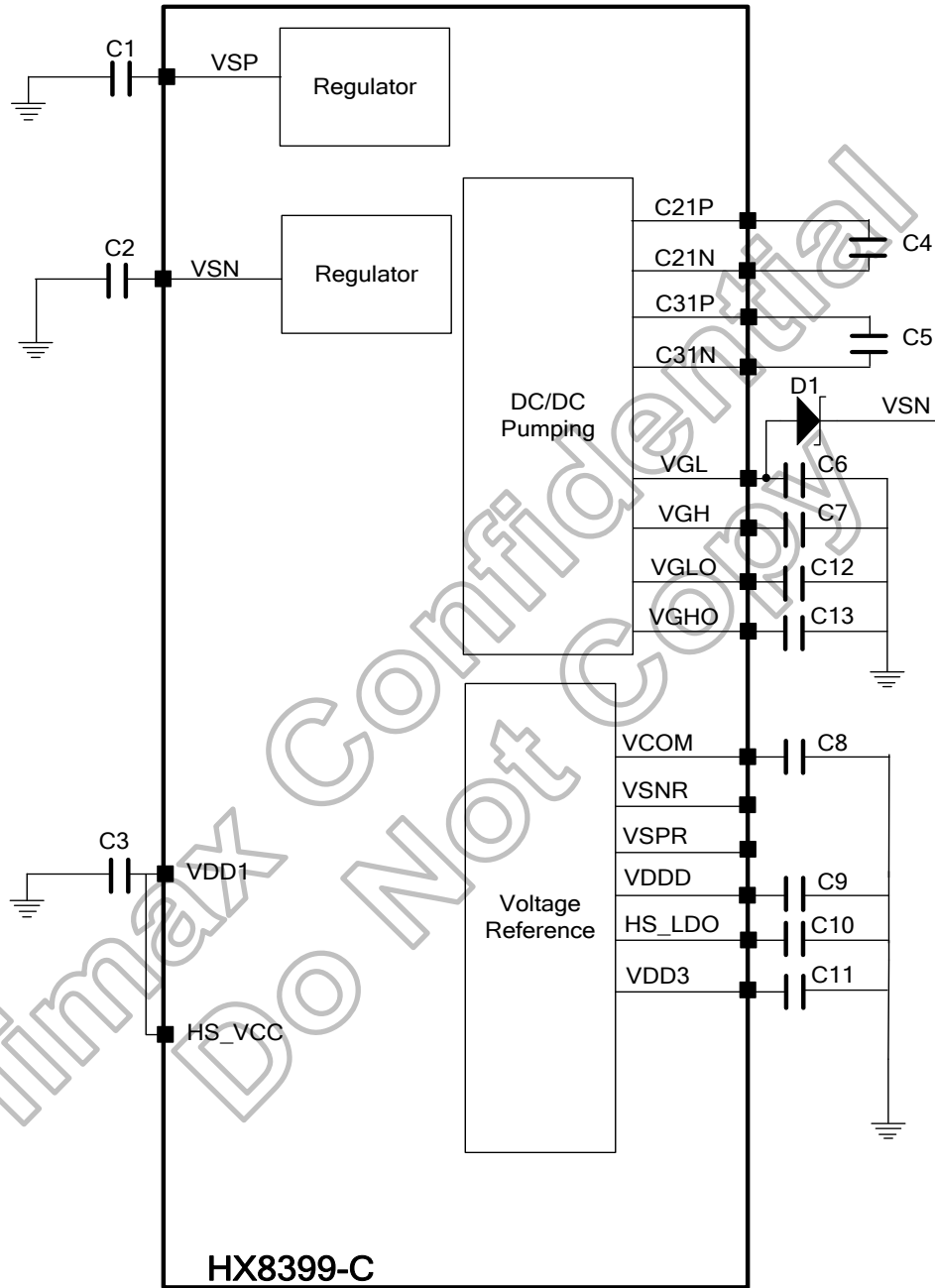


Figure 5.19: DC/DC converter circuit of external VSP/VSN

5.5.5 Use external VSP and VSN and VDD3 circuit

The input voltage range of VDD3 is 2.5V ~ 3.6V. The input voltage range of VSP is 4.8V ~ 6.0V. The input voltage range of VSN is -4.8V ~ -6.0V.

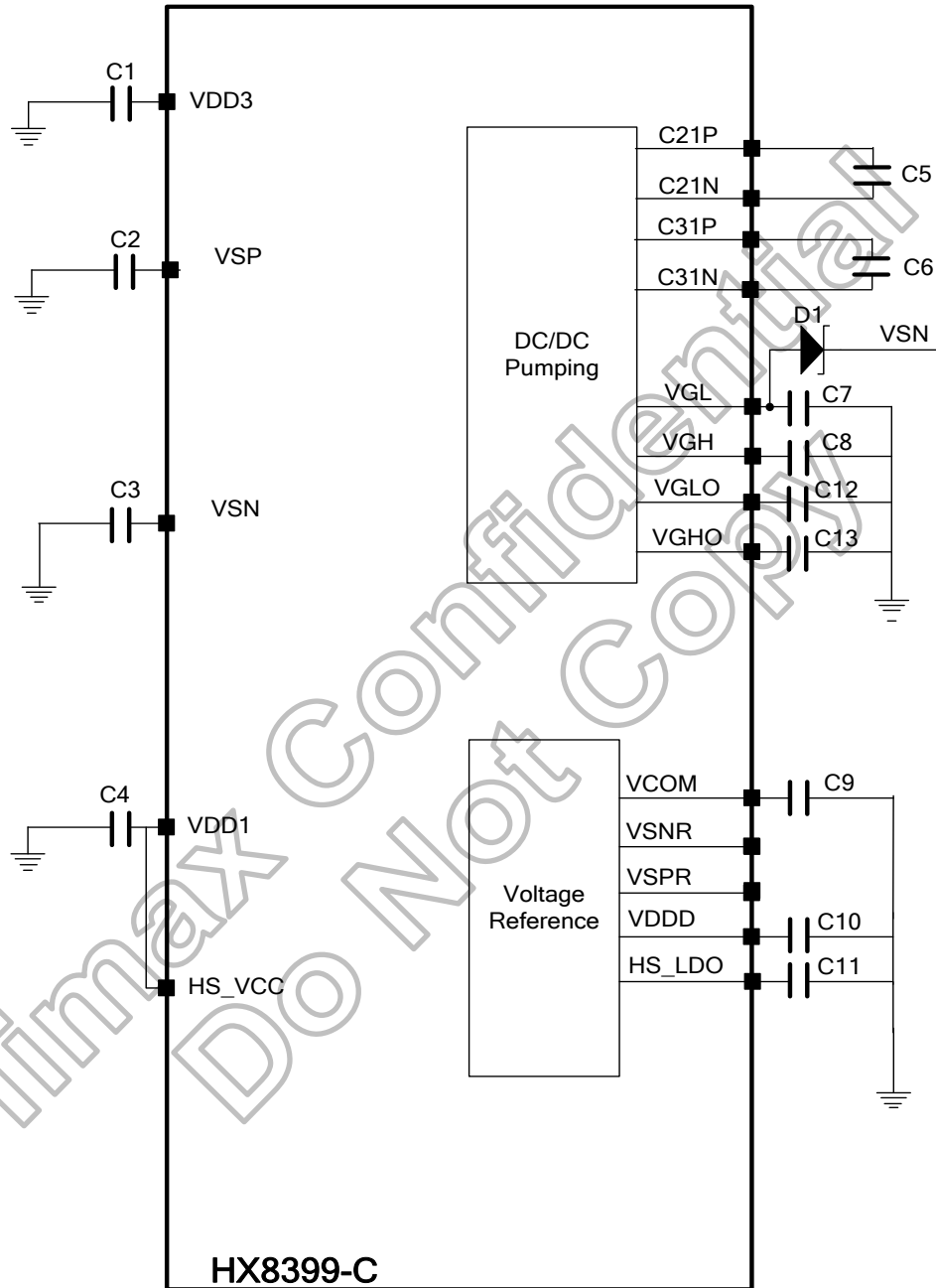


Figure 5.20: DC/DC converter circuit of external VDD3/VSP/VSN

5.5.6 Use external VSP, VSN, VGH and VGL circuit

VDD3 is generated from VSP by regulator. The input voltage range of VSP is from 4.8V ~ 6.0V. The input voltage range of VSN is from -4.8V ~ -6.0V.

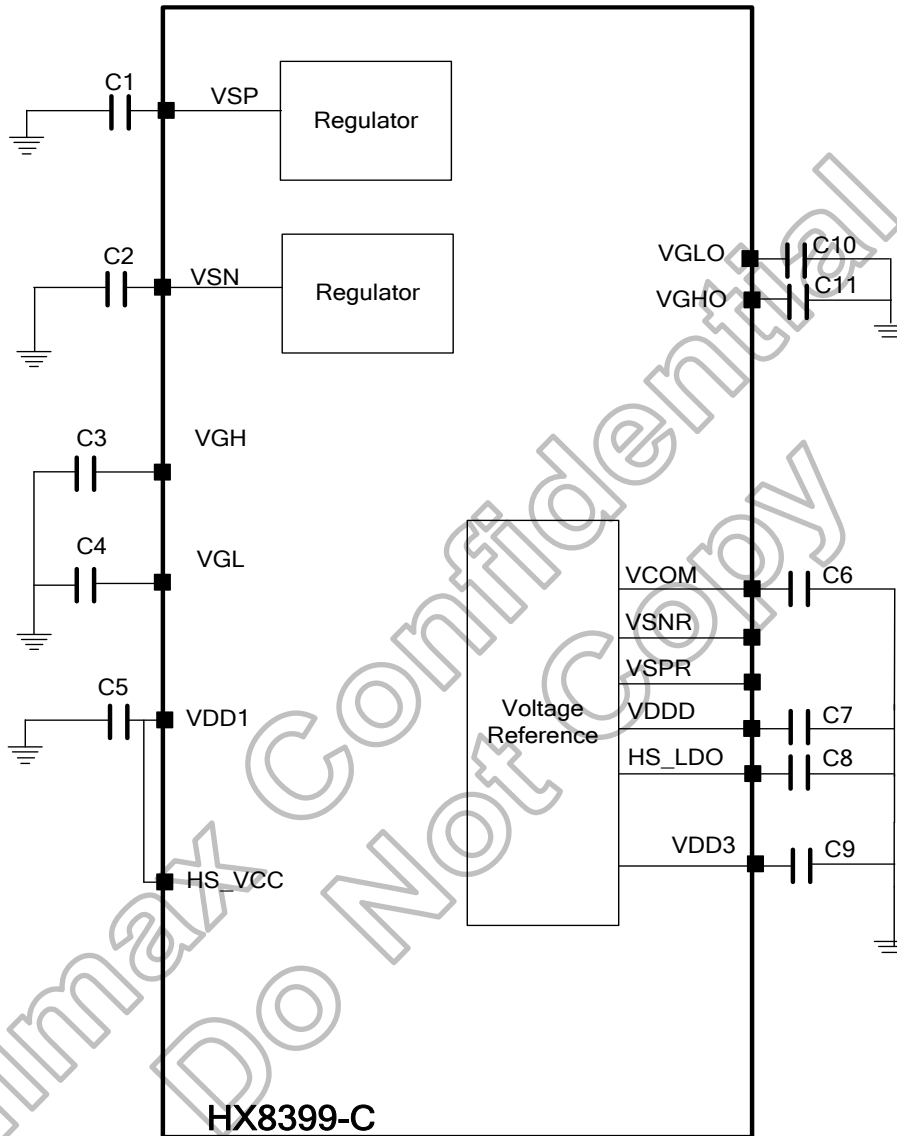


Figure 5.21: DC/DC converter circuit of external VSP/VSN/VGH/VGL

5.6 Idle display

The HX8399-C supports an idle display mode. The grayscale level to be used is 0 and 255 with R7, G7, B7 decoding, and the other levels (1~254) are halted to reduce power consumption. In idle display mode, the Gamma-center-adjustment registers are invalid and only the upper bits of RGB are used for display.

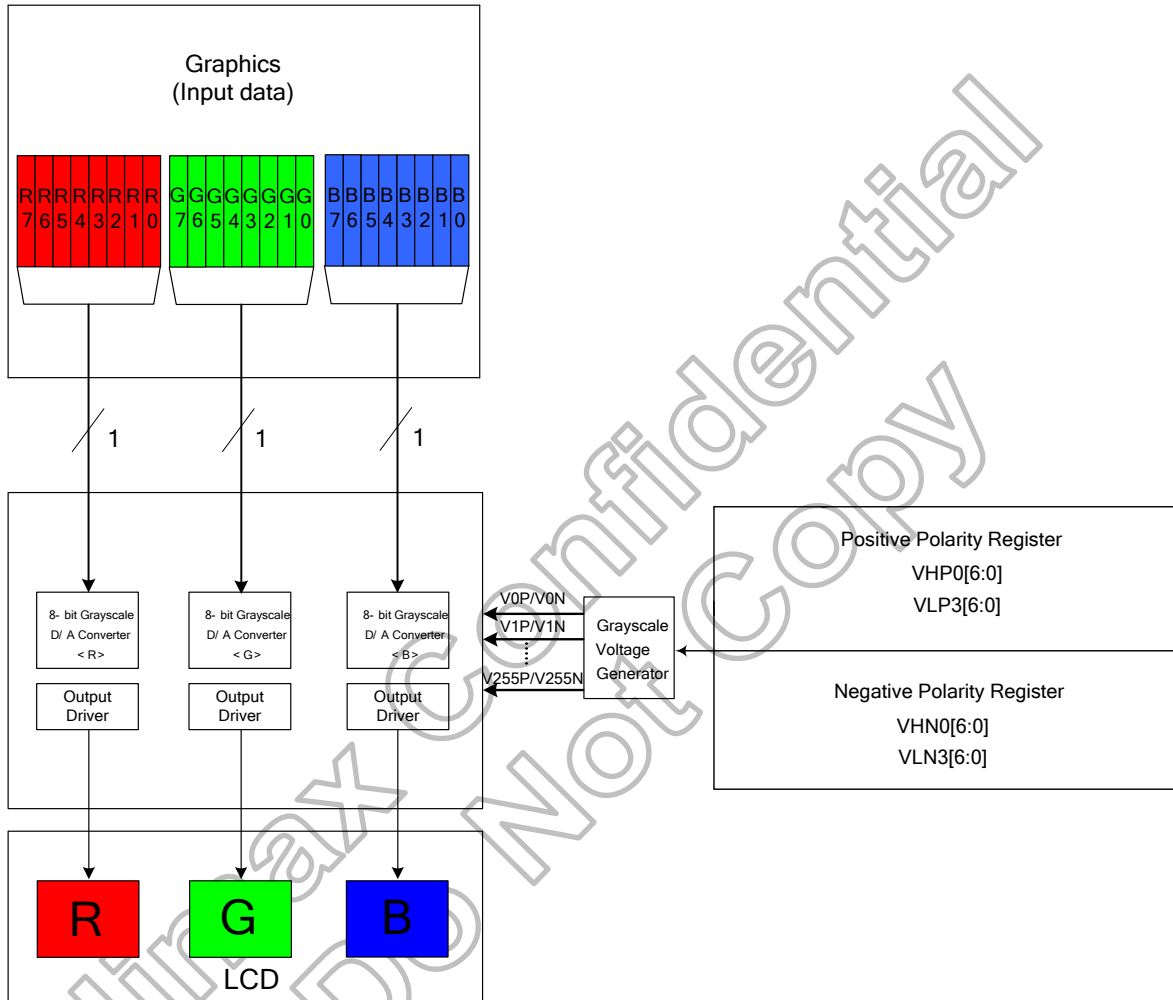
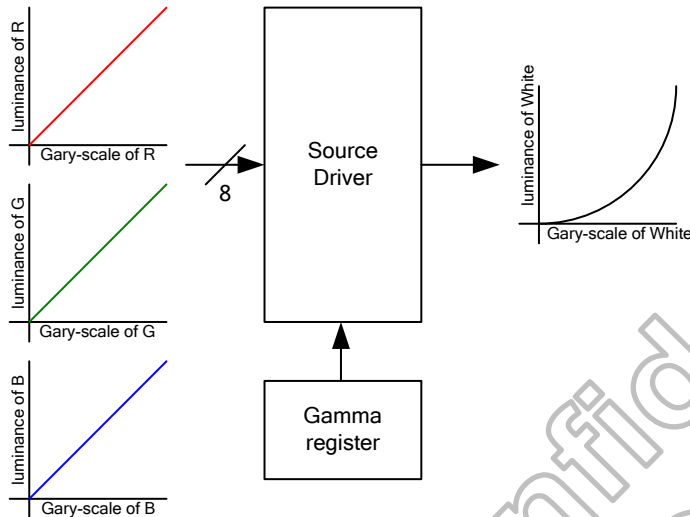


Figure 5.22: Idle mode grayscale control

5.7 Gamma characteristic correction function

The HX8399-C offers two kinds of Gamma adjustment. One kind is through Source Driver directly, another one is adjusted by the digital gamma correction. The Gamma adjustment way is selected by internal register DGC_EN bit.

A) Gamma adjustment of Source Driver



B) Gamma adjustment of Digital Gamma Correction

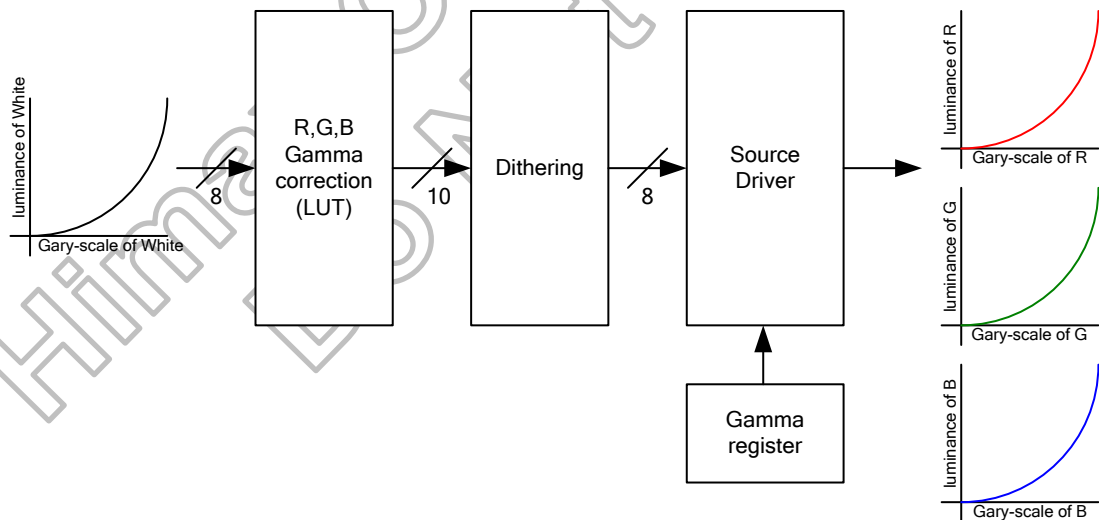


Figure 5.23: Gamma adjustments different of source driver with digital gamma correction

The HX8399-C incorporates gamma adjustment function for the 16,7M colors display (256 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 16 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 512 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

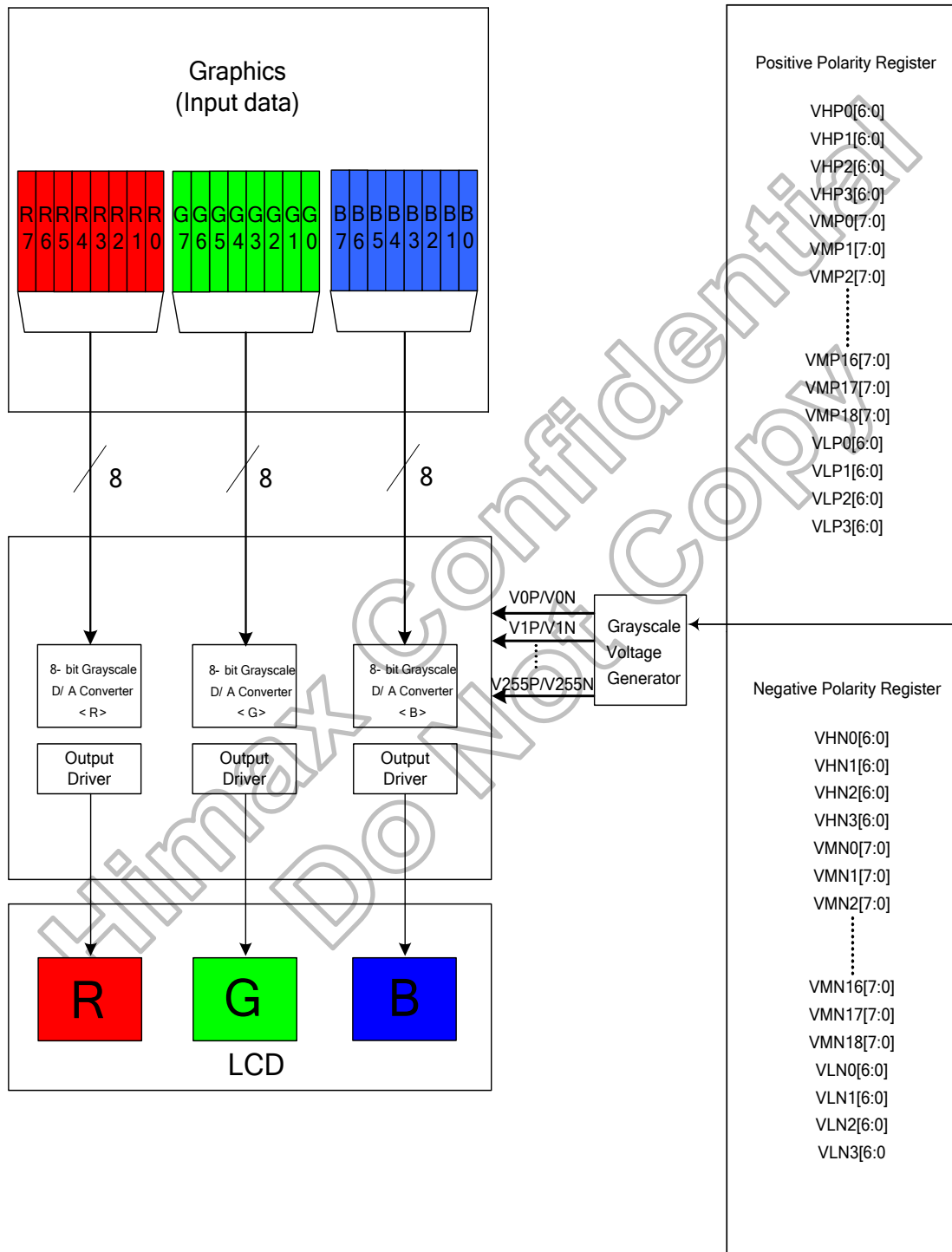


Figure 5.24: Grayscale control

5.7.1 Gamma characteristics adjustment register

The HX8399-C has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

A. Center adjustment registers

This gamma adjustment registers are used to adjust the reference gamma voltage for center grayscale level. This function is implemented by controlling the 256-to-1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

B. Edge adjustment registers

This gamma adjustment registers are used to adjust the reference gamma voltage for both edge grayscale level. This function is implemented by controlling the 128-to-1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
Up Edge adjustment	VHP0 6-0	VHN0 6-0	128-to-1 selector (voltage level of grayscale 255)
	VHP1 6-0	VHN1 6-0	128-to-1 selector (voltage level of grayscale 251)
	VHP2 6-0	VHN2 6-0	128-to-1 selector (voltage level of grayscale 247)
	VHP3 6-0	VHN3 6-0	128-to-1 selector (voltage level of grayscale 243)
Center adjustment	VMP0 7-0	VMN0 7-0	256-to-1 selector (voltage level of grayscale 235)
	VMP1 7-0	VMN1 7-0	256-to-1 selector (voltage level of grayscale 227)
	VMP2 7-0	VMN2 7-0	256-to-1 selector (voltage level of grayscale 215)
	VMP3 7-0	VMN3 7-0	256-to-1 selector (voltage level of grayscale 203)
	VMP4 7-0	VMN4 7-0	256-to-1 selector (voltage level of grayscale 191)
	VMP5 7-0	VMN5 7-0	256-to-1 selector (voltage level of grayscale 179)
	VMP6 7-0	VMN6 7-0	256-to-1 selector (voltage level of grayscale 167)
	VMP7 7-0	VMN7 7-0	256-to-1 selector (voltage level of grayscale 155)
	VMP8 7-0	VMN8 7-0	256-to-1 selector (voltage level of grayscale 143)
	VMP9 7-0	VMN9 7-0	256-to-1 selector (voltage level of grayscale 127)
	VMP10 7-0	VMN10 7-0	256-to-1 selector (voltage level of grayscale 111)
	VMP11 7-0	VMN11 7-0	256-to-1 selector (voltage level of grayscale 99)
	VMP12 7-0	VMN12 7-0	256-to-1 selector (voltage level of grayscale 87)
	VMP13 7-0	VMN13 7-0	256-to-1 selector (voltage level of grayscale 75)
	VMP14 7-0	VMN14 7-0	256-to-1 selector (voltage level of grayscale 63)
	VMP15 7-0	VMN15 7-0	256-to-1 selector (voltage level of grayscale 51)
	VMP16 7-0	VMN16 7-0	256-to-1 selector (voltage level of grayscale 39)
	VMP17 7-0	VMN17 7-0	256-to-1 selector (voltage level of grayscale 27)
VMP18 7-0	VMN18 7-0	256-to-1 selector (voltage level of grayscale 19)	
Down Edge adjustment	VLP0 6-0	VLN0 6-0	128-to-1 selector (voltage level of grayscale 12)
	VLP1 6-0	VLN1 6-0	128-to-1 selector (voltage level of grayscale 8)
	VLP2 6-0	VLN2 6-0	128-to-1 selector (voltage level of grayscale 4)
	VLP3 6-0	VLN3 6-0	128-to-1 selector (voltage level of grayscale 0)

Table 5.4: Gamma-Adjustment registers for normally black panel

Register Groups	Positive Polarity	Negative Polarity	Description
Up Edge adjustment	VHP0 6-0	VHN0 6-0	128-to-1 selector (voltage level of grayscale 0)
	VHP1 6-0	VHN1 6-0	128-to-1 selector (voltage level of grayscale 4)
	VHP2 6-0	VHN2 6-0	128-to-1 selector (voltage level of grayscale 8)
	VHP3 6-0	VHN3 6-0	128-to-1 selector (voltage level of grayscale 12)
Center adjustment	VMP0 7-0	VMN0 7-0	256-to-1 selector (voltage level of grayscale 20)
	VMP1 7-0	VMN1 7-0	256-to-1 selector (voltage level of grayscale 28)
	VMP2 7-0	VMN2 7-0	256-to-1 selector (voltage level of grayscale 40)
	VMP3 7-0	VMN3 7-0	256-to-1 selector (voltage level of grayscale 52)
	VMP4 7-0	VMN4 7-0	256-to-1 selector (voltage level of grayscale 64)
	VMP5 7-0	VMN5 7-0	256-to-1 selector (voltage level of grayscale 76)
	VMP6 7-0	VMN6 7-0	256-to-1 selector (voltage level of grayscale 88)
	VMP7 7-0	VMN7 7-0	256-to-1 selector (voltage level of grayscale 100)
	VMP8 7-0	VMN8 7-0	256-to-1 selector (voltage level of grayscale 112)
	VMP9 7-0	VMN9 7-0	256-to-1 selector (voltage level of grayscale 128)
	VMP10 7-0	VMN10 7-0	256-to-1 selector (voltage level of grayscale 144)
	VMP11 7-0	VMN11 7-0	256-to-1 selector (voltage level of grayscale 156)
	VMP12 7-0	VMN12 7-0	256-to-1 selector (voltage level of grayscale 168)
	VMP13 7-0	VMN13 7-0	256-to-1 selector (voltage level of grayscale 180)
	VMP14 7-0	VMN14 7-0	256-to-1 selector (voltage level of grayscale 192)
	VMP15 7-0	VMN15 7-0	256-to-1 selector (voltage level of grayscale 204)
	VMP16 7-0	VMN16 7-0	256-to-1 selector (voltage level of grayscale 216)
	VMP17 7-0	VMN17 7-0	256-to-1 selector (voltage level of grayscale 228)
VMP18 7-0	VMN18 7-0	256-to-1 selector (voltage level of grayscale 236)	
Down Edge adjustment	VLP0 6-0	VLN0 6-0	128-to-1 selector (voltage level of grayscale 243)
	VLP1 6-0	VLN1 6-0	128-to-1 selector (voltage level of grayscale 247)
	VLP2 6-0	VLN2 6-0	128-to-1 selector (voltage level of grayscale 251)
	VLP3 6-0	VLN3 6-0	128-to-1 selector (voltage level of grayscale 255)

Table 5.5: Gamma-Adjustment registers for normally white panel

Gamma resister stream and selector

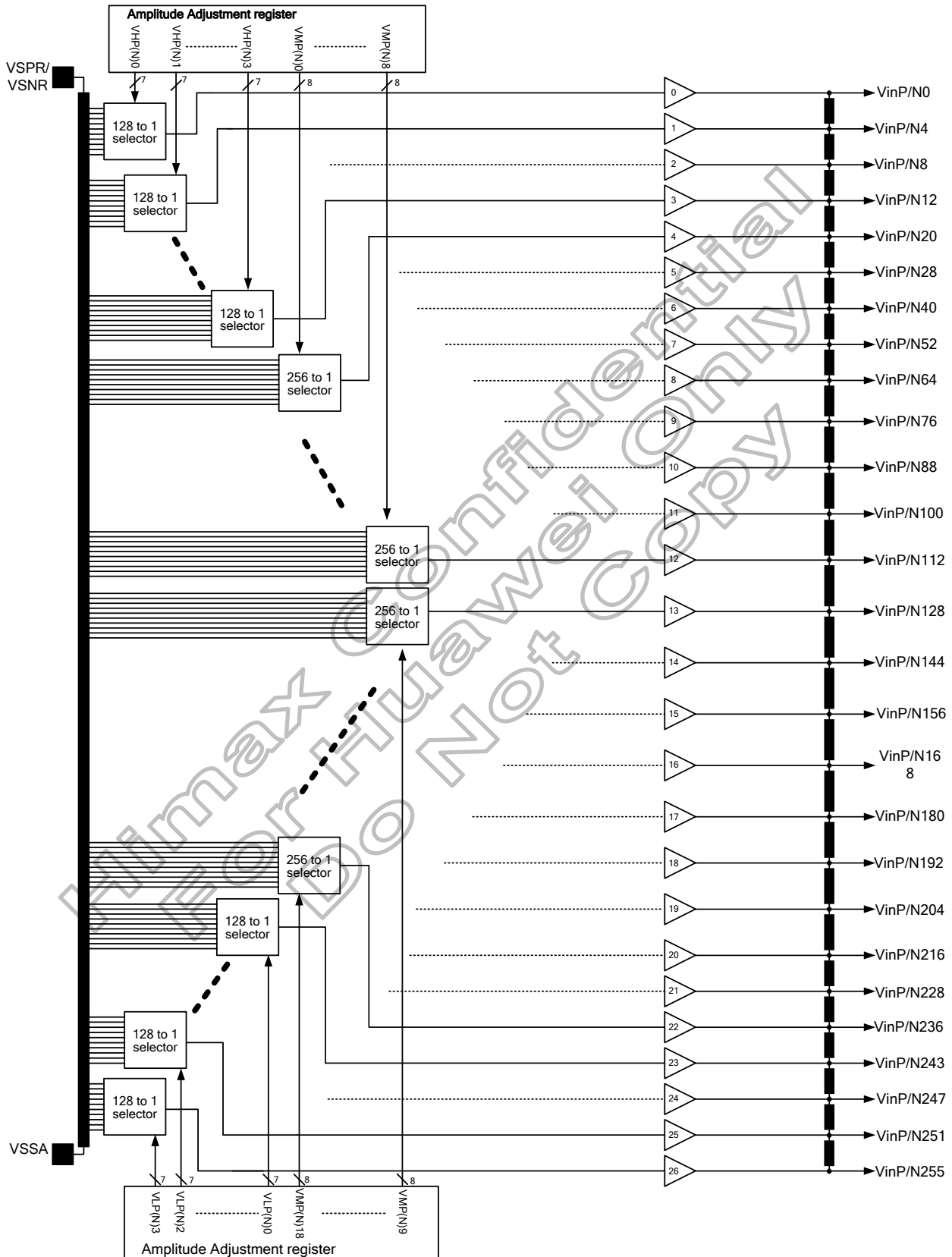


Figure 5.25: Gamma resister stream and gamma reference voltage

Variable resistor

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register VH(P/N)0~3 [6:0]	Resistance VH(P/N) 0~3	Value in Register VL(P/N)0~3 [6:0]	Resistance VL(P/N) 0~3
000_0000	0R	000_0000	0R
000_0001	2R	000_0001	2R
000_0010	4R	000_0010	4R
000_0011	6R	000_0011	6R
:	:	:	:
011_1101	122R	011_1101	122R
011_1110	124R	011_1110	124R
011_1111	126R	011_1111	126R
100_0000	128R	100_0000	128R
100_0001	130R	100_0001	130R
100_0010	132R	100_0010	132R
:	:	:	:
111_1101	250R	111_1101	250R
111_1110	252R	111_1110	252R
111_1111	254R	111_1111	254R

Table 5.6: Offset adjustment 0~5

Value in Register VM(P/N)0~18 [7:0]	Resistance VM(P/N)0~18
0000_0000	0R
0000_0001	1R
0000_0010	2R
:	:
0101_0101	85R
0101_0110	86R
0101_0111	87R
:	:
1101_0101	213R
1101_0110	214R
1101_0111	215R
:	:
1111_1101	253R
1111_1110	254R
1111_1111	255R

Table 5.7: Center adjustment

The grayscale levels are determined by the following formulas:

Reference voltage	Macro adjustment value	VinP/N0 formula
VinP/N0	VHP0 [6:0] = 000_0000	VSP/NR
	VHP0 [6:0] = 000_0001	$((600R - 2R) / 600R) * VSP/NR$
	VHP0 [6:0] = 000_0010	$((600R - 4R) / 600R) * VSP/NR$
	VHP0 [6:0] = 000_0011	$((600R - 6R) / 600R) * VSP/NR$
	VHP0 [6:0] = 000_0100	$((600R - 8R) / 600R) * VSP/NR$
	VHP0 [6:0] = 000_0101	$((600R - 10R) / 600R) * VSP/NR$
	:	:
	VHP0 [6:0] = 100_0001	$((600R - 130R) / 600R) * VSP/NR$
	VHP0 [6:0] = 100_0010	$((600R - 132R) / 600R) * VSP/NR$
	VHP0 [6:0] = 100_0011	$((600R - 134R) / 600R) * VSP/NR$
	VHP0 [6:0] = 100_0100	$((600R - 136R) / 600R) * VSP/NR$
	VHP0 [6:0] = 100_0101	$((600R - 138R) / 600R) * VSP/NR$
	:	:
	VHP0 [6:0] = 111_1011	$((600R - 246R) / 600R) * VSP/NR$
	VHP0 [6:0] = 111_1100	$((600R - 248R) / 600R) * VSP/NR$
	VHP0 [6:0] = 111_1101	$((600R - 250R) / 600R) * VSP/NR$
VHP0 [6:0] = 111_1110	$((600R - 252R) / 600R) * VSP/NR$	
VHP0 [6:0] = 111_1111	$((600R - 254R) / 600R) * VSP/NR$	

Table 5.8: VinP/N0

Reference voltage	Macro adjustment value	VinP/N1 formula
VinP/N4	VHP1 [6:0] = 000_0000	$(596R / 600R) * VSP/NR$
	VHP1 [6:0] = 000_0001	$((596R - 2R) / 600R) * VSP/NR$
	VHP1 [6:0] = 000_0010	$((596R - 4R) / 600R) * VSP/NR$
	VHP1 [6:0] = 000_0011	$((596R - 6R) / 600R) * VSP/NR$
	VHP1 [6:0] = 000_0100	$((596R - 8R) / 600R) * VSP/NR$
	VHP1 [6:0] = 000_0101	$((596R - 10R) / 600R) * VSP/NR$
	:	:
	VHP1 [6:0] = 100_0001	$((596R - 130R) / 600R) * VSP/NR$
	VHP1 [6:0] = 100_0010	$((596R - 132R) / 600R) * VSP/NR$
	VHP1 [6:0] = 100_0011	$((596R - 134R) / 600R) * VSP/NR$
	VHP1 [6:0] = 100_0100	$((596R - 136R) / 600R) * VSP/NR$
	VHP1 [6:0] = 100_0101	$((596R - 138R) / 600R) * VSP/NR$
	:	:
	VHP1 [6:0] = 111_1011	$((596R - 246R) / 600R) * VSP/NR$
	VHP1 [6:0] = 111_1100	$((596R - 248R) / 600R) * VSP/NR$
	VHP1 [6:0] = 111_1101	$((596R - 250R) / 600R) * VSP/NR$
VHP1 [6:0] = 111_1110	$((596R - 252R) / 600R) * VSP/NR$	
VHP1 [6:0] = 111_1111	$((596R - 254R) / 600R) * VSP/NR$	

Table 5.9: VinP/N4

Reference voltage	Macro adjustment value	VinP/N3 formula
VinP/N8	VHP2 [6:0] = 000_0000	$(592R / 600R) * VSP/NR$
	VHP2 [6:0] = 000_0001	$((592R - 2R) / 600R) * VSP/NR$
	VHP2 [6:0] = 000_0010	$((592R - 4R) / 600R) * VSP/NR$
	VHP2 [6:0] = 000_0011	$((592R - 6R) / 600R) * VSP/NR$
	VHP2 [6:0] = 000_0100	$((592R - 8R) / 600R) * VSP/NR$
	VHP2 [6:0] = 000_0101	$((592R - 10R) / 600R) * VSP/NR$
	:	:
	VHP2 [6:0] = 100_0001	$((592R - 130R) / 600R) * VSP/NR$
	VHP2 [6:0] = 100_0010	$((592R - 132R) / 600R) * VSP/NR$
	VHP2 [6:0] = 100_0011	$((592R - 134R) / 600R) * VSP/NR$
	VHP2 [6:0] = 100_0100	$((592R - 136R) / 600R) * VSP/NR$
	VHP2 [6:0] = 100_0101	$((592R - 138R) / 600R) * VSP/NR$
	:	:
	VHP2 [6:0] = 111_1011	$((592R - 246R) / 600R) * VSP/NR$
	VHP2 [6:0] = 111_1100	$((592R - 248R) / 600R) * VSP/NR$
	VHP2 [6:0] = 111_1101	$((592R - 250R) / 600R) * VSP/NR$
VHP2 [6:0] = 111_1110	$((592R - 252R) / 600R) * VSP/NR$	
VHP2 [6:0] = 111_1111	$((592R - 254R) / 600R) * VSP/NR$	

Table 5.10: VinP/N8

Reference voltage	Macro adjustment value	VinP/N5 formula
VinP/N12	VHP3 [6:0] = 000_0000	$(560R / 600R) * VSP/NR$
	VHP3 [6:0] = 000_0001	$((560R - 2R) / 600R) * VSP/NR$
	VHP3 [6:0] = 000_0010	$((560R - 4R) / 600R) * VSP/NR$
	VHP3 [6:0] = 000_0011	$((560R - 6R) / 600R) * VSP/NR$
	VHP3 [6:0] = 000_0100	$((560R - 8R) / 600R) * VSP/NR$
	VHP3 [6:0] = 000_0101	$((560R - 10R) / 600R) * VSP/NR$
	:	:
	VHP3 [6:0] = 100_0001	$((560R - 130R) / 600R) * VSP/NR$
	VHP3 [6:0] = 100_0010	$((560R - 132R) / 600R) * VSP/NR$
	VHP3 [6:0] = 100_0011	$((560R - 134R) / 600R) * VSP/NR$
	VHP3 [6:0] = 100_0100	$((560R - 136R) / 600R) * VSP/NR$
	VHP3 [6:0] = 100_0101	$((560R - 138R) / 600R) * VSP/NR$
	:	:
	VHP3 [6:0] = 111_1011	$((560R - 246R) / 600R) * VSP/NR$
	VHP3 [6:0] = 111_1100	$((560R - 248R) / 600R) * VSP/NR$
	VHP3 [6:0] = 111_1101	$((560R - 250R) / 600R) * VSP/NR$
VHP3 [6:0] = 111_1110	$((560R - 252R) / 600R) * VSP/NR$	
VHP3 [6:0] = 111_1111	$((560R - 254R) / 600R) * VSP/NR$	

Table 5.11: VinP/N12

Reference voltage	Macro adjustment value	VinP/N20 formula
VinP/N20	VMP0 [7:0] = 0000_0000	$(536R / 600R) * VSP/NR$
	VMP0 [7:0] = 0000_0001	$((536R - 1R) / 600R) * VSP/NR$
	VMP0 [7:0] = 0000_0010	$((536R - 2R) / 600R) * VSP/NR$
	VMP0 [7:0] = 0000_0011	$((536R - 3R) / 600R) * VSP/NR$
	VMP0 [7:0] = 0000_0100	$((536R - 4R) / 600R) * VSP/NR$
	VMP0 [7:0] = 0000_0101	$((536R - 5R) / 600R) * VSP/NR$
	:	:
	VMP0 [7:0] = 1000_0001	$((536R - 129R) / 600R) * VSP/NR$
	VMP0 [7:0] = 1000_0010	$((536R - 130R) / 600R) * VSP/NR$
	VMP0 [7:0] = 1000_0011	$((536R - 131R) / 600R) * VSP/NR$
	VMP0 [7:0] = 1000_0100	$((536R - 132R) / 600R) * VSP/NR$
	VMP0 [7:0] = 1000_0101	$((536R - 133R) / 600R) * VSP/NR$
	:	:
	VMP0 [7:0] = 1111_1011	$((536R - 251R) / 600R) * VSP/NR$
	VMP0 [7:0] = 1111_1100	$((536R - 252R) / 600R) * VSP/NR$
	VMP0 [7:0] = 1111_1101	$((536R - 253R) / 600R) * VSP/NR$
VMP0 [7:0] = 1111_1110	$((536R - 254R) / 600R) * VSP/NR$	
VMP0 [7:0] = 1111_1111	$((536R - 255R) / 600R) * VSP/NR$	

Table 5.12: VinP/N20

Reference voltage	Macro adjustment value	VinP/N28 formula
VinP/N28	VMP1 [7:0] = 0000_0000	$(520R / 600R) * VSP/NR$
	VMP1 [7:0] = 0000_0001	$((520R - 1R) / 600R) * VSP/NR$
	VMP1 [7:0] = 0000_0010	$((520R - 2R) / 600R) * VSP/NR$
	VMP1 [7:0] = 0000_0011	$((520R - 3R) / 600R) * VSP/NR$
	VMP1 [7:0] = 0000_0100	$((520R - 4R) / 600R) * VSP/NR$
	VMP1 [7:0] = 0000_0101	$((520R - 5R) / 600R) * VSP/NR$
	:	:
	VMP1 [7:0] = 1000_0001	$((520R - 129R) / 600R) * VSP/NR$
	VMP1 [7:0] = 1000_0010	$((520R - 130R) / 600R) * VSP/NR$
	VMP1 [7:0] = 1000_0011	$((520R - 131R) / 600R) * VSP/NR$
	VMP1 [7:0] = 1000_0100	$((520R - 132R) / 600R) * VSP/NR$
	VMP1 [7:0] = 1000_0101	$((520R - 133R) / 600R) * VSP/NR$
	:	:
	VMP1 [7:0] = 1111_1011	$((520R - 251R) / 600R) * VSP/NR$
	VMP1 [7:0] = 1111_1100	$((520R - 252R) / 600R) * VSP/NR$
	VMP1 [7:0] = 1111_1101	$((520R - 253R) / 600R) * VSP/NR$
VMP1 [7:0] = 1111_1110	$((520R - 254R) / 600R) * VSP/NR$	
VMP1 [7:0] = 1111_1111	$((520R - 255R) / 600R) * VSP/NR$	

Table 5.13: VinP/N28

Reference voltage	Macro adjustment value	VinP/N40 formula
VinP/N40	VMP2 [7:0] = 0000_0000	$(504R / 600R) * VSP/NR$
	VMP2 [7:0] = 0000_0001	$((504R - 1R) / 600R) * VSP/NR$
	VMP2 [7:0] = 0000_0010	$((504R - 2R) / 600R) * VSP/NR$
	VMP2 [7:0] = 0000_0011	$((504R - 3R) / 600R) * VSP/NR$
	VMP2 [7:0] = 0000_0100	$((504R - 4R) / 600R) * VSP/NR$
	VMP2 [7:0] = 0000_0101	$((504R - 5R) / 600R) * VSP/NR$
	:	:
	VMP2 [7:0] = 1000_0001	$((504R - 129R) / 600R) * VSP/NR$
	VMP2 [7:0] = 1000_0010	$((504R - 130R) / 600R) * VSP/NR$
	VMP2 [7:0] = 1000_0011	$((504R - 131R) / 600R) * VSP/NR$
	VMP2 [7:0] = 1000_0100	$((504R - 132R) / 600R) * VSP/NR$
	VMP2 [7:0] = 1000_0101	$((504R - 133R) / 600R) * VSP/NR$
	:	:
	VMP2 [7:0] = 1111_1011	$((504R - 251R) / 600R) * VSP/NR$
	VMP2 [7:0] = 1111_1100	$((504R - 252R) / 600R) * VSP/NR$
	VMP2 [7:0] = 1111_1101	$((504R - 253R) / 600R) * VSP/NR$
VMP2 [7:0] = 1111_1110	$((504R - 254R) / 600R) * VSP/NR$	
VMP2 [7:0] = 1111_1111	$((504R - 255R) / 600R) * VSP/NR$	

Table 5.14: VinP/N40

Reference voltage	Macro adjustment value	VinP/N52 formula
VinP/N52	VMP3 [7:0] = 0000_0000	$(476R / 600R) * VSP/NR$
	VMP3 [7:0] = 0000_0001	$((476R - 1R) / 600R) * VSP/NR$
	VMP3 [7:0] = 0000_0010	$((476R - 2R) / 600R) * VSP/NR$
	VMP3 [7:0] = 0000_0011	$((476R - 3R) / 600R) * VSP/NR$
	VMP3 [7:0] = 0000_0100	$((476R - 4R) / 600R) * VSP/NR$
	VMP3 [7:0] = 0000_0101	$((476R - 5R) / 600R) * VSP/NR$
	:	:
	VMP3 [7:0] = 1000_0001	$((476R - 129R) / 600R) * VSP/NR$
	VMP3 [7:0] = 1000_0010	$((476R - 130R) / 600R) * VSP/NR$
	VMP3 [7:0] = 1000_0011	$((476R - 131R) / 600R) * VSP/NR$
	VMP3 [7:0] = 1000_0100	$((476R - 132R) / 600R) * VSP/NR$
	VMP3 [7:0] = 1000_0101	$((476R - 133R) / 600R) * VSP/NR$
	:	:
	VMP3 [7:0] = 1111_1011	$((476R - 251R) / 600R) * VSP/NR$
	VMP3 [7:0] = 1111_1100	$((476R - 252R) / 600R) * VSP/NR$
	VMP3 [7:0] = 1111_1101	$((476R - 253R) / 600R) * VSP/NR$
VMP3 [7:0] = 1111_1110	$((476R - 254R) / 600R) * VSP/NR$	
VMP3 [7:0] = 1111_1111	$((476R - 255R) / 600R) * VSP/NR$	

Table 5.15: VinP/N52

Reference voltage	Macro adjustment value	VinP/N64 formula
VinP/N64	VMP4 [7:0] = 0000_0000	$(464R / 600R) * VSP/NR$
	VMP4 [7:0] = 0000_0001	$((464R - 1R) / 600R) * VSP/NR$
	VMP4 [7:0] = 0000_0010	$((464R - 2R) / 600R) * VSP/NR$
	VMP4 [7:0] = 0000_0011	$((464R - 3R) / 600R) * VSP/NR$
	VMP4 [7:0] = 0000_0100	$((464R - 4R) / 600R) * VSP/NR$
	VMP4 [7:0] = 0000_0101	$((464R - 5R) / 600R) * VSP/NR$
	:	:
	VMP4 [7:0] = 1000_0001	$((464R - 129R) / 600R) * VSP/NR$
	VMP4 [7:0] = 1000_0010	$((464R - 130R) / 600R) * VSP/NR$
	VMP4 [7:0] = 1000_0011	$((464R - 131R) / 600R) * VSP/NR$
	VMP4 [7:0] = 1000_0100	$((464R - 132R) / 600R) * VSP/NR$
	VMP4 [7:0] = 1000_0101	$((464R - 133R) / 600R) * VSP/NR$
	:	:
	VMP4 [7:0] = 1111_1011	$((464R - 251R) / 600R) * VSP/NR$
	VMP4 [7:0] = 1111_1100	$((464R - 252R) / 600R) * VSP/NR$
	VMP4 [7:0] = 1111_1101	$((464R - 253R) / 600R) * VSP/NR$
VMP4 [7:0] = 1111_1110	$((464R - 254R) / 600R) * VSP/NR$	
VMP4 [7:0] = 1111_1111	$((464R - 255R) / 600R) * VSP/NR$	

Table 5.16: VinP/N64

Reference voltage	Macro adjustment value	VinP/N76 formula
VinP/N76	VMP5 [7:0] = 0000_0000	$(456R / 600R) * VSP/NR$
	VMP5 [7:0] = 0000_0001	$((456R - 1R) / 600R) * VSP/NR$
	VMP5 [7:0] = 0000_0010	$((456R - 2R) / 600R) * VSP/NR$
	VMP5 [7:0] = 0000_0011	$((456R - 3R) / 600R) * VSP/NR$
	VMP5 [7:0] = 0000_0100	$((456R - 4R) / 600R) * VSP/NR$
	VMP5 [7:0] = 0000_0101	$((456R - 5R) / 600R) * VSP/NR$
	:	:
	VMP5 [7:0] = 1000_0001	$((456R - 129R) / 600R) * VSP/NR$
	VMP5 [7:0] = 1000_0010	$((456R - 130R) / 600R) * VSP/NR$
	VMP5 [7:0] = 1000_0011	$((456R - 131R) / 600R) * VSP/NR$
	VMP5 [7:0] = 1000_0100	$((456R - 132R) / 600R) * VSP/NR$
	VMP5 [7:0] = 1000_0101	$((456R - 133R) / 600R) * VSP/NR$
	:	:
	VMP5 [7:0] = 1111_1011	$((456R - 251R) / 600R) * VSP/NR$
	VMP5 [7:0] = 1111_1100	$((456R - 252R) / 600R) * VSP/NR$
	VMP5 [7:0] = 1111_1101	$((456R - 253R) / 600R) * VSP/NR$
VMP5 [7:0] = 1111_1110	$((456R - 254R) / 600R) * VSP/NR$	
VMP5 [7:0] = 1111_1111	$((456R - 255R) / 600R) * VSP/NR$	

Table 5.17: VinP/N76

Reference voltage	Macro adjustment value	VinP/N88 formula
VinP/N88	VMP6 [7:0] = 0000_0000	$(448R / 600R) * VSP/NR$
	VMP6 [7:0] = 0000_0001	$((448R - 1R) / 600R) * VSP/NR$
	VMP6 [7:0] = 0000_0010	$((448R - 2R) / 600R) * VSP/NR$
	VMP6 [7:0] = 0000_0011	$((448R - 3R) / 600R) * VSP/NR$
	VMP6 [7:0] = 0000_0100	$((448R - 4R) / 600R) * VSP/NR$
	VMP6 [7:0] = 0000_0101	$((448R - 5R) / 600R) * VSP/NR$
	:	:
	VMP6 [7:0] = 1000_0001	$((448R - 129R) / 600R) * VSP/NR$
	VMP6 [7:0] = 1000_0010	$((448R - 130R) / 600R) * VSP/NR$
	VMP6 [7:0] = 1000_0011	$((448R - 131R) / 600R) * VSP/NR$
	VMP6 [7:0] = 1000_0100	$((448R - 132R) / 600R) * VSP/NR$
	VMP6 [7:0] = 1000_0101	$((448R - 133R) / 600R) * VSP/NR$
	:	:
	VMP6 [7:0] = 1111_1011	$((448R - 251R) / 600R) * VSP/NR$
	VMP6 [7:0] = 1111_1100	$((448R - 252R) / 600R) * VSP/NR$
	VMP6 [7:0] = 1111_1101	$((448R - 253R) / 600R) * VSP/NR$
VMP6 [7:0] = 1111_1110	$((448R - 254R) / 600R) * VSP/NR$	
VMP6 [7:0] = 1111_1111	$((448R - 255R) / 600R) * VSP/NR$	

Table 5.18: VinP/N88

Reference voltage	Macro adjustment value	VinP/N100 formula
VinP/N100	VMP7 [7:0] = 0000_0000	$(440R / 600R) * VSP/NR$
	VMP7 [7:0] = 0000_0001	$((440R - 1R) / 600R) * VSP/NR$
	VMP7 [7:0] = 0000_0010	$((440R - 2R) / 600R) * VSP/NR$
	VMP7 [7:0] = 0000_0011	$((440R - 3R) / 600R) * VSP/NR$
	VMP7 [7:0] = 0000_0100	$((440R - 4R) / 600R) * VSP/NR$
	VMP7 [7:0] = 0000_0101	$((440R - 5R) / 600R) * VSP/NR$
	:	:
	VMP7 [7:0] = 1000_0001	$((440R - 129R) / 600R) * VSP/NR$
	VMP7 [7:0] = 1000_0010	$((440R - 130R) / 600R) * VSP/NR$
	VMP7 [7:0] = 1000_0011	$((440R - 131R) / 600R) * VSP/NR$
	VMP7 [7:0] = 1000_0100	$((440R - 132R) / 600R) * VSP/NR$
	VMP7 [7:0] = 1000_0101	$((440R - 133R) / 600R) * VSP/NR$
	:	:
	VMP7 [7:0] = 1111_1011	$((440R - 251R) / 600R) * VSP/NR$
	VMP7 [7:0] = 1111_1100	$((440R - 252R) / 600R) * VSP/NR$
	VMP7 [7:0] = 1111_1101	$((440R - 253R) / 600R) * VSP/NR$
VMP7 [7:0] = 1111_1110	$((440R - 254R) / 600R) * VSP/NR$	
VMP7 [7:0] = 1111_1111	$((440R - 255R) / 600R) * VSP/NR$	

Table 5.19: VinP/N100

Reference voltage	Macro adjustment value	VinP/N112 formula
VinP/N112	VMP8 [7:0] = 0000_0000	$(432R / 600R) * VSP/NR$
	VMP8 [7:0] = 0000_0001	$((432R - 1R) / 600R) * VSP/NR$
	VMP8 [7:0] = 0000_0010	$((432R - 2R) / 600R) * VSP/NR$
	VMP8 [7:0] = 0000_0011	$((432R - 3R) / 600R) * VSP/NR$
	VMP8 [7:0] = 0000_0100	$((432R - 4R) / 600R) * VSP/NR$
	VMP8 [7:0] = 0000_0101	$((432R - 5R) / 600R) * VSP/NR$
	:	:
	VMP8 [7:0] = 1000_0001	$((432R - 129R) / 600R) * VSP/NR$
	VMP8 [7:0] = 1000_0010	$((432R - 130R) / 600R) * VSP/NR$
	VMP8 [7:0] = 1000_0011	$((432R - 131R) / 600R) * VSP/NR$
	VMP8 [7:0] = 1000_0100	$((432R - 132R) / 600R) * VSP/NR$
	VMP8 [7:0] = 1000_0101	$((432R - 133R) / 600R) * VSP/NR$
	:	:
	VMP8 [7:0] = 1111_1011	$((432R - 251R) / 600R) * VSP/NR$
	VMP8 [7:0] = 1111_1100	$((432R - 252R) / 600R) * VSP/NR$
	VMP8 [7:0] = 1111_1101	$((432R - 253R) / 600R) * VSP/NR$
VMP8 [7:0] = 1111_1110	$((432R - 254R) / 600R) * VSP/NR$	
VMP8 [7:0] = 1111_1111	$((432R - 255R) / 600R) * VSP/NR$	

Table 5.20: VinP/N112

Reference voltage	Macro adjustment value	VinP/N128 formula
VinP/N128	VMP9 [7:0] = 0000_0000	$(424R / 600R) * VSP/NR$
	VMP9 [7:0] = 0000_0001	$((424R - 1R) / 600R) * VSP/NR$
	VMP9 [7:0] = 0000_0010	$((424R - 2R) / 600R) * VSP/NR$
	VMP9 [7:0] = 0000_0011	$((424R - 3R) / 600R) * VSP/NR$
	VMP9 [7:0] = 0000_0100	$((424R - 4R) / 600R) * VSP/NR$
	VMP9 [7:0] = 0000_0101	$((424R - 5R) / 600R) * VSP/NR$
	:	:
	VMP9 [7:0] = 1000_0001	$((424R - 129R) / 600R) * VSP/NR$
	VMP9 [7:0] = 1000_0010	$((424R - 130R) / 600R) * VSP/NR$
	VMP9 [7:0] = 1000_0011	$((424R - 131R) / 600R) * VSP/NR$
	VMP9 [7:0] = 1000_0100	$((424R - 132R) / 600R) * VSP/NR$
	VMP9 [7:0] = 1000_0101	$((424R - 133R) / 600R) * VSP/NR$
	:	:
	VMP9 [7:0] = 1111_1011	$((424R - 251R) / 600R) * VSP/NR$
	VMP9 [7:0] = 1111_1100	$((424R - 252R) / 600R) * VSP/NR$
	VMP9 [7:0] = 1111_1101	$((424R - 253R) / 600R) * VSP/NR$
VMP9 [7:0] = 1111_1110	$((424R - 254R) / 600R) * VSP/NR$	
VMP9 [7:0] = 1111_1111	$((424R - 255R) / 600R) * VSP/NR$	

Table 5.21: VinP/N128

Reference voltage	Macro adjustment value	VinP/N144 formula
VinP/N144	VMP10 [7:0] = 0000_0000	$(415R / 600R) * VSP/NR$
	VMP10 [7:0] = 0000_0001	$((415R - 1R) / 600R) * VSP/NR$
	VMP10 [7:0] = 0000_0010	$((415R - 2R) / 600R) * VSP/NR$
	VMP10 [7:0] = 0000_0011	$((415R - 3R) / 600R) * VSP/NR$
	VMP10 [7:0] = 0000_0100	$((415R - 4R) / 600R) * VSP/NR$
	VMP10 [7:0] = 0000_0101	$((415R - 5R) / 600R) * VSP/NR$
	:	:
	VMP10 [7:0] = 1000_0001	$((415R - 129R) / 600R) * VSP/NR$
	VMP10 [7:0] = 1000_0010	$((415R - 130R) / 600R) * VSP/NR$
	VMP10 [7:0] = 1000_0011	$((415R - 131R) / 600R) * VSP/NR$
	VMP10 [7:0] = 1000_0100	$((415R - 132R) / 600R) * VSP/NR$
	VMP10 [7:0] = 1000_0101	$((415R - 133R) / 600R) * VSP/NR$
	:	:
	VMP10 [7:0] = 1111_1011	$((415R - 251R) / 600R) * VSP/NR$
	VMP10 [7:0] = 1111_1100	$((415R - 252R) / 600R) * VSP/NR$
	VMP10 [7:0] = 1111_1101	$((415R - 253R) / 600R) * VSP/NR$
VMP10 [7:0] = 1111_1110	$((415R - 254R) / 600R) * VSP/NR$	
VMP10 [7:0] = 1111_1111	$((415R - 255R) / 600R) * VSP/NR$	

Table 5.22: VinP/N144

Reference voltage	Macro adjustment value	VinP/N156 formula
VinP/N156	VMP11 [7:0] = 0000_0000	$(407R / 600R) * VSP/NR$
	VMP11 [7:0] = 0000_0001	$((407R - 1R) / 600R) * VSP/NR$
	VMP11 [7:0] = 0000_0010	$((407R - 2R) / 600R) * VSP/NR$
	VMP11 [7:0] = 0000_0011	$((407R - 3R) / 600R) * VSP/NR$
	VMP11 [7:0] = 0000_0100	$((407R - 4R) / 600R) * VSP/NR$
	VMP11 [7:0] = 0000_0101	$((407R - 5R) / 600R) * VSP/NR$
	:	:
	VMP11 [7:0] = 1000_0001	$((407R - 129R) / 600R) * VSP/NR$
	VMP11 [7:0] = 1000_0010	$((407R - 130R) / 600R) * VSP/NR$
	VMP11 [7:0] = 1000_0011	$((407R - 131R) / 600R) * VSP/NR$
	VMP11 [7:0] = 1000_0100	$((407R - 132R) / 600R) * VSP/NR$
	VMP11 [7:0] = 1000_0101	$((407R - 133R) / 600R) * VSP/NR$
	:	:
	VMP11 [7:0] = 1111_1011	$((407R - 251R) / 600R) * VSP/NR$
	VMP11 [7:0] = 1111_1100	$((407R - 252R) / 600R) * VSP/NR$
	VMP11 [7:0] = 1111_1101	$((407R - 253R) / 600R) * VSP/NR$
VMP11 [7:0] = 1111_1110	$((407R - 254R) / 600R) * VSP/NR$	
VMP11 [7:0] = 1111_1111	$((407R - 255R) / 600R) * VSP/NR$	

Table 5.23: VinP/N156

Reference voltage	Macro adjustment value	VinP/N168 formula
VinP/N168	VMP12 [7:0] = 0000_0000	$(399R / 600R) * VSP/NR$
	VMP12 [7:0] = 0000_0001	$((399R - 1R) / 600R) * VSP/NR$
	VMP12 [7:0] = 0000_0010	$((399R - 2R) / 600R) * VSP/NR$
	VMP12 [7:0] = 0000_0011	$((399R - 3R) / 600R) * VSP/NR$
	VMP12 [7:0] = 0000_0100	$((399R - 4R) / 600R) * VSP/NR$
	VMP12 [7:0] = 0000_0101	$((399R - 5R) / 600R) * VSP/NR$
	:	:
	VMP12 [7:0] = 1000_0001	$((399R - 129R) / 600R) * VSP/NR$
	VMP12 [7:0] = 1000_0010	$((399R - 130R) / 600R) * VSP/NR$
	VMP12 [7:0] = 1000_0011	$((399R - 131R) / 600R) * VSP/NR$
	VMP12 [7:0] = 1000_0100	$((399R - 132R) / 600R) * VSP/NR$
	VMP12 [7:0] = 1000_0101	$((399R - 133R) / 600R) * VSP/NR$
	:	:
	VMP12 [7:0] = 1111_1011	$((399R - 251R) / 600R) * VSP/NR$
	VMP12 [7:0] = 1111_1100	$((399R - 252R) / 600R) * VSP/NR$
	VMP12 [7:0] = 1111_1101	$((399R - 253R) / 600R) * VSP/NR$
VMP12 [7:0] = 1111_1110	$((399R - 254R) / 600R) * VSP/NR$	
VMP12 [7:0] = 1111_1111	$((399R - 255R) / 600R) * VSP/NR$	

Table 5.24: VinP/N168

Reference voltage	Macro adjustment value	VinP/N180 formula
VinP/N180	VMP13 [7:0] = 0000_0000	$(395R / 600R) * VSP/NR$
	VMP13 [7:0] = 0000_0001	$((395R - 1R) / 600R) * VSP/NR$
	VMP13 [7:0] = 0000_0010	$((395R - 2R) / 600R) * VSP/NR$
	VMP13 [7:0] = 0000_0011	$((395R - 3R) / 600R) * VSP/NR$
	VMP13 [7:0] = 0000_0100	$((395R - 4R) / 600R) * VSP/NR$
	VMP13 [7:0] = 0000_0101	$((395R - 5R) / 600R) * VSP/NR$
	:	:
	VMP13 [7:0] = 1000_0001	$((395R - 129R) / 600R) * VSP/NR$
	VMP13 [7:0] = 1000_0010	$((395R - 130R) / 600R) * VSP/NR$
	VMP13 [7:0] = 1000_0011	$((395R - 131R) / 600R) * VSP/NR$
	VMP13 [7:0] = 1000_0100	$((395R - 132R) / 600R) * VSP/NR$
	VMP13 [7:0] = 1000_0101	$((395R - 133R) / 600R) * VSP/NR$
	:	:
	VMP13 [7:0] = 1111_1011	$((395R - 251R) / 600R) * VSP/NR$
	VMP13 [7:0] = 1111_1100	$((395R - 252R) / 600R) * VSP/NR$
	VMP13 [7:0] = 1111_1101	$((395R - 253R) / 600R) * VSP/NR$
VMP13 [7:0] = 1111_1110	$((395R - 254R) / 600R) * VSP/NR$	
VMP13 [7:0] = 1111_1111	$((395R - 255R) / 600R) * VSP/NR$	

Table 5.25: VinP/N180

Reference voltage	Macro adjustment value	VinP/N192 formula
VinP/N192	VMP14 [7:0] = 0000_0000	$(383R / 600R) * VSP/NR$
	VMP14 [7:0] = 0000_0001	$((383R - 1R) / 600R) * VSP/NR$
	VMP14 [7:0] = 0000_0010	$((383R - 2R) / 600R) * VSP/NR$
	VMP14 [7:0] = 0000_0011	$((383R - 3R) / 600R) * VSP/NR$
	VMP14 [7:0] = 0000_0100	$((383R - 4R) / 600R) * VSP/NR$
	VMP14 [7:0] = 0000_0101	$((383R - 5R) / 600R) * VSP/NR$
	:	:
	VMP14 [7:0] = 1000_0001	$((383R - 129R) / 600R) * VSP/NR$
	VMP14 [7:0] = 1000_0010	$((383R - 130R) / 600R) * VSP/NR$
	VMP14 [7:0] = 1000_0011	$((383R - 131R) / 600R) * VSP/NR$
	VMP14 [7:0] = 1000_0100	$((383R - 132R) / 600R) * VSP/NR$
	VMP14 [7:0] = 1000_0101	$((383R - 133R) / 600R) * VSP/NR$
	:	:
	VMP14 [7:0] = 1111_1011	$((383R - 251R) / 600R) * VSP/NR$
	VMP14 [7:0] = 1111_1100	$((383R - 252R) / 600R) * VSP/NR$
	VMP14 [7:0] = 1111_1101	$((383R - 253R) / 600R) * VSP/NR$
VMP14 [7:0] = 1111_1110	$((383R - 254R) / 600R) * VSP/NR$	
VMP14 [7:0] = 1111_1111	$((383R - 255R) / 600R) * VSP/NR$	

Table 5.26: VinP/N192

Reference voltage	Macro adjustment value	VinP/N204 formula
VinP/N204	VMP15 [7:0] = 0000_0000	$(375R / 600R) * VSP/NR$
	VMP15 [7:0] = 0000_0001	$((375R - 1R) / 600R) * VSP/NR$
	VMP15 [7:0] = 0000_0010	$((375R - 2R) / 600R) * VSP/NR$
	VMP15 [7:0] = 0000_0011	$((375R - 3R) / 600R) * VSP/NR$
	VMP15 [7:0] = 0000_0100	$((375R - 4R) / 600R) * VSP/NR$
	VMP15 [7:0] = 0000_0101	$((375R - 5R) / 600R) * VSP/NR$
	:	:
	VMP15 [7:0] = 1000_0001	$((375R - 129R) / 600R) * VSP/NR$
	VMP15 [7:0] = 1000_0010	$((375R - 130R) / 600R) * VSP/NR$
	VMP15 [7:0] = 1000_0011	$((375R - 131R) / 600R) * VSP/NR$
	VMP15 [7:0] = 1000_0100	$((375R - 132R) / 600R) * VSP/NR$
	VMP15 [7:0] = 1000_0101	$((375R - 133R) / 600R) * VSP/NR$
	:	:
	VMP15 [7:0] = 1111_1011	$((375R - 251R) / 600R) * VSP/NR$
	VMP15 [7:0] = 1111_1100	$((375R - 252R) / 600R) * VSP/NR$
	VMP15 [7:0] = 1111_1101	$((375R - 253R) / 600R) * VSP/NR$
VMP15 [7:0] = 1111_1110	$((375R - 254R) / 600R) * VSP/NR$	
VMP15 [7:0] = 1111_1111	$((375R - 255R) / 600R) * VSP/NR$	

Table 5.27: VinP/N204

Reference voltage	Macro adjustment value	VinP/N216 formula
VinP/N216	VMP16 [7:0] = 0000_0000	$(343R / 600R) * VSP/NR$
	VMP16 [7:0] = 0000_0001	$((343R - 1R) / 600R) * VSP/NR$
	VMP16 [7:0] = 0000_0010	$((343R - 2R) / 600R) * VSP/NR$
	VMP16 [7:0] = 0000_0011	$((343R - 3R) / 600R) * VSP/NR$
	VMP16 [7:0] = 0000_0100	$((343R - 4R) / 600R) * VSP/NR$
	VMP16 [7:0] = 0000_0101	$((343R - 5R) / 600R) * VSP/NR$
	:	:
	VMP16 [7:0] = 1000_0001	$((343R - 129R) / 600R) * VSP/NR$
	VMP16 [7:0] = 1000_0010	$((343R - 130R) / 600R) * VSP/NR$
	VMP16 [7:0] = 1000_0011	$((343R - 131R) / 600R) * VSP/NR$
	VMP16 [7:0] = 1000_0100	$((343R - 132R) / 600R) * VSP/NR$
	VMP16 [7:0] = 1000_0101	$((343R - 133R) / 600R) * VSP/NR$
	:	:
	VMP16 [7:0] = 1111_1011	$((343R - 251R) / 600R) * VSP/NR$
	VMP16 [7:0] = 1111_1100	$((343R - 252R) / 600R) * VSP/NR$
	VMP16 [7:0] = 1111_1101	$((343R - 253R) / 600R) * VSP/NR$
VMP16 [7:0] = 1111_1110	$((343R - 254R) / 600R) * VSP/NR$	
VMP16 [7:0] = 1111_1111	$((343R - 255R) / 600R) * VSP/NR$	

Table 5.28: VinP/N216

Reference voltage	Macro adjustment value	VinP/N228 formula
VinP/N228	VMP17 [7:0] = 0000_0000	$(331R / 600R) * VSP/NR$
	VMP17 [7:0] = 0000_0001	$((331R - 1R) / 600R) * VSP/NR$
	VMP17 [7:0] = 0000_0010	$((331R - 2R) / 600R) * VSP/NR$
	VMP17 [7:0] = 0000_0011	$((331R - 3R) / 600R) * VSP/NR$
	VMP17 [7:0] = 0000_0100	$((331R - 4R) / 600R) * VSP/NR$
	VMP17 [7:0] = 0000_0101	$((331R - 5R) / 600R) * VSP/NR$
	:	:
	VMP17 [7:0] = 1000_0001	$((331R - 129R) / 600R) * VSP/NR$
	VMP17 [7:0] = 1000_0010	$((331R - 130R) / 600R) * VSP/NR$
	VMP17 [7:0] = 1000_0011	$((331R - 131R) / 600R) * VSP/NR$
	VMP17 [7:0] = 1000_0100	$((331R - 132R) / 600R) * VSP/NR$
	VMP17 [7:0] = 1000_0101	$((331R - 133R) / 600R) * VSP/NR$
	:	:
	VMP17 [7:0] = 1111_1011	$((331R - 251R) / 600R) * VSP/NR$
	VMP17 [7:0] = 1111_1100	$((331R - 252R) / 600R) * VSP/NR$
	VMP17 [7:0] = 1111_1101	$((331R - 253R) / 600R) * VSP/NR$
	VMP17 [7:0] = 1111_1110	$((331R - 254R) / 600R) * VSP/NR$
VMP17 [7:0] = 1111_1111	$((331R - 255R) / 600R) * VSP/NR$	

Table 5.29: VinP/N228

Reference voltage	Macro adjustment value	VinP/N236 formula
VinP/N236	VMP18 [7:0] = 0000_0000	$(311R / 600R) * VSP/NR$
	VMP18 [7:0] = 0000_0001	$((311R - 1R) / 600R) * VSP/NR$
	VMP18 [7:0] = 0000_0010	$((311R - 2R) / 600R) * VSP/NR$
	VMP18 [7:0] = 0000_0011	$((311R - 3R) / 600R) * VSP/NR$
	VMP18 [7:0] = 0000_0100	$((311R - 4R) / 600R) * VSP/NR$
	VMP18 [7:0] = 0000_0101	$((311R - 5R) / 600R) * VSP/NR$
	:	:
	VMP18 [7:0] = 1000_0001	$((311R - 129R) / 600R) * VSP/NR$
	VMP18 [7:0] = 1000_0010	$((311R - 130R) / 600R) * VSP/NR$
	VMP18 [7:0] = 1000_0011	$((311R - 131R) / 600R) * VSP/NR$
	VMP18 [7:0] = 1000_0100	$((311R - 132R) / 600R) * VSP/NR$
	VMP18 [7:0] = 1000_0101	$((311R - 133R) / 600R) * VSP/NR$
	:	:
	VMP18 [7:0] = 1111_1011	$((311R - 251R) / 600R) * VSP/NR$
	VMP18 [7:0] = 1111_1100	$((311R - 252R) / 600R) * VSP/NR$
	VMP18 [7:0] = 1111_1101	$((311R - 253R) / 600R) * VSP/NR$
	VMP18 [7:0] = 1111_1110	$((311R - 254R) / 600R) * VSP/NR$
VMP18 [7:0] = 1111_1111	$((311R - 255R) / 600R) * VSP/NR$	

Table 5.30: VinP/N236

Reference voltage	Macro adjustment value	VinP/N243 formula
VinP/N243	VLP0 [6:0] = 000_0000	$(290R / 600R) * VSP/NR$
	VLP0 [6:0] = 000_0001	$((290R - 2R) / 600R) * VSP/NR$
	VLP0 [6:0] = 000_0010	$((290R - 4R) / 600R) * VSP/NR$
	VLP0 [6:0] = 000_0011	$((290R - 6R) / 600R) * VSP/NR$
	VLP0 [6:0] = 000_0100	$((290R - 8R) / 600R) * VSP/NR$
	VLP0 [6:0] = 000_0101	$((290R - 10R) / 600R) * VSP/NR$
	:	:
	VLP0 [6:0] = 100_0001	$((290R - 130R) / 600R) * VSP/NR$
	VLP0 [6:0] = 100_0010	$((290R - 132R) / 600R) * VSP/NR$
	VLP0 [6:0] = 100_0011	$((290R - 134R) / 600R) * VSP/NR$
	VLP0 [6:0] = 100_0100	$((290R - 136R) / 600R) * VSP/NR$
	VLP0 [6:0] = 100_0101	$((290R - 138R) / 600R) * VSP/NR$
	:	:
	VLP0 [6:0] = 111_1011	$((290R - 246R) / 600R) * VSP/NR$
	VLP0 [6:0] = 111_1100	$((290R - 248R) / 600R) * VSP/NR$
	VLP0 [6:0] = 111_1101	$((290R - 250R) / 600R) * VSP/NR$
	VLP0 [6:0] = 111_1110	$((290R - 252R) / 600R) * VSP/NR$
VLP0 [6:0] = 111_1111	$((290R - 254R) / 600R) * VSP/NR$	

Table 5.31: VinP/N243

Reference voltage	Macro adjustment value	VinP/N247 formula
VinP/N247	VLP1 [6:0] = 000_0000	$(262R / 600R) * VSP/NR$
	VLP1 [6:0] = 000_0001	$((262R - 2R) / 600R) * VSP/NR$
	VLP1 [6:0] = 000_0010	$((262R - 4R) / 600R) * VSP/NR$
	VLP1 [6:0] = 000_0011	$((262R - 6R) / 600R) * VSP/NR$
	VLP1 [6:0] = 000_0100	$((262R - 8R) / 600R) * VSP/NR$
	VLP1 [6:0] = 000_0101	$((262R - 10R) / 600R) * VSP/NR$
	:	:
	VLP1 [6:0] = 100_0001	$((262R - 130R) / 600R) * VSP/NR$
	VLP1 [6:0] = 100_0010	$((262R - 132R) / 600R) * VSP/NR$
	VLP1 [6:0] = 100_0011	$((262R - 134R) / 600R) * VSP/NR$
	VLP1 [6:0] = 100_0100	$((262R - 136R) / 600R) * VSP/NR$
	VLP1 [6:0] = 100_0101	$((262R - 138R) / 600R) * VSP/NR$
	:	:
	VLP1 [6:0] = 111_1011	$((262R - 246R) / 600R) * VSP/NR$
	VLP1 [6:0] = 111_1100	$((262R - 248R) / 600R) * VSP/NR$
	VLP1 [6:0] = 111_1101	$((262R - 250R) / 600R) * VSP/NR$
VLP1 [6:0] = 111_1110	$((262R - 252R) / 600R) * VSP/NR$	
VLP1 [6:0] = 111_1111	$((262R - 254R) / 600R) * VSP/NR$	

Table 5.32: VinP/N247

Reference voltage	Macro adjustment value	VinP/N251 formula
VinP/N251	VLP2 [6:0] = 000_0000	$(258R / 600R) * VSP/NR$
	VLP2 [6:0] = 000_0001	$((258R - 2R) / 600R) * VSP/NR$
	VLP2 [6:0] = 000_0010	$((258R - 4R) / 600R) * VSP/NR$
	VLP2 [6:0] = 000_0011	$((258R - 6R) / 600R) * VSP/NR$
	VLP2 [6:0] = 000_0100	$((258R - 8R) / 600R) * VSP/NR$
	VLP2 [6:0] = 000_0101	$((258R - 10R) / 600R) * VSP/NR$
	:	:
	VLP2 [6:0] = 100_0001	$((258R - 130R) / 600R) * VSP/NR$
	VLP2 [6:0] = 100_0010	$((258R - 132R) / 600R) * VSP/NR$
	VLP2 [6:0] = 100_0011	$((258R - 134R) / 600R) * VSP/NR$
	VLP2 [6:0] = 100_0100	$((258R - 136R) / 600R) * VSP/NR$
	VLP2 [6:0] = 100_0101	$((258R - 138R) / 600R) * VSP/NR$
	:	:
	VLP2 [6:0] = 111_1011	$((258R - 246R) / 600R) * VSP/NR$
	VLP2 [6:0] = 111_1100	$((258R - 248R) / 600R) * VSP/NR$
	VLP2 [6:0] = 111_1101	$((258R - 250R) / 600R) * VSP/NR$
VLP2 [6:0] = 111_1110	$((258R - 252R) / 600R) * VSP/NR$	
VLP2 [6:0] = 111_1111	$((258R - 254R) / 600R) * VSP/NR$	

Table 5.33: VinP/N251

Reference voltage	Macro adjustment value	VinP/N255 formula
VinP/N255	VLP3 [6:0] = 000_0000	$(254R / 600R) * VSP/NR$
	VLP3 [6:0] = 000_0001	$((254R - 2R) / 600R) * VSP/NR$
	VLP3 [6:0] = 000_0010	$((254R - 4R) / 600R) * VSP/NR$
	VLP3 [6:0] = 000_0011	$((254R - 6R) / 600R) * VSP/NR$
	VLP3 [6:0] = 000_0100	$((254R - 8R) / 600R) * VSP/NR$
	VLP3 [6:0] = 000_0101	$((254R - 10R) / 600R) * VSP/NR$
	:	:
	VLP3 [6:0] = 100_0001	$((254R - 130R) / 600R) * VSP/NR$
	VLP3 [6:0] = 100_0010	$((254R - 132R) / 600R) * VSP/NR$
	VLP3 [6:0] = 100_0011	$((254R - 134R) / 600R) * VSP/NR$
	VLP3 [6:0] = 100_0100	$((254R - 136R) / 600R) * VSP/NR$
	VLP3 [6:0] = 100_0101	$((254R - 138R) / 600R) * VSP/NR$
	:	:
	VLP3 [6:0] = 111_1011	$((254R - 246R) / 600R) * VSP/NR$
	VLP3 [6:0] = 111_1100	$((254R - 248R) / 600R) * VSP/NR$
	VLP3 [6:0] = 111_1101	$((254R - 250R) / 600R) * VSP/NR$
VLP3 [6:0] = 111_1110	$((254R - 252R) / 600R) * VSP/NR$	
VLP3 [6:0] = 111_1111	$((254R - 254R) / 600R) * VSP/NR$	

Table 5.34: VinP/N255

Grayscale voltage (NW/NB)	Formula
V0/V255	VinP/N0
V1/V254	VinP/N0 - (VinP/N0 - VinP/N4)*(R/4R)
V2/V253	VinP/N0 - (VinP/N0 - VinP/N4)*(2R/4R)
V3/V252	VinP/N0 - (VinP/N0 - VinP/N4)*(3R/4R)
V4/V251	VinP/N4
V5/V250	VinP/N4 - (VinP/N4 - VinP/N8)*(R/4R)
V6/V249	VinP/N4 - (VinP/N4 - VinP/N8)*(2R/4R)
V7/V248	VinP/N4 - (VinP/N4 - VinP/N8)*(3R/4R)
V8/V247	VinP/N8
V9/V246	VinP/N8 - (VinP/N8 - VinP/N12)*(R/4R)
V10/V245	VinP/N8 - (VinP/N8 - VinP/N12)*(2R/4R)
V11/V244	VinP/N8 - (VinP/N8 - VinP/N12)*(3R/4R)
V12/V243	VinP/N12
V13/V242	VinP/N12 - (VinP/N12 - VinP/N20)*(1R/8R)
V14/V241	VinP/N12 - (VinP/N12 - VinP/N20)*(2R/8R)
V15/V240	VinP/N12 - (VinP/N12 - VinP/N20)*(3R/8R)
V16/V239	VinP/N12 - (VinP/N12 - VinP/N20)*(4R/8R)
V17/V238	VinP/N12 - (VinP/N12 - VinP/N20)*(5R/8R)
V18/V237	VinP/N12 - (VinP/N12 - VinP/N20)*(6R/8R)
V19/V236	VinP/N12 - (VinP/N12 - VinP/N20)*(7R/8R)
V20/V235	VinP/N20
V21/V234	VinP/N20 - (VinP/N20 - VinP/N28)*(1R/8R)
V22/V233	VinP/N20 - (VinP/N20 - VinP/N28)*(2R/8R)
V23/V232	VinP/N20 - (VinP/N20 - VinP/N28)*(3R/8R)
V24/V231	VinP/N20 - (VinP/N20 - VinP/N28)*(4R/8R)
V25/V230	VinP/N20 - (VinP/N20 - VinP/N28)*(5R/8R)
V26/V229	VinP/N20 - (VinP/N20 - VinP/N28)*(6R/8R)
V27/V228	VinP/N20 - (VinP/N20 - VinP/N28)*(7R/8R)
V28/V227	VinP/N28
V29/V226	VinP/N28 - (VinP/N28 - VinP/N40)*(1R/12R)
V30/V225	VinP/N28 - (VinP/N28 - VinP/N40)*(2R/12R)
V31/V224	VinP/N28 - (VinP/N28 - VinP/N40)*(3R/12R)
V32/V223	VinP/N28 - (VinP/N28 - VinP/N40)*(4R/12R)
V33/V222	VinP/N28 - (VinP/N28 - VinP/N40)*(5R/12R)
V34/V221	VinP/N28 - (VinP/N28 - VinP/N40)*(6R/12R)
V35/V220	VinP/N28 - (VinP/N28 - VinP/N40)*(7R/12R)
V36/V219	VinP/N28 - (VinP/N28 - VinP/N40)*(8R/12R)
V37/V218	VinP/N28 - (VinP/N28 - VinP/N40)*(9R/12R)
V38/V217	VinP/N28 - (VinP/N28 - VinP/N40)*(10R/12R)
V39/V216	VinP/N28 - (VinP/N28 - VinP/N40)*(11R/12R)
V40/V215	VinP/N40
V41/V214	VinP/N40 - (VinP/N40 - VinP/N52)*(1R/12R)
V42/V213	VinP/N40 - (VinP/N40 - VinP/N52)*(2R/12R)
V43/V212	VinP/N40 - (VinP/N40 - VinP/N52)*(3R/12R)

Grayscale voltage (NW/NB)	Formula
V44/V211	VinP/N40 - (VinP/N40 - VinP/N52)*(4R/12R)
V45/V210	VinP/N40 - (VinP/N40 - VinP/N52)*(5R/12R)
V46/V209	VinP/N40 - (VinP/N40 - VinP/N52)*(6R/12R)
V47/V208	VinP/N40 - (VinP/N40 - VinP/N52)*(7R/12R)
V48/V207	VinP/N40 - (VinP/N40 - VinP/N52)*(8R/12R)
V49/V206	VinP/N40 - (VinP/N40 - VinP/N52)*(9R/12R)
V50/V205	VinP/N40 - (VinP/N40 - VinP/N52)*(10R/12R)
V51/V204	VinP/N40 - (VinP/N40 - VinP/N52)*(11R/12R)
V52/V203	VinP/N52
V53/V202	VinP/N52 - (VinP/N52 - VinP/N64)*(1R/12R)
V54/V201	VinP/N52 - (VinP/N52 - VinP/N64)*(2R/12R)
V55/V200	VinP/N52 - (VinP/N52 - VinP/N64)*(3R/12R)
V56/V199	VinP/N52 - (VinP/N52 - VinP/N64)*(4R/12R)
V57/V198	VinP/N52 - (VinP/N52 - VinP/N64)*(5R/12R)
V58/V197	VinP/N52 - (VinP/N52 - VinP/N64)*(6R/12R)
V59/V196	VinP/N52 - (VinP/N52 - VinP/N64)*(7R/12R)
V60/V195	VinP/N52 - (VinP/N52 - VinP/N64)*(8R/12R)
V61/V194	VinP/N52 - (VinP/N52 - VinP/N64)*(9R/12R)
V62/V193	VinP/N52 - (VinP/N52 - VinP/N64)*(10R/12R)
V63/V192	VinP/N52 - (VinP/N52 - VinP/N64)*(11R/12R)
V64/V191	VinP/N64
V65/V190	VinP/N64 - (VinP/N64 - VinP/N76)*(1R/12R)
V66/V189	VinP/N64 - (VinP/N64 - VinP/N76)*(2R/12R)
V67/V188	VinP/N64 - (VinP/N64 - VinP/N76)*(3R/12R)
V68/V187	VinP/N64 - (VinP/N64 - VinP/N76)*(4R/12R)
V69/V186	VinP/N64 - (VinP/N64 - VinP/N76)*(5R/12R)
V70/V185	VinP/N64 - (VinP/N64 - VinP/N76)*(6R/12R)
V71/V184	VinP/N64 - (VinP/N64 - VinP/N76)*(7R/12R)
V72/V183	VinP/N64 - (VinP/N64 - VinP/N76)*(8R/12R)
V73/V182	VinP/N64 - (VinP/N64 - VinP/N76)*(9R/12R)
V74/V181	VinP/N64 - (VinP/N64 - VinP/N76)*(10R/12R)
V75/V180	VinP/N64 - (VinP/N64 - VinP/N76)*(11R/12R)
V76/V179	VinP/N76
V77/V178	VinP/N76 - (VinP/N76 - VinP/N88)*(1R/12R)
V78/V177	VinP/N76 - (VinP/N76 - VinP/N88)*(2R/12R)
V79/V176	VinP/N76 - (VinP/N76 - VinP/N88)*(3R/12R)
V80/V175	VinP/N76 - (VinP/N76 - VinP/N88)*(4R/12R)
V81/V174	VinP/N76 - (VinP/N76 - VinP/N88)*(5R/12R)
V82/V173	VinP/N76 - (VinP/N76 - VinP/N88)*(6R/12R)
V83/V172	VinP/N76 - (VinP/N76 - VinP/N88)*(7R/12R)
V84/V171	VinP/N76 - (VinP/N76 - VinP/N88)*(8R/12R)
V85/V170	VinP/N76 - (VinP/N76 - VinP/N88)*(9R/12R)
V86/V169	VinP/N76 - (VinP/N76 - VinP/N88)*(10R/12R)
V87/V168	VinP/N76 - (VinP/N76 - VinP/N88)*(11R/12R)

Grayscale voltage (NW/NB)	Formula
V88/V167	VinP/N88
V89/V166	VinP/N88- (VinP/N88 - VinP/N100)*(1R/12R)
V90/V165	VinP/N88- (VinP/N88 - VinP/N100)*(2R/12R)
V91/V164	VinP/N88- (VinP/N88 - VinP/N100)*(3R/12R)
V92/V163	VinP/N88- (VinP/N88 - VinP/N100)*(4R/12R)
V93/V162	VinP/N88- (VinP/N88 - VinP/N100)*(5R/12R)
V94/V161	VinP/N88- (VinP/N88 - VinP/N100)*(6R/12R)
V95/V160	VinP/N88- (VinP/N88 - VinP/N100)*(7R/12R)
V96/V159	VinP/N88- (VinP/N88 - VinP/N100)*(8R/12R)
V97/V158	VinP/N88- (VinP/N88 - VinP/N100)*(9R/12R)
V98/V157	VinP/N88- (VinP/N88 - VinP/N100)*(10R/12R)
V99/V156	VinP/N88- (VinP/N88 - VinP/N100)*(11R/12R)
V100/V155	VinP/N100
V101/V154	VinP/N100- (VinP/N100 - VinP/N112)*(1R/12R)
V102/V153	VinP/N100- (VinP/N100 - VinP/N112)*(2R/12R)
V103/V152	VinP/N100- (VinP/N100 - VinP/N112)*(3R/12R)
V104/V151	VinP/N100- (VinP/N100 - VinP/N112)*(4R/12R)
V105/V150	VinP/N100- (VinP/N100 - VinP/N112)*(5R/12R)
V106/V149	VinP/N100- (VinP/N100 - VinP/N112)*(6R/12R)
V107/V148	VinP/N100- (VinP/N100 - VinP/N112)*(7R/12R)
V108/V147	VinP/N100- (VinP/N100 - VinP/N112)*(8R/12R)
V109/V146	VinP/N100- (VinP/N100 - VinP/N112)*(9R/12R)
V110/V145	VinP/N100- (VinP/N100 - VinP/N112)*(10R/12R)
V111/V144	VinP/N100- (VinP/N100 - VinP/N112)*(11R/12R)
V112/V143	VinP/N112
V113/V142	VinP/N112- (VinP/N112 - VinP/N128)*(1R/16R)
V114/V141	VinP/N112- (VinP/N112 - VinP/N128)*(2R/16R)
V115/V140	VinP/N112- (VinP/N112 - VinP/N128)*(3R/16R)
V116/V139	VinP/N112- (VinP/N112 - VinP/N128)*(4R/16R)
V117/V138	VinP/N112- (VinP/N112 - VinP/N128)*(5R/16R)
V118/V137	VinP/N112- (VinP/N112 - VinP/N128)*(6R/16R)
V119/V136	VinP/N112- (VinP/N112 - VinP/N128)*(7R/16R)
V120/V135	VinP/N112- (VinP/N112 - VinP/N128)*(8R/16R)
V121/V134	VinP/N112- (VinP/N112 - VinP/N128)*(9R/16R)
V122/V133	VinP/N112- (VinP/N112 - VinP/N128)*(10R/16R)
V123/V132	VinP/N112- (VinP/N112 - VinP/N128)*(11R/16R)
V124/V131	VinP/N112- (VinP/N112 - VinP/N128)*(12R/16R)
V125/V130	VinP/N112- (VinP/N112 - VinP/N128)*(13R/16R)
V126/V129	VinP/N112- (VinP/N112 - VinP/N128)*(14R/16R)
V127/V128	VinP/N112- (VinP/N112 - VinP/N128)*(15R/16R)
V128/V127	VinP/N128
V129/V126	VinP/N128- (VinP/N128 - VinP/N144)*(1R/16R)
V130/V125	VinP/N128- (VinP/N128 - VinP/N144)*(2R/16R)
V131/V124	VinP/N128- (VinP/N128 - VinP/N144)*(3R/16R)

Grayscale voltage (NW/NB)	Formula
V132/V123	VinP/N128- (VinP/N128 - VinP/N144)*(4R/16R)
V133/V122	VinP/N128- (VinP/N128 - VinP/N144)*(5R/16R)
V134/V121	VinP/N128- (VinP/N128 - VinP/N144)*(6R/16R)
V135/V120	VinP/N128- (VinP/N128 - VinP/N144)*(7R/16R)
V136/V119	VinP/N128- (VinP/N128 - VinP/N144)*(8R/16R)
V137/V118	VinP/N128- (VinP/N128 - VinP/N144)*(9R/16R)
V138/V117	VinP/N128- (VinP/N128 - VinP/N144)*(10R/16R)
V139/V116	VinP/N128- (VinP/N128 - VinP/N144)*(11R/16R)
V140/V115	VinP/N128- (VinP/N128 - VinP/N144)*(12R/16R)
V141/V114	VinP/N128- (VinP/N128 - VinP/N144)*(13R/16R)
V142/V113	VinP/N128- (VinP/N128 - VinP/N144)*(14R/16R)
V143/V112	VinP/N128- (VinP/N128 - VinP/N144)*(15R/16R)
V144/V111	VinP/N144
V145/V110	VinP/N144 - (VinP/N144 - VinP/N156)*(1R/12R)
V146/V109	VinP/N144 - (VinP/N144 - VinP/N156)*(2R/12R)
V147/V108	VinP/N144 - (VinP/N144 - VinP/N156)*(3R/12R)
V148/V107	VinP/N144 - (VinP/N144 - VinP/N156)*(4R/12R)
V149/V106	VinP/N144 - (VinP/N144 - VinP/N156)*(5R/12R)
V150/V105	VinP/N144 - (VinP/N144 - VinP/N156)*(6R/12R)
V151/V104	VinP/N144 - (VinP/N144 - VinP/N156)*(7R/12R)
V152/V103	VinP/N144 - (VinP/N144 - VinP/N156)*(8R/12R)
V153/V102	VinP/N144 - (VinP/N144 - VinP/N156)*(9R/12R)
V154/V101	VinP/N144 - (VinP/N144 - VinP/N156)*(10R/12R)
V155/V100	VinP/N144 - (VinP/N144 - VinP/N156)*(11R/12R)
V156/V99	VinP/N156
V157/V98	VinP/156 - (VinP/N156 - VinP/N168)*(1R/12R)
V158/V97	VinP/156 - (VinP/N156 - VinP/N168)*(2R/12R)
V159/V96	VinP/156 - (VinP/N156 - VinP/N168)*(3R/12R)
V160/V95	VinP/156 - (VinP/N156 - VinP/N168)*(4R/12R)
V161/V94	VinP/156 - (VinP/N156 - VinP/N168)*(5R/12R)
V162/V93	VinP/156 - (VinP/N156 - VinP/N168)*(6R/12R)
V163/V92	VinP/156 - (VinP/N156 - VinP/N168)*(7R/12R)
V164/V91	VinP/156 - (VinP/N156 - VinP/N168)*(8R/12R)
V165/V90	VinP/156 - (VinP/N156 - VinP/N168)*(9R/12R)
V166/V89	VinP/156 - (VinP/N156 - VinP/N168)*(10R/12R)
V167/V88	VinP/156 - (VinP/N156 - VinP/N168)*(11R/12R)
V168/V87	VinP/N168
V169/V86	VinP/168 - (VinP/N168 - VinP/N180)*(1R/12R)
V170/V85	VinP/168 - (VinP/N168 - VinP/N180)*(2R/12R)
V171/V84	VinP/168 - (VinP/N168 - VinP/N180)*(3R/12R)
V172/V83	VinP/168 - (VinP/N168 - VinP/N180)*(4R/12R)
V173/V82	VinP/168 - (VinP/N168 - VinP/N180)*(5R/12R)
V174/V81	VinP/168 - (VinP/N168 - VinP/N180)*(6R/12R)
V175/V80	VinP/168 - (VinP/N168 - VinP/N180)*(7R/12R)

Grayscale voltage (NW/NB)	Formula	Grayscale voltage (NW/NB)	Formula
V176/V79	$VinP/168 - (VinP/N168 - VinP/N180) \cdot (8R/12R)$	V216/V39	VinP/N216
V177/V78	$VinP/168 - (VinP/N168 - VinP/N180) \cdot (9R/12R)$	V217/V38	$VinP/N216 - (VinP/N216 - VinP/N228) \cdot (1R/12R)$
V178/V77	$VinP/168 - (VinP/N168 - VinP/N180) \cdot (10R/12R)$	V218/V37	$VinP/N216 - (VinP/N216 - VinP/N228) \cdot (2R/12R)$
V179/V76	$VinP/168 - (VinP/N168 - VinP/N180) \cdot (11R/12R)$	V219/V36	$VinP/N216 - (VinP/N216 - VinP/N228) \cdot (3R/12R)$
V180/V75	VinP/N180	V220/V35	$VinP/N216 - (VinP/N216 - VinP/N228) \cdot (4R/12R)$
V181/V74	$VinP/N180 - (VinP/N180 - VinP/N192) \cdot (1R/12R)$	V221/V34	$VinP/N216 - (VinP/N216 - VinP/N228) \cdot (5R/12R)$
V182/V73	$VinP/N180 - (VinP/N180 - VinP/N192) \cdot (2R/12R)$	V222/V33	$VinP/N216 - (VinP/N216 - VinP/N228) \cdot (6R/12R)$
V183/V72	$VinP/N180 - (VinP/N180 - VinP/N192) \cdot (3R/12R)$	V223/V32	$VinP/N216 - (VinP/N216 - VinP/N228) \cdot (7R/12R)$
V184/V71	$VinP/N180 - (VinP/N180 - VinP/N192) \cdot (4R/12R)$	V224/V31	$VinP/N216 - (VinP/N216 - VinP/N228) \cdot (8R/12R)$
V185/V70	$VinP/N180 - (VinP/N180 - VinP/N192) \cdot (5R/12R)$	V225/V30	$VinP/N216 - (VinP/N216 - VinP/N228) \cdot (9R/12R)$
V186/V69	$VinP/N180 - (VinP/N180 - VinP/N192) \cdot (6R/12R)$	V226/V29	$VinP/N216 - (VinP/N216 - VinP/N228) \cdot (10R/12R)$
V187/V68	$VinP/N180 - (VinP/N180 - VinP/N192) \cdot (7R/12R)$	V227/V28	$VinP/N216 - (VinP/N216 - VinP/N228) \cdot (11R/12R)$
V188/V67	$VinP/N180 - (VinP/N180 - VinP/N192) \cdot (8R/12R)$	V228/V27	VinP/N228
V189/V66	$VinP/N180 - (VinP/N180 - VinP/N192) \cdot (9R/12R)$	V229/V26	$VinP/N228 - (VinP/N228 - VinP/N236) \cdot (1R/8R)$
V190/V65	$VinP/N180 - (VinP/N180 - VinP/N192) \cdot (10R/12R)$	V230/V25	$VinP/N228 - (VinP/N228 - VinP/N236) \cdot (2R/8R)$
V191/V64	$VinP/N180 - (VinP/N180 - VinP/N192) \cdot (11R/12R)$	V231/V24	$VinP/N228 - (VinP/N228 - VinP/N236) \cdot (3R/8R)$
V192/V63	VinP/N192	V232/V23	$VinP/N228 - (VinP/N228 - VinP/N236) \cdot (4R/8R)$
V193/V62	$VinP/N192 - (VinP/N192 - VinP/N204) \cdot (1R/12R)$	V233/V22	$VinP/N228 - (VinP/N228 - VinP/N236) \cdot (5R/8R)$
V194/V61	$VinP/N192 - (VinP/N192 - VinP/N204) \cdot (2R/12R)$	V234/V21	$VinP/N228 - (VinP/N228 - VinP/N236) \cdot (6R/8R)$
V195/V60	$VinP/N192 - (VinP/N192 - VinP/N204) \cdot (3R/12R)$	V235/V20	$VinP/N228 - (VinP/N228 - VinP/N236) \cdot (7R/8R)$
V196/V59	$VinP/N192 - (VinP/N192 - VinP/N204) \cdot (4R/12R)$	V236/V19	VinP/N236
V197/V58	$VinP/N192 - (VinP/N192 - VinP/N204) \cdot (5R/12R)$	V237/V18	$VinP/N236 - (VinP/N236 - VinP/N243) \cdot (1R/7R)$
V198/V57	$VinP/N192 - (VinP/N192 - VinP/N204) \cdot (6R/12R)$	V238/V17	$VinP/N236 - (VinP/N236 - VinP/N243) \cdot (2R/7R)$
V199/V56	$VinP/N192 - (VinP/N192 - VinP/N204) \cdot (7R/12R)$	V239/V16	$VinP/N236 - (VinP/N236 - VinP/N243) \cdot (3R/7R)$
V200/V55	$VinP/N192 - (VinP/N192 - VinP/N204) \cdot (8R/12R)$	V240/V15	$VinP/N236 - (VinP/N236 - VinP/N243) \cdot (4R/7R)$
V201/V54	$VinP/N192 - (VinP/N192 - VinP/N204) \cdot (9R/12R)$	V241/V14	$VinP/N236 - (VinP/N236 - VinP/N243) \cdot (5R/7R)$
V202/V53	$VinP/N192 - (VinP/N192 - VinP/N204) \cdot (10R/12R)$	V242/V13	$VinP/N236 - (VinP/N236 - VinP/N243) \cdot (6R/7R)$
V203/V52	$VinP/N192 - (VinP/N192 - VinP/N204) \cdot (11R/12R)$	V243/V12	VinP/N243
V204/V51	VinP/N204	V244/V11	$VinP/N243 - (VinP/N243 - VinP/N247) \cdot (R/4R)$
V205/V50	$VinP/N204 - (VinP/N204 - VinP/N216) \cdot (1R/12R)$	V245/V10	$VinP/N243 - (VinP/N243 - VinP/N247) \cdot (2R/4R)$
V206/V49	$VinP/N204 - (VinP/N204 - VinP/N216) \cdot (2R/12R)$	V246/V9	$VinP/N243 - (VinP/N243 - VinP/N247) \cdot (3R/4R)$
V207/V48	$VinP/N204 - (VinP/N204 - VinP/N216) \cdot (3R/12R)$	V247/V8	VinP/N247
V208/V47	$VinP/N204 - (VinP/N204 - VinP/N216) \cdot (4R/12R)$	V248/V7	$VinP/N247 - (VinP/N247 - VinP/N251) \cdot (R/4R)$
V209/V46	$VinP/N204 - (VinP/N204 - VinP/N216) \cdot (5R/12R)$	V249/V6	$VinP/N247 - (VinP/N247 - VinP/N251) \cdot (2R/4R)$
V210/V45	$VinP/N204 - (VinP/N204 - VinP/N216) \cdot (6R/12R)$	V250/V5	$VinP/N247 - (VinP/N247 - VinP/N251) \cdot (3R/4R)$
V211/V44	$VinP/N204 - (VinP/N204 - VinP/N216) \cdot (7R/12R)$	V251/V4	VinP/N251
V212/V43	$VinP/N204 - (VinP/N204 - VinP/N216) \cdot (8R/12R)$	V252/V3	$VinP/N251 - (VinP/N251 - VinP/N255) \cdot (R/4R)$
V213/V42	$VinP/N204 - (VinP/N204 - VinP/N216) \cdot (9R/12R)$	V253/V2	$VinP/N251 - (VinP/N251 - VinP/N255) \cdot (2R/4R)$
V214/V41	$VinP/N204 - (VinP/N204 - VinP/N216) \cdot (10R/12R)$	V254/V1	$VinP/N251 - (VinP/N251 - VinP/N255) \cdot (3R/4R)$
V215/V40	$VinP/N204 - (VinP/N204 - VinP/N216) \cdot (11R/12R)$	V255/V0	VinP/N255

Table 5.35: Voltage calculation formula of 256-grayscale voltage (positive/negative polarity)

5.8 Gray voltage generator for digital gamma correction

The HX8399-C digital gamma correction can reach the independent GAMMA curve of RGB. HX8399-C utilizes DGC_LUT (**Digital Gamma Correction Look Up Table**) to change input data from 8-bit into 10-bit and sends 10-bit data to Dithering circuit, and then drive Source Driver via Dithering circuit.

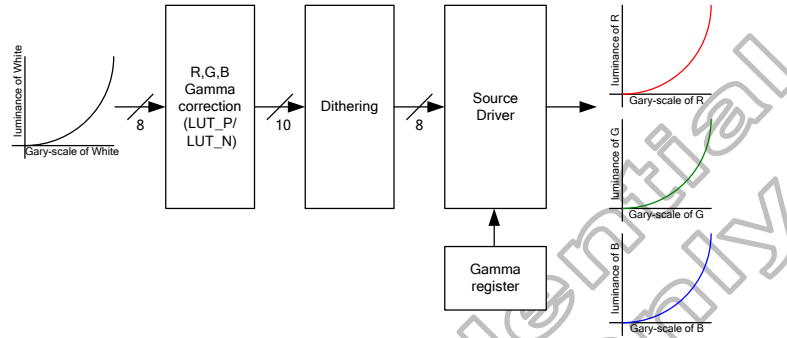


Figure 5.26: Block diagram of digital gamma correction

Himax Confidential
For Huawei Do Not Copy

There are 126 bytes DGC LUT to set R, G, B gamma independently. When DGC_EN=1, R, G, B gamma will mapping Gray level 0, 8, 16, ..., 240, 248, 255 voltage to the LUT register setting value of real gamma gray level voltage.

LUT	D7	D6	D5	D4	D3	D2	D1	D0	Default
1 st	R009	R008	R007	R006	R005	R004	R003	R002	-
2 nd	R019	R018	R017	R016	R015	R014	R013	R012	-
3 rd	R029	R028	R027	R026	R025	R024	R023	R022	-
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	-
32 nd	R319	R318	R317	R316	R315	R314	R313	R312	-
33 rd	R329	R328	R327	R326	R325	R324	R323	R322	-
34 th	R001	R000	R011	R010	R021	R020	R031	R030	-
35 th	R041	R040	R051	R050	R061	R060	R071	R070	-
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	-
41 st	R281	R280	R291	R290	R301	R300	R311	R310	-
42 nd	R321	R320	0	0	0	0	0	0	-
43 rd	G009	G008	G007	G006	G005	G004	G003	G002	-
44 th	G019	G018	G017	G016	G015	G014	G013	G012	-
45 th	G029	G028	G027	G026	G025	G024	G023	G022	-
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	-
74 th	G319	G318	G317	G316	G315	G314	G313	G312	-
75 th	G329	G328	G327	G326	G325	G324	G323	G322	-
76 th	G001	G000	G011	G010	G021	G020	G031	G030	-
77 th	G041	G040	G051	G050	G061	G060	G071	G070	-
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	-
83 rd	G281	G280	G291	G290	G301	G300	G311	G310	-
84 th	G321	G320	0	0	0	0	0	0	-
85 th	B009	B008	B007	B006	B005	B004	B003	B002	-
86 th	B019	B018	B017	B016	B015	B014	B013	B012	-
87 th	B029	B028	B027	B026	B025	B024	B023	B022	-
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	-
116 th	B319	B318	B317	B316	B315	B314	B313	B312	-
117 th	B329	B328	B327	B326	B325	B324	B323	B322	-
118 th	B001	B000	B011	B010	B021	B020	B031	B030	-
119 th	B041	B040	B051	B050	B061	B060	B071	B070	-
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	-
125 th	B281	B280	B291	B290	B301	B300	B311	B310	-
126 th	B321	B320	0	0	0	0	0	0	-

Table 5.36: DGC look-up table

5.9 Characteristics of I/O

5.9.1 Output or bi-directional (I/O) pins

Output or bi-directional pins	After power on	After hardware reset	After software reset
TE	Low	Low	Low
TE1	Low	Low	Low
SDO	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
CABC_PWM_OUT	Low	Low	Low

Table 5.37: Characteristics of output or bi-directional (I/O) pins

5.9.2 Input pins

Input pins	During power on process	After power on	After hardware reset	After software reset	During power off process
RESX	Input invalid	Input valid	Input valid	Input valid	Input invalid
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
DCX	Input invalid	Input valid	Input valid	Input valid	Input invalid
SCL	Input invalid	Input valid	Input valid	Input valid	Input invalid
DB7~DB0 SDI_SDA	Input invalid	Input valid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input valid	Input valid	Input invalid
VSYNC	Input invalid	Input valid	Input valid	Input valid	Input invalid
PCLK	Input invalid	Input valid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input valid	Input invalid
OSC, IM2, IM1, IM0,	Input invalid	Input valid	Input valid	Input valid	Input invalid
FRM	Low	Low	Low	Low	Low
TEST2, TEST1, TEST0	Low	Low	Low	Low	Low

Table 5.38: Characteristics of input pins

5.10 Sleep Out–command and self–diagnostic functions of the display module

5.10.1 Register loading detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (or similar device) to registers of the display controller is working properly. There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (=increased by 1). The flow chart for this internal function is as following:

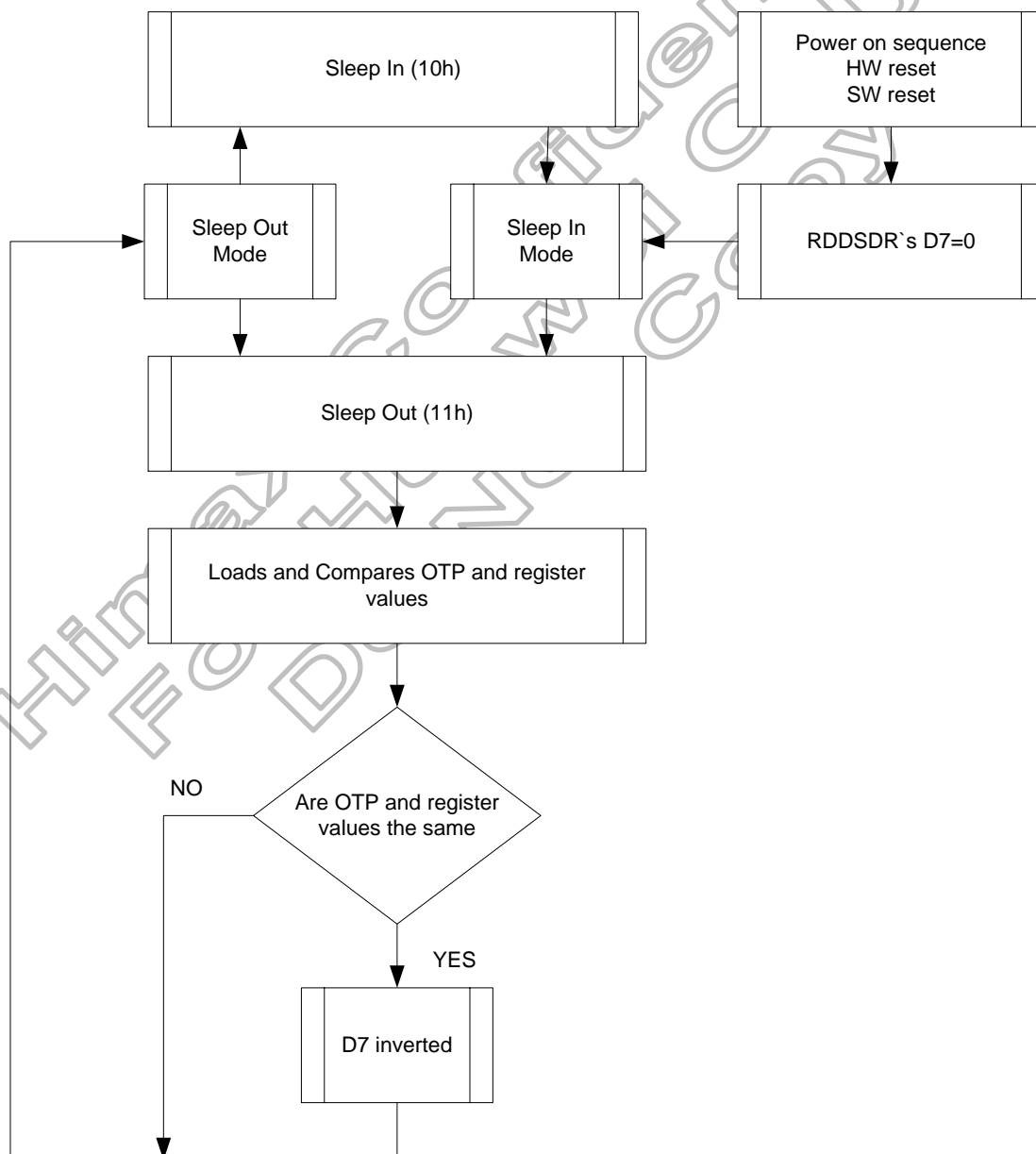
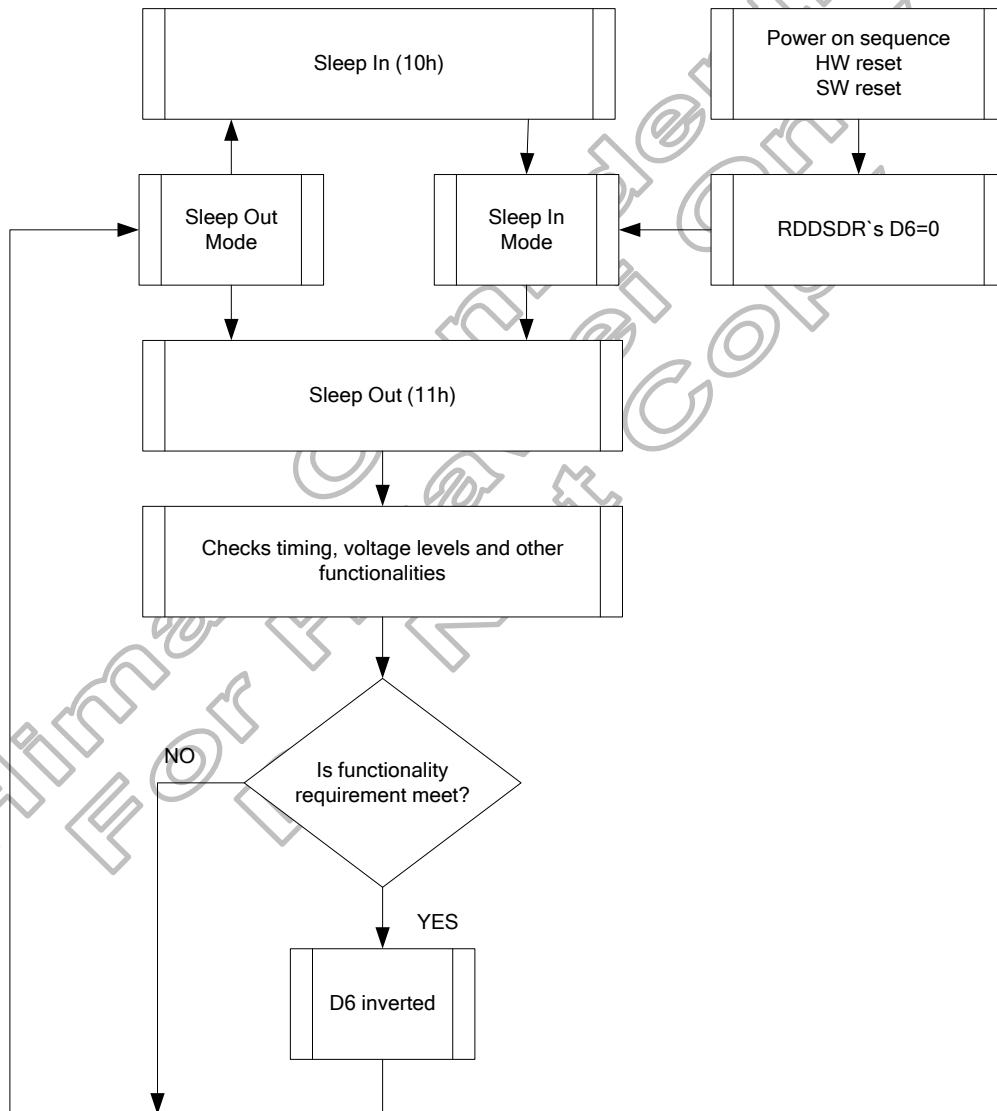


Figure 5.27: Sleep out flow chart–command and self-diagnostic functions

5.10.2 Functionality detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (=the display controller) is comparing, if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, 1 bit will be inverted (=increased by 1), which is defined in command “Read Display Self- Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (=increased by 1). The flow chart for this internal function is shown as below.



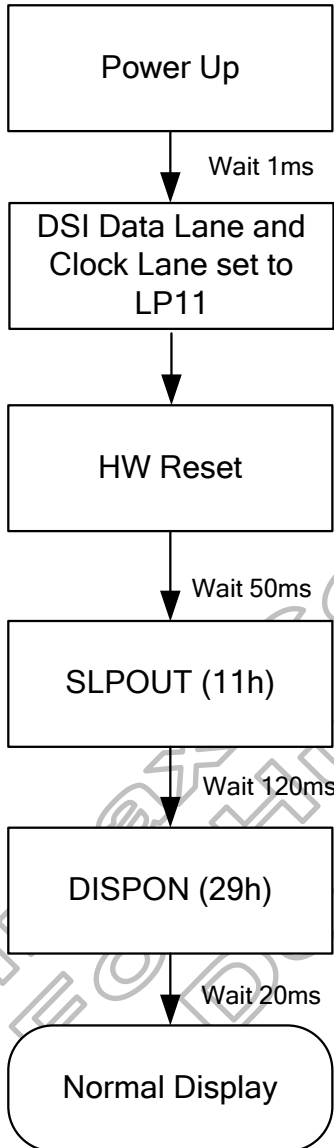
Note: (1) There is needed 120msec after Sleep Out -command, when there is changing from Sleep In-mode to Sleep Out -mode, before there is possible to check if Customer's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out -command is sent in Sleep Out -mode.

Figure 5.28: Sleep out flow chart internal function detection

5.11 Power on/off sequence

The Power supply On/Off, Sleep In/Out and Display On/Off sequence is illustrated below.

Power On Sequence



Power Off Sequence

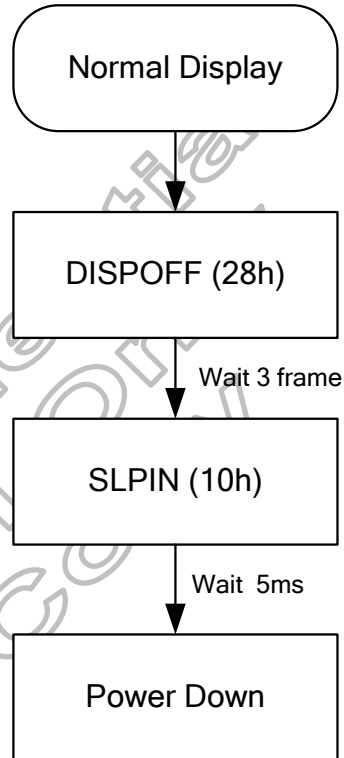


Figure 5.29: Power on/off sequence

5.11.1 VDD3/VDD1 input power (PCCS[2:0]=000, 001, 101)

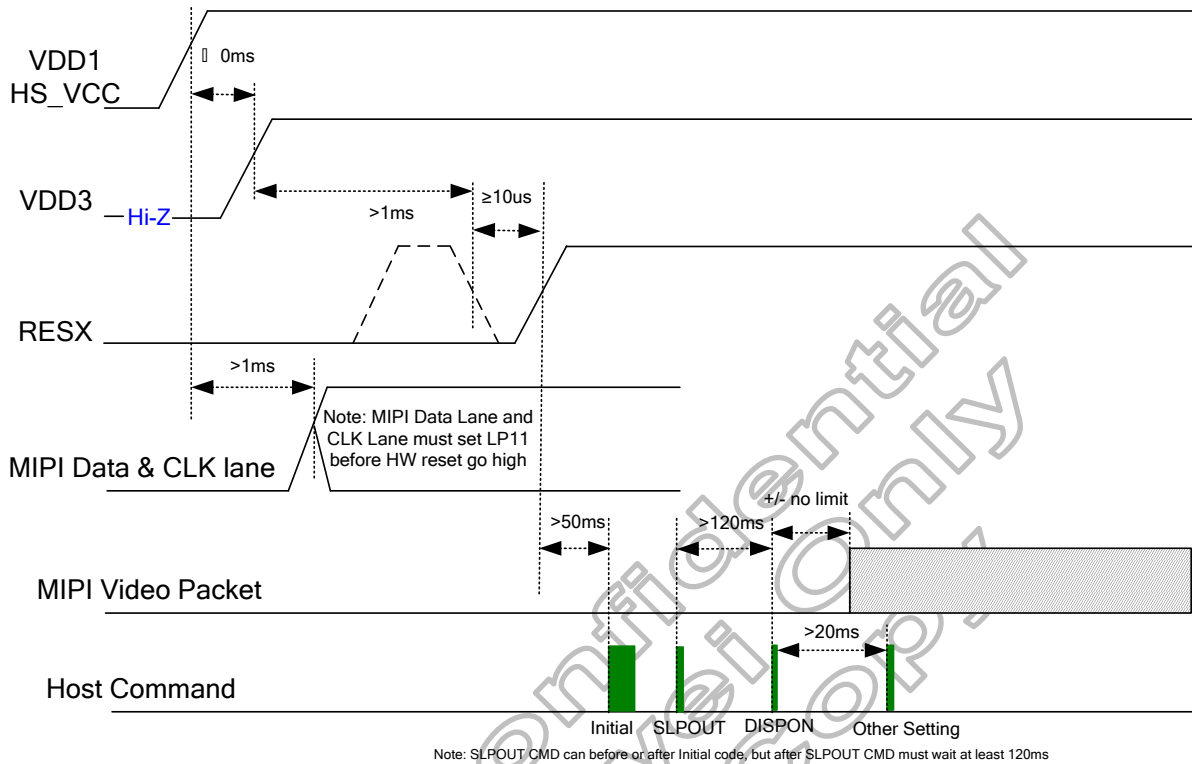


Figure 5.30: VDD3/VDD1 input power on sequence (PCCS[2:0]=000/001/101)

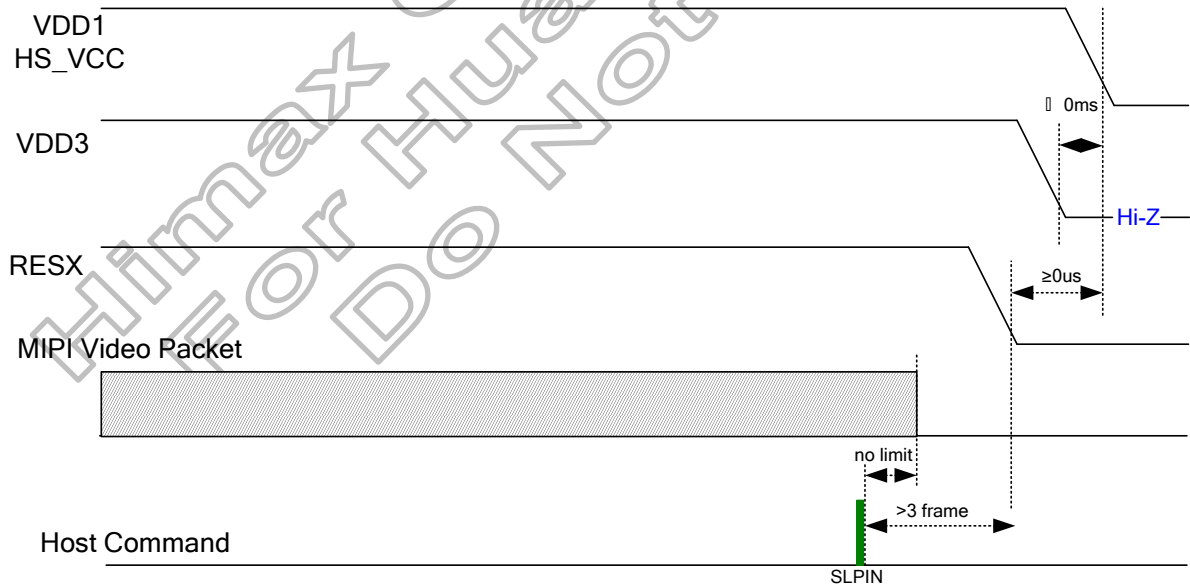


Figure 5.31: VDD3/VDD1 input power off sequence (PCCS[2:0] =000/001/101)

5.11.2 VSP/VDD1 input power (PCCS[2:0]=010)

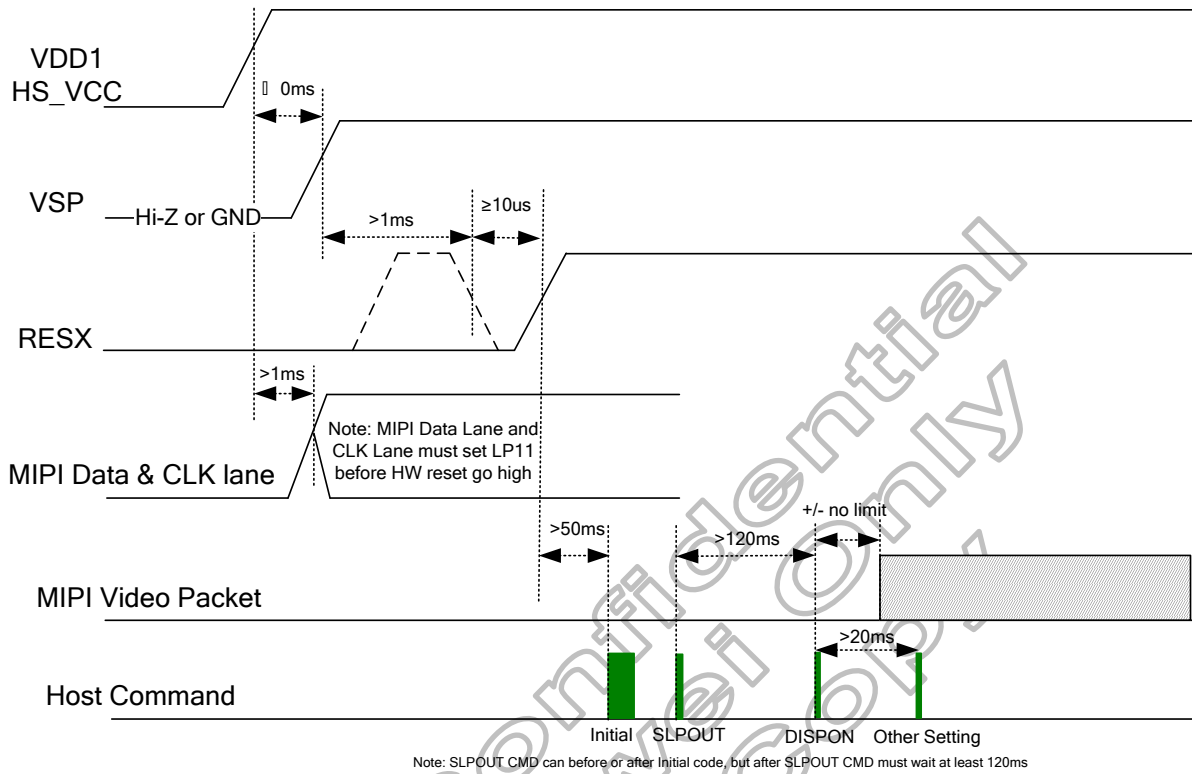


Figure 5.32: VSP/VDD1 input power on sequence (PCCS[2:0] =010)

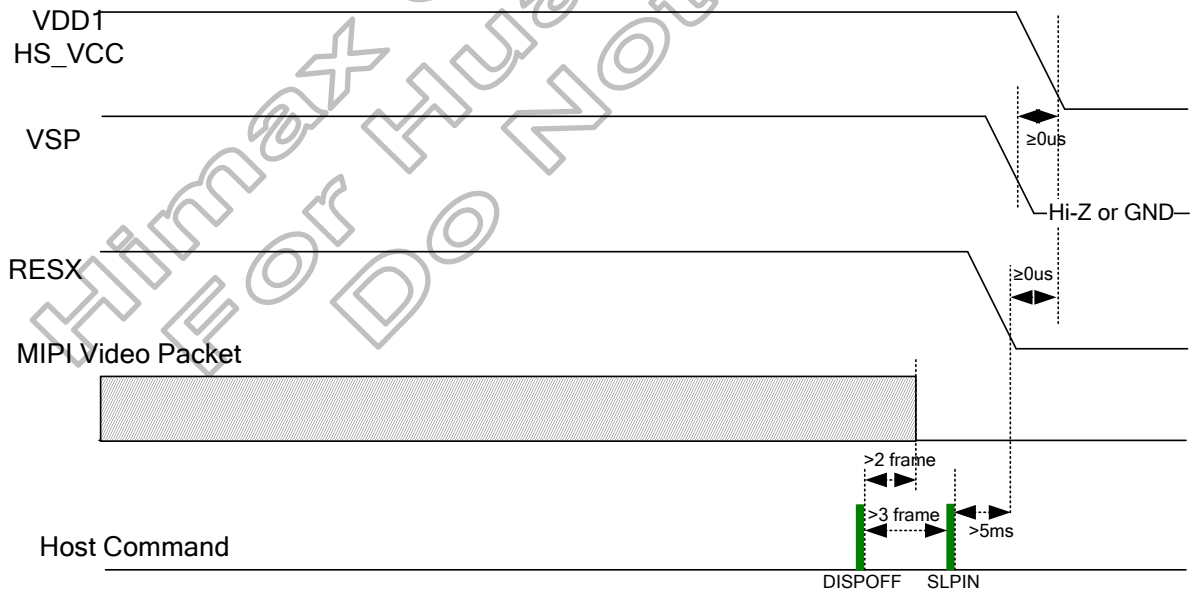


Figure 5.33: VSP/VDD1 input power off sequence (PCCS[2:0] =010)

5.11.3 VSP/VSN/VDD1 input power (PCCS[2:0]=011)

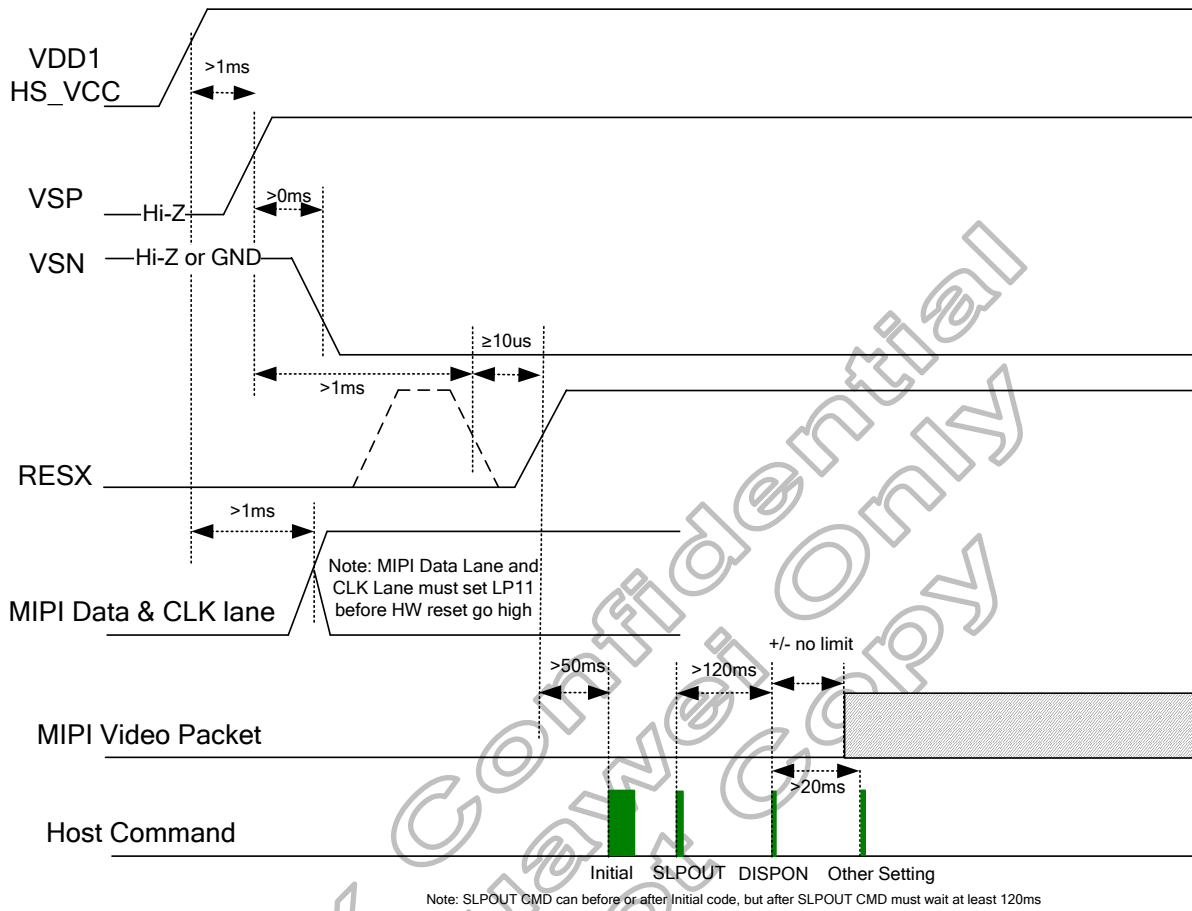


Figure 5.34: VSP/VSN/VDD1 input power on sequence (PCCS[2:0]=011)

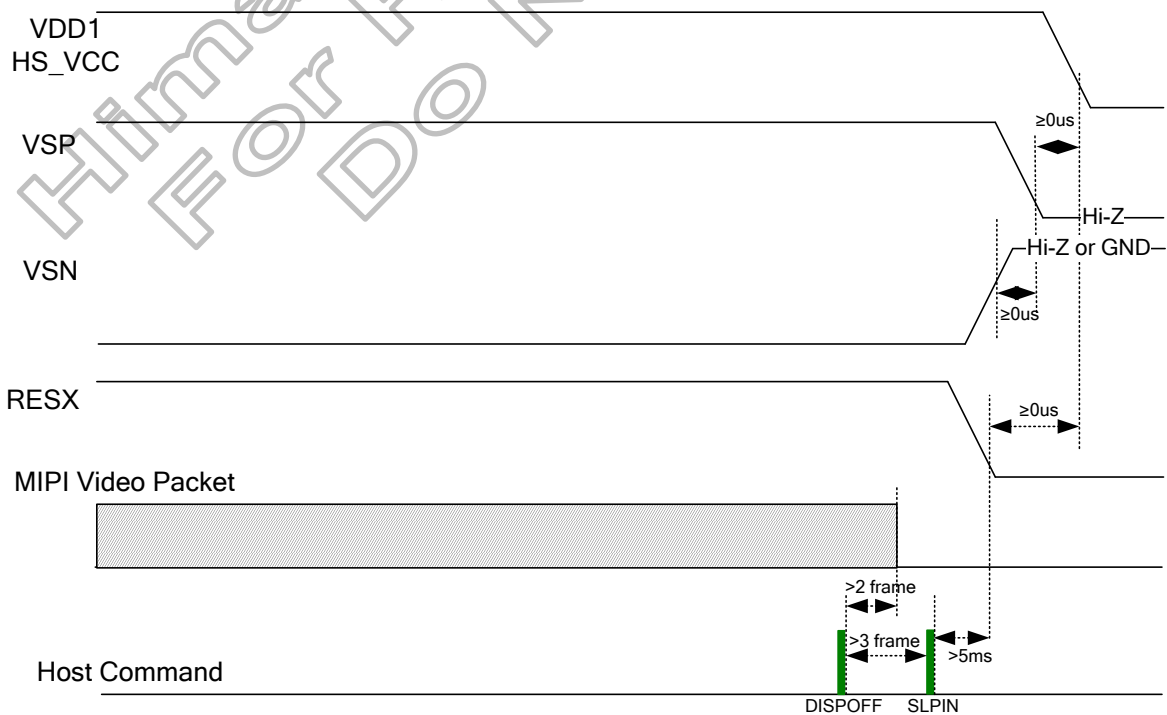


Figure 5.35: VSP/VSN/VDD1 input power off sequence (PCCS[2:0]=011)

5.11.4 VDD3/VSP/VSN/VDD1 input power (PCCS[2:0]=111)

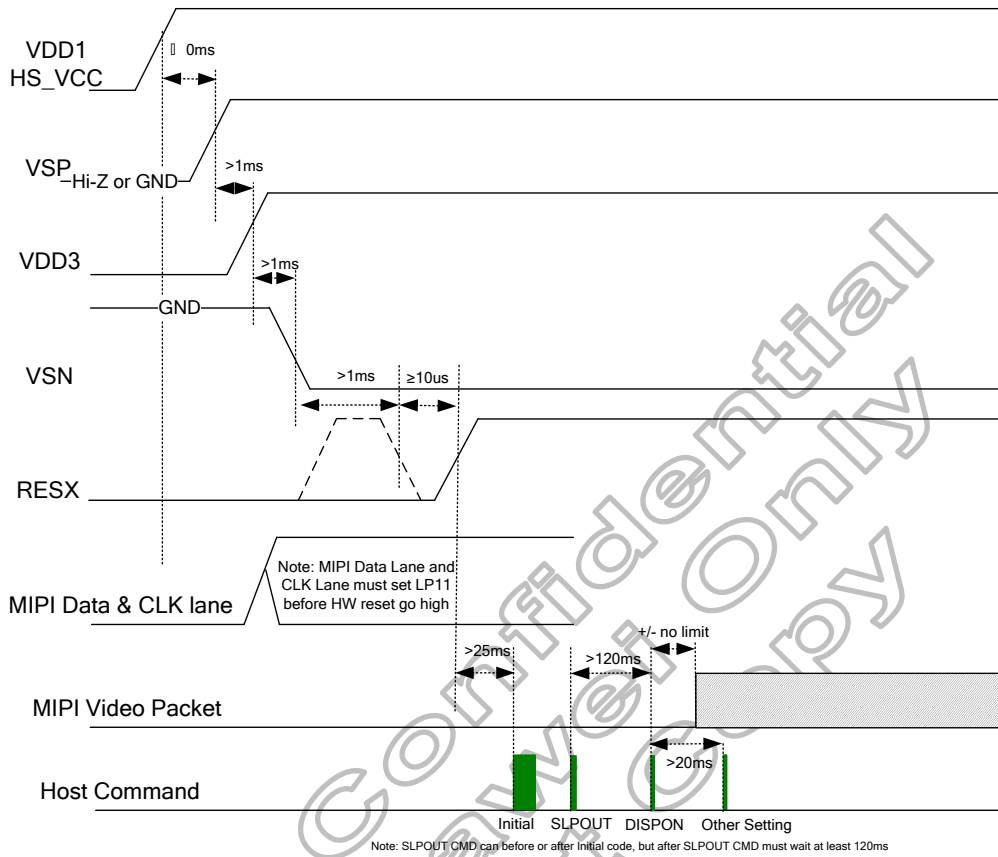


Figure 5.36: VDD3/VSP/VSN/VDD1 input power on sequence (PCCS[2:0]=111)

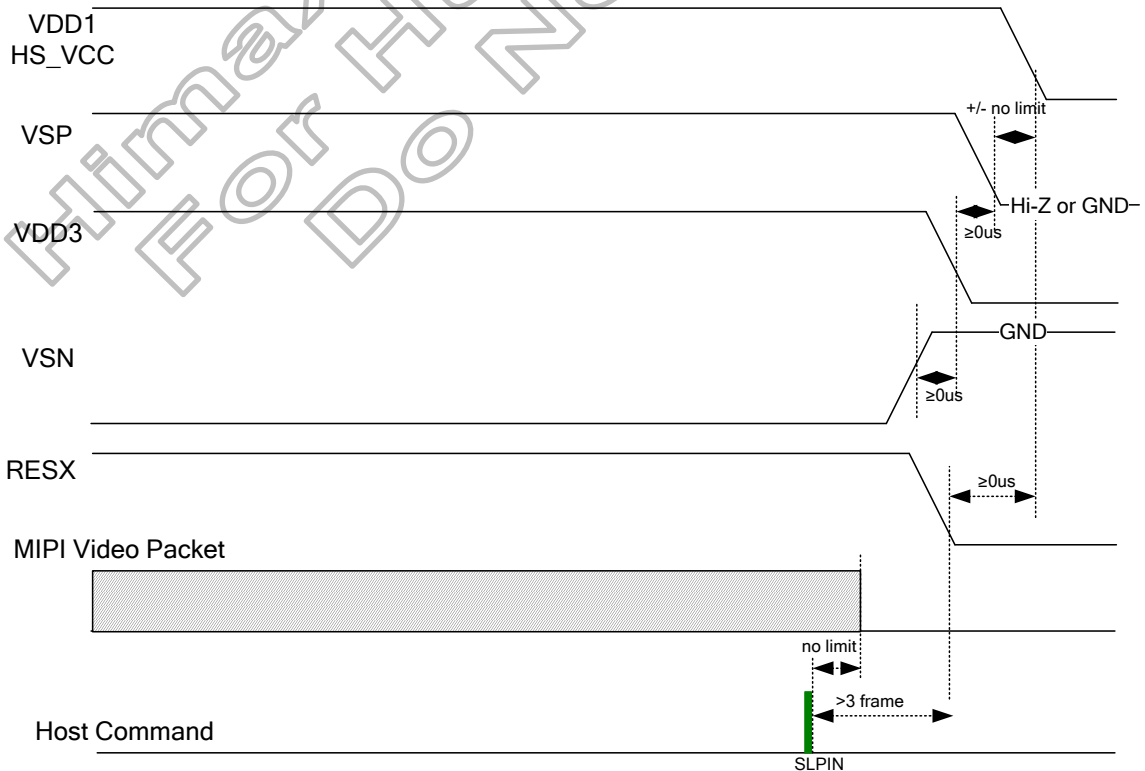


Figure 5.37: VDD3/VSP/VSN/VDD1 input power off sequence

5.11.5 VSP/VSN/VGH/VGL/VDD1 input power (PCCS[2:0]=100)

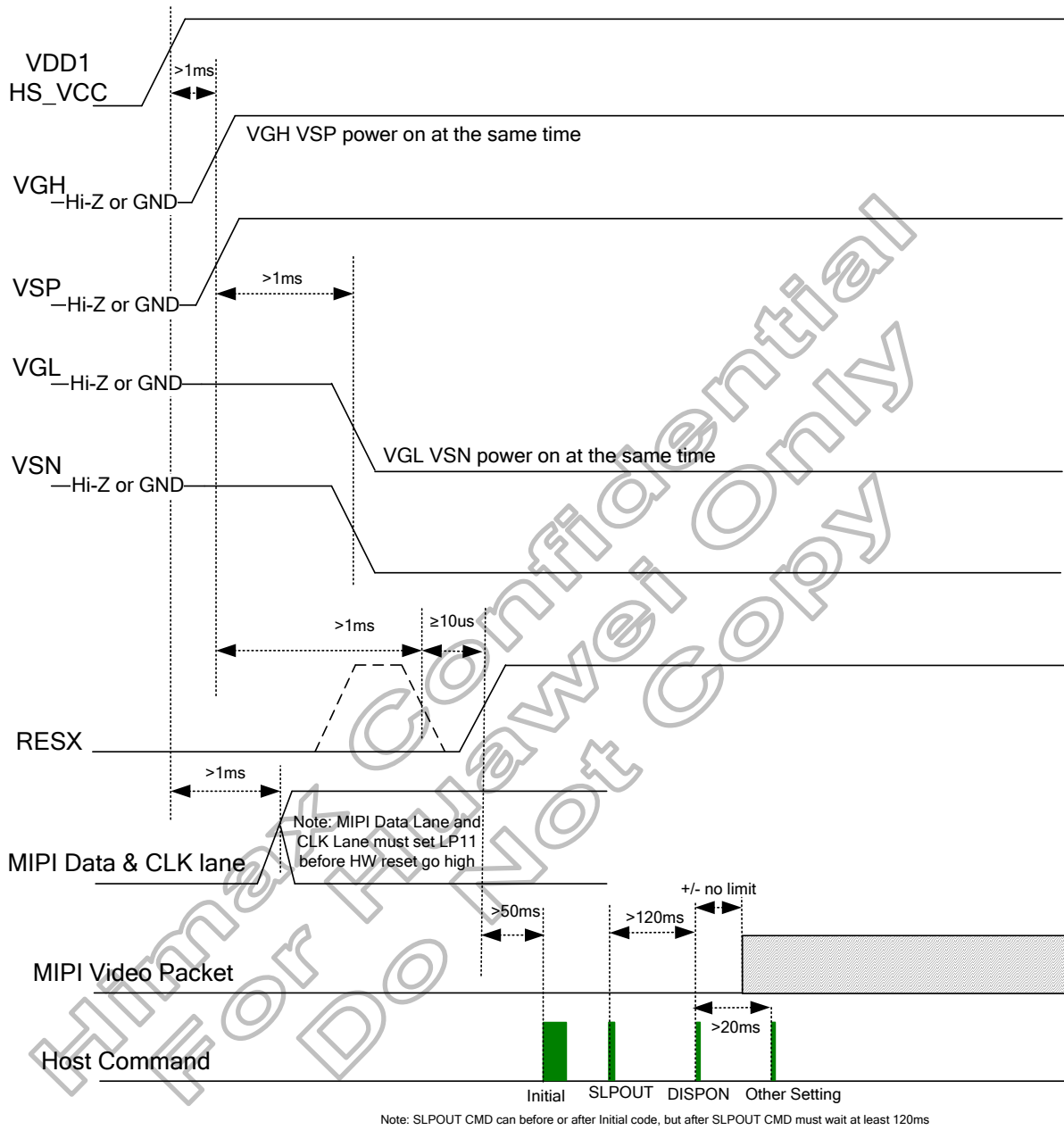


Figure 5.38: VSP/VSN/VGH/VGL/VDD1 input power on sequence

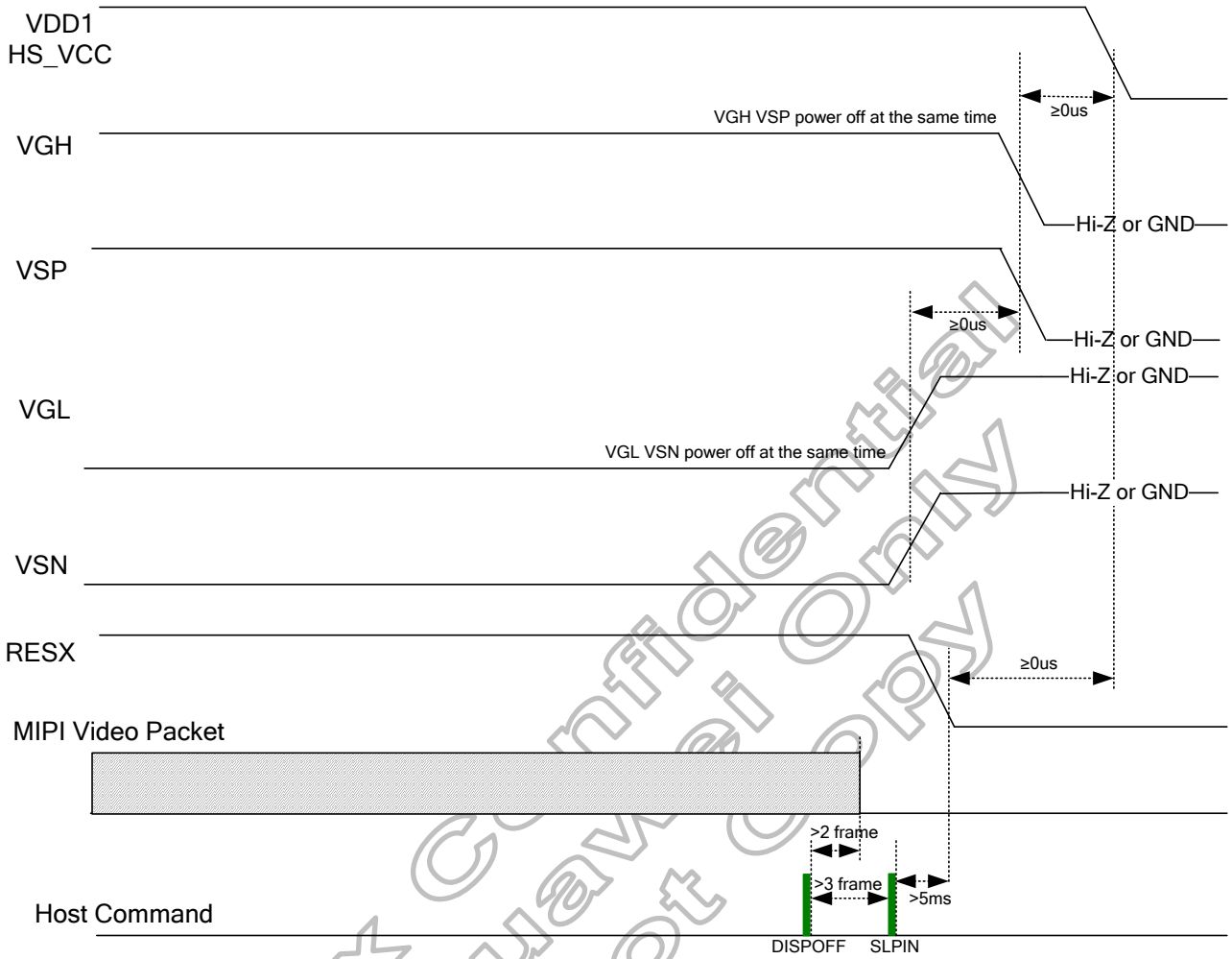
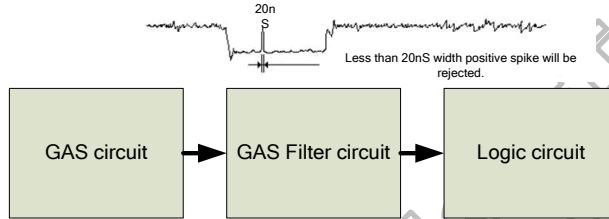


Figure 5.39: VSP/VSX/VGH/VGL/VDD1 input power off sequence

5.12 Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (**blank display**) and remains blank until “Power on Sequence” powers it up.

Note: (1) HX8399-C is support the noise reject filter (**20ns**) to reject spike or noise.



Himax Confidential
For Huawei Only
Do Not Copy

5.13 Content adaptive brightness control (CABC) function

The general block diagram of the CABC and the brightness control is illustrated below:

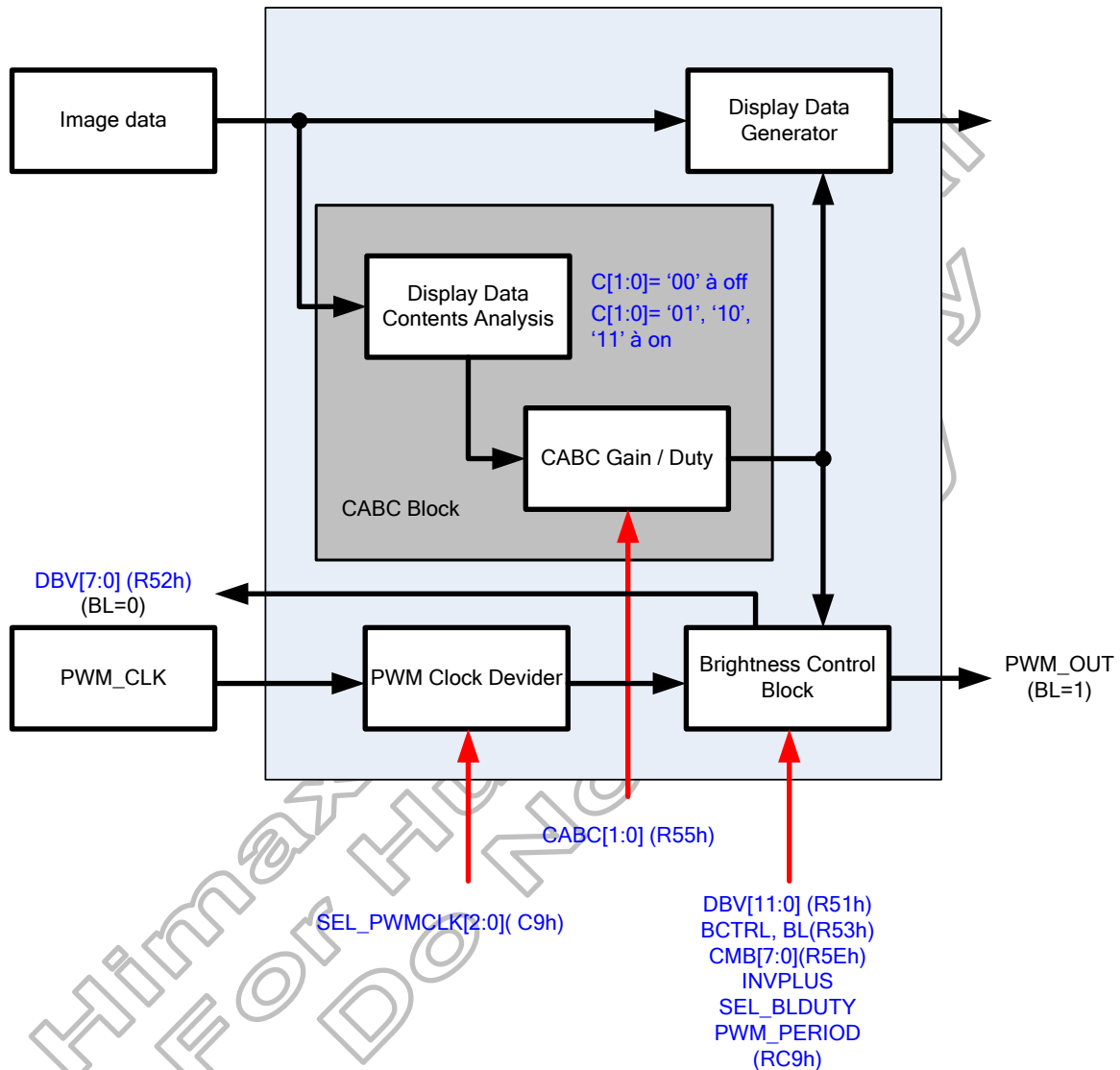
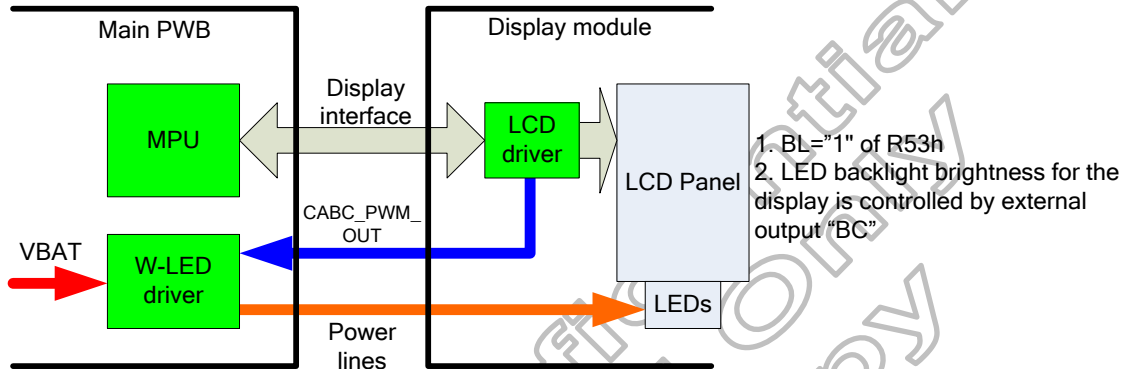


Figure 5.40: CABC block diagram

5.13.1 Module architectures

HX8399-C can support two module architectures for CABC operation. The BL bit setting of R53h can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

• Architecture I



• Architecture II

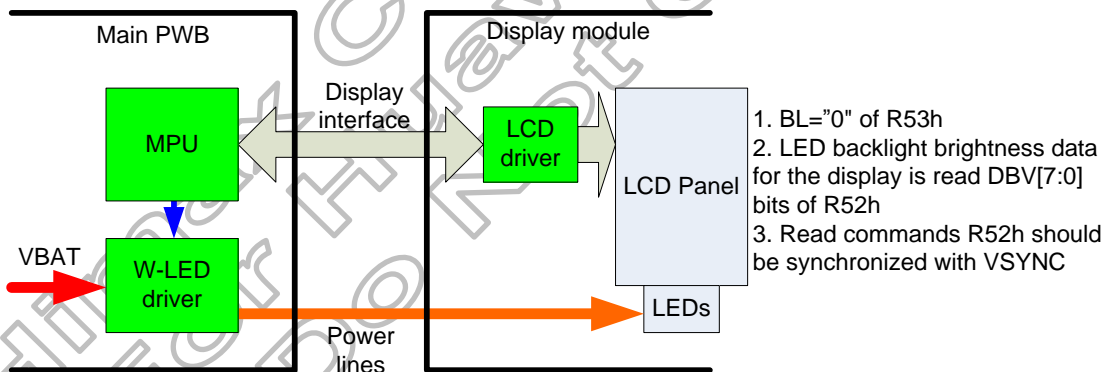


Figure 5.41: Module architecture

5.13.2 Brightness control block

There is an external output signal from brightness block, CABC_PWM_OUT, to control the LED driver IC in order to control display brightness.

There are register bits, DBV[11:0] of R51h, for display brightness of manual brightness setting. The CABC_PWM_OUT duty is calculated as $(DBV[11:0])/4095 \times \text{CABC duty (generated after one-frame display data content analysis)}$.

For ex: CABC_PWM_OUT period=2.95 ms, and DBV[11:0] (R51h)='2048DEC' and CABC duty is 74%. Then CABC_PWM_OUT duty= $(2048) / 4095 \times 74.42\% \approx 37.22\%$. Correspond to the CABC_PWM_OUT period=2.95 ms, the high-level of CABC_PWM_OUT (high effective)=1.10ms, and the low-level of CABC_PWM_OUT =1.85ms.

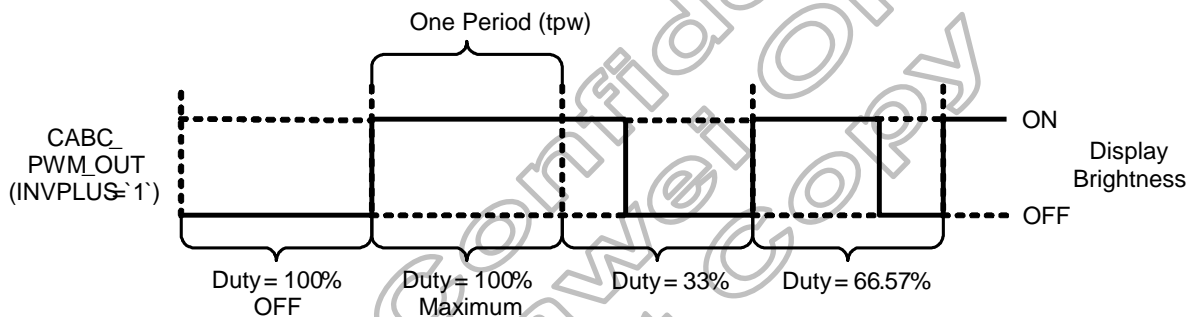


Figure 5.42: CABC_PWM_OUT output duty

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Pulse width	tpw	0.0333	-	8.33	ms

Note: (1) The signal rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.
 (2) The pulse width range by setting CABC related registers is located between 0.0333ms to 8.33ms.

Table 5.39: CABC timing table

When Architecture II module is used (BL='0') with the example below, the CABC_PWM_OUT is always output low and the DBV[11:0] (R51h) will be read a value as 1084DEC ($(1084)/4095 \approx 26.47\%$).

5.13.3 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting (**CMB[7:0] bits of R5Eh**) is to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (**BCTRL='0'** of **R53h**), CABC minimum brightness setting is ignored. "**CMB[7:0]**, Read CABC minimum brightness (**R5Fh**) "always read the setting value of "**CMB[7:0]**, Write CABC minimum brightness (**R5Eh**)"

Himax Confidential
For Huawei Only
Do Not Copy

5.14 FRM (Free running mode)

Burn-in of TFT displays consists of driving each module for 10hr at a temperature of 60°C. In order to drive the modules, it requires extra electronics. To reduce the burn-in cost, it is requested that the driver IC will generate the required display image without requiring extra electronics. We term this a free running mode (FRM). For burn-in, it is sufficient that the display is powered up with a plane saturated black or white pattern. The Display pattern sequence and power on sequence is as below Figure.

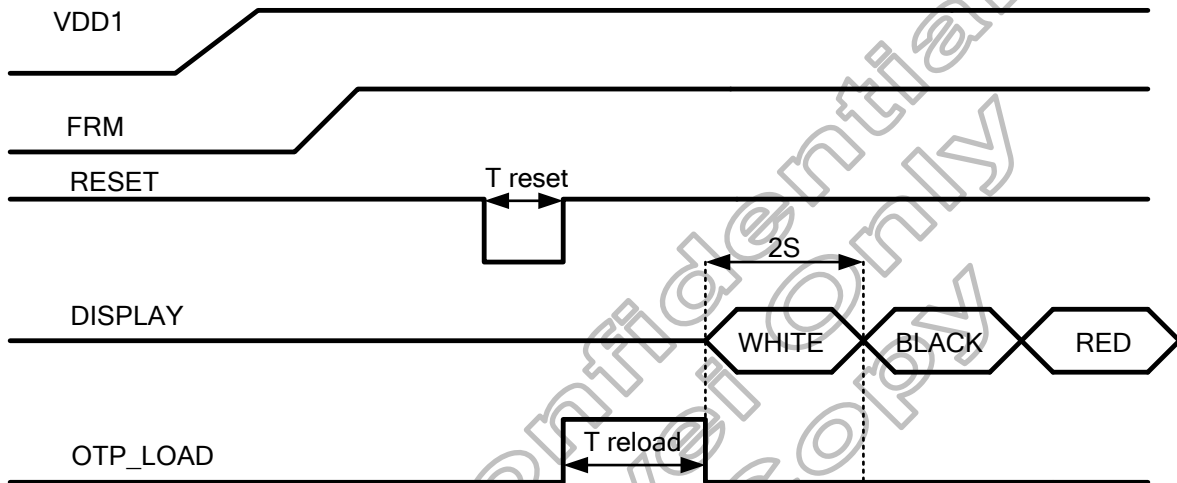


Figure 5.43: FRM power on sequence

5.15 OTP programming

5.15.1 OTP table

OTP_INDEX (HEX)	B7	B6	B5	B4	B3	B2	B1	B0
0	ID1_1[7:0]							
1	ID2_1[7:0]							
2	ID3_1[7:0]							
3	ID4_1[7:0]							
4	ID1_2[7:0]							
5	ID2_2[7:0]							
6	ID3_2[7:0]							
7	ID4_2[7:0]							
8	ID1_3[7:0]							
9	ID2_3[7:0]							
A	ID3_3[7:0]							
B	ID4_3[7:0]							
C	NVALID_ID1	NVALID_ID2	NVALID_ID3	-	-	-	-	-
D	VCMC_F1[7:0]							
E	VCMC_B1[7:0]							
F	VCMC_F2[7:0]							
10	VCMC_B2[7:0]							
11	VCMC_F3[7:0]							
12	VCMC_B3[7:0]							
13	-	-	VCMC_B38	VCMC_B38	VCMC_B28	VCMC_B28	VCMC_B18	VCMC_B18
14	NVALID_VC MC1	NVALID_VC MC2	NVALID_VC MC3	-	-	-	-	-
15	NVALID_PANEL	-	-	-	SS_PANEL	GS_PANEL	REV_PANE	BGR_PANEL
45	NVALID_GAMMA	VHP_0[6:0]						
46	-	VHP_1[6:0]						
47	-	VHP_2[6:0]						
48	-	VHP_3[6:0]						
49	VMP_0[7:0]							
4A	VMP_1[7:0]							
4B	VMP_2[7:0]							
4C	VMP_3[7:0]							
4D	VMP_4[7:0]							
4E	VMP_5[7:0]							
4F	VMP_6[7:0]							
50	VMP_7[7:0]							
51	VMP_8[7:0]							
52	VMP_9[7:0]							
53	VMP_10[7:0]							
54	VMP_11[7:0]							
55	VMP_12[7:0]							
56	VMP_13[7:0]							
57	VMP_14[7:0]							
58	VMP_15[7:0]							
59	VMP_16[7:0]							
5A	VMP_17[7:0]							
5B	VMP_18[7:0]							
5C	-	VLP_0[6:0]						
5D	-	VLP_1[6:0]						
5E	-	VLP_2[6:0]						
5F	-	VLP_3[6:0]						
60	-	VHN_0[6:0]						
61	-	VHN_1[6:0]						
62	-	VHN_2[6:0]						
63	-	VHN_3[6:0]						
64	VMN_0[7:0]							
65	VMN_1[7:0]							
66	VMN_21[7:0]							

67	VMN_3[7:0]							
68	VMN_4[7:0]							
69	VMN_5[7:0]							
6A	VMN_6[7:0]							
6B	VMN_7[7:0]							
6C	VMN_8[7:0]							
6D	VMN_9[7:0]							
6E	VMN_10[7:0]							
6F	VMN_11[7:0]							
70	VMN_12[7:0]							
71	VMN_13[7:0]							
72	VMN_14[7:0]							
73	VMN_15[7:0]							
74	VMN_16[7:0]							
75	VMN_17[7:0]							
76	VMN_18[7:0]							
77	-	VLN_0[6:0]						
78	-	VLN_1[6:0]						
79	-	VLN_2[6:0]						
7A	-	VLN_3[6:0]						
7F	NVALID_DG C	-	-	DGC_PN	-	-	-	DGC_EN
80	R_GAMMA0[9:2]							
81	R_GAMMA1[9:2]							
82	R_GAMMA2[9:2]							
83	R_GAMMA3[9:2]							
84	R_GAMMA4[9:2]							
85	R_GAMMA5[9:2]							
86	R_GAMMA6[9:2]							
87	R_GAMMA7[9:2]							
88	R_GAMMA8[9:2]							
89	R_GAMMA9[9:2]							
8A	R_GAMMA10[9:2]							
8B	R_GAMMA11[9:2]							
8C	R_GAMMA12[9:2]							
8D	R_GAMMA13[9:2]							
8E	R_GAMMA14[9:2]							
8F	R_GAMMA15[9:2]							
90	R_GAMMA16[9:2]							
91	R_GAMMA17[9:2]							
92	R_GAMMA18[9:2]							
93	R_GAMMA19[9:2]							
94	R_GAMMA20[9:2]							
95	R_GAMMA21[9:2]							
96	R_GAMMA22[9:2]							
97	R_GAMMA23[9:2]							
98	R_GAMMA24[9:2]							
99	R_GAMMA25[9:2]							
9A	R_GAMMA26[9:2]							
9B	R_GAMMA27[9:2]							
9C	R_GAMMA28[9:2]							
9D	R_GAMMA29[9:2]							
9E	R_GAMMA30[9:2]							
9F	R_GAMMA31[9:2]							
A0	R_GAMMA32[9:2]							
A1	R_GAMMA0[1:0]	R_GAMMA1[1:0]	R_GAMMA2[1:0]	R_GAMMA3[1:0]				
A2	R_GAMMA4[1:0]	R_GAMMA5[1:0]	R_GAMMA6[1:0]	R_GAMMA7[1:0]				
A3	R_GAMMA8[1:0]	R_GAMMA9[1:0]	R_GAMMA10[1:0]	R_GAMMA11[1:0]				
A4	R_GAMMA12[1:0]	R_GAMMA13[1:0]	R_GAMMA14[1:0]	R_GAMMA15[1:0]				
A5	R_GAMMA16[1:0]	R_GAMMA17[1:0]	R_GAMMA18[1:0]	R_GAMMA19[1:0]				
A6	R_GAMMA20[1:0]	R_GAMMA21[1:0]	R_GAMMA22[1:0]	R_GAMMA23[1:0]				
A7	R_GAMMA24[1:0]	R_GAMMA25[1:0]	R_GAMMA26[1:0]	R_GAMMA27[1:0]				
A8	R_GAMMA28[1:0]	R_GAMMA29[1:0]	R_GAMMA30[1:0]	R_GAMMA31[1:0]				
A9	R_GAMMA32[1:0]	-	-	-	-	-	-	
AA	G_GAMMA0[9:2]							

AB	G_GAMMA1[9:2]			
AC	G_GAMMA2[9:2]			
AD	G_GAMMA3[9:2]			
AE	G_GAMMA4[9:2]			
AF	G_GAMMA5[9:2]			
B0	G_GAMMA6[9:2]			
B1	G_GAMMA7[9:2]			
B2	G_GAMMA8[9:2]			
B3	G_GAMMA9[9:2]			
B4	G_GAMMA10[9:2]			
B5	G_GAMMA11[9:2]			
B6	G_GAMMA12[9:2]			
B7	G_GAMMA13[9:2]			
B8	G_GAMMA14[9:2]			
B9	G_GAMMA15[9:2]			
BA	G_GAMMA16[9:2]			
BB	G_GAMMA17[9:2]			
BC	G_GAMMA18[9:2]			
BD	G_GAMMA19[9:2]			
BE	G_GAMMA20[9:2]			
BF	G_GAMMA21[9:2]			
C0	G_GAMMA22[9:2]			
C1	G_GAMMA23[9:2]			
C2	G_GAMMA24[9:2]			
C3	G_GAMMA25[9:2]			
C4	G_GAMMA26[9:2]			
C5	G_GAMMA27[9:2]			
C6	G_GAMMA28[9:2]			
C7	G_GAMMA29[9:2]			
C8	G_GAMMA30[9:2]			
C9	G_GAMMA31[9:2]			
CA	G_GAMMA32[9:2]			
CB	G_GAMMA0[1:0]	G_GAMMA1[1:0]	G_GAMMA2[1:0]	G_GAMMA3[1:0]
CC	G_GAMMA4[1:0]	G_GAMMA5[1:0]	G_GAMMA6[1:0]	G_GAMMA7[1:0]
CD	G_GAMMA8[1:0]	G_GAMMA9[1:0]	G_GAMMA10[1:0]	G_GAMMA11[1:0]
CE	G_GAMMA12[1:0]	G_GAMMA13[1:0]	G_GAMMA14[1:0]	G_GAMMA15[1:0]
CF	G_GAMMA16[1:0]	G_GAMMA17[1:0]	G_GAMMA18[1:0]	G_GAMMA19[1:0]
D0	G_GAMMA20[1:0]	G_GAMMA21[1:0]	G_GAMMA22[1:0]	G_GAMMA23[1:0]
D1	G_GAMMA24[1:0]	G_GAMMA25[1:0]	G_GAMMA26[1:0]	G_GAMMA27[1:0]
D2	G_GAMMA28[1:0]	G_GAMMA29[1:0]	G_GAMMA30[1:0]	G_GAMMA31[1:0]
D3	G_GAMMA32[1:0]	-	-	-
D4	B_GAMMA0[9:2]			
D5	B_GAMMA1[9:2]			
D6	B_GAMMA2[9:2]			
D7	B_GAMMA3[9:2]			
D8	B_GAMMA4[9:2]			
D9	B_GAMMA5[9:2]			
DA	B_GAMMA6[9:2]			
DB	B_GAMMA7[9:2]			
DC	B_GAMMA8[9:2]			
DD	B_GAMMA9[9:2]			
DE	B_GAMMA10[9:2]			
DF	B_GAMMA11[9:2]			
E0	B_GAMMA12[9:2]			
E1	B_GAMMA13[9:2]			
E2	B_GAMMA14[9:2]			
E3	B_GAMMA15[9:2]			
E4	B_GAMMA16[9:2]			
E5	B_GAMMA17[9:2]			
E6	B_GAMMA18[9:2]			
E7	B_GAMMA19[9:2]			
E8	B_GAMMA20[9:2]			
E9	B_GAMMA21[9:2]			
EA	B_GAMMA22[9:2]			
EB	B_GAMMA23[9:2]			

EC	B_GAMMA24[9:2]			
ED	B_GAMMA25[9:2]			
EE	B_GAMMA26[9:2]			
EF	B_GAMMA27[9:2]			
F0	B_GAMMA28[9:2]			
F1	B_GAMMA29[9:2]			
F2	B_GAMMA30[9:2]			
F3	B_GAMMA31[9:2]			
F4	B_GAMMA32[9:2]			
F5	B_GAMMA0[1:0]	B_GAMMA1[1:0]	B_GAMMA2[1:0]	B_GAMMA3[1:0]
F6	B_GAMMA4[1:0]	B_GAMMA5[1:0]	B_GAMMA6[1:0]	B_GAMMA7[1:0]
F7	B_GAMMA8[1:0]	B_GAMMA9[1:0]	B_GAMMA10[1:0]	B_GAMMA11[1:0]
F8	B_GAMMA12[1:0]	B_GAMMA13[1:0]	B_GAMMA14[1:0]	B_GAMMA15[1:0]
F9	B_GAMMA16[1:0]	B_GAMMA17[1:0]	B_GAMMA18[1:0]	B_GAMMA19[1:0]
FA	B_GAMMA20[1:0]	B_GAMMA21[1:0]	B_GAMMA22[1:0]	B_GAMMA23[1:0]
FB	B_GAMMA24[1:0]	B_GAMMA25[1:0]	B_GAMMA26[1:0]	B_GAMMA27[1:0]
FC	B_GAMMA28[1:0]	B_GAMMA29[1:0]	B_GAMMA30[1:0]	B_GAMMA31[1:0]
FD	B_GAMMA32[1:0]	-	-	-
100	NVALID_GAMMA	VHP_0[6:0]		
101	-	VHP_1[6:0]		
102	-	VHP_2[6:0]		
103	-	VHP_3[6:0]		
104	VMP_0[7:0]			
105	VMP_1[7:0]			
106	VMP_2[7:0]			
107	VMP_3[7:0]			
108	VMP_4[7:0]			
109	VMP_5[7:0]			
10A	VMP_6[7:0]			
10B	VMP_7[7:0]			
10C	VMP_8[7:0]			
10D	VMP_9[7:0]			
10E	VMP_10[7:0]			
10F	VMP_11[7:0]			
110	VMP_12[7:0]			
111	VMP_13[7:0]			
112	VMP_14[7:0]			
113	VMP_15[7:0]			
114	VMP_16[7:0]			
115	VMP_17[7:0]			
116	VMP_18[7:0]			
117	-	VLP_0[6:0]		
118	-	VLP_1[6:0]		
119	-	VLP_2[6:0]		
11A	-	VLP_3[6:0]		
11B	-	VHN_0[6:0]		
11C	-	VHN_1[6:0]		
11D	-	VHN_2[6:0]		
11E	-	VHN_3[6:0]		
11F	VMN_0[7:0]			
120	VMN_1[7:0]			
121	VMN_21[7:0]			
122	VMN_3[7:0]			
123	VMN_4[7:0]			
124	VMN_5[7:0]			
125	VMN_6[7:0]			
126	VMN_7[7:0]			
127	VMN_8[7:0]			
128	VMN_9[7:0]			
129	VMN_10[7:0]			
12A	VMN_11[7:0]			
12B	VMN_12[7:0]			
12C	VMN_13[7:0]			
12D	VMN_14[7:0]			

12E	VMN_15[7:0]							
12F	VMN_16[7:0]							
130	VMN_17[7:0]							
131	VMN_18[7:0]							
132	-	VLN_0[6:0]						
133	-	VLN_1[6:0]						
134	-	VLN_2[6:0]						
135	-	VLN_3[6:0]						
13A	NVALID_DG C	-	-	-	-	-	-	-
13B	R(_N)_GAMMA0[9:2]							
13C	R(_N)_GAMMA1[9:2]							
13D	R(_N)_GAMMA2[9:2]							
13E	R(_N)_GAMMA3[9:2]							
13F	R(_N)_GAMMA4[9:2]							
140	R(_N)_GAMMA5[9:2]							
141	R(_N)_GAMMA6[9:2]							
142	R(_N)_GAMMA7[9:2]							
143	R(_N)_GAMMA8[9:2]							
144	R(_N)_GAMMA9[9:2]							
145	R(_N)_GAMMA10[9:2]							
146	R(_N)_GAMMA11[9:2]							
147	R(_N)_GAMMA12[9:2]							
148	R(_N)_GAMMA13[9:2]							
149	R(_N)_GAMMA14[9:2]							
14A	R(_N)_GAMMA15[9:2]							
14B	R(_N)_GAMMA16[9:2]							
14C	R(_N)_GAMMA17[9:2]							
14D	R(_N)_GAMMA18[9:2]							
14E	R(_N)_GAMMA19[9:2]							
14F	R(_N)_GAMMA20[9:2]							
150	R(_N)_GAMMA21[9:2]							
151	R(_N)_GAMMA22[9:2]							
152	R(_N)_GAMMA23[9:2]							
153	R(_N)_GAMMA24[9:2]							
154	R(_N)_GAMMA25[9:2]							
155	R(_N)_GAMMA26[9:2]							
156	R(_N)_GAMMA27[9:2]							
157	R(_N)_GAMMA28[9:2]							
158	R(_N)_GAMMA29[9:2]							
159	R(_N)_GAMMA30[9:2]							
15A	R(_N)_GAMMA31[9:2]							
15B	R(_N)_GAMMA32[9:2]							
15C	R(_N)_GAMMA0[1:0]	R(_N)_GAMMA1[1:0]	R(_N)_GAMMA2[1:0]	R(_N)_GAMMA3[1:0]				
15D	R(_N)_GAMMA4[1:0]	R(_N)_GAMMA5[1:0]	R(_N)_GAMMA6[1:0]	R(_N)_GAMMA7[1:0]				
15E	R(_N)_GAMMA8[1:0]	R(_N)_GAMMA9[1:0]	R(_N)_GAMMA10[1:0]	R(_N)_GAMMA11[1:0]				
15F	R(_N)_GAMMA12[1:0]	R(_N)_GAMMA13[1:0]	R(_N)_GAMMA14[1:0]	R(_N)_GAMMA15[1:0]				
160	R(_N)_GAMMA16[1:0]	R(_N)_GAMMA17[1:0]	R(_N)_GAMMA18[1:0]	R(_N)_GAMMA19[1:0]				
161	R(_N)_GAMMA20[1:0]	R(_N)_GAMMA21[1:0]	R(_N)_GAMMA22[1:0]	R(_N)_GAMMA23[1:0]				
162	R(_N)_GAMMA24[1:0]	R(_N)_GAMMA25[1:0]	R(_N)_GAMMA26[1:0]	R(_N)_GAMMA27[1:0]				
163	R(_N)_GAMMA28[1:0]	R(_N)_GAMMA29[1:0]	R(_N)_GAMMA30[1:0]	R(_N)_GAMMA31[1:0]				
164	R(_N)_GAMMA32[1:0]	-	-	-	-	-	-	-
165	G(_N)_GAMMA0[9:2]							
166	G(_N)_GAMMA1[9:2]							
167	G(_N)_GAMMA2[9:2]							
168	G(_N)_GAMMA3[9:2]							
169	G(_N)_GAMMA4[9:2]							
16A	G(_N)_GAMMA5[9:2]							
16B	G(_N)_GAMMA6[9:2]							
16C	G(_N)_GAMMA7[9:2]							
16D	G(_N)_GAMMA8[9:2]							
16E	G(_N)_GAMMA9[9:2]							
16F	G(_N)_GAMMA10[9:2]							
170	G(_N)_GAMMA11[9:2]							
171	G(_N)_GAMMA12[9:2]							

172	G(_N)_GAMMA13[9:2]			
173	G(_N)_GAMMA14[9:2]			
174	G(_N)_GAMMA15[9:2]			
175	G(_N)_GAMMA16[9:2]			
176	G(_N)_GAMMA17[9:2]			
177	G(_N)_GAMMA18[9:2]			
178	G(_N)_GAMMA19[9:2]			
179	G(_N)_GAMMA20[9:2]			
17A	G(_N)_GAMMA21[9:2]			
17B	G(_N)_GAMMA22[9:2]			
17C	G(_N)_GAMMA23[9:2]			
17D	G(_N)_GAMMA24[9:2]			
17E	G(_N)_GAMMA25[9:2]			
17F	G(_N)_GAMMA26[9:2]			
180	G(_N)_GAMMA27[9:2]			
181	G(_N)_GAMMA28[9:2]			
182	G(_N)_GAMMA29[9:2]			
183	G(_N)_GAMMA30[9:2]			
184	G(_N)_GAMMA31[9:2]			
185	G(_N)_GAMMA32[9:2]			
186	G(_N)_GAMMA0[1:0]	G(_N)_GAMMA1[1:0]	G(_N)_GAMMA2[1:0]	G(_N)_GAMMA3[1:0]
187	G(_N)_GAMMA4[1:0]	G(_N)_GAMMA5[1:0]	G(_N)_GAMMA6[1:0]	G(_N)_GAMMA7[1:0]
188	G(_N)_GAMMA8[1:0]	G(_N)_GAMMA9[1:0]	G(_N)_GAMMA10[1:0]	G(_N)_GAMMA11[1:0]
189	G(_N)_GAMMA12[1:0]	G(_N)_GAMMA13[1:0]	G(_N)_GAMMA14[1:0]	G(_N)_GAMMA15[1:0]
18A	G(_N)_GAMMA16[1:0]	G(_N)_GAMMA17[1:0]	G(_N)_GAMMA18[1:0]	G(_N)_GAMMA19[1:0]
18B	G(_N)_GAMMA20[1:0]	G(_N)_GAMMA21[1:0]	G(_N)_GAMMA22[1:0]	G(_N)_GAMMA23[1:0]
18C	G(_N)_GAMMA24[1:0]	G(_N)_GAMMA25[1:0]	G(_N)_GAMMA26[1:0]	G(_N)_GAMMA27[1:0]
18D	G(_N)_GAMMA28[1:0]	G(_N)_GAMMA29[1:0]	G(_N)_GAMMA30[1:0]	G(_N)_GAMMA31[1:0]
18E	G(_N)_GAMMA32[1:0]	-	-	-
18F	B(_N)_GAMMA0[9:2]			
190	B(_N)_GAMMA1[9:2]			
191	B(_N)_GAMMA2[9:2]			
192	B(_N)_GAMMA3[9:2]			
193	B(_N)_GAMMA4[9:2]			
194	B(_N)_GAMMA5[9:2]			
195	B(_N)_GAMMA6[9:2]			
196	B(_N)_GAMMA7[9:2]			
197	B(_N)_GAMMA8[9:2]			
198	B(_N)_GAMMA9[9:2]			
199	B(_N)_GAMMA10[9:2]			
19A	B(_N)_GAMMA11[9:2]			
19B	B(_N)_GAMMA12[9:2]			
19C	B(_N)_GAMMA13[9:2]			
19D	B(_N)_GAMMA14[9:2]			
19E	B(_N)_GAMMA15[9:2]			
19F	B(_N)_GAMMA16[9:2]			
1A0	B(_N)_GAMMA17[9:2]			
1A1	B(_N)_GAMMA18[9:2]			
1A2	B(_N)_GAMMA19[9:2]			
1A3	B(_N)_GAMMA20[9:2]			
1A4	B(_N)_GAMMA21[9:2]			
1A5	B(_N)_GAMMA22[9:2]			
1A6	B(_N)_GAMMA23[9:2]			
1A7	B(_N)_GAMMA24[9:2]			
1A8	B(_N)_GAMMA25[9:2]			
1A9	B(_N)_GAMMA26[9:2]			
1AA	B(_N)_GAMMA27[9:2]			
1AB	B(_N)_GAMMA28[9:2]			
1AC	B(_N)_GAMMA29[9:2]			
1AD	B(_N)_GAMMA30[9:2]			
1AE	B(_N)_GAMMA31[9:2]			
1AF	B(_N)_GAMMA32[9:2]			
1B0	B(_N)_GAMMA0[1:0]	B(_N)_GAMMA1[1:0]	B(_N)_GAMMA2[1:0]	B(_N)_GAMMA3[1:0]
1B1	B(_N)_GAMMA4[1:0]	B(_N)_GAMMA5[1:0]	B(_N)_GAMMA6[1:0]	B(_N)_GAMMA7[1:0]
1B2	B(_N)_GAMMA8[1:0]	B(_N)_GAMMA9[1:0]	B(_N)_GAMMA10[1:0]	B(_N)_GAMMA11[1:0]

1B3	B(N)_GAMMA12[1:0]	B(N)_GAMMA13[1:0]	B(N)_GAMMA14[1:0]	B(N)_GAMMA15[1:0]
1B4	B(N)_GAMMA16[1:0]	B(N)_GAMMA17[1:0]	B(N)_GAMMA18[1:0]	B(N)_GAMMA19[1:0]
1B5	B(N)_GAMMA20[1:0]	B(N)_GAMMA21[1:0]	B(N)_GAMMA22[1:0]	B(N)_GAMMA23[1:0]
1B6	B(N)_GAMMA24[1:0]	B(N)_GAMMA25[1:0]	B(N)_GAMMA26[1:0]	B(N)_GAMMA27[1:0]
1B7	B(N)_GAMMA28[1:0]	B(N)_GAMMA29[1:0]	B(N)_GAMMA30[1:0]	B(N)_GAMMA31[1:0]
1B8	B(N)_GAMMA32[1:0]	-	-	-
1B9	NVALID_GI P_D3	-	GIP_EQ_OPT[1:0]	-
1BA	-	-	-	EQ_DELAY_HSYNC[1:0]
1BB	EQ_DELAY_ON1[7:0]			
1BC	EQ_DELAY_OFF1[7:0]			
1BD	GTO[7:0]			
1BE	GNO[7:0]			
1BF	USER_GIP_GATE[7:0]			
1C0	USER_GIP_GATE1[7:0]			
1C1	SHR0_3[3:0]		SHR0_2[3:0]	
1C2	SHR0_1[3:0]		SHR0[11:8]	
1C3	SHR0[7:0]			
1C4	-	-	-	SHR0_GS[11:8]
1C5	SHR0_GS[7:0]			
1C6	SHR1_3[3:0]		SHR1_2[3:0]	
1C7	SHR1_1[3:0]		SHR1[11:8]	
1C8	SHR1[7:0]			
1C9	-	-	-	SHR1_GS[11:8]
1CA	SHR1_GS[7:0]			
1CB	SHR2_3[3:0]		SHR2_2[3:0]	
1CC	SHR2_1[3:0]		SHR2[11:8]	
1CD	SHR2[7:0]			
1CE	-	-	-	SHR2_GS[11:8]
1CF	SHR2_GS[7:0]			
1D0	SHP0[3:0]		SCP[3:0]	
1D1	SHP2[3:0]		SHP1[3:0]	
1D2	CHR0[7:0]			
1D3	CHR0_GS[7:0]			
1D4	CHP0[3:0]		CCP0[3:0]	
1D5	CHR1[7:0]			
1D6	CHR1_GS[7:0]			
1D7	CHP1[3:0]		CCP1[3:0]	
1D8	vbp_setting[7:0]			
1D9	-	vbp_self_lea rning	-	-
1F5	NVALID_CA BC	-	-	SLR_EN
1F6	PWM_PERIOD[15:8]			
1F7	PWM_PERIOD[7:0]			
200	NVALID_GI P_D8	-	-	-
201	INIT_0_SEL_CGOUT1_L[1:0]	INIT_0_SEL_CGOUT2_L[1:0]	INIT_0_SEL_CGOUT3_L[1:0]	INIT_0_SEL_CGOUT4_L[1:0]
202	INIT_0_SEL_CGOUT5_L[1:0]	INIT_0_SEL_CGOUT6_L[1:0]	INIT_0_SEL_CGOUT7_L[1:0]	INIT_0_SEL_CGOUT8_L[1:0]
203	INIT_0_SEL_CGOUT9_L[1:0]	INIT_0_SEL_CGOUT10_L [1:0]	INIT_0_SEL_CGOUT11_ L[1:0]	INIT_0_SEL_CGOUT12_L [1:0]
204	INIT_0_SEL_CGOUT13_ L[1:0]	INIT_0_SEL_CGOUT14_L [1:0]	INIT_0_SEL_CGOUT15_ L[1:0]	INIT_0_SEL_CGOUT16_L [1:0]
205	INIT_0_SEL_CGOUT1_R[1:0]	INIT_0_SEL_CGOUT2_R[1:0]	INIT_0_SEL_CGOUT3_R[1:0]	INIT_0_SEL_CGOUT4_R[1:0]
206	INIT_0_SEL_CGOUT5_R[1:0]	INIT_0_SEL_CGOUT6_R[1:0]	INIT_0_SEL_CGOUT7_R[1:0]	INIT_0_SEL_CGOUT8_R[1:0]
207	INIT_0_SEL_CGOUT9_R[1:0]	INIT_0_SEL_CGOUT10_ R[1:0]	INIT_0_SEL_CGOUT11_ R[1:0]	INIT_0_SEL_CGOUT12_ R[1:0]
208	INIT_0_SEL_CGOUT13_ R[1:0]	INIT_0_SEL_CGOUT14_ R[1:0]	INIT_0_SEL_CGOUT15_ R[1:0]	INIT_0_SEL_CGOUT16_ R[1:0]
209	INIT_1_SEL_CGOUT1_L[1:0]	INIT_1_SEL_CGOUT2_L[1:0]	INIT_1_SEL_CGOUT3_L[1:0]	INIT_1_SEL_CGOUT4_L[1:0]

20A	INIT_1_SEL_CGOUT5_L[1:0]	INIT_1_SEL_CGOUT6_L[1:0]	INIT_1_SEL_CGOUT7_L[1:0]	INIT_1_SEL_CGOUT8_L[1:0]				
20B	INIT_1_SEL_CGOUT9_L[1:0]	INIT_1_SEL_CGOUT10_L[1:0]	INIT_1_SEL_CGOUT11_L[1:0]	INIT_1_SEL_CGOUT12_L[1:0]				
20C	INIT_1_SEL_CGOUT13_L[1:0]	INIT_1_SEL_CGOUT14_L[1:0]	INIT_1_SEL_CGOUT15_L[1:0]	INIT_1_SEL_CGOUT16_L[1:0]				
20D	INIT_1_SEL_CGOUT1_R[1:0]	INIT_1_SEL_CGOUT2_R[1:0]	INIT_1_SEL_CGOUT3_R[1:0]	INIT_1_SEL_CGOUT4_R[1:0]				
20E	INIT_1_SEL_CGOUT5_R[1:0]	INIT_1_SEL_CGOUT6_R[1:0]	INIT_1_SEL_CGOUT7_R[1:0]	INIT_1_SEL_CGOUT8_R[1:0]				
20F	INIT_1_SEL_CGOUT9_R[1:0]	INIT_1_SEL_CGOUT10_R[1:0]	INIT_1_SEL_CGOUT11_R[1:0]	INIT_1_SEL_CGOUT12_R[1:0]				
210	INIT_1_SEL_CGOUT13_R[1:0]	INIT_1_SEL_CGOUT14_R[1:0]	INIT_1_SEL_CGOUT15_R[1:0]	INIT_1_SEL_CGOUT16_R[1:0]				
211	END_0_SEL_CGOUT1_L[1:0]	END_0_SEL_CGOUT2_L[1:0]	END_0_SEL_CGOUT3_L[1:0]	END_0_SEL_CGOUT4_L[1:0]				
212	END_0_SEL_CGOUT5_L[1:0]	END_0_SEL_CGOUT6_L[1:0]	END_0_SEL_CGOUT7_L[1:0]	END_0_SEL_CGOUT8_L[1:0]				
213	END_0_SEL_CGOUT9_L[1:0]	END_0_SEL_CGOUT10_L[1:0]	END_0_SEL_CGOUT11_L[1:0]	END_0_SEL_CGOUT12_L[1:0]				
214	END_0_SEL_CGOUT13_L[1:0]	END_0_SEL_CGOUT14_L[1:0]	END_0_SEL_CGOUT15_L[1:0]	END_0_SEL_CGOUT16_L[1:0]				
215	END_0_SEL_CGOUT1_R[1:0]	END_0_SEL_CGOUT2_R[1:0]	END_0_SEL_CGOUT3_R[1:0]	END_0_SEL_CGOUT4_R[1:0]				
216	END_0_SEL_CGOUT5_R[1:0]	END_0_SEL_CGOUT6_R[1:0]	END_0_SEL_CGOUT7_R[1:0]	END_0_SEL_CGOUT8_R[1:0]				
217	END_0_SEL_CGOUT9_R[1:0]	END_0_SEL_CGOUT10_R[1:0]	END_0_SEL_CGOUT11_R[1:0]	END_0_SEL_CGOUT12_R[1:0]				
218	END_0_SEL_CGOUT1_R[1:0]	END_0_SEL_CGOUT2_R[1:0]	END_0_SEL_CGOUT3_R[1:0]	END_0_SEL_CGOUT4_R[1:0]				
219	END_1_SEL_CGOUT1_L[1:0]	END_1_SEL_CGOUT2_L[1:0]	END_1_SEL_CGOUT3_L[1:0]	END_1_SEL_CGOUT4_L[1:0]				
21A	END_1_SEL_CGOUT5_L[1:0]	END_1_SEL_CGOUT6_L[1:0]	END_1_SEL_CGOUT7_L[1:0]	END_1_SEL_CGOUT8_L[1:0]				
21B	END_1_SEL_CGOUT9_L[1:0]	END_1_SEL_CGOUT10_L[1:0]	END_1_SEL_CGOUT11_L[1:0]	END_1_SEL_CGOUT12_L[1:0]				
21C	END_1_SEL_CGOUT13_L[1:0]	END_1_SEL_CGOUT14_L[1:0]	END_1_SEL_CGOUT15_L[1:0]	END_1_SEL_CGOUT16_L[1:0]				
21D	END_1_SEL_CGOUT1_R[1:0]	END_1_SEL_CGOUT2_R[1:0]	END_1_SEL_CGOUT3_R[1:0]	END_1_SEL_CGOUT4_R[1:0]				
21E	END_1_SEL_CGOUT5_R[1:0]	END_1_SEL_CGOUT6_R[1:0]	END_1_SEL_CGOUT7_R[1:0]	END_1_SEL_CGOUT8_R[1:0]				
21F	END_1_SEL_CGOUT9_R[1:0]	END_1_SEL_CGOUT10_R[1:0]	END_1_SEL_CGOUT11_R[1:0]	END_1_SEL_CGOUT12_R[1:0]				
220	END_1_SEL_CGOUT13_R[1:0]	END_1_SEL_CGOUT14_R[1:0]	END_1_SEL_CGOUT15_R[1:0]	END_1_SEL_CGOUT16_R[1:0]				
229	GAS_0_SEL_CGOUT1_L[1:0]	GAS_0_SEL_CGOUT2_L[1:0]	GAS_0_SEL_CGOUT3_L[1:0]	GAS_0_SEL_CGOUT4_L[1:0]				
22A	GAS_0_SEL_CGOUT5_L[1:0]	GAS_0_SEL_CGOUT6_L[1:0]	GAS_0_SEL_CGOUT7_L[1:0]	GAS_0_SEL_CGOUT8_L[1:0]				
22B	GAS_0_SEL_CGOUT9_L[1:0]	GAS_0_SEL_CGOUT10_L[1:0]	GAS_0_SEL_CGOUT11_L[1:0]	GAS_0_SEL_CGOUT12_L[1:0]				
22C	GAS_0_SEL_CGOUT13_L[1:0]	GAS_0_SEL_CGOUT14_L[1:0]	GAS_0_SEL_CGOUT15_L[1:0]	GAS_0_SEL_CGOUT16_L[1:0]				
22D	GAS_0_SEL_CGOUT1_R[1:0]	GAS_0_SEL_CGOUT2_R[1:0]	GAS_0_SEL_CGOUT3_R[1:0]	GAS_0_SEL_CGOUT4_R[1:0]				
22E	GAS_0_SEL_CGOUT5_R[1:0]	GAS_0_SEL_CGOUT6_R[1:0]	GAS_0_SEL_CGOUT7_R[1:0]	GAS_0_SEL_CGOUT8_R[1:0]				
22F	GAS_0_SEL_CGOUT9_R[1:0]	GAS_0_SEL_CGOUT10_R[1:0]	GAS_0_SEL_CGOUT11_R[1:0]	GAS_0_SEL_CGOUT12_R[1:0]				
230	GAS_0_SEL_CGOUT13_R[1:0]	GAS_0_SEL_CGOUT14_R[1:0]	GAS_0_SEL_CGOUT15_R[1:0]	GAS_0_SEL_CGOUT16_R[1:0]				
234	NVALID_SCL	-	-	-	-	-	SCALING_T YPE	SCALING_E N
23B	NVALID_1B PP	-	-	-	-	-	NW_I[2:0]	

23C	BP_I[7:0]				
23D	FP_I[7:0]				
23E	RTN_I[7:0]				
23F	VCMC_F_I[7:0]				
240	VCMC_B_I[7:0]				
241	AP_I[2:0]	-	-	-	VCMC_B_I[8] VCMC_F_I[8]
242	FS0_I[3:0]			FS1_I[3:0]	
243	FS2_I[3:0]			-	-
246	NVALID_CE_MODE	-	-	-	DYN_CEH_EN
247	HUE_MODE[1:0]	SE_MODE[1:0]	BE_MODE[1:0]	CE_MODE[1:0]	
249	NVALID_GIP_D5	CGTS_L_INV[1]	COS1_L[5:0] (CGOUT1_L)		
24A	-	CGTS_R_INV[1]	COS1_R[5:0] (CGOUT1_R)		
24B	-	CGTS_L_INV[2]	COS2_L[5:0] (CGOUT2_L)		
24C	-	CGTS_R_INV[2]	COS2_R[5:0] (CGOUT2_R)		
24D	-	CGTS_L_INV[3]	COS3_L[5:0] (CGOUT3_L)		
24E	-	CGTS_R_INV[3]	COS3_R[5:0] (CGOUT3_R)		
24F	-	CGTS_L_INV[4]	COS4_L[5:0] (CGOUT4_L)		
250	-	CGTS_R_INV[4]	COS4_R[5:0] (CGOUT4_R)		
251	-	CGTS_L_INV[5]	COS5_L[5:0] (CGOUT5_L)		
252	-	CGTS_R_INV[5]	COS5_R[5:0] (CGOUT5_R)		
253	-	CGTS_L_INV[6]	COS6_L[5:0] (CGOUT6_L)		
254	-	CGTS_R_INV[6]	COS6_R[5:0] (CGOUT6_R)		
255	-	CGTS_L_INV[7]	COS7_L[5:0] (CGOUT7_L)		
256	-	CGTS_R_INV[7]	COS7_R[5:0] (CGOUT7_R)		
257	-	CGTS_L_INV[8]	COS8_L[5:0] (CGOUT8_L)		
258	-	CGTS_R_INV[8]	COS8_R[5:0] (CGOUT8_R)		
259	-	CGTS_L_INV[9]	COS9_L[5:0] (CGOUT9_L)		
25A	-	CGTS_R_INV[9]	COS9_R[5:0] (CGOUT9_R)		
25B	-	CGTS_L_INV[10]	COS10_L[5:0] (CGOUT10_L)		
25C	-	CGTS_R_INV[10]	COS10_R[5:0] (CGOUT10_R)		
25D	-	CGTS_L_INV[11]	COS11_L[5:0] (CGOUT11_L)		
25E	-	CGTS_R_INV[11]	COS11_R[5:0] (CGOUT11_R)		
25F	-	CGTS_L_INV[12]	COS12_L[5:0] (CGOUT12_L)		
260	-	CGTS_R_INV[12]	COS12_R[5:0] (CGOUT12_R)		
261	-	CGTS_L_INV[13]	COS13_L[5:0] (CGOUT13_L)		
262	-	CGTS_R_INV[13]	COS13_R[5:0] (CGOUT13_R)		
263	-	CGTS_L_INV[14]	COS14_L[5:0] (CGOUT14_L)		

264	-	CGTS_R_IN V[14]	COS14_R[5:0] (CGOUT14_R)
265	-	CGTS_L_INV [15]	COS15_L[5:0] (CGOUT15_L)
266	-	CGTS_R_IN V[15]	COS15_R[5:0] (CGOUT15_R)
267	-	CGTS_L_INV [16]	COS16_L[5:0] (CGOUT16_L)
268	-	CGTS_R_IN V[16]	COS16_R[5:0] (CGOUT16_R)
275	NVALID_GI P_D6	CGOUT_L_H IZ_IN[1]	COS1_L_GS[5:0] (CGOUT1_L)
276	-	CGOUT_R_ HIZ_IN[1]	COS1_R_GS[5:0] (CGOUT1_R)
277	-	CGOUT_L_H IZ_IN[2]	COS2_L_GS[5:0] (CGOUT2_L)
278	-	CGOUT_R_ HIZ_IN[2]	COS2_R_GS[5:0] (CGOUT2_R)
279	-	CGOUT_L_H IZ_IN[3]	COS3_L_GS[5:0] (CGOUT3_L)
27A	-	CGOUT_R_ HIZ_IN[3]	COS3_R_GS[5:0] (CGOUT3_R)
27B	-	CGOUT_L_H IZ_IN[4]	COS4_L_GS[5:0] (CGOUT4_L)
27C	-	CGOUT_R_ HIZ_IN[4]	COS4_R_GS[5:0] (CGOUT4_R)
27D	-	CGOUT_L_H IZ_IN[5]	COS5_L_GS[5:0] (CGOUT5_L)
27E	-	CGOUT_R_ HIZ_IN[5]	COS5_R_GS[5:0] (CGOUT5_R)
27F	-	CGOUT_L_H IZ_IN[6]	COS6_L_GS[5:0] (CGOUT6_L)
280	-	CGOUT_R_ HIZ_IN[6]	COS6_R_GS[5:0] (CGOUT6_R)
281	-	CGOUT_L_H IZ_IN[7]	COS7_L_GS[5:0] (CGOUT7_L)
282	-	CGOUT_R_ HIZ_IN[7]	COS7_R_GS[5:0] (CGOUT7_R)
283	-	CGOUT_L_H IZ_IN[8]	COS8_L_GS[5:0] (CGOUT8_L)
284	-	CGOUT_R_ HIZ_IN[8]	COS8_R_GS[5:0] (CGOUT8_R)
285	-	CGOUT_L_H IZ_IN[9]	COS9_L_GS[5:0] (CGOUT9_L)
286	-	CGOUT_R_ HIZ_IN[9]	COS9_R_GS[5:0] (CGOUT9_R)
287	-	CGOUT_L_H IZ_IN[10]	COS10_L_GS[5:0] (CGOUT10_L)
288	-	CGOUT_R_ HIZ_IN[10]	COS10_R_GS[5:0] (CGOUT10_R)
289	-	CGOUT_L_H IZ_IN[11]	COS11_L_GS[5:0] (CGOUT11_L)
28A	-	CGOUT_R_ HIZ_IN[11]	COS11_R_GS[5:0] (CGOUT11_R)
28B	-	CGOUT_L_H IZ_IN[12]	COS12_L_GS[5:0] (CGOUT12_L)
28C	-	CGOUT_R_ HIZ_IN[12]	COS12_R_GS[5:0] (CGOUT12_R)
28D	-	CGOUT_L_H IZ_IN[13]	COS13_L_GS[5:0] (CGOUT13_L)
28E	-	CGOUT_R_ HIZ_IN[13]	COS13_R_GS[5:0] (CGOUT13_R)
28F	-	CGOUT_L_H IZ_IN[14]	COS14_L_GS[5:0] (CGOUT14_L)
290	-	CGOUT_R_ HIZ_IN[14]	COS14_R_GS[5:0] (CGOUT14_R)

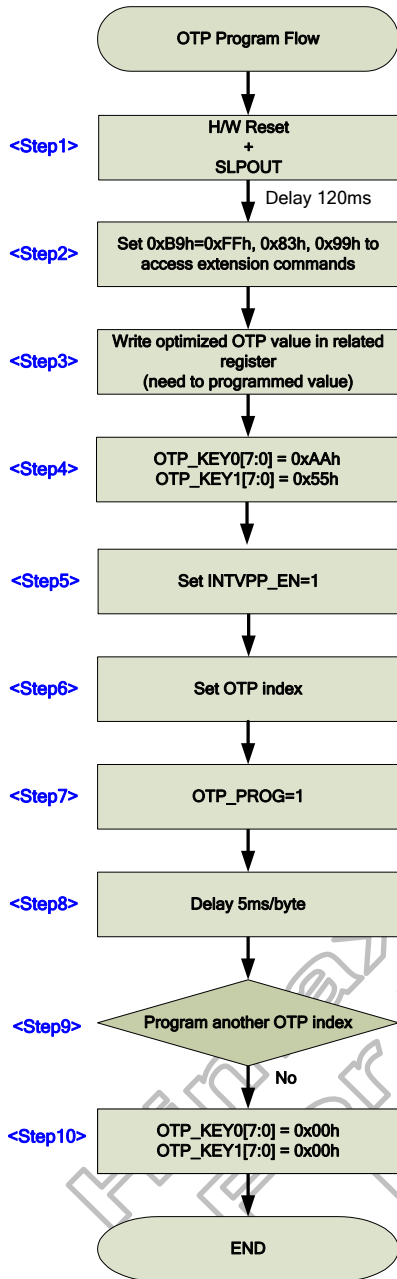
291	-	CGOUT_L_HIZ_IN[15]	COS15_L_GS[5:0] (CGOUT15_L)						
292	-	CGOUT_R_HIZ_IN[15]	COS15_R_GS[5:0] (CGOUT15_R)						
293	-	CGOUT_L_HIZ_IN[16]	COS16_L_GS[5:0] (CGOUT16_L)						
294	-	CGOUT_R_HIZ_IN[16]	COS16_R_GS[5:0] (CGOUT16_R)						
2ED	NVALID_POWER	-	-	-	-	-	-	DSTB	
2EE	-	-	-	-	VSP_FBOF	AP[2:0]			
2EF	-	VCI_LDOS[1:0]			VRHP[4:0]				
2F0	VPPS[2:0]			VRHN[4:0]					
2F1	-	-	-	-	XDK[2:0]				
2F2	-	-	CLK_OPT2	CLK_OPT1	FS0[3:0]				
2F3	FS1[3:0]			FS2[3:0]					
2F4	-	-	-	BTP[4:0]					
2F5	-	-	-	BTN[4:0]					
2F6	VGHS[7:0]								
2F7	VGLS[7:0]								
2F8	DT1[1:0]		DT2[1:0]		DCDIV[3:0]				
2F9	-	DCS[2:0]			-	DC[2:0]			
2FA	-	DTPS[2:0]			-	DTP[2:0]			
2FB	-	DTNS[2:0]			-	DTN[2:0]			
309	NVALID_GAS	APF_EN	GASIOVCC_OPT[1:0]		-	GASVCI_OPT[2:0]			
30A	-	GASVSN_OPT[2:0]				-	GASVSP_OPT[2:0]		
30D	NVALID_DSP	ZZ_LR	ZZ_EO	ZZ_2PL	-	NW[2:0]			
30E	MUX_SEL	-			TGS[3:0]				
30F	MESSI_ENB	-	-	-	-	-	-	-	
310	NL[7:0]								
311	BP [7:0]								
312	FP [7:0]								
313	RTN[7:0]								
314	-	END_SET	END_SET_0[1:0]		-	INIT_SET	INIT_SET_0[1:0]		
315	-	-	INIT_SET_1[1:0]		-	-	-		
316	-	-	END_SET_1[1:0]		-	-	-		
317	-	-	INIT_SD_SEL	INIT_VCOM_SEL	-	-	END_SD_SEL	END_VCOM_SEL	
318	FRM_PATTERN_CYCLE[3:0]				DISP_BIST_EN	FRM_SCAN_CYCLE[2:0]			
31D	NVALID_I2CSA	I2C_SA[6:0]							
320	NVALID_CYC	-	-	DX2_EN	-	-	-	-	
321	GEN_ON[7:0]								
322	GEN_OFF[7:0]								
323	SPON[7:0]								
324	SPOFF[7:0]								
325	CON[7:0]								
326	COFF[7:0]								
327	CON1[7:0]								
328	COFF1[7:0]								
329	N_t1[7:0]								
32A	N_t2[7:0]								
32B	N_t3[7:0]								
32C	N_t4[7:0]								
32D	N_t5[7:0]								
32E	N_t6[7:0]								
32F	N_t7[7:0]								
330	N_t8[7:0]								
331	N_t9[7:0]								
332	SAP1_P[3:0]				SAP1_N[3:0]				

333	-	-	-	-	-	SAP2[2:0]
334	-	-	-	-	-	EQT[3:0]
335						N_t10[7:0]
336						SON[7:0]
337						SOFF[7:0]
338						DX2OFF[7:0]
339						SPON_MPU[7:0]
33A						SPOFF_MPU[7:0]
33B						CON_MPU[7:0]
33C						COFF_MPU[7:0]
33D						CON1_MPU[7:0]
33E						COFF1_MPU[7:0]
33F						N_t1_MPU[7:0]
340						N_t2_MPU[7:0]
341						N_t3_MPU[7:0]
342						N_t4_MPU[7:0]
343						N_t5_MPU[7:0]
344						N_t6_MPU[7:0]
345						N_t7_MPU[7:0]
346						N_t8_MPU[7:0]
347						N_t9_MPU[7:0]
348	-	-	-	-	-	EQT_MPU[3:0]
349						N_t10_MPU[7:0]
34A						SON_MPU[7:0]
34B						SOFF_MPU[7:0]
34C						DX2OFF_MPU[7:0]

Table 5.40: OTP table

Himax Confidential
For Huawei Co., Ltd.
Do Not Copy

5.15.2 OTP programming flow



OTP_KEY0[7:0] OTP_KEY1[7:0]	Description	Note
OTP_KEY0[7:0] = 0xAAh OTP_KEY1[7:0] = 0x55h	Enter OTP program mode	
OTP_KEY0[7:0] = 0x00h OTP_KEY1[7:0] = 0x00h	Leave OTP program mode	
Other value	Invalid	A. If HX8399-C operate on OTP program mode, then keep on OTP program mode. B. If HX8399-C operate on non-OTP program mode, then keep on non-OTP program mode.

Figure 5.44: OTP programming sequence

5.15.3 OTP programming sequence

Step	Operation
1	Power on, reset the module and SLPOUT.
2	Set 0xB9h = 0xFFh, 0x83h, 0x99h to access the extension commands.
3	Write optimized values to related registers.
4	Set OTP_KEY0[7:0]=0xAAh and OTP_KEY1[7:0]=0x55h to enter OTP program mode.
5	Set INTVPP_EN=1 for internal power mode. (or external fed 8.5V to VPP.)
6	Specify OTP_Index, please refer to the OTP table.
7	Set OTP_PROG=1, Internal register begin write to OTP according to OTP_index.
8	Wait 10 ms/byte for programming time (Note 1)
9	Complete programming one parameter to OTP. If continue to programming other parameter, return to step (6). Otherwise, go to step (10)
10	Set OTP_KEY0[7:0]=0x00h and OTP_KEY1[7:0]=0x00h to leave OTP program mode.

Note1: When do the OTP programming process, it must be added 10ms/byte delay time after setting OTP_PROG=1.

Note2: If user want to program ID1~ID4, only need program OTP Index 0x00h.State machine will program ID1~ID4 and valid bit automatically.

Note3: If user want to program VCMC_F and VCMC_B, only need program OTP Index 0x0Dh.State machine will program VCMC_F and VCMC_B and valid bit automatically.

Table 5.41: OTP programming sequence

Himax Confidential
For Huawei Only
Do Not Copy

5.15.4 OTP programming example of VCOM setting VCMC

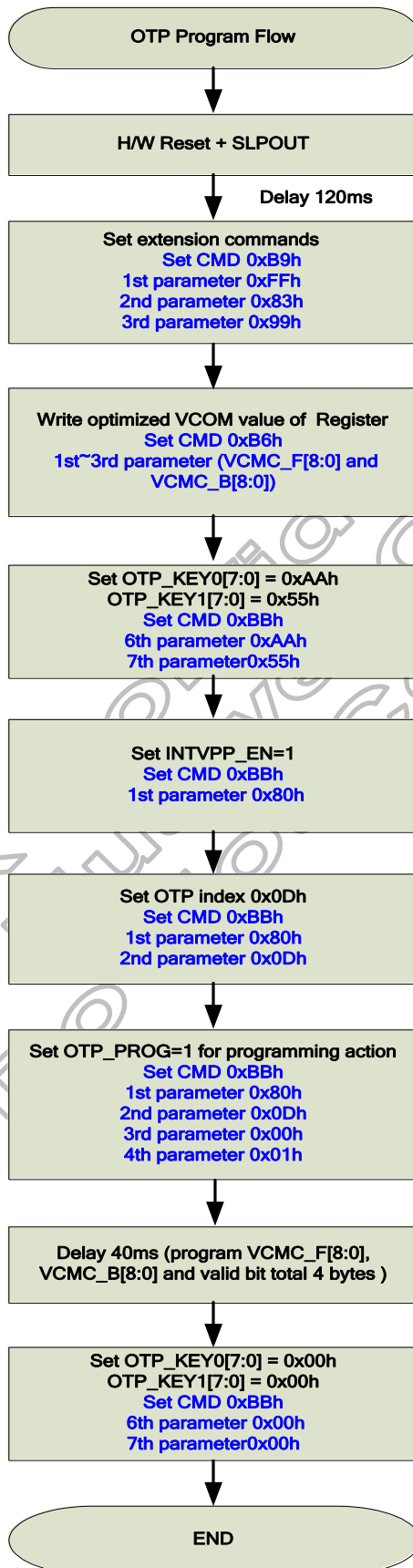


Figure 5.45: OTP programming sequence example 1

5.15.5 OTP programming example of ID1, ID2, ID3 and ID4

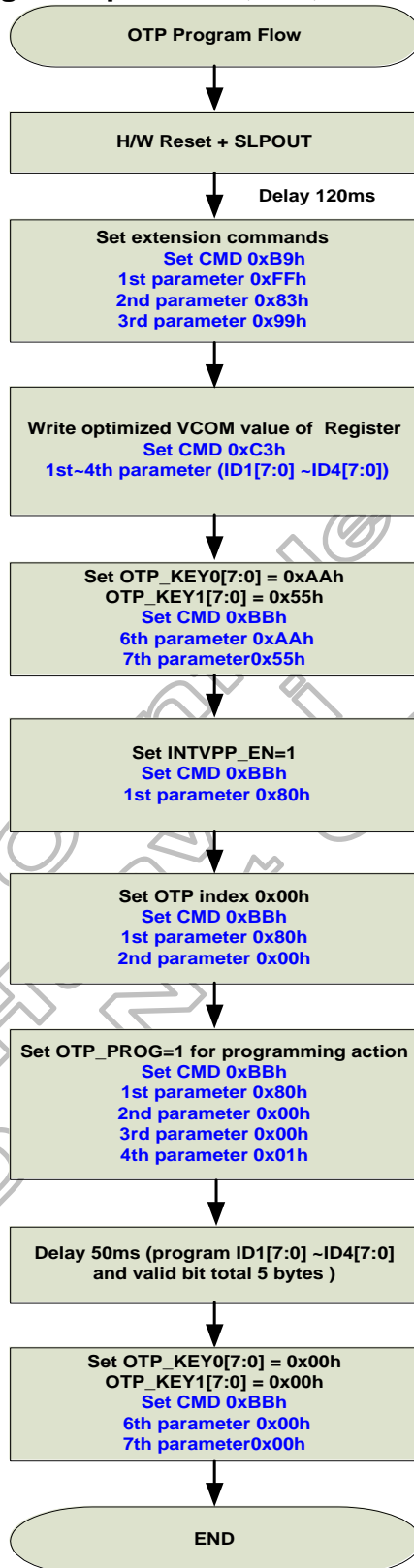


Figure 5.46: OTP programming sequence example 2

5.15.6 OTP Programming all OTP Index(000h~366h except 02Eh~044h)

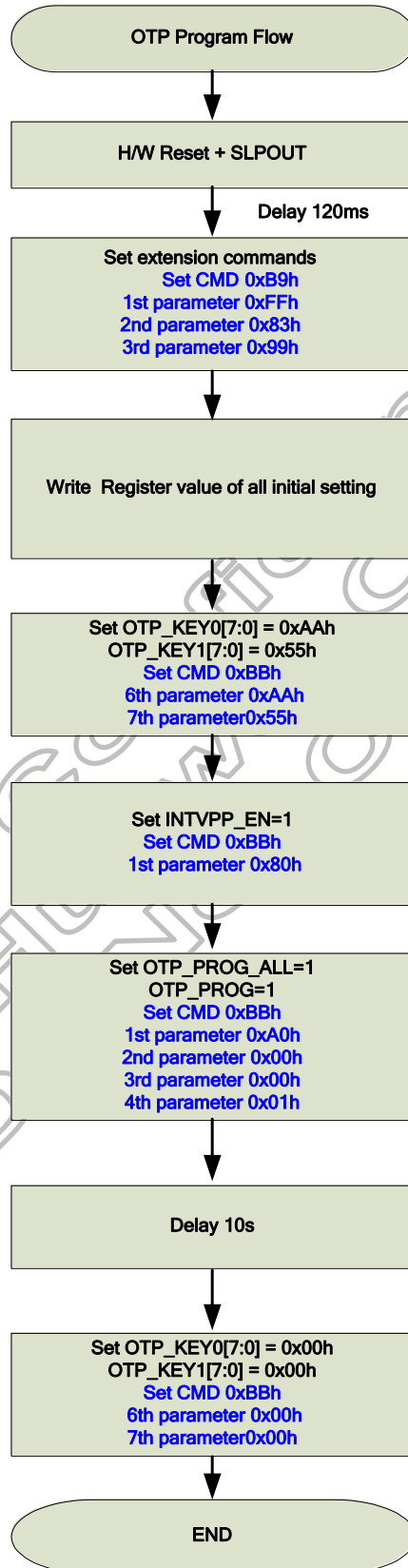
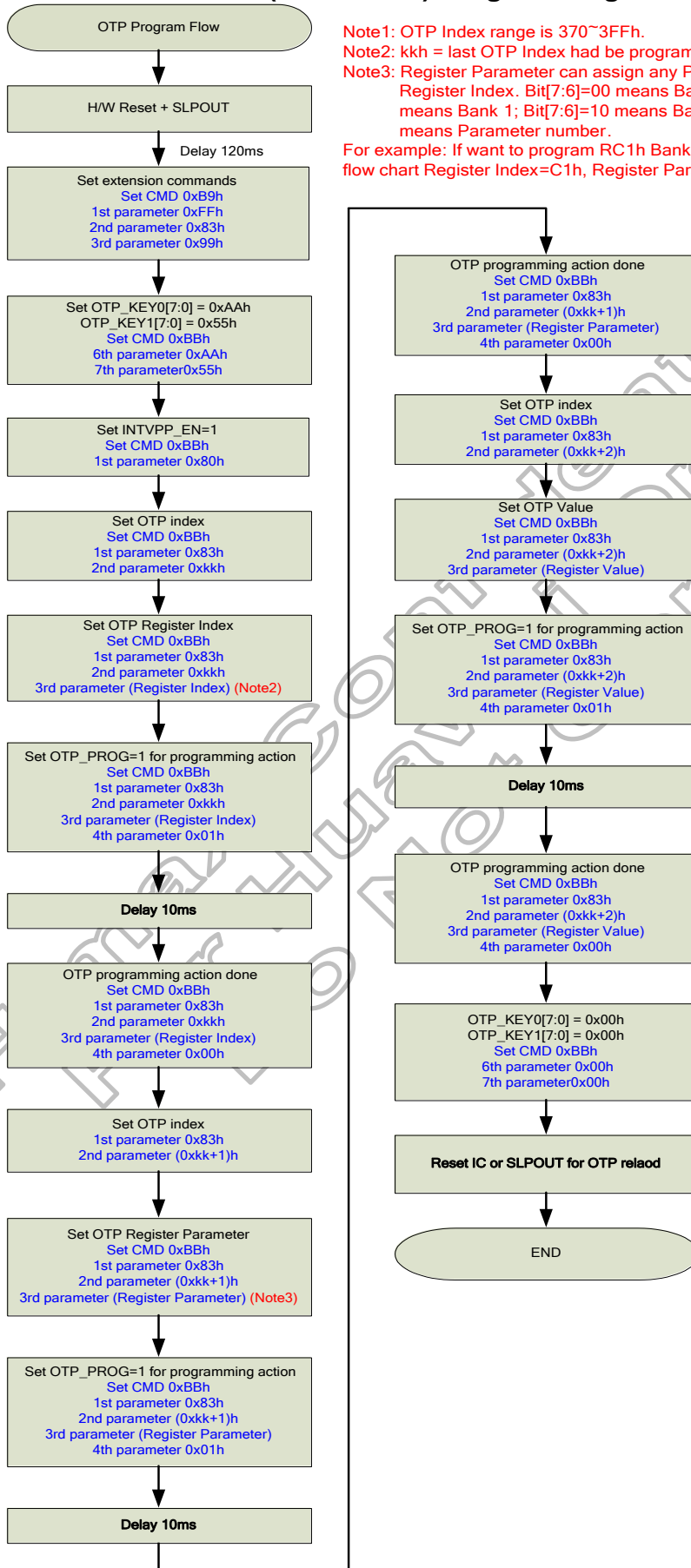


Figure 5.47: OTP programming all Index sequence

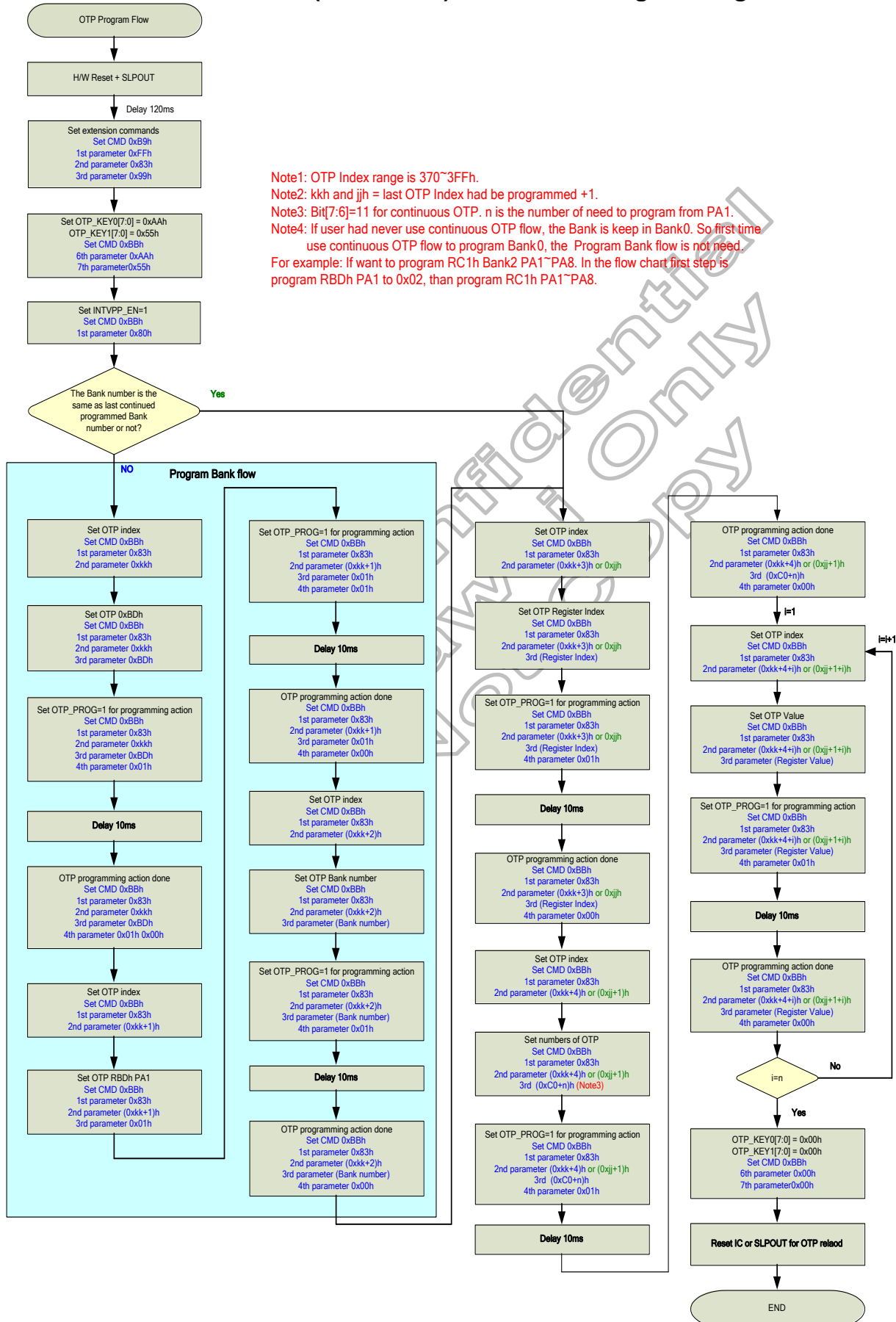
5.15.7 Flexible OTP Index(370h~3FFh) Programming



Note1: OTP Index range is 370~3FFh.
 Note2: kkh = last OTP Index had be programmed +1.
 Note3: Register Parameter can assign any Parameter of Register Index. Bit[7:6]=00 means Bank 0; Bit[7:6]=01 means Bank 1; Bit[7:6]=10 means Bank 2. Bit[5:0] means Parameter number.
 For example: If want to program RC1h Bank1 Parameter 3. In the flow chart Register Index=C1h, Register Parameter=43h.

Figure 5.48: Flexible OTP programming sequence

5.15.8 Flexible OTP Index(370h~3FFh) Continuous Programming



Note1: OTP Index range is 370~3FFh.
 Note2: kkh and jjh = last OTP Index had be programmed +1.
 Note3: Bit[7:6]=11 for continuous OTP. n is the number of need to program from PA1.
 Note4: If user had never use continuous OTP flow, the Bank is keep in Bank0. So first time use continuous OTP flow to program Bank0, the Program Bank flow is not need.
 For example: If want to program RC1h Bank2 PA1~PA8. In the flow chart first step is program RBDh PA1 to 0x02, than program RC1h PA1~PA8.

Figure 5.49: Flexible OTP continuous programming sequence

5.15.9 OTP read example of OTP Index 00h (ID1)

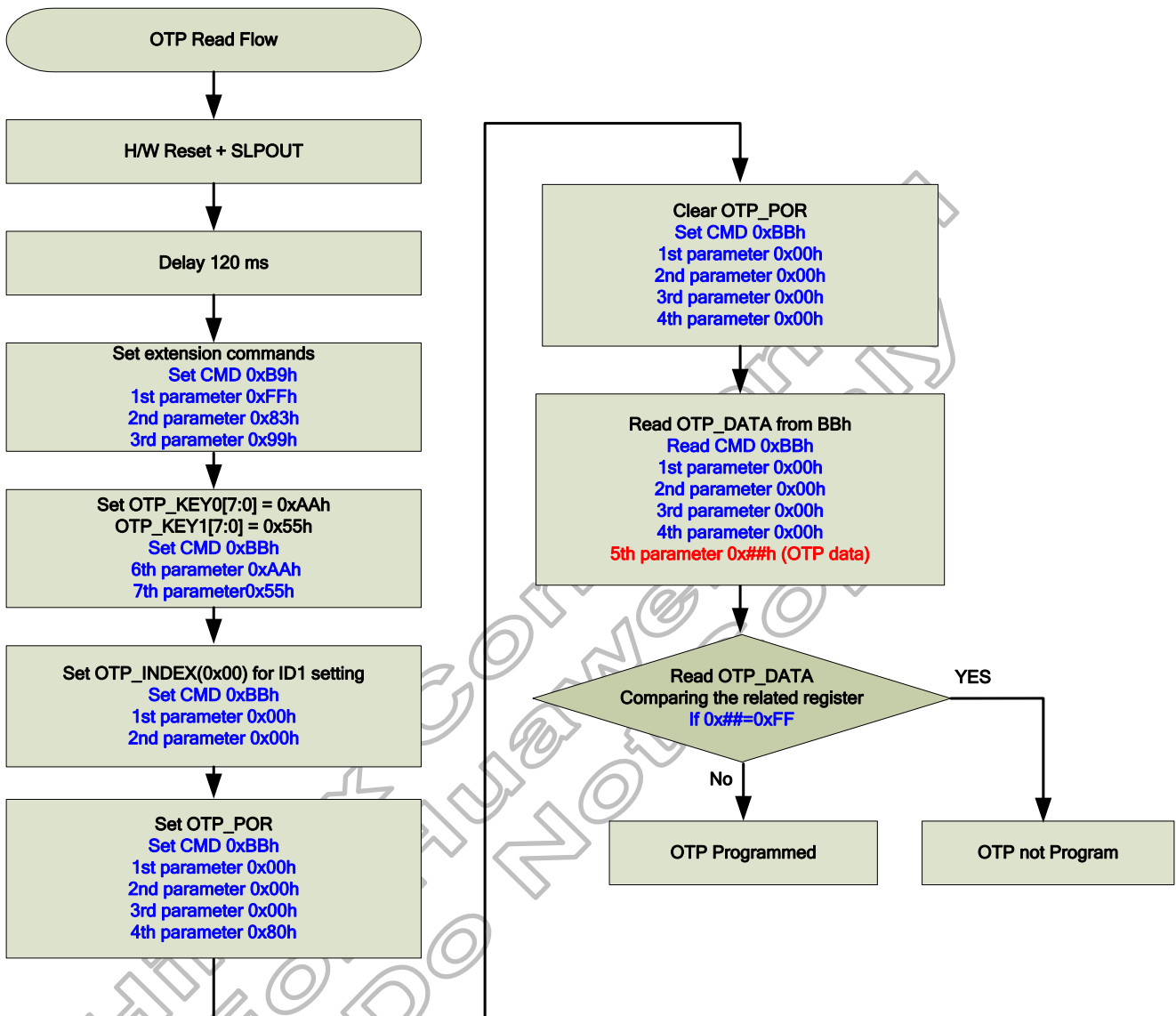


Figure 5.50: OTP read sequence flow of Index 00h

6. Command

6.1 Command list

6.1.1 Standard command

(Hex)	Operation code	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)
00	NOP	0	0	0	0	0	0	0	0	0	No Operation	-
01	SWRESET	0	0	0	0	0	0	0	0	1	Software Reset	-
04	RDDIDIF	0	0	0	0	0	0	1	0	0	Read Display Identification Information	-
		1	ID1[7:0]									83h
		1	ID2[7:0]									99h
05	RDNUMPE	0	0	0	0	0	0	1	0	1	Read Number of DSI Parity Error	0Ch
		1	P[7:0]									-
06	RDRED	0	0	0	0	0	0	1	1	0	Read Red Colour	-
		1	R7	R6	R5	R4	R3	R2	R1	R0		-
07	RDGREEN	0	0	0	0	0	0	1	1	1	Read Green Colour	-
		1	G7	G6	G5	G4	G3	G2	G1	G0		-
08	RDBLUE	0	0	0	0	0	1	0	0	0	Read Blue Colour	-
		1	B7	B6	B5	B4	B3	B2	B1	B0		-
09	RDDST	0	0	0	0	0	1	0	0	1	Read display status	-
		1	D31	D30	D29	0	0	D26	D25	D24		00h
		1	D23	D22	D21	D20	D19	0	D17	D16		71h
		1	0	0	D13	D12	D11	D10	D9	D8		00h
0A	RDDPM	0	0	0	0	0	1	0	1	0	Read display power mode	00h
		1	D7	D6	0	D4	D3	D2	0	0		08h
0B	RDDMADCTL	0	0	0	0	0	1	0	1	1	Read display MADCTL	-
		1	D7	D6	-	-	D3	D2	D1	D0		00h
0C	RDDCOLMOD	0	0	0	0	0	1	1	0	0	Read display pixel format	-
		1	0	D6	D5	D4	0	0	0	0		70h
0D	RDDIM	0	0	0	0	0	1	1	1	0	Read display image mode	-
		1	0	0	D5	D4	D3	D2	D1	D0		00h
0E	RDDSM	0	0	0	0	0	1	1	1	0	Read display signal mode	-
		1	D7	D6	D5	D4	D3	D2	0	D0		00h
0F	RDDSDR	0	0	0	0	0	1	1	1	1	Read display self-diagnostic result	-
		1	D7	D6	D5	D4	0	0	0	0		00h
10	SLPIN	0	0	0	0	1	0	0	0	0	Sleep In	-
11	SLPOUT	0	0	0	0	1	0	0	0	1	Sleep Out	-
13	NORON	0	0	0	0	1	0	0	1	1	Normal display mode on	-
20	INVOFF	0	0	0	1	0	0	0	0	0	Display inversion off	-
21	INVON	0	0	0	1	0	0	0	0	1	Display inversion on	-
22	ALLPOFF	0	0	0	1	0	0	0	1	0	All pixel off (black)	-
23	ALLPON	0	0	0	1	0	0	0	1	1	All pixel on (white)	-
26	GAMSET	0	0	0	1	0	0	1	1	0	Gamma set	-
		1	GC[7:0]									01h
28	DISPOFF	0	0	0	1	0	1	0	0	0	Display off	-
29	DISPON	0	0	0	1	0	1	0	0	1	Display on	-
34	TEOFF	0	0	0	1	1	0	1	0	0	Tearing Effect Line OFF	-
35	TEON	0	0	0	1	1	0	1	0	1	Tearing Effect Line ON	-
		1	X	X	X	X	X	X	X	M		00h
36	MADCTL	0	0	0	1	1	0	1	1	0	Memory access Control	-
		1	D7	D6	X	X	D3	D2	D1	D0		00h
38	IDMOFF	0	0	0	1	1	1	0	0	0	Idle mode off	-
39	IDMON	0	0	0	1	1	1	0	0	1	Idle mode on	-
3A	COLMOD	0	0	0	1	1	1	0	1	0	-	-
		1	X	D6	D5	D4	X	X	X	X	-	70h

(Hex)	Operation Code	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	
44	TESL	0	0	1	0	0	0	1	0	0	Tearing Effect Scan Line number	-	
		1	TELIN[15:8]									00h	
		1	TELIN[7:0]									00h	
45	GETSCAN	0	0	1	0	0	0	1	0	1	Return the current scanline SLN[15:0]	-	
		1	SLN[15:8]									00h	
		1	SLN[7:0]									00h	
51	WRDISBV	0	0	1	0	1	0	0	0	1	Write Display Brightness	-	
		1	DBV[11:8]									00h	
			DBV[7:0]										
52	RDDISBV	0	0	1	0	1	0	0	1	0	Read Display Brightness Value	-	
		1	DBV[7:0]									00h	
53	WRCTRLD	0	0	1	0	1	0	0	1	1	Write CTRL Display	-	
		1	X	X	BCT RL	X	DD	BL	X	X		00h	
54	RDCTRLD	0	0	1	0	1	0	1	0	0	Read Control Value Display	-	
		1	0	0	BCT RL	0	DD	BL	0	0		00h	
55	WRCABC	0	0	1	0	1	0	1	0	1	Write Adaptive Brightness Control	-	
		1	X	X	X	X	X	X	CABC[1:0]			00h	
56	RDCABC	0	0	1	0	1	0	1	1	0	Read Adaptive Brightness Control Content	-	
		1	0	0	0	0	0	0	C1	C0		00h	
5E	WRCABCMB	0	0	1	0	1	1	1	1	0	Write CAB minimum brightness	-	
		1	CMB[7:0]									00h	
5F	RDCABCMB	0	0	1	0	1	1	1	1	1	Read CAB minimum brightness	-	
		1	CMB[7:0]									00h	
68	RDABCSDR	0	0	1	1	0	1	0	0	0	Read Automatic Brightness Control Self-Diagnostic Result	-	
		1	D[7:6]		0	0	0	0	0	0		00h	
A1	Read_DDB_start	0	1	0	1	0	0	0	0	1	Read the DDB from the provided location.	-	
		1	xx	xx	xx	xx	xx	xx	xx	xx		-	
		1	xx	xx	xx	xx	xx	xx	xx	xx		-	
		1	xx	xx	xx	xx	xx	xx	xx	xx		-	
A8	Read_DDB_continue	0	1	0	1	0	1	0	0	0	Continue reading the DDB from the last read location.	-	
		1	xx	xx	xx	xx	xx	xx	xx	xx		-	
		1	xx	xx	xx	xx	xx	xx	xx	xx		-	
		1	xx	xx	xx	xx	xx	xx	xx	xx		-	
DA	RDID1	0	1	1	0	1	1	0	1	0	Read ID1	-	
		1	ID1[7:0]									83h	
DB	RDID2	0	1	1	0	1	1	0	1	1	Read ID2	-	
		1	ID2[7:0]									99h	
DC	RDID3	0	1	1	0	1	1	1	0	0	Read ID3	-	
		1	ID3[7:0]									0Ch	

Note: (1) Undefined commands are treated as NOP (00h) command.

6.1.2 User define command list table

User define command list is available only set "SETEXC" command.

(Hex)	Operation Code	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
B1	SETPOWER	0	1	0	1	1	0	0	0	1	-	Set power control
		1	-	-	-	-	-	-	DSTB_OPT	DSTB	00h	Bank0
		1	-	-	-	-	VSP_FB OFF	APP[2:0]		04h		
		1	-	VCI_LDOS[1:0]		VRHP[4:0]		72h				
		1	VPPS[2:0]		VRHN[4:0]		92h					
		1	-	-	-	-	XDK[2:0]	01h				
		1	CLK_O PT2		CLK_O PT1	FS0[3:0]		32h				
		1	FS1[3:0]		FS2[3:0]		33h					
		1	-		BTP[4:0]		11h					
		1	-		BTN[4:0]		11h					
		1	VGHS[7:0]				B5h					
		1	VGLS[7:0]				6Bh					
		1	DT1[1:0]	DT2[1:0]	DCDIV[3:0]		56h					
		1	-	DCS[2:0]		DC[2:0]	73h					
		1	-	DTPS[2:0]		DTP[2:0]	02h					
		1	-	DTNS[3:0]		DTN[2:0]	02h					
		B1	SETPOWER	1	-	APF_EN	GASIOVCC_OP T1[1:0]	-	GASVCI_OPT[2:0]		64h	Bank1
				1	-	GASVSN_OPT[2:0]		-	GASVSP_OPT[2:0]		44h	
				1	-	-	GASVGL_OPT[1:0]	-	GASVGH_OPT[1:0]		11h	
				0	1	0	1	1	0	0	1	
B2	SETDISP	1	-	ZZ_LR	ZZ_EO	ZZ_2PL	-	NW[2:0]		40h	Bank 0	
		1	MUX_SEL	-	-	-	TGS[3:0]		00h			
		1	MESSI_EN	-	-	-	-	-	-	80h		
		1	NL[7:0]				AEh					
		1	BP [7:0]				08h					
		1	FP [7:0]				08h					
		1	RTN[7:0]				5Ah					
		1	-	END_SET	END_SET_0[1:0]		-	INIT_SET	INIT_SET_0[1:0]			00h
		1	-	-	INIT_SET_1[1:0]		-		00h			
		1	-	-	END_SET_1[1:0]		-		00h			
		1	-	-	INIT_S D_SEL	INIT_V COM_S EL	-	-	END_S D_SEL	END_V COM_S EL		00h
		1	FRM_PATTERN_CYCLE[3:0]			DISP_BI ST_EN	FRM_SCAN_CYCLE[2:0]		C0h	Bank 1		
		1	PTN_2ND_NUM[3:0]			PTN_1ST_NUM[3:0]		10h				
		1	PTN_4TH_NUM[3:0]			PTN_3RD_NUM[3:0]		32h				
		1	PTN_6TH_NUM[3:0]			PTN_5TH_NUM[3:0]		54h				
		1	PTN_8TH_NUM[3:0]			PTN_7TH_NUM[3:0]		76h				
		1	PTN_10TH_NUM[3:0]			PTN_9TH_NUM[3:0]		98h				
		1	PTN_12TH_NUM[3:0]			PTN_11TH_NUM[3:0]		BAh				
		1	PTN_14TH_NUM[3:0]			PTN_13TH_NUM[3:0]		DCh				
		1	PTN_16TH_NUM[3:0]			PTN_15TH_NUM[3:0]		FEh				

(Hex)	Operation Code	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
B4	SETCYC	0	1	0	1	1	0	1	0	0	-	Set Cycle
		1	GEN_ON[7:0]							00h		
		1	GEN_OFF[7:0]							FFh		
		1	SPON[7:0]							03h		
		1	SPOFF[7:0]							38h		
		1	CON[7:0]							0Ah		
		1	COFF[7:0]							8Dh		
		1	CON1[7:0]							05h		
		1	COFF1[7:0]							36h		
		1	N_t1[7:0]							00h		
		1	N_t2[7:0]							18h		
		1	N_t3[7:0]							02h		
		1	N_t4[7:0]							02h		
		1	N_t5[7:0]							2Ch		
		1	N_t6[7:0]							02h		
		1	N_t7[7:0]							02h		
		1	N_t8[7:0]							04h		
		1	N_t9[7:0]							04h		
		1	SAP1_P[3:0]				SAP1_N[3:0]				22h	
		1	-				SAP2[2:0]				03h	
		1	-				EQT[3:0]				00h	
		1	N_t10[7:0]							00h		
		1	SON[7:0]							00h		
		1	SOFF[7:0]							FFh		
		1	DX2_TON[7:0]							3Ah		
		1	SPON_MPU[7:0]							03h		
		1	SPOFF_MPU[7:0]							38h		
		1	CON_MPU[7:0]							0Ah		
		1	COFF_MPU[7:0]							8Dh		
		1	CON1_MPU[7:0]							05h		
		1	COFF1_MPU[7:0]							36h		
		1	N_t1_MPU[7:0]							00h		
		1	N_t2_MPU[7:0]							18h		
		1	N_t3_MPU[7:0]							02h		
		1	N_t4_MPU[7:0]							02h		
		1	N_t5_MPU[7:0]							00h		
		1	N_t6_MPU[7:0]							2Ch		
		1	N_t7_MPU[7:0]							02h		
		1	N_t8_MPU[7:0]							04h		
		1	N_t9_MPU[7:0]							04h		
1	-				EQT_MPU[3:0]				05h			
1	N_t10_MPU[7:0]							00h				
1	SON_MPU[7:0]							10h				
1	SOFF_MPU[7:0]							75h				
1	DX2_TOFF[7:0]							3Ah				
1	-				DX2_E	-	-	-	-	00h		
B6	SETVCOM	0	1	0	1	1	0	1	1	0	-	Set VCOM Voltage
		1	VCMC_F[7:0]							C8h		
		1	VCMC_B[7:0]							C8h		
		1	VCOM_TIMES[2:0]			-	-	-	VCMC_B8	VCMC_F8	E0h	
B7	SETTE	0	1	0	1	1	0	1	1	1	-	Set TE function
		1	-	TEI[3:0]				TEP[10:8]				
		1	TEP[7:0]							00h		
B9	SETEXTC	0	1	0	1	1	1	0	0	1	-	Set extended command
		1	EXTC1[7:0]							00h		
		1	EXTC2[7:0]							00h		
		1	EXTC3[7:0]							00h		

(Hex)	Operation Code	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function	
BA	SETRMIPI	0	1	0	1	1	1	0	1	0	-	Set MIPI Control	
		1	-	DSSETUP0[6:0]									63h
		1	DSSETUP1[7:0]								03h		
BB	SETOTP	0	1	0	1	1	1	0	1	1	-	Set OTP	
		1	INTVP_P_EN	-	OTP_PR OG_ALL	-	-	-	OTP_INDEX[9:8]				00h
		1	OTP_INDEX[7:0]								00h		
		1	OTP_DATA[7:0]								00h		
		1	OTP_P OR	OTP_P WE	OTP_P WR_SE L	OTP_PTM[2:0]			OTP_TE ST	OTP_PR OG	00h		
		1	OTP_DATA_READ[7:0]								00h		
		1	OTP_KEY0[7:0]								00h		
		1	OTP_KEY1[7:0]								00h		
BD	SETBANK	0	1	0	1	1	1	1	0	1	-	Set Register Bank	
		1	-	-	-	-	-	-	BANK_INDEX[1:0]		00h		
C1	SETDGC	0	1	1	0	0	0	0	0	1	-	Set DGC	
		1	-	-	-	DGC_P N	-	-	-	DGC_E N	00h		
		1	R_GAMMA0[9:2]								-		
		1	R_GAMMA1[9:2]								-		
		1	R_GAMMA2[9:2]								-		
		1	R_GAMMA3[9:2]								-		
		1	R_GAMMA4[9:2]								-		
		1	R_GAMMA5[9:2]								-		
		1	R_GAMMA6[9:2]								-		
		1	R_GAMMA7[9:2]								-		
		1	R_GAMMA8[9:2]								-		
		1	R_GAMMA9[9:2]								-		
		1	R_GAMMA10[9:2]								-		
		1	R_GAMMA11[9:2]								-		
		1	R_GAMMA12[9:2]								-		
		1	R_GAMMA13[9:2]								-		
		1	R_GAMMA14[9:2]								-		
		1	R_GAMMA15[9:2]								-		
		1	R_GAMMA16[9:2]								-		
		1	R_GAMMA17[9:2]								-		
		1	R_GAMMA18[9:2]								-		
		1	R_GAMMA19[9:2]								-		
		1	R_GAMMA20[9:2]								-		
		1	R_GAMMA21[9:2]								-		
		1	R_GAMMA22[9:2]								-		
		1	R_GAMMA23[9:2]								-		
		1	R_GAMMA24[9:2]								-		
		1	R_GAMMA25[9:2]								-		
		1	R_GAMMA26[9:2]								-		
		1	R_GAMMA27[9:2]								-		
		1	R_GAMMA28[9:2]								-		
		1	R_GAMMA29[9:2]								-		
		1	R_GAMMA30[9:2]								-		
		1	R_GAMMA31[9:2]								-		
		1	R_GAMMA32[9:2]								-		
1	R_GAMMA0[1:0]	R_GAMMA1[1:0]	R_GAMMA2[1:0]	R_GAMMA3[1:0]							-		
1	R_GAMMA4[1:0]	R_GAMMA5[1:0]	R_GAMMA6[1:0]	R_GAMMA7[1:0]							-		
1	R_GAMMA8[1:0]	R_GAMMA9[1:0]	R_GAMMA10[1:0]	R_GAMMA11[1:0]							-		
1	R_GAMMA12[1:0]	R_GAMMA13[1:0]	R_GAMMA14[1:0]	R_GAMMA15[1:0]							-		
1	R_GAMMA16[1:0]	R_GAMMA17[1:0]	R_GAMMA18[1:0]	R_GAMMA19[1:0]							-		
1	R_GAMMA20[1:0]	R_GAMMA21[1:0]	R_GAMMA22[1:0]	R_GAMMA23[1:0]							-		
1	R_GAMMA24[1:0]	R_GAMMA25[1:0]	R_GAMMA26[1:0]	R_GAMMA27[1:0]							-		
1	R_GAMMA28[1:0]	R_GAMMA29[1:0]	R_GAMMA30[1:0]	R_GAMMA31[1:0]							-		
1	R_GAMMA32[1:0]	-	-	-	-	-	-	-	-	-	40h		
1	G_GAMMA0[9:2]								-				
1	G_GAMMA1[9:2]								-				
1	G_GAMMA2[9:2]								-				
1	G_GAMMA3[9:2]								-				
1	G_GAMMA4[9:2]								-				
1	G_GAMMA5[9:2]								-				
1	G_GAMMA6[9:2]								-				

1									G_GAMMA7[9:2]	-
1									G_GAMMA8[9:2]	-
1									G_GAMMA9[9:2]	-
1									G_GAMMA10[9:2]	-
1									G_GAMMA11[9:2]	-
1									G_GAMMA12[9:2]	-
1									G_GAMMA13[9:2]	-
1									G_GAMMA14[9:2]	-
1									G_GAMMA15[9:2]	-
1									G_GAMMA16[9:2]	-
1									G_GAMMA17[9:2]	-
1									G_GAMMA18[9:2]	-
1									G_GAMMA19[9:2]	-
1									G_GAMMA20[9:2]	-
1									G_GAMMA21[9:2]	-
1									G_GAMMA22[9:2]	-
1									G_GAMMA23[9:2]	-
1									G_GAMMA24[9:2]	-
1									G_GAMMA25[9:2]	-
1									G_GAMMA26[9:2]	-
1									G_GAMMA27[9:2]	-
1									G_GAMMA28[9:2]	-
1									G_GAMMA29[9:2]	-
1									G_GAMMA30[9:2]	-
1									G_GAMMA31[9:2]	-
1									G_GAMMA32[9:2]	-
1	G_GAMMA0[1:0]	G_GAMMA1[1:0]	G_GAMMA2[1:0]	G_GAMMA3[1:0]						-
1	G_GAMMA4[1:0]	G_GAMMA5[1:0]	G_GAMMA6[1:0]	G_GAMMA7[1:0]						-
1	G_GAMMA8[1:0]	G_GAMMA9[1:0]	G_GAMMA10[1:0]	G_GAMMA11[1:0]						-
1	G_GAMMA12[1:0]	G_GAMMA13[1:0]	G_GAMMA14[1:0]	G_GAMMA15[1:0]						-
1	G_GAMMA16[1:0]	G_GAMMA17[1:0]	G_GAMMA18[1:0]	G_GAMMA19[1:0]						-
1	G_GAMMA20[1:0]	G_GAMMA21[1:0]	G_GAMMA22[1:0]	G_GAMMA23[1:0]						-
1	G_GAMMA24[1:0]	G_GAMMA25[1:0]	G_GAMMA26[1:0]	G_GAMMA27[1:0]						-
1	G_GAMMA28[1:0]	G_GAMMA29[1:0]	G_GAMMA30[1:0]	G_GAMMA31[1:0]						-
1	G_GAMMA32[1:0]	-	-	-	-	-	-	-	-	40h
1									B_GAMMA0[5:2]	-
1									B_GAMMA1[5:2]	-
1									B_GAMMA2[6:2]	-
1									B_GAMMA3[6:2]	-
1									B_GAMMA4[7:2]	-
1									B_GAMMA5[7:2]	-
1									B_GAMMA6[7:2]	-
1									B_GAMMA7[7:2]	-
1									B_GAMMA8[8:2]	-
1									B_GAMMA9[8:2]	-
1									B_GAMMA10[8:2]	-
1									B_GAMMA11[8:2]	-
1									B_GAMMA12[8:2]	-
1									B_GAMMA13[8:2]	-
1									B_GAMMA14[8:2]	-
1									B_GAMMA15[8:2]	-
1									B_GAMMA16[9:2]	-
1									B_GAMMA17[9:2]	-
1									B_GAMMA18[9:2]	-
1									B_GAMMA19[9:2]	-
1									B_GAMMA20[8:2]	-
1									B_GAMMA21[8:2]	-
1									B_GAMMA22[8:2]	-
1									B_GAMMA23[8:2]	-
1									B_GAMMA24[8:2]	-
1									B_GAMMA25[8:2]	-
1									B_GAMMA26[8:2]	-
1									B_GAMMA27[7:2]	-
1									B_GAMMA28[7:2]	-
1									B_GAMMA29[7:2]	-
1									B_GAMMA30[7:2]	-
1									B_GAMMA31[6:2]	-
1									B_GAMMA32[5:2]	-
1	B_GAMMA0[1:0]	B_GAMMA1[1:0]	B_GAMMA2[1:0]	B_GAMMA3[1:0]						-
1	B_GAMMA4[1:0]	B_GAMMA5[1:0]	B_GAMMA6[1:0]	B_GAMMA7[1:0]						-
1	B_GAMMA8[1:0]	B_GAMMA9[1:0]	B_GAMMA10[1:0]	B_GAMMA11[1:0]						-
1	B_GAMMA12[1:0]	B_GAMMA13[1:0]	B_GAMMA14[1:0]	B_GAMMA15[1:0]						-

Bank2

		1	B_GAMMA16[1:0]	B_GAMMA17[1:0]	B_GAMMA18[1:0]	B_GAMMA19[1:0]	-				
		1	B_GAMMA20[1:0]	B_GAMMA21[1:0]	B_GAMMA22[1:0]	B_GAMMA23[1:0]	-				
		1	B_GAMMA24[1:0]	B_GAMMA25[1:0]	B_GAMMA26[1:0]	B_GAMMA27[1:0]	-				
		1	B_GAMMA28[1:0]	B_GAMMA29[1:0]	B_GAMMA30[1:0]	B_GAMMA31[1:0]	-				
		1	B_GAMMA32[1:0]	-	-	-	-	-	40h		
C2	SETDISMO	0	1	1	0	0	0	1	0	-	Set DISMO
		1	-	-	-	-	RM	-	DM[1:0]	03h	
C3	SETID	0	1	1	0	0	0	1	1	-	Set ID
		1	ID1[7:0]							83h	
		1	ID2[7:0]							99h	
		1	ID3[7:0]							0Ch	
		1	ID4[7:0]							00h	
		1	ID_TIMES[2:0]	-	-	-	-	-	-	E0h	
C4	SETDDB	0	1	1	0	0	0	1	0	0	Set DDB
		1	DDB1[7:0]							00h	
		1	DDB2[7:0]							00h	
		1	DDB3[7:0]							00h	
		1	DDB4[7:0]							00h	
		1	DDB5[7:0]							00h	
		1	DDB6[7:0]							00h	
C9	SETCABC	0	1	1	0	0	1	0	0	1	Set CAB Control
		1	-	-	-	-	SLR_E N	BC_CT RL_EN	INVPUL S	SEL_BL DUTY	03h
		1	PWM_PERIOD[15:8]							00h	
		1	PWM_PERIOD[7:0]							2Eh	
CB	SETCLOCK	0	1	1	0	0	1	0	1	1	Set Oscillator
		1	-	-	-	-	-	-	UADJ[4:0]	10h	
CC	SETPANEL	0	1	1	0	0	1	1	0	0	Set Panel
		1	-	-	-	-	SS_PA NEL	GS_PA NEL	REV_PA NE	BGR_PA NEL	00h
D3	SETGIPO	0	1	1	0	1	0	0	1	1	Set GIP Option0
		1	-	-	GIP_EQ_OPT[1:0]	-	-	-	EQ_DELAY_HSY NC[1:0]	00h	
		1	-	-	-	-	VSEL[1:0]	-	EQ_DISC[1:0]	00h	
		1	EQ_DELAY_ON1[7:0]							00h	
		1	EQ_DELAY_OFF1[7:0]							00h	
		1	GTO[7:0]							00h	
		1	GNO[7:0]							00h	
		1	USER_GIP_GATE[7:0]							08h	
		1	USER_GIP_GATE1[7:0]							08h	
		1	SHR0_3[3:0]			SHR0_2[3:0]				32h	
		1	SHR0_1[3:0]			SHR0[11:8]				10h	
		1	SHR0[7:0]							00h	
		1	-	-	-	-	-	-	SHR0_GS[11:8]	00h	
		1	SHR0_GS[7:0]							02h	
		1	SHR1_3[3:0]			SHR1_2[3:0]				32h	
		1	SHR1_1[3:0]			SHR1[11:8]				13h	
		1	SHR1[7:0]							C0h	
		1	-	-	-	-	-	-	SHR1_GS[11:8]	00h	
		1	SHR1_GS[7:0]							00h	
		1	SHR2_3[3:0]			SHR2_2[3:0]				32h	
		1	SHR2_1[3:0]			SHR2[11:8]				10h	
		1	SHR2[7:0]							08h	
		1	-	-	-	-	-	-	SHR2_GS[11:8]	00h	
		1	SHR2_GS[7:0]							00h	
		1	SHP[3:0]			SCP[3:0]				4Bh	
		1	SHP2[3:0]			SHP1[3:0]				00h	
		1	CHR0[7:0]							06h	
		1	CHR0_GS[7:0]							06h	
		1	CHP0[3:0]			CCP0[3:0]				47h	
		1	CHR1[7:0]							04h	
		1	CHR1_GS[7:0]							00h	
		1	CHP1[3:0]			CCP1[3:0]				27h	
		1	vbp_setting[7:0]							00h	
		1	-	vbp_self _learnin g	-	-	-	-	-	00h	
D5	SETGIP1	0	1	1	0	1	0	1	0	1	Set GIP Option1
		1	-	CGTS_L _INV[1]	COS1_L[5:0]					-	
		1	-	CGTS_R _INV[1]	COS1_R[5:0]					-	

		1	-	CGTS_L_INV[2]						COS2_L[5:0]	-	
		1	-	CGTS_R_INV[2]						COS2_R[5:0]	-	
		1	-	CGTS_L_INV[3]						COS3_L[5:0]	-	
		1	-	CGTS_R_INV[3]						COS3_R[5:0]	-	
		1	-	CGTS_L_INV[4]						COS4_L[5:0]	-	
		1	-	CGTS_R_INV[4]						COS4_R[5:0]	-	
		1	-	CGTS_L_INV[5]						COS5_L[5:0]	-	
		1	-	CGTS_R_INV[5]						COS5_R[5:0]	-	
		1	-	CGTS_L_INV[6]						COS6_L[5:0]	-	
		1	-	CGTS_R_INV[6]						COS6_R[5:0]	-	
		1	-	CGTS_L_INV[7]						COS7_L[5:0]	-	
		1	-	CGTS_R_INV[7]						COS7_R[5:0]	-	
		1	-	CGTS_L_INV[8]						COS8_L[5:0]	-	
		1	-	CGTS_R_INV[8]						COS8_R[5:0]	-	
		1	-	CGTS_L_INV[9]						COS9_L[5:0]	-	
		1	-	CGTS_R_INV[9]						COS9_R[5:0]	-	
		1	-	CGTS_L_INV[10]						COS10_L[5:0]	-	
		1	-	CGTS_R_INV[10]						COS10_R[5:0]	-	
		1	-	CGTS_L_INV[11]						COS11_L[5:0]	-	
		1	-	CGTS_R_INV[11]						COS11_R[5:0]	-	
		1	-	CGTS_L_INV[12]						COS12_L[5:0]	-	
		1	-	CGTS_R_INV[12]						COS12_R[5:0]	-	
		1	-	CGTS_L_INV[13]						COS13_L[5:0]	-	
		1	-	CGTS_R_INV[13]						COS13_R[5:0]	-	
		1	-	CGTS_L_INV[14]						COS14_L[5:0]	-	
		1	-	CGTS_R_INV[14]						COS14_R[5:0]	-	
		1	-	CGTS_L_INV[15]						COS15_L[5:0]	-	
		1	-	CGTS_R_INV[15]						COS15_R[5:0]	-	
		1	-	CGTS_L_INV[16]						COS16_L[5:0]	-	
		1	-	CGTS_R_INV[16]						COS16_R[5:0]	-	
		0	1	1	0	1	0	1	1	0	-	
D6	SETGIP2	1	-	CGOUT_L_HIZ_IN[1]						COS1_L_GS[5:0]	-	Set GIP Option2
		1	-	CGOUT_R_HIZ_IN[1]						COS1_R_GS[5:0]	-	
		1	-	CGOUT_L_HIZ_IN[2]						COS2_L_GS[5:0]	-	
		1	-	CGOUT_R_HIZ_IN[2]						COS2_R_GS[5:0]	-	
		1	-	CGOUT_L_HIZ_IN[3]						COS3_L_GS[5:0]	-	
		1	-	CGOUT_R_HIZ_IN[3]						COS3_R_GS[5:0]	-	
		1	-	CGOUT_L_HIZ_IN[4]						COS4_L_GS[5:0]	-	
		1	-	CGOUT_R_HIZ_IN[4]						COS4_R_GS[5:0]	-	

		1	-	CGOUT_L_HIZ_IN [5]	COS5_L_GS[5:0]				-			
		1	-	CGOUT_R_HIZ_IN [5]	COS5_R_GS[5:0]				-			
		1	-	CGOUT_L_HIZ_IN [6]	COS6_L_GS[5:0]				-			
		1	-	CGOUT_R_HIZ_IN [6]	COS6_R_GS[5:0]				-			
		1	-	CGOUT_L_HIZ_IN [7]	COS7_L_GS[5:0]				-			
		1	-	CGOUT_R_HIZ_IN [7]	COS7_R_GS[5:0]				-			
		1	-	CGOUT_L_HIZ_IN [8]	COS8_L_GS[5:0]				-			
		1	-	CGOUT_R_HIZ_IN [8]	COS8_R_GS[5:0]				-			
		1	-	CGOUT_L_HIZ_IN [9]	COS9_L_GS[5:0]				-			
		1	-	CGOUT_R_HIZ_IN [9]	COS9_R_GS[5:0]				-			
		1	-	CGOUT_L_HIZ_IN [10]	COS10_L_GS[5:0]				-			
		1	-	CGOUT_R_HIZ_IN [10]	COS10_R_GS[5:0]				-			
		1	-	CGOUT_L_HIZ_IN [11]	COS11_L_GS[5:0]				-			
		1	-	CGOUT_R_HIZ_IN [11]	COS11_R_GS[5:0]				-			
		1	-	CGOUT_L_HIZ_IN [12]	COS12_L_GS[5:0]				-			
		1	-	CGOUT_R_HIZ_IN [12]	COS12_R_GS[5:0]				-			
		1	-	CGOUT_L_HIZ_IN [13]	COS13_L_GS[5:0]				-			
		1	-	CGOUT_R_HIZ_IN [13]	COS13_R_GS[5:0]				-			
		1	-	CGOUT_L_HIZ_IN [14]	COS14_L_GS[5:0]				-			
		1	-	CGOUT_R_HIZ_IN [14]	COS14_R_GS[5:0]				-			
		1	-	CGOUT_L_HIZ_IN [15]	COS15_L_GS[5:0]				-			
		1	-	CGOUT_R_HIZ_IN [15]	COS15_R_GS[5:0]				-			
		1	-	CGOUT_L_HIZ_IN [16]	COS16_L_GS[5:0]				-			
		1	-	CGOUT_R_HIZ_IN [16]	COS16_R_GS[5:0]				-			
D8	SETGIP_3	0	1	1	0	1	1	0	0	0	-	
		1		INIT_0_SEL_CG OUT1_L[1:0]	INIT_0_SEL_CGO UT2_L[1:0]	INIT_0_SEL_CG OUT3_L[1:0]	INIT_0_SEL_CG OUT4_L[1:0]				-	
		1		INIT_0_SEL_CG OUT5_L[1:0]	INIT_0_SEL_CGO UT6_L[1:0]	INIT_0_SEL_CG OUT7_L[1:0]	INIT_0_SEL_CG OUT8_L[1:0]				-	
		1		INIT_0_SEL_CG OUT9_L[1:0]	INIT_0_SEL_CGO UT10_L[1:0]	INIT_0_SEL_CG OUT11_L[1:0]	INIT_0_SEL_CG OUT12_L[1:0]				-	Set GIP Option3
		1		INIT_0_SEL_CG OUT13_L[1:0]	INIT_0_SEL_CGO UT14_L[1:0]	INIT_0_SEL_CG OUT15_L[1:0]	INIT_0_SEL_CG OUT16_L[1:0]				-	
		1		INIT_0_SEL_CG OUT1_R[1:0]	INIT_0_SEL_CGO UT2_R[1:0]	INIT_0_SEL_CG OUT3_R[1:0]	INIT_0_SEL_CG OUT4_R[1:0]				-	

		1	INIT_0_SEL_CG OUT5_R[1:0]	INIT_0_SEL_CGO UT6_R[1:0]	INIT_0_SEL_CG OUT7_R[1:0]	INIT_0_SEL_CG OUT8_R[1:0]	-					
		1	INIT_0_SEL_CG OUT9_R[1:0]	INIT_0_SEL_CGO UT10_R[1:0]	INIT_0_SEL_CG OUT11_R[1:0]	INIT_0_SEL_CG OUT12_R[1:0]	-					
		1	INIT_0_SEL_CG OUT13_R[1:0]	INIT_0_SEL_CGO UT14_R[1:0]	INIT_0_SEL_CG OUT15_R[1:0]	INIT_0_SEL_CG OUT16_R[1:0]	-					
		1	INIT_1_SEL_CG OUT1_L[1:0]	INIT_1_SEL_CGO UT2_L[1:0]	INIT_1_SEL_CG OUT3_L[1:0]	INIT_1_SEL_CG OUT4_L[1:0]	-					
		1	INIT_1_SEL_CG OUT5_L[1:0]	INIT_1_SEL_CGO UT6_L[1:0]	INIT_1_SEL_CG OUT7_L[1:0]	INIT_1_SEL_CG OUT8_L[1:0]	-					
		1	INIT_1_SEL_CG OUT9_L[1:0]	INIT_1_SEL_CGO UT10_L[1:0]	INIT_1_SEL_CG OUT11_L[1:0]	INIT_1_SEL_CG OUT12_L[1:0]	-					
		1	INIT_1_SEL_CG OUT13_L[1:0]	INIT_1_SEL_CGO UT14_L[1:0]	INIT_1_SEL_CG OUT15_L[1:0]	INIT_1_SEL_CG OUT16_L[1:0]	-					
		1	INIT_1_SEL_CG OUT1_R[1:0]	INIT_1_SEL_CGO UT2_R[1:0]	INIT_1_SEL_CG OUT3_R[1:0]	INIT_1_SEL_CG OUT4_R[1:0]	-					
		1	INIT_1_SEL_CG OUT5_R[1:0]	INIT_1_SEL_CGO UT6_R[1:0]	INIT_1_SEL_CG OUT7_R[1:0]	INIT_1_SEL_CG OUT8_R[1:0]	-					
		1	INIT_1_SEL_CG OUT9_R[1:0]	INIT_1_SEL_CGO UT10_R[1:0]	INIT_1_SEL_CG OUT11_R[1:0]	INIT_1_SEL_CG OUT12_R[1:0]	-					
		1	INIT_1_SEL_CG OUT13_R[1:0]	INIT_1_SEL_CGO UT14_R[1:0]	INIT_1_SEL_CG OUT15_R[1:0]	INIT_1_SEL_CG OUT16_R[1:0]	-					
		1	END_0_SEL_CG OUT1_L[1:0]	END_0_SEL_CG OUT2_L[1:0]	END_0_SEL_CG OUT3_L[1:0]	END_0_SEL_CG OUT4_L[1:0]	-					
		1	END_0_SEL_CG OUT5_L[1:0]	END_0_SEL_CG OUT6_L[1:0]	END_0_SEL_CG OUT7_L[1:0]	END_0_SEL_CG OUT8_L[1:0]	-					
		1	END_0_SEL_CG OUT9_L[1:0]	END_0_SEL_CG OUT10_L[1:0]	END_0_SEL_CG OUT11_L[1:0]	END_0_SEL_CG OUT12_L[1:0]	-					
		1	END_0_SEL_CG OUT13_L[1:0]	END_0_SEL_CG OUT14_L[1:0]	END_0_SEL_CG OUT15_L[1:0]	END_0_SEL_CG OUT16_L[1:0]	-					
		1	END_0_SEL_CG OUT1_R[1:0]	END_0_SEL_CG OUT2_R[1:0]	END_0_SEL_CG OUT3_R[1:0]	END_0_SEL_CG OUT4_R[1:0]	-					
		1	END_0_SEL_CG OUT5_R[1:0]	END_0_SEL_CG OUT6_R[1:0]	END_0_SEL_CG OUT7_R[1:0]	END_0_SEL_CG OUT8_R[1:0]	-					
		1	END_0_SEL_CG OUT9_R[1:0]	END_0_SEL_CG OUT10_R[1:0]	END_0_SEL_CG OUT11_R[1:0]	END_0_SEL_CG OUT12_R[1:0]	-					
		1	END_0_SEL_CG OUT13_R[1:0]	END_0_SEL_CG OUT14_R[1:0]	END_0_SEL_CG OUT15_R[1:0]	END_0_SEL_CG OUT16_R[1:0]	-					
		1	END_1_SEL_CG OUT1_L[1:0]	END_1_SEL_CG OUT2_L[1:0]	END_1_SEL_CG OUT3_L[1:0]	END_1_SEL_CG OUT4_L[1:0]	-					
		1	END_1_SEL_CG OUT5_L[1:0]	END_1_SEL_CG OUT6_L[1:0]	END_1_SEL_CG OUT7_L[1:0]	END_1_SEL_CG OUT8_L[1:0]	-					
		1	END_1_SEL_CG OUT9_L[1:0]	END_1_SEL_CG OUT10_L[1:0]	END_1_SEL_CG OUT11_L[1:0]	END_1_SEL_CG OUT12_L[1:0]	-					
		1	END_1_SEL_CG OUT13_L[1:0]	END_1_SEL_CG OUT14_L[1:0]	END_1_SEL_CG OUT15_L[1:0]	END_1_SEL_CG OUT16_L[1:0]	-					
		1	END_1_SEL_CG OUT1_R[1:0]	END_1_SEL_CG OUT2_R[1:0]	END_1_SEL_CG OUT3_R[1:0]	END_1_SEL_CG OUT4_R[1:0]	-					
		1	END_1SEL_CG OUT5_R[1:0]	END_1_SEL_CG OUT6_R[1:0]	END_1_SEL_CG OUT7_R[1:0]	END_1_SEL_CG OUT8_R[1:0]	-					
		1	END_1_SEL_CG OUT9_R[1:0]	END_1_SEL_CG OUT10_R[1:0]	END_1_SEL_CG OUT11_R[1:0]	END_1_SEL_CG OUT12_R[1:0]	-					
		1	END_1_SEL_CG OUT13_R[1:0]	END_1_SEL_CG OUT14_R[1:0]	END_1_SEL_CG OUT15_R[1:0]	END_1_SEL_CG OUT16_R[1:0]	-					
		1	GAS_0_SEL_CG OUT1_L[1:0]	GAS_0_SEL_CG OUT2_L[1:0]	GAS_0_SEL_CG OUT3_L[1:0]	GAS_0_SEL_CG OUT4_L[1:0]	00h					
		1	GAS_0_SEL_CG OUT5_L[1:0]	GAS_0_SEL_CG OUT6_L[1:0]	GAS_0_SEL_CG OUT7_L[1:0]	GAS_0_SEL_CG OUT8_L[1:0]	00h					
		1	GAS_0_SEL_CG OUT9_L[1:0]	GAS_0_SEL_CG OUT10_L[1:0]	GAS_0_SEL_CG OUT11_L[1:0]	GAS_0_SEL_CG OUT12_L[1:0]	00h					
		1	GAS_0_SEL_CG OUT13_L[1:0]	GAS_0_SEL_CG OUT14_L[1:0]	GAS_0_SEL_CG OUT15_L[1:0]	GAS_0_SEL_CG OUT16_L[1:0]	00h					
		1	GAS_0_SEL_CG OUT1_R[1:0]	GAS_0_SEL_CG OUT2_R[1:0]	GAS_0_SEL_CG OUT3_R[1:0]	GAS_0_SEL_CG OUT4_R[1:0]	00h					
		1	GAS_0_SEL_CG OUT5_R[1:0]	GAS_0_SEL_CG OUT6_R[1:0]	GAS_0_SEL_CG OUT7_R[1:0]	GAS_0_SEL_CG OUT8_R[1:0]	00h					
		1	GAS_0_SEL_CG OUT9_R[1:0]	GAS_0_SEL_CG OUT10_R[1:0]	GAS_0_SEL_CG OUT11_R[1:0]	GAS_0_SEL_CG OUT12_R[1:0]	00h					
		1	GAS_0_SEL_CG OUT13_R[1:0]	GAS_0_SEL_CG OUT14_R[1:0]	GAS_0_SEL_CG OUT15_R[1:0]	GAS_0_SEL_CG OUT16_R[1:0]	00h					
D9	SETGPO	0	1	1	0	1	0	0	1	-		
		1	ESD_D ET							TE_GPO[3:0]	00h	Set GPO

		1	ESD_DET_DSIS_PD							TE1_GPO[3:0]	01h	
		1	EXT_PWR_CTRL							CABC_GPO[3:0]	02h	
		1	-							SDO_GPO[3:0]	07h	
DD	SETSCL	1	-	-	-	-	-	-	SCALIN_G_TYP_E	SCALIN_G_EN	00h	Set Scaling
		0	1	1	0	1	1	1	1	0	-	Set DGC
		1								R_N_GAMMA0[9:2]	-	
		1								R_N_GAMMA1[9:2]	-	
		1								R_N_GAMMA2[9:2]	-	
		1								R_N_GAMMA3[9:2]	-	
		1								R_N_GAMMA4[9:2]	-	
		1								R_N_GAMMA5[9:2]	-	
		1								R_N_GAMMA6[9:2]	-	
		1								R_N_GAMMA7[9:2]	-	
		1								R_N_GAMMA8[9:2]	-	
		1								R_N_GAMMA9[9:2]	-	
		1								R_N_GAMMA10[9:2]	-	
		1								R_N_GAMMA11[9:2]	-	
		1								R_N_GAMMA12[9:2]	-	
		1								R_N_GAMMA13[9:2]	-	
		1								R_N_GAMMA14[9:2]	-	
		1								R_N_GAMMA15[9:2]	-	
		1								R_N_GAMMA16[9:2]	-	
		1								R_N_GAMMA17[9:2]	-	
		1								R_N_GAMMA18[9:2]	-	
		1								R_N_GAMMA19[9:2]	-	
		1								R_N_GAMMA20[9:2]	-	
		1								R_N_GAMMA21[9:2]	-	
		1								R_N_GAMMA22[9:2]	-	
		1								R_N_GAMMA23[9:2]	-	
		1								R_N_GAMMA24[9:2]	-	
		1								R_N_GAMMA25[9:2]	-	
		1								R_N_GAMMA26[9:2]	-	
		1								R_N_GAMMA27[9:2]	-	
		1								R_N_GAMMA28[9:2]	-	
		1								R_N_GAMMA29[9:2]	-	
		1								R_N_GAMMA30[9:2]	-	
		1								R_N_GAMMA31[9:2]	-	
		1								R_N_GAMMA32[9:2]	-	
		1	R_N_GAMMA0[1:0]	R_N_GAMMA1[1:0]	R_N_GAMMA2[1:0]	R_N_GAMMA3[1:0]					-	
		1	R_N_GAMMA4[1:0]	R_N_GAMMA5[1:0]	R_N_GAMMA6[1:0]	R_N_GAMMA7[1:0]					-	
		1	R_N_GAMMA8[1:0]	R_N_GAMMA9[1:0]	R_N_GAMMA10[1:0]	R_N_GAMMA11[1:0]					-	
		1	R_N_GAMMA12[1:0]	R_N_GAMMA13[1:0]	R_N_GAMMA14[1:0]	R_N_GAMMA15[1:0]					-	
		1	R_N_GAMMA16[1:0]	R_N_GAMMA17[1:0]	R_N_GAMMA18[1:0]	R_N_GAMMA19[1:0]					-	
		1	R_N_GAMMA20[1:0]	R_N_GAMMA21[1:0]	R_N_GAMMA22[1:0]	R_N_GAMMA23[1:0]					-	
		1	R_N_GAMMA24[1:0]	R_N_GAMMA25[1:0]	R_N_GAMMA26[1:0]	R_N_GAMMA27[1:0]					-	
		1	R_N_GAMMA28[1:0]	R_N_GAMMA29[1:0]	R_N_GAMMA30[1:0]	R_N_GAMMA31[1:0]					-	
		1	R_N_GAMMA32[1:0]	-	-	-	-	-	-	-	40h	
		1								G_N_GAMMA0[9:2]	-	
		1								G_N_GAMMA1[9:2]	-	
		1								G_N_GAMMA2[9:2]	-	
		1								G_N_GAMMA3[9:2]	-	
		1								G_N_GAMMA4[9:2]	-	
		1								G_N_GAMMA5[9:2]	-	
		1								G_N_GAMMA6[9:2]	-	
		1								G_N_GAMMA7[9:2]	-	
		1								G_N_GAMMA8[9:2]	-	
		1								G_N_GAMMA9[9:2]	-	
		1								G_N_GAMMA10[9:2]	-	
		1								G_N_GAMMA11[9:2]	-	

1				G_N_GAMMA12[9:2]				-
1				G_N_GAMMA13[9:2]				-
1				G_N_GAMMA14[9:2]				-
1				G_N_GAMMA15[9:2]				-
1				G_N_GAMMA16[9:2]				-
1				G_N_GAMMA17[9:2]				-
1				G_N_GAMMA18[9:2]				-
1				G_N_GAMMA19[9:2]				-
1				G_N_GAMMA20[9:2]				-
1				G_N_GAMMA21[9:2]				-
1				G_N_GAMMA22[9:2]				-
1				G_N_GAMMA23[9:2]				-
1				G_N_GAMMA24[9:2]				-
1				G_N_GAMMA25[9:2]				-
1				G_N_GAMMA26[9:2]				-
1				G_N_GAMMA27[9:2]				-
1				G_N_GAMMA28[9:2]				-
1				G_N_GAMMA29[9:2]				-
1				G_N_GAMMA30[9:2]				-
1				G_N_GAMMA31[9:2]				-
1				G_N_GAMMA32[9:2]				-
1	G_N_GAMMA0[1:0]	G_N_GAMMA1[1:0]	G_N_GAMMA2[1:0]	G_N_GAMMA3[1:0]				-
1	G_N_GAMMA4[1:0]	G_N_GAMMA5[1:0]	G_N_GAMMA6[1:0]	G_N_GAMMA7[1:0]				-
1	G_N_GAMMA8[1:0]	G_N_GAMMA9[1:0]	G_N_GAMMA10[1:0]	G_N_GAMMA11[1:0]				-
1	G_N_GAMMA12[1:0]	G_N_GAMMA13[1:0]	G_N_GAMMA14[1:0]	G_N_GAMMA15[1:0]				-
1	G_N_GAMMA16[1:0]	G_N_GAMMA17[1:0]	G_N_GAMMA18[1:0]	G_N_GAMMA19[1:0]				-
1	G_N_GAMMA20[1:0]	G_N_GAMMA21[1:0]	G_N_GAMMA22[1:0]	G_N_GAMMA23[1:0]				-
1	G_N_GAMMA24[1:0]	G_N_GAMMA25[1:0]	G_N_GAMMA26[1:0]	G_N_GAMMA27[1:0]				-
1	G_N_GAMMA28[1:0]	G_N_GAMMA29[1:0]	G_N_GAMMA30[1:0]	G_N_GAMMA31[1:0]				-
1	G_N_GAMMA32[1:0]	-	-	-	-	-	-	40h
1				B_N_GAMMA0[5:2]				-
1				B_N_GAMMA1[5:2]				-
1				B_N_GAMMA2[6:2]				-
1				B_N_GAMMA3[6:2]				-
1				B_N_GAMMA4[7:2]				-
1				B_N_GAMMA5[7:2]				-
1				B_N_GAMMA6[7:2]				-
1				B_N_GAMMA7[7:2]				-
1				B_N_GAMMA8[8:2]				-
1				B_N_GAMMA9[8:2]				-
1				B_N_GAMMA10[8:2]				-
1				B_N_GAMMA11[8:2]				-
1				B_N_GAMMA12[8:2]				-
1				B_N_GAMMA13[8:2]				-
1				B_N_GAMMA14[8:2]				-
1				B_N_GAMMA15[8:2]				-
1				B_N_GAMMA16[9:2]				-
1				B_N_GAMMA17[9:2]				-
1				B_N_GAMMA18[9:2]				-
1				B_N_GAMMA19[9:2]				-
1				B_N_GAMMA20[8:2]				-
1				B_N_GAMMA21[8:2]				-
1				B_N_GAMMA22[8:2]				-
1				B_N_GAMMA23[8:2]				-
1				B_N_GAMMA24[8:2]				-
1				B_N_GAMMA25[8:2]				-
1				B_N_GAMMA26[8:2]				-
1				B_N_GAMMA27[7:2]				-
1				B_N_GAMMA28[7:2]				-
1				B_N_GAMMA29[7:2]				-
1				B_N_GAMMA30[7:2]				-
1				B_N_GAMMA31[6:2]				-
1				B_N_GAMMA32[5:2]				-
1	B_N_GAMMA0[1:0]	B_N_GAMMA1[1:0]	B_N_GAMMA2[1:0]	B_N_GAMMA3[1:0]				-

Bank2

		1	B_N_GAMMA4[1:0]	B_N_GAMMA5[1:0]	B_N_GAMMA6[1:0]	B_N_GAMMA7[1:0]	-			
		1	B_N_GAMMA8[1:0]	B_N_GAMMA9[1:0]	B_N_GAMMA10[1:0]	B_N_GAMMA11[1:0]	-			
		1	B_N_GAMMA12[1:0]	B_N_GAMMA13[1:0]	B_N_GAMMA14[1:0]	B_N_GAMMA15[1:0]	-			
		1	B_N_GAMMA16[1:0]	B_N_GAMMA17[1:0]	B_N_GAMMA18[1:0]	B_N_GAMMA19[1:0]	-			
		1	B_N_GAMMA20[1:0]	B_N_GAMMA21[1:0]	B_N_GAMMA22[1:0]	B_N_GAMMA23[1:0]	-			
		1	B_N_GAMMA24[1:0]	B_N_GAMMA25[1:0]	B_N_GAMMA26[1:0]	B_N_GAMMA27[1:0]	-			
		1	B_N_GAMMA28[1:0]	B_N_GAMMA29[1:0]	B_N_GAMMA30[1:0]	B_N_GAMMA31[1:0]	-			
		1	B_N_GAMMA32[1:0]	-	-	-	-	40h		
DF	SET1BPP	0	1	1	0	1	1	1	1	-
		1	-	-	-	-	-	-	NW_I[2:0]	00h
		1	BP_I[7:0]							08h
		1	FP_I[7:0]							08h
		1	RTN_I[7:0]							5Ah
		1	VCMC_F_I[7:0]							FEh
		1	VCMC_B_I[7:0]							FEh
		1	AP_I[2:0]	-	-	-	VCMC_B_I[8]	VCMC_F_I[8]		83h
		1	FS0_I[3:0]			FS1_I[3:0]				23h
		1	FS2_I[3:0]			-	-	-	-	30h
E0	SETGAMMA	0	1	1	1	0	0	0	0	-
		1	-	VHP_0[6:0]						00h
		1	-	VHP_1[6:0]						0Bh
		1	-	VHP_2[6:0]						1Dh
		1	-	VHP_3[6:0]						1Fh
		1	VMP_0[7:0]						57h	
		1	VMP_1[7:0]						6Dh	
		1	VMP_2[7:0]						78h	
		1	VMP_3[7:0]						7Eh	
		1	VMP_4[7:0]						86h	
		1	VMP_5[7:0]						92h	
		1	VMP_6[7:0]						98h	
		1	VMP_7[7:0]						9Fh	
		1	VMP_8[7:0]						A9h	
		1	VMP_9[7:0]						B9h	
		1	VMP_10[7:0]						BEh	
		1	VMP_11[7:0]						BDh	
		1	VMP_12[7:0]						C4h	
		1	VMP_13[7:0]						CEh	
		1	VMP_14[7:0]						D3h	
		1	VMP_15[7:0]						DCh	
		1	VMP_16[7:0]						CCh	
		1	VMP_17[7:0]						D4h	
		1	VMP_18[7:0]						D2h	
		1	-	VLP_0[6:0]						67h
		1	-	VLP_1[6:0]						60h
		1	-	VLP_2[6:0]						6Ah
		1	-	VLP_3[6:0]						77h
		1	-	VHN_0[6:0]						00h
		1	-	VHN_1[6:0]						0Bh
		1	-	VHN_2[6:0]						1Dh
		1	-	VHN_3[6:0]						1Fh
		1	VMN_0[7:0]						57h	
		1	VMN_1[7:0]						6Dh	
		1	VMN_2[7:0]						78h	
		1	VMN_3[7:0]						7Eh	
		1	VMN_4[7:0]						86h	
		1	VMN_5[7:0]						92h	
		1	VMN_6[7:0]						98h	
		1	VMN_7[7:0]						9Fh	
		1	VMN_8[7:0]						A9h	
		1	VMN_9[7:0]						B9h	
1	VMN_10[7:0]						BEh			
1	VMN_11[7:0]						BDh			
1	VMN_12[7:0]						C4h			
1	VMN_13[7:0]						CEh			

		1	VMN_14[7:0]							D3h			
		1	VMN_15[7:0]							DCh			
		1	VMN_16[7:0]							CCh			
		1	VMN_17[7:0]							D4h			
		1	VMN_18[7:0]							57h			
		1	-	VLN_0[6:0]						D2h			
		1	-	VLN_1[6:0]						67h			
		1	-	VLN_2[6:0]						60h			
		0	-	VLN_3[6:0]						6Ah			
E4	SETCHEMODE	0	1	1	1	0	0	1	0	0	-	Set color enhancement mode	
		1	-	-	-	-	-	-	-	-	DYN_CEH_EN		01h
		1	HUE_MODE[1:0]		SE_MODE[1:0]		BE_MODE[1:0]		CE_MODE[1:0]				00h
E8	SETI2C_SA	0	1	1	1	0	1	0	0	0	-	Set I2C slave address	
		1	-	I2C_SA[6:0]							00h		
E9	SET_SP_CMD	0	1	1	1	0	1	0	0	0	-	Set SP Command	
		1	FORCE_OPT	RAND_WR_SERIAL_EN	RAND_WR_CNT[5:0]								3Fh
FD	SETCNCN/GETCNCN	0	1	1	1	1	1	1	0	1	-	Set/Get Continue Command	
		1	WR_CMD_CN[7:0]								-		
FE	SET SPIREAD INDEX	0	1	1	1	1	1	1	1	0	-	SET SPI read Command Address	
		1	CMD_ADD[7:0]								-		
FF	GETSPIREAD	0	1	1	1	1	1	1	1	1	-	Read SPI Command Data	
		1	CMD_DATA1[7:0]								-		
		1	:								-		
		1	CMD_DATAN[7:0]								-		

6.2 Command description

6.2.1 NOP: No operation (00h)

00H	NOP (No Operation)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER									
Description	This command is an empty command; it does not have any effect on the display module.									
Restriction	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	N/A									
Flow Chart	-									

Himax Confidential
Do Not Copy

6.2.2 SWRESET: Software reset (01h)

01H	SWRESET (Software Reset)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	0	0	0	0	1	01
Parameter	NO PARAMETER									
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description)									
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence. The host processor needs continuing to send PCLK, HSYNC, VSYNC and DE signals to HX8399-C for two frames after this command is sent.									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	N/A									
Flow Chart	<pre> graph TD A[SWRESET] --> B[Display whole blank screen] B --> C[Set Commands to S/W Default Value] C --> D[Sleep In Mode] </pre> <p>Legend</p> <ul style="list-style-type: none"> Red and Blue: Parameter Display: Display Action: Action Mode: Mode Sequential transfer: Sequential transfer 									

6.2.3 RDDIDIF: Read display identification information (04h)

04H	RDDIDIF (Read Display Identification Information)										
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	0	0	0	0	0	1	0	0	04	
1 st parameter	1	ID1[7:0]									-
2 nd parameter	1	ID2[7:0]									-
3 rd parameter	1	ID3[7:0]									-
Description	This read byte returns 24-bit display identification information. The 1 st Parameter identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX. The 2 nd Parameter has 2 purposes. Bit7 (MSB) defines the type of panel. 0=Driver (STN B/W), 1=Module (Colour). Bits 6...0 are used to track the LCD module/driver version. It is defined by display supplier and it changes each time a revision is made to the display, material or construction specifications. See Table:										
	ID Byte Value V[7:0]		Version				Changes				
	80h		-				-				
	81h		-				-				
	82h		-				-				
	83h		-				-				
	84h		-				-				
	85h		-				-				
The 3 rd parameter identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.											
Restriction	-										
Register Availability	Status					Availability					
	Normal Mode On, Idle Mode Off, Sleep Out					Yes					
	Normal Mode On, Idle Mode On, Sleep Out					Yes					
	Sleep In or Booster Off					Yes					
Default	Status					Default Value					
	Power On Sequence					OTP Value					
	S/W Reset					No change					
	H/W Reset					OTP Value					
Flow Chart	Serial I/F Mode Host RDDIDIF (04h) Driver Send ID1[7:0] Send ID2[7:0] Send ID3[7:0]					Legend Command Parameter Display Action Mode Sequential transfer					

6.2.4 RDNUMPE: Read number of the errors on DSI (05h)

05H	RDNUMPE (Read Number of the Errors on DSI)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	0	0	1	0	1	05
1 st parameter	1	P7	P6	P5	P4	P3	P2	P1	P0	00
Description	The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below. P[6:0] bits are telling a number of the errors. P[7] is set to '1' if there is overflow with P[6:0] bits. P[7:0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (The read function is completed).									
Restriction	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart										

6.2.5 Get_red_channel (06h)

06H	RDRED (Read Red Colour)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	0	0	1	1	0	06
1 st parameter	1	P7	P6	P5	P4	P3	P2	P1	P0	00
Description	The first parameter is telling red colour value of the first pixel of the frame when there is used DPI I/F. 16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to '0'. 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to '0'. 24 bit format: R7 is MSB and R0 is LSB.									
Restriction	-									
Register Availability	Status							Availability		
	Normal Mode On, Idle Mode Off, Sleep Out							Yes		
	Normal Mode On, Idle Mode On, Sleep Out							Yes		
	Sleep In or Booster Off							Yes		
Default	Status							Default Value		
	Power On Sequence							00h		
	S/W Reset							00h		
	H/W Reset							00h		
Flow Chart										

6.2.6 Get_green_channel (07h)

06H	RDGREEN (Read Green Colour)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	0	0	1	1	1	07
1 st parameter	1	P7	P6	P5	P4	P3	P2	P1	P0	00
Description	The first parameter is telling blue colour value of the first pixel of the frame when there is used DPI I/F. 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and B0 are set to '0'. 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to '0'. 24 bit format: B7 is MSB and B0 is LSB.									
Restriction	-									
Register Availability	Status							Availability		
	Normal Mode On, Idle Mode Off, Sleep Out							Yes		
	Normal Mode On, Idle Mode On, Sleep Out							Yes		
	Sleep In or Booster Off							Yes		
Default	Status							Default Value		
	Power On Sequence							00h		
	S/W Reset							00h		
	H/W Reset							00h		
Flow Chart										

6.2.7 Get_blue_channel (08h)

06H	RDBLUE (Read Blue Colour)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	0	1	0	0	0	07
1 st parameter	1	P7	P6	P5	P4	P3	P2	P1	P0	00
Description	The first parameter is telling blue colour value of the first pixel of the frame when there is used DPI I/F. 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and B0 are set to '0'. 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to '0'. 24 bit format: B7 is MSB and B0 is LSB.									
Restriction	SETEXTC turn on to enable this command									
Register Availability	Status							Availability		
	Normal Mode On, Idle Mode Off, Sleep Out							Yes		
	Normal Mode On, Idle Mode On, Sleep Out							Yes		
	Sleep In or Booster Off							Yes		
Default	Status							Default Value		
	Power On Sequence							00h		
	S/W Reset							00h		
	H/W Reset							00h		
Flow Chart										

6.2.8 RDDST: Read display status (09h)

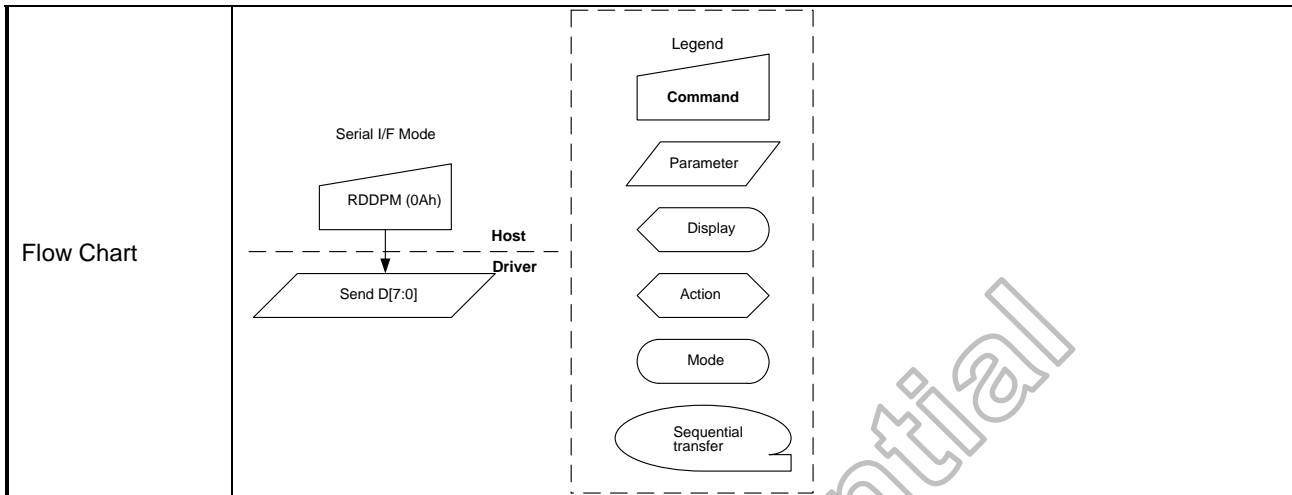
09H	RDDST (Read Display Status)										
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	0	0	0	0	1	0	0	1	09	
1 st parameter	1	D[31:24]									00
2 nd parameter	1	D[23:16]									71
3 rd parameter	1	D[15:8]									00
4 th parameter	1	D[7:0]									00
Description	This command indicates the current status of the display as described in the table below:										
	Bit	Description								Comment	
	D31	Booster Voltage Status								-	
	D30	Page Address Order								-	
	D29	Column Address Order								-	
	D28	Page/Column Order								Set to '0'	
	D27	Line Address Order								Set to '0'	
	D26	RGB/BGR Order								-	
	D25	Display Data Latch Order								-	
	D24	Flip Horizontal								-	
	D23	Flip Vertical								-	
	D22	Interface Colour Pixel Format Definition								-	
	D21										
	D20										
	D19	Idle Mode On/Off								-	
	D18	Partial Mode On/Off								Set to '0'	
	D17	Sleep In/Out								-	
	D16	Display Normal Mode On/Off								-	
	D15	Vertical Scrolling Status								Set to '0'	
	D14	Horizontal Scrolling Status								Set to '0'	
	D13	Inversion Status								-	
	D12	All Pixels On								-	
	D11	All Pixels Off								-	
	D10	Display On/Off								-	
	D9	Tearing Effect Line On/Off								-	
	D8	Gamma Curve Selection								-	
	D7										
	D6										
	D5	Tearing Effect Output Line Mode								-	
	D4	Horizontal Sync. (HSYNC, DPI I/F)								-	
	D3	Vertical Sync. (VSYNC, DPI I/F)								-	
	D2	Pixel Clock (DCK, DPI I/F)								-	
	D1	Data Enable (ENABLE, DPI I/F)								-	
D0	Error on DSI								-		
Bit Values are explained overleaf.											
Bit D31 – Booster Voltage Status											
'0' = Booster Off or has a fault.											
'1' = Booster On and working OK (Meets display supplier's optical requirements).											
Bit D30 – Page Address Order											
'0' = Top to Bottom (When MADCTL B7='0').											
'1' = Bottom to Top (When MADCTL B7='1').											
Bit D29 – Column Address Order											
'0' = Left to Right (When MADCTL B6='0').											
'1' = Right to Left (When MADCTL B6='1').											
Bit D28 – Page/Column Order											
'0' = Normal (When MADCTL B5='0').											
'1' = Rotation (When MADCTL B5='1').											
This bit is not applicable for this project, so it is set to '0'											

Description	<p>Bit D27 – Line Address Order '0' = LCD Refresh Top to Bottom (When MADCTL B4='0'). '1' = LCD Refresh Bottom to Top (When MADCTL B4='1'). This bit is not applicable for this project, so it is set to '0'</p> <p>Bit D26 – RGB/BGR Order '0' = RGB (When MADCTL B3='0'). '1' = BGR (When MADCTL B3='1').</p> <p>Bit D25 – Display Data Latch Order '0' = LCD Refresh Left to Right (When MADCTL B2='0'). '1' = LCD Refresh Right to Left (When MADCTL B2='1').</p> <p>Bit D24 – Flip Horizontal '0' = Normal (When MADCTL B1='0'). '1' = Flipped (When MADCTL B1='1').</p> <p>Bit D23 – Flip Vertical '0' = Normal (When MADCTL B0='0'). '1' = Flipped (When MADCTL B0='1').</p> <p>Bits D22, D21, D20 – Interface Colour Pixel Format Definition</p> <table border="1"> <thead> <tr> <th>Interface Format</th> <th>D22</th> <th>D21</th> <th>D20</th> </tr> </thead> <tbody> <tr> <td>Not Defined</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>16 Bit/Pixel</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>18 Bit/Pixel</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>24 Bit/Pixel</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	Interface Format	D22	D21	D20	Not Defined	0	0	0	Not Defined	0	0	1	Not Defined	0	1	0	Not Defined	0	1	1	Not Defined	1	0	0	16 Bit/Pixel	1	0	1	18 Bit/Pixel	1	1	0	24 Bit/Pixel	1	1	1
	Interface Format	D22	D21	D20																																	
Not Defined	0	0	0																																		
Not Defined	0	0	1																																		
Not Defined	0	1	0																																		
Not Defined	0	1	1																																		
Not Defined	1	0	0																																		
16 Bit/Pixel	1	0	1																																		
18 Bit/Pixel	1	1	0																																		
24 Bit/Pixel	1	1	1																																		
<p>Bit D19 – Idle Mode On/Off '0' = Idle Mode Off. '1' = Idle Mode On.</p> <p>Bit D18 – Partial Mode On/Off '0' = Partial Mode Off. '1' = Partial Mode On. This bit is not applicable for this project, so it is set to '0'</p> <p>Bit D17 – Sleep In/Out '0' = Sleep In Mode. '1' = Sleep Out Mode.</p> <p>Bit D16 – Display Normal Mode On/Off '0' = Display Normal Mode Off. '1' = Display Normal Mode On.</p> <p>Bit D15 – Vertical Scrolling On/Off '0' = Vertical Scrolling is Off. '1' = Vertical Scrolling is On. This bit is not applicable for this project, so it is set to '0'</p> <p>Bit D14 – Horizontal Scrolling Status This bit is not applicable for this project, so it is set to '0'</p> <p>Bit D13 – Inversion On/Off '0' = Inversion is Off. '1' = Inversion is On.</p> <p>Bit D12 – All Pixels On. '0' = Normal mode. '1' = All Pixels On.</p> <p>Bit D11 – All Pixels Off. '0' = Normal mode. '1' = All Pixels Off.</p> <p>Bit D10 – Display On/Off '0' = Display is Off. '1' = Display is On.</p> <p>Bit D9 – Tearing Effect Line On/Off '0' = Tearing Effect Line Off. '1' = Tearing Effect On.</p>																																					

Description	Bits D8, D7, D6 – Gamma Curve Selection				
	Gamma Curve Selected	D8	D7	D6	Gamma Set (26h) Parameter
	Gamma Curve 1	0	0	0	GC0
	Gamma Curve 2	0	0	1	Setting Inhibit
	Gamma Curve 3	0	1	0	Setting Inhibit
	Gamma Curve 4	0	1	1	Setting Inhibit
	Not Defined	1	0	0	Not Defined
	Not Defined	1	0	1	Not Defined
	Not Defined	1	1	0	Not Defined
	Not Defined	1	1	1	Not Defined
	Bit D5 – Tearing Effect Line Output Mode.				
	'0' = Mode 1, V-Blanking only.				
	'1' = Mode 2, both H-Blanking and V-Blanking.				
	Bit D4 – Horizontal Sync. (HSYNC) On/Off⁽¹⁾				
	'0' = Horizontal Sync. Line is Off (Low).				
	'1' = Horizontal Sync. Line is On (High).				
	Bit D3 – Vertical Sync. (VSYNC) On/Off⁽¹⁾				
	'0' = Vertical Sync. Line is Off. (Low)				
	'1' = Vertical Sync. Line is On. (High)				
	Bit D2 – Pixel Clock (PCLK) On/Off⁽¹⁾				
	'0' = Pixel Clock line is Off. (Low)				
	'1' = Pixel Clock line is On. (High)				
	Bit D1 – Data Enable (DE) On/Off⁽¹⁾				
	'0' = Data Enable line is Off. (Low)				
	'1' = Data Enable line is On. (High)				
	Bit D0 –Error on DSI				
	'0' = No Error				
	'1' = Error.				
	Note: (1) This bit indicates current status of the line when this command has been sent.				
Restriction	-				
Register Availability	Status		Availability		
	Normal Mode On, Idle Mode Off, Sleep Out		Yes		
	Normal Mode On, Idle Mode On, Sleep Out		Yes		
	Sleep In or Booster Off		Yes		
Default	Status		Default Value		
	Power On Sequence		Refer to Description		
	S/W Reset		Refer to Description		
	H/W Reset		Refer to Description		
Flow Chart	<p>Serial I/F Mode</p> <pre> graph TD subgraph Host C1[Command: RDDST 09h] end subgraph Driver P1[/Parameter: Send ST[31:24]/] P2[/Parameter: Send ST[23:16]/] P3[/Parameter: Send ST[15:8]/] P4[/Parameter: Send ST[7:0]/] end C1 --> P1 P1 --> P2 P2 --> P3 P3 --> P4 </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: Parallelogram Parameter: Slanted parallelogram Display: Hexagon Action: Arrowhead Mode: Oval Sequential transfer: Double-line oval 				

6.2.9 RDDPM: Read display power mode (0Ah)

0AH	RDDPM (Read Display Power Mode)										
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	0	0	0	0	1	0	1	0	0A	
1 st parameter	1	D7	D6	0	D4	D3	D2	0	0	08	
Description	This command indicates the current status of the display as described in the table below:										
	Bit		Description						Comment		
	D7		Booster Voltage Status						Set to '0'		
	D6		Idle Mode On/Off						-		
	D5		Partial Mode On/Off						Set to '0'		
	D4		Sleep In/Out						-		
	D3		Display Normal Mode On/Off						-		
	D2		Display On/Off						-		
	D1		Not Defined						Set to '0'		
	D0		ESD detection bit						Set to '0'		
	<p>Bit D7 – Booster Voltage Status '0' = Booster Off or has a fault. '1' = Booster On and working OK. (Meets display supplier's optical requirements) This bit is not applicable, so it is set to '0'</p> <p>Bit D6 – Idle Mode On/Off '0' = Idle Mode Off. '1' = Idle Mode On.</p> <p>Bit D5 – Partial Mode On/Off '0' = Partial Mode Off. '1' = Partial Mode On. This bit is not applicable, so it is set to '0'</p> <p>Bit D4 – Sleep In/Out '0' = Sleep In Mode. '1' = Sleep Out Mode.</p> <p>Bit D3 – Display Normal Mode On/Off '0' = Display Normal Mode Off. '1' = Display Normal Mode On.</p> <p>Bit D2 – Display On/Off '0' = Display is Off. '1' = Display is On.</p> <p>Bit D0 – ESD detection bit (in sleep out mode) '0' = ESD detected '1' = normal display(no ESD issue detected) Bits D1 and D0 are for future use and set to '0'.</p>										
	Restrictions	-									
Register Availability	Status						Availability				
	Normal Mode On, Idle Mode Off, Sleep Out						Yes				
	Normal Mode On, Idle Mode On, Sleep Out						Yes				
	Sleep In or Booster Off						Yes				
Default	Status						Default Value				
	Power On Sequence						08h				
	S/W Reset						08h				
	H/W Reset						08h				



6.2.10 RDDMADCTL: Read display MADCTL (0Bh)

0BH	RDDMADCTL (Read Display MADCTL)										
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	0	0	0	0	1	0	1	1	0B	
1 st parameter	1	D7	D6	0	0	D3	D2	D1	D0	00	
Description	This command indicates the current status of the display as described in the table below:										
	Bit		Description						Comment		
	D7		Page Address Order						-		
	D6		Column Address Order						-		
	D5		Page/Column Order						Set to '0'		
	D4		Line Address Order						Set to '0'		
	D3		RGB/BGR Order						-		
	D2		Display Data Latch Order						-		
	D1		Flip Horizontal						-		
	D0		Flip Vertical						-		
	<p>Bit D7 – Page Address Order '0' = Top to Bottom (When MADCTL B7='0'). '1' = Bottom to Top (When MADCTL B7='1').</p> <p>Bit D6 – Column Address Order '0' = Left to Right (When MADCTL B6='0'). '1' = Right to Left (When MADCTL B6='1').</p> <p>Bit D5 – Page/Column Order This bit is not applicable, so it is set to '0'</p> <p>Bit D4 – Line Address Order This bit is not applicable, so it is set to '0'</p> <p>Bit D3 – RGB/BGR Order '0' = RGB (When MADCTL B3='0') '1' = BGR (When MADCTL B3='1')</p> <p>Bit D2 – Display Data Latch Order '0' = LCD Refresh Left to Right (When MADCTL B2='0') '1' = LCD Refresh Right to Left (When MADCTL B2='1')</p> <p>Bit D1 – Flip Horizontal '0' = Normal (When MADCTL B1='0') '1' = Flipped (When MADCTL B1='1')</p> <p>Bit D0 – Flip Vertical '0' = Normal (When MADCTL B0='0') '1' = Flipped (When MADCTL B0='1')</p>										
	Restrictions	-									
	Register Availability	Status								Availability	
Normal Mode On, Idle Mode Off, Sleep Out								Yes			
Normal Mode On, Idle Mode On, Sleep Out								Yes			
Sleep In or Booster Off								Yes			

Default	Status		Default Value
	Power On Sequence		00h
	S/W Reset		No Change
	H/W Reset		00h

Flow Chart	<p>Serial I/F Mode</p>		<p>Legend</p> <ul style="list-style-type: none"> Red and Blue Parameter Display Action Mode Sequential transfer
	<p>Host Driver</p>		

Himax Confidential
Do Not Copy

6.2.11 RDDCOLMOD: Read display COLMOD (0Ch)

0Ch	RDDCOLMOD (Read Display COLMOD)										
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	0	0	0	0	1	1	0	0	0C	
1 st parameter	1	0	D6	D5	D4	0	D2	D1	D0	77	
Description	This command indicates the current status of the display as described in the table below:										
	Bit		Description					Comment			
	D7		Reserved					Set to '0'			
	D6		DPI Interface Pixel format					-			
	D5							-			
	D4							-			
	D3		Reserved					Set to '0'			
	D2		DBI Interface Pixel format					-			
	D1							-			
	D0							-			
Bits D6, D5, D4 – DPI Interface Colour Pixel Format Definition Bits D2, D1, D0 – DBI Interface Colour Pixel Format Definition.											
Interface Colour Format		D6/D2		D5/D1		D4/D0					
Not Defined		0		0		0					
Not Defined		0		0		1					
Not Defined		0		1		0					
Not Defined		0		1		1					
Not Defined		1		0		0					
16 bit/pixel		1		0		1					
18 bit/pixel		1		1		0					
24 bit/pixel		1		1		1					
If the setting is not used then the corresponding bits in the parameter returned from the display module are undefined.											
Restrictions	-										
Register Availability	Status					Availability					
	Normal Mode On, Idle Mode Off, Sleep Out					Yes					
	Normal Mode On, Idle Mode On, Sleep Out					Yes					
	Sleep In or Booster Off					Yes					
Default	Status					Default Value					
	Power On Sequence					70h					
	S/W Reset					No Change					
	H/W Reset					70h					
Flow Chart	<p>The flow chart illustrates the process of reading the display COLMOD. It starts with 'Serial I/F Mode' leading to the 'RDDCOLMOD (0Ch)' command. This command is sent from the 'Host' to the 'Driver'. The driver then returns the data 'Send D[7:0]'. A legend defines the symbols used: a red box for 'Red and Blue', a parallelogram for 'Parameter', a rounded rectangle for 'Display', a hexagon for 'Action', an oval for 'Mode', and a cloud-like shape for 'Sequential transfer'.</p>										

6.2.12 RDDIM: Read display image mode (0Dh)

0DH	RDDIM (Read Display Image Mode)																																																						
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																													
Command	0	0	0	0	0	1	1	0	1	0D																																													
1 st parameter	1	0	0	D5	D4	D3	D2	D1	D0	00																																													
Description	<p>This command indicates the current status of the display as described in the table below:</p> <p>Bit D7 – Vertical Scrolling On/Off This bit is not applicable, so it is set to '0'</p> <p>Bit D6 – Horizontal Scrolling Status This bit is not applicable, so it is set to '0'</p> <p>Bit D5 – Inversion On/Off '0' = Inversion is Off. '1' = Inversion is On.</p> <p>Bit D4 – All Pixels On '0' = Normal Display '1' = White Display</p> <p>Bit D3 – All Pixels Off '0' = Normal Display '1' = Black Display</p> <p>Bits D2, D1, D0 – Gamma Curve Selection</p> <table border="1"> <thead> <tr> <th>Gamma Curve Selected</th> <th>D2</th> <th>D1</th> <th>D0</th> <th>Gamma Set (26h) Parameter</th> </tr> </thead> <tbody> <tr> <td>Gamma Curve1</td> <td>0</td> <td>0</td> <td>0</td> <td>GC0</td> </tr> <tr> <td>Gamma Curve2</td> <td>0</td> <td>0</td> <td>1</td> <td>Setting Inhibit</td> </tr> <tr> <td>Gamma Curve3</td> <td>0</td> <td>1</td> <td>0</td> <td>Setting Inhibit</td> </tr> <tr> <td>Gamma Curve4</td> <td>0</td> <td>1</td> <td>1</td> <td>Setting Inhibit</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>0</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>1</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>1</td> <td>0</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>1</td> <td>1</td> <td>Not Defined</td> </tr> </tbody> </table>										Gamma Curve Selected	D2	D1	D0	Gamma Set (26h) Parameter	Gamma Curve1	0	0	0	GC0	Gamma Curve2	0	0	1	Setting Inhibit	Gamma Curve3	0	1	0	Setting Inhibit	Gamma Curve4	0	1	1	Setting Inhibit	Not Defined	1	0	0	Not Defined	Not Defined	1	0	1	Not Defined	Not Defined	1	1	0	Not Defined	Not Defined	1	1	1	Not Defined
Gamma Curve Selected	D2	D1	D0	Gamma Set (26h) Parameter																																																			
Gamma Curve1	0	0	0	GC0																																																			
Gamma Curve2	0	0	1	Setting Inhibit																																																			
Gamma Curve3	0	1	0	Setting Inhibit																																																			
Gamma Curve4	0	1	1	Setting Inhibit																																																			
Not Defined	1	0	0	Not Defined																																																			
Not Defined	1	0	1	Not Defined																																																			
Not Defined	1	1	0	Not Defined																																																			
Not Defined	1	1	1	Not Defined																																																			
Restrictions	-																																																						
Register Availability	<table border="1"> <thead> <tr> <th colspan="2">Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td colspan="2">Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td colspan="2">Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td colspan="2">Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>					Status		Availability	Normal Mode On, Idle Mode Off, Sleep Out		Yes	Normal Mode On, Idle Mode On, Sleep Out		Yes	Sleep In or Booster Off		Yes																																						
Status		Availability																																																					
Normal Mode On, Idle Mode Off, Sleep Out		Yes																																																					
Normal Mode On, Idle Mode On, Sleep Out		Yes																																																					
Sleep In or Booster Off		Yes																																																					
Default	<table border="1"> <thead> <tr> <th colspan="2">Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td colspan="2">Power On Sequence</td> <td>00h</td> </tr> <tr> <td colspan="2">S/W Reset</td> <td>00h</td> </tr> <tr> <td colspan="2">H/W Reset</td> <td>00h</td> </tr> </tbody> </table>					Status		Default Value	Power On Sequence		00h	S/W Reset		00h	H/W Reset		00h																																						
Status		Default Value																																																					
Power On Sequence		00h																																																					
S/W Reset		00h																																																					
H/W Reset		00h																																																					
Flow Chart																																																							

6.2.13 RDDSM: Read display signal mode (0Eh)

0EH	RDDSM (Read Display Signal Mode)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	0	0	1	1	1	0	0E								
1 st parameter	1	D7	D6	D5	D4	D3	D2	0	D0	00								
Description	<p>This command indicates the current status of the display described in the table as below:</p> <p>Bit D7 – Tearing Effect Line On/Off '0' = Tearing Effect Line Off. '1' = Tearing Effect On.</p> <p>Bit D6 – Tearing Effect Line Output Mode. '0' = Mode 1, V-Blanking only. '1' = Mode 2, both H-Blanking and V-Blanking.</p> <p>Bit D5 – Horizontal Sync. (DPI I/F) On/Off. '0' = Horizontal Sync. Line is Off. (Low) '1' = Horizontal Sync. Line is On. (High)</p> <p>Bit D4 – Vertical Sync. (DPI I/F) On/Off. '0' = Vertical Sync. Line is Off. (Low) '1' = Vertical Sync. Line is On. (High)</p> <p>Bit D3 – Pixel Clock (PCLK, DPI I/F) On/Off. '0' = PCLK line is Off. (Low) '1' = PCLK line is On. (High)</p> <p>Bit D2 – Data Enable (DE, DPI I/F) On/Off. '0' = DE line is Off. (Low) '1' = DE line is On. (High)</p> <p>Bit D1 – Reserved.</p> <p>Bit D0 –Error on DSI '0' = No Error. '1' = Error.</p>																	
Restrictions	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value																	
Power On Sequence	00h																	
S/W Reset	00h																	
H/W Reset	00h																	
Flow Chart	<p>The flow chart illustrates the RDDSM (0Eh) command sequence. It starts with a 'Serial I/F Mode' box, which leads to a 'Parameter' box labeled 'RDDSM (0Eh)'. An arrow points from this parameter box to a 'Host' box, which then sends the command to a 'Driver' box. The driver's response is shown as 'Send D[7:0]'. A legend on the right defines the symbols used: a trapezoid for 'Red and Blue', a parallelogram for 'Parameter', a rounded rectangle for 'Display', a hexagon for 'Action', an oval for 'Mode', and a rounded rectangle with a tail for 'Sequential transfer'.</p>																	

6.2.14 RDDSDR: Read display self-diagnostic result) (0Fh)

0FH	RDDSDR (Read Display Self-Diagnostic Result)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	0	1	1	1	1	0F
1 st parameter	1	D7	D6	D5	D4	0	0	0	0	00
Description	The display module returns the self-diagnostic results following a Sleep Out command. Bit D7 – Register Loading Detection Bit D6 – Functionality Detection Bit D5 – Chip Attachment Detection Set to '0' if feature unimplemented. Bit D4 – Display Glass Break Detection Set to '0' if feature unimplemented. Bits D[3:0] – Reserved.									
Restrictions	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	<p>Serial I/F Mode</p> <p>RDDSDR (0Fh)</p> <p>Host</p> <p>Driver</p> <p>Send D[7:0]</p> <p>Legend</p> <ul style="list-style-type: none"> Red and Blue Parameter Display Action Mode Sequential transfer 									

6.2.15 SLPIN: Sleep in (10h)

10H	SLPIN (Sleep In)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	0	1	0	0	0	0	10								
Parameter	NO PARAMETER																	
Description	<p>This command initial power down sequence. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.</p>																	
Restriction	<p>This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p> <p>The host processor continues to send PCLK, HSYNC, and VSYNC and DE signals to HX8399-C for two frames after this command is sent.</p>																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>					Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes					
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	N/A																	
Flow Chart	<p>It takes 120msec to get into Sleep In mode after SLPIN command issued.</p>																	

6.2.16 SLPOUT: Sleep out (11h)

11H	SLPOUT (Sleep Out)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	0	1	0	0	0	1	11								
Parameter	NO PARAMETER																	
Description	<p>This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.</p>																	
Restriction	<p>This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</p> <p>The host processor continues to send PCLK, HSYNC, and VSYNC and DE signals to HX8399-C for two frames after this command is sent.</p>																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	N/A																	
Flow Chart	<p>It takes 120msec to become Sleep Out mode after SLPOUT command issued.</p>																	

6.2.17 NORON: Normal display mode on (13h)

13H	NORON (Normal Display Mode On)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	1	0	0	1	1	13
Parameter	NO PARAMETER									
Description	This command returns the display to normal mode.									
Restriction	This command has no effect when Normal Display mode is active.									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					Normal display mode				
	S/W Reset					Normal display mode				
	H/W Reset					Normal display mode				
Flow Chart	-									

Himax Confidential
Do Not Copy

6.2.18 INVOFF: Display inversion off (20h)

20H	INVOFF (Display Inversion Off)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	0	0	0	0	0	20								
Parameter	NO PARAMETER																	
Description	<p>This command is used to recover from display inversion mode. This command does not change any other status.</p> <p style="text-align: center;">(Example)</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Input Data</p> </div> <div style="font-size: 2em;">→</div> <div style="text-align: center;"> <p>Display</p> </div> </div>																	
Restriction	This command has no effect when module is already in inversion off mode.																	
Register Availability	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>					Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes					
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal display mode</td> </tr> <tr> <td>S/W Reset</td> <td>Normal display mode</td> </tr> <tr> <td>H/W Reset</td> <td>Normal display mode</td> </tr> </tbody> </table>					Status	Default Value	Power On Sequence	Normal display mode	S/W Reset	Normal display mode	H/W Reset	Normal display mode					
Status	Default Value																	
Power On Sequence	Normal display mode																	
S/W Reset	Normal display mode																	
H/W Reset	Normal display mode																	
Flow Chart																		

6.2.19 INVON: Display inversion on (21h)

21H	INVON (Display Inversion On)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	1	0	0	0	0	1	21
Parameter	NO PARAMETER									
Description	<p>This command is used to enter into display inversion mode. This command does not change any other status.</p> <p>(Example)</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Input Data</p> </div> <div style="font-size: 2em;">→</div> <div style="text-align: center;"> <p>Display</p> </div> </div>									
Restriction	This command has no effect when module is already in inversion on mode.									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
Default	Status					Default Value				
	Power On Sequence					Normal display mode				
	S/W Reset					Normal display mode				
H/W Reset					Normal display mode					
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A([Display Inversion OFF Mode]) --> B[INVON] B --> C([Display Inversion ON Mode]) </pre> </div> <div style="border: 1px dashed black; padding: 5px; margin-left: 20px;"> <p>Legend</p> <ul style="list-style-type: none"> Command: [Rectangle] Parameter: [Trapezoid] Display: [Arrow] Action: [Arrow] Mode: [Oval] Sequential transfer: [Oval] </div> </div>									

6.2.20 ALLPOFF: All pixel off (22h)

22H	ALLPOFF (All Pixel Off)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	0	0	0	1	0	22								
Parameter	NO PARAMETER																	
Description	<p>This command turns the display panel black in 'Sleep Out' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'. This command does not change any other status.</p> <p>(Example)</p> <div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center;"> <p>Input Data</p> </div> <div style="margin: 0 20px;"> </div> <div style="text-align: center;"> <p>Display</p> </div> </div> <p>'All Pixels On' or 'Normal Display Mode On' – commands are used to leave this mode. The display is showing the input data after 'Normal Display Mode On' command.</p>																	
Restriction	This command has no effect when module is already in inversion on mode.																	
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 70%;">Status</th> <th style="width: 30%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 70%;">Status</th> <th style="width: 30%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td style="text-align: center;">Normal display mode</td> </tr> <tr> <td>S/W Reset</td> <td style="text-align: center;">Normal display mode</td> </tr> <tr> <td>H/W Reset</td> <td style="text-align: center;">Normal display mode</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Normal display mode	S/W Reset	Normal display mode	H/W Reset	Normal display mode
Status	Default Value																	
Power On Sequence	Normal display mode																	
S/W Reset	Normal display mode																	
H/W Reset	Normal display mode																	
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A([Normal Display mode]) --> B[ALLPOFF] B --> C([Black Display]) </pre> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p style="text-align: center; margin: 0;">Legend</p> <ul style="list-style-type: none"> <li style="margin-bottom: 5px;">[] Command <li style="margin-bottom: 5px;">/ / Parameter <li style="margin-bottom: 5px;">◀ Display <li style="margin-bottom: 5px;">▶ Action <li style="margin-bottom: 5px;">○ Mode <li style="margin-bottom: 5px;">◌ Sequential transfer </div> </div>																	

6.2.21 ALLPON: All pixel on (23h)

23H	ALLPON(All Pixel On)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	1	0	0	0	1	1	23
Parameter	NO PARAMETER									
Description	<p>This command turns the display panel white in 'Sleep out' mode and a status of the 'Display On/Off' register can be 'on' or 'off'. This command does not change any other status.</p> <p>(Example)</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Input Data</p> </div> <div style="font-size: 2em;">→</div> <div style="text-align: center;"> <p>Display</p> </div> </div> <p>'All Pixels Off' or 'Normal Display Mode On' – commands are used to leave this mode. The display is showing the input data after 'Normal Display Mode On' command.</p>									
Restriction	This command has no effect when module is already in inversion on mode.									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					Normal display mode				
	S/W Reset					Normal display mode				
	H/W Reset					Normal display mode				
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A([Normal Display mode]) --> B[ALLPON] B --> C([White Display]) </pre> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>									

6.2.22 GAMSET: Gamma set (26h)

26H	GAMSET (Gamma Set)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	1	0	0	1	1	0	26
Parameter	1	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	01
Description	This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curves are defined in Curve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the Table:									
	GC[7:0]			Parameter			Curve selected			
	01h			GC0			Gamma Curve 1			
	02h			GC1			Setting Inhibit			
	04h			GC2			Setting Inhibit			
08h			GC3			Setting Inhibit				
Note: (1) All other values are undefined.										
Restriction	Values of GC[7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					01h				
	S/W Reset					01h				
	H/W Reset					01h				
Flow Chart	<pre> graph TD A[GAMSET] --> B[/GC [7:0]/] B --> C{{New Gamma Curve Loaded}} </pre>									

6.2.23 DISPOFF: Display off (28h)

28H	DISPOFF (Display Off)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	0	1	0	0	0	28								
Parameter	NO PARAMETER																	
Description	<p>This command is used to enter into DISPLAY OFF mode. In this mode, the output from DPI I/F are disabled and blank page inserted. This command does not change any other status. There will be no abnormal visible effect on the display.</p> <p>(Example)</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Input Data</p> </div> <div style="font-size: 2em;">→</div> <div style="text-align: center;"> <p>Display</p> </div> </div>																	
Restriction	This command has no effect when module is already in display off mode.																	
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 70%;">Status</th> <th style="width: 30%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 70%;">Status</th> <th style="width: 30%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td style="text-align: center;">Display off</td> </tr> <tr> <td>S/W Reset</td> <td style="text-align: center;">Display off</td> </tr> <tr> <td>H/W Reset</td> <td style="text-align: center;">Display off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off
Status	Default Value																	
Power On Sequence	Display off																	
S/W Reset	Display off																	
H/W Reset	Display off																	
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A{{Display On Mode}} --> B[DISPOFF] B --> C{{Display Off Mode}} </pre> </div> <div style="border: 1px dashed black; padding: 5px; margin-left: 20px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>																	

6.2.24 DISPON: Display on (29h)

29H	DISPON (Display On)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	1	0	1	0	0	1	29
Parameter	NO PARAMETER									
Description	<p>This command is used to recover from DISPLAY OFF mode. Output from DPI I/F is enabled. This command does not change any other status. (Example)</p> <div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center;"> <p>Input Data</p> </div> <div style="margin: 0 20px;">→</div> <div style="text-align: center;"> <p>Display</p> </div> </div>									
Restriction	This command has no effect when module is already in display on mode.									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
Default	Status					Default Value				
	Power On Sequence					Display on				
	S/W Reset					Display on				
Flow Chart						<div style="border: 1px dashed black; padding: 5px;"> <p style="text-align: center;">Legend</p> <div style="display: flex; flex-direction: column; gap: 10px;"> <div style="border: 1px solid black; padding: 2px; width: 100px; margin: 0 auto;">Command</div> <div style="border: 1px solid black; padding: 2px; width: 100px; margin: 0 auto;">Parameter</div> <div style="border: 1px solid black; padding: 2px; width: 100px; margin: 0 auto;">Display</div> <div style="border: 1px solid black; padding: 2px; width: 100px; margin: 0 auto;">Action</div> <div style="border: 1px solid black; padding: 2px; width: 100px; margin: 0 auto;">Mode</div> <div style="border: 1px solid black; padding: 2px; width: 100px; margin: 0 auto;">Sequential transfer</div> </div> </div>				
	<pre> graph TD A[Display Off Mode] --> B[DISPON] B --> C[Display On Mode] </pre>									

6.2.25 TEOFF: Tearing effect line off (34h)

34H	TEOFF (Tearing Effect Line OFF)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	1	1	0	1	0	0	34
Parameter	NO PARAMETER									
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.									
Restriction	This command has no effect when Tearing Effect output is OFF.									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					Off				
	S/W Reset					Off				
	H/W Reset					Off				
Flow Chart	<p style="text-align: center;">Legend</p> <div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>TE Line Output ON</p> <p>↓</p> <p>TEOFF</p> <p>↓</p> <p>TE Line Output OFF</p> </div> <div style="text-align: center;"> <p>Command</p> <p>Parameter</p> <p>Display</p> <p>Action</p> <p>Mode</p> <p>Sequential transfer</p> </div> </div>									

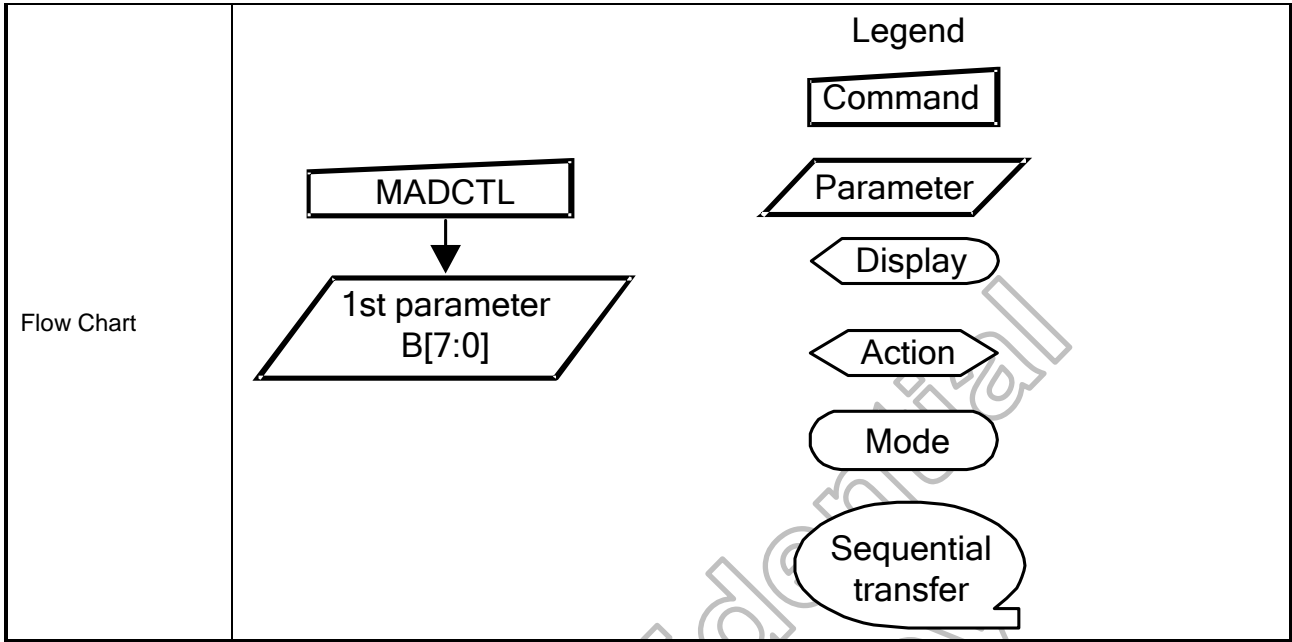
6.2.26 TEON: Tearing effect line on (35h)

35H	TEON (Tearing Effect Line ON)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	1	0	1	0	1	35								
Parameter	1	X	X	X	X	X	X	X	M	00								
Description	<p>This command is used to turn ON the Tearing Effect output signal from the TE signal line.</p> <p>The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care)</p> <p>When M=0: The Tearing Effect Output line consists of V-Blanking information only:</p> <p>When M=1: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:</p>																	
Restriction	This command has no effect when Tearing Effect output is ON.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>S/W Reset</td> <td>Off</td> </tr> <tr> <td>H/W Reset</td> <td>Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off
Status	Default Value																	
Power On Sequence	Off																	
S/W Reset	Off																	
H/W Reset	Off																	
Flow Chart																		

6.2.27 MADCTL: Memory access control (36h)

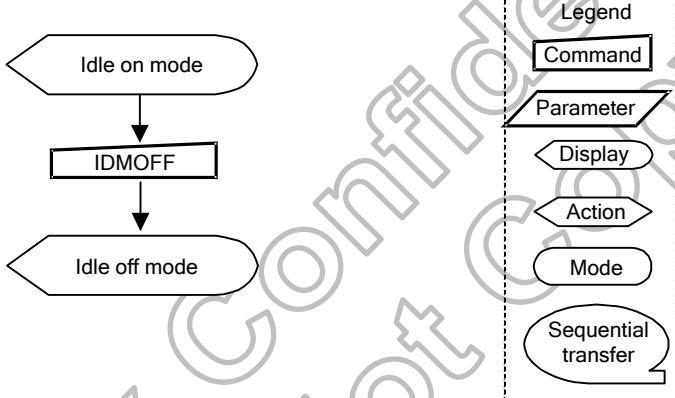
36H	MADCTL (Memory Access Control)																																			
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																										
Command	0	0	0	1	1	0	1	1	0	36																										
1 st parameter	1	D7	D6	X	X	D3	D2	D1	D0	00																										
Description	This command defines the display scanning direction of LCD. This command makes no change on the other driver status.																																			
	Bit Assignment																																			
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>PAGE ADDRESS ORDER (MY)</td> <td>LCD vertical updating order direction control</td> </tr> <tr> <td>D6</td> <td>COLUMN ADDRESS ORDER (MX)</td> <td>LCD horizontal updating order direction control</td> </tr> <tr> <td>D5</td> <td>PAGE/COLUMN SELECTION (MV)</td> <td rowspan="2">It is not applicable for this project, so it is set to "0"</td> </tr> <tr> <td>D4</td> <td>Vertical ORDER (ML)</td> </tr> <tr> <td>D3</td> <td>RGB-BGR ORDER (BGR)</td> <td>Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)</td> </tr> <tr> <td>D2</td> <td>Horizontal ORDER (MH)</td> <td>LCD horizontal refresh direction control</td> </tr> <tr> <td>D1</td> <td>Flip Horizontal (SS)</td> <td>Select the Source driver scan direction on panel module</td> </tr> <tr> <td>D0</td> <td>Flip Vertical (GS)</td> <td>Select the Gate driver scan direction on panel module</td> </tr> </tbody> </table>										Bit	Name	Description	D7	PAGE ADDRESS ORDER (MY)	LCD vertical updating order direction control	D6	COLUMN ADDRESS ORDER (MX)	LCD horizontal updating order direction control	D5	PAGE/COLUMN SELECTION (MV)	It is not applicable for this project, so it is set to "0"	D4	Vertical ORDER (ML)	D3	RGB-BGR ORDER (BGR)	Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)	D2	Horizontal ORDER (MH)	LCD horizontal refresh direction control	D1	Flip Horizontal (SS)	Select the Source driver scan direction on panel module	D0	Flip Vertical (GS)	Select the Gate driver scan direction on panel module
	Bit	Name	Description																																	
	D7	PAGE ADDRESS ORDER (MY)	LCD vertical updating order direction control																																	
	D6	COLUMN ADDRESS ORDER (MX)	LCD horizontal updating order direction control																																	
	D5	PAGE/COLUMN SELECTION (MV)	It is not applicable for this project, so it is set to "0"																																	
	D4	Vertical ORDER (ML)																																		
	D3	RGB-BGR ORDER (BGR)	Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)																																	
	D2	Horizontal ORDER (MH)	LCD horizontal refresh direction control																																	
	D1	Flip Horizontal (SS)	Select the Source driver scan direction on panel module																																	
	D0	Flip Vertical (GS)	Select the Gate driver scan direction on panel module																																	
	RGB-BGR Order																																			
	<table border="0"> <tr> <td style="text-align: center;">D3= 0</td> <td style="text-align: center;">D3= 1</td> </tr> <tr> <td style="text-align: center;"> </td> <td style="text-align: center;"> </td> </tr> </table>										D3= 0	D3= 1																								
	D3= 0	D3= 1																																		
Display Data Latch Order																																				
<table border="0"> <tr> <td style="text-align: center;">D2= 0</td> <td style="text-align: center;">D2= 1</td> </tr> <tr> <td style="text-align: center;"> </td> <td style="text-align: center;"> </td> </tr> </table>										D2= 0	D2= 1																									
D2= 0	D2= 1																																			

	<p style="text-align: center;">SS - Source scan sequence</p> <p>SS= 0</p> <p>Host Image: Display Image: </p> <p>SS= 1</p> <p>Host Image: Display Image: </p> <p style="text-align: center;">GS - Gate scan sequence</p> <p>GS= 0</p> <p>Host Image: Display Image: </p> <p>GS= 1</p> <p>Host Image: Display Image: </p>								
Restriction	D7 and D6 and D5 and D4 are set to '0' internally.								
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In or Booster Off	Yes								
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	No Change	H/W Reset	00h
Status	Default Value								
Power On Sequence	00h								
S/W Reset	No Change								
H/W Reset	00h								



Himax Confidential
Do Not Copy

6.2.28 IDMOFF: Idle mode off (38h)

38H	IDMOFF (Idle mode off)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER									
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16.7M colours.									
Restriction	This command has no effect when module is already in idle off mode.									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
Default	Status					Default Value				
	Power On Sequence					Off				
	S/W Reset					Off				
Flow Chart	S/W Reset					Off				
	H/W Reset					Off				
										

6.2.29 IDMON: Idle mode on (39h)

39H	IDMON (Idle mode on)																																													
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	0	0	0	1	1	1	0	0	1	39																																				
Parameter	NO PARAMETER																																													
Description	<p>This command is used to enter into Idle mode on. In the idle on mode, colour expression is reduced. The primary and the secondary colours using MSB of each R, G and B, 8 colour depth data is displayed.</p> <p>(Example)</p> <div style="display: flex; align-items: center;"> <div style="text-align: center;"> <p>Memory</p> </div> <div style="margin: 0 20px;">→</div> <div style="text-align: center;"> <p>Display</p> </div> </div> <p>Display Colour</p> <table border="1"> <thead> <tr> <th></th> <th>R7 – R0</th> <th>G7 – G0</th> <th>B7 – B0</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Blue</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Red</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Magenta</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Green</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Cyan</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Yellow</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>White</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> </tbody> </table> <p>X=don't care</p>											R7 – R0	G7 – G0	B7 – B0	Black	0XXXXX	0XXXXX	0XXXXX	Blue	0XXXXX	0XXXXX	1XXXXX	Red	1XXXXX	0XXXXX	0XXXXX	Magenta	1XXXXX	0XXXXX	1XXXXX	Green	0XXXXX	1XXXXX	0XXXXX	Cyan	0XXXXX	1XXXXX	1XXXXX	Yellow	1XXXXX	1XXXXX	0XXXXX	White	1XXXXX	1XXXXX	1XXXXX
	R7 – R0	G7 – G0	B7 – B0																																											
Black	0XXXXX	0XXXXX	0XXXXX																																											
Blue	0XXXXX	0XXXXX	1XXXXX																																											
Red	1XXXXX	0XXXXX	0XXXXX																																											
Magenta	1XXXXX	0XXXXX	1XXXXX																																											
Green	0XXXXX	1XXXXX	0XXXXX																																											
Cyan	0XXXXX	1XXXXX	1XXXXX																																											
Yellow	1XXXXX	1XXXXX	0XXXXX																																											
White	1XXXXX	1XXXXX	1XXXXX																																											
Restriction	This command has no effect when module is already in idle on mode.																																													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes																												
Status	Availability																																													
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																													
Normal Mode On, Idle Mode On, Sleep Out	Yes																																													
Sleep In or Booster Off	Yes																																													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>S/W Reset</td> <td>Off</td> </tr> <tr> <td>H/W Reset</td> <td>Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off																												
Status	Default Value																																													
Power On Sequence	Off																																													
S/W Reset	Off																																													
H/W Reset	Off																																													
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A[Idle off mode] --> B[IDMON] B --> C[Idle on mode] </pre> </div> <div style="border: 1px dashed black; padding: 5px; margin-left: 20px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>																																													

6.2.30 COLMOD: Interface pixel format 3Ah)

3A H	COLMOD (Interface Pixel Format)																																												
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																			
Command	0	0	0	1	1	1	0	1	0	3A																																			
1 st parameter	1	X	D6	D5	D4	X	X	X	X	77																																			
Description	This command is used to define the format of RGB picture data. D6~D4 : DPI Pixel format Definition. Bit D7, Reserved The formats are shown in the table:																																												
	<table border="1"> <thead> <tr> <th>Pixel Format</th> <th>D6</th> <th>D5</th> <th>D4</th> </tr> </thead> <tbody> <tr> <td>Not Defined</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>16 Bit/Pixel</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>18 Bit/Pixel</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>24 Bit/Pixel</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>										Pixel Format	D6	D5	D4	Not Defined	0	0	0	Not Defined	0	0	1	Not Defined	0	1	0	Not Defined	0	1	1	Not Defined	1	0	0	16 Bit/Pixel	1	0	1	18 Bit/Pixel	1	1	0	24 Bit/Pixel	1	1
Pixel Format	D6	D5	D4																																										
Not Defined	0	0	0																																										
Not Defined	0	0	1																																										
Not Defined	0	1	0																																										
Not Defined	0	1	1																																										
Not Defined	1	0	0																																										
16 Bit/Pixel	1	0	1																																										
18 Bit/Pixel	1	1	0																																										
24 Bit/Pixel	1	1	1																																										
If the setting is not used then the corresponding bits in the parameter returned from the display module are undefined.																																													
Restriction	There is no visible effect until the image data is written.																																												
Register Availability	Status					Availability																																							
	Normal Mode On, Idle Mode Off, Sleep Out					Yes																																							
	Normal Mode On, Idle Mode On, Sleep Out					Yes																																							
	Sleep In or Booster Off					Yes																																							
Default	Status					Default Value																																							
	Power On Sequence					77h																																							
	S/W Reset					77h																																							
	H/W Reset					77h																																							
Flow Chart	<pre> graph TD A([n Bit/Pixel Mode]) --> B[Set Pixel Format] B --> C[/Parameter/] C --> D([New n Bit/Pixel Mode]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: [] Parameter: [/ /] Display: [] Action: [] Mode: [] Sequential transfer: [] 																																												

6.2.31 TESL: Tear effect scan lines (44h)

44H	TESL (Tear Effect Scan Lines)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	0	0	0	1	0	0	44
1 st parameter	1	TELINE[15:8]								00
2 nd parameter	1	TELINE[7:0]								00
Description	<p>This command is turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reaches line TELINE. The TE signal is not affected by changing MADCTL bit D4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. The Tearing Effect Output line consists of V-Blanking information only:</p> <p>Note: (1) That TELINE=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.</p>									
Restriction	The command has no effect when Tearing Effect output is already ON.									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					0000h				
	S/W Reset					0000h				
	H/W Reset					0000h				
Flow Chart	<pre> graph TD Start([TE Output On or Off]) --> SetTearOn[/set_tear_on/] subgraph DashedBox [] SetTearOn --> LineNLSB[/Line N (LSB)/] LineNLSB --> LineNMSB[/Line N (MSB)/] end LineNMSB --> End([TE Output On]) </pre>									

6.2.32 GETSCAN: Get the current scanline (45h)

45H	GETSCAN (Get the current scanline)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	0	0	0	1	0	1	45
1 st parameter	1	SLN[15:8]								00
2 nd parameter	1	SLN[7:0]								00F
Description	The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined.									
Restriction	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					0000h				
	S/W Reset					0000h				
	H/W Reset					0000h				
Flow Chart	<pre> graph TD subgraph Host_Processor [Host Processor] A[get_scanline] end subgraph Display_Module [Display Module] B[/scanline MSB/] C[/scanline LSB/] end A --- B B --- C </pre>									

6.2.33 WRDISBV: Write display brightness (51h)

51H	WRDISBV (Write Display Brightness)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	0	1	0	0	0	1	51
1 st parameter	1	X	X	X	X	DBV[11:7]				00
2 nd parameter	1	DBV[7:0]							00	
Description	This command is used to adjust the brightness value of the display. It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	<pre> graph TD A[WRDISBV] --> B[/DBV[11:0]/] B --> C{{New Display Luminance Value Loaded}} </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: [] Parameter: / / Display: <> Action: > Mode: () Sequential transfer: [] 									

6.2.34 RDDISBV: Read display brightness value (52h)

52H	RDDISBV (Read Display Brightness Value)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	0	1	0	0	1	0	52
1 st parameter	1	X	X	X	X	DBV[11:8]				00
2 nd parameter	1	DBV[7:0]							00	
Description	<p>This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>DBV[7:0] is reset when display is in sleep-in mode. DBV[7:0] is '00h' when bit BCTRL of R53h command is '0'. DBV[7:0] is manual set brightness specified with "R53h" command when bit BCTRL is '1'. When bit BCTRL of "R53h" command is '1' and bit C1/C0 of "R55h" command are '0', DBV[7:0] output is the brightness value specified with "R51h" command.</p>									
Restriction	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	<div style="display: flex; justify-content: space-between; align-items: center;"> <div style="text-align: center;"> <p>Serial I/F Mode</p> <div style="border: 1px solid black; padding: 5px; width: 150px; margin: 0 auto;">Read RDDISBV</div> <p>↓</p> <div style="border: 1px solid black; padding: 5px; width: 150px; margin: 0 auto;">Parameter</div> </div> <div style="border-left: 1px dashed black; padding-left: 10px;"> <p>Host</p> <p>Display</p> </div> <div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <div style="border: 1px solid black; padding: 2px; width: 60px; margin-bottom: 5px;">Command</div> <div style="border: 1px solid black; padding: 2px; width: 100px; margin-bottom: 5px;">Parameter</div> <div style="border: 1px solid black; padding: 2px; width: 80px; margin-bottom: 5px;">Display</div> <div style="border: 1px solid black; padding: 2px; width: 80px; margin-bottom: 5px;">Action</div> <div style="border: 1px solid black; padding: 2px; width: 80px; margin-bottom: 5px;">Mode</div> <div style="border: 1px solid black; padding: 2px; width: 100px; margin-bottom: 5px;">Sequential transfer</div> </div> </div>									

6.2.35 WRCTRLD: Write control display (53h)

53H	WRCTRLD (Write Control Display)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	0	1	0	0	1	1	53
1 st parameter	1	X	X	BCTRL	X	DD	BL	X	X	00
Description	<p>This command is used to control display brightness. BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) DD: Display Dimming(Only for manual brightness setting) DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 → 1 or 1 → 0. When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected. X = Don't care.</p>									
Restriction	-									
Register Availability	Status						Availability			
	Normal Mode On, Idle Mode Off, Sleep Out						Yes			
	Normal Mode On, Idle Mode On, Sleep Out						Yes			
	Sleep In or Booster Off						Yes			
Default	Status						Default Value			
	Power On Sequence						00h			
	S/W Reset						00h			
	H/W Reset						00h			
Flow Chart	<pre> graph TD WRCTRLD[WRCTRLD] --> Params[/BCTRL, DD, BL/] Params --> Loaded{New Control Value Loaded} </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: [] Parameter: / / Display: <> Action: <> Mode: () Sequential transfer: () 									

6.2.36 RDCTRLD: Read control value display (54h)

54H	RDCTRLD (Read Control Value Display)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	0	1	0	1	0	0	54
1 st parameter	1	0	0	BCTRL	0	DD	BL	0	0	00
Description	This command returns ambient light and brightness control values, see chapter: "6.2.39 Write CTRL Display (53h)". BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off 1 = On DD: Display Dimming. DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (completely turn off backlight circuit) 1 = On									
Restriction	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart										

6.2.37 WRCABC: Write content adaptive brightness control (55h)

55 H	WRCABC (Write Content Adaptive Brightness Control)																								
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	0	1	0	1	0	1	0	1	55															
1 st parameter	1	X	X	X	X	X	X	C[1:0]		00															
Description	<p>This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter “5.13 Content Adaptive Brightness Control (CABC)”.</p> <table border="1"> <thead> <tr> <th>C1</th> <th>C0</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Off</td> </tr> <tr> <td>0</td> <td>1</td> <td>User Interface Image</td> </tr> <tr> <td>1</td> <td>0</td> <td>Still Picture</td> </tr> <tr> <td>1</td> <td>1</td> <td>Moving Image</td> </tr> </tbody> </table>										C1	C0	Function	0	0	Off	0	1	User Interface Image	1	0	Still Picture	1	1	Moving Image
C1	C0	Function																							
0	0	Off																							
0	1	User Interface Image																							
1	0	Still Picture																							
1	1	Moving Image																							
Restriction	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>					Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes												
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>					Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h												
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
Flow Chart	<pre> graph TD WRCABC[Command: WRCABC] --> Param[/Parameter: 1st parameter: C[1:0]/] Param --> Mode[/Action: New Adaptive Image Mode/] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Hexagon Action: Arrow Mode: Oval Sequential transfer: Cloud shape 																								

6.2.38 RDCABC: Read content adaptive brightness control (56h)

56H	RDCABC (Read Content Adaptive Brightness Control)																								
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	0	1	0	1	0	1	1	0	56															
1 st parameter	1	0	0	0	0	0	0	C1	C0	00															
Description	<p>This command is used to set parameters for image content based adaptive brightness control functionality.</p> <p>There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter "5.13 Content Adaptive Brightness Control (CABC)".</p> <table border="1"> <thead> <tr> <th>C1</th> <th>C0</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Off</td> </tr> <tr> <td>0</td> <td>1</td> <td>User Interface Image</td> </tr> <tr> <td>1</td> <td>0</td> <td>Still Picture</td> </tr> <tr> <td>1</td> <td>1</td> <td>Moving Image</td> </tr> </tbody> </table>										C1	C0	Function	0	0	Off	0	1	User Interface Image	1	0	Still Picture	1	1	Moving Image
C1	C0	Function																							
0	0	Off																							
0	1	User Interface Image																							
1	0	Still Picture																							
1	1	Moving Image																							
Restriction																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>					Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes												
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>					Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h												
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
Flow Chart																									

6.2.39 WRCABCMB: Write CABC minimum brightness (5Eh)

5E H	WRCABCMB (Write CABC minimum brightness)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	0	1	1	1	1	0	5E
1 st parameter	1	CMB[7:0]								00
Description	This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. See chapter "5.13.3 Minimum brightness setting of CABC function".									
Restriction	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	<pre> graph TD WRCABCMB[Command] --> CMB[CMB[7..0] Parameter] CMB --> Luminance{New Display Luminance Value Loaded} </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Double-headed arrow Action: Arrow Mode: Oval Sequential transfer: Callout bubble 									

6.2.40 RDCABCMB: Read CABC minimum brightness (5Fh)

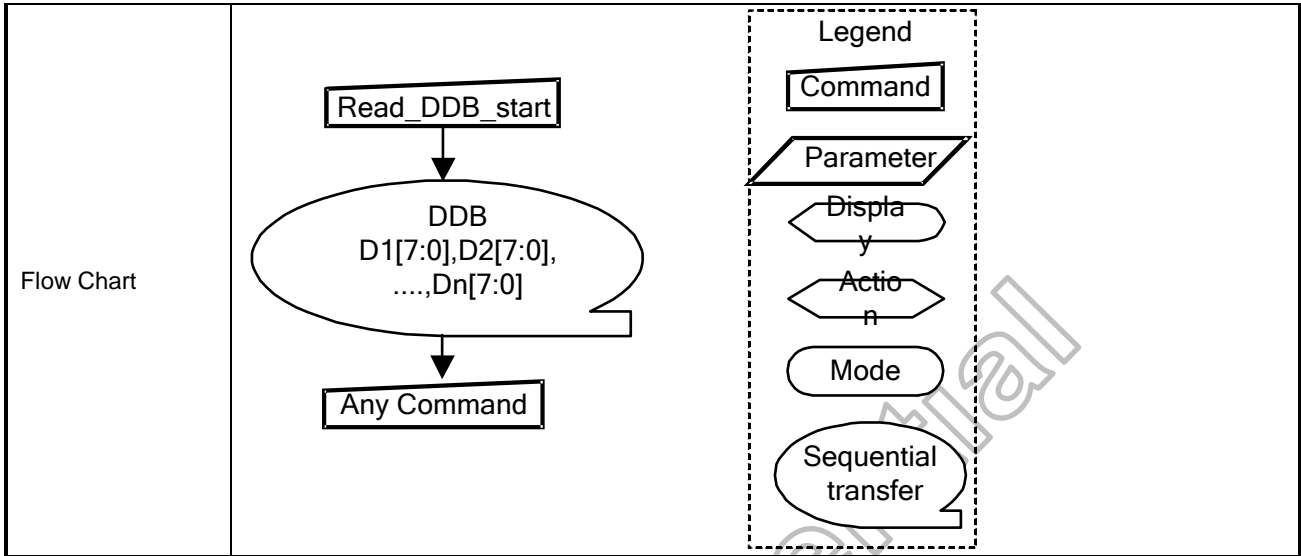
5FH	RDCABCMB (Read CABC minimum brightness)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	0	1	1	1	1	1	5F
1 st parameter	1	CMB[7:0]								00
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter "5.13.3 Minimum brightness setting of CABC function". CMB[7:0] is CABC minimum brightness specified with "R5Eh" command.									
Restriction	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	<div style="display: flex; justify-content: space-between; align-items: center;"> <div style="text-align: center;"> <p>Serial I/F Mode</p> <div style="border: 1px solid black; padding: 2px; display: inline-block;">Read RDCABCMB</div> <p>↓</p> <div style="border: 1px solid black; padding: 2px; display: inline-block;">Parameter</div> </div> <div style="text-align: center;"> <p>Host</p> <p>-----</p> <p>Display</p> </div> <div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <div style="border: 1px solid black; padding: 2px; display: inline-block; width: 40px; height: 15px; margin-bottom: 5px;"></div> Command <div style="border: 1px solid black; padding: 2px; display: inline-block; width: 60px; height: 15px; transform: rotate(-15deg); margin-bottom: 5px;"></div> Parameter <div style="border: 1px solid black; padding: 2px; display: inline-block; width: 60px; height: 15px; transform: rotate(15deg); margin-bottom: 5px;"></div> Display <div style="border: 1px solid black; padding: 2px; display: inline-block; width: 60px; height: 15px; transform: rotate(15deg); margin-bottom: 5px;"></div> Action <div style="border: 1px solid black; padding: 2px; display: inline-block; width: 60px; height: 15px; border-radius: 10px; margin-bottom: 5px;"></div> Mode <div style="border: 1px solid black; padding: 2px; display: inline-block; width: 60px; height: 15px; border-radius: 10px; margin-bottom: 5px;"></div> Sequential transfer</div> </div>									

6.2.41 RDABCSDR: Read automatic brightness control self-diagnostic result (68h)

68H	RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	1	0	1	0	0	0	68
1 st parameter	1	D[7:6]		0	0	0	0	0	0	00
Description	This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out –command as described in the table below: Bit D7 – Register Loading Detection. See section “5.10.1 Register loading Detection”. Bit D6 – Functionality Detection. See section “5.10.2 Functionality Detection “. Bits D[5:0] are for future use and are set to ‘0’.									
Restriction	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	<div style="display: flex; align-items: center;"> <div style="margin-right: 20px;"> <p>Serial I/F Mode</p> <p>Read RDABCSDR</p> <p>Host</p> <p>↓</p> <p>Display</p> <p>Parameter</p> </div> <div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>									

6.2.42 Read_DDB_start (A1h)

A1H	Read_DDB_start									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	0	0	0	0	1	A1
1 st parameter	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2 nd parameter	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
:	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
N th parameter	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
Description	<p>This command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block (DDB) stored on the peripheral. The response to this command returns a sequence of bytes that may be any length up to 64K bytes. Note that the returned sequence of bytes does not necessarily correspond to the entire DDB; it may be a portion of a larger block of data.</p> <p>The format of returned data is as follows: Parameter 1: LS (least significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization. Parameter 2: MS (most significant) byte of Supplier ID. Parameter 3: LS (least significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example. Parameter 4: MS (most significant) byte of Supplier Elective Data Parameter 5: single-byte <i>Escape or Exit Code (EEC)</i>. The code is interpreted as follows: - FFh – Exit code – there is no more data in the Descriptor Block - 00h – Escape code – there is supplier-proprietary data in the Descriptor Block (does not conform to any MIPI standard) - Any other value – there is DDB data in the Descriptor Block. The format and interpretation of this data is documented in <i>MIPI Alliance Standard for Device Descriptor Block (DDB)</i>. DDBs may contain many more data fields providing information about the peripheral. In a DSI system, read activity takes the form of two separate transactions across the bus: first the read command read_DDB_start from host processor to peripheral, which includes the bus turn-around token. The peripheral then takes control of the bus and returns the requested data. The peripheral response to read_DDB_start is a Long Packet type, so its length may be up to 64K bytes unless limited by a previous set_max_return_size command. The response to a read_DDB_start command always starts at the beginning of the Device Descriptor Block. After receiving the first packet and processing the returned DDB data, the host processor may initiate a read_DDB_continue command to access the next portion of the DDB. A read_DDB_continue command begins the next read at the location following the last byte of the previous data read from the DDB. Subsequent read_DDB_continue commands can be used to read a DDB or supplier-proprietary block of arbitrary size. There is, however, no obligation to read the entire block. The host processor may choose to stop reading after completion of any read_DDB_xxx command.</p>									
Restrictions	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					PA1st-4 th is OTP value, PA5th is FFh				
	S/W Reset					No change				
	H/W Reset					PA1st-4 th is OTP value, PA5th is FFh				



Himax Confidential
Do Not Copy

6.2.43 Read_DDB_continue (A8h)

A8H	Read_DDB_continue									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	0	1	0	0	0	A8
1 st parameter	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2 nd parameter	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
:	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
N th parameter	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
Description	A read_DDB_start command should be executed at least once before a read_DDB_continue command to define the read location. Otherwise, data read with a read_DDB_continue command is undefined.									
Restrictions	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					Without A1h read, 1 st ~4 th read is the same as A8h 1 st ~4 th OTP value, after 5 th read is FFh.				
	S/W Reset					No change				
	H/W Reset					Without A1h read, 1 st ~4 th read is the same as A8h 1 st ~4 th OTP value, after 5 th read is FFh.				
Flow Chart	<pre> graph TD A[Read_DDB_continue] --> B(DDB D1[7:0], D2[7:0], ..., Dn[7:0]) B --> C[Any Command] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Trapezoid Action: Arrow Mode: Rounded Rectangle Sequential transfer: Speech Bubble 									

6.2.44 RDID1: Read ID1 (DAh)

DAH	RDID1 (Read ID1)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	1	1	0	1	0	DA
1 st parameter	1	ID1[7:0]								83
Description	This read byte identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX.									
Restriction	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					OTP value				
	S/W Reset					No change				
	H/W Reset					OTP value				
Flow Chart	<div style="display: flex; justify-content: space-between; align-items: center;"> <div style="text-align: center;"> <p>Serial I/F Mode</p> </div> <div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>									

6.2.45 RDID2: Read ID2 (DBh)

DBH	RDID2 (Read ID2)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	1	1	0	1	1	DB
1 st parameter	1	ID2[7:0]								99
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications.									
Restriction	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					OTP value				
	S/W Reset					No change				
	H/W Reset					OTP value				
Flow Chart	<div style="display: flex; justify-content: space-between; align-items: center;"> <div style="text-align: center;"> <p>Serial I/F Mode</p> <pre> graph TD subgraph Host C[Read ID2] end subgraph Display P[/Parameter/] end C --> P </pre> </div> <div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> ▭ Command ▱ Parameter ◀ Display ▶ Action ○ Mode ⌚ Sequential transfer </div> </div>									

6.2.46 RDID3: Read ID3 (DCh)

DCH	RDID3 (Read ID3)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	1	1	1	0	0	DC
1 st parameter	1	ID3[7:0]								0C
Description	This read byte identifies the LCD module/driver.									
Restriction	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				
Default	Status					Default Value				
	Power On Sequence					OTP value				
	S/W Reset					No change				
	H/W Reset					OTP value				
Flow Chart	<div style="display: flex; justify-content: space-between; align-items: center;"> <div style="text-align: center;"> <p>Serial I/F Mode</p> <pre> graph TD subgraph "Serial I/F Mode" A[Read ID3] --> B[/Parameter/] end B --- C[Host Display] </pre> </div> <div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>									

6.3 User define command description

6.3.1 SETSEQUENCE: Set Sequence (B0h)

B0H	SETSEQUENCE(Set Sequence)																												
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	0	1	1	0	0	0	0	B0																			
1 st parameter	1	-	-	-	-	-	-	-	-	00																			
2 nd parameter	1	-	-	-	-	-	-	-	OSC_EN	00																			
3 rd parameter	1	-	1	1	1	1	1	-	STB	7D																			
4 th parameter	1	-	-	-	-	GON	DTE	D[1:0]		0C																			
Description	This command is used for DCS command auto sequence and manual mode debug use, please don't access this command in initial code.																												
	OSC_EN: Enable internal oscillator. "1": Enable; "0": Disable.																												
	STB: When STB = "1", the HX8399-C enters the standby mode																												
	GON: GIP control signal enable selection																												
	<table border="1"> <thead> <tr> <th>GON</th> <th>GIP Enable</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>GIP Off</td> </tr> <tr> <td>1</td> <td>GIP On</td> </tr> </tbody> </table>										GON	GIP Enable	0	GIP Off	1	GIP On													
GON	GIP Enable																												
0	GIP Off																												
1	GIP On																												
DTE: Source output enable selection																													
<table border="1"> <thead> <tr> <th>DTE</th> <th>Source Output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Source output off</td> </tr> <tr> <td>1</td> <td>Source output on</td> </tr> </tbody> </table>										DTE	Source Output	0	Source output off	1	Source output on														
DTE	Source Output																												
0	Source output off																												
1	Source output on																												
D[1:0]: Setting Source driver output																													
<table border="1"> <thead> <tr> <th>D1</th> <th>D0</th> <th>Source Output</th> <th>HX8399-C Internal Operations</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Halt</td> <td>Halt</td> </tr> <tr> <td>0</td> <td>1</td> <td>Blanking or GND</td> <td>GIP initial sequence</td> </tr> <tr> <td>1</td> <td>0</td> <td>V255 or V0</td> <td>Blanking</td> </tr> <tr> <td>1</td> <td>1</td> <td>Normal</td> <td>Operate</td> </tr> </tbody> </table>										D1	D0	Source Output	HX8399-C Internal Operations	0	0	Halt	Halt	0	1	Blanking or GND	GIP initial sequence	1	0	V255 or V0	Blanking	1	1	Normal	Operate
D1	D0	Source Output	HX8399-C Internal Operations																										
0	0	Halt	Halt																										
0	1	Blanking or GND	GIP initial sequence																										
1	0	V255 or V0	Blanking																										
1	1	Normal	Operate																										
Restrictions	SETEXTC turn on to enable this command.																												
Register Availability	Status					Availability																							
	Normal Mode On, Idle Mode Off, Sleep Out					Yes																							
	Normal Mode On, Idle Mode On, Sleep Out					Yes																							
	Sleep In or Booster Off					Yes																							

6.3.2 SETPOWER: Set power related register (B1h)

B1H	SETPOWER(Set power related setting)																																													
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	0	1	0	1	1	0	0	0	1	B1																																				
Bank0 1 st parameter	1	-	-	-	-	-	-	DSTB_OPT	DSTB	02																																				
2 nd parameter	1	-	-	-	-	VSP_FBOFF	AP[2:0]			04																																				
3 rd parameter	1	-	VCI_LDOS[1:0]		VRHP[4:0]					72																																				
4 th parameter	1	VPPS[2:0]			VRHN[4:0]					92																																				
5 th parameter	1	-	-	-	-	-	XDK[2:0]			01																																				
6 th parameter	1	-	-	CLK_OPT2	CLK_OTP1	FS0[3:0]					32																																			
7 th parameter	1	FS1[3:0]				FS2[3:0]					33																																			
8 th parameter	1	-	-	-	BTP[4:0]					11																																				
9 th parameter	1	-	-	-	BTN[4:0]					11																																				
10 st parameter	1	VGHS[7:0]								B3																																				
11 nd parameter	1	VGLS[7:0]								6B																																				
12 rd parameter	1	DT1[1:0]		DT2[1:0]		DCDIV[3:0]				56																																				
13 th parameter	1	-	DCS[2:0]			-	DC[2:0]			73																																				
14 th parameter	1	-	DTPS[2:0]			-	DTP[2:0]			02																																				
15 th parameter	1	-	DTNS[2:0]			-	DTN[2:0]			02																																				
Bank1 1 st parameter	1	-	APP_EN	GASIOVCC_OPT1[1:0]		-	GASVCI_OPT[2:0]			64																																				
2 nd parameter	1	-	GASVSN_OPT[2:0]			-	GASVSP_OPT[2:0]			44																																				
3 rd parameter	1	-	-	GASVGL_OPT[1:0]		-	GASVGH_OPT[1:0]			11																																				
Description	<p>This command is used to set related setting of power.</p> <p>DSTBY_OPT: DSTB mode option. When DSTBY_OPT=0, logic power will be off and must HWRESET to leave deep standby mode.</p> <p>DSTB: Set '1' to enter deep standby mode for saving power in SLPIN mode. User must enter SLPIN mode before enter deep standby mode and leave deep stand by mode before SLPOUT.</p> <p>VSP_FBOFF: VSP voltage feedback to control VSP pumping clock operation. "1" no feedback. For HX5186 mode, no effect for PFM circuit. When AUTO_XDK=0, set VSP at fixed pumping ratio</p> <p>AP[2:0]: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption. During no display operation, when AP[2:0] = 000, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.</p> <table border="1"> <thead> <tr> <th>AP2</th> <th>AP1</th> <th>AP0</th> <th>Constant Current of Operational Amplifier</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Stop</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0.5μA</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1.0μA</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1.5μA</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>2.0μA</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>2.5μA</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>3.0μA</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>3.5μA</td> </tr> </tbody> </table>										AP2	AP1	AP0	Constant Current of Operational Amplifier	0	0	0	Stop	0	0	1	0.5μA	0	1	0	1.0μA	0	1	1	1.5μA	1	0	0	2.0μA	1	0	1	2.5μA	1	1	0	3.0μA	1	1	1	3.5μA
AP2	AP1	AP0	Constant Current of Operational Amplifier																																											
0	0	0	Stop																																											
0	0	1	0.5μA																																											
0	1	0	1.0μA																																											
0	1	1	1.5μA																																											
1	0	0	2.0μA																																											
1	0	1	2.5μA																																											
1	1	0	3.0μA																																											
1	1	1	3.5μA																																											

VCI_LDOS[1:0]: Set the regulated voltage of VDD3 in external VSP mode.
(PCCS[2:0]= 010 or 011)

VCI_LDOS 1	VCI_LDOS 0	VDD3 threshold voltage
0	0	2.4V
0	1	3.0V
1	0	3.3V
1	1	3.6V

VRHP[4:0]: VSPR regulator output control setting for source data output driving.

VRHP[4:0]					VSPR Voltage
0	0	0	0	0	Inhibited
0	0	0	0	1	3.1V
0	0	0	1	0	3.2V
0	0	0	1	1	3.3V
0	0	1	0	0	3.4V
0	0	1	0	1	3.5V
0	0	1	1	0	3.6V
0	0	1	1	1	3.7V
0	1	0	0	0	3.8V
0	1	0	0	1	3.9V
0	1	0	1	0	4.0V
0	1	0	1	1	4.1V
0	1	1	0	0	4.2V
0	1	1	0	1	4.3V
0	1	1	1	0	4.4V
0	1	1	1	1	4.5V
1	0	0	0	0	4.6V
1	0	0	0	1	4.7V
1	0	0	1	0	4.8V
1	0	0	1	1	4.9V
1	0	1	0	0	5.0V
1	0	1	0	1	5.1V
1	0	1	1	0	5.2V
1	0	1	1	1	5.3V
1	1	0	0	0	5.4V
1	1	0	0	1	5.5V
1	1	0	1	0	5.6V
1	1	0	1	1	5.7V
1	1	1	0	0	5.8V
Others					Inhibited

VRHN[4:0]: VSNR regulator output control setting for source data output driving

VRHN[4:0]					VSNR Voltage
0	0	0	0	0	Inhibited
0	0	0	0	1	-3.1V
0	0	0	1	0	-3.2V
0	0	0	1	1	-3.3V
0	0	1	0	0	-3.4V
0	0	1	0	1	-3.5V
0	0	1	1	0	-3.6V
0	0	1	1	1	-3.7V
0	1	0	0	0	-3.8V
0	1	0	0	1	-3.9V
0	1	0	1	0	-4.0V
0	1	0	1	1	-4.1V
0	1	1	0	0	-4.2V
0	1	1	0	1	-4.3V

0	1	1	1	0	-4.4V
0	1	1	1	1	-4.5V
1	0	0	0	0	-4.6V
1	0	0	0	1	-4.7V
1	0	0	1	0	-4.8V
1	0	0	1	1	-4.9V
1	0	1	0	0	-5.0V
1	0	1	0	1	-5.1V
1	0	1	1	0	-5.2V
1	0	1	1	1	-5.3V
1	1	0	0	0	-5.4V
1	1	0	0	1	-5.5V
1	1	0	1	0	-5.6V
1	1	0	1	1	-5.7V
1	1	1	0	0	-5.8V
Others					Inhibited

VPPS[2:0]: Set VPP output voltage for OTP.

VPPS[2:0]			VPP voltage
0	0	0	8.0V
0	0	1	8.1V
0	1	0	8.2V
0	1	1	8.25V
1	0	0	8.3V
1	0	1	8.4V
1	1	0	8.5V
1	1	1	External from VGH

XDK[2:0]: Setting charge pump mode of VSP Voltage

XDK2	XDK1	XDK0	VSP
0	0	0	inhibit
0	0	1	X2
0	1	0	X1.5
0	1	1	inhibit
1	0	0	inhibit
1	0	1	inhibit
1	1	0	inhibit
1	1	1	X3

CLK_OPT0: The pumping clock of VGH will reset with Hsync when CLK_OPT0 = 1.

CLK_OPT1: The pumping clock of VGL will reset with Hsync when CLK_OPT2 = 1.

FS0[3:0]: Set the operating frequency of the step-up circuit for VSP and VSN voltage generation. (Fosc_pump=5.68MHz)

FS03	FS02	FS01	FS00	Operation Frequency of Step-up Circuit
0	0	0	0	Fosc_pump/2
0	0	0	1	Fosc_pump/4
0	0	1	0	Fosc_pump/8
0	0	1	1	Fosc_pump/16
0	1	0	0	Fosc_pump/32
0	1	0	1	Fosc_pump/48
0	1	1	0	Fosc_pump/64
0	1	1	1	Fosc_pump/80
1	0	0	0	Fosc_pump/96
1	0	0	1	Fosc_pump/112
1	0	1	0	Fosc_pump/128

1	0	1	1	Fosc_pump/144
1	1	0	0	Fosc_pump/160
1	1	0	1	Fosc_pump/176
1	1	1	0	Fosc_pump/192
1	1	1	1	Fosc_pump/208

FS1[3:0]: Set the operating frequency of the step-up circuit for VGH voltage generation. (Fosc_pump=5.68MHz)

FS13	FS12	FS11	FS10	Operation Frequency of Step-up Circuit
0	0	0	0	Fosc_pump/72
0	0	0	1	Fosc_pump/96
0	0	1	0	Fosc_pump/128
0	0	1	1	Fosc_pump/160
0	1	0	0	Fosc_pump/192
0	1	0	1	Fosc_pump/224
0	1	1	0	Fosc_pump/256
0	1	1	1	Fosc_pump/336
1	0	0	0	Hsync*4
1	0	0	1	Hsync*2
1	0	1	0	Hsync
1	0	1	1	Hsync/2
1	1	0	0	Hsync/4
1	1	0	1	Hsync/8
1	1	1	0	Hsync/16
1	1	1	1	Inhibited

FS2[3:0]: Adjust the charge pump frequency of internal VGL. (Fosc_pump=5.68MHz)

FS23	FS22	FS21	FS20	Operation Frequency of Step-up Circuit
0	0	0	0	Fosc_pump/72
0	0	0	1	Fosc_pump/96
0	0	1	0	Fosc_pump/128
0	0	1	1	Fosc_pump/160
0	1	0	0	Fosc_pump/192
0	1	0	1	Fosc_pump/224
0	1	1	0	Fosc_pump/256
0	1	1	1	Fosc_pump/336
1	0	0	0	Hsync*4
1	0	0	1	Hsync*2
1	0	1	0	Hsync
1	0	1	1	Hsync/2
1	1	0	0	Hsync/4
1	1	0	1	Hsync/8
1	1	1	0	Hsync/16
1	1	1	1	Inhibited

BTP[4:0]: Switch the output factor for DC/DC circuit for VSP voltage generation. The LCD drive voltage level VSP can be selected according to the characteristic of liquid crystal which panel used.

BTP4	BTP3	BTP2	BTP1	BTP0	VSP Voltage
0	0	0	0	0	3.00V
0	0	0	0	1	3.15V
0	0	0	1	0	3.30V
0	0	0	1	1	3.45V
0	0	1	0	0	3.60V
:					:
1	0	0	0	0	5.40V
1	0	0	0	1	5.55V
1	0	0	1	0	5.70V
1	0	0	1	1	5.85V

1	0	1	0	0	6.00V
1	0	1	0	1	6.15V
1	0	1	1	0	6.30V
1	0	1	1	1	6.45V
1	1	0	0	0	6.60V
1	1	0	0	1	6.75V
Others					Inhibited

BTN[4:0]: Switch the output factor of DC/DC circuit for VSN voltage generation. The LCD drive voltage level VSN can be selected according to the characteristic of liquid crystal which panel used.

BTN4	BTN3	BTN2	BTN1	BTN0	VSN Voltage
0	0	0	0	0	-3.00V
0	0	0	0	1	-3.15V
0	0	0	1	0	-3.30V
0	0	0	1	1	-3.45V
0	0	1	0	0	-3.60V
:					:
1	0	0	0	0	-5.40V
1	0	0	0	1	-5.55V
1	0	0	1	0	-5.70V
1	0	0	1	1	-5.85V
1	0	1	0	0	-6.00V
1	0	1	0	1	-6.15V
1	0	1	1	0	-6.30V
1	0	1	1	1	-6.45V
1	1	0	0	0	-6.60V
1	1	0	0	1	-6.75V
Others					Inhibited

VGHS[7:6]: Specify the VGH voltage source.

VGHS7	VGHS6	VGH Voltage
0	0	VDD1-VSN
0	1	VSP-VSN
1	0	VSP-VSN+VDD1
1	1	2*VSP -VSN

VGHS[5:0]: VGH regulator output voltage setting. The LCD drive voltage level VGH can be selected according to the characteristic of liquid crystal which panel used.

VGHS5	VGHS4	VGHS3	VGHS2	VGHS1	VGHS0	VGH Voltage
0	0	0	0	0	0	6.7V
0	0	0	0	0	1	6.8V
0	0	0	0	1	0	6.9V
0	0	0	0	1	1	7.0V
:						:
1	0	0	1	0	0	10.3V
:						:
1	1	1	1	0	1	12.8V
1	1	1	1	1	0	12.9v
1	1	1	1	1	1	13.0V

VGLS[7:6]: Specify the VGL voltage source.

VGLS7	VGLS6	VGL Voltage
0	0	VSN-VDD3
0	1	VSN-VSP
1	0	2*VSN-VDD3
1	1	2*VSN-VSP

VGLS[5:0]: VGL regulator output voltage setting. The LCD drive voltage level VGL can be selected according to the characteristic of liquid crystal which panel used.

VGLS5	VGLS4	VGLS3	VGLS2	VGLS1	VGLS0	VGL Voltage
0	0	0	0	0	0	-5.7V
0	0	0	0	0	1	-5.8V
0	0	0	0	1	0	-5.9V
0	0	0	0	1	1	-6.0V
:						:
0	0	1	1	1	0	-7.1V
:						:
1	1	1	1	0	1	-11.8V
1	1	1	1	1	0	-11.9V
1	1	1	1	1	1	-12.0V

DT1[1:0]: Delay time of power on and power off sequence.

DT1[1:0]	Delay time of power on and power off sequence
0 0	0ms
0 1	2.5ms
1 0	5ms
1 1	7.5ms

DT2[1:0]: Delay time of power on and power off sequence.

DT2[1:0]	Delay time of power on and power off sequence
0 0	0ms
0 1	2.5ms
1 0	5ms
1 1	7.5ms

DCDIV[3:0]: Set the normal operate frequency FoscD of DC/DC converter circuit during normal mode. (Fosc=100MHz)

DCDIV[3:0]				Normal operate frequency of DC/DC converter(foscD)
0	0	0	0	Fosc/1
0	0	0	1	Fosc/2
0	0	1	0	Fosc/3
0	0	1	1	Fosc/4
0	1	0	0	Fosc/5
0	1	0	1	Fosc/6
0	1	1	0	Fosc/7
0	1	1	1	Fosc/8
1	0	0	0	Fosc/9
1	0	0	1	Fosc/10
1	0	1	0	Fosc/11
1	0	1	1	Fosc/12
1	1	0	0	Fosc/13
1	1	0	1	Fosc/14
1	1	1	0	Fosc/15
1	1	1	1	Fosc/16

DCS[2:0]: Soft start VSP/VSN frequency of DC/DC clock.

DCS[2:0]	Operation Frequency of DC/DC Clock
0 0 0	foscD/4
0 0 1	foscD/5
0 1 0	foscD/6
0 1 1	foscD/7
1 0 0	foscD/8
1 0 1	foscD/10

1	1	0	foscD/11
1	1	1	foscD/12

DC[2:0]: Operation VSP/VSN frequency of DC/DC clock.

DC[2:0]			Operation Frequency of DC/DC Clock
0	0	0	foscD/4
0	0	1	foscD/5
0	1	0	foscD/6
0	1	1	foscD/7
1	0	0	foscD/8
1	0	1	foscD/10
1	1	0	foscD/11
1	1	1	foscD/12

DTPS[3:0]: For PFM circuit. Set the soft start operating duty cycle of DC/DC circuit.

DTPS[2:0]			Soft start operation duty of VSP
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

DTP[3:0]: For PFM circuit. Set the operating duty cycle of DC/DC clock for VSP.

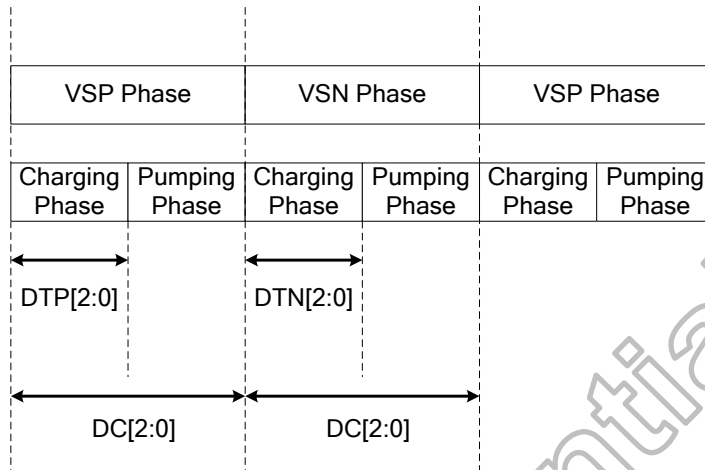
DTP[2:0]			Operation duty of VSP
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

DTNS[3:0]: For PFM circuit. Set the soft start operating duty cycle of DC/DC circuit.

DTNS[2:0]			Soft start operation duty of VSN
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

DTN[3:0]: For PFM circuit. Set the operating duty cycle of DC/DC clock for VSN.

DTN[2:0]			Operation duty of VSN
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8



APF_EN: Abnormal power-off detection enable(GAS function). "1": Enable.

GASIOVCC_OPT[1:0]: Set VDD1 threshold voltage of GAS function.

GASIOVCC_OPT[1:0]		GAS threshold VDD1 voltage
0	0	1.2V
0	1	1.3V
1	0	1.4V
1	1	1.5V

GASVCI_OPT[2:0]: Set VDD3 threshold voltage of GAS function.

GASVCI_OPT[2:0]			GAS threshold VDD3 voltage
0	0	0	1.9V
0	0	1	2.0V
0	1	0	2.1V
0	1	1	2.2V
1	0	0	2.3V
1	0	1	2.4V
1	1	0	2.5V
1	1	1	2.6V

GASVSN_OPT[2:0]: Set VSN threshold voltage of GAS function.

GASVSN_OPT[2:0]			GAS threshold VSN voltage
0	0	0	-2.8V
0	0	1	-3.0V
0	1	0	-3.2V
0	1	1	-3.4V
1	0	0	-3.6V
1	0	1	-3.8V
1	1	0	-4.0V
1	1	1	-4.2V

GASVSP_OPT[2:0]: Set VSP threshold voltage of GAS function.

GASVSP_OPT[2:0]			GAS threshold VSP voltage
0	0	0	2.8V
0	0	1	3.0V
0	1	0	3.2V
0	1	1	3.4V
1	0	0	3.6V
1	0	1	3.8V
1	1	0	4.0V
1	1	1	4.2V

	GASVGH_OPT[1:0]: Set VGH threshold voltage of GAS function.																
	<table border="1"> <thead> <tr> <th colspan="2">GASVGH_OPT[1:0]</th> <th>GAS threshold VGH voltage</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>6V</td> </tr> <tr> <td>0</td> <td>1</td> <td>7V</td> </tr> <tr> <td>1</td> <td>0</td> <td>8V</td> </tr> <tr> <td>1</td> <td>1</td> <td>9V</td> </tr> </tbody> </table>		GASVGH_OPT[1:0]		GAS threshold VGH voltage	0	0	6V	0	1	7V	1	0	8V	1	1	9V
GASVGH_OPT[1:0]		GAS threshold VGH voltage															
0	0	6V															
0	1	7V															
1	0	8V															
1	1	9V															
Restrictions	SETEXTC turn on to enable this command.																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes							
Status	Availability																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																
Normal Mode On, Idle Mode On, Sleep Out	Yes																
Sleep In or Booster Off	Yes																

Himax Confidential
Do Not Copy

6.3.3 SETDISP: Set display related register (B2h)

B2H	SETDISP(Set display related register)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	0	0	1	0	B2
Bank0 1 st parameter	1	-	ZZ_LR	ZZ_E O	ZZ_2P L	-	NW[2:0]			40
2 nd parameter	1	MUX_ SEL	-	-	-	TGS[3:0]			00	
3 rd parameter	1	MESS I_ENB	-	-	-	-	-	-	-	80
4 th parameter	1	NL[7:0]								AE
5 th parameter	1	BP [7:0]								08
6 th parameter	1	FP [7:0]								08
7 th parameter	1	RTN[7:0]								5A
8 th parameter	1	-	END_ SET	END_SET_0[1:0]		-	INIT_ S ET	INIT_SET_0[1:0]		00
9 th parameter	1	-	-	INIT_SET_1[1:0]		-	-	-	-	00
10 th parameter	1	-	-	END_SET_1[1: 0]		-	-	-	-	00
11 st parameter	1	-	-	INIT_ SD_S EL	INIT_ VCOM _SEL	-	-	END_ SD_S EL	END_ VCOM _SEL	00
Bank1 1 st parameter	1	FRM_PATTERN_CYCLE[3:0]				DISP_ BIST_ EN	FRM_SCAN_CYCLE[2:0]			C0
2 nd parameter	1	PTN_2ND_NUM[3:0]				PTN_1ST_NUM[3:0]				10
3 rd parameter	1	PTN_4TH_NUM[3:0]				PTN_3RD_NUM[3:0]				32
4 th parameter	1	PTN_6TH_NUM[3:0]				PTN_5TH_NUM[3:0]				54
5 th parameter	1	PTN_8TH_NUM[3:0]				PTN_7TH_NUM[3:0]				76
6 th parameter	1	PTN_10TH_NUM[3:0]				PTN_9TH_NUM[3:0]				98
7 th parameter	1	PTN_12TH_NUM[3:0]				PTN_11TH_NUM[3:0]				BA
8 th parameter	1	PTN_14TH_NUM[3:0]				PTN_13TH_NUM[3:0]				DC
9 th parameter	1	PTN_16TH_NUM[3:0]				PTN_15TH_NUM[3:0]				FE

Description	This command is used to set display related register									
	ZZ_LR: Zig-zag Left / Right mode selection.									
	ZZ_LR		Zig-zag Left / Right mode selection							
	0		SL1~S1080							
	1		S1~SR1							
	ZZ_EO: Zig-zag Odd / Even mode selection.									
	ZZ_EO		Zig-zag Odd / Even mode selection							
	0		Odd-line shift							
	1		Even-line shift							
	ZZ_2PL: Zig-zag 1H/2H selection when NW[2:0]=101									
ZZ_2PL		Zig-zag 1H/2H selection								
0		1H Zig-zag								
1		2H Zig-zag								
NW[2:0]: Inversion type setting.										
NW2			NW1			NW0			Inversion type	
0			0			0			Column inversion	
0			0			1			1-dot inversion	
0			1			0			2-dot inversion	

0	1	1	4-dot inversion
1	0	0	8-dot inversion
1	0	1	Zig-zag inversion
1	1	1	Pixel-column inversion

MUX_SEL: Source driver switch select.

0: Setting 1:3 MUX

1: Setting 2:6 MUX

TGS[2:0]: Source switch sequence select.

TGS2	TGS1	TGS0	TG sequence
0	0	0	SW1→SW2→SW3
0	0	1	SW1→SW3→SW2
0	1	0	SW2→SW1→SW3
0	1	1	SW2→SW3→SW1
1	0	0	SW3→SW1→SW2
1	0	1	SW3→SW2→SW1

TGS[3]: Set "1" to enable RGB-BGR function.

※When enable this function, vertical porch total(VSA+VBP+VFP) must be even number.

MESSI_ENB: Support Nokia DCS enable bit. "0" Enable.

0: support Nokia, don't support 44h CMD

1: support 44h CMD to adjust the position of TE(horizontal)

NL[7:0]: Setting the number of lines to drive the LCD at an interval of 8 lines. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel. If user want to use this function.

NL[7:0]								Lines
0	0	0	0	0	0	0	0	528
0	0	0	0	0	0	0	1	536
⋮								⋮
1	0	1	0	1	1	1	0	1920
⋮								⋮
1	1	1	0	1	0	1	0	2400
Others								Inibited

BP[7:0] : Specify the amount of scan line for back porch(BP) in blanking.

FP[7:0]: Specify the amount of scan line for front porch (FP) in blanking.

FP[7:0] / BP[7:0]	Number of front porch/ back porch Lines
8h'00	2 lines
8h'01	3 lines
8h'02	4 lines
8h'03	5 lines
8h'04	6 lines
8h'05	7 lines
⋮	⋮
8h'FB	253 lines
8h'FC	254 lines
8h'FD	255 lines
8h'FE	256 lines

8h'FF	257 lines
-------	-----------

Note: Set BP[7:0] = VS + VBP - 2, and FP[7:0] = VFP - 2.

RTN[7:0]: A cycle time of line width in blanking.
(1 clock period= 4 OSC period)

RTN[7:0]	Clock per Line
8h'00	150 clocks
8h'01	151 clocks
8h'02	152 clocks
:	:
8h'FD	403 clocks
8h'FE	404 clocks
8h'FF	405 clocks

INIT_SET_X/END_SET_X: GIP control at D[1:0]=01, GIP state set by RD8h

INIT_SET	INIT_SET_0[1:0]/ INIT_SET_1[1:0]	Time or Frame	By time/frame
0	00	0 frame	By frame
0	01	1 frame	By frame
0	10	2 frames	By frame
0	11	3 frames	By frame
1	00	8ms	By time
1	01	16ms	By time
1	10	24ms	By time
1	11	32ms	By time

END_SET	END_SET_0[1:0]/ END_SET_1[1:0]	Time or Frame	By time/frame
0	00	0 frame	By frame
0	01	1 frame	By frame
0	10	2 frames	By frame
0	11	3 frames	By frame
1	00	8ms	By time
1	01	16ms	By time
1	10	24ms	By time
1	11	32ms	By time

Note: INIT means SLPin to SLPOUT

END means SLPout to SLPIN

INIT_SD_SEL/END_SD_SEL: Source driver voltage control at D[1:0]=01

INIT_SD_SEL /END_SD_SEL	Voltage level
0	GND
1	Blanking

INIT_VCOM_SEL/END_VCOM_SEL: VCOM voltage control at D[1:0]=01

INIT/END_VCOM_SEL	Voltage level
0	GND
1	VCMC_F/VCMC_B

DISP_BIST_EN: Set "1" enable SW free running mode.

FRM_PATTERN_CYCLE[3:0]: Number of Free-running mode pattern.

FRM_PATTERN_CYCLE[3:0]	Free-running mode pattern number

0000	1 pattern
0001	2 patterns
0002	3 patterns
:	:
1101	14 patterns
1110	15 patterns
1111	16 patterns

PTN_nST_NUM[3:0]: select n_th frame pattern in free-running mode.

PTN_xST_NUM[3:0]	Free-running mode pattern number
0000	White
0001	Black
0010	Red
0011	Green
0100	Blue
0101	Gray127
0110	Gray128
0111	Color Bar
1000	H-Grayscale Gradation
1001	V-Grayscale Gradation
1010	Cross-Talk: white square in black pattern
1011	Cross-Talk: black square in white pattern
1100	Dot Checker: 2x2
1101	Dot Checker: 1x1
Others	Inhibited

FRM_SCAN_CYCLE[2:0]: Free-running each pattern keeps time.

FRM_SCAN_CYCLE[2:0]	Free-running mode pattern keep time
000	1 s
001	2 s
010	4 s
011	8 s
Others	Inhibited

Restrictions SETEXTC turn on to enable this command.

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

6.3.4 SETCYC: Set display waveform cycles (B4h)

B4H	SETCYC(Set panel driving timing)											
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	0	1	1	0	1	0	0	B4		
1 st parameter	1	GEN_ON[7:0]									00	
2 nd parameter	1	GEN_OFF[7:0]									FF	
3 rd parameter	1	SPON[7:0]									03	
4 th parameter	1	SPOFF[7:0]									38	
5 th parameter	1	CON[7:0]									0A	
6 th parameter	1	COFF[7:0]									8D	
7 th parameter	1	CON1[7:0]									05	
8 th parameter	1	COFF1[7:0]									36	
9 th parameter	1	N_t1[7:0]									00	
10 th parameter	1	N_t2[7:0]									18	
11 st parameter	1	N_t3[7:0]									02	
12 nd parameter	1	N_t4[7:0]									02	
13 rd parameter	1	N_t5[7:0]									00	
14 th parameter	1	N_t6[7:0]									2C	
15 th parameter	1	N_t7[7:0]									02	
16 th parameter	1	N_t8[7:0]									04	
17 th parameter	1	N_t9[7:0]									04	
18 th parameter	1	SAP[3:0]							SAP1_N[3:0]			22
19 th parameter	1	-	-	-	-	-	SAP2[2:0]				03	
20 th parameter	1	-	-	-	-	EQT[3:0]				00		
21 st parameter	1	N_t10[7:0]									00	
22 nd parameter	1	SON[7:0]									00	
23 rd parameter	1	SOFF[7:0]									FF	
24 th parameter	1	DX2_TON[7:0]									3A	
25 th parameter	1	SPON_MPU[7:0]									03	
26 th parameter	1	SPOFF_MPU[7:0]									38	
27 th parameter	1	CON_MPU[7:0]									0A	
28 th parameter	1	COFF_MPU[7:0]									8D	
29 th parameter	1	CON1_MPU[7:0]									05	
30 th parameter	1	COFF1_MPU[7:0]									36	
31 st parameter	1	N_t1_MPU[7:0]									00	
32 nd parameter	1	N_t2_MPU[7:0]									18	
33 rd parameter	1	N_t3_MPU[7:0]									02	
34 th parameter	1	N_t4_MPU[7:0]									02	
35 th parameter	1	N_t5_MPU[7:0]									00	
36 th parameter	1	N_t6_MPU[7:0]									2C	
37 th parameter	1	N_t7_MPU[7:0]									02	
38 th parameter	1	N_t8_MPU[7:0]									04	
39 th parameter	1	N_t9_MPU[7:0]									04	
40 th parameter	1	-	-	-	-	EQT_MPU[3:0]				05		
41 st parameter	1	N_t10_MPU[7:0]									00	
42 nd parameter	1	SON_MPU[7:0]									10	
43 rd parameter	1	SOFF_MPU[7:0]									75	
44 th parameter	1	DX2OFF [7:0]									3A	
Description	This command is used to set display waveform cycles.											
	<p>GEN_ON[7:0]: Gamma OP turned on timing (in-house function not open).</p> <p>GEN_OFF[7:0]: Gamma OP turned off timing (in-house function not open).</p> <p>SPON[7:0]: Fine tune the Start and End signal delay from original starting point. (1 TCON CLK = 4 OSC)</p>											
	SPON[7:0]		Start / END signal output start delay									

0x00h	0 x TCON CLK
0x01h	1 x TCON CLK
0x02h	2 x TCON CLK
0x03h	3 x TCON CLK
:	
0xFEh	254 TCON CLK
0xFFh	255 TCON CLK

SPOFF[7:0]: Fine tune the Start and End signal ending point.

SPOFF[7:0]	Start / END signal output end delay
0x00h	0 x TCON CLK
0x01h	1 x TCON CLK
0x02h	2 x TCON CLK
0x03h	3 x TCON CLK
:	
0xFEh	254 x TCON CLK
0xFFh	255 x TCON CLK

Note: When output Start / End signal width is 1- Hsync only, set SPON[7:0] < SPOFF[7:0]

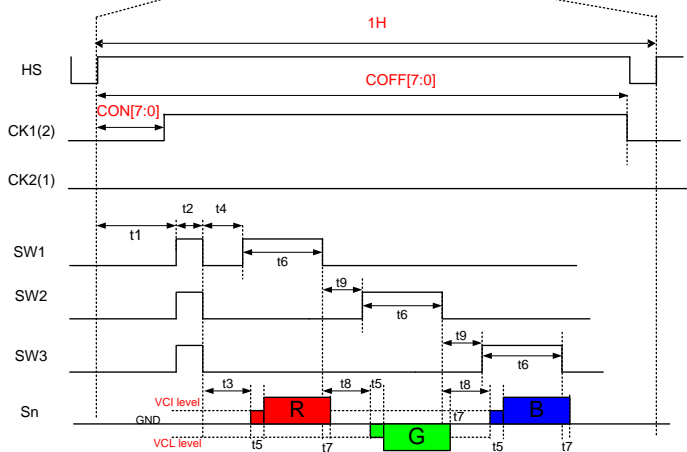
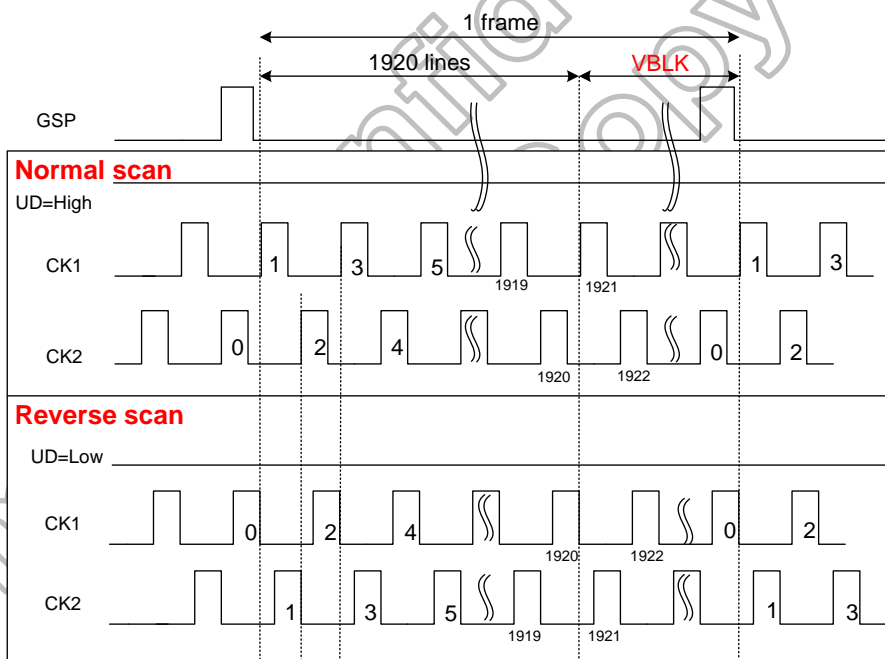
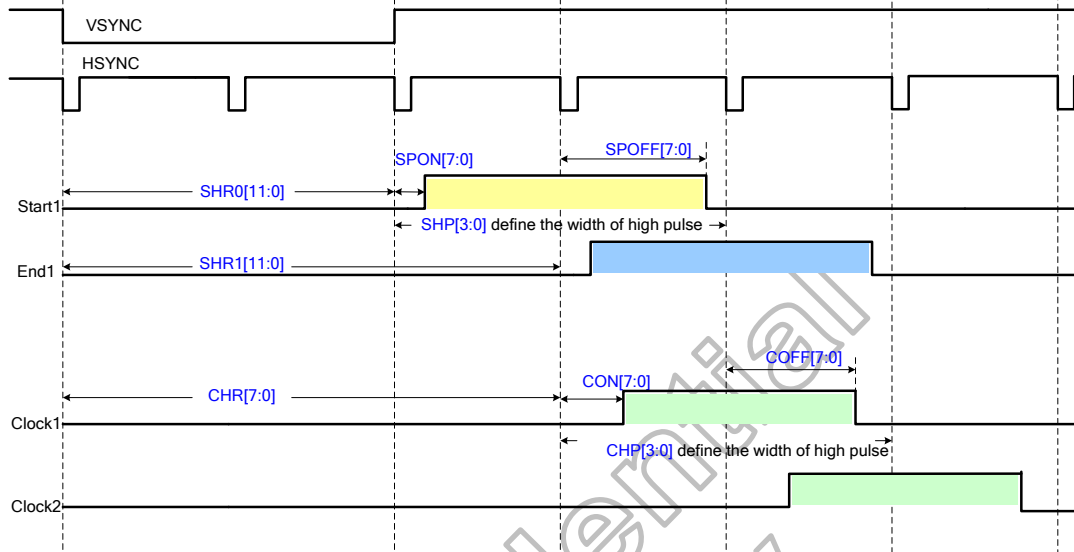
CON[7:0]/CON1[7:0]: Fine tune the Clock signal delay from original starting point.

CON[7:0]/CON1[7:0]	Clock signal output start delay
0x00h	0 x TCON CLK
0x01h	1 x TCON CLK
0x02h	2 x TCON CLK
0x03h	3 x TCON CLK
:	
0xFEh	254 TCON CLK
0xFFh	255 TCON CLK

COFF[7:0]/COFF1[7:0]: Fine tune the Clock signal ending point.

COFF[7:0]/COFF1[7:0]	Clock signal output end delay
0x00h	0 x TCON CLK
0x01h	1 x TCON CLK
0x02h	2 x TCON CLK
0x03h	3 x TCON CLK
:	
0xFEh	254 TCON CLK
0xFFh	255 TCON CLK

Note: When output Clock signal width is 1- Hsync only, set COFF[7:0] ≥ CON[7:0] + 2



N_t1~t9[7:0]: The timing definition of t1~t9.

N_t1~9[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x TCON CLK
0	0	0	0	0	0	0	1	1 x TCON CLK
0	0	0	0	0	0	1	0	2 x TCON CLK
0	0	0	0	0	0	1	1	3 x TCON CLK
0	0	0	0	0	1	0	0	4 x TCON CLK
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	0	252 x TCON CLK
1	1	1	1	1	1	0	1	253 x TCON CLK
1	1	1	1	1	1	1	0	254 x TCON CLK
1	1	1	1	1	1	1	1	255 x TCON CLK

N_t10[7:0]: Reserved.

SAP1_P[3:0]: 1st stage OP bias current adjust

SAP2[2:0]: class-AB (2nd) stage OP bias current adjust:

SAP2[2:0] (SAP1_P[3:0] =0011)			1 st stage OP	Class AB OP	Total
0	0	0	0.757 uA	0.224uA	0.981 uA
0	0	1	0.778 uA	0.245uA	1.023 uA
0	1	0	0.815 uA	0.271uA	1.086 uA
0	1	1	0.857 uA	0.306uA	1.163 uA
1	0	0	0.906 uA	0.346uA	1.252 uA
1	0	1	0.954 uA	0.383uA	1.337uA
1	1	0	1.008 uA	0.423uA	1.431 uA
1	1	1	1.059 uA	0.463uA	1.522 uA
1	1	1	1.059 uA	0.463uA	1.522 uA

Total OP biase current = 1st OP current + class-AB biase current

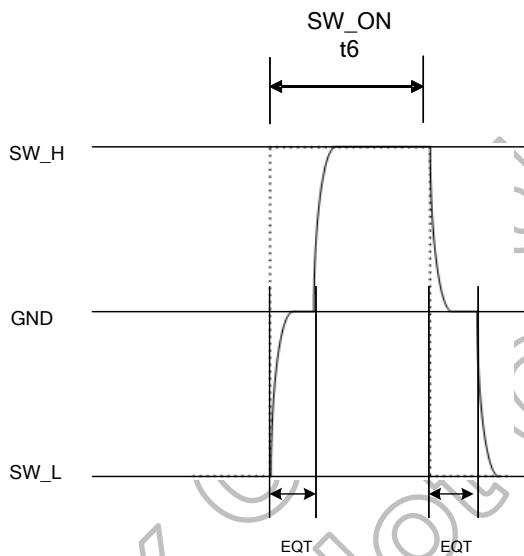
Different SAP1_P[3:0] will have map to diffent class-AB current setting

SAP1_P[3:0] (SAP2[2:0]=011)				1 st stage OP	Class AB OP	Total
0	0	0	0	0.222 uA	0.076 uA	0.298 uA
0	0	0	1	0.431 uA	0.149 uA	0.58 uA
0	0	1	0	0.657 uA	0.23 uA	0.887uA
0	0	1	1	0.857 uA	0.307 uA	1.164 uA
0	1	0	0	1.075 uA	0.392 uA	1.467 uA
0	1	0	1	1.269 uA	0.477 uA	1.746uA
0	1	1	0	1.484 uA	0.563 uA	2.047 uA
0	1	1	1	1.677 uA	0.644 uA	2.321 uA
1	0	0	0	1.888 uA	0.738 uA	2.626 uA
1	0	0	1	2.079 uA	0.823uA	2.902 uA
1	0	1	0	2.289 uA	0.916 uA	3.205 uA
1	0	1	1	2.476 uA	0.999 uA	3.475 uA
1	1	0	0	2.683 uA	1.096 uA	3.779 uA
1	1	0	1	2.874 uA	1.182 uA	4.056 uA
1	1	1	0	3.074 uA	1.277 uA	4.351 uA
1	1	1	1	3.258 uA	1.359 uA	4.617 uA

EQT[3:0]: Equalizing period of TG output.

EQT3	EQT2	EQT1	EQT0	Clock cycles
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3

0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15



SON[7:0]: Source OP turn on time.

SOFF[7:0]: Source OP turn off time.

SON[7:0]/SOFF[7:0]	Source OP turn on/off time
0x00h	0 x TCON CLK
0x01h	1 x TCON CLK
0x02h	2 x TCON CLK
:	
0xFEh	254 TCON CLK
0xFFh	255 TCON CLK

DX2OFF[7:0]: Source driving enhancement period setting.

DX2OFF_MPU[7:0]: Source driving enhancement period setting for blanking frame.

DX2OFF[7:0]/DX2OFF_MPU[7:0]	Set source enhancement time
0x00h	0 TCON CLK
0x01h	1 TCON CLK
0x02h	2 TCON CLK
0x03h	3 TCON CLK
:	
0xFEh	254 TCON CLK
0xFFh	255 TCON CLK

SPON_MPU[7:0]: Fine tune the Start and End signal delay from original starting point for blanking frame.

SPOFF_MPU[7:0]: Fine tune the Start and End signal ending point for blanking frame.

CON_MPU[7:0]/CON1_MPU[7:0]: Fine tune the Clock signal delay from original starting point for blanking frame.

COFF_MPU[7:0]/COFF1_MPU[7:0]: Fine tune the Clock signal ending point for blanking frame.

SON_MPU[7:0]: Source OP turn on time for blanking frame.

SOFF_MPU[7:0]: Source OP turn off time for blanking frame.

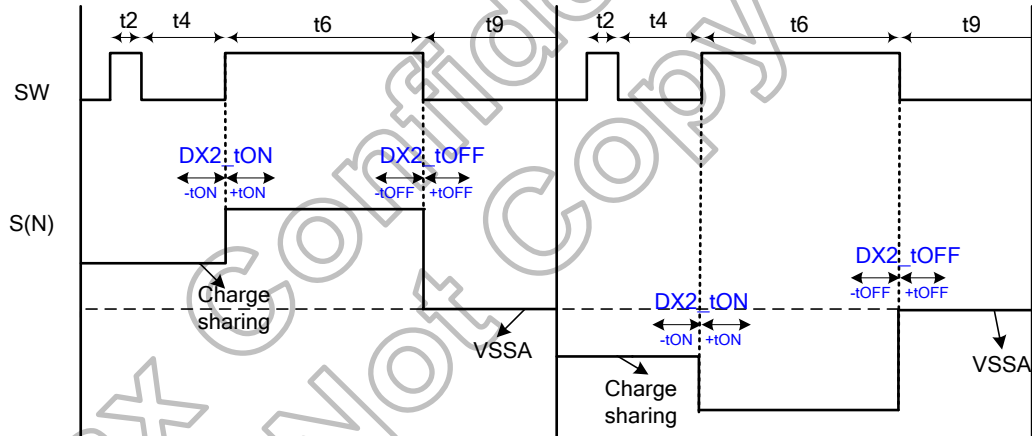
N_t1~t9_MPU[7:0]: The timing definition of t1~t9 for blanking frame.

N_t10_MPU[7:0]: Reserved.

EQT_MPU[3:0]: Equalizing period of TG output for blanking frame.

DX2_TON[7]: 1:+DX2_tON; 0: -DX2_tON

DX2_TOFF[7]: 1:+DX2_tOFF; 0: -DX2_tOFF



Restrictions

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

6.3.5 SETVCOM: Set VCOM voltage (B6h)

B6H	SETVCOM (Set VCOM Voltage)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	0	1	1	0	B6
1 st parameter	1	VCMC_F[7:0]								C8
2 nd parameter	1	VCMC_B[7:0]								C8
3 rd parameter	1	VCOM_TIMES[2:0]			-	-	-	VCMC_B[8]	VCMC_F[8]	E0
Description	This command is used to set VCOM Voltage.									
	VCMC_F[8:0]: Forward scan VCOM voltage control.									
	VCMC_B[8:0]: Backward scan VCOM voltage control.									
	VCMC_F[8:0]/VCMC_B[8:0]									VCOM
	0	0	0	0	0	0	0	0	0	1.00
	0	0	0	0	0	0	0	0	1	0.99V
	0	0	0	0	0	0	0	1	0	0.98V
	0	0	0	0	0	0	0	1	1	0.97V
	0	0	0	0	0	0	1	0	0	0.96V
	0	0	0	0	0	0	1	0	1	0.95V
	0	0	0	0	0	0	1	1	0	0.94V
	0	0	0	0	0	0	1	1	1	0.93V
	0	0	0	0	0	1	0	0	0	0.92V
	0	0	0	0	0	1	0	0	1	0.91V
	0	0	0	0	0	1	0	1	0	0.90V
	0	0	0	0	0	1	0	1	1	0.89V
	:									:
	0	1	1	0	0	1	0	0	0	-1.00V
	0	1	1	0	0	1	0	0	1	-1.01V
	0	1	1	0	0	1	0	1	0	-1.02V
	0	1	1	0	0	1	0	1	1	-1.03V
	0	1	1	0	0	1	1	0	0	-1.04V
	0	1	1	0	0	1	1	0	1	-1.05V
	:									:
	1	1	0	0	0	1	1	1	0	-2.98V
1	1	0	0	0	1	1	1	1	-2.99V	
1	1	0	0	1	0	0	0	0	-3.00V	
Others									Inhibited	
1	1	1	1	1	1	1	1	0	VSSA	
1	1	1	1	1	1	1	1	1	HZ	

	VCOM_TIMES[2:0]: Read the VCOM OTP programmed times.	
	VCOM_TIMES[2:0]	VCOM OTP Programmed Times
	111	No programmed
	011	VCOM has been programmed 1 time
	001	VCOM has been programmed 2 times
	000	VCOM has been programmed 3 times
Restrictions	SETEXTC turn on to enable this command.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Himax Confidential
Do Not Copy

6.3.6 SETTE: Set internal TE function (B7h)

B7H	SETTE (Set internal TE function)																																																														
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																					
Command	0	1	0	1	1	0	1	1	1	B7																																																					
1 st parameter	1	TEI[3:0]				-	TEP[10:8]				00																																																				
2 nd parameter	1	TEP[7:0]									00																																																				
Description	<p>TEI[3:0]: Set the output interval of TE signal according to the display data rewrite cycle and data transfer rate.</p> <table border="1"> <thead> <tr> <th>TEI3</th> <th>TEI2</th> <th>TEI1</th> <th>TEI0</th> <th>Output Interval</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1 frame</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>2 frames</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>3 frames</td> </tr> <tr> <td colspan="4" style="text-align:center">:</td> <td style="text-align:center">:</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>15 frames</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>16 frames</td> </tr> </tbody> </table> <p>TEP[10:0]: Set the output position of frame cycle signal. TE can be used as the trigger signal for frame synchronous write operation. Make sure the setting restriction $11'h000 \leq TEP[10:0] \leq \text{Numbers of Line}-1$.</p> <table border="1"> <thead> <tr> <th>TEP[10:0]</th> <th>Output position</th> </tr> </thead> <tbody> <tr> <td>000h</td> <td>0th line</td> </tr> <tr> <td>001h</td> <td>1st line</td> </tr> <tr> <td>002h</td> <td>2nd line</td> </tr> <tr> <td>003h</td> <td>3rd line</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>77Fh</td> <td>1919th line</td> </tr> <tr> <td>780h</td> <td>1920th line</td> </tr> <tr> <td>Others</td> <td>Inhibited</td> </tr> </tbody> </table>										TEI3	TEI2	TEI1	TEI0	Output Interval	0	0	0	0	1 frame	0	0	0	1	2 frames	0	0	1	0	3 frames	:				:	1	1	1	0	15 frames	1	1	1	1	16 frames	TEP[10:0]	Output position	000h	0th line	001h	1st line	002h	2nd line	003h	3rd line	:	:	77Fh	1919th line	780h	1920th line	Others	Inhibited
	TEI3	TEI2	TEI1	TEI0	Output Interval																																																										
	0	0	0	0	1 frame																																																										
	0	0	0	1	2 frames																																																										
	0	0	1	0	3 frames																																																										
	:				:																																																										
	1	1	1	0	15 frames																																																										
	1	1	1	1	16 frames																																																										
	TEP[10:0]	Output position																																																													
	000h	0th line																																																													
001h	1st line																																																														
002h	2nd line																																																														
003h	3rd line																																																														
:	:																																																														
77Fh	1919th line																																																														
780h	1920th line																																																														
Others	Inhibited																																																														
Restrictions	SETEXTC turn on to enable this command.																																																														
Register Availability	Status					Availability																																																									
	Normal Mode On, Idle Mode Off, Sleep Out					Yes																																																									
	Normal Mode On, Idle Mode On, Sleep Out					Yes																																																									
	Sleep In or Booster Off					Yes																																																									

6.3.7 SETEXTC: Set extension command (B9h)

B9H	SETEXTC (Set extended command)										
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	0	1	1	1	0	0	1	B9	
1 st parameter	1	EXTC1[7:0]									00/FF
2 nd parameter	1	EXTC2[7:0]									00/83
3 rd parameter	1	EXTC3[7:0]									00/99
Description	This command is used to set extended command set access enable.										
	Extend command					Command description					
	Enable					After command (B9h), must write 3 parameters (FFh, 83h, 99h) by order					
Disable(default)					After command (B9h), write 3 parameters (xxh, xxh, xxh) any value except (FFh, 83h, 99h)						
Restrictions	-										
Register Availability	Status					Availability					
	Normal Mode On, Idle Mode Off, Sleep Out					Yes					
	Normal Mode On, Idle Mode On, Sleep Out					Yes					
	Sleep In or Booster Off					Yes					

Himax Confidential
Do Not Copy

6.3.8 SETMIPI: Set MIPI control (BAh)

BAH	SETMIPI(Set MIPI control)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	0	1	0	BA
1 st parameter	1	-	DSISETUP0[6:0]							63
2 nd parameter	1	DSISETUP1[7:0]							03	
Description	This command is used to set MIPI DSI Related Setting.									
	DSISETUP0[6]	Tx Type: Define the LP-TX BTA behavior when there are error. 0: only BTA Error 1: BTA Read + Error								
	DSISETUP0[5]	CD_disable: Define the contention detection (LP-CD) function. 0 : LP-CD function enable 1: LP-CD function disable								
	DSISETUP0[4]	Tx_OscDiv: LP-TX clock (T _{LPX}) selection. 0 : 50ns (10MHz) 1 :100ns (5MHz)								
	DSISETUP0[3:2]	UpRstDsiSel:uP controlled reset timer setting when enter HS by LP11→LP00: 00:no reset, 01:180ms, 10:200ms, 11:220ms								
	DSISETUP0[1:0]	LAN_NUM: Define the DSI lane number 00 : 1-lane 01 : 2-lane 10 : 3-lane 11 : 4-lane								
	DSISETUP1[7]	RxCRC_enable; Enable RX CRC Check.								
	DSISETUP1[6]	ECC_ignore: Define the RX behavior when error occurring. 0 : the transmission will be broken when there are ECC or CRC error 1 : the transmission will keep when there are ECC or CRC error								
	DSISETUP1[5]	slpin_hs_wd_en:watch dog enable when enter HS by LP11→LP00.								
	DSISETUP1[4]	conti_w_en: 29h continuous write function 0:disable,1:enable								
DSISETUP1[3:2]	Txe_Wait: BTA from Tx into Rx overlap waiting time counter(T _{TA-GO}) 00: TA-go = 2 Tlpx 01: TA-go = 4 Tlpx 10: TA-go = 6 Tlpx 11: TA-go = 8 Tlpx									
DSISETUP1[1:0]	Txs_Wait: BTA from Rx into Tx overlap waiting time counter(T _{TA-GET}) 00: Disable, no wait time 01: TA-get = 2 Tlpx 10: TA-get = 4 Tlpx 11: TA-get = 6 Tlpx									
Restrictions	SETEXTC turn on to enable this command.									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				

6.3.9 SETOTP: Set OTP (BBh)

BBH	SETOTP(Set OTP Related Setting)																				
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	0	1	1	1	0	1	1	BB											
1 st parameter	1	INTVP P_EN	-	OTP_P ROG_ ALL	-	-	-	OTP_INDEX[9:8]		00											
2 nd parameter	1	OTP_INDEX[7:0]								00											
3 rd parameter	1	OTP_DATA[7:0]								00											
4 th parameter	1	OTP_P OR	OTP_P WE	OTP_P WR_S EL	OTP_PTM[2:0]			OTP_T EST	OTP_P ROG	00											
5 th parameter	1	OTP_DATA_READ[7:0]								-											
6 th parameter	1	OTP_KEY0[7:0]								00											
7 th parameter	1	OTP_KEY1[7:0]								00											
Description	This command is used to set OTP related setting.																				
	<table border="1"> <thead> <tr> <th>OTP_KEY0[7:0], OTP_KEY1[7:0]</th> <th>Description</th> <th>Note</th> </tr> </thead> <tbody> <tr> <td>OTP_KEY0[7:0] = 0xAAh OTP_KEY1[7:0] = 0x55h</td> <td>Enter OTP program mode</td> <td></td> </tr> <tr> <td>OTP_KEY0[7:0] = 0x00h OTP_KEY1[7:0] = 0x00h</td> <td>Leave OTP program mode</td> <td></td> </tr> <tr> <td>Other value</td> <td>Invalid</td> <td>If HX8399-C operate on OTP program mode, Then keep on OTP program mode. If HX8399-C operate on non-OTP program mode, Then keep on non-OTP program mode.</td> </tr> </tbody> </table> <p>INTVPP_EN: OTP_PWR power selected. "0" : External OTP_PWR is selected when programmed. "1" : Internal OTP_PWR is selected when programmed.</p> <p>OTP_PROG_ALL: When set to "1", all OTP index is programmed, except for CAh, E5h, E6h.</p> <p>OTP_INDEX[9:0]: Set index of OTP table for programming.</p> <p>OTP_PROG: When set to "1", the register content of OTP index is programmed.</p> <p>OTP_PWR_SEL: When written to "1", OTP power voltage is fed to OTP circuit.</p> <p>OTP_PTM[2:0]: For test mode using. Not open..</p> <p>OTP_PWE: OTP program write enable, "1" means OTP is able to be programmed.</p> <p>OTP_POR: Pulse for OTP data read operation.</p> <p>OTP_TEST: "0", setting OTP_PROG high will trigger internal state machine. "1", setting OTP_PROG high will not trigger internal state machine.</p> <p>OTP_DATA[7:0]: Write data of OTP index.</p> <p>OTP_DATA_READ[7:0]: Read back the OTP index data.</p>										OTP_KEY0[7:0], OTP_KEY1[7:0]	Description	Note	OTP_KEY0[7:0] = 0xAAh OTP_KEY1[7:0] = 0x55h	Enter OTP program mode		OTP_KEY0[7:0] = 0x00h OTP_KEY1[7:0] = 0x00h	Leave OTP program mode		Other value	Invalid
OTP_KEY0[7:0], OTP_KEY1[7:0]	Description	Note																			
OTP_KEY0[7:0] = 0xAAh OTP_KEY1[7:0] = 0x55h	Enter OTP program mode																				
OTP_KEY0[7:0] = 0x00h OTP_KEY1[7:0] = 0x00h	Leave OTP program mode																				
Other value	Invalid	If HX8399-C operate on OTP program mode, Then keep on OTP program mode. If HX8399-C operate on non-OTP program mode, Then keep on non-OTP program mode.																			
Restrictions	SETEXTC turn on to enable this command.																				

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Himax Confidential
Do Not Copy

6.3.10 SET_BANK: Set register bank (BDh)

BDH	SET_BANK(Set register bank)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	1	BD
1 st parameter	1	-	-	-	-	-	-	BANK_INDEX [1:0]		00
Description	<p>Set the register bank for some Commands that beyond 64 parameters</p> <p>For example: Write RC1h, PA44~PA85 Step1: write RBDh = 01h Step2: write RC1h, PA1~42</p> <p>Read RC1h, PA86~PA127 Step1: write RBDh = 02h Step2: read RC1h, PA1~42</p>									
Restrictions	SETEXTC turn on to enable this command.									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				

6.3.11 SETDGCLUT_P: Set DGC LUT_P (C1h)

C1H	SETDGCLUT (Set DGC LUT)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	0	0	1	C1
Bank0 1 st parameter	1	-	-	-	DGC_PN	1	1	-	DGC_EN	0C
2 nd parameter	1	R_GAMMA0[9:2]								-
3 rd parameter	1	R_GAMMA1[9:2]								-
4 th parameter	1	R_GAMMA2[9:2]								-
5 th parameter	1	R_GAMMA3[9:2]								-
6 th parameter	1	R_GAMMA4[9:2]								-
7 th parameter	1	R_GAMMA5[9:2]								-
8 th parameter	1	R_GAMMA6[9:2]								-
9 th parameter	1	R_GAMMA7[9:2]								-
10 th parameter	1	R_GAMMA8[9:2]								-
11 st parameter	1	R_GAMMA9[9:2]								-
12 nd parameter	1	R_GAMMA10[9:2]								-
13 rd parameter	1	R_GAMMA11[9:2]								-
14 th parameter	1	R_GAMMA12[9:2]								-
15 th parameter	1	R_GAMMA13[9:2]								-
16 th parameter	1	R_GAMMA14[9:2]								-
17 th parameter	1	R_GAMMA15[9:2]								-
18 th parameter	1	R_GAMMA16[9:2]								-
19 th parameter	1	R_GAMMA17[9:2]								-
20 th parameter	1	R_GAMMA18[9:2]								-
21 st parameter	1	R_GAMMA19[9:2]								-
22 nd parameter	1	R_GAMMA20[9:2]								-
23 rd parameter	1	R_GAMMA21[9:2]								-
24 th parameter	1	R_GAMMA22[9:2]								-
25 th parameter	1	R_GAMMA23[9:2]								-
26 th parameter	1	R_GAMMA24[9:2]								-
27 th parameter	1	R_GAMMA25[9:2]								-
28 th parameter	1	R_GAMMA26[9:2]								-
29 th parameter	1	R_GAMMA27[9:2]								-
30 th parameter	1	R_GAMMA28[9:2]								-
31 st parameter	1	R_GAMMA29[9:2]								-
32 nd parameter	1	R_GAMMA30[9:2]								-
33 rd parameter	1	R_GAMMA31[9:2]								-
34 th parameter	1	R_GAMMA32[9:2]								-
35 th parameter	1	R_GAMMA0[1:0]	R_GAMMA1[1:0]	R_GAMMA2[1:0]	R_GAMMA3[1:0]					-
36 th parameter	1	R_GAMMA4[1:0]	R_GAMMA5[1:0]	R_GAMMA6[1:0]	R_GAMMA7[1:0]					-
37 th parameter	1	R_GAMMA8[1:0]	R_GAMMA9[1:0]	R_GAMMA10[1:0]	R_GAMMA11[1:0]					-
38 th parameter	1	R_GAMMA12[1:0]	R_GAMMA13[1:0]	R_GAMMA14[1:0]	R_GAMMA15[1:0]					-
39 th parameter	1	R_GAMMA16[1:0]	R_GAMMA17[1:0]	R_GAMMA18[1:0]	R_GAMMA19[1:0]					-
40 th parameter	1	R_GAMMA20[1:0]	R_GAMMA21[1:0]	R_GAMMA22[1:0]	R_GAMMA23[1:0]					-
41 st parameter	1	R_GAMMA24[1:0]	R_GAMMA25[1:0]	R_GAMMA26[1:0]	R_GAMMA27[1:0]					-
42 nd parameter	1	R_GAMMA28[1:0]	R_GAMMA29[1:0]	R_GAMMA30[1:0]	R_GAMMA31[1:0]					-
43 rd parameter	1	R_GAMMA32[1:0]	-	-	-	-	-	-	-	-
Bank1 1 st parameter	1	G_GAMMA0[9:2]								-

2 nd parameter	1	G_GAMMA1[9:2]				-
3 rd parameter	1	G_GAMMA2[9:2]				-
4 th parameter	1	G_GAMMA3[9:2]				-
5 th parameter	1	G_GAMMA4[9:2]				-
6 th parameter	1	G_GAMMA5[9:2]				-
7 th parameter	1	G_GAMMA6[9:2]				-
8 th parameter	1	G_GAMMA7[9:2]				-
9 th parameter	1	G_GAMMA8[9:2]				-
10 th parameter	1	G_GAMMA9[9:2]				-
11 st parameter	1	G_GAMMA10[9:2]				-
12 nd parameter	1	G_GAMMA11[9:2]				-
13 rd parameter	1	G_GAMMA12[9:2]				-
14 th parameter	1	G_GAMMA13[9:2]				-
15 th parameter	1	G_GAMMA14[9:2]				-
16 th parameter	1	G_GAMMA15[9:2]				-
17 th parameter	1	G_GAMMA16[9:2]				-
18 th parameter	1	G_GAMMA17[9:2]				-
19 th parameter	1	G_GAMMA18[9:2]				-
20 th parameter	1	G_GAMMA19[9:2]				-
21 st parameter	1	G_GAMMA20[9:2]				-
22 nd parameter	1	G_GAMMA21[9:2]				-
23 rd parameter	1	G_GAMMA22[9:2]				-
24 th parameter	1	G_GAMMA23[9:2]				-
25 th parameter	1	G_GAMMA24[9:2]				-
26 th parameter	1	G_GAMMA25[9:2]				-
27 th parameter	1	G_GAMMA26[9:2]				-
28 th parameter	1	G_GAMMA27[9:2]				-
29 th parameter	1	G_GAMMA28[9:2]				-
30 th parameter	1	G_GAMMA29[9:2]				-
31 st parameter	1	G_GAMMA30[9:2]				-
32 nd parameter	1	G_GAMMA31[9:2]				-
33 rd parameter	1	G_GAMMA32[9:2]				-
34 th parameter	1	G_GAMMA0[1:0]	G_GAMMA1[1:0]	G_GAMMA2[1:0]	G_GAMMA3[1:0]	-
35 th parameter	1	G_GAMMA4[1:0]	G_GAMMA5[1:0]	G_GAMMA6[1:0]	G_GAMMA7[1:0]	-
36 th parameter	1	G_GAMMA8[1:0]	G_GAMMA9[1:0]	G_GAMMA10[1:0]	G_GAMMA11[1:0]	-
37 th parameter	1	G_GAMMA12[1:0]	G_GAMMA13[1:0]	G_GAMMA14[1:0]	G_GAMMA15[1:0]	-
38 th parameter	1	G_GAMMA16[1:0]	G_GAMMA17[1:0]	G_GAMMA18[1:0]	G_GAMMA19[1:0]	-
39 th parameter	1	G_GAMMA20[1:0]	G_GAMMA21[1:0]	G_GAMMA22[1:0]	G_GAMMA23[1:0]	-
40 th parameter	1	G_GAMMA24[1:0]	G_GAMMA25[1:0]	G_GAMMA26[1:0]	G_GAMMA27[1:0]	-
41 st parameter	1	G_GAMMA28[1:0]	G_GAMMA29[1:0]	G_GAMMA30[1:0]	G_GAMMA31[1:0]	-
42 nd parameter	1	G_GAMMA32[1:0]	-	-	-	-
Bank2						
1 st parameter	1	B_GAMMA0[9:2]				-
2 nd parameter	1	B_GAMMA1[9:2]				-
3 rd parameter	1	B_GAMMA2[9:2]				-
4 th parameter	1	B_GAMMA3[9:2]				-
5 th parameter	1	B_GAMMA4[9:2]				-
6 th parameter	1	B_GAMMA5[9:2]				-
7 th parameter	1	B_GAMMA6[9:2]				-
8 th parameter	1	B_GAMMA7[9:2]				-

9 th parameter	1	B_GAMMA8[9:2]				-
10 th parameter	1	B_GAMMA9[9:2]				-
11 st parameter	1	B_GAMMA10[9:2]				-
12 nd parameter	1	B_GAMMA11[9:2]				-
13 rd parameter	1	B_GAMMA12[9:2]				-
14 th parameter	1	B_GAMMA13[9:2]				-
15 th parameter	1	B_GAMMA14[9:2]				-
16 th parameter	1	B_GAMMA15[9:2]				-
17 th parameter	1	B_GAMMA16[9:2]				-
18 th parameter	1	B_GAMMA17[9:2]				-
19 th parameter	1	B_GAMMA18[9:2]				-
20 th parameter	1	B_GAMMA19[9:2]				-
21 st parameter	1	B_GAMMA20[9:2]				-
22 nd parameter	1	B_GAMMA21[9:2]				-
23 rd parameter	1	B_GAMMA22[9:2]				-
24 th parameter	1	B_GAMMA23[9:2]				-
25 th parameter	1	B_GAMMA24[9:2]				-
26 th parameter	1	B_GAMMA25[9:2]				-
27 th parameter	1	B_GAMMA26[9:2]				-
28 th parameter	1	B_GAMMA27[9:2]				-
29 th parameter	1	B_GAMMA28[9:2]				-
30 th parameter	1	B_GAMMA29[9:2]				-
31 st parameter	1	B_GAMMA30[9:2]				-
32 nd parameter	1	B_GAMMA31[9:2]				-
33 rd parameter	1	B_GAMMA32[9:2]				-
34 th parameter	1	B_GAMMA0[1:0]	B_GAMMA1[1:0]	B_GAMMA2[1:0]	B_GAMMA3[1:0]	-
35 th parameter	1	B_GAMMA4[1:0]	B_GAMMA5[1:0]	B_GAMMA6[1:0]	B_GAMMA7[1:0]	-
36 th parameter	1	B_GAMMA8[1:0]	B_GAMMA9[1:0]	B_GAMMA10[1:0]	B_GAMMA11[1:0]	-
37 th parameter	1	B_GAMMA12[1:0]	B_GAMMA13[1:0]	B_GAMMA14[1:0]	B_GAMMA15[1:0]	-
38 th parameter	1	B_GAMMA16[1:0]	B_GAMMA17[1:0]	B_GAMMA18[1:0]	B_GAMMA19[1:0]	-
39 th parameter	1	B_GAMMA20[1:0]	B_GAMMA21[1:0]	B_GAMMA22[1:0]	B_GAMMA23[1:0]	-
40 th parameter	1	B_GAMMA24[1:0]	B_GAMMA25[1:0]	B_GAMMA26[1:0]	B_GAMMA27[1:0]	-
41 st parameter	1	B_GAMMA28[1:0]	B_GAMMA29[1:0]	B_GAMMA30[1:0]	B_GAMMA31[1:0]	-
42 nd parameter	1	B_GAMMA32[1:0]	-	-	-	-

Description	This command is used to set Digital Gamma Curve Look-Up Table.					
	DGC_PN: Enable individual positive and negative DGC. "1": Enable; "0": Disable					
	DGC_EN: Enable the DGC function. "1": Enable; "0": Disable.					
	R/G/B_GAMMA0[9:0] ~ R/G/B_GAMMA32[9:0]: MSB 8-bit is setting to mapping related gray level to which gray level voltage of real gamma. LSB 2-bit is for dithering.					
	LUT		Mapping Gray level			
	R_GAMMA0[9:0]		R0			
	R_GAMMA1[9:0]		R8			
	R_GAMMA2[9:0]		R16			
	:		:			
	R_GAMMA31[9:0]		R240			
	R_GAMMA32[9:0]		R255			
	G_GAMMA0[9:0]		G0			
	G_GAMMA1[9:0]		G8			
	G_GAMMA2[9:0]		G16			
	:		:			
G_GAMMA31[9:0]		G240				

	<table border="1"> <tr><td>G_GAMMA32[9:0]</td><td>G255</td></tr> <tr><td>B_GAMMA0[9:0]</td><td>B0</td></tr> <tr><td>B_GAMMA1[9:0]</td><td>B8</td></tr> <tr><td>B_GAMMA2[9:0]</td><td>B16</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>B_GAMMA31[9:0]</td><td>B240</td></tr> <tr><td>B_GAMMA32[9:0]</td><td>B255</td></tr> </table>	G_GAMMA32[9:0]	G255	B_GAMMA0[9:0]	B0	B_GAMMA1[9:0]	B8	B_GAMMA2[9:0]	B16	:	:	B_GAMMA31[9:0]	B240	B_GAMMA32[9:0]	B255	
G_GAMMA32[9:0]	G255															
B_GAMMA0[9:0]	B0															
B_GAMMA1[9:0]	B8															
B_GAMMA2[9:0]	B16															
:	:															
B_GAMMA31[9:0]	B240															
B_GAMMA32[9:0]	B255															
Restrictions	SETEXTC turn on to enable this command.															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes							
Status	Availability															
Normal Mode On, Idle Mode Off, Sleep Out	Yes															
Normal Mode On, Idle Mode On, Sleep Out	Yes															
Sleep In or Booster Off	Yes															

Himax Confidential
Do Not Copy

6.3.12 SETID: Set ID (C3h)

C3H	SETID (Set ID)																			
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX										
Command	0	1	1	0	0	0	0	1	1	C3										
1 st parameter	1	ID1[7:0]									83									
2 nd parameter	1	ID2[7:0]									99									
3 rd parameter	1	ID3[7:0]									0C									
4 th parameter	1	ID4[7:0]									00									
5 th parameter	1	ID_TIMES[2:0]		-	-	-	-	-	-	E0										
Description	<p>ID1[7:0] is used to set ID RDAh value.</p> <p>ID2[7:0] is used to set ID RDBh value.</p> <p>ID3[7:0] is used to set ID RDCh value.</p> <p>ID4[7:0] is used to set the fourth ID.</p> <p>ID_TIMES[2:0]: Read the ID OTP programmed times.</p> <table border="1"> <thead> <tr> <th>ID_TIMES[2:0]</th> <th>ID OTP Programmed Times</th> </tr> </thead> <tbody> <tr> <td>111</td> <td>No programmed</td> </tr> <tr> <td>011</td> <td>ID has been programmed 1 time</td> </tr> <tr> <td>001</td> <td>ID has been programmed 2 times</td> </tr> <tr> <td>000</td> <td>ID has been programmed 3 times</td> </tr> </tbody> </table>										ID_TIMES[2:0]	ID OTP Programmed Times	111	No programmed	011	ID has been programmed 1 time	001	ID has been programmed 2 times	000	ID has been programmed 3 times
	ID_TIMES[2:0]	ID OTP Programmed Times																		
	111	No programmed																		
	011	ID has been programmed 1 time																		
	001	ID has been programmed 2 times																		
	000	ID has been programmed 3 times																		
Restrictions	SETEXTC turn on to enable this command.																			
Register Availability	Status					Availability														
	Normal Mode On, Idle Mode Off, Sleep Out					Yes														
	Normal Mode On, Idle Mode On, Sleep Out					Yes														
	Sleep In or Booster Off					Yes														

6.3.13 SETDDB: Set DDB (C4h)

C4H	SETDDB (Set DDB)										
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	0	0	0	1	0	0	C4	
1 st parameter	1	DDB1[7:0]									00
2 nd parameter	1	DDB2[7:0]									00
3 rd parameter	1	DDB3[7:0]									00
4 th parameter	1	DDB4[7:0]									00
5 th parameter	1	DDB5[7:0]									00
6 th parameter	1	DDB6[7:0]									00
7 th parameter	1	DDB7[7:0]									00
Description	This command is used to set CMD RA1h DDB1~7 value.										
Restrictions	SETEXTC turn on to enable this command.										
Register Availability	Status					Availability					
	Normal Mode On, Idle Mode Off, Sleep Out					Yes					
	Normal Mode On, Idle Mode On, Sleep Out					Yes					
	Sleep In or Booster Off					Yes					

Himax Confidential
Do Not Copy

6.3.14 SETCABC: Set CABC control (C9h)

C9H	SETCABC (Set CABC Control)																																																																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																								
Command	0	1	1	0	0	1	0	0	1	C9																																																								
1 st Parameter	1	-	-	-	-	SLR_EN	BC_CTRL_EN	INVPULS	SEL_BLDUTY	03																																																								
2 nd Parameter	1	PWM_PERIOD[15:8]								00																																																								
3 rd Parameter	1	PWM_PERIOD[7:0]								2E																																																								
Description	This command is used to set CABC parameter.																																																																	
	<p>SLR_EN: SLR function enable. '0', Disable. '1', Enable.</p> <p>SEL_BLDUTY: Backligh pwm output duty on/off control when CABC operation. '0', The Backligh pwm output duty is 100%. '1', The Backligh pwm output duty is calculate from CABC operation.</p> <p>INVPULS: The backlight PWM output polarity select. '0', The backlight PWM output is low level active. '1', The backlight PWM output is high level active.</p> <p>BC_CTRL_EN: Enable Backlight EN signal output</p> <p>PWM_PERIOD[15:0]: The backlight PWM output period setting.</p> <p>The PWM_CLK frequency mapping table is as bellows: PWM_PERIOD[15:6] setting inhibited.</p> <table border="1"> <thead> <tr> <th>PWM_PERIOD[5:0]</th> <th>PWM_CLK</th> </tr> </thead> <tbody> <tr><td>00h</td><td>40KHz</td></tr> <tr><td>01h</td><td>39KHz</td></tr> <tr><td>02h</td><td>38KHz</td></tr> <tr><td>03h</td><td>37KHz</td></tr> <tr><td>04h</td><td>36KHz</td></tr> <tr><td>05h</td><td>35KHz</td></tr> <tr><td>06h</td><td>34KHz</td></tr> <tr><td>07h</td><td>33KHz</td></tr> <tr><td>08h</td><td>32KHz</td></tr> <tr><td>09h</td><td>31KHz</td></tr> <tr><td>0Ah</td><td>30KHz</td></tr> <tr><td>0Bh</td><td>29KHz</td></tr> <tr><td>0Ch</td><td>28KHz</td></tr> <tr><td>0Dh</td><td>27KHz</td></tr> <tr><td>0Eh</td><td>26KHz</td></tr> <tr><td>0Fh</td><td>25KHz</td></tr> <tr><td>10h</td><td>24KHz</td></tr> <tr><td>11h</td><td>23KHz</td></tr> <tr><td>12h</td><td>22KHz</td></tr> <tr><td>13h</td><td>21KHz</td></tr> <tr><td>14h</td><td>20KHz</td></tr> <tr><td>15h</td><td>19KHz</td></tr> <tr><td>16h</td><td>18KHz</td></tr> <tr><td>17h</td><td>17KHz</td></tr> <tr><td>18h</td><td>16KHz</td></tr> <tr><td>19h</td><td>15KHz</td></tr> <tr><td>1Ah</td><td>14KHz</td></tr> </tbody> </table>										PWM_PERIOD[5:0]	PWM_CLK	00h	40KHz	01h	39KHz	02h	38KHz	03h	37KHz	04h	36KHz	05h	35KHz	06h	34KHz	07h	33KHz	08h	32KHz	09h	31KHz	0Ah	30KHz	0Bh	29KHz	0Ch	28KHz	0Dh	27KHz	0Eh	26KHz	0Fh	25KHz	10h	24KHz	11h	23KHz	12h	22KHz	13h	21KHz	14h	20KHz	15h	19KHz	16h	18KHz	17h	17KHz	18h	16KHz	19h	15KHz	1Ah	14KHz
	PWM_PERIOD[5:0]	PWM_CLK																																																																
	00h	40KHz																																																																
	01h	39KHz																																																																
	02h	38KHz																																																																
	03h	37KHz																																																																
	04h	36KHz																																																																
	05h	35KHz																																																																
	06h	34KHz																																																																
	07h	33KHz																																																																
	08h	32KHz																																																																
	09h	31KHz																																																																
	0Ah	30KHz																																																																
	0Bh	29KHz																																																																
	0Ch	28KHz																																																																
	0Dh	27KHz																																																																
	0Eh	26KHz																																																																
	0Fh	25KHz																																																																
	10h	24KHz																																																																
	11h	23KHz																																																																
	12h	22KHz																																																																
	13h	21KHz																																																																
	14h	20KHz																																																																
	15h	19KHz																																																																
16h	18KHz																																																																	
17h	17KHz																																																																	
18h	16KHz																																																																	
19h	15KHz																																																																	
1Ah	14KHz																																																																	

	<table border="1"> <tr><td>1Bh</td><td>13KHz</td></tr> <tr><td>1Ch</td><td>12KHz</td></tr> <tr><td>1Dh</td><td>11KHz</td></tr> <tr><td>1Eh</td><td>10KHz</td></tr> <tr><td>1Fh</td><td>9KHz</td></tr> <tr><td>20h</td><td>8KHz</td></tr> <tr><td>21h</td><td>7KHz</td></tr> <tr><td>22h</td><td>6KHz</td></tr> <tr><td>23h</td><td>5KHz</td></tr> <tr><td>24h</td><td>4KHz</td></tr> <tr><td>25h</td><td>3KHz</td></tr> <tr><td>26h</td><td>2KHz</td></tr> <tr><td>27h</td><td>1KHz</td></tr> <tr><td>28h</td><td>900Hz</td></tr> <tr><td>29h</td><td>800Hz</td></tr> <tr><td>2Ah</td><td>700Hz</td></tr> <tr><td>2Bh</td><td>600Hz</td></tr> <tr><td>2Ch</td><td>500Hz</td></tr> <tr><td>2Dh</td><td>400Hz</td></tr> <tr><td>2Eh</td><td>300Hz</td></tr> <tr><td>2Fh</td><td>200Hz</td></tr> <tr><td>30h</td><td>100Hz</td></tr> <tr><td>Other</td><td>inhibited</td></tr> </table>	1Bh	13KHz	1Ch	12KHz	1Dh	11KHz	1Eh	10KHz	1Fh	9KHz	20h	8KHz	21h	7KHz	22h	6KHz	23h	5KHz	24h	4KHz	25h	3KHz	26h	2KHz	27h	1KHz	28h	900Hz	29h	800Hz	2Ah	700Hz	2Bh	600Hz	2Ch	500Hz	2Dh	400Hz	2Eh	300Hz	2Fh	200Hz	30h	100Hz	Other	inhibited
1Bh	13KHz																																														
1Ch	12KHz																																														
1Dh	11KHz																																														
1Eh	10KHz																																														
1Fh	9KHz																																														
20h	8KHz																																														
21h	7KHz																																														
22h	6KHz																																														
23h	5KHz																																														
24h	4KHz																																														
25h	3KHz																																														
26h	2KHz																																														
27h	1KHz																																														
28h	900Hz																																														
29h	800Hz																																														
2Ah	700Hz																																														
2Bh	600Hz																																														
2Ch	500Hz																																														
2Dh	400Hz																																														
2Eh	300Hz																																														
2Fh	200Hz																																														
30h	100Hz																																														
Other	inhibited																																														
Restriction	SETEXTC turn on to enable this command.																																														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes																																						
Status	Availability																																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																																														
Sleep In or Booster Off	Yes																																														

6.3.15 SETCLOCK (CBh)

CBH	SETCLOCK									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	1	0	1	1	CB
1 st Parameter	1	-	-	-	UADJ[4:0]					10
Description	UADJ[4:0]: For user to adjust OSC frequency, default is 100MHz.									
	UADJ[4:0]					Internal oscillator frequency				
	0	0	0	0	0	31.4%				
	0	0	0	0	1	36.2%				
	0	0	0	1	0	40.6%				
	0	0	0	1	1	45.1%				
	0	0	1	0	0	49.7%				
	0	0	1	0	1	55.0%				
	0	0	1	1	0	58.8%				
	0	0	1	1	1	63.8%				
	0	1	0	0	0	66.4%				
	0	1	0	0	1	71.2%				
	0	1	0	1	0	75.0%				
	0	1	0	1	1	80.5%				
	0	1	1	0	0	83.5%				
	0	1	1	0	1	89.1%				
	0	1	1	1	0	94.0%				
	0	1	1	1	1	100.9%				
	1	0	0	0	0	100.0%				
	1	0	0	0	1	104.5%				
	1	0	0	1	0	106.6%				
	1	0	0	1	1	114.0%				
	1	0	1	0	0	116.8%				
	1	0	1	0	1	122.8%				
	1	0	1	1	0	127.4%				
	1	0	1	1	1	132.5%				
	1	1	0	0	0	133.6%				
	1	1	0	0	1	139.0%				
	1	1	0	1	0	142.7%				
	1	1	0	1	1	148.7%				
1	1	1	0	0	152.2%					
1	1	1	0	1	157.3%					
1	1	1	1	0	160.7%					
1	1	1	1	1	165.2%					
Restrictions	SETEXTC turn on to enable this command									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				

6.3.16 SETPANEL: Set panel related register (CCh)

CCH	SETPANEL(Set panel related register)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	1	0	0	1	1	0	0	CC								
1 st parameter	1	-	-	-	-	SS_PA NEL	GS_PA NEL	REV_P ANEL	BGR_P ANEL	00.								
Description0	<p>This command is used to set setting of panel related register and make panel module meets below spec from viewpoint of user</p> <p>BGR_PANEL: The order of <R><G> dot color for module supplier, default value is stored in OTP. If color filter of panel is <G><R> type, setting BGR_PANEL = 1, if color filter of panel is <R><G> type, setting BGR_PANEL = 0. This bit is to make panel module look like a <R><G> type panel form the user viewpoint.</p> <p>REV_PANEL: The REV_PANEL setting is used to select the inversion of the display of all characters and graphics. This setting allows the display of the same data on both normally white and normally black panels.</p> <p>GS_PANEL: Specify the shift direction of gate driver output. When GS_PANEL = 0, the panel control signal is normal scan. When GS_PANEL = 1, the panel control signal is reverse scan.</p> <p>SS_PANEL: Specify the shift direction of source driver output. When SS_PANEL = 0, the shift direction from S1 to S1200 When SS_PANEL = 1, the shift direction from S1200 to S1.</p>																	
Restrictions	SETEXTC turn on to enable this command																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	

6.3.17 SETCRC (D0h)

D0H	SETCRC									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command / Parameter	0	1	1	0	1	0	0	0	0	D0
1 st PA	1	-	-	CRC_CYCLE_SEL [2:0]			CRC_ERR OR_FLG	CRC_CHK_ONCE	CRC_CHK_EN	00h
Description	CRC_CYCLE_SEL[2:0]: CRC check cycle selection (only for CRC_CHK_EN=1)									
	CRC_CYCLE_SEL [2:0]			CRC count duration / per cycle						
	0	0	0	30 frame (0.5 sec)						
	0	0	1	60 frame (1 sec)						
	0	1	0	120 frame (2 sec)						
	0	1	1	180 frame (3 sec)						
	1	0	0	1 frame						
	1	0	1	2 frame						
	1	1	0	3 frame						
	1	1	1	4 frame						
CRC_ERROR_FLG: When CRC_ERROR_FLG='1', the current CRC value is different with previous CRC value.										
CRC_CHK_ONCE: To enable CRC check function for customer manual setting.										
CRC_CHK_EN: To enable CRC check function for ESD.										
Restrictions	SETEXTC turn on to enable this command.									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				

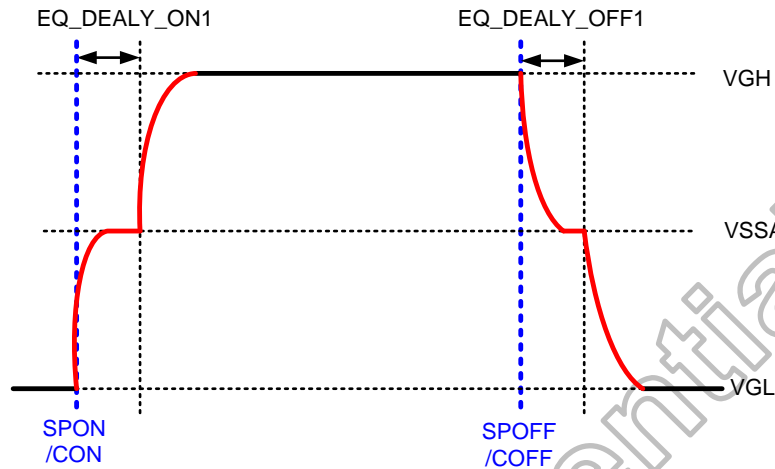
6.3.18 SETOFFSET (D2h)

D2H	SETOFFSET																																																																																														
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																					
Command	0	1	1	0	1	0	0	1	0	D2																																																																																					
1 st parameter	1	VN_REFS[3:0]				VP_REFS[3:0]				66																																																																																					
Description	VP_REFS[3:0]: Positive reference voltage VP_REF setting. <table border="1"> <thead> <tr> <th colspan="4">VP_REFS[3:0]</th> <th>VP_REF Voltage</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>4.0V</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>4.3V</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>4.5V</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>4.6V</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>4.7V</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>4.8V</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4.9V</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>5.0V</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5.1V</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5.2V</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5.3V</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>5.4V</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>5.5V</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>5.6V</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>5.8V</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Inhibited</td></tr> </tbody> </table>										VP_REFS[3:0]				VP_REF Voltage	0	0	0	0	4.0V	0	0	0	1	4.3V	0	0	1	0	4.5V	0	0	1	1	4.6V	0	1	0	0	4.7V	0	1	0	1	4.8V	0	1	1	0	4.9V	0	1	1	1	5.0V	1	0	0	0	5.1V	1	0	0	1	5.2V	1	0	1	0	5.3V	1	0	1	1	5.4V	1	1	0	0	5.5V	1	1	0	1	5.6V	1	1	1	0	5.8V	1	1	1	1	Inhibited
	VP_REFS[3:0]				VP_REF Voltage																																																																																										
	0	0	0	0	4.0V																																																																																										
	0	0	0	1	4.3V																																																																																										
	0	0	1	0	4.5V																																																																																										
	0	0	1	1	4.6V																																																																																										
	0	1	0	0	4.7V																																																																																										
	0	1	0	1	4.8V																																																																																										
	0	1	1	0	4.9V																																																																																										
	0	1	1	1	5.0V																																																																																										
	1	0	0	0	5.1V																																																																																										
	1	0	0	1	5.2V																																																																																										
	1	0	1	0	5.3V																																																																																										
	1	0	1	1	5.4V																																																																																										
	1	1	0	0	5.5V																																																																																										
	1	1	0	1	5.6V																																																																																										
	1	1	1	0	5.8V																																																																																										
	1	1	1	1	Inhibited																																																																																										
	VN_REFS[3:0]: Negative reference voltage VN_REF setting. <table border="1"> <thead> <tr> <th colspan="4">VN_REFS[3:0]</th> <th>VN_REF Voltage</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>-4.0V</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>-4.3V</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>-4.5V</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>-4.6V</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>-4.7V</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>-4.8V</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>-4.9V</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>-5.0V</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>-5.1V</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>-5.2V</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>-5.3V</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>-5.4V</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>-5.5V</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>-5.6V</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>-5.8V</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Inhibited</td></tr> </tbody> </table>										VN_REFS[3:0]				VN_REF Voltage	0	0	0	0	-4.0V	0	0	0	1	-4.3V	0	0	1	0	-4.5V	0	0	1	1	-4.6V	0	1	0	0	-4.7V	0	1	0	1	-4.8V	0	1	1	0	-4.9V	0	1	1	1	-5.0V	1	0	0	0	-5.1V	1	0	0	1	-5.2V	1	0	1	0	-5.3V	1	0	1	1	-5.4V	1	1	0	0	-5.5V	1	1	0	1	-5.6V	1	1	1	0	-5.8V	1	1	1	1	Inhibited
	VN_REFS[3:0]				VN_REF Voltage																																																																																										
	0	0	0	0	-4.0V																																																																																										
	0	0	0	1	-4.3V																																																																																										
	0	0	1	0	-4.5V																																																																																										
	0	0	1	1	-4.6V																																																																																										
	0	1	0	0	-4.7V																																																																																										
	0	1	0	1	-4.8V																																																																																										
	0	1	1	0	-4.9V																																																																																										
0	1	1	1	-5.0V																																																																																											
1	0	0	0	-5.1V																																																																																											
1	0	0	1	-5.2V																																																																																											
1	0	1	0	-5.3V																																																																																											
1	0	1	1	-5.4V																																																																																											
1	1	0	0	-5.5V																																																																																											
1	1	0	1	-5.6V																																																																																											
1	1	1	0	-5.8V																																																																																											
1	1	1	1	Inhibited																																																																																											
Restrictions	SETEXTC turn on to enable this command.																																																																																														
Register Availability	Status					Availability																																																																																									
	Normal Mode On, Idle Mode Off, Sleep Out					Yes																																																																																									
	Normal Mode On, Idle Mode On, Sleep Out					Yes																																																																																									
	Sleep In or Booster Off					Yes																																																																																									

6.3.19 SETGIP0: Set GIP Option0 (D3h)

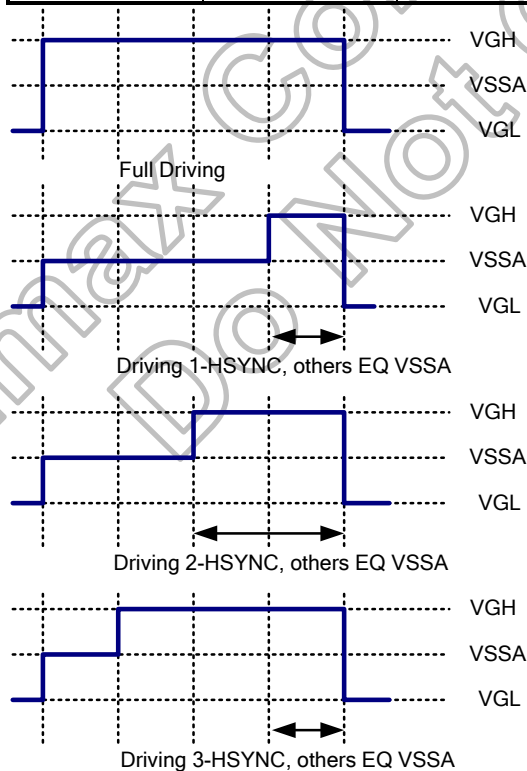
D3H	SETGIP0(Set GIP Option0)										
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	0	1	0	0	1	1	D3	
Bank0 1 st parameter	1	-	-	GIP_EQ_OPT[1:0]		-	-	EQ_DELAY_HSYN C[1:0]		00	
2 nd parameter	1	-	-	-	-	VSEL[1:0]		EQ_DISC[1:0]		00	
3 rd parameter	1	EQ_DELAY_ON1[7:0]									00
4 th parameter	1	EQ_DELAY_OFF1[7:0]									00
5 th parameter	1	GTO[7:0]									00
6 th parameter	1	GNO[7:0]									00
7 th parameter	1	USER_GIP_GATE[7:0]									08
8 th parameter	1	USER_GIP_GATE1[7:0]									08
9 th parameter		SHR0_3[3:0]				SHR0_2[3:0]				32	
10 th parameter	1	SHR0_1[3:0]				SHR0[11:8]				10	
11 st parameter	1	SHR0[7:0]									02
12 nd parameter	1	-	-	-	-	SHR0_GS[11:8]				00	
13 rd parameter	1	SHR0_GS[7:0]									02
14 th parameter	1	SHR1_3[3:0]				SHR1_2[3:0]				32	
15 th parameter	1	SHR1_1[3:0]				SHR1[11:8]				13	
16 th parameter	1	SHR1[7:0]									C0
17 th parameter	1	-	-	-	-	SHR1_GS[11:8]				00	
18 th parameter	1	SHR1_GS[7:0]									00
19 th parameter	1	SHR2_3[3:0]				SHR2_2[3:0]				32	
20 th parameter	1	SHR2_1[3:0]				SHR2[11:8]				10	
21 st parameter	1	SHR2[7:0]									08
22 nd parameter	1	-	-	-	-	SHR2_GS[11:8]				00	
23 rd parameter	1	SHR2_GS[7:0]									00
24 th parameter	1	SHP[3:0]				SCP[3:0]				4B	
25 th parameter	1	SHP2[3:0]				SHP1[3:0]				00	
26 th parameter	1	CHR0[7:0]									06
27 th parameter	1	CHR0_GS[7:0]									06
28 th parameter	1	CHP0[3:0]				CCP0[3:0]				47	
29 th parameter	1	CHR1[7:0]									04
30 th parameter	1	CHR1_GS[7:0]									00
31 st parameter	1	CHP1[3:0]				CCP1[3:0]				27	
32 nd parameter	1	vbp_setting[7:0]									00
33 rd parameter	1	-	vbp_self_learning	-	-					00	
Description	This command is used for GIP signal setting.										
	GIP_EQ_OPT[1:0]: GIP EQ (pre-charge) type selection										
	GIP_EQ_OPT 1		GIP_EQ_OPT 0		GIP EQ Type						
	0		0		Both rising / falling EQ						
	0		1		Only rising edge EQ						
1		0		Only falling edge EQ							
1		1		EQ Off							
EQ_DELAY_ON1[7:0] / EQ_DELAY_OFF1[7:0]: Set GIP control signal EQ period (1 TCON CLK = 4 OSC)											
EQ_DELAY_ON1[7:0] / EQ_DELAY_OFF1[7:0]								GIP EQ Period			
0 0 0 0 0 0 0 0								Inhibited			
0 0 0 0 0 0 0 1								1 TCON clock cycle			
0 0 0 0 0 0 1 0								2 TCON clock cycle			
0 0 0 0 0 0 1 1								3 TCON clock cycle			
:								:			
1 1 1 1 1 1 0 1								253 TCON clock cycle			
1 1 1 1 1 1 1 0								254 TCON clock cycle			

1 1 1 1 1 1 1 1 255 TCON clock cycle



EQ_DELAY_HSYNC[1:0]: Set the EQ period in HSYNC width.

EQ_DELAY_HSYNC[1:0]		EQ Period in HSYNC width
0	0	Normal Driving
0	1	1 x Hsync
1	0	2 x Hsync
1	1	3 x Hsync



VSEL[1:0]: select CGOUTL/R_11~13 and CGOUTL/R_14~16 output voltage slew rate.

VSEL[1]	CGOUTL/R_14~16
0	Normal VGH/VGL rising/falling slew rate
1	Weak VGH/VGL rising/falling slew rate

VSEL[0]	CGOUTL/R_11~13
0	Normal VGH/VGL rising/falling slew rate
1	Weak VGH/VGL rising/falling slew rate

EQ_DISC[1:0]: GIP EQ GND slew rate option.

EQ_DISC[1:0]	GIP EQ GND Ability
00	Strong
01	Middle Strong
10	Middle Weak
11	Weak

GTO[7:0]: GPWR signal toggle frequency.

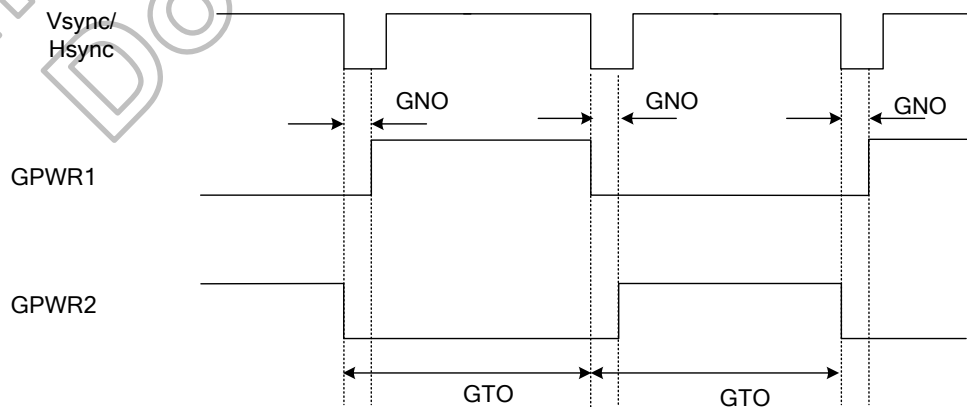
GTO[7:0]	GPWR toggle frequency
6'h00	256 x Frame/Line
6'h01	1 x Frame/ Line
6'h02	2 x Frame/ Line
6'h03	3 x Frame/ Line
:	:
6'h3D	253 x Frame/ Line
6'h3E	254 x Frame/ Line
6'h3F	255 x Frame/ Line

GNO[7:0]: GPWR signal non-overlap timing.

GNO[7:0]	GPWR non-overlap timing
8'h00	0
8'h01	1 TCON clock cycle
8'h02	2 TCON clock cycle
8'h03	3 TCON clock cycle
:	:
8'hFD	253 TCON clock cycle
8'hFE	254 TCON clock cycle
8'hFF	255 TCON clock cycle

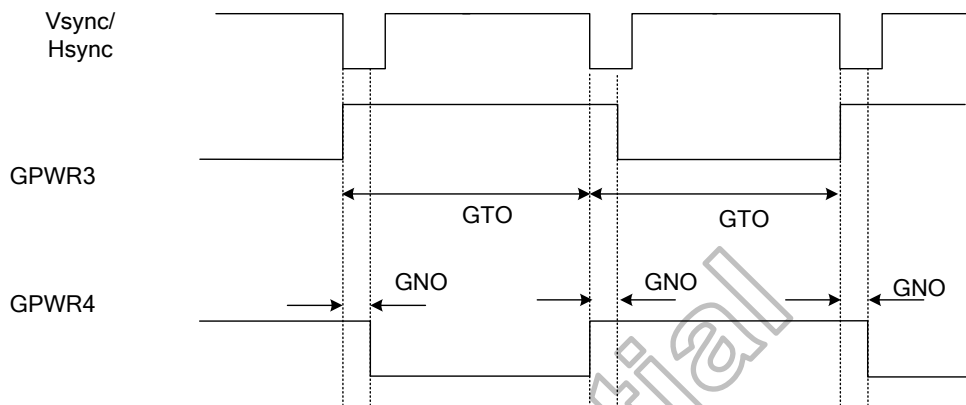
GPWR1/2 toggle period by Frame or Line depend on GIP_OPT[2]. Non-overlap time depends on GNO.

GPWR1/2 non-overlap signal are as below:



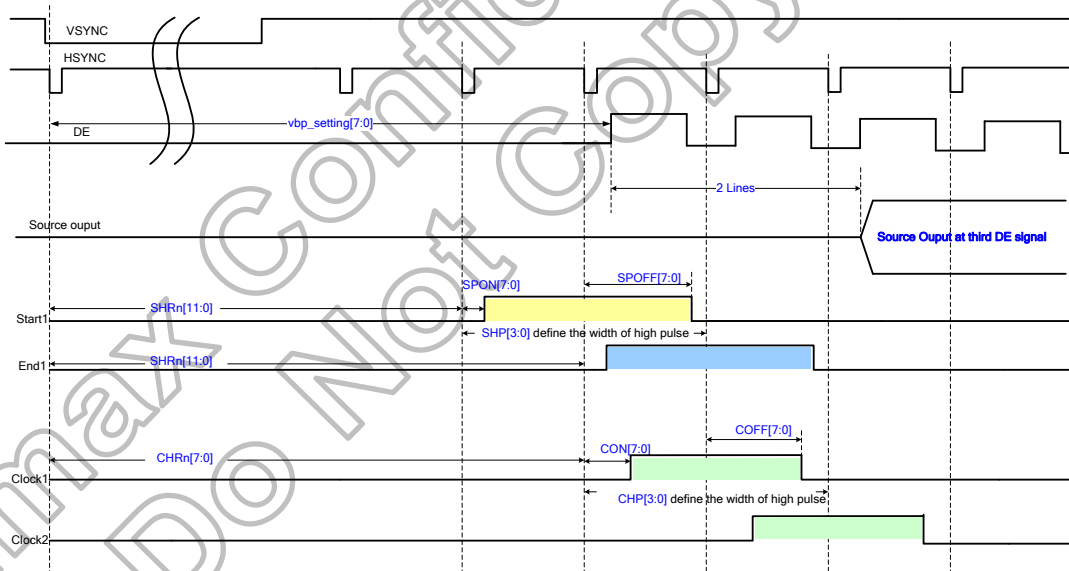
GPWR3/4 toggle period by Frame or Line depend on GIP_OPT[2]. Overlap time depends on GNO.

GPWR3/4 overlap signal are as below:



USER_GIP_Gate[7:0]: Set the GIP dummy clock numbers for first CKV.

USER_GIP_Gate1[7:0]: Set the GIP dummy clock numbers for second CKV.



Group0:

SHR0[11:0]: Set the 1st Start/End signal delay from VSYNC falling edge when GS=0.

SHR0_GS[11:0]: Set the 1st Start/End signal delay from VSYNC falling edge when GS=1.

SHR0_1 / SHR0_2 / SHR0_3[3:0]: Set the 2nd/3rd/4th Start / End signal delay from the 1st Start/End signal.

Group1:

SHR1[11:0]: Set the 1st Start/End signal delay from VSYNC falling edge when GS=0.

SHR1_GS[11:0]: Set the 1st Start/End signal delay from VSYNC falling edge when GS=1.

SHR1_1 / SHR1_2 / SHR1_3[3:0]: Set the 2nd/3rd/4th Start / End signal delay from the 1st Start/End signal.

Group2:

SHR2[11:0]: Set the 1st Start/End signal delay from VSYNC falling edge when GS=0.

SHR2_GS[11:0]: Set the 1st Start/End signal delay from VSYNC falling edge when GS=1.

SHR2_1 / SHR2_2 / SHR2_3[3:0]: Set the 2nd/3rd/4th Start / End signal delay from the 1st Start/End signal.

SHR0/SHR1/SHR2[11:0]	Start signal output delay
SHR0_GS/SHR1_GS/SHR2_GS[11:0]	
0x000h	2 x Hsync

0x001h	3 x Hsync
0x002h	4 x Hsync
:	:
0xFFEh	4096 x Hsync
0xFFFh	4097 x Hsync

SHR0_1 / SHR1_1 / SHR2_1[3:0]	2nd Start / End signal output delay
SHR0_2 / SHR1_2 / SHR2_2[3:0]	3th Start / End signal output delay
SHR0_3 / SHR1_3 / SHR2_3[3:0]	4th Start / End signal output delay
0000	0 x Hsync
0001	1 x Hsync
0010	2 x Hsync
:	:
1110	14 x Hsync
1111	15 x Hsync

SCP[3:0]: Numbers of output Start and End signal.

SCP3	SCP2	SCP1	SCP0	Start and End numbers
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
:	:	:	:	:
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

SHP0[1/2][3:0]: Width of Start and End signal high pulse.

SHP3	SHP2	SHP1	SHP0	Start Pulse Width
0	0	0	0	1 x Hsync
0	0	0	1	2 x Hsync
0	0	1	0	3 x Hsync
:	:	:	:	:
1	1	1	0	15 x Hsync
1	1	1	1	16 x Hsync

CHR0[7:0]/CHR1[7:0]: Set the Clock signal delay from VSYNC falling edge when GS=0.

CHR0_GS[7:0]/CHR1_GS[7:0]: Set the Clock signal delay from VSYNC falling edge when GS=1.

CHR0[7:0]/CHR0_GS[7:0] CHR1[7:0]/CHR1_GS[7:0]	Clock signal output delay
0x00h	2 x HSYNC
0x01h	3 x HSYNC
0x02h	4 x HSYNC
:	:
0xFEh	256 x HSYNC
0xFFh	257 x HSYNC

CCP0[3:0]/CCP1[3:0]: Numbers of Output Clock signal.

CCP0[3:0]/CCP1[3:0]	Clock numbers
0 0 0 0	1
0 0 0 1	2
0 0 1 0	3
:	:
1 1 1 0	15
1 1 1 1	16

CHP0[3:0]/CHP1[3:0]: Width of Clock signal high pulse.

		CHP0[3:0]/CHP1[3:0]				Clock signal width
		0	0	0	0	1 x Hsync
		0	0	0	1	2 x Hsync
		0	0	1	0	3 x Hsync
		:				:
		1	1	1	0	15 x Hsync
		1	1	1	1	16 x Hsync
		vbp_setting[7:0]: Set Vertical porch lines. (Vbp_setting[7:0]=VS+VBP-3)				
		vbp_self_learning: Set '1' to enable self-learning.				
Restrictions	SETEXTC turn on to enable this command.					
Register Availability	Status			Availability		
	Normal Mode On, Idle Mode Off, Sleep Out			Yes		
	Normal Mode On, Idle Mode On, Sleep Out			Yes		
	Sleep In or Booster Off			Yes		

Himax Confidential
Do Not Copy

6.3.20 SETGIP1: Set GIP Option1 (D5h)

D5H	SETGIP1(Set GIP Option1)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	1	0	1	0	1	D5
1 st parameter	1	-	CGTS_L_INV[1]	COS1_L[5:0]					18	
2 nd parameter	1	-	CGTS_R_INV[1]	COS1_R[5:0]					18	
3 rd parameter	1	-	CGTS_L_INV[2]	COS2_L[5:0]					18	
4 th parameter	1	-	CGTS_R_INV[2]	COS2_R[5:0]					18	
5 th parameter	1	-	CGTS_L_INV[3]	COS3_L[5:0]					18	
6 th parameter	1	-	CGTS_R_INV[3]	COS3_R[5:0]					18	
7 th parameter	1	-	CGTS_L_INV[4]	COS4_L[5:0]					18	
8 th parameter	1	-	CGTS_R_INV[4]	COS4_R[5:0]					18	
9 th parameter	1	-	CGTS_L_INV[5]	COS5_L[5:0]					18	
10 th parameter	1	-	CGTS_R_INV[5]	COS5_R[5:0]					18	
11 st parameter	1	-	CGTS_L_INV[6]	COS6_L[5:0]					18	
12 nd parameter	1	-	CGTS_R_INV[6]	COS6_R[5:0]					18	
13 rd parameter	1	-	CGTS_L_INV[7]	COS7_L[5:0]					18	
14 th parameter	1	-	CGTS_R_INV[7]	COS7_R[5:0]					18	
15 th parameter	1	-	CGTS_L_INV[8]	COS8_L[5:0]					18	
16 th parameter	1	-	CGTS_R_INV[8]	COS8_R[5:0]					18	
17 th parameter	1	-	CGTS_L_INV[9]	COS9_L[5:0]					18	
18 th parameter	1	-	CGTS_R_INV[9]	COS9_R[5:0]					18	
19 th parameter	1	-	CGTS_L_INV[10]	COS10_L[5:0]					18	
20 th parameter	1	-	CGTS_R_INV[10]	COS10_R[5:0]					18	
21 st parameter	1	-	CGTS_L_INV[11]	COS11_L[5:0]					18	
22 nd parameter	1	-	CGTS_R_INV[11]	COS11_R[5:0]					18	
23 rd parameter	1	-	CGTS_L_INV[12]	COS12_L[5:0]					18	
24 th parameter	1	-	CGTS_R_INV[12]	COS12_R[5:0]					18	
25 th parameter	1	-	CGTS_L_INV[13]	COS13_L[5:0]					18	
26 th parameter	1	-	CGTS_R_INV[13]	COS13_R[5:0]					18	
27 th parameter	1	-	CGTS_L_INV[14]	COS14_L[5:0]					18	
28 th parameter	1	-	CGTS_R_INV[14]	COS14_R[5:0]					18	
29 th parameter	1	-	CGTS_L_INV[15]	COS15_L[5:0]					18	
30 th parameter	1	-	CGTS_R_INV[15]	COS15_R[5:0]					18	
31 st parameter	1	-	CGTS_L_INV[16]	COS16_L[5:0]					18	
32 nd parameter	1	-	CGTS_R_INV[16]	COS16_R[5:0]					18	
Description	<p>CGTS_L_INV[16:1]: Set the corresponding signal CGOUTL_n output polarity,n=1~16 CGTS_R_INV[16:1]: Set the corresponding signal CGOUTR_n output polarity,n=1~16 0: Normal output 1: Invert output signal</p> <p>COSn_L[3:0]: When GS_Panel=0, select CGOUTL_n output, n=1~16 COSn_R[3:0]: When GS_Panel=0, select CGOUTR_n output, n=1~16</p>									

COSn_L[5:0]~ COSn_R[5:0]~ n=1~16	Output Signal	Description
00_0000	CK[0]	GROUP0: Gate CLK
00_0001	CK[1]	Gate CLK
00_0010	CK[2]	Gate CLK
00_0011	CK[3]	Gate CLK
00_0100	CK[4]	Gate CLK
00_0101	CK[5]	Gate CLK
00_0110	CK[6]	Gate CLK
00_0111	CK[7]	Gate CLK
00_1000	CK[8]	Gate CLK
00_1001	CK[9]	Gate CLK
00_1010	CK[10]	Gate CLK
00_1011	CK[11]	Gate CLK
00_1100	CK[12]	Gate CLK
00_1101	CK[13]	Gate CLK
00_1110	CK[14]	Gate CLK
00_1111	CK[15]	Gate CLK
01_0000	CK_1[0]	GROUP1: Gate CLK
01_0001	CK_1 [1]	Gate CLK
01_0010	CK_1 [2]	Gate CLK
01_0011	CK_1 [3]	Gate CLK
01_0100	CK_1 [4]	Gate CLK
01_0101	CK_1 [5]	Gate CLK
01_0110	CK_1 [6]	Gate CLK
01_0111	CK_1 [7]	Gate CLK
01_1000	1'b0	VGL
01_1001	1'b1	VGH
01_1010	GPWR1	Frame or Line toggle signal GPWR1
01_1011	GPWR2	Frame or Line toggle signal GPWR2
01_1100	GPWR3	Frame or Line toggle signal GPWR3
01_1101	GPWR4	Frame or Line toggle signal GPWR4
01_1110	DIR	When GS=0, output VGH. When GS=1, output VGL.
01_1111	DIRB	When GS=0, output VGL. When GS=1, output VGH.
10_0000	STV[0]	GROUP 0 SHR0[11:0]
10_0001	STV[1]	SHR0[11:0]+SHR0_1[3:0]
10_0010	STV[2]	SHR0[11:0]+SHR0_2[3:0]
10_0011	STV[3]	SHR0[11:0]+SHR0_3[3:0]
10_0100	STV[4]	GROUP 1 SHR1[11:0]
10_0101	STV[5]	SHR1[11:0]+SHR1_1[3:0]
10_0110	STV[6]	SHR1[11:0]+SHR1_2[3:0]
10_0111	STV[7]	SHR1[11:0]+SHR1_3[3:0]
10_1000	STV[8]	GROUP-2 SHR2[11:0]
10_1001	STV[9]	SHR2[11:0]+SHR2_1[3:0]
10_1010	STV[10]	SHR2[11:0]+SHR2_2[3:0]
10_1011	STV[11]	SHR2[11:0]+SHR2_3[3:0]
10_1111	SW1_L/R	Source driver switch
11_0000	SW2_L/R	Source driver switch
11_0001	SW3_L/R	Source driver switch
11_0010	SW1B_L/R	Source driver switch inveter
11_0011	SW2B_L/R	Source driver switch inveter
11_0100	SW3B_L/R	Source driver switch inveter

	11_0101	SW_INI	Source drive precharge signal
	11_0110	SW_INI_INV	Source drive precharge signal inverter
	Others	inhibited	-
Restrictions	-		
Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In or Booster Off		Yes

Himax Confidential
Do Not Copy

6.3.21 SETGIP2: Set GIP Option2 (D6h)

D6H	SETGIP2(Set GIP Option2)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	1	0	1	1	0	D6
1 st parameter	1	-	CGOUT_L_HIZ_IN [1]	COS1_L_GS[5:0]						18
2 nd parameter	1	-	CGOUT_R_HIZ_IN [1]	COS1_R_GS[5:0]						18
3 rd parameter	1	-	CGOUT_L_HIZ_IN [2]	COS2_L_GS[5:0]						18
4 th parameter	1	-	CGOUT_R_HIZ_IN [2]	COS2_R_GS[5:0]						18
5 th parameter	1	-	CGOUT_L_HIZ_IN [3]	COS3_L_GS[5:0]						18
6 th parameter	1	-	CGOUT_R_HIZ_IN [3]	COS3_R_GS[5:0]						18
7 th parameter	1	-	CGOUT_L_HIZ_IN [4]	COS4_L_GS[5:0]						18
8 th parameter	1	-	CGOUT_R_HIZ_IN [4]	COS4_R_GS[5:0]						18
9 th parameter	1	-	CGOUT_L_HIZ_IN [5]	COS5_L_GS[5:0]						18
10 th parameter	1	-	CGOUT_R_HIZ_IN [5]	COS5_R_GS[5:0]						18
11 st parameter	1	-	CGOUT_L_HIZ_IN [6]	COS6_L_GS[5:0]						18
12 nd parameter	1	-	CGOUT_R_HIZ_IN [6]	COS6_R_GS[5:0]						18
13 rd parameter	1	-	CGOUT_L_HIZ_IN [7]	COS7_L_GS[5:0]						18
14 th parameter	1	-	CGOUT_R_HIZ_IN [7]	COS7_R_GS[5:0]						18
15 th parameter	1	-	CGOUT_L_HIZ_IN [8]	COS8_L_GS[5:0]						18
16 th parameter	1	-	CGOUT_R_HIZ_IN [8]	COS8_R_GS[5:0]						18
17 th parameter	1	-	CGOUT_L_HIZ_IN [9]	COS9_L_GS[5:0]						18
18 th parameter	1	-	CGOUT_R_HIZ_IN [9]	COS9_R_GS[5:0]						18
19 th parameter	1	-	CGOUT_L_HIZ_IN [10]	COS10_L_GS[5:0]						18
20 th parameter	1	-	CGOUT_R_HIZ_IN [10]	COS10_R_GS[5:0]						18
21 st parameter	1	-	CGOUT_L_HIZ_IN [11]	COS11_L_GS[5:0]						18
22 nd parameter	1	-	CGOUT_R_HIZ_IN [11]	COS11_R_GS[5:0]						18
23 rd parameter	1	-	CGOUT_L_HIZ_IN [12]	COS12_L_GS[5:0]						18
24 th parameter	1	-	CGOUT_R_HIZ_IN [12]	COS12_R_GS[5:0]						18
25 th parameter	1	-	CGOUT_L_HIZ_IN [13]	COS13_L_GS[5:0]						18
26 th parameter	1	-	CGOUT_R_HIZ_IN	COS13_R_GS[5:0]						18

27 th parameter	1	-	[13] CGOUT_ L_HIZ_IN [14]	COS14_L_GS[5:0]	18
28 th parameter	1	-	CGOUT_ R_HIZ_IN [14]	COS14_R_GS[5:0]	18
29 th parameter	1	-	CGOUT_ L_HIZ_IN [15]	COS15_L_GS[5:0]	18
30 th parameter	1	-	CGOUT_ R_HIZ_IN [15]	COS15_R_GS[5:0]	18
31 st parameter	1	-	CGOUT_ L_HIZ_IN [16]	COS16_L_GS[5:0]	18
32 nd parameter	1	-	CGOUT_ R_HIZ_IN [16]	COS16_R_GS[5:0]	18

CGOUT_L_HIZ_IN[n]: Set the CGOUTL_n output = Hi-Z, n=1~16
CGOUT_R_HIZ_IN[n]: Set the CGOUTR_n output = Hi-Z, n=1~16
 0: Normal output
 1: Hi-Z

COSn_L_GS[3:0]: When GS_Panel=1, select CGOUTL_n output, n=1~16
COSn_R_GS[3:0]: When GS_Panel=1, select CGOUTR_n output, n=1~16

Description

COSn_L[5:0]~ COSn_R[5:0]~ n=1~16	Output Signal	Description
00_0000	CK[0]	GROUP0: Gate CLK
00_0001	CK[1]	Gate CLK
00_0010	CK[2]	Gate CLK
00_0011	CK[3]	Gate CLK
00_0100	CK[4]	Gate CLK
00_0101	CK[5]	Gate CLK
00_0110	CK[6]	Gate CLK
00_0111	CK[7]	Gate CLK
00_1000	CK[8]	Gate CLK
00_1001	CK[9]	Gate CLK
00_1010	CK[10]	Gate CLK
00_1011	CK[11]	Gate CLK
00_1100	CK[12]	Gate CLK
00_1101	CK[13]	Gate CLK
00_1110	CK[14]	Gate CLK
00_1111	CK[15]	Gate CLK
01_0000	CK_1[0]	GROUP1: Gate CLK
01_0001	CK_1 [1]	Gate CLK
01_0010	CK_1 [2]	Gate CLK
01_0011	CK_1 [3]	Gate CLK
01_0100	CK_1 [4]	Gate CLK
01_0101	CK_1 [5]	Gate CLK
01_0110	CK_1 [6]	Gate CLK
01_0111	CK_1 [7]	Gate CLK
01_1000	1'b0	VGL
01_1001	1'b1	VGH
01_1010	GPWR1	Frame or Line toggle signal GPWR1
01_1011	GPWR2	Frame or Line toggle signal GPWR2
01_1100	GPWR3	Frame or Line toggle signal GPWR3
01_1101	GPWR4	Frame or Line toggle signal GPWR4
01_1110	DIR	When GS=0, output VGH. When GS=1, output VGL.

	01_1111	DIRB	When GS=0, output VGL. When GS=1, output VGH.								
	10_0000	STV[0]	GROUP 0 SHR0[11:0]								
	10_0001	STV[1]	SHR0[11:0]+SHR0_1[3:0]								
	10_0010	STV[2]	SHR0[11:0]+SHR0_2[3:0]								
	10_0011	STV[3]	SHR0[11:0]+SHR0_3[3:0]								
	10_0100	STV[4]	GROUP 1 SHR1[11:0]								
	10_0101	STV[5]	SHR1[11:0]+SHR1_1[3:0]								
	10_0110	STV[6]	SHR1[11:0]+SHR1_2[3:0]								
	10_0111	STV[7]	SHR1[11:0]+SHR1_3[3:0]								
	10_1000	STV[8]	GROUP-2 SHR2[11:0]								
	10_1001	STV[9]	SHR2[11:0]+SHR2_1[3:0]								
	10_1010	STV[10]	SHR2[11:0]+SHR2_2[3:0]								
	10_1011	STV[11]	SHR2[11:0]+SHR2_3[3:0]								
	10_1111	SW1_L/R	Source driver switch								
	11_0000	SW2_L/R	Source driver switch								
	11_0001	SW3_L/R	Source driver switch								
	11_0010	SW1B_L/R	Source driver switch inveter								
	11_0011	SW2B_L/R	Source driver switch inveter								
	11_0100	SW3B_L/R	Source driver switch inveter								
	11_0101	SW_INI	Source drive precharge signal								
	11_0110	SW_INI_INV	Source drive precharge signal inverter								
	Others	inhibited	-								
Restrictions	-										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes	
Status	Availability										
Normal Mode On, Idle Mode Off, Sleep Out	Yes										
Normal Mode On, Idle Mode On, Sleep Out	Yes										
Sleep In or Booster Off	Yes										

6.3.22 SETGIP3: Set GIP Option3 (D8h)

D8H	SETGIP3(Set GIP Option3)									HEX
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	
Command	0	1	1	0	1	1	0	0	0	D8
Bank0 1 st parameter	1	INIT_0_SEL_C GOUT1_L[1:0]	INIT_0_SEL_C GOUT2_L[1:0]	INIT_0_SEL_C GOUT3_L[1:0]	INIT_0_SEL_C GOUT4_L[1:0]	INIT_0_SEL_C GOUT5_L[1:0]	INIT_0_SEL_C GOUT6_L[1:0]	INIT_0_SEL_C GOUT7_L[1:0]	INIT_0_SEL_C GOUT8_L[1:0]	00
2 nd parameter	1	INIT_0_SEL_C GOUT9_L[1:0]	INIT_0_SEL_C GOUT10_L[1:0]	INIT_0_SEL_C GOUT11_L[1:0]	INIT_0_SEL_C GOUT12_L[1:0]	INIT_0_SEL_C GOUT13_L[1:0]	INIT_0_SEL_C GOUT14_L[1:0]	INIT_0_SEL_C GOUT15_L[1:0]	INIT_0_SEL_C GOUT16_L[1:0]	00
3 rd parameter	1	INIT_0_SEL_C GOUT1_R[1:0]	INIT_0_SEL_C GOUT2_R[1:0]	INIT_0_SEL_C GOUT3_R[1:0]	INIT_0_SEL_C GOUT4_R[1:0]	INIT_0_SEL_C GOUT5_R[1:0]	INIT_0_SEL_C GOUT6_R[1:0]	INIT_0_SEL_C GOUT7_R[1:0]	INIT_0_SEL_C GOUT8_R[1:0]	00
4 th parameter	1	INIT_0_SEL_C GOUT9_R[1:0]	INIT_0_SEL_C GOUT10_R[1:0]	INIT_0_SEL_C GOUT11_R[1:0]	INIT_0_SEL_C GOUT12_R[1:0]	INIT_0_SEL_C GOUT13_R[1:0]	INIT_0_SEL_C GOUT14_R[1:0]	INIT_0_SEL_C GOUT15_R[1:0]	INIT_0_SEL_C GOUT16_R[1:0]	00
5 th parameter	1	INIT_1_SEL_C GOUT1_L[1:0]	INIT_1_SEL_C GOUT2_L[1:0]	INIT_1_SEL_C GOUT3_L[1:0]	INIT_1_SEL_C GOUT4_L[1:0]	INIT_1_SEL_C GOUT5_L[1:0]	INIT_1_SEL_C GOUT6_L[1:0]	INIT_1_SEL_C GOUT7_L[1:0]	INIT_1_SEL_C GOUT8_L[1:0]	00
6 th parameter	1	INIT_1_SEL_C GOUT9_L[1:0]	INIT_1_SEL_C GOUT10_L[1:0]	INIT_1_SEL_C GOUT11_L[1:0]	INIT_1_SEL_C GOUT12_L[1:0]	INIT_1_SEL_C GOUT13_L[1:0]	INIT_1_SEL_C GOUT14_L[1:0]	INIT_1_SEL_C GOUT15_L[1:0]	INIT_1_SEL_C GOUT16_L[1:0]	00
7 th parameter	1	INIT_1_SEL_C GOUT1_R[1:0]	INIT_1_SEL_C GOUT2_R[1:0]	INIT_1_SEL_C GOUT3_R[1:0]	INIT_1_SEL_C GOUT4_R[1:0]	INIT_1_SEL_C GOUT5_R[1:0]	INIT_1_SEL_C GOUT6_R[1:0]	INIT_1_SEL_C GOUT7_R[1:0]	INIT_1_SEL_C GOUT8_R[1:0]	00
8 th parameter	1	INIT_1_SEL_C GOUT9_R[1:0]	INIT_1_SEL_C GOUT10_R[1:0]	INIT_1_SEL_C GOUT11_R[1:0]	INIT_1_SEL_C GOUT12_R[1:0]	INIT_1_SEL_C GOUT13_R[1:0]	INIT_1_SEL_C GOUT14_R[1:0]	INIT_1_SEL_C GOUT15_R[1:0]	INIT_1_SEL_C GOUT16_R[1:0]	00
9 th parameter	1	END_0_SEL_C GOUT1_L[1:0]	END_0_SEL_C GOUT2_L[1:0]	END_0_SEL_C GOUT3_L[1:0]	END_0_SEL_C GOUT4_L[1:0]	END_0_SEL_C GOUT5_L[1:0]	END_0_SEL_C GOUT6_L[1:0]	END_0_SEL_C GOUT7_L[1:0]	END_0_SEL_C GOUT8_L[1:0]	00
10 th parameter	1	END_0_SEL_C GOUT9_L[1:0]	END_0_SEL_C GOUT10_L[1:0]	END_0_SEL_C GOUT11_L[1:0]	END_0_SEL_C GOUT12_L[1:0]	END_0_SEL_C GOUT13_L[1:0]	END_0_SEL_C GOUT14_L[1:0]	END_0_SEL_C GOUT15_L[1:0]	END_0_SEL_C GOUT16_L[1:0]	00
11 st parameter	1	END_0_SEL_C GOUT1_R[1:0]	END_0_SEL_C GOUT2_R[1:0]	END_0_SEL_C GOUT3_R[1:0]	END_0_SEL_C GOUT4_R[1:0]	END_0_SEL_C GOUT5_R[1:0]	END_0_SEL_C GOUT6_R[1:0]	END_0_SEL_C GOUT7_R[1:0]	END_0_SEL_C GOUT8_R[1:0]	00
12 nd parameter	1	END_0_SEL_C GOUT9_R[1:0]	END_0_SEL_C GOUT10_R[1:0]	END_0_SEL_C GOUT11_R[1:0]	END_0_SEL_C GOUT12_R[1:0]	END_0_SEL_C GOUT13_R[1:0]	END_0_SEL_C GOUT14_R[1:0]	END_0_SEL_C GOUT15_R[1:0]	END_0_SEL_C GOUT16_R[1:0]	00
13 rd parameter	1	END_1_SEL_C GOUT1_L[1:0]	END_1_SEL_C GOUT2_L[1:0]	END_1_SEL_C GOUT3_L[1:0]	END_1_SEL_C GOUT4_L[1:0]	END_1_SEL_C GOUT5_L[1:0]	END_1_SEL_C GOUT6_L[1:0]	END_1_SEL_C GOUT7_L[1:0]	END_1_SEL_C GOUT8_L[1:0]	00
14 th parameter	1	END_1_SEL_C GOUT9_L[1:0]	END_1_SEL_C GOUT10_L[1:0]	END_1_SEL_C GOUT11_L[1:0]	END_1_SEL_C GOUT12_L[1:0]	END_1_SEL_C GOUT13_L[1:0]	END_1_SEL_C GOUT14_L[1:0]	END_1_SEL_C GOUT15_L[1:0]	END_1_SEL_C GOUT16_L[1:0]	00
15 th parameter	1	END_1_SEL_C GOUT1_R[1:0]	END_1_SEL_C GOUT2_R[1:0]	END_1_SEL_C GOUT3_R[1:0]	END_1_SEL_C GOUT4_R[1:0]	END_1_SEL_C GOUT5_R[1:0]	END_1_SEL_C GOUT6_R[1:0]	END_1_SEL_C GOUT7_R[1:0]	END_1_SEL_C GOUT8_R[1:0]	00
16 th parameter	1	END_1_SEL_C GOUT9_R[1:0]	END_1_SEL_C GOUT10_R[1:0]	END_1_SEL_C GOUT11_R[1:0]	END_1_SEL_C GOUT12_R[1:0]	END_1_SEL_C GOUT13_R[1:0]	END_1_SEL_C GOUT14_R[1:0]	END_1_SEL_C GOUT15_R[1:0]	END_1_SEL_C GOUT16_R[1:0]	00
Bank1 1 st parameter	1	END_0_SEL_C GOUT1_L[1:0]	END_0_SEL_C GOUT2_L[1:0]	END_0_SEL_C GOUT3_L[1:0]	END_0_SEL_C GOUT4_L[1:0]	END_0_SEL_C GOUT5_L[1:0]	END_0_SEL_C GOUT6_L[1:0]	END_0_SEL_C GOUT7_L[1:0]	END_0_SEL_C GOUT8_L[1:0]	00
2 nd parameter	1	END_0_SEL_C GOUT9_L[1:0]	END_0_SEL_C GOUT10_L[1:0]	END_0_SEL_C GOUT11_L[1:0]	END_0_SEL_C GOUT12_L[1:0]	END_0_SEL_C GOUT13_L[1:0]	END_0_SEL_C GOUT14_L[1:0]	END_0_SEL_C GOUT15_L[1:0]	END_0_SEL_C GOUT16_L[1:0]	00
3 rd parameter	1	END_0_SEL_C GOUT1_R[1:0]	END_0_SEL_C GOUT2_R[1:0]	END_0_SEL_C GOUT3_R[1:0]	END_0_SEL_C GOUT4_R[1:0]	END_0_SEL_C GOUT5_R[1:0]	END_0_SEL_C GOUT6_R[1:0]	END_0_SEL_C GOUT7_R[1:0]	END_0_SEL_C GOUT8_R[1:0]	00
4 th parameter	1	END_0_SEL_C GOUT9_R[1:0]	END_0_SEL_C GOUT10_R[1:0]	END_0_SEL_C GOUT11_R[1:0]	END_0_SEL_C GOUT12_R[1:0]	END_0_SEL_C GOUT13_R[1:0]	END_0_SEL_C GOUT14_R[1:0]	END_0_SEL_C GOUT15_R[1:0]	END_0_SEL_C GOUT16_R[1:0]	00
5 th parameter	1	END_1_SEL_C GOUT1_L[1:0]	END_1_SEL_C GOUT2_L[1:0]	END_1_SEL_C GOUT3_L[1:0]	END_1_SEL_C GOUT4_L[1:0]	END_1_SEL_C GOUT5_L[1:0]	END_1_SEL_C GOUT6_L[1:0]	END_1_SEL_C GOUT7_L[1:0]	END_1_SEL_C GOUT8_L[1:0]	00
6 th parameter	1	END_1_SEL_C GOUT9_L[1:0]	END_1_SEL_C GOUT10_L[1:0]	END_1_SEL_C GOUT11_L[1:0]	END_1_SEL_C GOUT12_L[1:0]	END_1_SEL_C GOUT13_L[1:0]	END_1_SEL_C GOUT14_L[1:0]	END_1_SEL_C GOUT15_L[1:0]	END_1_SEL_C GOUT16_L[1:0]	00
7 th parameter	1	END_1_SEL_C GOUT1_R[1:0]	END_1_SEL_C GOUT2_R[1:0]	END_1_SEL_C GOUT3_R[1:0]	END_1_SEL_C GOUT4_R[1:0]	END_1_SEL_C GOUT5_R[1:0]	END_1_SEL_C GOUT6_R[1:0]	END_1_SEL_C GOUT7_R[1:0]	END_1_SEL_C GOUT8_R[1:0]	00
8 th parameter	1	END_1_SEL_C GOUT9_R[1:0]	END_1_SEL_C GOUT10_R[1:0]	END_1_SEL_C GOUT11_R[1:0]	END_1_SEL_C GOUT12_R[1:0]	END_1_SEL_C GOUT13_R[1:0]	END_1_SEL_C GOUT14_R[1:0]	END_1_SEL_C GOUT15_R[1:0]	END_1_SEL_C GOUT16_R[1:0]	00
9 th parameter	1	END_1_SEL_C GOUT1_L[1:0]	END_1_SEL_C GOUT2_L[1:0]	END_1_SEL_C GOUT3_L[1:0]	END_1_SEL_C GOUT4_L[1:0]	END_1_SEL_C GOUT5_L[1:0]	END_1_SEL_C GOUT6_L[1:0]	END_1_SEL_C GOUT7_L[1:0]	END_1_SEL_C GOUT8_L[1:0]	00

10 th parameter	1	END_1_SEL_C GOUT5_L[1:0]	END_1_SEL_C GOUT6_L[1:0]	END_1_SEL_C GOUT7_L[1:0]	END_1_SEL_C GOUT8_L[1:0]	00
11 st parameter	1	END_1_SEL_C GOUT9_L[1:0]	END_1_SEL_C GOUT10_L[1:0]	END_1_SEL_C GOUT11_L[1:0]	END_1_SEL_C GOUT12_L[1:0]	00
12 nd parameter	1	END_1_SEL_C GOUT13_L[1:0]	END_1_SEL_C GOUT14_L[1:0]	END_1_SEL_C GOUT15_L[1:0]	END_1_SEL_C GOUT16_L[1:0]	00
13 rd parameter	1	END_1_SEL_C GOUT1_R[1:0]	END_1_SEL_C GOUT2_R[1:0]	END_1_SEL_C GOUT3_R[1:0]	END_1_SEL_C GOUT4_R[1:0]	00
14 th parameter	1	END_1_SEL_C GOUT5_R[1:0]	END_1_SEL_C GOUT6_R[1:0]	END_1_SEL_C GOUT7_R[1:0]	END_1_SEL_C GOUT8_R[1:0]	00
15 th parameter	1	END_1_SEL_C GOUT9_R[1:0]	END_1_SEL_C GOUT10_R[1:0]	END_1_SEL_C GOUT11_R[1:0]	END_1_SEL_C GOUT12_R[1:0]	00
16 th parameter	1	END_1_SEL_C GOUT13_R[1:0]	END_1_SEL_C GOUT14_R[1:0]	END_1_SEL_C GOUT15_R[1:0]	END_1_SEL_C GOUT16_R[1:0]	00
Bank2 1 st parameter	1	GAS_0_SEL_C GOUT1_L[1:0]	GAS_0_SEL_C GOUT2_L[1:0]	GAS_0_SEL_C GOUT3_L[1:0]	GAS_0_SEL_C GOUT4_L[1:0]	00
2 nd parameter	1	GAS_0_SEL_C GOUT5_L[1:0]	GAS_0_SEL_C GOUT6_L[1:0]	GAS_0_SEL_C GOUT7_L[1:0]	GAS_0_SEL_C GOUT8_L[1:0]	00
3 rd parameter	1	GAS_0_SEL_C GOUT9_L[1:0]	GAS_0_SEL_C GOUT10_L[1:0]	GAS_0_SEL_C GOUT11_L[1:0]	GAS_0_SEL_C GOUT12_L[1:0]	00
4 th parameter	1	GAS_0_SEL_C GOUT13_L[1:0]	GAS_0_SEL_C GOUT14_L[1:0]	GAS_0_SEL_C GOUT15_L[1:0]	GAS_0_SEL_C GOUT16_L[1:0]	00
5 th parameter	1	GAS_0_SEL_C GOUT1_R[1:0]	GAS_0_SEL_C GOUT2_R[1:0]	GAS_0_SEL_C GOUT3_R[1:0]	GAS_0_SEL_C GOUT4_R[1:0]	00
6 th parameter	1	GAS_0_SEL_C GOUT5_R[1:0]	GAS_0_SEL_C GOUT6_R[1:0]	GAS_0_SEL_C GOUT7_R[1:0]	GAS_0_SEL_C GOUT8_R[1:0]	00
7 th parameter	1	GAS_0_SEL_C GOUT9_R[1:0]	GAS_0_SEL_C GOUT10_R[1:0]	GAS_0_SEL_C GOUT11_R[1:0]	GAS_0_SEL_C GOUT12_R[1:0]	00
8 th parameter	1	GAS_0_SEL_C GOUT13_R[1:0]	GAS_0_SEL_C GOUT14_R[1:0]	GAS_0_SEL_C GOUT15_R[1:0]	GAS_0_SEL_C GOUT16_R[1:0]	00
Description	<p>INIT means SLPIN to SLPOUT: INIT_0_SEL_CGOUTn_L: Set CGOUTL_n output state of first frame or first time interval when D[1:0]=01. INIT_0_SEL_CGOUTn_R: Set CGOUTR_n output state of first frame or first time interval when D[1:0]=01. n=1~16</p> <p>INIT_1_SEL_CGOUTn_L: Set CGOUTL_n output state of second frame or second time interval when D[1:0]=01. INIT_1_SEL_CGOUTn_R: Set CGOUTR_n output state of second frame or second time interval when D[1:0]=01. n=1~16</p> <p>END means SLPOUT to SLPIN END_0_SEL_CGOUTn_L: Set CGOUTL_n output state of first frame or first time interval when D[1:0]=01. END_0_SEL_CGOUTn_R: Set CGOUTR_n output state of first frame or first time interval when D[1:0]=01. n=1~16</p> <p>END_1_SEL_CGOUTn_L: Set CGOUTL_n output state of second frame or second time interval when D[1:0]=01. END_1_SEL_CGOUTn_R: Set CGOUTR_n output state of second frame or second time interval when D[1:0]=01. n=1~16</p>					

	<p>END_2_SEL_CGOUTn_L: Set CGOUTL_n output state of third frame or third time interval when D[1:0]=01.</p> <p>END_2_SEL_CGOUTn_R: Set CGOUTR_n output state of third frame or third time interval when D[1:0]=01. n=1~16</p> <p>GAS means abnormal power off</p> <p>GAS_0_SEL_CGOUTn_L: When abnormal power off happens,set CGOUTL_n output state.</p> <p>GAS_0_SEL_CGOUTn_R: When abnormal power off happens,set CGOUTR_n output state. n=1~16</p> <p>GIP output state: "00": Keep normal GIP output. "01": GND. "10": Fixed VGL. "11": Fixed VGH.</p>								
Restrictions	-								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In or Booster Off	Yes								

Himax Confidential
Do Not Copy

6.3.23 SETGPO (D9h)

D9H	SETGPO																																																									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																
Command	0	1	1	0	1	1	0	0	1	D9																																																
1 st parameter	1	-	-	-	-	TE_GPO[3:0]				00																																																
2 nd parameter	1	-	-	-	-	TE1_GPO[3:0]				01																																																
3 rd parameter	1	-	-	-	-	CABC_GPO[3:0]				02																																																
4 th parameter	1	-	-	-	-	SDO_GPO[3:0]				07																																																
Description	<p>TE_GPO[3:0]: Set the output pin TE. TE1_GPO[3:0]: Set the output pin TE1. CABC_GPO[3:0]: : Set the output pin CABC_PWM_OUT. SDO_GPO[3:0]: Set the output pin SDO.</p> <table border="1"> <thead> <tr> <th colspan="4">TE_GPO[3:0]/ TE1_GPO[3:0]/ CABC_GPO[3:0]/ SDO_GPO[3:0]</th> <th colspan="2">TE/ TE1/ CABC_PWM_OUT/ SDO Output signal</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td colspan="2">TE</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td colspan="2">TE1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td colspan="2">CABC</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td colspan="2">HSYNC</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td colspan="2">VSYNC</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td colspan="2">DE</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td colspan="2">SDO</td> </tr> </tbody> </table>										TE_GPO[3:0]/ TE1_GPO[3:0]/ CABC_GPO[3:0]/ SDO_GPO[3:0]				TE/ TE1/ CABC_PWM_OUT/ SDO Output signal		0	0	0	0	TE		0	0	0	1	TE1		0	0	1	0	CABC		0	0	1	1	HSYNC		0	1	0	0	VSYNC		0	1	0	1	DE		0	1	1	1	SDO	
	TE_GPO[3:0]/ TE1_GPO[3:0]/ CABC_GPO[3:0]/ SDO_GPO[3:0]				TE/ TE1/ CABC_PWM_OUT/ SDO Output signal																																																					
	0	0	0	0	TE																																																					
	0	0	0	1	TE1																																																					
	0	0	1	0	CABC																																																					
	0	0	1	1	HSYNC																																																					
	0	1	0	0	VSYNC																																																					
	0	1	0	1	DE																																																					
	0	1	1	1	SDO																																																					
Restrictions	SETEXTC turn on to enable this command																																																									
Register Availability	Status					Availability																																																				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes																																																				
	Normal Mode On, Idle Mode On, Sleep Out					Yes																																																				
	Sleep In or Booster Off					Yes																																																				

6.3.24 SETSCALING (DDh)

DDH	SETSCALING									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	1	1	1	0	1	DD
1 st parameter	1	-	-	-	-	-	-	SCALING_TYPE	SCALING_EN	00
Description	<p>SCALING_EN: Set "1" enable scaling function.</p> <p>SCALING_TYPE: 0: 2x scaling 1: 1.5x scaling</p>									
Restrictions	SETEXTC turn on to enable this command									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				

Himax Confidential
Do Not Copy

6.3.25 SETDGCLUT_N: Set DGC LUT_N (DEh)

DEH	SETDGCLUT (Set DGC LUT)										
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	0	1	1	1	1	0	DE	
Bank0											
1 st parameter	1	R_N_GAMMA0[9:2]									-
2 nd parameter	1	R_N_GAMMA1[9:2]									-
3 rd parameter	1	R_N_GAMMA2[9:2]									-
4 th parameter	1	R_N_GAMMA3[9:2]									-
5 th parameter	1	R_N_GAMMA4[9:2]									-
6 th parameter	1	R_N_GAMMA5[9:2]									-
7 th parameter	1	R_N_GAMMA6[9:2]									-
8 th parameter	1	R_N_GAMMA7[9:2]									-
9 th parameter	1	R_N_GAMMA8[9:2]									-
10 th parameter	1	R_N_GAMMA9[9:2]									-
11 st parameter	1	R_N_GAMMA10[9:2]									-
12 nd parameter	1	R_N_GAMMA11[9:2]									-
13 rd parameter	1	R_N_GAMMA12[9:2]									-
14 th parameter	1	R_N_GAMMA13[9:2]									-
15 th parameter	1	R_N_GAMMA14[9:2]									-
16 th parameter	1	R_N_GAMMA15[9:2]									-
17 th parameter	1	R_N_GAMMA16[9:2]									-
18 th parameter	1	R_N_GAMMA17[9:2]									-
19 th parameter	1	R_N_GAMMA18[9:2]									-
20 th parameter	1	R_N_GAMMA19[9:2]									-
21 st parameter	1	R_N_GAMMA20[9:2]									-
22 nd parameter	1	R_N_GAMMA21[9:2]									-
23 rd parameter	1	R_N_GAMMA22[9:2]									-
24 th parameter	1	R_N_GAMMA23[9:2]									-
25 th parameter	1	R_N_GAMMA24[9:2]									-
26 th parameter	1	R_N_GAMMA25[9:2]									-
27 th parameter	1	R_N_GAMMA26[9:2]									-
28 th parameter	1	R_N_GAMMA27[9:2]									-
29 th parameter	1	R_N_GAMMA28[9:2]									-
30 th parameter	1	R_N_GAMMA29[9:2]									-
31 st parameter	1	R_N_GAMMA30[9:2]									-
32 nd parameter	1	R_N_GAMMA31[9:2]									-
33 rd parameter	1	R_N_GAMMA32[9:2]									-
34 th parameter	1	R_N_GAMMA0[1:0]	R_N_GAMMA1[1:0]	R_N_GAMMA2[1:0]	R_N_GAMMA3[1:0]					-	
35 th parameter	1	R_N_GAMMA4[1:0]	R_N_GAMMA5[1:0]	R_N_GAMMA6[1:0]	R_N_GAMMA7[1:0]					-	
36 th parameter	1	R_N_GAMMA8[1:0]	R_N_GAMMA9[1:0]	R_N_GAMMA10[1:0]	R_N_GAMMA11[1:0]					-	
37 th parameter	1	R_N_GAMMA12[1:0]	R_N_GAMMA13[1:0]	R_N_GAMMA14[1:0]	R_N_GAMMA15[1:0]					-	
38 th parameter	1	R_N_GAMMA16[1:0]	R_N_GAMMA17[1:0]	R_N_GAMMA18[1:0]	R_N_GAMMA19[1:0]					-	
39 th parameter	1	R_N_GAMMA20[1:0]	R_N_GAMMA21[1:0]	R_N_GAMMA22[1:0]	R_N_GAMMA23[1:0]					-	
40 th parameter	1	R_N_GAMMA24[1:0]	R_N_GAMMA25[1:0]	R_N_GAMMA26[1:0]	R_N_GAMMA27[1:0]					-	
41 st parameter	1	R_N_GAMMA28[1:0]	R_N_GAMMA29[1:0]	R_N_GAMMA30[1:0]	R_N_GAMMA31[1:0]					-	
42 nd parameter	1	R_N_GAMMA32[1:0]	-	-	-	-	-	-	-	-	

Bank1							
1 st parameter	1	G_N_GAMMA0[9:2]				-	
2 nd parameter	1	G_N_GAMMA1[9:2]				-	
3 rd parameter	1	G_N_GAMMA2[9:2]				-	
4 th parameter	1	G_N_GAMMA3[9:2]				-	
5 th parameter	1	G_N_GAMMA4[9:2]				-	
6 th parameter	1	G_N_GAMMA5[9:2]				-	
7 th parameter	1	G_N_GAMMA6[9:2]				-	
8 th parameter	1	G_N_GAMMA7[9:2]				-	
9 th parameter	1	G_N_GAMMA8[9:2]				-	
10 th parameter	1	G_N_GAMMA9[9:2]				-	
11 st parameter	1	G_N_GAMMA10[9:2]				-	
12 nd parameter	1	G_N_GAMMA11[9:2]				-	
13 rd parameter	1	G_N_GAMMA12[9:2]				-	
14 th parameter	1	G_N_GAMMA13[9:2]				-	
15 th parameter	1	G_N_GAMMA14[9:2]				-	
16 th parameter	1	G_N_GAMMA15[9:2]				-	
17 th parameter	1	G_N_GAMMA16[9:2]				-	
18 th parameter	1	G_N_GAMMA17[9:2]				-	
19 th parameter	1	G_N_GAMMA18[9:2]				-	
20 th parameter	1	G_N_GAMMA19[9:2]				-	
21 st parameter	1	G_N_GAMMA20[9:2]				-	
22 nd parameter	1	G_N_GAMMA21[9:2]				-	
23 rd parameter	1	G_N_GAMMA22[9:2]				-	
24 th parameter	1	G_N_GAMMA23[9:2]				-	
25 th parameter	1	G_N_GAMMA24[9:2]				-	
26 th parameter	1	G_N_GAMMA25[9:2]				-	
27 th parameter	1	G_N_GAMMA26[9:2]				-	
28 th parameter	1	G_N_GAMMA27[9:2]				-	
29 th parameter	1	G_N_GAMMA28[9:2]				-	
30 th parameter	1	G_N_GAMMA29[9:2]				-	
31 st parameter	1	G_N_GAMMA30[9:2]				-	
32 nd parameter	1	G_N_GAMMA31[9:2]				-	
33 rd parameter	1	G_N_GAMMA32[9:2]				-	
34 th parameter	1	G_N_GAMMA0[1:0]	G_N_GAMMA1[1:0]	G_N_GAMMA2[1:0]	G_N_GAMMA3[1:0]	-	
35 th parameter	1	G_N_GAMMA4[1:0]	G_N_GAMMA5[1:0]	G_N_GAMMA6[1:0]	G_N_GAMMA7[1:0]	-	
36 th parameter	1	G_N_GAMMA8[1:0]	G_N_GAMMA9[1:0]	G_N_GAMMA10[1:0]	G_N_GAMMA11[1:0]	-	
37 th parameter	1	G_N_GAMMA12[1:0]	G_N_GAMMA13[1:0]	G_N_GAMMA14[1:0]	G_N_GAMMA15[1:0]	-	
38 th parameter	1	G_N_GAMMA16[1:0]	G_N_GAMMA17[1:0]	G_N_GAMMA18[1:0]	G_N_GAMMA19[1:0]	-	
39 th parameter	1	G_N_GAMMA20[1:0]	G_N_GAMMA21[1:0]	G_N_GAMMA22[1:0]	G_N_GAMMA23[1:0]	-	
40 th parameter	1	G_N_GAMMA24[1:0]	G_N_GAMMA25[1:0]	G_N_GAMMA26[1:0]	G_N_GAMMA27[1:0]	-	
41 st parameter	1	G_N_GAMMA28[1:0]	G_N_GAMMA29[1:0]	G_N_GAMMA30[1:0]	G_N_GAMMA31[1:0]	-	
42 nd parameter	1	G_N_GAMMA32[1:0]	-	-	-	-	
Bank2							
1 st parameter	1	B_N_GAMMA0[9:2]				-	
2 nd parameter	1	B_N_GAMMA1[9:2]				-	
3 rd parameter	1	B_N_GAMMA2[9:2]				-	
4 th parameter	1	B_N_GAMMA3[9:2]				-	

5 th parameter	1	B_N_GAMMA4[9:2]				-
6 th parameter	1	B_N_GAMMA5[9:2]				-
7 th parameter	1	B_N_GAMMA6[9:2]				-
8 th parameter	1	B_N_GAMMA7[9:2]				-
9 th parameter	1	B_N_GAMMA8[9:2]				-
10 th parameter	1	B_N_GAMMA9[9:2]				-
11 st parameter	1	B_N_GAMMA10[9:2]				-
12 nd parameter	1	B_N_GAMMA11[9:2]				-
13 rd parameter	1	B_N_GAMMA12[9:2]				-
14 th parameter	1	B_N_GAMMA13[9:2]				-
15 th parameter	1	B_N_GAMMA14[9:2]				-
16 th parameter	1	B_N_GAMMA15[9:2]				-
17 th parameter	1	B_N_GAMMA16[9:2]				-
18 th parameter	1	B_N_GAMMA17[9:2]				-
19 th parameter	1	B_N_GAMMA18[9:2]				-
20 th parameter	1	B_N_GAMMA19[9:2]				-
21 st parameter	1	B_N_GAMMA20[9:2]				-
22 nd parameter	1	B_N_GAMMA21[9:2]				-
23 rd parameter	1	B_N_GAMMA22[9:2]				-
24 th parameter	1	B_N_GAMMA23[9:2]				-
25 th parameter	1	B_N_GAMMA24[9:2]				-
26 th parameter	1	B_N_GAMMA25[9:2]				-
27 th parameter	1	B_N_GAMMA26[9:2]				-
28 th parameter	1	B_N_GAMMA27[9:2]				-
29 th parameter	1	B_N_GAMMA28[9:2]				-
30 th parameter	1	B_N_GAMMA29[9:2]				-
31 st parameter	1	B_N_GAMMA30[9:2]				-
32 nd parameter	1	B_N_GAMMA31[9:2]				-
33 rd parameter	1	B_N_GAMMA32[9:2]				-
34 th parameter	1	B_N_GAMMA0[1:0]	B_N_GAMMA1[1:0]	B_N_GAMMA2[1:0]	B_N_GAMMA3[1:0]	-
35 th parameter	1	B_N_GAMMA4[1:0]	B_N_GAMMA5[1:0]	B_N_GAMMA6[1:0]	B_N_GAMMA7[1:0]	-
36 th parameter	1	B_N_GAMMA8[1:0]	B_N_GAMMA9[1:0]	B_N_GAMMA10[1:0]	B_N_GAMMA11[1:0]	-
37 th parameter	1	B_N_GAMMA12[1:0]	B_N_GAMMA13[1:0]	B_N_GAMMA14[1:0]	B_N_GAMMA15[1:0]	-
38 th parameter	1	B_N_GAMMA16[1:0]	B_N_GAMMA17[1:0]	B_N_GAMMA18[1:0]	B_N_GAMMA19[1:0]	-
39 th parameter	1	B_N_GAMMA20[1:0]	B_N_GAMMA21[1:0]	B_N_GAMMA22[1:0]	B_N_GAMMA23[1:0]	-
40 th parameter	1	B_N_GAMMA24[1:0]	B_N_GAMMA25[1:0]	B_N_GAMMA26[1:0]	B_N_GAMMA27[1:0]	-
41 st parameter	1	B_N_GAMMA28[1:0]	B_N_GAMMA29[1:0]	B_N_GAMMA30[1:0]	B_N_GAMMA31[1:0]	-
42 nd parameter	1	B_N_GAMMA32[1:0]	-	-	-	-
Description	This command is used to set Negative Polarity Digital Gamma Curve Look-Up Table when DGC_PN=1.					
	R/G/B_N_GAMMA0[9:0] ~ R/G/B_N_GAMMA32[9:0]: MSB 8-bit is setting to mapping related gray level to which gray level voltage of real gamma. LSB 2-bit is for dithering.					
		LUT	Mapping Gray level			
		R_GAMMA0[9:0]	R0			
		R_GAMMA1[9:0]	R8			
		R_GAMMA2[9:0]	R16			
		:	:			
		R_GAMMA31[9:0]	R240			

	R_GAMMA32[9:0]	R255	
	G_GAMMA0[9:0]	G0	
	G_GAMMA1[9:0]	G8	
	G_GAMMA2[9:0]	G16	
	:	:	
	G_GAMMA31[9:0]	G240	
	G_GAMMA32[9:0]	G255	
	B_GAMMA0[9:0]	B0	
	B_GAMMA1[9:0]	B8	
	B_GAMMA2[9:0]	B16	
	:	:	
	B_GAMMA31[9:0]	B240	
	B_GAMMA32[9:0]	B255	
Restrictions	SETEXTC turn on to enable this command.		
Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In or Booster Off		Yes

Himax Confidential
Do Not Copy

6.3.26 SETIDLE (DFh)

DFH	SETIDLE									HEX	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0		
Command	0	1	1	0	1	1	1	1	1	DF	
1 st parameter	1	-	-	-	-	-	NW_I[2:0]			00	
2 nd parameter	1	BP_I[7:0]									08
3 rd parameter	1	FP_I[7:0]									08
4 th parameter	1	RTN_I[7:0]									2F
5 th parameter	1	VCMC_F_I[7:0]									FE
6 th parameter	1	VCMC_B_I[7:0]									FE
7 th parameter	1	AP_I[2:0]			-	-	-	VCMC_B_I[8]	VCMC_F_I[8]	83	
8 th parameter	1	FS0_I[3:0]				FS1_I[3:0]				23	
9 th parameter	1	FS2_I[3:0]				-	-	-	-	30	

Set Idle mode related setting.

NW_I[2:0]: Inversion type setting in idle mode.

NW_I[2:0]			Inversion type
0	0	0	Column inversion
0	0	1	1-dot inversion
0	1	0	2-dot inversion
0	1	1	4-dot inversion
1	0	0	8-dot inversion
1	0	1	Zig-zag inversion
1	1	0	Pixel-column inversion
1	1	1	Inhibited

BP_I[7:0] : Specify the amount of scan line for back porch(BP) in idle mode.

FP_I[7:0]: Specify the amount of scan line for front porch (FP) in idle mode.

FP[7:0]_I / BP_I[7:0]	Number of front porch/ back porch Lines
8h'00	2 lines
8h'01	3 lines
8h'02	4 lines
8h'03	5 lines
8h'04	6 lines
8h'05	7 lines
:	:
8h'FB	253 lines
8h'FC	254 lines
8h'FD	255 lines
8h'FE	256 lines
8h'FF	257 lines

Note: Set BP_I[7:0] = VS + VBP – 2, and FP_I[7:0] = VFP – 2.

RTN_I[7:0]: A cycle time of line width in idle mode.

(1 clock period= 4 OSC period)

RTN_I[7:0]	Clock per Line
8h'00	150 clocks
8h'01	151 clocks
8h'02	152 clocks
:	:
8h'FD	403 clocks
8h'FE	404 clocks
8h'FF	405 clocks

Description

VCMC_F_I[8:0]: Forward scan VCOM voltage control in Idle mode.

VCMC_B_I[8:0]: Backward scan VCOM voltage control in Idle mode.

VCMC_F_I[8:0]/VCMC_B_I[8:0]									VCOM
0	0	0	0	0	0	0	0	0	1.00
0	0	0	0	0	0	0	0	1	0.99V
0	0	0	0	0	0	0	1	0	0.98V
0	0	0	0	0	0	0	1	1	0.97V
0	0	0	0	0	0	1	0	0	0.96V
0	0	0	0	0	0	1	0	1	0.95V
0	0	0	0	0	0	1	1	0	0.94V
0	0	0	0	0	0	1	1	1	0.93V
0	0	0	0	0	1	0	0	0	0.92V
0	0	0	0	0	1	0	0	1	0.91V
0	0	0	0	0	1	0	1	0	0.90V
0	0	0	0	0	1	0	1	1	0.89V
:									:
0	1	1	0	0	1	0	0	0	-1.00V
0	1	1	0	0	1	0	0	1	-1.01V
0	1	1	0	0	1	0	1	0	-1.02V
0	1	1	0	0	1	0	1	1	-1.03V
0	1	1	0	0	1	1	0	0	-1.04V
0	1	1	0	0	1	1	0	1	-1.05V
:									:
1	1	0	0	0	1	1	1	0	-2.98V
1	1	0	0	0	1	1	1	1	-2.99V
1	1	0	0	1	0	0	0	0	-3.00V
Others									Inhibited
1	1	1	1	1	1	1	1	0	VSSA
1	1	1	1	1	1	1	1	1	HZ

AP_I[2:0]: Adjust the amount of fixed current from the fixed current source for the operational amplifier in idle mode.

AP_I[2:0]			Constant Current of Operational Amplifier
0	0	0	Stop
0	0	1	0.5μA
0	1	0	1.0μA
0	1	1	1.5μA
1	0	0	2.0μA
1	0	1	2.5μA
1	1	0	3.0μA
1	1	1	3.5μA

FS0_I[3:0]: Set the operating frequency of the step-up circuit for VSP and VSN voltage generation in idle mode. (Fosc_pump=5.68MHz)

FS0_I[3:0]				Operation Frequency of Step-up Circuit
0	0	0	0	Fosc_pump/2
0	0	0	1	Fosc_pump/4
0	0	1	0	Fosc_pump/8
0	0	1	1	Fosc_pump/16
0	1	0	0	Fosc_pump/32
0	1	0	1	Fosc_pump/48
0	1	1	0	Fosc_pump/64
0	1	1	1	Fosc_pump/80
1	0	0	0	Fosc_pump/96
1	0	0	1	Fosc_pump/112
1	0	1	0	Fosc_pump/128
1	0	1	1	Fosc_pump/144
1	1	0	0	Fosc_pump/160
1	1	0	1	Fosc_pump/176
1	1	1	0	Fosc_pump/192
1	1	1	1	Fosc_pump/208

FS1_I[3:0]: Set the operating frequency of the step-up circuit for VGH voltage generation in idle mode. (Fosc_pump=5.68MHz)

FS1_I[3:0]				Operation Frequency of Step-up Circuit
0	0	0	0	Fosc_pump/72
0	0	0	1	Fosc_pump/96
0	0	1	0	Fosc_pump/128
0	0	1	1	Fosc_pump/160
0	1	0	0	Fosc_pump/192
0	1	0	1	Fosc_pump/224
0	1	1	0	Fosc_pump/256
0	1	1	1	Fosc_pump/336
1	0	0	0	Hsync*4
1	0	0	1	Hsync*2
1	0	1	0	Hsync
1	0	1	1	Hsync/2
1	1	0	0	Hsync/4
1	1	0	1	Hsync/8
1	1	1	0	Hsync/16
1	1	1	1	Inhibited

FS2_I[3:0]: Adjust the charge pump frequency of VGL in idle mode. (Fosc_pump=5.68MHz)

FS2_I[3:0]				Operation Frequency of Step-up Circuit
0	0	0	0	Fosc_pump/72
0	0	0	1	Fosc_pump/96
0	0	1	0	Fosc_pump/128
0	0	1	1	Fosc_pump/160
0	1	0	0	Fosc_pump/192
0	1	0	1	Fosc_pump/224
0	1	1	0	Fosc_pump/256
0	1	1	1	Fosc_pump/1336
1	0	0	0	Hsync*4
1	0	0	1	Hsync*2
1	0	1	0	Hsync
1	0	1	1	Hsync/2
1	1	0	0	Hsync/4
1	1	0	1	Hsync/8
1	1	1	0	Hsync/16

» HX8399-C

1080RGBx2400dots, LTPS Mobile Single Chip Driver



DATA SHEET V01

	1	1	1	1	Inhibited
Restrictions	SETEXTC turn on to enable this command				
Register Availability	Status			Availability	
	Normal Mode On, Idle Mode Off, Sleep Out			Yes	
	Normal Mode On, Idle Mode On, Sleep Out			Yes	
	Sleep In or Booster Off			Yes	

Himax Confidential
Do Not Copy

6.3.27 SETGAMMA: Set gamma curve related setting (E0h)

E0H	SETGAMMA (Set Gamma Curve Related Setting)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	1	0	0	0	0	0	E0
1 st Parameter	1	-	VHP_0[6:0]							00
2 nd parameter	1	-	VHP_1[6:0]							0B
3 rd parameter	1	-	VHP_2[6:0]							1D
4 th parameter	1	-	VHP_3[6:0]							1F
5 th parameter	1				VMP_0[7:0]				57	
6 th parameter	1				VMP_1[7:0]				6D	
7 th parameter	1				VMP_2[7:0]				78	
8 th parameter	1				VMP_3[7:0]				7E	
9 th parameter	1				VMP_4[7:0]				86	
10 th parameter	1				VMP_5[7:0]				92	
11 st parameter	1				VMP_6[7:0]				98	
12 nd parameter	1				VMP_7[7:0]				9F	
13 rd parameter	1				VMP_8[7:0]				A9	
14 th parameter	1				VMP_9[7:0]				B9	
15 th parameter	1				VMP_10[7:0]				BE	
16 th parameter	1				VMP_11[7:0]				BD	
17 th parameter	1				VMP_12[7:0]				C4	
18 th parameter	1				VMP_13[7:0]				CE	
19 th parameter	1				VMP_14[7:0]				D3	
20 th parameter	1				VMP_15[7:0]				DC	
21 st parameter	1				VMP_16[7:0]				CC	
22 nd parameter	1				VMP_17[7:0]				D4	
23 rd parameter	1				VMP_18[7:0]				D2	
24 th parameter	1	-				VLP_0[6:0]				67
25 th parameter	1	-				VLP_1[6:0]				60
26 th parameter	1	-				VLP_2[6:0]				6A
27 th parameter	1	-				VLP_3[6:0]				77
28 th parameter	1	-				VHN_0[6:0]				00
29 th parameter	1	-				VHN_1[6:0]				0B
30 th parameter	1	-				VHN_2[6:0]				1D
31 st parameter	1	-				VHN_3[6:0]				1F
32 nd parameter	1				VMN_0[7:0]				57	
33 rd parameter	1				VMN_1[7:0]				6D	
34 th parameter	1				VMN_2[7:0]				78	
35 th parameter	1				VMN_3[7:0]				7E	
36 th parameter	1				VMN_4[7:0]				86	
37 th parameter	1				VMN_5[7:0]				92	
38 th parameter	1				VMN_6[7:0]				98	
39 th parameter	1				VMN_7[7:0]				9F	
40 th parameter	1				VMN_8[7:0]				A9	
41 st parameter	1				VMN_9[7:0]				B9	
42 nd parameter	1				VMN_10[7:0]				BE	
43 rd parameter	1				VMN_11[7:0]				BD	
44 th parameter	1				VMN_12[7:0]				C4	
45 th parameter	1				VMN_13[7:0]				CE	
46 th parameter	1				VMN_14[7:0]				D3	
47 th parameter	1				VMN_15[7:0]				DC	
48 th parameter	1				VMN_16[7:0]				CC	
49 th parameter	1				VMN_17[7:0]				D4	
50 th parameter	1				VMN_18[7:0]				D2	
51 st parameter	1	-				VLN_0[6:0]				67
52 nd parameter	1	-				VLN_1[6:0]				60

53 rd parameter	1	-	VLN_2[6:0]	6A
54 th parameter	1	-	VLN_3[6:0]	77
Description	This command is to set gamma register.			
	Register Groups	Positive Polarity	Negative Polarity	Description
	Up Edge adjustment	VHP0 6-0	VHN0 6-0	128-to-1 selector (voltage level of grayscale 255)
		VHP1 6-0	VHN1 6-0	128-to-1 selector (voltage level of grayscale 251)
		VHP2 6-0	VHN2 6-0	128-to-1 selector (voltage level of grayscale 247)
		VHP3 6-0	VHN3 6-0	128-to-1 selector (voltage level of grayscale 243)
	Center adjustment	VMP0 7-0	VMN0 7-0	256-to-1 selector (voltage level of grayscale 235)
		VMP1 7-0	VMN1 7-0	256-to-1 selector (voltage level of grayscale 227)
		VMP2 7-0	VMN2 7-0	256-to-1 selector (voltage level of grayscale 215)
		VMP3 7-0	VMN3 7-0	256-to-1 selector (voltage level of grayscale 203)
		VMP4 7-0	VMN4 7-0	256-to-1 selector (voltage level of grayscale 191)
		VMP5 7-0	VMN5 7-0	256-to-1 selector (voltage level of grayscale 179)
		VMP6 7-0	VMN6 7-0	256-to-1 selector (voltage level of grayscale 167)
		VMP7 7-0	VMN7 7-0	256-to-1 selector (voltage level of grayscale 155)
		VMP8 7-0	VMN8 7-0	256-to-1 selector (voltage level of grayscale 143)
		VMP9 7-0	VMN9 7-0	256-to-1 selector (voltage level of grayscale 127)
		VMP10 7-0	VMN10 7-0	256-to-1 selector (voltage level of grayscale 111)
		VMP11 7-0	VMN11 7-0	256-to-1 selector (voltage level of grayscale 99)
		VMP12 7-0	VMN12 7-0	256-to-1 selector (voltage level of grayscale 87)
		VMP13 7-0	VMN13 7-0	256-to-1 selector (voltage level of grayscale 75)
		VMP14 7-0	VMN14 7-0	256-to-1 selector (voltage level of grayscale 63)
		VMP15 7-0	VMN15 7-0	256-to-1 selector (voltage level of grayscale 51)
		VMP16 7-0	VMN16 7-0	256-to-1 selector (voltage level of grayscale 39)
		VMP17 7-0	VMN17 7-0	256-to-1 selector (voltage level of grayscale 27)
	VMP18 7-0	VMN18 7-0	256-to-1 selector (voltage level of grayscale 19)	
	Down Edge adjustment	VLP0 6-0	VLN0 6-0	128-to-1 selector (voltage level of grayscale 12)
		VLP1 6-0	VLN1 6-0	128-to-1 selector (voltage level of grayscale 8)
VLP2 6-0		VLN2 6-0	128-to-1 selector (voltage level of grayscale 4)	
VLP3 6-0		VLN3 6-0	128-to-1 selector (voltage level of grayscale 0)	
Restriction	SETEXTC turn on to enable this command.			
Register Availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In or Booster Off		Yes	

6.3.28 SETCHEMODE_DYN (E4h)





E4H	SETCHEMODE_DYN (Set color enhancement mode, dynamic)																											
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	0	1	1	1	0	0	1	0	0	E4																		
1 st parameter	1	-	-	-	-	-	-	-	DYN_C EH_EN	01																		
2 nd parameter	1	HUE_MODE[1:0]		SE_MODE[1:0]		BE_MODE[1:0]		CE_MODE[1:0]		00																		
Description	<p>This command is to set color enhancement and dynamic mode.</p> <p>DYN_CHE_EN: Select the color enhancement reload mode. 0: static mode, 1: dynamic mode.</p> <p>CE_MODE[1:0]: Set color (saturation) enhancement.</p> <p>BE_MODE[1:0]: Set brightness enhancement.</p> <p>SE_MODE[1:0]: Set sharpness enhancement.</p> <p>HUE_MODE[1:0]: Set hue enhancement.</p> <p>In Static mode: Enhancement level selection: when SE/BE/CE/HUE is turn on, the enhancement effect depends on the gobal gain curve set by user in command RE5h and RE6h.</p> <table border="1"> <thead> <tr> <th>CE_MODE[1:0]/ BE_MODE[1:0]/ SE_MODE[1:0]/ HUE_MODE[1:0]</th> <th>Enhance</th> </tr> </thead> <tbody> <tr> <td>0 0 0 0</td> <td>Off</td> </tr> <tr> <td>0 0 1 0</td> <td rowspan="3">On</td> </tr> <tr> <td>1 0 0 0</td> </tr> <tr> <td>1 0 1 0</td> </tr> </tbody> </table> <p>In Dynamic mode: Enhance level selection. wWhen SE/BE/CE/HUE turn on, the enhancement gain setting will be read from the ROM table. Three sets of enhancement gain are provide for selection.</p> <table border="1"> <thead> <tr> <th>CE_MODE[1:0]/ BE_MODE[1:0]/ SE_MODE[1:0]/ HUE_MODE[1:0]</th> <th>Enhance</th> </tr> </thead> <tbody> <tr> <td>0 0 0 0</td> <td>Off</td> </tr> <tr> <td>0 0 1 0</td> <td>Low</td> </tr> <tr> <td>1 0 0 0</td> <td>Medium</td> </tr> <tr> <td>1 0 1 0</td> <td>High</td> </tr> </tbody> </table>										CE_MODE[1:0]/ BE_MODE[1:0]/ SE_MODE[1:0]/ HUE_MODE[1:0]	Enhance	0 0 0 0	Off	0 0 1 0	On	1 0 0 0	1 0 1 0	CE_MODE[1:0]/ BE_MODE[1:0]/ SE_MODE[1:0]/ HUE_MODE[1:0]	Enhance	0 0 0 0	Off	0 0 1 0	Low	1 0 0 0	Medium	1 0 1 0	High
	CE_MODE[1:0]/ BE_MODE[1:0]/ SE_MODE[1:0]/ HUE_MODE[1:0]	Enhance																										
	0 0 0 0	Off																										
	0 0 1 0	On																										
	1 0 0 0																											
	1 0 1 0																											
	CE_MODE[1:0]/ BE_MODE[1:0]/ SE_MODE[1:0]/ HUE_MODE[1:0]	Enhance																										
	0 0 0 0	Off																										
	0 0 1 0	Low																										
	1 0 0 0	Medium																										
1 0 1 0	High																											
Color Enhancemet																												
Off		Low		Medium		High																						
Brightness Enhancement																												
Off		Low		Medium		High																						
Sharpness Enhancement																												
Off		Low		Medium		High																						

» **HX8399-C**

1080RGBx2400dots, LTPS Mobile Single Chip Driver



DATA SHEET V01

				
Restrictions	SETEXTC turn on to enable this command.			
Register Availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In or Booster Off		Yes	

Himax Confidential
Do Not Copy

6.3.29 SET I2C_SA: Set I2C slave address (E8h)

E8H	SETI2C_SA(Set I2C Slave Address)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	1	0	1	0	0	0	E8
1 st parameter	1	-	I2C_SA[6:0]							00
Description	This register is for setting I2C slave address.									
	I2C_SA[6 :0]					Slave address (A6-A0)				
	000_0000					000_0000				
	000_0001~000_0111					Reserved				
	000_1000					000_1000				
	:					:				
	111_0110					111_0110				
	111_0111					111_0111				
111_1xxx					Reserved					
Restrictions	SETEXTC turn on to enable this command									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				

6.3.30 SET_SP_CMD (E9h)

E9H	SET_SP_CMD									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	1	0	1	0	0	1	E9
1 st parameter	1	FORCE_OPT	RAND_WR_SERIAL_EN	RAND_WR_CNT[5:0]						3F
Description	This command is used to directly set register value of specific parameter. FORCE_OPT: 0: disable, 1: enable RAND_WR_SERIAL_EN: Set to "1" for more than 1 parameter access. RAND_WR_CNT[5:0]: Specify the parameter index.									
Restrictions	SETEXTC turn on to enable this command.									
Register Availability	Status		Availability							
	Normal Mode On, Idle Mode Off, Sleep Out		Yes							
	Normal Mode On, Idle Mode On, Sleep Out		Yes							
	Sleep In or Booster Off		Yes							

Himax Confidential
Do Not Copy

6.3.31 SETCNCD/GETCNCD (FDh)

FDH	SETCNCD/GETCNCD (Set/Get Continue Command)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	1	1	1	1	0	1	FD
1 st parameter	1	WR_CMD_CN[7:0]								-
Description	This function is use to instead of Register-Content interface mode. The parameter for SETCNCD will continue to write or read from the last command address automatically.									
Restrictions	SETEXTC turn on to enable this command									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				

Himax Confidential
Do Not Copy

6.3.32 SETREADINDEX: Set SPI Read Index (FEh)

FEH	SET SPI READ INDEX (Set SPI READ Command Address)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	1	1	1	1	1	0	FE
1 st parameter	1	CMD_ADD[7:0]								-
Description	SET SPI Read Command Address for User Define Command.									
Restrictions	SETEXTC turn on to enable this command									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				

Himax Confidential
Do Not Copy

6.3.33 GETSPIREAD: SPI Read Command Data (FFh)

FFH	GETSPIREAD (Read Command Data)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	1	1	1	1	1	1	FF
1 st parameter	1	CMD_DATA1[7:0]								-
:	1	:								-
n th parameter	1	CMD_DATA _n [7:0]								-
Description	Read SPI Command Data for User Define Command.									
Restrictions	SETEXTC turn on to enable this command.									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				

Himax Confidential
Do Not Copy

7. Layout Recommendation

7.1 Maximum layout resistance

Name	Type	Maximum series resistance	Unit
VDD1	Power supply	5	Ω
VDD3	Power supply	5	Ω
VSSD	Power supply	5	Ω
VSSA	Power supply	5	Ω
HS_VCC	Power supply	5	Ω
HS_VSS	Power supply	5	Ω
VSSAC	Power supply	5	Ω
IM[2:0]	Input	100	Ω
DSWAP[1:0], PNSWAP	Input	100	Ω
SCL, DCX, CSX, RESX	Input	100	Ω
HSYNC, VSYNC, DE, PCLK	Input	100	Ω
SDI_SDA	Input	100	Ω
SDO	Output	100	Ω
DB[7:0]	Input + Output	100	Ω
CABC_PWM_OUT, TE, TE1, VCSW1, VCSW2	Output	100	Ω
VCOM	Output	10	Ω
HS_CLKP, HS_CLKN	Input	5	Ω
HS_D0P, HS_D0N	Input + Output	5	Ω
HS_D1P, HS_D1N	Input	5	Ω
HS_D2P, HS_D2N	Input	5	Ω
HS_D3P, HS_D3N	Input	5	Ω
PCCS[2:0]	Input	100	
VDDD	Capacitor Connection	5	Ω
VSP	Capacitor Connection	5	Ω
VSN	Capacitor Connection	5	Ω
VGH, VGL, VGHO, VGLO	Capacitor Connection	10	Ω
HS_LDO	Capacitor Connection	5	Ω
OSC	Input	100	Ω
C31P, C31N,	Capacitor Connection	5	Ω
C21P, C21N	Capacitor Connection	5	Ω
TEST[2:0]	Input	100	Ω
VTESTOUTP, VTESTOUTN	Output	100	Ω

Table 7.1: Maximum Layout Resistance(include IC and FPC bonding)

7.2 External Components Connection

7.2.1 HX5186-A/B/C mode

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)---- --- (+)---- VSSA	1.0 μ F
VGH	C2	Connect to Capacitor (Max 25V): VGH ---(+)- --- (-)---- VSSA	1.0 μ F
VGL	C3	Connect to Capacitor (Max 25V): VGL ---(-)---- --- (+)---- VSSA	1.0 μ F
	D1	Connect to Schottky Diode(VR \geq 30V): VSSA ---(-)---- --- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR \geq 30V (Recommended diode: RB521S-30)
C21P – C21N	C4	Connect to Capacitor (Max 16V): C21P ---(+)- --- (-)---- C21N	1.0 μ F
C31P – C31N	C5	Connect to Capacitor (Max 16V): C31P ---(+)- --- (-)---- C31N	1.0 μ F
VDDD	C6	Connect to Capacitor (Max 6V): VDDD ---(+)- --- (-)---- VSSA	2.2 μ F
VSP	C7	Connect to Capacitor (Max 10V): VSP ---(+)- --- (-)---- VSSA	2.2 μ F
VSN	C8	Connect to Capacitor (Max 10V): VSN ---(-)---- --- (+)---- VSSA	2.2 μ F
VDD3	C9	Connect to Capacitor (Max 10V): VDD3 ---(+)- --- (-)---- VSSA	2.2 μ F
VDD1	C10	Connect to Capacitor (Max 6V): VDD1 ---(+)- --- (-)---- VSSA	2.2 μ F
HS_VCC	C11	Connect to Capacitor (Max 6V): HS_VCC ---(+)- --- (-)---- VSSA (The capacitor can be reduced, if HS_VCC is connected to VDD1)	2.2 μ F
HS_LDO	C12	Connect to Capacitor (Max 6V): HS_LDO ---(+)- --- (-)---- HS_VSS	2.2 μ F
VGHO	C13	Connect to Capacitor (Max 16V): VGHO ---(+)- --- (-)---- VSSA	1.0 μ F
VGLO	C14	Connect to Capacitor (Max 16V): VGLO ---(-)---- --- (+)---- VSSA	1.0 μ F
HX5186-C	U1	Please refer HX5186-C datasheet	-
HX5186-C	C15	Please refer HX5186-C datasheet	1.0uF
HX5186-C	C16	Please refer HX5186-C datasheet	1.0uF
HX5186-C	C17	Please refer HX5186-C datasheet	1.0uF

Table 7.2: HX5186-C mode external components

7.2.2 PFM Type–A mode

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)---- --- (+)----- VSSA	1.0 μF
VGH	C2	Connect to Capacitor (Max 25V): VGH ---(+)- --- (-)----- VSSA	1.0 μF
VGL	C3	Connect to Capacitor (Max 25V): VGL ---(-)---- --- (+)----- VSSA	1.0 μF
	D1	Connect to Schottky Diode(VR≥30V): VSSA ---(-)---- ◀--- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
C21P – C21N	C4	Connect to Capacitor (Max 16V): C21P ---(+)- --- (-)-----C21N	1.0 μF
C31P – C31N	C5	Connect to Capacitor (Max 16V): C31P ---(+)- --- (-)-----C31N	1.0 μF
VDDD	C6	Connect to Capacitor (Max 6V): VDDD ---(+)- --- (-)-----VSSA	2.2 μF
VSP	C7	Connect to Capacitor (Max 10V):VSP ---(+)- --- (-)-----VSSA	2.2 μF
VSN	C8	Connect to Capacitor (Max 10V):VSN ---(-)---- --- (+)-----VSSA	2.2 μF
VDD3	C9	Connect to Capacitor (Max 10V): VDD3 ---(+)- --- (-)-----VSSA	2.2 μF
VDD1	C10	Connect to Capacitor (Max 6V): VDD1 ---(+)- --- (-)-----VSSA	2.2 μF
HS_VCC	C11	Connect to Capacitor (Max 6V): HS_VCC ---(+)- --- (-)-----VSSA (The capacitor can be reduced, if HS_VCC is connected to VDD1)	2.2 μF
HS_LDO	C12	Connect to Capacitor (Max 6V): HS_LDO ---(+)- --- (-)-----HS_VSS	2.2 μF
VGHO	C13	Connect to Capacitor (Max 16V): VGHO ---(+)- --- (-)-----VSSA	1.0 μF
VGLO	C14	Connect to Capacitor (Max 16V): VGLO ---(-)---- --- (+)-----VSSA	1.0 μF
PFM	L1	Inductance, reference PFM Type A connection	-
PFM	SW1	MOS switch, reference PFM Type A connection	-
PFM	SW2	MOS switch, reference PFM Type A connection	-
PFM	D2	Schottkey diode, reference PFM Type A connection	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
PFM	D3	Schottkey diode, reference PFM Type A connection	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)

Table 7.3: PFM Type A mode external components

7.2.3 PFM Type-D mode

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)---- --- (+)----- VSSA	1.0 μ F
VGH	C2	Connect to Capacitor (Max 25V): VGH ---(+)----- --- (-)----- VSSA	1.0 μ F
VGL	C3	Connect to Capacitor (Max 25V): VGL ---(-)---- --- (+)----- VSSA	1.0 μ F
	D1	Connect to Schottky Diode(VR \geq 30V): VSSA ---(-)---- ◀--- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR \geq 30V (Recommended diode: RB521S-30)
C21P – C21N	C4	Connect to Capacitor (Max 16V): C21P ---(+)----- --- (-)-----C21N	1.0 μ F
C31P – C31N	C5	Connect to Capacitor (Max 16V): C31P ---(+)----- --- (-)-----C31N	1.0 μ F
VDDD	C6	Connect to Capacitor (Max 6V): VDDD ---(+)----- --- (-)-----VSSA	2.2 μ F
VSP	C7	Connect to Capacitor (Max 10V):VSP ---(+)----- --- (-)-----VSSA	2.2 μ F
VSN	C8	Connect to Capacitor (Max 10V):VSN ---(-)---- --- (+)-----VSSA	2.2 μ F
VDD3	C9	Connect to Capacitor (Max 10V): VDD3 ---(+)----- --- (-)-----VSSA	2.2 μ F
VDD1	C10	Connect to Capacitor (Max 6V): VDD1 ---(+)----- --- (-)-----VSSA	2.2 μ F
HS_VCC	C11	Connect to Capacitor (Max 6V): HS_VCC ---(+)----- --- (-)-----VSSA	2.2 μ F
HS_LDO	C12	Connect to Capacitor (Max 6V): HS_LDO ---(+)----- --- (-)-----HS_VSS (The capacitor can be reduced, if HS_VCC is connected to VDD1)	2.2 μ F
VGHO	C13	Connect to Capacitor (Max 16V): VGHO ---(+)----- --- (-)-----VSSA	1.0 μ F
VGLO	C14	Connect to Capacitor (Max 16V): VGLO ---(-)---- --- (+)-----VSSA	1.0 μ F
PFM	L1	Inductance, reference PFM Type D connection	-
PFM	SW1	MOS switch, reference PFM Type D connection	-
PFM	D2	Schottkey diode, reference PFM Type D connection	VF < 0.4V / 20mA @ 25°C, VR \geq 30V (Recommended diode: RB521S-30)

Table 7.4: PFM Type D mode external components

7.2.4 PFM Type-C mode

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)---- --- (+)----- VSSA	1.0µF
VGH	C2	Connect to Capacitor (Max 25V): VGH ---(+)----- --- (-)----- VSSA	1.0 µF
VGL	C3	Connect to Capacitor (Max 25V): VGL ---(-)---- --- (+)----- VSSA	1.0 µF
	D1	Connect to Schottky Diode(VR≥30V): VSSA ---(-)---- ◀--- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
C21P – C21N	C4	Connect to Capacitor (Max 16V): C21P ---(+)----- --- (-)-----C21N	1.0 µF
C31P – C31N	C5	Connect to Capacitor (Max 16V): C31P ---(+)----- --- (-)-----C31N	1.0 µF
VDDD	C6	Connect to Capacitor (Max 6V): VDDD ---(+)----- --- (-)-----VSSA	2.2 µF
VSP	C7	Connect to Capacitor (Max 10V):VSP ---(+)----- --- (-)-----VSSA	2.2 µF
VSN	C8	Connect to Capacitor (Max 10V):VSN ---(-)---- --- (+)-----VSSA	2.2 µF
VDD3	C9	Connect to Capacitor (Max 10V): VDD3 ---(+)----- --- (-)-----VSSA	2.2 µF
VDD1	C10	Connect to Capacitor (Max 6V): VDD1 ---(+)----- --- (-)-----VSSA	2.2 µF
HS_VCC	C11	Connect to Capacitor (Max 6V): HS_VCC ---(+)----- --- (-)-----VSSA (The capacitor can be reduced, if HS_VCC is connected to VDD1)	2.2 µF
HS_LDO	C12	Connect to Capacitor (Max 6V): HS_LDO ---(+)----- --- (-)-----HS_VSS	2.2 µF
VGHO	C13	Connect to Capacitor (Max 16V): VGHO ---(+)----- --- (-)-----VSSA	1.0 µF
VGLO	C14	Connect to Capacitor (Max 16V): VGLO ---(-)---- --- (+)-----VSSA	1.0 µF
PFM	L1	Inductance, reference PFM Type C connection	-
PFM	SW1	MOS switch, reference PFM Type C connection	-
PFM	D2	Schottkey diode, reference PFM Type C connection	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
PFM	D3	Schottkey diode, reference PFM Type C connection	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
PFM	D4	Schottkey diode, reference PFM Type C connection	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
PFM	C14	Capacitor, reference PFM Type C connection	1.0uF

Table 7.5: PFM Type C mode external components

7.2.5 External VSP/VSN mode

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)---- --- (+)----- VSSA	1.0 μ F
VGH	C2	Connect to Capacitor (Max 25V): VGH ---(+)---- --- (-)----- VSSA	1.0 μ F
VGL	C3	Connect to Capacitor (Max 25V): VGL ---(-)---- --- (+)----- VSSA	1.0 μ F
	D1	Connect to Schottky Diode(VR \geq 30V): VSN ---(-)---- ◀--- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR \geq 30V (Recommended diode: RB521S-30)
C21P – C21N	C4	Connect to Capacitor (Max 16V): C21P ---(+)---- --- (-)-----C21N	1.0 μ F
C31P – C31N	C5	Connect to Capacitor (Max 16V): C31P ---(+)---- --- (-)-----C31N	1.0 μ F
VDDD	C6	Connect to Capacitor (Max 6V): VDDD ---(+)---- --- (-)-----VSSA	2.2 μ F
VSP	C7	Connect to Capacitor (Max 10V):VSP ---(+)---- --- (-)-----VSSA	2.2 μ F
VSN	C8	Connect to Capacitor (Max 10V):VSN ---(-)---- --- (+)-----VSSA	2.2 μ F
VDD3	C9	Connect to Capacitor (Max 10V): VDD3 ---(+)---- --- (-)-----VSSA	2.2 μ F
VDD1	C10	Connect to Capacitor (Max 6V): VDD1 ---(+)---- --- (-)-----VSSA	2.2 μ F
HS_VCC	C11	Connect to Capacitor (Max 6V): HS_VCC ---(+)---- --- (-)-----VSSA (The capacitor can be reduced, if HS_VCC is connected to VDD1)	2.2 μ F
HS_LDO	C12	Connect to Capacitor (Max 6V): HS_LDO ---(+)---- --- (-)----HS_VSS	2.2 μ F
VGHO	C13	Connect to Capacitor (Max 16V): VGHO ---(+)---- --- (-)-----VSSA	1.0 μ F
VGLO	C14	Connect to Capacitor (Max 16V): VGLO ---(-)---- --- (+)-----VSSA	1.0 μ F

Table 7.6: External VSP/VSN mode external components

7.2.6 External VDD3/VSP/VSN mode

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)---- --- (+)----- VSSA	2.2 μ F
VGH	C2	Connect to Capacitor (Max 25V): VGH ---(+)---- --- (-)----- VSSA	1.0 μ F
VGL	C3	Connect to Capacitor (Max 25V): VGL ---(-)---- --- (+)----- VSSA	1.0 μ F
	D1	Connect to Schottky Diode(VR \geq 30V): VSN---(-)---- ◀--- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR \geq 30V (Recommended diode: RB521S-30)
C21P – C21N	C4	Connect to Capacitor (Max 16V): C21P ---(+)---- --- (-)-----C21N	1.0 μ F
C31P – C31N	C5	Connect to Capacitor (Max 16V): C31P ---(+)---- --- (-)-----C31N	1.0 μ F
VDDD	C6	Connect to Capacitor (Max 6V): VDDD ---(+)---- --- (-)-----VSSA	2.2 μ F
VSP	C7	Connect to Capacitor (Max 10V):VSP ---(+)---- --- (-)-----VSSA	2.2 μ F
VSN	C8	Connect to Capacitor (Max 10V):VSN ---(-)---- --- (+)-----VSSA	2.2 μ F
VDD3	C9	Connect to Capacitor (Max 10V): VDD3 ---(+)---- --- (-)-----VSSA	2.2 μ F
VDD1	C10	Connect to Capacitor (Max 6V): VDD1 ---(+)---- --- (-)-----VSSA	2.2 μ F
HS_VCC	C11	Connect to Capacitor (Max 6V): HS_VCC ---(+)---- --- (-)-----VSSA (The capacitor can be reduced, if HS_VCC is connected to VDD1)	2.2 μ F
HS_LDO	C12	Connect to Capacitor (Max 6V): HS_LDO ---(+)---- --- (-)----HS_VSS	2.2 μ F
VGHO	C13	Connect to Capacitor (Max 16V): VGHO ---(+)---- --- (-)-----VSSA	1.0 μ F
VGLO	C14	Connect to Capacitor (Max 16V): VGLO ---(-)---- --- (+)-----VSSA	1.0 μ F

Table 7.7: External VDD3/VSP/VSN mode external components

7.2.7 External VSP/VSN/VGH/VGL mode

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)---- --- (+)---- VSSA	1.0 μ F
VGH	C2	Connect to Capacitor (Max 25V): VGH ---(+)---- --- (-)---- VSSA	1.0 μ F
VGL	C3	Connect to Capacitor (Max 25V): VGL ---(-)---- --- (+)---- VSSA	1.0 μ F
VDDD	C4	Connect to Capacitor (Max 6V): VDDD ---(+)---- --- (-)----VSSA	2.2 μ F
VSP	C5	Connect to Capacitor (Max 10V):VSP ---(+)---- --- (-)----VSSA	2.2 μ F
VSN	C6	Connect to Capacitor (Max 10V):VSN ---(-)---- --- (+)----VSSA	2.2 μ F
VDD3	C7	Connect to Capacitor (Max 10V): VDD3 ---(+)---- --- (-)----VSSA	2.2 μ F
VDD1	C8	Connect to Capacitor (Max 6V): VDD1 ---(+)---- --- (-)----VSSA	2.2 μ F
HS_VCC	C9	Connect to Capacitor (Max 6V): HS_VCC ---(+)---- --- (-)----VSSA (The capacitor can be reduced, if HS_VCC is connected to VDD1)	2.2 μ F
HS_LDO	C10	Connect to Capacitor (Max 6V): HS_LDO ---(+)---- --- (-)----HS_VSS	2.2 μ F
VGHO	C11	Connect to Capacitor (Max 16V): VGHO ---(+)---- --- (-)----VSSA	1.0 μ F
VGLO	C12	Connect to Capacitor (Max 16V): VGLO ---(-)---- --- (+)----VSSA	1.0 μ F

Table 7.8: External VSP/VSN mode external components

Himax Confidential
Do Not Copy

8. Electrical Characteristics

8.1 Absolute maximum ratings

The absolute maximum ratings are list on Table 8.1. When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power Supply Voltage 1 ^{(1),(2)}	VDD1 ~ VSSD	-0.3	-	+3.6	V
Power Supply Voltage 2 ^{(1),(3)}	VDD3 ~ VSSA	-0.3	-	+5.5	V
Power Supply Voltage 3 ^{(1),(4)}	HS_VCC ~ HS_VSS	-0.3	-	+3.6	V
Power Supply Voltage 4 ⁽⁵⁾	VSP ~ VSSA	-0.3	-	+6.6	V
Power Supply Voltage 5 ⁽⁶⁾	VSSA ~ VSN	0	-	-6.6	V
Power Supply Voltage 6 ⁽⁷⁾	VGH ~ VSSA	0	-	+25	V
Power Supply Voltage 7 ⁽⁸⁾	VSSA ~ VGL	0	-	-16	V
Operating Temperature ⁽⁹⁾	Topr	-40	-	+85	°C
Storage Temperature ⁽¹⁰⁾	Tstg	-55	-	+110	°C

- Note:** (1) VDD1, VSSD must be maintained.
 (2) To make sure $VDD1 \geq VSSD$.
 (3) To make sure $VDD3 \geq VSSA$.
 (4) To make sure $HS_VCC \geq HS_VSS$.
 (5) To make sure $VSP \geq VSSA$.
 (6) To make sure $VSSA \geq VSN$.
 (7) To make sure $VGH \geq VSSA$.
 (8) To make sure $VSSA \geq VGL$
 $VGH + |VGL| < 30V$
 (9) For die and wafer products, specified up to +85°C.
 (10) This temperature specifications apply to the TCP package.

Table 8.1: Absolute maximum rating

8.2 DC characteristics

(VSP=4.8 to 6V, VSN=-4.8 to -6, VDD1=1.65 to 3.3V, TA=-40 to 85 °C)

Parameter	Symbol	Test condition	Spec.			Unit
			Min.	Typ.	Max.	
Input high voltage	V _{IH}	VDD1= 1.65 ~ 3.3V	0.7 VDD1	-	VDD1	V
Input low voltage	V _{IL}		0	-	0.3 VDD1	V
VPP	V _{IH}	VPP	7.25V	7.5V	7.75V	V
	V _{IL}					
Output high voltage (SDO, CAB_C_PWM_OUT)	V _{OH1}	I _{OH} = -1.0 mA	0.8 VDD1	-	VDD1	V
Output low voltage (SDO, CAB_C_PWM_OUT)	V _{OL1}	VDD1= 1.65 ~ 2.4V I _{OL} = 1.0 mA	0	-	0.2 VDD1	V
Logic High level input current	I _{IH}	VSYNC, HSYNC	-	-	1	uA
		RESX, DCX, CSX, SCL	-	-	1	uA
	I _{IHD}	DB[7...0], SDI_SDA, DCX	-	-	1	uA
		DB[7...0]	-	-	1	uA
Logic Low level input current	I _{IL}	VSYNC, HSYNC	-1	-	-	uA
		RESX, DCX, CSX, SCL	-1	-	-	uA
	I _{ILD}	DB[7...0], SDI_SDA, DCX	-1	-	-	uA
		DB[7...0]	-1	-	-	uA
Current consumption (VSP-VSSA)	I _{ST(VSP)}	Sleep in mode VSP=5.5V, VSN=-5.5V, VDD1=HS_VCC=1.8V, T _A =25°C ULPS/ DSTB (DSTB_OPT=1) VSP=5.5V, VSN=-5.5V, VDD1=HS_VCC=1.8V, T _A =25°C	-	-	60	uA
Current consumption (VSN-VSSA)	I _{ST(VSN)}		-	-	35	uA
Current consumption (VDD1- VSSD)	I _{ST(VDD1)}		-	-	300	uA
Current consumption (HS_VCC- HS_VSS)	I _{ST(HS_VCC)}		-	-	90	uA
Current consumption (VSP-VSSA)	I _{ULPS(VSP)}		-	-	20	uA
Current consumption (VSN-VSSA)	I _{ULPS(VSN)}		-	-	35	uA
Current consumption Deep Sleep in mode (VDD1- VSSD)	I _{ULPS(VDD1)}		-	-	230	uA
Current consumption (HS_VCC- HS_VSS)	I _{ULPS(HS_VCC)}		-	-	10	uA
Current consumption (VSP-VSSA)	I _{DST(VSP)}		-	-	5	uA
Current consumption (VSN-VSSA)	I _{DST(VSN)}		-	-	35	uA
Current consumption (VDD1- VSSD)	I _{DST(VDD1)}	-	-	15	uA	
Current consumption (HS_VCC- HS_VSS)	I _{DST(HS_VCC)}	-	-	5	uA	

Note: (1) The VPP pin is open on normal mode and in used while OTP programming condition.

Table 8.2: DC characteristic

8.3 AC characteristics

8.3.1 I2C AC characteristics

Characteristics of SDA and SCL bus lines for I2C-bus devices

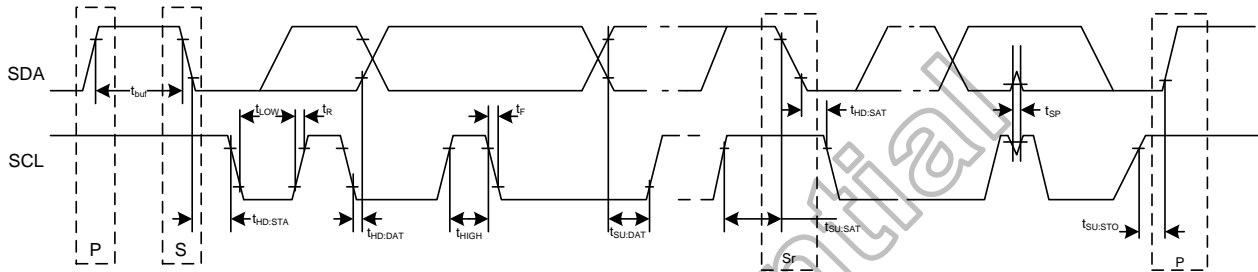


Figure 8.1: I2C timing

Parameter	Symbol	Standard-Mode I2C-BUS		Fast-Mode I2C-BUS		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	KHz
Bus free time between STOP and START condition	t_{BUF}	4.7	-	1.3	-	μs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD:STA}$	4.0	-	0.6	-	μs
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	μs
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7	-	0.6	-	μs
Data hold time	$t_{HD:DAT}$	0	-	0	0.9	μs
Data set-up time	$t_{SU:DAT}$	250	-	100	-	ns
Rise time of both SDA and SCL signals	t_R	-	1000	$20+0.1 C_b$	300	ns
Fall time of both SDA and SCL signals	t_F	-	300	$20+0.1 C_b$	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	-	0.6	-	μs
Capacitive load for each bus line.	C_b	-	400	-	400	pF

Note: (1) All values are referred to VIH (0.7xVCCIO) and VIL (0.3xVCCIO) level.

(2) A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the VIH of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

(3) The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

(4) A fast-mode I2C-bus device can be used in a standard-mode I2C-bus system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{Rmax} + t_{SU:DAT} = 1000+250=1250ns$ (according to the standard-mode I2C-bus specification) before the SCL line is released.

(5) C_b = total capacitance of one bus line in pF.

Table 8.3 I2C timing spec

8.3.2 DBI Type-C interface characteristics

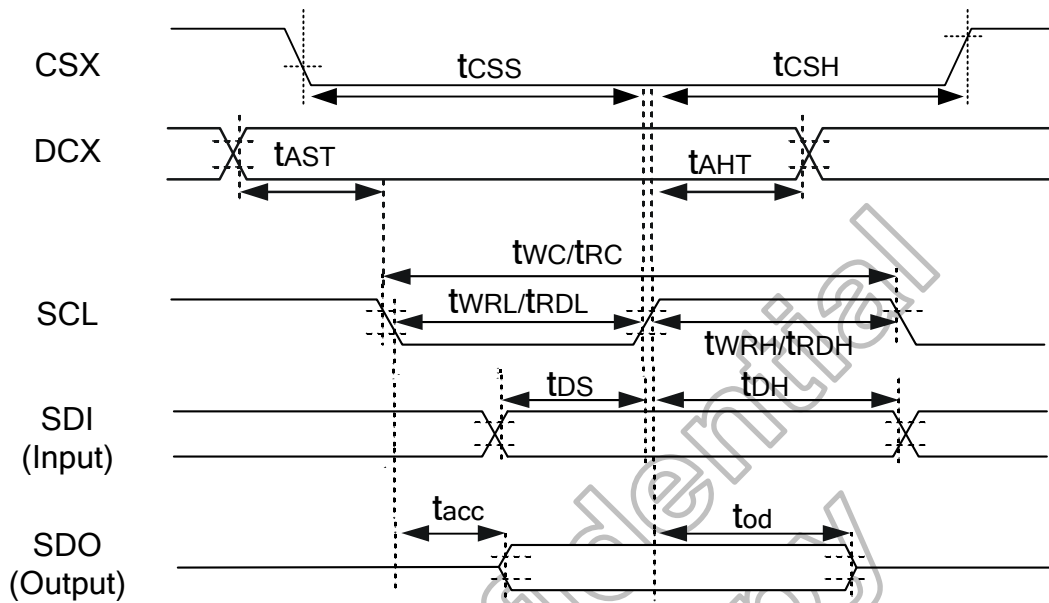


Figure 8.2: DBI Type-C interface characteristics

(VSSA=0V, VDD1=1.8V, VDD3=2.8V, T_A = 25°C)

Parameter	Signal	Symbol	Description	Spec.			Unit
				Min.	Typ.	Max.	
Chip select setup time (Write)	CSX	t_{CSS}	-	40	-	-	ns
Chip select setup time (Read)		t_{CSH}	-	40	-	-	
Address setup time	DCX	t_{AST}	-	10	-	-	ns
Address hold time (Write/Read)		t_{AHT}	-	10	-	-	
Write cycle	SCL (Write)	t_{WC}	-	100	-	-	ns
Control pulse "H" duration		t_{WRH}	-	40	-	-	
Control pulse "L" duration		t_{WRL}	-	40	-	-	
Read cycle	SCL (Read)	t_{RC}	-	150	-	-	ns
Control pulse "H" duration		t_{RDH}	-	60	-	-	
Control pulse "L" duration		t_{RDL}	-	60	-	-	
Data setup time	SDI/SDO (Input)	t_{DS}	For maximum CL=30pF	30	-	-	ns
Data hold time		t_{DT}	For minimum CL=8pF	30	-	-	
Read access time	SDI/SDO (Output)	t_{RACC}	-	10	-	-	ns
Output disable time		t_{OD}	-	10	-	50	

Note: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Table 8.4: DBI Type-C interface characteristics

8.3.3 DSI D-PHY electrical characteristics

8.3.3.1 The Electrical Characteristics of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: High-Speed Receiver (HS-RX), Low Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and the Low-Power Contention Detector (LP-CD). Figure 8.3 shows the complete set of electrical functions required for a fully featured PHY transceiver.

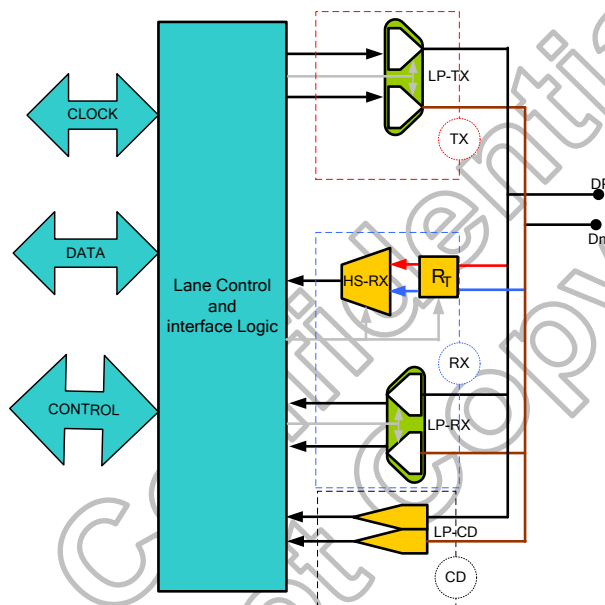


Figure 8.3: Electrical functions of a fully D-PHY transceiver

Where, the HS receiver utilize low-voltage swing differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism. The Figure 8.4 shows both the HS and LP signal levels on the left and right sides, respectively.

Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

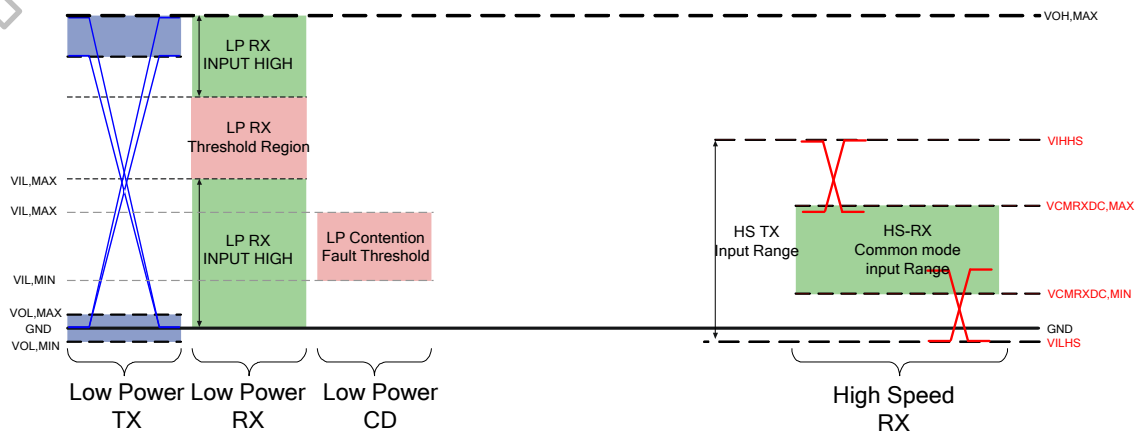


Figure 8.4: Shows both the HS and LP signal levels

8.3.3.2 The Electrical Characteristics of Low-Power Transmitter

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes. It is therefore important that the static power consumption of a LP transmitter be as low as possible. Under tables list DC and AC characteristic for LP-TX

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Thevenin output low level	V_{OL}	-50	-	50	mV
Thevenin output high level	V_{OH}	1.1	1.2	1.3	V
Output impedance of LP-TX ⁽¹⁾	Z_{OLP}	110	-	-	Ω

Note: (1) Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 8.5: LP transmitter DC specifications

Parameter	Symbol	Spec.			Unit	
		Min.	Typ.	Max.		
15%-85% rise time and fall time ⁽¹⁾	t_{RLP}/t_{FLP}	-	-	25	ns	
Slew rate @ CLOAD = 0pF ^{(1),(3),(5),(6)}	$\delta V/\delta t_{SR}$	30	-	500	mV/ns	
Slew rate @ CLOAD = 5pF ^{(1),(3),(5),(6)}		-	-	300	mV/ns	
Slew rate @ CLOAD = 20pF ^{(1),(3),(5),(6)}		-	-	250	mV/ns	
Slew rate @ CLOAD = 70pF ^{(1),(3),(5),(6)}		-	-	150	mV/ns	
Slew rate @ CLOAD = 0 to 70pF ^{(1),(2),(3)} (Falling Edge Only)		30	-	-	mV/ns	
Slew rate @ CLOAD = 0 to 70pF ^{(1),(3),(7)} (Rising Edge Only)		30	-	-	mV/ns	
Slew rate @ CLOAD = 0 to 70pF ^{(1),(8),(9)} (Rising Edge Only)		30 – 0.075 * ($V_{O,INST} - 700$)	-	-	mV/ns	
Load capacitance		C_{LOAD}	-	-	70	pF

Note: (1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

(2) When the output voltage is between 400 mV and 930 mV.

(3) Measured as average across any 50 mV segment of the output signal transition.

(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.

(5) This value represents a corner point in a piecewise linear curve.

(6) When the output voltage is in the range specified by VPIN (**absmax**).

(7) When the output voltage is between 400 mV and 700 mV.

(8) Where VO, INST is the instantaneous output voltage, VDP or VDN, in millivolts.

(9) When the output voltage is between 700mV and 930mV.

Table 8.6: LP transmitter AC specifications

8.3.3.3 The Electrical Characteristics of Receiver

This part will contain two parts which High-Speed Receiver and Low-Power Receiver. Because their have differential DC and AC characteristic, describe HS-RX first then describe LP-RX.

8.3.3.4 High-speed receiver

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, Z_{ID}, between the positive input pin D_p and the negative input pin D_n. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Differential input high threshold ⁽¹⁾	V _{IDTH}	-	-	70	mV
Differential input low threshold ⁽¹⁾	V _{IDTL}	-70	-	-	mV
Single-ended input low voltage ⁽²⁾	V _{ILHS}	-40	-	-	mV
Single-ended input high voltage ⁽²⁾	V _{IHHS}	-	-	460	mV
Common-mode voltage HS receive mode ^{(2) (3)}	V _{CMRXDC}	70	-	330	mV
Differential input impedance	Z _{ID}	80	100	125	Ω

Note: (1) +/-70mV only for reference, related to power and ground noise on system environment, this spec need to check on panel performance to fine tune.

(2) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

(3) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 8.7: HS receiver DC specifications

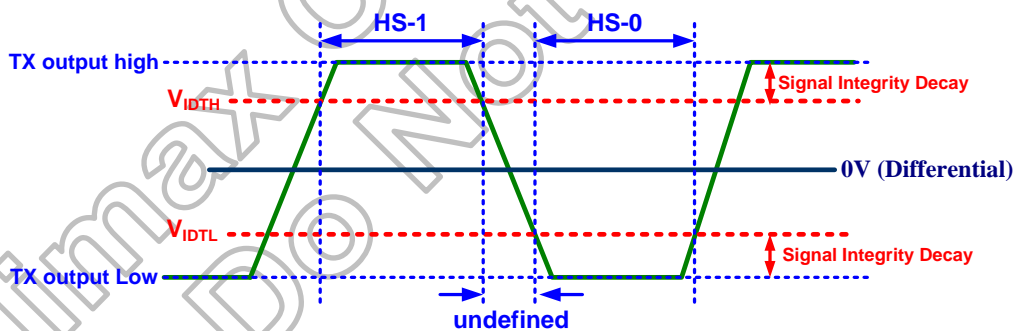


Figure 8.5: Differential HS signals for HS receive

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Common mode interference beyond 450 MHz ⁽¹⁾	ΔV _{CMRX(HF)}	-	-	100	mV _{PP}
Common mode termination ⁽²⁾	C _{CM}	-	-	60	pF

Note: (1) ΔV_{CMRX(HF)} is the peak amplitude of a sine wave superimposed on the receiver inputs.

(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 8.8: HS receiver AC specifications

8.3.3.5 Low-Power Receiver

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The related diagram shows as Figure 8.5 Input Glitch Rejection of Low-Power Receivers. Besides, under tables list DC and AC characteristic for LP-RX.

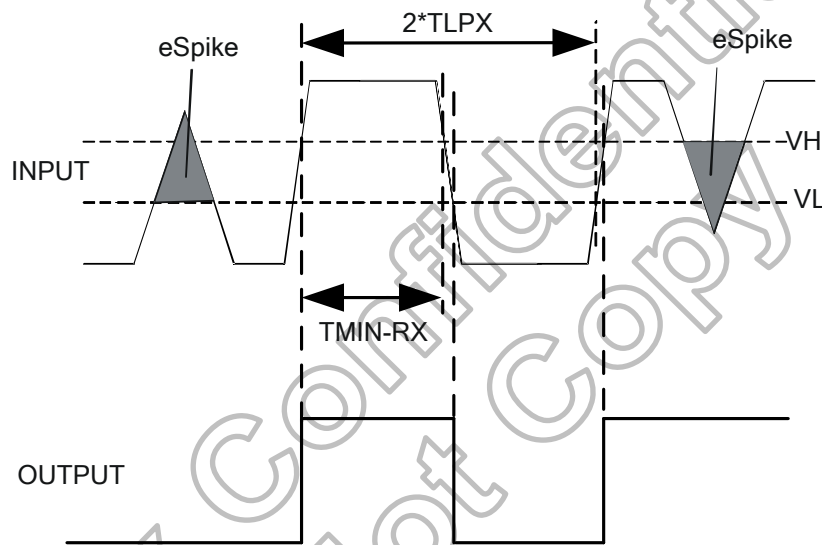


Figure 8.6: Input glitch rejections of low-power receivers

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Logic 0 input threshold	V_{IL}	-	-	550	mV
Logic 1 input threshold	V_{IH}	880	-	-	mV

Table 8.9: LP receiver DC specifications

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Input pulse rejection ^{(1),(2)(3)}	e_{SPIKE}	-	-	300	V.ps
Minimum pulse width response ⁽⁴⁾	T_{MIN}	20	-	-	ns
Peak-to-peak interference voltage	V_{INT}	-	-	200	mV
Interference frequency	f_{INT}	450	-	-	MHz

Note: (1) Time voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state
 (2) An impulse less than this will not change the receiver state.
 (3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
 (4) An input pulse greater than this shall toggle the output.

Table 8.10: LP receiver AC specifications

8.3.3.6 Line Contention Detection

Contention can be inferred from any of the following conditions:

- A. An LP high fault shall be detected when the LP transmitter is driving high and the pin voltage is less than VIL.
- B. An LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than VILF.

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Logic 1 contention threshold	V_{IHCD}	450	-	-	mV
Logic 0 contention threshold	V_{ILCD}	-	-	200	mV

Table 8.11: Contention detector DC specifications

Himax Confidential
Do Not Copy

8.3.3.7 High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (**half-rate**) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CP – CN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 8.6.

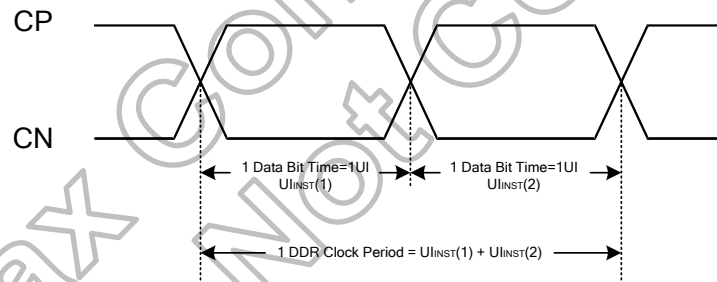


Figure 8.7: DDR clock definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in Table 8.12.

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
UI instantaneous ^{(1),(2)(3)}	UI _{INST}	-	-	12.5	ns

- Note:** (1) This value corresponds to a minimum 80 Mbps data rate.
 (2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
 (3) Maximum total bit rate is 4.6Gbps of 4 data lanes 24-bit data format/ 3.45Gbps of 4 data lane 18-bit data format/ 3.07Gbps of 4 data lane 16-bit data format.

Table 8.12: Reverse HS data transmission timing parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.7. Data is launched in a quadrate relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

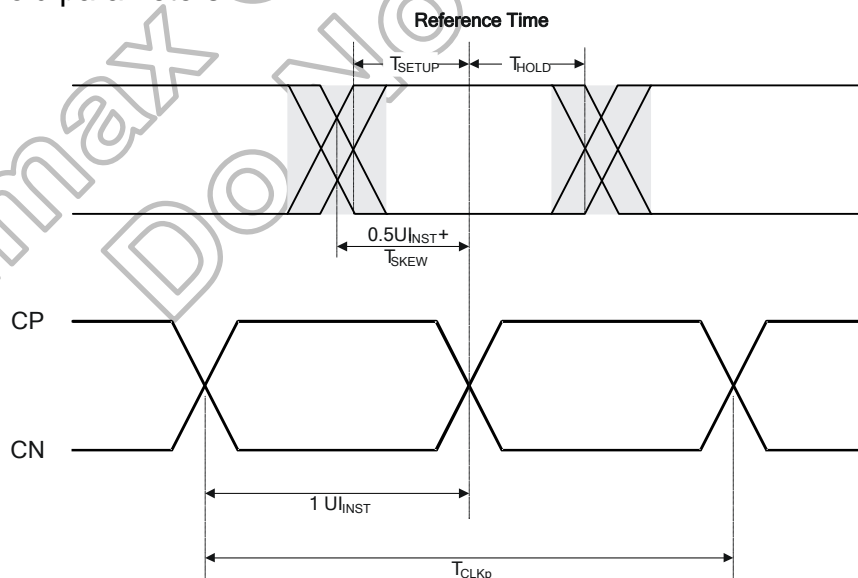


Figure 8.8: Data to clock timing definitions

8.3.3.8 Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 8.13. Implementers shall specify a value $UI_{INST, MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 8.13 are specified as a part of this value. The skew specification, $TSKEW[TX]$, is the allowed deviation of the data launch time to the ideal $\frac{1}{2}UI_{INST}$ displaced quadrature clock edge. The setup and hold times, $T_{SETUP}[RX]$ and $T_{HOLD}[RX]$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP}[RX]$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD}[RX]$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4 * UI_{INST}$, i.e. $\pm 0.2 * UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [Receiver]	$T_{SETUP}[RX]$	0.15	-	-	UI_{INST}	1
Clock to Data Hold Time [Receiver]	$T_{HOLD}[RX]$	0.15	-	-	UI_{INST}	1

Note: (1) Total setup and hold window for receiver of $0.3 * UI_{INST}$.
 (2) $0.15UI$ is only for reference, related to the signal jitter caused by the transmission path, this spec need to check on panel performance to fine tune.

Table 8.13: Data to clock timing specifications

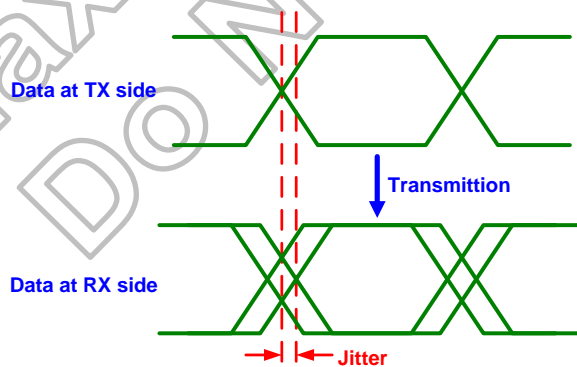


Figure 8.9: Skew window of transmitter and receiver

8.3.4 Timings for DSI video mode

8.3.4.1 Vertical Timings

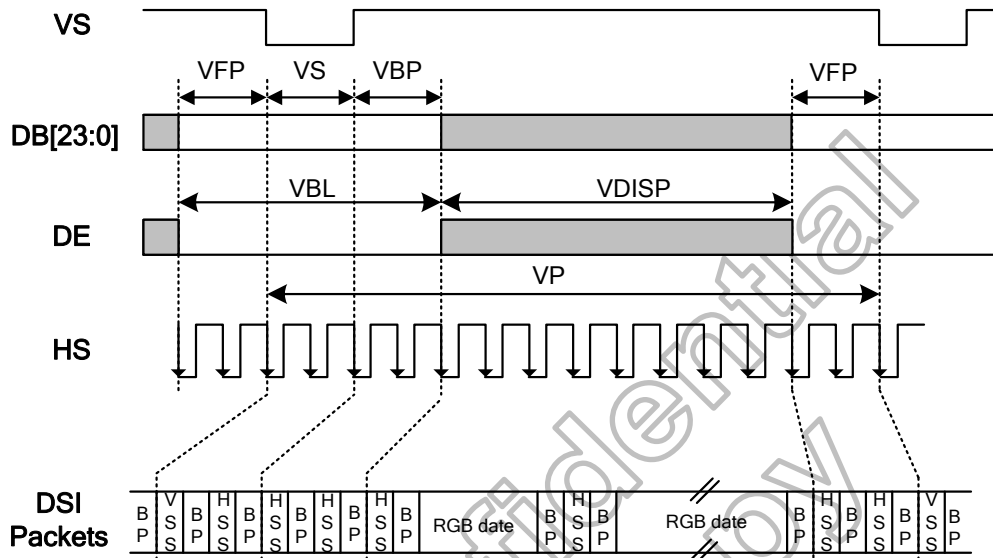


Figure 8.10: Vertical timings for DSI I/F

Vertical Resolution=528+8xNL (VSSA=0V, VDD1=1.8V, VDD3=2.8V, T_A=25°C)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Vertical cycle	VP	-	534+8xNL	-	-	Line
Vertical low pulse width	VS	-	2	-	Note ⁽¹⁾	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note ⁽¹⁾	Line
Vertical data start point	-	VS+VBP	4	-	Note ⁽¹⁾	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	528+8xNL	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GSP and GCK timing. The GSP and GCK must be set at corresponding position for LCD normal display.

Table 8.14: Vertical timings for DSI I/F

8.3.4.2 Horizontal Timings

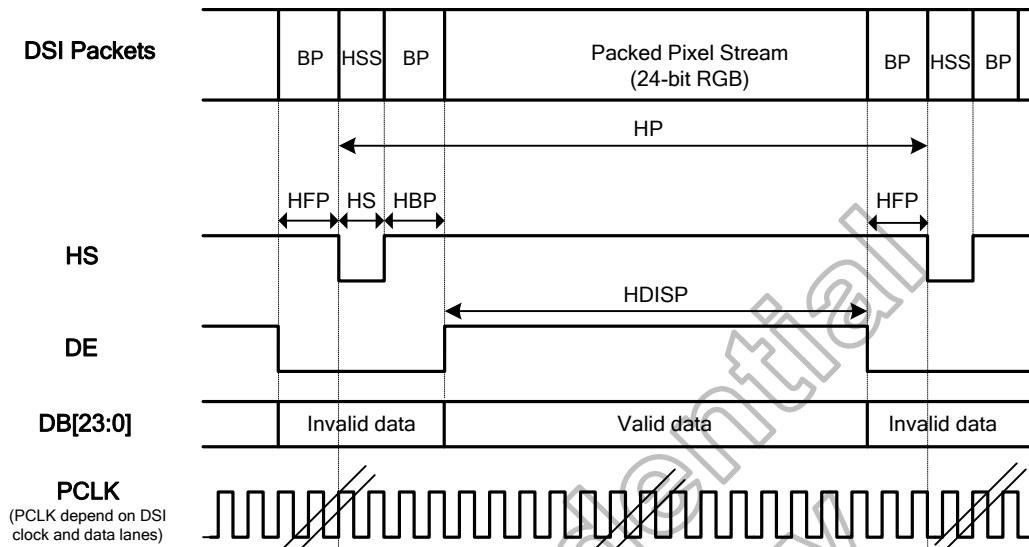


Figure 8.11: Horizontal timing for DSI video mode I/F

VSSA=0V, VDD1=1.8V, VDD3 = HS_VCC =2.8V, T_A=25°C

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
HS cycle	HP	-	1186	-	-	DCK
HS low pulse width	HS	-	16	-	-	DCK
Horizontal back porch	HBP	-	16	-	-	DCK
Horizontal front porch	HFP	-	16	-	-	DCK
Horizontal data start point	-	HS+HBP	90 (Note1)	-	-	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	106	-	-	DCK
Horizontal active area	HDISP	-	-	1080	-	DCK

Note: (1) HS+HBP must larger than 90 PCLK.

Table 8.15: Horizontal timings for DSI video mode I/F

8.3.5 Reset input timing

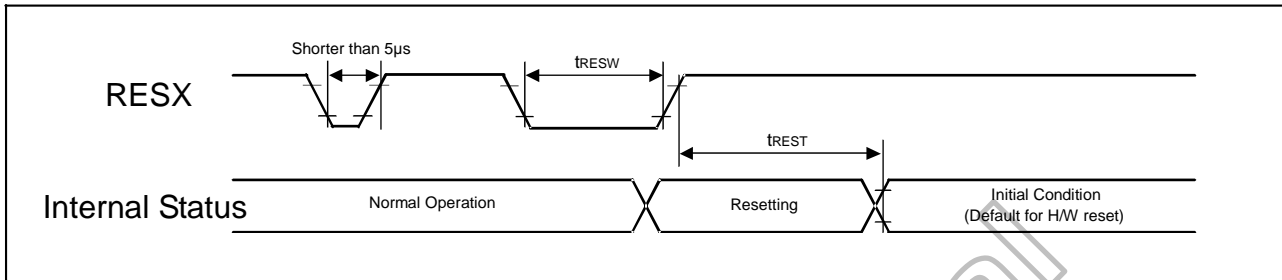


Figure 8.12: Reset input timing

Symbol	Parameter	Related pins	Spec.			Unit	Note
			Min.	Typ.	Max.		
t_{RESW}	Reset low pulse width ⁽¹⁾	RESX	10	-	-	μs	-
t_{REST}	Reset complete time ⁽²⁾	-	-	-	50	ms	-

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(2) During Reset Complete Time, OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (**tREST**) within 5ms after a rising edge of RESX.

(3) Spike Rejection also applies during a valid reset pulse as shown below:

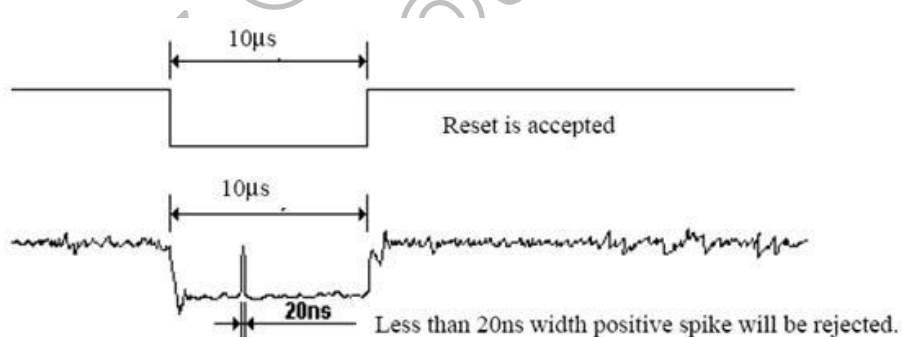


Table 8.16: Reset timing

9. Ordering Information

Part no.	Package
HX8399-C <u>PDxxx-GP</u>	PD: mean COG xxx: mean chip thickness (μm), (default: 250 μm)

Himax Confidential
Do Not Copy